2-Phase Synchronous-Rectified Buck Controller for Mobile GPU Power

General Description

The uP1666Q is a 2/1-phase synchronous-rectified buck controller specifically designed to work with 2.5V ~ 20V input voltage and deliver high quality output voltage for high performance graphic processor power.

The uP1666Q adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP1666Q supports NVIDIA Open Voltage Regulator 2+ with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP1666Q uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance. The uP1666Q also implements a multi-function pin (FS/OC) for switching frequency selection and OCP threshold setting.

Other features include power saving control input, and power good output. This part is available in WQFN3x3-20L package.

Ordering Information

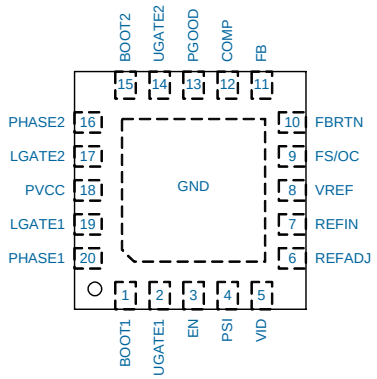
Order Number	Package	Top Marking
uP1666QQKF	WQFN3x3 - 20L	uP1666Q

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Features

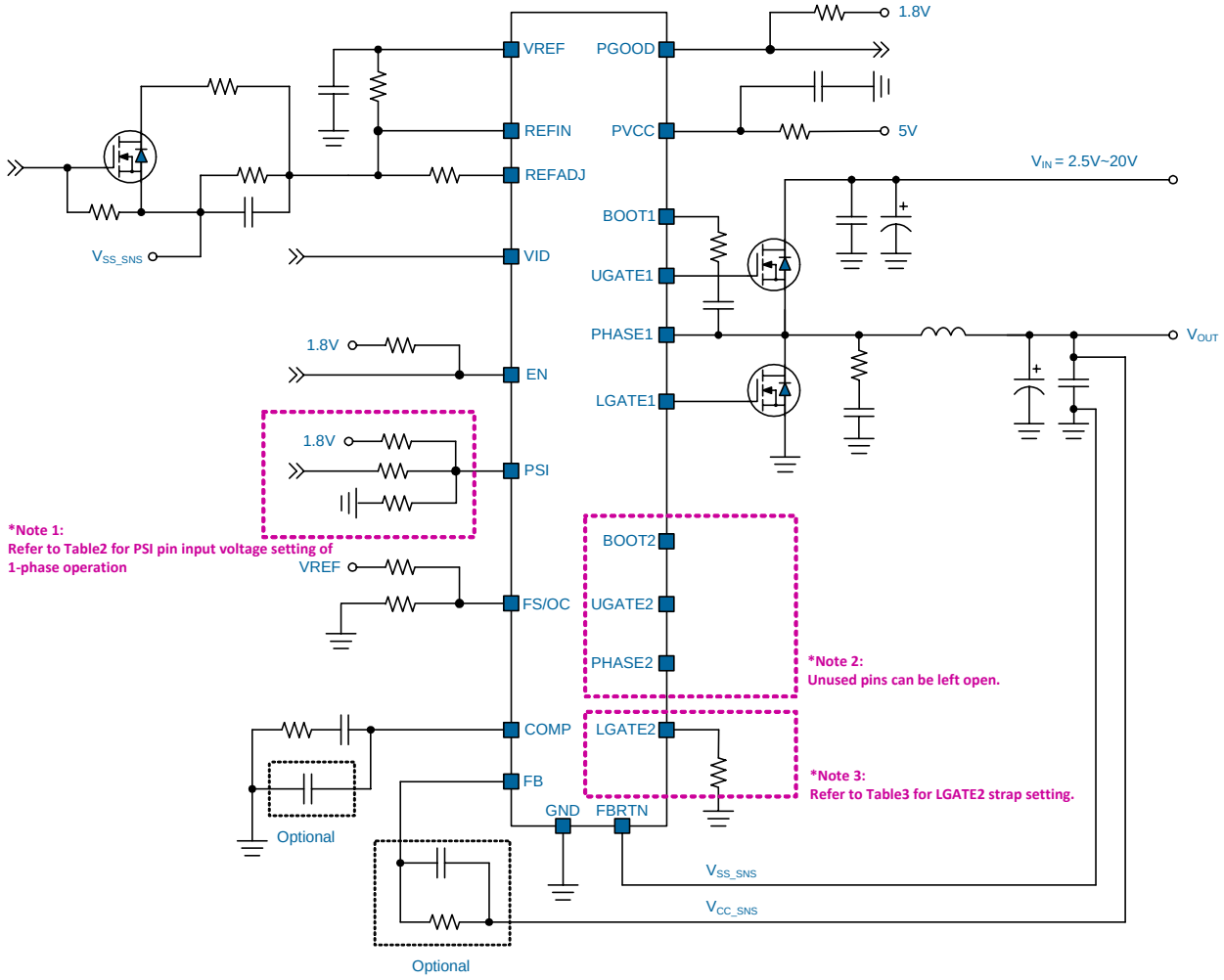
- **Support NVIDIA Open VReg Type-2+ PWMVID Technology**
- **Wide Input Voltage Range 2.5V ~ 20V**
- **Robust Constant On-Time Control**
- **2/1 Phase Operation**
- **Two Integrated MOSFET Drivers with Shoot-Through Protection and Internal Bootstrap Schottky Diode**
- **Selectable Soft-Start**
- **Multi-Function Pin (FS/OC) for Linear OCP Threshold Setting and Switching Frequency Selection**
- **External Compensation**
- **Dynamic Output Voltage Adjustment**
- **Power Good Indication**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

- **Middle-High End GPU Core Power**
- **High End Desktop PC Memory Core Power**
- **Low Output Voltage, High Power Density DC-DC Converters**
- **Voltage Regulator Modules**

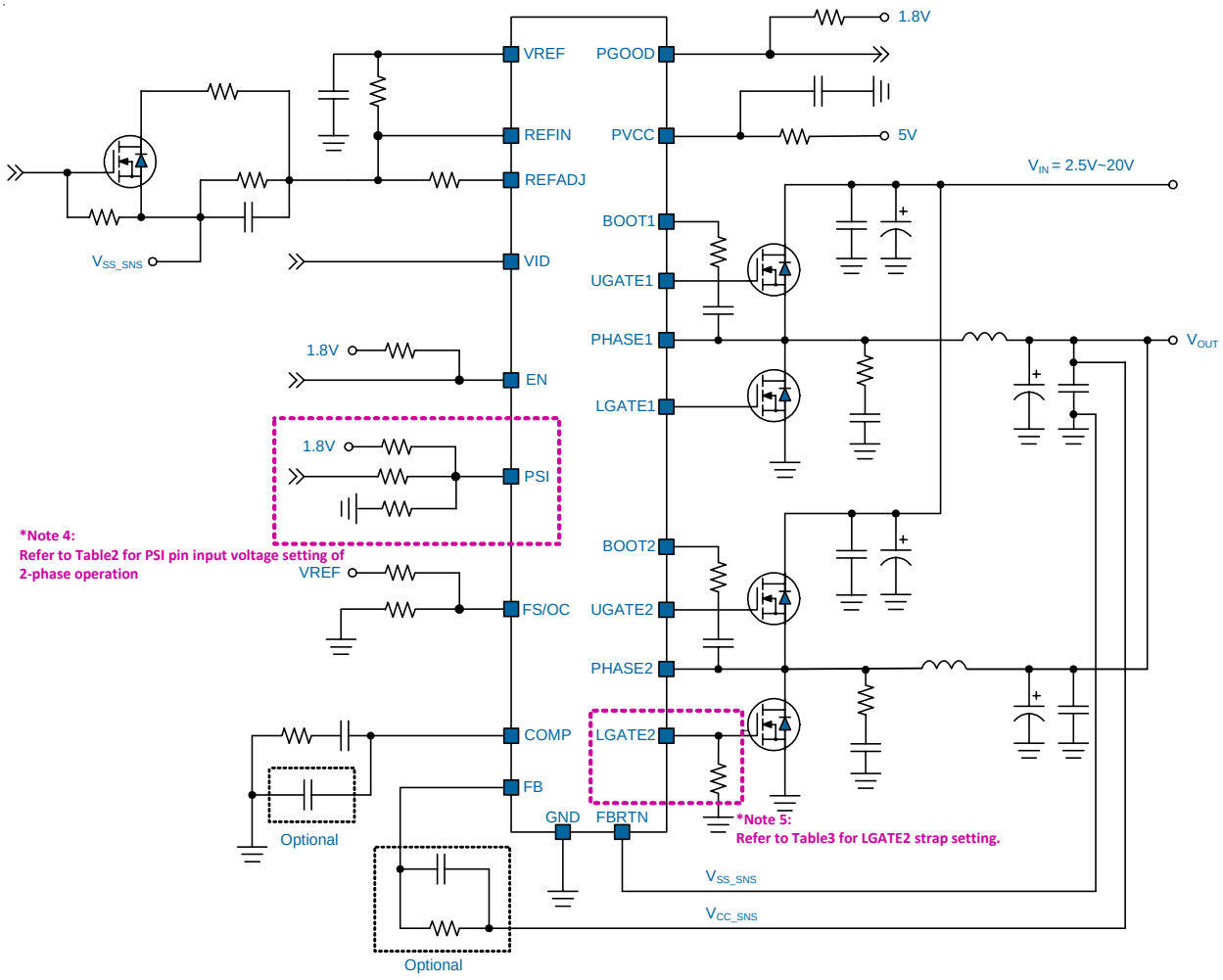
Typical Application Circuit

1-Phase Mode



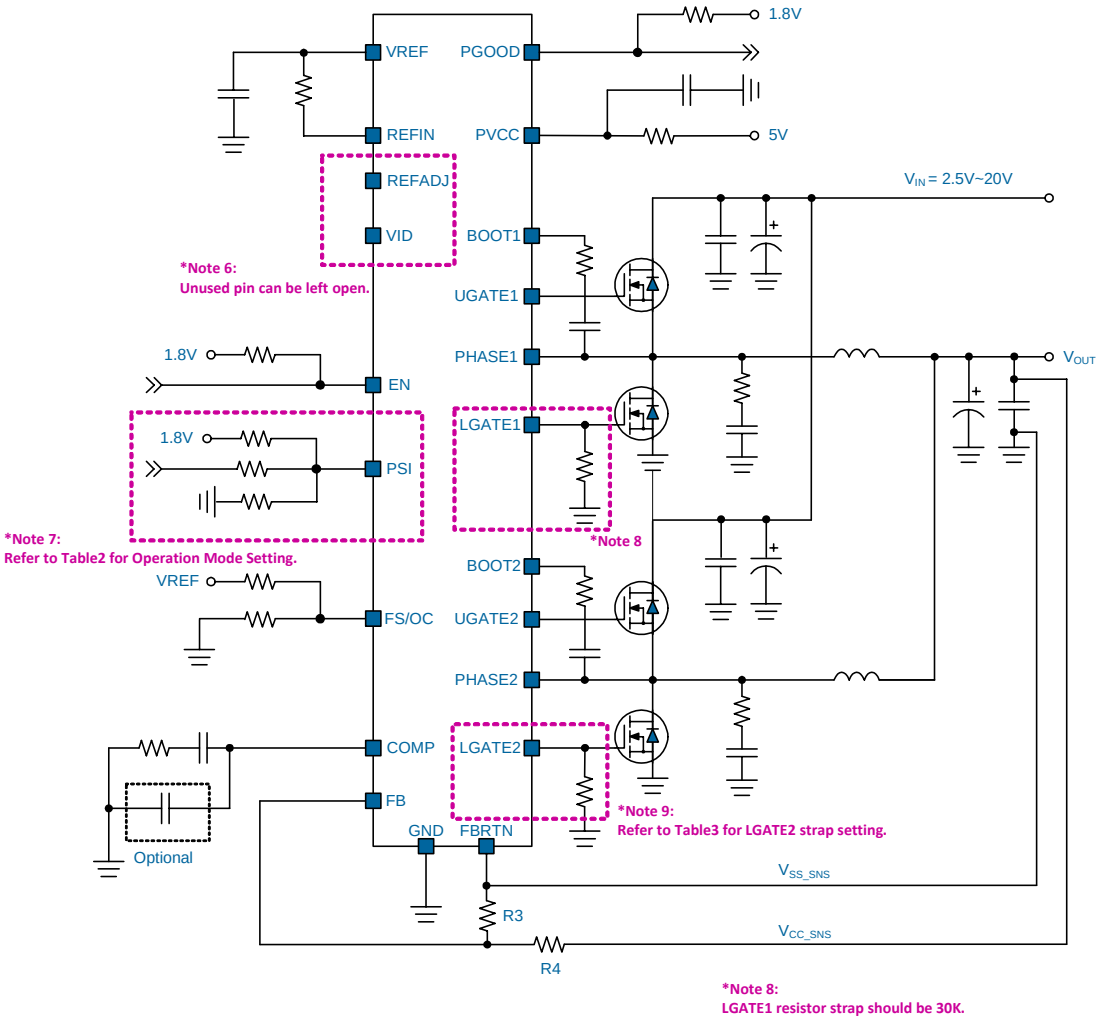
Typical Application Circuit

2-Phase Mode



Typical Application Circuit

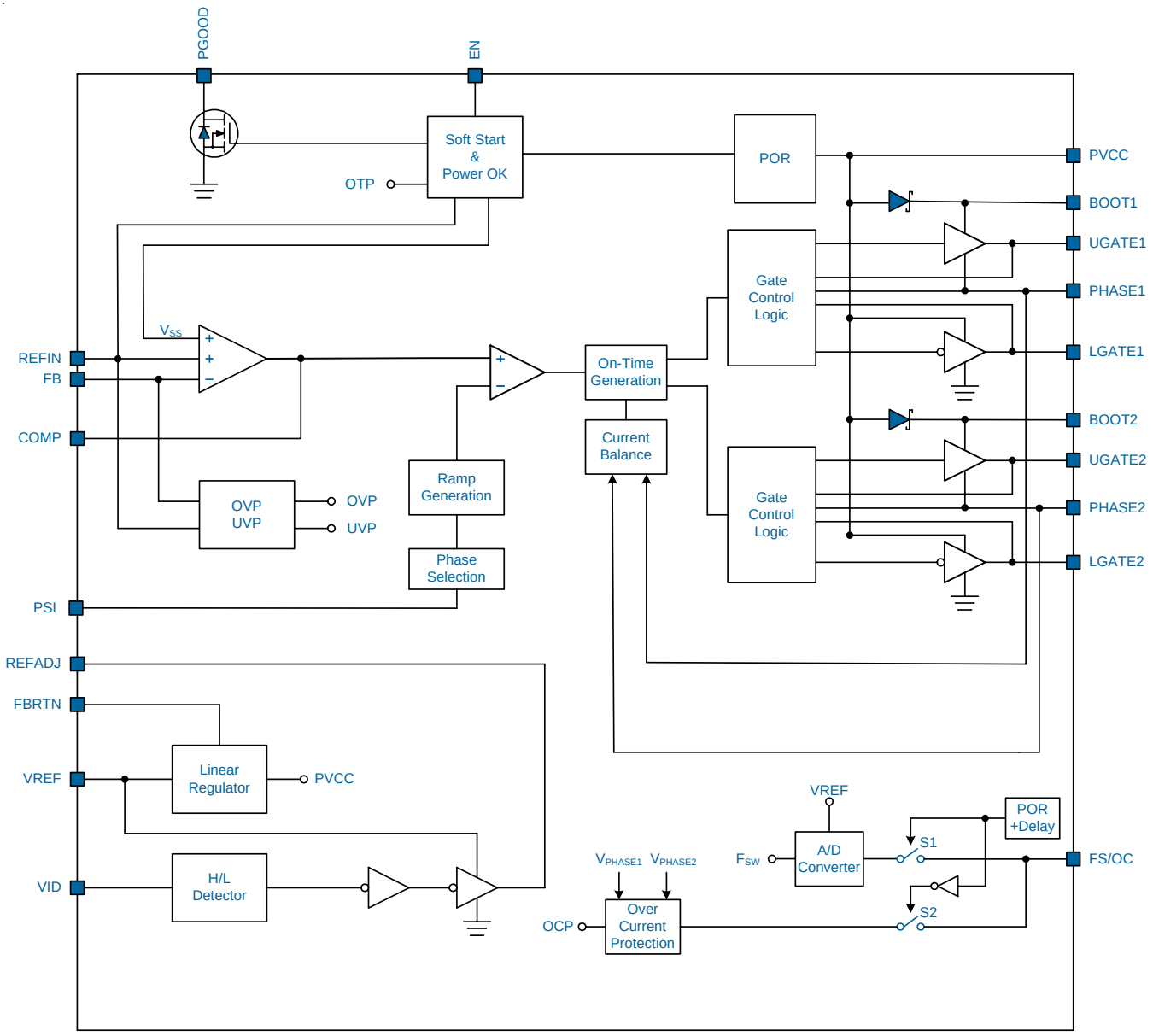
Application for Output Above 2V



Functional Pin Description

Pin No.	Name	Pin Function
1	BOOT1	**BOOT for Phase 1.** Connect a capacitor from this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
2	UGATE1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
3	EN	**Enable.** Chip enable.
4	PSI	**Power Saving Input.** An input pin receives power saving control signal from GPU.
5	VID	**VID.** PWMVID input pin.
6	REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
7	REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit.
8	VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1uF decoupling capacitor between this pin and GND.
9	FS/OC	**Switching Frequency and OCP setting.** Connect a resistive voltage divider from VREF to GND to set OCP threshold and switching frequency.
10	FBRTN	**Return for the Reference Circuit.** Connect this pin to the ground point where output voltage is to be regulated.
11	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
12	COMP	**Compensation Output.** This pin is the output of the error amplifier.
13	PGOOD	**Power Good Indication.** Open-drain structure. Connect this pin to a voltage source with a pull-up resistor.
14	UGATE2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET
15	BOOT2	**BOOT for Phase 2.** Connect a capacitor from this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
16	PHASE2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase 2.
17	LGATE2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET
18	PVCC	**Supply Input for the IC.** Voltage power supply of the IC. Connect this pin to a 5V supply and decouple using at least a 1uF ceramic capacitor.
19	LGATE1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
20	PHASE1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
Exposed Pad		**Ground.** Tie this pin to ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Supply Input and Power On Reset

The uP1666Q receives supply input from PVCC and EN pin to provide current to gate drivers and internal control circuit. The uP1666Q continuously monitors PVCC and EN voltages to ensure all power voltages are ready for normal operation. The PVCC POR level is typically 4.1V. The EN high level is typically 1V.

The uP1666Q integrates floating MOSFET gate driver that are powered from the PVCC pin. A bootstrap schottky diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications. An external Schottky diode with lower voltage drop can improve the power conversion efficiency.

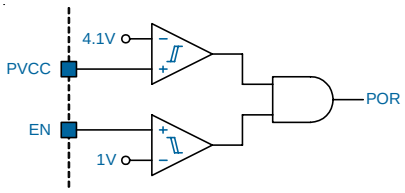


Figure 1. Circuit of Power Ready Detection

Voltage Control Loop and PWMVID Function

Figure 2 illustrates the voltage control loop of the uP1666Q. FB and REFIN are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} of buck converter to force FB voltage V_{FB} follows V_{REFIN}.

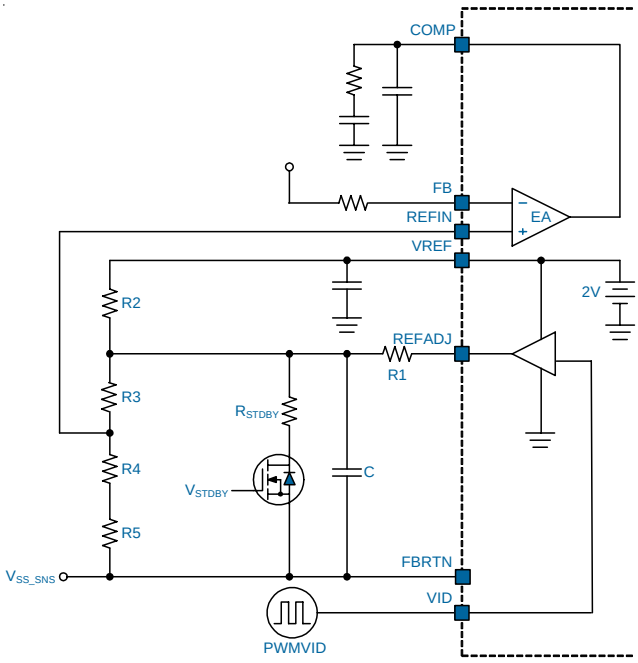


Figure 2. Voltage Control Loop

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2 // (R3+R4+R5)}{R1+R2 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1 // (R3+R4+R5)}{R2+R1 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where V_{REFIN} is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input. The VREF pin is an internal LDO, therefore an output decoupling capacitor is required. Recommend connecting at least a 1uF capacitor from VREF pin to local GND.

Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 3 to generate the standby mode voltage:

$$V_{REFIN,STDBY} =$$

$$V_{VREF} \times \frac{(R3+R4+R5) // R_{STDBY}}{R2+(R3+R4+R5) // R_{STDBY}} \times \frac{R4+R5}{R3+R4+R5}$$

Functional Description

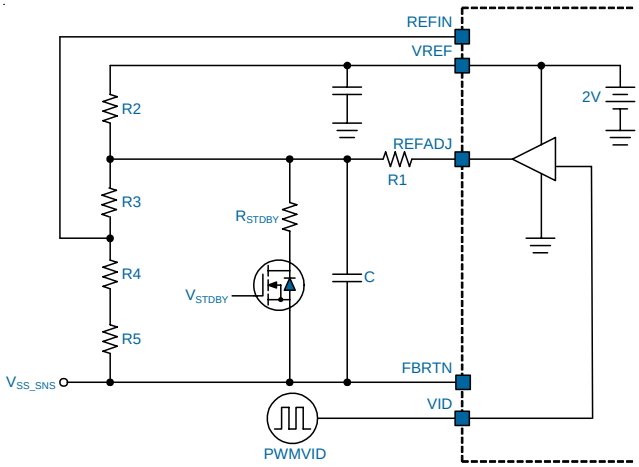


Figure 3. Standby Mode Configuration

Operation Frequency Selection and OCP Setting

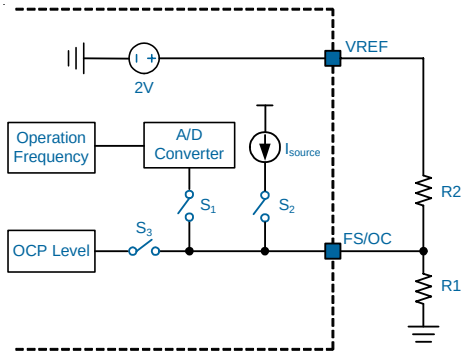


Figure 4. FS/OC pin for Operation Frequency Selection and OCP Threshold Setting

Figure 4 shows the multi-function FS/OC pin for operation frequency selection and OCP threshold setting. After PVCC POR, S1, and S2 switches turn on. Internal current source I_{SOURCE} flows out to FS/OC pin to generate a voltage V_{FS1}. Then, S2 switch turns off, the FS/OC pin voltage V_{FS2} is determined by the external voltage divider. Controller samples/holds the V_{FS1} and V_{FS2} to calculate the ΔV_{FS} and determine the controller operation frequency according to the following table.

Table 1. Controller Operation Frequency Table

Level	ΔV_{FS}	F_{SW}
1	60mV	200kHz
2	120mV	300kHz
3	180mV	400kHz
4	240mV	500kHz
5	300mV	600kHz
6	360mV	800kHz

After the operation frequency is determined, the uP1666Q turns off S1 and S2 switches and turns on S3 switch for OCP setting. When S3 is turned on, the FS/OC pin voltage is determined by the external voltage divider, and the FS/OC pin voltage is connect to the internal OCP circuit for OCP level V_{OC} setting.

V_{OC} is the per-phase GND-PHASE voltage when the power stage low-side MOSFETs are turned on. When per-phase $I_{SD,LMOS}$*$R_{DS(ON),LMOS}$ exceeds V_{OC}, uP1666Q will limit the phase current. Since the OC mechanism detects per-phase current for inductor valley current limiting, the per-phase limited current can be calculated as:

$$I_{MAX,per-phase} = \frac{V_{OC}}{R_{DS(ON)}} + \frac{1}{2}\Delta I_{L(pk-pk)}$$

And the total limited current can be calculated as:

$$I_{MAX,total} = N \times \left[\frac{V_{OC}}{R_{DS(ON)}} + \frac{1}{2}\Delta I_{L(pk-pk)} \right]$$

Where N is the operating phase number, $R_{DS(ON)}$ is the on-resistance of equivalent per-phase power stage low side MOSFET. If any phase current exceeds $I_{MAX,per-phase}$, the current limit protection is triggered, that phase current will be limited.

uP1666Q's operation frequency and OC level setting is related to resistance of R1 and R2. Therefore, the proper resistance of R1 and R2 is needed. The following is the equation to calculate the value of R1 and R2.

$$R1 = \frac{V_{FS}}{4uA} \times \frac{2V}{0.6V + 2 \times V_{OC}}$$

$$R2 = \left[\frac{2V}{1.4V - 2 \times V_{OC}} - 1 \right] \times R1$$

Functional Description

Where V_{FS} is the recommended ΔV_{FS} for operating frequency select and the V_{OC} is the OC level for each phase.
Take 300kHz(V_{FS}=120mV) operation frequency and 100mV per-phase OC level as an example. The resistance of R1 and R2 should be:

$$R1 = \frac{120mV}{4uA} \times \frac{2V}{0.6V + 2 \times 100mV} = 75k\Omega$$

$$R2 = \left[\frac{2V}{1.4V - 2 \times 100mV} - 1 \right] \times 75k\Omega = 50k\Omega$$

Operation Mode

The uP1666Q provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: Full-phase CCM, Full-phase DCM, Single-phase CCM, and Single-phase DCM. The uP1666Q switches between these four operation modes according to the input voltage level of the PSI pin. Table 2 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP1666Q auto-selects phase 1 to be the operating phase. DCM operation mode is activated by two conditions:

1. PSI Voltage stays at “Single-Phase” DCM or “Multi-Phase DCM” operation modes.
2. After PGOOD goes high, VID pin recieves a high or low input signal.

Once the DCM mode is activated, the uP1666Q automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode.
uP1666Q’s power saving feature is a non-latch-off function, the operation mode can be changed anytime after controller POR.

Table 2. Recommended V_{PSI} Setting in Four Operation Modes

Operation Mode	Recommended V_{PSI}
Full-Phase CCM	1.8V
Full-Phase DCM	1.2V
Single-Phase CCM	0.6V
Single-Phase DCM	GND

Application of Output Voltage Above 2V

The uP1666Q supports the application of output voltage above 2V through a voltage divider at FB pin. To support this application, connect a 30kΩ resistor between LGATE1 and GND. To ensure LGATE1 functional setting to work normally, the total capacitance from LGATE1 to GND must **NOT** exceed 12nF (including C_{ISS} capacitance of Low Side MOSFET). It is recommended to set $V_{REFIN} = V_{REF}$ or provide a fixed reference voltage for V_{REFIN}. The output voltage can be programmed as:

$V_{OUT} = V_{REFIN}$ x (1 + R4/R3)

Where R1 and R2 are the resistors of the voltage divider on FB pin. The typical application circuit of output above 2V is shown in the section of *Typical Application Circuit*.

Over Voltage Protection (OVP)

The OVP is triggered if $V_{FB} > 1.5xV_{REFIN}$ sustained 10us. When OVP is activated, the uP1666 turns on all low-side MOSFET and turns off all high-side MOSFET. The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if $V_{FB} < 0.5xV_{REFIN}$ sustained 10us. When UVP is activated, the uP1666Q turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP1666Q monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP1666Q is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Output Ramp Up Time (T_ramp)

The uP1666Q provides 150us, 450us, 900us, and 1.5 ms output ramp up time selection. The output ramp up time is selected through an external resistor connected between LGATE2 to GND. To ensure LGATE2 functional setting to work normally, the total capacitance from LGATE2 to GND must **NOT** exceed 12nF (including C_{ISS} capacitance of Low Side MOSFET). The output ramp up time is determined and latched off before output soft-start cycle initiates. The following table shows the four output ramp up time and its recommended R_{LG2}.

Table 3. Recommended R_{LG2} Setting in Output Ramp Up Time

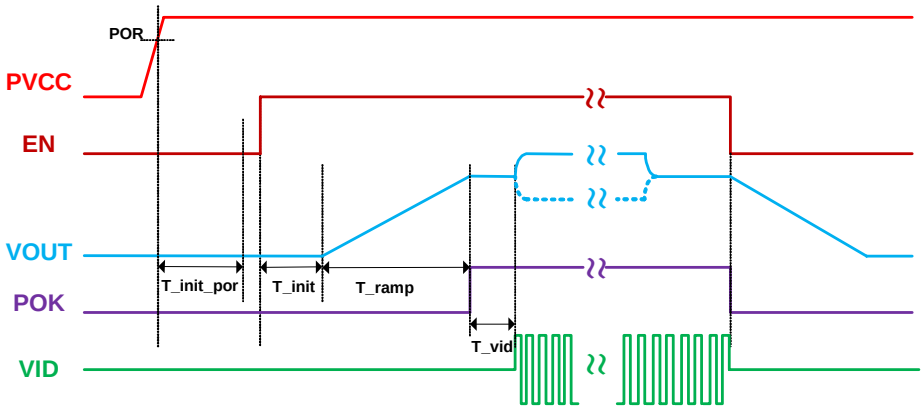
Output Ramp Up Time (T_ramp)	Recommended R_{LG2}
150us	30kΩ
450us	62kΩ
900us	120kΩ
1500us	Open

Power Up Sequence

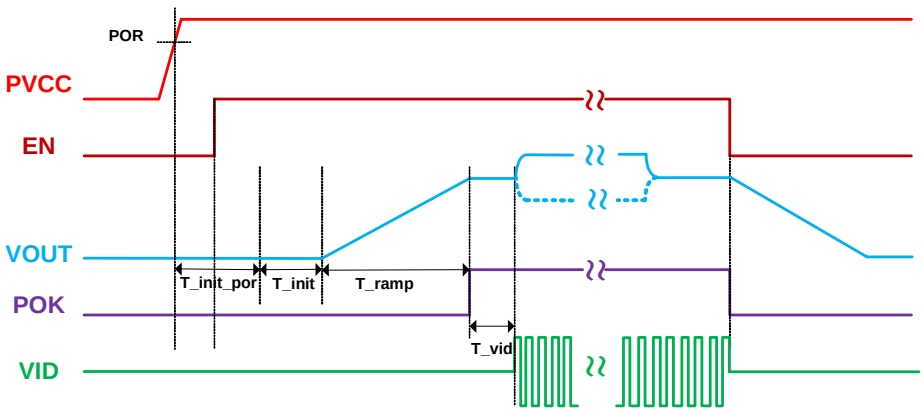
A built-in soft-start function is used to prevent surge current from power supply input during power on. Controller starts the soft-start process right on EN (soft-start I). If EN asserts in the middle of POR initialization, soft-start process is waiting for PVCC_POR initialization to complete (soft-start II). The error amplifier is a three-input device. Reference voltage (V_{REFIN}) or the internal soft-start voltage (V_{SS}) whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. Internal soft-start voltage(V_{SS}) starts to ramp up linearly with a slew rate determined by R_{LG2} resistor after the soft-start cycle is initiated. The output voltage will follow the internal soft-start voltage(V_{SS}) and ramp up linearly. If there is no fault detected at the end of the soft-start, the controller then asserts PGOOD when the output voltage reaches its target level. The PWMVID signal is ignored before PGOOD goes high and the output voltage might not follow V_{REFIN} (which is generated by PWMVID network) during T_vid time. Hence, it is recommended to let PWMVID be toggled after T_vid time. The T_vid time can be calculated as :

$$T\_vid = (V_{REFIN,MAX} - V_{REFIN,BOOT}) \times \left(\frac{T\_ramp}{V_{REFIN,BOOT}} \right)$$

where, $V_{REFIN,MAX}$ is the maximum voltage when PWMVID duty cycle=100%. $V_{REFIN,BOOT}$ is the boot voltage generated by PWMVID network. Tramp is the output voltage ramp up time determined by R_{LG2} resistor. The following graphs show the power up sequence of uP1666Q.



Soft Start I



Soft Start II

Figure 5. Soft-Start Sequence

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC ---------- -0.3V to +6.5V

BOOTx to PHASEx

- DC ---------- -0.3V to +6V
- < 100ns ---------- -5V to +8V

PHASEx to GND

- DC ---------- -0.7V to +28V
- < 100ns ---------- -8V to +36V

BOOTx to GND

- DC ---------- -0.3V to +34V
- < 100ns ---------- -5V to +42V

UGATEx to PHASEx

- DC ---------- -0.3V to +6V
- < 100ns ---------- -5V to +7V

LGATEx to GND

- DC ---------- -0.3V to +6V
- < 100ns ---------- -5V to +7V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

- WQFN3x3 - 20L θ_{JA} ---------- 68°C/W
- WQFN3x3 - 20L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C

- WQFN3x3 - 20L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Input Voltage, V_{IN} ---------- 2.5V to 20V

Control Voltage, V_{PVCC} ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(PVCC = 5V, T_A = 25°C, unless otherwise specified)

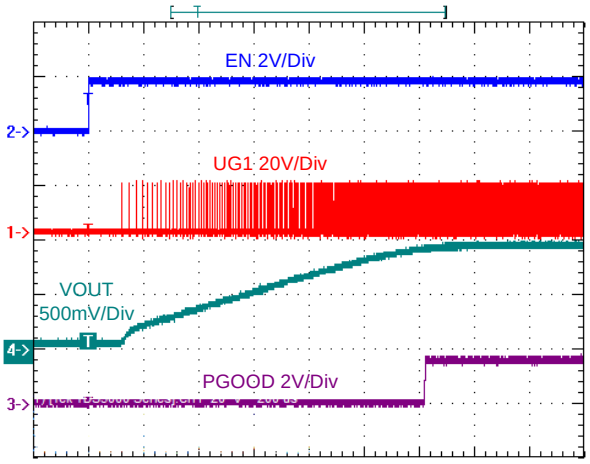
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Quiescent Current	I_Q	EN = 1.8V, 1-phase DCM, No switching	--	800	--	uA
Shutdown Current	I_{SHDN}	EN = 0V	--	2	--	uA
PVCC POR Threshold	$V_{PVCCRTH}$	V_{PVCC} Rising.	3.9	4.1	4.3	V
PVCC POR Hysteresis	$V_{PVCCHYS}$		--	0.3	--	V
VREF Voltage Accuracy	V_{REF}		1.98	2	2.02	V
VREF Sourcing Current	I_{REF}		10	--	--	mA
Control Input: EN						
Logic Low Threshold	V_{EN_L}		--	--	0.4	V
Logic High Threshold	V_{EN_H}		1.2	--	--	V
Internal Pull-down Resistance	R_{EN}		--	200	--	kΩ
On Time						
One Shot Width	T_{ON}	V_{IN} = 12V, V_{OUT} = 0.9V, F_{SW} = 300kHz	--	250	--	ns
Minimum On Time	T_{ON_MIN}		--	80	--	ns
Minimum Off Time	T_{OFF_MIN}		--	300	--	ns
Error Amplifier						
Open Loop DC Gain	A_O	Guaranteed by Design	70	80	--	dB
Trans-conductance	GM		--	800	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}		--	80	--	uA
FBRTN						
FBRTN Current	I_{FBRTN}	EN > 1.4V, no switching	--	--	500	uA
Soft Start						
Initialization Time at POR	$T_{\_INIT\_POR}$	Refer to Figure 5	--	--	350	us
Initialization Time	$T_{\_INIT}$	Refer to Figure 5	--	--	250	us
Selectable Soft Start Time	T_{SS}	EN to PGOOD	250	--	2000	us
PSI						
Power Saving Mode Logic	V_{PSI}	2-phase CCM	1.6	--	--	V
		2-phase DCM	1	--	1.4	
		1-phase CCM	0.4	--	0.8	
		1-phase DCM	--	--	0.2	

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWMVID Buffer						
VID Input Low Level	V_{IL_VID}		--	--	0.6	V
VID Input High Level	V_{IH_VID}		1.2	--	--	V
VID Tri-state Delay	T_{TRI_VID}		--	100	--	ns
REFADJ Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA	--	20	--	Ω
REFADJ Sink Resistance	R_{BF_SNK}	I_{SNK} = 1mA	--	20	--	Ω
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	1	2	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	0.5	1	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	1	2	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.4	0.8	Ω
Dead Time	T_{DT}		--	10	--	ns
Internal Bootstrap Schottky Diode						
Forward Voltage	V_F	Forward Bias Current = 3.5mA	--	0.33	--	V
Zero Current Detection Threshold						
Zero Current Threshold	V_{ZC}	GND-PHASE	--	0.5	--	mV
Protection						
OCP Threshold	V_{OC}	GND-PHASE	40	--	400	mV
OVP Threshold	V_{OVP}	V_{FB}/V_{REFIN}	--	150	--	%
OVP Delay			--	10	--	us
UVP Threshold	V_{UVP}	V_{FB}/V_{REFIN}	40	--	50	%
UVP Delay			--	10	--	us
OTP Threshold			--	150	--	°C
Power Good Indicator						
Power Good Indicator	V_{PG}	I_{SINK} = 4mA	--	--	0.3	V
Power Good Leakage Current	I_{PG_Leak}	V_{PG} = 5V	--	--	0.2	uA

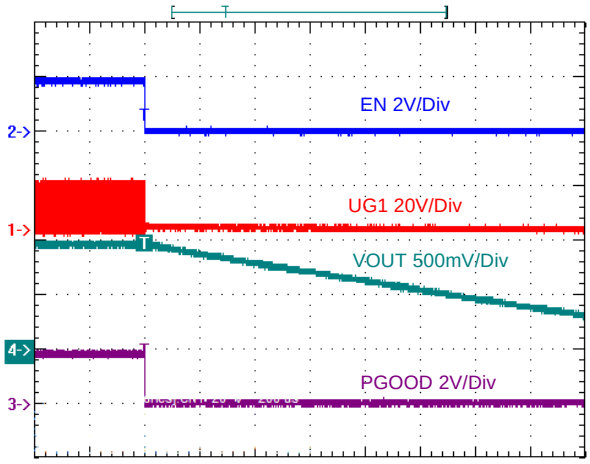
Typical Operation Characteristics

Power On from EN



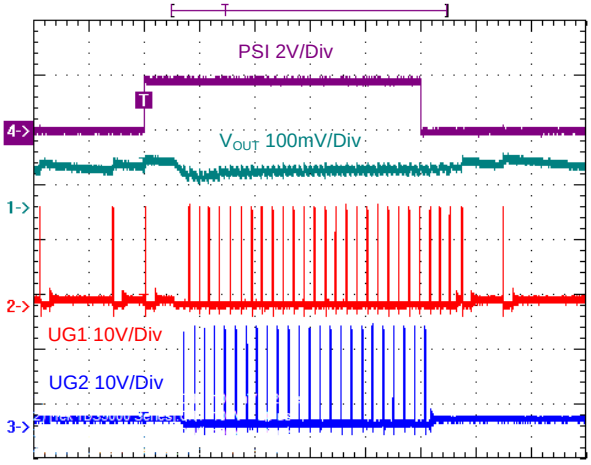
Time：200us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1A, R_{LG2} = OPEN

Power Off from EN



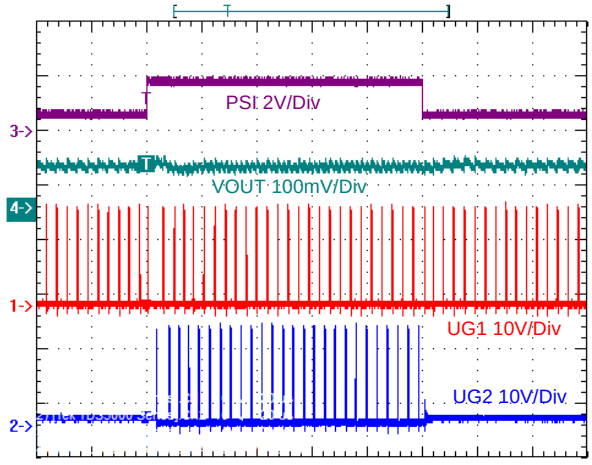
Time：200us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1A, R_{LG2} = OPEN

1 Phase DCM to 2 Phase CCM



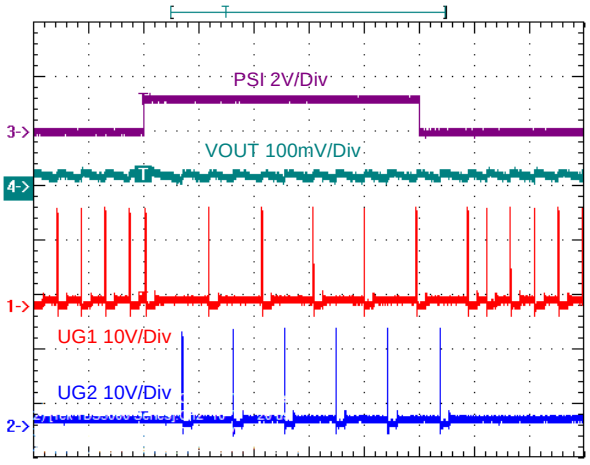
Time：20us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1A

1 Phase CCM to 2 Phase CCM



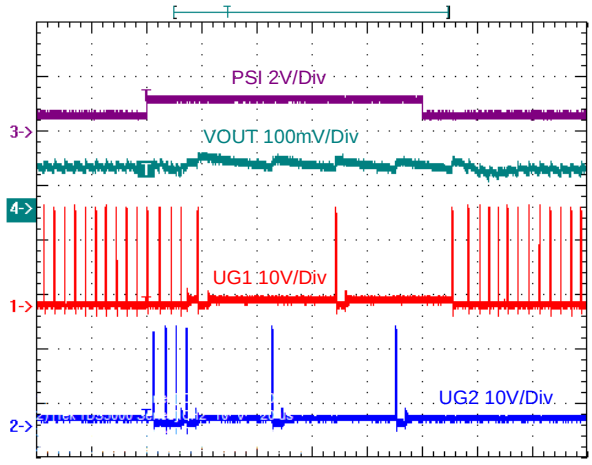
Time：20us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1A

1 Phase DCM to 2 Phase DCM



Time：20us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 2A

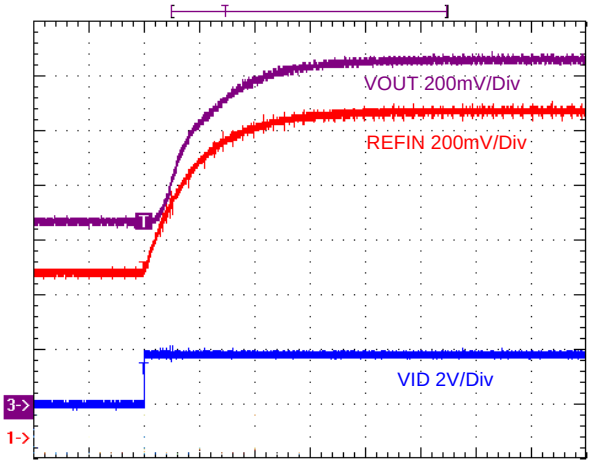
1 Phase CCM to 2 Phase DCM



Time：20us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1A

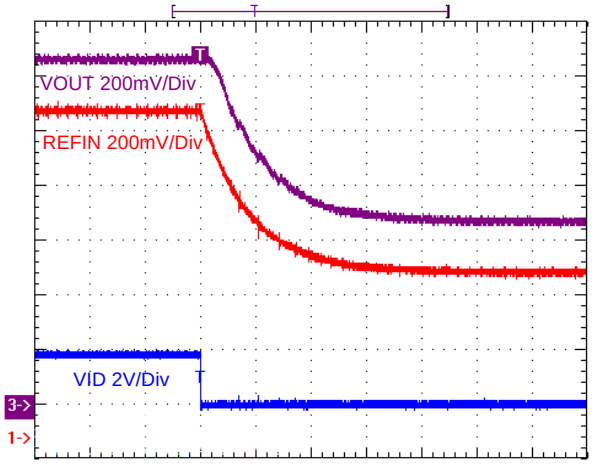
Typical Operation Characteristics

PWMVID Duty Cycle 0% to 100%



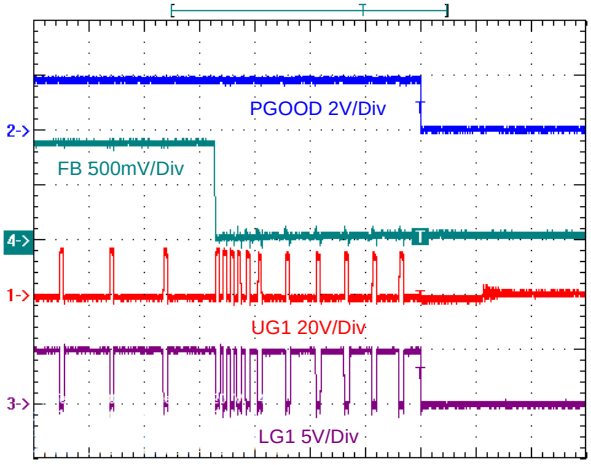
Time：20us/Div
V_{IN} = 12V, I_{OUT} = 1A

PWMVID Duty Cycle 100% to 0%



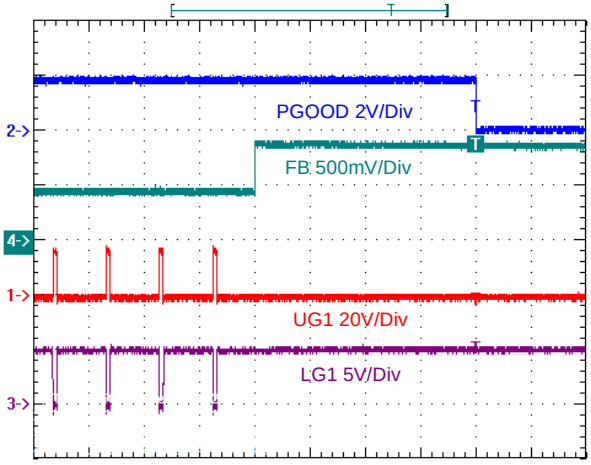
Time：20us/Div
V_{IN} = 12V, I_{OUT} = 1A

Under Voltage Protection



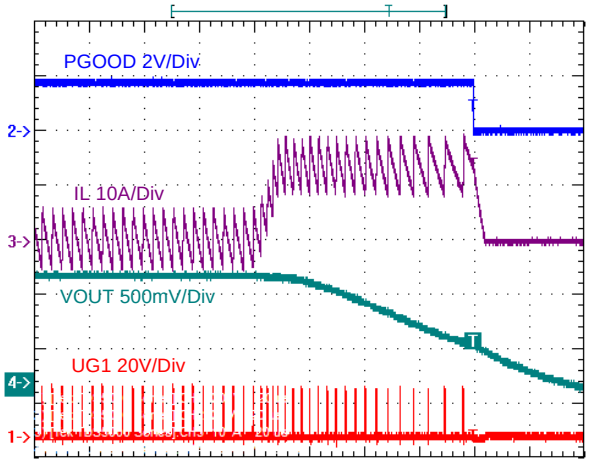
Time：4us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0A

Over Voltage Protection



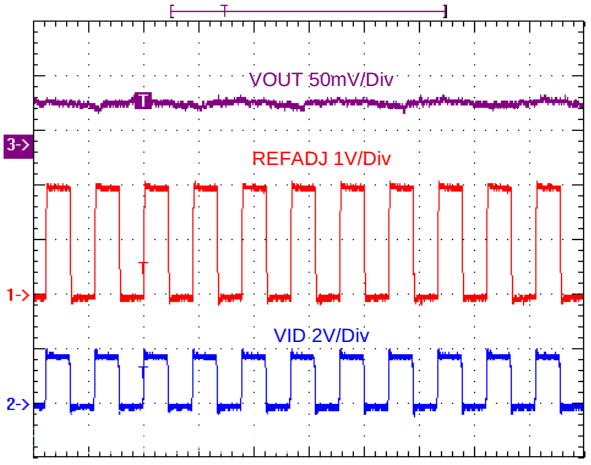
Time：4us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0A

Over Current Protection



Time：20us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, F_{SW} = 300kHz, ΔV_{FS} = 40mV,
Low Side MOSFET = QM3056 ($R_{DS(on)}$ = 4.2mΩ),
R1 = 91kΩ, R2 = 47kΩ

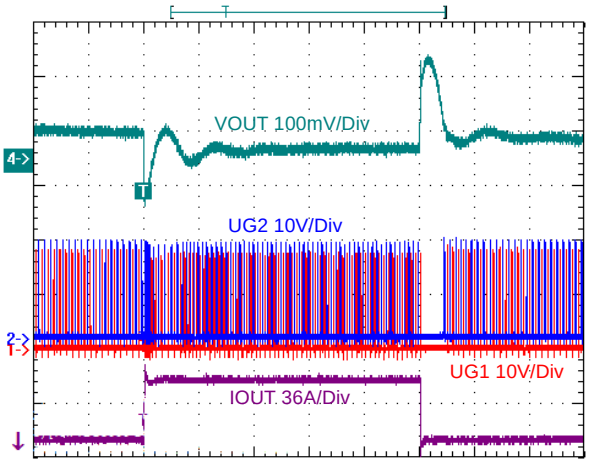
PWMVID: 50%



Time：1us/Div
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0A

Typical Operation Characteristics

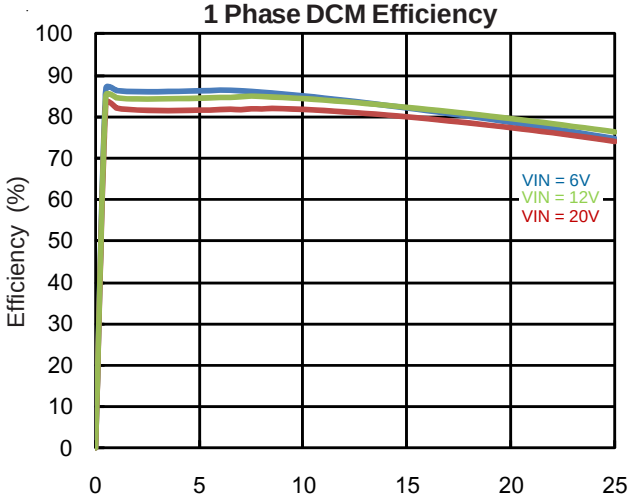
Load Transient



Time : 20us/Div

V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1-50A, F_{SW} = 300kHz,
2 Phase CCM, L = 0.22uH, C = 2848uF

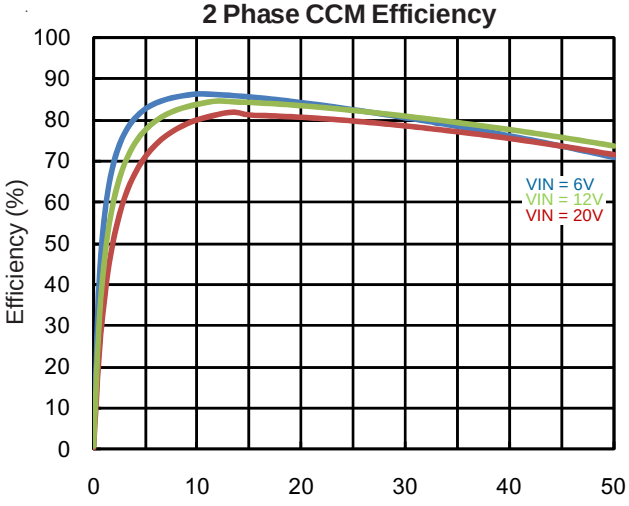
1 Phase DCM Efficiency



Load (A)

V_{CC} = 5V, 1 Phase DCM Operation

2 Phase CCM Efficiency

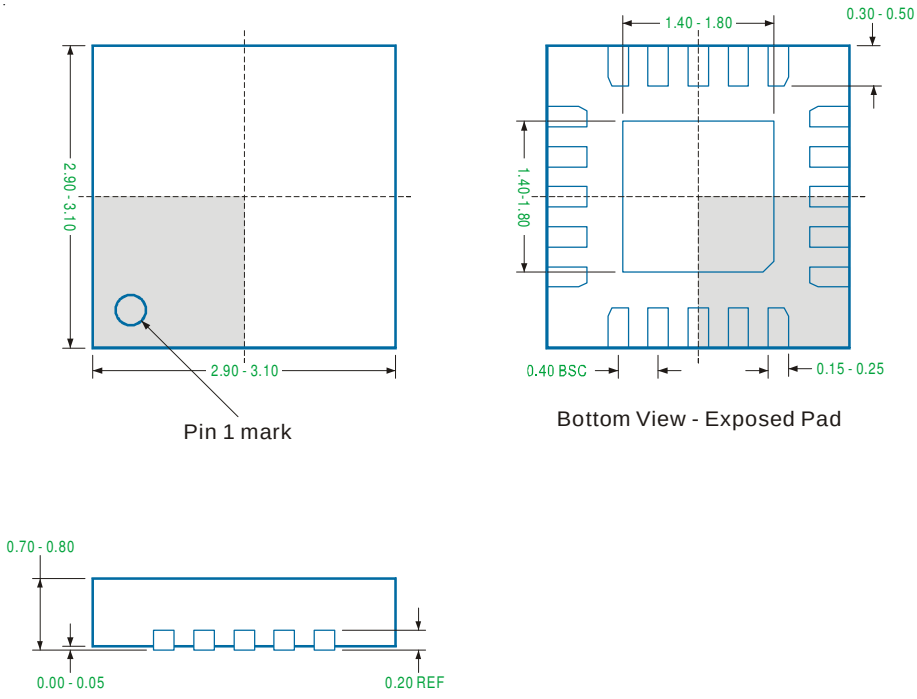


Load (V)

V_{CC} = 5V, 2 Phase CCM Operation

Package Information

WQFN3x3 - 20L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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