1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-05-09

SCHEM,MLB,KEPLER,2PHASE,D2

FSB, 5/9/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9589	1	SCHEM,MLB,KEPLER_2PHASE,D2	SCH	CRITICAL	
820-3332	1	PCBF,MLB,KEPLER_2PHASE,D2	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Wed May 9 13:50:52 2012

DRAWING TITLE: SCHEM,MLB,KEPLER,2PHASE,D2

Apple Inc.

DRAWING NUMBER: 051-9589 | SIZE: D
REVISION: 4.18.0
BRANCH:
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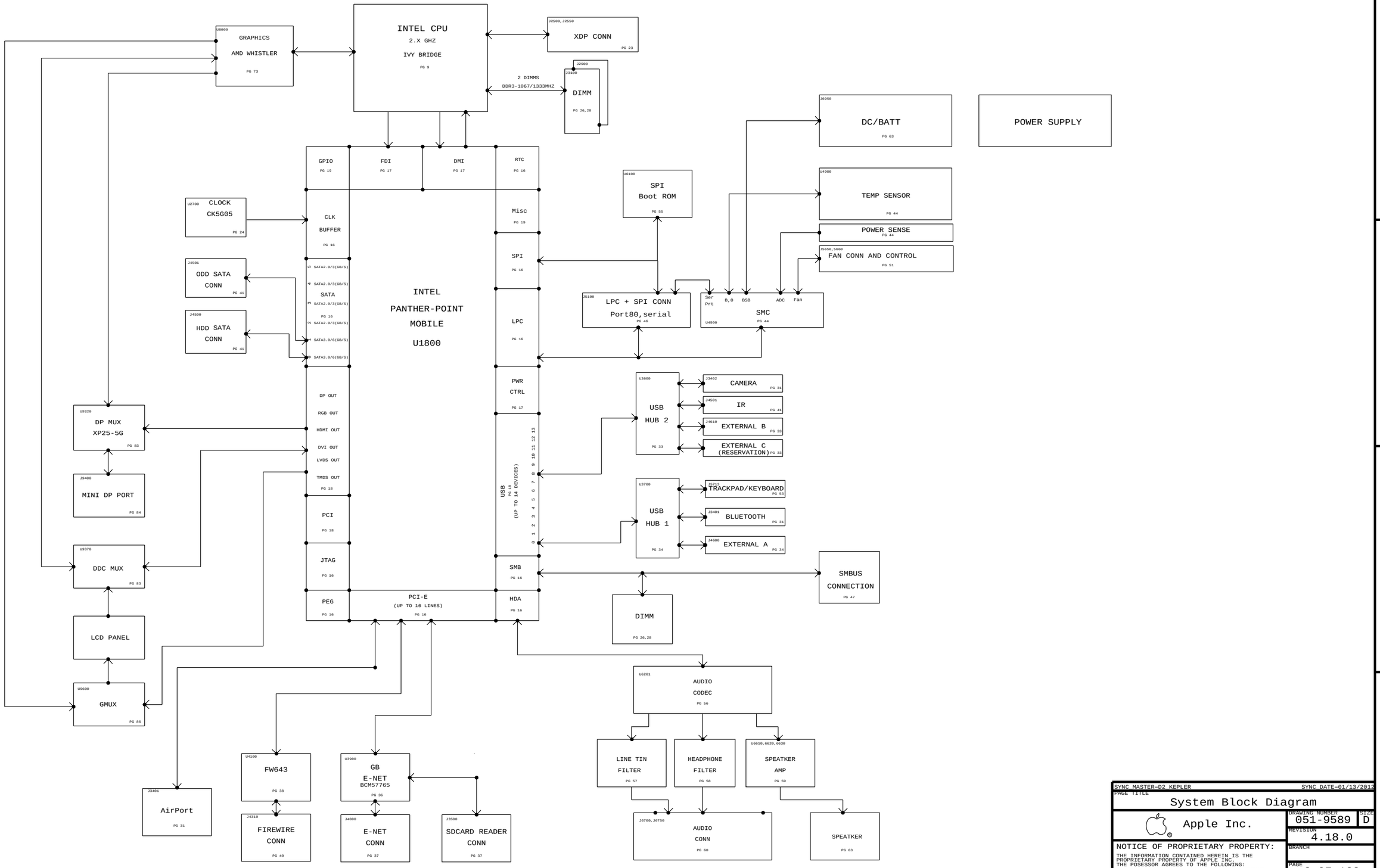

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

System Block Diagram

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D2 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
F6905 6A FUSE
DCIN(16.5V)
R7020
SMC_DCIN_ISENSE
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64)
SMC_RESET_L
R7050
SMC_BATT_ISENSE
PPVBAT_G3H
F7040 8A FUSE
PPBUS_G3H
D6990
R6990
PP18V5_DCIN_CONN
SMC_PBUS_VSENSE
Q5315
ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 62)
PP3V42_G3H
SMC PWRGD NCP303LSN U5000 (PAGE 45)
SMC_RESET_L
SMC AVREF SUPPLY REF3333 (PAGE 45)
PP3V3_S5_AVREF_SMC
PP3V3_S5_SMC
SMC_TPAD_RST_L
SMC_ONOFF_L
U5001
J6950
3S2P (9 TO 12.6V)
PPVBATT_G3H_CONN
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
SMC_CPU_HI_ISENSE
CPU VCORE ISL95831 U7400 (PAGE 67)
CPUIMVP7_VR_ON
SMC_CPU_ISENSE
SMC_CPU_VSENSE
PPVCORE_S0_CPU
CPUIMVP7_AXG_PGOOD
PP5V_S3_GFXIMVP6_VDD
GPU VCORE ISL6263C U8900 (PAGE 82)
R5388/U5388
GPUVCORE_EN
GPUVCORE_PGOOD
U5410
SMC_GPU_ISENSE
SMC_GPU_VSENSE
PPVCORE_GPU
PP5V_S0_CPUVTTS0
1.05V ISL95870 U7600 (PAGE 70)
CPUVTTS0_EN
CPUVTTS0_PGOOD
R7640
PPCPUVTT_S0
SMC_CPU_FSB_ISENSE
TPS22924 U4202 (PAGE 39)
PP1V0_FW_FWPHY
FW_PWR_EN
PANTHER_POINT U1800 (PAGE 16~21)
PM_PWRBTN_L
SYS_RERST#
RSMRST#
ACPRESENT
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
PM_PCH_PWRGD
U2850
PS_PWRGD
PLTRST#
PROCPWRGD
DRAMPWROK
CPU U1000 (PAGE 9~14)
SM_DRAMPWROK
VCCCPUPWRGD
RESET*
GMUX U9600 XP25-5 (PAGE 86)
PB16B EG_RAIL1_EN → P1V1GPU_EN
PB17A EG_RAIL2_EN → P3V3GPU_EN
PB17B EG_RAIL3_EN → GPUVCORE_EN
PB18A EG_RAIL4_EN
PL32A PM_ALL_GPU_PGOOD
SMC U4900 (PAGE 44)
P60 SMC_PM_G2_EN
RC DELAY
P3V3S5_EN
PANTHER-POINT MOBILE U1800 (PAGE 16~21)
SLP_S5#(E4) PM_SLP_S5_L
SLP_S4#(H7) PM_SLP_S4_L
SLP_S3#(P12) PM_SLP_S3_L
P5VS3_EN
DDRREG_EN
P3V3S3_EN
R7978
PM_SLP_S3_L_R
P1V8S0_EN
P1V2S0_EN
CPUVTTS0_EN
P1V5CPU_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
PP5V_S3_DDRREG
U5440
SMC_CPU_DDR_VSENSE
R7350
SMC_DDR_ISENSE
PPDDR_S3_REG
PP1V5_S3
P1V0GPU_EN
P1V5FB_EN
1.003V(L/H) 1.503V(R/H) ISL6236 U9500 (PAGE 85)
PP1V0_S0GPU_REG
R5413
PP1V5_GPU_REG
SMC_GPU_1V8_ISENSE
P1V0GPU_PGOOD
P1V5FB_PGOOD
DDRREG_EN
DDRVTT_EN
1.5V 0.75V TPS51116 U7300 (PAGE 66)
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
4.5V MAX8840 U6200
PP4V5_AUDIO_ANALOG
PP3V3_S0
P1V5CPU_EN
SLG5AP020 U7801
Q7801
PP1V5_S3RS0
P1V5S0FET_GATE
Q7860
PP5V_S0
P5VS0_EN
P5VS3_EN
P3V3S5_EN
5V (L/H) 3.3V (R/H) TPS51125 U7201 (PAGE 65)
PP5V_S3
PP3V3_S5
P5V3V3_PGOOD
Q9806
BKLT_PLT_RST_L && LCD_BKLT_NO
BKLT_EN
LP8550 U9701 (PAGE 87)
PPVOUT_S0_LCDBKLT
Q4260
PFWB0OST
SMC_ADAPTER_EN&&PM_SLP_S3_L
Q7870
PP3V3_S0GPU
P3V3GPU_EN
Q7810
PP3V3_S3
P3V3S3_EN
Q7830
PP3V3_S0_FET
P3V3S0_EN
TPS22924 U4201 (PAGE 39)
PP3V3_FW_FWPHY
FW_PWR_EN
Q7922
PP3V3_ENET
PM_SLP_S3_L&&WOL_EN|SMC_ADAPTER_EN
P1V8_S0_EN
ISL8014A U7720 (PAGE 70)
PP1V8_S0
P1V8S0_PGOOD
P1V2ENET_EN
ISL8014A U7760 (PAGE 70)
PP1V2_ENET
P1V2ENET_PGOOD
Q7850
PP1V2_S0
P1V2S0_EN
U7980
PM_ALL_GPU_PGOOD
P1V8FB_EN
SLG5AP020 U7880
PP1V8_GPUIFP
P1V8GPUIFPXFET_GATE
PP1V8_S0
PP3V3_S0_PWRCTL
P1V8S0_PGOOD
P5V3V3_PGOOD
S0PGOOD_PWROK
U7971 ISL88042IRTJJZ (PAGE 72)
PP3V3_S0
PP1V5_S0
PP1V05_S0
TRST = 200mS
SMC U4900 H8S2117 (PAGE 45)
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
90ms DLY
PP3V3_S0_PWRCTL
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
SMC_ADAPTER_EN
PM_RSMRST_L
CPUIMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	Power Block Diagram
Apple Inc.	DRAWING NUMBER 051-9589 · SIZE D · REVISION 4.18.0 · BRANCH · PAGE 3 OF 132 · SHEET 3 OF 99

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Revision History

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BOM Variants (continued on CSA 6)

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG
085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB
607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR
685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET
685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO
639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3627	PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600

BOM Groups

BOM GROUP	BOM OPTIONS
D2_COMMON	ALTERNATE,COMMON,D2_COMMON1,D2_COMMON2,D2_PROGPARTS,D2_PVB
D2_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,DPMUX:HOCO,TBTRTR:PRQ,TBTBST:Y,TBTHV:P15V,HUB_2NONREM,USBHUB2512B,SPEAKERID,SMC_PACKAGE:PROD,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,P1V5S0:LDO
D2_COMMON2	EDP:YES,MIKEY,PPCPUVCCIO:IVB,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,KBD_BL:SANDWICH,CAPS:INT,BTPWR:S4,XDP,XDP_CPU:BPM,GPU:2P,TPAD_5V:LDO_S5
D2_PVB	VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:N
D2_PROGPARTS	SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG
D2_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,S0PGOOD_ISL,DPMUX_DEBUG,DDRVREF_DAC,VREF:ENG_M3,SENSOR_NONPROD:Y,D_BKL:DEV
D2_DEVEL:FSB	ALTERNATE,IVB_PPT_XDP
IVB_PPT_XDP	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4266	1	IVB,S RDMP,PRQ,E1,2.3,45W,4+2,1.2,0M,BGA	U1000	CRITICAL	CPU_IVY:2_3GHZ
337S4267	1	IVB,S RDMP,PRQ,E1,2.6,45W,4+2,1.25,0M,BGA	U1000	CRITICAL	CPU_IVY:2_6GHZ
337S4268	1	IVB,S RDMP,PRQ,E1,2.7,45W,4+2,1.25,0M,BGA	U1000	CRITICAL	CPU_IVY:2_7GHZ
337S4269	1	PANTHER POINT,C1,SLJ8C,PRQ,BDS2HM77	U1800	CRITICAL	
337S4256	1	IC,GPU,NV GK107-GTX-PS-A2	U8000	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B3,PRQ,C1D,22B 12X12 FC-CSP	U3600	CRITICAL	TBTRTR:PRQ
333S0622	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,HYNIX,C-DIE,38NM		CRITICAL	2G_HYNIX_1600
333S0623	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,SAMSUNG		CRITICAL	2G_SAMSUNG_1600
333S0628	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA		CRITICAL	2G_ELPIDA_1600
333S0625	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX		CRITICAL	4G_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4G_SAMSUNG_1600
333S0629	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA		CRITICAL	4G_ELPIDA_1600
333S0630	4	IC,SDRAM,GDDR5,64MX32,A-DIE,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,GDDR5,64MX32,D-DIE,SAMSUNG	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG
128S0264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO
128S0257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET
725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO
725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET
725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL	
725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL	
725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL	
806-2897	2	CAN,COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL	
825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	

PD Parts

Bar Code Labels / EEEE #'s (continued on CSA 6)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3V]	CRITICAL	EEEE:DY3V
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3W]	CRITICAL	EEEE:DY3W
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3Y]	CRITICAL	EEEE:DY3Y
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY40]	CRITICAL	EEEE:DY40
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY43]	CRITICAL	EEEE:DY43
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY44]	CRITICAL	EEEE:DY44
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY45]	CRITICAL	EEEE:DY45
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY4C]	CRITICAL	EEEE:DY4C
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF1]	CRITICAL	EEEE:DRF1
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF4]	CRITICAL	EEEE:DRF4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDN]	CRITICAL	EEEE:DRDN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDW]	CRITICAL	EEEE:DRDW
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9H]	CRITICAL	EEEE:DT9H
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9D]	CRITICAL	EEEE:DT9D
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9F]	CRITICAL	EEEE:DT9F
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9G]	CRITICAL	EEEE:DT9G
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HN]	CRITICAL	EEEE:F0HN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HR]	CRITICAL	EEEE:F0HR
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW4]	CRITICAL	EEEE:DYW4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HV]	CRITICAL	EEEE:F0HV
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HM]	CRITICAL	EEEE:F0HM
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW5]	CRITICAL	EEEE:DYW5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HY]	CRITICAL	EEEE:F0HY
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HT]	CRITICAL	EEEE:F0HT

Programmables

341S3584	1	IC,TRKPD/KYBD CNTRLR,DVB,D2	U5701	CRITICAL	TPAD_PSOC:PROG
337S2983	1	IC,TP PSOC,QFN,BLANK	U5701	CRITICAL	TPAD_PSOC:BLANK
341S3597	1	IC,EEPROM,CACTUS RIDGE (0.1) FSB,D2	U3690	CRITICAL	TBTROM:PROG
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U3690	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPU ROM,D2,BLANK	U8701	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C, (RENESAS) V3.2.0,DVB,D2	U9100	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,8X8MM,TLP-145V	U9100	CRITICAL	DPMUXMCU:BLANK

DRAM VREF Configs

BOM GROUP	BOM OPTIONS
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_1G_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_1G_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600	2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_SAMSUNG_1333	RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_2G_HYNIX_1600	2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_2G_ELPIDA_1600_S	RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_ELPIDA_1600	2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3726	1	D2 MLB KEPLER DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM
085-4776	1	D2 MLB KEPLER FSB DEVEL BOM	DEVEL_FSB	CRITICAL	DEVEL_FSB_BOM
607-9546	1	D2 MLB KEPLER 2PHASE BASE BOM	BASE	CRITICAL	BASE_BOM
685-0016	1	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	POSCAP_MYLAR	CRITICAL	POSCAP_MYLAR_PAIR

SMC

341S3308	1	IC,SMC,DEVELOPMENT-FSB,A3,D2	U4900	CRITICAL	SMC_PROG:FSB
341S3309	1	IC,SMC,PVB,A3,2.2F36,D2	U4900	CRITICAL	SMC_PROG:PVB

EFI ROM

341S3595	1	IC,EFI,ROM,FSB, D2	U6100	CRITICAL	BOOTROM_PROG:FSB

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0257	128S0264		ALL	Kemet alt to Sanyo
353S3527	353S3528		ALL	Pericom eDP MUX
353S3526	353S3528		ALL	TI eDP MUX
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0855	376S0613	VREFDQ:M1_M3	ALL	Diodes alt to Toshiba
376S1076	376S0634		ALL	Diodes alt to On Semi
376S0903	376S0796		ALL	Fairchild alt to Siliconix
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0434	197S0343		ALL	Epson Alt to TXC
197S0435	197S0343		ALL	NDK Alt to TXC
197S0432	197S0431		ALL	NDK Alt to Epson
197S0452	197S0181		ALL	Epson Alt to TXC
197S0453	197S0181		ALL	NDK Alt to TXC
685-0017	685-0016		ALL	Sanyo POSCAP/Mylar alt to Kemet
376S0975	376S1081		ALL	Toshiba alt to diodes
371S0709	371S0652		ALL	NXP alt to infineon
371S0713	371S0558		ALL	DDS alt to ST
377S0126	377S0066		ALL	New Semtech package
377S0147	377S0066		ALL	On Semi alt to Semtech
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0129		ALL	Cyntec alt to TFT
197S0466	197S0464		ALL	Epson alt to NDK
341S3564	341S3565		ALL	Avnet eDP MUX alt to Renesas

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BOM Configuration

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BOM Variants (continued from CSA 5)

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3382	PCBA,2.3G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DY41	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY41,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3383	PCBA,2.3G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DY42	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY42,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3445	PCBA,2.3G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DYJ5	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYJ5,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3446	PCBA,2.3G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DYJ6	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DYJ6,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2818	PCBA,2.6G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRF0	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF0,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2820	PCBA,2.6G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDP	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDP,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2823	PCBA,2.6G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRDT	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDT,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2819	PCBA,2.6G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDQ	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDQ,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3632	PCBA,2.7G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0JD	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0JD,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3633	PCBA,2.7G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0J3	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0J3,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3630	PCBA,2.7G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0J4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0J4,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3631	PCBA,2.7G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0JC	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0JC,DEVEL_BOM,RAM_4G_ELPIDA_1600

Bar Code Labels / EEEE #’s (continued from CSA 5)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY41]	CRITICAL	EEEE:DY41
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY42]	CRITICAL	EEEE:DY42
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ5]	CRITICAL	EEEE:DYJ5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ6]	CRITICAL	EEEE:DYJ6
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF0]	CRITICAL	EEEE:DRF0
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDP]	CRITICAL	EEEE:DRDP
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDT]	CRITICAL	EEEE:DRDT
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDQ]	CRITICAL	EEEE:DRDQ
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JD]	CRITICAL	EEEE:F0JD
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J3]	CRITICAL	EEEE:F0J3
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J4]	CRITICAL	EEEE:F0J4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JC]	CRITICAL	EEEE:F0JC

Elipda DQ’d
Keeping for PRQ

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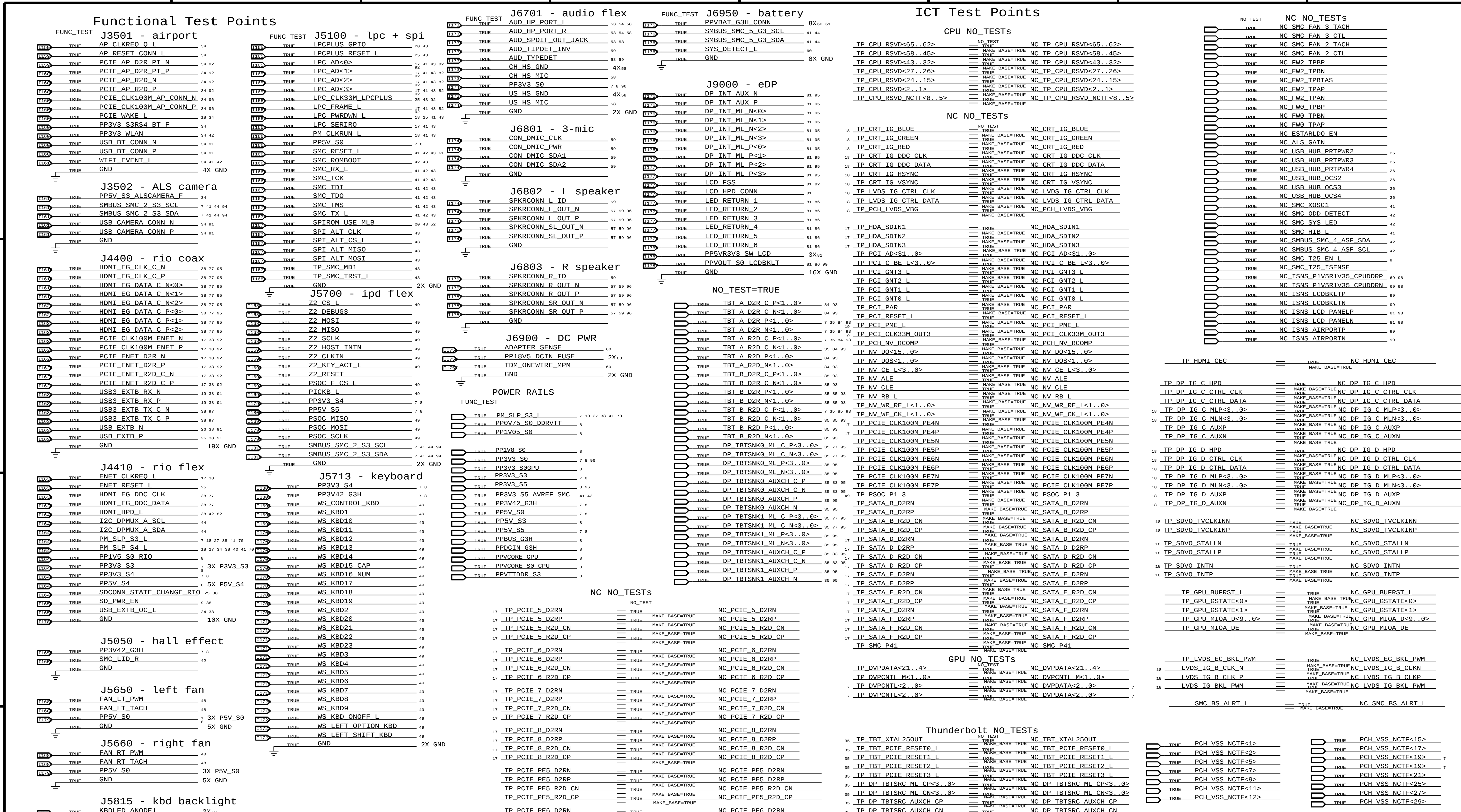

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Functional / ICT Test

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NOTICE OF PROPRIETARY PROPERTY:

G3H Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT
=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_GPU_ISNS_R
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_CPUVCCIOS0
=PPVIN_S0_CPUAXG
=PPVIN_S0_VCCSAS0
=PPVIN_S0_PCHVCCIOS0

=PPVIN_S5_HS_GPU_ISNS
PPVIN_S5_HS_GPU_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S0_GFXIMVP
=PPVIN_S0GPU_P1V5P1V0

=PPVIN_S5_HS_OTHER_ISNS
PPVIN_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMC
=PP3V42_G3H_CHGR
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TPAD
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK

=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL
For PCH RTC Power

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.5 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP5V_S5_P1V5S3RS0FET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD

=PP5V_SUS_FET
PP5V_SUS
MIN_LINE_WIDTH=0.8 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_SUS_PCH

=PP5V_S4_REG
PP5V_S4
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S4_RIO
=PP5V_S4_P5V5Q0FET
=PP5V_S4_P5V3FET
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_ISNS
=PP5V_S4_TPAD
=PP5V_S4_AUDIO

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S3_ISNS
=PP5V_S3_ALSCAMERA
=PP5V_S3_DDRREG
=PP5V_S3_DEBUG_ADC_AVDD
=PP5V_S3_DEBUG_ADC_DVDD
=PP5V_S3_DEBUG_ISNS
=PP5V_S3_MEMRESET

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S0GPU_P1V0P1V35_GPU
=PP5V_S0_P1V5_LDO
=PP5V_S0_AUDIO_XW
=PP5V_S0_BKL
=PP5V_S0_CPUIMVP
=PP5V_S0_CPUVCCIOS0
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_GFXIMVP
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_PCHVCCIOS0
=PP5V_S0_RMC
=PP5V_S0_VCCSAS0
=PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET
PP3V3_S4
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP3V3_S4_TBT_R
=PP3V3_S4_TPAD
=PP3V3_S4_SMC
=PP3V3_S4_RIO
=PP3V3_S4_BT

=PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.8 MM MAKE_BASE=TRUE
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_CNTRL
=PP3V3_SUS_SMC

=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCC_SPI

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_GPU_P3V3GPUFET
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_DPAPWRSW
=PP3V3_S4_DPBPWRSW
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_P1V2P1V8
=PP3V3_S5_P1V5S0
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SMCBATLOW
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_XDP
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_S3_BT
=PP3V3_S3_DPMUX_UC
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_PCH_GPIO
=PP3V3_S3_RIO
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_SMBUS_SMC_3
=PP3V3_S3_TPAD
=PP3V3_S3_USBMUX
=PP3V3_S3_USB_HUB
=PP3V3_S3_USB_RESET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_GYRO
=PP3V3_S3_SMS
=PP3V3_S3_SDBUF

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 mm MAKE_BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_DPMUX
=PP3V3_S0_DPMUXI2C
=PP3V3_S0_DPMUX_UC
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_IMVPISNS
=PP3V3_S0_ISNS
=PP3V3_S0_LCD
=PP3V3_S0_P1V8GPUFET
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SATAMUX
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD
=PP3V3_S0_SYSCLK
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_TPAD
=PP3V3_S0_VMON
=PP3V3_S0_X29THMSNS
=PP3V3_S0_XDP
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS

TBT RAILS

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V MIN_NECK_WIDTH=0.15 MM
MAKE_BASE=TRUE
=PP3V3_TBT_PCH_GPIO
=PPVDDIO_TBT_CLK
=PP3V3_TBTLC_RTR

=PP1V05_TBTLC_FET
PP1V05_TBTLC
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_TBTLC_RTR

=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_TBTCIO_RTR

=PP15V_TBT_REG
PP15V_TBT
MIN_LINE_WIDTH=0.4 MM VOLTAGE=15V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPHV_SW_TBTAPWRSW
=PPHV_SW_TBTBPWRSW

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG
4A max supply
PP1V8_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_PCH_VCCVRM
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_GPUFET
=PP1V8_S0_PCH_VCCTX_LVDS
=PP1V8_S0_PCH_VCC_DFTERM
=PPVDDIO_S0_SBCLK
=PP1V8_S0_P1V5_LDO

=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.5 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPDDR_S3_REG
PP1V5R1V35_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V5R1V35_MEM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B

=PP1V5_S3RS0_FET_ISNS
PP1V5_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3RS0_VMON
=PP1V5_S3_CPU_VCCDDR

=PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA

=PP1V5_S0_RIO_LDO
PP1V5_S0_RIO
MIN_LINE_WIDTH=0.8 MM VOLTAGE=1.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V5_S0_RIO

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU_VCCIO
=PPVCCIO_S0_XDP
=PPVCCIO_S0_CPUIMVP
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PP1V05_S0_RMC

=PPPCHVCCIO_S0_REG
PP1V05_PCHVCCIO_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCIO_PLLPCIE
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCCIO_PLLUSB
=PP1V05_S0_PCH_VCC_DMI
=PP1V05_S0_PCH_VCCIO_PLLFDI
=PP1V05_S0_PCH_VCCDMI_FDI
=PP1V05_S0_P1V05TBTFET_R

Defined here since TBT page does not know PBUS voltage
IGBT PPVIN_SW_TBTBST
VOLTAGE=12.8V

Backlight Rails

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.6V
PPBUS_S0_LCDBKLT_PWR

=SMC_T25_EN_L
NC_SMC_T25_EN_L
MAKE_BASE=TRUE

=PP1V05_S0_P1V05TBTFET
PP1V05_S0_P1V05TBTFET
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_IFPX_PLLVDD
=PP3V3_S0_GFX3V3BIAS
=PP3V3_GPU_VDD33

=PP3V3_S0GPU_MISC_FET
PP3V3_S0GPU_MISC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_MISC

TP_P1V8GPU_EN =P1V8GPU_EN

=PP1V5R1V35_GPU_REG
PP1V5R1V35_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V35_GPU_FBVDDQ
=PP1V35_GPU_S0_FB

=PP1V8_GPU_FET
TP_GPU_PGOOD2
MAKE_BASE=TRUE

=PP1V05_S0GPU_REG
PP1V0_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V0_GPU_DPLL
=PP1V0_GPU_DP_AB
=PP1V0_GPU_DP_CD
=PP1V05_GPU_IFPCD_IOVDD
=PP1V05_GPU_IFPEF_IOVDD
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.0V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCORE_GPU
=PPVCORE_S0_GFX_REG

GND =LVDS_VCCA
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.08SMM
VOLTAGE=0V
MAKE_BASE=TRUE

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 MM VOLTAGE=1.25V
=PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
=PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V

=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPVCCSA_S0_REG
PPVCCSA_S0_REG
MIN_LINE_WIDTH=0.6 MM VOLTAGE=0.9V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCCSA_S0_CPU

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Frame Holes

ZT0915 2.8R2.3 — GND_BATT_CHGND

ZT0950 TH-NSP — GND_CHASSIS_FAN — SL-2.3X3.9-2.9X4.5

ZT0974 TH-NSP — GND_CHASSIS_MLBCAN5 — SL-1.1X0.45-1.1x4x0.75

ZT0975 TH-NSP — GND_CHASSIS_MLBCAN6 — SL-1.1X0.45-1.1x4x0.75

GND (MAKE_BASE=TRUE) — GND_CHASSIS_MLBCAN4

ZT0970 TH-NSP — GND_CHASSIS_MLBCAN1 — SL-1.1X0.45-1.4x0.75

ZT0971 TH-NSP — GND_CHASSIS_MLBCAN2 — SL-1.1X0.45-1.4x0.75

ZT0972 TH-NSP — GND_CHASSIS_MLBCAN3 — SL-1.1X0.45-1.4x0.75

ZT0973 TH-NSP — SL-1.1X0.45-1.4x0.75

THERMAL MODULE STANDOFFS

SH0920 STDOFF-4.5OD2.15H-SM

SH0927 STDOFF-4.5OD2.15H-SM

SH0926 STDOFF-4.5OD2.15H-SM

SH0925 STDOFF-4.5OD1.8H-SM

SH0928 STDOFF-4.5OD2.15H-SM

SH0923 STDOFF-4.5OD1.8H-SM

SH0921 STDOFF-4.5OD2.15H-SM-1

SH0929 STDOFF-4.5OD2.15H-SM

SH0924 STDOFF-4.5OD1.9H-SM

SH0922 STDOFF-4.5OD2.15H-SM

SH0930 STDOFF-4.5OD2.15H-SM

SH0946 STDOFF-4.9OD2.38H-SM-2

SH0945 STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

APN 806-2247

SH0950 SM — SHLD-J5-USB

SH0952 SM — SHLD-J5-CAN-FENCE-MDP-2

SH0951 SM — SHLD-J5-CAN-FENCE-MDP-1

BR0901 MLB-MTG-BRKT-J5

POGO PINS

SH0931 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0932 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0933 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0934 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0935 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0936 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0940 2.8OD1.2ID-1.35H-SM

SH0941 2.8OD1.2ID-1.35H-SM

SH0944 2.8OD1.2ID-1.35H-SM

SH0942 2.8OD1.2ID-1.35H-SM

SH0943 2.8OD1.2ID-1.35H-SM

T29 / GMUX JTAG Signals

TBT_LSOE<3> — TBT_LSEO_LSOE3 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TBT_LSEO<3>

TBT_LSOE<2> — TBT_LSEO_LSOE2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TBT_LSEO<2>

GMUX ALIASES

82 EG_RESET_L (MAKE_BASE=TRUE) — GPU_RESET_L 71 78

18 LVDS_IG_BKL_ON (MAKE_BASE=TRUE) — IG_BKLT_EN 82

18 LVDS_IG_PANEL_PWR (MAKE_BASE=TRUE) — IG_LCD_PWR_EN 82

PEX_CLKREQ_L (MAKE_BASE=TRUE) — EG_CLKREQ_IN_L 78 82

17 PEG_CLKREQ_L (MAKE_BASE=TRUE) — EG_CLKREQ_OUT_L 82

82 DP_TBTSNK0_HPD_IG (MAKE_BASE=TRUE) — DPA_IG_HPD 18 82

82 DP_TBTSNK1_HPD_IG (MAKE_BASE=TRUE) — DPB_IG_HPD 18 82

17 PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE) — NC_PCIE_EXCARD_D2R_N

17 PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE) — NC_PCIE_EXCARD_D2R_P

17 PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE) — NC_PCIE_EXCARD_R2D_C_N

17 PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE) — NC_PCIE_EXCARD_R2D_C_P

92 17 PCIE_CLK100M_EXCARD_N (MAKE_BASE=TRUE) — NC_PCIE_CLK100M_EXCARD_N

92 17 PCIE_CLK100M_EXCARD_P (MAKE_BASE=TRUE) — NC_PCIE_CLK100M_EXCARD_P

17 TP_PCH_CLKOUT_DPN (MAKE_BASE=TRUE) — DPLL_REF_CLKN 11 89

17 TP_PCH_CLKOUT_DPP (MAKE_BASE=TRUE) — DPLL_REF_CLKP 11 89

17 TP_PCH_GPIO64_CLKOUTFLEX0 (MAKE_BASE=TRUE) — NC_PCH_GPIO64_CLKOUTFLEX0

17 TP_PCH_GPIO65_CLKOUTFLEX1 (MAKE_BASE=TRUE) — NC_PCH_GPIO65_CLKOUTFLEX1

17 TP_PCH_GPIO66_CLKOUTFLEX2 (MAKE_BASE=TRUE) — NC_PCH_GPIO66_CLKOUTFLEX2

17 TP_PCH_GPIO67_CLKOUTFLEX3 (MAKE_BASE=TRUE) — NC_PCH_GPIO67_CLKOUTFLEX3

SD_PWR_EN_PCH (MAKE_BASE=TRUE) — ENET_LOW_PWR_PCH 20 24 25

38 7 SD_PWR_EN (MAKE_BASE=TRUE) — ENET_LOW_PWR 25

TP_FW_PWR_EN (MAKE_BASE=TRUE) — FW_PWR_EN 25

SMT GND TEST PONTS

ZT0990 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0991 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0992 2.1SM2.0MM-CIR SMT-PAD-NSP

SH0937 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

ZT0993 2.1SM2.0MM-CIR SMT-PAD-NSP

SH0960 2.8OD1.2ID-1.35H-SM

SH0961 2.8OD1.2ID-1.35H-SM

Digital Ground

MLB_RAMCFG3 — RAMCFG3:L R0913 1K 5% 1/20W MF 201

MLB_RAMCFG2 — RAMCFG2:L R0912 1K 5% 1/20W MF 201

MLB_RAMCFG1 — RAMCFG1:L R0911 1K 5% 1/20W MF 201

MLB_RAMCFG0 — RAMCFG0:L R0910 1K 5% 1/20W MF 201

CPU signals

CPU_VID<0..6> (MAKE_BASE=TRUE) — CPUIMVP_VID<0..6>

27 MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN 27 64

TP_CPU_VTT_SELECT (MAKE_BASE=TRUE) — CPU_VTTSELECT

Unused PEG signals

NC_PEG_D2R_P<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_D2R_P<15..14> 10

NC_PEG_D2R_N<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_D2R_N<15..14> 10

NC_PEG_R2D_C_P<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_R2D_C_P<15..14> 10

NC_PEG_R2D_C_N<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_R2D_C_N<15..14> 10

T29 Signals Through PEG

92 35 PCIE_TBT_D2R_P<3..0> (MAKE_BASE=TRUE) — =PEG_D2R_P<11..8> 10

92 35 PCIE_TBT_D2R_N<3..0> (MAKE_BASE=TRUE) — =PEG_D2R_N<11..8> 10

92 35 PCIE_TBT_R2D_C_P<3..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_P<11..8> 10

92 35 PCIE_TBT_R2D_C_N<3..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_N<11..8> 10

GPU signals

89 88 71 PEG_D2R_P<7..0> (MAKE_BASE=TRUE) — =PEG_D2R_P<7..0> 10

89 88 71 PEG_D2R_N<7..0> (MAKE_BASE=TRUE) — =PEG_D2R_N<7..0> 10

89 71 PEG_R2D_C_P<7..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_P<7..0> 10

89 71 PEG_R2D_C_N<7..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_N<7..0> 10

UNUSED TBT PORTS

TBT_D2R_P<3..2> (MAKE_BASE=TRUE) — NC_TBT_D2RP<3..2> (NO_TEST=TRUE)

TBT_D2R_N<3..2> (MAKE_BASE=TRUE) — NC_TBT_D2RN<3..2> (NO_TEST=TRUE)

TBT_R2D_C_P<3..2> (MAKE_BASE=TRUE) — NC_TBT_R2D_CP<3..2> (NO_TEST=TRUE)

TBT_R2D_C_N<3..2> (MAKE_BASE=TRUE) — NC_TBT_R2D_CN<3..2> (NO_TEST=TRUE)

DPMUX TX & RX

82 DPMUX_UC_BOOT_TX (MAKE_BASE=TRUE) — DPMUX_UC_TX 82

82 DPMUX_UC_BOOT_RX (MAKE_BASE=TRUE) — DPMUX_UC_RX 82

SSD PCIE SIGNALS

92 39 PCIE_SSD_D2R_P<1..0> (MAKE_BASE=TRUE) — =PEG_D2R_P<13..12> 10

92 39 PCIE_SSD_D2R_N<1..0> (MAKE_BASE=TRUE) — =PEG_D2R_N<13..12> 10

92 39 PCIE_SSD_R2D_C_P<1..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_P<13..12> 10

92 39 PCIE_SSD_R2D_C_N<1..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_N<13..12> 10

TP_PCIE_CLK100M_FW_P (MAKE_BASE=TRUE) — PCIE_CLK100M_FW_P 17 92

TP_PCIE_CLK100M_FW_N (MAKE_BASE=TRUE) — PCIE_CLK100M_FW_N 17 92

UNUSED FDI SIGNALS

NC_PCH_FDI_DATA_N<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_DATA_N<7..0> 18

NC_PCH_FDI_DATA_P<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_DATA_P<7..0> 18

NC_PCH_FDI_FSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_FSYNC<1..0> 18

NC_PCH_FDI_LSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_LSYNC<1..0> 18

NC_CPU_FDI_DATA_N<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_DATA_N<7..0> 10 89

NC_CPU_FDI_DATA_P<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_DATA_P<7..0> 10 89

NC_CPU_FDI_FSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_FSYNC<1..0> 10 89

NC_CPU_FDI_LSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_LSYNC<1..0> 10 89

USB SIGNALS

91 34 USB_BT_P (MAKE_BASE=TRUE) — USBHUB_DN1_P 26

91 34 USB_BT_N (MAKE_BASE=TRUE) — USBHUB_DN1_N 26

91 49 USB_TPAD_P (MAKE_BASE=TRUE) — USBHUB_DN2_P 26

91 49 USB_TPAD_N (MAKE_BASE=TRUE) — USBHUB_DN2_N 26

91 41 USB_SMC_P (MAKE_BASE=TRUE) — USBHUB_DN3_P 26

91 41 USB_SMC_N (MAKE_BASE=TRUE) — USBHUB_DN3_N 26

PU_USBHUB_DN4P (MAKE_BASE=TRUE) — USBHUB_DN4_P 26

PU_USBHUB_DN4N (MAKE_BASE=TRUE) — USBHUB_DN4_N 26

8 =PP5V_S0_AUDIO_XW

XW0902 SM — PP5V_S0_AUDIO_AMP_L 57
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XW0903 SM — PP5V_S0_AUDIO_AMP_R 57
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

NC_LVDS_IG_A_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_P<3> 18 91

NC_LVDS_IG_A_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_N<3> 18 91

NC_LVDS_IG_B_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_P<3> 18

NC_LVDS_IG_B_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_N<3> 18

NC_LVDS_IG_A_CLK_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_CLK_N 18 91

NC_LVDS_IG_A_CLK_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_CLK_P 18 91

NC_LVDS_IG_A_DATA_N<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_N<2..0> 18 91

NC_LVDS_IG_A_DATA_P<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_P<2..0> 18 91

NC_LVDS_IG_B_DATA_N<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_N<2..0> 18 91

NC_LVDS_IG_B_DATA_P<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_P<2..0> 18 91

NC_LVDS_IG_DDC_CLK (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_DDC_CLK 18

NC_LVDS_IG_DDC_DATA (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_DDC_DATA 18

NC_PCIE_FW_D2RN (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_D2R_N 17

NC_PCIE_FW_D2RP (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_D2R_P 17

NC_PCIE_FW_R2D_CN (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_R2D_C_N 17

NC_PCIE_FW_R2D_CP (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_R2D_C_P 17

NC_SATA_ODD_R2D_N (MAKE_BASE=TRUE) — SATA_ODD_D2R_N 17 91

NC_SATA_ODD_R2D_P (MAKE_BASE=TRUE) — SATA_ODD_D2R_P 17 91

NC_SATA_ODD_R2D_C_N (MAKE_BASE=TRUE) — SATA_ODD_R2D_C_N 17 91

NC_SATA_ODD_R2D_C_P (MAKE_BASE=TRUE) — SATA_ODD_R2D_C_P 17 91

NC_DP_IG_MLP<3..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_DP_IG_B_MLP<3..0> 18

NC_DP_IG_MLN<3..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_DP_IG_B_MLN<3..0> 18

TBTBST:N

37 8 =PPVIN_SW_TBTBST — R0950 0 5% 1/8W MF-LF 805 — =PP15V_TBT_REG 8 37

UNUSED USB SIGNALS

NC_USB3_EXTD_TX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_TX_P 19

NC_USB3_EXTD_TX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_TX_N 19

NC_USB3_EXTD_RX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_RX_P 19

NC_USB3_EXTD_RX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_RX_N 19

NC_USB_EXTD_EHCI_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTD_EHCI_P 19

NC_USB_EXTD_EHCI_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTD_EHCI_N 19

NC_USB3_EXTC_TX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_TX_P 19 91

NC_USB3_EXTC_TX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_TX_N 19 91

NC_USB3_EXTC_RX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_RX_P 19 91

NC_USB3_EXTC_RX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_RX_N 19 91

NC_USB_EXTC_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTC_P 19 91

NC_USB_EXTC_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTC_N 19 91

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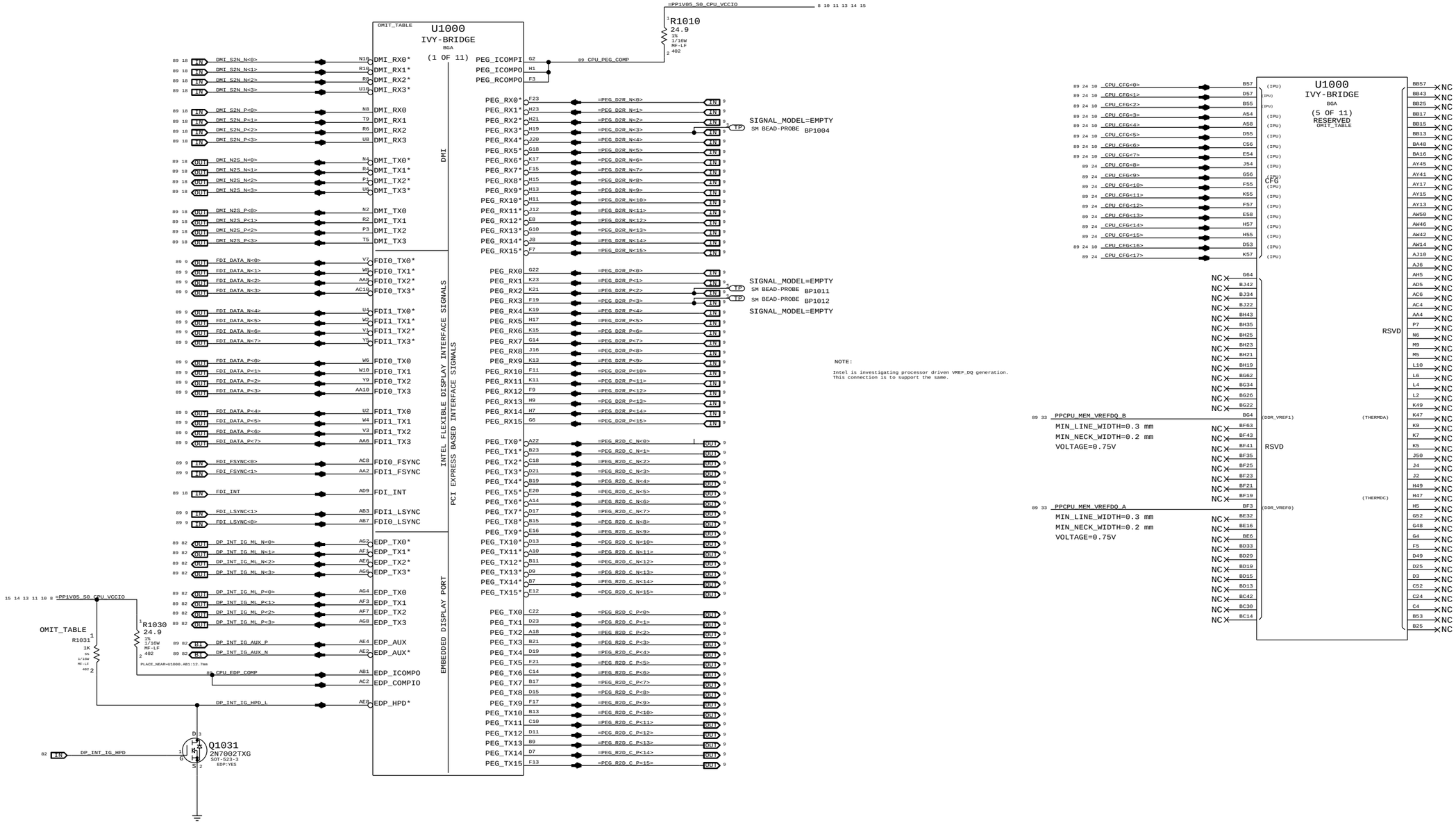

NOTE:

Intel is investigating processor driven VREF_DQ generation.
This connection is to support the same.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/10W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/10W,10K,0402,SMD,LF	R1031		EDP:NO

CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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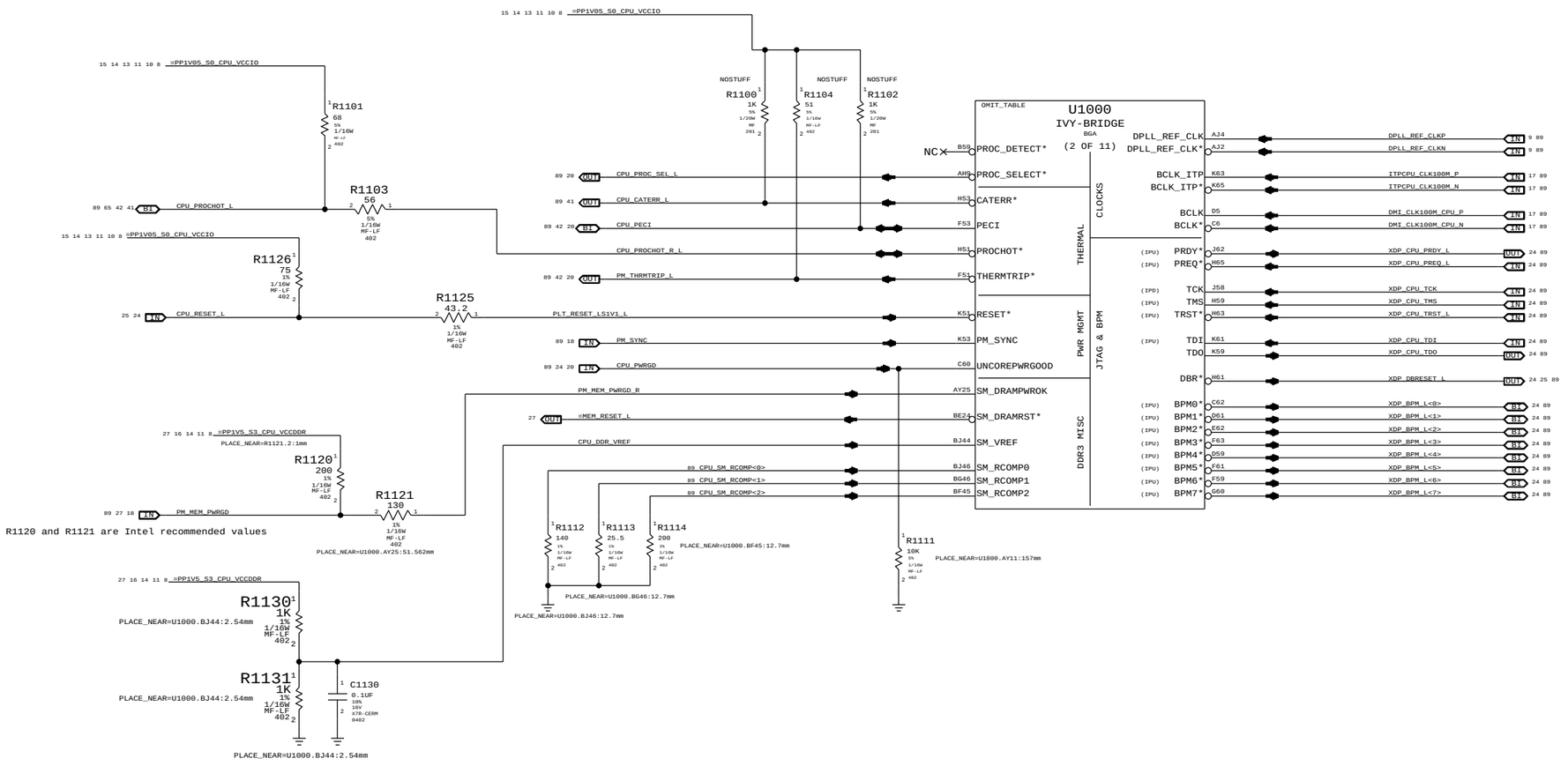

PAGE TITLE	CPU CLOCK/MISC/JTAG
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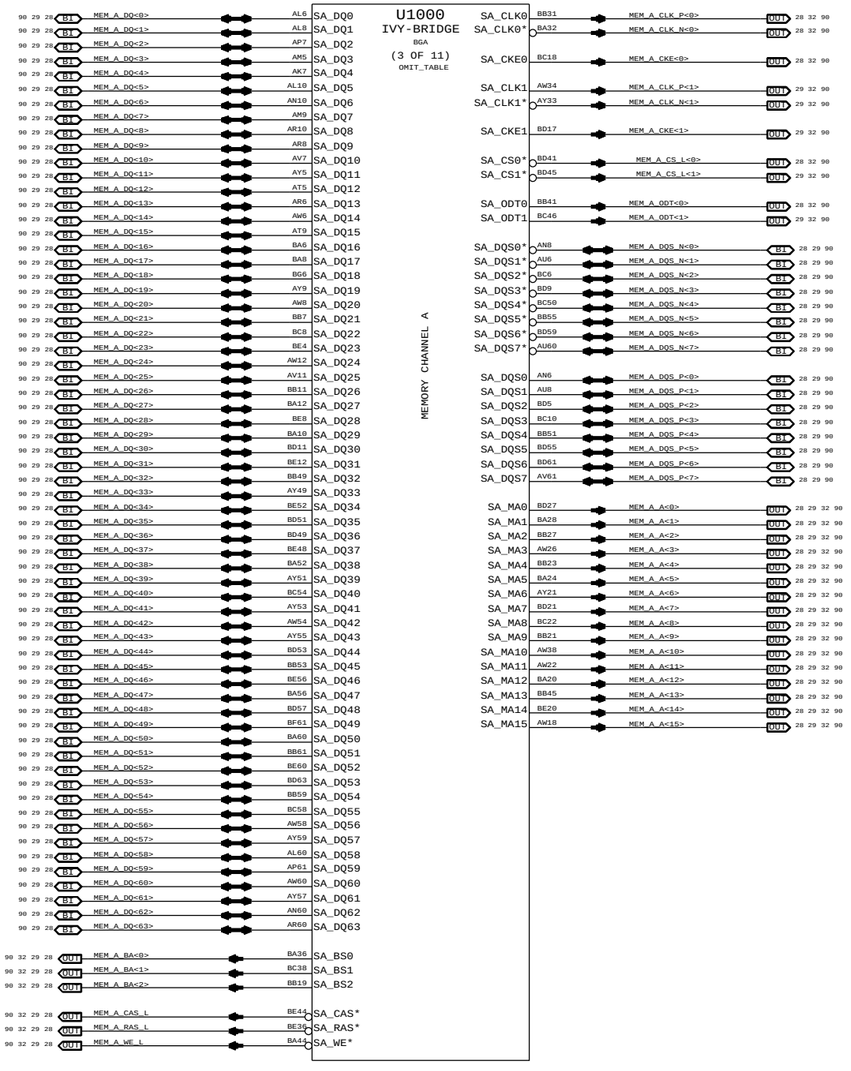

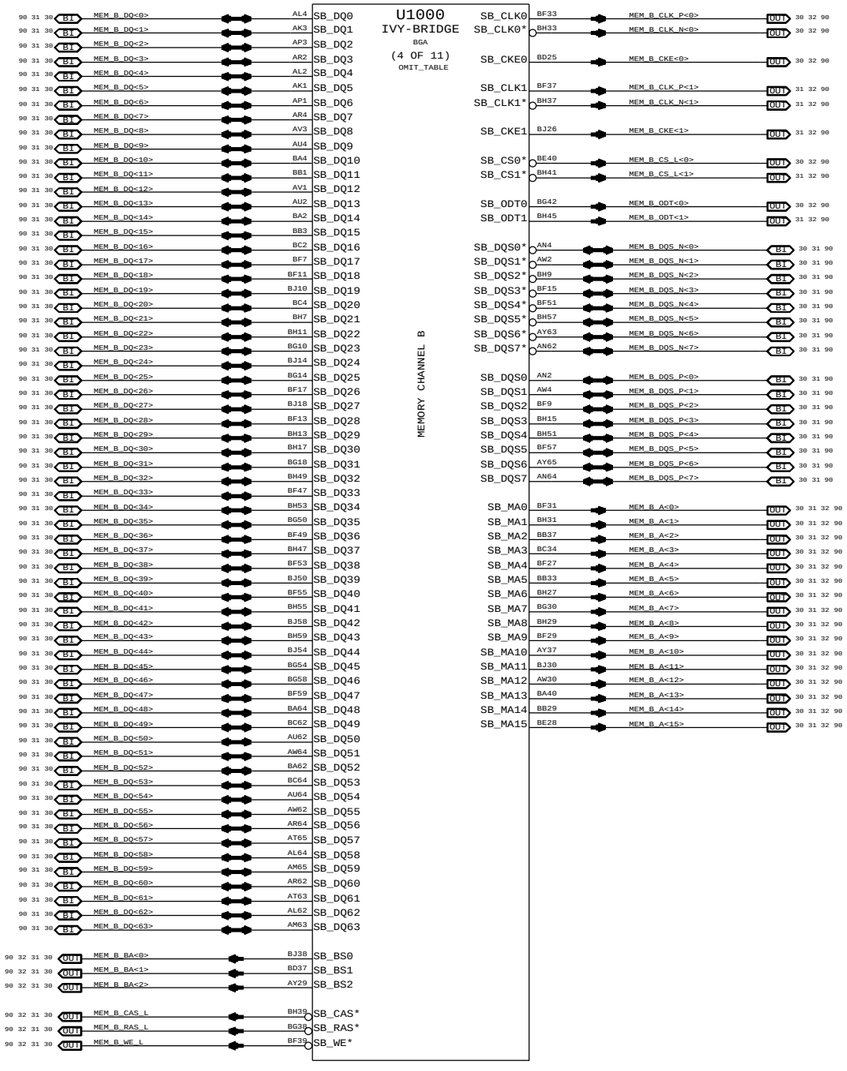

SYNC_DATE=01/13/2012

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

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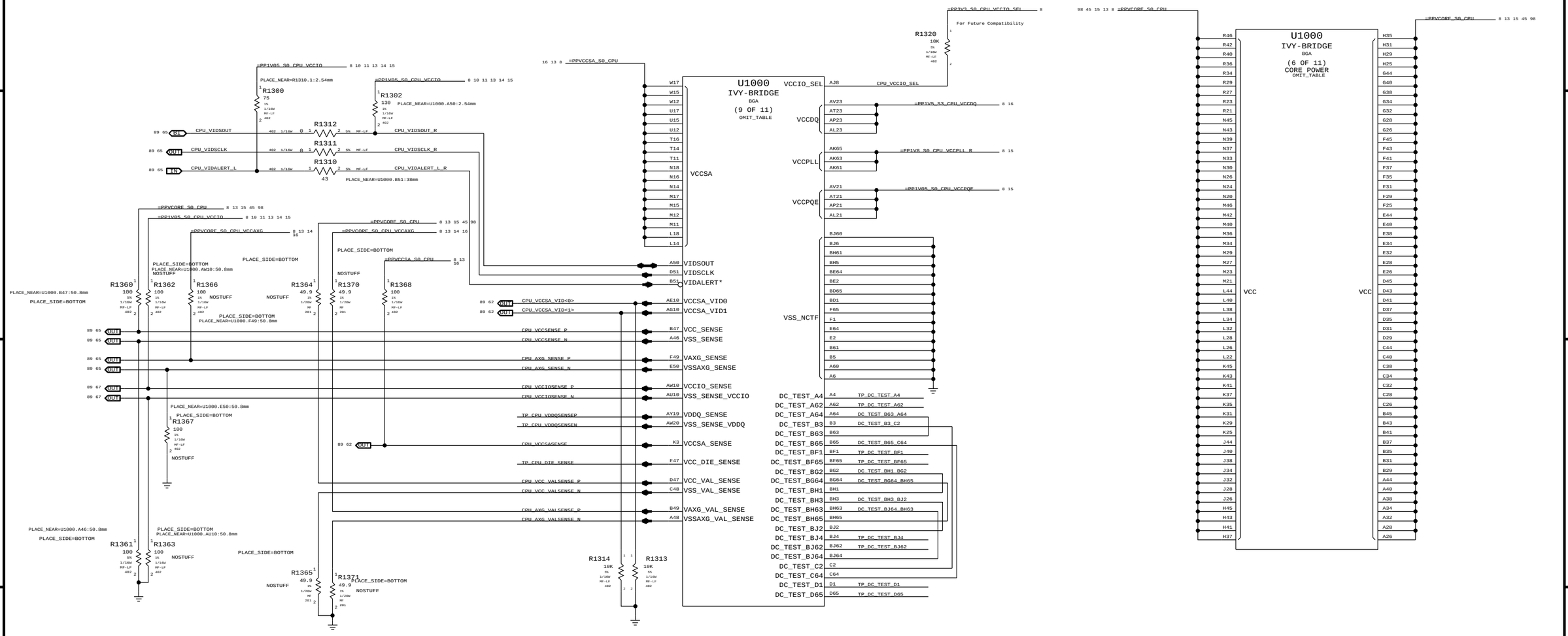

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

CPU POWER

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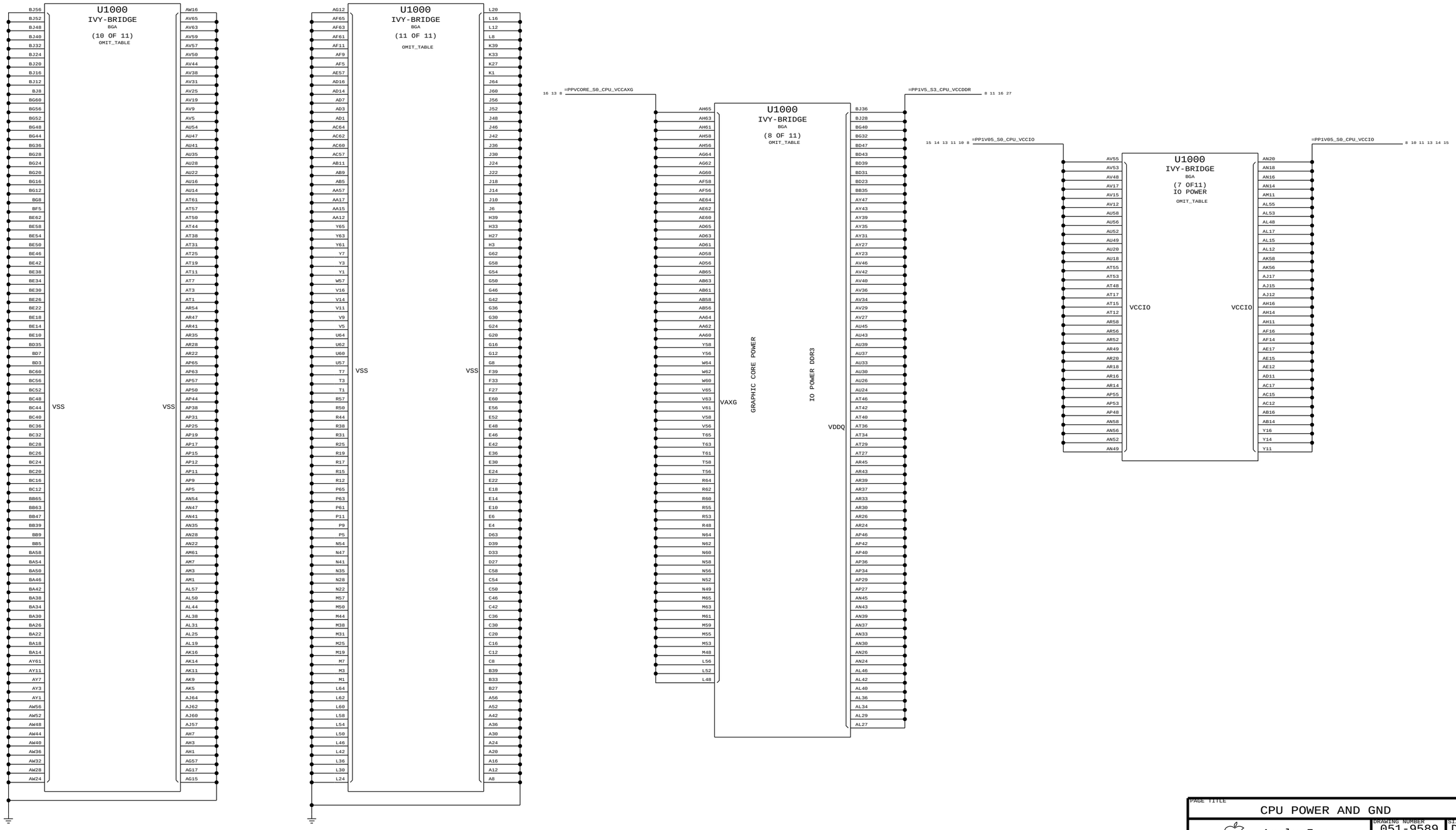

PAGE TITLE
CPU POWER AND GND

Apple Inc.

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm , 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

98 45 13 8 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X6S-CERM 0402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 4V CERM-X6S 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 4V CERM-X6S 0201

PLACEMENT_NOTE (C1620-C1623):
Place near inductors on bottom side.
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 4V X6S 0402

NOSTUFF CRITICAL C1690 C1691 C1698 C1693 C1694 C1695 C1696 C1699
20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639 NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1640-C1645):

CRITICAL C1640 C1641 C1642 C1643 C1644 C1645 C1688 C1689
270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

13 11 10 8 14 =PP1V05_S0_CPU_VCCIO

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X6S-CERM 0402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 4V X6S-CERM 0603

CRITICAL C1682 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
CRITICAL C1683 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 8 13
C1684 1UF 10% 10V X6S-CERM 0402

CPU VCCPLL DECOUPLING

8 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF-LF 402
=PP1V8_S0_CPU_VCCPLL_R 8 13
PLACE_NEAR=U1000.AK61:5MM
C1685 1UF 10% 10V X6S-CERM 0402
C1686 1UF 10% 10V X6S-CERM 0402
CRITICAL C1687 220UF 20% 2.5V TANT B16 (Z = 1.2mm, place on short side behind CPU)
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2013

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VAXG DECOUPLING

INTEL RECOMMENDATION: 2X 470UF 4MOHM, 2X 470UF 4MOHM (NOSTUFF), 6X 22UF 0805, 2X 22UF 0805 (NOSTUFF), 6X 10UF 0603, 2X 10UF 0603 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)
APPLE IMPLEMENTATION: 0X 470UF 4MOHM, 3X 330UF 9MOHM , 6X 22UF 0603, 2X 22UF 0603 (NOSTUFF), 6X 10UF 0402, 2X 10UF 0402 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)

14 13 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 — 1UF 10% 10V X6S-CERM 0402
NOSTUFF: C1709 C1710 C1711 C1712 C1713 C1714 C1715 C1716 C1717 — 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 C1719 C1720 C1721 C1722 C1723 — 10UF 20% 4V X6S 0402
NOSTUFF: C1724 C1725 — 10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 C1727 C1728 C1729 C1730 C1731 — 22UF 20% 4V X6S 0603
NOSTUFF: C1732 C1733 — 22UF 20% 4V X6S 0603

PLACEMENT_NOTE (C1734-C1735):

CRITICAL C1734 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1735 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1737 330UF-6MOHM 20% 2.0V POLY-TANT D15T
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

27 14 11 8 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747 — 1UF 10% 10V X6S-CERM 0402

Place close to U1000 on bottom side

C1748 C1749 C1750 C1751 C1752 C1753 C1754 C1755 — 10UF 20% 4V X6S-CERM 0603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603
=PP1V5_S3_CPU_VCCDQ 8 13
C1757 1UF 10% 10V X6S-CERM 0402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

13 8 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 C1759 C1760 C1761 C1762 — 1UF 10% 10V X6S-CERM 0402

C1763 C1764 C1765 C1766 C1767 — 10UF 20% 4V X6S-CERM 0603

CRITICAL C1768 330UF-6MOHM 20% 2.0V POLY-TANT DIST-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

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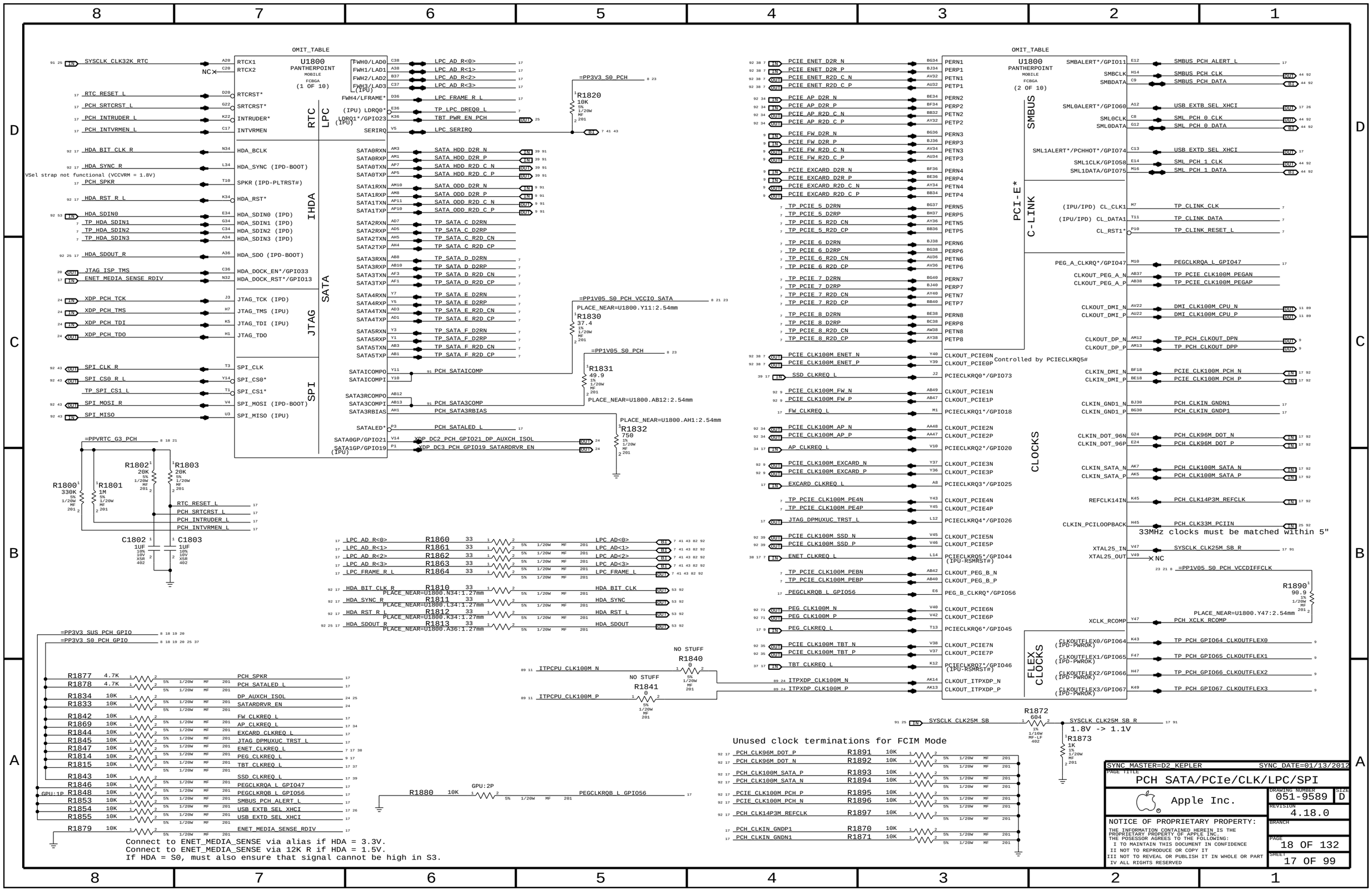
OMIT_TABLE
U1800
PANTHERPOINT
MOBILE
FCBGA
(1 OF 10)
RTCX1
RTCX2
RTCRST*
SRTCRST*
INTRUDER*
INTVRMEN
RTC
LPC
IHDA
SATA
JTAG
SPI
HDA_BCLK
HDA_SYNC (IPD-BOOT)
SPKR (IPD-PLTRST#)
HDA_RST*
HDA_SDIN0 (IPD)
HDA_SDIN1 (IPD)
HDA_SDIN2 (IPD)
HDA_SDIN3 (IPD)
HDA_SDO (IPD-BOOT)
HDA_DOCK_EN*/GPIO33
HDA_DOCK_RST*/GPIO13
JTAG_TCK (IPD)
JTAG_TMS (IPU)
JTAG_TDI (IPU)
JTAG_TDO
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_MOSI (IPD-BOOT)
SPI_MISO (IPU)
SYSCLK_CLK32K_RTC
NCX
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
VSel strap not functional (VCCVRM = 1.8V)
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_ISP_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
=PPVRTC_G3_PCH
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1UF
C1803 1UF
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
(IPU)
FWH4/LFRAME*
(IPU) LDRQ0*
LDRQ1*/GPIO23
(IPU)
SERIRQ
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
=PP3V3_S0_PCH
R1820 10K
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
SATAICOMPO
SATAICOMPI
PCH_SATAICOMPI
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.Y11:2.54mm
R1830 37.4
=PP1V05_S0_PCH
R1831 49.9
PLACE_NEAR=U1800.AB12:2.54mm
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AH1:2.54mm
R1832 750
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
SATA1GP/GPIO19
(IPU)
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1810 33
R1811 33
R1812 33
R1813 33
HDA_BIT_CLK
HDA_SYNC
HDA_RST
HDA_SDOUT
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1877 4.7K
R1878 4.7K
R1834 10K
R1833 10K
R1842 10K
R1869 10K
R1844 10K
R1845 10K
R1847 10K
R1814 10K
R1815 10K
R1843 10K
R1846 10K
R1848 10K
R1853 10K
R1854 10K
R1855 10K
R1879 10K
GPU:1P
GPU:2P
R1880 10K
PEGCLKRQB_L_GPIO56
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
OMIT_TABLE
U1800
PANTHERPOINT
MOBILE
FCBGA
(2 OF 10)
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
TP_PCIE_5_D2RN
TP_PCIE_5_D2RP
TP_PCIE_5_R2D_CN
TP_PCIE_5_R2D_CP
TP_PCIE_6_D2RN
TP_PCIE_6_D2RP
TP_PCIE_6_R2D_CN
TP_PCIE_6_R2D_CP
TP_PCIE_7_D2RN
TP_PCIE_7_D2RP
TP_PCIE_7_R2D_CN
TP_PCIE_7_R2D_CP
TP_PCIE_8_D2RN
TP_PCIE_8_D2RP
TP_PCIE_8_R2D_CN
TP_PCIE_8_R2D_CP
CLKOUT_PCIE0N
CLKOUT_PCIE0P
Controlled by PCIECLKRQ5#
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
(IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46
(IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
TP_PCIE_5_D2RN
TP_PCIE_5_D2RP
TP_PCIE_5_R2D_CN
TP_PCIE_5_R2D_CP
TP_PCIE_6_D2RN
TP_PCIE_6_D2RP
TP_PCIE_6_R2D_CN
TP_PCIE_6_R2D_CP
TP_PCIE_7_D2RN
TP_PCIE_7_D2RP
TP_PCIE_7_R2D_CN
TP_PCIE_7_R2D_CP
TP_PCIE_8_D2RN
TP_PCIE_8_D2RP
TP_PCIE_8_R2D_CN
TP_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
SSD_CLKREQ_L
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L_GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
NO STUFF
R1840 0
R1841 0
SMBUS
PCI-E*
C-LINK
CLOCKS
FLEX CLOCKS
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
SMBUS_PCH_ALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEGCLKRQA_L_GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
33MHz clocks must be matched within 5"
SYSCLK_CLK25M_SB_R
NC
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9
PLACE_NEAR=U1800.Y47:2.54mm
PCH_XCLK_RCOMP
SYSCLK_CLK25M_SB
R1872 604
1.8V -> 1.1V
R1873 1K
Unused clock terminations for FCIM Mode
PCH_CLK96M_DOT_P
PCH_CLK96M_DOT_N
PCH_CLK100M_SATA_P
PCH_CLK100M_SATA_N
PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH_N
PCH_CLK14P3M_REFCLK
PCH_CLKIN_GNDP1
PCH_CLKIN_GNDN1
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
R1870 10K
R1871 10K
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SYNC_DATE=01/13/2012
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
BRANCH
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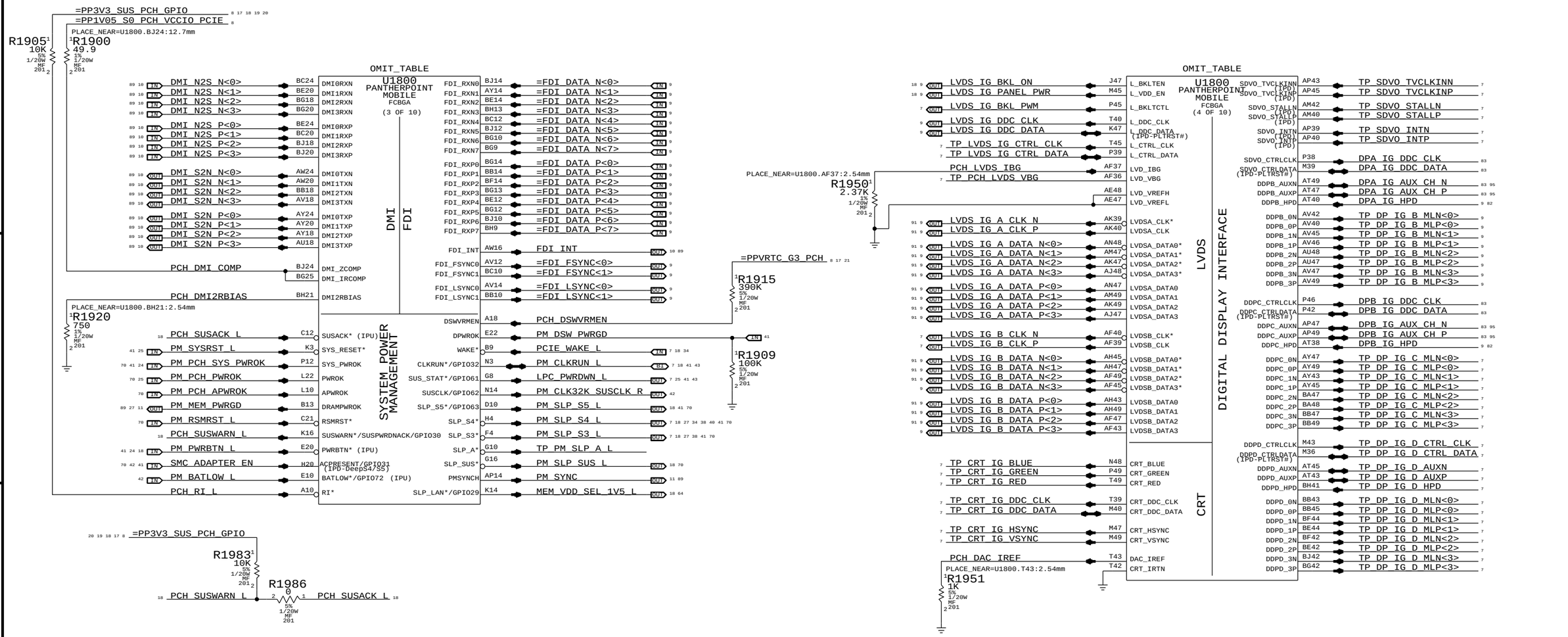

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PAGE TITLE: PCH DMI/FDI/PM/Graphics

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DRAWING NUMBER: 051-9589 SIZE: D

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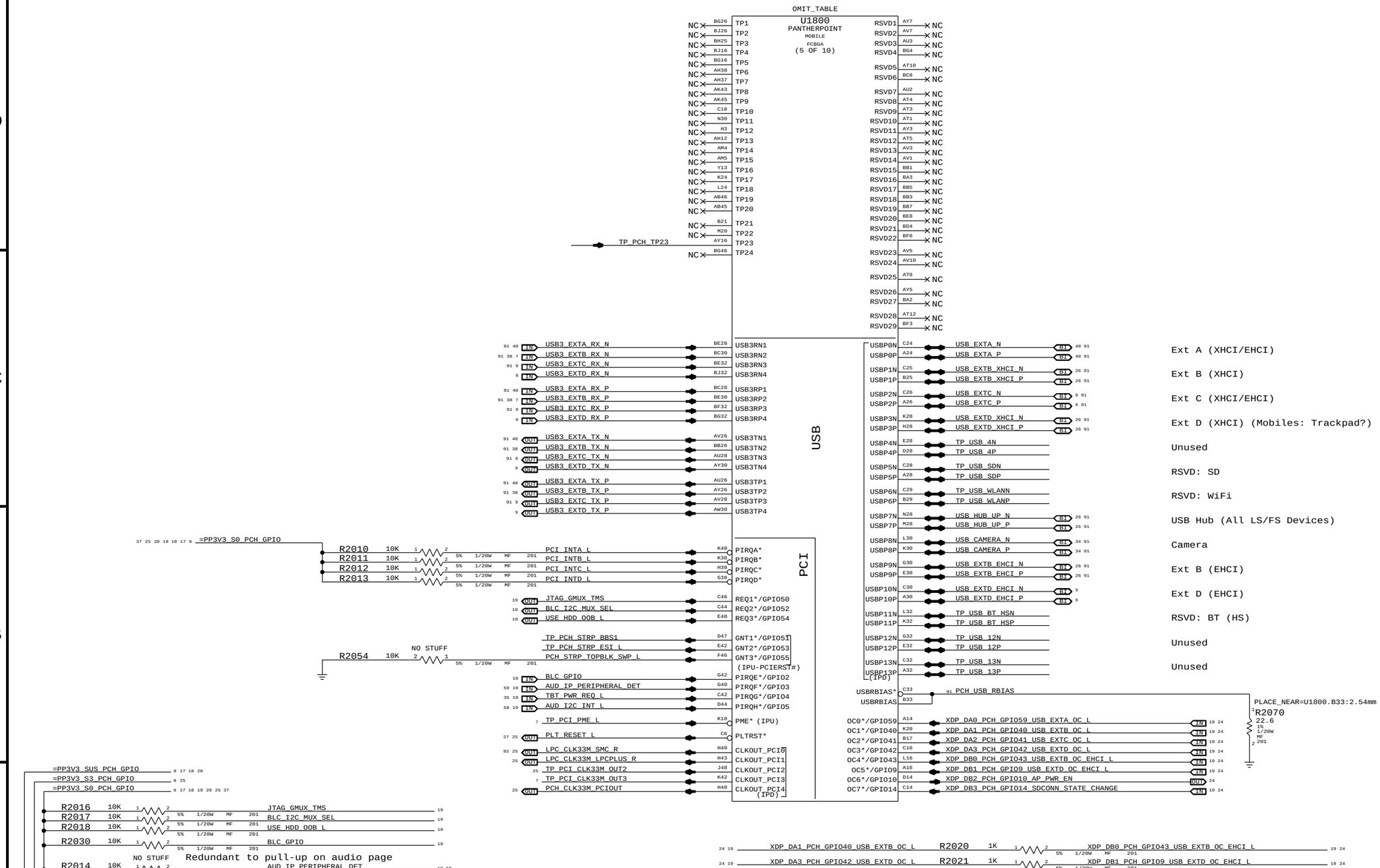

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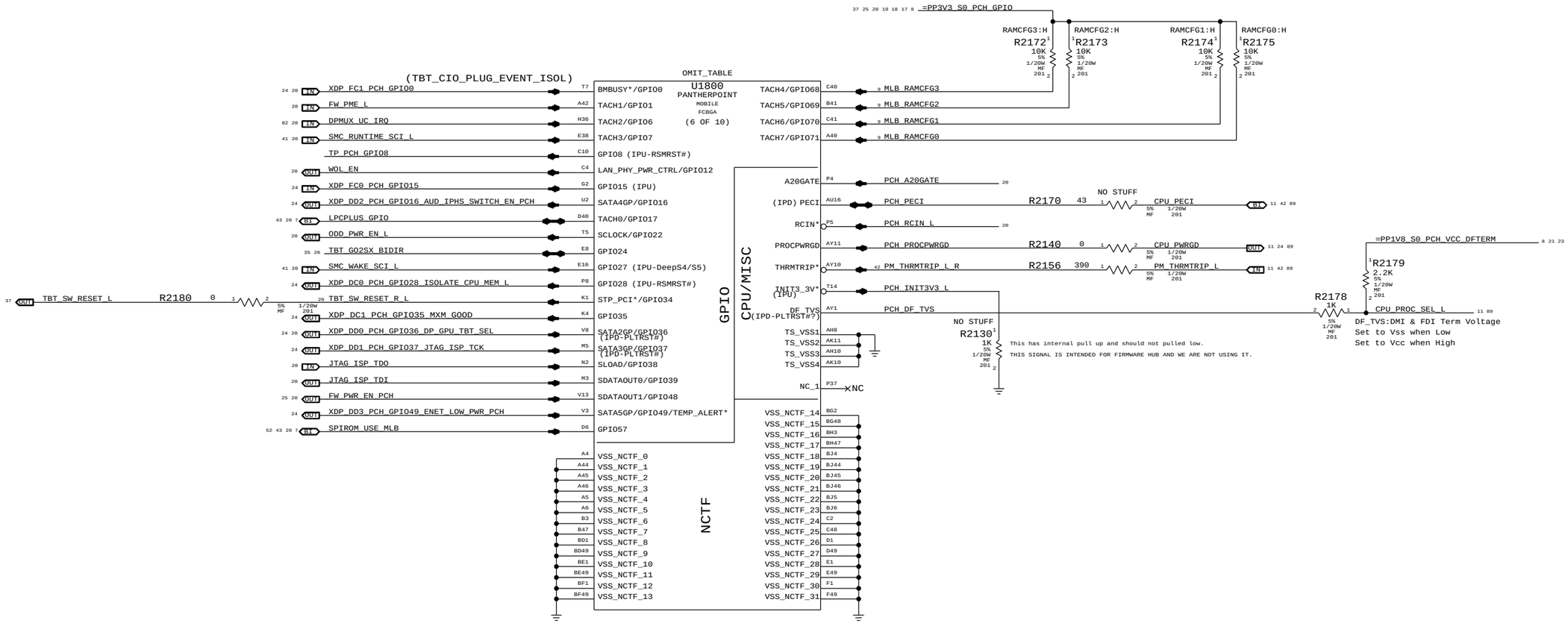
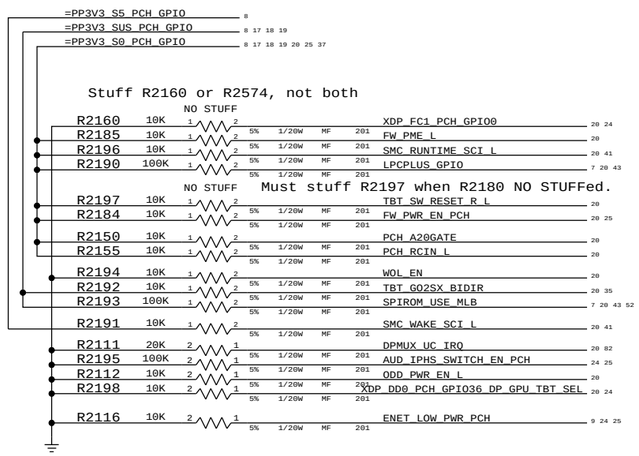
PAGE TITLE	PCH PCI/USB/TP/RSVD
Apple Inc.	DRAWING NUMBER 051-9589 · SIZE D · REVISION 4.18.0 · BRANCH · PAGE 20 OF 132 · SHEET 19 OF 99

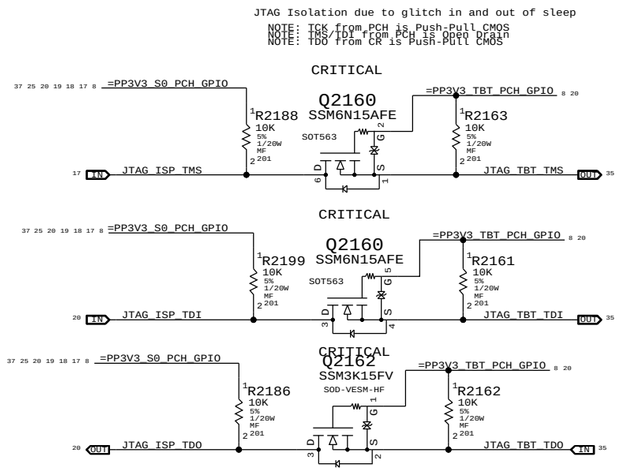
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

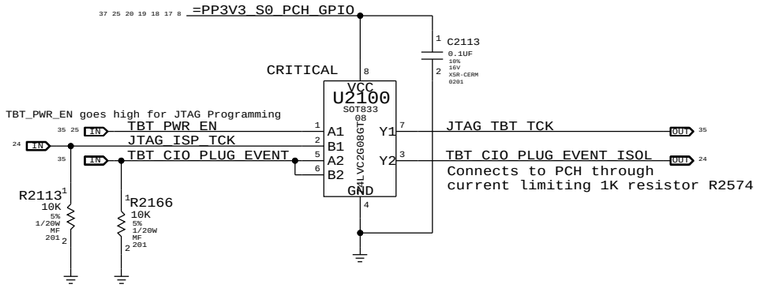
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.









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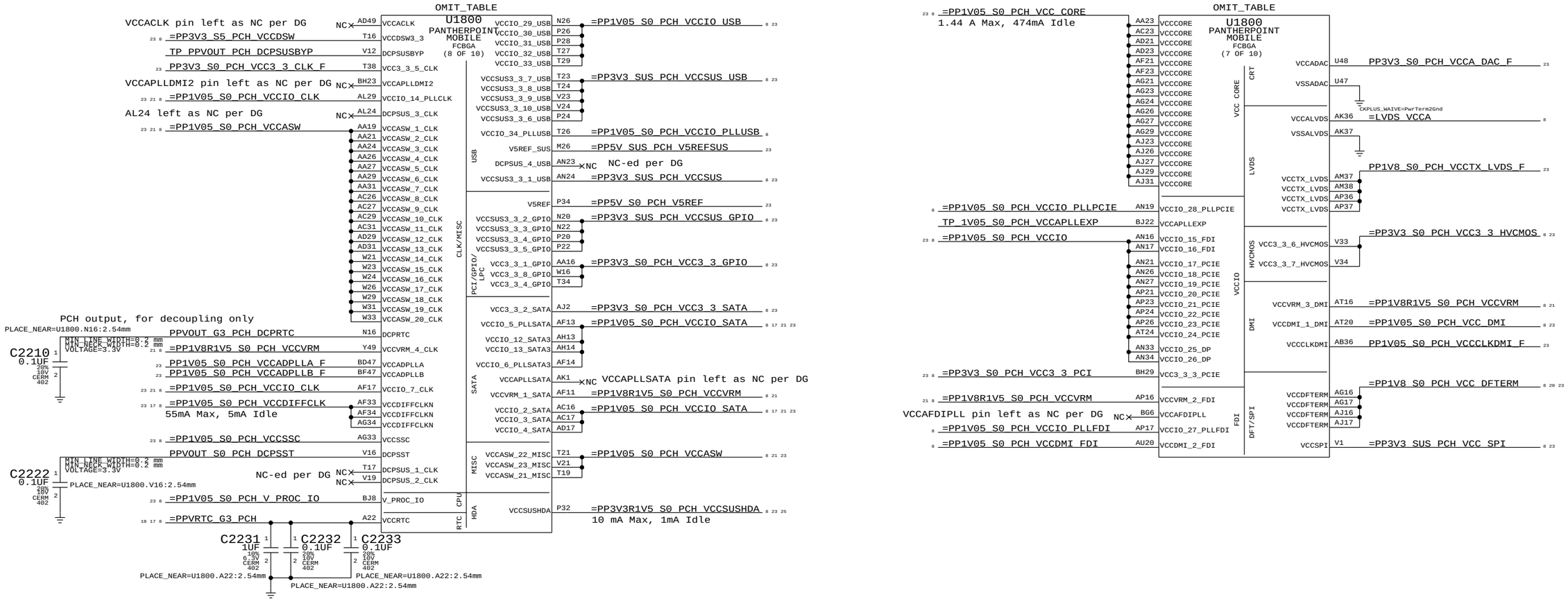

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PAGE TITLE: PCH POWER

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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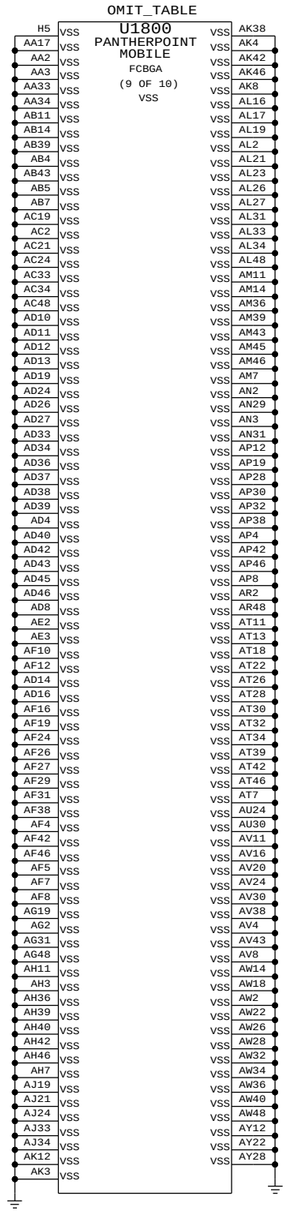

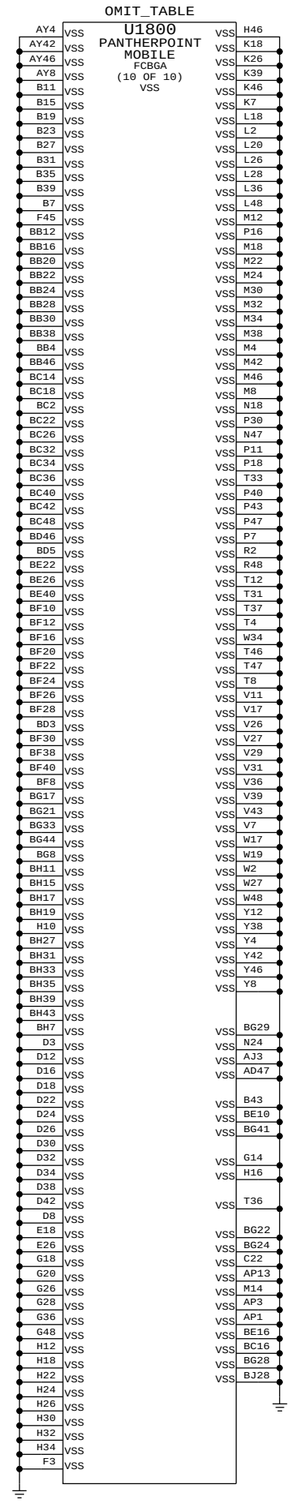

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PCH GROUNDS

Apple Inc.

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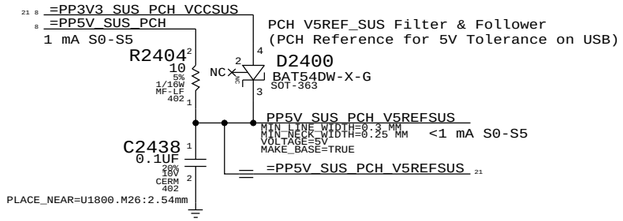

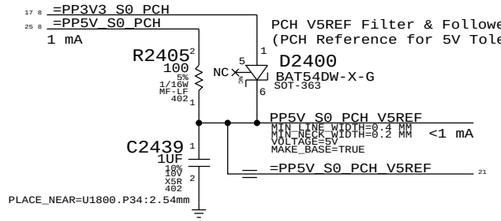

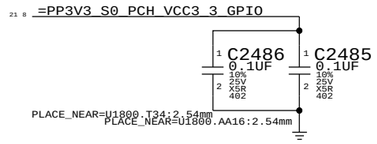

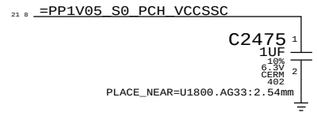

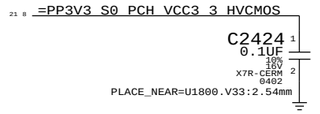

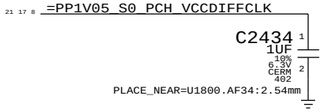

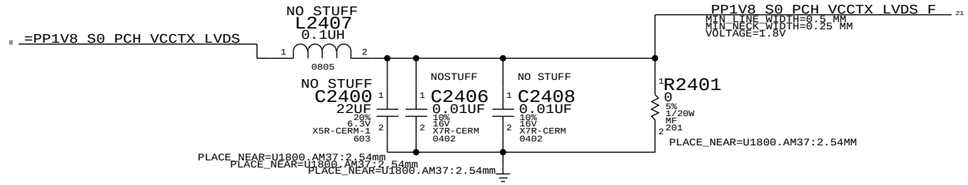

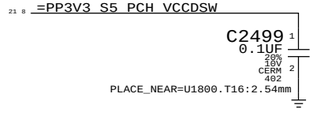

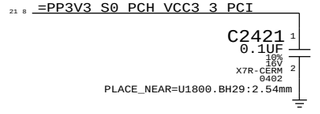

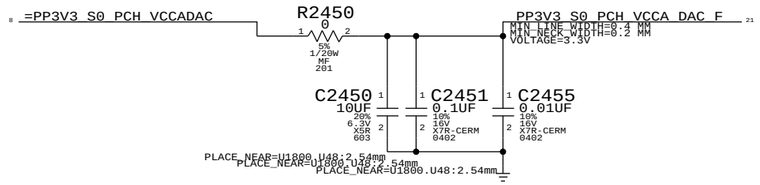

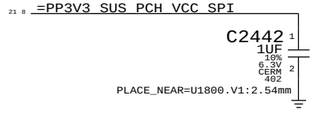

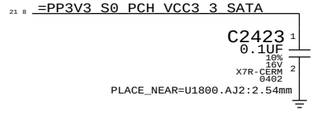

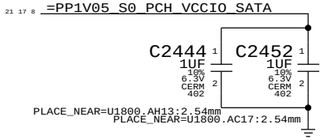

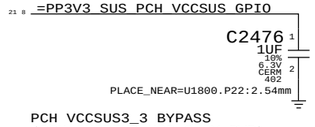

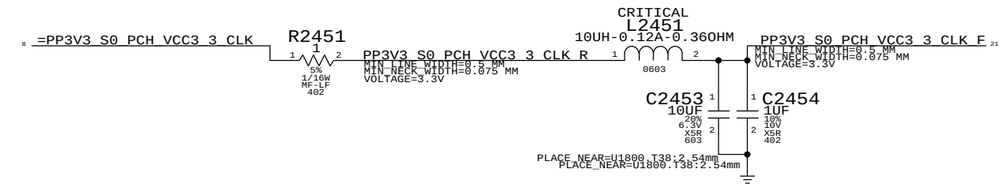

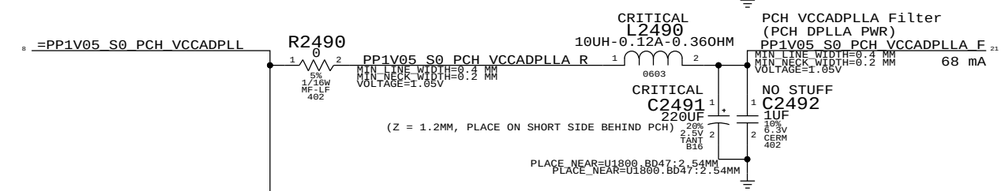

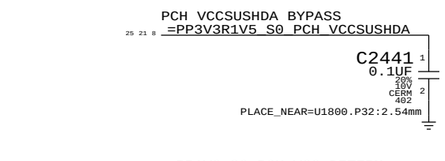

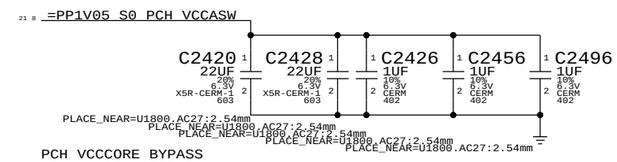

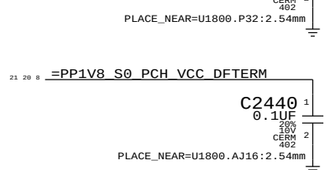

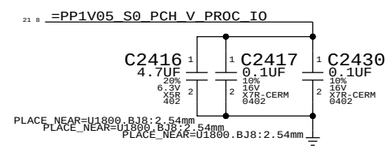

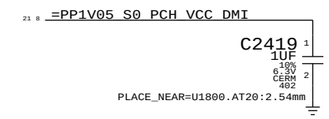

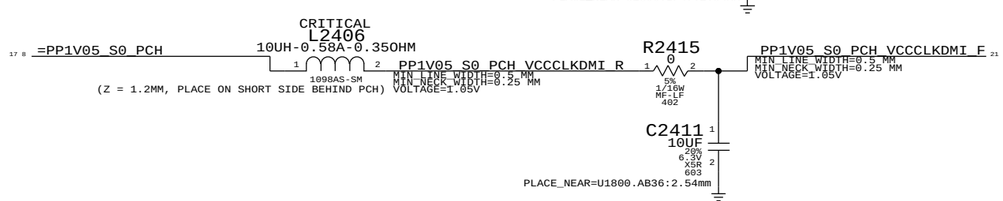

PCH VCCIO BYPASS

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

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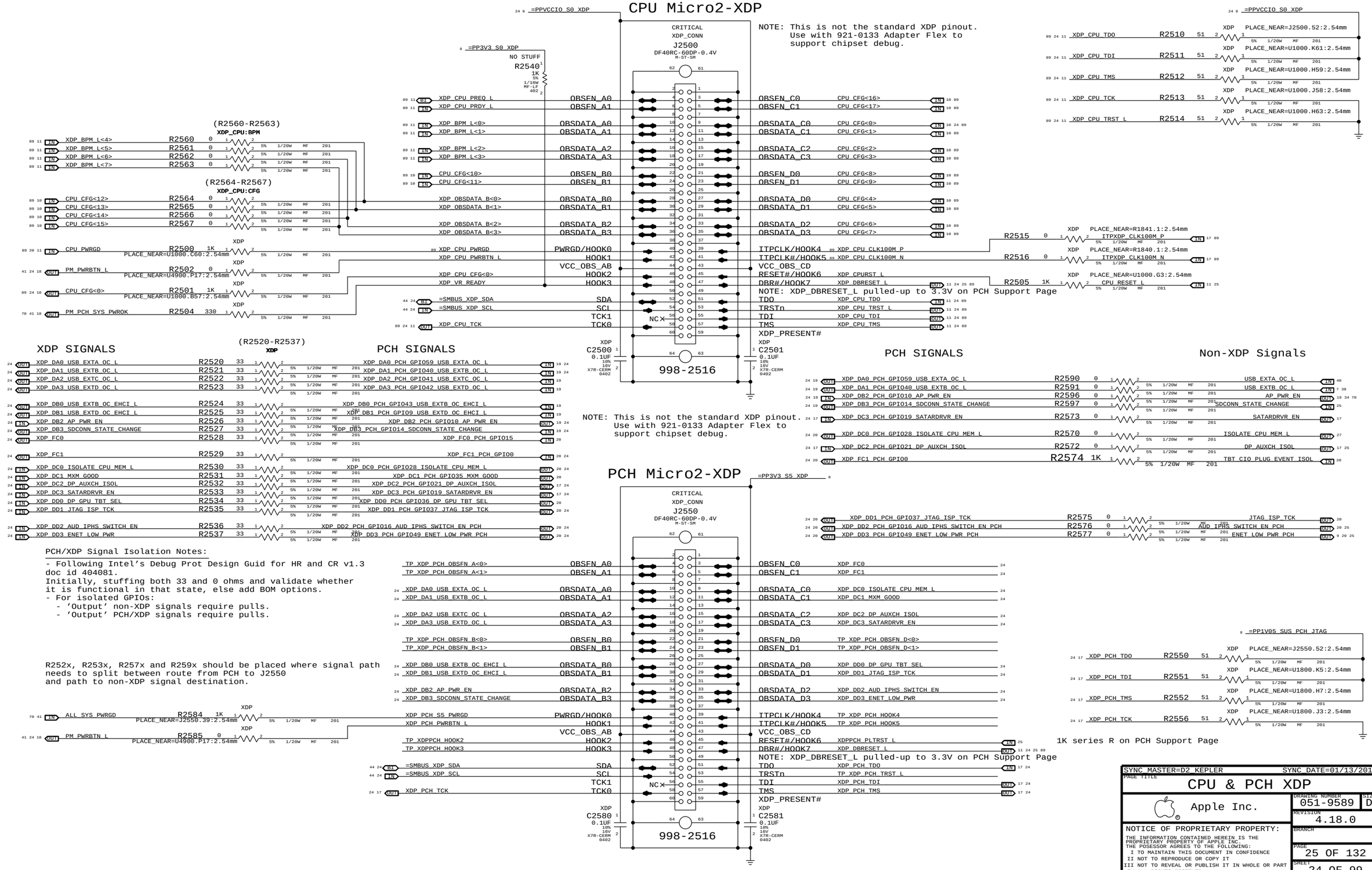
CPU Micro2-XDP



XDP SIGNALS

(R2520-R2537)

XDP

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC1_PCH_GPIO0	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH

Non-XDP Signals

PCH Micro2-XDP

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

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PAGE TITLE	CPU & PCH XDP		
Apple Inc.		DRAWING NUMBER	051-9589
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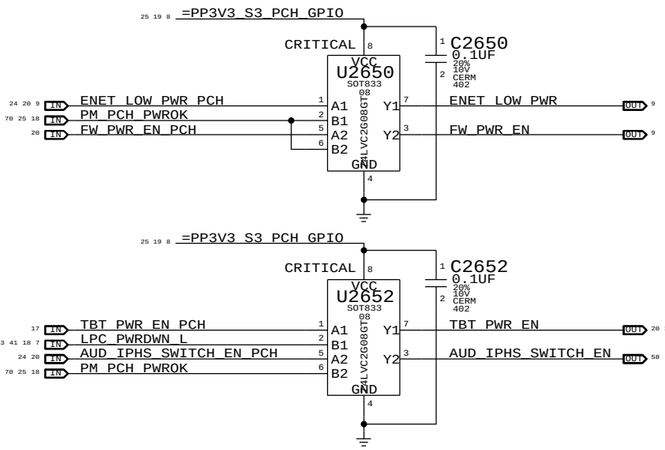
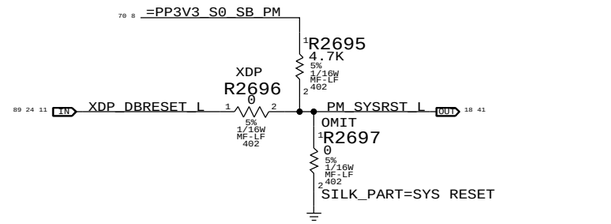
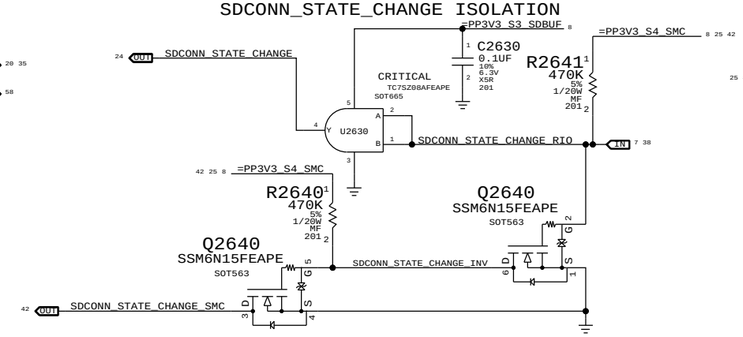
GPIO Glitch Prevention



PCH Reset Button

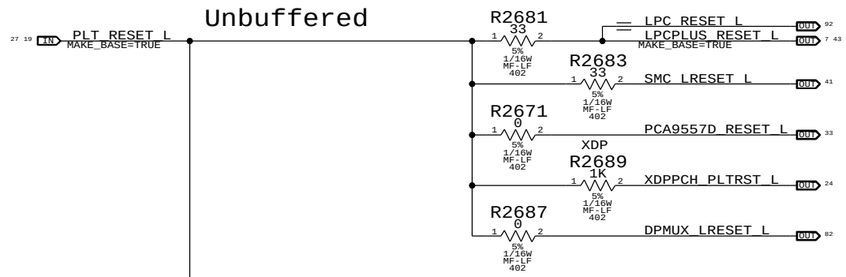


SDCONN_STATE_CHANGE ISOLATION

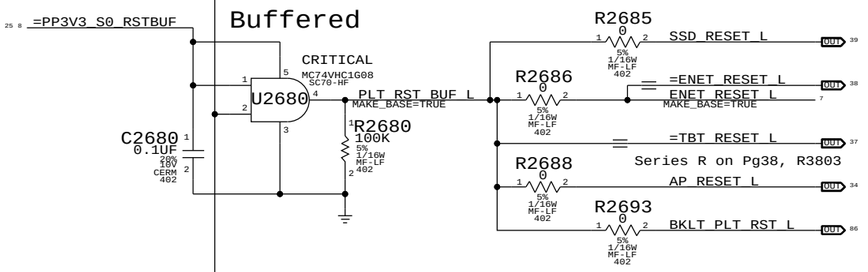


Platform Reset Connections

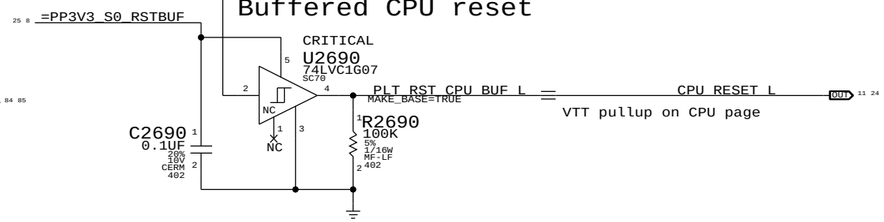
Unbuffered



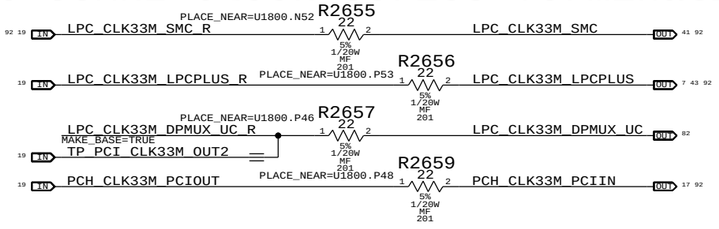
Buffered

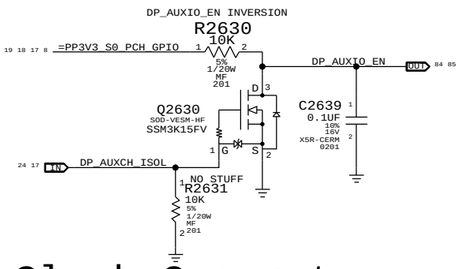


Buffered CPU reset



LPC 33MHz Clock Series Termination

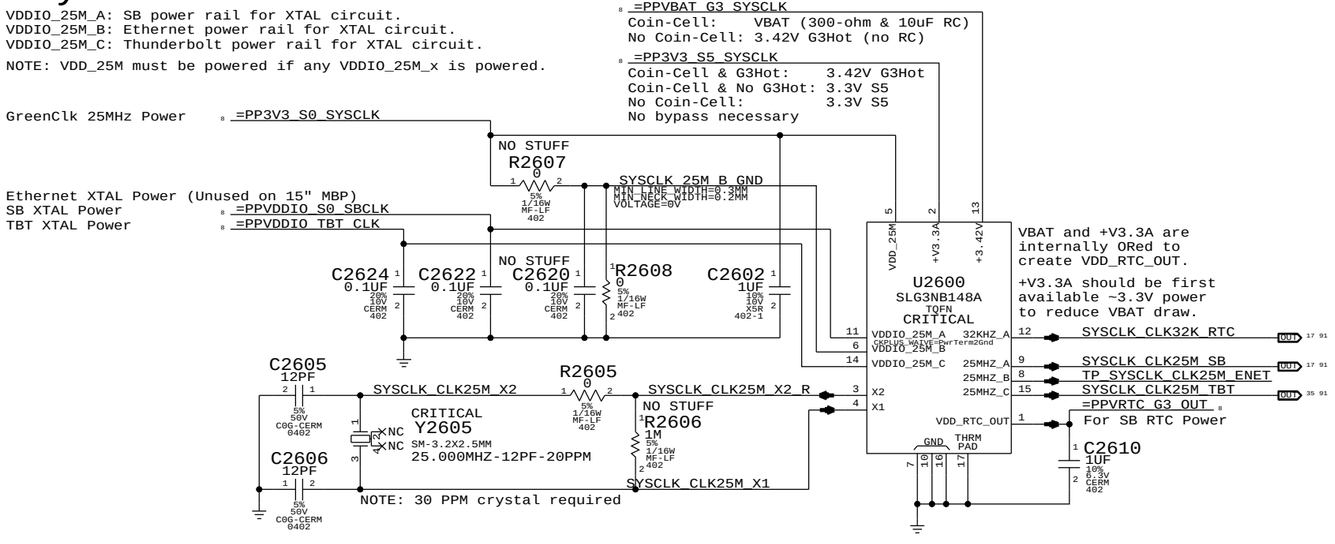




System RTC Power Source & 32kHz / 25MHz Clock Generator

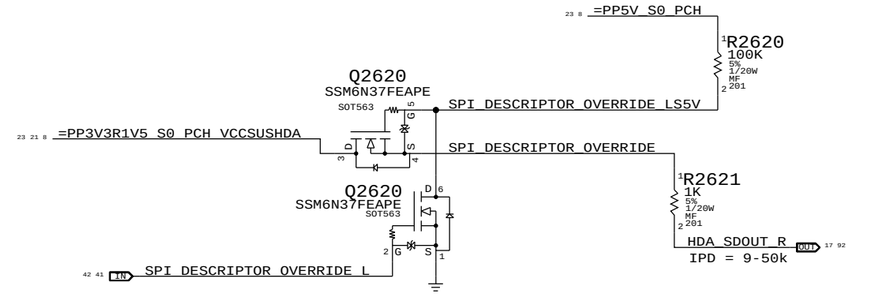
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

USB MUX FOR LS/FS INTERNAL DEVICES

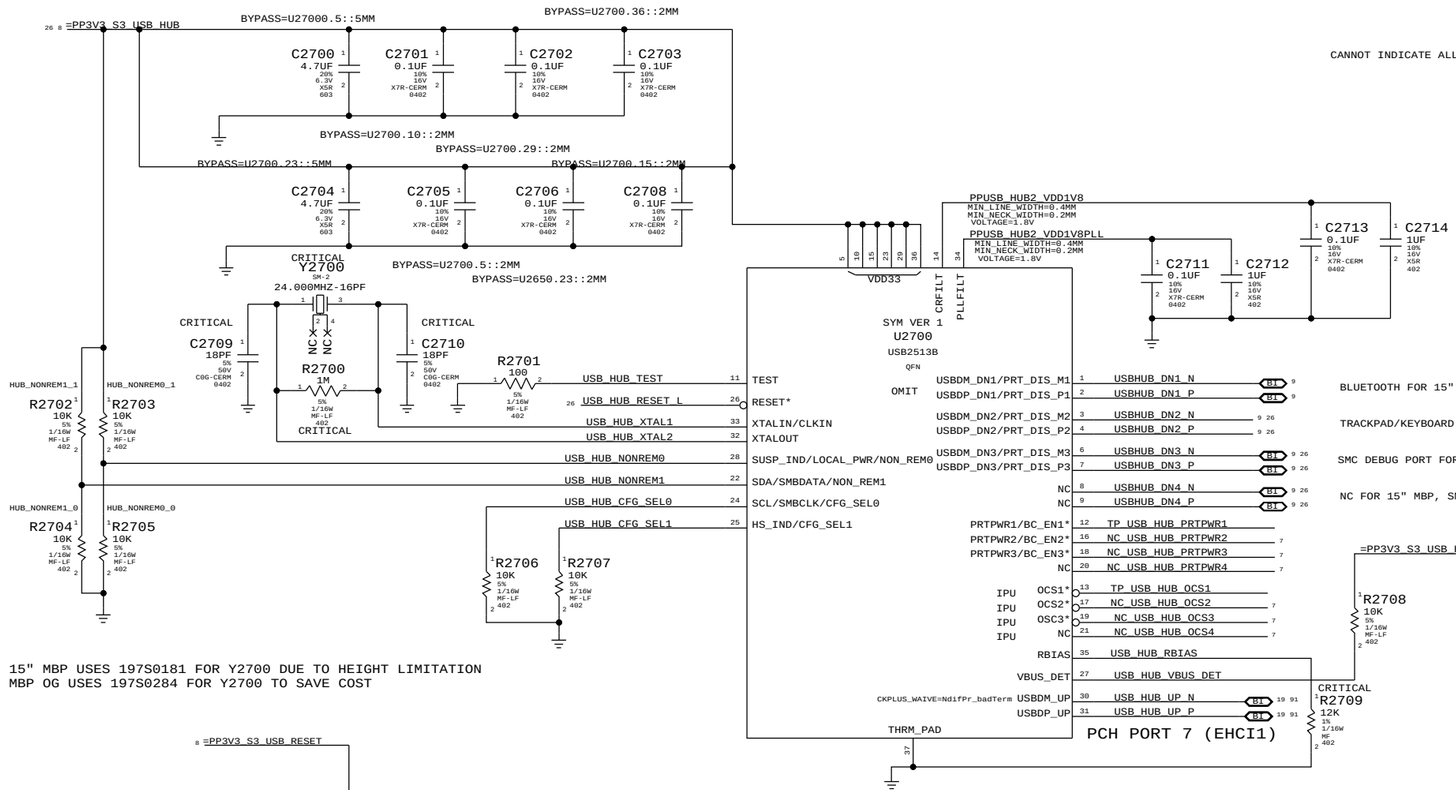
NON_REM 1 :	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

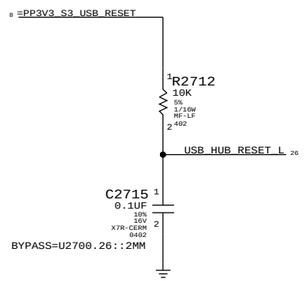
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

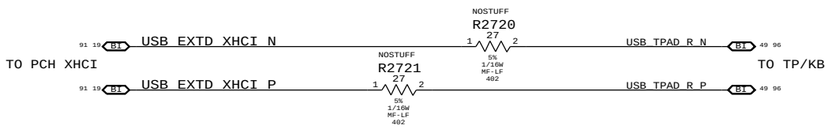
15" MBP ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
MBP OG ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



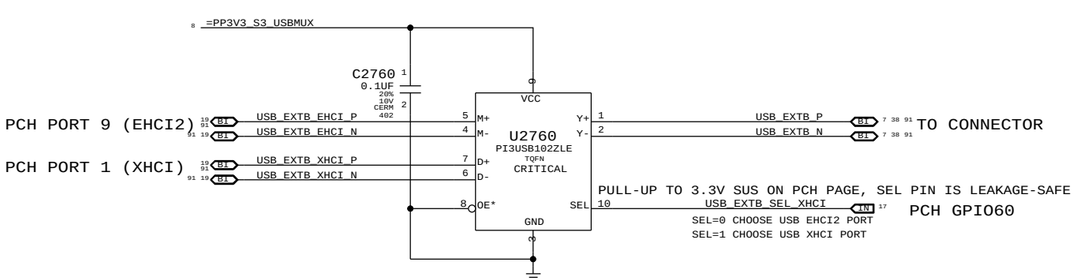
15" MBP USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
MBP OG USES 197S0284 FOR Y2700 TO SAVE COST



TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



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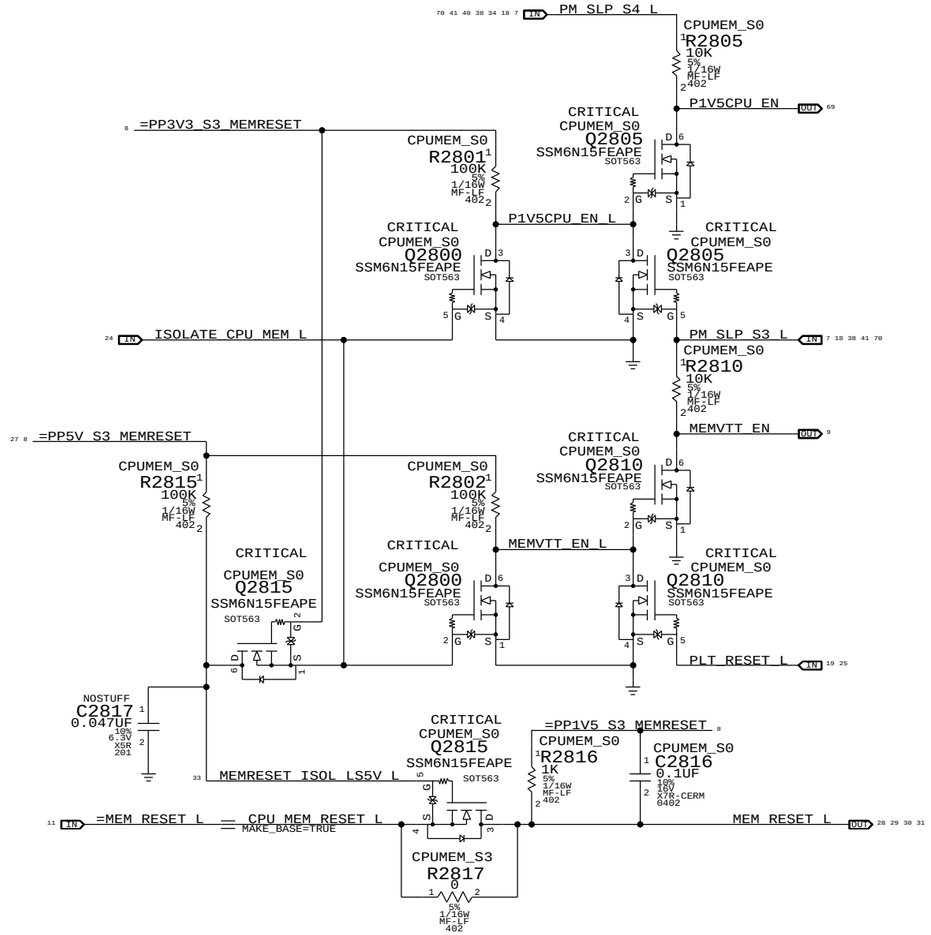
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



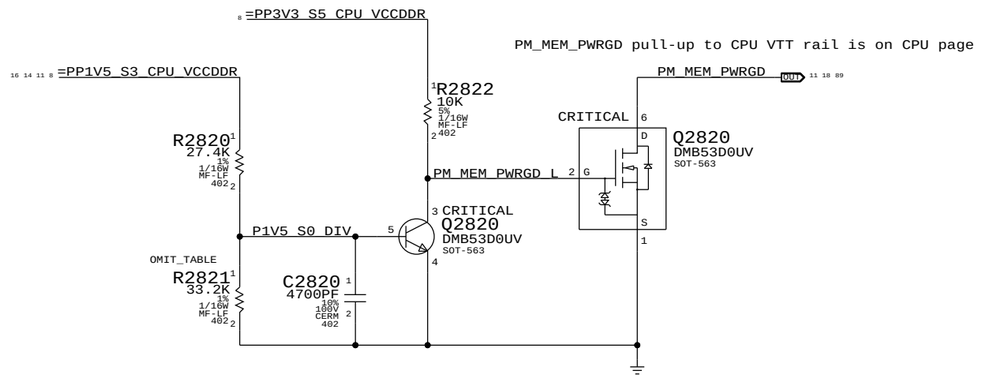
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
S3	2	0	0	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

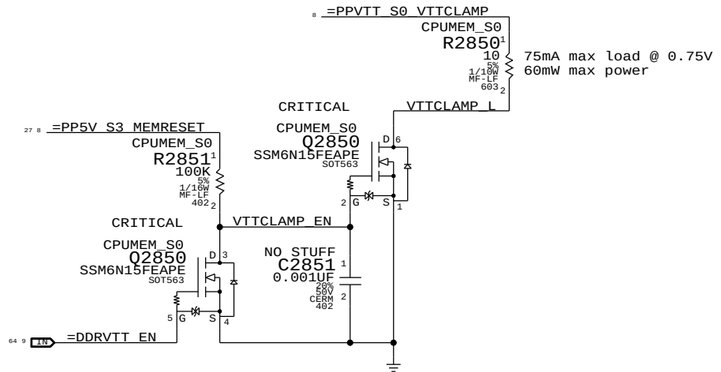
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0365	1	RES,MTL FILM,1/16W,33.2K,1,0402,SMD,LF	R2821		PPDDR:1V5
114S0376	1	RES,MTL FILM,1/16W,43.2K,1,0402,SMD,LF	R2821		PPDDR:1V35

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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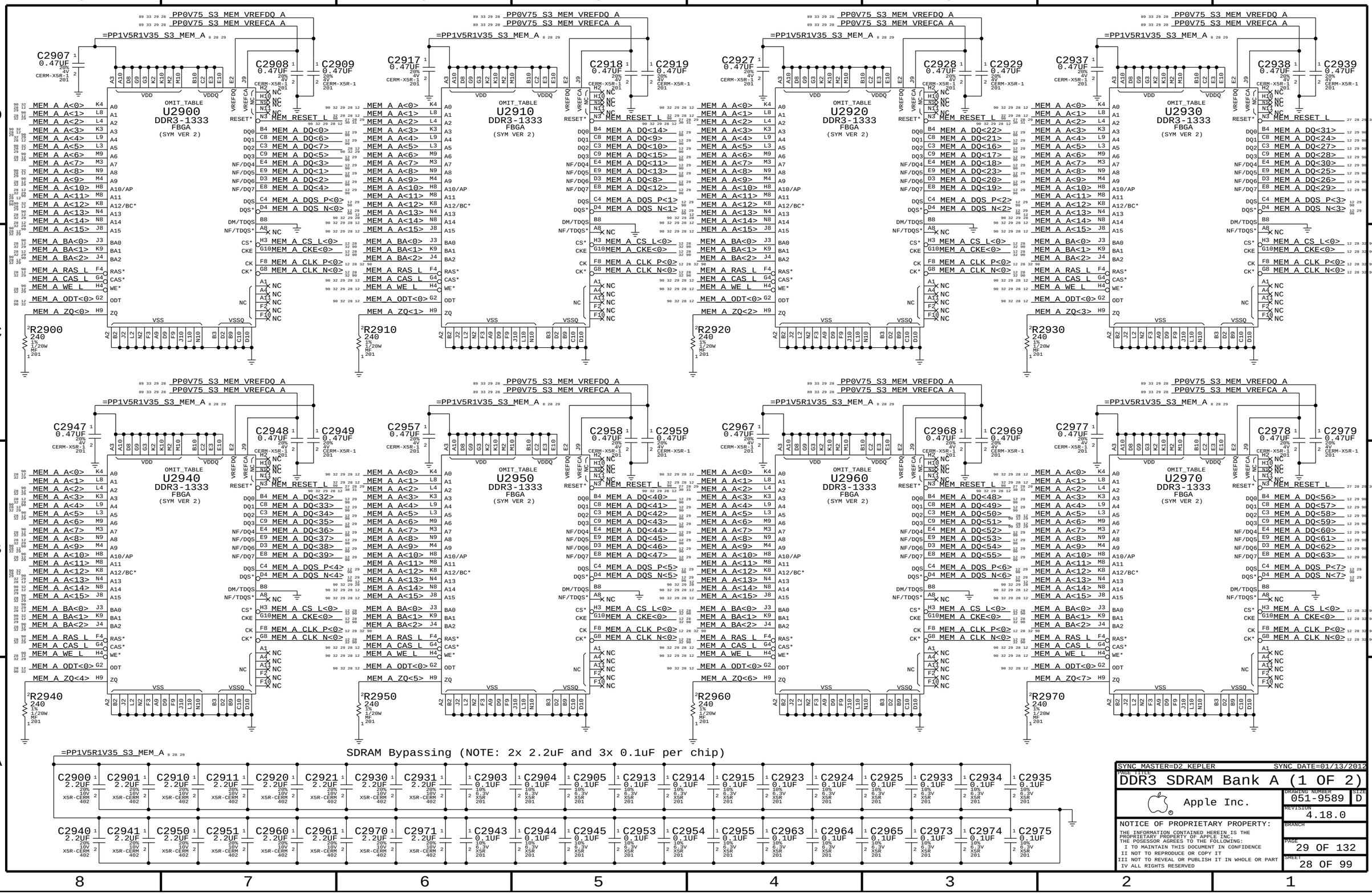
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PP0V75_S3_MEM_VREFCA_A
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C2909 0.47UF
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DDR3 SDRAM Bank A (1 OF 2)
Apple Inc.
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SIZE D
REVISION 4.18.0
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SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
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DDR3 SDRAM Bank A (2 OF 2)
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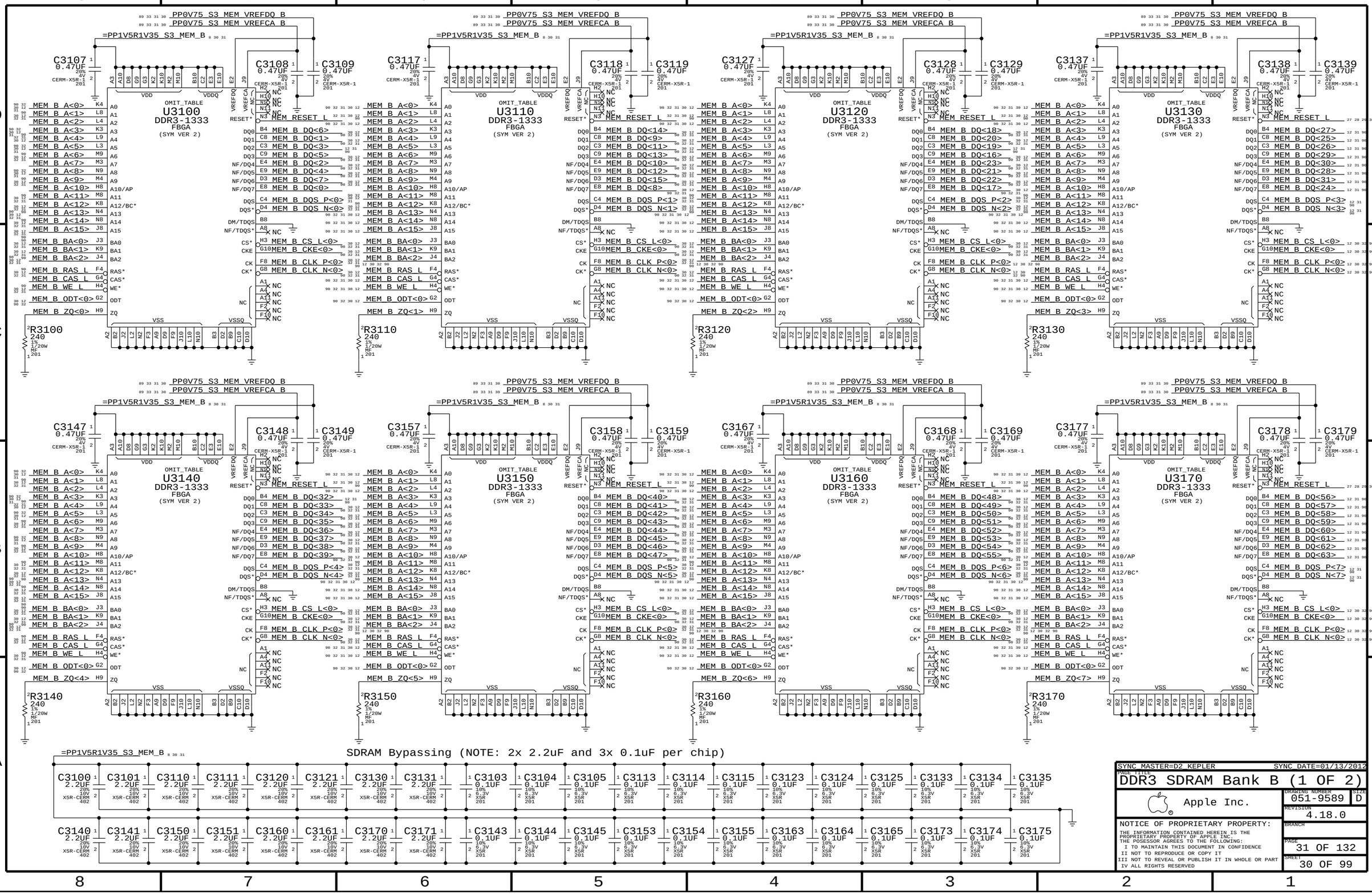

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

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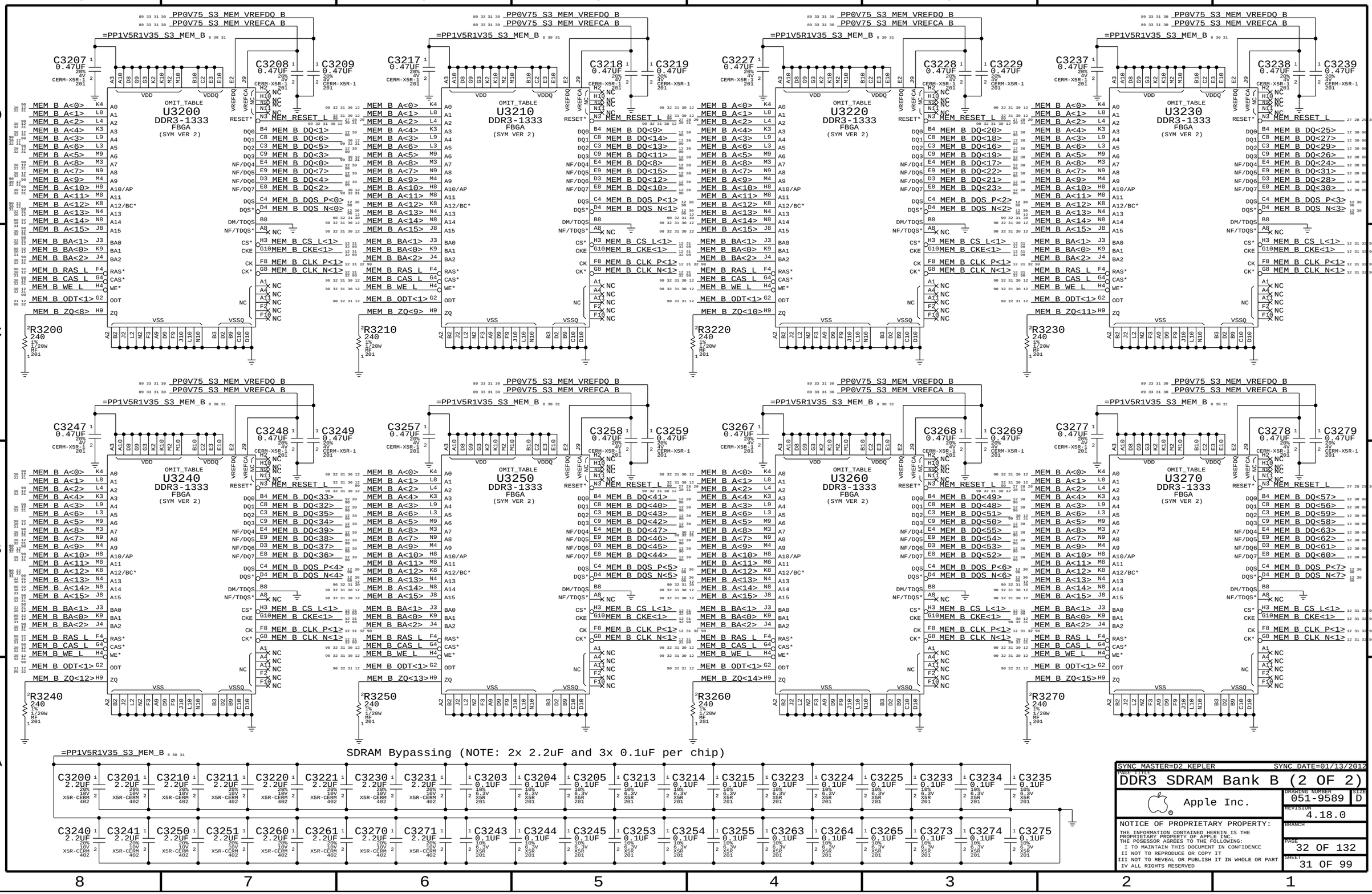

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

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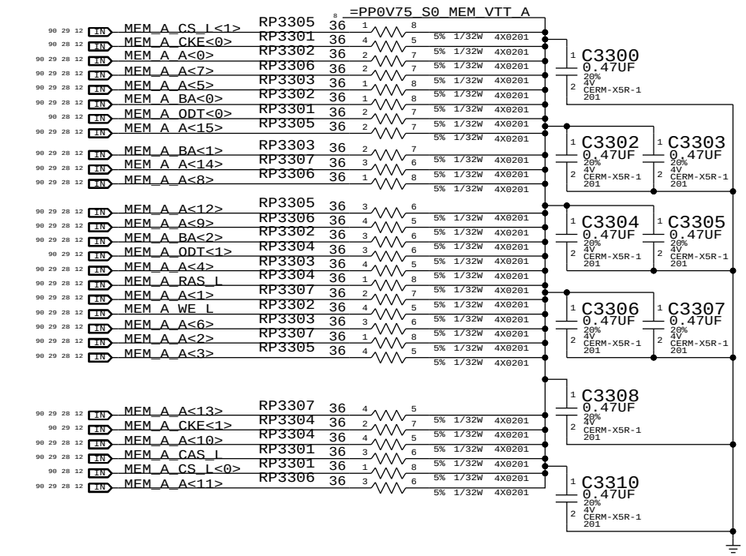
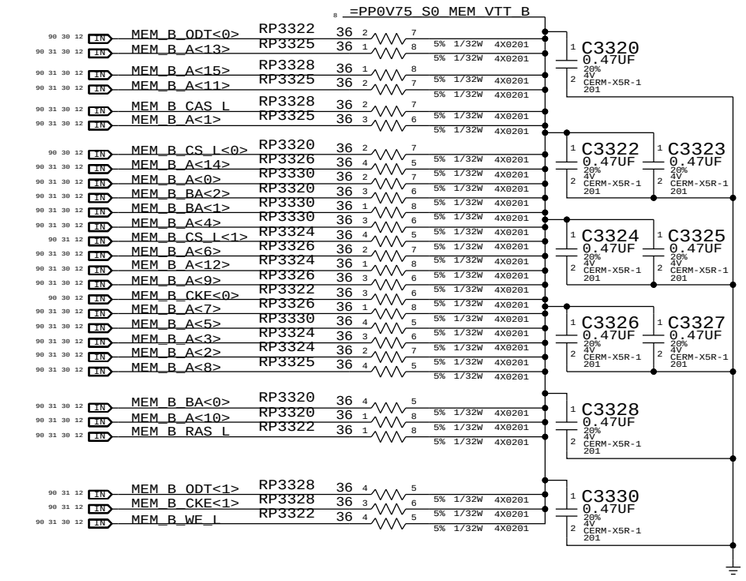
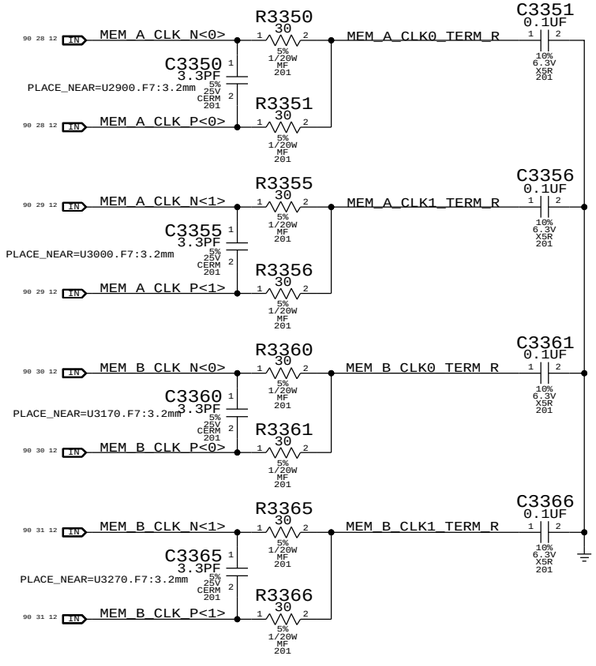
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3 Termination

Apple Inc.

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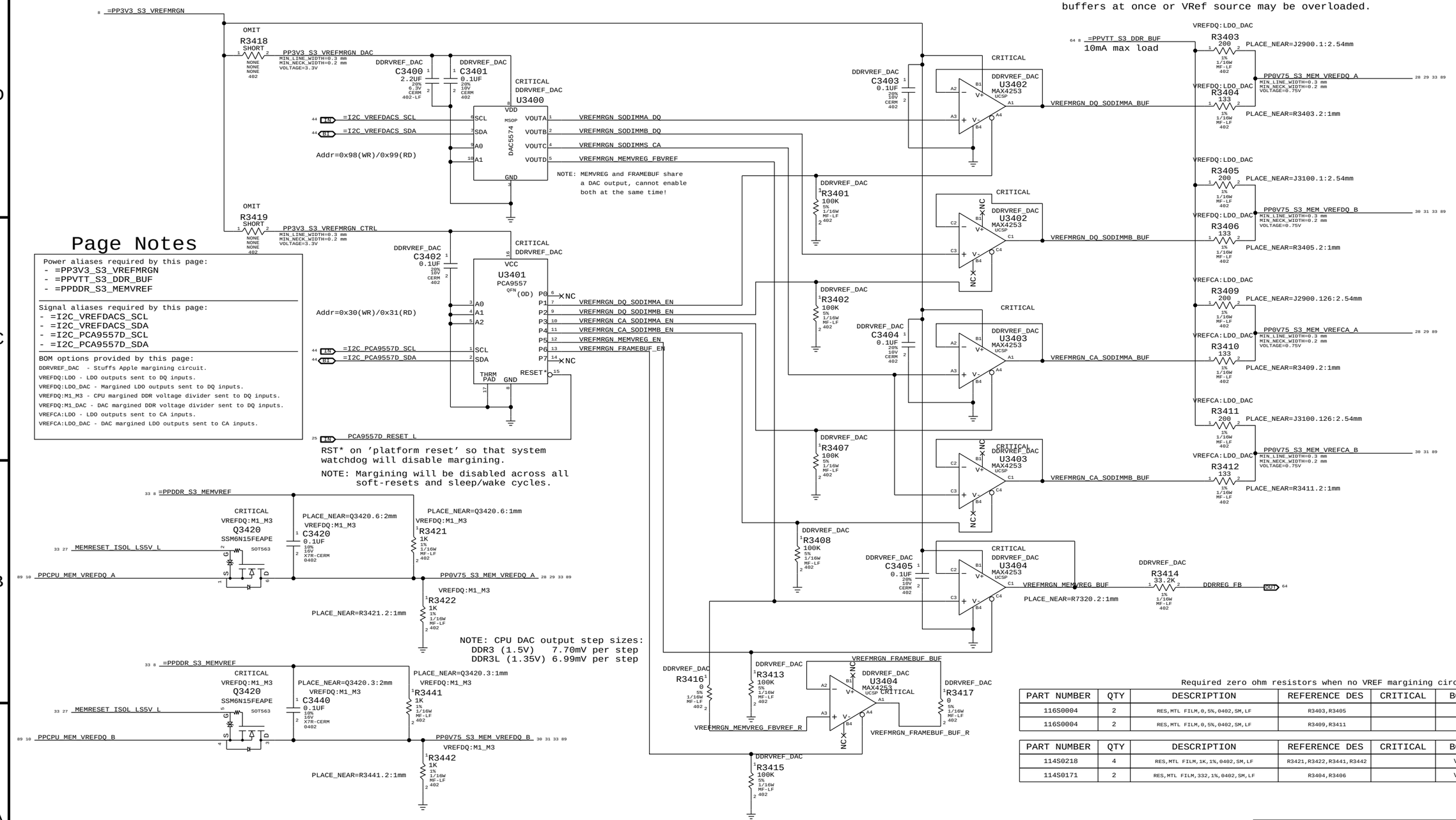

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 000HM, 0201	L3570,L3571,L3573,L3574		

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0767	1	CONN,HDR,TWIN:AX,P=0.4MM,GP,HF	J3502	CRITICAL	

OMIT_TABLE
L3570
0.6NH+/-0.1NH-0.85A
0201
92 PCIE_AP_R2D_PI_P
PLACE_NEAR=J3501.15:2.54MM
C3531 0.1UF 10% 16V X7R-CERM0402
PCIE_AP_R2D_C_P IN 17 92
NOSTUFF C3570 0.1UF 10% 16V XSR-CERM 0201
NOSTUFF C3571 0.1UF 10% 16V XSR-CERM 0201
L3571
0.6NH+/-0.1NH-0.85A
0201
92 PCIE_AP_R2D_PI_N
C3530 0.1UF 10% 16V X7R-CERM0402
PCIE_AP_R2D_C_N IN 17 92
WIFI_EVENT_L IN 7 41 42
OMIT_TABLE
NOSTUFF C3572 0.1UF 10% 16V XSR-CERM 0201
NOSTUFF C3573 0.1UF 10% 16V XSR-CERM 0201
PLACE_NEAR=J3501.17:2.54MM
OMIT_TABLE
L3573
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_P OUT 17 92
92 7 PCIE_AP_R2D_P
92 7 PCIE_AP_R2D_N
NOSTUFF C3574 0.1UF 10% 16V XSR-CERM 0201
NOSTUFF C3575 0.1UF 10% 16V XSR-CERM 0201
L3574
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_N OUT 17 92
OMIT_TABLE
NOSTUFF C3576 0.1UF 10% 16V XSR-CERM 0201
NOSTUFF C3577 0.1UF 10% 16V XSR-CERM 0201
92 7 PCIE_AP_D2R_PI_P
92 7 PCIE_AP_D2R_PI_N
CRITICAL
514S0335
J3501
SSD-K99
F-RT-SM1
AIRPORT
CRITICAL
L3501
90-OHM-100MA
DLP11S
SYM_VER-1
96 7 PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_P IN 17 92
96 7 PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_N IN 17 92
PLACE_NEAR=J3501.11:2.54MM
BLUETOOTH
PCIE_WAKE_L OUT 7 18
91 7 USB_BT_CONN_N
91 7 USB_BT_CONN_P
PP3V3_S3RS4_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3532 0.01UF 10% 16V X7R-CERM 0402
BTPWR:S4 L3505 =PP3V3_S4_BT 8
FERR-120-OHM-1.5A 0402-LF
PLACE_NEAR=J3501.27:2.54MM
BTPWR:S3 L3506 =PP3V3_S3_BT 8
FERR-120-OHM-1.5A 0402-LF
PLACE_NEAR=J3501.27:2.54MM
NOSTUFF R3517 15K 1% 1/20W MF 201
BTPWR:S3 R3518 0 5% 1/20W MF 201
NOSTUFF R3515 15K 1% 1/20W MF 201
NOSTUFF R3516 15K 1% 1/20W MF 201
PP3V3_S3RS4_BT_F 7 34
C3510 0.1UF 10% 6.3V X5R 201
U3510 PI3USB102ZLE TQFN CRITICAL
VCC
SEL
GND
USB_BT_WAKE_P
USB_BT_WAKE_N
USB_BT_P BI 9 91
USB_BT_N BI 9 91
NOSTUFF R3514 15K 1% 1/20W MF 201
BTPWR:S4 R3512 15K 1% 1/20W MF 201
NOSTUFF R3513 15K 1% 1/20W MF 201
SIGNAL_MODEL=EMPTY
BTPWR:S4
Q3510
SSM3K15FV
SOD-VESM-HF
=BT_WAKE_L OUT 42
BTPWR:S4 R3511 0 5% 1/20W MF 201
PM_SLP_S4_L IN
BTMUX_SEL
NOSTUFF C3511 0.01UF 10% 16V X7R-CERM 0402
SEL | OUTPUT
L | USB_BT_WAKE
H | USB_BT
Supervisor & CLKFREG # Isolation
Delay = 130 ms +/- 20%
PP3V3_WLAN_F 34 99
=PP3V3_S3_WLAN 8 34
R3553 100K 1% 1/16W MF-LF 402
R3554 232K 1% 1/16W MF-LF 402
P3V3WLAN_VMON
CRITICAL
U3540
SLG4AP041V
TDFN
VDD
SENSE
VREF
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND
C3540 0.1uF 20% 10V CERM 402
AP_RESET_L IN 25
AP_PWR_EN IN 19 24 70
AP_CLKREQ_L OUT 17
R3555 100K 1% 1/16W MF-LF 402
7 AP_RESET_CONN_L
7 AP_CLKREQ_Q_L
OMIT
CRITICAL
J3502
CCR20-6K710S
F-RT-SM
=I2C_ALS_SDA BI 44
=I2C_ALS_SCL IN 44
7 PP5V_S3_ALSCAMERA_F
91 7 USB_CAMERA_CONN_N
91 7 USB_CAMERA_CONN_P
ALS
CAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
CRITICAL
L3507
90-OHM
DLP0NS
SYM_VER-1
USB_CAMERA_N BI 19 91
USB_CAMERA_P BI 19 91
PLACE_NEAR=J3502.3:2.54MM
275 mA peak
206 mA nominal max
PLACE_NEAR=J3502.6:2.54MM
L3508
FERR-120-OHM-1.5A
0402-LF
=PP5V_S3_ALSCAMERA 8
C3552 0.1uF 20% 10V CERM 402
3V S3 WLAN FET
MOSFET | DMP2018LFK
CHANNEL | P-TYPE
RDS(ON) @ 2.5V | 14 mOhm Typ 20 mOhm Max
LOADING | 1 A (EDP)
CRITICAL
Q3550
DMP2018LFK
DFN2563-6
CURRENT SENSE
155S0367
L3504
FERR-120-OHM-3A
1A PEAK
0603
42 7 PP3V3_WLAN
PP3V3_WLAN_F IN 34 99
PP3V3_WLAN_R OUT
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
C3522 0.1uF 20% 10V CERM 402
C3521 0.1uF 20% 10V CERM 402
PLACE_NEAR=J3501.29:2.54MM
PLACE_NEAR=J3501.29:2.54MM
=PP3V3_S3_WLAN 8 34
C3551 0.033UF 10% 16V X5R 402
R3551 10K 5% 1/16W MF-LF 402
C3550 0.1UF 10% 16V X7R-CERM 0402
P3V3WLAN_SS
R3550 33K 5% 1/16W MF-LF 402
PM_WLAN_EN_L IN 70

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE: X29/ALS/CAMERA CONNECTOR	
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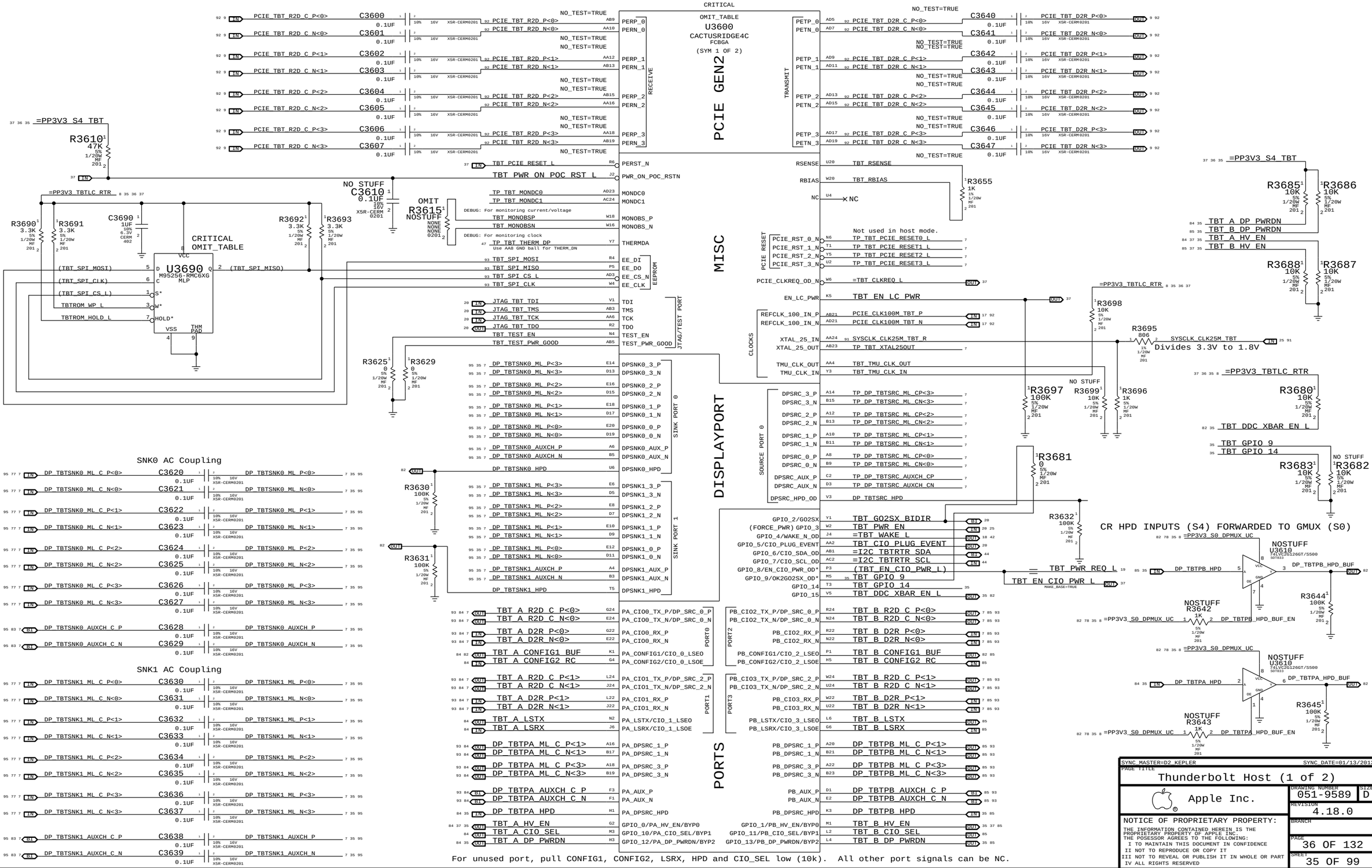
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
CRITICAL
OMIT_TABLE
PCIE GEN2
MISC
DISPLAYPORT
PORTS
U3690
M95256-RMC6XG
MLP
U3610
74LVC2G126GT/S500
SOT833
=PP3V3_S4_TBT
=PP3V3_TBTLC_RTR
=PP3V3_S0_DPMUX_UC
Divides 3.3V to 1.8V
CR HPD INPUTS (S4) FORWARDED TO GMUX (S0)
SNK0 AC Coupling
SNK1 AC Coupling
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
Apple Inc.
Thunderbolt Host (1 of 2)
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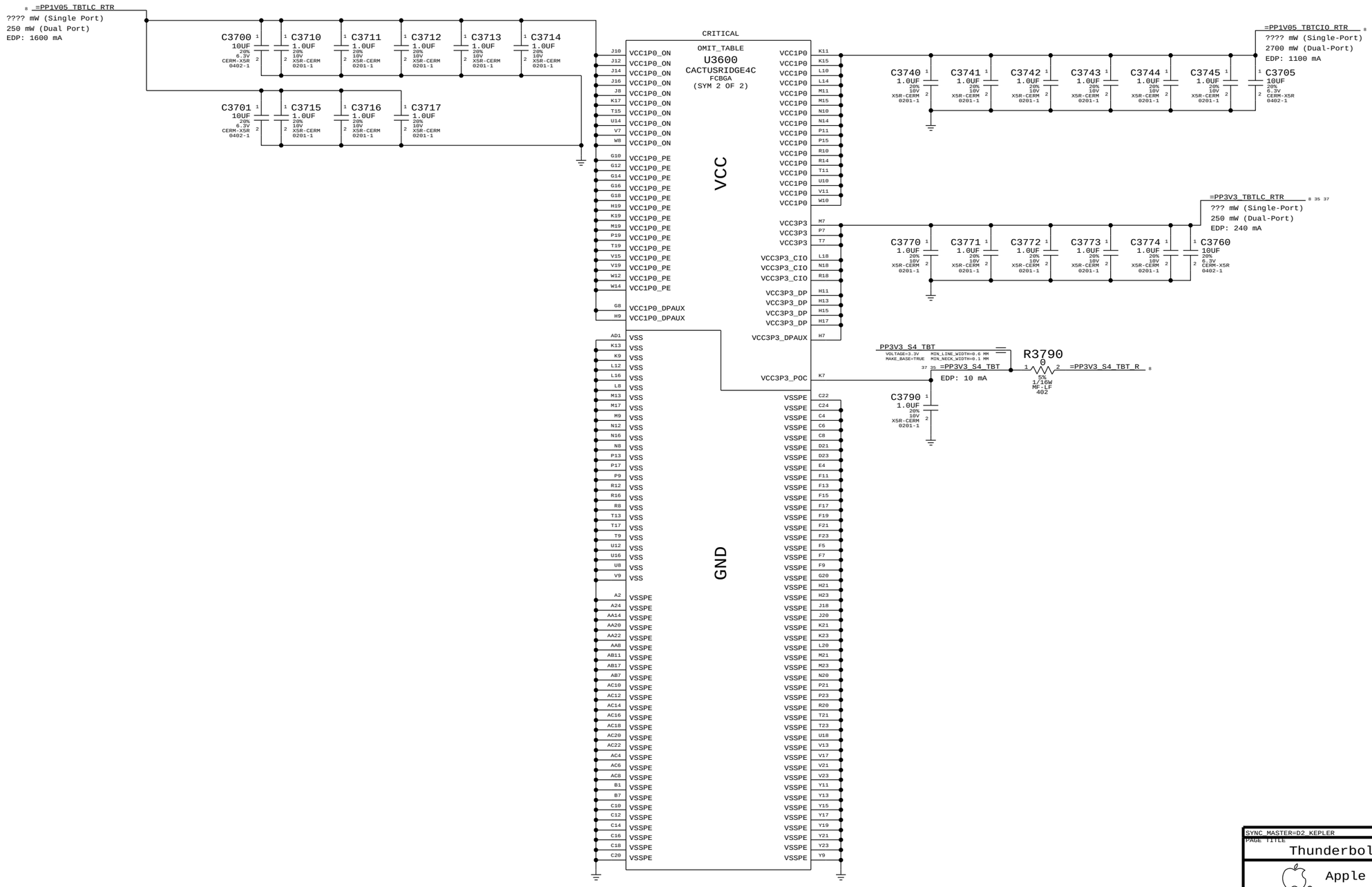

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Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL TBTBST:Y Q3880 SI8409DB 8GA

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 16V X5R-CERM 402
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 1% 1/16W MF-LF 402
TBTBST_PWREN_L

TBTBST:Y C3860 10UF 20% 25V X5R-CERM 0603
TBTBST:Y C3861 10UF 20% 25V X5R-CERM 0603
TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>

CRITICAL TBTBST:Y L3895 3.3UH-6.5A PIMB063T-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIOT=TRUE

CRITICAL TBTBST:Y U3890 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

TBTBST:Y C3890 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3891 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3892 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3887 68PF 5% 50V C0G-CERM 0402
TBTBST:Y R3893 49.9K 1% 1/16W MF-LF 402
TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3893 0.0033UF 10% 50V X7R-CERM 0402
TBTBST:Y R3894 28.7K 1% 1/16W MF-LF 402
TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX
NC
SGND
GND

TBTBST:Y R3889 0 5% 1/20W MF 201
CRITICAL TBTBST:Y D3895 PDS540XF PWRDI5
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
TBTBST:Y C3888 10PF 5% 50V C0G-CERM 0402
TBTBST:Y R3895 137K 1% 1/16W MF-LF 402 <Ra>
NO STUFF C3889 100PF 5% 50V CERM 402
TBTBST:Y R3896 15.8K 1% 1/16W MF-LF 402 <Rb>
TBTBST:Y C3895 10UF 10% 25V X5R 1206-2
TBTBST:Y C3896 20% 25V POLY-TANT CASE-D3L
NO STUFF C3897 10UF 10% 25V X5R 805

=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 300KHz
TBTBST:Y C3899 0.001UF 10% 50V X7R-CERM 0402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

33UF-0.060HM

TBT_A_HV_EN
TBT_B_HV_EN

TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBTBST:Y Q3805 SSM6N37FEAPE SOT563

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
Q3840 SSM3K15FV SOD-VESM-HF
C3800 0.1UF 10% 16V X5R-CERM 0201
R3840 10K 5% 1/20W MF 201
TBT_EN_LC_PWR
Platform (PCIe) Reset
=TBT_RESET_L
TBT_CLKREQ_L
Pull-ups provided by SB page.

CRITICAL U3800 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
THRM PAD
GND

=PP3V3_TBTLC_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
U3810 TPS22924 CSP
VIN VOUT ON CRITICAL GND
R3811 36.5K 1% 1/20W MF 201
C3810 1UF 20% 6.3V X5R 0201
C3811 1UF 10% 6.3V CERM 402
TBT_EN_LC_3V3
=PP3V3_TBTLC_FET
Max Current = 2A (85C)

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

TBT_EN_LC_ISOL
R3816 0 5% 1/20W MF 201
TBT_EN_LC_1V05

1.05V TBT "LC" Switch

=PP1V05_S0_P1V05TBTFET
U3815 TPS22924 CSP
VIN VOUT ON CRITICAL GND
C3815 1UF 20% 6.3V X5R 0201
NOSTUFF C3816 1UF 10% 6.3V CERM 402
C3816 must be 10%
RC guarantees minimum 5ms to reach 0.5V
=PP1V05_TBTLC_FET
Max Current = 2A (85C)

U3815

Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
TBTBST:Y R3888 330K 5% 1/10W MF-LF 402
Max Vgs: 10V
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K 5% 1/10W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
CRITICAL
U3830 TPS3808 QFN
VDD SENSE RESET* CT MR* GND THRM PAD
Pull-up: R3610
TBTPOCRST_CT
C3831 0.0047UF 10% 25V CERM 0402
C3830 0.1UF 10% 25V X5R 402
TBTPOCRST_MR_L
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
TBT_PWR_ON_POC_RST_L
Q3825 SSM6N37FEAPE SOT563
C3825 330PF 10% 16V X7R-CERM 0201
=PP3V3_S0_PCH_GPIO
R3830 100K 5% 1/20W MF 201
TBT_SW_RESET_L

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTFET
=PP3V3_TBTLC_RTR
U3820 TPS22920 CSP
VIN VOUT ON CRITICAL GND
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
C3820 1UF 20% 6.3V X5R 0201
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

Q3825 SSM6N37FEAPE SOT563
TBT_EN_CIO_PWR_L

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012
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516S0853

J4410
AXK732327G
F-ST-SM

25	IN	=ENET_RESET_L	1	2	PM_SLP_S3_L	IN	7 18 27 41 70
17 7	OUT	ENET_CLKREQ_L	3	4	PM_SLP_S4_L	IN	7 18 27 34 40 41 70
9 7	IN	SD_PWR_EN	5	6	HDMI_EG_DDC_CLK	IN	7 77
25 7	OUT	SDCONN_STATE_CHANGE_RIO	7	8	HDMI_EG_DDC_DATA	BI	7 77
24 7	OUT	USB_EXTB_OC_L	9	10	HDMI_HPD_L	OUT	7 42 82
8		=PP1V5_S0_RIO	11	12			
8		=PP3V3_S3_RIO	13	14			
			15	16			
			17	18			
8		=PP3V3_S4_RIO	19	20			
44		=I2C_HDMIRDRV_SCL	21	22			
44		=I2C_HDMIRDRV_SDA	23	24			
			25	26			
			27	28			
8		=PP5V_S4_RIO	29	30			
			31	32			

33 (GND) — 34 (GND)

SIGNAL_MODEL=EMPTY
BP4401 BEAD-PROBE SM
BP4402 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY

91 19 7 IN USB3_EXTB_TX_P — C4402 0.1UF X5R-CERM 0201 10% 16V — C4401 0.1UF X5R-CERM 0201 10% 16V — USB3_EXTB_TX_C_P 97 7
91 19 7 IN USB3_EXTB_TX_N — GND_VOID=TRUE — GND_VOID=TRUE — USB3_EXTB_TX_C_N 97 7
91 19 7 OUT USB3_EXTB_RX_P — 12 R4403 1/20W 1% MF 201 GND_VOID=TRUE — 15PF 5% 25V NP0-CERM 0201 C4403 GND_VOID=TRUE — USB3_EXTB_RX_RC_P 97
91 19 7 OUT USB3_EXTB_RX_N — 12 R4404 1/20W 1% MF 201 GND_VOID=TRUE — 15PF 5% 25V NP0-CERM 0201 C4404 GND_VOID=TRUE — USB3_EXTB_RX_RC_N 97

SIGNAL_MODEL=EMPTY
BP4405 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY
BP4406 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY
BP4403 BEAD-PROBE SM
BP4404 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY

91 26 7 BI USB_EXTB_P
91 26 7 BI USB_EXTB_N

95 77 7 IN HDMI_EG_DATA_C_P<0>
95 77 7 IN HDMI_EG_DATA_C_N<0>
95 77 7 IN HDMI_EG_DATA_C_P<1>
95 77 7 IN HDMI_EG_DATA_C_N<1>
95 77 7 IN HDMI_EG_DATA_C_P<2>
95 77 7 IN HDMI_EG_DATA_C_N<2>
95 77 7 IN HDMI_EG_CLK_C_P
95 77 7 IN HDMI_EG_CLK_C_N

92 17 7 IN PCIE_CLK100M_ENET_P
92 17 7 IN PCIE_CLK100M_ENET_N
92 17 7 OUT PCIE_ENET_D2R_P
92 17 7 OUT PCIE_ENET_D2R_N
92 17 7 IN PCIE_ENET_R2D_C_P
92 17 7 IN PCIE_ENET_R2D_C_N

J4400
20525-130E-01
F-RT-SM

31			
1	91 26 7 BI	USB_EXTB_P	
2	91 26 7 BI	USB_EXTB_N	
3			
4	97 7	USB3_EXTB_TX_C_P	GND_VOID=TRUE
5	97 7	USB3_EXTB_TX_C_N	GND_VOID=TRUE
6			
7	97	USB3_EXTB_RX_RC_P	GND_VOID=TRUE
8	97	USB3_EXTB_RX_RC_N	GND_VOID=TRUE
9			
10	95 77 7 IN	HDMI_EG_DATA_C_P<0>	GND_VOID=TRUE
11	95 77 7 IN	HDMI_EG_DATA_C_N<0>	GND_VOID=TRUE
12			
13	95 77 7 IN	HDMI_EG_DATA_C_P<1>	GND_VOID=TRUE
14	95 77 7 IN	HDMI_EG_DATA_C_N<1>	GND_VOID=TRUE
15			
16	95 77 7 IN	HDMI_EG_DATA_C_P<2>	GND_VOID=TRUE
17	95 77 7 IN	HDMI_EG_DATA_C_N<2>	GND_VOID=TRUE
18			
19	95 77 7 IN	HDMI_EG_CLK_C_P	
20	95 77 7 IN	HDMI_EG_CLK_C_N	
21			
22	92 17 7 IN	PCIE_CLK100M_ENET_P	
23	92 17 7 IN	PCIE_CLK100M_ENET_N	
24			
25	92 17 7 OUT	PCIE_ENET_D2R_P	GND_VOID=TRUE
26	92 17 7 OUT	PCIE_ENET_D2R_N	GND_VOID=TRUE
27			
28	92 17 7 IN	PCIE_ENET_R2D_C_P	GND_VOID=TRUE
29	92 17 7 IN	PCIE_ENET_R2D_C_N	GND_VOID=TRUE
30			
33			
34			
35			
36			
37			
38			
39			
40			
41			
32			

518S0829

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
RIO CONNECTOR

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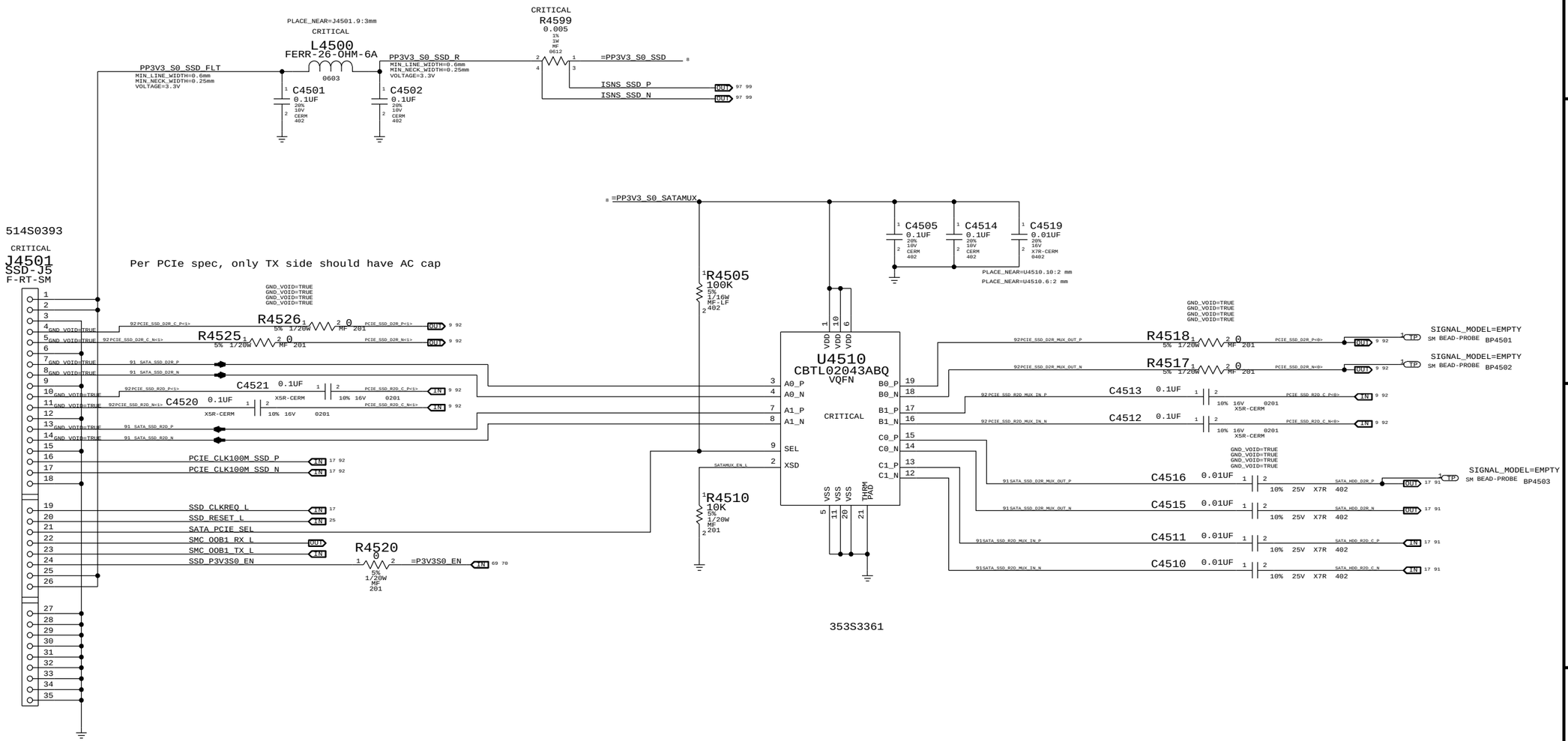

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	SSD CONNECTOR
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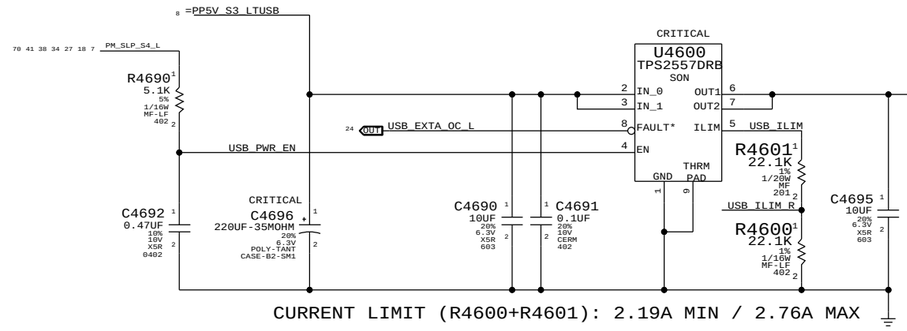
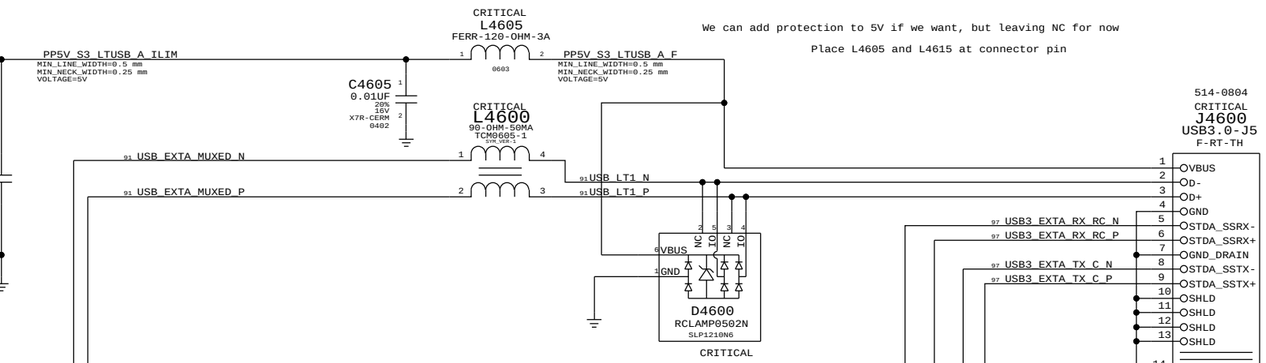
USB Port Power Switch



CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

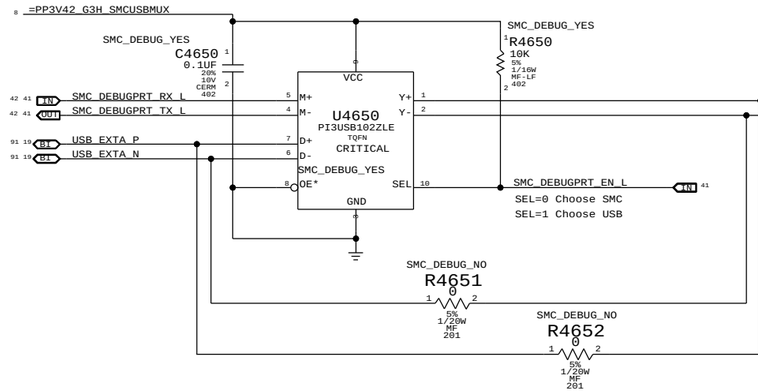
Left USB Port A

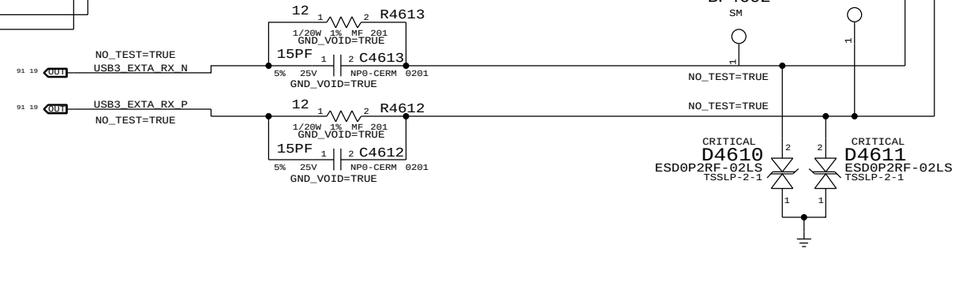


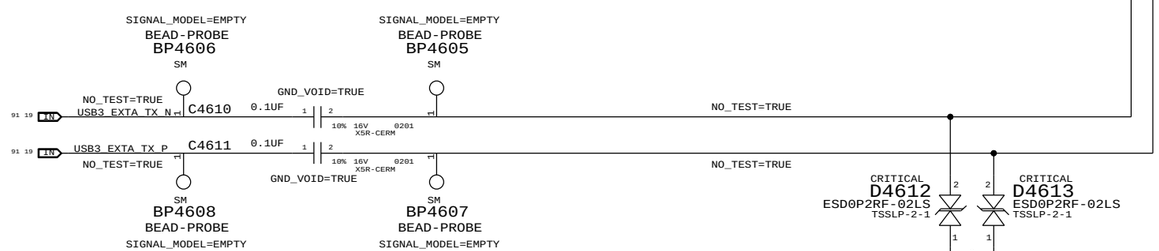
We can add protection to 5V if we want, but leaving NC for now

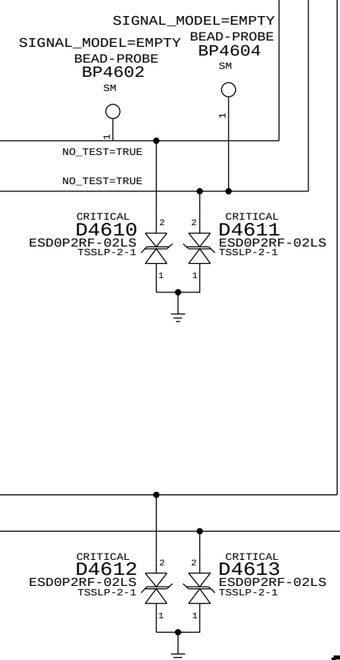
Place L4605 and L4615 at connector pin

USB/SMC Debug Mux









SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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USB 3.0 CONNECTORS

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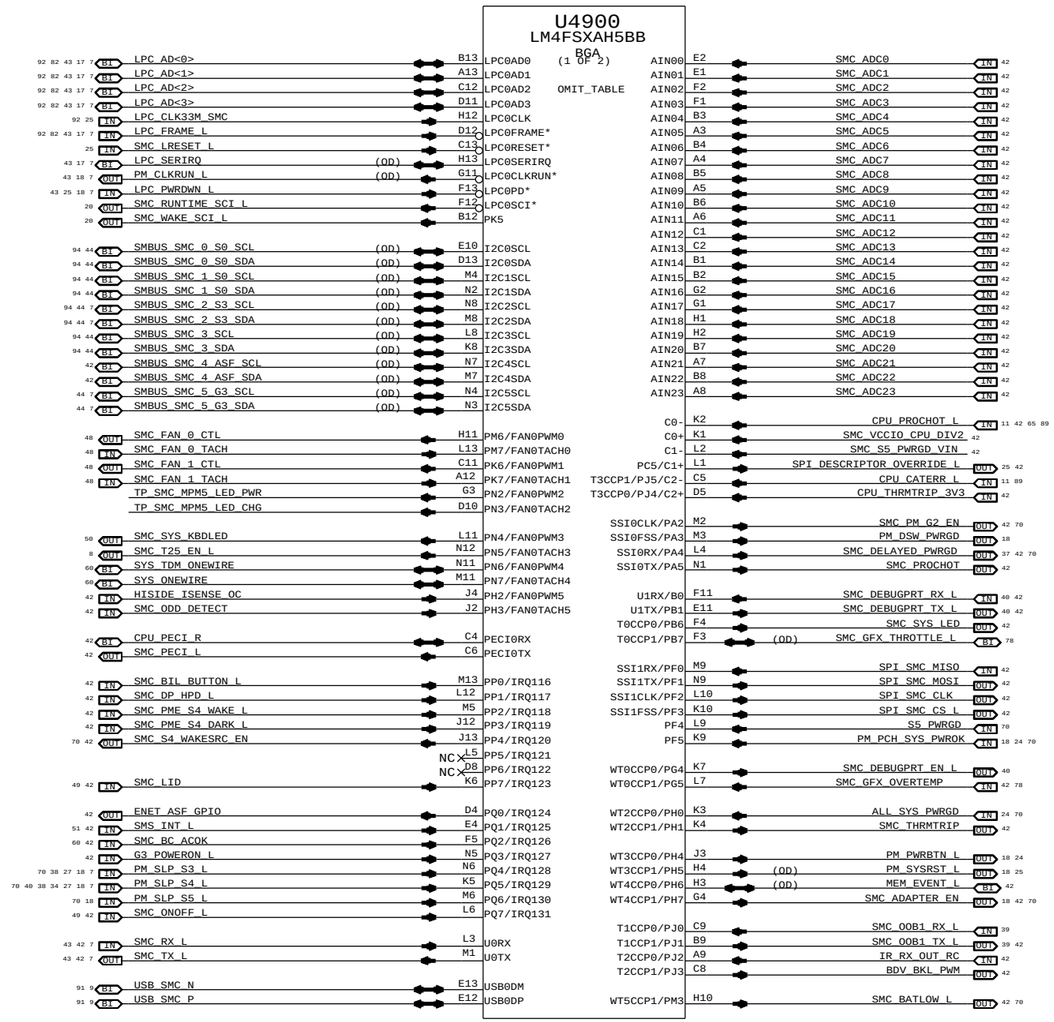
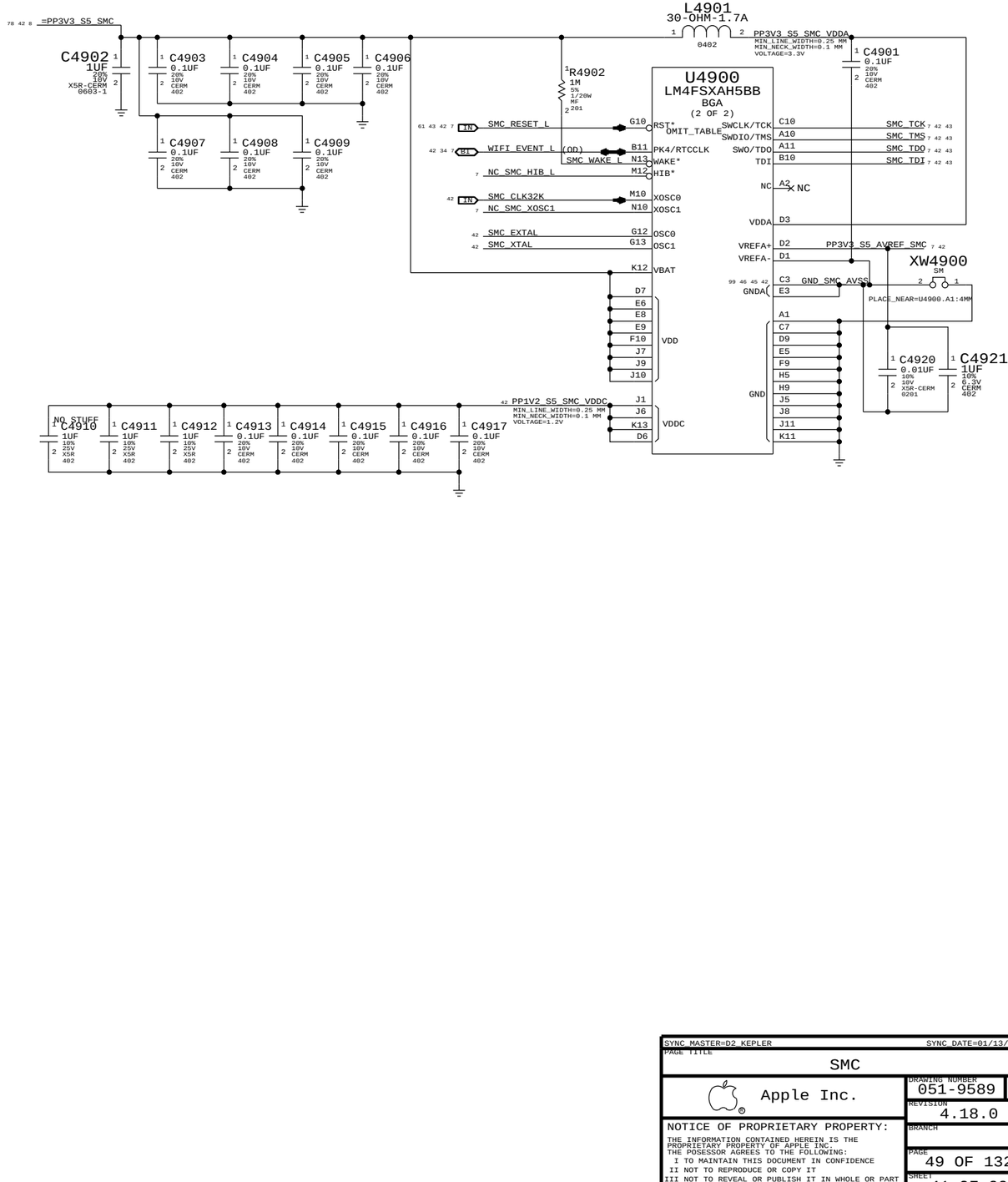
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



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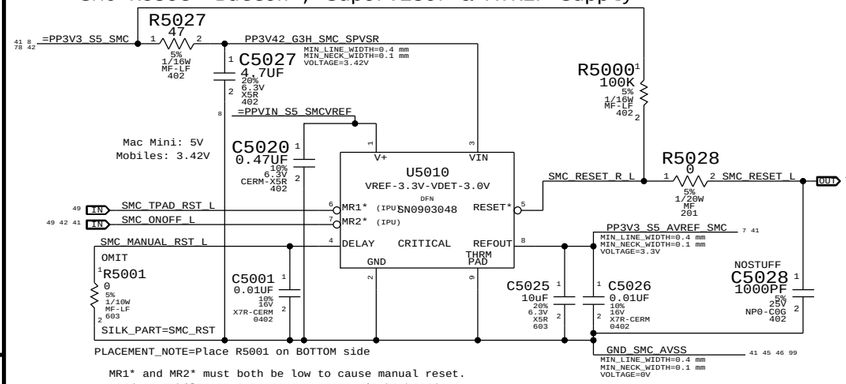
SMC Reset "Button", Supervisor & AVREF Supply

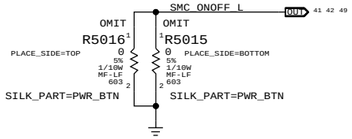


PLACEMENT_NOTE=Place R5001 on BOTTOM side

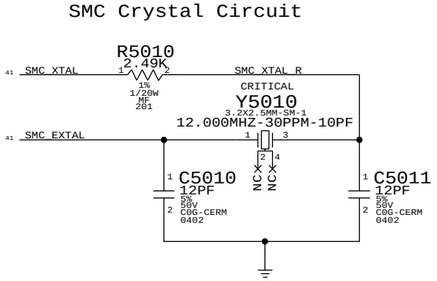
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



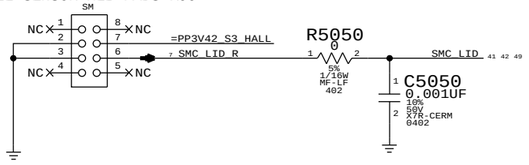
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

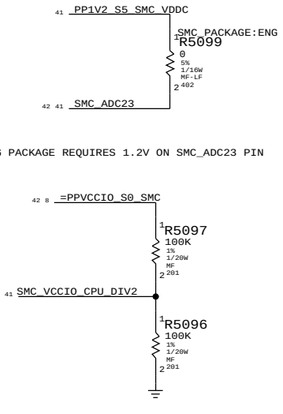
Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5050
HALL-SENSOR-MLB-PADS-K99



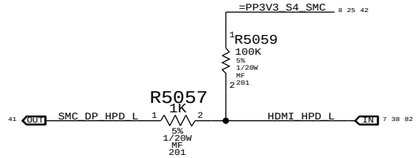
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5050	CRITICAL	

Power Rail Connections



HDMI HPD ESD PROTECTION

Inversion now taking place on RIO



1K for ESD protection

Signal Connections

=CHGR_ACOK	SMC_BC_ACOK		
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC		
SMC_ADC0	SMC_CPU_VSENSE	45	
SMC_ADC1	SMC_CPU_ISENSE	46	
SMC_ADC2	SMC_GPU_HI_ISENSE	46	
SMC_ADC3	SMC_DCIN_VSENSE	45	
SMC_ADC4	SMC_DCIN_ISENSE	46	
SMC_ADC5	SMC_PBUS_VSENSE	45	
SMC_ADC6	SMC_SSD_ISENSE	99	
SMC_ADC7	SMC_CHGR_BMON_ISENSE	46	
SMC_ADC8	SMC_CPU_HI_ISENSE	46	
SMC_ADC9	SMC_OTHER_HI_ISENSE	46	
SMC_ADC10	SMC_P1V5MEM_ISENSE	45	
SMC_ADC11	SMC_CPUVCCIO_ISENSE	45	
SMC_ADC12	SMC_GFX_VSENSE	45	
SMC_ADC13	SMC_CPU_SA_ISENSE	45	
SMC_ADC14	SMC_GPU_CORE_VSENSE	45	
SMC_ADC15	SMC_GPU_CORE_ISENSE	45	
SMC_ADC16	SMC_LCDBKLT_VSENSE	99	
SMC_ADC17	SMC_LCDBKLT_ISENSE	99	
SMC_ADC18	SMC_CPU_GFX_ISENSE	46	
SMC_ADC19	SMC_GPU_P1V35_ISENSE	99	
SMC_ADC20	SMC_CPU_SA_VSENSE	99	
SMC_ADC21	SMC_PCH_CORE_ISENSE	99	
SMC_ADC22	SMC_X29_ISENSE	99	
SMC_ADC23	SMC_TBT_ISENSE_R	99	
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	7	
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	7	
BDV_BKL_PWM	NC_BDV_BKL_PWM		
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC	25	
	=TBT_WAKE_L	18 35	

SMC_PACKAGE:PROD
R5013 0 5% 1/16W MF-LF 402
SMC_TBT_ISENSE

R5012 22 5% 1/20W MF 201
PM_CLK32K_SUSCLK_R
PLACE_NEAR=U1800.N14:5.1mm
SMC_CLK32K

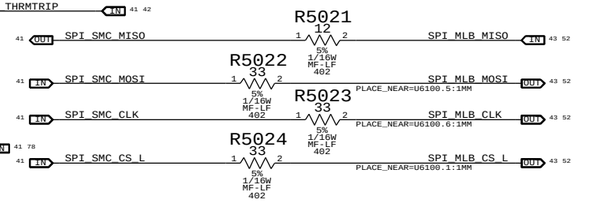
ENET_ASF_GPIO	NC_ENET_ASF_GPIO		
SMC_SYS_LED	NC_SMC_SYS_LED	7	
MEM_EVENT_L	NC_MEM_EVENT_L		
SMC_ODD_DETECT	NC_SMC_ODD_DETECT	7	
IR_RX_OUT_RC	NC_IR_RX_OUT_RC		

MAKE_BASE=TRUE

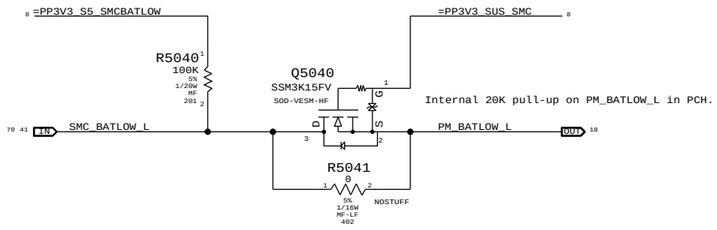
ADC10 AND ADC11 ARE SHARED WITH COMPARATORS ON STACK BOARD

SMC12 PECI SUPPORT

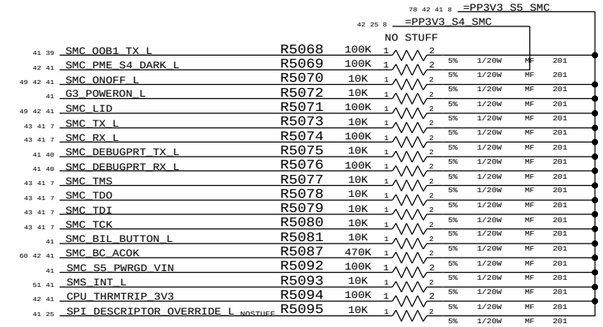
SMC12 SPI SUPPORT

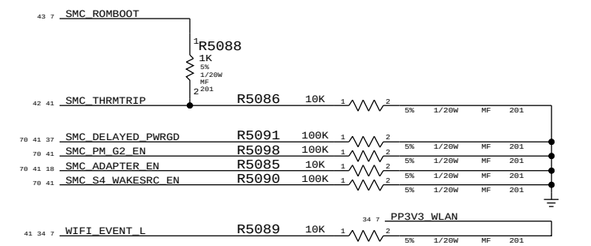


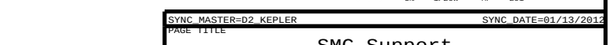
BATLOW# ISOLATION

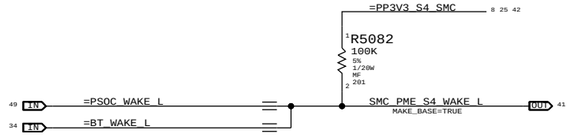


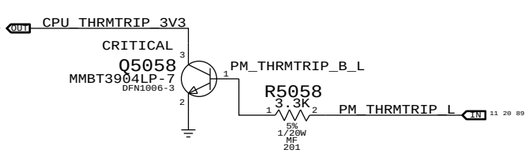
PULL-UPS











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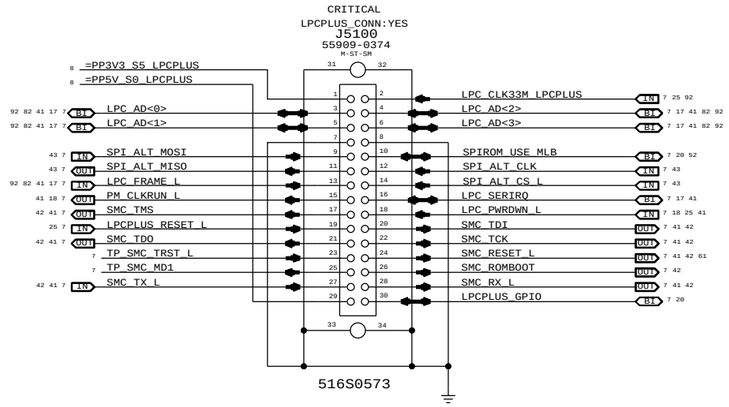
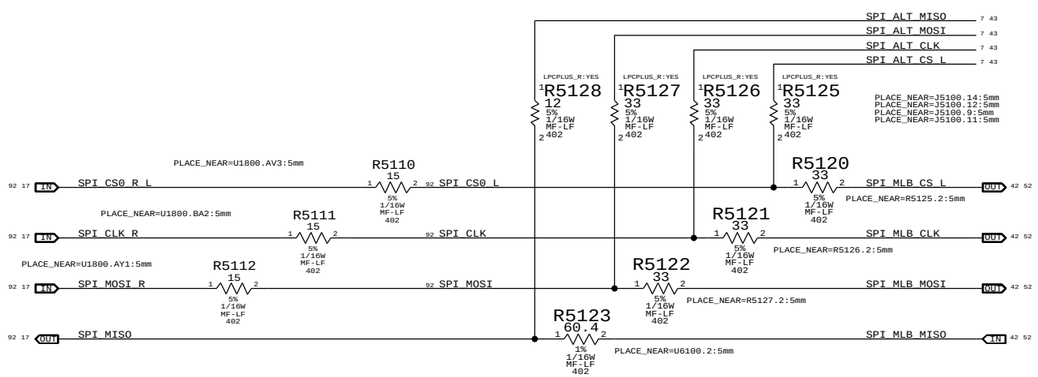
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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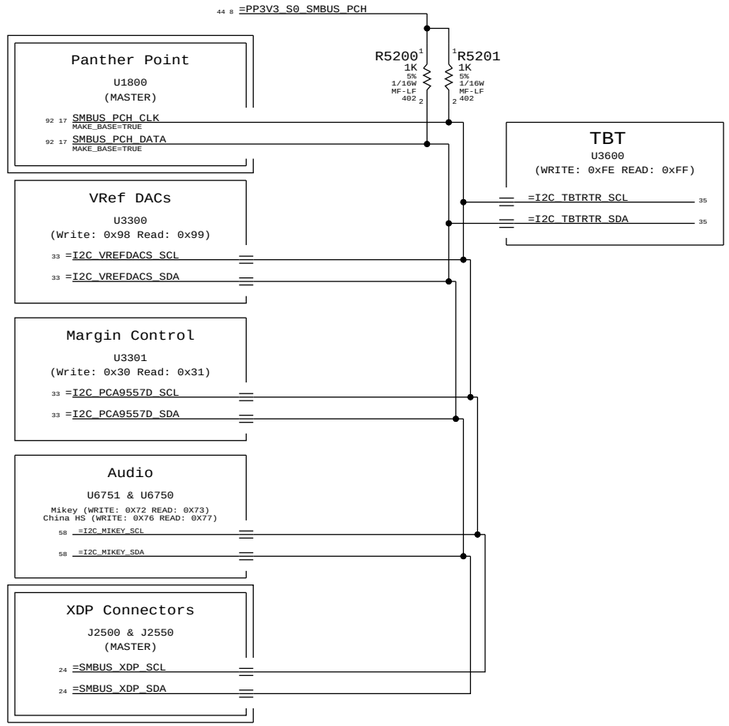
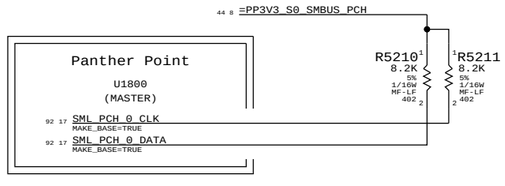
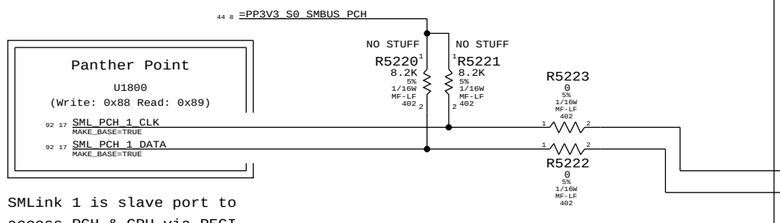
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

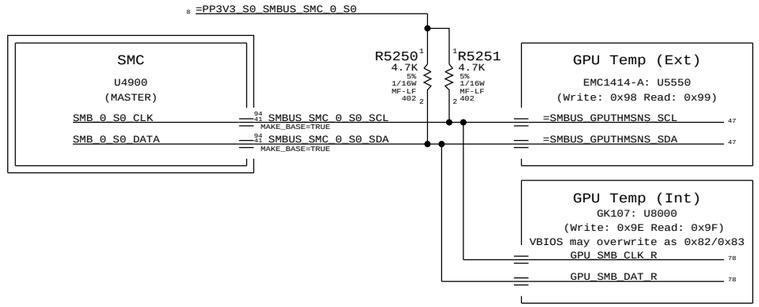


PCH "SMLink 1" Connections



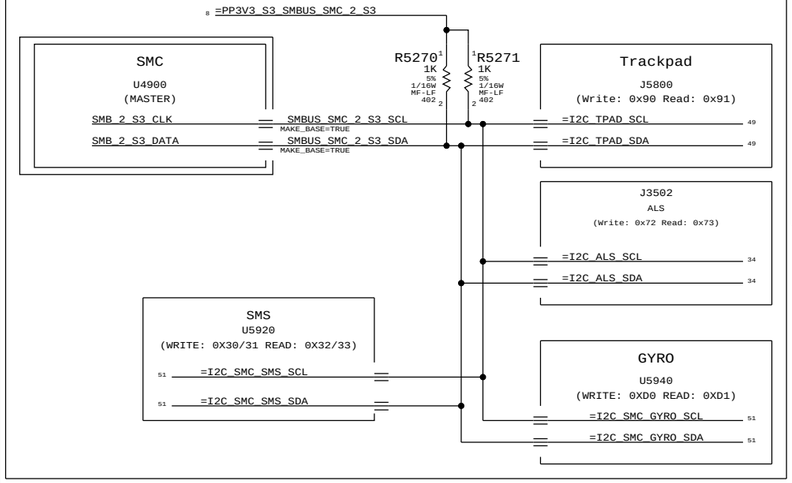
SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

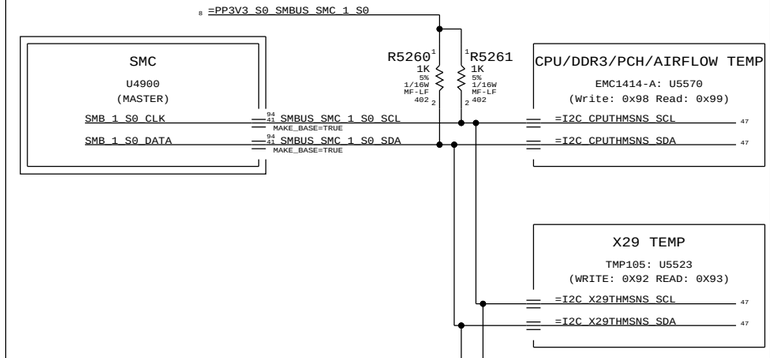


SMC "2" SMBUS CONNECTIONS

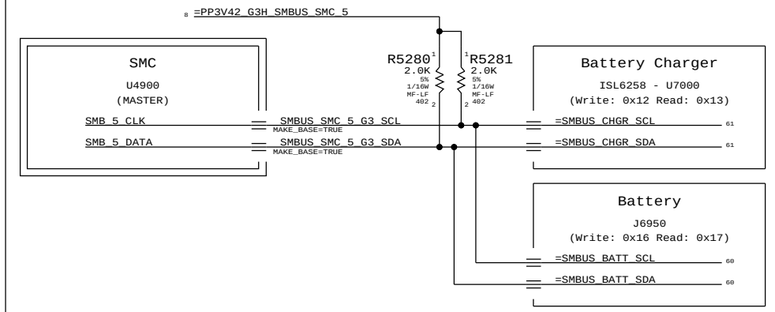
NOTE: SMC RMT bus remains powered and may be active in S3 state



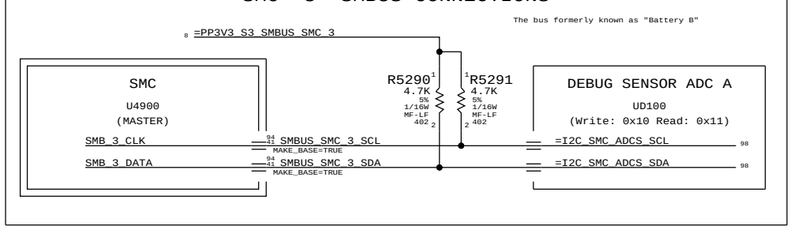
SMC "1" SMBUS CONNECTIONS



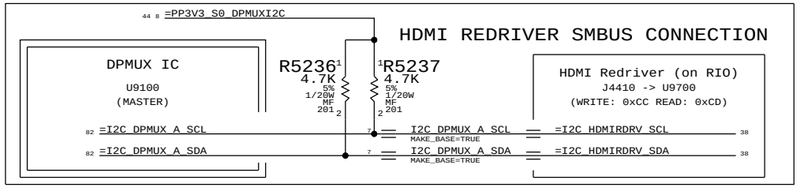
SMC "5" SMBUS CONNECTIONS



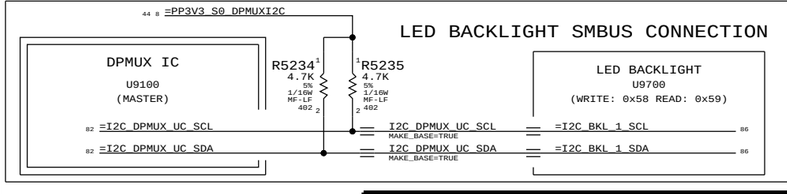
SMC "3" SMBUS CONNECTIONS



HDMI REDRIVER SMBUS CONNECTION



LED BACKLIGHT SMBUS CONNECTION



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SMBus Connections

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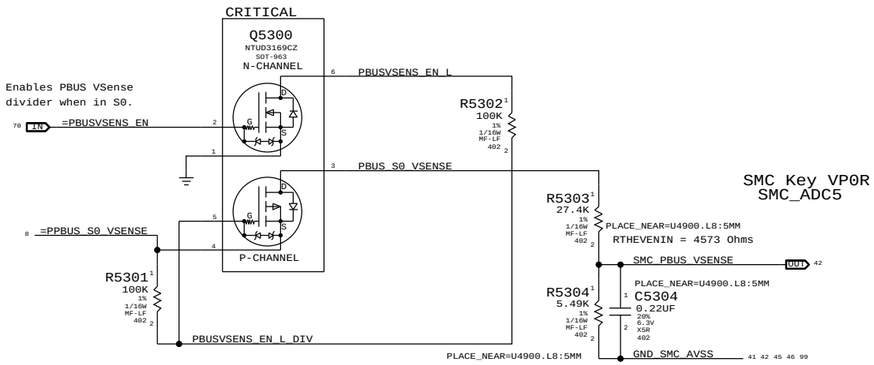
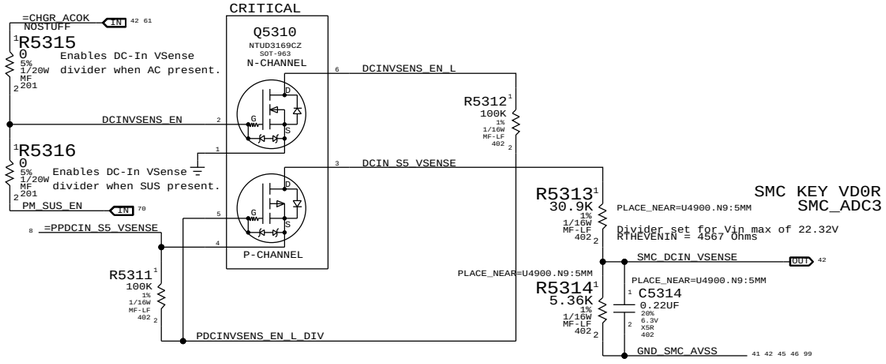
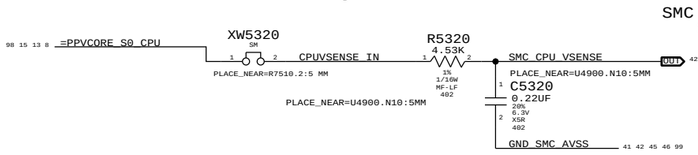
PBUS Voltage Sense Enable & Filter



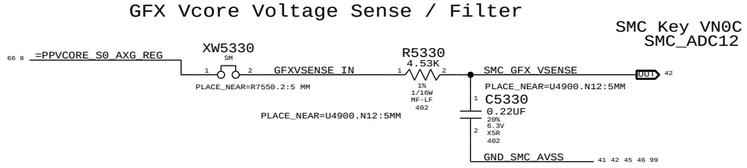
DC-In Voltage Sense Enable & Filter



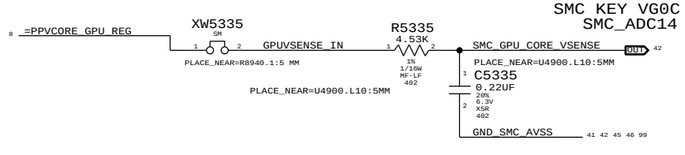
CPU Vcore Voltage Sense / Filter



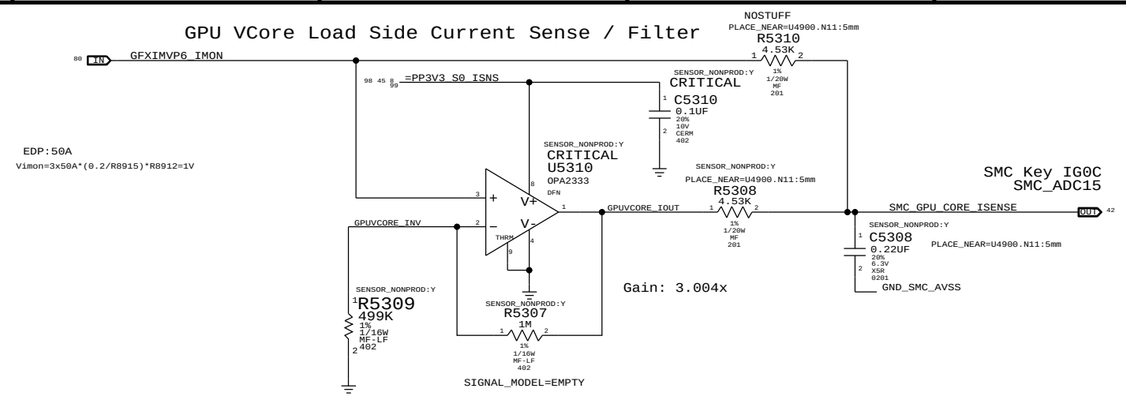
GFX Vcore Voltage Sense / Filter



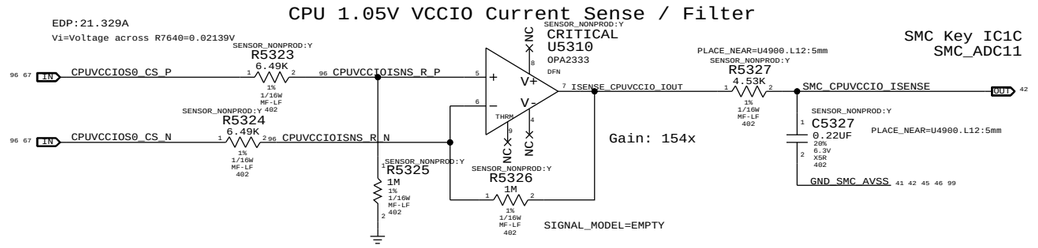
GPU Vcore Voltage Sense / Filter



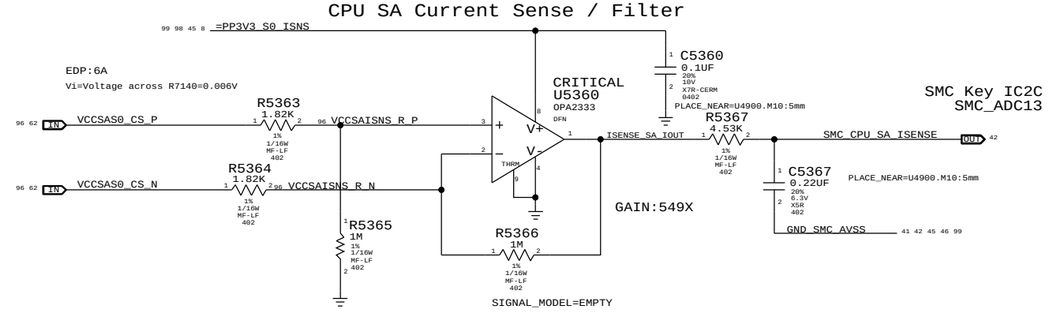
GPU VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter

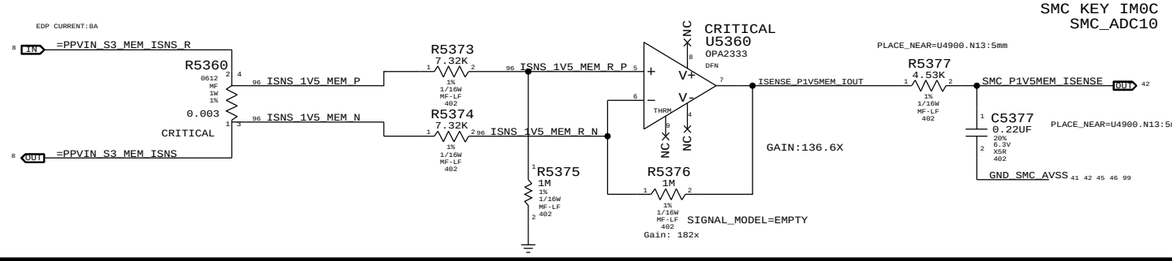


CPU SA Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	1	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	C5327		SENSOR_NONPROD:N
1175O008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5308		SENSOR_NONPROD:N

DDR3 1.5V DRAM ONLY CURRENT SENSE / FILTER



SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2013

PAGE TITLE

Voltage & Load Side Current Sensing

Apple Inc.

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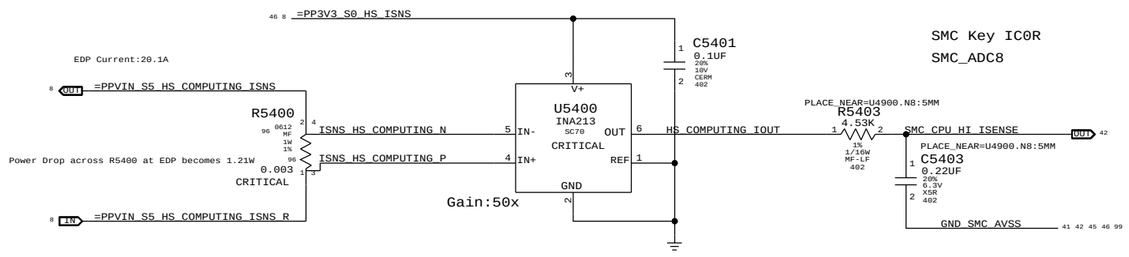
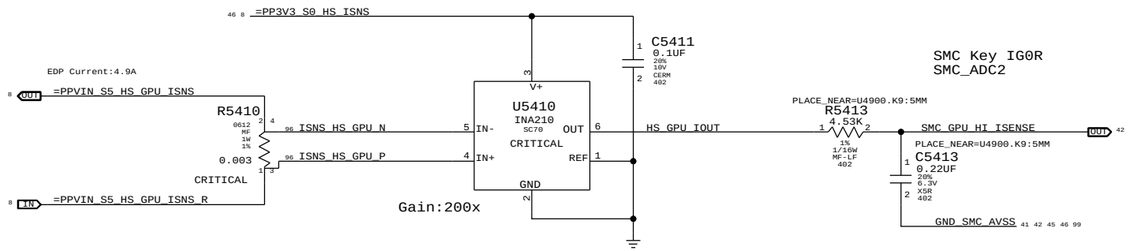
COMPUTING High Side Current Sense / Filter



GRAPHICS High Side Current Sense / Filter

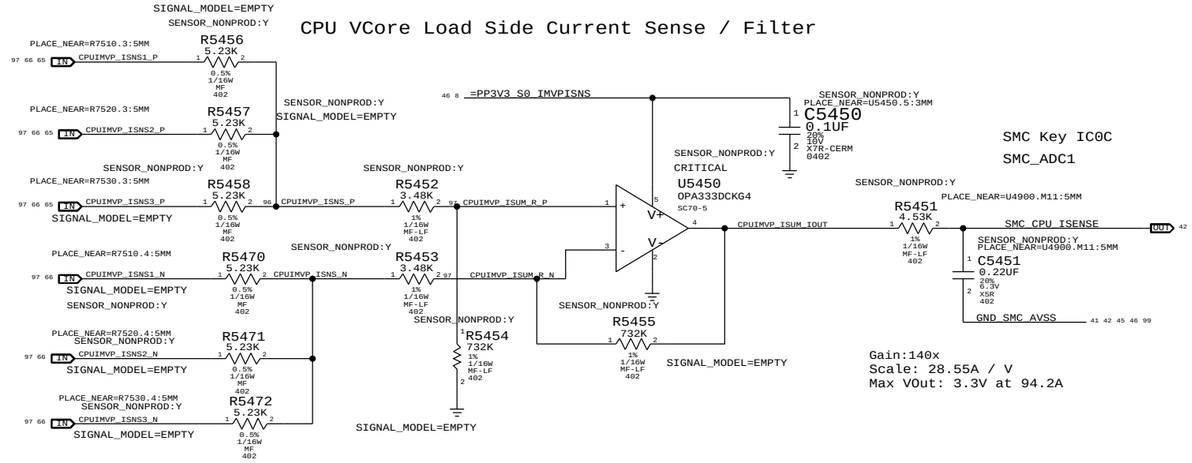


OTHER High Side Current Sense / Filter

CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER

DC-IN (AMON) Current Sense Filter

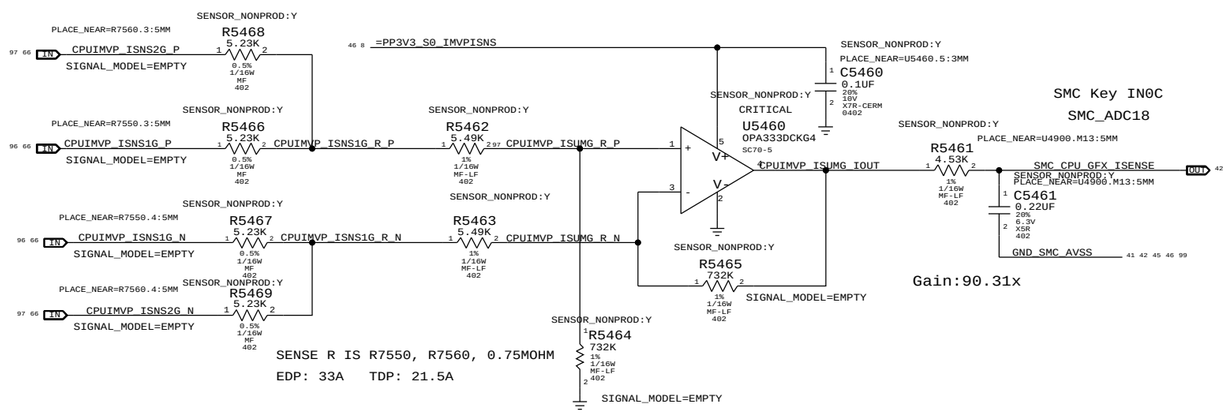
CPU VCore Load Side Current Sense / Filter



Sense R is R7510, R7520 & R7530
Individual Sense R is 0.75mOhm
EDP: 94A TDP :45A

(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

GFX/IG VCore Load Side Current Sense / Filter



SENSE R IS R7550, R7560, 0.75MOHM
EDP: 33A TDP: 21.5A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	2	RES,MTL FILM,100K,1,1/16W,0402,SMD,LF	C5451,C5461		SENSOR_NONPROD:N

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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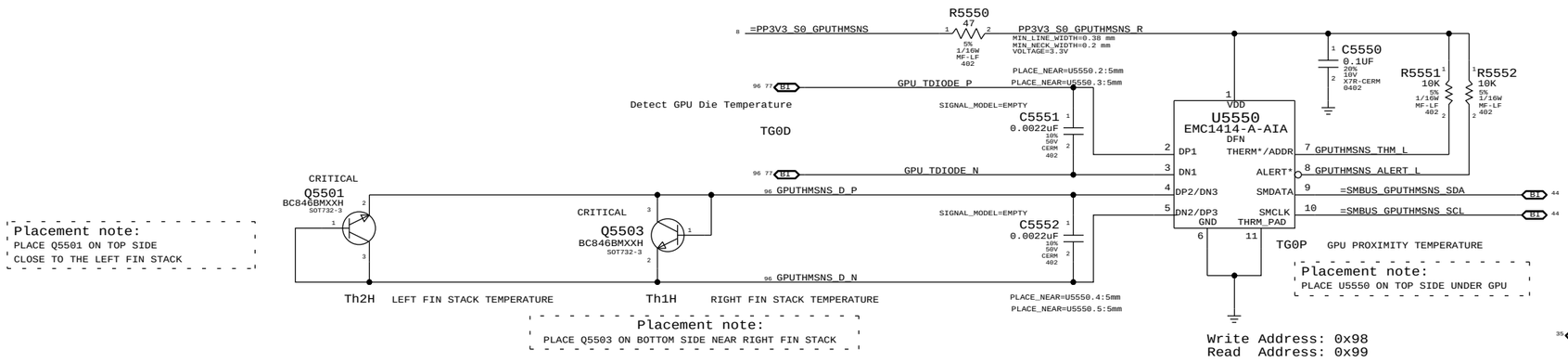
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK

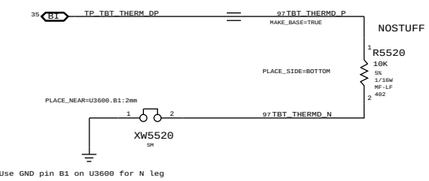


Placement note:
PLACE Q5501 ON TOP SIDE
CLOSE TO THE LEFT FIN STACK

Placement note:
PLACE Q5503 ON BOTTOM SIDE NEAR RIGHT FIN STACK

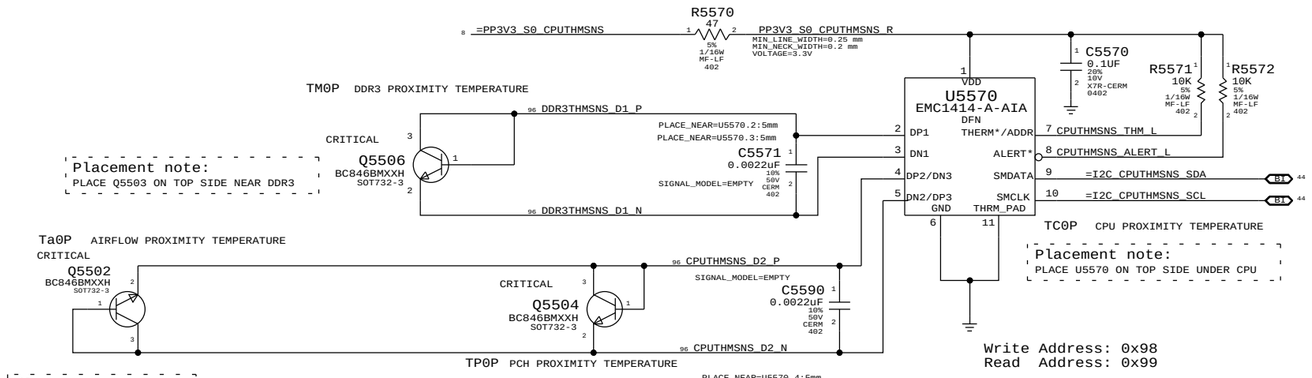
Placement note:
PLACE U5550 ON TOP SIDE UNDER GPU

TBT DIE



Use GND pin B1 on U3600 for N leg

DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



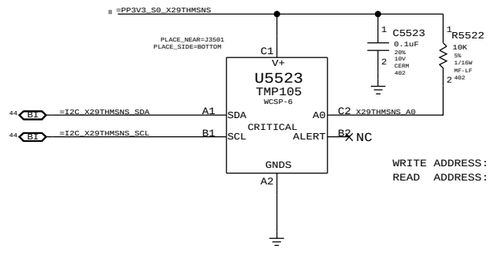
Placement note:
PLACE Q5503 ON TOP SIDE NEAR DDR3

Placement note:
PLACE Q5502 ON TOP SIDE
CLOSE TO BOARD EDGE

Placement note:
PLACE Q5504 ON TOP SIDE UNDER PCH

Placement note:
PLACE U5570 ON TOP SIDE UNDER CPU

TW0P X29 PROXIMITY



Placement note:
PLACE U5523 ON BOTTOM NEAR X29 CONN

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE
Thermal Sensors

Apple Inc.

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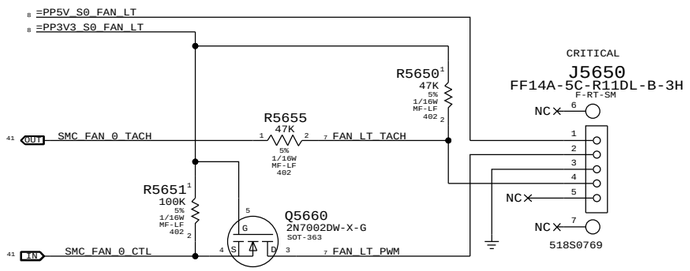
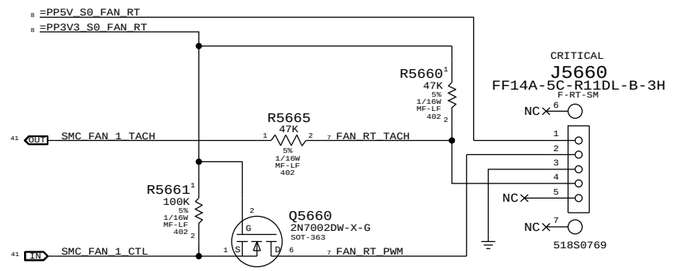
Left Fan



Right Fan



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Fan Connectors

Apple Inc.

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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

PLACE_SIDE=BOTTOM

=PP3V3_S4_TPAD — R5704 0 5% 1/16W MF-LF 402 — PP3V3_S3_PSOC (MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V)

BYPASS=U5701.49:50:5 mm — BYPASS=U5701.49:50:8 mm — BYPASS=U5701.49:50:11 mm

C5704 100PF 5% 50V C0G-CERM 0201 — C5705 0.1UF 10% 6.3V X5R 201 — C5706 4.7UF 20% 6.3V X5R 402

R5703 220K 5% 1/20W MF 201

=PSOC_WAKE_L (OUT 42)
PICKB_L (49 7)
BUTTON_DISABLE (49)
Z2_HOST_INTN (49 7)
WS_LEFT_SHIFT_KEY (49)
WS_LEFT_OPTION_KEY (49)

WS_CONTROL_KEY (49)
Z2_KEY_ACT_L (49 7)
TPAD_VBUS_EN (IN 78)
PSOC_MISO (49 7)
PSOC_F_CS_L (49 7)
PSOC_MOSI (49 7)
PSOC_SCLK (49 7)
Z2_MISO (49 7)
Z2_CS_L (49 7)
Z2_MOSI (49 7)
Z2_SCLK (49 7)

CRITICAL
OMIT
U5701
CY8C24794
MLF
(SYM-VER2)
337S2983

WS_KBD23 … WS_KBD18 (7 49)
WS_KBD17 … WS_KBD3 (7 49)
WS_KBD4 … WS_KBD6 (7 49)
Z2_CLKIN (7 49)
TP_P7_7

TP_PSOC_SCL
TP_PSOC_SDA
TP_PSOC_P1_3
TP_ISSP_SCLK_P1_1
ISSP SCLK/I2C SCL
TP_ISSP_SDATA_P1_0
ISSP SDATA/I2C SDA

R5701 24 5% 1/20W MF 201 — USB_TPAD_P (91 9) — USB_TPAD_R_P
R5702 24 5% 1/20W MF 201 — USB_TPAD_N (91 9) — USB_TPAD_R_N

(PP3V3_S3_PSOC)

C5702 100PF 5% 50V C0G-CERM 0201 — C5703 0.1UF 10% 6.3V X5R 201 — C5701 4.7UF 20% 6.3V X5R 402

BYPASS=U5701.22:19:5 mm — BYPASS=U5701.22:19:8 mm — BYPASS=U5701.22:19:11 mm

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector

CRITICAL
J5700 516S0689
55560-0228
M-ST-SM

=PP3V3_S4_TPAD — R5708 0 5% 1/20W MF 201 — NOSTUFF C5708 0.1UF 10% 6.3V X5R 201

PP3V3_TPAD_CONN (VOLTAGE=3.3V, MIN_NECK_WIDTH=0.20MM, MIN_LINE_WIDTH=0.50MM)

Z2_CS_L (49 7) — Z2_KEY_ACT_L (7 49)
Z2_MOSI (49 7) — PSOC_F_CS_L (7 49)
Z2_MISO (49 7) — PICKB_L (7 49)
Z2_SCLK (49 7) — PSOC_MISO (7 49)
Z2_HOST_INTN (49 7) — PSOC_MOSI (7 49)
Z2_CLKIN (49 7) — PSOC_SCLK (7 49)
=I2C_TPAD_SDA (44)
=I2C_TPAD_SCL (44)
NC

TPAD_5V_SW_S4
PLACE_NEAR=J5800.18:3MM
L5700 FERR-120-OHM-1.5A 0402-LF
=PP5V_S4_TPAD (8) — PP5V_S4_CUMULUS (VOLTAGE=5V, MIN_NECK_WIDTH=0.20MM, MIN_LINE_WIDTH=0.50MM)
C5700 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=J5800.18:3MM

TPAD_5V_LDO
PLACE_NEAR=J5800.18:3MM
L5707 FERR-120-OHM-1.5A 0402-LF
=PP5V_S5RS4_CUMULUS (49)
C5707 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=J5800.18:3MM

R5700 220K 5% 1/20W MF 201

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

=PP3V42_G3H_TPAD (49 8) — R5710 10 — VDD — C5750 0.1UF 10% 16V X7R-CERM 0402

U5750 SLG4AP021 TQFN

=PP3V3_S4_TPAD (49 8)	OE (IPD)		
WS_LEFT_SHIFT_KBD (49 7)	IN_1 (IPD)	OUT_1	WS_LEFT_SHIFT_KEY (49)
WS_LEFT_OPTION_KBD (49 7)	IN_2 (IPD)	OUT_2	WS_LEFT_OPTION_KEY (49)
WS_CONTROL_KBD (49 7)	IN_3 (IPD)	OUT_3	WS_CONTROL_KEY (49)
		OUT_ALL#	SMC_TPAD_RST_L (OUT 42)

Pull-up in U5010.
GND (5) — THRM PAD (11)

Keyboard Connector

=PP3V3_S4_TPAD (49 8) — =PP3V42_G3H_TPAD (49 8)

WS_KBD1 … WS_KBD23 (49 7)
WS_KBD15_CAP (49 7)
WS_KBD16_NUM (7)
WS_KBD_ONOFF_L (7)
WS_LEFT_SHIFT_KBD (49 7)
WS_LEFT_OPTION_KBD (49 7)
WS_CONTROL_KBD (49 7)

F-RT-SM
FF14A-30C-R11DL-B-3H
J5713
CRITICAL
518S0752

WS_KBD15_C (49) — CAPS:INT R5714 56.2 1% 1/16W MF-LF 402
WS_KBD16N (49) — R5715 10K 1% 1/16W MF-LF 402
SMC_ONOFF_L (OUT 42 41) — R5710 1K 5% 1/16W MF-LF 402
C5710 0.1UF 20% 10V CERM 402 (PLACEMENT_NOTE=NEAR J5713)

WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

Caps Lock LED Drive

TPAD_5V_NO_FET
R5720 0 5% 1/16W MF-LF 402

5V TPAD FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

TPAD_5V_FET CRITICAL Q5720 SIA413DJ SC70-6L

=PP3V3_S4_TPAD (49 8)

CAPS:EXT R5730 10K — R5732 10K — R5734 20K — R5731 10K — R5733 20K — R5735 10K (5% 1/20W MF 201)

WS_KBD15_C (49)
CAP_VREF_L
CAP_VREF_H
CAPS:EXT U5730 LM393ADGKR MSOP — GND

CAP_COMP_H
CAP_COMP_L

CAPS:EXT R5740 10K — R5738 10K — R5736 10K (5% 1/20W MF 201)

CAPS:EXT Q5736 NTZD3152P SOT-563-HF

CAP_SOURCE
CAPS:EXT R5737 113 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.1MM
WS_KBD15_CAP (7 49) — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.1MM
CAPS:EXT R5739 113 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.1MM
CAP_SINK

CAPS:EXT Q5738 DMN3730UFB4 DFN1006H4-3

CAP_COMP_L_INV

CAPS:EXT CRITICAL Q5734 SSM3K15AMFVAPE VESM

CAP_COMP_L

All RC values are TBD

5V TRACKPAD S4 FET

=PP5V_S5_TPAD (8)

TPAD_5V_FET Q5721 SSM3K15FV SOD-VESM-HF
=P5VS4_TPAD_EN (IN 78)

TPAD_5V_FET R5721 220K 5% 1/20W MF 201
P5VCUMULUS_EN_L

TPAD_5V_FET C5722 0.033UF 10% 16V X5R 402
TPAD_5V_FET R5722 3.3K 5% 1/20W MF 201
P5VCUMULUS_SS

TPAD_5V_FET C5723 0.01UF 10% 16V X5R 201

PP5V_S5RS4_CUMULUS (49) VOLTAGE=5V, MIN_NECK_WIDTH=0.20MM, MIN_LINE_WIDTH=0.50MM

TPAD Buttons Disable

BUTTON_DISABLE (49) — Q5701 SSM6N15FEAPE SOT563 — SMC_LID (IN 42 41)

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

BOM Options available to CSA 5

TPAD_5V:SW_S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

BOM GROUP	BOM OPTIONS
TPAD_5V:SW_S4	TPAD_5V_SW_S4
TPAD_5V:LDO_S4	TPAD_5V_FET,TPAD_5V_LDO
TPAD_5V:LDO_S5	TPAD_5V_NO_FET,TPAD_5V_LDO

SYNC_MASTER=D2_KEPLER — SYNC_DATE=01/13/2012
PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

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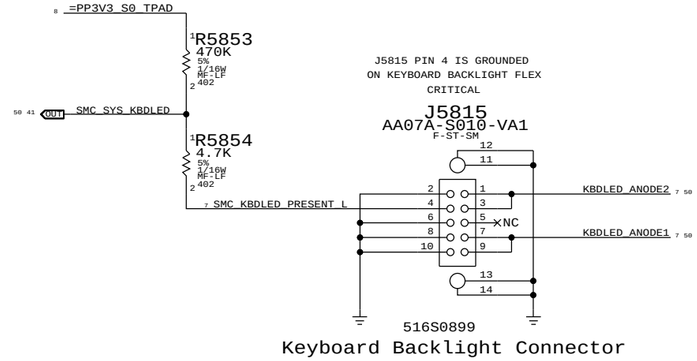
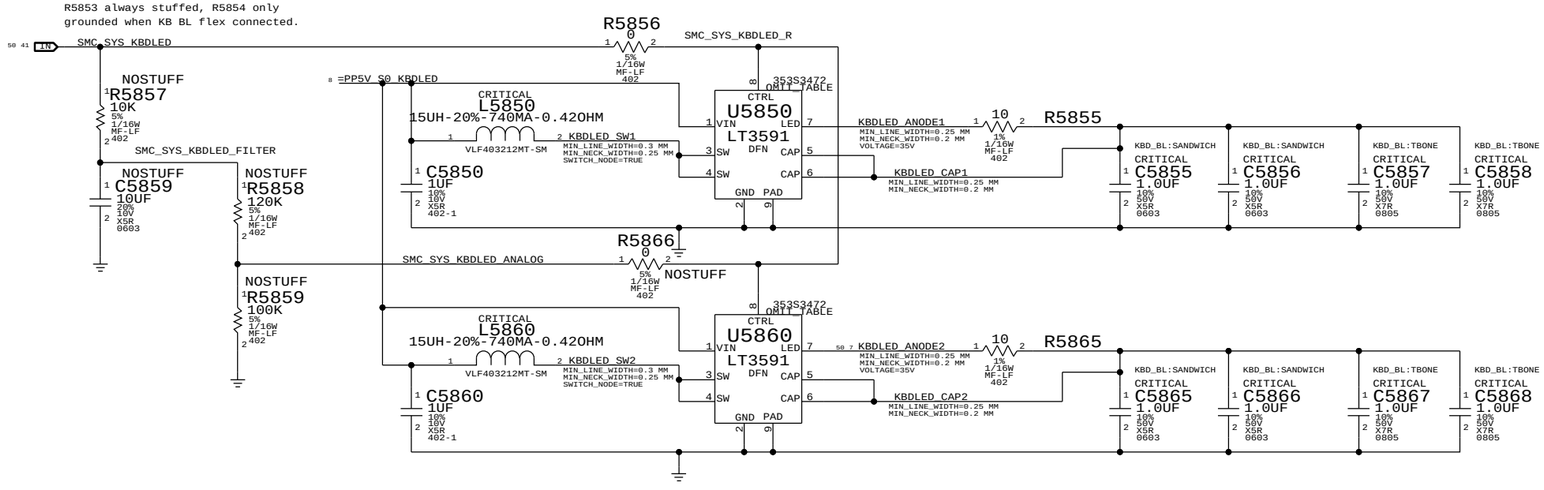


Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will
tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only
grounded when KB BL flex connected.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1612	2	IC,DC/DC CVTR,BOOST,WHITE LED,1MHZ,DFN8	U5850,U5860	CRITICAL	

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

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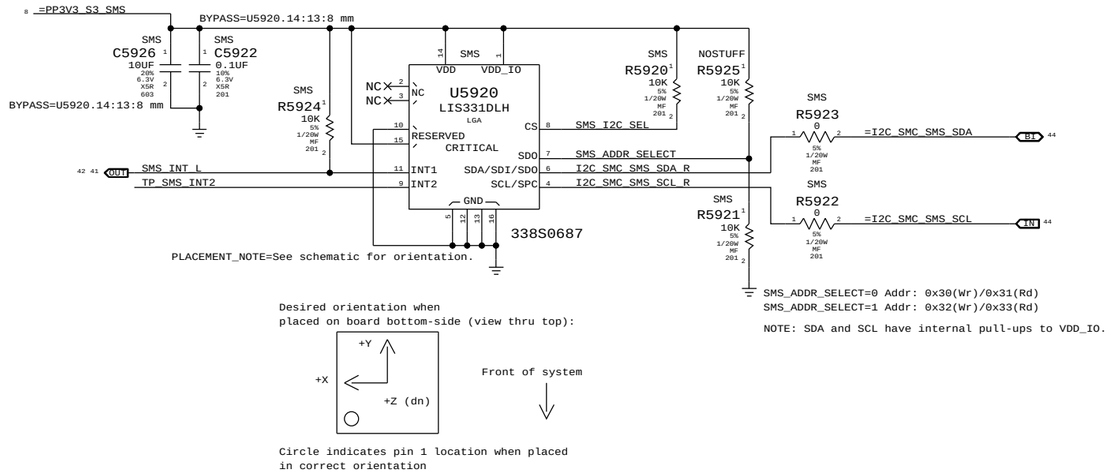

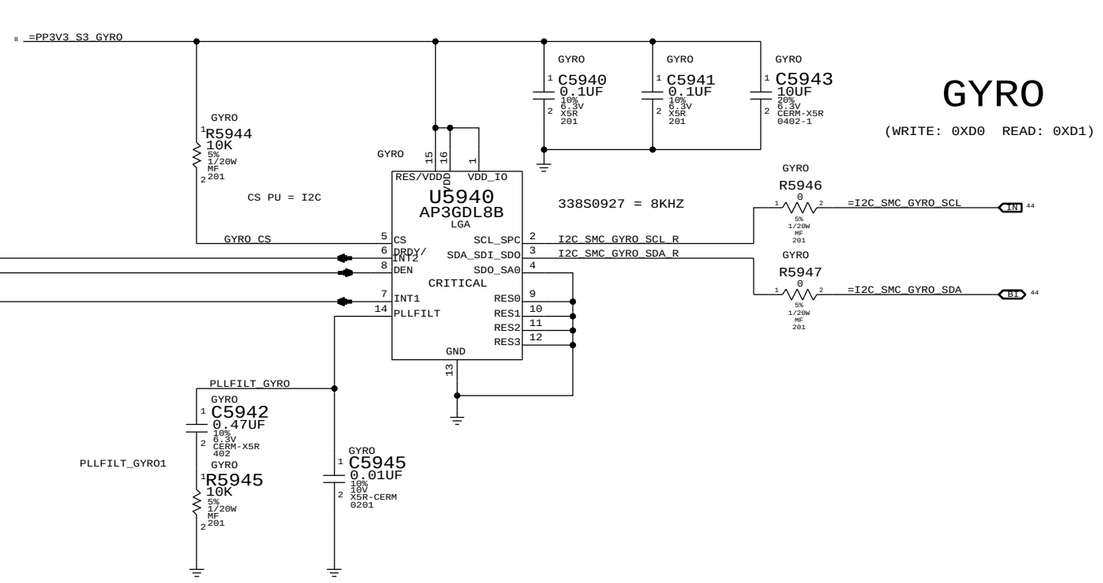

GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DIGITAL ACCELEROMETER & GYRO

Apple Inc.

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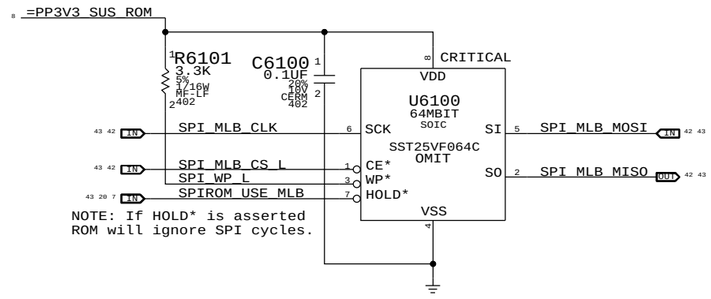

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

SPI ROM

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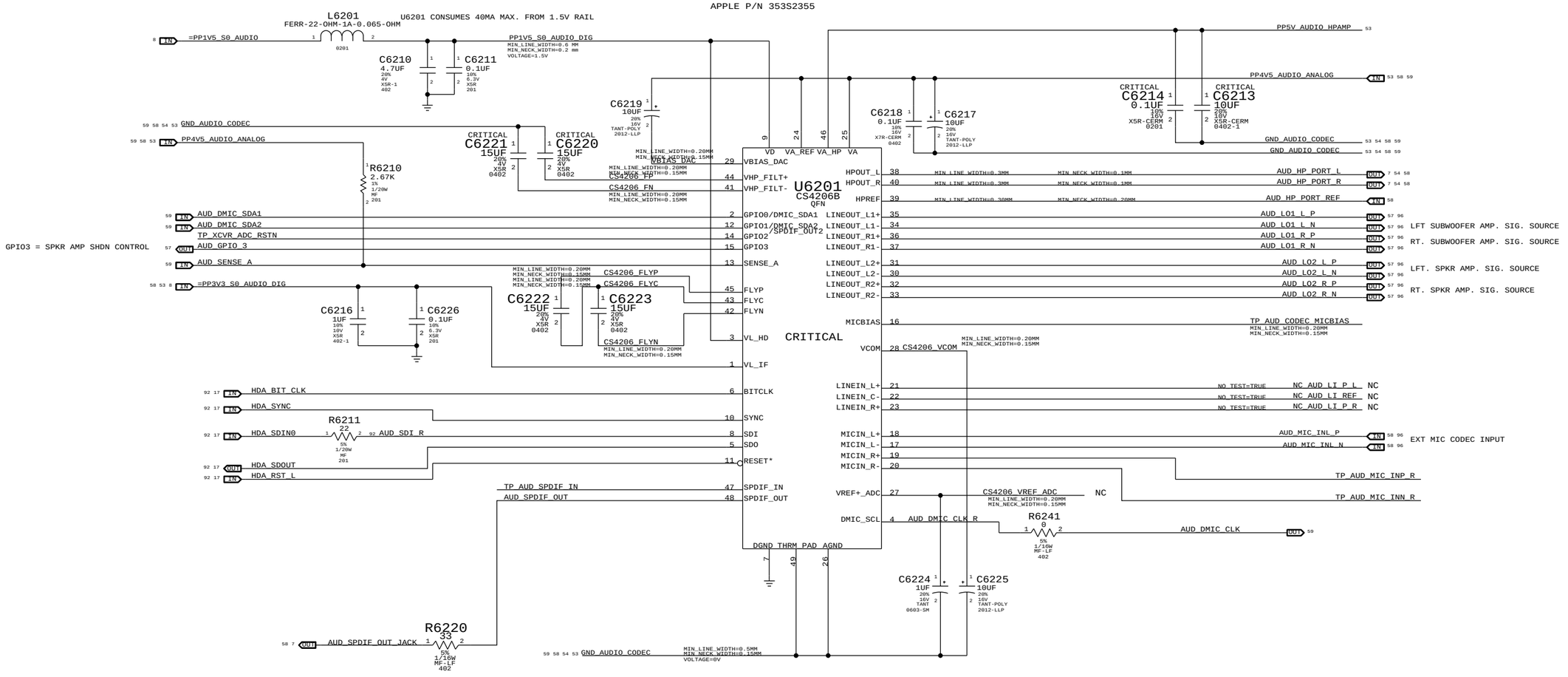
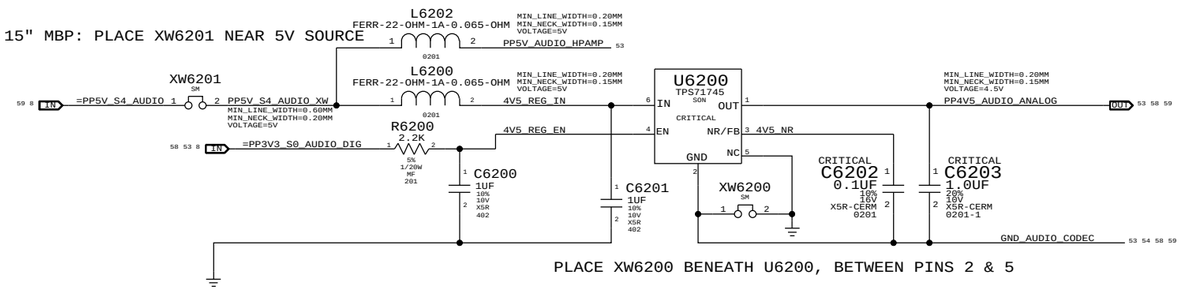
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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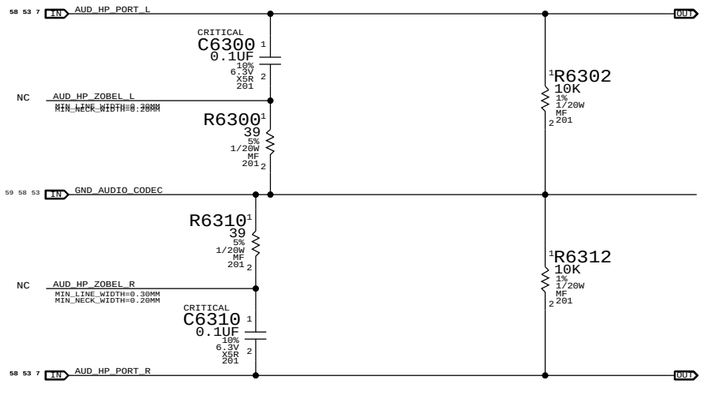
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: IV SENSE

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: IV SENSE FILTER

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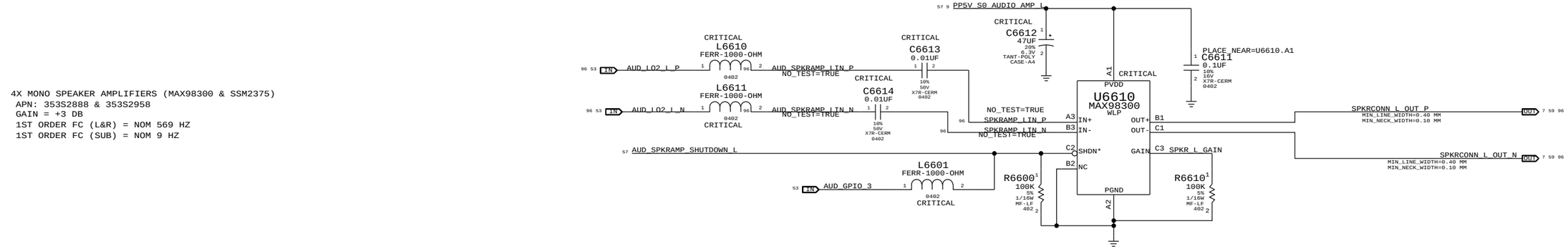
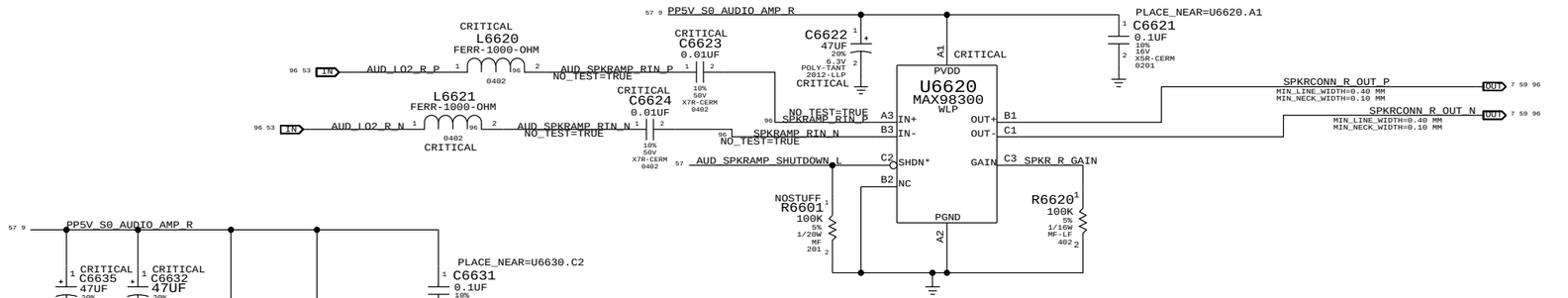
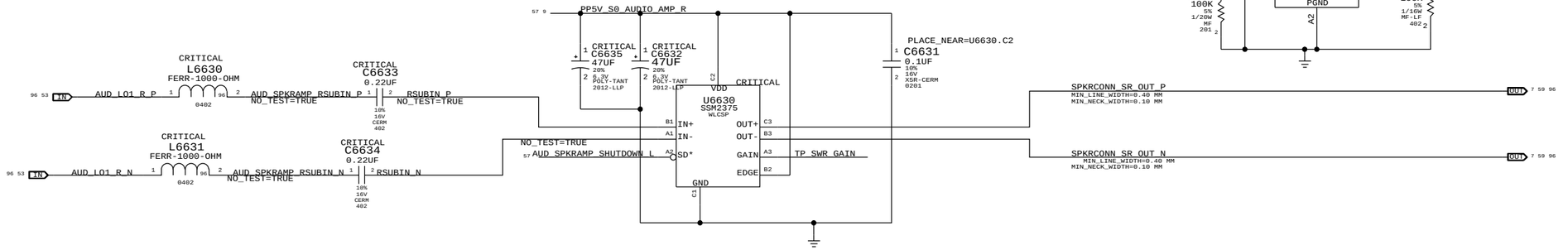
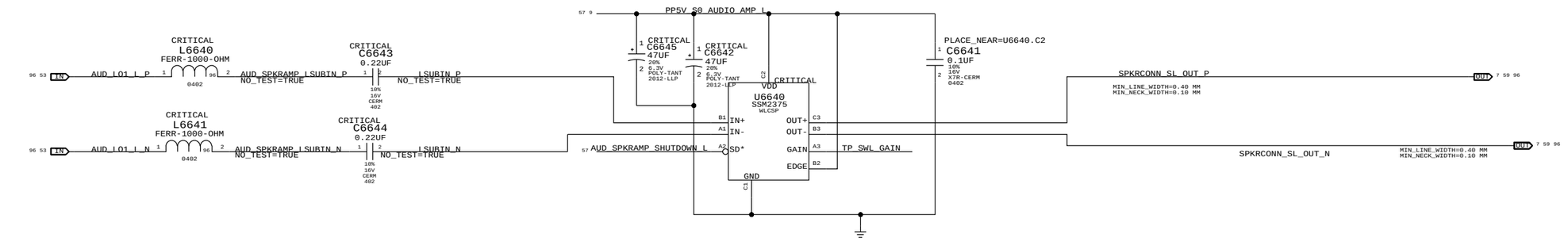
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC MASTER=D2_CARA
SYNC DATE=03/16/2012

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9589
SIZE D
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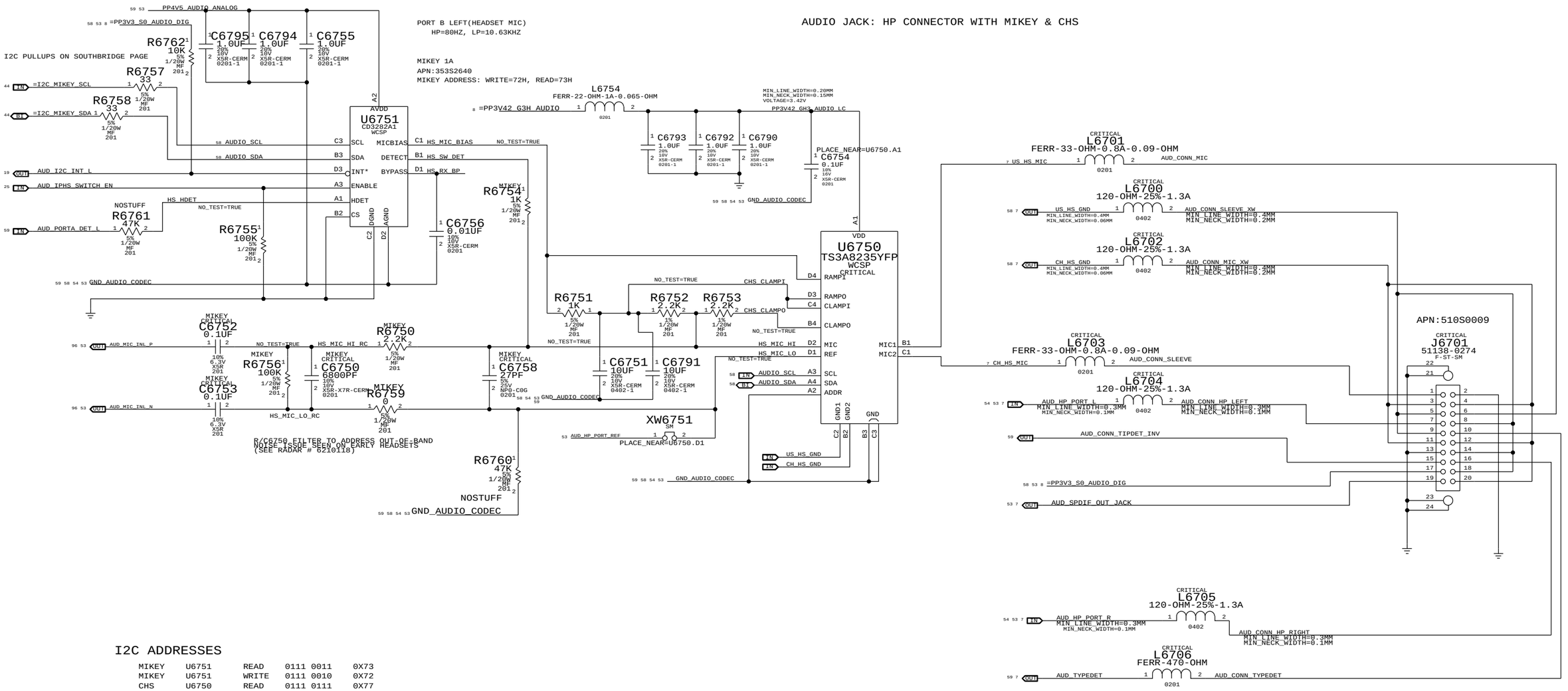
AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE



I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2017

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
REVISION: 4.18.0
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (D,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

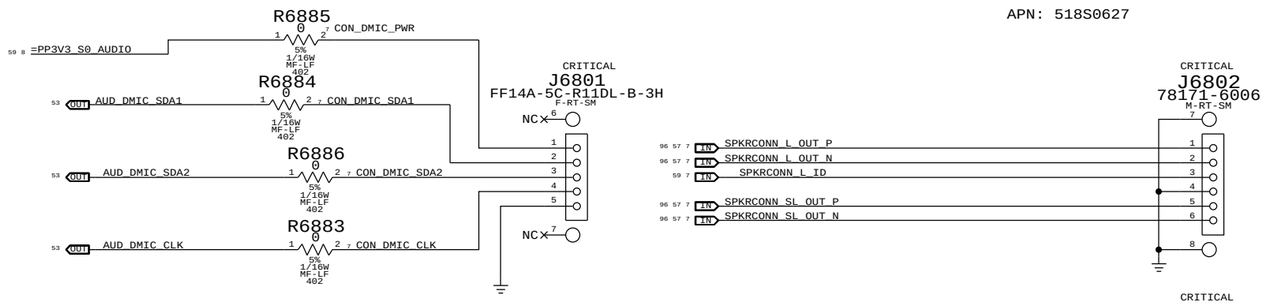
SYSTEM INT AND GPIO LINES

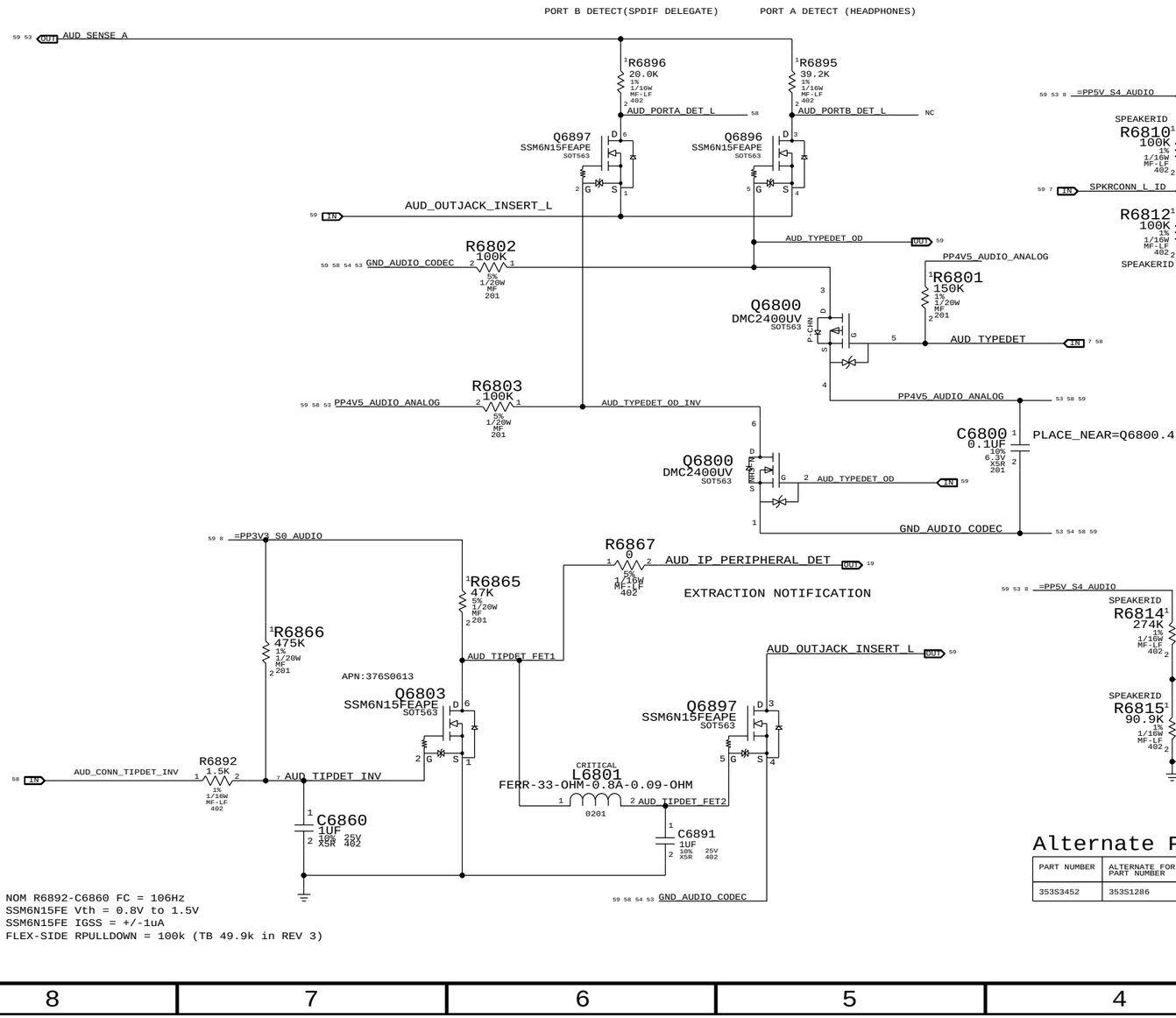
FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

3-MIC CONNECTOR

SPEAKER CONNECTOR HP=80HZ

APN: 518S0627





NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP

SYNC MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE: AUDIO: JACK TRANSLATORS

Apple Inc.

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MagSafe DC Power Jack

CRITICAL
J6900
WTB-PWR-M82
M-RT-SM

518S0508

CRITICAL
F6905
6AMP-32V-0.0095OHM
0603

=PP18V5_DCIN_CONN

PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=18.5V

C6905 0.01UF 20% 50V CERM 0603

TDM_ONEWIRE_MPM

=PP3V42_G3H_ONEWIREPROT

C6908 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=PLACE NEAR U6900 and U6901

CRITICAL
U6901
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC

C6900 0.1UF 20% 10V CERM 402

R6929 2.0K 5% 1/16W MF-LF 402

SMC_BC_ACOK

ADAPTER_SENSE

U6900
MAX9940
SC70-5
CRITICAL
EXT
INT
VCC
NC
GND

SYS_ONEWIRE

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

TDM LEVEL SHIFT

=PP3V42_G3H_TDM

TDM:MPM R6977 22 5% 1/20W MF 201

TDM:MLB R6975 2.21K 1% 1/20W MF 201

TDM:MLB R6976 22 5% 1/20W MF 201

SYS_TDM_ONEWIRE

TDM_ONEWIRE_MLB

R6912 22.1K 1% 1/20W MF 201

Input impedance of 22.1K meets sparkitecture requirements for 15" MBP design only

TDM:MLB
U6970
SLG4AP030
TDFN
CRITICAL
IN_A
IN_B1
IN_B2
OUT_C
OUT_D1
OUT_D2
VDD
GND
THRM PAD

TDM_PD_BASE_R

TDM:MLB CRITICAL D6970 DDZ9694T SOD523

TDM_RX_D

TDM_RX

TDM:MLB R6973 24.9K 1% 1/20W MF 201

TDM:MLB R6974 6.34K 1% 1/20W MF 201

TDM_PD_BASE

TDM:MLB CRITICAL Q6970 ZXTN619MA DFN

TDM:MLB CRITICAL Q6971 MMBT2222AM3T5G SOT723

TDM:MLB R6972 54.9 1% 1/20W MF 201

TDM_PD_DS

TDM:MLB R6971 12.1 1% 1/8W MF-LF 805

TDM:MLB R6970 12.1 1% 1/8W MF-LF 805

LAYOUT NOTE:
Q0220 NEEDS 10 SQ CM
OF 1 OZ CU FOR THERMAL

Q6910
SI5419DU
POWERPAK

R6910 100K 5% 1/20W MF 201

C6912 0.047UF 10% 25V X5R 0402

R6911 10K 5% 1/20W MF 201

DCIN_ISOL_GATE_R

DCIN_ISOL_GATE

=PP18V5_DCIN_ISOL

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

D6910
GDZT2R6.8
GDZ-0201
6.8V Zener

R6920 47 1% 1/3W MF 805

PP18V5_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

CRITICAL
D6905
BAT30CWFILM
SOT-323

R6905 10 5% 1/8W MF-LF 805

=PPBUS_G3H

PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

BATTERY CONNECTOR

518-0376
CRITICAL
J6950
BAT-J5
F-ST-TH

POS 1
POS 2
POS 3
POS 4
SCL 5
SDA 6
SYS_DETECT 7
NEG 8
NEG 9
NEG 10
NEG 11

PPVBAT_G3H_CONN
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA
SYS_DETECT_L

C6950 0.1UF 10% 25V X5R 402

C6960 1UF 10% 25V X5R 603-1

CRITICAL
D6950
RCLAMP2402B
SC-75

R6950 10K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

C6990 4.7UF 10% 35V X5R-CERM 0603

C6991 4.7UF 10% 35V X5R-CERM 0603

NOSTUFF C6992 4.7UF 10% 35V X5R-CERM 0603

NOSTUFF C6993 4.7UF 10% 35V X5R-CERM 0603

NOSTUFF C6996 4.7UF 10% 35V X5R-CERM 0603

NOSTUFF C6997 4.7UF 10% 35V X5R-CERM 0603

U6990
LT3470AED
DFN
CRITICAL
VIN
BOOST
SW
BIAS
FB
SHDN*
NC
GND
THRM PAD

P3V42G3H_BOOST
DIDT=TRUE

C6994 0.22UF 10% 10V CERM 402

CRITICAL
L6995
33UH-20%-0.39A-0.435OHM
DP418C-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

=PP3V42_G3H_REG

Vout = 3.425V
100MA MAX OUTPUT
(Switcher limit)

C6995 22PF 5% 50V NP0-C0G-CERM 0201

P3V42G3H_FB

<Ra> R6995 348K 1% 1/20W MF 201

<Rb> R6996 200K 1% 1/20W MF 201

C6999 22UF 20% 6.3V X5R-CERM-1 603

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

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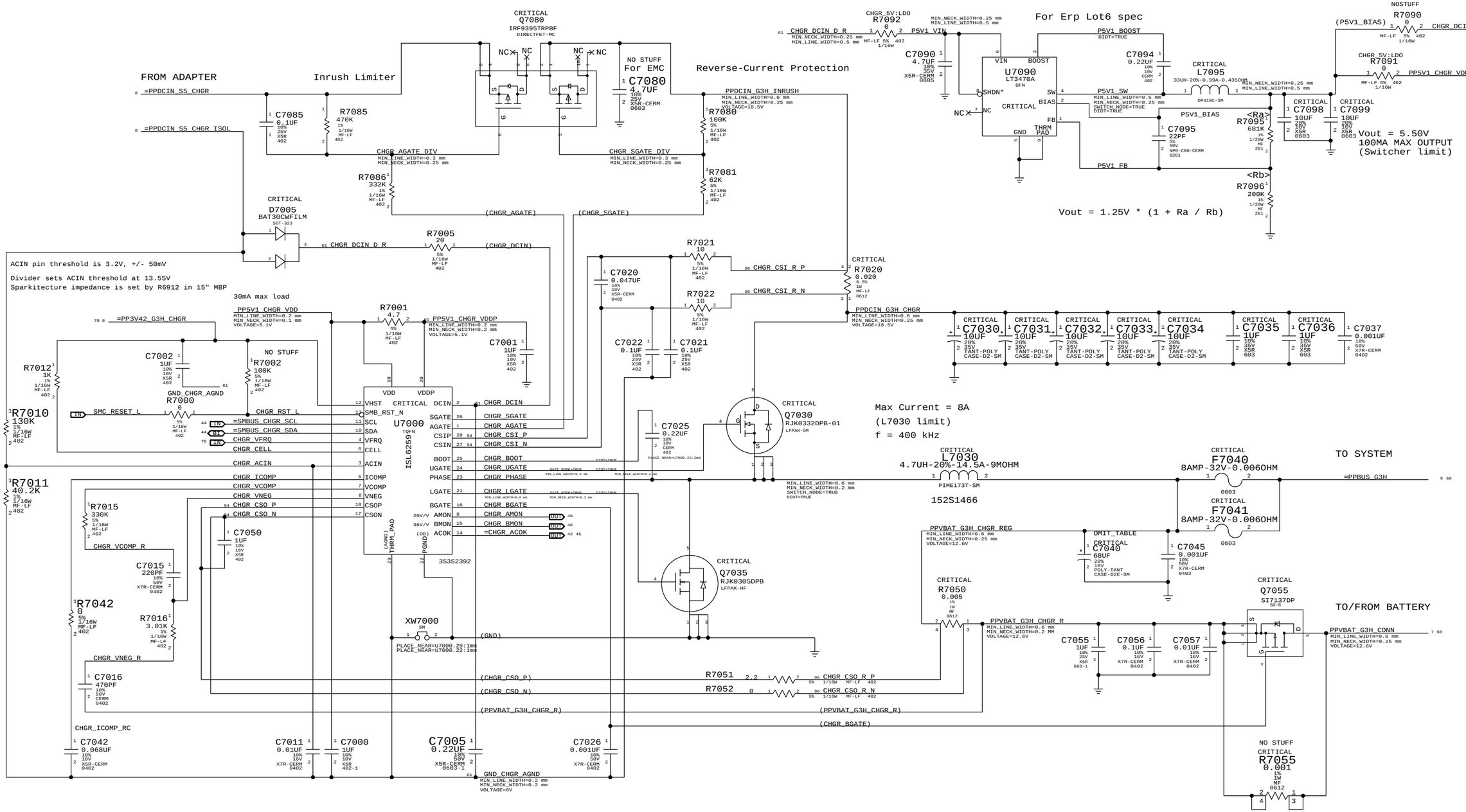

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

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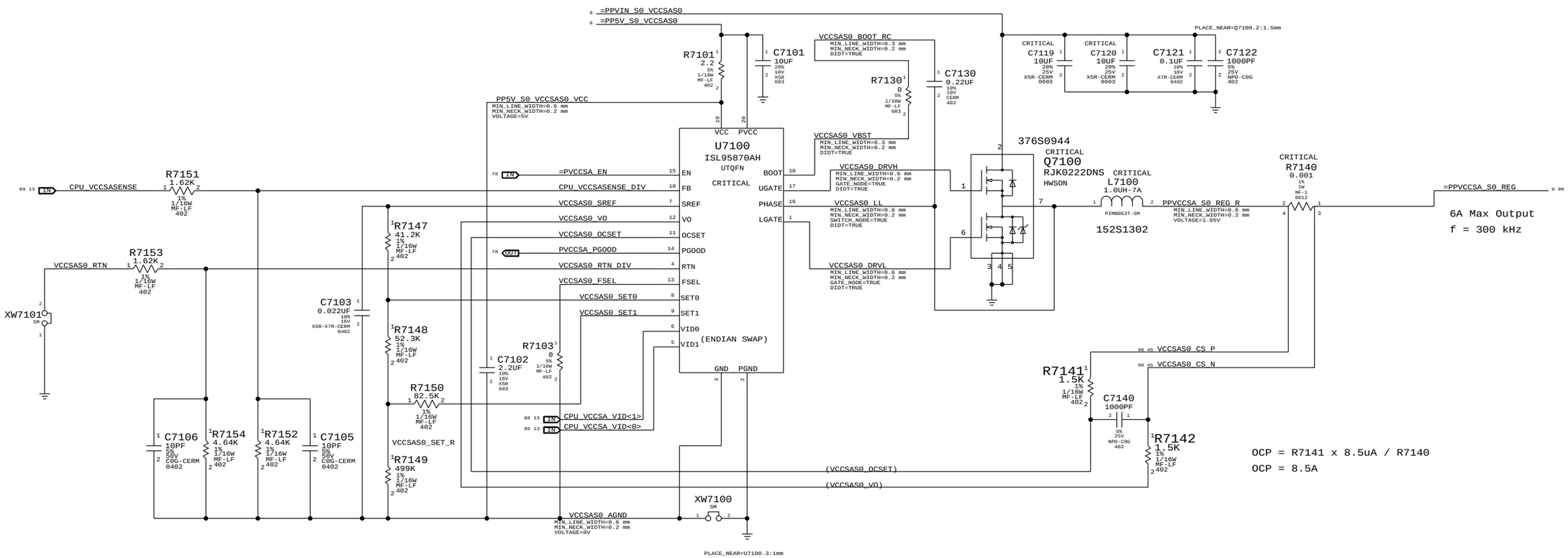

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

fb = (R7151+R7152)/R7152 = 1.349 and Vref = 0.5;

VID1=1, VIC0=1:
Vout<1,1> = Vref x fb;

VID1=0, VID0=1:
Vout<0,1> = Vref x (1+R7147 / (R7148 + R7149)) x fb

VID1=1, VID0=0
Vout<1,0> = Vref x (1+ (R7147 + R7148) / R7149)) x fb

VID1=0, VID0=0
Vout<0,0> = Vref x (1+ (R7147 / (R7148 + R7149 // R7150)) x fb

SYNC MASTER=D2_KEPLER SYNC DATE=01/13/2012

PAGE TITLE

System Agent Supply

Apple Inc.

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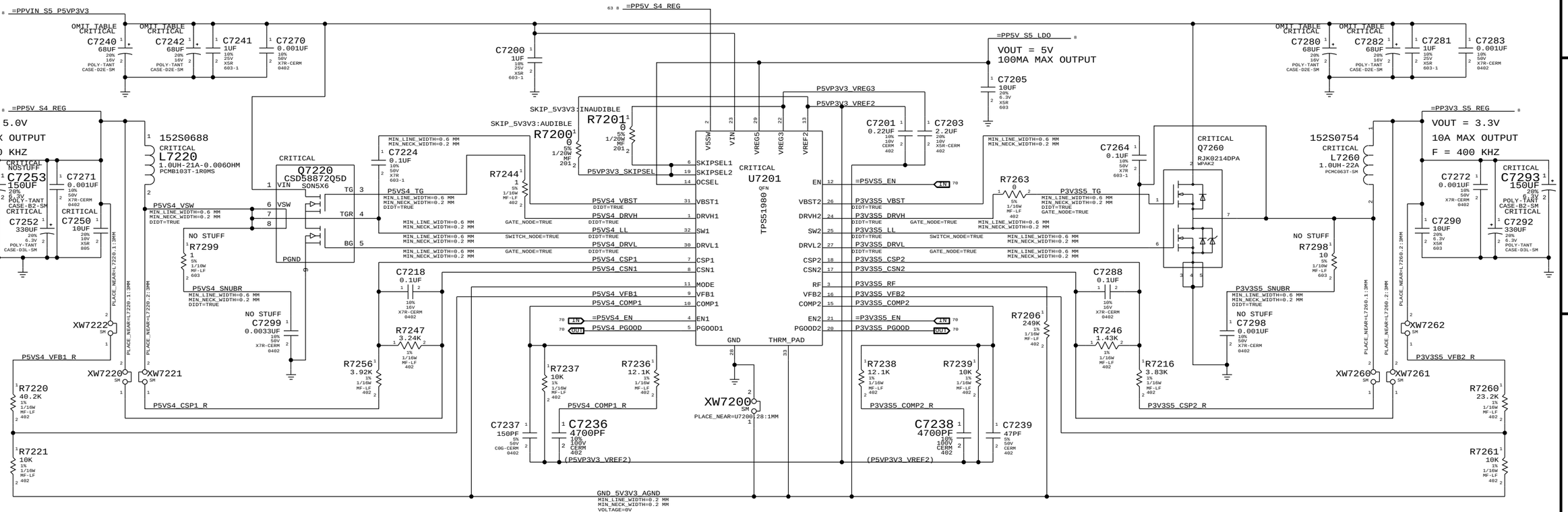

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

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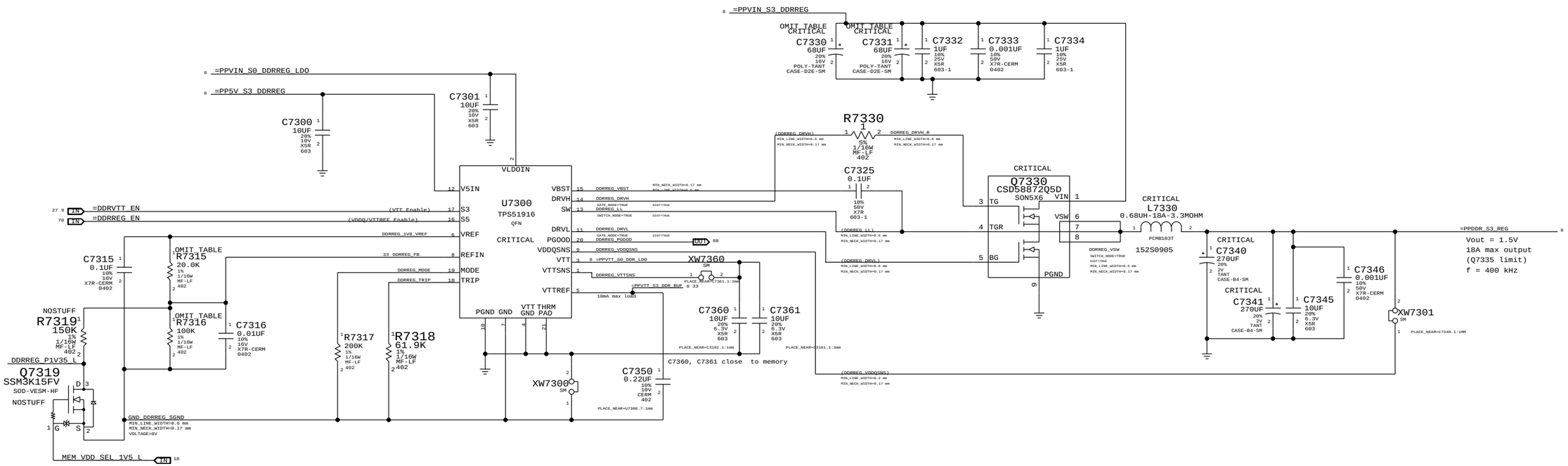
DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R7315		PPDDR:1V5
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7315		PPDDR:1V35
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316		PPDDR:1V5
114S0389	1	RES,MTL FILM,1/16W,57.6K,1,0402,SMD,LF	R7316		PPDDR:1V35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

1V5R1V35V DDR3 SUPPLY

Apple Inc.

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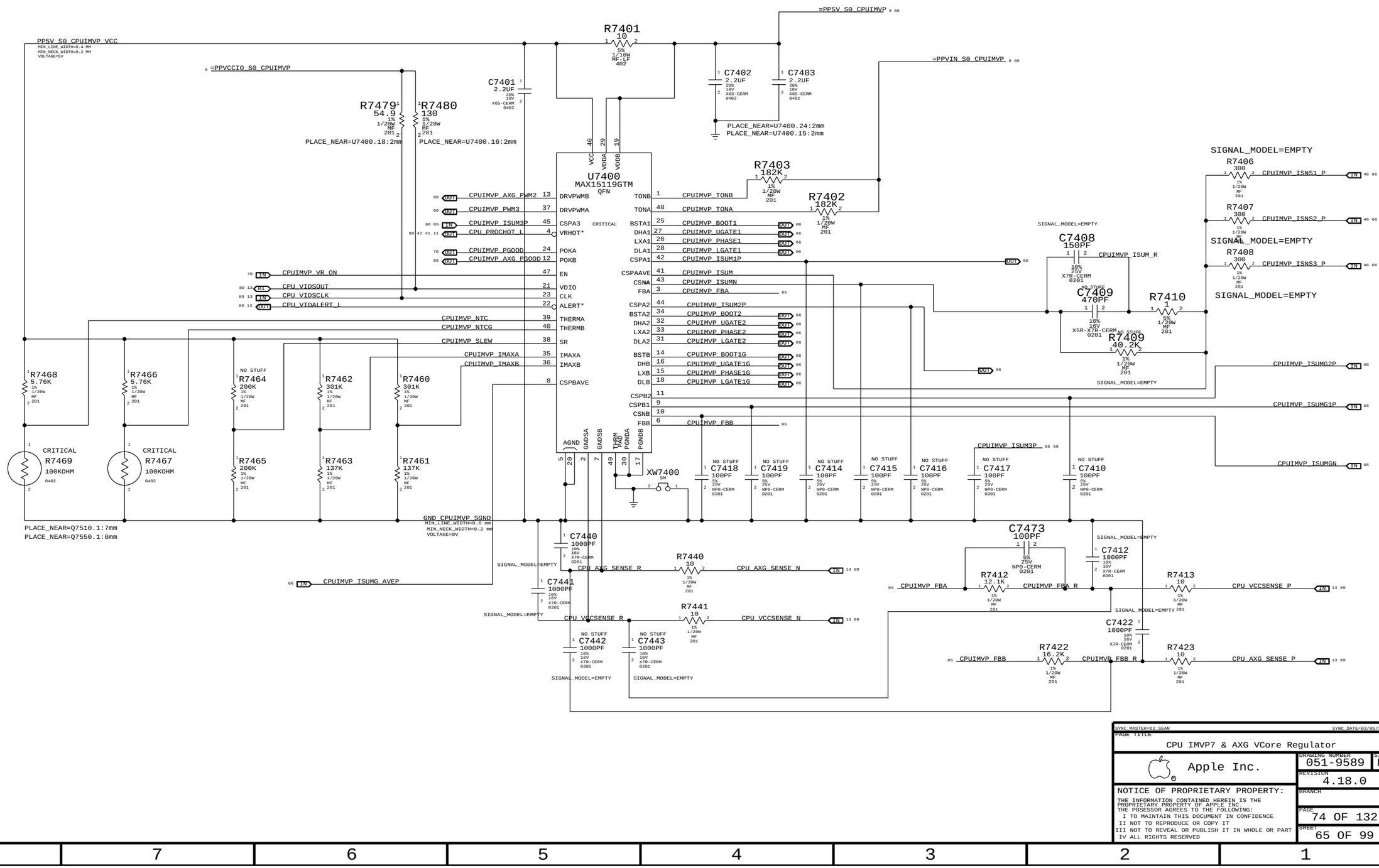

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2013

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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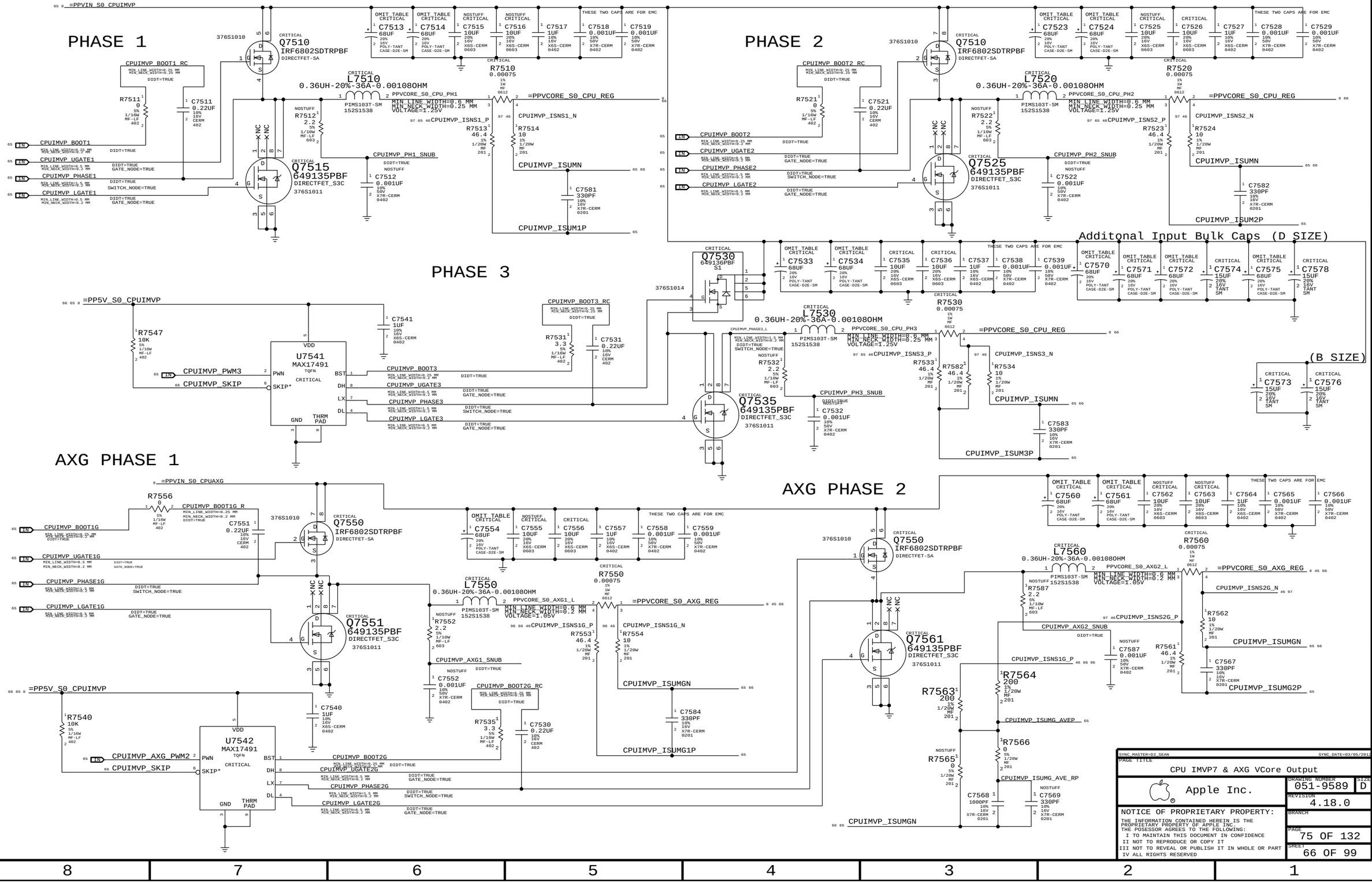
PHASE 1
=PPVIN_S0_CPUIMVP
376S1010
Q7510
IRF6802SDTRPBF
DIRECTFET-SA
CRITICAL
L7510
0.36UH-20%-36A-0.001080HM
PPVCORE_S0_CPU_PH1
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
PIMS103T-SM
152S1538
R7510
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P
CPUIMVP_ISUMN
CPUIMVP_ISUM1P
CPUIMVP_BOOT1_RC
R7511
0
C7511
0.22UF
R7512
2.2
CPUIMVP_PH1_SNUB
C7512
0.001UF
R7513
46.4
R7514
10
C7581
330PF
Q7515
649135PBF
DIRECTFET_S3C
376S1011
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
DIDT=TRUE
SWITCH_NODE=TRUE
GATE_NODE=TRUE
C7513
C7514
C7515
C7516
C7517
C7518
0.001UF
C7519
0.001UF
OMIT_TABLE CRITICAL
NOSTUFF CRITICAL
THESE TWO CAPS ARE FOR EMC
PHASE 2
376S1010
Q7510
IRF6802SDTRPBF
DIRECTFET-SA
CRITICAL
L7520
0.36UH-20%-36A-0.001080HM
PPVCORE_S0_CPU_PH2
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
PIMS103T-SM
152S1538
R7520
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS2_N
CPUIMVP_ISNS2_P
CPUIMVP_ISUMN
CPUIMVP_ISUM2P
CPUIMVP_BOOT2_RC
R7521
0
C7521
0.22UF
R7522
2.2
CPUIMVP_PH2_SNUB
C7522
0.001UF
R7523
46.4
R7524
10
C7582
330PF
Q7525
649135PBF
DIRECTFET_S3C
376S1011
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
DIDT=TRUE
GATE_NODE=TRUE
SWITCH_NODE=TRUE
C7523
C7524
C7525
C7526
C7527
C7528
0.001UF
C7529
0.001UF
OMIT_TABLE CRITICAL
NOSTUFF CRITICAL
THESE TWO CAPS ARE FOR EMC
PHASE 3
Q7530
649136PBF
S1
376S1014
CRITICAL
L7530
0.36UH-20%-36A-0.001080HM
PPVCORE_S0_CPU_PH3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
PIMS103T-SM
152S1538
R7530
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS3_N
CPUIMVP_ISNS3_P
CPUIMVP_ISUMN
CPUIMVP_ISUM3P
CPUIMVP_BOOT3_RC
R7531
3.3
C7531
0.22UF
R7532
2.2
CPUIMVP_PH3_SNUB
C7532
0.001UF
R7533
46.4
R7534
10
C7583
330PF
Q7535
649135PBF
DIRECTFET_S3C
376S1011
CPUIMVP_PHASE3_L
DIDT=TRUE
SWITCH_NODE=TRUE
C7533
C7534
C7535
C7536
C7537
C7538
0.001UF
C7539
0.001UF
Additonal Input Bulk Caps (D SIZE)
C7570
C7571
C7572
C7574
C7575
C7578
15UF
TANT
SM
(B SIZE)
C7573
C7576
=PP5V_S0_CPUIMVP
R7547
10K
C7541
1UF
U7541
MAX17491
TQFN
VDD
PWN
SKIP*
BST
DH
LX
DL
GND
THRM PAD
CRITICAL
CPUIMVP_PWM3
CPUIMVP_SKIP
CPUIMVP_BOOT3
CPUIMVP_UGATE3
CPUIMVP_PHASE3
CPUIMVP_LGATE3
AXG PHASE 1
=PPVIN_S0_CPUAXG
376S1010
Q7550
IRF6802SDTRPBF
DIRECTFET-SA
CRITICAL
L7550
0.36UH-20%-36A-0.001080HM
PPVCORE_S0_AXG1_L
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PIMS103T-SM
152S1538
R7550
0.00075
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
CPUIMVP_ISUMGN
CPUIMVP_ISUMG1P
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
DIDT=TRUE
SWITCH_NODE=TRUE
GATE_NODE=TRUE
R7556
0
CPUIMVP_BOOT1G_R
C7551
0.22UF
R7552
2.2
CPUIMVP_AXG1_SNUB
C7552
0.001UF
R7553
46.4
R7554
10
C7584
330PF
Q7551
649135PBF
DIRECTFET_S3C
376S1011
C7554
C7555
C7556
C7557
C7558
0.001UF
C7559
0.001UF
OMIT_TABLE CRITICAL
NOSTUFF CRITICAL
THESE TWO CAPS ARE FOR EMC
AXG PHASE 2
376S1010
Q7550
IRF6802SDTRPBF
DIRECTFET-SA
CRITICAL
L7560
0.36UH-20%-36A-0.001080HM
PPVCORE_S0_AXG2_L
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PIMS103T-SM
152S1538
R7560
0.00075
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS2G_N
CPUIMVP_ISNS2G_P
CPUIMVP_ISUMGN
CPUIMVP_ISUMG2P
CPUIMVP_AXG2_SNUB
R7587
2.2
C7587
0.001UF
R7561
46.4
R7562
10
C7567
330PF
Q7561
649135PBF
DIRECTFET_S3C
376S1011
CPUIMVP_ISNS1G_P
CPUIMVP_ISUMG_AVE
CPUIMVP_ISUMG_AVE_RP
R7563
200
R7564
200
R7565
0
R7566
0
C7568
1000PF
C7569
330PF
CPUIMVP_ISUMGN
C7560
C7561
C7562
C7563
C7564
C7565
0.001UF
C7566
0.001UF
OMIT_TABLE CRITICAL
NOSTUFF CRITICAL
THESE TWO CAPS ARE FOR EMC
=PP5V_S0_CPUIMVP
R7540
10K
C7540
1UF
U7542
MAX17491
TQFN
VDD
PWN
SKIP*
BST
DH
LX
DL
GND
THRM PAD
CRITICAL
CPUIMVP_AXG_PWM2
CPUIMVP_SKIP
CPUIMVP_BOOT2G
CPUIMVP_UGATE2G
CPUIMVP_PHASE2G
CPUIMVP_LGATE2G
R7535
3.3
C7530
0.22UF
CPUIMVP_BOOT2G_RC
DIDT=TRUE
SWITCH_NODE=TRUE
GATE_NODE=TRUE
SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012
PAGE TITLE
CPU IMVP7 & AXG VCore Output
Apple Inc.
DRAWING NUMBER
051-9589
SIZE
D
REVISION
4.18.0
BRANCH
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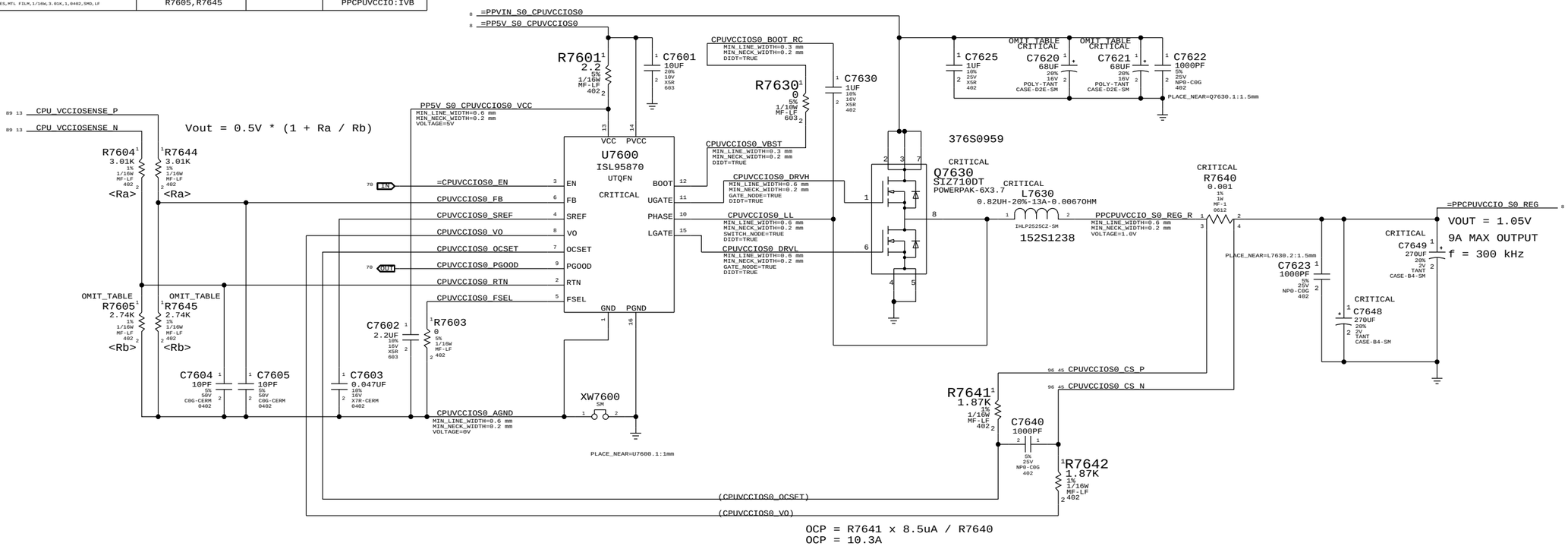
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	RES,MTL FILM,1/16W,2.74K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:SNB
114S0264	2	RES,MTL FILM,1/16W,3.01K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:IVB



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

CPU VCCIO (1V0R1V05 S0) POWER SUPPLY

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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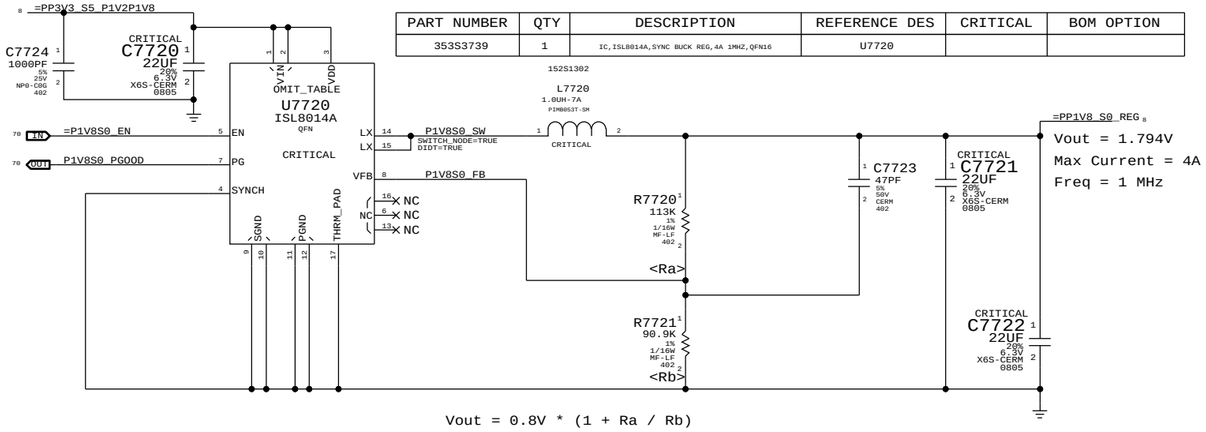
1.8V S0 Regulator

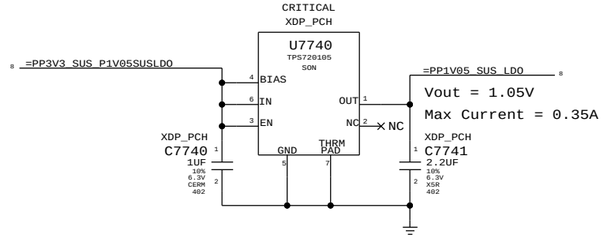


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3739	1	IC,ISL8014A,SYNC BUCK REG,4A 1MHZ,QFN16	U7720		

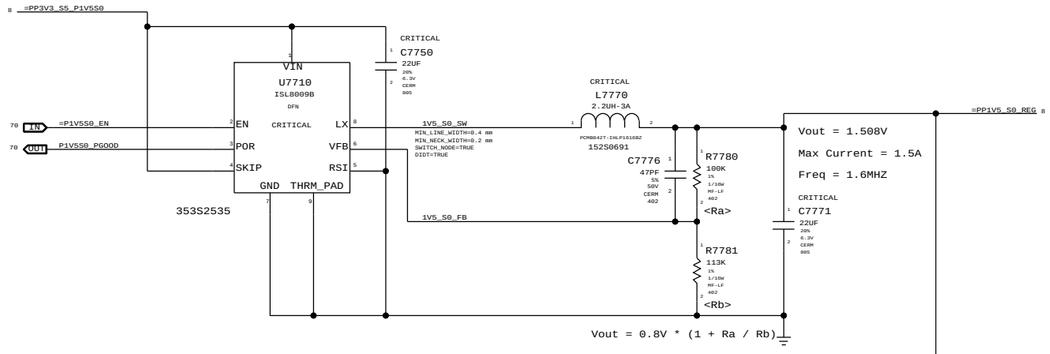
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

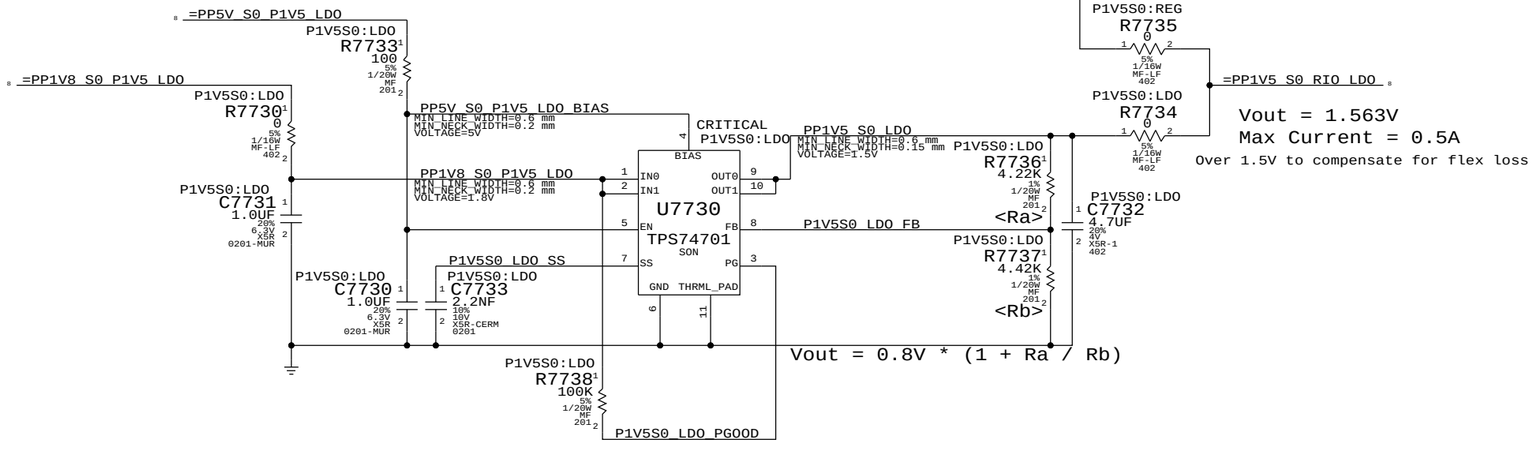
Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



1.5V S0 Regulator



1.5V S0 LDO (RIO)



SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	Misc Power Supplies
	Apple Inc.
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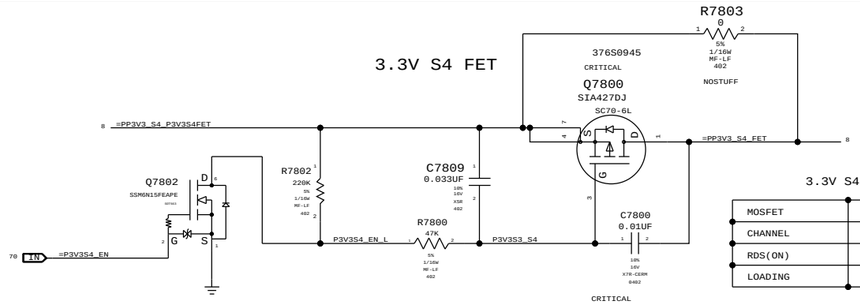
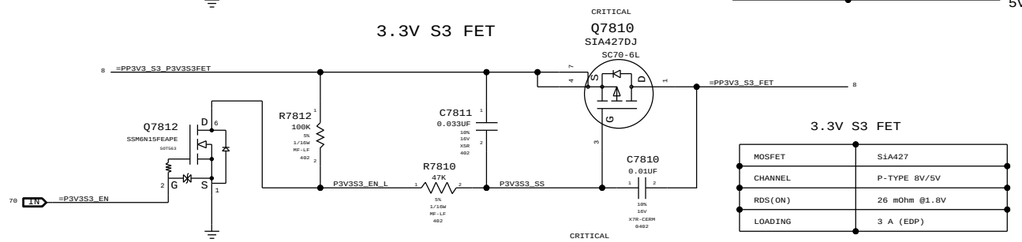
3.3V S4 FET



3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

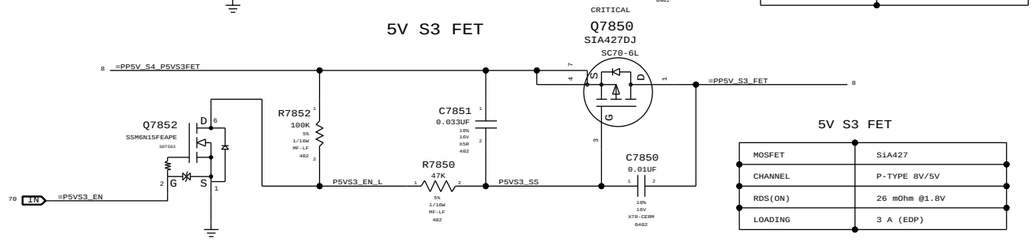
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

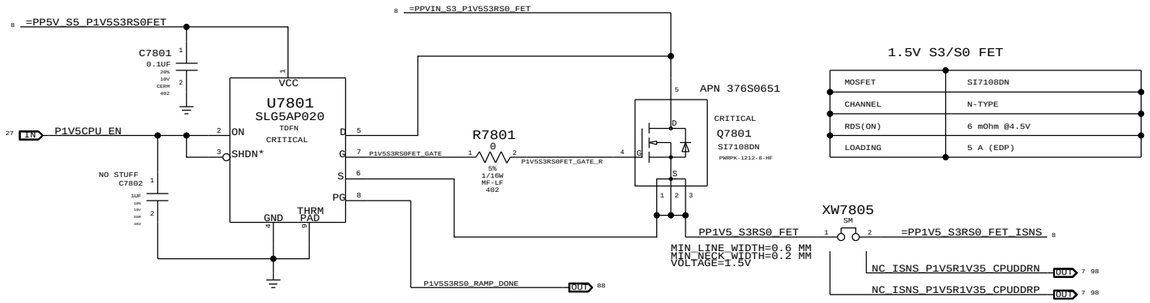
5V S3 FET



5V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

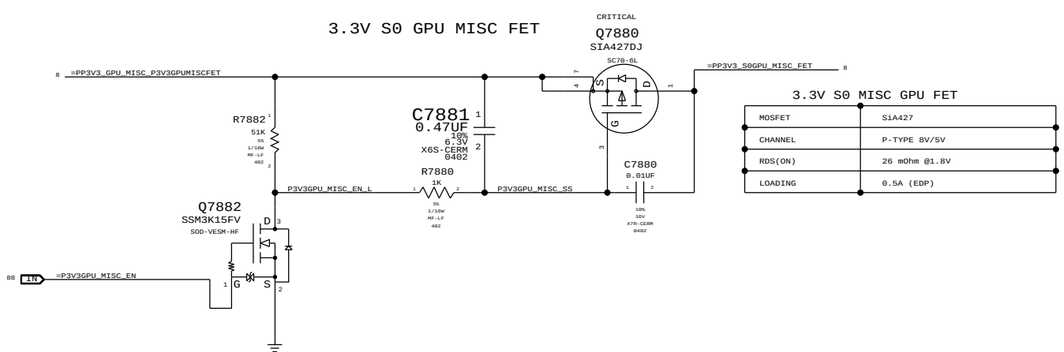
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 GPU MISC FET

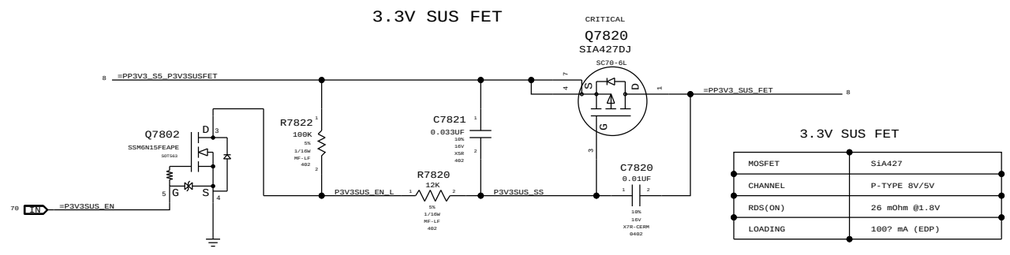


3.3V S0 MISC GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5A (EDP)

5V_SUS FET INPUT FILTER

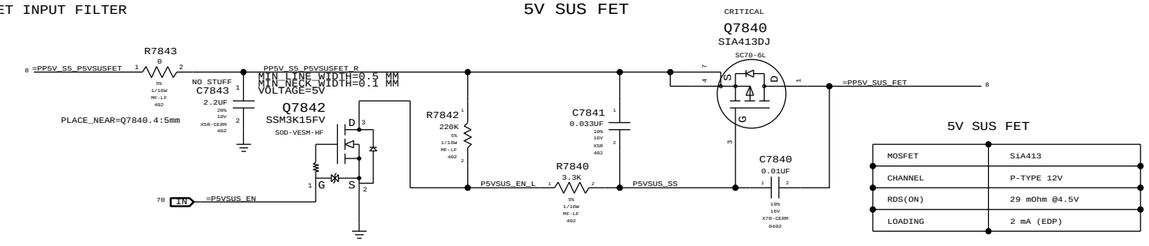
3.3V SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

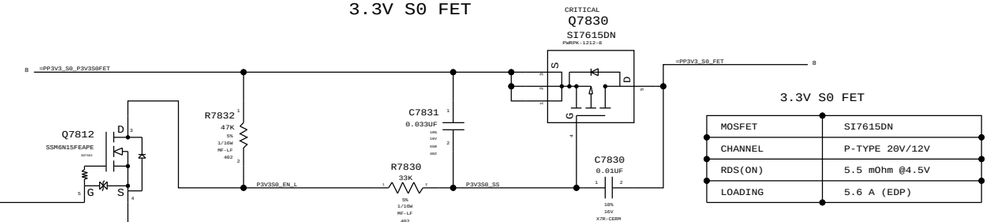
5V SUS FET



5V SUS FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

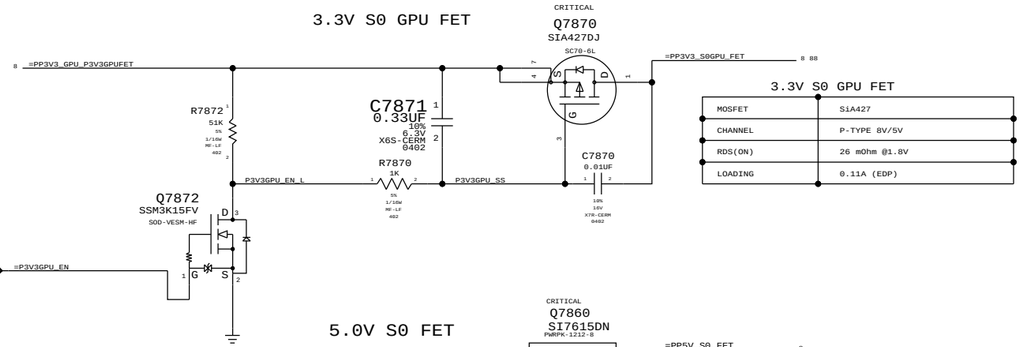
3.3V S0 FET



3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

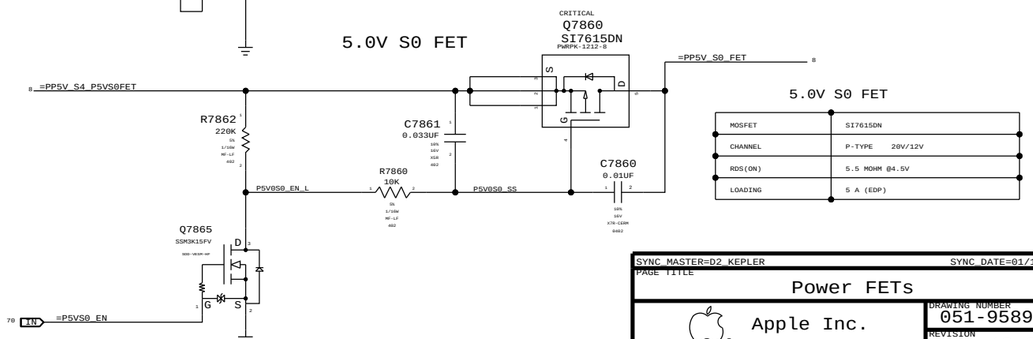
3.3V S0 GPU FET



3.3V S0 GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	5 A (EDP)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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S5 Rail Enables & PGOOD

63 OUT =P5VS5_EN
42 41 IN SMC_PM_G2_EN MAKE_BASE=TRUE
R7940 100 5% 1/16W MF-LF 402
PLACE_NEAR=U7201.21:7mm
P3V3S5_EN MAKE_BASE=TRUE
=P3V3S5_EN OUT 63
C7942 0.0033UF 10% 50V X7R-CERM 0402 NO STUFF

8 =PP3V42_G3H_PWRCTL
PLACE_NEAR=U7201.20:7mm
R7941 100K 5% 1/16W MF-LF 402
63 P3V3S5_PGOOD
S5_PWRGD MAKE_BASE=TRUE OUT 41
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

5V, 3.3V, DDR S3 ENABLE

41 40 38 34 27 18 7 IN PM_SLP_S4_L
PM_SLP_S4_L:100K pull down in PCH page
R7911 5.1K 5% 1/16W MF-LF 402 PLACE_NEAR=U7300.16:6mm
R7912 0 5% 1/16W MF-LF 402 PLACE_NEAR=Q7812.2:6mm
R7913 0 5% 1/16W MF-LF 402 PLACE_NEAR=Q7842.2:6MM
R7914 3.3K 5% 1/20W MF 201 PLACE_NEAR=U5701.4:6MM
TPAD_VBUS_EN OUT 49
P5VS3_EN MAKE_BASE=TRUE =P5VS3_EN OUT 69
P3V3S3_EN MAKE_BASE=TRUE =P3V3S3_EN OUT 69
DDRREG_EN MAKE_BASE=TRUE =DDRREG_EN OUT 64
C7910 0.47UF 10% 6.3V CERM-X5R 402
C7912 0.47UF 10% 6.3V CERM-X5R 402 NO STUFF
C7913 0.47UF 10% 6.3V CERM-X5R 402 NO STUFF
C7914 0.47UF 10% 6.3V CERM-X5R 402 NO STUFF

3.3V S4 ENABLE

70 8 =PP3V3_S5_PWRCTL
PLACE_NEAR=U7940.1:2.3mm
C7970 0.1uF 20% 10V CERM 402
PM_SLP_S5_L:100K pull down on PCH page
41 18 IN PM_SLP_S5_L
U7970 74LVC1G32 SOT891
P5V3V3_S4_EN MAKE_BASE=TRUE
=P5VS4_TPAD_EN OUT 49
=P3V3S4_EN OUT 69
=TBTAPWRSW_EN OUT 84
=TBTBPWRSW_EN OUT 85
NCX
42 41 IN SMC_S4_WAKESRC_EN MAKE_BASE=TRUE
NOSTUFF R7915 0 5% 1/16W MF-LF 402
R7975 0 5% 1/20W MF 201 MAKE_BASE=TRUE
P5VS4_EN =P5VS4_EN OUT 63
NO STUFF C7975 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

70 41 24 IN ALL_SYS_PWRGD
R7974 0 5% 1/16W MF-LF 402 PLACE_NEAR=U7400.7:5mm
CPUIMVP_VR_ON OUT 65

3.3V/5.0V Sus ENABLE

70 8 =PP3V3_S5_PWRCTL
PLACE_NEAR=U7940.1:2.3mm
C7940 0.1uF 20% 10V CERM 402
VCC U7940 74AUP1G3208 SOT891
SMC_BATLOW_L:100K pull up on SMC page
42 41 IN SMC_BATLOW_L
PM_SLP_SUS_L:100K pull down on PCH page
18 IN PM_SLP_SUS_L
PM_SUS_EN MAKE_BASE=TRUE
=P5VSUS_EN OUT 69
=P3V3SUS_EN OUT 69
NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

70 41 38 27 18 7 IN PM_SLP_S3_L
PM_SLP_S3_L:100K pull down in PCH page
R7978 100 5% 1/16W MF-LF 402
(PM_SLP_S3_R_L)
PM_SLP_S3_R_L MAKE_BASE=TRUE
R7987 33K 5% 1/16W MF-LF 402 PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7600.3:6mm
R7985 20K 5% 1/16W MF-LF 402 PLACE_NEAR=U7760.4:6mm
R7988 10K 5% 1/16W MF-LF 402 PLACE_NEAR=U7710.2:6mm
R7986 5.1K 5% 1/16W MF-LF 402 PLACE_NEAR=U7720.5:6mm
=P5VS0_EN OUT 69
=P3V3S0_EN OUT 39 69
=PBUSVSENS_EN OUT 45
=TBT_S0_EN OUT 84 85
P1V8S0_EN MAKE_BASE=TRUE =P1V8S0_EN OUT 68
P1V5S0_EN MAKE_BASE=TRUE =P1V5S0_EN OUT 68
PCHVCCIOS0_EN MAKE_BASE=TRUE =PCHVCCIOS0_EN OUT 87
CPUVCCIOS0_EN MAKE_BASE=TRUE =CPUVCCIOS0_EN OUT 67
PVCCSA_EN MAKE_BASE=TRUE =PVCCSA_EN OUT 62
C7987 0.47UF 10% 6.3V CERM-X5R 402
C7981 0.47UF 10% 6.3V CERM-X5R 402
C7985 1UF 10% 6.3V CERM-X5R 402
C7988 0.47UF 10% 6.3V CERM-X5R 402
C7986 0.47UF 10% 6.3V X6S-CERM 0402

CHGR VFRQ Generation

8 61 =PP3V42_G3H_CHGR
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ OUT 61
Q7931 SSM3K15FV SOD-VESM-HF
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

8 =PP3V3_S0_VMON
R7951 15.0K 1% 1/16W MF-LF 402
8 =PP3V3_S5_VMON
R7956 150K 1% 1/16W MF-LF 402
R7953 1K 5% 1/16W MF-LF 402 VMON_3V3_DIV
R7952 7.15K 1% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402 VMON_Q2_BASE
70 8 =PP1V5_S3RS0_VMON
PP1V5_S3RS0
R7955 1K 5% 1/16W MF-LF 402 VMON_Q3_BASE
70 8 =PP1V05_S0_VMON
VMON_Q4_BASE
S0PGD_C
ALL_SYS_PWRGD 24 41 70
Q7950 ASMCC0179 DFN2015H4-8 Q1 Q2 Q3 Q4 CRITICAL NC NC
353S2809 S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

=PP3V3_S5_PWRCTL
PLACE_NEAR=U7930.6:2.3mm
C7930 0.1uF 20% 10V CERM 402
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
CRITICAL
U7930 TPS3808G33DBVRG4 SOT23-6 VDD SENSE CT GND RESET* MR*
=PP3V3_SUS_CNTRL 5
Sus_PGOOD_CT 4
C7931 0.001UF 20% 50V CERM 402 NO STUFF
PM_RSMRST_L 1
PM_RSMRST_L goes to U1800.C21
SUS_PGOOD_MR_L 3
NOSTUFF R7930 0 5% 1/20W MF 201
=PP3V3_SUS_CNTRL 8 70
R7933 100K 5% 1/16W MF-LF 402
Could stuff to satisfy PCH power down timing t235

PCH S0 PWRGD

8 =PP3V3_S5_PCHPWRGD
25 8 =PP3V3_S0_SB_PM
R7950 1K 5% 1/16W MF-LF 402
C7950 0.1UF 20% 10V CERM 402
CKPLUS_WAIVE=UNCONNECTED_PINS
70 41 24 IN ALL_SYS_PWRGD
65 IN CPUIMVP_PGOOD
U7950 74LVC2G08GT SOT833 08
PLACE_NEAR=U1800.p12:7mm
PM_S0_PGOOD OUT 18
U7950 74LVC2G08GT SOT833 08
SYS_PWROK_R
R7949 1K 5% 1/16W MF-LF 402
PM_PCH_SYS_PWROK OUT 18 24 41
PM_PCH_APWROK OUT 18
42 41 37 SMC_DELAYED_PWRGD
R7948 0 5% 1/16W MF-LF 402
PM_PCH_PWROK MAKE_BASE=TRUE OUT 18 25

S0 Rail PGOOD Circuitry
(ISL Version in development)

88 8 =PP3V3_S0_PWRCTL
R7967 10K 5% 1/16W MF-LF 402
P1V5S0_PGOOD from U7710
68 IN P1V5S0_PGOOD R7968 100 5% 1/16W MF-LF 402
68 IN P1V8S0_PGOOD R7966 100 5% 1/16W MF-LF 402
63 IN P5VS4_PGOOD R7965 100 5% 1/16W MF-LF 402
67 IN CPUVCCIOS0_PGOOD R7964 100 5% 1/16W MF-LF 402
87 IN PCHVCCIOS0_PGOOD R7969 100 5% 1/16W MF-LF 402
62 IN PVCCSA_PGOOD R7963 100 5% 1/16W MF-LF 402
OUT 24 41 70
Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V
8 =P5VS_S0_VMON
70 8 =PP1V5_S3RS0_VMON
S0PGOOD_ISL R7960 6.04K 1% 1/16W MF-LF 402
70 8 =PP1V05_S0_VMON
S0PGOOD_ISL R7961 15.0K 1% 1/16W MF-LF 402
OMIT_TABLE
70 8 =PP3V3_S0_VMON
S0PGOOD_ISL C7960 0.1UF 20% 10V X7R-CERM 0402
S0PGOOD_ISL R7970 10K 1% 1/16W MF-LF 402
S0PGOOD_ISL R7972 6.04K 1% 1/16W MF-LF 402
P5V_DIV_VMON
S0PGOOD_ISL R7971 10K 1% 1/16W MF-LF 402
P1V05_DIV_VMON
S0PGOOD_ISL R7973 15.0K 1% 1/16W MF-LF 402
P1V05_VID_VMON
U7960 ISL88042IRTEZ TDFN VDD V2MON V3MON V4MON GND THRM_PAD MR* RST* CRITICAL (IPU) NC
S0PGOOD_ISL
353S2310
S0PGOOD_ISL R7962 330 5% 1/16W MF-LF 402
ALL_SYS_PWRGD_R
ALL_SYS_PWRGD

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L OUT 34
Q7925 SSM3K15FV SOD-VESM-HF
AP_PWR_EN IN 19 24 34
AC_EN_L
Q7920 SSM6N15FEAPE SOT563
NO STUFF R7929 0 5% 1/16W MF-LF 402
Q7920 SSM6N15FEAPE SOT563
42 41 18 IN SMC_ADAPTER_EN
70 41 38 27 18 7 IN PM_SLP_S3_L

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0315	1	RES,MTL FILM,1/16W,10K,1,0402,SMD,LF	R7971		PPDDR:1V5
114S0323	1	RES,MTL FILM,1/16W,12.4K,1,0402,SMD,LF	R7971		PPDDR:1V35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
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Power Control 1/ENABLE
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Page Notes

Power aliases required by this page:
- +PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

89 9	IN	PEG_R2D_C_P<0>	C8020 0.22UF GND_VOID=TRUE	PEG_R2D_P<0>	71 88 89
89 9	IN	PEG_R2D_C_N<0>	C8021 0.22UF GND_VOID=TRUE	PEG_R2D_N<0>	71 88 89
89 9	IN	PEG_R2D_C_P<1>	C8022 0.22UF GND_VOID=TRUE	PEG_R2D_P<1>	71 89
89 9	IN	PEG_R2D_C_N<1>	C8023 0.22UF GND_VOID=TRUE	PEG_R2D_N<1>	71 89
89 9	IN	PEG_R2D_C_P<2>	C8024 0.22UF GND_VOID=TRUE	PEG_R2D_P<2>	71 89
89 9	IN	PEG_R2D_C_N<2>	C8025 0.22UF GND_VOID=TRUE	PEG_R2D_N<2>	71 89
89 9	IN	PEG_R2D_C_P<3>	C8026 0.22UF GND_VOID=TRUE	PEG_R2D_P<3>	71 88 89
89 9	IN	PEG_R2D_C_N<3>	C8027 0.22UF GND_VOID=TRUE	PEG_R2D_N<3>	71 88 89
89 9	IN	PEG_R2D_C_P<4>	C8028 0.22UF GND_VOID=TRUE	PEG_R2D_P<4>	71 89
89 9	IN	PEG_R2D_C_N<4>	C8029 0.22UF GND_VOID=TRUE	PEG_R2D_N<4>	71 89
89 9	IN	PEG_R2D_C_P<5>	C8030 0.22UF GND_VOID=TRUE	PEG_R2D_P<5>	71 88 89
89 9	IN	PEG_R2D_C_N<5>	C8031 0.22UF GND_VOID=TRUE	PEG_R2D_N<5>	71 88 89
89 9	IN	PEG_R2D_C_P<6>	C8032 0.22UF GND_VOID=TRUE	PEG_R2D_P<6>	71 89
89 9	IN	PEG_R2D_C_N<6>	C8033 0.22UF GND_VOID=TRUE	PEG_R2D_N<6>	71 89
89 9	IN	PEG_R2D_C_P<7>	C8034 0.22UF GND_VOID=TRUE	PEG_R2D_P<7>	71 88 89
89 9	IN	PEG_R2D_C_N<7>	C8035 0.22UF GND_VOID=TRUE	PEG_R2D_N<7>	71 88 89

89 71	PEG_D2R_C_P<0>	C8055 0.22UF GND_VOID=TRUE	PEG_D2R_P<0>	OUT	9 88 89
89 71	PEG_D2R_C_N<0>	C8056 0.22UF GND_VOID=TRUE	PEG_D2R_N<0>	OUT	9 88 89
89 71	PEG_D2R_C_P<1>	C8057 0.22UF GND_VOID=TRUE	PEG_D2R_P<1>	OUT	9 89
89 71	PEG_D2R_C_N<1>	C8058 0.22UF GND_VOID=TRUE	PEG_D2R_N<1>	OUT	9 89
89 71	PEG_D2R_C_P<2>	C8059 0.22UF GND_VOID=TRUE	PEG_D2R_P<2>	OUT	9 89
89 71	PEG_D2R_C_N<2>	C8060 0.22UF GND_VOID=TRUE	PEG_D2R_N<2>	OUT	9 89
89 71	PEG_D2R_C_P<3>	C8061 0.22UF GND_VOID=TRUE	PEG_D2R_P<3>	OUT	9 89
89 71	PEG_D2R_C_N<3>	C8062 0.22UF GND_VOID=TRUE	PEG_D2R_N<3>	OUT	9 89
89 71	PEG_D2R_C_P<4>	C8063 0.22UF GND_VOID=TRUE	PEG_D2R_P<4>	OUT	9 88 89
89 71	PEG_D2R_C_N<4>	C8064 0.22UF GND_VOID=TRUE	PEG_D2R_N<4>	OUT	9 88 89
89 71	PEG_D2R_C_P<5>	C8065 0.22UF GND_VOID=TRUE	PEG_D2R_P<5>	OUT	9 89
89 71	PEG_D2R_C_N<5>	C8066 0.22UF GND_VOID=TRUE	PEG_D2R_N<5>	OUT	9 89
89 71	PEG_D2R_C_P<6>	C8067 0.22UF GND_VOID=TRUE	PEG_D2R_P<6>	OUT	9 89
89 71	PEG_D2R_C_N<6>	C8068 0.22UF GND_VOID=TRUE	PEG_D2R_N<6>	OUT	9 89
89 71	PEG_D2R_C_P<7>	C8069 0.22UF GND_VOID=TRUE	PEG_D2R_P<7>	OUT	9 88 89
89 71	PEG_D2R_C_N<7>	C8070 0.22UF GND_VOID=TRUE	PEG_D2R_N<7>	OUT	9 88 89

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89 88 71	PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14
89 88 71	PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14
89 71	PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14
89 71	PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14
89 71	PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15
89 71	PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15
89 88 71	PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16
89 88 71	PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16
89 71	PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17
89 71	PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17
89 88 71	PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17
89 88 71	PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17
89 71	PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18
89 71	PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18
89 88 71	PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19
89 88 71	PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19
NC		AP20	PEX_RX8	PEX_TX8	AK20
NC		AP21	PEX_RX8*	PEX_TX8*	AJ20
NC		AN21	PEX_RX9	PEX_TX9	AH20
NC		AM21	PEX_RX9*	PEX_TX9*	AG20
NC		AN23	PEX_RX10	PEX_TX10	AK21
NC		AM23	PEX_RX10*	PEX_TX10*	AJ21
NC		AP23	PEX_RX11	PEX_TX11	AL22
NC		AP24	PEX_RX11*	PEX_TX11*	AK22
NC		AN24	PEX_RX12	PEX_TX12	AK23
NC		AM24	PEX_RX12*	PEX_TX12*	AJ23
NC		AN26	PEX_RX13	PEX_TX13	AH23
NC		AM26	PEX_RX13*	PEX_TX13*	AG23
NC		AP26	PEX_RX14	PEX_TX14	AK24
NC		AP27	PEX_RX14*	PEX_TX14*	AJ24
NC		AN27	PEX_RX15	PEX_TX15	AL25
NC		AM27	PEX_RX15*	PEX_TX15*	AK25
92 17	PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26
92 17	PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26
78 9	GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29
78 71	PEX_CLKREQ_L_R	AK12	PEX_CLKREQ*	PEX_SVDD_3V3	AG12
NC		AJ11	PEX_WAKE*		

89 71	PEG_D2R_P<0>	AK14	PEG_D2R_C_P<0>	71 89
89 71	PEG_D2R_N<0>	AJ14	PEG_D2R_C_N<0>	71 89
89 71	PEG_D2R_P<1>	AH14	PEG_D2R_C_P<1>	71 89
89 71	PEG_D2R_N<1>	AG14	PEG_D2R_C_N<1>	71 89
89 71	PEG_D2R_P<2>	AK15	PEG_D2R_C_P<2>	71 89
89 71	PEG_D2R_N<2>	AJ15	PEG_D2R_C_N<2>	71 89
89 88 71	PEG_D2R_P<3>	AL16	PEG_D2R_C_P<3>	71 89
89 88 71	PEG_D2R_N<3>	AK16	PEG_D2R_C_N<3>	71 89
89 71	PEG_D2R_P<4>	AK17	PEG_D2R_C_P<4>	71 89
89 71	PEG_D2R_N<4>	AJ17	PEG_D2R_C_N<4>	71 89
89 88 71	PEG_D2R_P<5>	AH17	PEG_D2R_C_P<5>	71 89
89 88 71	PEG_D2R_N<5>	AG17	PEG_D2R_C_N<5>	71 89
89 71	PEG_D2R_P<6>	AK18	PEG_D2R_C_P<6>	71 89
89 71	PEG_D2R_N<6>	AJ18	PEG_D2R_C_N<6>	71 89
89 88 71	PEG_D2R_P<7>	AL19	PEG_D2R_C_P<7>	71 89
89 88 71	PEG_D2R_N<7>	AK19	PEG_D2R_C_N<7>	71 89
NC		AK20	NC	
NC		AJ20	NC	
NC		AH20	NC	
NC		AG20	NC	
NC		AK21	NC	
NC		AJ21	NC	
NC		AL22	NC	
NC		AK22	NC	
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NC		AJ23	NC	
NC		AH23	NC	
NC		AG23	NC	
NC		AK24	NC	
NC		AJ24	NC	
NC		AL25	NC	
NC		AK25	NC	
95 92		AJ26	PEX_TSTCLK_O_P	
95 92		AK26	PEX_TSTCLK_O_N	

=PP3V3_GPU_VDD33
79 78 77 8

R8001
10K
1% 1/20W MF 201
PEX_CLKREQ_L_R
78 71

NOSTUFF
R8002
200
1% 1/20W MF 201

R8000
0 GPU_RESET_R_L
MF 5% 1/20W 201

R8005
2.49K
1% 1/20W MF 201
GPU_PEX_TERMP

PP3V3_GPU_PEX_PLL_HVDD
79

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	KEPLER PCI-E
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
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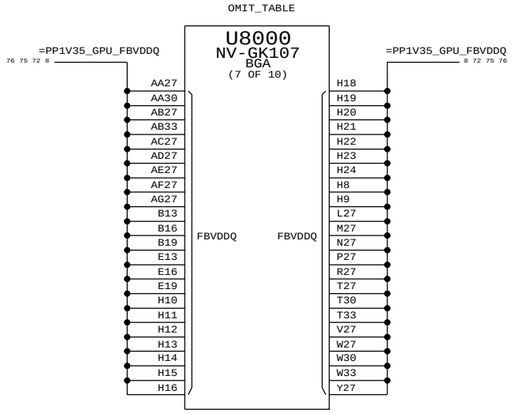
OMIT_TABLE



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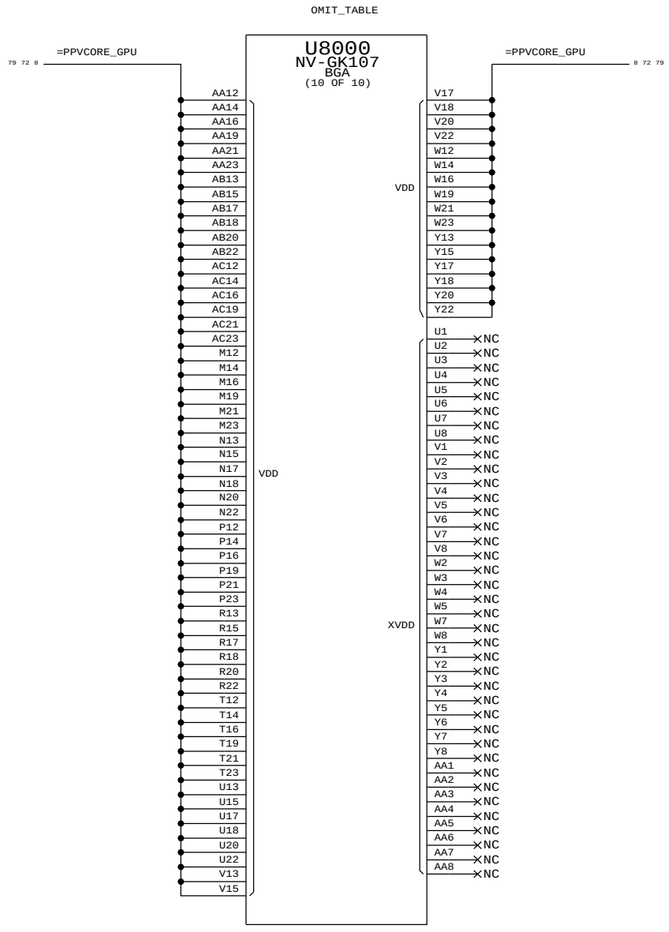


Page Notes

Power aliases required by this page:

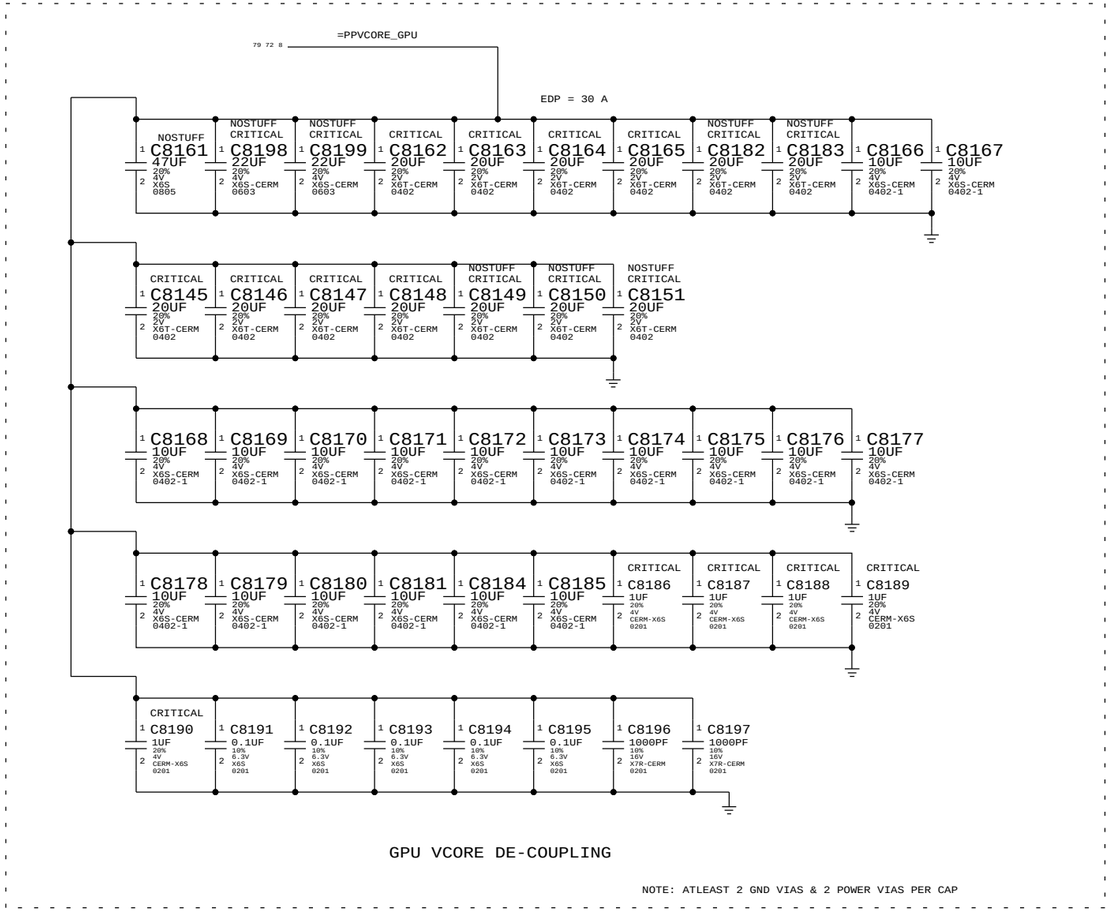
- =PPVCORE_GPU
- =PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

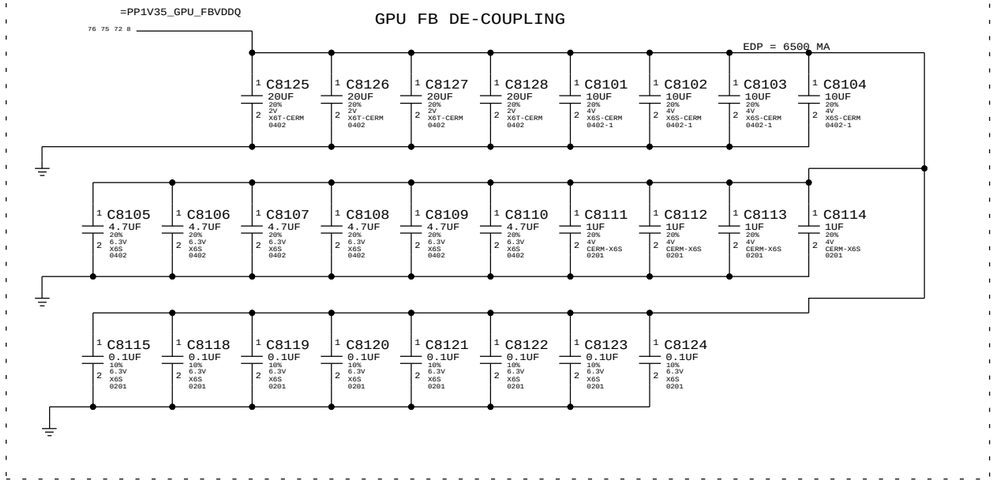
BOM options provided by this page:

(NONE)



GPU VCORE DE-COUPLING

NOTE: ATLEAST 2 GND VIAS & 2 POWER VIAS PER CAP



SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE

KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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NOTE:GDDR5 MODE H MAPPING

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MEM INTERFACE A

FB_A0_DQ<0>	L28	FBA_D0	U30	FBA_CMD0	FB_A0_CS_L	
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FB_A0_DQ<4>	N31	FBA_D4	R33	FBA_CMD4	FB_A0_A<5>	
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FB_A0_DQ<12>	G29	FBA_D12	U31	FBA_CMD12	FB_A0_RAS_L	
FB_A0_DQ<13>	E31	FBA_D13	V34	FBA_CMD13	FB_A0_RESET_L	73 75 95
FB_A0_DQ<14>	E32	FBA_D14	V33	FBA_CMD14	FB_A0_CKE_L	73 75 95
FB_A0_DQ<15>	F30	FBA_D15	Y32	FBA_CMD15	FB_A0_CAS_L	
FB_A0_DQ<16>	C34	FBA_D16	AA31	FBA_CMD16	FB_A1_CS_L	
FB_A0_DQ<17>	D32	FBA_D17	AA29	FBA_CMD17	FB_A1_A<3>	
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FB_A0_DQ<29>	L34	FBA_D29	Y34	FBA_CMD29	FB_A1_RESET_L	73 75 95
FB_A0_DQ<30>	L32	FBA_D30	Y33	FBA_CMD30	FB_A1_CKE_L	73 75 95
FB_A0_DQ<31>	L33	FBA_D31	V31	FBA_CMD31	FB_A1_CAS_L	
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FB_A1_DQ<23>	AK32	FBA_D55	AF32	FBA_DQS_RN7	NC	
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FB_A1_DQ<29>	AG34	FBA_D61	AE31	FBA_DQS_WP4	FB_A1_EDC<0>	
FB_A1_DQ<30>	AG32	FBA_D62	AK30	FBA_DQS_WP5	FB_A1_EDC<1>	
FB_A1_DQ<31>	AG33	FBA_D63	AN33	FBA_DQS_WP6	FB_A1_EDC<2>	
			AF33	FBA_DQS_WP7	FB_A1_EDC<3>	
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FB_A0_WCLK_P<1>	H34	FBA_WCK23	R28	FBA_DEBUG	GPU_FBA_DEBUG0	
FB_A0_WCLK_N<1>	J34	FBA_WCK23*	AC28	FBA_DEBUG	GPU_FBA_DEBUG1	
FB_A1_WCLK_P<0>	AG30	FBA_WCK45	J27	FB_CAL_PD_VDDQ	FB_CAL_PD_VDDQ	73
FB_A1_WCLK_N<0>	AG31	FBA_WCK45*	H27	FB_CAL_PU_GND	FB_CAL_PU_GND	73
FB_A1_WCLK_P<1>	AJ34	FBA_WCK67	H25	FB_CAL_TERM_GND	1 R8201 2 60.4 1% 1/20W MF 201	PLACE_NEAR=U8000.H25:8.4MM
FB_A1_WCLK_N<1>	AK34	FBA_WCK67*	E1	82 FB_CLAMP	FB_CLAMP	
	J30	FBA_WCKB01	R32	FB_CMD_RFU	1 R8261 2 10K 1% 1/20W 201	
NC	J31	FBA_WCKB01*	AC32	FB_CMD_RFU	NC	
NC	J32	FBA_WCKB23	F1	FB_VDDQ_SENSE	GPU_FBVDDQ_SENSE	OUT 74 97
NC	J33	FBA_WCKB23*	F2	FB_GND_SENSE	GPU_FBGND_SENSE	OUT 74 97
NC	AH31	FBA_WCKB45				
NC	AJ31	FBA_WCKB45*				
NC	AJ32	FBA_WCKB67				
NC	AJ33	FBA_WCKB67*				

95 75 73 FB_A0_RESET_L — 1 R8250 2 10K 1% 1/20W MF 201

95 75 73 FB_A1_RESET_L — 1 R8251 2 10K 1% 1/20W MF 201

FB_A0_CKE_L 73 75 95 — 1 R8252 2 10K 1% 1/20W MF 201

FB_A1_CKE_L 73 75 95 — 1 R8253 2 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 8 73

1 R8203 2 60.4 1% 1/20W MF 201

1 R8202 2 60.4 1% 1/20W MF 201

1 R8270 2 100 5% 1/20W MF 201

=PP1V35_GPU_S0_FB 8 73

1 R8258 2 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8000.H26:8.4MM

PLACE_NEAR=U8000.H26:8.4MM

FB_VREF 73

NOSTUFF 1 R8259 2 1.33K 1% 1/20W MF 201

NOSTUFF 1 C8260 2 0.1UF 10% 6.3V X6S 0201

PLACE_NEAR=U8000.H26:8.4MM

FB VREF GEN (TEST ONLY)

PLACE CLOSE TO BGA

73 FB_CAL_PU_GND — 1 R8204 2 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8000.H27:8.4MM

=PP1V35_GPU_S0_FB 8 73 — 1 R8205 2 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8000.J27:8.4MM

FB_CAL_PD_VDDQ 73

1 R8271 2 100 5% 1/20W MF 201

OMIT_TABLE

U8000
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

FB_B0_DQ<0>	G9	FBB_D0	D13	FBB_CMD0	FB_B0_CS_L	
FB_B0_DQ<1>	E9	FBB_D1	E14	FBB_CMD1	FB_B0_A<3>	
FB_B0_DQ<2>	G8	FBB_D2	F14	FBB_CMD2	FB_B0_A<2>	
FB_B0_DQ<3>	F9	FBB_D3	A12	FBB_CMD3	FB_B0_A<4>	
FB_B0_DQ<4>	F11	FBB_D4	B12	FBB_CMD4	FB_B0_A<5>	
FB_B0_DQ<5>	G11	FBB_D5	C14	FBB_CMD5	FB_B0_WE_L	
FB_B0_DQ<6>	F12	FBB_D6	B14	FBB_CMD6	FB_B0_A<7>	
FB_B0_DQ<7>	G12	FBB_D7	G15	FBB_CMD7	FB_B0_A<6>	
FB_B0_DQ<8>	G6	FBB_D8	F15	FBB_CMD8	FB_B0_ABI_L	
FB_B0_DQ<9>	F5	FBB_D9	E15	FBB_CMD9	FB_B0_A<8>	
FB_B0_DQ<10>	E6	FBB_D10	D15	FBB_CMD10	FB_B0_A<0>	
FB_B0_DQ<11>	F6	FBB_D11	A14	FBB_CMD11	FB_B0_A<1>	
FB_B0_DQ<12>	F4	FBB_D12	D14	FBB_CMD12	FB_B0_RAS_L	
FB_B0_DQ<13>	G4	FBB_D13	A15	FBB_CMD13	FB_B0_RESET_L	73 76 95
FB_B0_DQ<14>	E2	FBB_D14	B15	FBB_CMD14	FB_B0_CKE_L	73 76 95
FB_B0_DQ<15>	F3	FBB_D15	C17	FBB_CMD15	FB_B0_CAS_L	
FB_B0_DQ<16>	C2	FBB_D16	D18	FBB_CMD16	FB_B1_CS_L	
FB_B0_DQ<17>	D4	FBB_D17	E18	FBB_CMD17	FB_B1_A<3>	76 95 79 73 8
FB_B0_DQ<18>	D3	FBB_D18	F18	FBB_CMD18	FB_B1_A<2>	
FB_B0_DQ<19>	C1	FBB_D19	A20	FBB_CMD19	FB_B1_A<4>	
FB_B0_DQ<20>	B3	FBB_D20	B20	FBB_CMD20	FB_B1_A<5>	
FB_B0_DQ<21>	C4	FBB_D21	C18	FBB_CMD21	FB_B1_WE_L	
FB_B0_DQ<22>	B5	FBB_D22	B18	FBB_CMD22	FB_B1_A<7>	
FB_B0_DQ<23>	C5	FBB_D23	G18	FBB_CMD23	FB_B1_A<6>	
FB_B0_DQ<24>	A11	FBB_D24	G17	FBB_CMD24	FB_B1_ABI_L	
FB_B0_DQ<25>	C11	FBB_D25	F17	FBB_CMD25	FB_B1_A<8>	
FB_B0_DQ<26>	D11	FBB_D26	D16	FBB_CMD26	FB_B1_A<0>	
FB_B0_DQ<27>	B11	FBB_D27	A18	FBB_CMD27	FB_B1_A<1>	
FB_B0_DQ<28>	D8	FBB_D28	D17	FBB_CMD28	FB_B1_RAS_L	
FB_B0_DQ<29>	A8	FBB_D29	A17	FBB_CMD29	FB_B1_RESET_L	73 76 95
FB_B0_DQ<30>	C8	FBB_D30	B17	FBB_CMD30	FB_B1_CKE_L	73 76 95
FB_B0_DQ<31>	B8	FBB_D31	E17	FBB_CMD31	FB_B1_CAS_L	
FB_B1_DQ<0>	F24	FBB_D32				
FB_B1_DQ<1>	G23	FBB_D33	D12	FBB_CLK0	FB_B0_CLK_P	
FB_B1_DQ<2>	E24	FBB_D34	E12	FBB_CLK0*	FB_B0_CLK_N	
FB_B1_DQ<3>	G24	FBB_D35	E20	FBB_CLK1	FB_B1_CLK_P	
FB_B1_DQ<4>	D21	FBB_D36	F20	FBB_CLK1*	FB_B1_CLK_N	
FB_B1_DQ<5>	E21	FBB_D37				
FB_B1_DQ<6>	G21	FBB_D38	E11	FBB_DQM0	FB_B0_DBI_L<0>	
FB_B1_DQ<7>	F21	FBB_D39	E3	FBB_DQM1	FB_B0_DBI_L<1>	
FB_B1_DQ<8>	G27	FBB_D40	A3	FBB_DQM2	FB_B0_DBI_L<2>	
FB_B1_DQ<9>	D27	FBB_D41	C9	FBB_DQM3	FB_B0_DBI_L<3>	
FB_B1_DQ<10>	G26	FBB_D42	F23	FBB_DQM4	FB_B1_DBI_L<0>	
FB_B1_DQ<11>	E27	FBB_D43	F27	FBB_DQM5	FB_B1_DBI_L<1>	
FB_B1_DQ<12>	E29	FBB_D44	C30	FBB_DQM6	FB_B1_DBI_L<2>	
FB_B1_DQ<13>	F29	FBB_D45	A24	FBB_DQM7	FB_B1_DBI_L<3>	
FB_B1_DQ<14>	E30	FBB_D46				
FB_B1_DQ<15>	D30	FBB_D47	D9	FBB_DQS_RN0	NC	
FB_B1_DQ<16>	A32	FBB_D48	E4	FBB_DQS_RN1	NC	
FB_B1_DQ<17>	C31	FBB_D49	B2	FBB_DQS_RN2	NC	
FB_B1_DQ<18>	C32	FBB_D50	A9	FBB_DQS_RN3	NC	
FB_B1_DQ<19>	B32	FBB_D51	D22	FBB_DQS_RN4	NC	
FB_B1_DQ<20>	D29	FBB_D52	D28	FBB_DQS_RN5	NC	
FB_B1_DQ<21>	A29	FBB_D53	A30	FBB_DQS_RN6	NC	
FB_B1_DQ<22>	C29	FBB_D54	B23	FBB_DQS_RN7	NC	
FB_B1_DQ<23>	B29	FBB_D55				
FB_B1_DQ<24>	B21	FBB_D56	D10	FBB_DQS_WP0	FB_B0_EDC<0>	
FB_B1_DQ<25>	C23	FBB_D57	D5	FBB_DQS_WP1	FB_B0_EDC<1>	
FB_B1_DQ<26>	A21	FBB_D58	C3	FBB_DQS_WP2	FB_B0_EDC<2>	
FB_B1_DQ<27>	C21	FBB_D59	B9	FBB_DQS_WP3	FB_B0_EDC<3>	
FB_B1_DQ<28>	B24	FBB_D60	E23	FBB_DQS_WP4	FB_B1_EDC<0>	
FB_B1_DQ<29>	C24	FBB_D61	E28	FBB_DQS_WP5	FB_B1_EDC<1>	
FB_B1_DQ<30>	B26	FBB_D62	B30	FBB_DQS_WP6	FB_B1_EDC<2>	
FB_B1_DQ<31>	C26	FBB_D63	A23	FBB_DQS_WP7	FB_B1_EDC<3>	
FB_B0_WCLK_P<0>	F8	FBB_WCK01	H17	FBB_PLL_AVDD	PP1V05_GPU_FB_PLL_AVDD	73
FB_B0_WCLK_N<0>	E8	FBB_WCK01*	G14	FBB_DEBUG0	GPU_FBB_DEBUG0	73
FB_B0_WCLK_P<1>	A5	FBB_WCK23	G20	FBB_DEBUG1	GPU_FBB_DEBUG1	73
FB_B0_WCLK_N<1>	A6	FBB_WCK23*	H26	FB_VREF	FB_VREF	73
FB_B1_WCLK_P<0>	D24	FBB_WCK45	C12	FBB_CMD_RFU0	NC	
FB_B1_WCLK_N<0>	D25	FBB_WCK45*	C20	FBB_CMD_RFU1	NC	
FB_B1_WCLK_P<1>	B27	FBB_WCK67				
FB_B1_WCLK_N<1>	C27	FBB_WCK67*				
	D6	FBB_WCKB01				
NC	D7	FBB_WCKB01*				
NC	C6	FBB_WCKB23				
NC	B6	FBB_WCKB23*				
NC	F26	FBB_WCKB45				
NC	E26	FBB_WCKB45*				
NC	A26	FBB_WCKB67				
NC	A27	FBB_WCKB67*				

1 C8206 2 1UF 20% 4V CERM-X6S 0201

1 C8207 2 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 8 73

1 R8206 2 60.4 1% 1/20W MF 201

1 R8207 2 60.4 1% 1/20W MF 201

GPU_FBB_DEBUG0 73

GPU_FBB_DEBUG1 73

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

L8201
FERR-220-OHM-2A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD 8 73 79 — 1 0603 2 CRITICAL ESR = 0.050OHM — PP1V05_GPU_FB_PLL_AVDD 73

1 C8201 2 20UF 20% 2V X6T-CERM 0402

1 C8202 2 1UF 20% 4V CERM-X6S 0201

1 C8203 2 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

L8202
FERR-220-OHM-2A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD — 1 0603 2 CRITICAL ESR = 0.050OHM — PP1V05_GPU_FB_DLL_AVDD 73

1 C8208 2 20UF 20% 2V X6T-CERM 0402

1 C8204 2 1UF 20% 4V CERM-X6S 0201

1 C8205 2 0.1UF 10% 6.3V X6S 0201

95 76 73 FB_B0_RESET_L — 1 R8254 2 10K 1% 1/20W MF 201

95 76 73 FB_B1_RESET_L — 1 R8255 2 10K 1% 1/20W MF 201

73 76 95 FB_B0_CKE_L — 1 R8256 2 10K 1% 1/20W MF 201

73 76 95 FB_B1_CKE_L — 1 R8257 2 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH

FB_SW_LEG 76 75 OUT

Q8265 SSM3K15FV SOD-VESM-HF (3 D, 2 S, G 1)

GPU_ALT_VREF IN 78

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	KEPLER FRAME BUFFER I/F
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 82 OF 132
	SHEET 73 OF 99

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GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

U8350
ISL95870AH
UTQFN
CRITICAL

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

GPU 1V05 SUPPLY

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

U8310
ISL95870
UTQFN
CRITICAL

Vout = 0.5V * (1 + Ra / Rb)

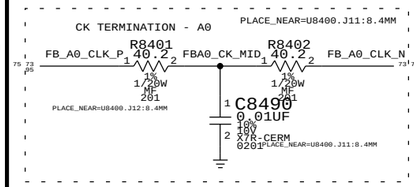
SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 83 OF 132
	SHEET 74 OF 99

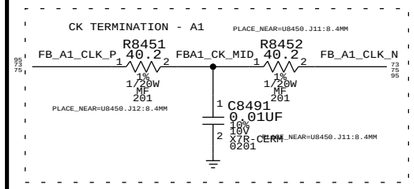
Page Notes

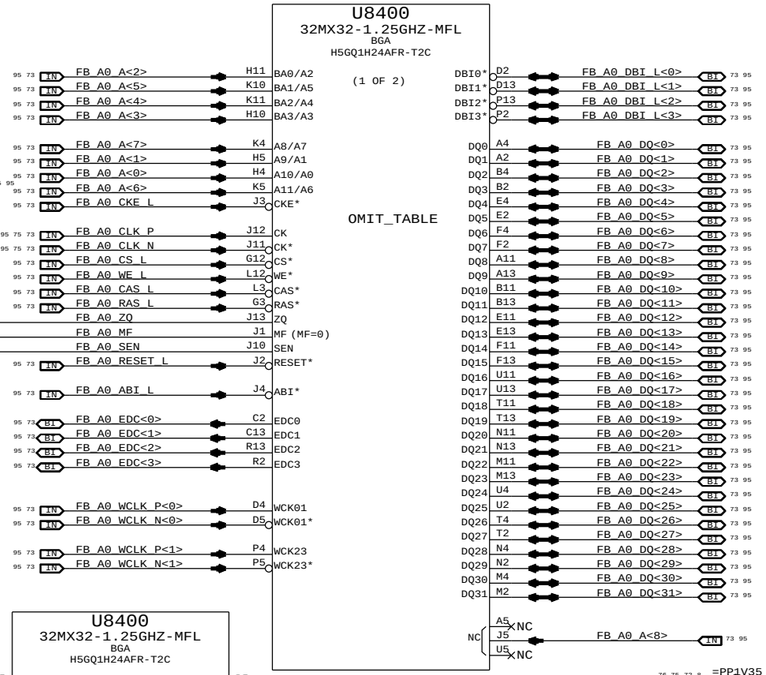
Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

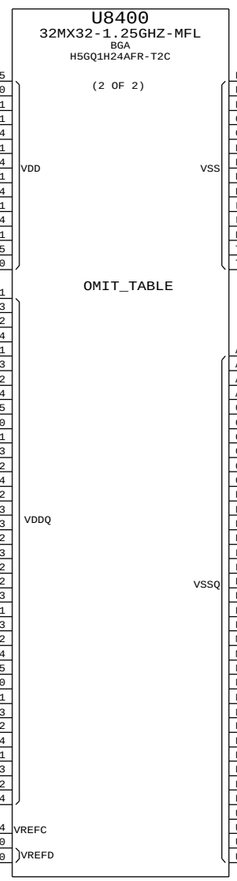
Signal aliases required by this page:
(NONE)

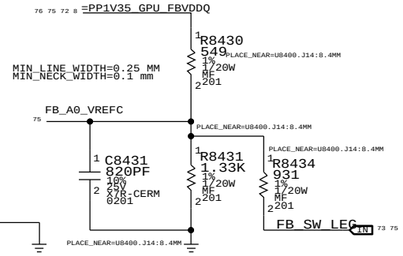
BOM options provided by this page:

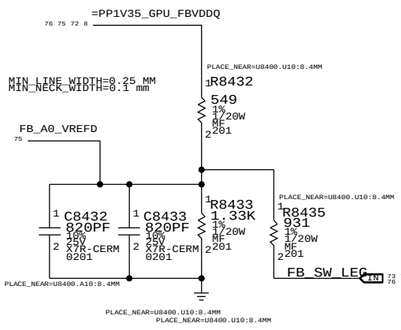


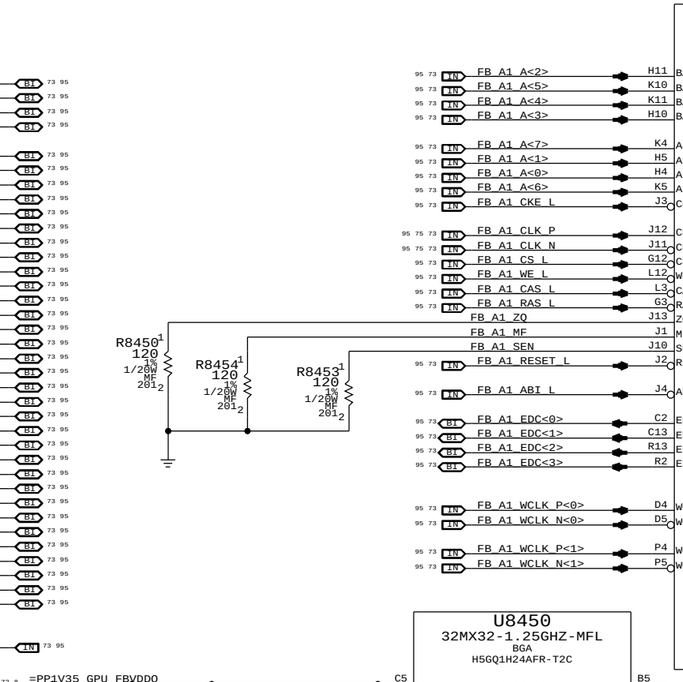


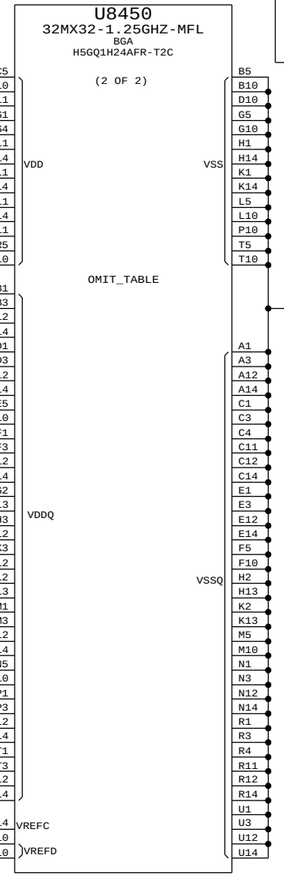


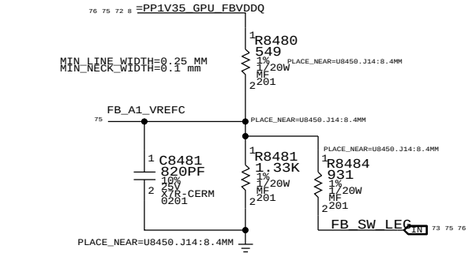


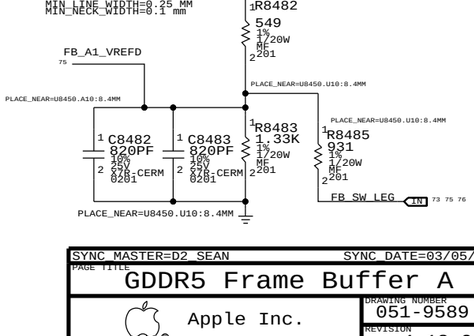












SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
REVISION: 4.18.0
BRANCH:
PAGE: 84 OF 132
SHEET: 75 OF 99

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CK TERMINATION - B0

R8501 40.2 1% 1/20W MF 201 — FB_B0_CLK_P — FBB0_CK_MID — R8502 40.2 1% 1/20W MF 201 — FB_B0_CLK_N
C8590 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8500.J12:8.4MM
PLACE_NEAR=U8500.J11:8.4MM

CK TERMINATION - B1

R8551 40.2 1% 1/20W MF 201 — FB_B1_CLK_P — FBB1_CK_MID — R8552 40.2 1% 1/20W MF 201 — FB_B1_CLK_N
C8591 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8550.J12:8.4MM
PLACE_NEAR=U8550.J11:8.4MM

R8500 120 1% 1/20W MF 201
R8504 120 1% 1/20W MF 201
R8503 120 1% 1/20W MF 201

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_B0_A<2>	H11	BA0/A2
FB_B0_A<5>	K10	BA1/A5
FB_B0_A<4>	K11	BA2/A4
FB_B0_A<3>	H10	BA3/A3
FB_B0_A<7>	K4	A8/A7
FB_B0_A<1>	H5	A9/A1
FB_B0_A<0>	H4	A10/A0
FB_B0_A<6>	K5	A11/A6
FB_B0_CKE_L	J3	CKE*
FB_B0_CLK_P	J12	CK
FB_B0_CLK_N	J11	CK*
FB_B0_CS_L	G12	CS*
FB_B0_WE_L	L12	WE*
FB_B0_CAS_L	L3	CAS*
FB_B0_RAS_L	G3	RAS*
FB_B0_ZQ	J13	ZQ
FB_B0_MF	J1	MF (MF=0)
FB_B0_SEN	J10	SEN
FB_B0_RESET_L	J2	RESET*
FB_B0_ABI_L	J4	ABI*
FB_B0_EDC<0>	C2	EDC0
FB_B0_EDC<1>	C13	EDC1
FB_B0_EDC<2>	R13	EDC2
FB_B0_EDC<3>	R2	EDC3
FB_B0_WCLK_P<0>	D4	WCK01
FB_B0_WCLK_N<0>	D5	WCK01*
FB_B0_WCLK_P<1>	P4	WCK23
FB_B0_WCLK_N<1>	P5	WCK23*

OMIT_TABLE

DBI0*	D2	FB_B0_DBI_L<0>
DBI1*	D13	FB_B0_DBI_L<1>
DBI2*	P13	FB_B0_DBI_L<2>
DBI3*	P2	FB_B0_DBI_L<3>
DQ0	A4	FB_B0_DQ<0>
DQ1	A2	FB_B0_DQ<1>
DQ2	B4	FB_B0_DQ<2>
DQ3	B2	FB_B0_DQ<3>
DQ4	E4	FB_B0_DQ<4>
DQ5	E2	FB_B0_DQ<5>
DQ6	F4	FB_B0_DQ<6>
DQ7	F2	FB_B0_DQ<7>
DQ8	A11	FB_B0_DQ<8>
DQ9	A13	FB_B0_DQ<9>
DQ10	B11	FB_B0_DQ<10>
DQ11	B13	FB_B0_DQ<11>
DQ12	E11	FB_B0_DQ<12>
DQ13	E13	FB_B0_DQ<13>
DQ14	F11	FB_B0_DQ<14>
DQ15	F13	FB_B0_DQ<15>
DQ16	U11	FB_B0_DQ<16>
DQ17	U13	FB_B0_DQ<17>
DQ18	T11	FB_B0_DQ<18>
DQ19	T13	FB_B0_DQ<19>
DQ20	N11	FB_B0_DQ<20>
DQ21	N13	FB_B0_DQ<21>
DQ22	M11	FB_B0_DQ<22>
DQ23	M13	FB_B0_DQ<23>
DQ24	U4	FB_B0_DQ<24>
DQ25	U2	FB_B0_DQ<25>
DQ26	T4	FB_B0_DQ<26>
DQ27	T2	FB_B0_DQ<27>
DQ28	N4	FB_B0_DQ<28>
DQ29	N2	FB_B0_DQ<29>
DQ30	M4	FB_B0_DQ<30>
DQ31	M2	FB_B0_DQ<31>
NC	A5	NC
NC	J5	NC
NC	U5	NC
FB_B0_A<8>		

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_B1_A<2>	H11	BA0/A2
FB_B1_A<5>	K10	BA1/A5
FB_B1_A<4>	K11	BA2/A4
FB_B1_A<3>	H10	BA3/A3
FB_B1_A<7>	K4	A8/A7
FB_B1_A<1>	H5	A9/A1
FB_B1_A<0>	H4	A10/A0
FB_B1_A<6>	K5	A11/A6
FB_B1_CKE_L	J3	CKE*
FB_B1_CLK_P	J12	CK
FB_B1_CLK_N	J11	CK*
FB_B1_CS_L	G12	CS*
FB_B1_WE_L	L12	WE*
FB_B1_CAS_L	L3	CAS*
FB_B1_RAS_L	G3	RAS*
FB_B1_ZQ	J13	ZQ
FB_B1_MF	J1	MF (MF=0)
FB_B1_SEN	J10	SEN
FB_B1_RESET_L	J2	RESET*
FB_B1_ABI_L	J4	ABI*
FB_B1_EDC<0>	C2	EDC0
FB_B1_EDC<1>	C13	EDC1
FB_B1_EDC<2>	R13	EDC2
FB_B1_EDC<3>	R2	EDC3
FB_B1_WCLK_P<0>	D4	WCK01
FB_B1_WCLK_N<0>	D5	WCK01*
FB_B1_WCLK_P<1>	P4	WCK23
FB_B1_WCLK_N<1>	P5	WCK23*

OMIT_TABLE

DBI0*	D2	FB_B1_DBI_L<0>
DBI1*	D13	FB_B1_DBI_L<1>
DBI2*	P13	FB_B1_DBI_L<2>
DBI3*	P2	FB_B1_DBI_L<3>
DQ0	A4	FB_B1_DQ<0>
DQ1	A2	FB_B1_DQ<1>
DQ2	B4	FB_B1_DQ<2>
DQ3	B2	FB_B1_DQ<3>
DQ4	E4	FB_B1_DQ<4>
DQ5	E2	FB_B1_DQ<5>
DQ6	F4	FB_B1_DQ<6>
DQ7	F2	FB_B1_DQ<7>
DQ8	A11	FB_B1_DQ<8>
DQ9	A13	FB_B1_DQ<9>
DQ10	B11	FB_B1_DQ<10>
DQ11	B13	FB_B1_DQ<11>
DQ12	E11	FB_B1_DQ<12>
DQ13	E13	FB_B1_DQ<13>
DQ14	F11	FB_B1_DQ<14>
DQ15	F13	FB_B1_DQ<15>
DQ16	U11	FB_B1_DQ<16>
DQ17	U13	FB_B1_DQ<17>
DQ18	T11	FB_B1_DQ<18>
DQ19	T13	FB_B1_DQ<19>
DQ20	N11	FB_B1_DQ<20>
DQ21	N13	FB_B1_DQ<21>
DQ22	M11	FB_B1_DQ<22>
DQ23	M13	FB_B1_DQ<23>
DQ24	U4	FB_B1_DQ<24>
DQ25	U2	FB_B1_DQ<25>
DQ26	T4	FB_B1_DQ<26>
DQ27	T2	FB_B1_DQ<27>
DQ28	N4	FB_B1_DQ<28>
DQ29	N2	FB_B1_DQ<29>
DQ30	M4	FB_B1_DQ<30>
DQ31	M2	FB_B1_DQ<31>
NC	A5	NC
NC	J5	NC
NC	U5	NC
FB_B1_A<8>		

R8550 120 1% 1/20W MF 201
R8554 120 1% 1/20W MF 201
R8553 120 1% 1/20W MF 201

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_B0_VREFC
VREFD	A10, U10	FB_B0_VREFD

OMIT_TABLE

=PP1V35_GPU_FBVDDQ

C8500 4.7UF 20% 6.3V X6S 0402
C8501 4.7UF 20% 6.3V X6S 0402
C8502 4.7UF 20% 6.3V X6S 0402
C8503 4.7UF 20% 6.3V X6S 0402
C8504 4.7UF 20% 6.3V X6S 0402
C8505 4.7UF 20% 6.3V X6S 0402
C8506 1UF 20% 4V CERM-X6S 0201
C8507 1UF 20% 4V CERM-X6S 0201
C8508 1UF 20% 4V CERM-X6S 0201
C8509 1UF 20% 4V CERM-X6S 0201
C8510 1UF 20% 4V CERM-X6S 0201
C8511 1UF 20% 4V CERM-X6S 0201
C8512 1UF 20% 4V CERM-X6S 0201
C8513 1UF 20% 4V CERM-X6S 0201
C8514 1UF 20% 4V CERM-X6S 0201
C8515 1UF 20% 4V CERM-X6S 0201
C8516 0.1UF 10% 6.3V X6S 0201
C8517 0.1UF 10% 6.3V X6S 0201
C8518 0.1UF 10% 6.3V X6S 0201
C8519 0.1UF 10% 6.3V X6S 0201
C8520 0.1UF 10% 6.3V X6S 0201
C8521 0.1UF 10% 6.3V X6S 0201
C8522 0.1UF 10% 6.3V X6S 0201
C8523 0.1UF 10% 6.3V X6S 0201
C8524 0.1UF 10% 6.3V X6S 0201
C8525 0.1UF 10% 6.3V X6S 0201

PLACE CLOSE TO U8500

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8530 549 1% 1/20W MF 201
FB_B0_VREFC
C8531 820PF 10% 25V X7R-CERM 0201
R8531 1.33K 1% 1/20W MF 201
R8534 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8500.J14:8.4MM

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8532 549 1% 1/20W MF 201
FB_B0_VREFD
C8532 820PF 10% 25V X7R-CERM 0201
R8533 1.33K 1% 1/20W MF 201
R8535 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8500.U10:8.4MM
PLACE_NEAR=U8500.A10:8.4MM

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_B1_VREFC
VREFD	A10, U10	FB_B1_VREFD

OMIT_TABLE

=PP1V35_GPU_FBVDDQ

C8550 4.7UF 20% 6.3V X6S 0402
C8551 4.7UF 20% 6.3V X6S 0402
C8552 4.7UF 20% 6.3V X6S 0402
C8553 4.7UF 20% 6.3V X6S 0402
C8554 4.7UF 20% 6.3V X6S 0402
C8555 4.7UF 20% 6.3V X6S 0402
C8556 1UF 20% 4V CERM-X6S 0201
C8557 1UF 20% 4V CERM-X6S 0201
C8558 1UF 20% 4V CERM-X6S 0201
C8559 1UF 20% 4V CERM-X6S 0201
C8560 1UF 20% 4V CERM-X6S 0201
C8561 1UF 20% 4V CERM-X6S 0201
C8562 1UF 20% 4V CERM-X6S 0201
C8563 1UF 20% 4V CERM-X6S 0201
C8564 1UF 20% 4V CERM-X6S 0201
C8565 1UF 20% 4V CERM-X6S 0201
C8566 0.1UF 10% 6.3V X6S 0201
C8567 0.1UF 10% 6.3V X6S 0201
C8568 0.1UF 10% 6.3V X6S 0201
C8569 0.1UF 10% 6.3V X6S 0201
C8570 0.1UF 10% 6.3V X6S 0201
C8571 0.1UF 10% 6.3V X6S 0201
C8572 0.1UF 10% 6.3V X6S 0201
C8573 0.1UF 10% 6.3V X6S 0201
C8574 0.1UF 10% 6.3V X6S 0201
C8575 0.1UF 10% 6.3V X6S 0201

PLACE CLOSE TO U8550

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8580 549 1% 1/20W MF 201
FB_B1_VREFC
C8581 820PF 10% 25V X7R-CERM 0201
R8581 1.33K 1% 1/20W MF 201
R8584 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8550.J14:8.4MM

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8582 549 1% 1/20W MF 201
FB_B1_VREFD
C8582 820PF 10% 25V X7R-CERM 0201
C8583 820PF 10% 25V X7R-CERM 0201
R8583 1.33K 1% 1/20W MF 201
R8585 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8550.U10:8.4MM
PLACE_NEAR=U8550.A10:8.4MM

SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012

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GDDR5 Frame Buffer B

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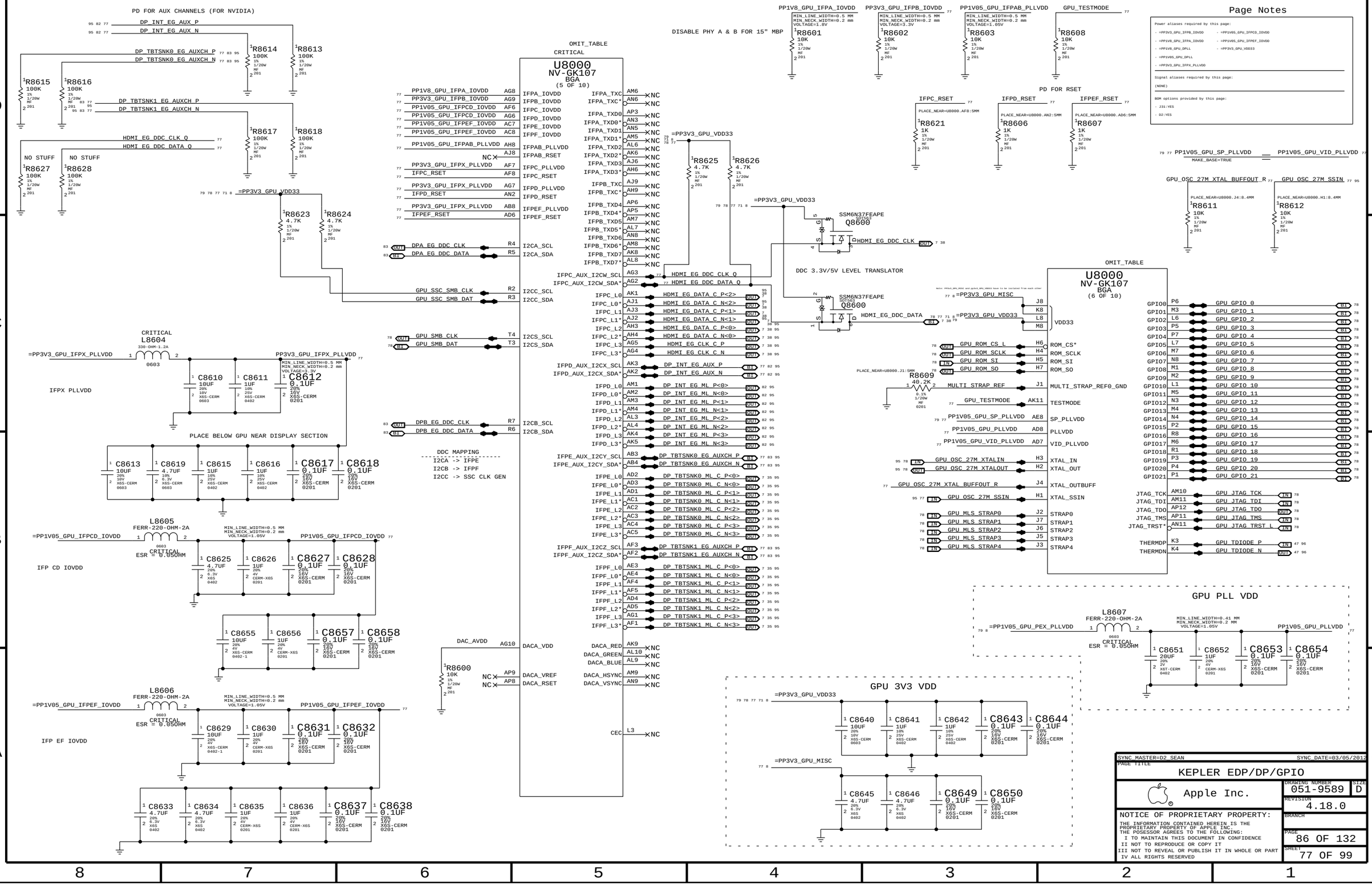
PD FOR AUX CHANNELS (FOR NVIDIA)
DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q
NO STUFF
NO STUFF
R8614 100K
R8613 100K
R8615 100K
R8616 100K
R8617 100K
R8618 100K
R8627 100K
R8628 100K
=PP3V3_GPU_VDD33
R8623 4.7K
R8624 4.7K
DISABLE PHY A & B FOR 15" MBP
OMIT_TABLE
CRITICAL
U8000
NV-GK107
BGA
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PP1V8_GPU_IFPA_IOVDD
PP3V3_GPU_IFPB_IOVDD
PP1V05_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPAB_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
IFPC_RSET
IFPD_RSET
IFPEF_RSET
IFPA_IOVDD
IFPB_IOVDD
IFPC_IOVDD
IFPD_IOVDD
IFPE_IOVDD
IFPF_IOVDD
IFPAB_PLLVDD
IFPAB_RSET
IFPC_PLLVDD
IFPC_RSET
IFPD_PLLVDD
IFPD_RSET
IFPEF_PLLVDD
IFPEF_RSET
DPA_EG_DDC_CLK
DPA_EG_DDC_DATA
I2C1A_SCL
I2C1A_SDA
GPU_SSC_SMB_CLK
GPU_SSC_SMB_DAT
I2C1C_SCL
I2C1C_SDA
GPU_SMB_CLK
GPU_SMB_DAT
I2C1S_SCL
I2C1S_SDA
DPB_EG_DDC_CLK
DPB_EG_DDC_DATA
I2C1B_SCL
I2C1B_SDA
DDC MAPPING
I2CA -> IFPE
I2CB -> IFPF
I2CC -> SSC CLK GEN
DAC_AVDD
R8600 10K
DACA_VDD
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
DACA_VREF
DACA_RSET
CEC
IFPC_AUX_I2CW_SCL
IFPC_AUX_I2CW_SDA*
IFPD_AUX_I2CX_SCL
IFPD_AUX_I2CX_SDA*
IFPE_AUX_I2CY_SCL
IFPE_AUX_I2CY_SDA*
IFPF_AUX_I2CZ_SCL
IFPF_AUX_I2CZ_SDA*
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q
DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
PP1V8_GPU_IFPA_IOVDD
R8601 10K
PP3V3_GPU_IFPB_IOVDD
R8602 10K
PP1V05_GPU_IFPAB_PLLVDD
R8603 10K
GPU_TESTMODE
R8608 10K
PD FOR RSET
IFPC_RSET
R8621 1K
IFPD_RSET
R8606 1K
IFPEF_RSET
R8607 1K
Page Notes
Power aliases required by this page:
- =PP3V3_GPU_IFPB_IOVDD
- =PP1V8_GPU_IFPA_IOVDD
- =PP1V8_GPU_DPLL
- =PP1V05_GPU_DPLL
- =PP3V3_GPU_IFPX_PLLVDD
- =PP1V05_GPU_IFPFCD_IOVDD
- =PP1V05_GPU_IFPEF_IOVDD
- =PP3V3_GPU_VDD33
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- J31:YES
- D2:YES
PP1V05_GPU_SP_PLLVDD
PP1V05_GPU_VID_PLLVDD
MAKE_BASE=TRUE
GPU_OSC_27M_XTAL_BUFFOUT_R
GPU_OSC_27M_SSIN
R8611 10K
R8612 10K
DDC 3.3V/5V LEVEL TRANSLATOR
SSM6N37FEAPE
Q8600
HDMI_EG_DDC_CLK
HDMI_EG_DDC_DATA
OMIT_TABLE
U8000
NV-GK107
BGA
(6 OF 10)
=PP3V3_GPU_MISC
=PP3V3_GPU_VDD33
VDD33
GPU_ROM_CS_L
GPU_ROM_SCLK
GPU_ROM_SI
GPU_ROM_SO
R8609 40.2K
MULTI_STRAP_REF
GPU_TESTMODE
PP1V05_GPU_SP_PLLVDD
PP1V05_GPU_PLLVDD
PP1V05_GPU_VID_PLLVDD
GPU_OSC_27M_XTALIN
GPU_OSC_27M_XTALOUT
GPU_OSC_27M_XTAL_BUFFOUT_R
GPU_OSC_27M_SSIN
GPU_MLS_STRAP0
GPU_MLS_STRAP1
GPU_MLS_STRAP2
GPU_MLS_STRAP3
GPU_MLS_STRAP4
ROM_CS*
ROM_SCLK
ROM_SI
ROM_SO
MULTI_STRAP_REF0_GND
TESTMODE
SP_PLLVDD
PLLVDD
VID_PLLVDD
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19 GPIO20 GPIO21
GPU_GPIO_0 GPU_GPIO_1 GPU_GPIO_2 GPU_GPIO_3 GPU_GPIO_4 GPU_GPIO_5 GPU_GPIO_6 GPU_GPIO_7 GPU_GPIO_8 GPU_GPIO_9 GPU_GPIO_10 GPU_GPIO_11 GPU_GPIO_12 GPU_GPIO_13 GPU_GPIO_14 GPU_GPIO_15 GPU_GPIO_16 GPU_GPIO_17 GPU_GPIO_18 GPU_GPIO_19 GPU_GPIO_20 GPU_GPIO_21
JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TRST*
GPU_JTAG_TCK GPU_JTAG_TDI GPU_JTAG_TDO GPU_JTAG_TMS GPU_JTAG_TRST_L
THERMDP THERMDN
GPU_TDIODE_P GPU_TDIODE_N
GPU PLL VDD
L8607 FERR-220-OHM-2A
=PP1V05_GPU_PEX_PLLVDD
PP1V05_GPU_PLLVDD
C8651 20UF
C8652 1UF
C8653 0.1UF
C8654 0.1UF
GPU 3V3 VDD
=PP3V3_GPU_VDD33
=PP3V3_GPU_MISC
C8640 10UF
C8641 1UF
C8642 1UF
C8643 0.1UF
C8644 0.1UF
C8645 4.7UF
C8646 4.7UF
C8649 0.1UF
C8650 0.1UF
CRITICAL
L8604 330-OHM-1.2A
=PP3V3_GPU_IFPX_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
IFPX PLLVDD
C8610 10UF
C8611 1UF
C8612 0.1UF
PLACE BELOW GPU NEAR DISPLAY SECTION
C8613 10UF
C8619 4.7UF
C8615 1UF
C8616 1UF
C8617 0.1UF
C8618 0.1UF
L8605 FERR-220-OHM-2A
=PP1V05_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPCD_IOVDD
IFP CD IOVDD
ESR = 0.050OHM
C8625 4.7UF
C8626 1UF
C8627 0.1UF
C8628 0.1UF
C8655 10UF
C8656 1UF
C8657 0.1UF
C8658 0.1UF
L8606 FERR-220-OHM-2A
=PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD
IFP EF IOVDD
C8629 10UF
C8630 1UF
C8631 0.1UF
C8632 0.1UF
C8633 4.7UF
C8634 4.7UF
C8635 1UF
C8636 1UF
C8637 0.1UF
C8638 0.1UF
SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012
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KEPLER EDP/DP/GPIO
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REVISION 4.18.0
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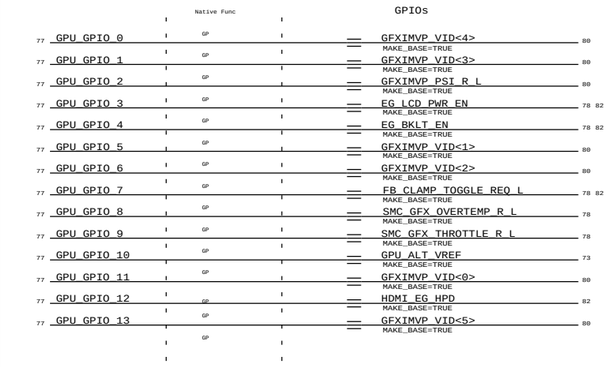
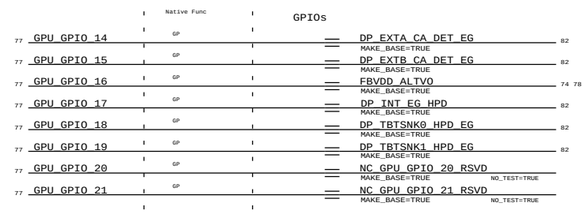
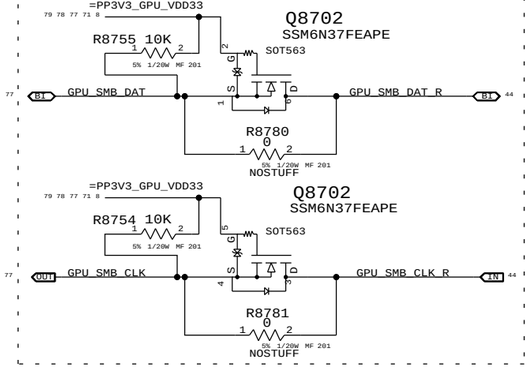


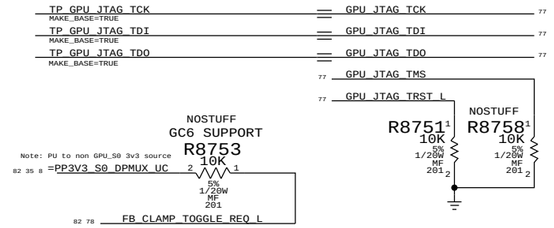


PEX_CLKREQ_L_R R8795 0 5% 1/20W MF 201 EG_CLKREQ_IN_L

GPU internal Temp isolation



Unused signals

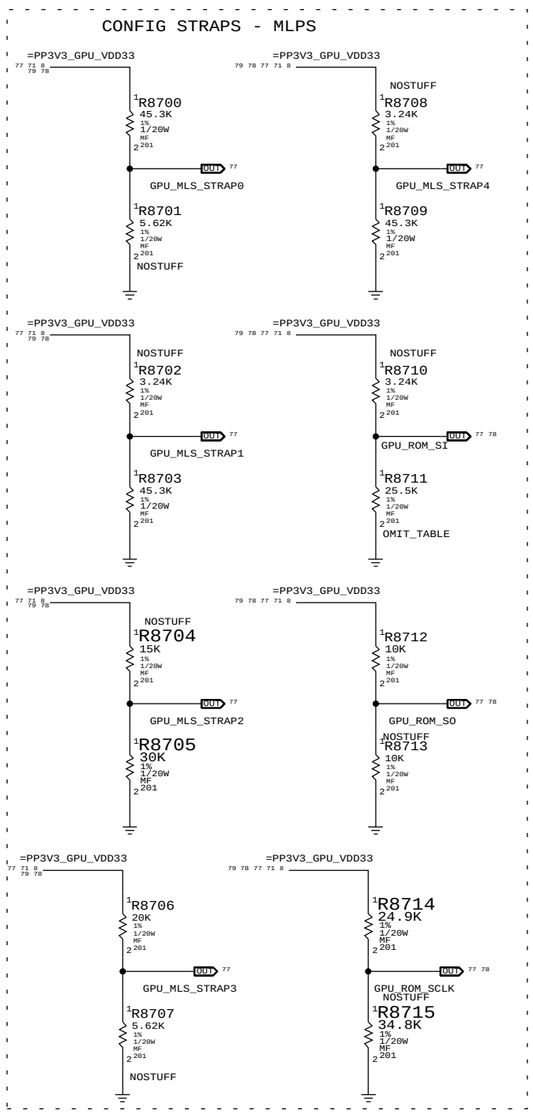


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0013	1	RES, 10KOHM, 0201	R8711		FB_2G_SAMSUNG
118S0414	1	RES,5.1KOHM, 0201	R8711		FB_2G_HYNIX_M_DIE
118S0230	1	RES,MF,24.9KOHM,1,1/20W,0201	R8711		FB_2G_HYNIX_A_DIE

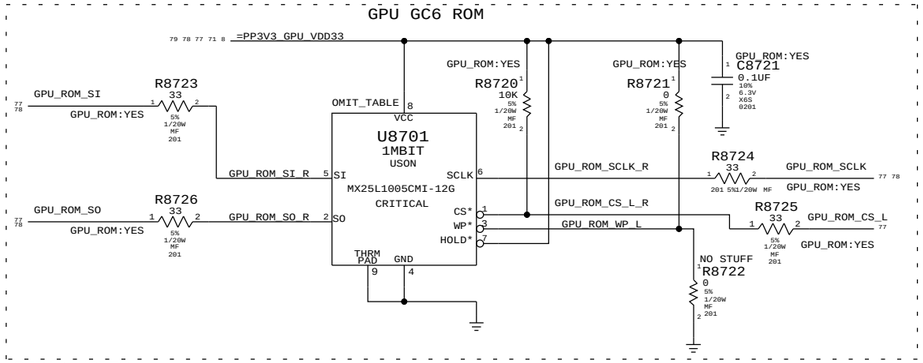
Die Rev	Strap
D-DIE	0x1
M-DIE	0x0
A-DIE	0x4

Straps for GK107. GF108 support has been removed.

CONFIG STRAPS - MLPS



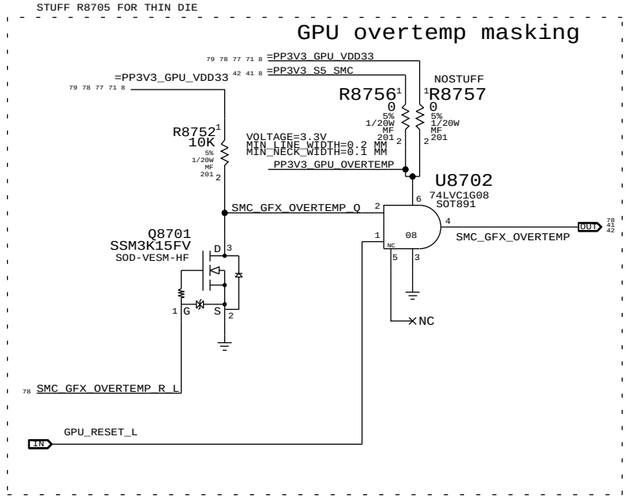
GPU GC6 ROM



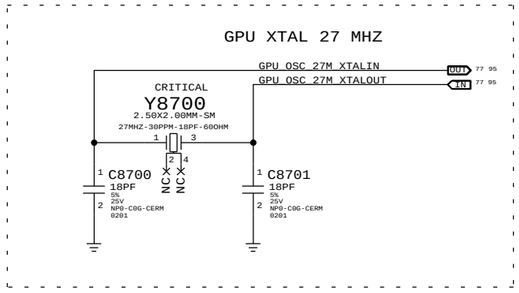
STRAP NOTES:

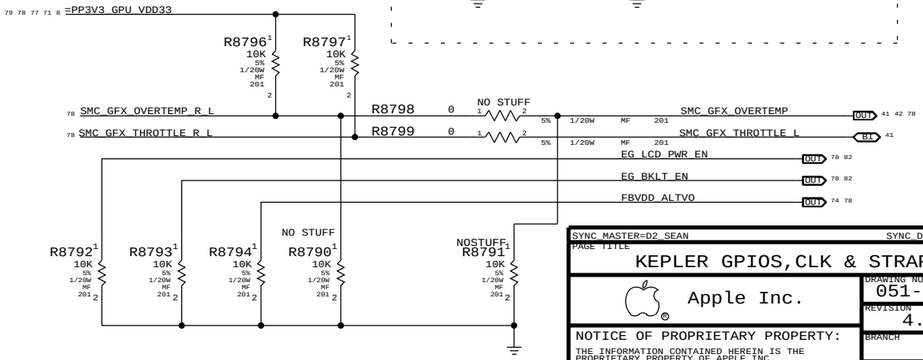
CURRENTLY STUFFED FOR GF108a/GK107-GTX
STUFF R8704 FOR THICK DIE
STUFF R8705 FOR THIN DIE

GPU overtemp masking



GPU XTAL 27 MHZ





SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

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KEPLER GPIOS,CLK & STRAPS

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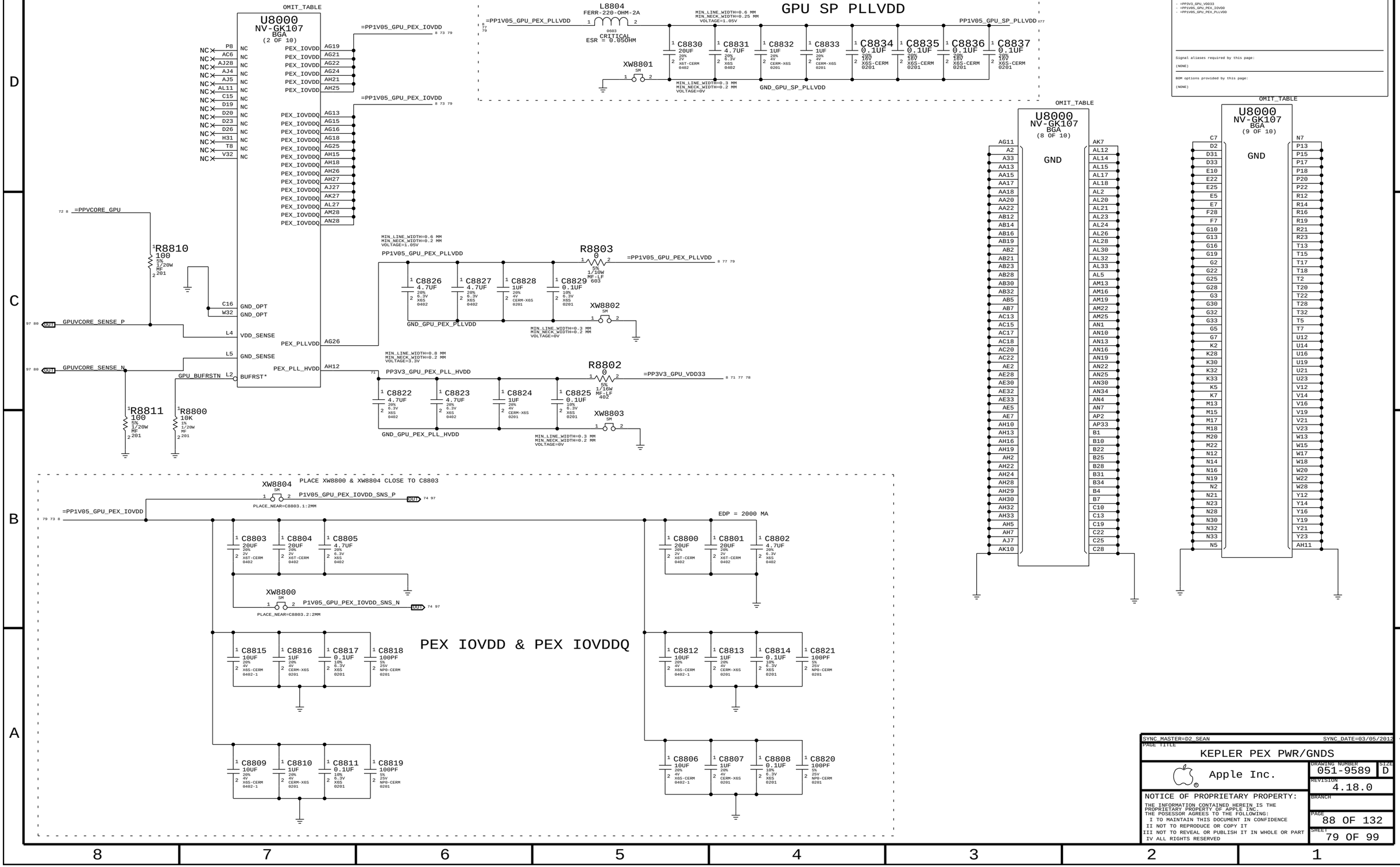
OMIT_TABLE
U8000
NV-GK107
BGA
(2 OF 10)
NC P8
NC AC6
NC AJ28
NC AJ4
NC AJ5
NC AL11
NC C15
NC D19
NC D20
NC D23
NC D26
NC H31
NC T8
NC V32
PEX_IOVDD AG19
PEX_IOVDD AG21
PEX_IOVDD AG22
PEX_IOVDD AG24
PEX_IOVDD AH21
PEX_IOVDD AH25
PEX_IOVDDQ AG13
PEX_IOVDDQ AG15
PEX_IOVDDQ AG16
PEX_IOVDDQ AG18
PEX_IOVDDQ AG25
PEX_IOVDDQ AH15
PEX_IOVDDQ AH18
PEX_IOVDDQ AH26
PEX_IOVDDQ AH27
PEX_IOVDDQ AJ27
PEX_IOVDDQ AK27
PEX_IOVDDQ AL27
PEX_IOVDDQ AM28
PEX_IOVDDQ AN28
GND_OPT C16
GND_OPT W32
VDD_SENSE L4
GND_SENSE L5
BUFRST* L2
PEX_PLLVDD AG26
PEX_PLL_HVDD AH12
=PP1V05_GPU_PEX_IOVDD
=PPVCORE_GPU
GPUVCORE_SENSE_P
GPUVCORE_SENSE_N
GPU_BUFRSTN
R8810 100 5% 1/20W MF 201
R8811 100 5% 1/20W MF 201
R8800 10K 1% 1/20W MF 201
GPU SP PLLVDD
L8804 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_PEX_PLLVDD
PP1V05_GPU_SP_PLLVDD
C8830 20UF 20% 2V X6T-CERM 0402
C8831 4.7UF 20% 6.3V X6S 0402
C8832 1UF 20% 4V CERM-X6S 0201
C8833 1UF 20% 4V CERM-X6S 0201
C8834 0.1UF 10% 16V X6S-CERM 0201
C8835 0.1UF 10% 16V X6S-CERM 0201
C8836 0.1UF 10% 16V X6S-CERM 0201
C8837 0.1UF 10% 16V X6S-CERM 0201
XW8801 SM
GND_GPU_SP_PLLVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
R8803 0 5% 1/10W MF-LF 603
C8826 4.7UF 20% 6.3V X6S 0402
C8827 4.7UF 20% 6.3V X6S 0402
C8828 1UF 20% 4V CERM-X6S 0201
C8829 0.1UF 10% 6.3V X6S 0201
XW8802 SM
GND_GPU_PEX_PLLVDD
PP1V05_GPU_PEX_PLLVDD
=PP1V05_GPU_PEX_PLLVDD
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
R8802 0 5% 1/16W MF-LF 402
C8822 4.7UF 20% 6.3V X6S 0402
C8823 4.7UF 20% 6.3V X6S 0402
C8824 1UF 20% 4V CERM-X6S 0201
C8825 0.1UF 10% 6.3V X6S 0201
XW8803 SM
GND_GPU_PEX_PLL_HVDD
PP3V3_GPU_PEX_PLL_HVDD
=PP3V3_GPU_VDD33
PLACE XW8800 & XW8804 CLOSE TO C8803
XW8804 SM
P1V05_GPU_PEX_IOVDD_SNS_P
PLACE_NEAR=C8803.1:2MM
XW8800 SM
P1V05_GPU_PEX_IOVDD_SNS_N
PLACE_NEAR=C8803.2:2MM
EDP = 2000 MA
C8803 20UF 20% 2V X6T-CERM 0402
C8804 20UF 20% 2V X6T-CERM 0402
C8805 4.7UF 20% 6.3V X6S 0402
C8800 20UF 20% 2V X6T-CERM 0402
C8801 20UF 20% 2V X6T-CERM 0402
C8802 4.7UF 20% 6.3V X6S 0402
C8815 10UF 20% 4V X6S-CERM 0402-1
C8816 1UF 20% 4V CERM-X6S 0201
C8817 0.1UF 10% 6.3V X6S 0201
C8818 100PF 5% 25V NP0-CERM 0201
C8812 10UF 20% 4V X6S-CERM 0402-1
C8813 1UF 20% 4V CERM-X6S 0201
C8814 0.1UF 10% 6.3V X6S 0201
C8821 100PF 5% 25V NP0-CERM 0201
C8809 10UF 20% 4V X6S-CERM 0402-1
C8810 1UF 20% 4V CERM-X6S 0201
C8811 0.1UF 10% 6.3V X6S 0201
C8819 100PF 5% 25V NP0-CERM 0201
C8806 10UF 20% 4V X6S-CERM 0402-1
C8807 1UF 20% 4V CERM-X6S 0201
C8808 0.1UF 10% 6.3V X6S 0201
C8820 100PF 5% 25V NP0-CERM 0201
PEX IOVDD & PEX IOVDDQ
OMIT_TABLE
U8000
NV-GK107
BGA
(8 OF 10)
GND
OMIT_TABLE
U8000
NV-GK107
BGA
(9 OF 10)
GND
Page Notes
Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012
PAGE TITLE
KEPLER PEX PWR/GNDS
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
BRANCH
PAGE 88 OF 132
SHEET 79 OF 99
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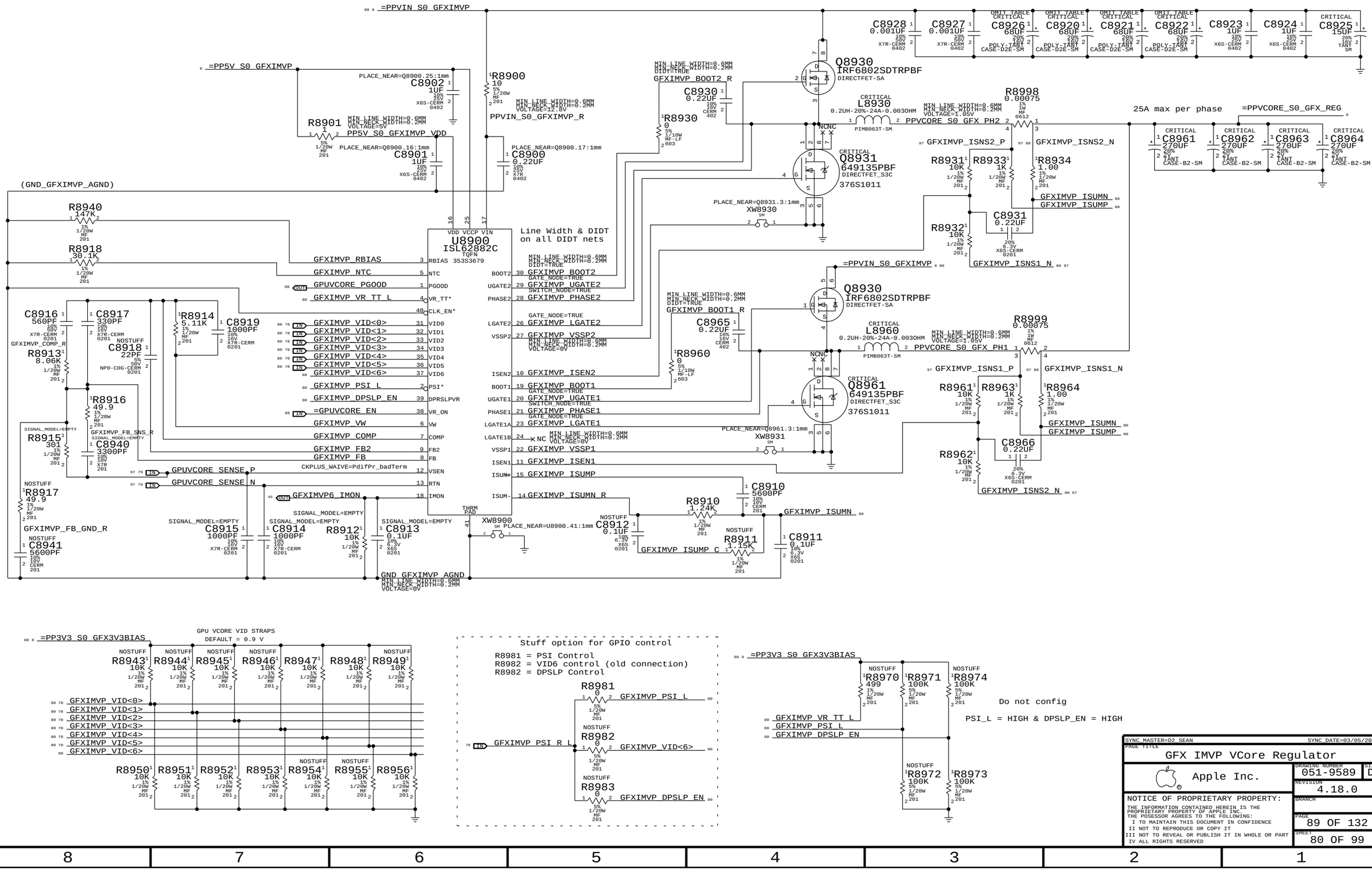

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: GFX IMVP VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

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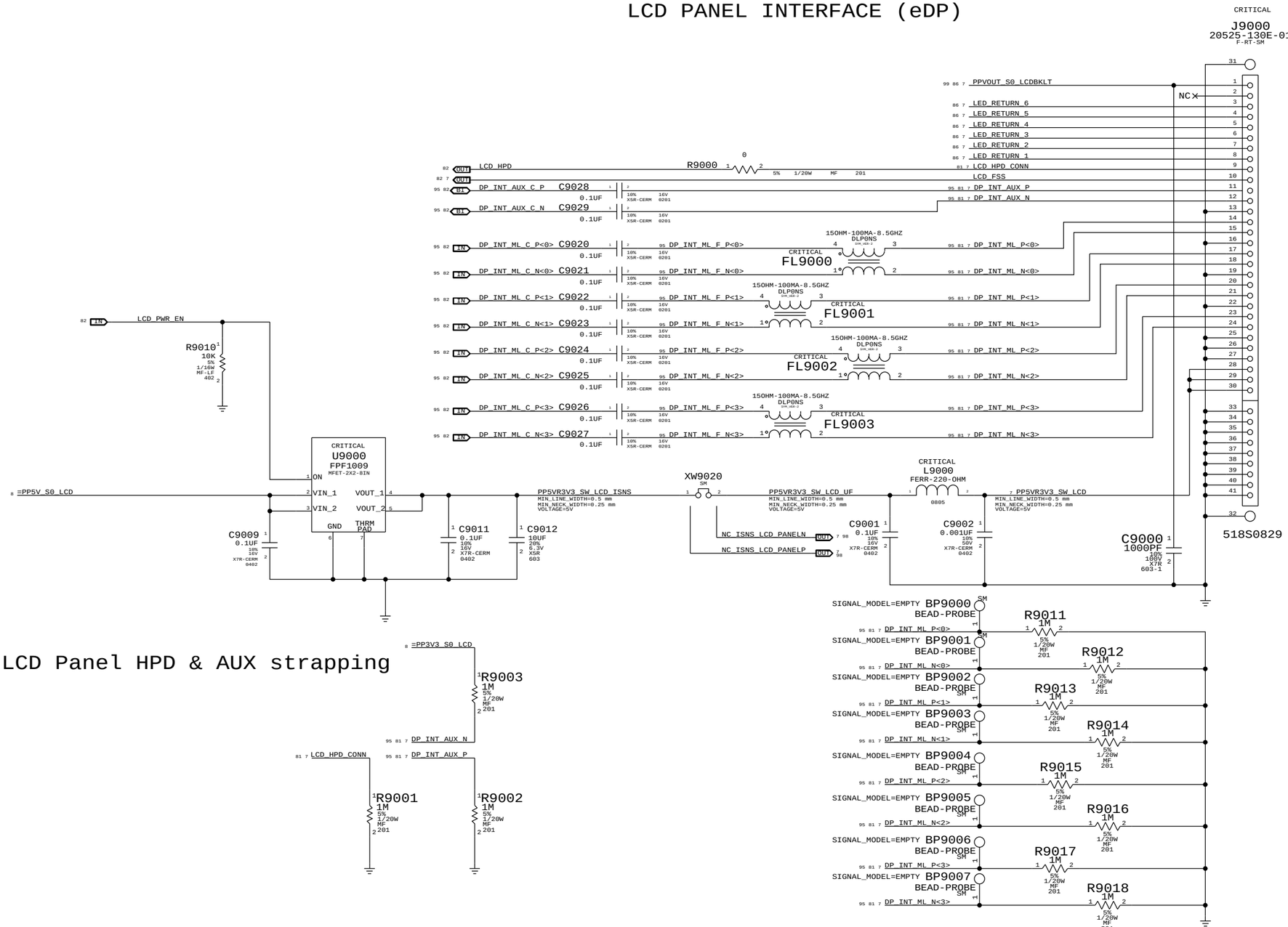
LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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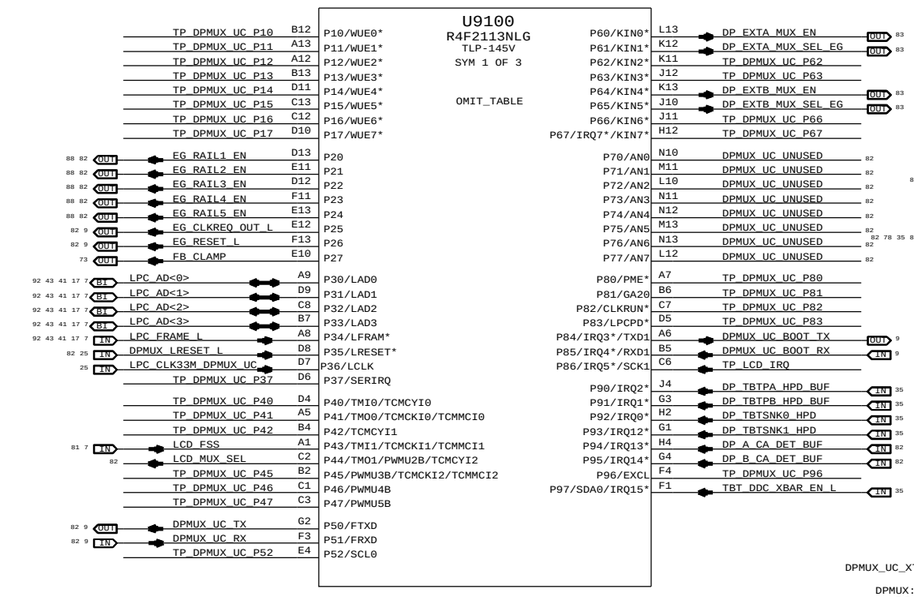
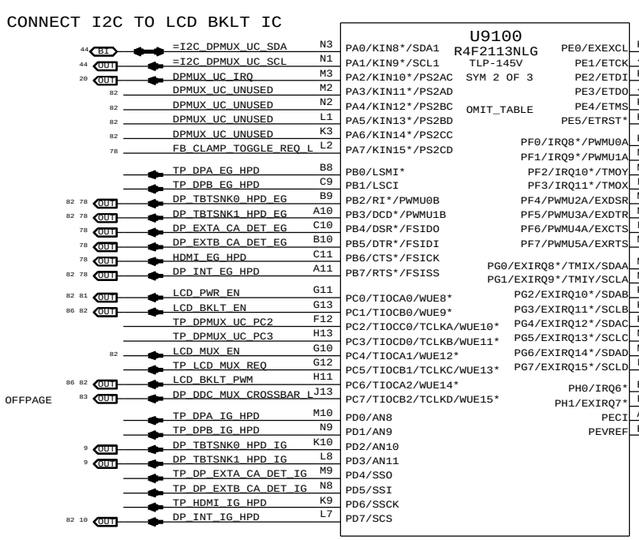
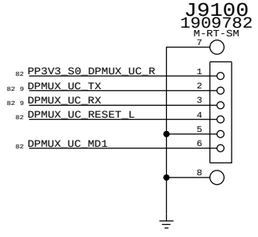


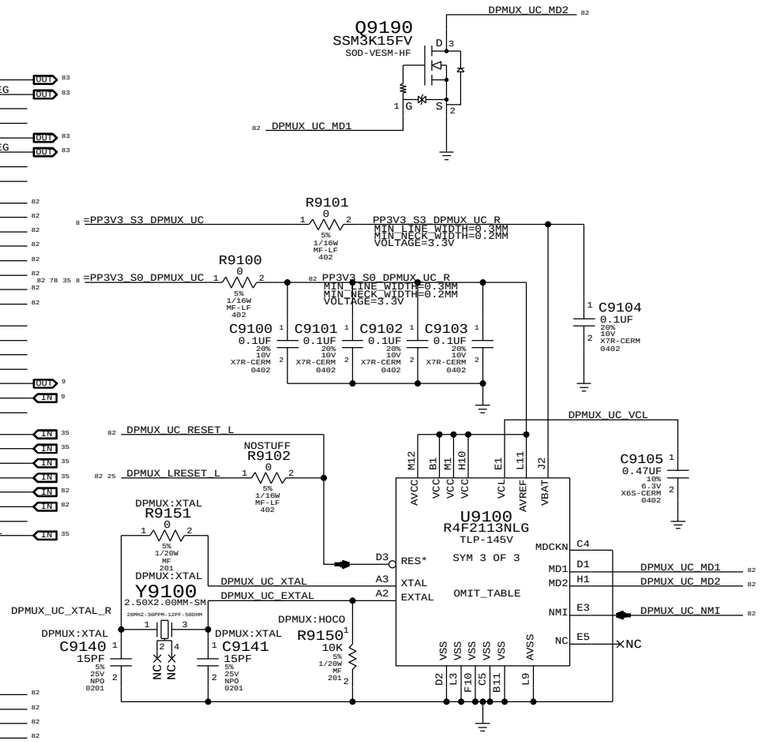


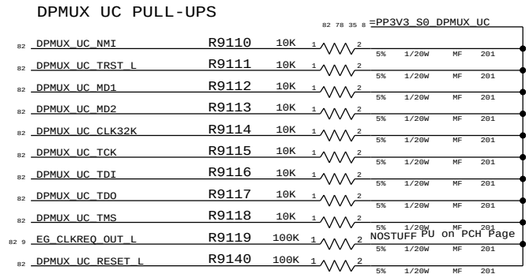
CONNECT I2C TO LCD BKLT IC

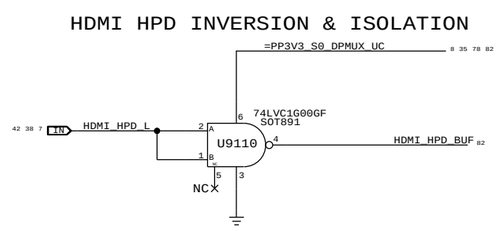
PU OFFPAGE

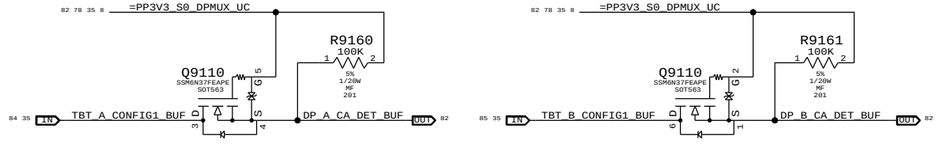


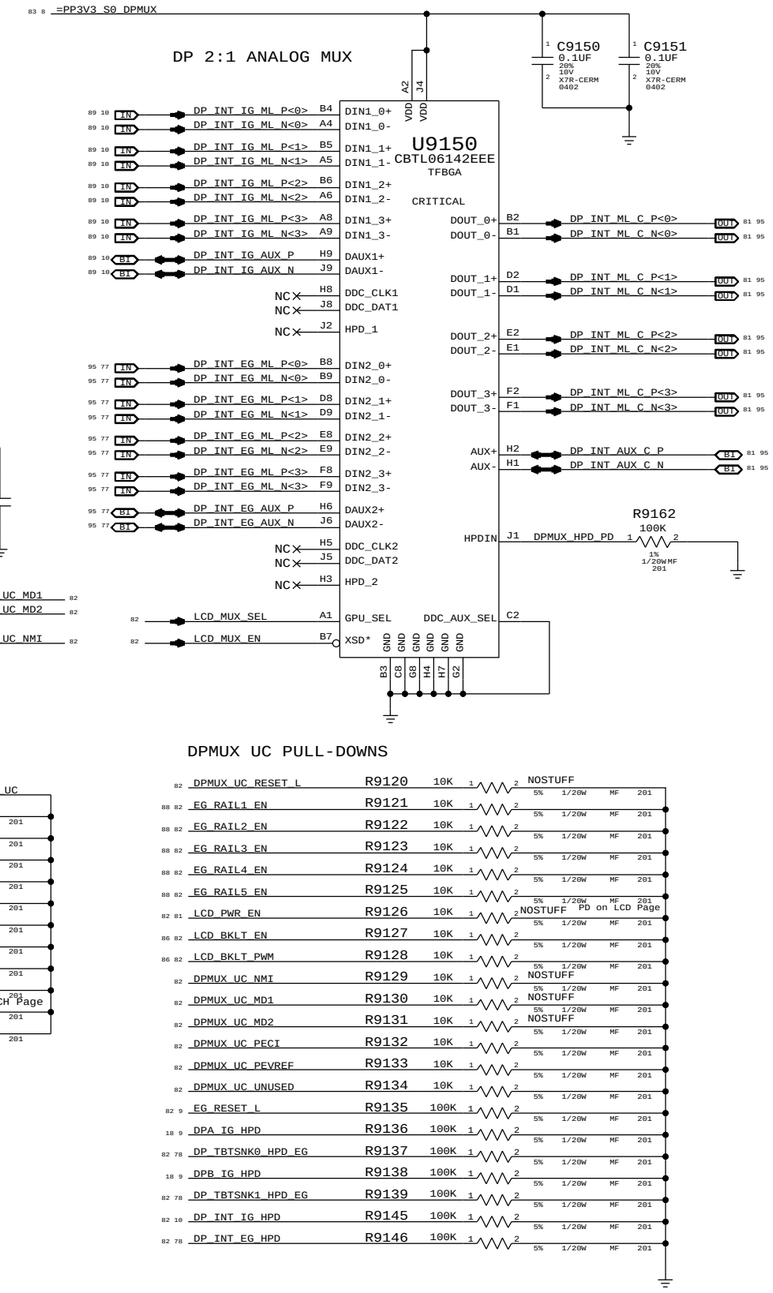
DPMUX UC DEBUG HEADER











SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	eDP Mux
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 91 OF 132
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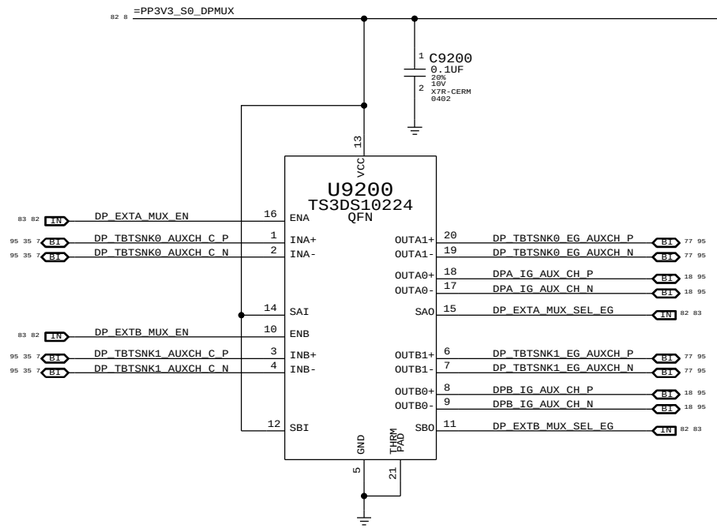
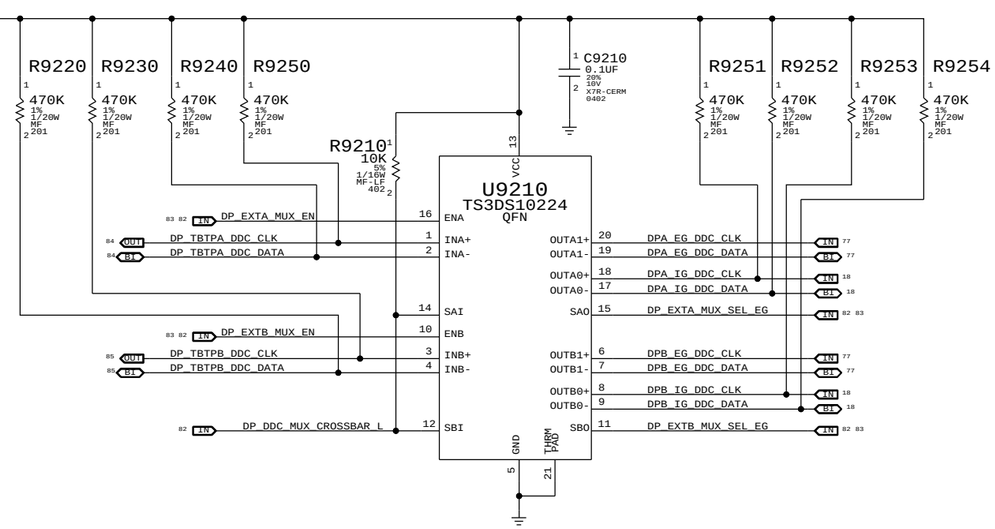
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: eDP Muxed Graphics Support

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 10% 16V X5R-CERM 0201
=PPHV_SW_TBTAPWRSW
18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 25V X5R 402
CRITICAL
U9410
CD3210A0RGP
QFN
V3P3
VHV
RSVD
EN
HV_EN
S0
V3P3OUT
OUT
RSVD
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
PP3V3_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C9485 0.1UF 10% 16V X5R-CERM 0201
C9486 10UF 20% 6.3V CERM-X5R 0402
C9411 0.1UF 10% 25V X5R 402
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R9410 22.6K 1% 1/20W MF 201
R9411 22.6K 1% 1/20W MF 201
R9412 36.5K 1% 1/20W MF 201 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/20W MF 201 <RHVS3>
R9414 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R_s_per HV ISET_SX with cd3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

SIGNAL_MODEL=TBT_MUX
VDD
CRITICAL
U9420
CBTL05023
HVQFN
TBT_A_CIO_SEL
DP_AUXIO_EN
BIASIN
AUXIO_EN
BIASOUT
AUX-
AUX+
AUXIO-
AUXIO+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
DPML0+
DPML0-
LSTX
LSRX
DP_PD
HPDOUT
HPD
GND_THMPAD
C9420 0.1UF 10% 16V X5R-CERM 0201
C9421 0.1UF 10% 16V X5R-CERM 0201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201
TBT_A_BIAS
C9425 0.1UF 10% 16V X5R-CERM 0201
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_BUF
TBT_A_CONFIG1_RC
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C9430 0.1UF 10% 16V X5R-CERM 0201
C9431 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
TBT_A_HPD
R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201
PP3V3_SW_TBTAPWR
CRITICAL
U9460
74AUP1T97
SOT891
VCC
GND
TBT_A_LSRX
Y = B
C9460 0.1UF 10% 16V X5R-CERM 0201
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

CRITICAL
L9400
FERR-120-OHM-3A
0603
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C9400 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V
R9401 12 5% 1/20W MF 201
C9401 0.01UF 10% 50V X7R-CERM 0402

For J9400 TBT SMT pads (3, 5, 17 & 19):

SHIELD PINS
J9400
MDP-D2
F-RT-TH
PORT B
SHIELD PINS
514-0803
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C9405 0.01UF 10% 25V X5R-CERM 0201
DP Dir
TBT Dir
(0-18.9V)
TBT: TX_0
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C9406 0.01UF 10% 25V X5R-CERM 0201
TBT: TX_1
TBT: LSX_R2P/P2R (P/N)
C9470 0.22UF 20% 6.3V X5R 0201
C9471 0.22UF 20% 6.3V X5R 0201
C9472 0.22UF 20% 6.3V X5R 0201
C9473 0.22UF 20% 6.3V X5R 0201
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
470k R's for ESD protection on AC-coupled signals.

C9474 0.47UF 20% 4V CERM-X5R-1 201
C9475 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
C9478 0.22UF 20% 6.3V X5R 0201
C9479 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
TBT: Unused
TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
C9476 0.47UF 20% 4V CERM-X5R-1 201
C9477 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
CRITICAL
SIGNAL_MODEL=TBTPIN
GND_VOID=TRUE
(Both D's)
D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL
L9498
650NH-5%-0.430MA-0.52OHM
0603
SIGNAL_MODEL=EMPTY
CRITICAL
L9499
650NH-5%-0.430MA-0.52OHM
0603
SIGNAL_MODEL=EMPTY
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V C0G-NP0 0402
C9499 30PF 5% 50V C0G-NP0 0402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R-CERM 0201
C9495 330PF 10% 16V X7R-CERM 0201
R9441 100K 5% 1/20W MF 201
C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012
PAGE TITLE: Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER: 051-9589
SIZE: D
REVISION: 4.18.0
BRANCH:
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW
CRITICAL
C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C9680 22UF 20% 6.3V X5R-CERM-1 603
C9681 0.1UF 10% 16V X5R-CERM 0201
=PPHV_SW_TBTBPWRSW
18V Max
C9615 4.7UF 10% 25V X5R-CERM 0603
C9610 0.1UF 10% 25V X5R 402
U9610 CRITICAL
CD3210A0RGP QFN
V3P3 V3P3OUT PP3V3_SW_TBTBPWR
VHV OUT PPHV_SW_TBTBPWR
RSVD RSVD
EN ISET_V3P3 TBTBPWRSW_ISET_V3P3
HV_EN ISET_S0 TBTBPWRSW_ISET_S0
S0 ISET_S3 TBTBPWRSW_ISET_S3
GND THRM PAD
C9685 0.1UF 10% 16V X5R-CERM 0201
C9686 10UF 20% 6.3V CERM-X5R 0402
C9611 0.1UF 10% 25V X5R 402
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
VOLTAGE=15V
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
12V: See below
TBTHV:P15V
R9610 22.6K 1% 1/20W MF 201
R9611 22.6K 1% 1/20W MF 201
R9612 36.5K 1% 1/20W MF 201 <RV3P3>
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
R9613 22.6K 1% 1/20W MF 201 <RHVS3>
R9614 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R_S per HV ISET_SX with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

PP3V3_SW_TBTBPWR
C9620 0.1UF 10% 16V X5R-CERM 0201
C9621 0.1UF 10% 16V X5R-CERM 0201
R9627 10K 5% 1/20W MF 201
R9629 100K 5% 1/20W MF 201
VDD
CRITICAL
U9620
CBTL05023
HVQFN
SIGNAL_MODEL=TBT_MUX
TBT_B_BIAS VOLTAGE=3.3V
C9625 0.1UF 10% 16V X5R-CERM 0201
TBT_B_CIO_SEL
DP_AUXIO_EN
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
C9630 0.1UF 10% 16V X5R-CERM 0201
C9631 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
C9632 0.22UF 20% 6.3V X5R 0201
C9633 0.22UF 20% 6.3V X5R 0201
TBT_B_LSTX
TBT_B_LSRX_UNBUF
TBT_B_DP_PWRDN
DP_TBTPB_HPD
BIASIN BIASOUT
AUXIO_EN
AUX- AUX+
DDC_DAT DDC_CLK
CA_DETOUT CA_DET
DP+ DP-
LSTX LSRX
DP_PD
HPDOUT HPD
GND THMPAD
R9626 1M 5% 1/20W MF 201
R9628 100K 5% 1/20W MF 201
TBT_B_AUXCH_DDC_N
TBT_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC
TBT_B_LSX_ML_P<1>
TBT_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_HPD
PP3V3_SW_TBTBPWR
CRITICAL
U9660
74AUP1T97
SOT891
VCC GND
A B C
TBT_B_LSRX
Y = B
C9660 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L9600
FERR-120-OHM-3A
0603
PP3V3RHV_SW_TBTBPWR
C9600 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_20_RC
R9601 12 5% 1/20W MF 201
C9601 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_1_C
C9605 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C
C9606 0.01UF 10% 16V X5R-CERM 0201
For J9600 TBT SMT pads (3, 5, 17 & 19):
TBT Dir DP Dir
J9400
MDP-D2
F-RT-TH
SHIELD PINS
PORT A
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
514-0803
DP Dir TBT Dir
(0-18.9V)
TBT: TX_0
TBT: TX_1
TBT: LSX_R2P/P2R (P/N)
GND_VOID=TRUE (Both C's)
C9670 0.22UF 20% 6.3V X5R 0201
C9671 0.22UF 20% 6.3V X5R 0201
R9670 470K 5% 1/20W MF 201
R9671 470K 5% 1/20W MF 201
C9672 0.22UF 20% 6.3V X5R 0201
C9673 0.22UF 20% 6.3V X5R 0201
R9672 470K 5% 1/20W MF 201
R9673 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

C9674 0.47UF 20% 4V CERM-X5R-1 201
C9675 0.47UF 20% 4V CERM-X5R-1 201
C9676 0.47UF 20% 4V CERM-X5R-1 201
C9677 0.47UF 20% 4V CERM-X5R-1 201
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
R9694 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9695 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9678 470K 5% 1/20W MF 201
R9679 470K 5% 1/20W MF 201
C9678 0.22UF 20% 6.3V X5R 0201
C9679 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
TBT: Unused
R9698 2.2K 5% 1/20W MF 201
R9699 2.2K 5% 1/20W MF 201
D9698 BAR90-02LRH TSLP-2-7
D9699 BAR90-02LRH TSLP-2-7
CRITICAL
SIGNAL_MODEL=TBTPIN
GND_VOID=TRUE
(Both D's)
CRITICAL
L9698
650NH-5%-0.430MA-0.52OHM
0603
SIGNAL_MODEL=EMPTY
CRITICAL
L9699
650NH-5%-0.430MA-0.52OHM
0603
SIGNAL_MODEL=EMPTY
DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N
C9698 30PF 5% 50V C0G-NP0 0402
C9699 30PF 5% 50V C0G-NP0 0402
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R9652 1M 5% 1/20W MF 201
R9651 1M 5% 1/20W MF 201
C9694 330PF 10% 16V X7R-CERM 0201
C9695 330PF 10% 16V X7R-CERM 0201
R9641 100K 5% 1/20W MF 201
C9602 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF

F9700
3AMP-32V-467
603-HF
BOTTOM

=PPBUS_S0_LCDBKLT → PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!

R9788 301K 1% 1/16W MF-LF 402
C9782 0.1UF 10% 16V X7R-CERM 0402

LCDBKLT_EN_DIV

R9789 147K 1% 1/16W MF-LF 402

LCDBKLT_EN_L

Q9707 SSM6N15FEAPE SOT563

LCD_BKLT_EN
LCDBKLT_DISABLE

Q9707 SSM6N15FEAPE SOT563

BKLT_PLT_RST_L

*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.

=PP5V_S0_BKL

PPBUS_S0_LCDBKLT_PWR
PLACE_NEAR=L9710.1:5MM
PLACE_NEAR=L9710.1:3MM

CRITICAL
C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402

CRITICAL
L9710
22UH-20%-2.4A-0.105OHM
DEM8030C-SM
152S1527
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=50V
SWITCH_NODE=TRUE

PPBUS_S0_LCDBKLT_PWR_SW

PLACE_NEAR=L9710.2:3MM
CRITICAL
D9701
POWERDI-123
DFLS2100

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719
C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE

PLACE_NEAR=D9701.2:5MM
PLACE_NEAR=D9701.2:5MM
CRITICAL C9715 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9716 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9718 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9719 2.2UF 10% 100V X7R-CERM 1210
C9717 1000PF 10% 100V X7R-CERM 0603
PLACE_NEAR=R9708.1:5MM
PLACE_NEAR=D9701.2:3MM
PLACE_NEAR=D9701.2:3MM
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=55V

=PP3V3_S0_BKL_VDDIO

PLACE_NEAR=U9701.22:3MM
PLACE_NEAR=U9701.22:5MM
PLACE_NEAR=U9701.8:3MM
C9714 0.01UF 10% 16V X7R-CERM 0402
C9710 1UF 10% 25V X5R 603-1
C9711 0.1UF 10% 16V X7R-CERM 0402

PLACE_NEAR=L9710.2:3MM

R9708 63.4K 1% 1/16W MF-LF 402
R9709 59.0K 1% 1/16W MF-LF 402

CRITICAL
Q9701
SI7812DN
PWRPK-1212-8

BKL_FET_CNTL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM

U9701
LP8545SQX-EXTJ
LLP

8	VDDIO	SW	24
22	VLDO	FB	21
23	VIN	OUT1	12
6	GD	OUT2	13
		OUT3	14
BKL_FSET	5 FSET	OUT4	16
BKL_FLT	20 FILTER	OUT5	17
BKL_ISET	3 ISET	OUT6	18
BKL_SCL	10 SCLK	VSYNC	19
BKL_SDA	11 SDA		
LVDS_BKL_PWM_RC	2 PWM		
TP_BKL_FAULT	7 FAULT		
BKLT_EN	4 EN		
1 GND_SW	9 GND_S	15 GND_L	25 THRM PAD

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

BKL_SW
BKL_FB
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSYNC_R

D_BKL:DEV
R9717 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.12:10MM
LED_RETURN_1

D_BKL:DEV
R9718 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.13:10MM
LED_RETURN_2

D_BKL:DEV
R9719 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.14:10MM
LED_RETURN_3

D_BKL:DEV
R9720 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.16:10MM
LED_RETURN_4

D_BKL:DEV
R9721 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.17:10MM
LED_RETURN_5

D_BKL:DEV
R9722 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.18:10MM
LED_RETURN_6

R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS

=I2C_BKL_1_SCL R9753 0 5% 1/16W MF-LF 402
=I2C_BKL_1_SDA R9757 0 5% 1/16W MF-LF 402

PPBUS_S0_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
R9715 100K 1% 1/16W MF-LF 402

LCD_BKLT_PWM
R9704 0 5% 1/16W MF-LF 402
LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT

NO STUFF
C9704 33PF 5% 50V C0G-CERM 0402

(EEPROM should set EN_I_RES=1)
R9714 15.4K 1% 1/16W MF-LF 402
I_LED=23.96MA
I_LED=369/Riset

R9716 12.7K 1% 1/16W MF-LF 402
FPWM=19.2KHZ
details in spec

R9765 10K 5% 1/16W MF-LF 402
R9755 10K 5% 1/16W MF-LF 402
(APN: 353S3376)
PWM RES = 9+3

XW9710 SM
BKL_SGND
PLACE_NEAR=U9701.9:10MM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES, 0OHM, 0402	R9717,R9718,R9719,R9720,R9721,R9722		D_BKL:PROD

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012
PAGE TITLE
LCD Backlight Driver (LP8545)

Apple Inc.

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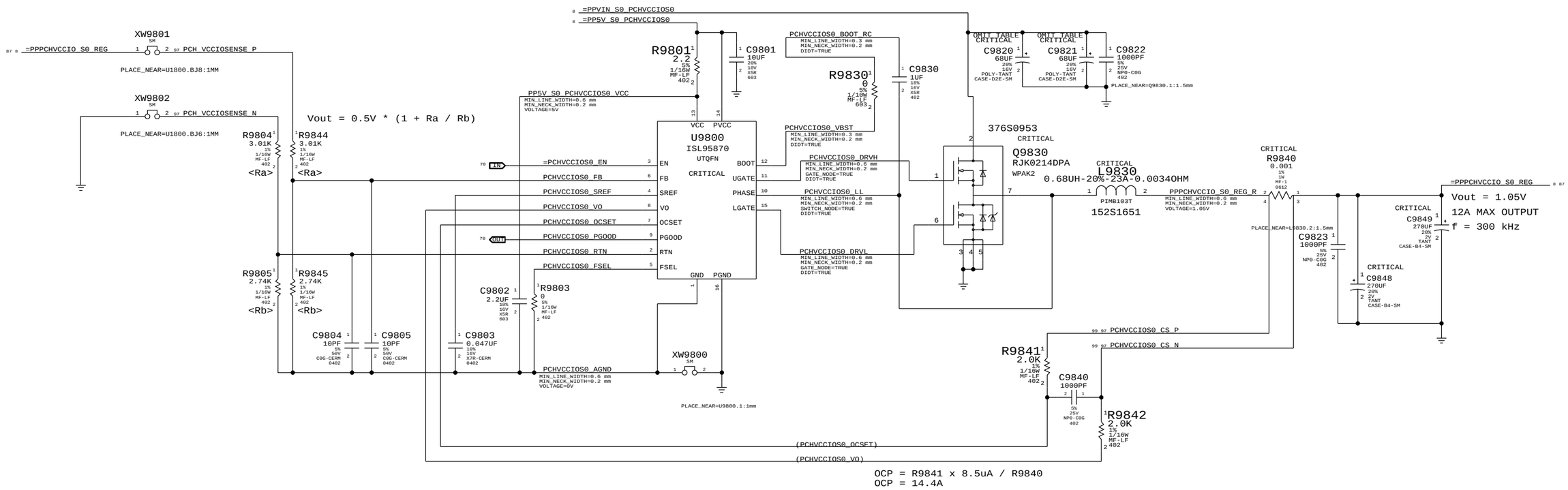
PCH VCCIO (1.05V S0) REGULATOR



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

PCH VCCIO (1.05V) POWER SUPPLY

Apple Inc.

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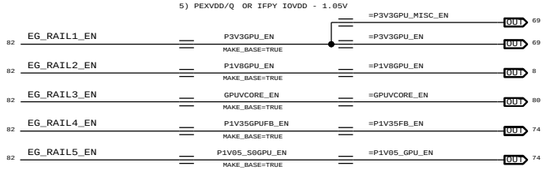
GPU Rail Sequencing

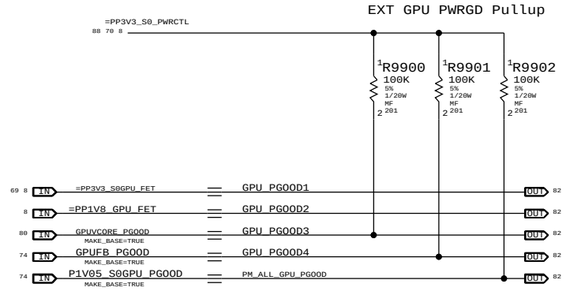
KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

1) GPU_3.3V
2) IFPX IOVDD - 1.8V
3) GPUVCORE
4) FBVDDQ/GDDR5 1.35V
5) PEXVDD/Q OR IFPY IOVDD - 1.05V



NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

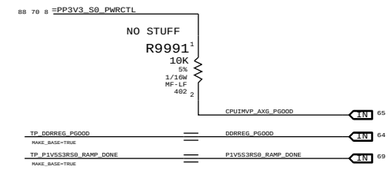
EXT GPU PWRGD Pullup



NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

Unused PGOOD signal



PEG_R2D_P<0> / PEG_R2D_N<0> — R9910 82 5% 1/20W MF 201 — NOSTUFF
PEG_R2D_P<5> / PEG_R2D_N<5> — R9915 82 5% 1/20W MF 201 — NOSTUFF
PEG_R2D_P<3> / PEG_R2D_N<3> — R9913 82 5% 1/20W MF 201 — NOSTUFF
PEG_R2D_P<7> / PEG_R2D_N<7> — R9917 82 5% 1/20W MF 201 — NOSTUFF

PLACE R9910 - R9917 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_D2R_P<0> / PEG_D2R_N<0> — R9920 82 5% 1/20W MF 201 — NOSTUFF
PEG_D2R_P<4> / PEG_D2R_N<4> — R9924 82 5% 1/20W MF 201 — NOSTUFF
PEG_D2R_P<7> / PEG_D2R_N<7> — R9927 82 5% 1/20W MF 201 — NOSTUFF

PLACE R9920 - R9927 CLOSE TO U1000

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	15 MIL	?

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RXRX	*	=4X_DIELECTRIC	?
PEG_TXTX	*	=4X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RXRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 10
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 10
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 10
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 10
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
1125 DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 17
1126 DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 17
1127 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3:0>	10 82
1128 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3:0>	10 82
1129 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	10 82
1131 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	10 82
1132 CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
1130 CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
1133 CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
1138 DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	9 11
1139 DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	9 11
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
1134 XDP_RDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
1135 XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
1136 XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 41
1115 CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 42
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 41 42 65
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	11 20 42
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
1140 CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 65
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 65
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 65
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 62
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 65
1120 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	13
1121 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	13
1122 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	13
1123 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	13
1137 CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 62
1140 CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 33
1141 CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 33
1144 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 29 33
1145 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	30 31 33
1146 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 29 33
1147 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	30 31 33
1148 XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
1149 XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	71 88
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	71 88
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	9 71
	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	9 71
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	71
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	71

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?
MEM_DQBL2BL	*	16 MILS	?
MEM_DQCH2CH	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

DDR3 (Memory Down):
DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 12 28 29 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..2>
MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_CS_L<1> 12 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0> 12 28 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..2>
MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_ODT<1> 12 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0> 12 28 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 12 28 29 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0> 12 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8> 12 28 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16> 12 28 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24> 12 28 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32> 12 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40> 12 28 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48> 12 28 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56> 12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 12 28 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 12 30 31 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..2>
MEM_B_CNTL1	MEM_37S	MEM_CTRL	MEM_B_CKE<1> 12 31 32
MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_CKE<0> 12 30 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..1> 12 31 32
MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_ODT<0> 12 30 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..7> 12 30 31 32
MEM_B_CMD6	MEM_40S	MEM_CMD	MEM_B_A<6> 12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<5..0> 12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 12 30 31 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0> 12 30 31
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8> 12 30 31
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16> 12 30 31
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24> 12 30 31
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32> 12 30 31
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40> 12 30 31
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48> 12 30 31
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56> 12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 12 30 31

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	1to3,1to4,1to9,1to10	=4:1_SPACING	?
LVDS	1to3,1to4,1to9,1to10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	1to3,1to4,1to9,1to10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	1to3,1to4,1to9,1to10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	1to3,1to4,1to9,1to10	=5:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	9 18
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	9 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 39
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 39
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 39
	SATA_90D	SATA	SATA_HDD_D2R_N	17 39
SATA_HDD_D2R	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_P	39
	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_N	39
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_P	39
	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_N	39
T233 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSD_D2R_P	39
T233	SATA_90D	SATA	SATA_SSD_D2R_N	39
T235 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_P	39
T235	SATA_90D	SATA	SATA_SSD_R2D_N	39
T218 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	
T219	SATA_90D	SATA	SATA_HDD_R2D_UF_N	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 17
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 17
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 17
	SATA_90D	SATA	SATA_ODD_D2R_N	9 17
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P	
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	
T213 PCH_SATA3_TCOMP	SATA_50SE	SATA_TCOMP	PCH_SATA3COMP	17
PCH_SATA_TCOMP	SATA_37SE	SATA_TCOMP	PCH_SATAICOMP	17
T235 USB_HUB1_UP	USB_85D	USB	USB_EXTB_XHCI_P	19 26
T237	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_HUB1_UP	USB_85D	USB	USB_EXTB_EHCI_P	19 26
	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 40
	USB_85D	USB	USB_EXTA_N	19 40
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 38
	USB_85D	USB	USB_EXTB_N	7 26 38
USB_EXTC	USB_85D	USB	USB_EXTC_P	9 19
	USB_85D	USB	USB_EXTC_N	9 19
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 34
	USB_85D	USB	USB_CAMERA_CONN_N	7 34
USB_BT	USB_85D	USB	USB_BT_P	9 34
	USB_85D	USB	USB_BT_N	9 34
USB_BT	USB_85D	USB	USB_BT_CONN_P	7 34
	USB_85D	USB	USB_BT_CONN_N	7 34
T260 USB_BT	USB_85D	USB	USB_BT_WAKE_P	34
T259	USB_85D	USB	USB_BT_WAKE_N	34
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 49
	USB_85D	USB	USB_TPAD_N	9 49
USB_IR	USB_85D	USB	USB_SMC_P	9 41
	USB_85D	USB	USB_SMC_N	9 41
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
T231 USB_T29A	USB_85D	USB	USB_EXTD_XHCI_P	19 26
T232	USB_85D	USB	USB_EXTD_XHCI_N	19 26
T241 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	40
T242	USB_85D	USB	USB_EXTA_MUXED_N	40
T247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 34
T248	USB_85D	USB	USB_CAMERA_N	19 34
T245 USB_EXTA	USB_85D	USB	USB_LT1_P	40
T246	USB_85D	USB	USB_LT1_N	40
T220 USB3_EXTB_TX	USB_85D	USB3	USB3_EXTB_TX_P	19 38
T224	USB_85D	USB3	USB3_EXTB_TX_N	19 38
T227 USB3_EXTB_RX	USB_85D	USB3	USB3_EXTB_RX_P	7 19 38
T228	USB_85D	USB3	USB3_EXTB_RX_N	7 19 38
T223 USB3_EXTC_TX	USB_85D	USB3	USB3_EXTC_TX_P	9 19
T225	USB_85D	USB3	USB3_EXTC_TX_N	9 19
T229 USB3_EXTC_RX	USB_85D	USB3	USB3_EXTC_RX_P	9 19
T227	USB_85D	USB3	USB3_EXTC_RX_N	9 19
T238 USB3_EXTA_TX	USB_85D	USB3	USB3_EXTA_TX_P	19 40
T239	USB_85D	USB3	USB3_EXTA_TX_N	19 40
T240 USB3_EXTA_RX	USB_85D	USB3	USB3_EXTA_RX_P	19 40
T243	USB_85D	USB3	USB3_EXTA_RX_N	19 40

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
T255 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
T255 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
T254	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
T253 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
T252	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
T251 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 35
T250	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	7 17 41 43 82
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	7 17 41 43 82
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 43
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 44
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 44
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 44
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 44
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 44
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 44
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 53
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 53
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 53
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 53
	HDA_50S	HDA	AUD_SDI_R	53
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 53
	HDA_50S	HDA	HDA_SDOUT_R	17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 43
	SPI_55S	SPI	SPI_CLK	43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 43
	SPI_55S	SPI	SPI_MOSI	43
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 43
	SPI_55S	SPI	SPI_CS0_L	43
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	7 17 38
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_85D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 34
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 34
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	17 34
	PCIE_85D	PCIE	PCIE_AP_D2R_N	17 34
1275 PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	7 34
1276	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	7 34
1277 PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	34
1277	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	34
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_P	39
	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_N	39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_C_P<1..0>	9 39
	PCIE_85D	PCIE	PCIE_SSD_R2D_C_N<1..0>	9 39
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_P<1..0>	9 39
	PCIE_85D	PCIE	PCIE_SSD_D2R_N<1..0>	9 39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_P	39
	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_N	39
1274 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_C_P<1>	39
1275	PCIE_85D	PCIE	PCIE_SSD_D2R_C_N<1>	39
1276 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_P<1>	39
1277	PCIE_85D	PCIE	PCIE_SSD_R2D_N<1>	39
1253 PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17
1254	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17
1262 PCIE_CLK100M_TBT_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	17 35
1261	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	17 35
1255	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
1257	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
1256 PCIE_CLK100M_TBT_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17
1259	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
1258	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
1266	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 25
1270 PCIE_CLK100M	1:1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_P	71 95
1280	1:1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_N	71 95
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 71
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 71
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 38
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 34
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	9 17
1281 PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P	17 39
1282	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N	17 39
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	9 17
1263 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	9 35
1264 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	9 35
1265 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	35
1267 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	35
1268 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	9 35
1269 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	9 35
1270 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	35
1271 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
TBTDP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius’s Thunderbolt Routing Notes

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 35 84
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 35 84
	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 84
	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	35 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1..0>	7 84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1..0>	7 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_P<1..0>	7 35 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_N<1..0>	7 35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	84
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 35 85
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 35 85
	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 85
	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	35 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1..0>	7 85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1..0>	7 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_P<1..0>	7 35 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_N<1..0>	7 35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	85
	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	85

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	35
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	35
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	35
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	35

Only used on hosts supporting Thunderbolt video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 41 44
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 41 44
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	61
	1TO1_DIFFPAIR		CHGR_CSI_N	61
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	61
	1TO1_DIFFPAIR		CHGR_CSO_N	61

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SMC Constraints

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 A<8..0>
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 A<8..0>
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 ABI L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 ABI L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 RAS L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 RAS L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CAS L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CAS L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 WE L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 WE L
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 CKE L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 CKE L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CS L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CS L
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0>
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1>
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2>
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3>
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0>
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1>
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2>
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3>
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1>
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7..0>
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15..8>
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23..16>
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31..24>
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7..0>
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15..8>
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23..16>
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31..24>
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 RESET L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 RESET L

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 A<8..0>
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 A<8..0>
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 ABI L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 ABI L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 RAS L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 RAS L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CAS L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CAS L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 WE L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 WE L
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 CKE L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 CKE L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CS L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CS L
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7..0>
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15..8>
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23..16>
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31..24>
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7..0>
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15..8>
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23..16>
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31..24>
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 RESET L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 RESET L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P
	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_AUX_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P
	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P
	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTALIN
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTALOUT
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_SSIN
	1:1_DIFFPAIR		PEX_TSTCLK_O_P
	1:1_DIFFPAIR		PEX_TSTCLK_O_N
HDMI_DATA	HDMI_90D	HDMI	HDMI_EG_DATA_C_P<2..0>
	HDMI_90D	HDMI	HDMI_EG_DATA_C_N<2..0>
HDMI_CLK	HDMI_90D	HDMI	HDMI_EG_CLK_C_P
	HDMI_90D	HDMI	HDMI_EG_CLK_C_N

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GPU (Kepler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_55S_CPUIMVPISNS1	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	47
	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 77
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 77
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	45 62
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	45 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	45
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_R_P	45
	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	45 67
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	45 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	45
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	
	SENSE_1TO1_55S	SENSE	GPUISENS_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_N	45
	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_P	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	96
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	96
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	96
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	96
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
	SENSE_1TO1_55S	SENSE	GPUFB_CS_P	74 99
	SENSE_1TO1_55S	SENSE	GPUFB_CS_N	74 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	98
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P	74 98
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N	74 98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	99
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	99
SENSE_DIFFPAIR_42	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	46 66
SENSE_DIFFPAIR_42	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	46 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	46
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	46
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_VSENSE_P	
	AUDIODIFF	AUDIO	ADC1_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_VSENSE_P	
	AUDIODIFF	AUDIO	ADC2_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_R_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_R_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_L_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_L_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_P	99
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_R_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	99

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 34
	1TO1_DIFFPAIR		CHGR_CSI_R_P	61
	1TO1_DIFFPAIR		CHGR_CSI_R_N	61
	1TO1_DIFFPAIR		CHGR_CSO_R_P	61
	1TO1_DIFFPAIR		CHGR_CSO_R_N	61
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	
	USB_85D	USB	USB_LT2_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SL_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SR_P	
	AUDIODIFF	AUDIO	SSM2375SR_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P_R	
	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N_R	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_P	
	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_P	
	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P_R	
	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N_R	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSUBIN_P	57
	DIFFPAIR	AUDIO	RSUBIN_N	57
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSUBIN_P	57
	DIFFPAIR	AUDIO	LSUBIN_N	57
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SR_P	
	DIFFPAIR	AUDIO	SSM4321SR_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SL_P	
	DIFFPAIR	AUDIO	SSM4321SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_N	
USB_85D	USB	USB_TPAD_R_P		26 49
USB_85D	USB	USB_TPAD_R_N		26 49
SB_POWER		PP3V3_S5		7 8
SB_POWER		PP3V3_S0		7 8
SB_POWER		PP1V5_S3RS0_CPUDDR		8
GND		GND		

SYNC_MASTER=D2_CLEAN SYNC_DATE=03/15/2012

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Project Specific Constraints

Apple Inc.

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15" MBP BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?

15" MBP Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
11	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_ISENSE_P	
12		AUDIODIFF	AUDIO	ADC1_ISENSE_N	
13	SENSE_DIFFPAIR_42	THERM_5S5_CPUIMVDPISNS1	THERM	CPUIMVP_ISNS1_P	46 65 66
14		THERM_5S5_CPUIMVDPISNS1	THERM	CPUIMVP_ISNS1_N	46 66
15	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	CPUIMVP_ISNS2G_P	46 66
16		THERM_1TO1_5S5	THERM	CPUIMVP_ISNS2G_N	46 66
17	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	CPUIMVP_ISNS2_P	46 65 66
18		THERM_1TO1_5S5	THERM	CPUIMVP_ISNS2_N	46 66
19	SENSE_DIFFPAIR	THERM_5S5_CPUIMVDPISNS1	THERM	CPUIMVP_ISNS3_P	46 65 66
110		THERM_5S5_CPUIMVDPISNS1	THERM	CPUIMVP_ISNS3_N	46 66
111	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	CPUIMVP_ISUM_R_P	46
112		THERM_1TO1_5S5	THERM	CPUIMVP_ISUM_R_N	46
113	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	CPUIMVP_ISUMG_R_P	46
114		THERM_1TO1_5S5	THERM	CPUIMVP_ISUMG_R_N	46
115	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	GFXIMVP_ISNS1_P	80
116		THERM_1TO1_5S5	THERM	GFXIMVP_ISNS1_N	80
117	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	GFXIMVP_ISNS2_P	80
118		THERM_1TO1_5S5	THERM	GFXIMVP_ISNS2_N	80
119	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	ISNS_CPU_DDR_R_P	98
120		THERM_1TO1_5S5	THERM	ISNS_CPU_DDR_R_N	98
121	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	ISNS_LCD_PANEL_P	
122		THERM_1TO1_5S5	THERM	ISNS_LCD_PANEL_N	
123	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	ISNS_P1V5R1V35_CPUDDR_P	
124		THERM_1TO1_5S5	THERM	ISNS_P1V5R1V35_CPUDDR_N	
126	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	ISNS_SSD_P	39 99
125		THERM_1TO1_5S5	THERM	ISNS_SSD_N	39 99
128	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	ISNS_SSD_R_P	99
127		THERM_1TO1_5S5	THERM	ISNS_SSD_R_N	99
130	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	PCHVCCIOS0_CS_P	87 99
129		THERM_1TO1_5S5	THERM	PCHVCCIOS0_CS_N	87 99
132	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	PCH_VCCIOSENSE_P	87
131		THERM_1TO1_5S5	THERM	PCH_VCCIOSENSE_N	87
167	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P	79 80
168	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N	79 80
164		THERM_1TO1_5S5	THERM	GPU_FBVDDQ_SENSE	73 74
163		THERM_1TO1_5S5	THERM	GPU_FBGND_SENSE	73 74
155		THERM_1TO1_5S5	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	74 79
156		THERM_1TO1_5S5	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	74 79
133	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	SPKRL_THMSNS_D2_P	
134		THERM_1TO1_5S5	THERM	SPKRL_THMSNS_D2_N	
135	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	SPKR_THMSNS_D2_P	
136		THERM_1TO1_5S5	THERM	SPKR_THMSNS_D2_N	
137	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	TBT_THERMD_P	47
138		THERM_1TO1_5S5	THERM	TBT_THERMD_N	47
139	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	X29THMSNS_D2_P	
140		THERM_1TO1_5S5	THERM	X29THMSNS_D2_N	
157	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	VDDCIS0_CS_P	
158	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	VDDCIS0_CS_N	
159	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	GFXIMVP6_VSEN_P	
160	SENSE_DIFFPAIR	THERM_1TO1_5S5	THERM	GFXIMVP6_VSEN_N	
141		USB_85D	USB3	USB3_EXTA_TX_F_P	
142		USB_85D	USB3	USB3_EXTA_TX_F_N	
143		USB_85D	USB3	USB3_EXTA_RX_F_P	
144		USB_85D	USB3	USB3_EXTA_RX_F_N	
145		USB_85D	USB3	USB3_EXTA_TX_C_P	40
146		USB_85D	USB3	USB3_EXTA_TX_C_N	40
147		USB_85D	USB3	USB3_EXTB_TX_C_P	7 38
148		USB_85D	USB3	USB3_EXTB_TX_C_N	7 38
149		USB_85D	USB3	USB3_EXTB_RX_RC_P	38
150		USB_85D	USB3	USB3_EXTB_RX_RC_N	38
170		USB_85D	USB3	USB3_EXTA_RX_RC_P	40
169		USB_85D	USB3	USB3_EXTA_RX_RC_N	40
161			CLK_25M	P1V5_GPU_VSNS	
162			CLK_25M	P1V0S0_VSNS	

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.058 MM	?
2:1_SPACING	TOP,BOTTOM	0.116 MM	?
3:1_SPACING	TOP,BOTTOM	0.174 MM	?
4:1_SPACING	TOP,BOTTOM	0.232 MM	?
5:1_SPACING	TOP,BOTTOM	0.290 MM	?
1:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
2:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.106 MM	?
3:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.159 MM	?
4:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.212 MM	?
5:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.265 MM	?
1:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?
2:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.202 MM	?
3:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.303 MM	?
4:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.404 MM	?
5:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.505 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
2x_DIELECTRIC	TOP,BOTTOM	0.116 MM	?
3x_DIELECTRIC	TOP,BOTTOM	0.174 MM	?
4x_DIELECTRIC	TOP,BOTTOM	0.232 MM	?
5x_DIELECTRIC	TOP,BOTTOM	0.290 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
2x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.106 MM	?
3x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.159 MM	?
4x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.212 MM	?
5x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.265 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?
2x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.202 MM	?
3x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.303 MM	?
4x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.404 MM	?
5x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.505 MM	?

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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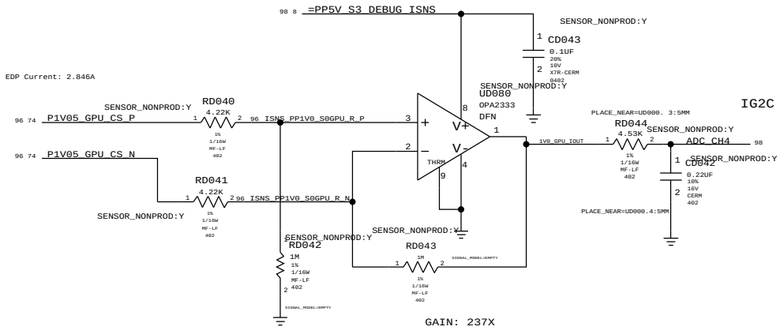
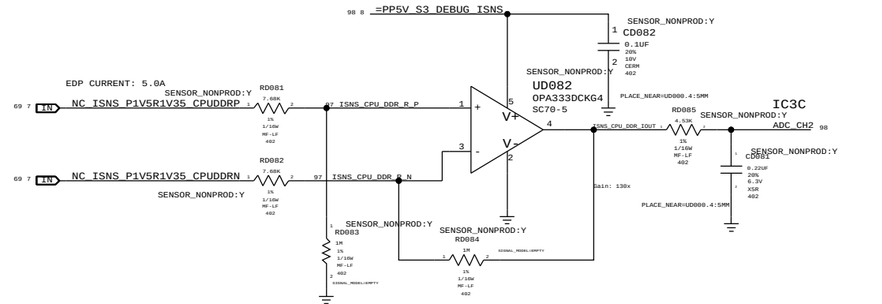
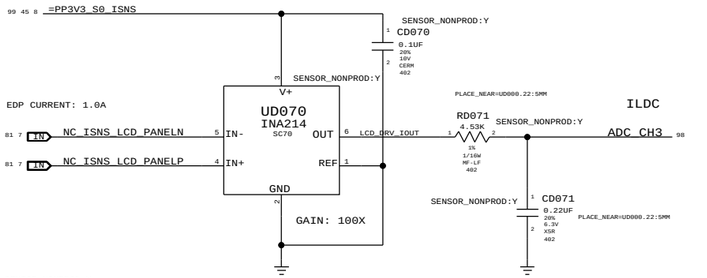
GPU 1.0V CURRENT SENSE



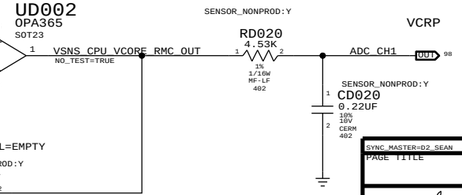
CPU DDR CURRENT SENSE



LCD PANEL CURRENT SENSE

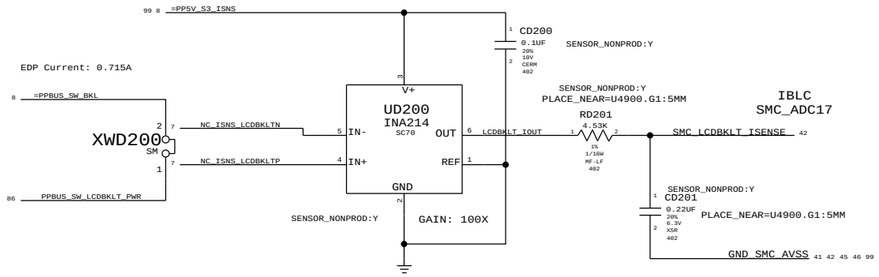


VCRP

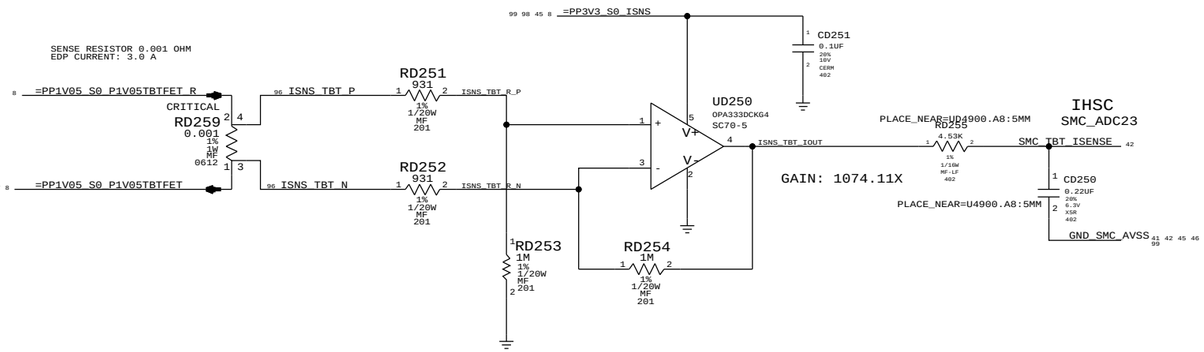


SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2013
PAGE TITLE	DEBUG SENSORS AND ADC
Apple Inc.	DRAWING NUMBER 051-9589 · SIZE D · REVISION 4.18.0 · BRANCH · PAGE 130 OF 132 · SHEET 98 OF 99

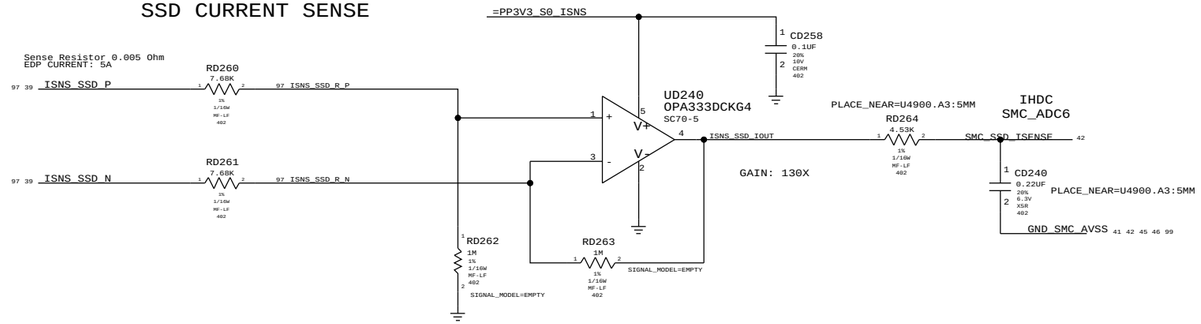
LCD BKLT Current Sense



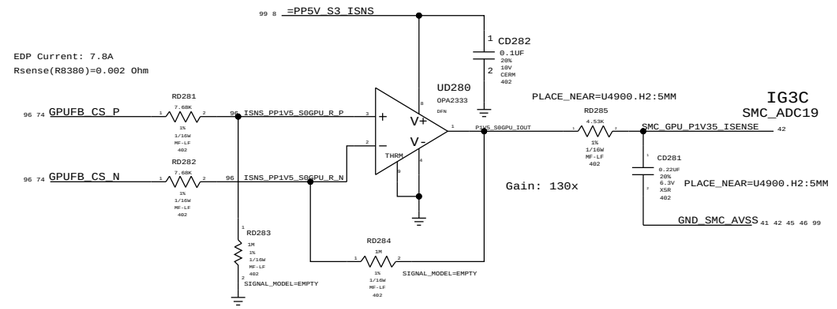
TBT (T29) CURRENT SENSE



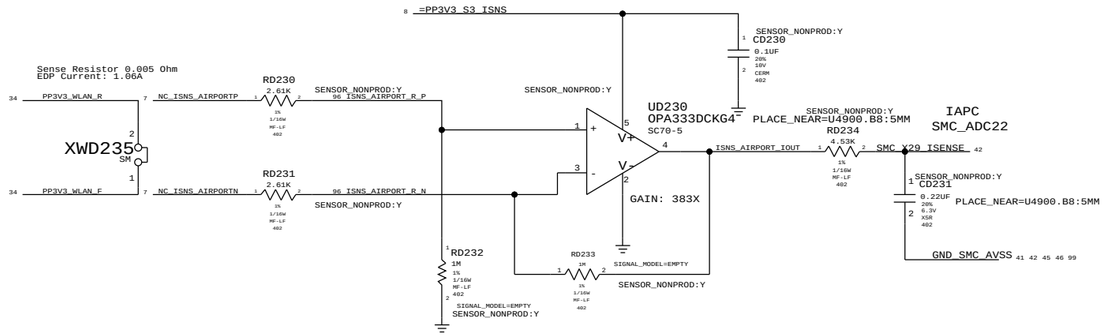
SSD CURRENT SENSE



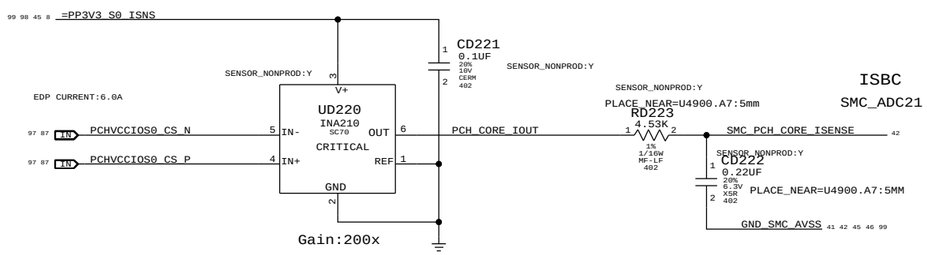
GPU FB (1.35V/1.5V) CURRENT SENSE



X29 AIRPORT CURRENT SENSE

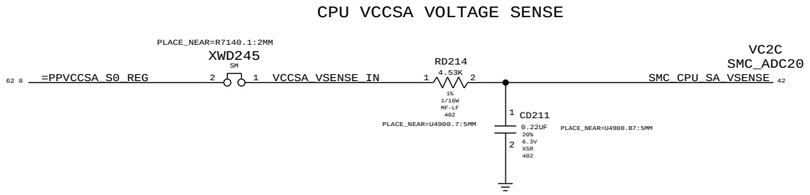


PCH VCORE CURRENT SENSE

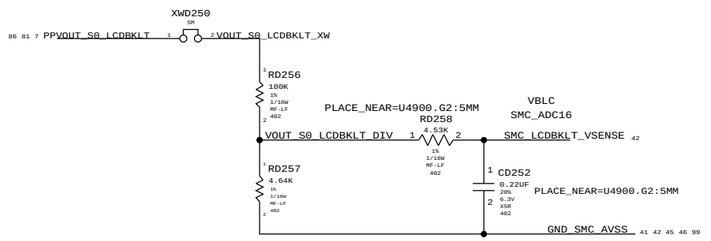


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	4	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	CD201,CD222,CD231		SENSOR_NONPROD:N

CPU VCCSA VOLTAGE SENSE



LCD BKLT Voltage Sense



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SMC12 SENSORS EXTENDED

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