1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,J45

DVT 8/6/2013

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM,MLB,J45	SCH	CRITICAL	
820-3662	1	PCBF,MLB,J45	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Tue Aug 6 17:09:28 2013

DRAWING TITLE: <PART_DESCRIPTION>

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW,SR18J,,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	CRW,SR18H,PRQ,C0,2.3,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	CRW,SR1BS,PRQ,C0,2.6,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC,SPI SRL 50MHZ,FLASH,64MBIT,SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TFT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2030, U7001)

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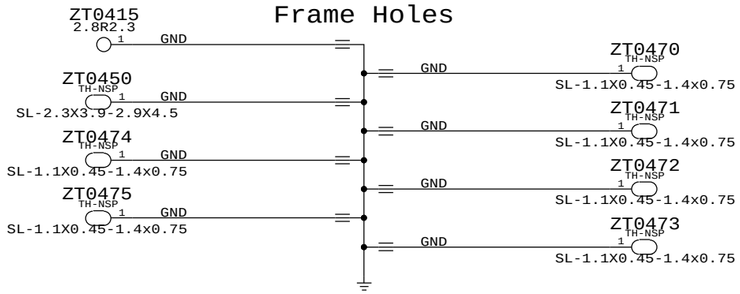
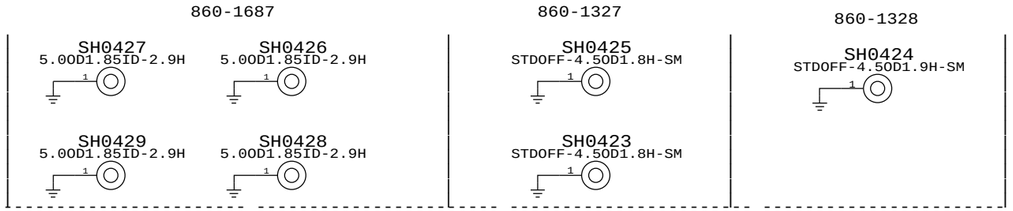
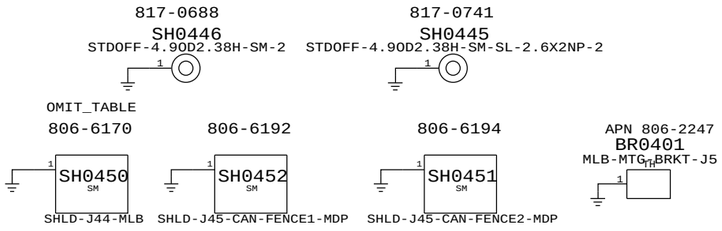
Frame Holes

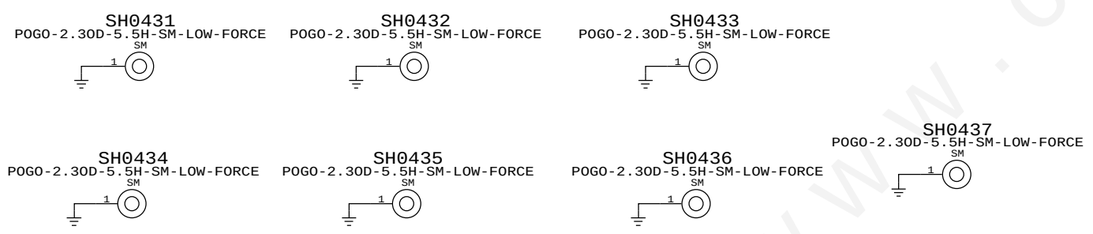


J45 THERMAL MODULE STANDOFF

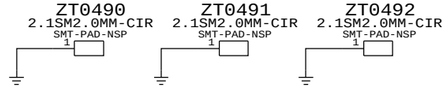




J45 POGO PINS

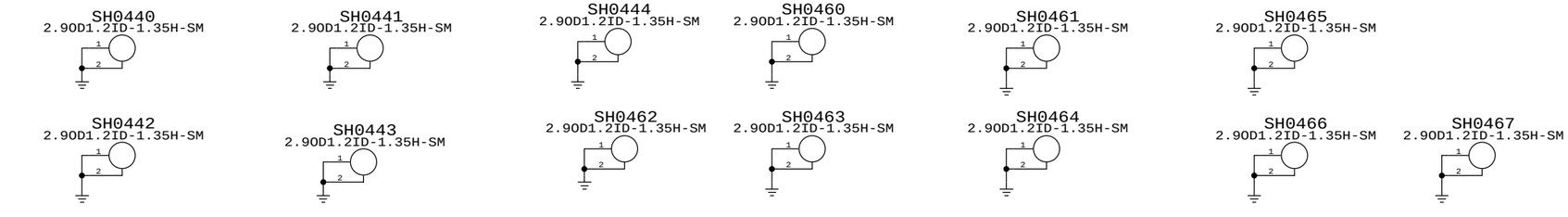


SMT GND TEST PONTS



J45 StAND OFF

860-1448



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR,REAR,MLB,J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR,CPU,J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR,PCH,J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER,mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB,J45	SH0450	CRITICAL	

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PAGE TITLE: PD Parts

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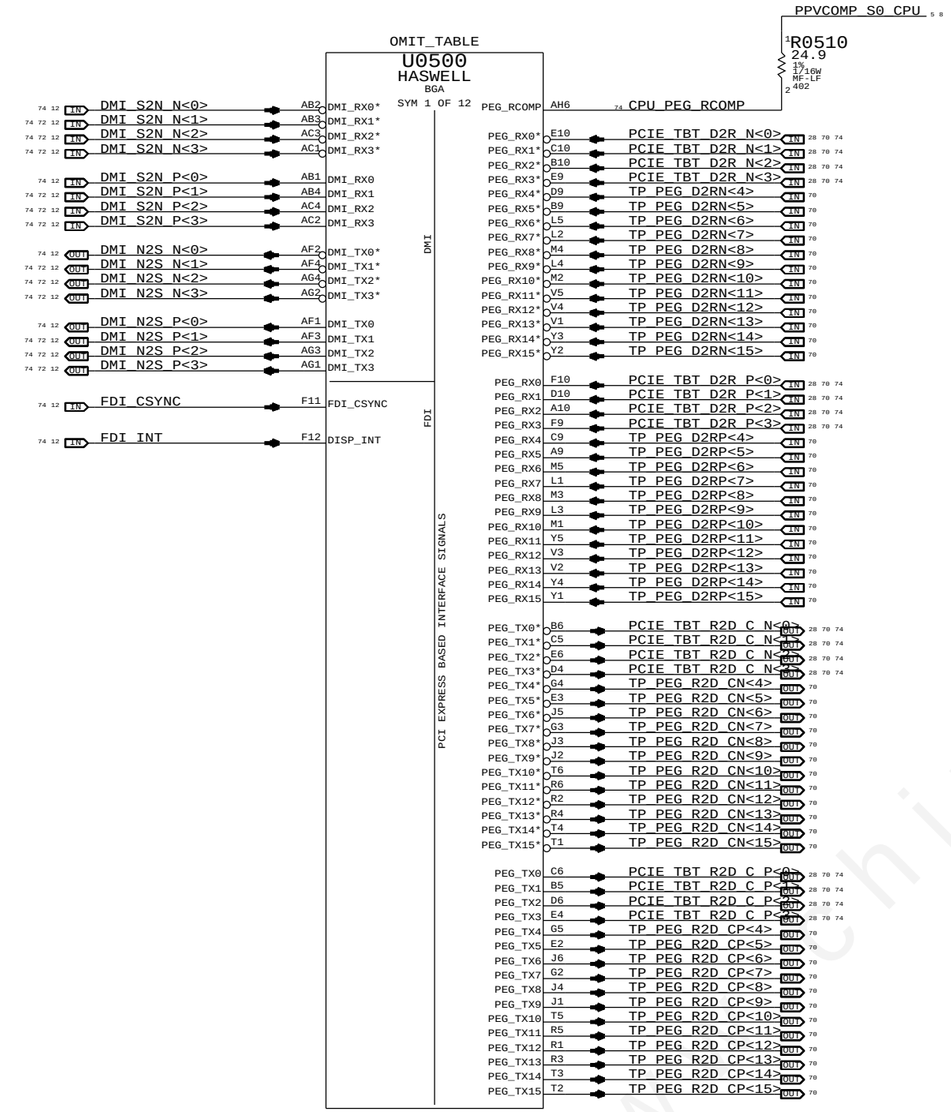

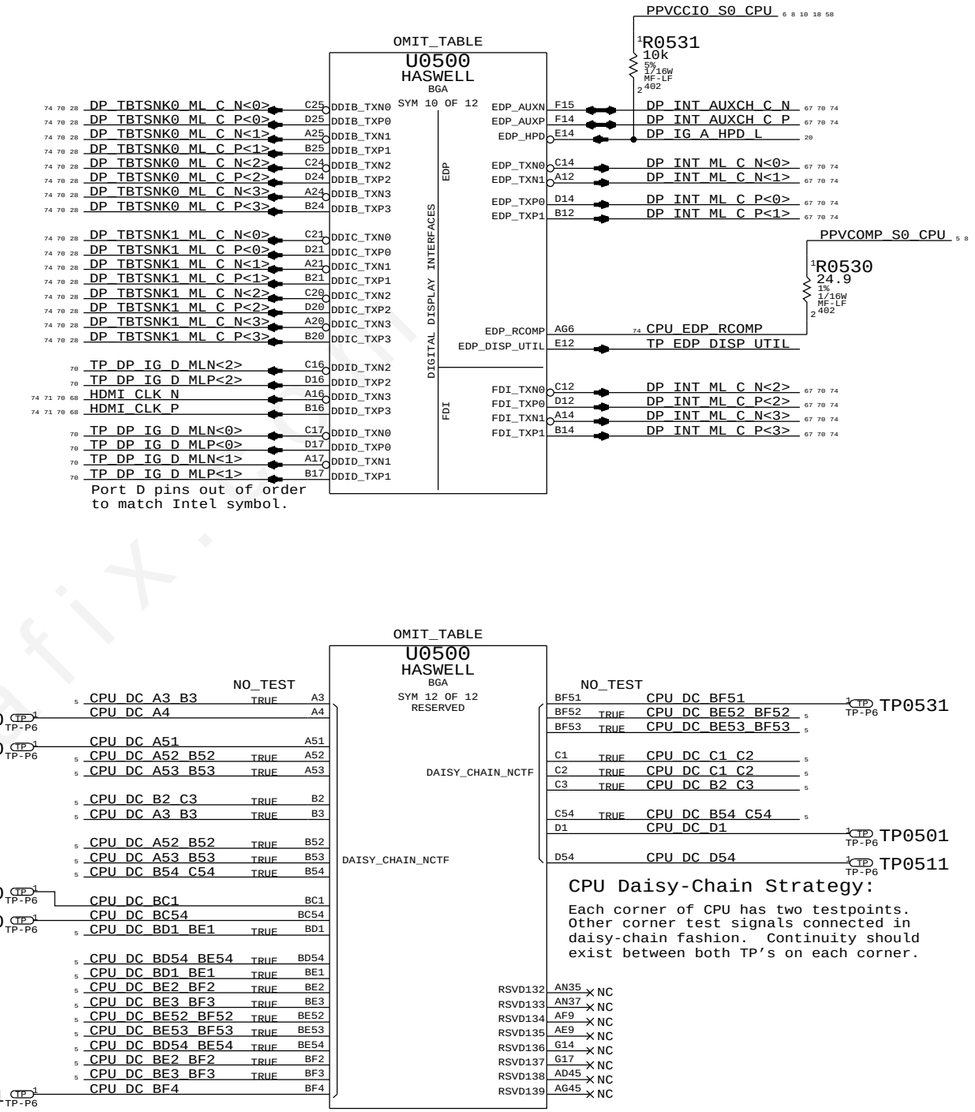

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PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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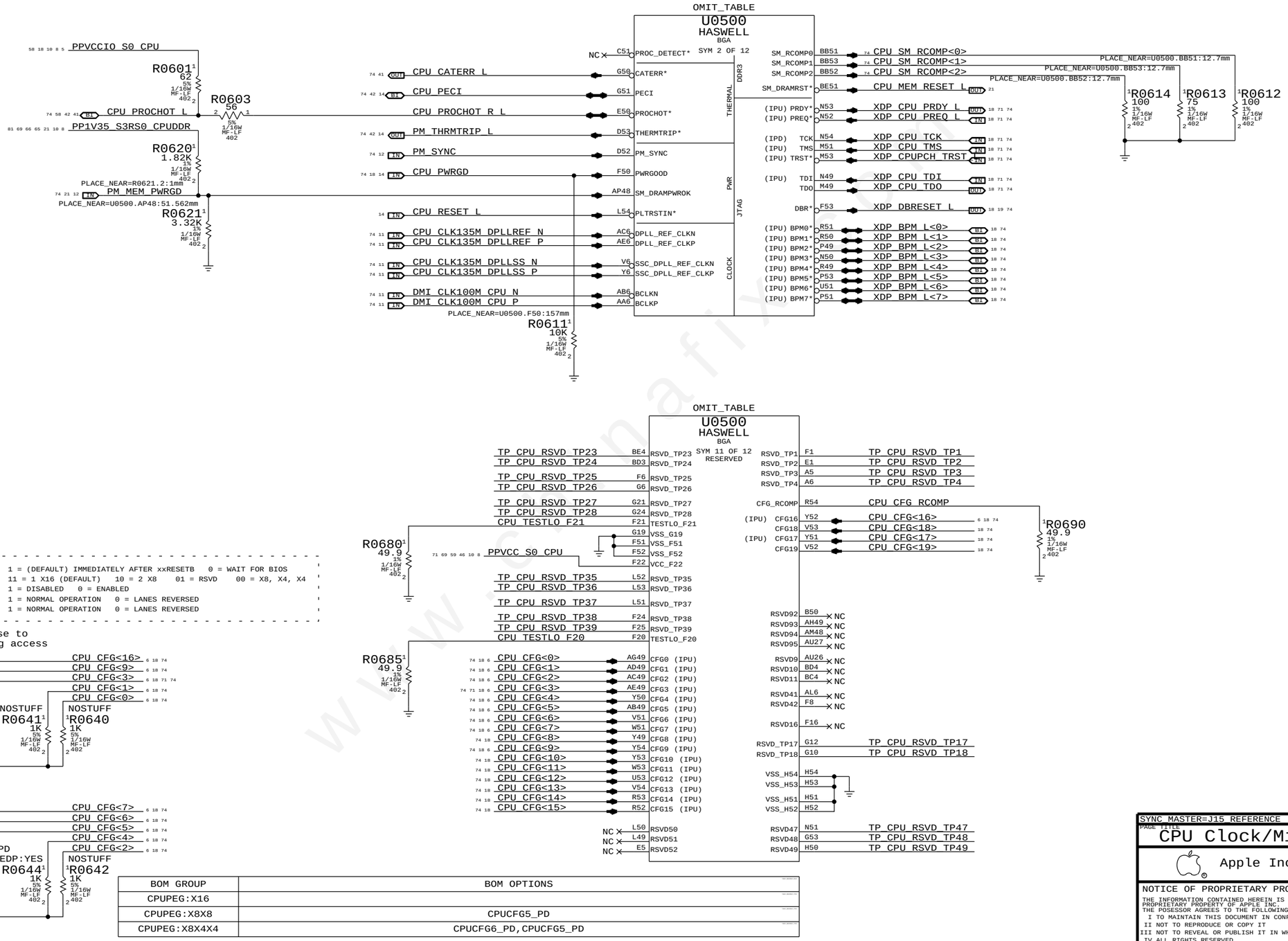

BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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CPU Clock/Misc/JTAG/CFG

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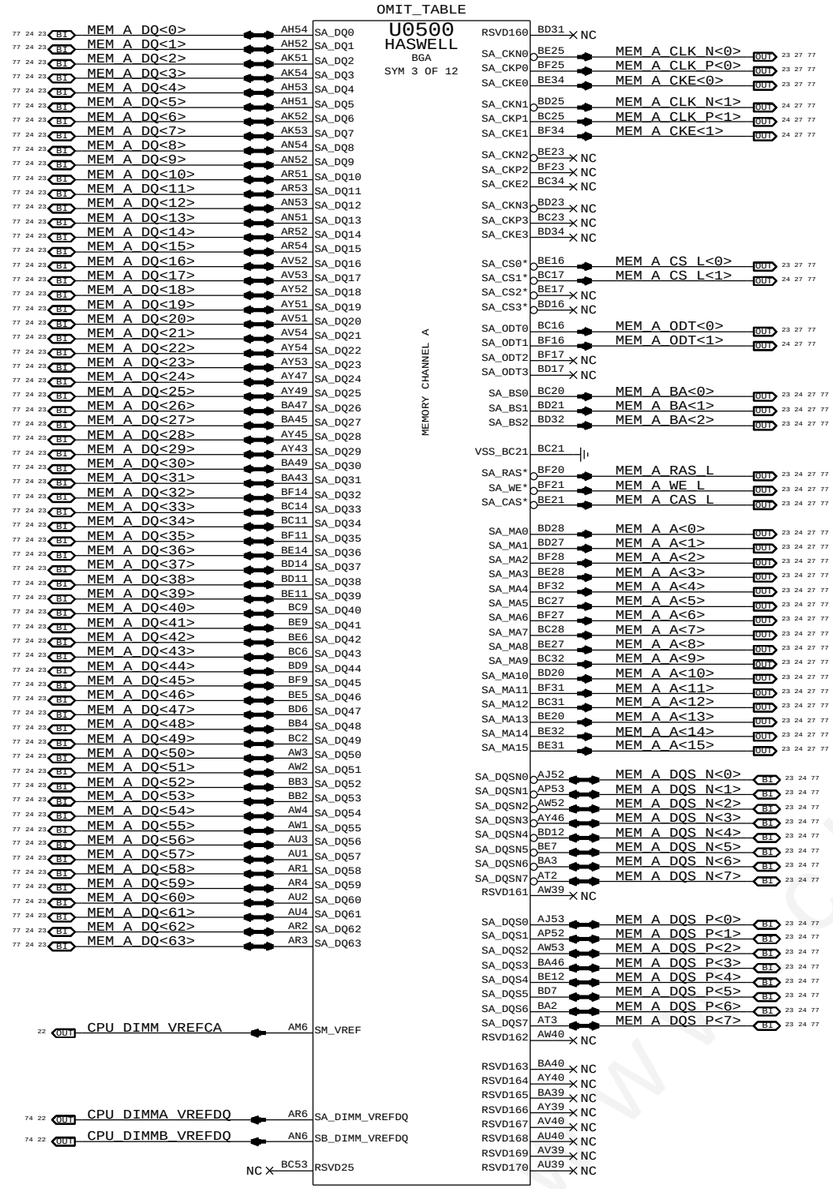

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CPU DDR3 Interfaces

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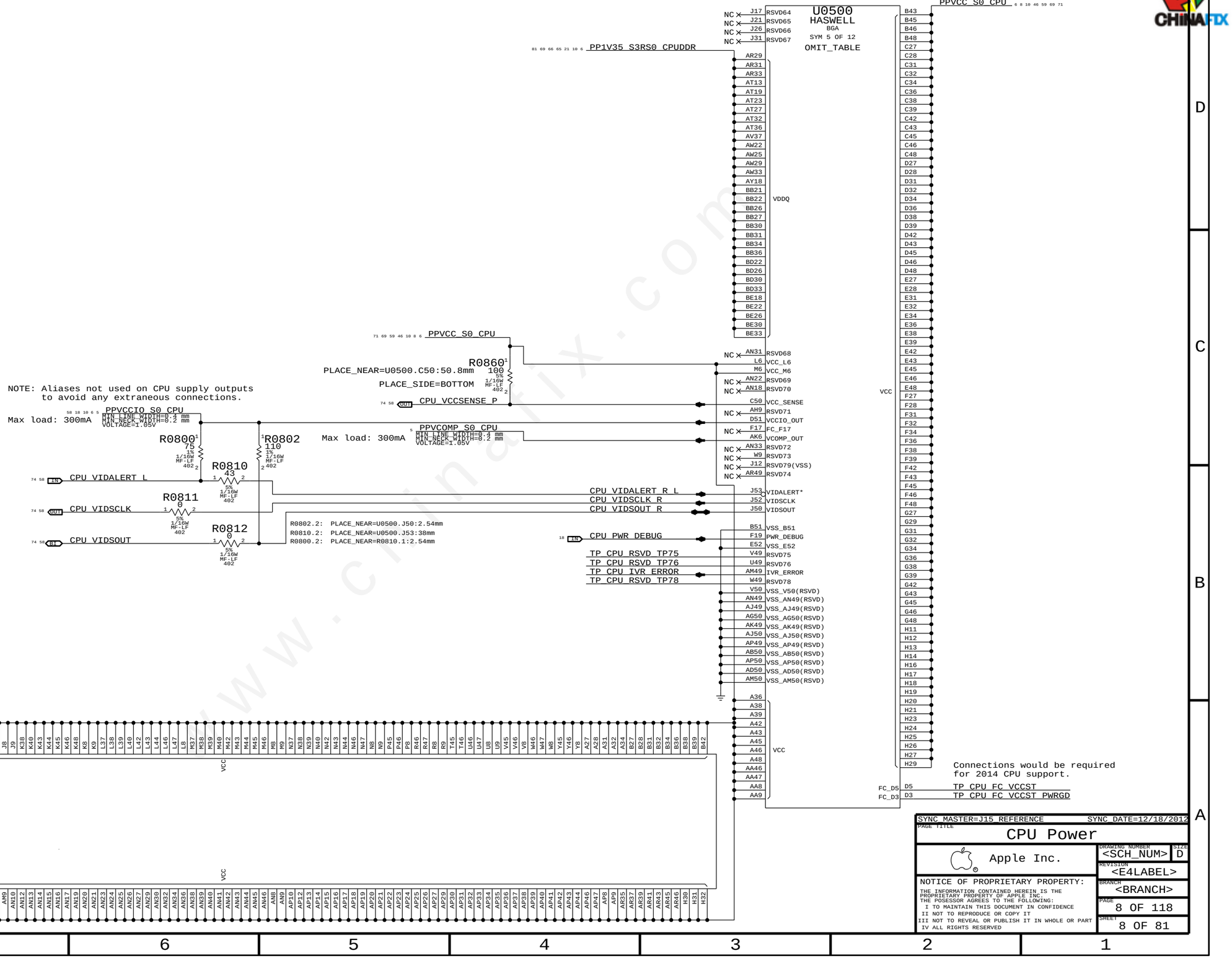
U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE
PP1V35_S3RS0_CPUDDR
PPVCC_S0_CPU
VDDQ
VCC
VCC_SENSE
VCCIO_OUT
FC_F17
VCOMP_OUT
VIDALERT*
VIDSCLK
VIDSOUT
VSS_B51
PWR_DEBUG
VSS_E52
RSVD75
RSVD76
IVR_ERROR
RSVD78
VSS_V50(RSVD)
VSS_AN49(RSVD)
VSS_AJ49(RSVD)
VSS_AG50(RSVD)
VSS_AK49(RSVD)
VSS_AJ50(RSVD)
VSS_AP49(RSVD)
VSS_AB50(RSVD)
VSS_AP50(RSVD)
VSS_AD50(RSVD)
VSS_AM50(RSVD)
RSVD68
VCC_L6
VCC_M6
RSVD69
RSVD70
RSVD71
RSVD72
RSVD73
RSVD79(VSS)
RSVD74
R0860 100 1% 1/10W MF-LF 402
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
CPU_VCCSENSE_P
PPVCCIO_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
R0800 75 1% 1/10W MF-LF 402
R0802 110 1% 1/16W MF-LF 402
R0810 43 5% 1/16W MF-LF 402
R0811 0 5% 1/16W MF-LF 402
R0812 0 5% 1/16W MF-LF 402
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
PPVCOMP_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_PWR_DEBUG
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78
R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.
Connections would be required
for 2014 CPU support.
FC_D5 TP_CPU_FC_VCCST
FC_D3 TP_CPU_FC_VCCST_PWRGD
OMIT_TABLE
U0500
HASWELL
BGA
SYM 6 OF 12
POWER
SYNC_MASTER=J15_REFERENCE
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CPU Power
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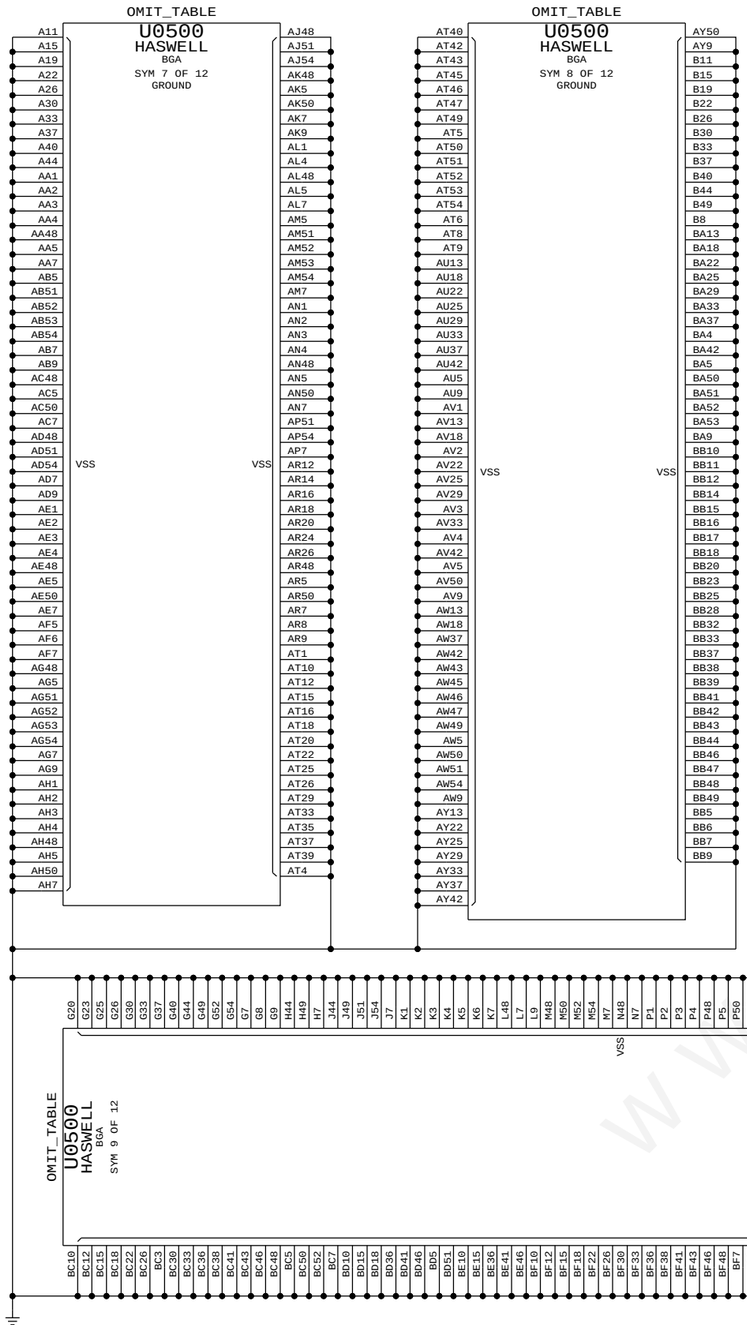

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CPU Ground

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

71 60 59 46 8 6 PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 | C1001 1UF 10% 10V X6S-CERM 0402 | C1002 1UF 10% 10V X6S-CERM 0402 | C1003 1UF 10% 10V X6S-CERM 0402 | C1004 1UF 10% 10V X6S-CERM 0402 | C1005 1UF 10% 10V X6S-CERM 0402 | C1006 1UF 10% 10V X6S-CERM 0402 | C1007 1UF 10% 10V X6S-CERM 0402 | C1008 1UF 10% 10V X6S-CERM 0402 | C1009 1UF 10% 10V X6S-CERM 0402 | C1010 1UF 10% 10V X6S-CERM 0402 | C1011 1UF 10% 10V X6S-CERM 0402 | C1012 1UF 10% 10V X6S-CERM 0402 | C1013 1UF 10% 10V X6S-CERM 0402 | C1014 1UF 10% 10V X6S-CERM 0402 | C1015 1UF 10% 10V X6S-CERM 0402 | C1016 1UF 10% 10V X6S-CERM 0402 | C1017 1UF 10% 10V X6S-CERM 0402 | C1018 1UF 10% 10V X6S-CERM 0402 | C1019 1UF 10% 10V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

CAPs for Acoustic control (C109A-C102D)

C1020 20UF 20% 4V X5R-CERM 0402-2 | C1021 20UF 20% 4V X5R-CERM 0402-2 | C1022 20UF 20% 4V X5R-CERM 0402-2 | C1023 20UF 20% 4V X5R-CERM 0402-2 | C109A 20UF 20% 4V X5R-CERM 0402-2 | C109B 20UF 20% 4V X5R-CERM 0402-2 | C109C 20UF 20% 4V X5R-CERM 0402-2 | C109D 20UF 20% 4V X5R-CERM 0402-2 | C109E 20UF 20% 4V X5R-CERM 0402-2 | C109F 20UF 20% 4V X5R-CERM 0402-2 | C101A 20UF 20% 4V X5R-CERM 0402-2 | C101B 20UF 20% 4V X5R-CERM 0402-2 | C101C 20UF 20% 4V X5R-CERM 0402-2 | C101D 20UF 20% 4V X5R-CERM 0402-2 | C101E 20UF 20% 4V X5R-CERM 0402-2 | C101F 20UF 20% 4V X5R-CERM 0402-2 | C102A 20UF 20% 4V X5R-CERM 0402-2 | C102B 20UF 20% 4V X5R-CERM 0402-2 | C102C 20UF 20% 4V X5R-CERM 0402-2 | C102D 20UF 20% 4V X5R-CERM 0402-2

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 | C1025 | C1026 | C1027 | C1028 | C1029 | C1030 | C1031 | C1032 | C1033 | C1034 | C1035 | C1036 | C1037 | C1038 | C1039 | C1040 | C1041 | C1042 | C1043 | C1044 | C1045

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2 | C1047 | C1048 | C1049 | C1050 | C1051 | C1052 | C1053 | C1054 | C1055 | C1056 | C1057 | C1058 | C1059 | C1060 | C1061 | C1062 | C1063 | C1064 | C1065 | C1066 | C1067

PLACEMENT_NOTE (C1068-C1076:

NO STUFF NO STUFF

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S | C1069 | C1070 | C1071 | C1072 | C1073 | C1074 | C1075 | C1076 | C1077

CAPs for Acoustic control (C102E-C103F)

NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF

C102E 20UF 20% 4V X5R-CERM 0402-2 | C102F | C103A | C103B | C103C | C103D | C103E | C103F

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

66 65 21 8 6 81 80 PP1V35_S3RS0_CPUDDR

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402 | C1081 | C1082 | C1083 | C1084 | C1085 | C1086 | C1087 | C1088 | C1089

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603 | C1091 | C1092 | C1093 | C1094 | C1095 | C1096 | C1097

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO

CRITICAL C1099 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO

(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

58 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(1 OF 11)

SYSCLK_CLK32K_RTC — B5 RTCX1; NC — B4 RTCX2

PCH_SRTCRST_L — B9 SRTCRST*
PCH_INTRUDER_L — A8 INTRUDER*
PCH_INTVRMEN_L — G10 INTVRMEN
RTC_RESET_L — D9 RTCRST*

RTC

HDA_BIT_CLK — R1110 33 1/20W MF 201 — HDA_BIT_CLK_R — B25 HDA_BCLK
HDA_SYNC — R1111 33 1/20W MF 201 — HDA_SYNC_R — A22 HDA_SYNC (IPD-boot)
PCH_SPKR — AL10 SPKR (IPD-PLTRST#)
HDA_RST_L — R1112 33 1/20W MF 201 — HDA_RST_R_L — C24 HDA_RST*
HDA_SDIN0 — L22 HDA_SDI0 (IPD)
NC_HDA_SDIN1 — K22 HDA_SDI1 (IPD)
NC_HDA_SDIN2 — G22 HDA_SDI2 (IPD)
NC_HDA_SDIN3 — F22 HDA_SDI3 (IPD)
HDA_SDOUT — R1113 33 1/20W MF 201 — HDA_SDOUT_R — A24 HDA_SDO (IPD-boot)

AZALIA

(IPD-DOCKENN#)
DP_TBT_SEL — B17 DOCKEN*/GPIO33
ENET_MEDIA_SENSE_RDIV — C22 HDA_DOCK_RST*/GPIO13

XDP_PCH_TCK — AB3 JTAG_TCK (IPD)
XDP_PCH_TMS — AD1 JTAG_TMS (IPU)
XDP_PCH_TDI — AE2 JTAG_TDI (IPU)
XDP_PCH_TDO — AD3 JTAG_TDO

JTAG

NC — F8 TP25
NC — C26 TP22
NC — AB6 TP20

SATA_RXN0 — BC8 — NC_SATA_A_D2RN
SATA_RXP0 — BE8 — NC_SATA_A_D2RP
SATA_TXN0 — AW8 — NC_SATA_A_R2D_CN
SATA_TXP0 — AY8 — NC_SATA_A_R2D_CP

SATA_RXN1 — BC10 — NC_SATA_B_D2RN
SATA_RXP1 — BE10 — NC_SATA_B_D2RP
SATA_TXN1 — AV10 — NC_SATA_B_R2D_CN
SATA_TXP1 — AW10 — NC_SATA_B_R2D_CP

SATA_RXN2 — BB9 — NC_SATA_ODD_D2RN
SATA_RXP2 — BD9 — NC_SATA_ODD_D2RP
SATA_TXN2 — AY13 — NC_SATA_ODD_R2D_CN
SATA_TXP2 — AW13 — NC_SATA_ODD_R2D_CP

SATA_RXN3 — BC12 — NC_SATA_D_D2RN
SATA_RXP3 — BE12 — NC_SATA_D_D2RP
SATA_TXN3 — AR13 — NC_SATA_D_R2D_CN
SATA_TXP3 — AT13 — NC_SATA_D_R2D_CP

SATA_RXN4/PERN1 — BD13 — TP_PCIE_ENET_D2RN
SATA_RXP4/PERP1 — BB13 — TP_PCIE_ENET_D2RP
SATA_TXN4/PETN1 — AV15 — TP_PCIE_ENET_R2D_CN
SATA_TXP4/PETP1 — AW15 — TP_PCIE_ENET_R2D_CP

SATA_RXN5/PERN2 — BC14 — NC_SATA_F_D2RN
SATA_RXP5/PERP2 — BE14 — NC_SATA_F_D2RP
SATA_TXN5/PETN2 — AP15 — NC_SATA_F_R2D_CN
SATA_TXP5/PETP2 — AR15 — NC_SATA_F_R2D_CP

SATA

SATA_RCOMP — AY5 — PCH_SATA_RCOMP
SATALED* — AP3 — PCH_SATALED_L
SATA0GP/GPIO21 — AT1 — XDP_DC0_DP_AUXCH_ISOL_L
SATA1GP/GPIO19 (IPU-PLTRST#) — AU2 — XDP_DC1_SATARDRVR_EN
SATA_IREF — BD4

TP9 — BA2 — NC
TP8 — BB2 — NC

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCIe:
Reserved: Ethernet
(if not combo w/SD Card)

Unused

PP1V5_S0 — R1130 7.5K 1% 1/20W MF 201 — PCH_SATA_RCOMP
PLACE_NEAR=U1100.AY5:2.54mm

PPVRTC_G3H
R1100 330K 5% 1/20W MF 201
R1101 1M 5% 1/20W MF 201
R1102 20K 5% 1/20W MF 201
R1103 20K 5% 1/20W MF 201

PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L

C1102 1UF 10% 10V X5R 402
C1103 1UF 10% 10V X5R 402

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(2 OF 11)

PCIE_CLK100M_SSD_N — Y43 CLKOUT_PCIE_N0
PCIE_CLK100M_SSD_P — Y45 CLKOUT_PCIE_P0
SSD_CLKREQ_L — AB1 PCIECLKRQ0*/GPIO73

NC_PCIE_CLK100M_ENETSDN — AA44 CLKOUT_PCIE_N1
NC_PCIE_CLK100M_ENETSDP — AA42 CLKOUT_PCIE_P1
XDP_DD2_ENETSD_CLKREQ_L — AF1 PCIECLKRQ1*/GPIO18

PCIE_CLK100M_AP_N — AB43 CLKOUT_PCIE_N2
PCIE_CLK100M_AP_P — AB45 CLKOUT_PCIE_P2
XDP_DD3_AP_CLKREQ_L — AF3 PCIECLKRQ2*/GPIO20/SMI*

PCIE_CLK100M_CAMERA_N — AD43 CLKOUT_PCIE_N3
PCIE_CLK100M_CAMERA_P — AD45 CLKOUT_PCIE_P3
CAMERA_CLKREQ_L — T3 PCIECLKRQ3*/GPIO25

NC_PCIE_CLK100M_GPUN — AF43 CLKOUT_PCIE_N4
NC_PCIE_CLK100M_GPUP — AF45 CLKOUT_PCIE_P4
TBT_CLKREQ_L — V3 PCIECLKRQ4*/GPIO26

NC_PCIE_CLK100M_PE5N — AE44 CLKOUT_PCIE_N5
NC_PCIE_CLK100M_PE5P — AE42 CLKOUT_PCIE_P5
PCH_CLKRQ5_L_GPIO44 — AA2 PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)

NC_PCIE_CLK100M_SWN — AB40 CLKOUT_PCIE_N6
NC_PCIE_CLK100M_SWP — AB39 CLKOUT_PCIE_P6
PEG_CLKREQ_L — AE4 PCIECLKRQ6*/GPIO45

PCIE_CLK100M_TBT_N — AJ44 CLKOUT_PCIE_N7
PCIE_CLK100M_TBT_P — AJ42 CLKOUT_PCIE_P7
PCH_CLKRQ7_L_GPIO46 — Y3 PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)

NC_ITPXDP_CLK100MN — AH43 CLKOUT_ITPXDP_N
NC_ITPXDP_CLK100MP — AH45 CLKOUT_ITPXDP_P

LPC_CLK33M_SMC_R — D44 CLKOUT_33MHZ0 (IPD-PWROK)
LPC_CLK33M_LPCPLUS_R — E44 CLKOUT_33MHZ1 (IPD-PWROK)
NC_PCI_CLK33M_OUT2 — B42 CLKOUT_33MHZ2 (IPD-PWROK)
NC_PCI_CLK33M_OUT3 — F41 CLKOUT_33MHZ3 (IPD-PWROK)
PCH_CLK33M_PCIOUT — A40 CLKOUT_33MHZ4 (IPD-PWROK)

CLOCKS

CLKOUT_PEG_A_N — AB35 — NC_PCIE_CLK100M_ENETN
CLKOUT_PEG_A_P — AB36 — NC_PCIE_CLK100M_ENETP
PEG_A_CLKRQ*/GPIO47 — AF6 — ENET_CLKREQ_L

CLKOUT_PEG_B_N — Y39 — NC_PCIE_CLK100M_PEGBN
CLKOUT_PEG_B_P — Y38 — NC_PCIE_CLK100M_PEGBP
PEG_B_CLKRQ*/GPIO56 — U4 — PCH_PEGCLKRQB_L_GPIO56

CLKOUT_DMI_N — AF39 — DMI_CLK100M_CPU_N
CLKOUT_DMI_P — AF40 — DMI_CLK100M_CPU_P

CLKOUT_DP_N — AJ40 — CPU_CLK135M_DPLLSS_N
CLKOUT_DP_P — AJ39 — CPU_CLK135M_DPLLSS_P

CLKOUT_DPNS_N — AF35 — CPU_CLK135M_DPLLREF_N
CLKOUT_DPNS_P — AF36 — CPU_CLK135M_DPLLREF_P

CLKIN_DMI_N — AY24 — PCIE_CLK100M_PCH_N
CLKIN_DMI_P — AW24 — PCIE_CLK100M_PCH_P

CLKIN_GND_N — AR24 — PCH_CLKIN_GNDN
CLKIN_GND_P — AT24 — PCH_CLKIN_GNDP

CLKIN_DOT96_N — H33 — PCH_CLK96M_DOT_N
CLKIN_DOT96_P — G33 — PCH_CLK96M_DOT_P

CLKIN_SATA_N — BE6 — PCH_CLK100M_SATA_N
CLKIN_SATA_P — BC6 — PCH_CLK100M_SATA_P

REFCLK14IN — F45 — PCH_CLK14P3M_REFCLK
CLKIN_33MHZLOOPBACK — D17 — PCH_CLK33M_PCIIN

XTAL25_IN — AM43 — SYSCLK_CLK25M_SB_R
XTAL25_OUT — AL44 — NC

(IPD-PWROK) CLKOUTFLEX0/GPIO64 — C40 — NC_PCH_GPIO64_CLKOUTFLEX0
(IPD-PWROK) CLKOUTFLEX1/GPIO65 — F38 — NC_PCH_GPIO65_CLKOUTFLEX1
(IPD-PWROK) CLKOUTFLEX2/GPIO66 — F36 — NC_PCH_GPIO66_CLKOUTFLEX2
(IPD-PWROK) CLKOUTFLEX3/GPIO67 — F39 — NC_PCH_GPIO67_CLKOUTFLEX3

ICLK_IREF — AM45 — PP1V5_S0

TP19 — AD39 — NC
TP18 — AD38 — NC

DIFFCLK_BIASREF — AN44 — PCH_DIFFCLK_BIASREF
PLACE_NEAR=U1100.AN44:2.54mm
R1190 7.5K 1% 1/20W MF 201 — PP1V5_S0

Unused clock terminations for FCIM Mode

R1196 10K 5% 1/20W MF 201 — PCIE_CLK100M_PCH_N
R1195 10K 5% 1/20W MF 201 — PCIE_CLK100M_PCH_P
R1171 10K 5% 1/20W MF 201 — PCH_CLKIN_GNDN
R1170 10K 5% 1/20W MF 201 — PCH_CLKIN_GNDP
R1192 10K 5% 1/20W MF 201 — PCH_CLK96M_DOT_N
R1191 10K 5% 1/20W MF 201 — PCH_CLK96M_DOT_P
R1194 10K 5% 1/20W MF 201 — PCH_CLK100M_SATA_N
R1193 10K 5% 1/20W MF 201 — PCH_CLK100M_SATA_P
R1197 10K 5% 1/20W MF 201 — PCH_CLK14P3M_REFCLK

R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

NOTE: ENET pair only used if SD Card Reader is USB3.

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

PP3V3_SUS
PP3V3_S0

R1177 4.7K 5% 1/20W MF 201 — PCH_SPKR
R1176 10K 5% 1/20W MF 201 — DP_TBT_SEL
R1178 4.7K 5% 1/20W MF 201 — PCH_SATALED_L
R1134 10K 5% 1/20W MF 201 — DP_AUXCH_ISOL_L
R1133 10K 5% 1/20W MF 201 — XDP_DC1_SATARDRVR_EN
R1143 10K 5% 1/20W MF 201 — SSD_CLKREQ_L
R1142 10K 5% 1/20W MF 201 — XDP_DD2_ENETSD_CLKREQ_L
R1169 10K 5% 1/20W MF 201 — AP_CLKREQ_L
R1144 10K 5% 1/20W MF 201 — CAMERA_CLKREQ_L
R1145 10K 5% 1/20W MF 201 — TBT_CLKREQ_L
R1147 10K 5% 1/20W MF 201 — PCH_CLKRQ5_L_GPIO44
R1114 10K 5% 1/20W MF 201 — PEG_CLKREQ_L
R1115 10K 5% 1/20W MF 201 — PCH_CLKRQ7_L_GPIO46
R1146 10K 5% 1/20W MF 201 — ENET_CLKREQ_L
R1148 10K 5% 1/20W MF 201 — PCH_PEGCLKRQB_L_GPIO56
R1179 10K 5% 1/20W MF 201 — ENET_MEDIA_SENSE_RDIV

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC_MASTER=J15_REFERENCE
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PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK

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OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (4 OF 11)

DMI_RXN0 AW22 ← DMI_N2S_N<0>
DMI_RXN1 AR20 ← DMI_N2S_N<1>
DMI_RXN2 AP17 ← DMI_N2S_N<2>
DMI_RXN3 AV20 ← DMI_N2S_N<3>
DMI_RXP0 AY22 ← DMI_N2S_P<0>
DMI_RXP1 AP20 ← DMI_N2S_P<1>
DMI_RXP2 AR17 ← DMI_N2S_P<2>
DMI_RXP3 AW20 ← DMI_N2S_P<3>
DMI_TXN0 BD21 → DMI_S2N_N<0>
DMI_TXN1 BE20 → DMI_S2N_N<1>
DMI_TXN2 BD17 → DMI_S2N_N<2>
DMI_TXN3 BE18 → DMI_S2N_N<3>
DMI_TXP0 BB21 → DMI_S2N_P<0>
DMI_TXP1 BC20 → DMI_S2N_P<1>
DMI_TXP2 BB17 → DMI_S2N_P<2>
DMI_TXP3 BC18 → DMI_S2N_P<3>
DMI_IREF BE16 ← PP1V5_S0 ← R1200 7.5K 1% 1/20W MF 201 → PCH_DMI_RCOMP AY17
PLACE_NEAR=U1100.AY17:12.7mm
TP12 AW17 → NC
TP7 AV17 → NC

FDI_RXN0 AJ35 → NC
FDI_RXN1 AL35 → NC
FDI_RXP0 AJ36 → NC
FDI_RXP1 AL36 → NC
TP16 AV43 → NC
TP5 AY45 → NC
TP15 AV45 → NC
TP10 AW44 → NC
FDI_CSYNC AL39 → FDI_CSYNC → OUT
FDI_INT AL40 → FDI_INT → OUT
FDI_IREF AT45 ← PP1V5_S0 ← R1210 7.5K 1% 1/20W MF 201 → PCH_FDI_RCOMP AR44
PLACE_NEAR=U1100.AR44:12.7mm
TP17 AU42 → NC
TP13 AU44 → NC
PPVRTC_G3H ← R1215 330K 5% 1/20W MF 201 ← PP1V5_S0
R1209 100K 5% 1/20W MF 201 → PM_DSW_PWRGD → IN

DMI, FDI

SYSTEM POWER MANAGEMENT

SUSACK* (IPU) R6 ← PCH_SUSACK_L
SYS_RESET* AM1 ← PM_SYSRST_L
SYS_PWROK AD7 ← PM_PCH_SYS_PWROK
PWROK F10 ← PM_PCH_PWROK
APWROK AB7 ← PM_PCH_PWROK
DRAMPWROK (OD) H3 → PM_MEM_PWRGD → OUT
RSMRST* J2 ← PM_RSMRST_L
SUSWARN*/SUSPWRNACK/GPIO30 J4 ← PCH_SUSWARN_L
PWRBTN* (IPU) K1 ← PM_PWRBTN_L
ACPRESENT/GPIO31 (IPD-DeepSx) E6 ← SMC_ADAPTER_EN
BATLOW*/GPIO72 K7 ← PM_BATLOW_L
RI* N4 ← PCH_RI_L
TP21 AB10 → TP_PCH_SLP_S0_L
SLP_WLAN*/GPIO29 D2 → TP_PCH_SLP_WLAN_L

R1286 0 5% 1/20W MF 0201 ← PM_PCH_PWROK
R1205 10K 5% 1/20W MF 201 ← PP3V3_SUS

DSWVRMEN C8 → PCH_DSWVRMEN
DPWROK L13 ← PM_DSW_PWRGD
WAKE* (IPD-DeepSx) K3 ↔ PCIE_WAKE_L → IN
CLKRUN* AN7 ↔ PM_CLKRUN_L → BI
SUS_STAT*/GPIO61 U7 → LPC_PWRDWN_L → OUT
SUSCLK/GPIO62 (IPU-RSMRST#) Y6 → PM_CLK32K_SUSCLK_R → OUT
SLP_S5*/GPIO63 Y7 → PM_SLP_S5_L → OUT
SLP_S4* C6 → PM_SLP_S4_L → OUT
SLP_S3* H1 → PM_SLP_S3_L → OUT
SLP_A* F3 → TP_PM_SLP_A_L
SLP_SUS* F1 → PM_SLP_SUS_L → OUT
PMSYNCH AY3 → PM_SYNC → OUT
SLP_LAN* G5 → TP_PCH_SLP_LAN_L

OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (5 OF 11)

VGA_BLUE T45 → NC
VGA_GREEN U44 → NC
VGA_RED V45 → NC
VGA_DDC_CLK M43 → NC
VGA_DDC_DATA M45 → NC
VGA_HSYNC N42 → NC
VGA_VSYNC N44 → NC
DAC_IREF U40 ← R1260 10K 5% 1/20W MF 201 ← PP3V3_S0
VGA_IRTN U39 ← R1261 10K 5% 1/20W MF 201 ← PP3V3_S0

VGA DAC Disabled per SB DG v1.0 (Table 12-18).

CRT, DISPLAY

DDPB_CTRLCLK R40 → DP_TBTSNK0_DDC_CLK
DDPB_CTRLDATA (IPD-PLTRST#) R39 → DP_TBTSNK0_DDC_DATA
DDPC_CTRLCLK R35 → DP_TBTSNK1_DDC_CLK
DDPC_CTRLDATA (IPD-PLTRST#) R36 → DP_TBTSNK1_DDC_DATA
DDPD_CTRLCLK N40 → HDMI_DDC_CLK
DDPD_CTRLDATA (IPD-PLTRST#) N38 → HDMI_DDC_DATA
DDPB_AUXN H45 → DP_TBTSNK0_AUXCH_C_N
DDPC_AUXN K43 → DP_TBTSNK1_AUXCH_C_N
DDPD_AUXN J42 → NC_DP_IG_D_AUXCHN
DDPB_AUXP H43 → DP_TBTSNK0_AUXCH_C_P
DDPC_AUXP K45 → DP_TBTSNK1_AUXCH_C_P
DDPD_AUXP J44 → NC_DP_IG_D_AUXCHP
DDPB_HPD K40 → DP_TBTSNK0_HPD
DDPC_HPD K38 → DP_TBTSNK1_HPD
DDPD_HPD H39 → HDMI_HPD

EDP

EDP_BKLTCTL N36 ← EDP_IG_BKL_PWM → OUT
EDP_BKLTEN K36 ← EDP_IG_BKL_ON → OUT
EDP_VDDEN G36 ← EDP_IG_PANEL_PWR → OUT

PCI

PIRQA* H20 ← PCI_INTA_L
PIRQB* L20 ← PCI_INTB_L
PIRQC* K17 ← PCI_INTC_L
PIRQD* M20 ← PCI_INTD_L
GPIO50 A12 ↔ ENET_LOW_PWR_PCH → OUT
GPIO52 B13 ↔ AUD_IPHS_SWITCH_EN_PCH → OUT
GPIO54 C12 ↔ BT_PWRRST_L → OUT
GPIO51 C10 → TP_PCH_STRP_BBS1
GPIO53 A10 → TP_PCH_STRP_ESI_L
GPIO55 AL6 → PCH_STRP_TOPBLK_SWP_L → IN
(IPU-PWROK&PCIRST#)

PIRQE*/GPIO2 G17 → SDCONN_OC_L → IN
PIRQF*/GPIO3 F17 → AUD_IP_PERIPHERAL_DET → IN
PIRQG*/GPIO4 L15 → TBT_PWR_REQ_L → IN
PIRQH*/GPIO5 M15 → AUD_I2C_INT_L → IN
(IPU) PME* AD10 → NC_PCI_PME_L
PLTRST* Y11 → PLT_RESET_L → OUT

R1260 10K 5% 1/20W MF 201 ← PP3V3_S0 → PCI_INTA_L
R1261 10K 5% 1/20W MF 201 ← PP3V3_S0 → PCI_INTB_L
R1262 10K 5% 1/20W MF 201 ← PP3V3_S0 → PCI_INTC_L
R1263 10K 5% 1/20W MF 201 ← PP3V3_S0 → PCI_INTD_L

PP3V3_S5
PP3V3_S0

R1239 3.0K 5% 1/20W MF 201 → PM_PWRBTN_L
R1240 10K 5% 1/20W MF 201 → PM_BATLOW_L
R1291 10K 5% 1/20W MF 201 → PM_CLKRUN_L
R1216 10K 5% 1/20W MF 201 → ENET_LOW_PWR_PCH
R1217 100K 5% 1/20W MF 201 → AUD_IPHS_SWITCH_EN_PCH
R1218 10K 5% 1/20W MF 201 → BT_PWRRST_L
R1230 10K 5% 1/20W MF 201 → SDCONN_OC_L

NO STUFF Redundant to pull-up on audio page

R1214 100K 5% 1/20W MF 201 → AUD_IP_PERIPHERAL_DET
R1231 10K 5% 1/20W MF 201 → TBT_PWR_REQ_L

NO STUFF Redundant to pull-up on audio page

R1233 10K 5% 1/20W MF 201 → AUD_I2C_INT_L
R1225 1K 5% 1/20W MF 201 → PCIE_WAKE_L
R1224 100K 5% 1/20W MF 201 → PM_SLP_S3_L
R1221 100K 5% 1/20W MF 201 → PM_SLP_S4_L
R1222 100K 5% 1/20W MF 201 → PM_SLP_S5_L
R1223 100K 5% 1/20W MF 201 → PM_SLP_SUS_L
R1281 100K 5% 1/20W MF 201 → EDP_IG_BKL_ON
R1284 100K 5% 1/20W MF 201 → EDP_IG_PANEL_PWR

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH DMI/FDI/PM/GFX/PCI

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USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader
(& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
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PCI-E

72 NC_USB3_SPARE_D2RN — AW31 PERN1_USB3RN3
72 NC_USB3_SPARE_D2RP — AY31 PERP1_USB3RP3
72 NC_USB3_SPARE_R2D_CN — BE32 PETN1_USB3TN3
72 NC_USB3_SPARE_R2D_CP — BC32 PETP1_USB3TP3

76 71 68 20 IN USB3_SD_D2R_N — AT31 PERN2_USB3RN4
76 71 68 20 IN USB3_SD_D2R_P — AR31 PERP2_USB3RP4
76 71 68 20 OUT USB3_SD_R2D_C_N — BD33 PETN2_USB3TN4
76 71 68 20 OUT USB3_SD_R2D_C_P — BB33 PETP2_USB3TP4

76 34 IN PCIE_AP_D2R_N — AW33 PERN3
76 34 IN PCIE_AP_D2R_P — AY33 PERP3
76 34 OUT PCIE_AP_R2D_C_N — BE34 PETN3
76 34 OUT PCIE_AP_R2D_C_P — BC34 PETP3

76 37 IN PCIE_CAMERA_D2R_N — AT33 PERN4
76 37 IN PCIE_CAMERA_D2R_P — AR33 PERP4
76 37 OUT PCIE_CAMERA_R2D_C_N — BE36 PETN4
76 37 OUT PCIE_CAMERA_R2D_C_P — BC36 PETP4

76 35 IN PCIE_SSD_D2R_N<0> — AW36 PERN5
76 35 IN PCIE_SSD_D2R_P<0> — AV36 PERP5
76 35 OUT PCIE_SSD_R2D_C_N<0> — BD37 PETN5
76 35 OUT PCIE_SSD_R2D_C_P<0> — BB37 PETP5

76 35 IN PCIE_SSD_D2R_N<1> — AY38 PERN6
76 35 IN PCIE_SSD_D2R_P<1> — AW38 PERP6
76 35 OUT PCIE_SSD_R2D_C_N<1> — BC38 PETN6
76 35 OUT PCIE_SSD_R2D_C_P<1> — BE38 PETP6

76 35 IN PCIE_SSD_D2R_N<2> — AT40 PERN7
76 35 IN PCIE_SSD_D2R_P<2> — AT39 PERP7
76 35 OUT PCIE_SSD_R2D_C_N<2> — BE40 PETN7
76 35 OUT PCIE_SSD_R2D_C_P<2> — BC40 PETP7

76 35 IN PCIE_SSD_D2R_N<3> — AN38 PERN8
76 35 IN PCIE_SSD_D2R_P<3> — AN39 PERP8
76 35 OUT PCIE_SSD_R2D_C_N<3> — BD42 PETN8
76 35 OUT PCIE_SSD_R2D_C_P<3> — BD41 PETP8

69 68 66 64 52 19 17 15 12 11 71 PP1V5_S0
R1300 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP — BD29 PCIE_RCOMP
BE30 PCIE_IREF
NC BC30 TP11
NC BB29 TP6

USB

USB2N0 B37 USB_EXTA_N — 38 75
USB2P0 D37 USB_EXTA_P — 38 75
USB2N1 A38 NC_USB_EXTCN — 72 75
USB2P1 C38 NC_USB_EXTCP — 72 75
USB2N2 A36 NC_USB_SDN — 72 75
USB2P2 C36 NC_USB_SDP — 72 75
USB2N3 A34 NC_USB_WLANN — 72
USB2P3 C34 NC_USB_WLANP — 72
USB2N4 B33 NC_USB_4N — 72
USB2P4 D33 NC_USB_4P — 72
USB2N5 F31 NC_USB_PSOCN — 72
USB2P5 G31 NC_USB_PSOCP — 72
USB2N6 K31 NC_USB_6N — 72 75
USB2P6 L31 NC_USB_6P — 72 75
USB2N7 G29 NC_USB_7N — 72 75
USB2P7 H29 NC_USB_7P — 72 75
USB2N8 A32 USB_EXTB_N — 68 71 75
USB2P8 C32 USB_EXTB_P — 68 71 75
USB2N9 A30 NC_USB_EXTDN — 72 75
USB2P9 C30 NC_USB_EXTDP — 72 75
USB2N10 B29 TP_USB_CAMERAN
USB2P10 D29 TP_USB_CAMERAP
USB2N11 A28 USB_BT_N — 34 75
USB2P11 C28 USB_BT_P — 34 75
USB2N12 G26 NC_USB_IRN — 72 75
USB2P12 F26 NC_USB_IRP — 72 75
USB2N13 F24 USB_TPAD_N — 39 75
USB2P13 G24 USB_TPAD_P — 39 75
(IPD)

USB3RN1 AR26 USB3_EXTA_D2R_N — IN 38 75
USB3RP1 AP26 USB3_EXTA_D2R_P — IN 38 75
USB3TN1 BE24 USB3_EXTA_R2D_C_N — OUT 38 75
USB3TP1 BD23 USB3_EXTA_R2D_C_P — OUT 38 75
USB3RN2 AW26 USB3_EXTB_D2R_N — IN 68 71 75
USB3RP2 AV26 USB3_EXTB_D2R_P — IN 68 71 75
USB3TN2 BD25 USB3_EXTB_R2D_C_N — OUT 68 75
USB3TP2 BC24 USB3_EXTB_R2D_C_P — OUT 68 75
USB3RN5 AW29 NC_USB3_EXTC_D2RN — IN 72 75
USB3RP5 AV29 NC_USB3_EXTC_D2RP — IN 72 75
USB3TN5 BE26 NC_USB3_EXTC_R2D_CN — OUT 72 75
USB3TP5 BC26 NC_USB3_EXTC_R2D_CP — OUT 72 75
USB3RN6 AR29 NC_USB3_EXTD_D2RN — IN 72 75
USB3RP6 AP29 NC_USB3_EXTD_D2RP — IN 72 75
USB3TN6 BD27 NC_USB3_EXTD_R2D_CN — OUT 72 75
USB3TP6 BE28 NC_USB3_EXTD_R2D_CP — OUT 72 75

USBRBIAS* K24
USBRBIAS K26
75 PCH_USB_RBIAS
R1370 22.6 1% 1/20W MF 201 — PLACE_NEAR=U1100.K24:11.4mm

TP24 M33 NC
TP23 L33 NC

OC0*/GPIO59 P3 XDP_DA0_USB_EXTA_OC_L — IN 13 18
OC1*/GPIO40 V1 XDP_DA1_USB_EXTC_OC_L — IN 13 18
OC2*/GPIO41 U2 XDP_DA2_SSD_PWR_EN — OUT 18
OC3*/GPIO42 P1 XDP_DA3_CAMERA_PWR_EN — OUT 18
OC4*/GPIO43 M3 XDP_DB0_USB_EXTB_OC_L — IN 13 18
OC5*/GPIO9 T1 XDP_DB1_USB_EXTD_OC_L — IN 13 18
OC6*/GPIO16 N2 XDP_DB2_SD_PWR_EN — OUT 18
OC7*/GPIO14 M1 XDP_DB3_SDCONN_STATE_CHANGE_L — IN 13 18

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Reserved: SD (HS)

Reserved: WiFi (HS)

Unused

Reserved: PSOC (Legacy Trackpad)

Unused

Unused

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

Reserved: Camera

BT

IR

Trackpad

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
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LPC

76 71 50 41 BI LPC_AD<0> — R1340 33 — LPC_AD_R<0> — A20 LAD0 (IPU)
76 71 50 41 BI LPC_AD<1> — R1341 33 — LPC_AD_R<1> — C20 LAD1 (IPU)
76 71 50 41 BI LPC_AD<2> — R1342 33 — LPC_AD_R<2> — A18 LAD2 (IPU)
76 71 50 41 BI LPC_AD<3> — R1343 33 — LPC_AD_R<3> — C18 LAD3 (IPU)
76 71 50 41 OUT LPC_FRAME_L — R1344 33 — LPC_FRAME_R_L — B21 LFRAME*
(5% 1/20W MF 201)

72 NC_LPC_DREQ0_L — D21 LDRQ0* (IPU)
20 13 OUT TBT_PWR_EN_PCH — G20 LDRQ1*/GPIO23 (IPU-LDRQ1#7)
71 50 41 13 BI LPC_SERIRQ — AL11 SERIRQ

SMBUS

SMBALERT*/GPIO11 N7 PCH_SMBALERT_L — 13
SMBCLK R10 SMBUS_PCH_CLK — OUT 18 22 44 63 68 71 76
SMBDATA U11 SMBUS_PCH_DATA — BI 18 22 44 63 68 71 76
SML0ALERT*/GPIO60 N8 PCH_SML0ALERT_L — 13
SML0CLK U8 SML_PCH_0_CLK — OUT 44 76
SML0DATA R7 SML_PCH_0_DATA — BI 44 76
SML1ALERT*/PCHHOT*/GPIO74 H6 PCH_SML1ALERT_L — 13
SML1CLK/GPIO58 K6 SML_PCH_1_CLK — IN 44 76
SML1DATA/GPIO75 N11 SML_PCH_1_DATA — BI 44 76

C-LINK

(IPU/IPD) CL_CLK AF11 NC_CLINK_CLK — 72
(IPU/IPD) CL_DATA AF10 NC_CLINK_DATA — 72
CL_RST* AF7 NC_CLINK_RESET_L — 72

SPI

76 50 OUT SPI_CLK_R — AJ11 SPI_CLK
76 50 OUT SPI_CS0_R_L — AJ7 SPI_CS0* (IPU)
TP_SPI_CS1_L — AL7 SPI_CS1* (IPU)
TP_SPI_CS2_L — AJ10 SPI_CS2* (IPU)
76 50 BI SPI_MOSI_R — AH1 SPI_MOSI (IPD)
76 50 BI SPI_MISO — AH3 SPI_MISO (IPU)
50 13 BI SPI_IO<2> — AJ4 SPI_IO2 (IPU)
50 13 BI SPI_IO<3> — AJ2 SPI_IO3 (IPU)

TP1 BA45 NC
TP2 BC45 NC
TP4 BE43 NC
TP3 BE44 NC
TD_IREF AY43 PCH_TD_IREF
R1380 0.2K 1% 1/20W MF 201

PP3V3_SUS — 11 12 13 14 15 17 50 64 65 66 69
PP3V3_SUS — 11 12 13 14 15 17 50 64 65 66 69
PP3V3_S3 — 20 21 22 44 46 47 65 68 69 71
PP3V3_S3RS0_CAMERA — 36 47 69
PP3V3_S0 — 66 67 69 71 81 11 12 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55 65

R1350 10K 5% 1/20W MF 201 — LPC_SERIRQ — 13 41 50 71
R1351 10K 5% 1/20W MF 201 — TBT_PWR_EN_PCH — 13 20
R1360 10K 5% 1/20W MF 201 — XDP_DA0_USB_EXTA_OC_L — 13 18
R1361 10K 5% 1/20W MF 201 — XDP_DA1_USB_EXTC_OC_L — 13 18
R1362 10K 5% 1/20W MF 201 — SSD_PWR_EN — 18 65
R1368 10K 5% 1/20W MF 201 — CAMERA_PWR_EN — 18 36
R1320 10K 5% 1/20W MF 201 — XDP_DB0_USB_EXTB_OC_L — 13 18
R1321 10K 5% 1/20W MF 201 — XDP_DB1_USB_EXTD_OC_L — 13 18
R1367 10K 5% 1/20W MF 201 — SD_PWR_EN — 18 68 71
R1369 10K 5% 1/20W MF 201 — XDP_DB3_SDCONN_STATE_CHANGE_L — 13 18
R1392 1K 5% 1/20W MF 201 — SPI_IO<2> — 13 50
R1393 1K 5% 1/20W MF 201 — SPI_IO<3> — 13 50
R1353 10K 5% 1/20W MF 201 — PCH_SMBALERT_L — 13
R1354 10K 5% 1/20W MF 201 — PCH_SML0ALERT_L — 13
R1355 10K 5% 1/20W MF 201 — PCH_SML1ALERT_L — 13

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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
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28 20	IN	TBT_CIO_PLUG_EVENT_L	AT8 BMBUSY*/GPIO0
70 14	IN	FW_PME_L	F13 TACH1/GPIO1
70 14	IN	DPMUX_UC_IRQ	A14 TACH2/GPIO6
41 14	IN	SMC_RUNTIME_SCI_L	G15 TACH3/GPIO7
18	OUT	XDP_FC0_HDD_PWR_EN	Y1 GPIO8 (IPU-RSMRST#)
70 14	OUT	WOL_EN	K13 LAN_PHY_PWR_CTRL/GPIO12
70 14	OUT	MEM_VDD_SEL_1V5_L	AB11 GPIO15
18 14	IN	XDP_DD0_SSD_PCIE_SEL_L	AN2 SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)
71 50 14	BI	LPCPLUS_GPIO	C14 TACH0/GPIO17
20 14	OUT	JTAG_TBT_TMS_PCH	BB4 SCLOCK/GPIO22
70 14	BI	TBT_GO2SX_BIDIR	Y10 GPIO24
41 14	IN	SMC_WAKE_SCI_L	R11 GPIO27 (IPU-DeepSx)
21	OUT	ISOLATE_CPU_MEM_L	AD11 GPIO28
20	OUT	TBT_POC_RESET_L	AN6 GPIO34
18	OUT	XDP_FC1_GPU_GOOD	AP1 GPIO35/NMI*
18 14	OUT	XDP_DC2_ODD_PWR_EN_L	AT3 SATA2GP/GPIO36 (IPD-PLTRST#)
18	OUT	XDP_DC3_JTAG_ISP_TCK	AK1 SATA3GP/GPIO37 (IPD-PLTRST#)
20 14	IN	JTAG_ISP_TDO	AT7 SLOAD/GPIO38
20 14	OUT	JTAG_ISP_TDI	AM3 SDATAOUT0/GPIO39
70 14	OUT	FW_PWR_EN_PCH	AN4 SDATAOUT1/GPIO48
		XDP_DD1_MLB_RAMCFG1	AK3 SATA5GP/GPIO49 (IPU-BOOT/SATA5GP?)
71 50 14	BI	SPIROM_USE_MLB	U12 GPIO57
20		MLB_RAMCFG3	C16 TACH4/GPIO68
20		MLB_RAMCFG2	D13 TACH5/GPIO69
20	IN	SD_SEL_PCIE_L_USB_H	G13 TACH6/GPIO70 (IPU-BOOT?)
20		MLB_RAMCFG0	H15 TACH7/GPIO71 (IPU-BOOT?)

CPU/MISC

TP14	AN10	PCH_A20GATE	14
(IPD) PECI	AY1	PCH_PECI	
RCIN*	AT6	PCH_RCIN_L	14 76
PROCPWRGD	AV3	PCH_PROCPWRGD	
THRMTRIP*	AV1	PM_THRMTRIP_L_R	15 42
PLTRST_PROC*	AU4	CPU_RESET_L	OUT 6
VSS	N10		

GPIO

BE41	
BE5	
C45	VSS
A5	

VSS

A2	
A41	
A43	
A44	
B1	
B2	
B44	
B45	
BA1	
BC1	
BD1	
BD2	
BD44	
BD45	
BE2	
BE3	
D1	
E1	
E45	
A4	

PP1V05_S0
15 17 18 42 62 66 69 71

NO STUFF
R1457 1K 5% 1/16W MF-LF 402

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI BI 6 42 74
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD OUT 6 18 74
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L IN 6 42 74

PP3V3_S0
33 29 20 19 81 71 69 67 66 65 55 52 51 49 48 47 46 45 44 35

RAMCFG0:H R1475 10K 5% 1/20W MF 201
RAMCFG1:H R1474 10K 5% 1/20W MF 201
RAMCFG2:H R1473 10K 5% 1/20W MF 201
RAMCFG3:H R1472 10K 5% 1/20W MF 201

20 18 IN

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	FW_PME_L	14 70
R1411	20K	DPMUX_UC_IRQ	14 70
R1496	10K	SMC_RUNTIME_SCI_L	14 41
R1494	10K	WOL_EN	14 70
R1489	10K	MEM_VDD_SEL_1V5_L	14 70
R1495	100K	XDP_DD0_SSD_PCIE_SEL_L	14 18
R1490	100K	LPCPLUS_GPIO	14 50 71
R1412	10K	JTAG_TBT_TMS_PCH	14 20
R1492	10K	TBT_GO2SX_BIDIR	14 70
R1491	10K	SMC_WAKE_SCI_L	14 41
R1498	10K	XDP_DC2_ODD_PWR_EN_L	14 18
R1413	10K	JTAG_ISP_TCK	18 20
R1486	10K	JTAG_ISP_TDO	14 20
R1499	10K	JTAG_ISP_TDI	14 20
R1484	10K	FW_PWR_EN_PCH	14 70
R1493	100K	SPIROM_USE_MLB	14 50 71

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	PCH_A20GATE	14
R1455	10K	PCH_RCIN_L	14 76

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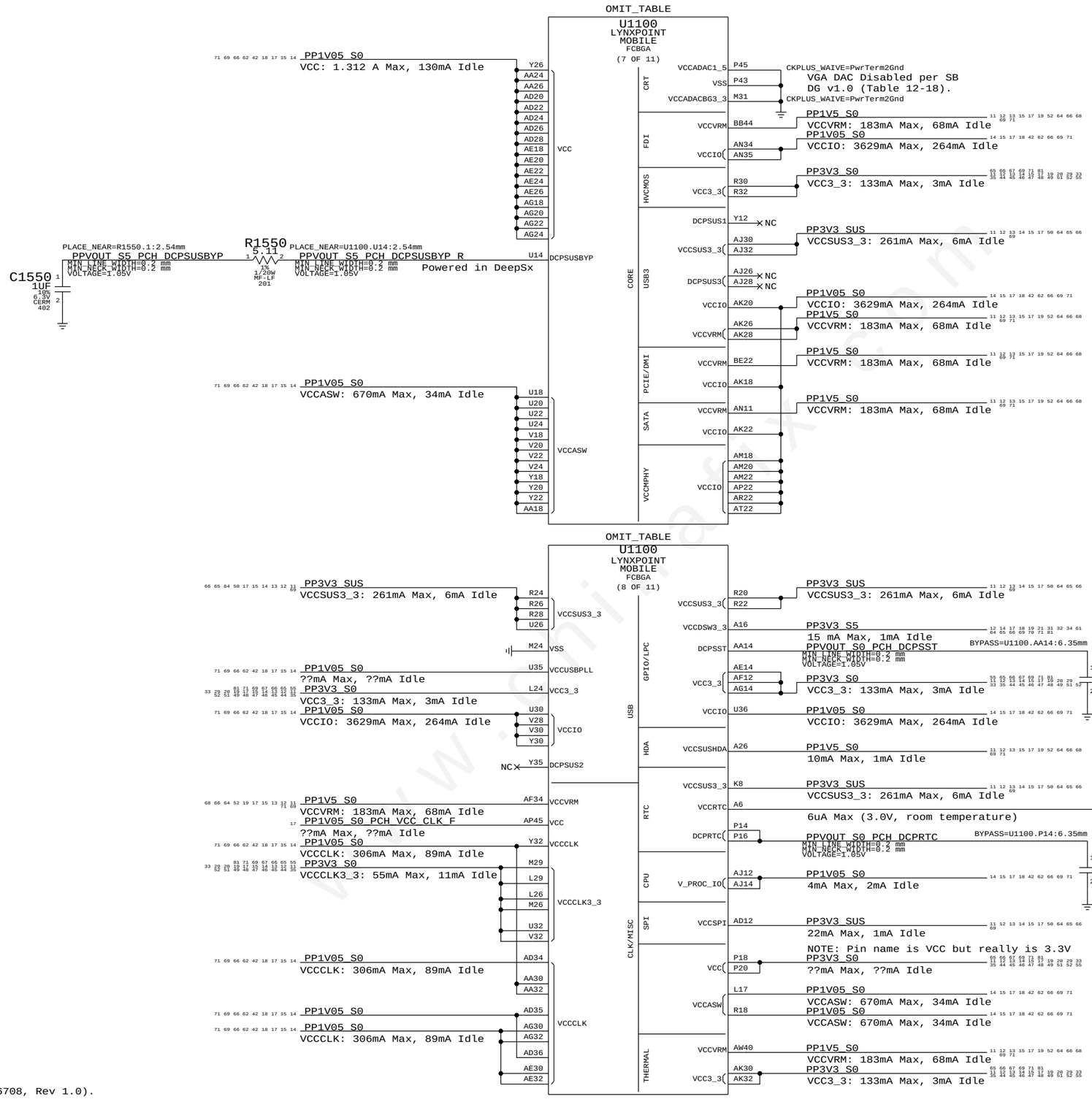

Current data from LPT EDS (doc #486708, Rev 1.0).

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PCH Power

Apple Inc.

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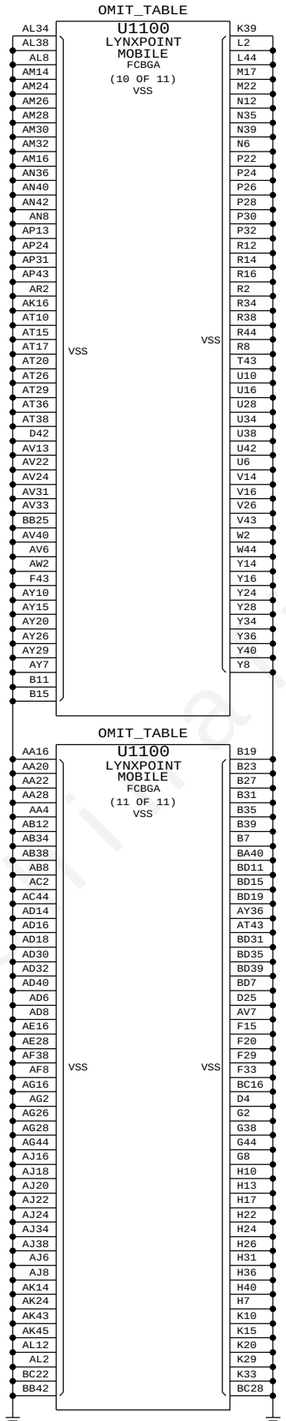

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PAGE TITLE

PCH Grounds

Apple Inc.

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AG22:6.35mm
BYPASS=U1100.AP20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AK18:6.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AK20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30:6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34:12.7mm

PP1V05_S0
??mA Max, ??mA Idle
R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT TABLE
L1790 4.7UH-170MA-0.321OHM 0603
PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402 → CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>

XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

XDP C1804 0.1UF 10% 6.3V CERM-X5R 0201
XDP R1831 1K 5% 1/16W MF-LF 402
XDP C1800 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1801 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1806 0.1UF 10% 6.3V CERM-X5R 0201

PP1V05_S0 → XDP_CPU_TDO R1820 51 5% 1/20W MF 201 PLACE_NEAR=U0500.M49:28mm
XDP_CPU_TCK R1823 51 5% 1/20W MF 201 PLACE_NEAR=U0500.N54:28mm
XDP_CPUPCH_TRST R1824 51 5% 1/20W MF 201 PLACE_NEAR=U0500.M53:28mm

TDI and TMS are terminated in CPU.

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.F50:2.54mm → XDP_CPU_VCCST_PWRGD
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:2.54mm → XDP_CPU_PWRBTN_L
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402 → XDP_SYS_PWROK
XDP_CPU_TCK

R1805 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.A67:2.54mm → XDP_PLT_RESET_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 → XDP_CPU_TDO
CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 → XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 → XDP_CPU_TDI
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 → XDP_CPU_TMS

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, A, Y, GND, NC, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

XDP_PCH_TDO	R1860 51 5% 1/20W MF 201	PLACE_NEAR=U1100.AD3:28mm
XDP_PCH_TDI	R1861 51 5% 1/20W MF 201	PLACE_NEAR=U1100.AE2:28mm
XDP_PCH_TMS	R1862 51 5% 1/20W MF 201	PLACE_NEAR=U1100.AD1:28mm
XDP_PCH_TCK	R1866 51 5% 1/20W MF 201	PLACE_NEAR=U1100.AB3:28mm

PCH/XDP Signals

				Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890	SHORT		USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT		SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT		CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT		USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT		SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT		SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT		DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN		MAKE_BASE=TRUE		XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L		MAKE_BASE=TRUE		XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT		JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT		SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1		MAKE_BASE=TRUE		XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L		MAKE_BASE=TRUE		XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879	SHORT		AP_CLKREQ_L

OMIT (All 10 R's)

NONE NONE NONE 201

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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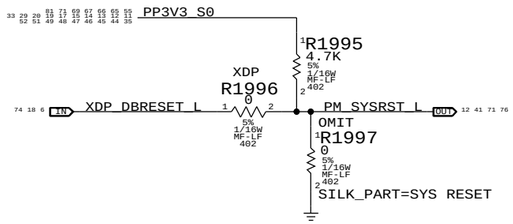
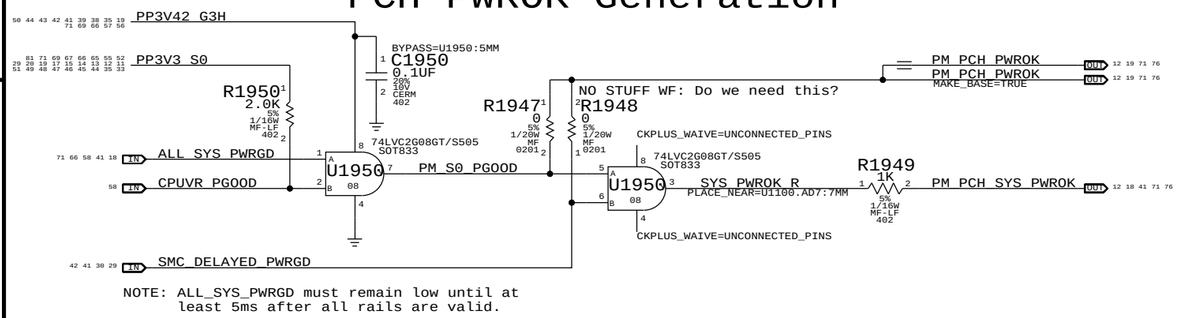
PCH Reset Button

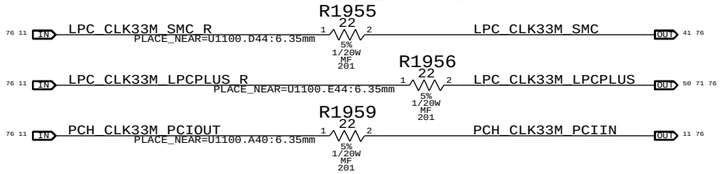


PCH PWROK Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

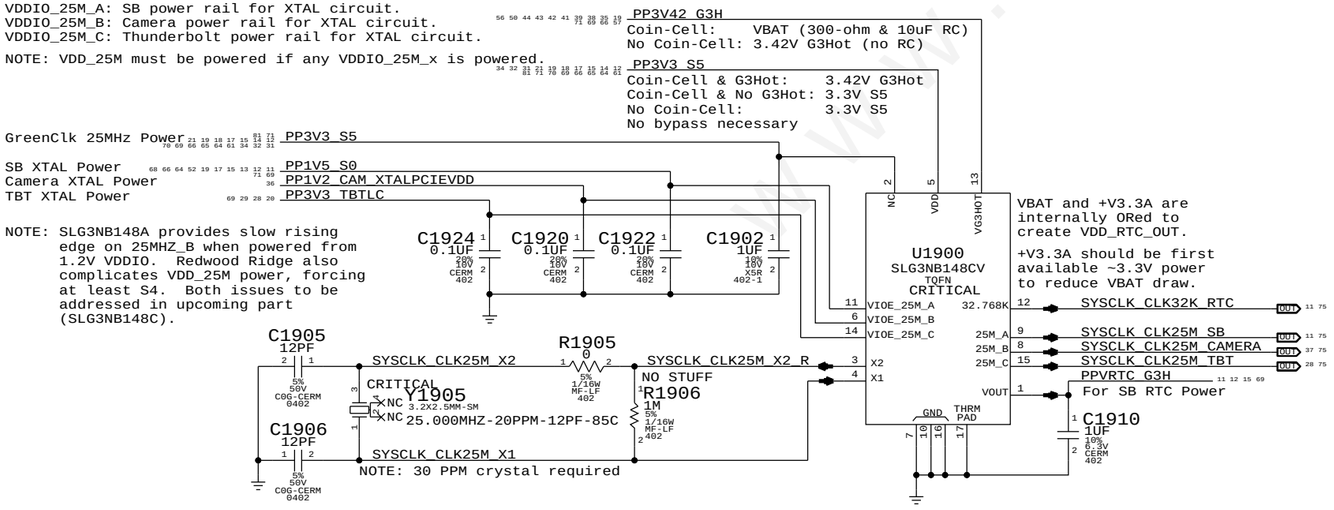
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

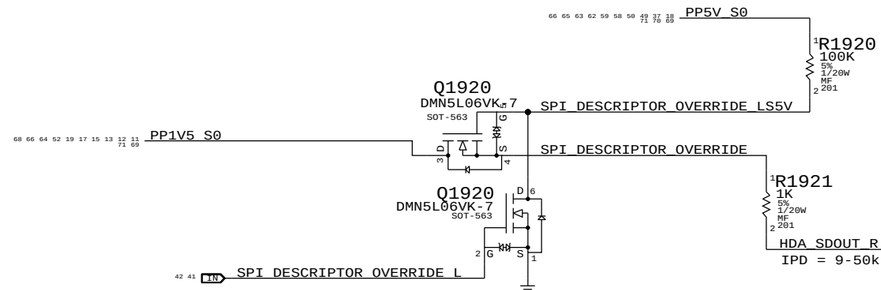
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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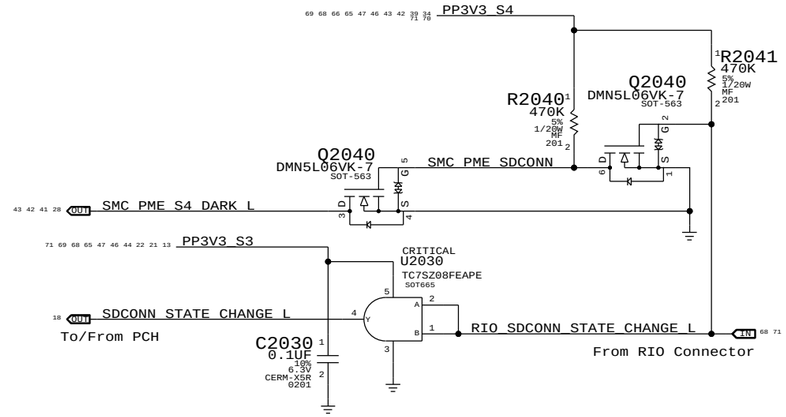
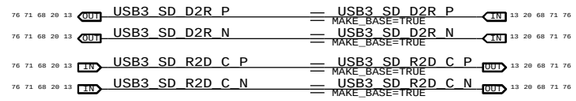
RIO SD Card Reader Support



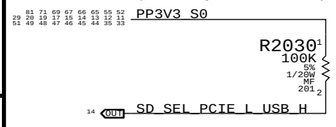
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



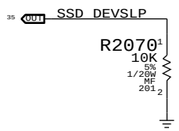
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



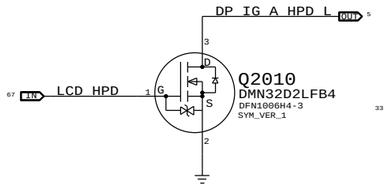
GS3 Connector Support

DEVSLP not supported on LPT-H

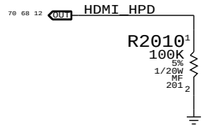


LCD HPD Inverter

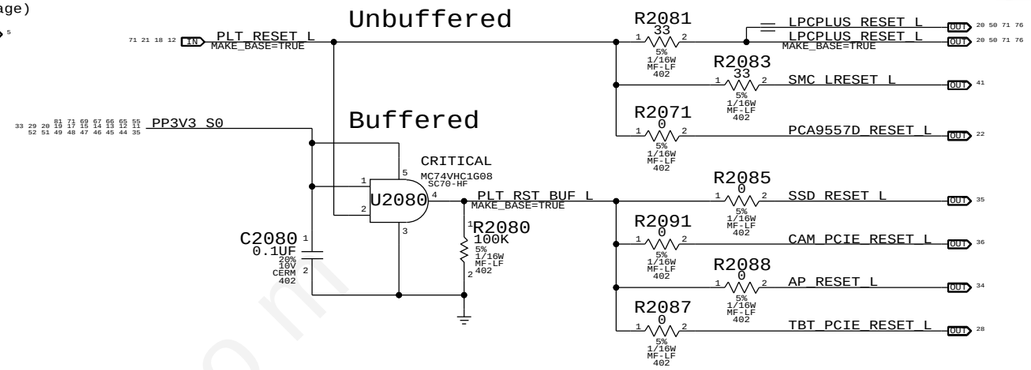
(Pull-Up on CPU Page)



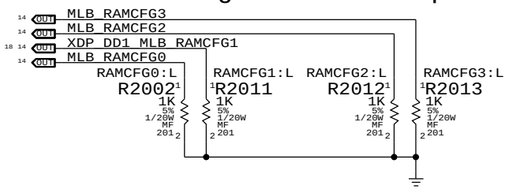
HDMI HPD pull-down



Platform Reset Connections

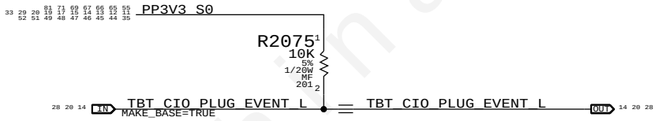


RAM Configuration Straps



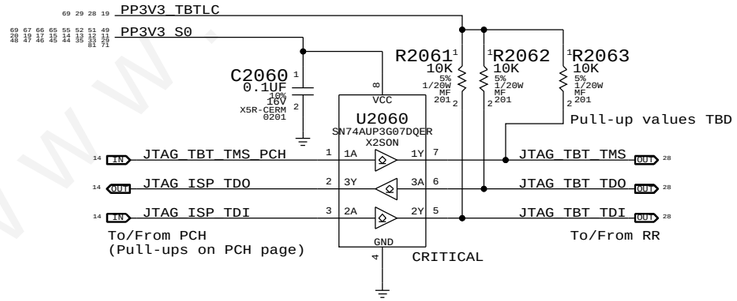
Redwood Ridge Support

RR output is open-drain, no isolation necessary

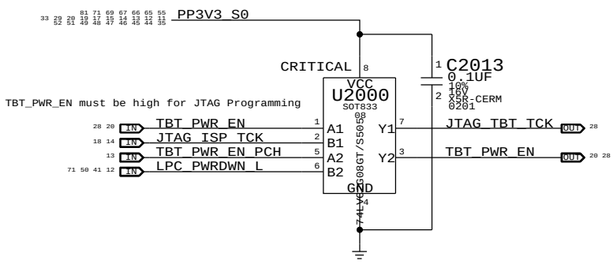


Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



GPIO Glitch Prevention



SYNC_MASTER=J15_REFERENCE SYNC_DATE=01/14/2013

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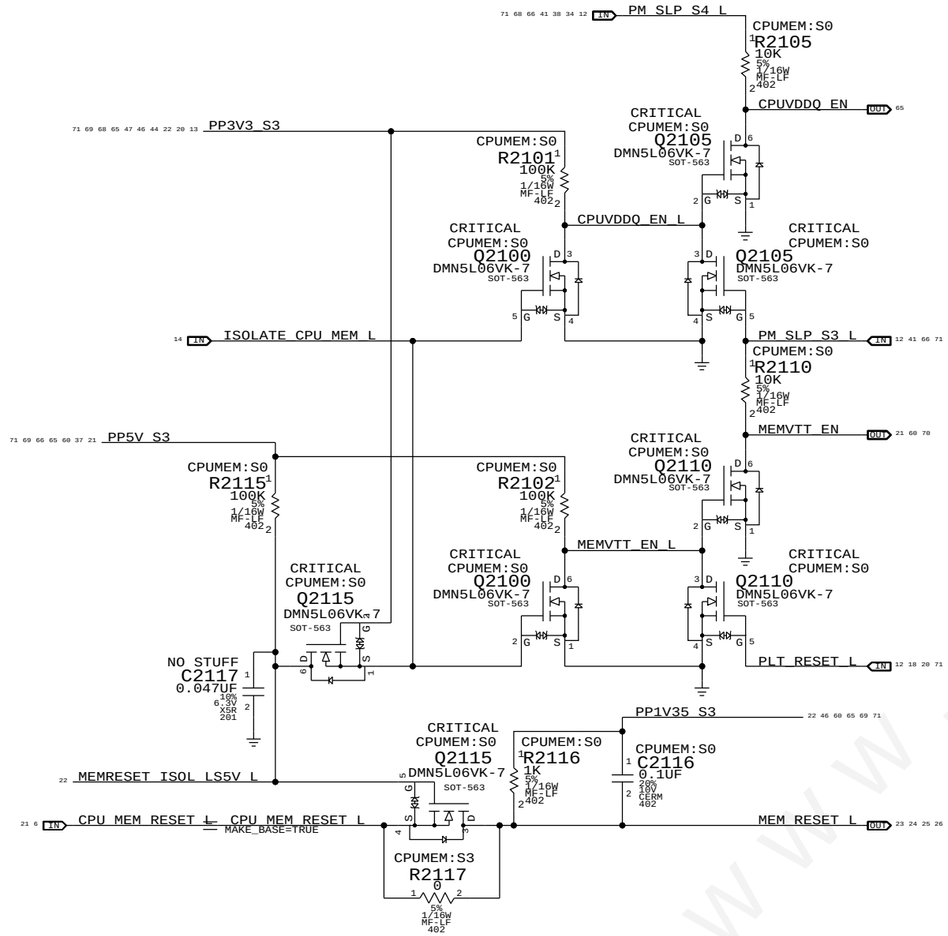
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



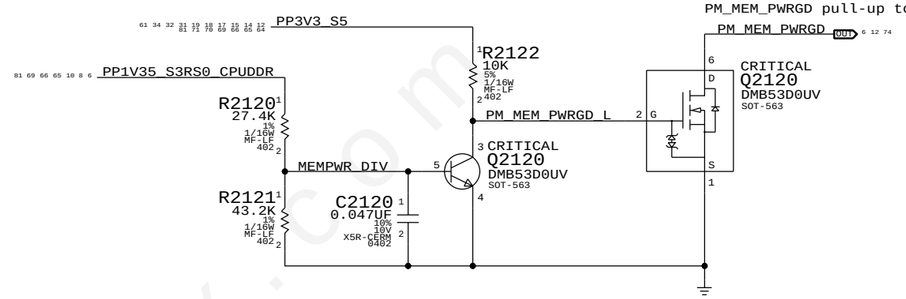
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

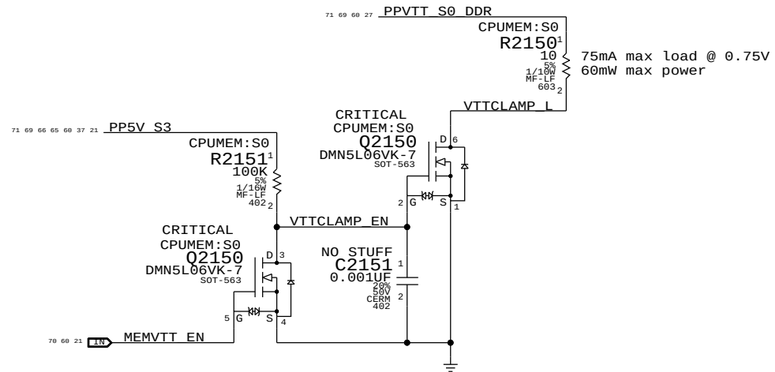
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



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DRAWING NUMBER: <SCH_NUM> SIZE: D
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

21 IN MEMRESET_ISOL_LS5V_L
74 7 IN CPU_DIMMA_VREFDQ
74 7 IN CPU_DIMMB_VREFDQ
7 IN CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches

DDRVREF_DAC R2225 100K 5% 1/10W MF-LF 402 — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2245 100K 5% 1/10W MF-LF 402 — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2265 100K 5% 1/10W MF-LF 402 — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2285 100K 5% 1/10W MF-LF 402 — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC R2208 100K 5% 1/20W MF 201

CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V35_S3

PLACE_NEAR=C2220.1:2mm — R2223 2 5% 1/20W MF 201 — PLACE_NEAR=C2223.2:1mm
PLACE_NEAR=C2220.6:2mm — C2220 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_A_RC
PLACE_NEAR=C2221.2:1mm — R2221 1K 1% 1/16W MF-LF 402 — PP0V75_S3_MEM_VREFDQ_A (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
PLACE_NEAR=C2222.2:1mm — R2222 1K 1% 1/16W MF-LF 402
R2220 24.9 1% 1/20W MF 201

PLACE_NEAR=C2240.1:2mm — R2243 2 5% 1/20W MF 201 — PLACE_NEAR=C2243.2:1mm
PLACE_NEAR=Q2260.6:2mm — C2240 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_B_RC
PLACE_NEAR=C2241.2:1mm — R2241 1K 1% 1/16W MF-LF 402 — PP0V75_S3_MEM_VREFDQ_B (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
PLACE_NEAR=C2242.2:1mm — R2242 1K 1% 1/16W MF-LF 402
R2240 24.9 1% 1/20W MF 201

PLACE_NEAR=C2260.1:2mm — R2263 2 5% 1/20W MF 201 — PLACE_NEAR=C2263.2:1mm
PLACE_NEAR=Q2220.3:2mm — C2260 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_A_RC
PLACE_NEAR=C2261.2:1mm — R2261 1K 1% 1/16W MF-LF 402 — PP0V75_S3_MEM_VREFCA_A (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
PLACE_NEAR=C2262.2:1mm — R2262 1K 1% 1/16W MF-LF 402
R2260 24.9 1% 1/20W MF 201

PLACE_NEAR=C2280.1:2mm — R2283 2 5% 1/20W MF 201 — PLACE_NEAR=C2283.2:1mm
PLACE_NEAR=Q2260.3:2mm — C2280 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_B_RC
PLACE_NEAR=C2281.2:1mm — R2281 1K 1% 1/16W MF-LF 402 — PP0V75_S3_MEM_VREFCA_B (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
PLACE_NEAR=C2282.2:1mm — R2282 1K 1% 1/16W MF-LF 402
R2280 24.9 1% 1/20W MF 201

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

47 46 44 22 20 18 13 71 68 60 PP3V3_S3 — OMIT R2218 SHORT NONE NONE NONE NONE 402

PP3V3_S3_VREFMRGN (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574 (VDD 8, GND 3)
44 22 18 13 76 71 68 63 IN SMBUS_PCH_CLK — SCL 6
44 22 18 13 76 71 68 63 BI SMBUS_PCH_DATA — SDA 7
Addr=0x98(WR)/0x99(RD) — A0 9, A1 10
VOUTA 1 — VREFMRGN_DQ_A
VOUTB 2 — VREFMRGN_DQ_B
VOUTC 4 — VREFMRGN_CA_AB
VOUTD 5 — VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2201 QFN PCA9557 (VCC 16)
Addr=0x30(WR)/0x31(RD) — A0 3, A1 4, A2 5
76 71 68 63 44 22 18 13 IN SMBUS_PCH_CLK — SCL 1
76 71 68 63 44 22 18 13 BI SMBUS_PCH_DATA — SDA 2
(OD) P0 6 NC
P1 7 — VREFMRGN_DQ_A_EN
P2 9 — VREFMRGN_DQ_B_EN
P3 10 — VREFMRGN_CA_A_EN
P4 11 — VREFMRGN_CA_B_EN
P5 12 — VREFMRGN_MEMVREG_EN
P6 13 — VREFMRGN_FRAMEBUF_EN
P7 14 NC
RESET* 15
THRM PAD 17, GND 8

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

20 IN PCA9557D_RESET_L

PP3V3_S3 — DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201 — CRITICAL DDRVREF_DAC

U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF — DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402 — DDRREG_FB OUT 60

DDRVREF_DAC R2213 100K 5% 1/20W MF 201 — CRITICAL DDRVREF_DAC

U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF — DDRVREF_DAC R2217 1M 5% 1/16W MF-LF 402

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

MEM VREG

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA		
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

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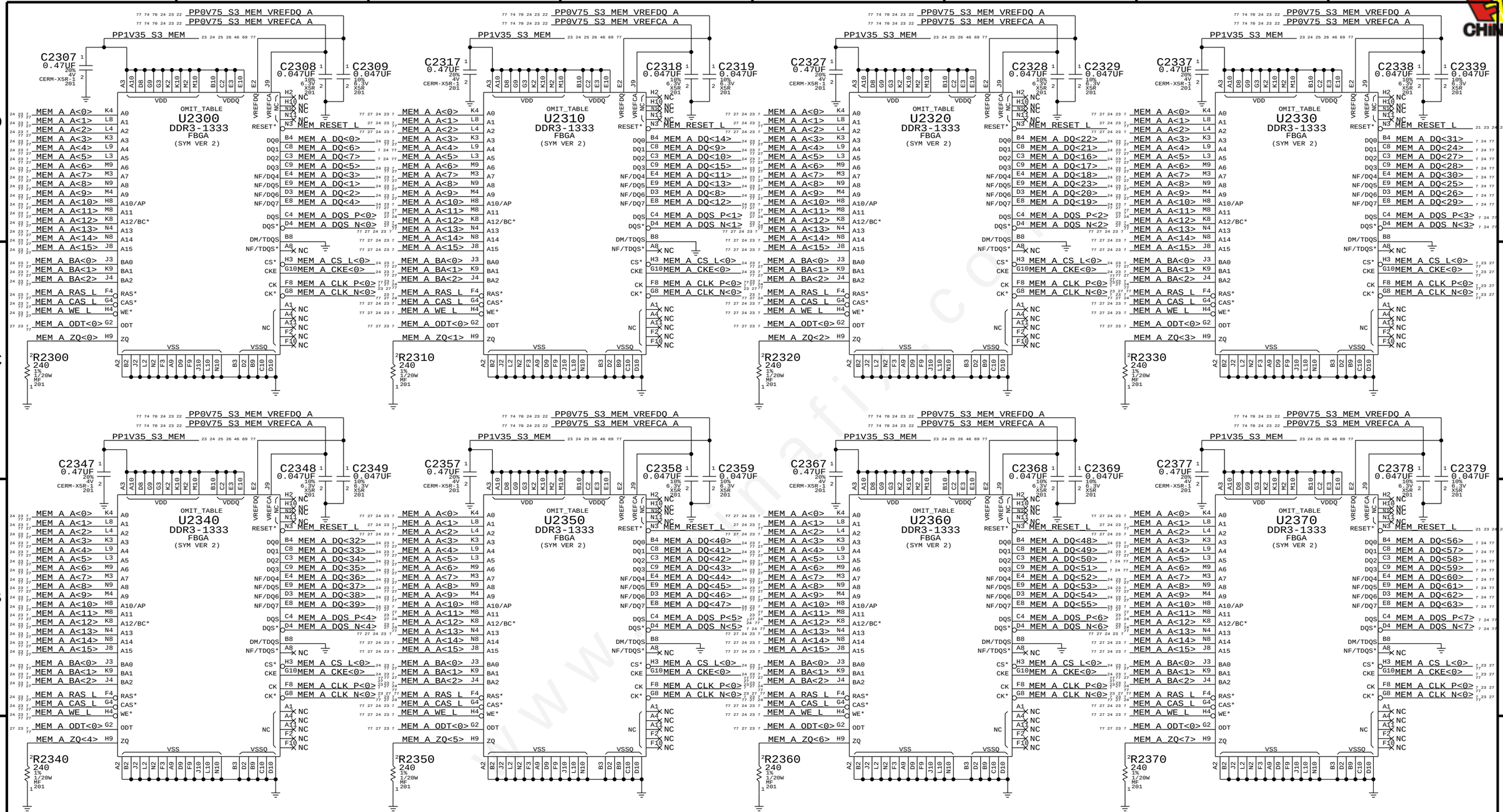
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C2309 0.047UF
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SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
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C2301 2.2UF
C2310 2.2UF
C2311 2.2UF
C2320 2.2UF
C2321 2.2UF
C2330 2.2UF
C2331 2.2UF
C2303 0.1UF
C2304 0.1UF
C2305 0.1UF
C2313 0.1UF
C2314 0.1UF
C2315 0.1UF
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C2373 0.1UF
C2374 0.1UF
C2375 0.1UF
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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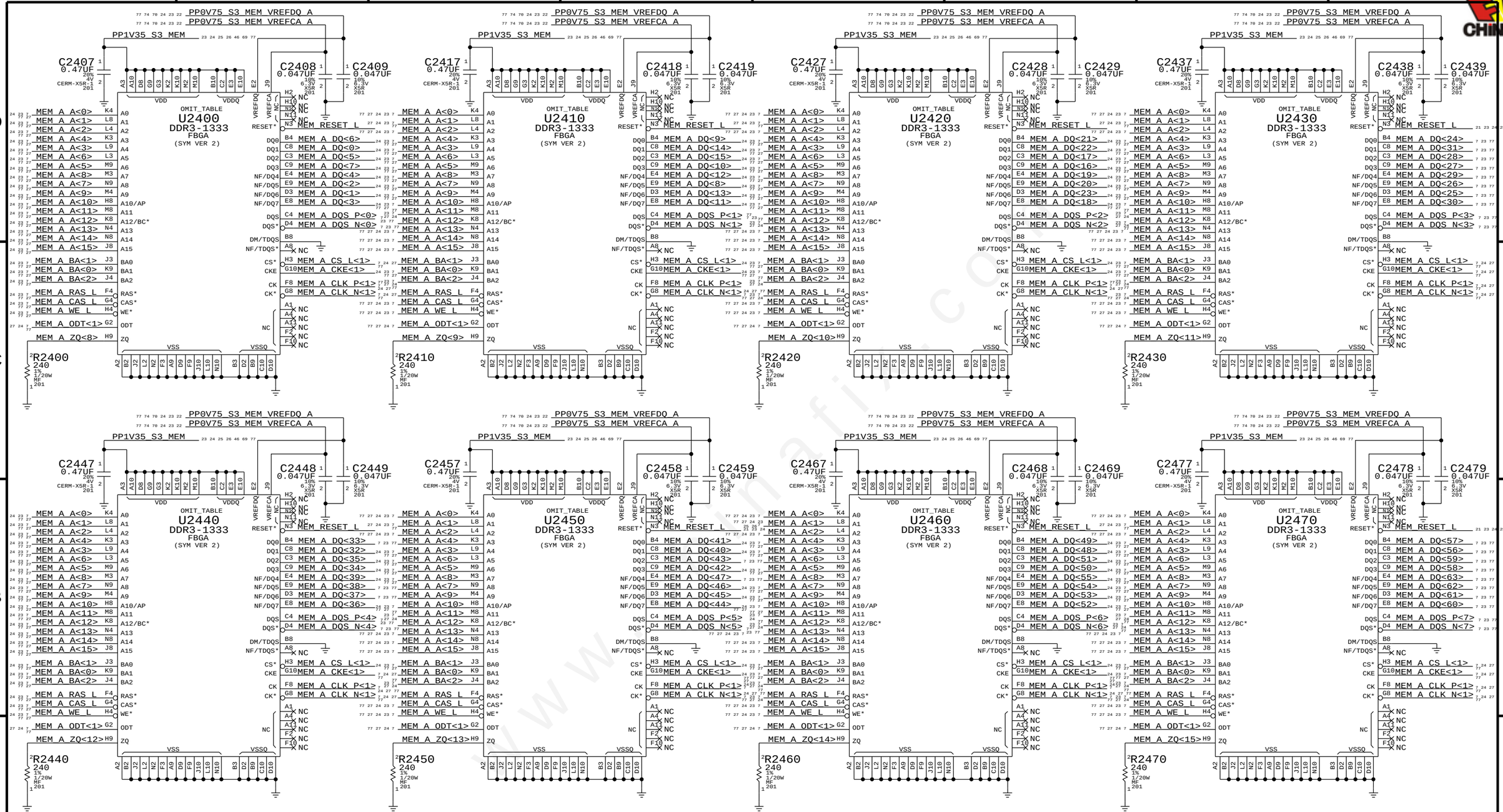

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
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Apple Inc.

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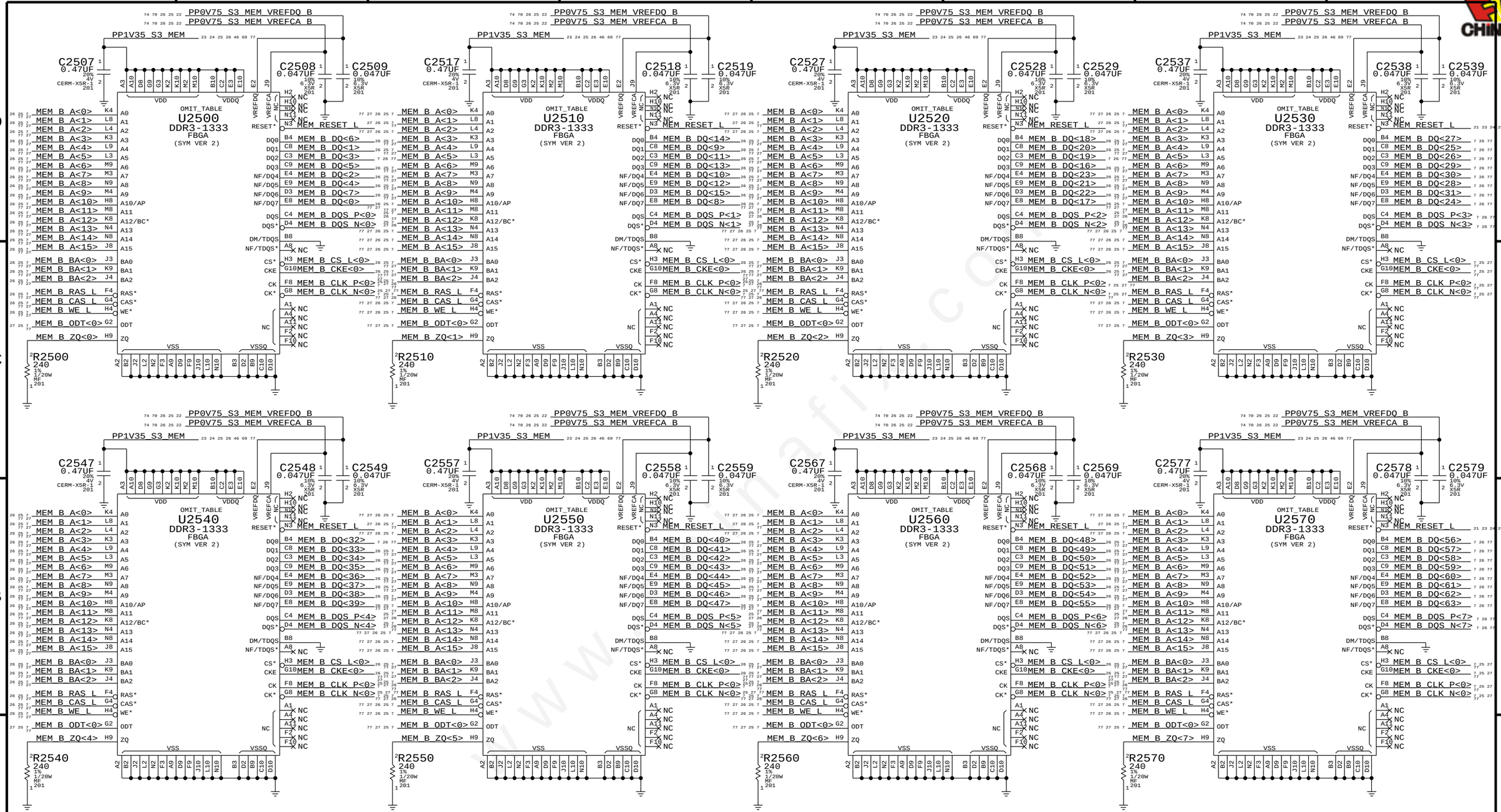

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PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

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PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

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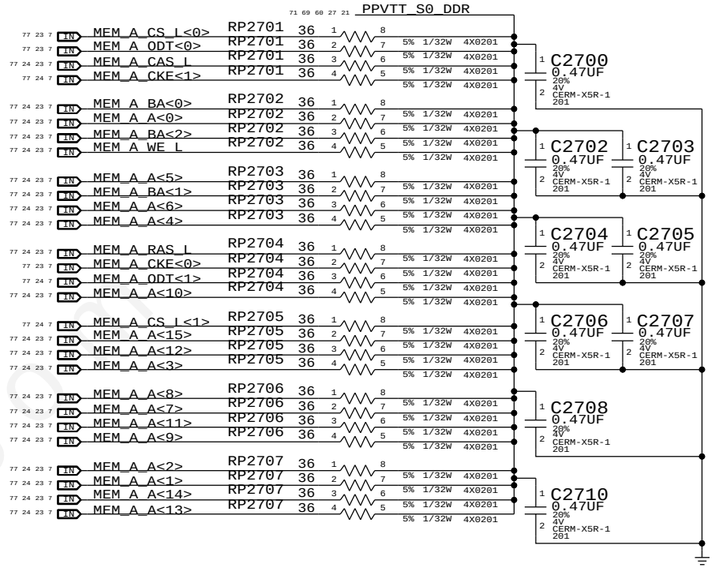
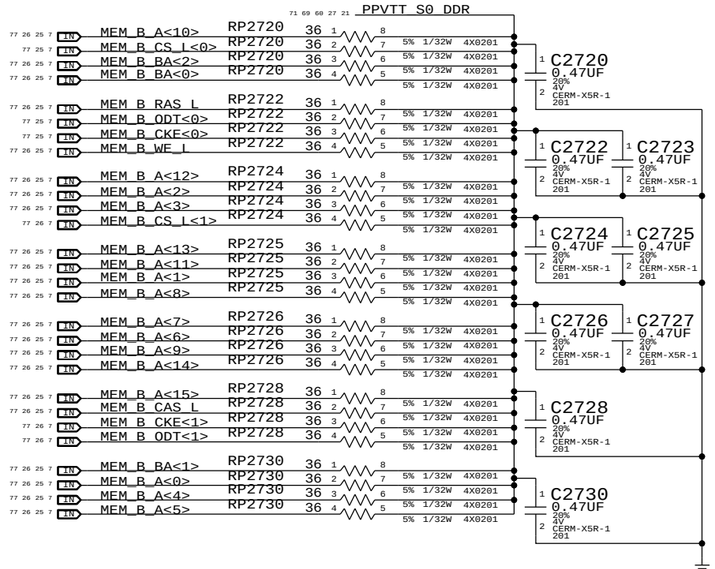
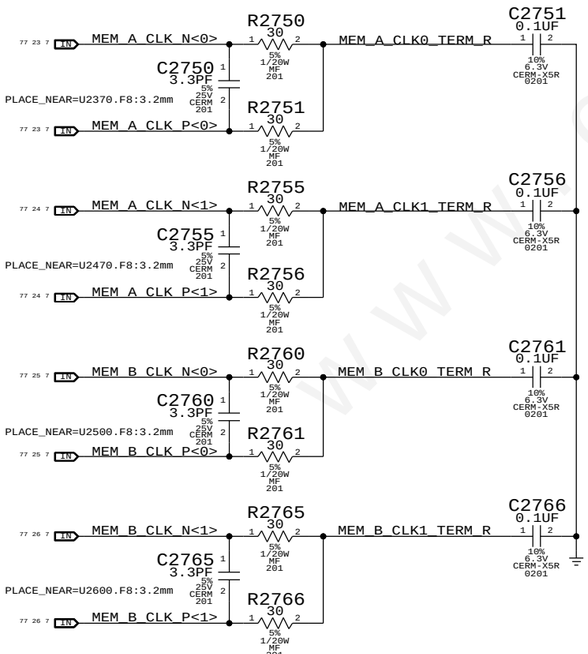
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DDR3 Termination

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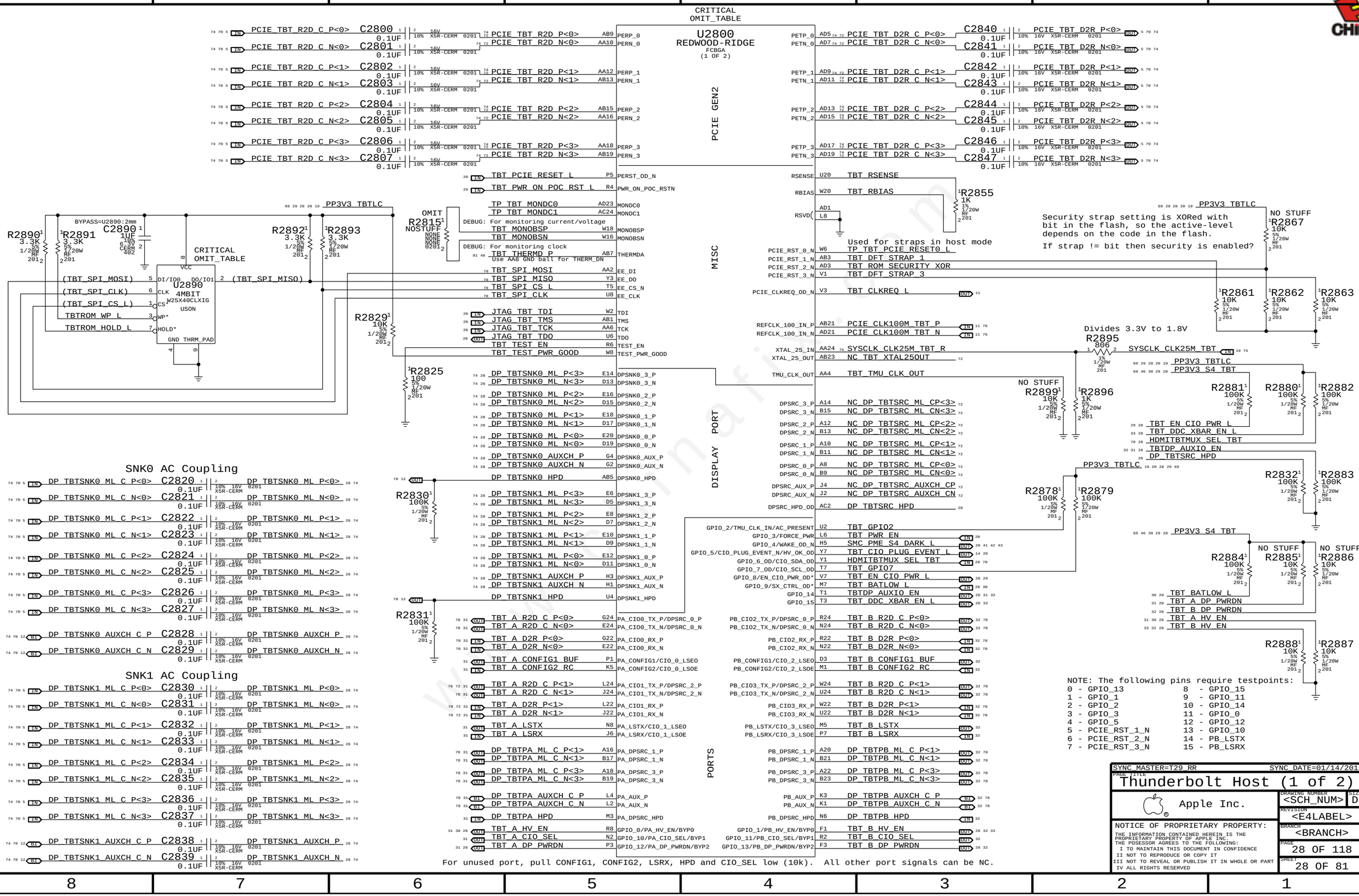
CRITICAL
OMIT_TABLE
U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TBT_RSENSE
TBT_RBIAS
TBT_GPIO2
TBT_PWR_EN
SMC_PME_S4_DARK_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
TBT_BATLOW_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
PP3V3_TBTLC
PP3V3_S4_TBT
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
Used for straps in host mode
Divides 3.3V to 1.8V
SYSCLK_CLK25M_TBT_R
SYSCLK_CLK25M_TBT
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
NC_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
TBT_TBTLC
TBT_S4_TBT
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
NO STUFF
OMIT
SNK0 AC Coupling
SNK1 AC Coupling
BYPASS=U2890:2mm
CRITICAL
OMIT_TABLE
U2890
4MBIT
W25X40CLXIG
USON
TBTROM_WP_L
TBTROM_HOLD_L
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
TBT_THERMD_P
TBT_TEST_EN
TBT_TEST_PWR_GOOD
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TP_TBT_MONDC0
TP_TBT_MONDC1
TBT_MONOBSP
TBT_MONOBSN
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
TBT_A_HPD
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
TBT_B_LSTX
TBT_B_LSRX
TBT_B_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
PAGE TITLE
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Apple Inc.
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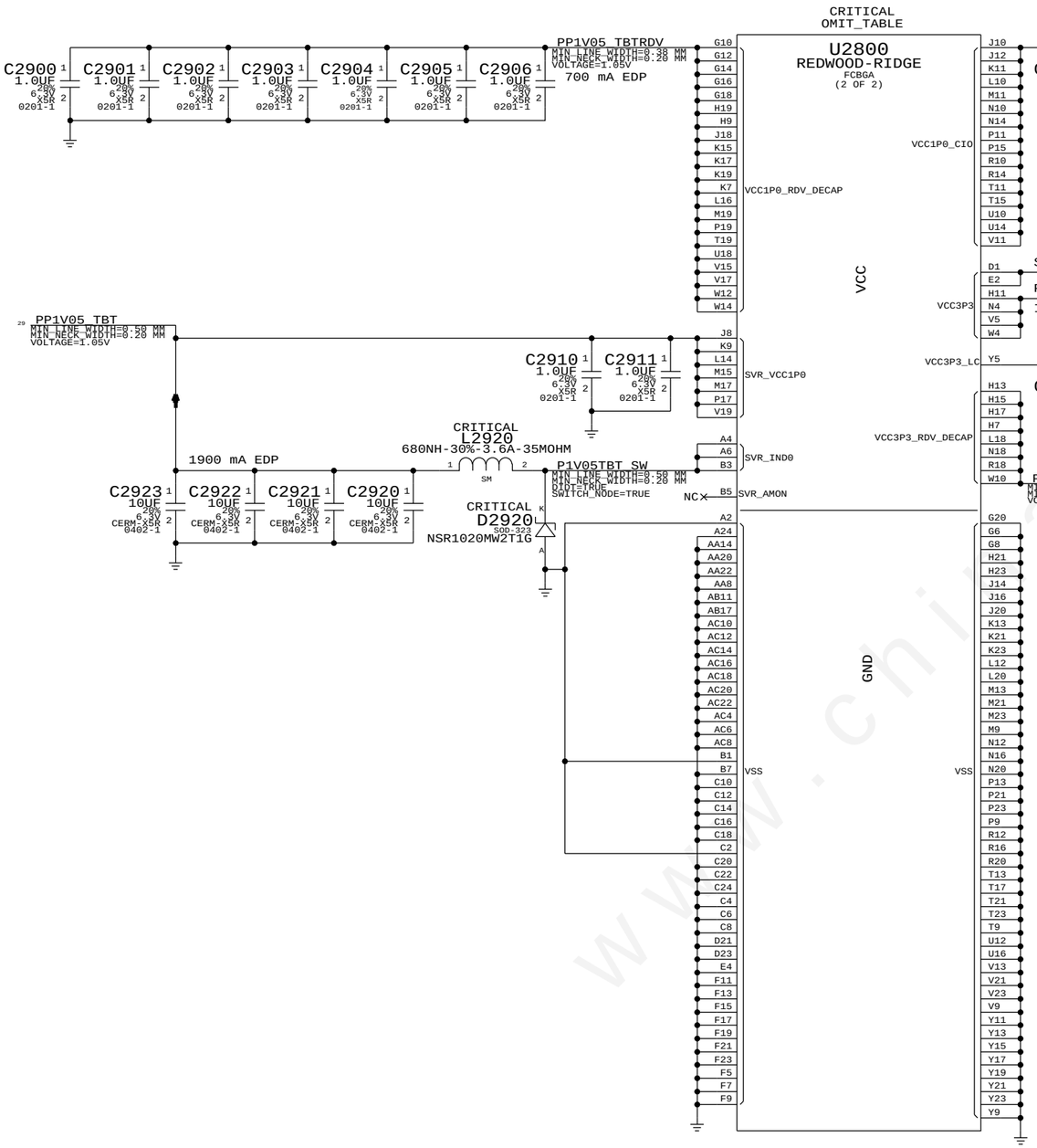
CRITICAL
OMIT_TABLE
U2800
REDWOOD-RIDGE
FCBGA
(2 OF 2)
VCC
GND
VSS
PP1V05_TBTRDV
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.05V
700 mA EDP
C2900 C2901 C2902 C2903 C2904 C2905 C2906
1.0UF 20% 6.3V X5R 0201-1
VCC1P0_RDV_DECAP
PP1V05_TBT
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.05V
C2910 C2911
1.0UF 20% 6.3V X5R 0201-1
SVR_VCC1P0
1900 mA EDP
CRITICAL
L2920
680NH-30%-3.6A-35MOHM
SM
C2923 C2922 C2921 C2920
10UF 20% 6.3V CERM-X5R 0402-1
P1V05TBT_SW
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
DIG_TRACE
SWITCH_NODE=TRUE
SVR_IND0
NC
SVR_AMON
CRITICAL
D2920
SOD-323
NSR1020MW2T1G
VCC1P0_CIO
C2930 C2931 C2932
1.0UF 20% 6.3V X5R 0201-1
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
1200 mA EDP
SVR input to RR - 1100 mA EDP
POC input to RR - 150 mA EDP
Isolated to reduce noise from SVR
VCC3P3
VCC3P3_LC
VCC3P3_RDV_DECAP
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=3.3V
100 mA EDP
C2970
1.0UF 20% 6.3V X5R 0201-1
PP3V3_TBTRDV
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
25 mA EDP
C2980 C2981
1.0UF 20% 6.3V X5R 0201-1
U2940
TPS22920
CSP
VOUT
VIN
ON
GND
CRITICAL
PP1V05_TBT
PP3V3_TBTLC
R2945
100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
C2940
1.0UF 20% 6.3V X5R 0201-1
Q2945
DMN5L06VK-7
SOT-563
PP3V3_S0
TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
Pull-up (S0) on PCH page
C2950 C2951 C2952 C2953
10UF 20% 6.3V CERM-X5R 0402-1
PP3V3_S4_TBT
3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A
PLACE_NEAR=C2953.1:1mm
XW2960
SM
C2960 C2961
1.0UF 20% 6.3V X5R 0201-1
PP3V3_S4_TBT_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TBT "POC" Power-up Reset
SMC_DELAYED_PWRGD
PP3V3_S0
TBT_POC_RESET_L
Q2995
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
R2995
100K 5% 1/20W MF 201
R2990
100K 5% 1/20W MF 201
R2992
100K 5% 1/20W MF 201
C2995
330PF 10% 16V X7R-CERM 0201
R2991
24.9K 1% 1/20W MF 201
U2990
TPS3895ADRY
USON
ENABLE
SENSE
SENSE_OUT
CT
GND
TBTPOCRST_MR_L
TBTPOCRST_SENSE
TBTPOCRST_CT
Push-pull output
TBT_PWR_ON_POC_RST_L
C2990
0.1UF 10% 16V X5R 402
C2991
0.001UF 10% 50V X7R-CERM 0402
Vth = 2.508V nominal
Delay = 4.04ms nominal
U2950
Part | TPS22920
Type | Load Switch
R(on) @ 1.05V | 8 mOhm Typ 11.5 mOhm Max
Max Current = 4A (85C)
1.05V TBT "CIO" Switch
Internal switch not functional on RR.
EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
PAGE TITLE
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Apple Inc.
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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/10W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/10W MF-LF 402
TBTBST_PWREN_L

Q3005 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
TBT_A_HV_EN
Second FET needed for dual-port designs.

CRITICAL
Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

R3091 200K 1% 1/10W MF-LF 402 <R1>
R3092 73.2K 1% 1/10W MF-LF 402 <R2>

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V C0G-CERM 0402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3093 49.9K 1% 1/10W MF-LF 402
R3094 26.7K 1% 1/10W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095 3.3UH-6.5A PIMB063T-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC

SGND shorted to GND inside package, no XW necessary.

TBTBST_SNS1
R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
TBTBST_SNS2
XW3095 SM
PLACE_NEAR=C3095.1:2 mm
TBTBST_VSNS
R3095 137K 1% 1/10W MF-LF 402 <Ra>
C3088 10PF 5% 50V C0G-CERM 0402
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/10W MF-LF 402 <Rb>
TBTBST_FBX

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

PP15V_TBT
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3096 10UF 10% 25V X5R 1206-2
NO STUFF
C3097 10UF 10% 25V X5R 805
C3099 0.001UF 10% 50V X7R-CERM 0402

Vout = 1.6V * (1 + Ra / Rb)

Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
R3088 330K 5% 1/10W MF-LF 402
TBTBST_SHDN_DIV
R3087 330K 5% 1/10W MF-LF 402
Q3088 DMN5L06VK-7 SOT-563
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

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Thunderbolt Mobile Support

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

PP3V3_S5

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM; C3280 22UF 20% 6.3V X5R-CERM 0603; C3281 0.1UF 10% 16V X5R-CERM 0201

PP15V_TBT 15.75V Max

C3215 4.7UF 10% 25V X5R-CERM 0603; C3210 0.1UF 10% 16V X5R 402

CRITICAL U3210 CD3211A0RGPR QFN

Pin	Name
19, 20	V3P3
18	V3P3OUT
6, 7	VHV
12	OUT
14	FAULTZ
16	ENHVU
5	EN
11	HV_EN
17	S0
8	ISET_V3P3
10	ISET_S0
9	ISET_S3
1, 2, 3, 13, 15	GND
21	THRM PAD

C3285 0.1UF 10% 16V X5R-CERM 0201; C3286 10UF 20% 6.3V CERM-X5R 0402; C3211 0.1UF 10% 25V X5R 402

PP3V3_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)

PP3V3RHV_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)

S4_PWR_EN (66 65 32 IN)

TBT_A_HV_EN (30 28 IN)

PM_SLP_S3_R_L (66 45 32 IN)

TBTAPWRSW_ISET_V3P3

TBTAPWRSW_ISET_S0

TBTAPWRSW_ISET_S3

TBTHV:P15V R3210 22.6K 1% 1/20W MF 201 — 12V: See below

TBTHV:P15V R3211 22.6K 1% 1/20W MF 201

R3212 36.5K 1% 1/20W MF 201 <RV3P3>

TBTAPWRSW_ISET_S3_R

TBTAPWRSW_ISET_S0_R

TBTHV:P15V R3213 22.6K 1% 1/20W MF 201 <RHVS3>

TBTHV:P15V R3214 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603

PP3V3RHV_S4_TBTAPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)

C3200 0.01UF 10% 16V X7R-CERM 0402

C3201 0.01UF 10% 16V X7R-CERM 0402

TBTACONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)

R3201 12 5% 1/20W MF 201

TBT Dir DP Dir

TBT: RX_0

GND_VOID=TRUE (Both C's)

TBT_A_D2R_P<0> (78 28 OUT) — C3274 0.47UF 20% 4V 201 CERM-X5R-1 — TBT_A_D2R_C_P<0> (78)

TBT_A_D2R_N<0> (78 28 OUT) — C3275 0.47UF 20% 4V 201 CERM-X5R-1 — TBT_A_D2R_C_N<0> (78)

GND_VOID=TRUE R3294 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE

GND_VOID=TRUE R3295 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE

DP_TBTPA_ML_C_P<3> (78 28 IN) — C3278 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<3> (78)

DP_TBTPA_ML_C_N<3> (78 28 IN) — C3279 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_N<3> (78)

R3279 470K 5% 1/20W MF 201; R3278 470K 5% 1/20W MF 201

TBT: Unused

TBT_A_D2R1_AUXDDC_P (78 31)

TBT_A_D2R1_AUXDDC_N (78 31)

TBT: RX_1

TBT_A_HPD (31)

TBT_A_CONFIG1_RC (31)

TBT_A_CONFIG2_RC (28 OUT)

R3252 1M 5% 1/20W MF 201; R3251 1M 5% 1/20W MF 201; C3294 330PF 10% 16V X7R-CERM 0201; C3295 330PF 10% 16V X7R-CERM 0201; R3241 100K 5% 1/20W MF 201

C3202 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL J3200 MDP-J44 F-RT-TH SHIELD PINS S16 S15 S14 S13 S12 S24 S22 S21 S20 S19 S18 S17 PORT B

Pin	Name	Pin	Name
B2	HPD	B1	GND0
B4	CONFIG1	B3	ML_LANE0P
B6	CONFIG2	B5	ML_LANE0N
B8	GND2	B7	GND1
B10	ML_LANE3P	B9	ML_LANE1P
B12	ML_LANE3N	B11	ML_LANE1N
B14	GND4	B13	GND3
B16	AUX_CHP	B15	ML_LANE2P
B18	AUX_CHN	B17	ML_LANE2N
B20	DP_PWR	B19	RETURN

514-0876

TBTACONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) — DP Dir TBT Dir — TBT: TX_0

GND_VOID=TRUE C3205 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)

TBTACONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)

GND_VOID=TRUE C3206 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)

TBT_A_R2D_P<0> (78) — TBT_A_R2D_N<0> (78)

TBT: TX_1

TBT_A_R2D_P<1> (78) — TBT_A_R2D_N<1> (78)

GND_VOID=TRUE (Both C's)

C3270 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<0> (IN 28 78)

C3271 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_N<0> (IN 28 78)

GND_VOID=TRUE R3270 470K 5% 1/20W MF 201

GND_VOID=TRUE R3271 470K 5% 1/20W MF 201

DP_A_LSX_ML_P<1> (31 78)

DP_A_LSX_ML_N<1> (31 78)

TBT: LSX_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)

C3272 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_P<1> (IN 28 72 78)

C3273 0.22UF 20% 6.3V X5R 0201 — TBT_A_R2D_C_N<1> (IN 28 78)

GND_VOID=TRUE R3272 470K 5% 1/20W MF 201

GND_VOID=TRUE R3273 470K 5% 1/20W MF 201

470K R's for ESD protection on AC-coupled signals.

PP3V3_S4_TBTAPWR (31)

C3220 0.1UF 10% 16V X5R-CERM 0201

SIGNAL_MODEL=TBT_MUX

CRITICAL U3220 CBTL05024 HVQFN24-COMBO

Pin	Name	Pin	Name
7	TB-	15	TB_ENA
8	TB+	24	AUXIO_EN
1	AUX-	6	DP_PD
2	AUX+	23	(IPU) AUXIO-
4	DDC_DAT	22	(IPD) AUXIO+
5	DDC_CLK	16	CA_DETOUT
11	DP+	18	CA_DET
10	DP-	19	DPML0+
14	LSTX (IPU)	20	DPML0-
13	LSRX (IPD)	12	HPDOUT
17	HPD	GND	THMPAD

TBT_A_D2R_C_N<1> (78) — TBT_A_D2R_C_P<1> (78)

DP_TBTPA_AUXCH_C_N (78 28 BI) — DP_TBTPA_AUXCH_C_P (78 28 BI)

C3230 0.1UF 10% 16V X5R-CERM 0201

C3231 0.1UF 10% 16V X5R-CERM 0201

DP_TBTPA_DDC_DATA (33 BI)

DP_TBTPA_DDC_CLK (33 IN)

TBT_A_CONFIG1_BUF (28 OUT)

DP_TBTPA_ML_C_P<1> (78 28 IN) — C3232 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_P<1> (78)

DP_TBTPA_ML_C_N<1> (78 28 IN) — C3233 0.22UF 20% 6.3V X5R 0201 — DP_TBTPA_ML_N<1> (78)

TBT_A_LSTX (28 IN)

TBT_A_LSRX (28 OUT)

DP_TBTPA_HPD (28 OUT)

TBT_A_CIO_SEL (IN 28)

TBTDP_AUXIO_EN (IN 28 32)

TBT_A_DP_PWRDN (IN 28)

TBT_A_D2R1_AUXDDC_N (31 78)

TBT_A_D2R1_AUXDDC_P (22 31 78)

TBT: RX_1

TBT_A_CONFIG1_RC (31)

TBT_A_HPD (17 31)

DPML0+ 19 — DP_A_LSX_ML_P<1> (31 78)

DPML0- 20 — DP_A_LSX_ML_N<1> (31 78)

TBT: LSX_A_R2P/P2R (P/N)

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

PP3V3_S5

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL
C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM 603
C3381 0.1UF 10% 16V X5R-CERM 0201

PP15V_TBT
15.75V Max

C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 16V X5R 402

CRITICAL
U3310
CD3211A0RGPR
QFN

V3P3OUT
VHV
ENHVU
EN
HV_EN
S0
ISET_V3P3
ISET_S0
ISET_S3
FAULTZ
GND
THRM PAD

C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V 402

PP3V3_S4_TBTBPWR
PP3V3RHV_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L

TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3

TBTHV:P15V
12V: See below
R3310 22.6K 1% 1/20W MF 201
R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>

TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R

TBTHV:P15V
R3313 22.6K 1% 1/20W MF 201 <RHVS3>
R3314 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.

<RHVS0> ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

CRITICAL
L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C3300 0.01UF 10% 50V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

R3301 12 5% 1/20W MF 201

TBT Dir DP Dir

TBT: RX_0

GND_VOID=TRUE (Both C's)

TBT_B_D2R_P<0> TBT_B_D2R_N<0>
C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
TBT_B_D2R_C_P<0> TBT_B_D2R_C_N<0>

GND_VOID=TRUE
R3394 1K 5% 1/20W MF 201
R3395 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE

DP_TBTPB_ML_C_P<3> DP_TBTPB_ML_C_N<3>
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_P<3> DP_TBTPB_ML_N<3>

R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201

TBT: Unused

TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N

TBT: RX_1

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC

R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201

C3302 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL
J3200
MDP-J44 F-RT-TH
SHIELD PINS
PORT A
514-0876

HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN

TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3305 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3306 0.01UF 10% 25V X5R-CERM 0201

DP Dir TBT Dir

TBT_B_R2D_P<0> TBT_B_R2D_N<0>

TBT: TX_0

TBT_B_R2D_P<1> TBT_B_R2D_N<1>

TBT: TX_1

GND_VOID=TRUE (Both C's)

C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0> TBT_B_R2D_C_N<0>

R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201

DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)

C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<1> TBT_B_R2D_C_N<1>

R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

PP3V3_S4_TBTBPWR

C3320 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
U3320
CBTL05024
HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
VDD
GND_THMPAD

TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX (IPU)
LSRX (IPD)
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
(IPU)AUXIO-
(IPD)AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD

TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD

TBT_B_CIO_SEL
TBTDP_AUXIO_EN
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P

TBT: RX_1

TBT_B_CONFIG1_RC
TBT_B_HPD

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

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REVISION: <E4LABEL>
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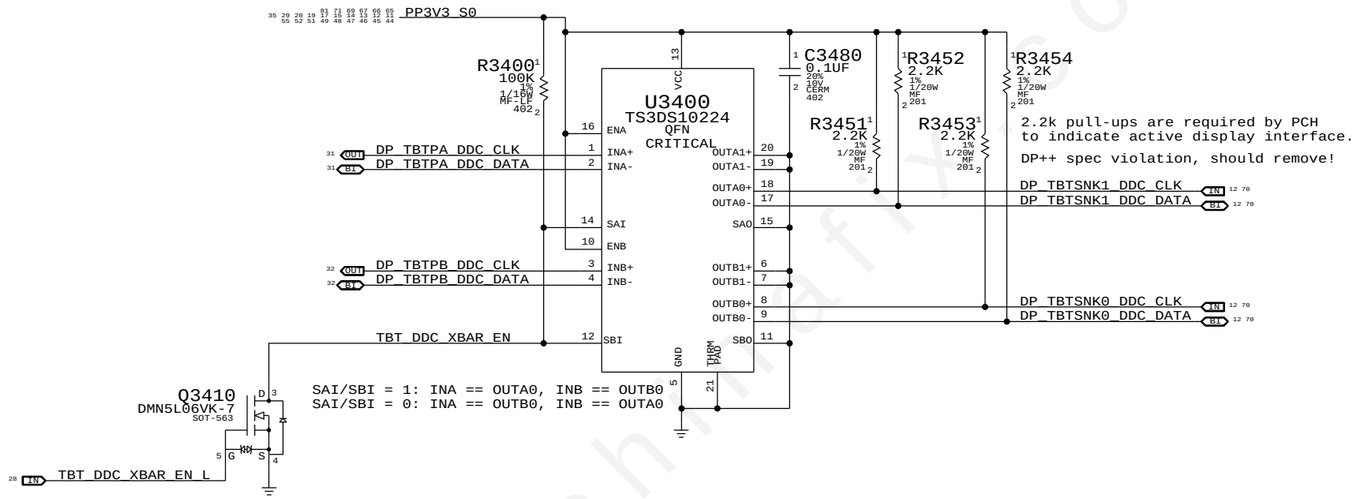
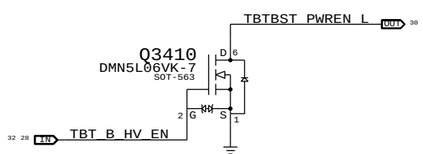
DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



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PAGE TITLE	DDC Crossbar
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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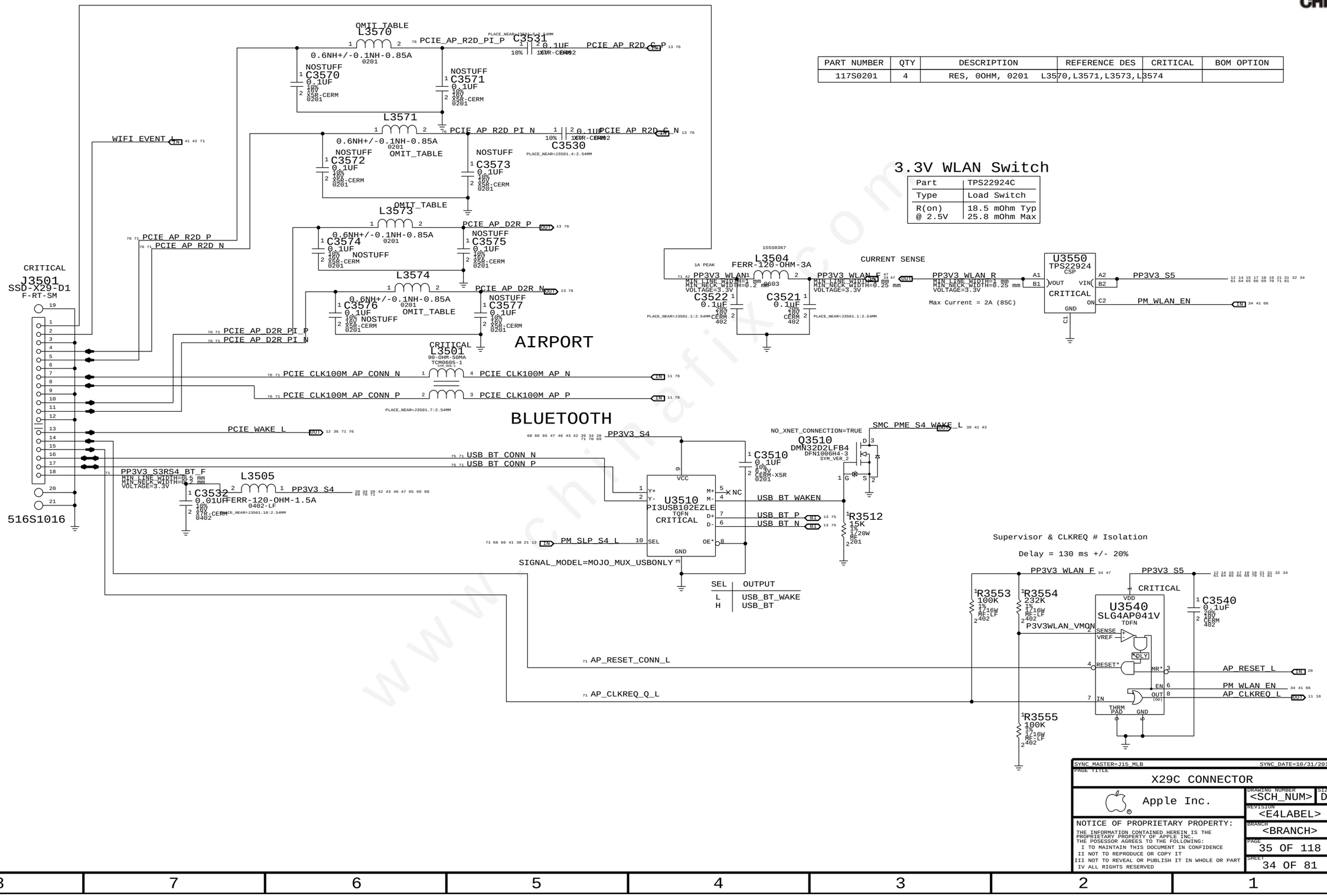
OMIT_TABLE
L3570
PCIE_AP_R2D_PI_P
C3531
0.1UF
PCIE_AP_R2D_C_P
0.6NH+/-0.1NH-0.85A
0201
NOSTUFF
C3570
0.1UF
C3571
L3571
PCIE_AP_R2D_PI_N
PCIE_AP_R2D_C_N
C3530
WIFI_EVENT_L
C3572
C3573
OMIT_TABLE
L3573
PCIE_AP_D2R_P
PCIE_AP_R2D_P
PCIE_AP_R2D_N
C3574
C3575
L3574
PCIE_AP_D2R_N
C3576
C3577
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
AIRPORT
CRITICAL
J3501
SSD-X29-D1
F-RT-SM
516S1016
L3501
90-OHM-50MA
TCM0605-1
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_P
BLUETOOTH
PCIE_WAKE_L
PP3V3_S4
USB_BT_CONN_N
USB_BT_CONN_P
PP3V3_S3RS4_BT_F
L3505
FERR-120-OHM-1.5A
0402-LF
C3532
0.01UF
U3510
PI3USB102EZLE
TQFN
CRITICAL
VCC
GND
NC
USB_BT_WAKEN
USB_BT_P
USB_BT_N
PM_SLP_S4_L
SEL
OE*
SIGNAL_MODEL=MOJO_MUX_USBONLY
C3510
0.1UF
NO_XNET_CONNECTION=TRUE
Q3510
DMN32D2LFB4
SMC_PME_S4_WAKE_L
R3512
15K
SEL | OUTPUT
L | USB_BT_WAKE
H | USB_BT
PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION
117S0201 | 4 | RES, 0OHM, 0201 | L3570,L3571,L3573,L3574
3.3V WLAN Switch
Part | TPS22924C
Type | Load Switch
R(on) @ 2.5V | 18.5 mOhm Typ 25.8 mOhm Max
CURRENT SENSE
L3504
FERR-120-OHM-3A
PP3V3_WLAN
PP3V3_WLAN_F
PP3V3_WLAN_R
C3522
C3521
Max Current = 2A (85C)
U3550
TPS22924
CSP
VOUT
VIN
ON
GND
PP3V3_S5
PM_WLAN_EN
Supervisor & CLKREQ # Isolation
Delay = 130 ms +/- 20%
R3553
100K
R3554
232K
P3V3WLAN_VMON
U3540
SLG4AP041V
TDFN
SENSE
VREF
DLY
RESET*
MR*
EN
OUT
IN
THRM PAD
GND
C3540
0.1uF
R3555
100K
AP_RESET_CONN_L
AP_CLKREQ_Q_L
AP_RESET_L
PM_WLAN_EN
AP_CLKREQ_L
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SYNC_DATE=10/31/2012
PAGE TITLE
X29C CONNECTOR
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
BRANCH
<BRANCH>
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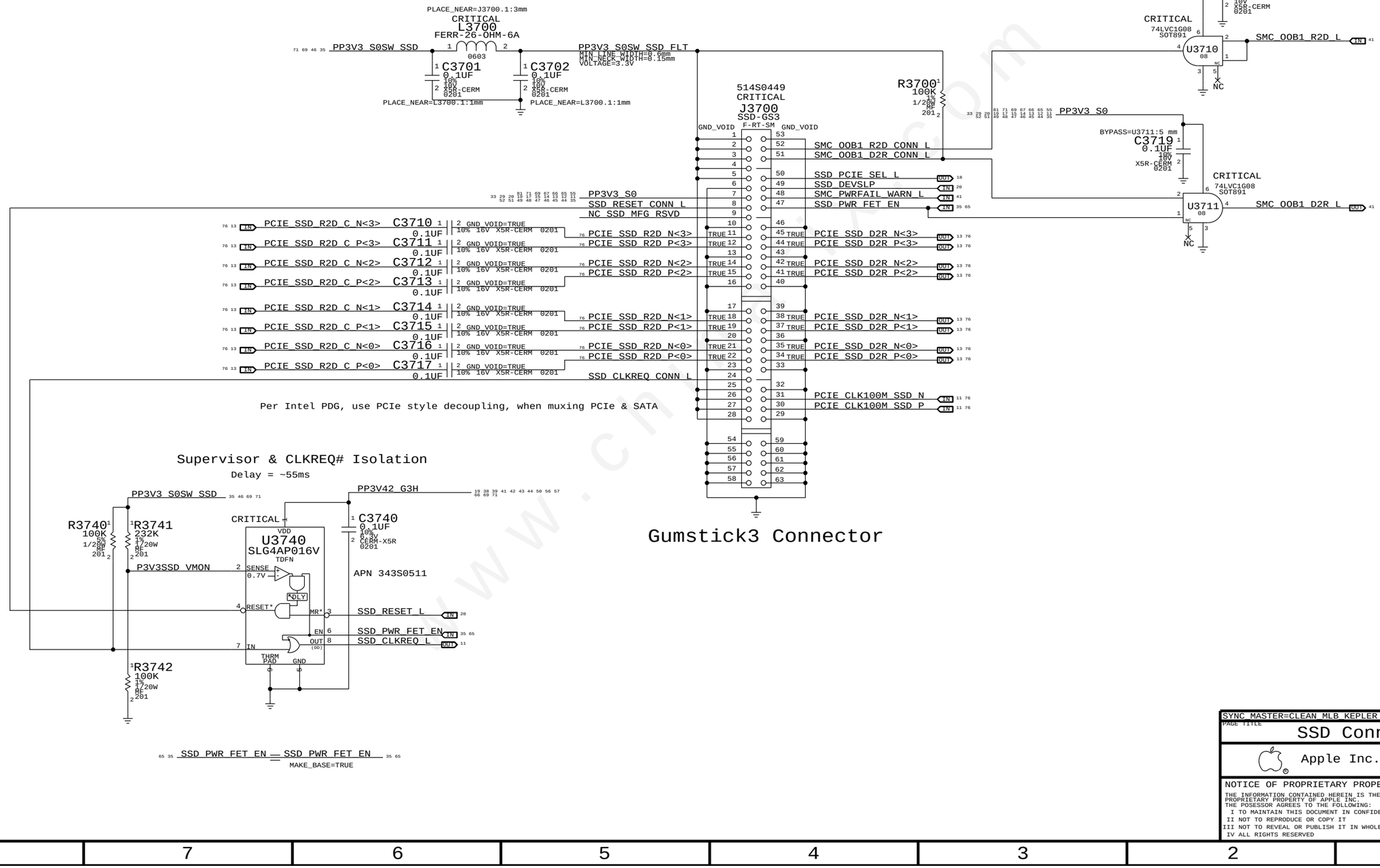

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	BRANCH <BRANCH>
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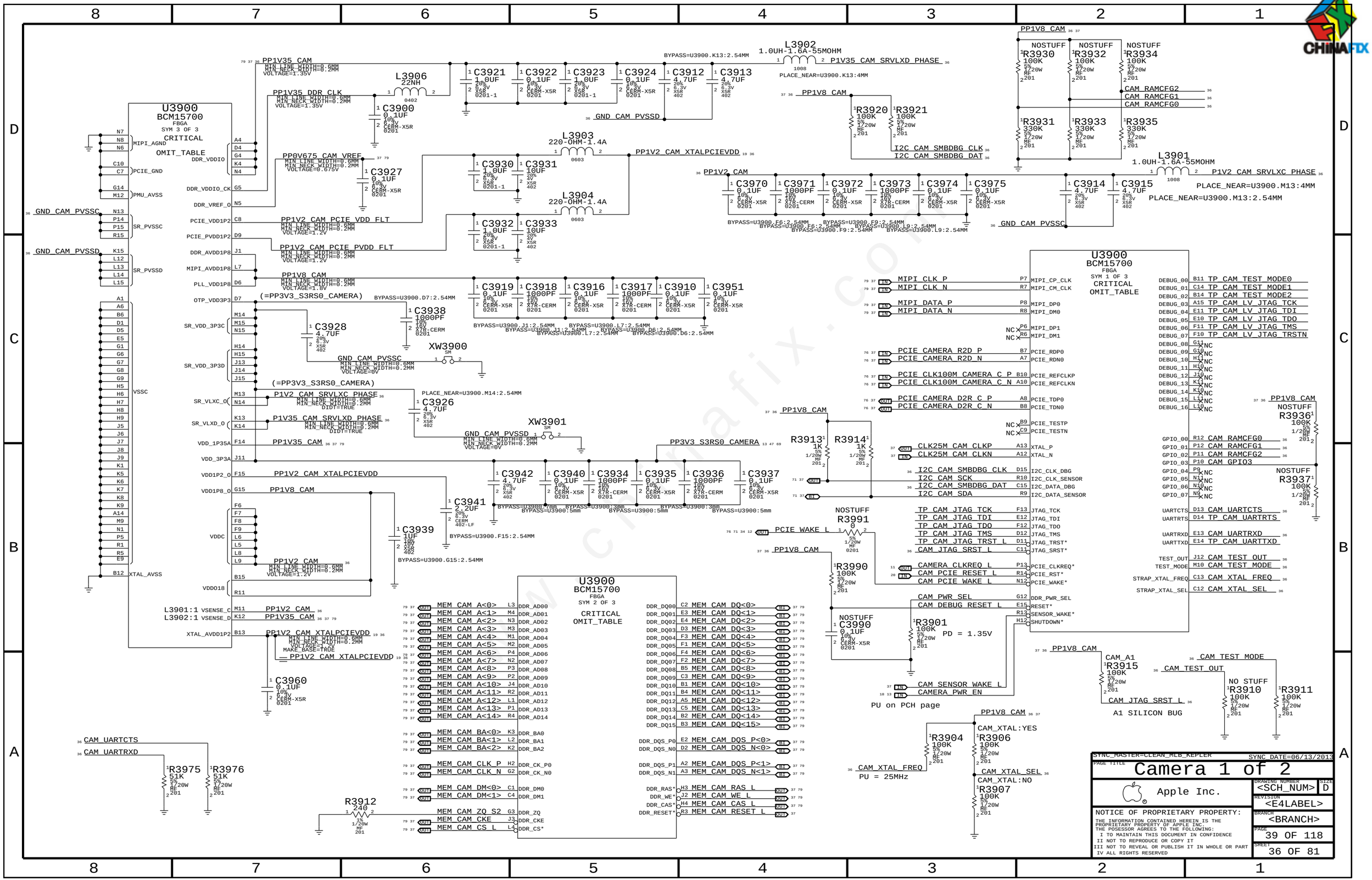
U3900
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FBGA
SYM 3 OF 3
CRITICAL
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PP1V35_CAM
PP1V35_DDR_CLK
L3906
22NH
L3902
1.0UH-1.6A-55MOHM
P1V35_CAM_SRVLXD_PHASE
PP1V8_CAM
GND_CAM_PVSSD
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PVDD_FLT
PP1V2_CAM_XTALPCIEVDD
L3901
1.0UH-1.6A-55MOHM
P1V2_CAM_SRVLXC_PHASE
PLACE_NEAR=U3900.M13:4MM
GND_CAM_PVSSC
(=PP3V3_S3RS0_CAMERA)
XW3900
XW3901
PP3V3_S3RS0_CAMERA
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP1V35_CAM
PP1V2_CAM_XTALPCIEVDD
PP1V8_CAM
PP1V2_CAM
GND_CAM_PVSSD
XTAL_AVSS
L3901:1 VSENSE_C
L3902:1 VSENSE_D
XTAL_AVDD1P2
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PCIE_WAKE_L
CAM_RAMCFG2
CAM_RAMCFG1
CAM_RAMCFG0
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
PU on PCH page
A1 SILICON BUG
CAM_XTAL:YES
CAM_XTAL:NO
CAM_XTAL_FREQ
PU = 25MHz
CAM_UARTCTS
CAM_UARTRXD
CAM_TEST_MODE
CAM_TEST_OUT
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
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MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
SYNC_MASTER=CLEAN_MLB_REPLER
SYNC_DATE=06/13/2013
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Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
39 OF 118
SHEET
36 OF 81
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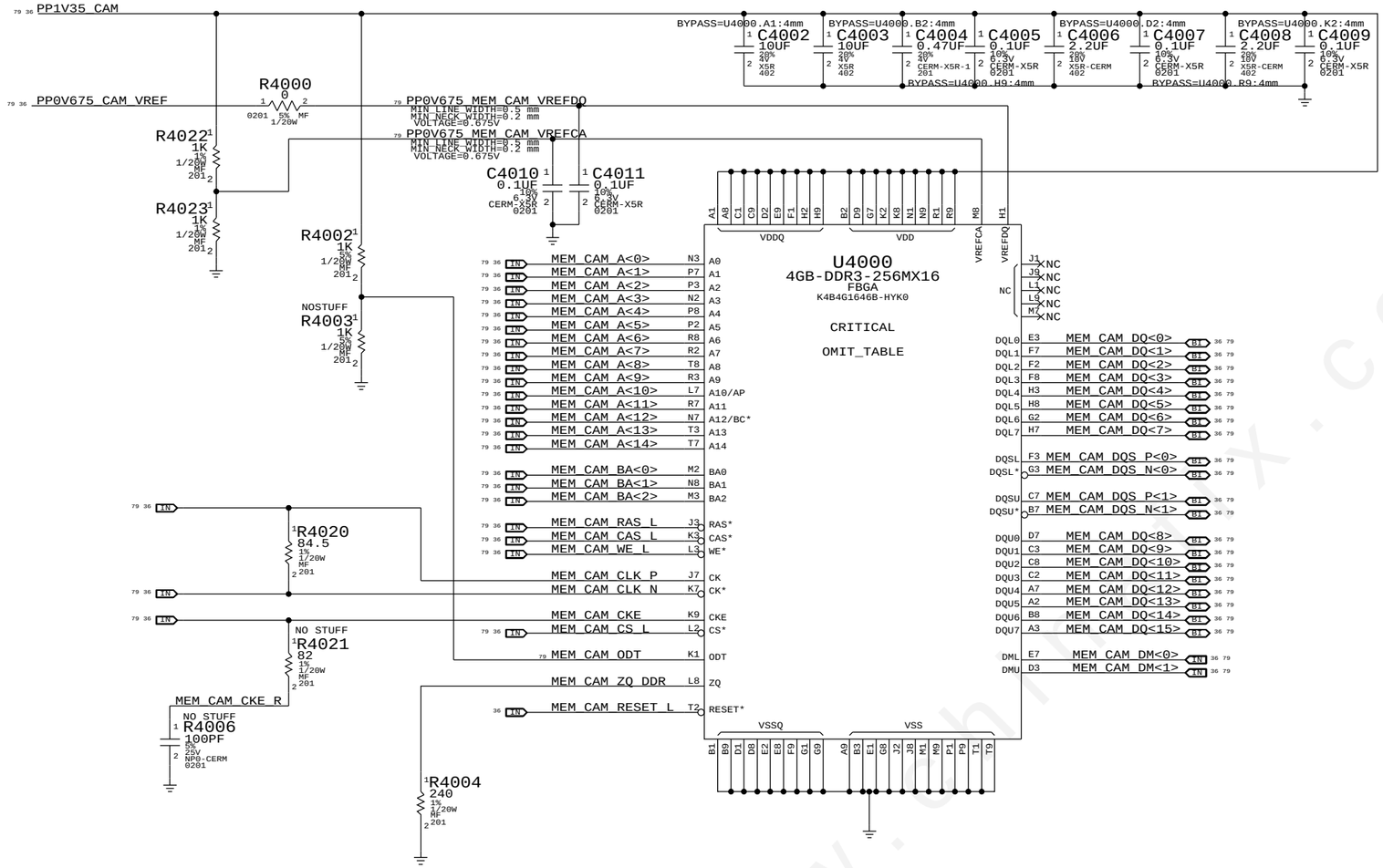


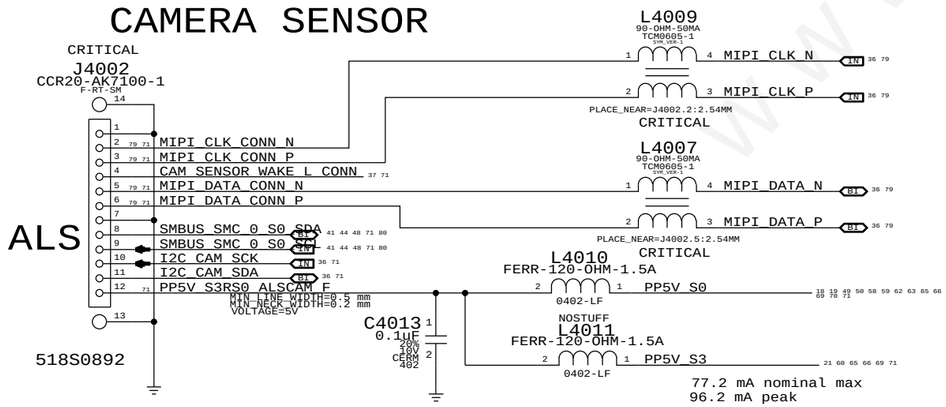
remove DRAM SPD Straps

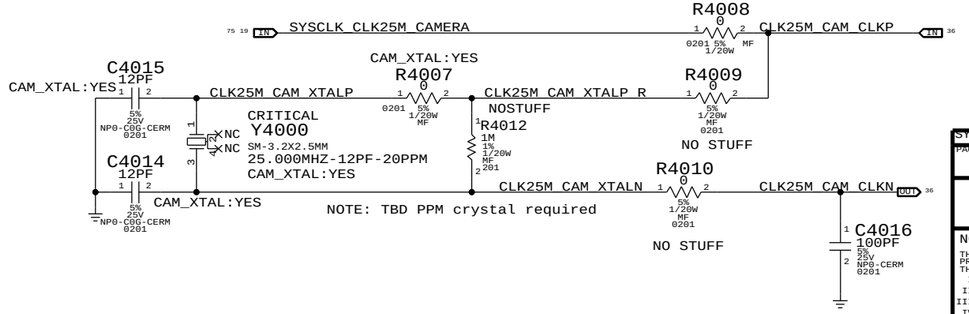
DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR





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PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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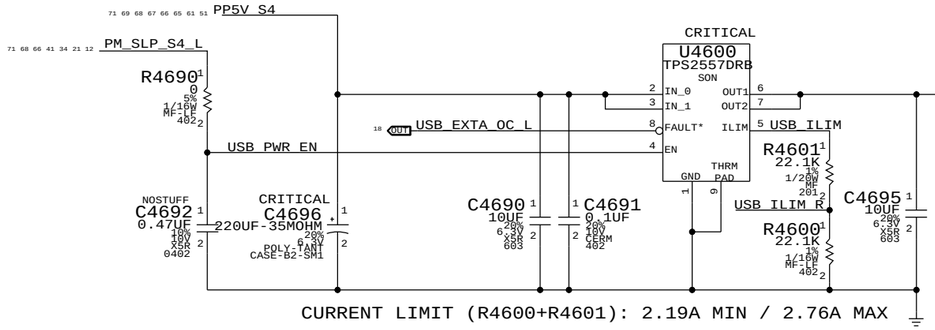
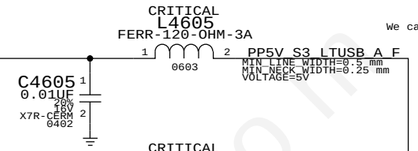
USB Port Power Switch



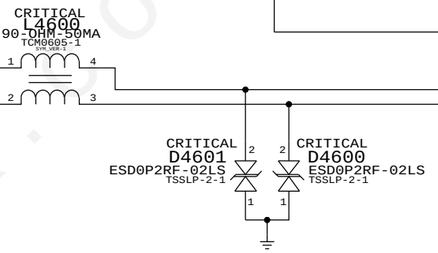
CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

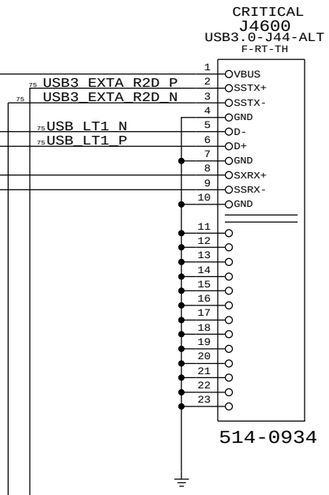
Left USB Port A



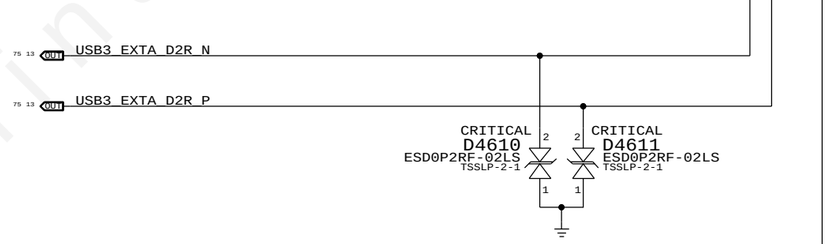
We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin

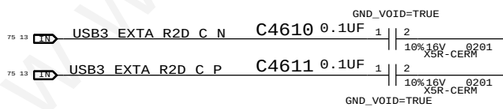


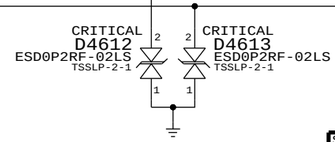


75 USB3_EXTA_R2D_P
75 USB3_EXTA_R2D_N
75 USB_LT1_N
75 USB_LT1_P



USB/SMC Debug Mux





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PAGE TITLE

USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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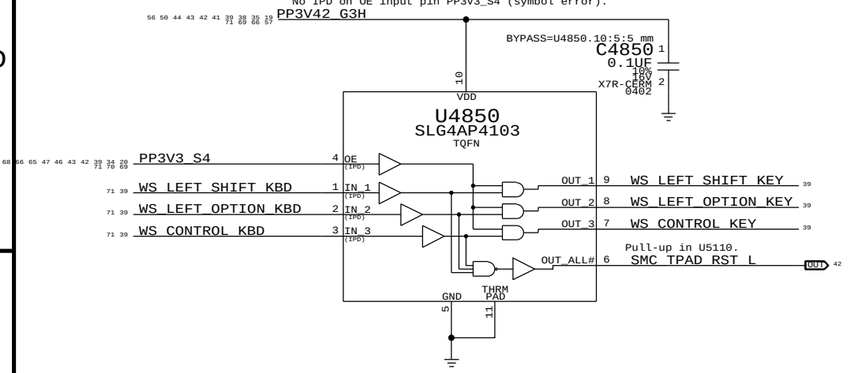
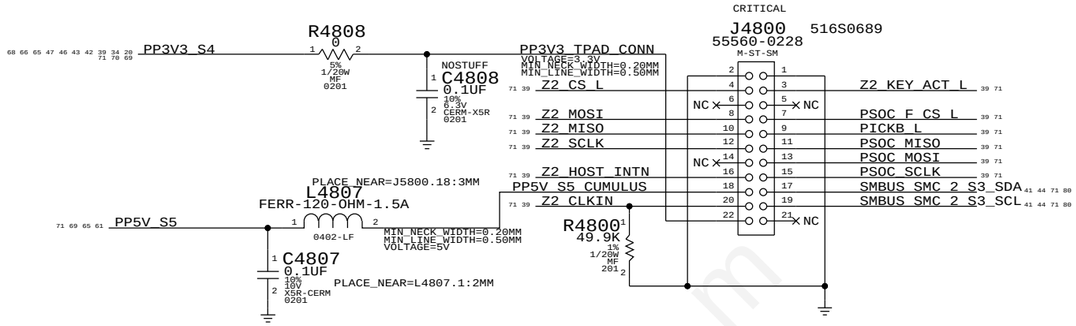
SMC Manual Reset & Isolation

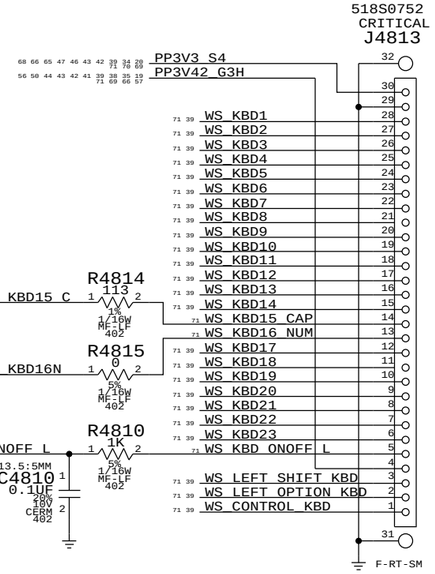
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IPD Flex Connector



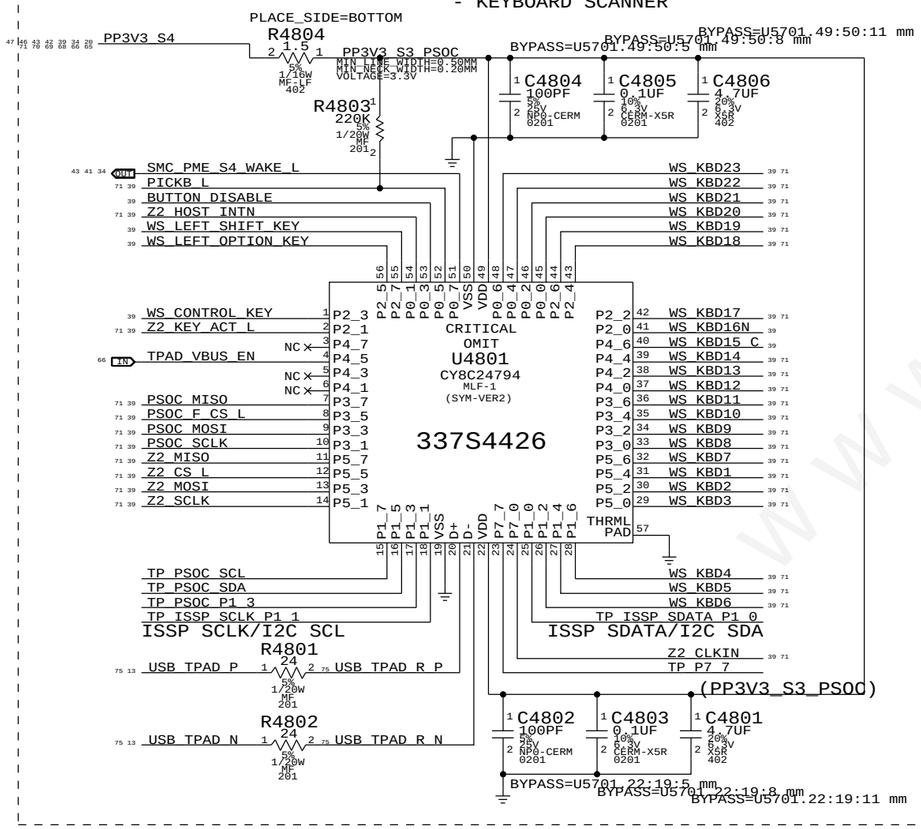
Keyboard Connector



FF14A-30C-R11DL-B-3H

PSOC USB CONTROLLER

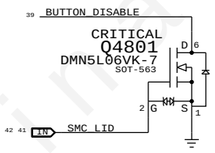
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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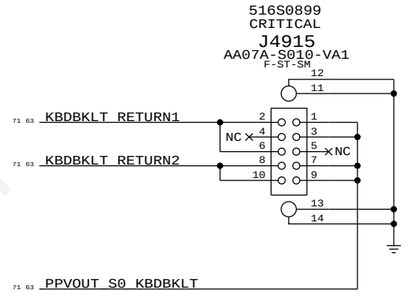
Keyboard Backlight Connector



SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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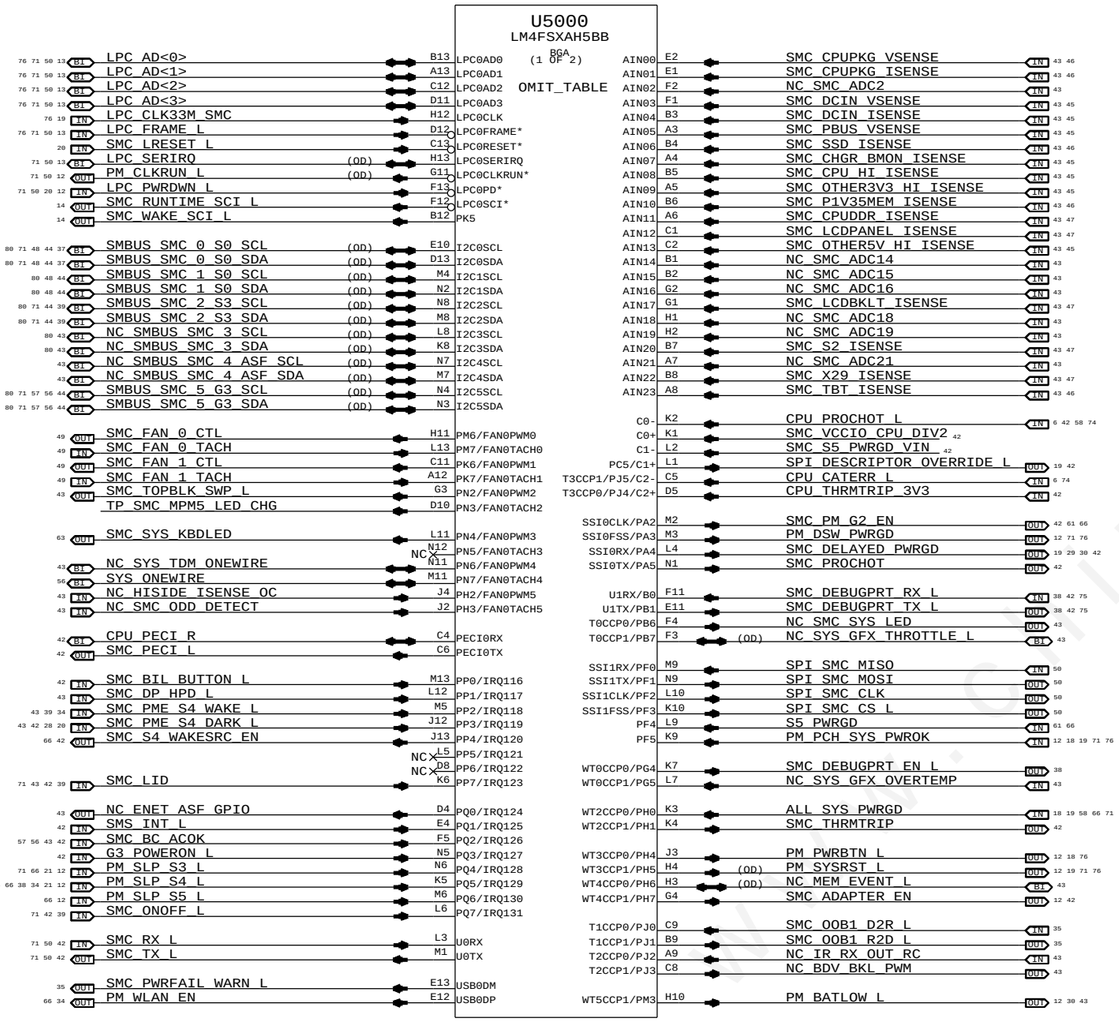
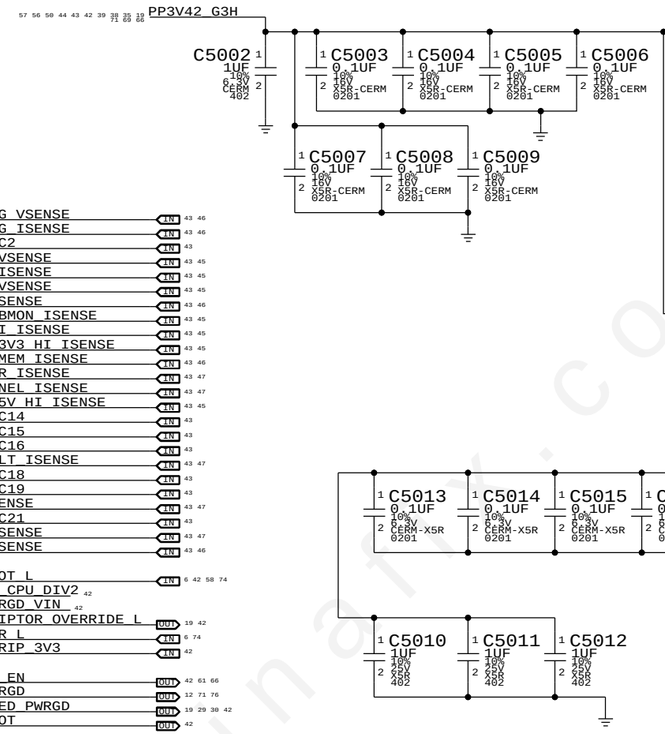
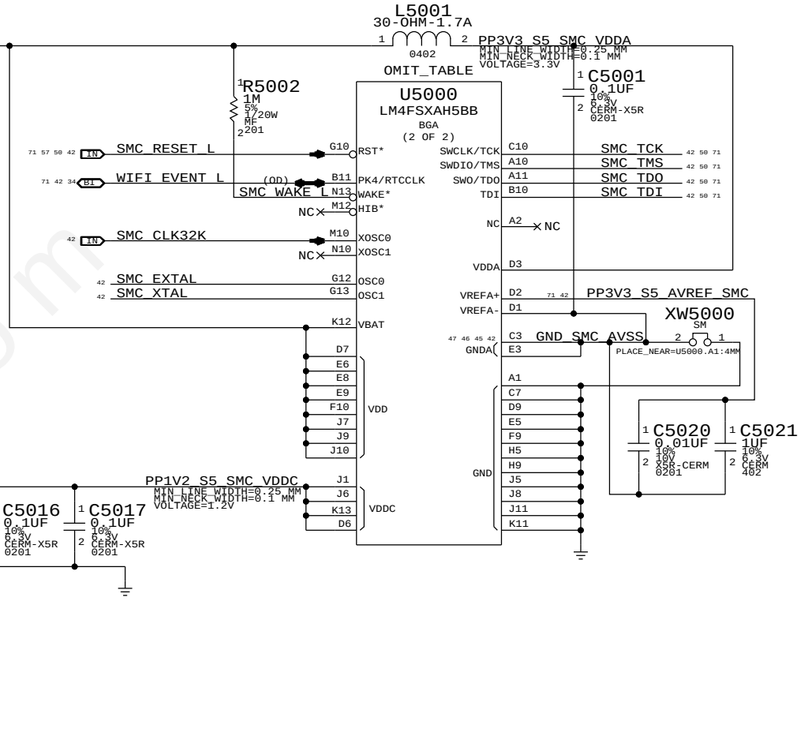
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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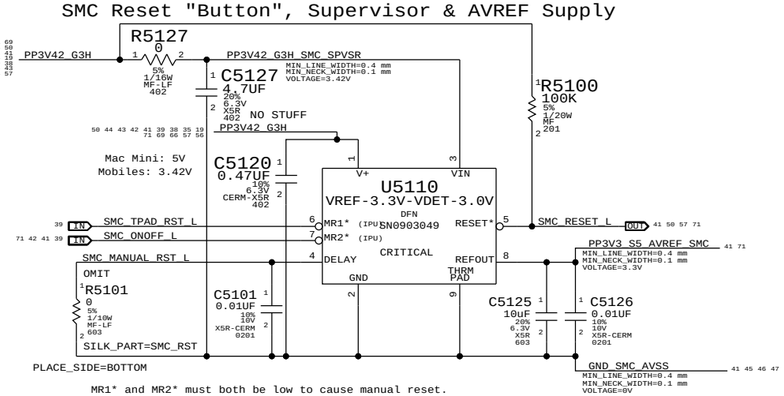
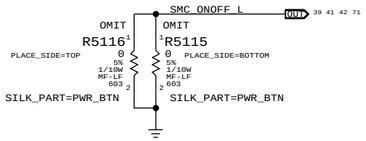
SMC Reset "Button", Supervisor & AVREF Supply



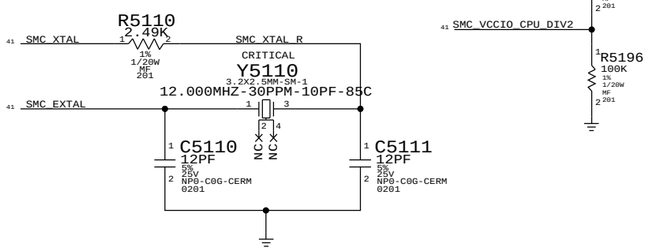
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

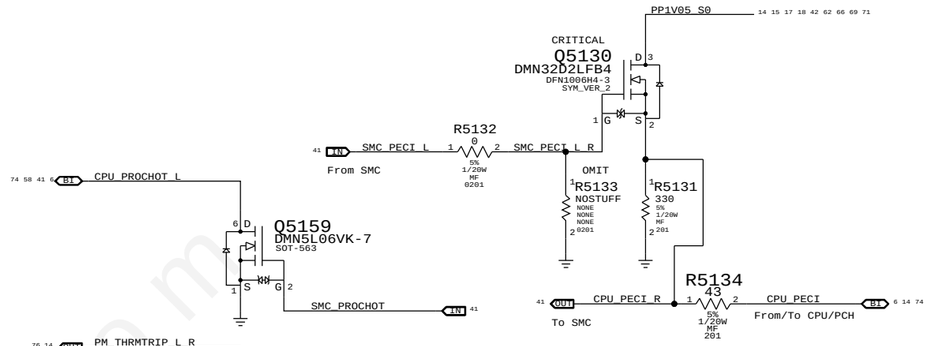


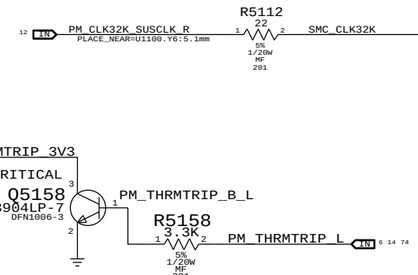
SMC Crystal Circuit

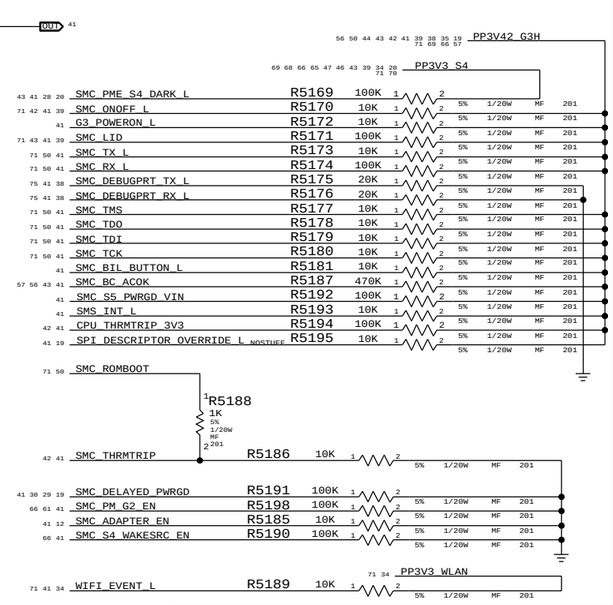


SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

SMC12 PECI SUPPORT







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PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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57 56 43 42 41	SMC_BC_ACOK		SMC_BC_ACOK	41 42 43 56 57	43 41	NC_ENET_ASF_GPIO	NC_ENET_ASF_GPIO	41 43
43 41	NC_HISIDE_ISENSE_OC		NC_HISIDE_ISENSE_OC	41 43	43 41	NC_SMC_SYS_LED	NC_SMC_SYS_LED	41 43
46 43 41	SMC_CPUPKG_VSENSE		SMC_CPUPKG_VSENSE	41 43 46	43 41	NC_MEM_EVENT_L	NC_MEM_EVENT_L	41 43
46 43 41	SMC_CPUPKG_ISENSE		SMC_CPUPKG_ISENSE	41 43 46	43 41	NC_SMC_ODD_DETECT	NC_SMC_ODD_DETECT	41 43
43 41	NC_SMC_ADC2		NC_SMC_ADC2	41 43	43 41	NC_IR_RX_OUT_RC	NC_IR_RX_OUT_RC	41 43
45 43 41	SMC_DCIN_VSENSE		SMC_DCIN_VSENSE	41 43 45	43 41	NC_SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	41 43
45 43 41	SMC_DCIN_ISENSE		SMC_DCIN_ISENSE	41 43 45	43 41	NC_SYS_GFX_THROTTLE_L	NC_SYS_GFX_THROTTLE_L	41 43
45 43 41	SMC_PBUS_VSENSE		SMC_PBUS_VSENSE	41 43 45	43 41	NC_SYS_GFX_OVERTEMP	NC_SYS_GFX_OVERTEMP	41 43
46 43 41	SMC_SSD_ISENSE		SMC_SSD_ISENSE	41 43 46				
45 43 41	SMC_CHGR_BMON_ISENSE		SMC_CHGR_BMON_ISENSE	41 43 45				
45 43 41	SMC_CPU_HI_ISENSE		SMC_CPU_HI_ISENSE	41 43 45				
45 43 41	SMC_OTHER3V3_HI_ISENSE		SMC_OTHER3V3_HI_ISENSE	41 43 45				
46 43 41	SMC_P1V35MEM_ISENSE		SMC_P1V35MEM_ISENSE	41 43 46				
47 43 41	SMC_CPUDDR_ISENSE		SMC_CPUDDR_ISENSE	41 43 47				
47 43 41	SMC_LCDPANEL_ISENSE		SMC_LCDPANEL_ISENSE	41 43 47				
45 43 41	SMC_OTHER5V_HI_ISENSE		SMC_OTHER5V_HI_ISENSE	41 43 45				
43 41	NC_SMC_ADC14		NC_SMC_ADC14	41 43				
43 41	NC_SMC_ADC15		NC_SMC_ADC15	41 43				
43 41	NC_SMC_ADC16		NC_SMC_ADC16	41 43				
47 43 41	SMC_LCDBKLT_ISENSE		SMC_LCDBKLT_ISENSE	41 43 47				
43 41	NC_SMC_ADC18		NC_SMC_ADC18	41 43				
43 41	NC_SMC_ADC19		NC_SMC_ADC19	41 43				
47 43 41	SMC_S2_ISENSE		SMC_S2_ISENSE	41 43 47				
43 41	NC_SMC_ADC21		NC_SMC_ADC21	41 43				
47 43 41	SMC_X29_ISENSE		SMC_X29_ISENSE	41 43 47				
46 43 41	SMC_TBT_ISENSE		SMC_TBT_ISENSE	41 43 46				
43 41	NC_SMBUS_SMC_4_ASF_SCL		NC_SMBUS_SMC_4_ASF_SCL	41 43				
43 41	NC_SMBUS_SMC_4_ASF_SDA		NC_SMBUS_SMC_4_ASF_SDA	41 43				
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43 41	NC_BDV_BKL_PWM		NC_BDV_BKL_PWM	41 43				
43 42 41 28 20	SMC_PME_S4_DARK_L		SMC_PME_S4_DARK_L	20 28 41 42 43				
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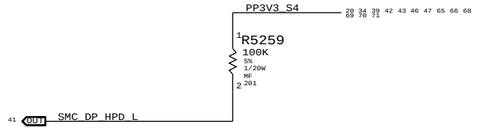
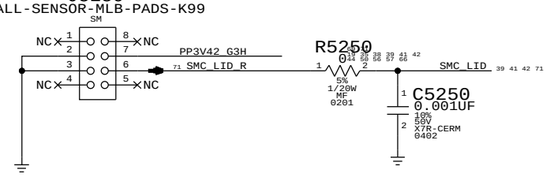
Spare S4 IRQ



Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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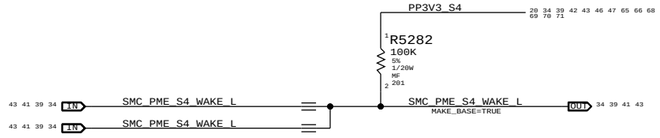

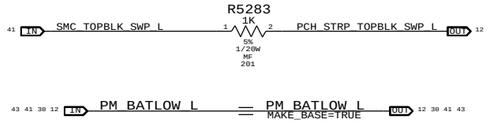

PAGE TITLE
SMC Project Support

Apple Inc.

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REVISION <E4LABEL>
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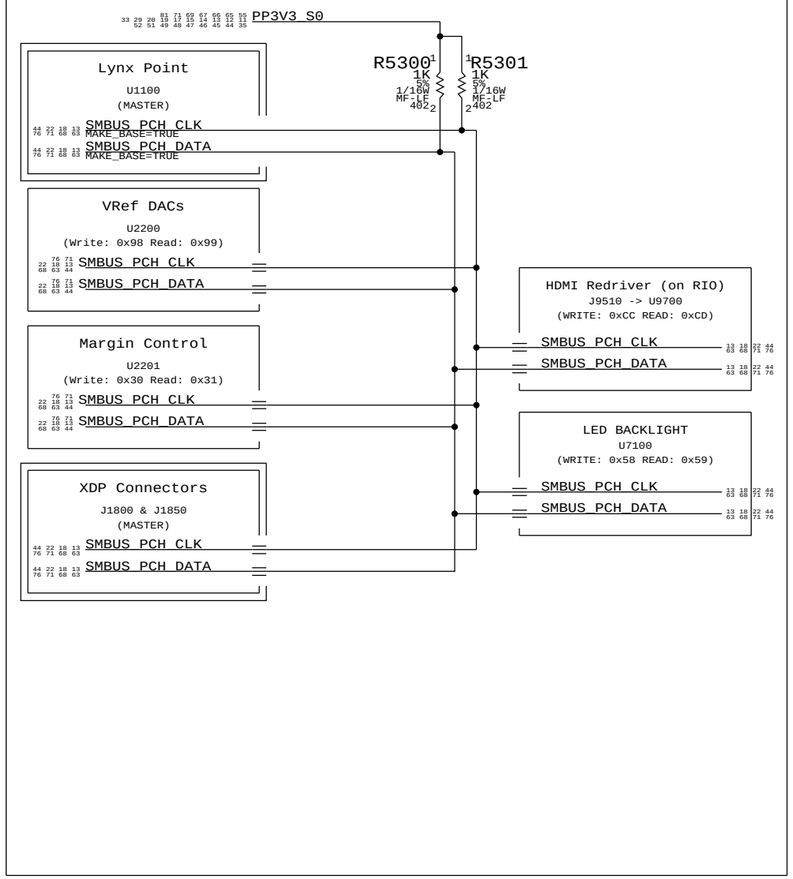
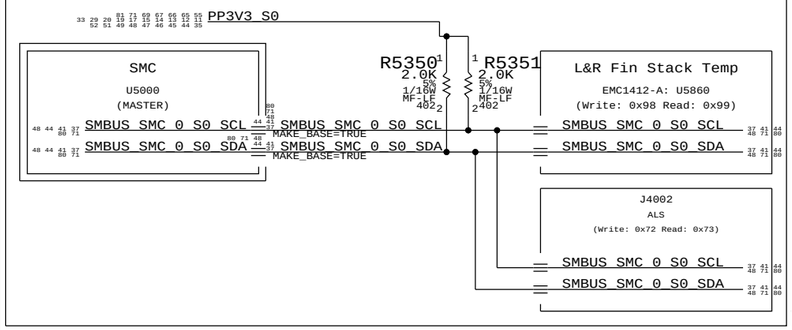
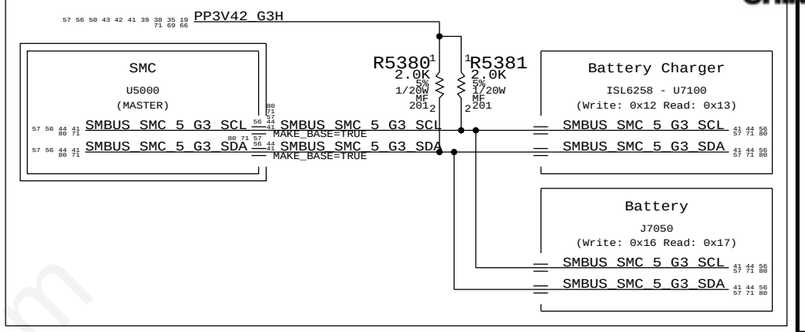
PCH SMBus "0" Connections



SMC "0" SMBus Connections

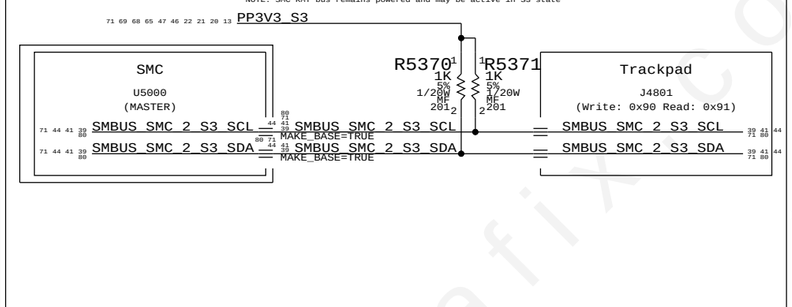


SMC "5" SMBUS CONNECTIONS



SMC "2" SMBUS CONNECTIONS

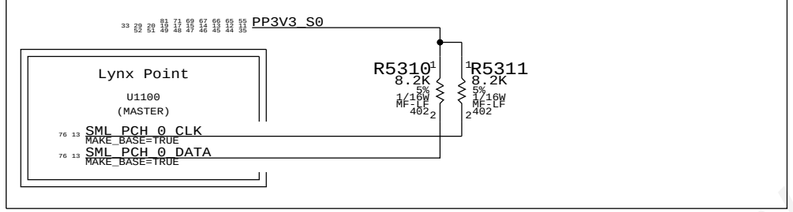
NOTE: SMC RMT bus remains powered and may be active in S3 state



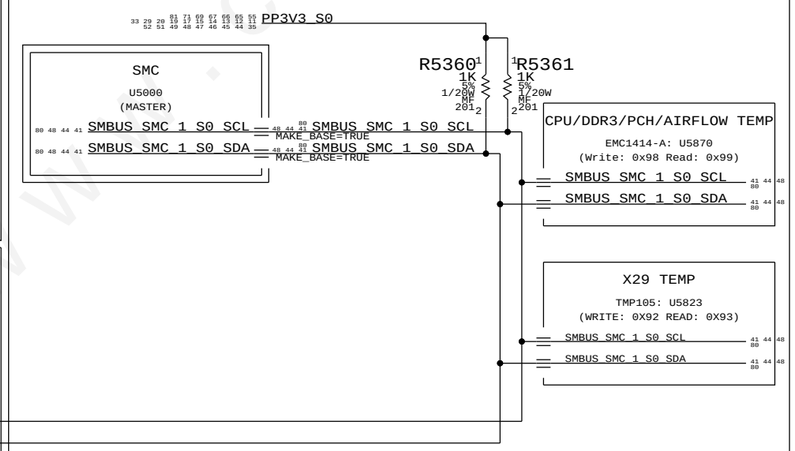
SMC "4" SMBUS CONNECTIONS

SMC "3" SMBUS CONNECTIONS

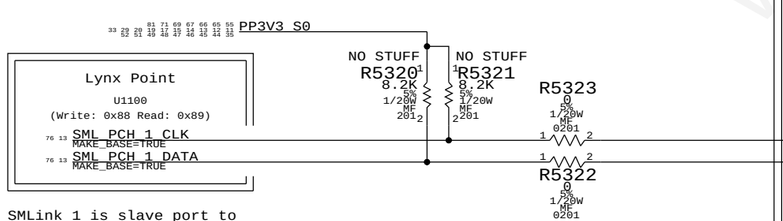
PCH "SMLink 0" Connections



SMC "1" SMBUS CONNECTIONS



PCH "SMLink 1" Connections



SMLink 1 is slave port to
access PCH & CPU via PECI.

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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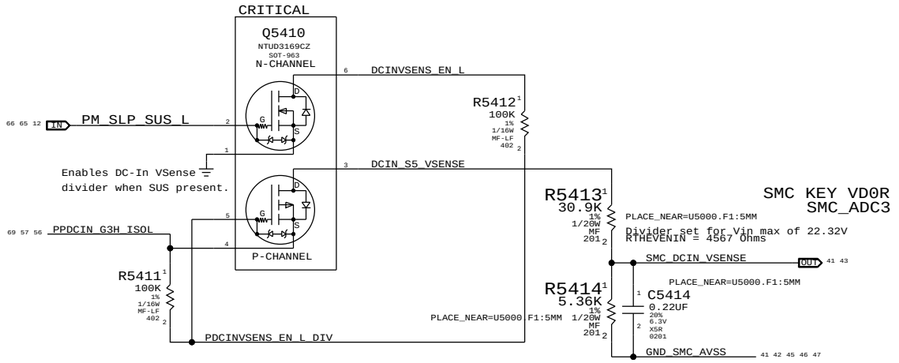
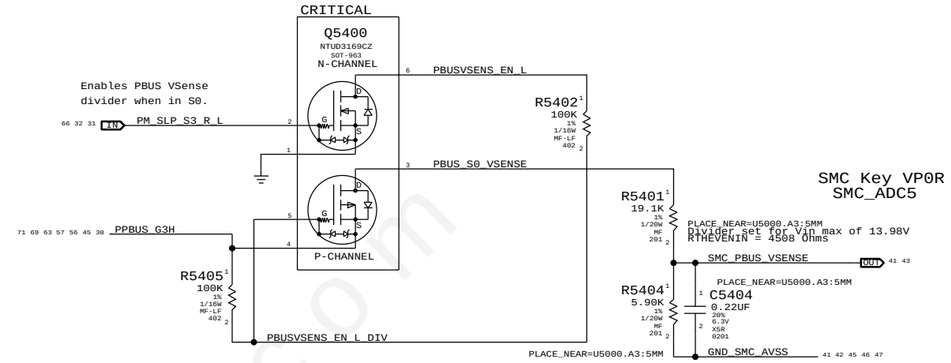
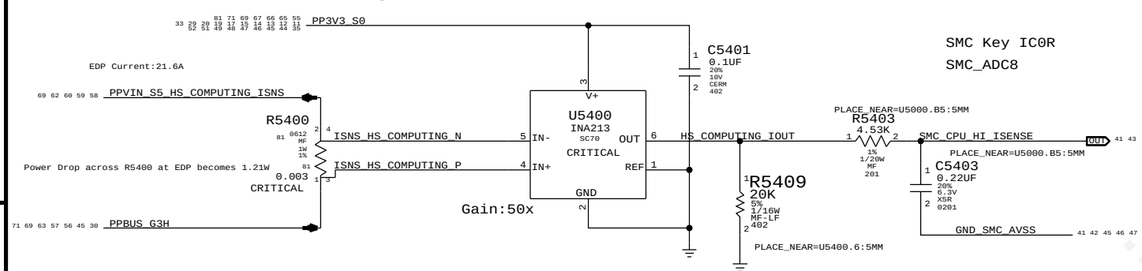
DC-In Voltage Sense Enable & Filter



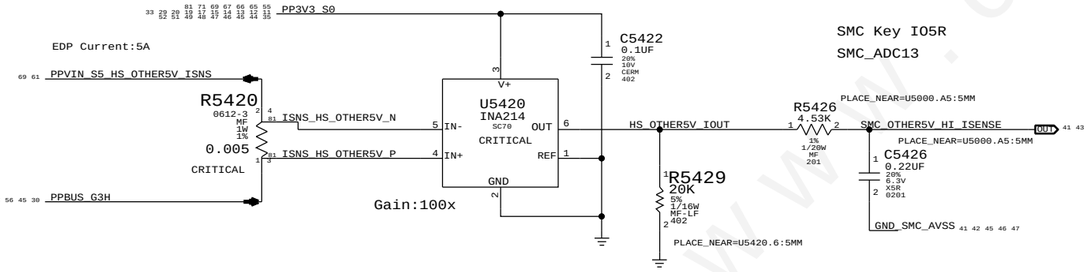
PBUS Voltage Sense Enable & Filter



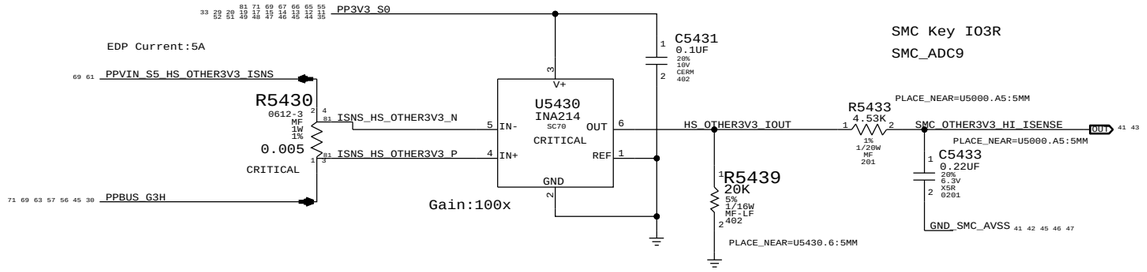
COMPUTING High Side Current Sense / Filter



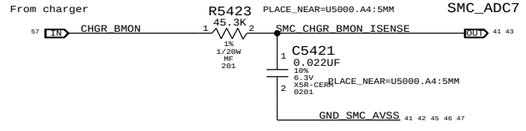
OTHERS (5V) High Side Current Sense / Filter



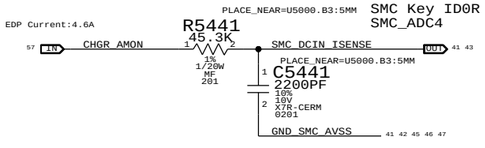
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CHANG_J45 SYNC_DATE=12/21/2012

PAGE TITLE: High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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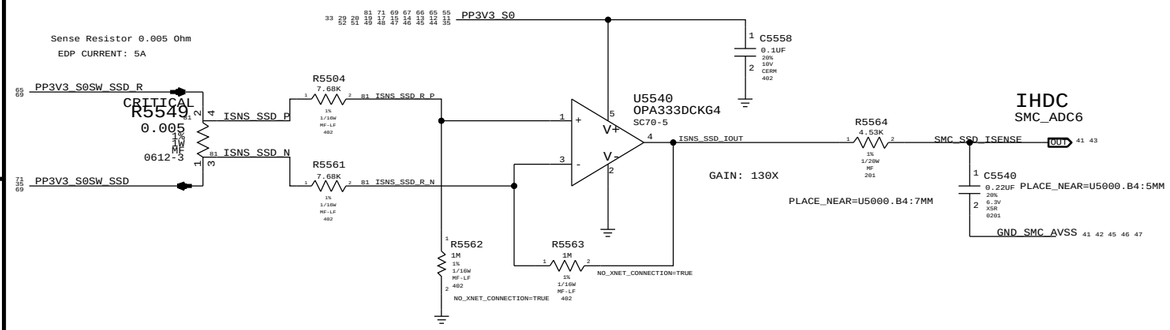
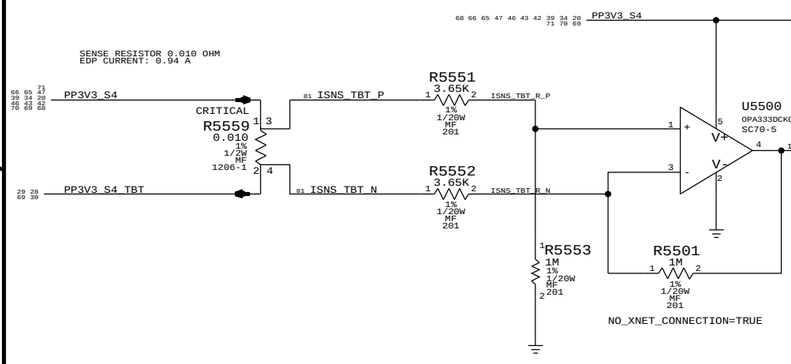
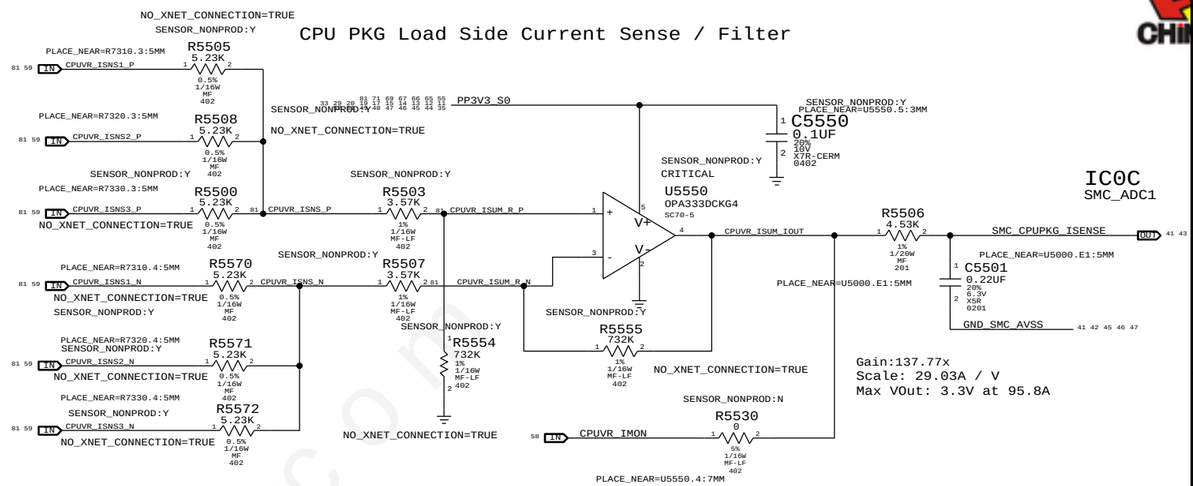
SSD CURRENT SENSE



TBT Router CURRENT SENSE

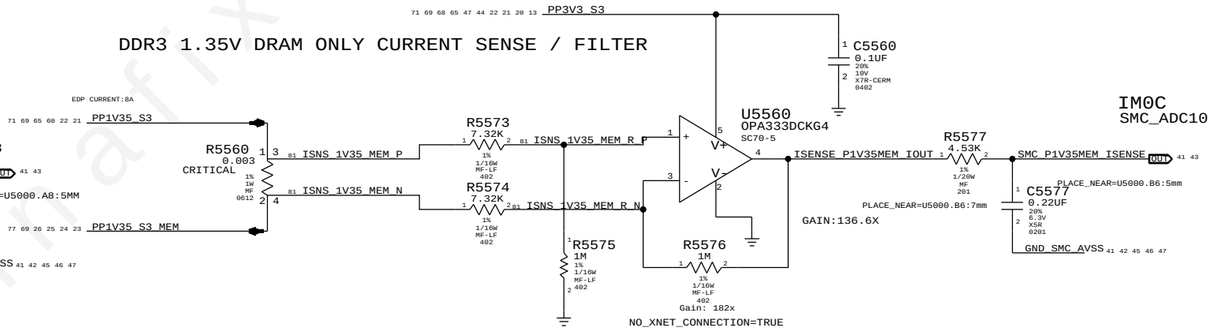


CPU PKG Load Side Current Sense / Filter

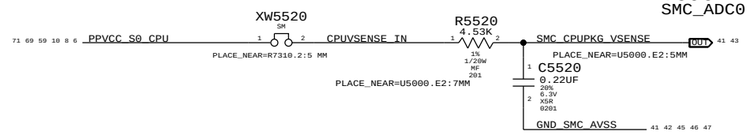


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



CPU Vcore Voltage Sense / Filter



SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: Load Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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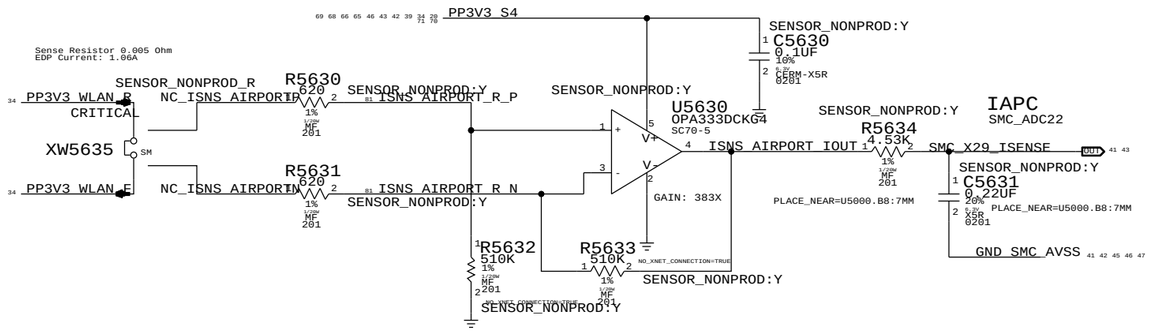
X29 AIRPORT CURRENT SENSE

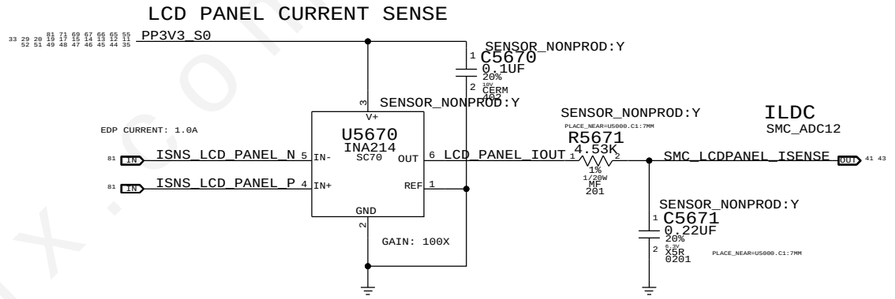


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5600,C5631,C5650,C5681,C5671,C5610		SENSOR_NONPROD:N

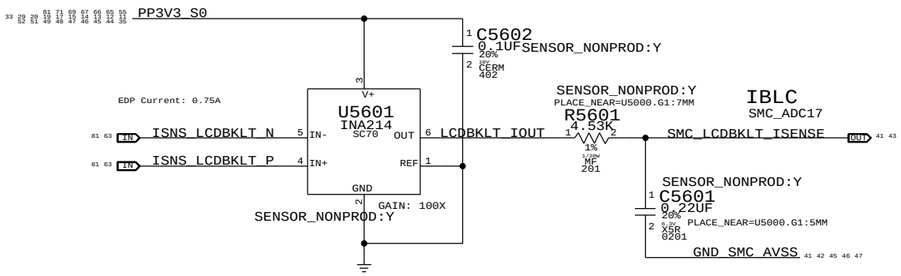
CPU DDR CURRENT SENSE

S2 CAMERA CONTROLLER CURRENT SENSE

LCD PANEL CURRENT SENSE



LCD BKLT Current Sense



SYNC_MASTER=CHANG_J45 SYNC_DATE=12/21/2012

PAGE TITLE

Debug Sensors

Apple Inc.

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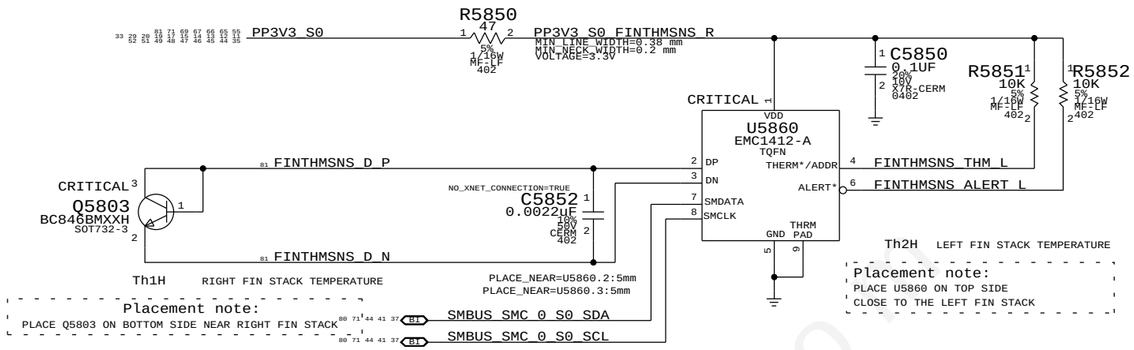
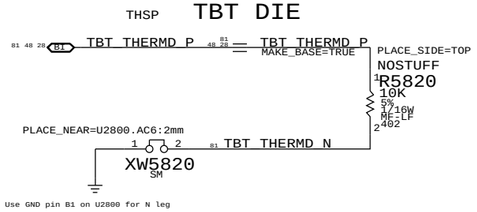
LEFT FIN STACK/RIGHT FIN STACK

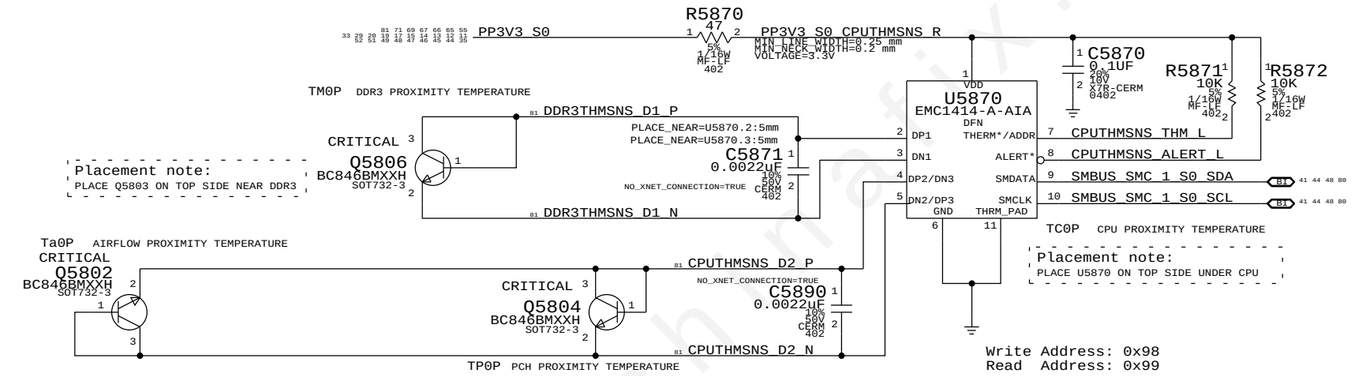


Write Address: 0x98
Read Address: 0x99

TBT DIE

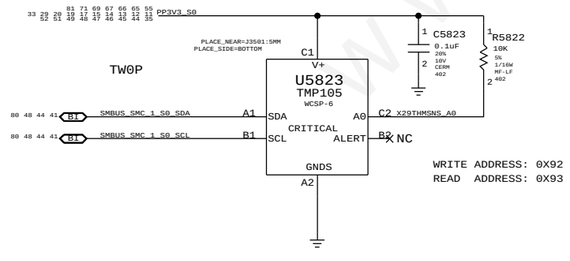


DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



Write Address: 0x98
Read Address: 0x99

X29 PROXIMITY



WRITE ADDRESS: 0X92
READ ADDRESS: 0X93

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE
Thermal Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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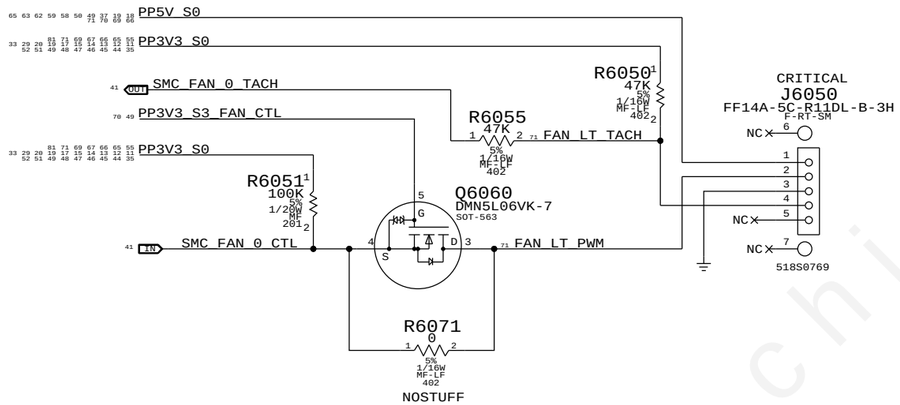
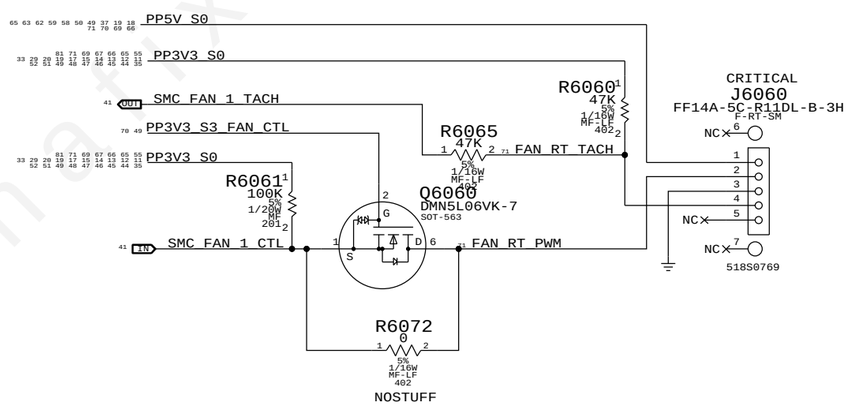
Left Fan



Right Fan



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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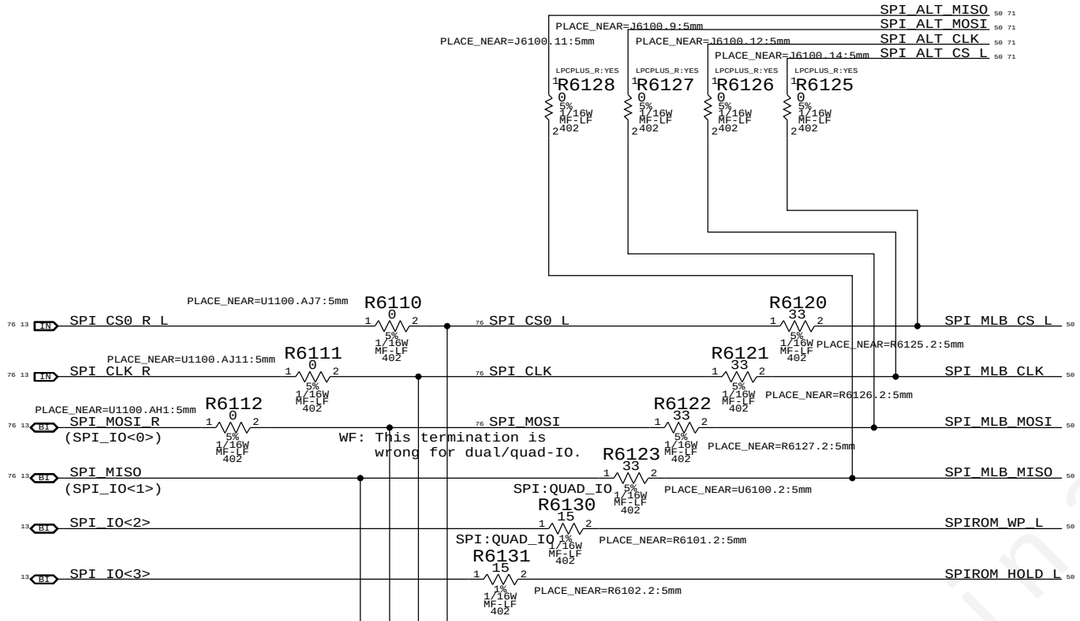
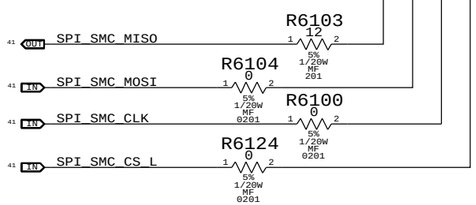
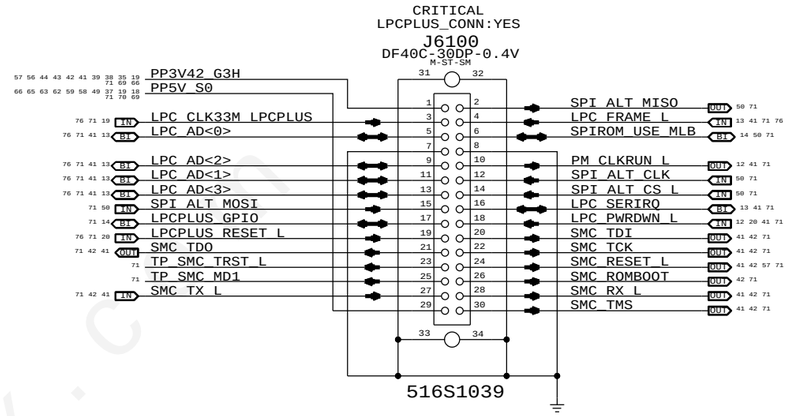
SPI Bus Series Termination



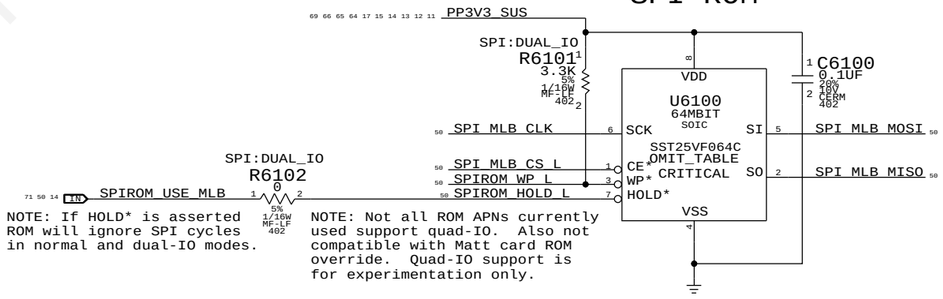
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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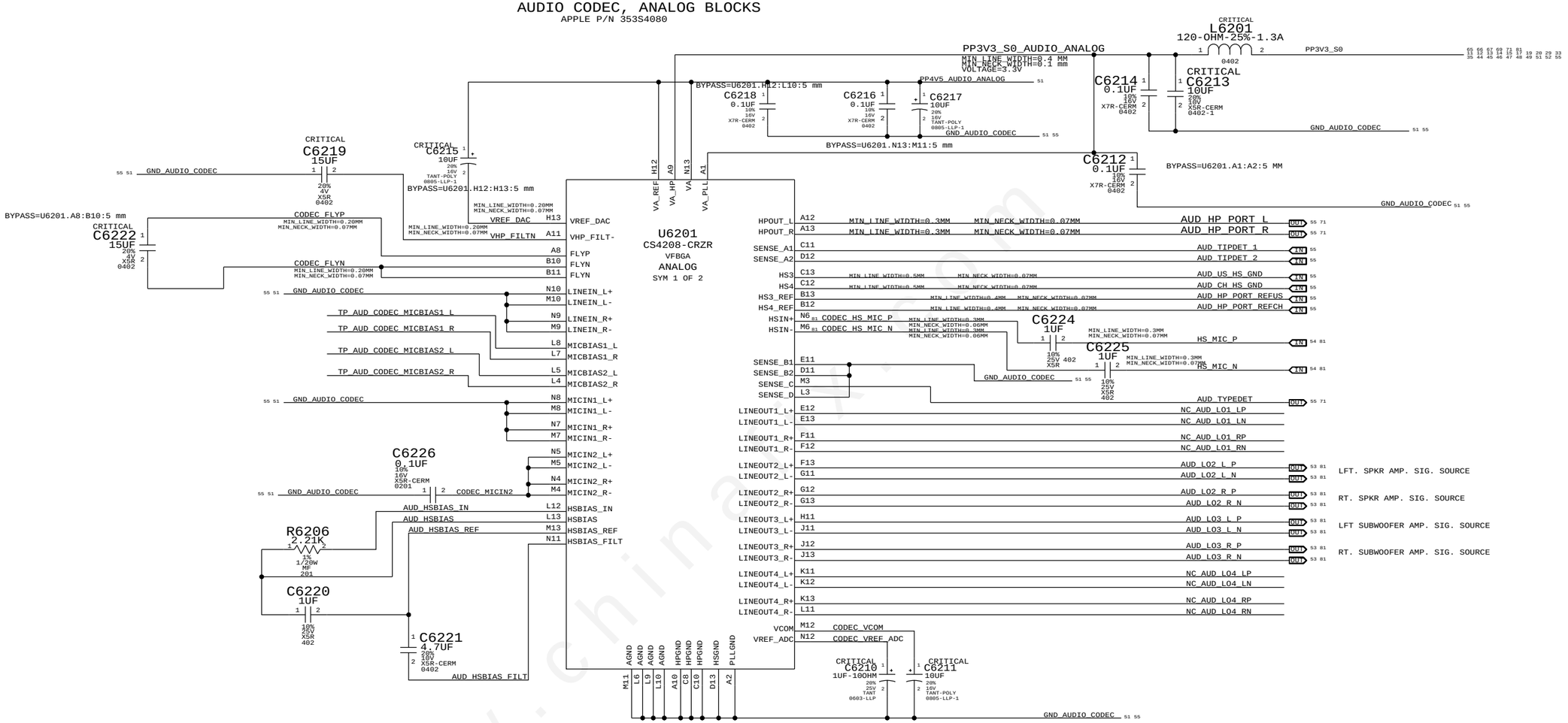
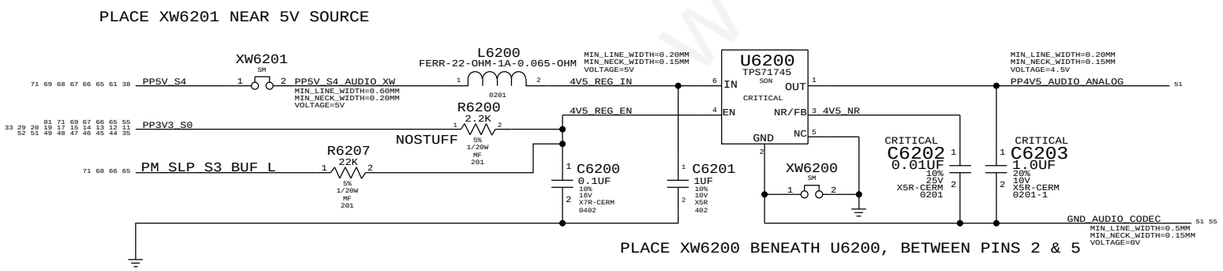
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC_MASTER=JOE_J45	SYNC_DATE=07/30/2013
PAGE TITLE	AUDIO:CODEC, ANALOG
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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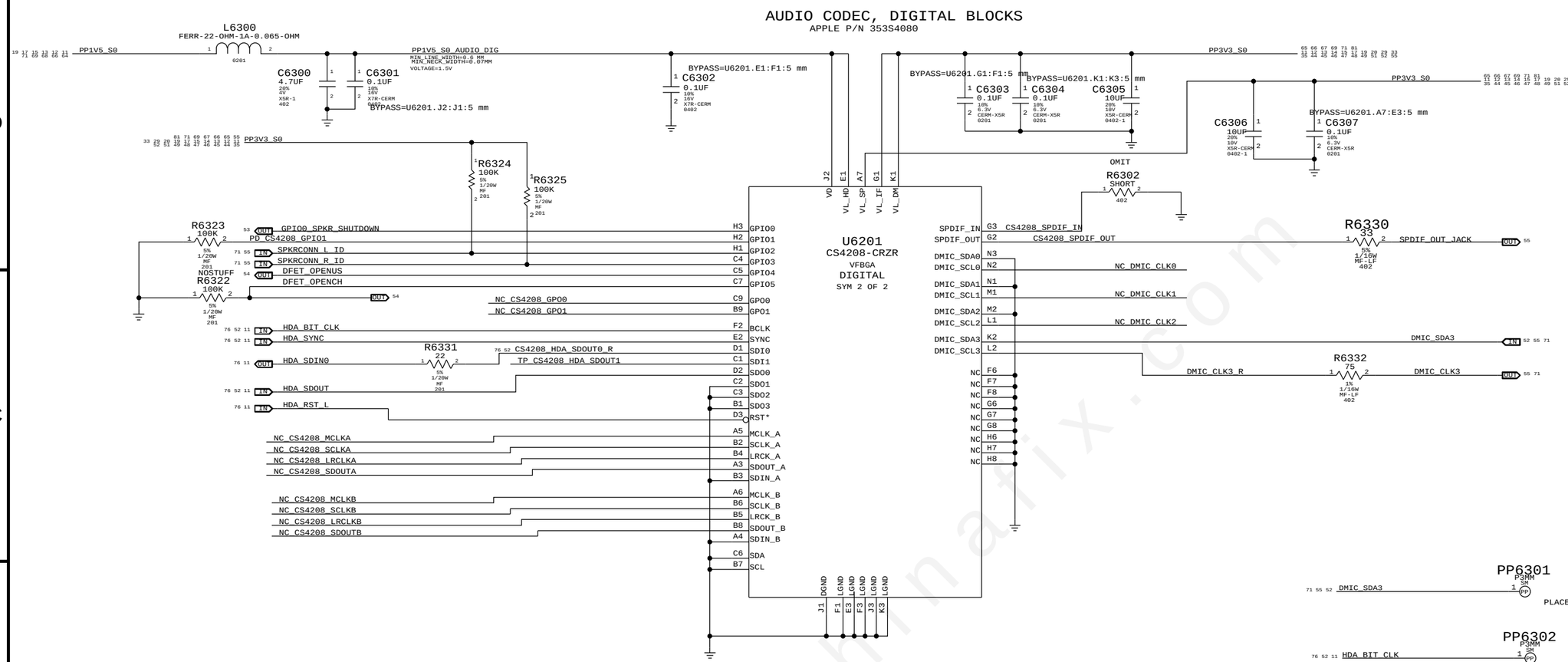
AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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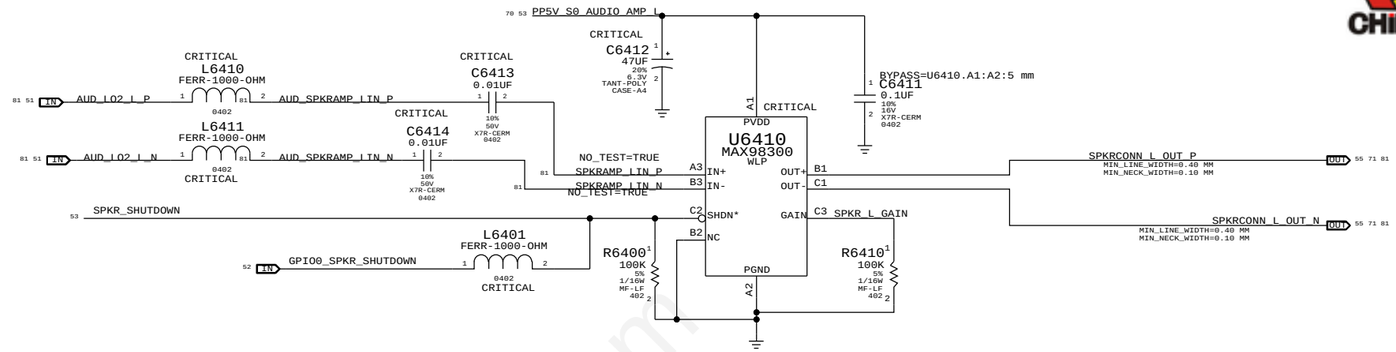
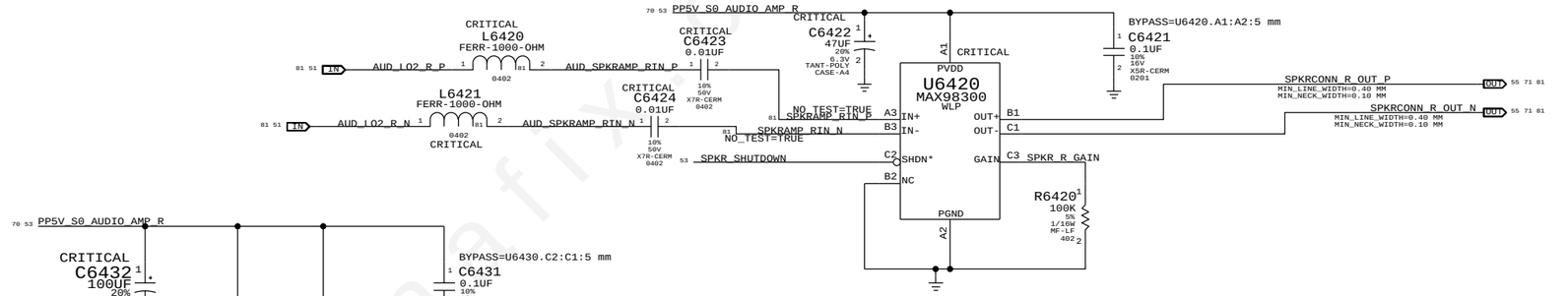
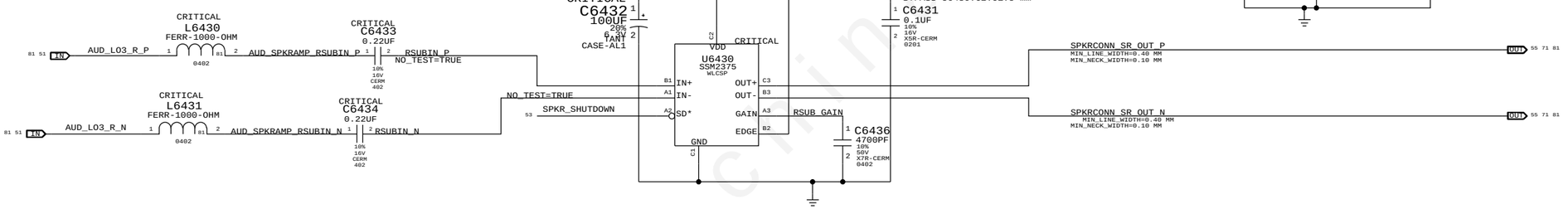
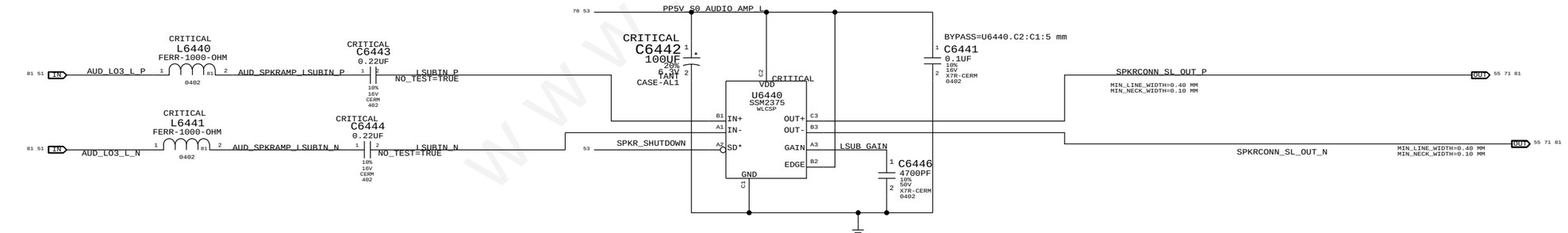
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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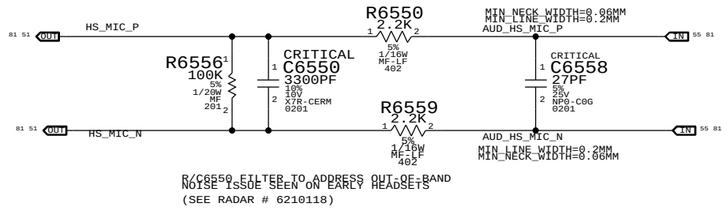

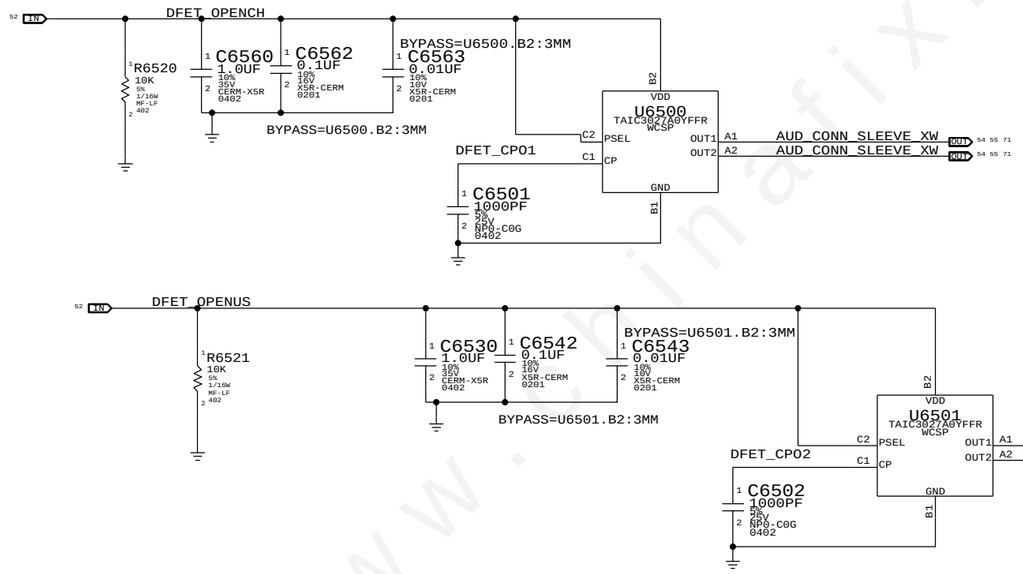

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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BRANCH: <BRANCH>

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

PP3V3_S0
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

L6611 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.3:2.54mm
XW6600 SM
L6612 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CH_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.5:2.54mm
XW6602 SM
L6614 120-OHM-25%-1.3A 0402 CRITICAL
AUD_US_HS_GND
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
XW6603 SM
AUD_HS_MIC_N

L6604 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
R6602 2.2K 5% 1/20W MF 201
L6608 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_2
AUD_CONN_TIPDET_2
GND_AUDIO_CODEC
R6603 2.2K 5% 1/20W MF 201
L6607 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_1
AUD_CONN_TIPDET_1
L6605 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
L6606 FERR-470-OHM 0201 CRITICAL
AUD_TYPEDET
AUD_CONN_TYPEDET
SPDIF_OUT_JACK
PP3V3_S0

R6601 10K 5% 1/16W MF-LF 402

DZ6607 ESDALC5-1BM2 SOD882 CRITICAL
C6602 100PF 5% 25V NP0-CERM 0201
DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
C6603 100PF 5% 25V NP0-CERM 0201
C6604 100PF 5% 25V NP0-CERM 0201
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
C6605 100PF 5% 25V NP0-CERM 0201
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
C6606 100PF 5% 25V NP0-CERM 0201
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
C6607 100PF 5% 25V NP0-CERM 0201
C6608 100PF 5% 25V NP0-CERM 0201
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC

VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF

SHELL PINS

C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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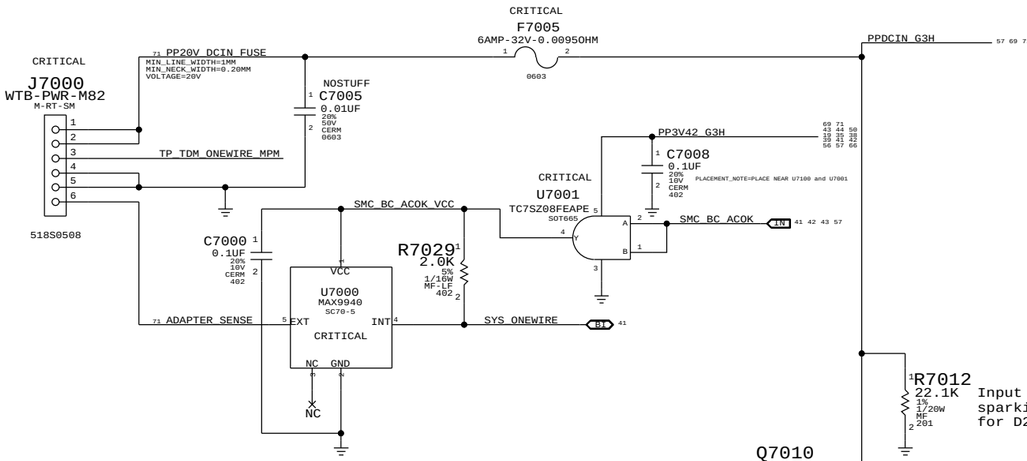
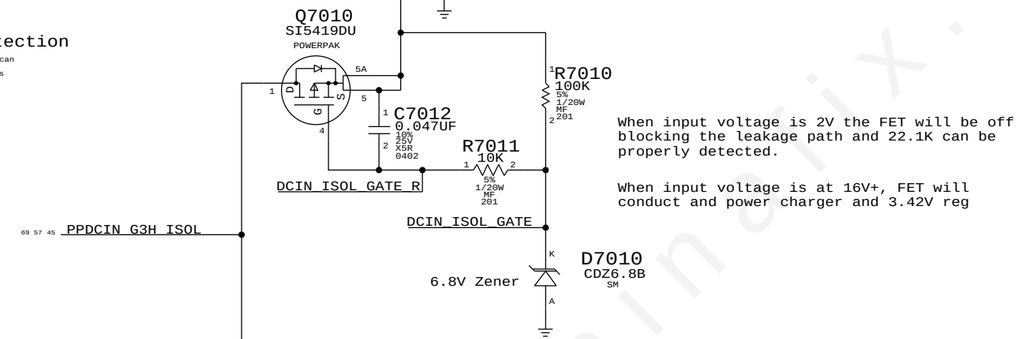
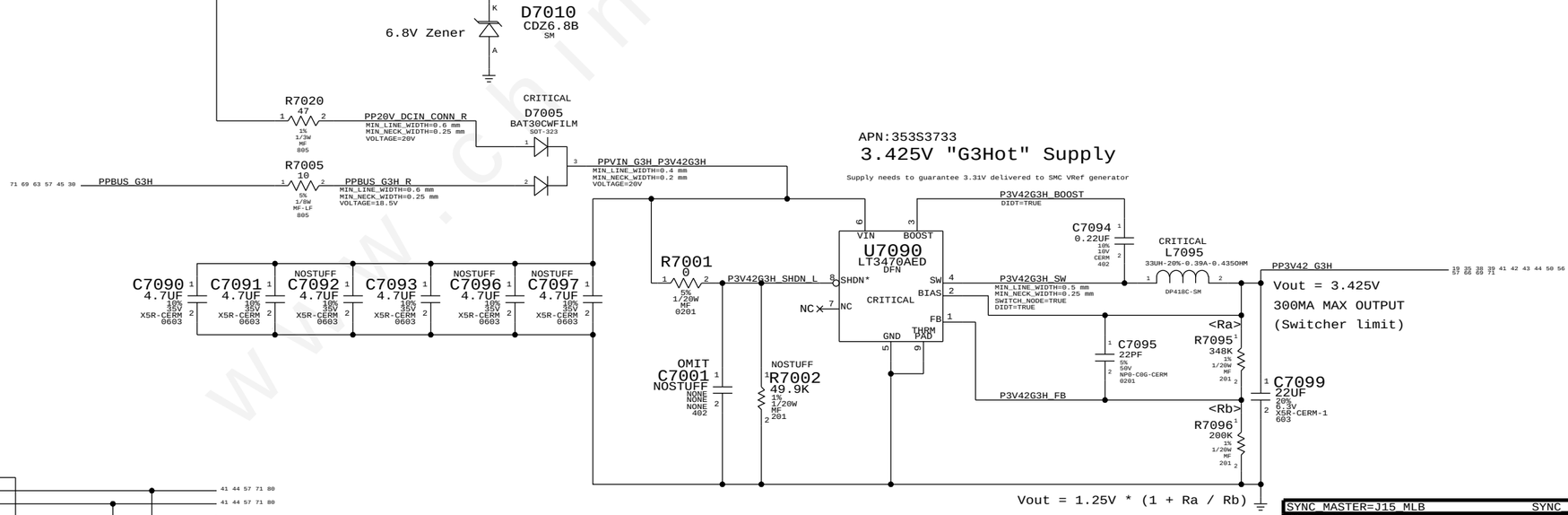
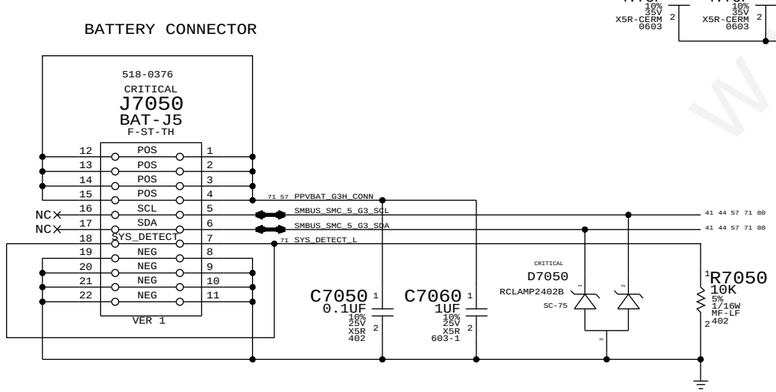
MagSafe DC Power Jack









SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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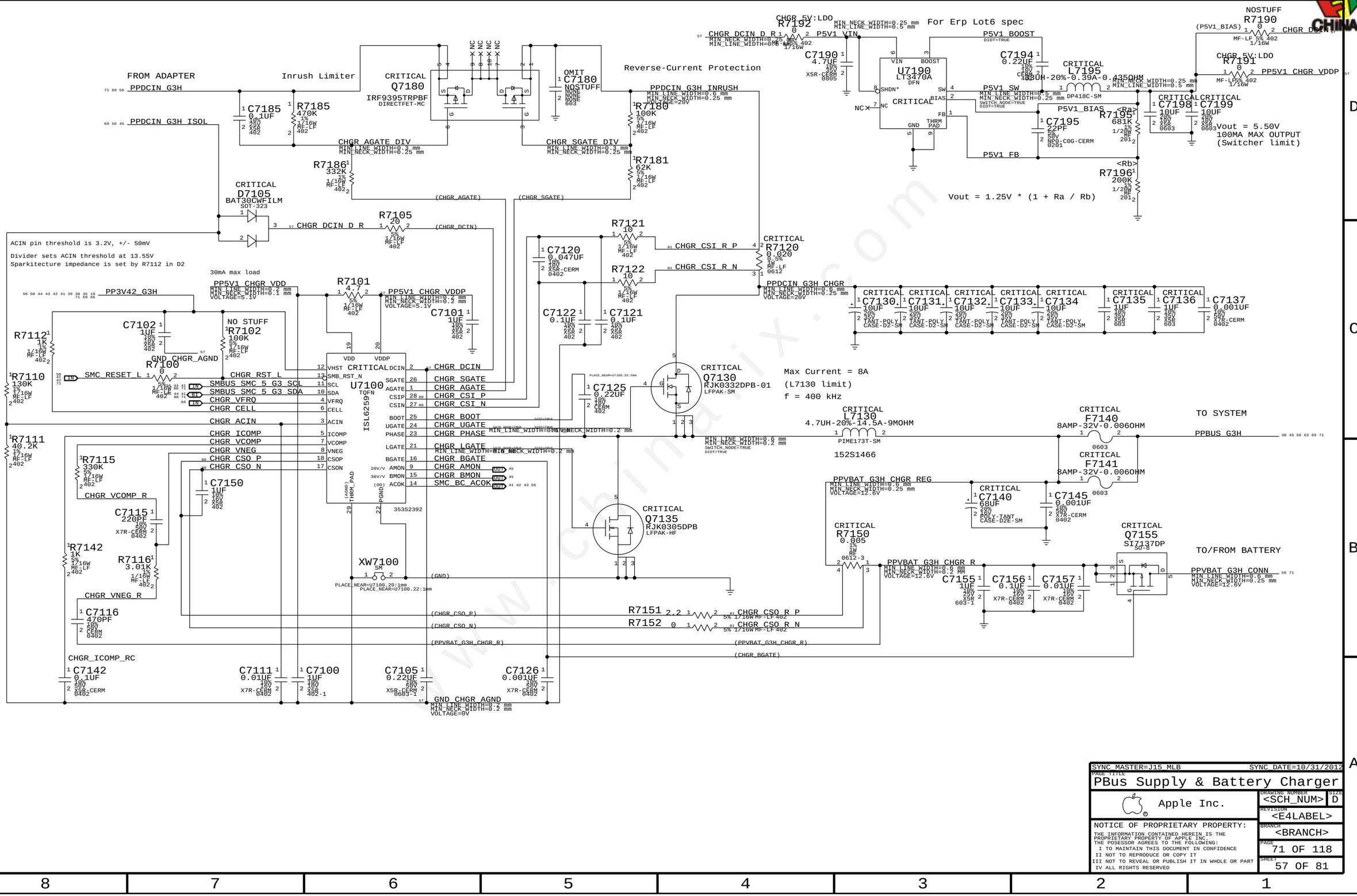

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

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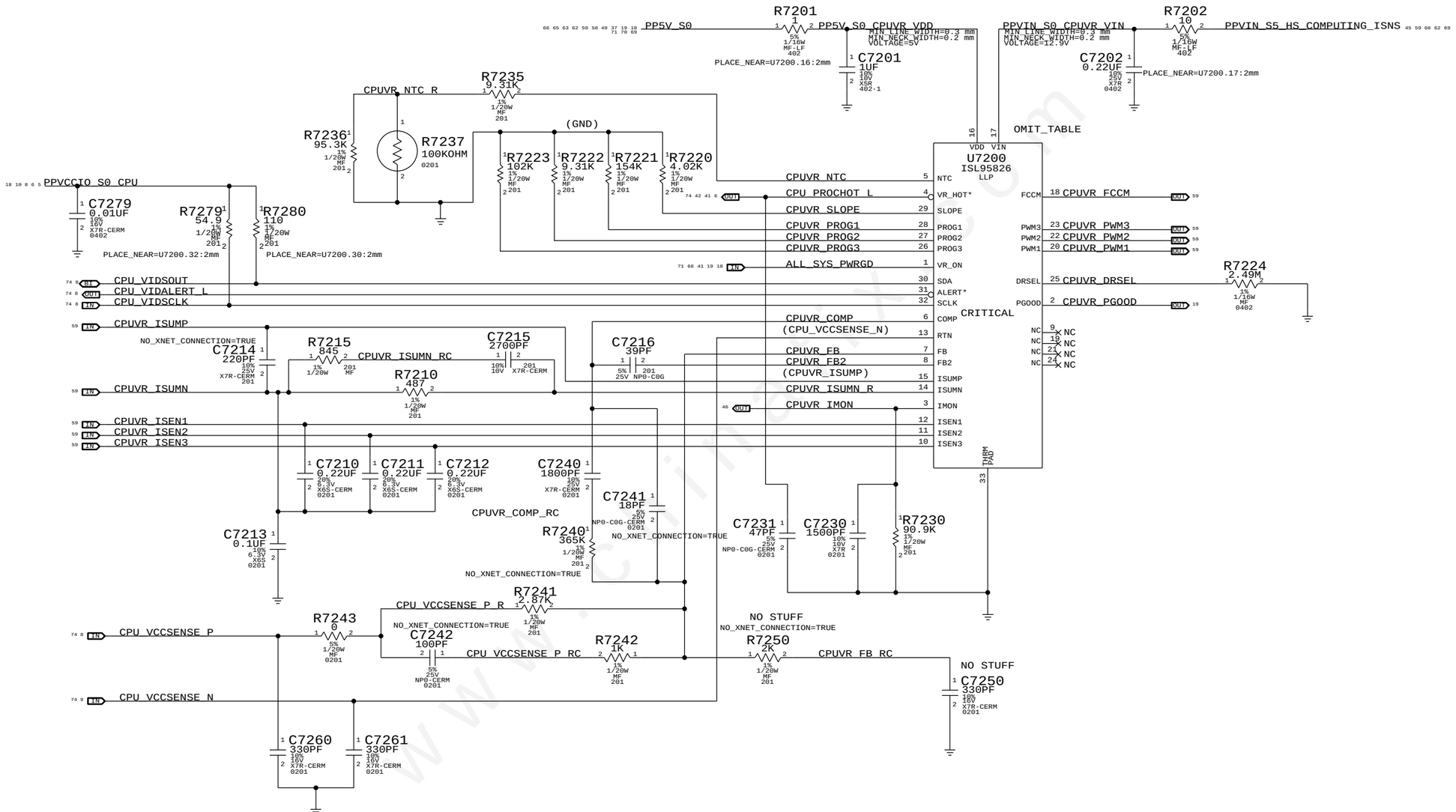
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	CPU VR12.5 VCC Regulator IC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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PP5V_S0
PPVIN_S5_HS_COMPUTING_ISNS
PHASE 1
PHASE 2
PHASE 3
U7310
U7320
U7330
FDMF6808N
PQFN
CRITICAL
353S3836
VDRV
R7311
R7321
R7331
0
C7310 1UF 10% 16V X6S-CERM 0402
C7320 1UF 10% 16V X6S-CERM 0402
C7330 1UF 10% 16V X6S-CERM 0402
C7311 0.22UF 10% 16V CERM 402
C7321 0.22UF 10% 16V CERM 402
C7331 0.22UF 10% 16V CERM 402
CPUVR_BOOT1_RC
CPUVR_BOOT2_RC
CPUVR_BOOT3_RC
CPUVR_BOOT1
CPUVR_BOOT2
CPUVR_BOOT3
CPUVR_PHASE1_K
CPUVR_PHASE2_K
CPUVR_PHASE3_K
CPUVR_PWM1
CPUVR_PWM2
CPUVR_PWM3
CPUVR_FCCM
BOOT
DISB*
GH
GL
PHASE
PWM
ZCD_EN*
THWN*
VCIN
NC
VIN
VSWH
CGND
PGND
CRITICAL
L7310
L7320
L7330
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
R7310 0.00075 1% 1W MF 0612
R7320 0.00075 1% 1W MF 0612
R7330 0.00075 1% 1W MF 0612
CPUVR_PHASE1
CPUVR_PHASE2
CPUVR_PHASE3
MIN_LINE_WIDTH=1.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE
SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH1
PPVCC_S0_CPU_PH2
PPVCC_S0_CPU_PH3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
CPUVR_ISNS1_P
CPUVR_ISNS2_P
CPUVR_ISNS3_P
R7312 2.2 5% 1/10W MF-LF 603
R7322 2.2 5% 1/10W MF-LF 603
R7332 2.2 5% 1/10W MF-LF 603
CPUVR_PH1_SNUB
CPUVR_PH2_SNUB
CPUVR_PH3_SNUB
NOSTUFF
C7312 0.001UF 10% 50V X7R-CERM 0402
C7322 0.001UF 10% 50V X7R-CERM 0402
C7332 0.001UF 10% 50V X7R-CERM 0402
CPUVR_ISNS1_N
CPUVR_ISNS2_N
CPUVR_ISNS3_N
R7314 3.9 1% 1/20W MF 201
R7324 3.9 1% 1/20W MF 201
R7334 3.9 1% 1/20W MF 201
CPUVR_ISUMN
CPUVR_ISUMP
CPUVR_ISEN1
CPUVR_ISEN2
CPUVR_ISEN3
NO_XNET_CONNECTION=TRUE
R7315 1K 1% 1/20W MF 201
R7325 1K 1% 1/20W MF 201
R7335 1K 1% 1/20W MF 201
R7316 10K 1% 1/20W MF 201
R7326 10K 1% 1/20W MF 201
R7336 10K 1% 1/20W MF 201
R7317 10K 1% 1/20W MF 201
R7318 10K 1% 1/20W MF 201
R7327 10K 1% 1/20W MF 201
R7328 10K 1% 1/20W MF 201
R7337 10K 1% 1/20W MF 201
R7338 10K 1% 1/20W MF 201
C7313 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7314 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7315 10UF 20% 16V X6S-CERM 0603
C7316 10UF 20% 16V X6S-CERM 0603
C7317 1UF 10% 16V X6S-CERM 0402
C7318 0.001UF 10% 50V X7R-CERM 0402
C7319 0.001UF 10% 50V X7R-CERM 0402
C7323 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7324 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7325 10UF 20% 16V X6S-CERM 0603
C7326 10UF 20% 16V X6S-CERM 0603
C7327 1UF 10% 16V X6S-CERM 0402
C7328 0.001UF 10% 50V X7R-CERM 0402
C7329 0.001UF 10% 50V X7R-CERM 0402
C7333 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7334 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7335 10UF 20% 16V X6S-CERM 0603
C7336 10UF 20% 16V X6S-CERM 0603
C7337 1UF 10% 16V X6S-CERM 0402
C7338 0.001UF 10% 50V X7R-CERM 0402
C7339 0.001UF 10% 50V X7R-CERM 0402
THESE TWO CAPS ARE FOR EMC
NOSTUFF CRITICAL
Additonal Input Bulk Caps
C7370 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7371 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7372 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7373 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7374 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7375 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7376 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7377 15UF 20% 16V TANT SM
C7378 15UF 20% 16V TANT SM
C7379 15UF 20% 16V TANT SM
C7380 15UF 20% 16V TANT SM
C7381 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7382 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7383 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7384 68UF 20% 16V POLY-TANT CASE-D2E-SM
PPVCC_S0_CPU
Vout = 1.85V max
95A max output
f = 450 kHz
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE TITLE
CPU VR12.5 VCC Power Stage
Apple Inc.
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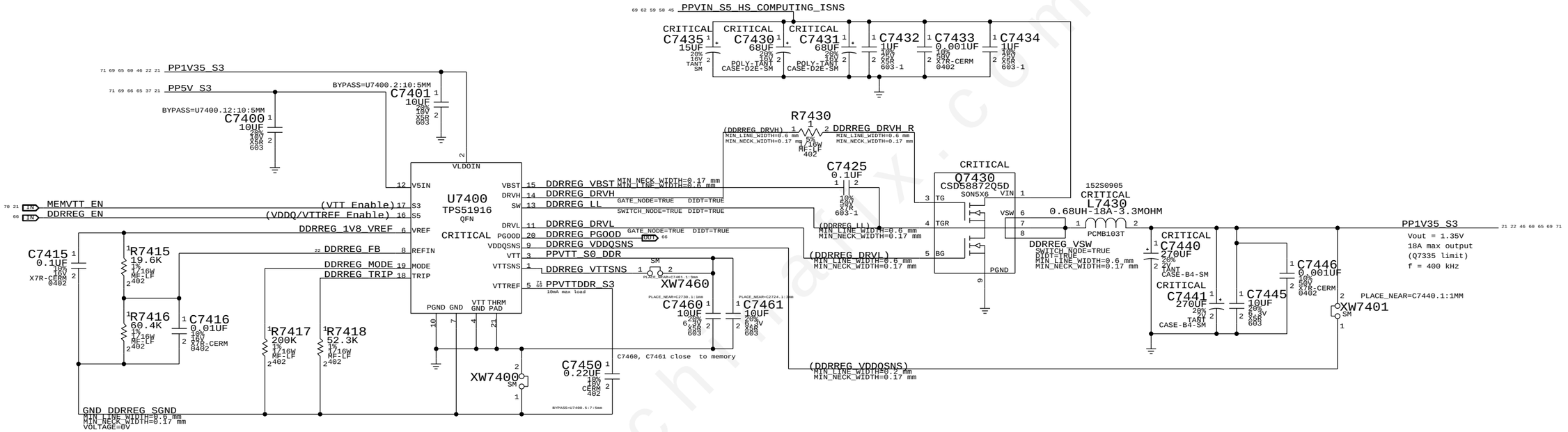
DDR3L (1V35 S3) REGULATOR



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: 1.35V DDR3L SUPPLY

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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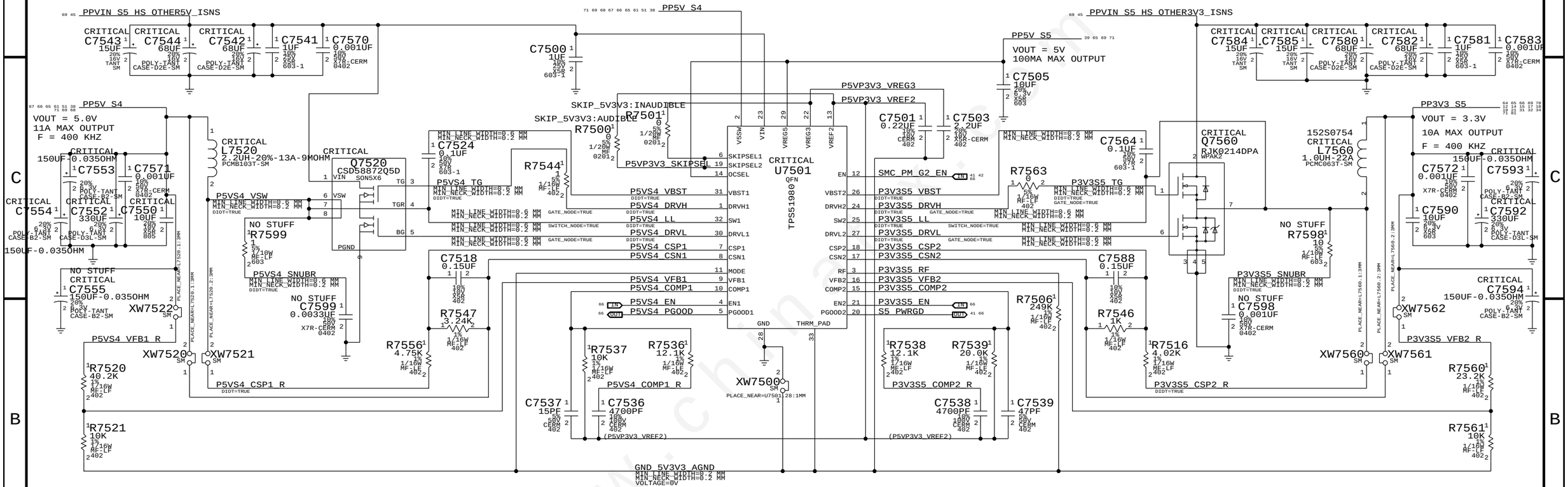

SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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1V05 S0 REGULATOR

PLACE_NEAR=U1100.AJ12:1MM
XW7601
SM
PP1V05 S0
P1V05S0 SENSE P
PLACE_NEAR=U1100.AK14:1MM
XW7602
SM
P1V05S0 SENSE N
Vout = 0.5V * (1 + Ra / Rb)
R7604 3.01K 1% 1/10W MF-LF 402
R7644 3.01K 1% 1/10W MF-LF 2402 <Ra>
R7605 2.74K 1% 1/10W MF-LF 402 <Rb>
R7645 2.74K 1% 1/16W MF-LF 2402 <Rb>
C7604 10PF 5% 50V C0G-CERM 0402
C7605 10PF 5% 50V C0G-CERM 0402
PPVIN S5 HS COMPUTING ISNS
PP5V S0
R7601 2.2 5% 1/10W MF-LF 402
C7601 10UF 20% 10V X5R 603
BYPASS=Q9800.14:16:5mm
P1V05S0 BOOT RC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
DIDT=TRUE
R7630 0 5% 1/10W MF-LF 603
C7630 1UF 10% 16V X5R 402
PP5V S0 P1V05S0 VCC
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
U7600
ISL95870
UTQFN
CRITICAL
VCC PVCC
EN FB SREF VO OCSET PGOOD RTN FSEL
BOOT UGATE PHASE LGATE
GND PGND
P1V05S0 VBST
P1V05S0 DRVH
P1V05S0 LL
P1V05S0 DRVL
P1V05S0 EN
P1V05S0 FB
P1V05S0 SREF
P1V05S0 VO
P1V05S0 OCSET
P1V05S0 PGOOD
P1V05S0 RTN
P1V05S0 FSEL
NO STUFF
R7603 0 5% 1/16W MF-LF 402
C7602 2.2UF 10% 16V X5R 603
C7603 0.047UF 10% 16V X7R-CERM 0402
P1V05S0 AGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
XW7600
SM
PLACE_NEAR=U7600.I:1mm
CRITICAL C7620 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7621 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7622 1000PF 5% 25V CERM 0402
BYPASS=Q7630.2:5:6mm
376S0953
CRITICAL
Q7630
RJK0214DPA
WPAK2
CRITICAL
L7630
0.68UH-25A-5.5MOHM
PCMC063T-SM
152S0955
PP1V05 S0 REG R2
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
CRITICAL R7640 0.001 1% 1W MF-1 0612
PP1V05 S0
Vout = 1.05V
12A MAX OUTPUT
f = 300 kHz
CRITICAL C7649 270UF 20% 2V TANT CASE-B4-SM
C7623 1000PF 5% 25V CERM 0402
PLACE_NEAR=L7630.2:1.5mm
CRITICAL C7648 270UF 20% 2V TANT CASE-B4-SM
P1V05S0 CS P
P1V05S0 CS N
R7641 1.2K 5% 1/16W MF-LF 402
C7640 0.0018UF 10% 50V X7R-CERM 0402
R7642 1.2K 5% 1/16W MF-LF 2402
(PCHVCCIOS0_OCSET)
(PCHVCCIOS0_VO)
OCP = R7641 x 8.5uA / R7640
OCP = 14.4A

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
1V05V POWER SUPPLY

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

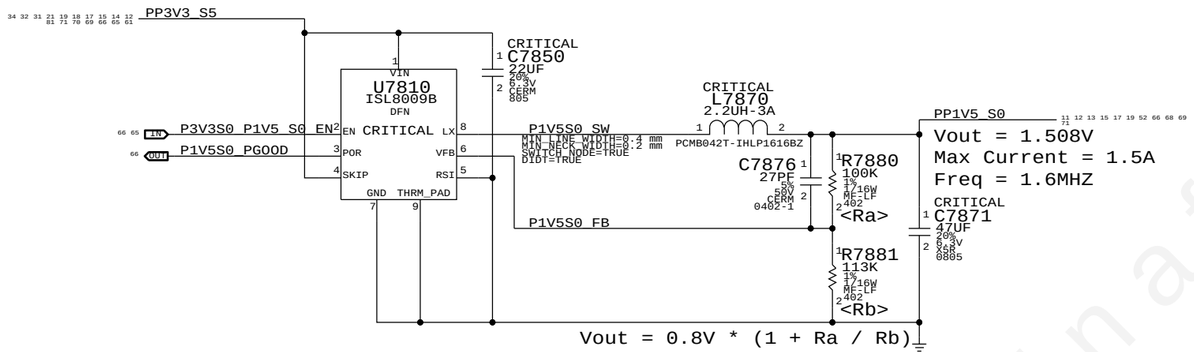
BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD

CRITICAL F7700 3AMP-32V-467 603-HF
PPBUS_G3H → PPBUS_S0_LCDBKLT_FUSED (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V)
R7700 0.025 1% 1W MTL 0612
PPBUS_SW_LCDBKLT_PWR (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V)
CRITICAL Q7706 FDC638APZ_SBMS001 SSOT6-HF
PPBUS_SW_BKL (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V)
C7700 1000PF 10% 16V X7R-CERM 0201
R7701 80.6K 1% 1/20W MF 201
NOSTUFF C7701 0.001UF 10% 50V CERM 402
152S1527 CRITICAL L7710 22UH-20%-2.4A-0.105OHM DEM8030C-SM
C7710 4.7UF 10% 25V X6S-CERM 0603
C7711 4.7UF 10% 25V X6S-CERM 0603
C7712 0.1UF 10% 25V X5R 402
PPBUS_S0_LCDBKLT_PWR_SW (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=45V, SWITCH_NODE=TRUE, DIDT=TRUE)
PLACE_NEAR=L7710.2:3MM
CRITICAL D7701 POWERDI-123 DFLS2100
PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE
C7715, C7716 SHOULD BE PLACED MIRRORED
C7718, C7719 SHOULD BE PLACED MIRRORED
CRITICAL C7715 2.2UF 10% 100V X7R 1210-1
CRITICAL C7716 2.2UF 10% 100V X7R 1210-1
CRITICAL C7718 2.2UF 10% 100V X7R 1210-1
CRITICAL C7719 2.2UF 10% 100V X7R 1210-1
C7717 1000PF 10% 100V X7R-CERM 0603
PPVOUT_S0_LCDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=55V)
PLACE_NEAR=D7701.K:3MM PLACE_NEAR=D7701.K:3MM PLACE_NEAR=R7708.1:5MM
PLACE_NEAR=D7701.K:5MM PLACE_NEAR=D7701.K:5MM
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
LCDBKLT_EN_L
PP5V_S0
R7743 0 5% 1/16W MF-LF 402
R7744 0 5% 1/16W MF-LF 402
VOLTAGE=5V MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM
PP5V_S0_BKLT_VDDA
PP5V_S0_BKLT_VDDD
R7702 63.4K 1% 1/16W MF-LF 402
C7740 1UF 10% 16V X5R 402-2
C7741 1UF 10% 16V X5R 402-2
GND_BKLT_SGND
R7740 1M 5% 1/20W MF 201
CRITICAL Q7701 SI7812DN PWRPK-1212-8
BKL_FET_CNTL_R (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)
R7703 0 5% 1/16W MF-LF 402
BKL_FET_CNTL (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)
R7708 18.2K 1% 1/16W MF-LF 402
R7709 150K 1% 1/16W MF-LF 402
U7701 LLP LP8548B1SQ_-03
BKL_SW (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)
BKL_FB
BKLT_SD
(PPBUS_S0_BKLT_PWR_R)
(PPBUS_S0_BKLT_PWR_F)
BKLT_SENSE_OUT
BKLT_EN_R
BKLT_ISET_KEYB
BKLT_KEYB1
BKLT_KEYB2
R7742 0 5% 1/20W MF 0201
EDP_IG_BKL_ON
NO STUFF C7742 33PF 5% 25V NPO-C0G 0201
R7747 0 5% 1/20W MF 0201
SMC_SYS_KBDLED
NO STUFF C7747 33PF 5% 25V NPO-C0G 0201
BKLT_PWM_KEYB
CRITICAL 353S4159
R7757 0 5% 1/20W MF 0201
BKLT_SDA_R → BKLT_SDA
R7758 0 5% 1/20W MF 0201
BKLT_SCL_R → BKLT_SCL
XW7700 SM
GND_BKLT_SGND (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)
BKLT:ENG R7723 10.2 1% 1/16W TF 402
BKLT:ENG R7724 10.2 1% 1/16W TF 402
KBDBKLT_RETURN1 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM)
KBDBKLT_RETURN2 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM)
R7741 31.6K 1% 1/20W MF 201
PPVOUT_BKLT_FB2 (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V)
KBDBKLT_SW (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)
PP5V_S0
NOSTUFF R7760 4.7K 5% 1/20W MF 201
NOSTUFF R7761 4.7K 5% 1/20W MF 201
BKLT_SCL_R
BKLT_SDA_R
C7750 1UF 10% 16V X5R 402-2
C7751 1UF 10% 16V X5R 402-2
GND_LCDBKLT_SGND
NOSTUFF C7752 1UF 10% 16V X5R 402-2
NOSTUFF R7752 0 5% 1/20W MF 0201
NOSTUFF C7753 1UF 10% 16V X5R 402-2
BKLT_FLT_RC
BKLT_FLT
NOSTUFF R7753 100K 5% 1/20W MF 201
U7750 LLP LP8549B1SP-03
NOSTUFF R7755 0 5% 1/20W MF 0201
LCD_FSS
R7780 0 5% 1/20W MF 0201
BKLT_SYNC
LCD_BKLT_PWM_R
EDP_IG_BKL_PWM
R7781 0 5% 1/20W MF 0201
BKL_EN_R_JERRY
SMBUS_PCH_DATA
R7782 0 5% 1/20W MF 0201
BKL_1_SDA
BKL_1_SCL
SMBUS_PCH_CLK
BKLT_ISET_LCD
R7754 27.4K 1% 1/16W MF-LF 402
R7756 10K 5% 1/16W MF-LF 402
CRITICAL APN353S4229
XW7701 SM
GND_LCDBKLT_SGND (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=0V)
BKL_ISEN1 → R7717 10.2 0.1% 1/16W TF 402 → LED_RETURN_1
BKL_ISEN2 → R7718 10.2 0.1% 1/16W TF 402 → LED_RETURN_2
BKL_ISEN3 → R7719 10.2 0.1% 1/16W TF 402 → LED_RETURN_3
BKL_ISEN4 → R7720 10.2 0.1% 1/16W TF 402 → LED_RETURN_4
BKL_ISEN5 → R7721 10.2 0.1% 1/16W TF 402 → LED_RETURN_5
BKL_ISEN6 → R7722 10.2 0.1% 1/16W TF 402 → LED_RETURN_6
(MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM)
R7783 0 5% 1/16W MF-LF 402
PP5V_S0_KBDLED_R (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V)
152S1701 CRITICAL L7720 10UH-20%-1.4A-0.17OHM PST041H-CDH46D14-SM
C7720 2.2UF 10% 25V X5R-CERM 603
C7721 2.2UF 10% 25V X5R-CERM 603
C7722 0.1UF 10% 16V X5R-CERM 0201
C7720, C7721 SHOULD BE PLACED MIRRORED
371S0572 CRITICAL D7720 SOD-123 RB160M-60G
XW7720 SM
PLACE_NEAR=D7720.K:2MM
C7726 1.0UF 10% 50V X7R 0805
C7727 1.0UF 10% 50V X7R 0805
C7723 1.0UF 10% 50V X7R 0805
C7724 1.0UF 10% 50V X7R 0805
C7725 0.001UF 10% 50V X7R-CERM 0402
C7723, C7724 SHOULD BE PLACED MIRRORED
PPVOUT_S0_KBDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V)

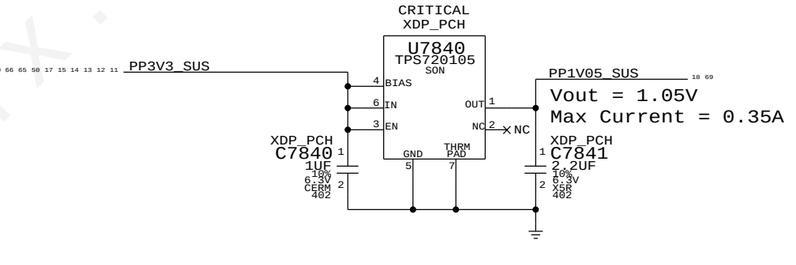
SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/13/2013
PAGE TITLE: LCD/KBD Backlight Driver
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 77 OF 118
SHEET: 63 OF 81

1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 78 OF 118

SHEET: 64 OF 81

3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per J45 Power Budget rev5

PP3V3_S5 → R8002 220K → P3V3S4_EN_L → R8000 47K → P3V3S3_S4 → PP3V3_S4
C8009 0.033UF
C8000 0.01UF
Q8002 DMN5L06VK-7 SOT-563
S4_PWR_EN

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70-6L

PP3V3_S5 → R8012 47K → P3V3S3_EN_L → R8010 39K → P3V3S3_SS → PP3V3_S3
C8011 0.033UF
C8010 0.01UF
Q8012 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
P3V3S3_EN

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

SSD_PWR_EN:GPIO
SSD_PWR_EN → R8073 0 (0201 1/20W 5% MF) → SSD_PWR_EN_S0 → R8074 0 (0201 1/20W 5% MF) → PM_SLP_S3_BUF_L
SSD_PWR_FET_EN

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70-6L

PP5V_S4 → R8052 200K → P5VS3_EN_L → R8050 5.1K → P5VS3_SS → PP5V_S3
C8051 0.033UF
C8050 0.01UF
Q8052 DMN5L06VK-7 SOT-563
P5VS3_EN

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5 → C8001 0.1UF → U8001 SLG5AP1438V TDFN CRITICAL (VDD, CAP, ON, GND, D, S)
P1V35CPU_SLEW_CTL
CPUVDDQ_EN
C8002 0.018UF
Slew rate : 0.8V/ms = 19.75nF

PP1V35_S3

Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R

XW8005 SM
PP1V35_S3RS0_FET → PP1V35_S3RS0_CPUDDR
NC_ISNS_CPUDDRN
NC_ISNS_CPUDDRP

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70-6L

PP3V3_S5 → R8022 100K → P3V3SUS_EN → R8020 12K → P3V3SUS_SS → PP3V3_SUS
C8021 0.033UF
C8020 0.01UF
Q8002 DMN5L06VK-7 SOT-563
PM_SLP_SUS

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm
CRITICAL
Q8070
SI7615DN
PWRPK-1212-8

PP3V3_S5 → R8072 47K → P3V3_SSD_EN_L → R8070 33K → P3V3_SSD_SS → PP3V3_S0SW_SSD_R
C8071 0.033UF
C8070 0.01UF
Q8072 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
SSD_PWR_FET_EN

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK-1212-8

PP5V_S4 → R8062 270K → P5V0S0_EN_L → R8060 6.2K → P5V0S0_SS → PP5V_S0
C8061 0.12UF
C8060 0.47UF
Q8052 DMN5L06VK-7 SOT-563
P5VS0_EN

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch

U8030
TPS22924
CSP
APN 353S2741

PP3V3_S5 → A2 VIN, B2 VIN → VOUT A1, VOUT B1 → PP3V3_S0
Max Current = 2A
P3V3S0_P1V5_S0_EN → C2 ON
GND → C1
C8030 1UF

U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 80 OF 118
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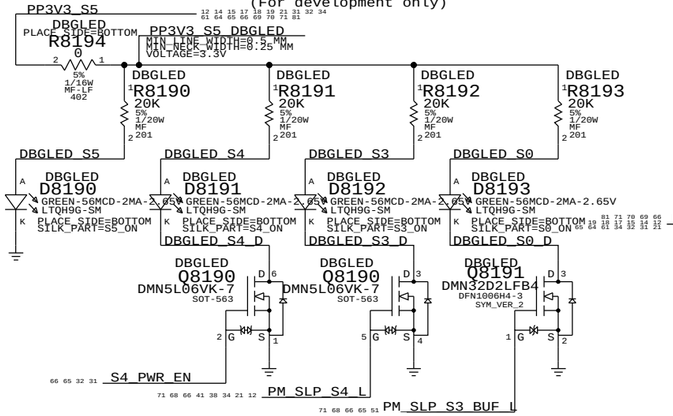
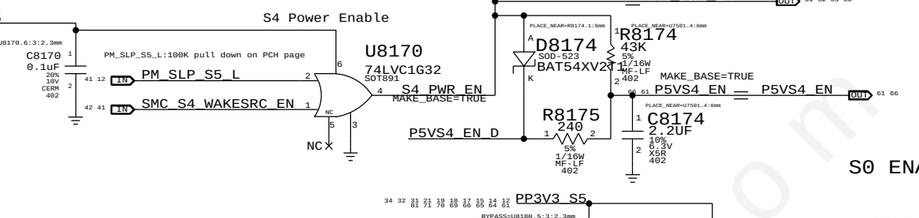
Power State Debug LEDs
(For development only)



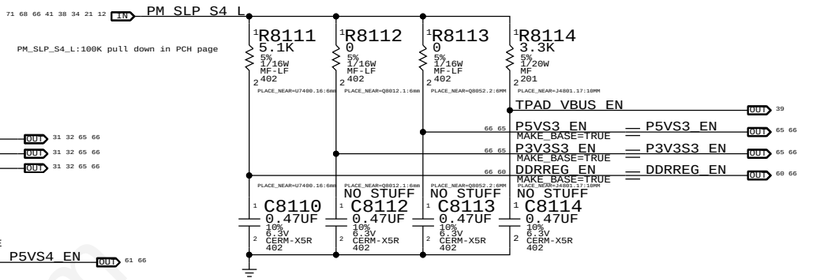
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

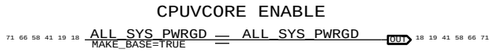
S4 Power Enable



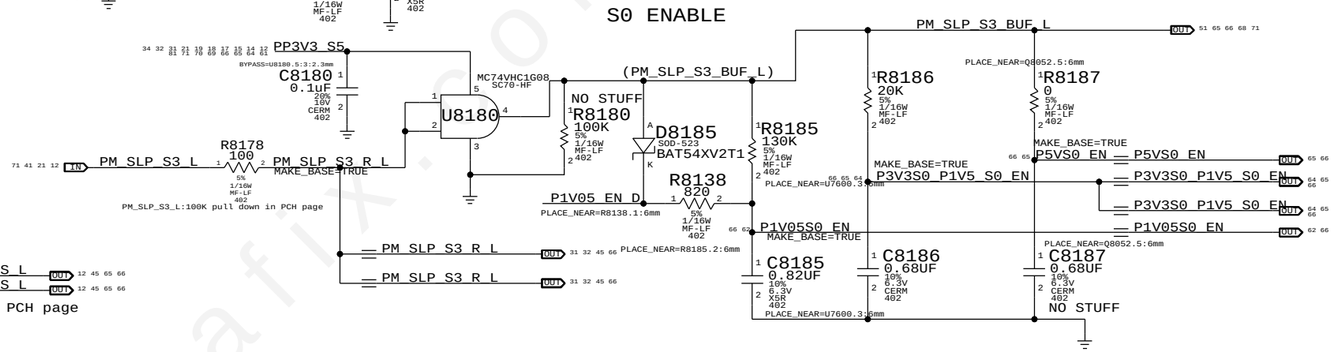
S3 ENABLE



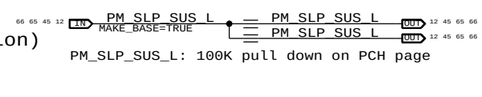
CPUVCORE ENABLE



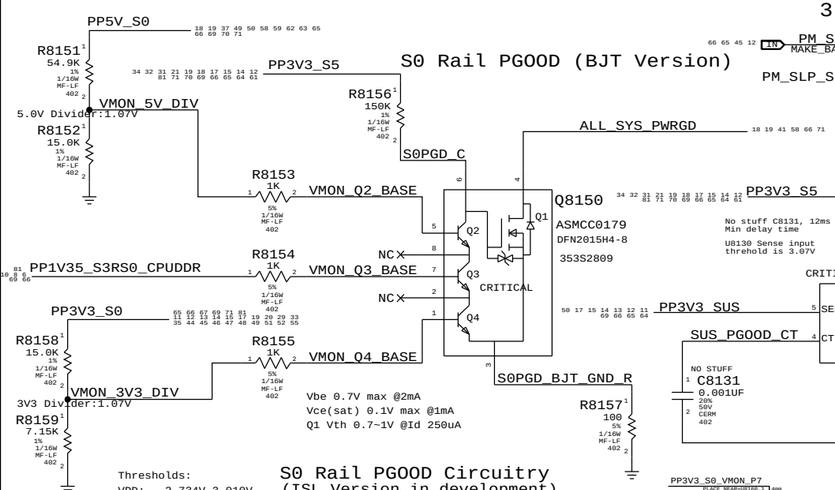
S0 ENABLE



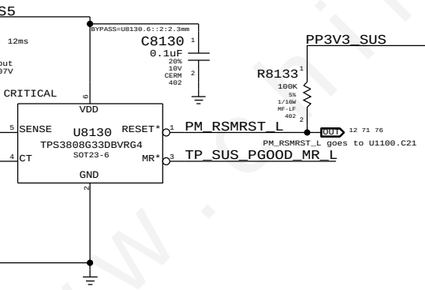
3.3V SUS Enable



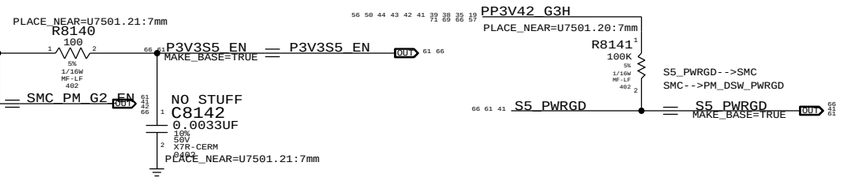
S0 Rail PGOOD (BJT Version)



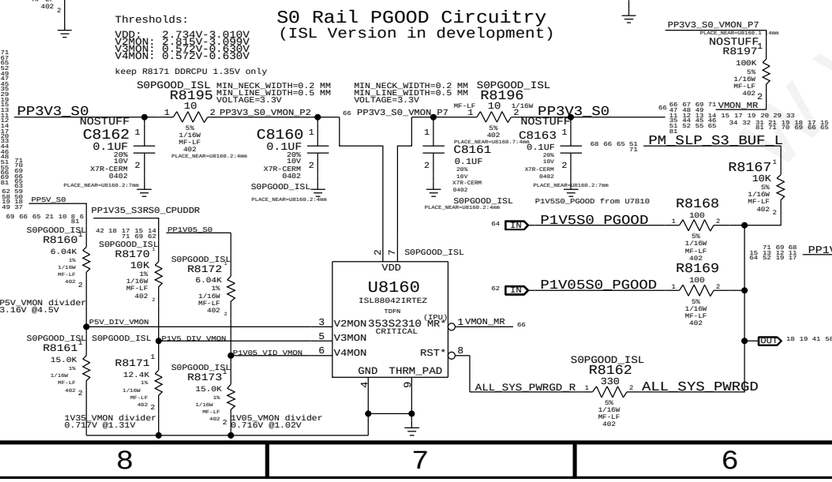
3.3V SUS Detect



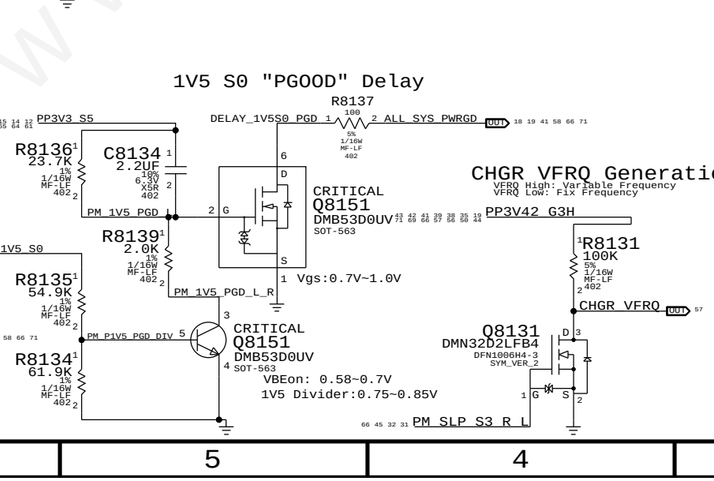
S5 Rail Enables & PGOOD



S0 Rail PGOOD Circuitry
(ISL Version in development)



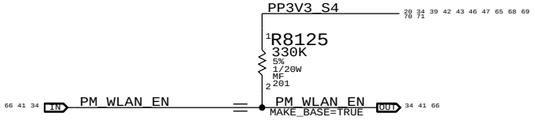
1V5 S0 "PGOOD" Delay



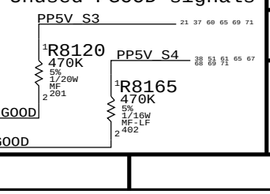
CHGR VFRQ Generation

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.



Unused PGOOD signals



SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 81 OF 118
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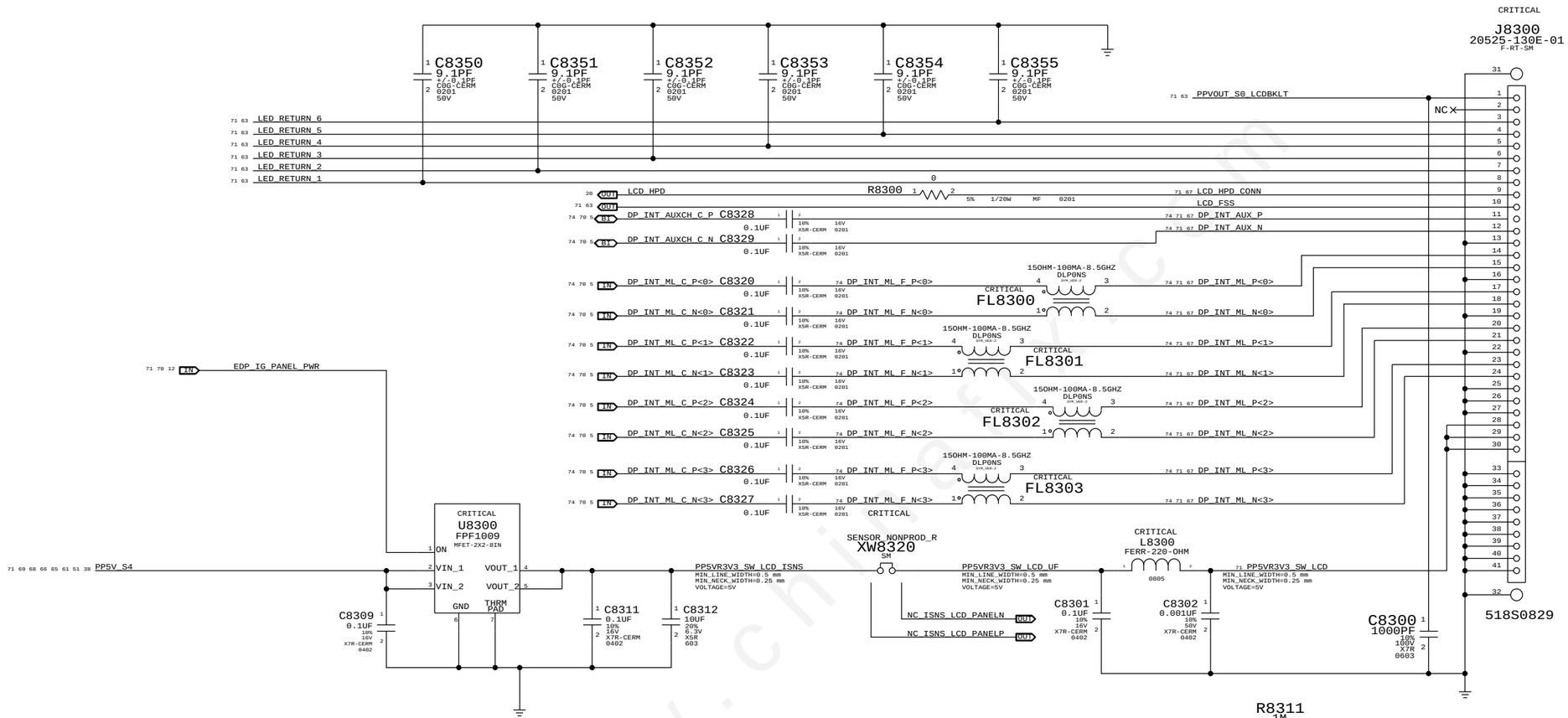
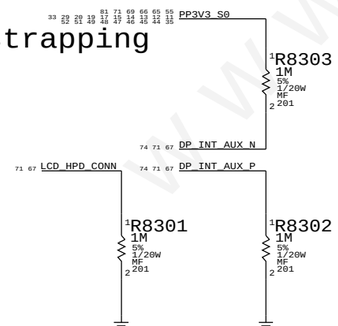
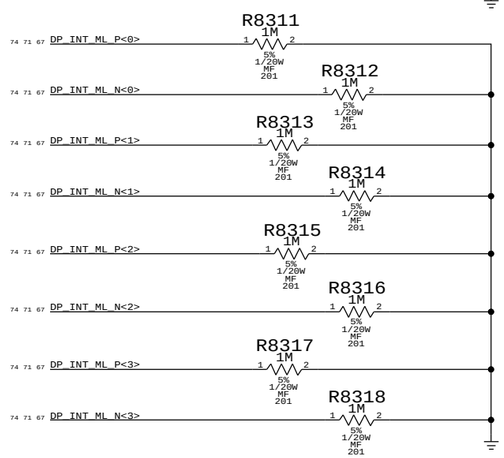
LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping





SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 83 OF 118

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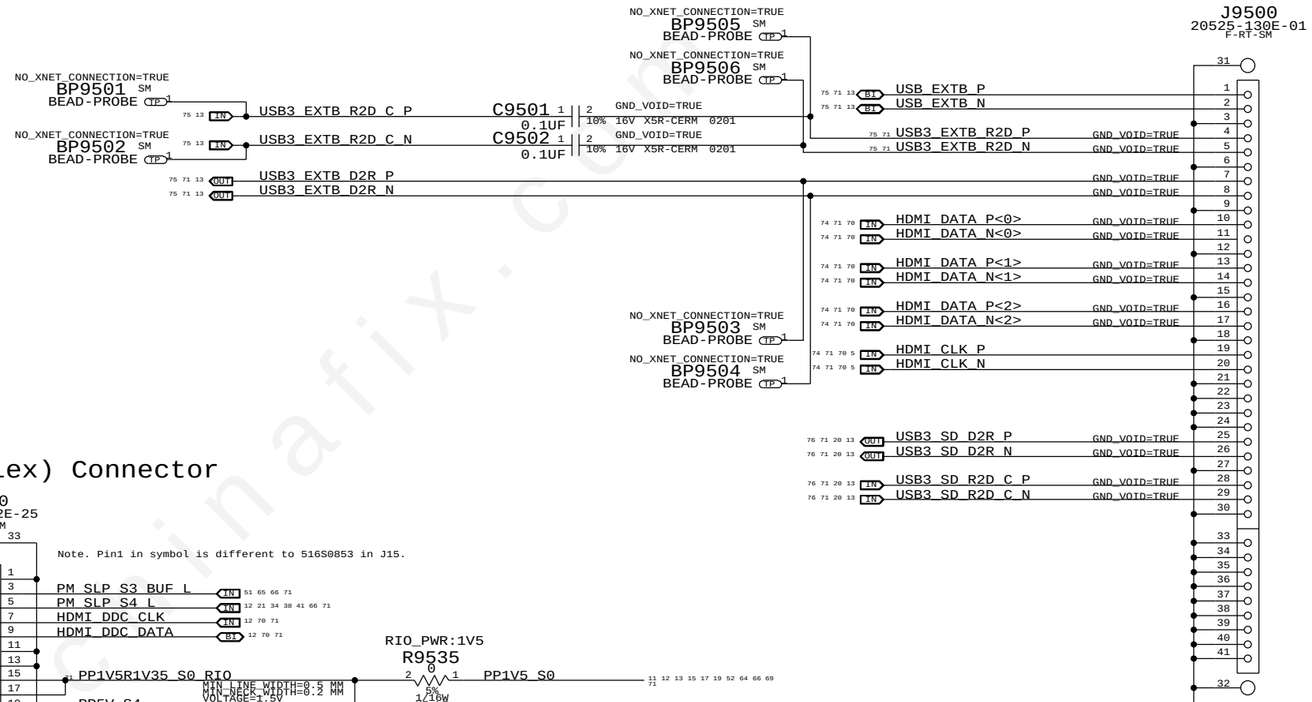
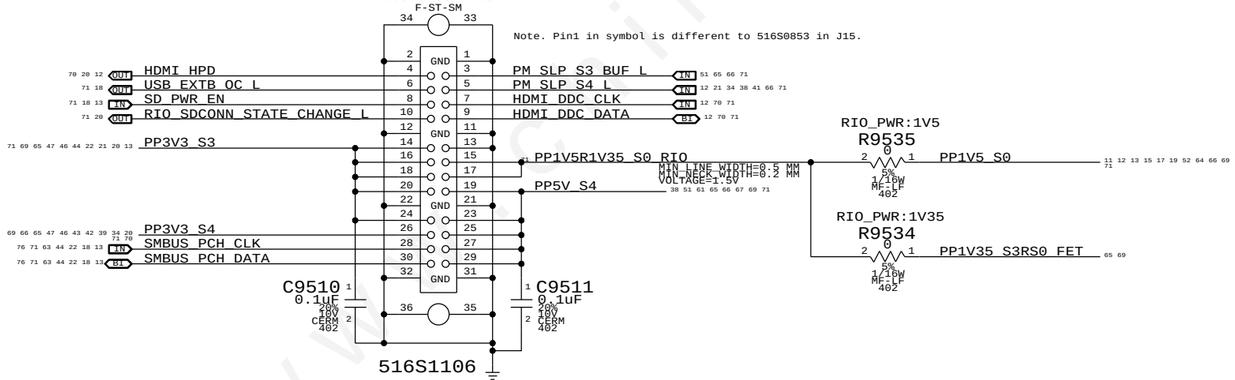
Wire-to-Board (Micro-coax) Connector



Board-to-Board (Flex) Connector



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
RIO Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 95 OF 118
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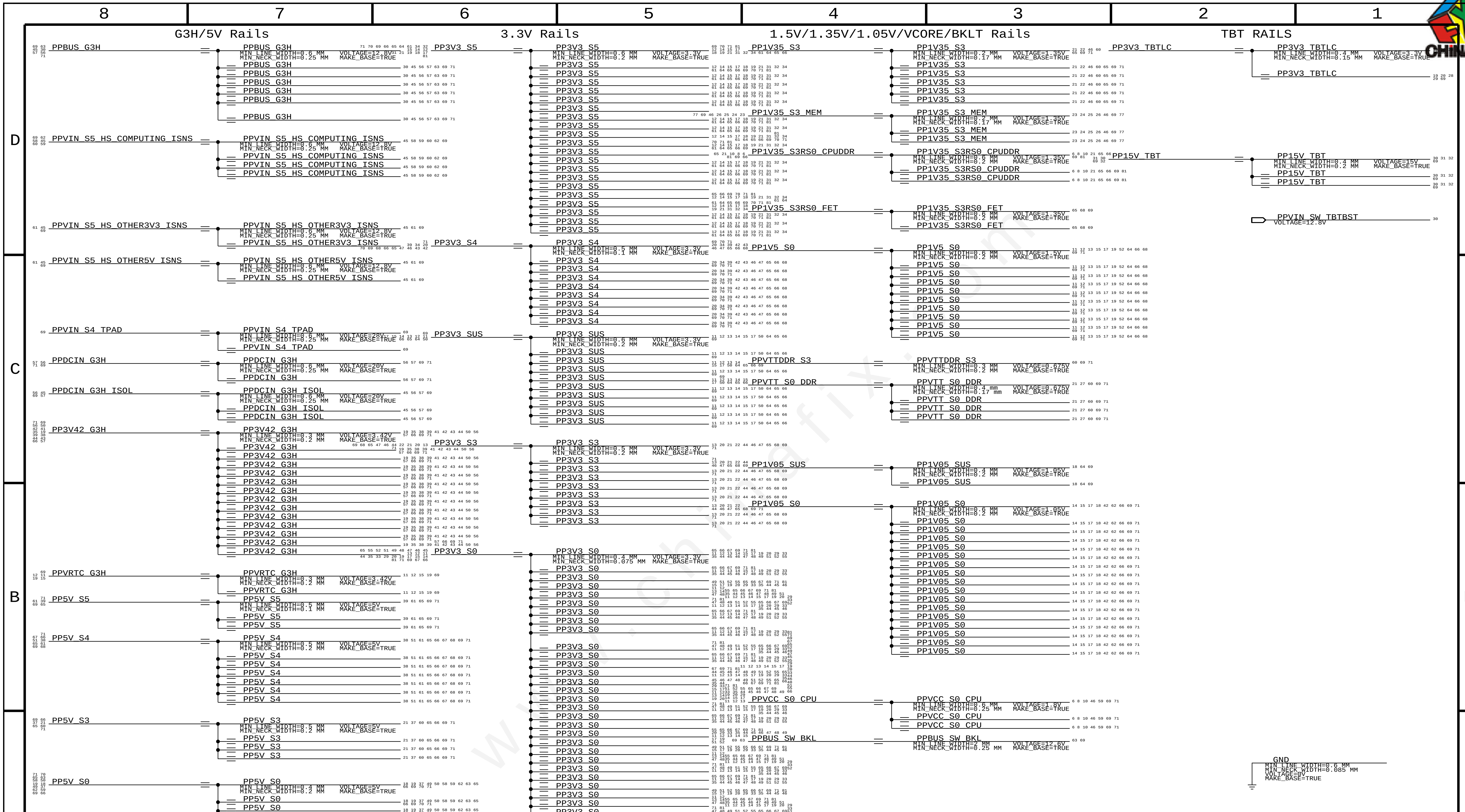

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

Power Aliases

DRAWING NUMBER <SCH_NUM> SIZE D

Apple Inc.

REVISION <E4LABEL>

BRANCH <BRANCH>

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Display Aliases

71 70 67 12	EDP_IG_PANEL_PWR	MAKE_BASE=TRUE	EDP_IG_PANEL_PWR	12 67 70 71
71 70 63 12	EDP_IG_BKL_ON	MAKE_BASE=TRUE	EDP_IG_BKL_ON	12 63 70 71
70 63 12	EDP_IG_BKL_PWM	MAKE_BASE=TRUE	EDP_IG_BKL_PWM	12 63 70
74 67 5	DP_INT_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLP<3..0>	
74 67 5	DP_INT_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLN<3..0>	
74 70 67 5	DP_INT_AUXCH_C_P	MAKE_BASE=TRUE	DP_INT_AUXCH_C_P	5 67 70 74
74 70 67 5	DP_INT_AUXCH_C_N	MAKE_BASE=TRUE	DP_INT_AUXCH_C_N	5 67 70 74
70 28 12	DP_TBTSNK0_HPD	MAKE_BASE=TRUE	DP_TBTSNK0_HPD	12 28 70
74 28 5	DP_TBTSNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLP<3..0>	
74 28 5	DP_TBTSNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLN<3..0>	
74 70 28 12	DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE	DP_TBTSNK0_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE	DP_TBTSNK0_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK0_DDC_DATA	MAKE_BASE=TRUE	DP_TBTSNK0_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK0_DDC_CLK	MAKE_BASE=TRUE	DP_TBTSNK0_DDC_CLK	12 33 70
70 28 12	DP_TBTSNK1_HPD	MAKE_BASE=TRUE	DP_TBTSNK1_HPD	12 28 70
74 28 5	DP_TBTSNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLP<3..0>	
74 28 5	DP_TBTSNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLN<3..0>	
74 70 28 12	DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK1_DDC_DATA	MAKE_BASE=TRUE	DP_TBTSNK1_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK1_DDC_CLK	MAKE_BASE=TRUE	DP_TBTSNK1_DDC_CLK	12 33 70
70 68 20 12	HDMI_HPD	MAKE_BASE=TRUE	HDMI_HPD	12 20 68 70
74 71 68	HDMI_DATA_P<0..2>	MAKE_BASE=TRUE	TP_DP_IG_D_MLP<2..0>	5
74 71 68	HDMI_DATA_N<0..2>	MAKE_BASE=TRUE	TP_DP_IG_D_MLN<2..0>	5
74 71 70 68 5	HDMI_CLK_P	MAKE_BASE=TRUE	HDMI_CLK_P	5 68 70 71 74
74 71 70 68 5	HDMI_CLK_N	MAKE_BASE=TRUE	HDMI_CLK_N	5 68 70 71 74
71 70 68 12	HDMI_DDC_CLK	MAKE_BASE=TRUE	HDMI_DDC_CLK	12 68 70 71
71 70 68 12	HDMI_DDC_DATA	MAKE_BASE=TRUE	HDMI_DDC_DATA	12 68 70 71

CPU signals

70 60 21	MEMVTT_EN	MAKE_BASE=TRUE	MEMVTT_EN	21 60 70

Thunderbolt Signals Through PEG

74 28 5	PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<3..0>	OUT
74 28 5	PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<3..0>	OUT
74 28 5	PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<3..0>	IN
74 28 5	PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<3..0>	IN

Unused PEG Lanes

5	TP_PEG_D2RP<15..4>	MAKE_BASE=TRUE	=PEG_D2R_P<15..4>
5	TP_PEG_D2RN<15..4>	MAKE_BASE=TRUE	=PEG_D2R_N<15..4>
5	TP_PEG_R2D_CP<15..4>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..4>
5	TP_PEG_R2D_CN<15..4>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..4>

70 49	PP3V3_S3_FAN_CTL		PP3V3_S3_FAN_CTL MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=3.3V MAKE_BASE=TRUE	49 70

RA201
0
1 2
5%
1/20W
MF
0201
PP3V3_S5
12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 71 81

RA202
0
1 2
5%
1/20W
MF
0201
PP3V3_S4
20 34 39 42 43 46 47 65 66 68 69 71

NOSTUFF

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
14	DPMUX_UC_IRQ
11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L

		VOLTAGE	MAKE_BASE		
77 74 70 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70 74
77 74 70 24 23 22	PP0V75_S3_MEM_VREFCA_A	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFCA_B	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B	22 25 26 70 74

65 63 62 59 58 50 49 37 19 18 71 69 66 PP5V_S0

XWA202
SM
1 2
PP5V_S0_AUDIO_AMP_L
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
53

XWA203
SM
1 2
PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
53

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

Apple Inc.

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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 76
TRUE	PCIE_AP_D2R_PI_P	34 76
TRUE	PCIE_AP_R2D_N	34 76
TRUE	PCIE_AP_R2D_P	34 76
TRUE	PCIE_CLK100M_AP_CONN_N	34 76
TRUE	PCIE_CLK100M_AP_CONN_P	34 76
TRUE	PCIE_WAKE_L	12 34 36 76
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 75
TRUE	USB_BT_CONN_P	34 75
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 79
TRUE	MIPI_CLK_CONN_P	37 79
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 79
TRUE	MIPI_DATA_CONN_P	37 79
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 80
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 80
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 68 70 74
TRUE	HDMI_CLK_P	5 68 70 74
TRUE	HDMI_DATA_N<0>	68 70 74
TRUE	HDMI_DATA_N<1>	68 70 74
TRUE	HDMI_DATA_N<2>	68 70 74
TRUE	HDMI_DATA_P<0>	68 70 74
TRUE	HDMI_DATA_P<1>	68 70 74
TRUE	HDMI_DATA_P<2>	68 70 74

TRUE	USB3_SD_D2R_N	13 20 68 76
TRUE	USB3_SD_D2R_P	13 20 68 76
TRUE	USB3_SD_R2D_C_N	13 20 68 76
TRUE	USB3_SD_R2D_C_P	13 20 68 76
TRUE	USB3_EXTB_D2R_N	13 68 75
TRUE	USB3_EXTB_D2R_P	13 68 75
TRUE	USB3_EXTB_R2D_N	68 75
TRUE	USB3_EXTB_R2D_P	68 75
TRUE	USB_EXTB_N	13 68 75
TRUE	USB_EXTB_P	13 68 75
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 68
TRUE	PP1V5R1V35_S0_RIO	68
TRUE	HDMI_DDC_CLK	12 68 70
TRUE	HDMI_DDC_DATA	12 68 70
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 18 22 44 63 68 76
TRUE	SMBUS_PCH_DATA	13 18 22 44 63 68 76
TRUE	PM_SLP_S3_BUF_L	51 65 66 68
TRUE	PM_SLP_S4_L	12 21 34 38 41 66 68
TRUE	PP3V3_S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S4	5X 38 51 61 65 66 67 68 69
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 68
TRUE	USB_EXTB_OC_L	18 68
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 50
TRUE	LPCPLUS_RESET_L	20 50 76
TRUE	LPC_AD<0>	13 41 50 76
TRUE	LPC_AD<1>	13 41 50 76
TRUE	LPC_AD<2>	13 41 50 76
TRUE	LPC_AD<3>	13 41 50 76
TRUE	LPC_CLK33M_LPCPLUS	19 50 76
TRUE	LPC_FRAME_L	13 41 50 76
TRUE	LPC_PWRDWN_L	12 20 41 50
TRUE	LPC_SERIRQ	13 41 50
TRUE	PM_CLKRUN_L	12 41 50
TRUE	PP5V_S0	10 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_ROMBOOT	42 50
TRUE	SMC_RX_L	41 42 50
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TDI	41 42 50
TRUE	SMC_TDO	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SMC_TX_L	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50
TRUE	SPI_ALT_CS_L	50
TRUE	SPI_ALT_MISO	50
TRUE	SPI_ALT_MOSI	50
TRUE	TP_SMC_MD1	50
TRUE	TP_SMC_TRST_L	50
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	39
TRUE	Z2_MOSI	39
TRUE	Z2_MISO	39
TRUE	Z2_SCLK	39
TRUE	Z2_HOST_INTN	39
TRUE	Z2_CLKIN	39
TRUE	Z2_KEY_ACT_L	39
TRUE	PSOC_F_CS_L	39
TRUE	PICKB_L	39
TRUE	PSOC_MOSI	39
TRUE	PSOC_MISO	39
TRUE	PSOC_SCLK	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 80
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 80
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_T101_COM_1	
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S5	39 61 65 69 71
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	51 55
TRUE	AUD_HP_PORT_R	51 55
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	51 55
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	AUD_CONN_SLEEVE_XW	4X 54 55
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 81
TRUE	SPKRCONN_L_OUT_P	53 55 81
TRUE	SPKRCONN_SL_OUT_N	53 55 81
TRUE	SPKRCONN_SL_OUT_P	53 55 81
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 81
TRUE	SPKRCONN_R_OUT_P	53 55 81
TRUE	SPKRCONN_SR_OUT_N	53 55 81
TRUE	SPKRCONN_SR_OUT_P	53 55 81
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 80
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 80
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 74
TRUE	DP_INT_AUX_P	67 74
TRUE	DP_INT_ML_N<0>	67 74
TRUE	DP_INT_ML_N<1>	67 74
TRUE	DP_INT_ML_N<2>	67 74
TRUE	DP_INT_ML_N<3>	67 74
TRUE	DP_INT_ML_P<0>	67 74
TRUE	DP_INT_ML_P<1>	67 74
TRUE	DP_INT_ML_P<2>	67 74
TRUE	DP_INT_ML_P<3>	67 74
TRUE	LCD_FSS	63 67
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	63 67
TRUE	LED_RETURN_2	63 67
TRUE	LED_RETURN_3	63 67
TRUE	LED_RETURN_4	63 67
TRUE	LED_RETURN_5	63 67
TRUE	LED_RETURN_6	63 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	63 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 66
TRUE	PPVTT_S0_DDR	21 27 60 69
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 81
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	PP5V_S0	10 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	PP5V_S3	21 37 60 65 66 69
TRUE	PP5V_S5	39 61 65 69 71
TRUE	PPBUS_G3H	30 45 56 57 63 69
TRUE	PPDCIN_G3H	56 57 69
TRUE	PPVCC_S0_CPU	6 8 10 46 59 69
TRUE	PPVTTDDR_S3	60 69
TRUE	PP3V3_S0SW_SSD	35 46 69
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 66 68 69
TRUE	PP1V35_S3	21 22 46 60 65 69

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 74
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 74
TRUE	XDP_CPU_TDO	6 18 74
TRUE	XDP_CPUPCH_TRST_L	6 18 74
TRUE	XDP_CPU_TMS	6 18 74
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 74
TRUE	XDP_CPU_PRDY_L	6 18 74
TRUE	PM_RSMRST_L	12 66 76
TRUE	PM_PCH_PWROK	12 19 76
TRUE	PM_SYSRST_L	12 19 41 76
TRUE	CPU_CFG<3>	6 18 74
TRUE	PP1V05_S0	14 15 17 18 42 62 66 69
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 76
TRUE	ALL_SYS_PWRGD	18 19 41 58 66
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 76
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 67 70
TRUE	EDP_IG_BKL_ON	12 63 70

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PAGE TITLE: Functional Test Points

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NC NO_TESTs

PCH

	NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP

NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP

NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP

NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	TRUE	TRUE	NC_USB_6N
NC_USB_6P	TRUE	TRUE	NC_USB_6P
NC_USB_7N	TRUE	TRUE	NC_USB_7N
NC_USB_7P	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	TRUE	TRUE	NC_USB_IRP

NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L

NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN

NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

	NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT

TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN

NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP

NC_PCIE_CLK100M_GPUN	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC_USB_4N	TRUE	TRUE	NC_USB_4N
NC_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	28 74
TRUE	PCIE_TBT_R2D_N<3..0>	28 74
TRUE	PCIE_TBT_D2R_C_P<3..0>	28 74
TRUE	PCIE_TBT_D2R_C_N<3..0>	28 74

TRUE	DMI_S2N_P<3..1>	5 12 74
TRUE	DMI_S2N_N<3..1>	5 12 74
TRUE	DMI_N2S_P<3..1>	5 12 74
TRUE	DMI_N2S_N<3..1>	5 12 74

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_R2D_C_P<1>	SM	BEAD-PROBE	BPA535 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<1>	SM	BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	SM	BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 72
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
1125 DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
1126 DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
1131 CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
1137 CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
1138 CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
1139 CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
1154 XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
1155 XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
1156 XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
1158 CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTI	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
1165 CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
1166 CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
1143 CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
1144 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
1145 CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
1146 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
1160 PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 70
1161 PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 70
1162	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 72
1163	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 72
1164 PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 72
1165 PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 72
1166	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 70
1167	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1243 DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 67 70
1244 DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 67 70
1165	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
1167	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
1231	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67
1232	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67
1234	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
1233	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
1246 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 67 70
1245 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 67 70
1177 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 71
1176 DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 71

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1213 HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	68 70 71
1214 HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	68 70 71
1215 HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 68 70 71
1216 HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 68 70 71
1235 DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 70
1236 DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 70
1237	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
1238	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
1239 DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 70
1240 DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 70
1241	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
1242	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
1222 TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
1224 TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
1221	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
1223	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
1227 TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
1226 TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
1225	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
1228	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 72
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 72
T277	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 72
T277	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 72
T299	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 72
T299	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 72
T300	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 72
T301	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 72
T213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_85D	USB	USB_EXTA_P	13 38
	USB_85D	USB	USB_EXTA_N	13 38
T245	USB_85D	USB	USB_EXTA_MUXED_P	38
T247	USB_85D	USB	USB_EXTA_MUXED_N	38
T243	USB_85D	USB	USB_LT1_P	38
T244	USB_85D	USB	USB_LT1_N	38
	USB_85D	USB	NC_USB_EXTCP	13 72
	USB_85D	USB	NC_USB_EXTCN	13 72
T233	USB_85D	USB	NC_USB_SDP	13 72
T235	USB_85D	USB	NC_USB_SDN	13 72
T227	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
T274	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_85D	USB	NC_USB_SMCP	72
	USB_85D	USB	NC_USB_SMCN	72
T281	USB_85D	USB	NC_USB_6P	13 72
T281	USB_85D	USB	NC_USB_6N	13 72
T281	USB_85D	USB	NC_USB_7P	13 72
T281	USB_85D	USB	NC_USB_7N	13 72
	USB_85D	USB	USB_EXTB_P	13 68 71
	USB_85D	USB	USB_EXTB_N	13 68 71
T250	USB_85D	USB	NC_USB_EXTDP	13 72
T250	USB_85D	USB	NC_USB_EXTDN	13 72
	USB_85D	USB	USB_BT_P	13 34
	USB_85D	USB	USB_BT_N	13 34
	USB_85D	USB	USB_BT_CONN_P	34 71
	USB_85D	USB	USB_BT_CONN_N	34 71
T281	USB_85D	USB	NC_USB_IRP	13 72
T281	USB_85D	USB	NC_USB_IRN	13 72
T281	USB_85D	USB	USB_TPAD_P	13 39
T281	USB_85D	USB	USB_TPAD_N	13 39
T302	USB_85D	USB	USB_TPAD_R_P	39
T303	USB_85D	USB	USB_TPAD_R_N	39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T222 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
T223 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
T267	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T265	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T233 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
T222 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
T266	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
T265	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
T222 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 68 71
T223 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 68 71
T267	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T265	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T222 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	68 71
T223 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	68 71
T266	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 68
T265	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 68
T281 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
T281 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
T267	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
T265	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
T281 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
T281 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
T266	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
T265	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T250 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T254	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T253 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
T251 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T256	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41 50 71
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41 50 71
LPC_RESET_L	LPC_45S	LPC	LPCPLUS_RESET_L	20 50 71
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 22 44 63 68 71
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 22 44 63 68 71
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 50
SPI_CLK	SPI_45S	SPI	SPI_CLK	50
	SPI_45S	SPI	SPI_MOSI_R	13 50
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	50
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 50
	SPI_45S	SPI	SPI_CS0_R_L	13 50
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	50
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 68 71
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 68 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 71
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
[180]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
[180]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
[179]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 71
[179]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 71
[175] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
[175] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
[174]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
[174]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
[176] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
[176] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
[33]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
[33]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 50 71
[240]	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
[243] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[254] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[255] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[255] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[257] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
[180]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 71
[179]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 71
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
[33]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
[33]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
[281] PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
[281]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
[181] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[181] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[181] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[181] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[180] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 66 71
[180] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 71
[181] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[181] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[180] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 71
[181] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 71
[180] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
[180] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
[180] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 71
[179] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[135] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 35
[136] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 35
[138] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 35
[137] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 35
[139]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	35
[140]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	35

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 23 27
1135 MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1>	7 24 27
1125 MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0>	7 23 27
1124 MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1>	7 24 27
1125 MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>	7 23 27
1107 MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>	7 24 27
1125 MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 23 27
1107 MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1>	7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 23 24
1105 MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 23 24
1105 MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 23 24
1111 MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 23 24
1111 MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 23 24
1111 MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 23 24
1111 MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 25 27
1127 MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1>	7 26 27
1127 MEM_B_CNTL1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0>	7 25 27
1127 MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1>	7 26 27
1127 MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>	7 25 27
1127 MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>	7 26 27
1127 MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 25 27
1127 MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1>	7 26 27
1103 MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 25 26
1113 MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 25 26
1113 MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 25 26
1113 MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 25 26
1113 MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 25 26
1119		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 78 74
1102		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 78 74
1119		MEM_PWR	PP1V35_S3_MEM	23 24 25 26 46 69

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31 72
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 36 37
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 36 37
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 36 37
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 36 37
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 36 37
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 36 37
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 36 37
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 36 37
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 36 37
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 36 37
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 36 37
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 36 37
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 36 37
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 36 37
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 36 37
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 36 37
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 37 71
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 37 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 36 37
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 36 37
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 37 71
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 37 71
		S2_MEM_PWR	PP1V35_CAM 36 37
		S2_MEM_PWR	PP0V675_CAM_VREF 36 37
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 37
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 37

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 71
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N	46 59
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	28 48
	THERM_1TO1_45S	THERM	TBT_THERMD_N	48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
SB_POWER			PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 71
SB_POWER			PP3V3_S0	60 66 67 11 12 13 14 15 17 19 29 33 35 44 45 46 47 48 49 51 52 55 69 71 8 10 21 65 66 69
SB_POWER			PP1V35_S3RS0_CPUDDR	
GND			GND	

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