1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J110 MLB SCHEMATIC

09/25/14

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00384	1	SCHEM,MLB,J110	SCH	CRITICAL	
820-00164	1	PCBF,MLB,J110	PCB	CRITICAL	

DRAWING
TITLE=MLB
ASSEMBLY=DRAWING
LAST_MODIFIED=Thu Sep 25 14:26:29 2014

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:PVT,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS,SSD_LPSR:S3
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	XDP,SAMCONN
MLB_DEBUG:PVT	BKLT:PROD,XDP,SAMCONN,ISNS:ENG,DBGLED,XDP_CONN
MLB_DEBUG:PROD	BKLT:PROD,SAMCONN,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,PSVNS_ISNS:YES,A3PORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,PSVSS_ISNS:YES,3VSSB_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,PSVNS_ISNS:NO,A3PORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,PSVSS_ISNS:NO,3VSSB_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:MICRON_8GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:MICRON_8GB
DDR3:HYNIX_16GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_16GB
DDR3:SAMSUNG_16GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:SAMSUNG_16GB
DDR3:ELPIDA_16GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_16GB
DDR3:MICRON_16GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:MICRON_16GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0915	1	EEPROM,4MBIT,SPI,50MHZ,1.8V,USON8	U2890	CRITICAL	TBTROM:BLANK
341S00159	1	T29,EEPROM,FALCON RIDGE(V27.1), PROTO 0,J110/J113	U2890	CRITICAL	TBTROM:PROG
338S1214	1	IC,SMC12-B1,40MHZ/56DMIPS MCU,157BGA	U5000	CRITICAL	SMC:BLANK
335S00006	1	IC,SERIAL FLASH,64 MBIT 3V,WSON,QE=1	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S00007	1	IC,SERIAL FLASH,64 MBIT 3V,WSON,QE=1	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S00153	1	IC,EFI ROM(V8108), PROTO 0,J110/J113	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00029	1	BDW,QGH9,DD,1.8,15W,2+2,0.7,4M,BI168	U0500	CRITICAL	CPU:2.1GHZ
337S00073	1	BDW,QGHB,DD,1.6,15W,2+2,0.6,4M,BI168	U0500	CRITICAL	CPU:1.6GHZ
338S00069	1	IC,TBT,FR-2C,288, 12X12 FC-CSP,TRAY	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2KFEB4G,52 CMRA,8XB,208FCBGA	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J110_MLB
946-5477	1	UV GLUE,MLB,J41_J43	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S00036	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S00037	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	
825-7987	1	LABEL,MLB,J41/J43	NEW_LABEL		

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S00001	4	IC,SDRAM,23NM,8GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S00003	4	IC,SDRAM,23NM,16GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0793	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0791	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0793	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0791	4	IC,SDRAM,16GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_8GB
333S0789	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_16GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
4GB	0	0
8GB	0	1
16GB	1	0
RSVD	1	1

Alternate Parts

PART NUMBER	ALTERNATE_FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Vale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	26Mhz Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S00014	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
870-5074	870-1938		ALL	ALT POGO PIN W_D CAP
870-5071	870-1940		ALL	ALT POGO PIN W_D CAP
860-3428	860-1327		ALL	ALT STANDOFF W_O MYLAR
860-3690	860-1328		ALL	ALT STANDOFF W_O MYLAR
333S0787	333S0677	DRAM_TYPE:HYNIX_4GB	ALL	ALT STANDOFF W_O MYLAR
333S0785	333S0681	DRAM_TYPE:HYNIX_8GB	ALL	ALT STANDOFF W_O MYLAR

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BOM Configuration

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00613	PCBA,MLB,BETTER,HY-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00614	PCBA,MLB,BETTER,HY-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00616	PCBA,MLB,BETTER,SM-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00617	PCBA,MLB,BETTER,SM-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00621	PCBA,MLB,BETTER,EL-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB
639-00622	PCBA,MLB,BETTER,EL-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB
639-00695	PCBA,MLB,BETTER,EL-16GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB
685-00043	CMN PTS,PCBA,MLB,X430	MLB_COMMON,J110_MLB
685-00044	VCORE FET,REN,X430	VCORE_FET:REN
685-00045	VCORE FET,VSHY,X430	VCORE_FET:VSHY

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00044	685-00045		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00147	1	IC,SMC-A3,EXT,Vxxxx,PROTO 0,J110	U5000	CRITICAL	SMC:PROG

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00043	1	CMN PTS,PCBA,MLB,J110	CMNPTS	CRITICAL	MLB_CMNPTS
685-00045	1	VCORE FET,VSHY,J110	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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BOM Variants

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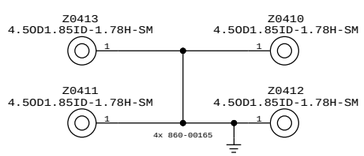
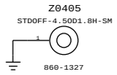
PD Module Parts

806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

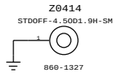
CPU Heat Sink Mounting Bosses



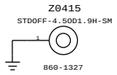
Fan Boss



X21 Boss

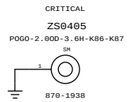


SSD Boss

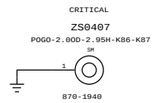


EMI I/O Pogo Pins

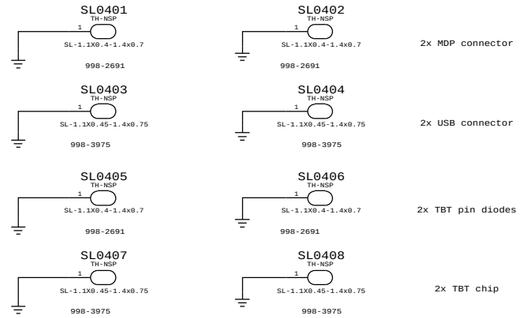
DisplayPort Pogo



USB/SD Card Pogo



Can Slots



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DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
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65 25	DP_TBTSNK0_ML_C_N<0>	C54	DDI1_TXN0	EDP_TXN0	C45	DP_INT_ML_C_N<0>	58 65
65 25	DP_TBTSNK0_ML_C_P<0>	C55	DDI1_TXP0	EDP_TXP0	B46	DP_INT_ML_C_P<0>	58 65
65 25	DP_TBTSNK0_ML_C_N<1>	B58	DDI1_TXN1	EDP_TXN1	A47	NC_INT_ML_CN<1>	62
65 25	DP_TBTSNK0_ML_C_P<1>	C58	DDI1_TXP1	EDP_TXP1	B47	NC_INT_ML_CP<1>	62
65 25	DP_TBTSNK0_ML_C_N<2>	B55	DDI1_TXN2	EDP_TXN2	C47	NC_INT_ML_CN<2>	62
65 25	DP_TBTSNK0_ML_C_P<2>	A55	DDI1_TXP2	EDP_TXP2	C46	NC_INT_ML_CP<2>	62
65 25	DP_TBTSNK0_ML_C_N<3>	A57	DDI1_TXN3	EDP_TXN3	A49	NC_INT_ML_CN<3>	62
65 25	DP_TBTSNK0_ML_C_P<3>	B57	DDI1_TXP3	EDP_TXP3	B49	NC_INT_ML_CP<3>	62
65 25 18	DP_TBTSNK1_ML_C_N<0>	C51	DDI2_TXN0				
65 25 18	DP_TBTSNK1_ML_C_P<0>	C50	DDI2_TXP0				
65 25 18	DP_TBTSNK1_ML_C_N<1>	C53	DDI2_TXN1	EDP_AUXN	A45	DP_INT_AUXCH_C_N	58 65
65 25 18	DP_TBTSNK1_ML_C_P<1>	B54	DDI2_TXP1	EDP_AUXP	B45	DP_INT_AUXCH_C_P	58 65
65 25 18	DP_TBTSNK1_ML_C_N<2>	C49	DDI2_TXN2				
65 25 18	DP_TBTSNK1_ML_C_P<2>	B50	DDI2_TXP2				
65 25 18	DP_TBTSNK1_ML_C_N<3>	A53	DDI2_TXN3	EDP_RCOMP	D20	MCP_EDP_RCOMP	
65 25 18	DP_TBTSNK1_ML_C_P<3>	B53	DDI2_TXP3	EDP_DISP_UTIL	A43	TP_EDP_DISP_UTIL	

eDP Port Assignment:

Internal panel

PPVCOMP_S0_CPU 8

R0530
24.9
1%
1/20W
MF
201

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
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			AY2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A3	TRUE	MCP_DC_A3_B3
			AY3	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A4		MCP_DC_A4
TP0531			AY60	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A60		MCP_DC_A60
			AY61	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A61	TRUE	MCP_DC_A61_B61
			AY62	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A62		MCP_DC_A62
TP0501			B2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AV1		MCP_DC_AV1
			B3	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW1		MCP_DC_AW1
			B61	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW2	TRUE	MCP_DC_AW2_AY2
			B62	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW3	TRUE	MCP_DC_AW3_AY3
			B63	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW61	TRUE	MCP_DC_AW61_AY61
			C1	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW62	TRUE	MCP_DC_AW62_AY62
			C2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW63		MCP_DC_AW63

NO_TEST

MCP_DC_AW2_AY2
MCP_DC_AW3_AY3
MCP_DC_AY60
MCP_DC_AW61_AY61
MCP_DC_AW62_AY62
MCP_DC_B2
MCP_DC_A3_B3
MCP_DC_A61_B61
MCP_DC_B62_B63
MCP_DC_C1_C2

TP0500
TP0510
TP0511
TP0520
TP0521
TP0530

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 18 OF 19
SPARE

NC	AT2	RSVD	RSVD	N23	NC
NC	AU44	RSVD	RSVD	R23	NC
NC	AV44	RSVD	RSVD	T23	NC
NC	D15	RSVD	RSVD	U10	NC
NC	F22	RSVD	RSVD	AL1	NC
NC	H22	RSVD	RSVD	AM11	NC
NC	J21	RSVD	RSVD	AP7	NC
			RSVD	AU10	NC
			RSVD	AU15	NC
			RSVD	AW14	NC
			RSVD	AY14	NC

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PAGE TITLE
CPU GFX/NCTF/RSVD

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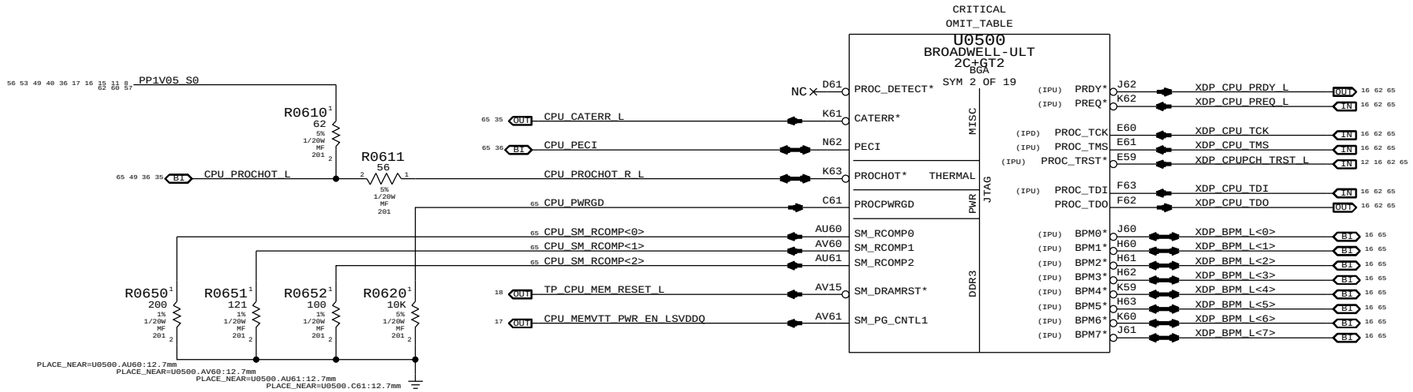
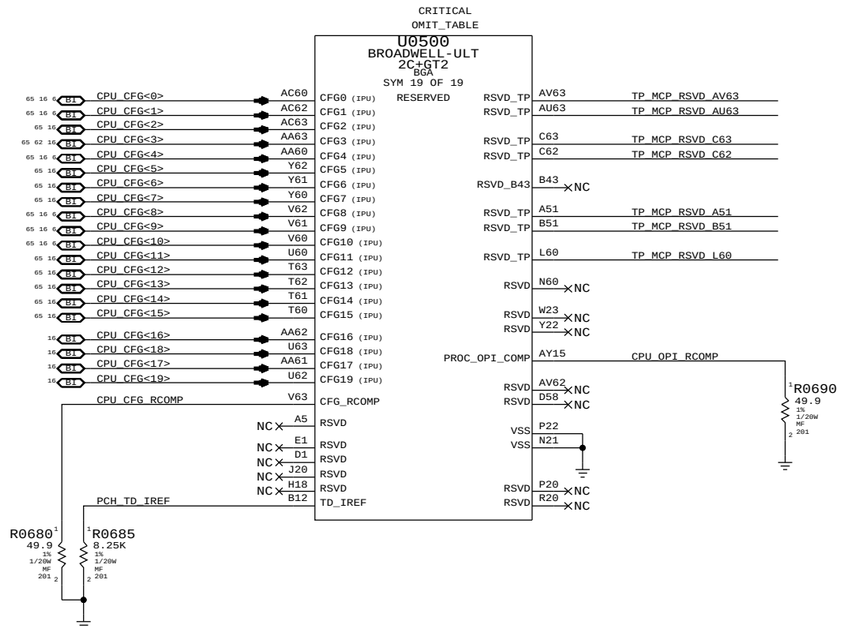
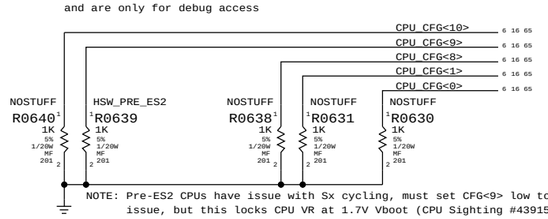


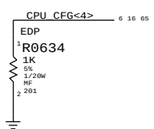


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE

CPU Misc/JTAG/CFG/RSVD

Apple Inc.

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REVISION <E4LABEL>

BRANCH <BRANCH>

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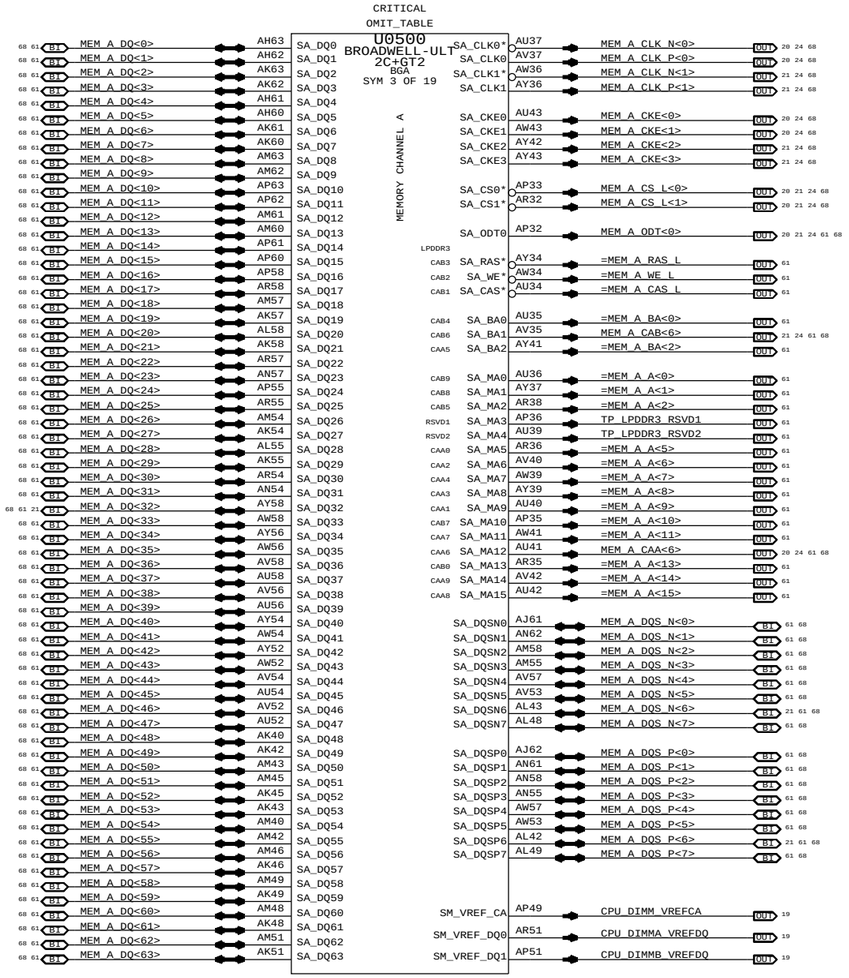

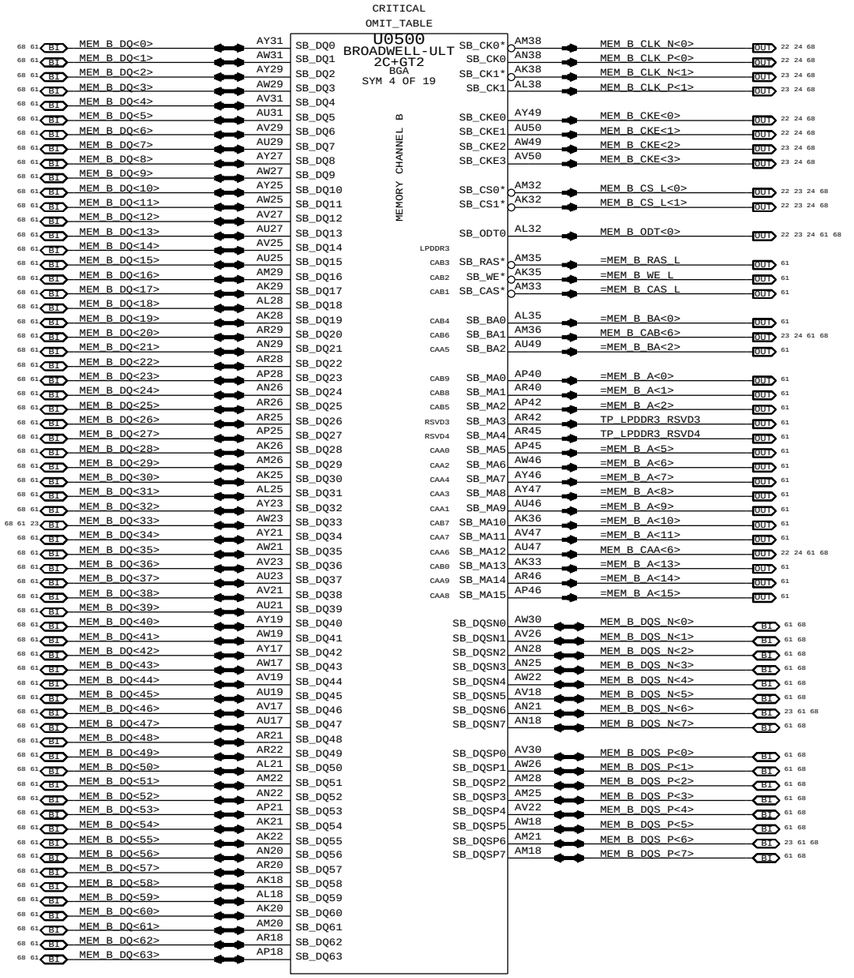

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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REVISION <E4LABEL>

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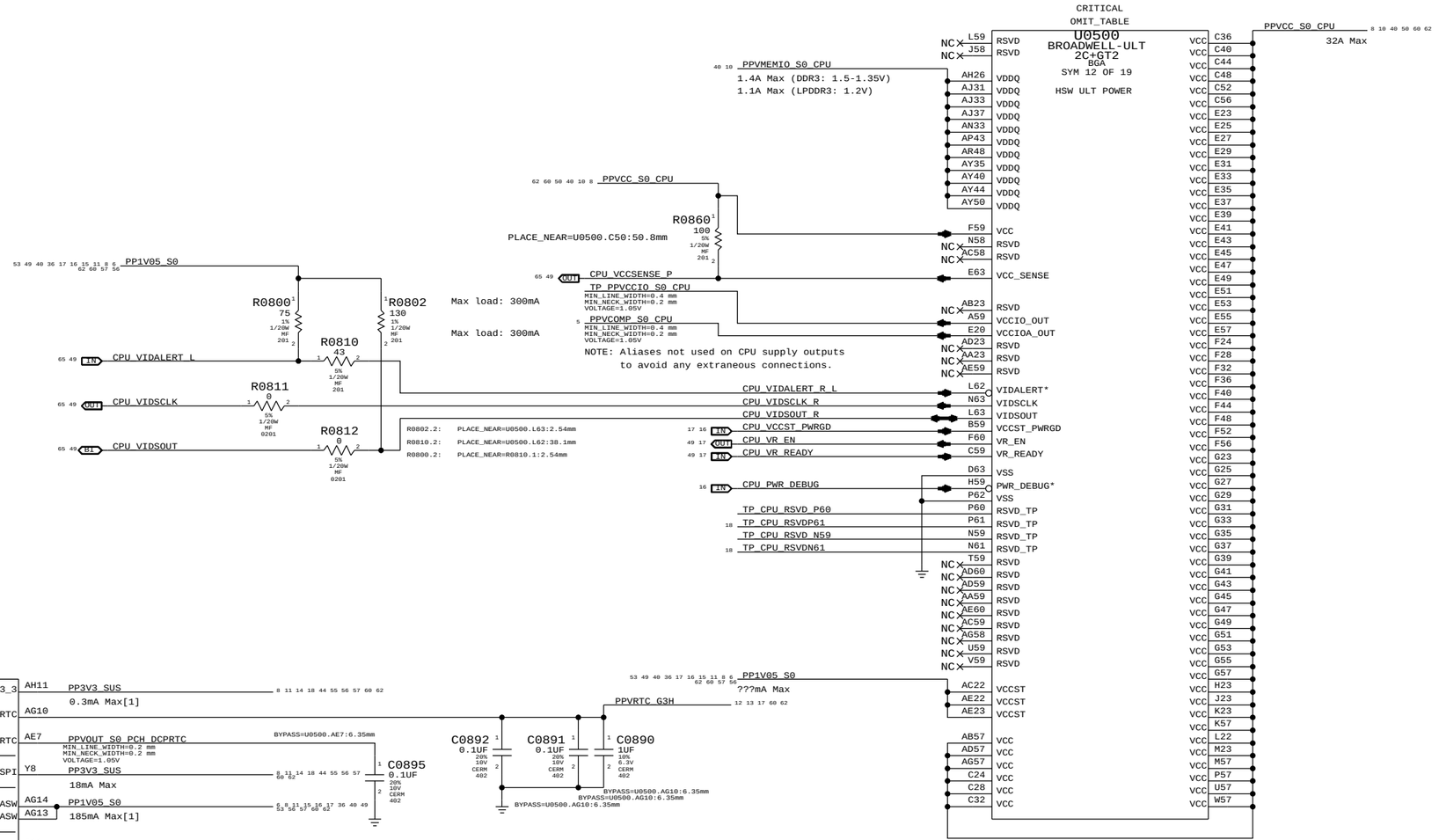
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J43_MLB	SYNC_DATE=10/02/2012
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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N → OUT 49 65

R0960
100
5% 1/20W MF 201
1 2

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

62 60 50 40 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402
NO STUFF C1001 10UF 20% 4V X6S 0402
NO STUFF C1002 10UF 20% 4V X6S 0402
NO STUFF C1003 10UF 20% 4V X6S 0402
NO STUFF C1004 10UF 20% 4V X6S 0402
NO STUFF C1005 10UF 20% 4V X6S 0402
NO STUFF C1006 10UF 20% 4V X6S 0402
NO STUFF C1007 10UF 20% 4V X6S 0402
NO STUFF C1008 10UF 20% 4V X6S 0402
NO STUFF C1009 10UF 20% 4V X6S 0402
NO STUFF C1010 10UF 20% 4V X6S 0402
NO STUFF C1011 10UF 20% 4V X6S 0402
NO STUFF C1012 10UF 20% 4V X6S 0402
NO STUFF C1013 10UF 20% 4V X6S 0402
NO STUFF C1014 10UF 20% 4V X6S 0402
NO STUFF C105A 10UF 20% 4V X6S 0402
CRITICAL C105B 10UF 20% 4V X6S 0402
CRITICAL C105C 10UF 20% 4V X6S 0402
NO STUFF C105D 10UF 20% 4V X6S 0402
NO STUFF C105E 10UF 20% 4V X6S 0402
CRITICAL C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402
NO STUFF C1016 10UF 20% 4V X6S 0402
NO STUFF C1017 10UF 20% 4V X6S 0402
NO STUFF C1018 10UF 20% 4V X6S 0402
NO STUFF C1019 10UF 20% 4V X6S 0402
NO STUFF C1020 10UF 20% 4V X6S 0402
NO STUFF C1021 10UF 20% 4V X6S 0402
NO STUFF C1030 10UF 20% 4V X6S 0402
NO STUFF C104A 10UF 20% 4V X6S 0402
NO STUFF C104B 10UF 20% 4V X6S 0402
NO STUFF C104C 10UF 20% 4V X6S 0402
CRITICAL C104D 10UF 20% 4V X6S 0402
NO STUFF C104E 10UF 20% 4V X6S 0402
CRITICAL C104F 10UF 20% 4V X6S 0402
CRITICAL C106A 10UF 20% 4V X6S 0402
NO STUFF C106B 10UF 20% 4V X6S 0402
NO STUFF C106C 10UF 20% 4V X6S 0402
NO STUFF C106D 10UF 20% 4V X6S 0402
NO STUFF C106E 10UF 20% 4V X6S 0402

CRITICAL C1070 10UF 20% 4V X6S 0402
CRITICAL C1071 10UF 20% 4V X6S 0402
NO STUFF C1072 10UF 20% 4V X6S 0402
NO STUFF C1073 10UF 20% 4V X6S 0402
NO STUFF C1074 10UF 20% 4V X6S 0402
NO STUFF C1075 10UF 20% 4V X6S 0402
CRITICAL C1076 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
NO STUFF C1078 10UF 20% 4V X6S 0402
NO STUFF C1079 10UF 20% 4V X6S 0402
NO STUFF C1080 10UF 20% 4V X6S 0402
NO STUFF C1081 10UF 20% 4V X6S 0402
NO STUFF C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402

CRITICAL C1085 10UF 20% 4V X6S 0402
CRITICAL C1086 10UF 20% 4V X6S 0402
CRITICAL C1087 10UF 20% 4V X6S 0402
NO STUFF C1088 10UF 20% 4V X6S 0402
NO STUFF C1089 10UF 20% 4V X6S 0402
NO STUFF C1090 10UF 20% 4V X6S 0402
CRITICAL C1091 10UF 20% 4V X6S 0402
CRITICAL C1092 10UF 20% 4V X6S 0402
NO STUFF C1093 10UF 20% 4V X6S 0402
NO STUFF C1094 10UF 20% 4V X6S 0402
NO STUFF C1095 10UF 20% 4V X6S 0402
NO STUFF C1096 10UF 20% 4V X6S 0402
CRITICAL C1097 10UF 20% 4V X6S 0402

NO STUFF C1022 10UF 20% 4V X6S 0402
NO STUFF C1023 10UF 20% 4V X6S 0402
NO STUFF C1024 10UF 20% 4V X6S 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
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NO STUFF C1036 10UF 20% 4V X6S 0402
NO STUFF C1037 10UF 20% 4V X6S 0402
NO STUFF C1038 10UF 20% 4V X6S 0402

NO STUFF C1039 10UF 20% 4V X6S 0402
NO STUFF C1044 10UF 20% 4V X6S 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
NO STUFF C1049 10UF 20% 4V X6S 0402

NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C1057 10UF 20% 4V X6S 0402
NO STUFF C1058 10UF 20% 4V X6S 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
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NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
NO STUFF C1068 10UF 20% 4V X6S 0402
NO STUFF C1069 10UF 20% 4V X6S 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
NO STUFF C109A 10UF 20% 4V X6S 0402

NO STUFF C109B 10UF 20% 4V X6S 0402
NO STUFF C109C 10UF 20% 4V X6S 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
NO STUFF C109E 10UF 20% 4V X6S 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
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NO STUFF C108B 10UF 20% 4V X6S 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

40 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

SYNC_MASTER=LABEL_J41 SYNC_DATE=01/11/2013
PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9:12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11:6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8:12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9:12.7mm
BYPASS=U0500.AE9:6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11:12.7mm
BYPASS=U0500.J11:6.35mm
BYPASS=U0500.AE8:6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9:6.35mm
BYPASS=U0500.L10:6.35mm
BYPASS=U0500.M9:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17:6.35mm
BYPASS=U0500.R21:6.35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:6.35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

R1275 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:6.35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

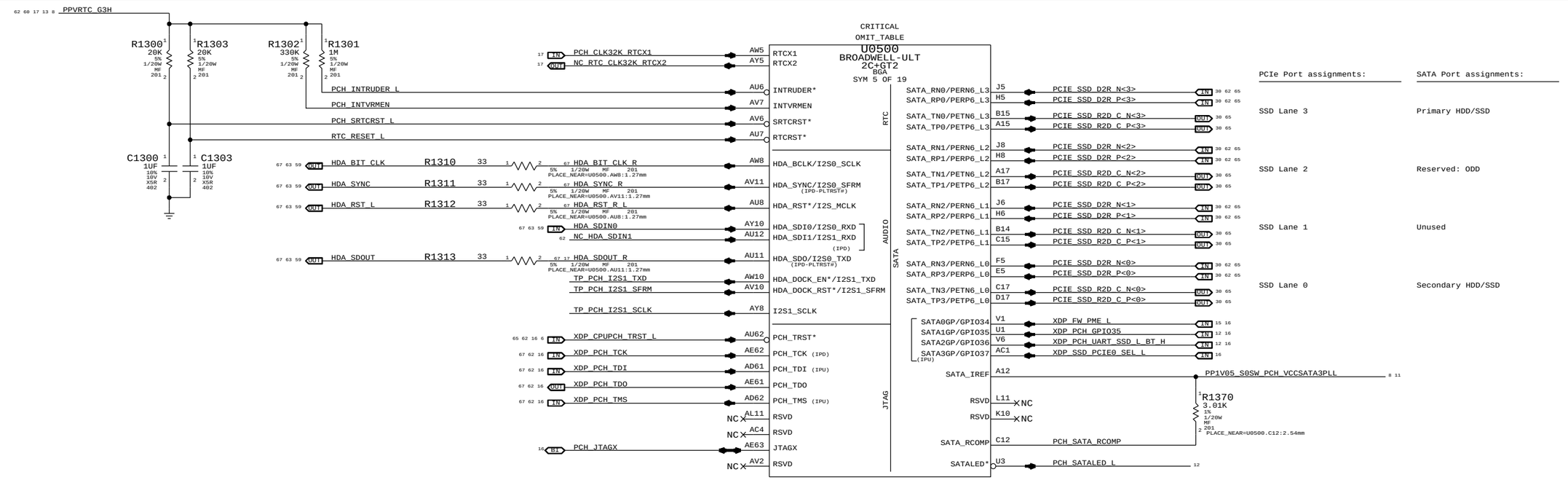
R1280 0 5% 1/10W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:6.35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

PP1V05_S0SW_PCH_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
NO STUFF C1290 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:6.35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
NO STUFF C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:6.35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012
PAGE TITLE: PCH Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 12 OF 120
SHEET: 11 OF 73



SYNC MASTER=WILL_J43 SYNC DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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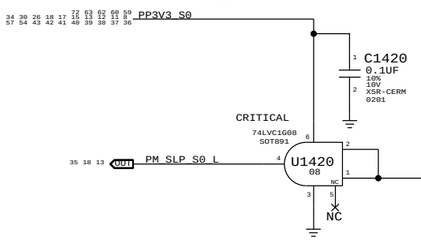
SLP_S0# Isolation



SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.

R1400 kept for debug purposes.

NO STUFF
R1400 0 5% 1/20W MF 0201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 8 OF 19
SYSTEM POWER MANAGEMENT

PCH_SUSACK_L	AK2	SUSACK* (IPU)	DSWVRMEN	AW7	PCH_DSWVRMEN	
PM_SYSRST_L	AC3	SYS_RESET*	DPWROK	AV5	PM_DSW_PWRGD	IN 35
PM_PCH_SYS_PWROK	AG2	SYS_PWROK	(IPD-DeepSx) WAKE*	AJ5	PCIE_WAKE_L	IN 13 29 31 62
PM_PCH_PWROK	AY7	PCH_PWROK	CLKRUN*/GPIO32	V5	PM_CLKRUN_L	BI 13 35 62
PM_PCH_PWROK	AB5	APWROK	SUS_STAT*/GPIO61	AG4	LPC_PWRDWN_L	OUT 35 62
PLT_RESET_L	AG7	PLTRST*	SUSCLK/GPIO62	AE6	PM_CLK32K_SUSCLK_R	OUT 36 67
PM_RSMRST_L	AW6	RSMRST*	SLP_S5*/GPIO63	AP5	PM_SLP_S5_L	OUT 13 35 57
PCH_SUSWARN_L	AV4	SUSWARN*/SUSPWRDNACK/GPIO30	SLP_S4*	AJ6	PM_SLP_S4_L	OUT 13 18 29 34 35 57
PM_PWRBTN_L	AL7	PWRBTN* (IPU)	SLP_S3*	AT4	PM_SLP_S3_L	OUT 13 17 18 35 57
SMC_ADAPTER_EN	AJ8	ACPRESENT/GPIO31 (IPD-DeepSx)	SLP_A*	AL5	TP_PM_SLP_A_L	
PM_BATLOW_L	AN4	BATLOW*/GPIO72	SLP_SUS*	AP4	PM_SLP_SUS_L	OUT 13 40 57
PCH_PM_SLP_S0_L	AF3	SLP_S0*	SLP_LAN*	AJ7	TP_PCH_SLP_LAN_L	
TP_PCH_SLP_WLAN_L	AM5	SLP_WLAN*/GPIO29				

PPVRTC_G3H — 8 12 17 60 62

R1450 330K 5% 1/20W MF 201

R1451 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
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EDP_BKLT_PWM	B8	EDP_BKLTCTL	eDP SIDEBAND	DDPB_CTRLCLK	B9	DP_TBTSNK0_DDC_CLK	OUT 18 28
EDP_BKLT_EN	A9	EDP_BKLEN		DDPB_CTRLDATA (IPD-PLTRST#)	C9	DP_TBTSNK0_DDC_DATA	BI 18 28
EDP_PANEL_PWR	C6	EDP_VDDEN		DDPC_CTRLCLK	D9	DP_TBTSNK1_DDC_CLK	OUT 18
				DDPC_CTRLDATA (IPD-PLTRST#)	D11	DP_TBTSNK1_DDC_DATA	BI 18
TBT_PWR_REQ_L	U6	PIRQA*/GPIO77	DISPLAY				
SMC_RUNTIME_SCI_L	P4	PIRQB*/GPIO78					
HDMITBTMUX_FLAG	N4	PIRQC*/GPIO79					
SSD_BOOT	N2	PIRQD*/GPIO80					
				DDPB_AUXN	C5	DP_TBTSNK0_AUXCH_C_N	BI 25 65
				DDPC_AUXN	B6	DP_TBTSNK1_AUXCH_C_N	BI 18 25 65
				DDPB_AUXP	B5	DP_TBTSNK0_AUXCH_C_P	BI 25 65
				DDPC_AUXP	A6	DP_TBTSNK1_AUXCH_C_P	BI 18 25 65
NC_PCI_PME_L	AD4	PME* (IPU)	PCI				
				DDPB_HPD	C8	DP_TBTSNK0_HPD	IN 25
ODD_PWR_EN_L	U7	GPIO55		DDPC_HPD	A8	DP_TBTSNK1_HPD	IN 18 25
HDMITBTMUX_LATCH	L1	GPIO52					
ENET_LOW_PWR	L3	GPIO54		EDP_HPD	D6	DP_INT_HPD	IN 58
AUD_PWR_EN	R5	GPIO51					
AP_PCIE_DEV_WAKE	L4	GPIO53					

PP3V3_S5 — 8 11 15 16 17 18 28 29 40 52 55 56 57 58 60 62 72
PP3V3_S0 — 8 11 12 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59

R1405	1K	PM_PWRBTN_L	13 16 35
R1410	10K	PM_BATLOW_L	13 27 35
R1452	10K	PCIE_WAKE_L	13 29 31 62
R1455	10K	PM_CLKRUN_L	13 35 62
R1460	100K	PM_SLP_S5_L	13 35 57
R1461	100K	PM_SLP_S4_L	13 18 29 34 35 57
R1462	100K	PM_SLP_S3_L	13 17 18 35 57
R1463	100K	PM_SLP_S0_L	13 18 35
R1464	100K	PM_SLP_SUS_L	13 40 57
R1430	100K	EDP_BKLT_EN	13 54
R1431	100K	EDP_PANEL_PWR	13 58
R1440	100K	TBT_PWR_REQ_L	13 26
R1441	100K	SMC_RUNTIME_SCI_L	13 35
R1442	100K	HDMITBTMUX_FLAG	13 62
R1443	100K	SSD_BOOT	13 30
R1445	100K	ODD_PWR_EN_L	13 62
R1446	100K	HDMITBTMUX_LATCH	13 62
R1447	100K	ENET_LOW_PWR	13 62
R1448	100K	AUD_PWR_EN	13 57 59 63
R1449	100K	AP_PCIE_DEV_WAKE	13 62

All: 5% 1/20W MF 201

SYNC_MASTER=J43_MLB — SYNC_DATE=02/20/2013

PAGE TITLE: PCH PM/PCI/GFX

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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PCIe Port Assignments:

Thunderbolt lane 0
Thunderbolt lane 1
Thunderbolt lane 2
Thunderbolt lane 3
AirPort
Reserved: FireWire
SD Card Reader (& Ethernet if combo)
Camera

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT 2C+GT2
BGA
SYM 11 OF 19

PCI-E
USB

PCIE_TBT_D2R_N<0>	F10	PERN5_L0
PCIE_TBT_D2R_P<0>	E10	PERP5_L0
PCIE_TBT_R2D_C_N<0>	C23	PETN5_L0
PCIE_TBT_R2D_C_P<0>	C22	PETP5_L0
PCIE_TBT_D2R_N<1>	F8	PERN5_L1
PCIE_TBT_D2R_P<1>	E8	PERP5_L1
PCIE_TBT_R2D_C_N<1>	B23	PETN5_L1
PCIE_TBT_R2D_C_P<1>	A23	PETP5_L1
PCIE_TBT_D2R_N<2>	H10	PERN5_L2
PCIE_TBT_D2R_P<2>	G10	PERP5_L2
PCIE_TBT_R2D_C_N<2>	B21	PETN5_L2
PCIE_TBT_R2D_C_P<2>	C21	PETP5_L2
PCIE_TBT_D2R_N<3>	E6	PERN5_L3
PCIE_TBT_D2R_P<3>	F6	PERP5_L3
PCIE_TBT_R2D_C_N<3>	B22	PETN5_L3
PCIE_TBT_R2D_C_P<3>	A21	PETP5_L3
PCIE_AP_D2R_N	G11	PERN3
PCIE_AP_D2R_P	F11	PERP3
PCIE_AP_R2D_C_N	C29	PETN3
PCIE_AP_R2D_C_P	B30	PETP3
NC_PCIE_FW_D2RN	F13	PERN4
NC_PCIE_FW_D2RP	G13	PERP4
NC_PCIE_FW_R2D_CN	B29	PETN4
NC_PCIE_FW_R2D_CP	A29	PETP4
NC_USB3RPCIE_SD_D2RN	G17	PERN1/USB3RN3
NC_USB3RPCIE_SD_D2RP	F17	PERP1/USB3RP3
NC_USB3RPCIE_SD_R2D_CN	C30	PETN1/USB3TN3
NC_USB3RPCIE_SD_R2D_CP	C31	PETP1/USB3TP3
PCIE_CAMERA_D2R_N	F15	PERN2/USB3RN4
PCIE_CAMERA_D2R_P	G15	PERP2/USB3RP4
PCIE_CAMERA_R2D_C_N	B31	PETN2/USB3TN4
PCIE_CAMERA_R2D_C_P	A31	PETP2/USB3TP4
NC	E15	RSVD
NC	E13	RSVD
PCH_PCIE_RCOMP	A27	PCIE_RCOMP
	B27	PCIE_IREF

USB Port Assignments:

Ext A (LS/FS/HS)
Ext B (LS/FS/HS)
BT
IR
Trackpad
Unused
Reserved: Camera
Reserved: SD (HS)

USB2N0	AN8	USB_EXTA_N
USB2P0	AM8	USB_EXTA_P
USB2N1	AR7	USB_EXTB_N
USB2P1	AT7	USB_EXTB_P
USB2N2	AR8	USB_BT_N
USB2P2	AP8	USB_BT_P
USB2N3	AR10	NC_USB_IRN
USB2P3	AT10	NC_USB_IRP
USB2N4	AM15	USB_TPAD_N
USB2P4	AL15	USB_TPAD_P
USB2N5	AM13	TP_USB_5N
USB2P5	AN13	TP_USB_5P
USB2N6	AP11	NC_USB_CAMERAN
USB2P6	AN11	NC_USB_CAMERAP
USB2N7	AR13	NC_USB_SDN
USB2P7 (IPD)	AP13	NC_USB_SDP

USB3 Port Assignments:

Ext A (SS)
Ext B (SS)

USB3RN1	G20	USB3_EXTA_D2R_N
USB3RP1	H20	USB3_EXTA_D2R_P
USB3TN1	C33	USB3_EXTA_R2D_C_N
USB3TP1	B34	USB3_EXTA_R2D_C_P
USB3RN2	E18	USB3_EXTB_D2R_N
USB3RP2	F18	USB3_EXTB_D2R_P
USB3TN2	B33	USB3_EXTB_R2D_C_N
USB3TP2	A33	USB3_EXTB_R2D_C_P

USBRBIAS*	AJ10	PCH_USB_RBIAS
USBRBIAS	AJ11	
RSVD	AN10	NC
RSVD	AM10	NC
OC0*/GPIO40	AL3	XDP_USB_EXTA_OC_L
OC1*/GPIO41	AT1	XDP_USB_EXTB_OC_L
OC2*/GPIO42	AH2	XDP_USB_EXTC_OC_L
OC3*/GPIO43	AV3	XDP_USB_EXTD_OC_L

PLACE_NEAR=U0500.AJ10:2.54mm
R1570 22.6 1% 1/20W MF 201

PP1V05_S0SW_PCH_VCCUSB3PLL
R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.A27:2.54mm

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT 2C+GT2
BGA
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LPC
SMBUS
SPI
C-LINK

LPC_AD<0>	AU14	LAD0
LPC_AD<1>	AW12	LAD1
LPC_AD<2>	AY12	LAD2
LPC_AD<3>	AW11	LAD3
LPC_FRAME_R_L	AV12	LFRAME*
SPI_CLK_R	AA3	SPI_CLK
SPI_CS0_R_L	Y7	SPI_CS0*
TP_SPI_CS1_L	Y4	SPI_CS1*
TP_SPI_CS2_L	AC2	SPI_CS2*
SPI_MOSI_R	AA2	SPI_MOSI
SPI_MISO	AA4	SPI_MISO
SPI_IO<2>	Y6	SPI_IO2
SPI_IO<3>	AF1	SPI_IO3
SMBALERT*/GPIO11	AN2	PCH_SMBALERT_L
SMBCLK	AP2	SMBUS_PCH_CLK
SMBDATA	AH1	SMBUS_PCH_DATA
SML0ALERT*/GPIO60	AL2	WOL_EN
SML0CLK	AN1	SML_PCH_0_CLK
SML0DATA	AK1	SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO73	AU4	PCH_SML1ALERT_L
SML1CLK_GPIO75	AU3	SMBUS_SMC_1_S0_SCL
SML1DATA/GPIO74	AH3	SMBUS_SMC_1_S0_SDA
CL_CLK	AF2	NC_CLINK_CLK
CL_DATA	AD2	NC_CLINK_DATA
CL_RST*	AF4	NC_CLINK_RESET_L

LPC_AD<0>	R1540	33	LPC_AD_R<0>
LPC_AD<1>	R1541	33	LPC_AD_R<1>
LPC_AD<2>	R1542	33	LPC_AD_R<2>
LPC_AD<3>	R1543	33	LPC_AD_R<3>
LPC_FRAME_L	R1544	33	LPC_FRAME_R_L

5% 1/20W MF 201

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS
PP3V3_SUS

R1580	100K	XDP_USB_EXTA_OC_L
R1581	100K	XDP_USB_EXTB_OC_L
R1582	100K	XDP_USB_EXTC_OC_L
R1583	100K	XDP_USB_EXTD_OC_L
R1548	1K	SPI_IO<2>
R1549	1K	SPI_IO<3>
R1590	100K	PCH_SMBALERT_L
R1591	100K	WOL_EN

5% 1/20W MF 201

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H R1631 100K 5% 1/20W MF 201

RAMCFG2:H R1636 100K 5% 1/20W MF 201

RAMCFG1:H R1635 100K 5% 1/20W MF 201

RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PP3V3_S3

SSD_LPSR:S3

R1696 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT 2C+GT2
BGA
SYM 10 OF 19

XDP_PCH_GPIO76	P1	BMBUSY*/GPIO76
XDP_MLB_RAMCFG0	AU2	GPIO8
HDMITBTMUX_SEL_TBT	AM7	LAN_PHY_PWR_CTRL/GPIO12
TP_MEM_VDD_SEL_1V5_L	AD6	GPIO15 (IPD-RSMRST#)
XDP_LPCPLUS_GPIO	Y1	GPIO16
XDP_PCH_GPIO17	T3	GPIO17
SD_RESET_L	AD5	GPIO24
SMC_WAKE_SCI_L	AN5	GPIO27 (IPD-DeepSx)
TPAD_SPI_INT_GPIO28_L	AD7	GPIO28
TPAD_USB_IF_EN	AN3	GPIO26
SSD_PWR_EN	AG6	GPIO56
PCH_TBT_PCIE_RESET_L	AP1	GPIO57
HDD_PWR_EN	AL4	GPIO58
XDP_SDCONN_STATE_CHANGE_L	AT5	GPIO59
SD_PWR_EN	AK4	GPIO44
TBT_PWR_EN	AB6	GPIO47
XDP_JTAG_ISP_TCK	U4	GPIO48
XDP_JTAG_ISP_TDI	Y3	GPIO49
JTAG_TBT_TMS_PCH	P3	GPIO50
PCH_HSIO_PWR_EN	Y2	HSIOPC/GPIO71
TPAD_SPI_IF_EN	AT3	GPIO13
XDP_MLB_RAMCFG3	AH4	GPIO14
SPIROM_USE_MLB	AM4	GPIO25
CAMERA_PWR_EN_PCH	AG5	GPIO45
TPAD_SPI_INT_GPIO46_L	AG3	GPIO46
XDP_MLB_RAMCFG1	AM3	GPIO9
XDP_MLB_RAMCFG2	AM2	GPIO10
SSD_SR_EN_L	P2	DEVSLP0/GPIO33
AP_S0IX_WAKE_SEL	C4	SDIO_POWER_EN/GPIO70
SSD_RESET_L	L2	DEVSLP1/GPIO38
CAM_PCIE_RESET_L	N5	DEVSLP2/GPIO39
PCH_TCO_TIMER_DISABLE	V2	SPKR/GPIO81 (IPD-PLTRST#)

CPU/MISC

THERMTRIP*	D60	PM_THRMTRIP_L
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT_L
SERIRQ	T4	LPC_SERIRQ
PCH_OPI_COMP	AW15	PCH_OPI_COMP
RSVD	AF20	NC
RSVD	AB21	NC

GPIO / LPIO

GSPI0_CS*/GPIO83	R6	AUD_SPI_CS_L
GSPI0_CLK/GPIO84	L6	AUD_SPI_CLK
GSPI0_MISO/GPIO85 (IPD)	N6	AUD_SPI_MISO
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	L8	AUD_SPI_MOSI
GSPI1_CS*/GPIO87	R7	TPAD_SPI_CS_L
GSPI1_CLK/GPIO88	L5	TPAD_SPI_CLK
GSPI1_MISO/GPIO89 (IPD)	N7	TPAD_SPI_MISO
GSPI_MOSI/GPIO90	K2	TPAD_SPI_MOSI
UART0_RXD/GPIO91	J1	PCH_BT_UART_D2R
UART0_TXD/GPIO92	K3	PCH_BT_UART_R2D
UART0_RTS*/GPIO93	J2	PCH_BT_UART_RTS_L
UART0_CTS*/GPIO94	G1	PCH_BT_UART_CTS_L
UART1_RXD/GPIO0	K4	PCH_UART1_RXD
UART1_TXD/GPIO1	G2	PCH_UART1_TXD
UART1_RST*/GPIO2	J3	JTAG_ISP_TDO
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L
I2C0_SDA/GPIO4	F2	AP_S0IX_WAKE_L
I2C0_SCL/GPIO5	F3	AP_RESET_L
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L
SDIO_CMD/GPIO65	F4	BT_PWRRST_L
SDIO_D0/GPIO66 (IPD-PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67	E4	ENET_MEDIA_SENSE
SDIO_D2/GPIO68	C3	LCD_IRQ_L
SDIO_D3/GPIO69	E2	LCD_PSR_EN

PP1V05_S0

R1650 1K 5% 1/20W MF 201

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

R1655 49.9 1% 1/20W MF 201

PLACE_NEAR=U0500.AW15:2.54mm

PLT_RESET_L

R1621 100K 5% 1/20W MF 201

R1671 100K 5% 1/20W MF 201

TPAD_SPI_INT_GPIO28_L

R1681 0 5% 1/20W MF 0201

TPAD_SPI_INT_L

R1682 0 5% 1/20W MF 0201

TPAD_SPI_INT_GPIO46_L

R1639 100K 5% 1/20W MF 201

R1680 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S0

R1641 1K 5% 1/20W MF 201

PP3V3_S5
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_S0

TBTLC for CR, S0 for RR

R1610	100K	XDP_PCH_GPIO76	
R1614	100K	XDP_LPCPLUS_GPIO	
R1615	100K	XDP_PCH_GPIO17	
SD_ON_MLB			
R1616	100K	SD_RESET_L	R1616 should also be stuffed if platform does not use SD card
R1617	100K	SMC_WAKE_SCI_L	
R1618	100K	TPAD_SPI_INT_L	
R1619	100K	TPAD_USB_IF_EN	
R1620	100K	SSD_PWR_EN	SSD_LPSR:S0 BOM option is on R1620
SSD_LPSR:S0			
R1622	100K	HDD_PWR_EN	
R1623	100K	XDP_SDCONN_STATE_CHANGE_L	
R1624	100K	SD_PWR_EN	
R1625	100K	TBT_PWR_EN	
R1626	100K	XDP_JTAG_ISP_TCK	
R1627	100K	XDP_JTAG_ISP_TDI	
R1628	100K	JTAG_TBT_TMS_PCH	
R1629	100K	PCH_HSIO_PWR_EN	
R1630	100K	TPAD_SPI_IF_EN	
R1632	100K	SPIROM_USE_MLB	Stuffed R1632
R1633	100K	CAMERA_PWR_EN_PCH	
R1634	100K	TPAD_SPI_INT_GPIO46_L	No-Stuffed R1634
NOSTUFF			
R1637	100K	SSD_SR_EN_L	
R1638	100K	AP_S0IX_WAKE_SEL	
R1640	100K	XDP_FW_PME_L	
R1652	10K	LPC_SERIRQ	
R1691	100K	BT_PWRRST_L	
R1693	100K	ENET_MEDIA_SENSE	
R1694	100K	LCD_IRQ_L	
R1695	100K	LCD_PSR_EN	

All: 5% 1/20W MF 201

R1660	100K	AUD_SPI_CS_L
R1661	100K	AUD_SPI_CLK
R1662	100K	AUD_SPI_MISO
R1663	100K	AUD_SPI_MOSI
R1664	47K	TPAD_SPI_CS_L
R1665	47K	TPAD_SPI_CLK
R1666	47K	TPAD_SPI_MISO
R1667	47K	TPAD_SPI_MOSI
R1668	47K	PCH_BT_UART_D2R
R1669	47K	PCH_BT_UART_R2D
R1672	47K	PCH_UART1_RXD
R1673	47K	PCH_UART1_TXD
R1674	100K	JTAG_ISP_TDO
R1675	47K	PCH_UART1_CTS_L
R1676	100K	AP_S0IX_WAKE_L
R1678	2.2K	PCH_I2C1_SDA
R1679	2.2K	PCH_I2C1_SCL
R1670	47K	PCH_BT_UART_RTS_L
R1677	47K	PCH_BT_UART_CTS_L

All: 5% 1/20W MF 201

SYNC_MASTER=WILL_J43 SYNC_DATE=01/14/2013

PAGE TITLE: PCH GPIO/MISC/LPIO

Apple Inc.

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

R1830 150 5% 1/16W MF-LF 402

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_TDO
R1810 51 5% 1/20W MF 201
PLACE_NEAR=U0500.F62:28mm

XDP_CPU_TCK
R1813 51 5% 1/20W MF 201
PLACE_NEAR=U0500.E60:28mm

TDI and TMS are terminated in CPU.

CPU_VCCST_PWRGD → R1800 1K → XDP_CPU_VCCST_PWRGD
PLACE_NEAR=U0500.C61:2.54mm

PM_PWRBTN_L → R1802 0 → XDP_CPU_PWRBTN_L
PLACE_NEAR=U5000.J3:2.54mm

PM_PCH_SYS_PWROK → R1804 0 → XDP_SYS_PWROK

XDP_CPU_TCK

PCH_JTAGX → R1835 0
PLACE_NEAR=J1800.58:28mm

R1805 1K → PLT_RESET_L
PLACE_NEAR=U0500.AG7:2.54mm

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL
Q1840 DMN5L06VK-7 SOT563
PLACE_NEAR=J1800.51:28MM
XDP_CPU_TDO

CRITICAL
Q1840 DMN5L06VK-7 SOT563
XDP_CPUPCH_TRST_L
MAKE_BASE=TRUE
XDP_CPUPCH_TRST_L

CRITICAL
Q1842 DMN5L06VK-7 SOT563
PLACE_NEAR=J1800.55:28mm
XDP_CPU_TDI

CRITICAL
Q1842 DMN5L06VK-7 SOT563
XDP_CPU_TMS

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals

XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L		XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L		XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L		XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK		XDP_JTAG_ISP_TCK
XDP_FW_PME_L	TP1879	
XDP_PCH_GPIO35	TP1880	
XDP_PCH_UART_SSD_L_BT_H	TP1881	
XDP_SSD_PCIE0_SEL_L	R1884 1K	
XDP_LPCPLUS_GPIO		XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI		XDP_JTAG_ISP_TDI

(TP-P6, MAKE_BASE=TRUE)

NOTE: Must not short XDP pins together!

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5

C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC, NC)
R1845 330K 5% 1/20W MF 201

ALL_SYS_PWRGD → XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

(5% 1/20W MF 201)

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: CPU/PCH Merged XDP

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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenCLK 25MHz Power — PP3V3_S5RS3RS0_SYSCLKGEN
Must be powered if any VDDIO is powered.

CAM XTAL Power — PP1V2_CAM_XTALPCIEVDD
TBT XTAL Power — PP3V3_TBTLC

C1924 0.1UF 10% 16V X5R-CERM 0201
C1922 0.1UF 10% 16V X5R-CERM 0201
C1902 1UF 20% 6.3V X5R 0201

U1900 SLG3NB148CV TQFN CRITICAL
NC, VDD, VG3HOT
VIOE_25M_A, VIOE_25M_B, VIOE_25M_C
32.768K
25M_A, 25M_B, 25M_C
VOUT
GND, THRM PAD

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

CKPLUS_WAIVE=PwrTerm2Gnd

PCH_CLK32K_RTCX1 (OUT)
SYSCLK_CLK25M_CAMERA (OUT)
SYSCLK_CLK25M_TBT (OUT)
PPVRTC_G3H (OUT) — For SB RTC Power

C1910 1UF 20% 6.3V X5R 0201

C1905 12PF 5% 25V NP0-C0G-CERM 0201
C1906 12PF 5% 25V NP0-C0G-CERM 0201
Y1905 CRITICAL 25.000MHZ-12PF-20PPM SM-3.2X2.5MM
R1905 0 5% 1/20W MF 0201 — NO STUFF
R1906 1M 5% 1/20W MF 201

SYSCLK_CLK25M_X2 → SYSCLK_CLK25M_X2_R → X2
SYSCLK_CLK25M_X1 → X1

NOTE: 30 PPM or better required for RTC accuracy

PCH 24MHz Crystal

C1915 6.8PF +/-0.1PF 25V C0G 0201
C1916 6.8PF +/-0.1PF 25V C0G 0201
Y1915 CRITICAL 24.000MHZ-20PPM-6PF 3.20X2.50MM-SM1
R1915 0 5% 1/20W MF 0201
R1916 1M 5% 1/20W MF 201

PCH_CLK24M_XTALOUT_R → PCH_CLK24M_XTALOUT (IN)
PCH_CLK24M_XTALIN (OUT)

PCH 24MHz Outputs

R1927 22 5% 1/20W MF 201

LPC_CLK24M_SMC_R (IN) → LPC_CLK24M_SMC (MAKE_BASE=TRUE) → LPC_CLK24M_SMC (OUT)
PLACE_NEAR=U0500.AN15:5.1mm

PCH Reset Button

PP3V3_S0
R1995 10K 5% 1/20W MF 201
XDP
R1996 0 1/20W 0201 MF 5%
XDP_DBRESET_L (IN) → PM_SYSRST_L (OUT)
NO STUFF
R1997 0 5% 1/16W MF-LF 402
SILK_PART=SYS RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3
C1970 0.1UF 10% 16V X5R-CERM 0201
U1970 74AUP1G07GF SOT891 — VCC, A, Y, NC, NC, NC, GND
PP3V3_S0
R1970 330K 5% 1/20W MF 201
TPS51916 I(leak) = +/- 1uA, Vih(min) = 1.8V
33uW when driven-low
CPU_MEMVTT_PWR_EN_LSVDDQ (IN)
MEMVTT_PWR_EN (MAKE_BASE=TRUE) → MEMVTT_PWR_EN (OUT)

PCH ME Disable Strap

PP5V_S0
R1920 100K 5% 1/20W MF 201
Q1920 DMN5L06VK-7 SOT563 VER 3
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE
Q1920 DMN5L06VK-7 SOT563 VER 3
R1921 1K 5% 1/20W MF 201
SPI_DESCRIPTOR_OVERRIDE_L (IN)
HDA_SDOUT_R (OUT) — IPD = 9-50k

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

PP3V3_S5
C1930 0.1UF 10% 16V X5R-CERM 0201
U1930 CRITICAL 74AUP1G09 SOT891 — VCC, A, B, NC, Y, GND
PP1V05_S0
R1931 10K 5% 1/20W MF 201
ALL_SYS_PWRGD
PM_SLP_S3_L (IN)
CPU_VCCST_PWRGD (OUT)

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0
C1950 0.1UF 10% 16V X5R-CERM 0201 — BYPASS=U1950:5MM
R1950 10K 5% 1/20W MF 201
U1950 74LVC2G08GT SOT833
CPU_VR_EN (IN)
R1955 10K 5% 1/20W MF 201
NO STUFF R1951 0 5% 1/20W MF 0201
CPU_VR_READY (OUT) MAKE_BASE=TRUE
CPU_VR_READY (IN)
ALL_SYS_PWRGD (IN)
CPUVR_PGOOD_R
PM_S0_PGOOD
NO STUFF R1961 100K 5% 1/20W MF 201
R1963 0 5% 1/20W MF 0201
NO STUFF R1960 0 5% 1/20W MF 0201 — WF: Do we need this?
U1950 74LVC2G08GT SOT833 — CKPLUS_WAIVE=UNCONNECTED_PINS
SYS_PWROK_R
R1962 1K 5% 1/20W MF 201
PM_PCH_SYS_PWROK (OUT)
PM_PCH_PWROK (OUT) MAKE_BASE=TRUE
SMC_DELAYED_PWRGD (IN)

SYNC_MASTER=J43_MLB1	SYNC_DATE=01/09/2013
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Platform Reset Connections

Unbuffered

PLT_RESET_L

R2071 0 5% 1/20W MF 0201

PCA9557D_RESET_L

Scrub for Layout Optimization

Buffered

PP3V3_S0

CRITICAL
U2071 MC74VHC1G08 SC70-HF

C2071 0.1UF 10% 16V X5R-CERM 0201

R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L

R2072 0 5% 1/20W MF 0201

SMC_LRESET_L

R2088 0 5% 1/20W MF 0201

BKLT_PLT_RST_L

NOSTUFF
R2089 0 5% 1/20W MF 0201

CAM_PCIE_RESET_L

PCH_TBT_PCIE_RESET_L
MAKE_BASE=TRUE

PCH_TBT_PCIE_RESET_L

PP3V3_S5

NOSTUFF
BYPASS=U2030:3mm
C2030 0.1UF 10% 10V X5R-CERM 0201

NOSTUFF
CRITICAL
U2030 74LVC1G08 SOT891 08

PM_SLP_S4_L

CAMERA_PWR_EN_PCH

CAMERA_PWR_EN

NC

R2030 0 5% 1/20W MF 0201

Power State Debug LEDs

(For development only)

DBGLED

PP3V3_S5

R2094 0 5% 1/16W MF-LF 402

PLACE_SIDE=BOTTOM

PP3V3_S5_DBGLED
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=3.3V

R2090 20K 5% 1/20W MF 201
R2091 20K 5% 1/20W MF 201
R2092 20K 5% 1/20W MF 201
R2093 20K 5% 1/20W MF 201
R2095 20K 5% 1/20W MF 201

DBGLED_S5
DBGLED_S4
DBGLED_S3
DBGLED_S0I3
DBGLED_S0

D2090 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S5_ON
D2091 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=STBY_ON
D2092 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S3_ON
D2093 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON
D2095 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0_ON

DBGLED_S4_D
DBGLED_S3_D
DBGLED_S0I3_D
DBGLED_S0_D

Q2090 DMN5L06VK-7 SOT563 VER 3
Q2091 DMN5L06VK-7 SOT563 VER 3

S4_PWR_EN
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_S0_L

GreenCLK 25MHz Power

NO STUFF
R2040 0 5% 1/20W MF 0201

PP3V3_S3

PP3V3_S5RS3RS0_SYSCLKGEN

PP3V3_S5RS3RS0_SYSCLKGEN
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

NO STUFF
R2041 0 5% 1/20W MF 0201

PP3V3_S0

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

R2042 0 5% 1/20W MF 0201

PP3V3_S5

Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

PP3V3_TBTLC

R2061 100K 5% 1/20W MF 201

C2060 0.1UF 20% 10V CERM 402

R2062 100K 5% 1/20W MF 201

U2060 74LVC2G07 SOT891
VCC
GND
1A 2A 1Y 2Y

From RR
From PCH

JTAG_TBT_TDO
JTAG_TBT_TMS_PCH
S0 pull-up on PCH page

S0 pull-up on PCH page

JTAG_ISP_TDO
JTAG_TBT_TMS

To PCH
To RR

NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary.

Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property

TP_CPU_RSVDN61 — TP_CPU_RSVDN61 MAKE_BASE=TRUE

TP_CPU_RSVDP61 — TP_CPU_RSVDP61 MAKE_BASE=TRUE

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

RAMCFG3:L R2050 10K 5% 1/20W MF 201
RAMCFG2:L R2051 10K 5% 1/20W MF 201
RAMCFG1:L R2052 10K 5% 1/20W MF 201
RAMCFG0:L R2053 10K 5% 1/20W MF 201

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L — TP_CPU_MEM_RESET_L MAKE_BASE=TRUE

TP_MEM_VDD_SEL_1V5_L — TP_MEM_VDD_SEL_1V5_L MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFDQ_A — PP0V6_S3_MEM_VREFDQ_A MAKE_BASE=TRUE VOLTAGE=0.6V

PP0V6_S3_MEM_VREFCA_A — PP0V6_S3_MEM_VREFCA_A MAKE_BASE=TRUE VOLTAGE=0.6V

PP0V6_S3_MEM_VREFDQ_B — PP0V6_S3_MEM_VREFDQ_B MAKE_BASE=TRUE VOLTAGE=0.6V

PP0V6_S3_MEM_VREFCA_B — PP0V6_S3_MEM_VREFCA_B MAKE_BASE=TRUE VOLTAGE=0.6V

DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0

NO STUFF
R2020 2.2K 5% 1/20W MF 201

R2021 2.2K 5% 1/20W MF 201

NO STUFF
R2022 2.2K 5% 1/20W MF 201

R2023 2.2K 5% 1/20W MF 201

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that
DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so
DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

PP3V3_S0

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC (on TBT page)

R2015 100K 5% 1/20W MF 201

Falcon Ridge PLUG_EVENT is active-low, always driven (pull-up)

TBT_CIO_PLUG_EVENT_L — MAKE_BASE TRUE — TBT_CIO_PLUG_EVENT_L

Required for unused second TBT port

TBT_B_CIO_SEL
DP_TBTPB_HPD
TBT_B_CONFIG2_RC
TBT_B_CONFIG1_BUF
TBT_B_LSRX

R2016 10K 5% 1/20W MF 201
R2017 10K 5% 1/20W MF 201
R2018 10K 5% 1/20W MF 201
R2019 10K 5% 1/20W MF 201
R2014 10K 5% 1/20W MF 201

TBT Aliases

MAKE_BASE

DP_TBTSNK0_DDC_CLK — TRUE — DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA — TRUE — DP_TBTSNK0_DDC_DATA

MAKE_BASE

DP_TBTSNK1_HPD — TRUE — DP_TBTSNK1_HPD
=DP_TBTSNK1_ML_C_P<3..0> — TRUE — DP_TBTSNK1_ML_C_P<3..0>
=DP_TBTSNK1_ML_C_N<3..0> — TRUE — DP_TBTSNK1_ML_C_N<3..0>
DP_TBTSNK1_AUXCH_C_P — TRUE — DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N — TRUE — DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK1_DDC_CLK — TRUE — DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA — TRUE — DP_TBTSNK1_DDC_DATA

Single-port TBT implementation does not require DDC Crossbar

XDP_JTAG_ISP_TCK — XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI — XDP_JTAG_ISP_TDI

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

PP3V3_SUS

R2010 100K 5% 1/20W MF 201

PCH_SML1ALERT_L

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 20 OF 120
SHEET: 18 OF 73

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

Q2220 DMN5L06VK-7 SOT563 CRITICAL VER 3
Q2260 DMN5L06VK-7 SOT563 CRITICAL VER 3
Q2220 DMN5L06VK-7 SOT563 CRITICAL VER 3
Q2260 DMN5L06VK-7 SOT563 CRITICAL VER 3

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches
May not be necessary due to C22x0

DDRVREF_DAC R2225 100K 1% 1/20W MF 201 — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC R2201 100K 1% 1/20W MF 201; DDRVREF_DAC C2225 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2245 100K 1% 1/20W MF 201 — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC R2202 100K 1% 1/20W MF 201; DDRVREF_DAC C2245 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2265 100K 1% 1/20W MF 201 — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC R2215 100K 1% 1/20W MF 201; DDRVREF_DAC C2265 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2285 100K 1% 1/20W MF 201 — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC R2207 100K 1% 1/20W MF 201; DDRVREF_DAC C2285 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT563 VER 3
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT563 VER 3
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT563 VER 3
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT563 VER 3

Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm
R22x6 pin 2: PLACE_NEAR=Q2225.1:2.54mm; PLACE_NEAR=Q2265.1:2.54mm; PLACE_NEAR=Q2225.4:2.54mm; PLACE_NEAR=Q2265.4:2.54mm

(All 4 R's) DDRVREF_DAC
R2226 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_A_RDIV
R2246 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_B_RDIV
R2266 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_A_RDIV
R2286 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_B_RDIV

VRef Dividers

Always used, regardless of margining option.

PP1V2_S3 (17 20 21 22 23 40 51 60 68)

R2223 10 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:2mm — C2220 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_A_RC
R2221 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:3mm — PP0V6_S3_MEM_VREFDQ_A (18 20 21 68) MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm
R2222 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2221.2:1mm
R2220 24.9 1% 1/20W MF 201

R2243 10 1% 1/20W MF 201 — PLACE_NEAR=Q2260.6:2mm — C2240 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_B_RC
R2241 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2260.6:3mm — PP0V6_S3_MEM_VREFDQ_B (18 22 23 68) MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm
R2242 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2241.2:1mm
R2240 24.9 1% 1/20W MF 201

R2263 10 1% 1/20W MF 201 — PLACE_NEAR=Q2220.3:2mm — C2260 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_A_RC
R2261 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2220.3:3mm — PP0V6_S3_MEM_VREFCA_A (18 20 21 68) MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm
R2262 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2261.2:1mm
R2260 24.9 1% 1/20W MF 201

R2283 10 1% 1/20W MF 201 — PLACE_NEAR=Q2260.3:2mm — C2280 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_B_RC
R2281 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2260.3:3mm — PP0V6_S3_MEM_VREFCA_B (18 22 23 68) MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm
R2282 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2281.2:1mm
R2280 24.9 1% 1/20W MF 201

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.
OMIT

PP3V3_S3 (28 24 19 18 15 65 62 58 56 55) — R2218 SHORT NONE NONE NONE 402 — PP3V3_S3_VREFMRGN_DAC (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF; DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574 (VDD 8, GND 9)
54 38 19 16 14 67 I2C_SMBUS_PCH_CLK → SCL 6
54 38 19 16 14 67 I2C_SMBUS_PCH_DATA → SDA 7
Addr=0x98(WR)/0x99(RD)
A0 8, A1 10
VOUTA 1 → VREFMRGN_DQ_A
VOUTB 2 → VREFMRGN_DQ_B
VOUTC 4 → VREFMRGN_CA_AB
VOUTD 5 → VREFMRGN_MEMVREG

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2201 PCA9557 QFN (OD) (VCC 16, THRM PAD 17, GND 8)
Addr=0x30(WR)/0x31(RD)
A0 3, A1 4, A2 5
67 54 38 19 16 14 I2C_SMBUS_PCH_CLK → SCL 1
67 54 38 19 16 14 I2C_SMBUS_PCH_DATA → SDA 2
P0 6 VREFMRGN_CPU_EN
P1 7 VREFMRGN_DQ_A_EN
P2 9 VREFMRGN_DQ_B_EN
P3 10 VREFMRGN_CA_A_EN
P4 11 VREFMRGN_CA_B_EN
P5 12 VREFMRGN_MEMVREG_EN
P6 13 VREFMRGN_SPARE_EN
P7 14 NC
RESET* 15 ← 18 PCA9557D_RESET_L

R2200 100K 5% 1/20W MF 201 — DDRVREF_DAC

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3 (15 18 19 34 38 39 56 60 62 63)

DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP (V+ B1, V- B4, C2, C3, C1, C4)
VREFMRGN_MEMVREG_BUF

DDRVREF_DAC R2214 38.3K 1% 1/20W MF 201 — PLACE_NEAR=R7415.2:1mm — DDRREG_FB (OUT 51)

DDRVREF_DAC R2213 100K 5% 1/20W MF 201

CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP (V+ B1, V- B4, A2, A3, A1, A4)
VREFMRGN_SPARE_BUF

DDRVREF_DAC R2217 1M 5% 1/20W MF 201

Pins B1 & B4: **CKPLUS_WAIVE=unconnected_pins**

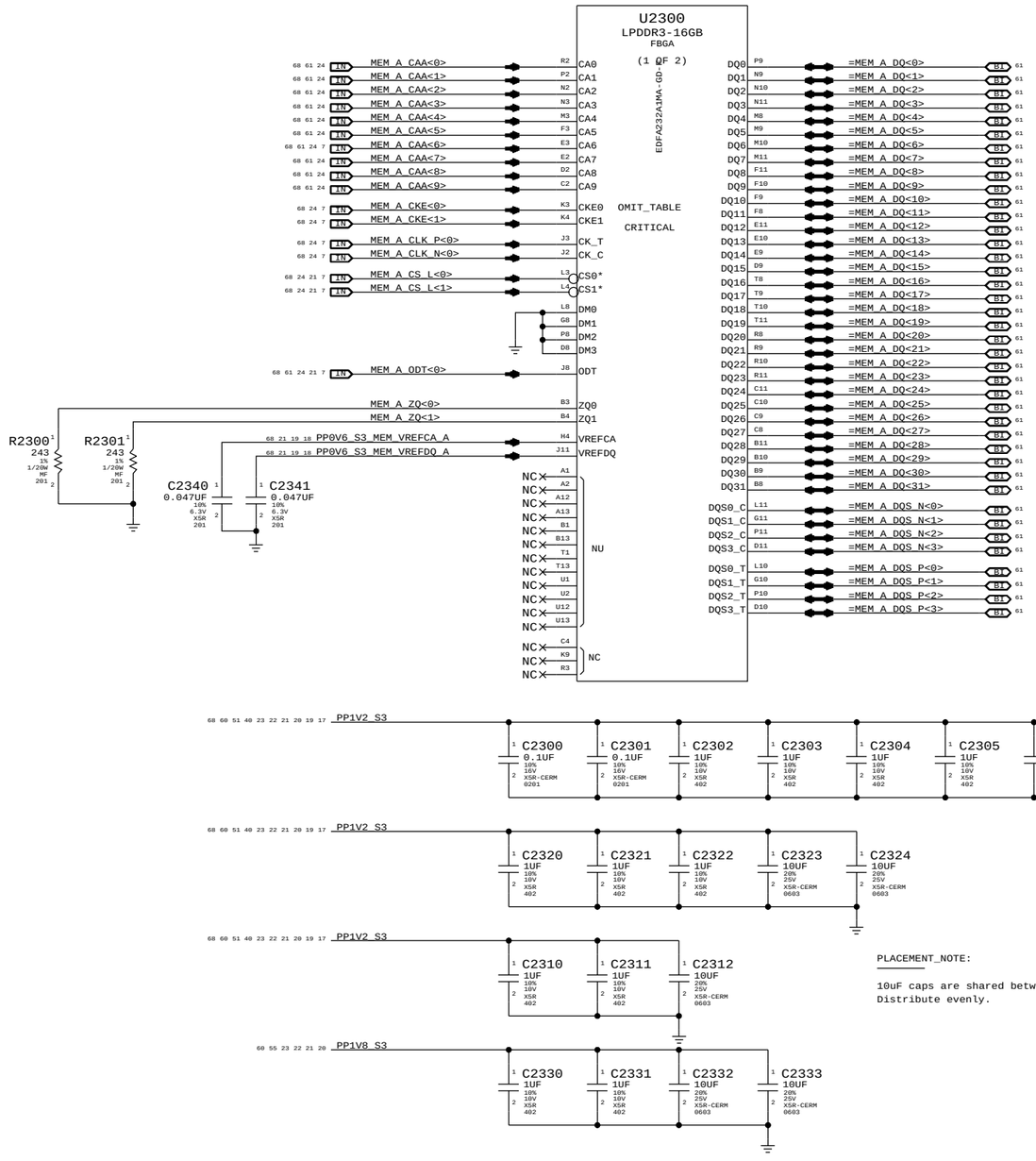
DDRVREF_DAC R2212 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=WILL_J43 SYNC_DATE=02/04/2013
PAGE TITLE: DDR3 VREF MARGINING
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 22 OF 120
SHEET: 19 OF 73

LPDDR3 CHANNEL A (0-31)



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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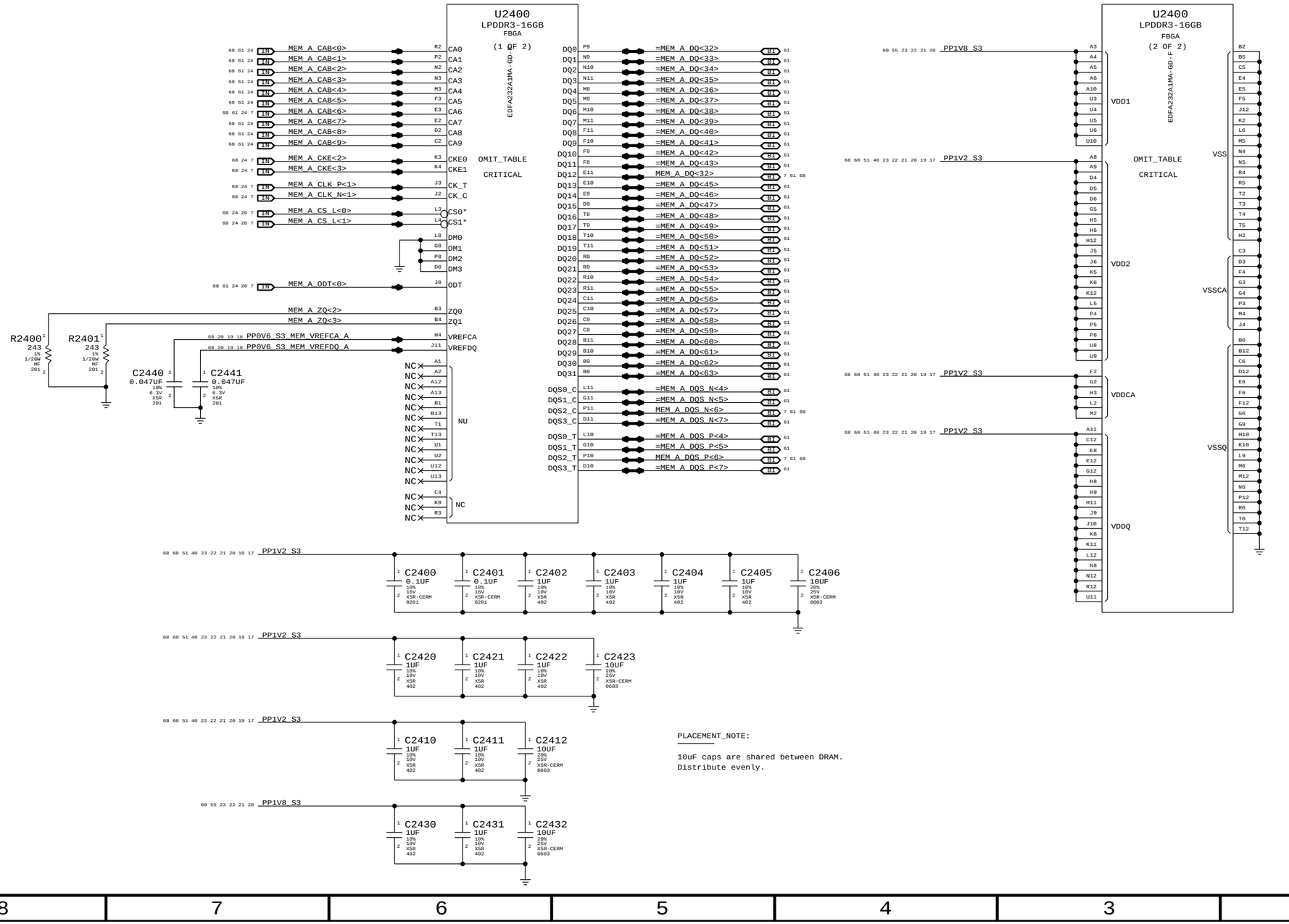
SHEET 20 OF 73

LPDDR3 CHANNEL A (32-63)



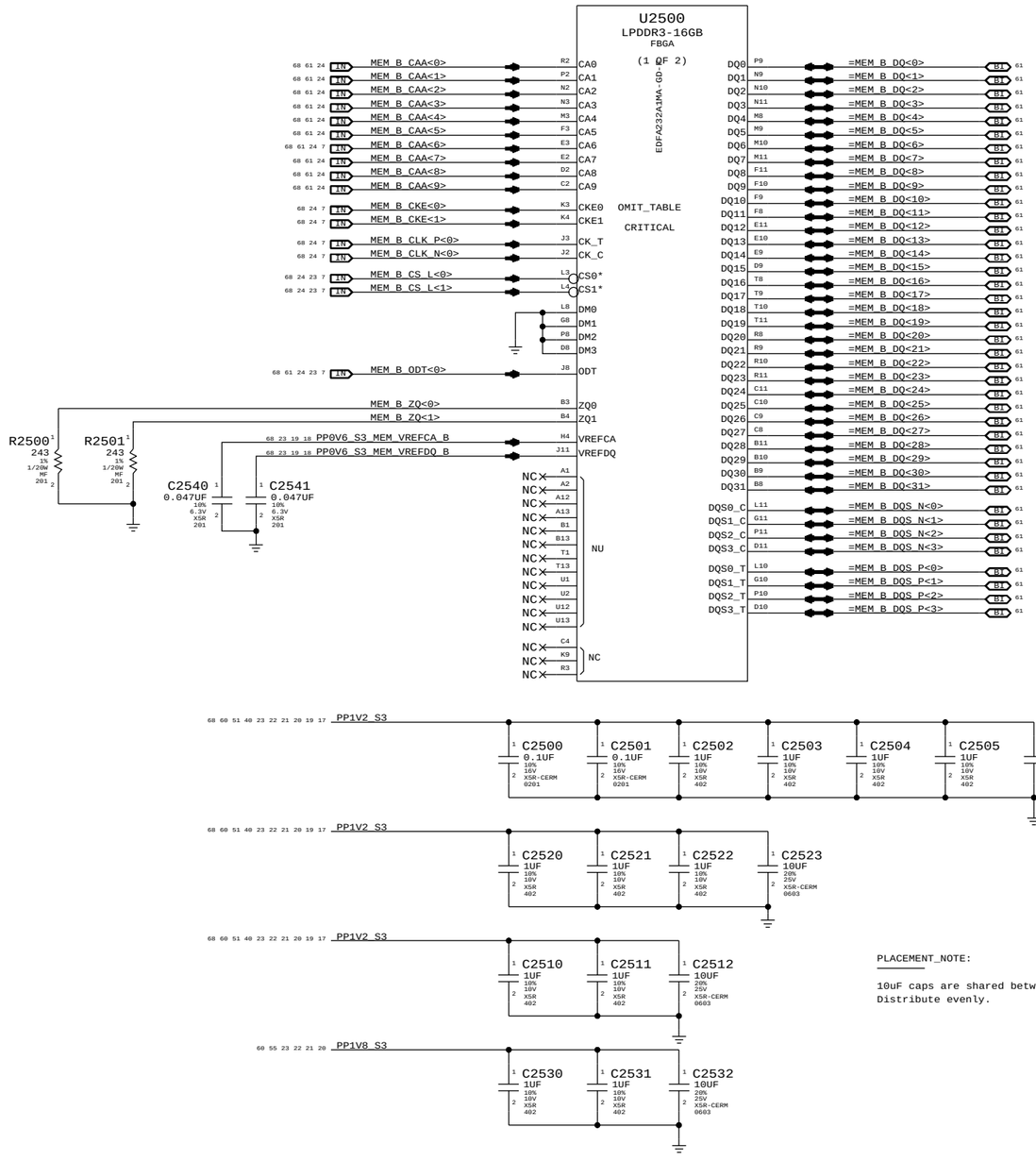
SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 24 OF 120
SHEET 21 OF 73

LPDDR3 CHANNEL B (0-31)



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: LPDDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 25 OF 120

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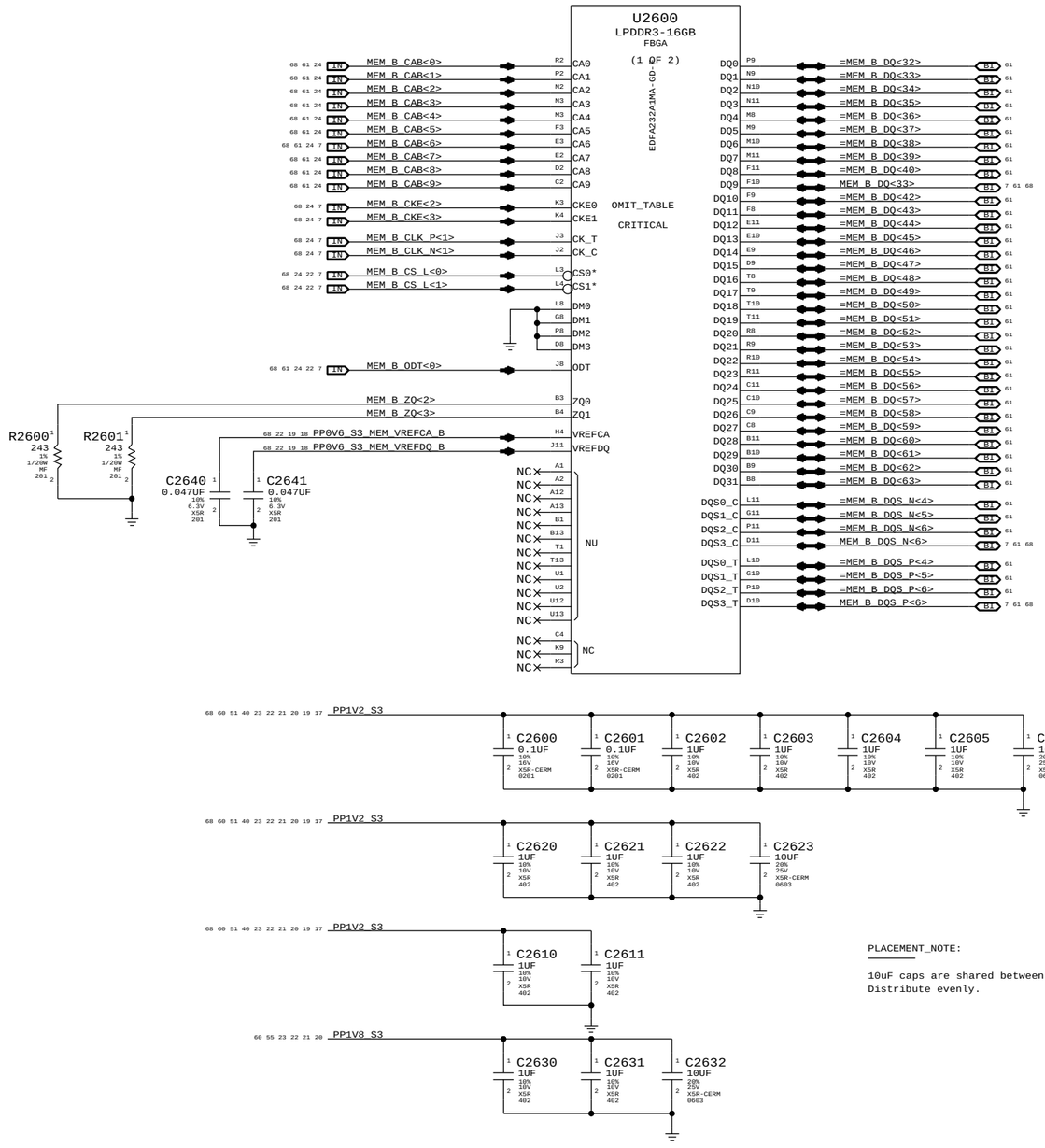
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

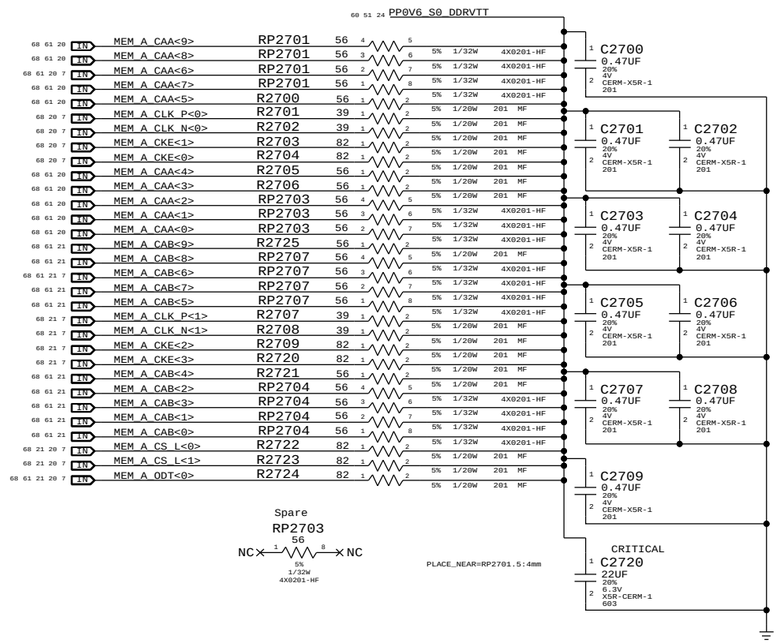
SYNC_MASTER=MASTER SYNC_DATE=MASTER

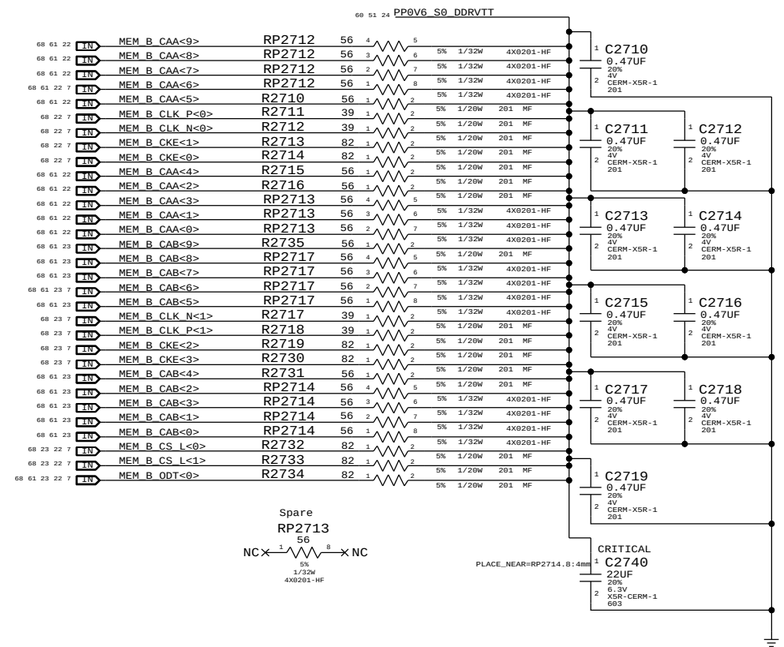
PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 26 OF 120
SHEET 23 OF 73

Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC MASTER=J43_MLB SYNC DATE=09/21/2012

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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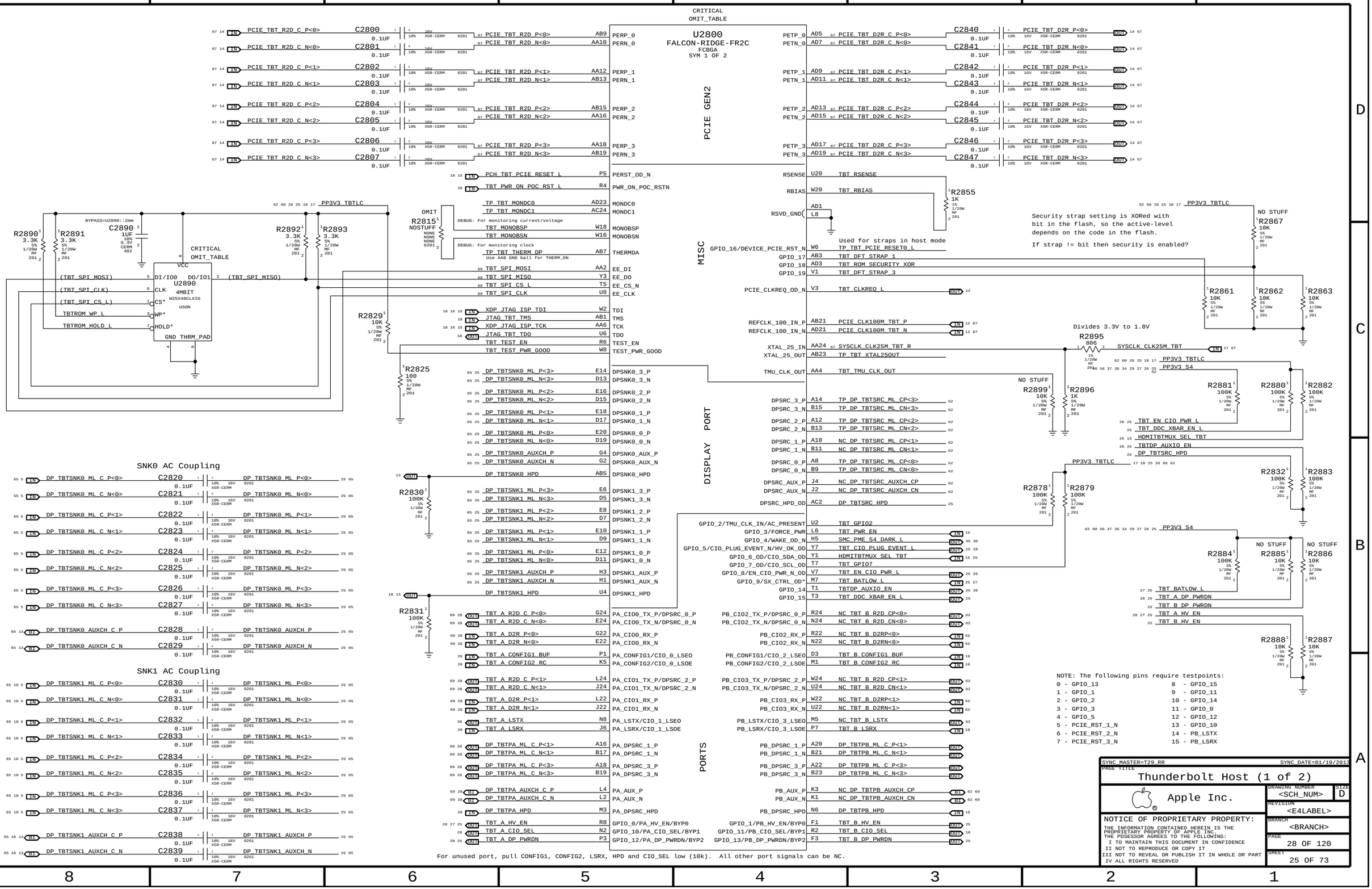

SYNC_MASTER=T29_RR SYNC_DATE=01/19/2013

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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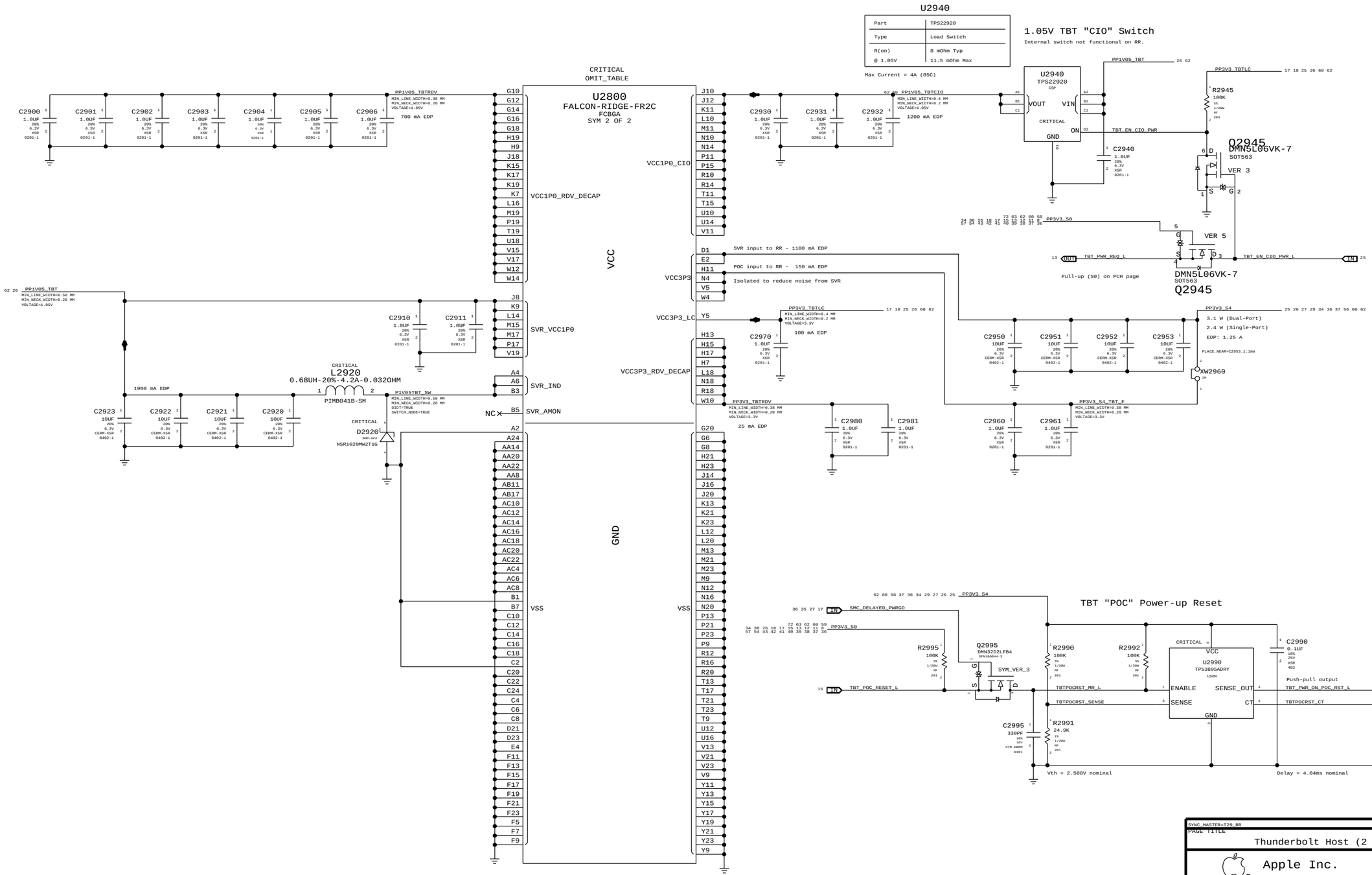

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=T29_RR SYNC_DATE=12/17/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 29 OF 120
SHEET: 26 OF 73

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required
for 2S.

CRITICAL
Q3080
SI8409DB
BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_S4SW_TBTBST_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 25V X5R 402
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_DIV_L
TBTBST_PWREN_L

Q3005
DMN32D2LFB4
SYM_VER_2
TBT_A_HV_EN

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095
6.8UH-4.0A
PIMB062D-SM

CRITICAL
D3095
POWERDI-123
DFLS230L

PP15V_TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

R3089 0 5% 1/20W MF 0201

TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

TBTBST_SNS2
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

XW3095 SM
TBTBST_VSNS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
PLACE_NEAR=C3095.1:2 mm

R3091 200K 1% 1/20W MF 201 <R1>

CRITICAL
U3090
LT3957
QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
GND_TBTBST_SGND
TBTBST_VC_RC
TBTBST_FBX
TBTBST_VSNS_RC

C3081 2.2UF 20% 10V X5R-CERM 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3087 47PF 5% 25V NPO-C0G-CERM 0201
R3093 10K 1% 1/20W MF 201
R3092 73.2K 1% 1/20W MF 201 <R2>
C3082 2.2UF 20% 10V X5R-CERM 402
C3093 3300PF 10% 10V X7R-CERM 0201
R3094 41.2K 1% 1/20W MF 201
C3094 0.33UF 10% 6.3V CERM-X5R 402

SGND shorted to GND inside package, no XW necessary.

R3090 49.9K 1% 1/16W MF-LF 402
C3088 22PF 5% 50V CERM 0402
R3095 133K 1% 1/16W MF-LF 402 <Ra>
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>

C3095 10UF 20% 25V X5R-CERM 0603
C3097 10UF 20% 25V X5R-CERM 0603
C3096 10UF 20% 25V X5R-CERM 0603
C3098 10UF 20% 25V X5R-CERM 0603
C3084 10UF 20% 25V X5R-CERM 0603
C3309A 10UF 20% 25V X5R-CERM 0603
C3099 0.001UF 10% 50V X7R-CERM 0402
C3085 10UF 20% 25V X5R-CERM 0603
C3309B 10UF 20% 25V X5R-CERM 0603

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Vout = 1.6V * (1 + Ra / Rb)

Q3088
DMN5L06VK-7
SOT563
VER 3
Max Vgs: 10V

R3088 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201

Q3088
DMN5L06VK-7
SOT563
VER 3

SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000
DMN32D2LFB4
SYM_VER_3

PP3V3_S4
PM_BATLOW_L
Pull-up on RR page
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=WILL_J43	SYNC_DATE=12/17/2012
PAGE TITLE	TBT Power Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5 — CRITICAL
C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V XSR-CERM-1 603
C3281 0.1UF 10% 16V XSR-CERM 0201

PP15V_TBT — 15.75V Max

U3210 CRITICAL
CD3211A1RGP QFN
V3P3 (19,20) → V3P3OUT (18)
VHV (6,7) → OUT (12,14)
ENHVU (16)
EN (5) ← S4_PWR_EN
HV_EN (11) ← TBT_A_HV_EN
S0 (17) ← PM_SLP_S3_BUF_L
FAULTZ (4)
ISET_V3P3 (8) ← TBTAPWRSW_ISET_V3P3
ISET_S0 (10) ← TBTAPWRSW_ISET_S0
ISET_S3 (9) ← TBTAPWRSW_ISET_S3
GND, THRM PAD (1,2,3,13,15,21)

C3215 4.7UF 10% 25V XSR-CERM 0603
C3210 0.1UF 10% 25V XSR 402
C3285 0.1UF 10% 16V XSR-CERM 0201
C3286 10UF 20% 6.3V CERM-XSR 0402
C3211 0.1UF 10% 25V XSR 402

PP3V3_S4_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V → 28 60
PP3V3RHV_S4_TBTAPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

12V: See below

R3210 22.6K 1% 1/20W MF 201 — TBTHV:P15V
R3211 22.6K 1% 1/20W MF 201 — TBTHV:P15V
R3212 36.5K 1% 1/20W MF 201 → <RV3P3>
R3213 22.6K 1% 1/20W MF 201 — TBTHV:P15V → <RHVS3>
R3214 22.6K 1% 1/20W MF 201 — TBTHV:P15V → <RHVS0>

TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

Single-fault protection requires two R's per HV ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

CRITICAL
L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V
R3201 12 5% 1/20W MF 201

TBT Dir / DP Dir

J3200 MDP-J11 F-RT-TH
CRITICAL 514-0818
HOT_PLUG_DETECT (2)
CONFIG1 (4)
CONFIG2 (6)
GND (13)
ML_LANE3P (10)
ML_LANE3N (12)
GND (14)
AUX_CHP (16)
AUX_CHN (18)
DP_PWR (20)
GND (1,3,5,7,9,11,15,17,19)
ML_LANE0P (3)
ML_LANE0N (5)
ML_LANE1P (9)
ML_LANE1N (11)
ML_LANE2P (15)
ML_LANE2N (17)
RETURN (19)
SHIELD PINS (20,27,26,25,24,23,22,21)

TBTACONN_1_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V
(0-18.9V)
C3205 0.01UF 10% 25V XSR-CERM 0201
C3206 0.01UF 10% 25V XSR-CERM 0201
TBTACONN_7_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V

TBT: TX_0
TBT: LSX_R2P/P2R (P/N)
TBT: TX_1

C3270 0.22UF 20% 6.3V XSR 0201
C3271 0.22UF 20% 6.3V XSR 0201
C3272 0.22UF 20% 6.3V XSR 0201
C3273 0.22UF 20% 6.3V XSR 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

C3274 0.47UF 20% 4V CERM-XSR-1 201
C3275 0.47UF 20% 4V CERM-XSR-1 201
C3276 0.47UF 20% 4V CERM-XSR-1 201
C3277 0.47UF 20% 4V CERM-XSR-1 201
C3278 0.22UF 20% 6.3V XSR 0201
C3279 0.22UF 20% 6.3V XSR 0201
C3230 0.1UF 10% 16V XSR-CERM 0201
C3231 0.1UF 10% 16V XSR-CERM 0201
C3232 0.22UF 20% 6.3V XSR 0201
C3233 0.22UF 20% 6.3V XSR 0201

R3294 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201

C3202 0.01UF 10% 16V XSR-CERM 0201
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

C3220 0.1UF 10% 16V XSR-CERM 0201
U3220 CRITICAL CBTL05024 HVQFN24-COMBO SIGNAL_MODEL=TBT_MUX
VDD (7)
TB- (7) ← DP_TBTSNK0_DDC_DATA
TB+ (8) ← DP_TBTSNK0_DDC_CLK
AUX- (1) ← DP_TBTPA_AUXCH_N
AUX+ (2) ← DP_TBTPA_AUXCH_P
DDC_DAT (4) → TBT_A_CONFIG1_BUF
DDC_CLK (5) ← TBT_A_CONFIG1_RC
CA_DETOUT (16) → TBT_A_CA_DET
DP+ (11) ← DP_TBTPA_ML_P<1>
DP- (10) ← DP_TBTPA_ML_N<1>
LSTX (IPU) (14) ← TBT_A_LSTX
LSRX (IPO) (13) → TBT_A_LSRX
HPDOUT (12) → DP_TBTPA_HPD
TB_ENA (15) ← TBT_A_CIO_SEL
AUXIO_EN (24) ← TBTDP_AUXIO_EN
DP_PD (6) ← TBT_A_DP_PWRDN
(IPU) AUXIO- (23) ↔ TBT_A_D2R1_AUXDDC_N
(IPD) AUXIO+ (22) ↔ TBT_A_D2R1_AUXDDC_P
DPML0+ (19) → DP_A_LSX_ML_P<1>
DPML0- (20) → DP_A_LSX_ML_N<1>
HPD (17) → TBT_A_HPD
GND, THMPAD (9,21,25)

TBT: RX_0
TBT: Unused
TBT: RX_1
TBT: TX_0
TBT: LSX_R2P/P2R (P/N)
TBT: TX_1
TBT: RX_1

SYNC_MASTER=T29_RR	SYNC_DATE=10/26/2012
PAGE TITLE: Thunderbolt Connector A	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 32 OF 120
	SHEET: 28 OF 73

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
35 36 37 39 62

PP3V3_WLAN_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
Max Current = 2A (85C)

U3550
TPS22924
CSP
CRITICAL
A1 VOUT
B1
A2 VIN
B2 ON
C2
GND
C1

PP3V3_S5
8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 62 72

SMC_WIFI_PWR_EN
IN 29 35 37

C3550
1.0UF
20%
6.3V
X5R
0201-1

514S0335
CRITICAL
J3501
SSD-K99
F-RT-SM1

C3521
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:5mm

AIRPORT

67 62 PCIE_AP_R2D_N — C3531 0.1UF 10% XSR-CERM 16V 0201 — PCIE_AP_R2D_C_N OUT 35 36 62
67 62 PCIE_AP_R2D_P — C3530 0.1UF 10% XSR-CERM 16V 0201 — PCIE_AP_R2D_C_P OUT 35 36 62
PCIE_CLK100M_AP_N IN 12 62 67
PCIE_CLK100M_AP_P IN 12 62 67
PCIE_AP_D2R_P IN 14 62 67
PCIE_AP_D2R_N IN 14 62 67

PP3V3_S4
25 26 27 29 34 36 37 56 60 62

C3532
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:1.5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

PP3V3_S5
8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 62 72

C3540
0.1UF
10%
6.3V
CERM-X5R
0201

APCLKRQ:ISOL
R3553
100K
5%
1/20W
MF
201

R3554
232K
1%
1/20W
MF
201

P3V3WLAN_VMON

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

R3558
0
5%
1/20W
MF
0201

62 AP_RESET_CONN_L — AP_RESET_CONN_R_L — AP_RESET_L IN 15

SMC_WIFI_PWR_EN IN 29 35 37

62 AP_CLKREQ_Q_L — AP_CLKREQ_R_L

R3555
100K
1%
1/20W
MF
201

APCLKRQ:ISOL
R3556
0
5%
1/20W
MF
0201

APCLKRQ:BIDIR
R3557
0
5%
1/20W
MF
0201

AP_CLKREQ_L BI 12

NOSTUFF
R3559
0
5%
1/20W
MF
0201

PCIe Wake Muxing

56 57 58 13 15 16 17 18 PP3V3_S5
72 62 60

R3561
100K
5%
1/20W
MF
201

C3560
0.1UF
10%
6.3V
CERM-X5R
0201

U3560
NC7SB3157P6XG
SC70
VER-3
CRITICAL
VCC
GND
S
B0
B1
A

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

AP_S0IX_WAKE_SEL IN 15
PCIE_WAKE_L OUT 13 31 62
AP_S0IX_WAKE_L OUT 15
AP_PCIE_WAKE_L

NOSTUFF
R3560
0
5%
1/20W
MF
0201

36 34 29 27 26 25 22 60 59 57 PP3V3_S4

BLUETOOTH

C3510
0.1UF
10%
6.3V
CERM-X5R
0201

U3510
USB3740
DFN
CRITICAL
VDD
DP
DM
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
NC

66 62 USB_BT_CONN_P
66 62 USB_BT_CONN_N
USB_BT_P BI 14 66
USB_BT_N BI 14 66
BT_WAKE
PM_SLP_S4_L IN 13 18 34 35 57

SIGNAL_MODEL=BT_MUX

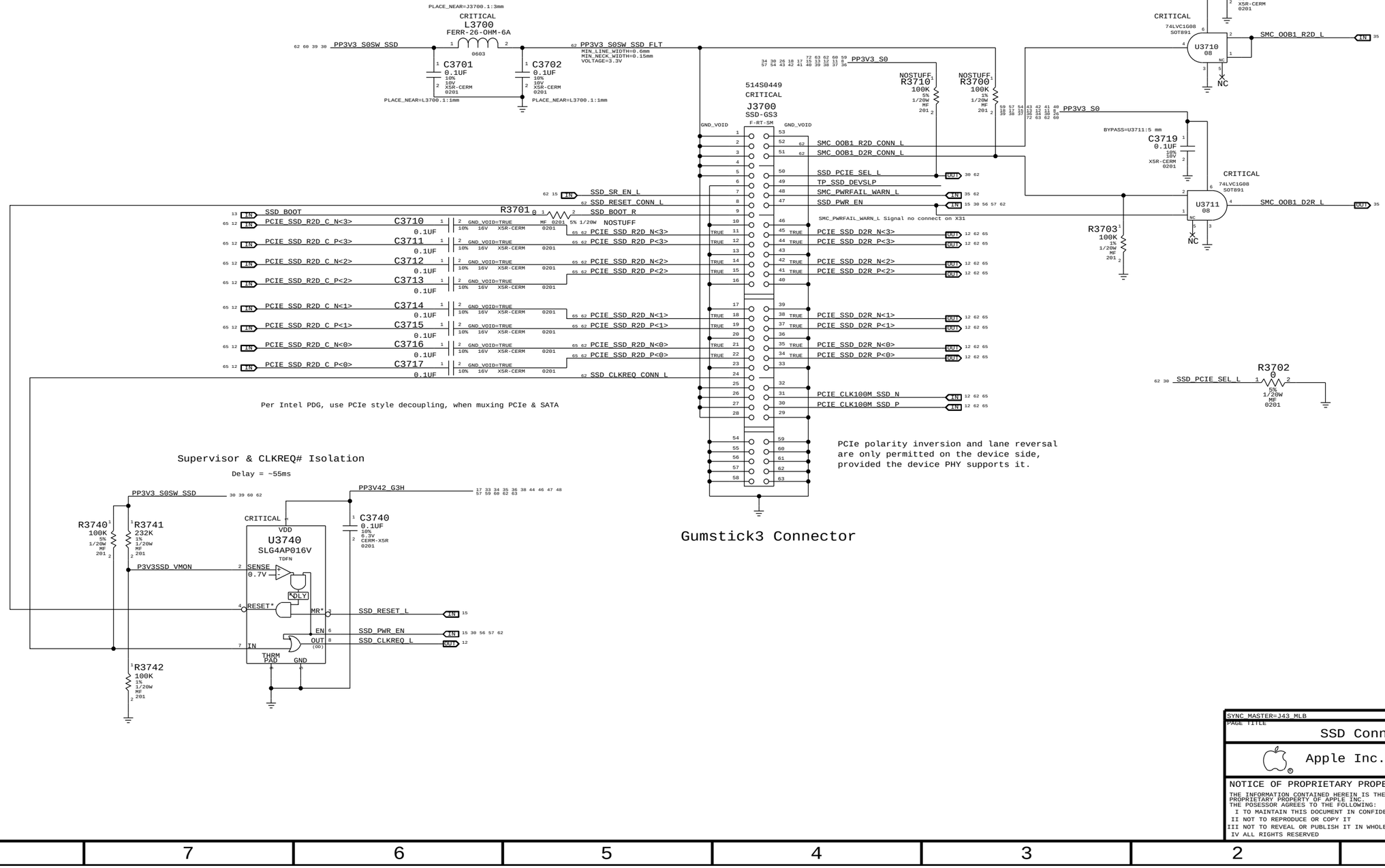
SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

NO_XNET_CONNECTION=TRUE
Q3510
DMN32D2LFB4
DFN1006H-3
SYM_VER_2
D
G
S

SMC_PME_S4_WAKE_L OUT 34 35 37

R3512
15K
1%
1/20W
MF
201

SYNC_MASTER=J43_MLB
SYNC_DATE=10/02/2012
PAGE TITLE
Wireless Connector
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 35 OF 120
SHEET 29 OF 73



SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

SSD Connector

Apple Inc.

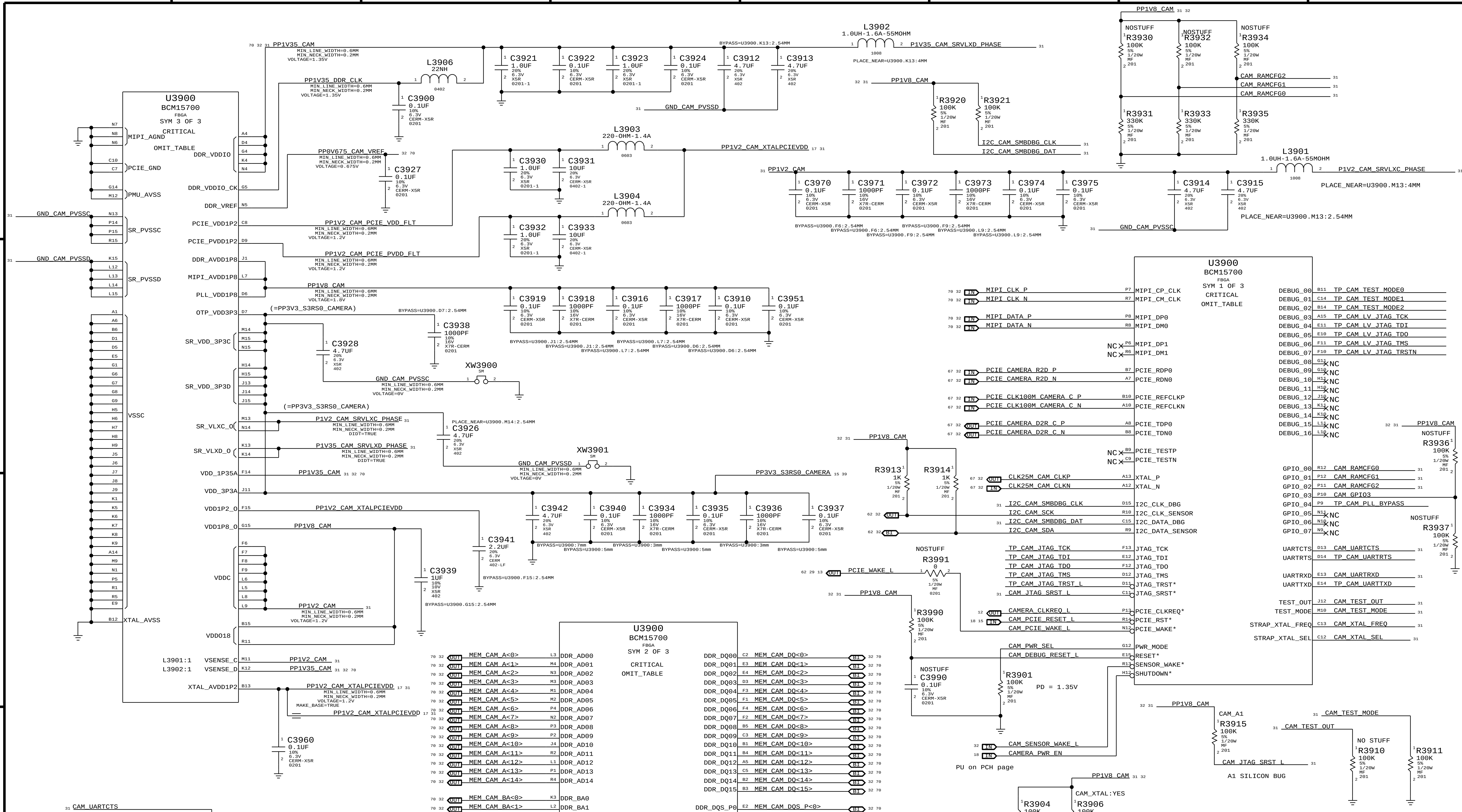
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 37 OF 120

SHEET 30 OF 73



SYNC_MASTER=J43_MLB1 SYNC_DATE=01/09/2013

PAGE TITLE

Camera 1 of 2

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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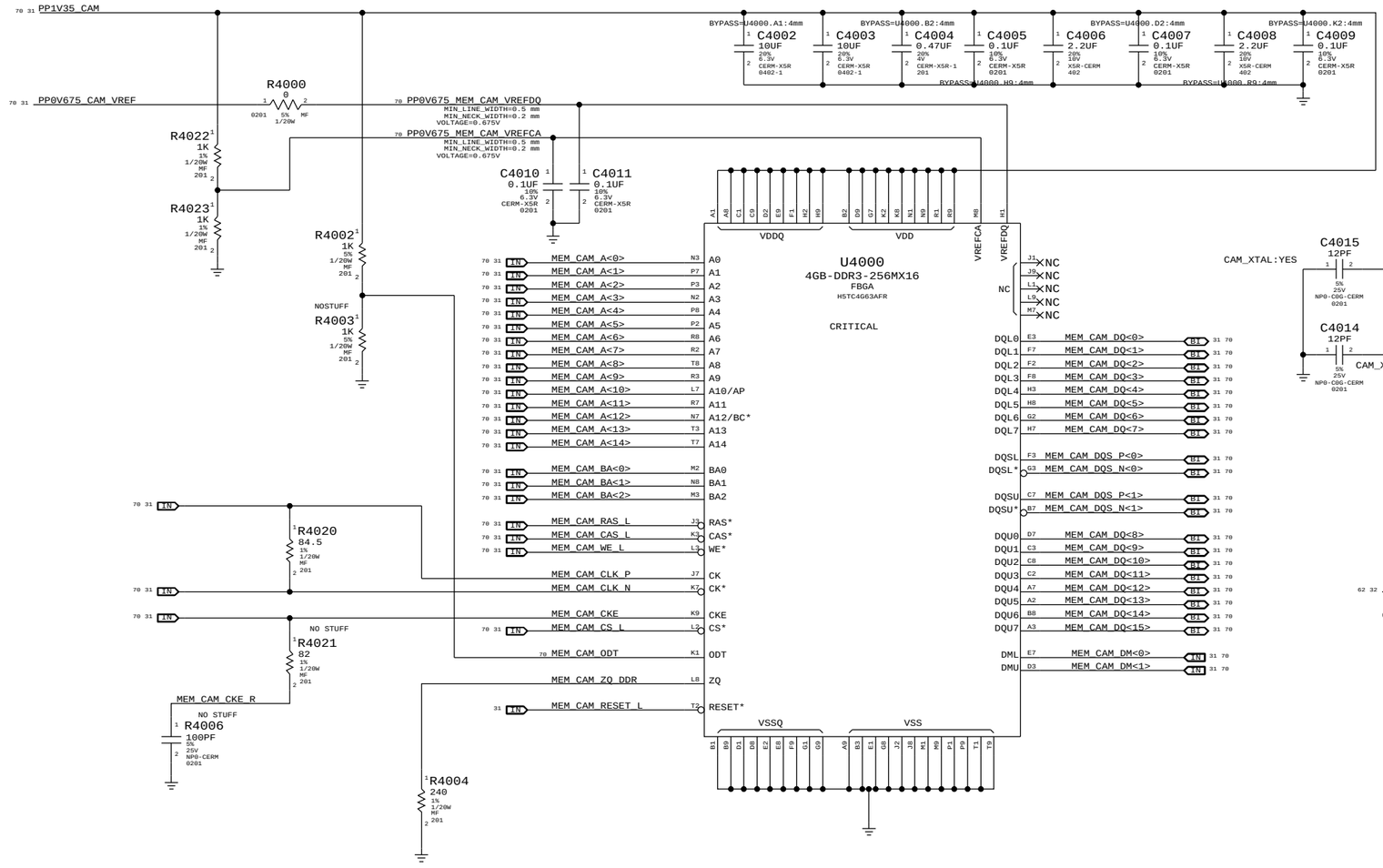
SHEET 31 OF 73



SYNC_MASTER=J43_MLB
SYNC_DATE=09/14/2012

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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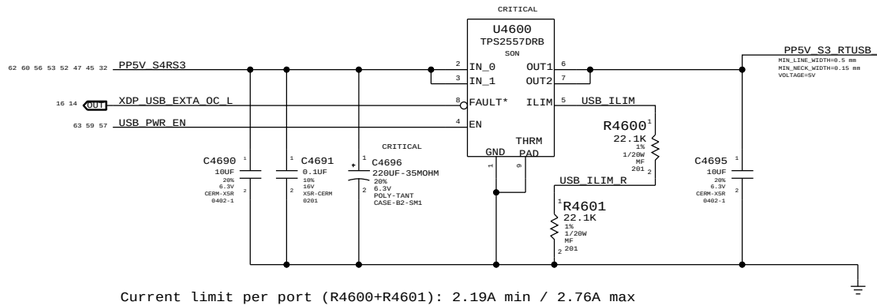
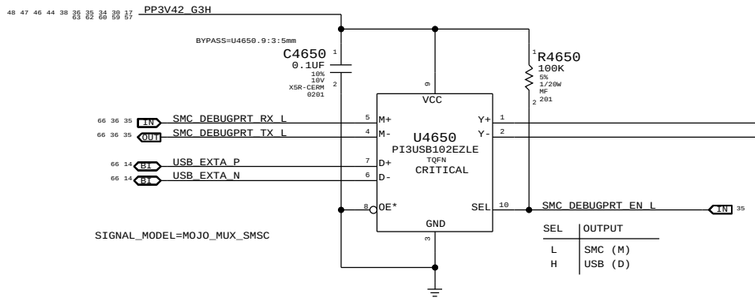
Right USB Port A

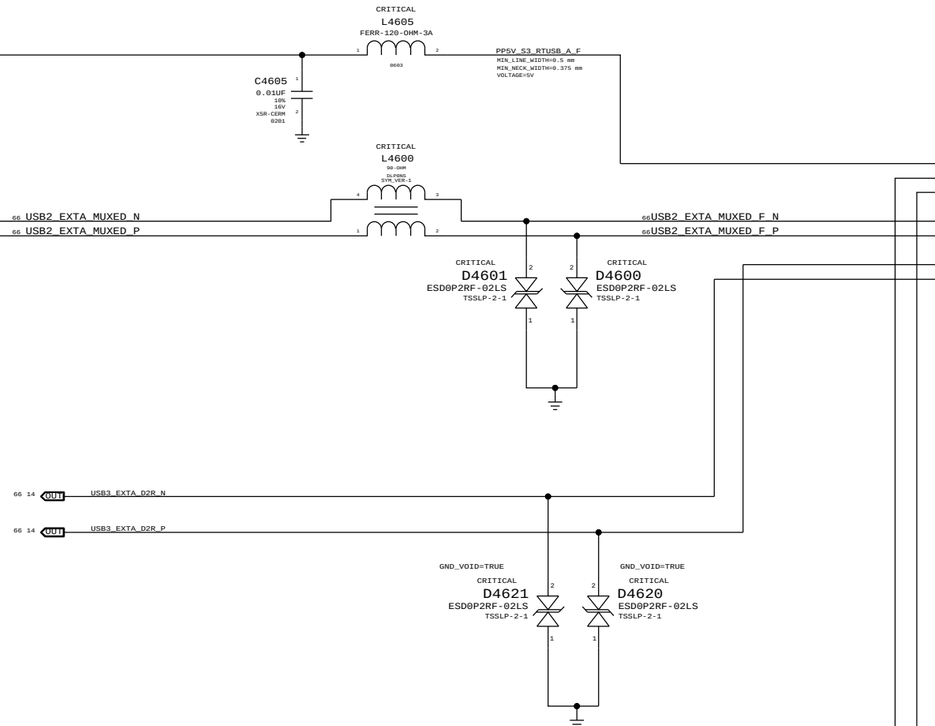
USB Port Power Switch



Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux





APN: 514-0819

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

External A USB3 Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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IPD Flex Connector

R4830 0 5% 1/20W MF 0201
C4800 0.1UF 10% 6.3V CERM-X5R 0201
L4820 FERR-120-OHM-1.5A 0402-LF
C4810 0.1UF 10% 16V X5R-CERM 0201
C4820 0.1UF 10% 6.3V CERM-X5R 0201
R4841 0 5% 1/20W MF 0201
R4843 0 5% 1/20W MF 0201
R4844 0 5% 1/20W MF 0201
Q4800 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
R4842 0 5% 1/20W MF 0201
C4841 0.1UF 10% 6.3V CERM-X5R 0201
U4810 74LVC2G08GT SOT833 08
R4810 100K 5% 1/20W MF 201
Q4860 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
R4860 100K 5% 1/20W MF 201

R4850 33 5% 1/20W MF 201
R4851 33 5% 1/20W MF 201
R4852 33 5% 1/20W MF 201
R4853 33 5% 1/20W MF 201

C4832 100PF 5% 25V NP0-CERM 0201
C4833 100PF 5% 25V NP0-CERM 0201
C4834 100PF 5% 25V NP0-CERM 0201
C4835 100PF 5% 25V NP0-CERM 0201
C4836 100PF 5% 25V NP0-CERM 0201

CRITICAL
518S0884
J4800 TF13BS-20S-0.4SH F-RT-SM-1

1		IN	SMC_LID
2	TPAD_SPI_MISO	OUT	TPAD_SPI_MISO_R
3			
4	USB_TPAD_P	BI	
5	USB_TPAD_N	BI	
6			
7	TPAD_SPI_CLK	IN	TPAD_SPI_CLK_R
8			TPAD_WAKE_L
9	TPAD_SPI_MOSI	IN	TPAD_SPI_MOSI_R
10			PP3V3_S4_IPD
11			TPAD_SPI_CS_R_L
12			TPAD_SPI_IF_EN_CONN
13			TPAD_SPI_INT_S4_WAKE_L_CONN
14			PP5V_S4_IPD
15			TPAD_USB_IF_EN_CONN
16	SMBUS_SMC_3_SDA	BI	
17	SMBUS_SMC_3_SCL	BI	
18	SMC_LSOC_RST_L	OUT	
19	(=PP3V42_G3H_IPD)		
20	SMC_ONOFF_L	OUT	
21			

SMC_PME_S4_WAKE_L — To SMC
TPAD_SPI_INT_L — To PCH
PM_SLP_S4_L — From PCH
TPAD_USB_IF_EN — From PCH
TPAD_SPI_IF_EN — From PCH
TPAD_SPI_CS_L
TPAD_SPI_CS_CONN_L

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013
PAGE TITLE: IPD Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 48 OF 120
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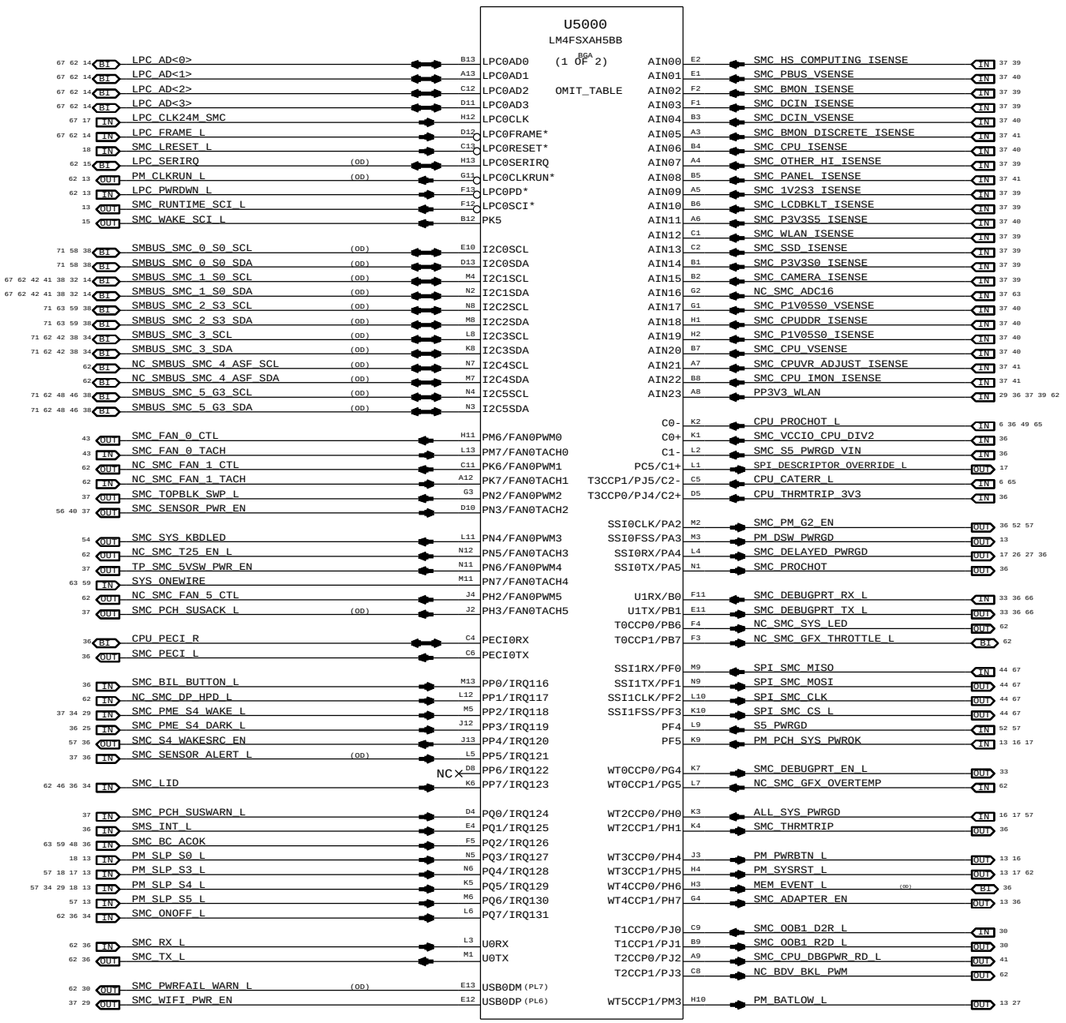
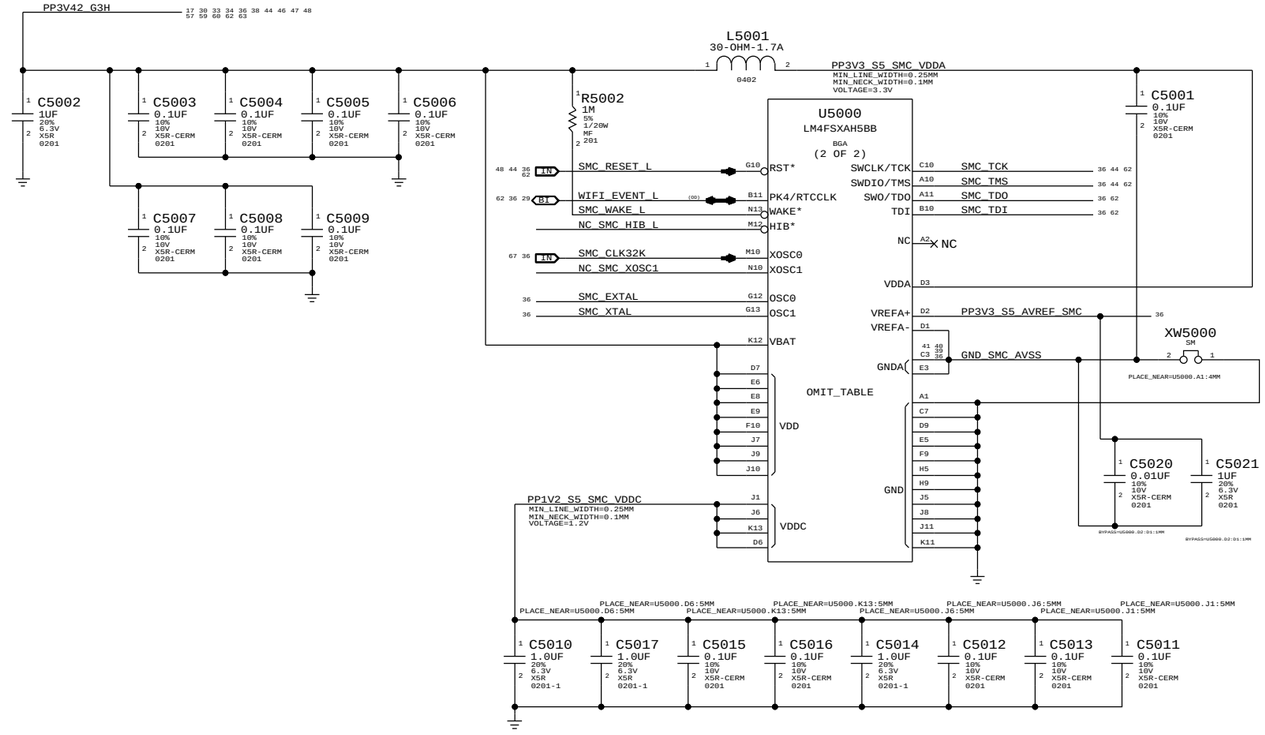


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



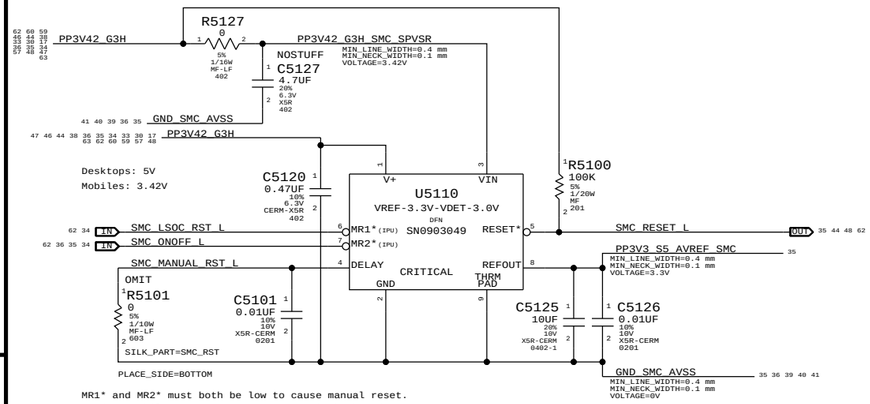
SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE
SMC

Apple Inc.

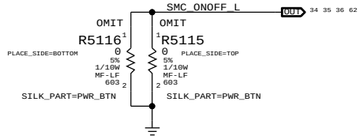
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 50 OF 120
SHEET 35 OF 73

SMC Reset "Button", Supervisor & AVREF Supply



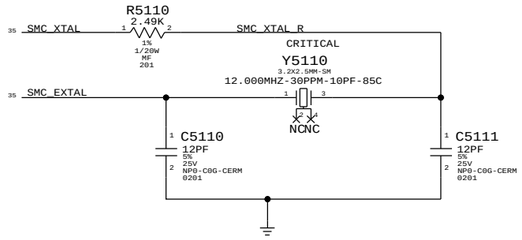
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

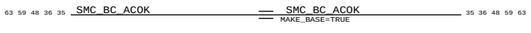
Debug Power "Buttons"

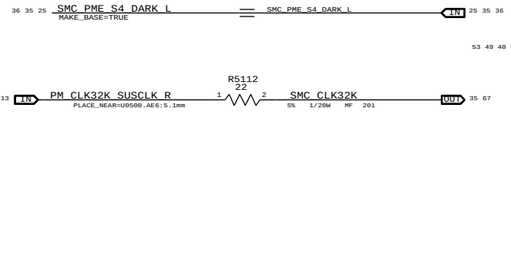


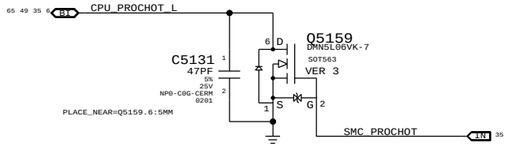
SMC Crystal Circuit

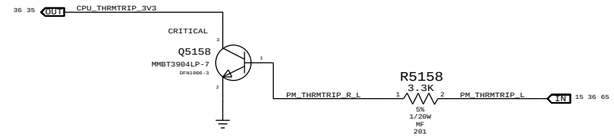
SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz



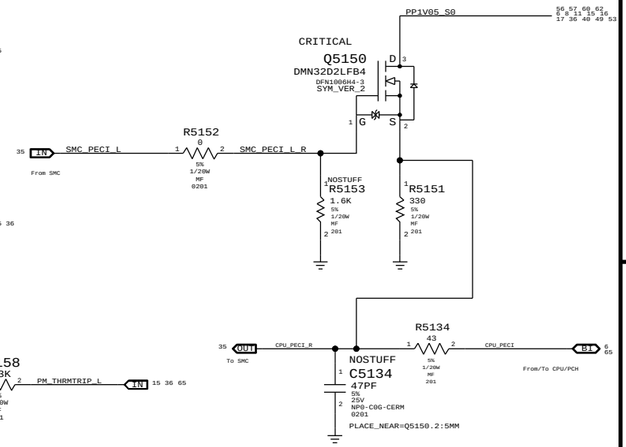


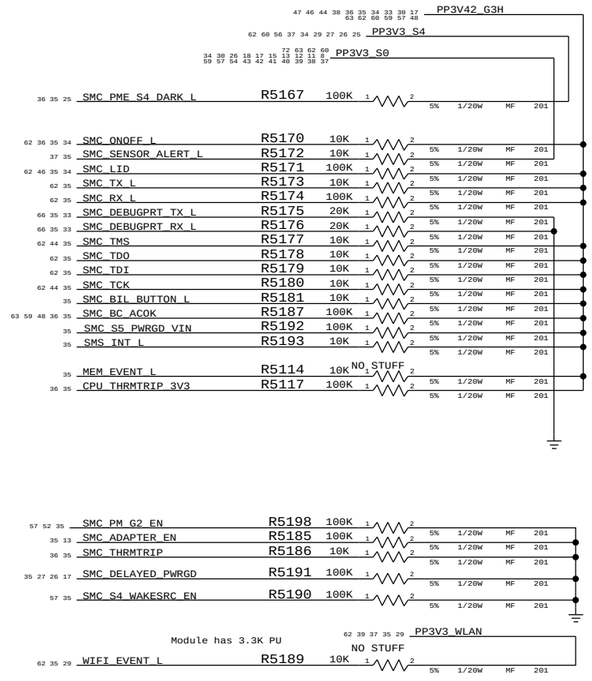






SMC12 PECI Support





SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 51 OF 120
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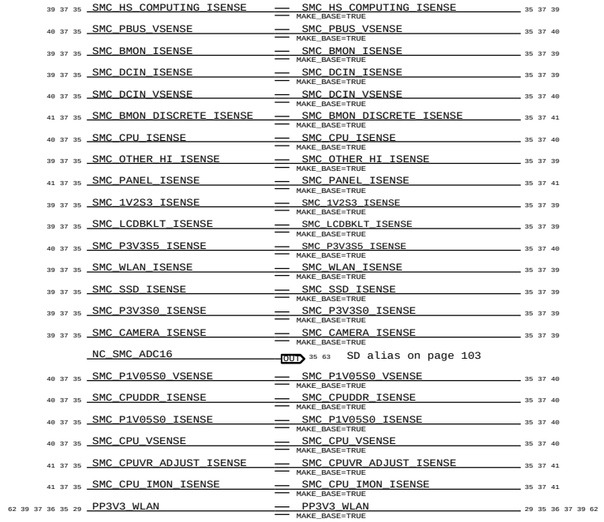
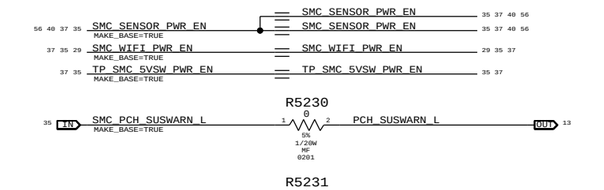
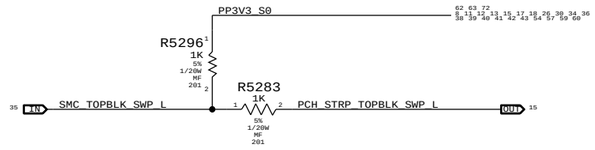
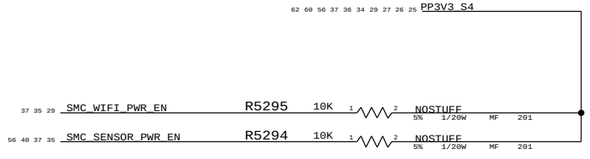
8	7	6	5	4	3	2	1

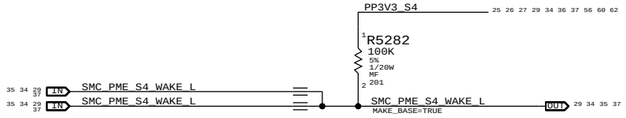


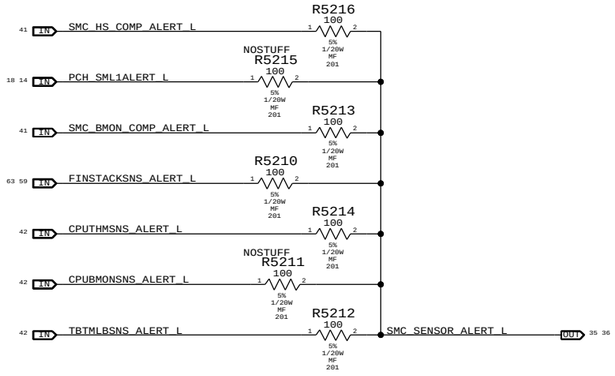


Top-Block Swap









SYNC_MASTER=J43_MLB	SYNC_DATE=02/20/2013
PAGE TITLE: SMC Project Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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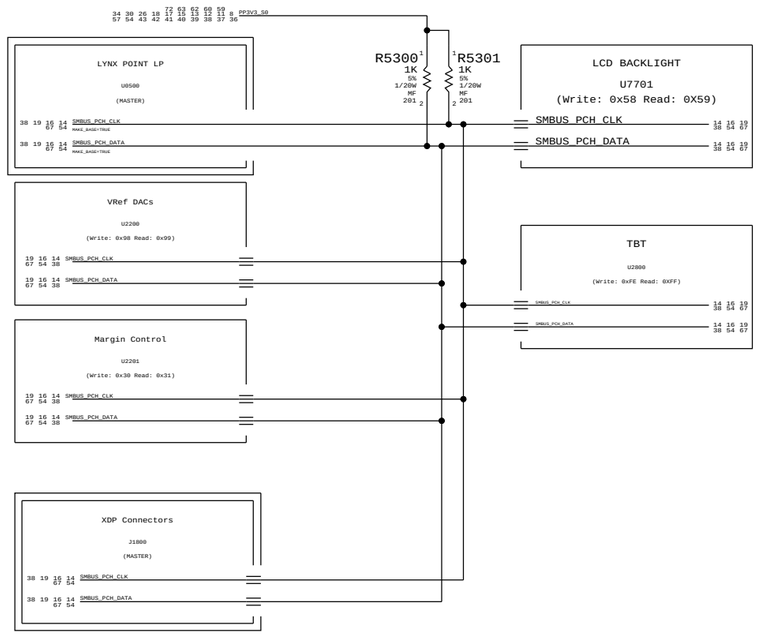
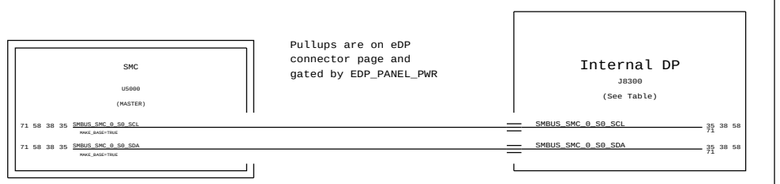
	SHEET: 37 OF 73

LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

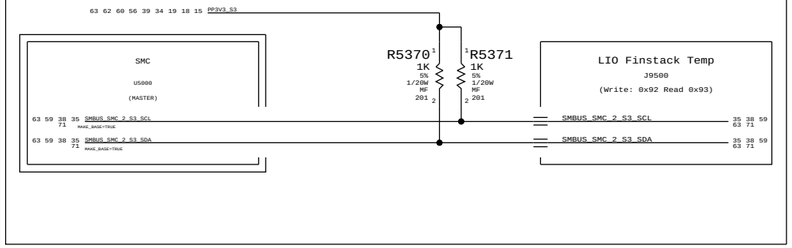


(* = Multiple options)

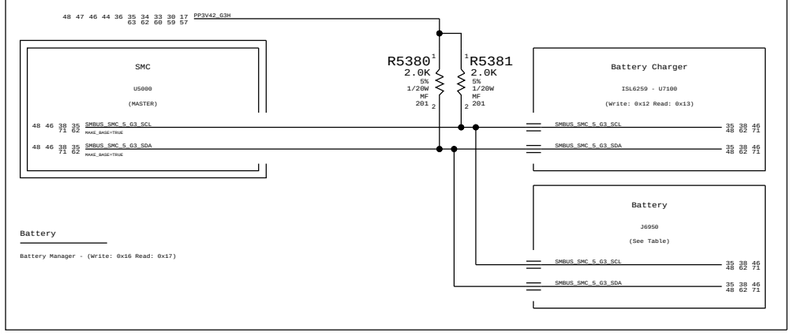
Internal DP

		J43			J41	
		Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x8B)	N	Y	*	Y	*	
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*	
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	*	Y	N	

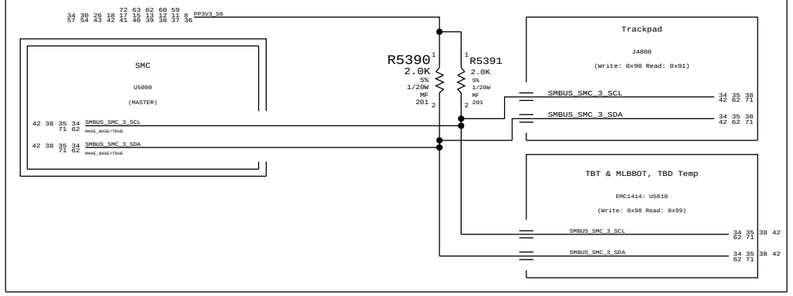
SMC "2" SMBus S3 Connections



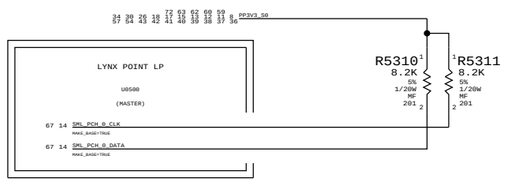
SMC "5" SMBus G3H Connections



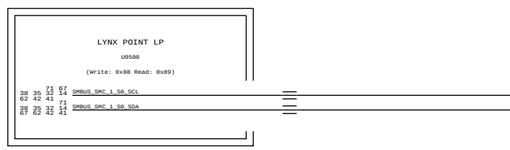
SMC "3" SMBus S0 Connections



LYNX POINT LP S0 "SMLink 0" Connections



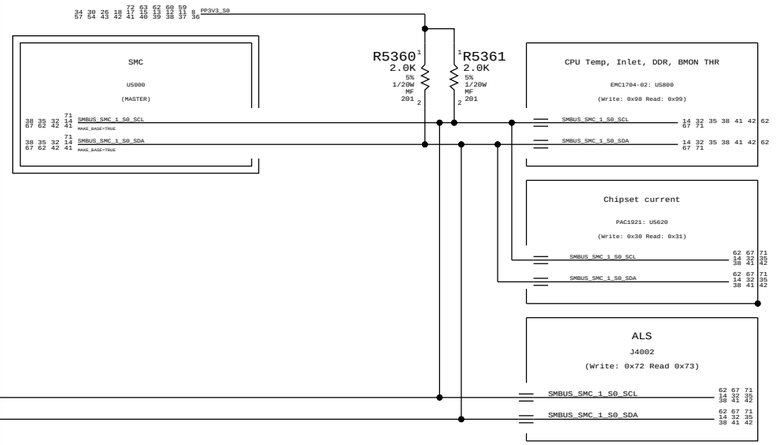
LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to

access PCH

SMC S0 "1" SMBus Connections



SYNC_MASTER=J43_MLB SYNC_DATE=09/28/2012

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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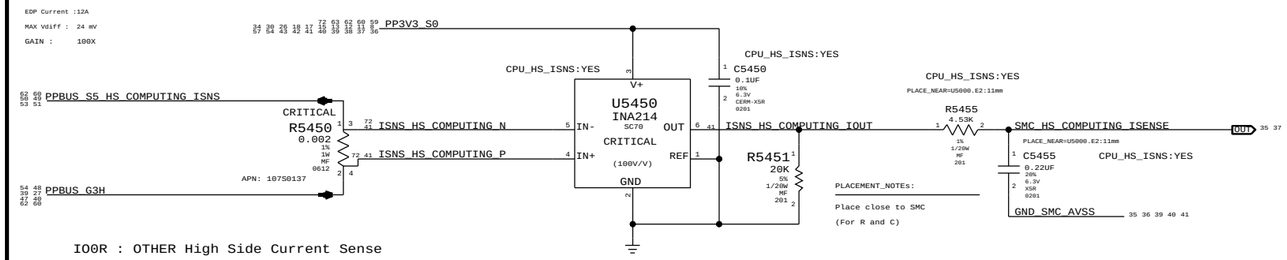
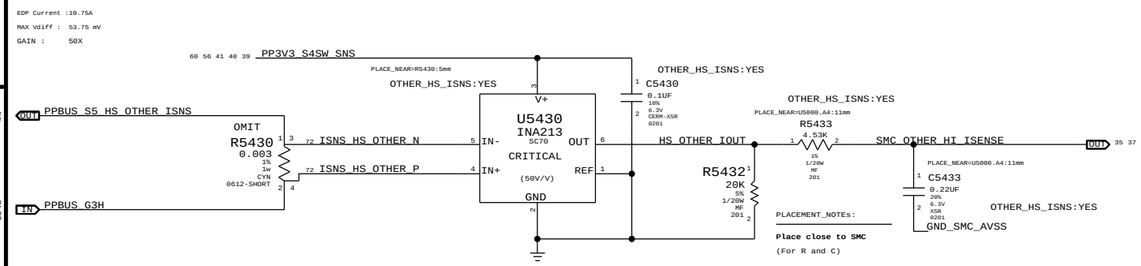
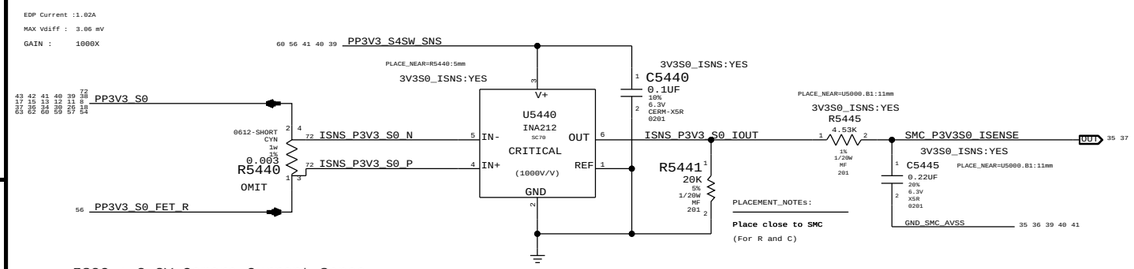
IC0R : COMPUTING High Side Current Sense



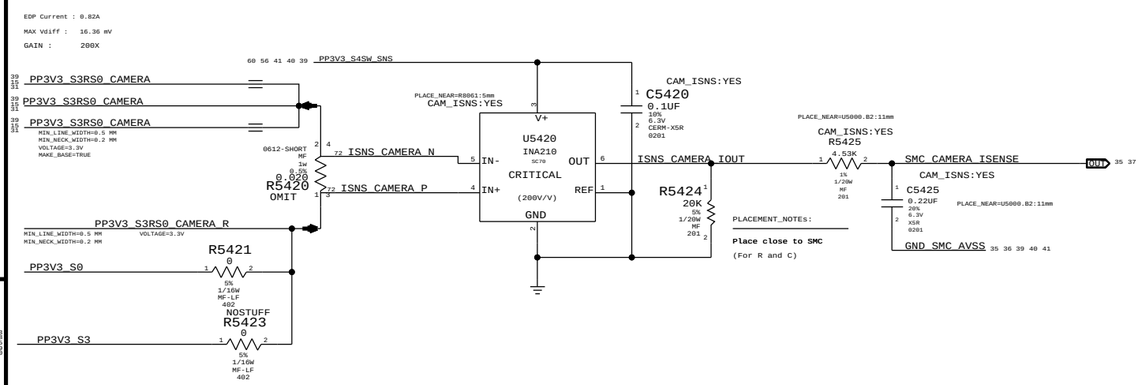
IO0R : OTHER High Side Current Sense



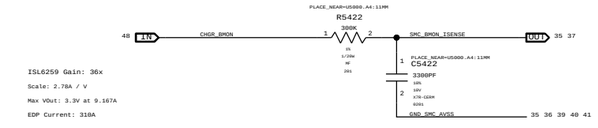
IR0C : 3.3V S0 FET Current Sense



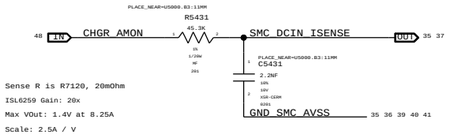
IS2C : 3.3V Camera Current Sense



CHARGER BMON High Side Current Sense

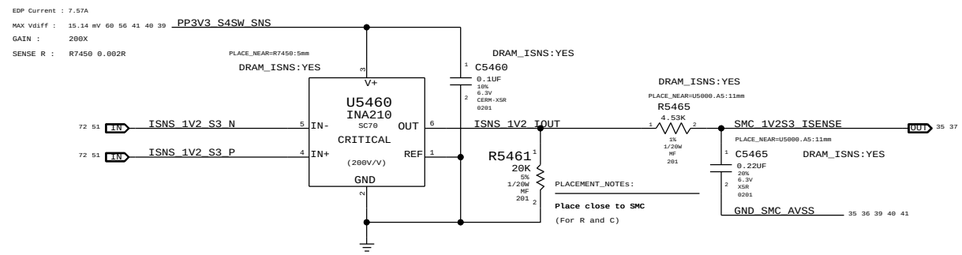


DC-IN (AMON) Current Sense

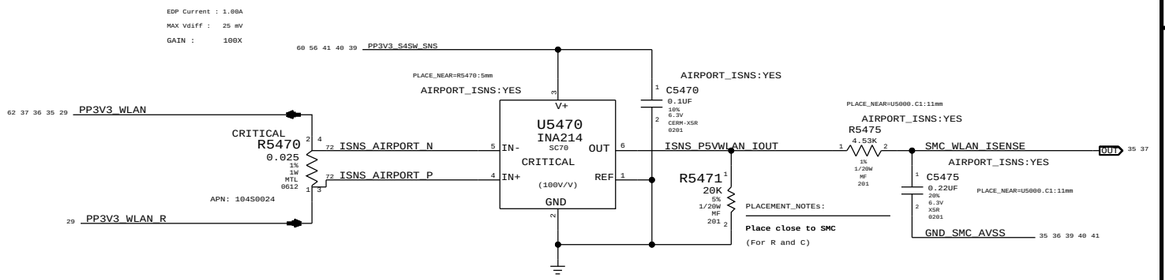


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

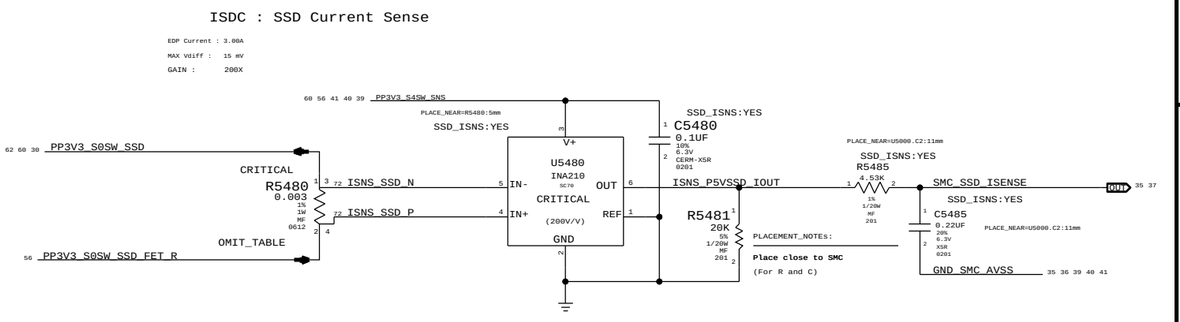
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)



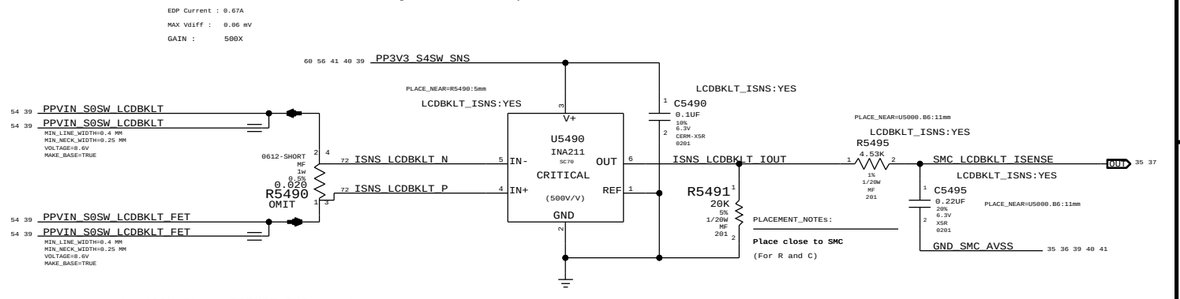
IAPC :AirPort Current Sense



ISDC : SSD Current Sense



IBLC : LCD Backlight Driver Input Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE: High Side Current Sensing

Apple Inc.

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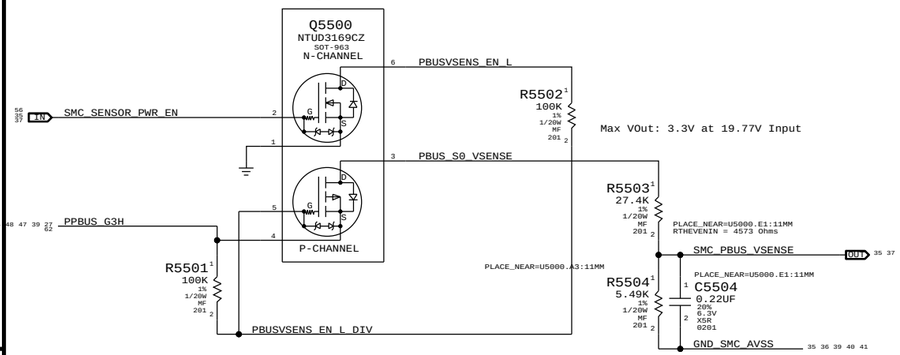
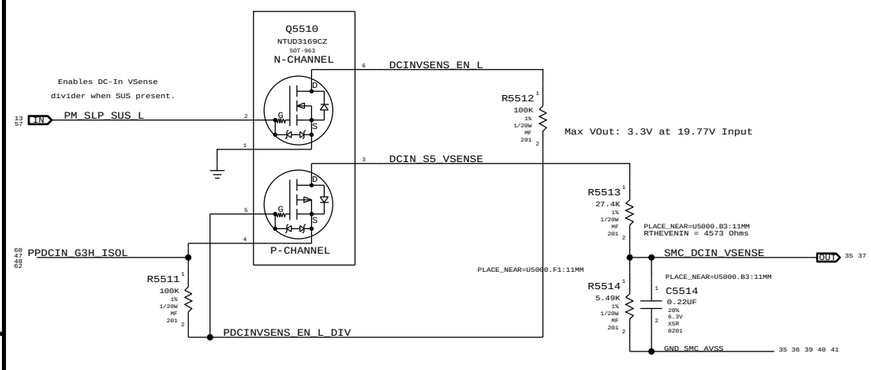
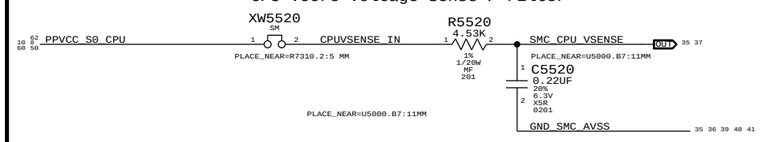
VP0R: PBUS Voltage Sense Enable & Filter



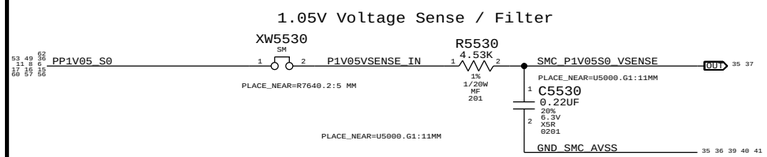
VD0R: DC-In Voltage Sense Enable & Filter



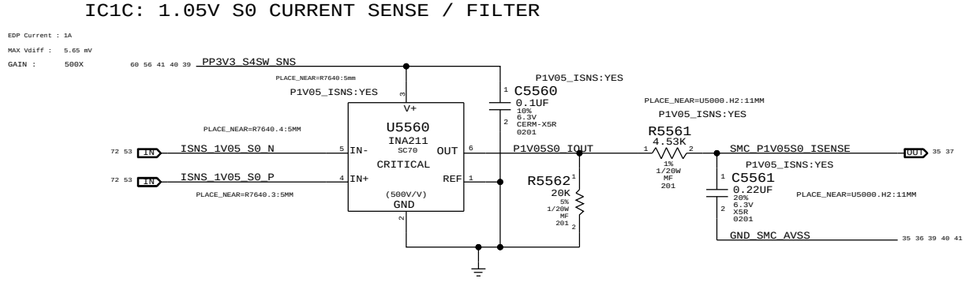
CPU Vcore Voltage Sense / Filter



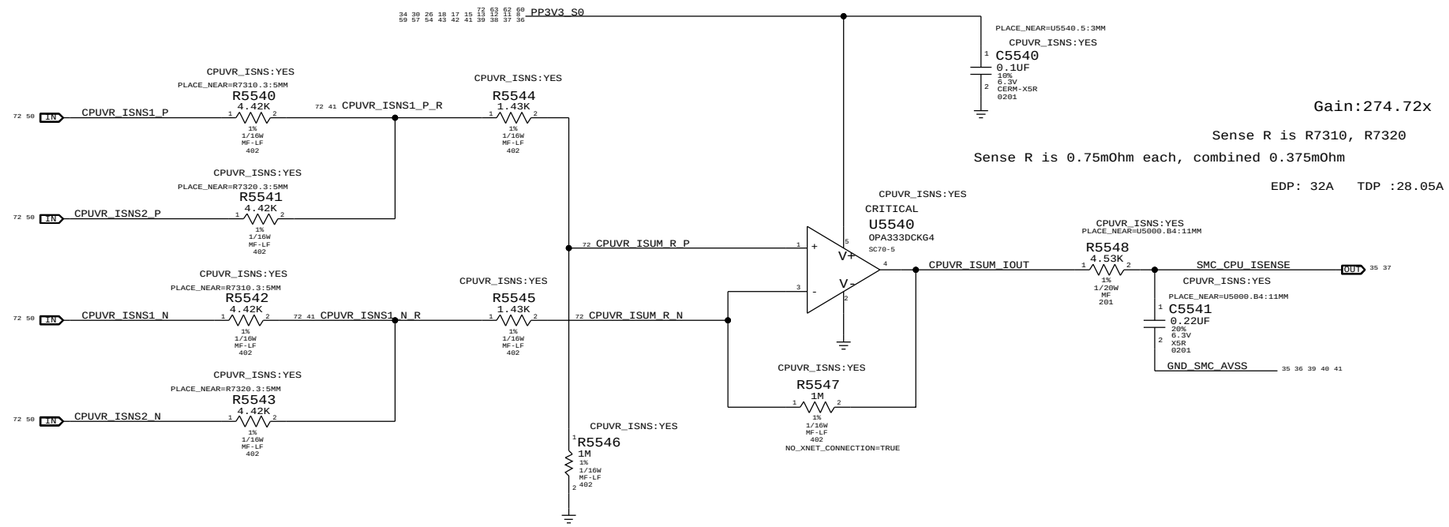
1.05V Voltage Sense / Filter



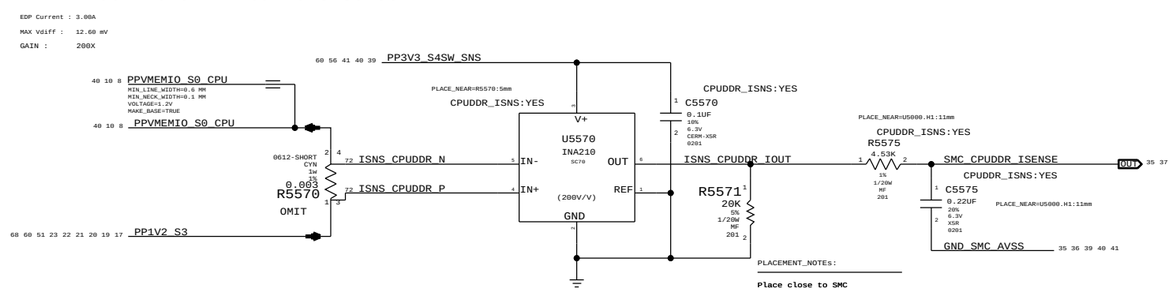
IC1C: 1.05V S0 CURRENT SENSE / FILTER



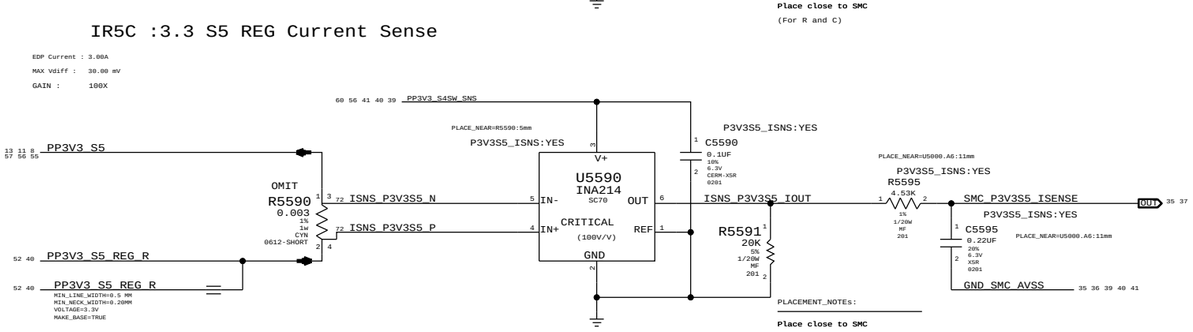
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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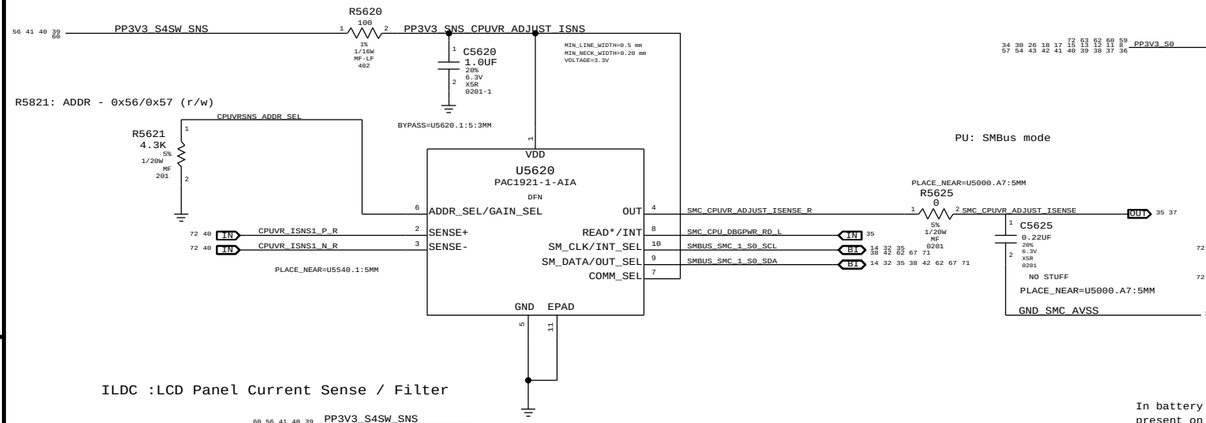
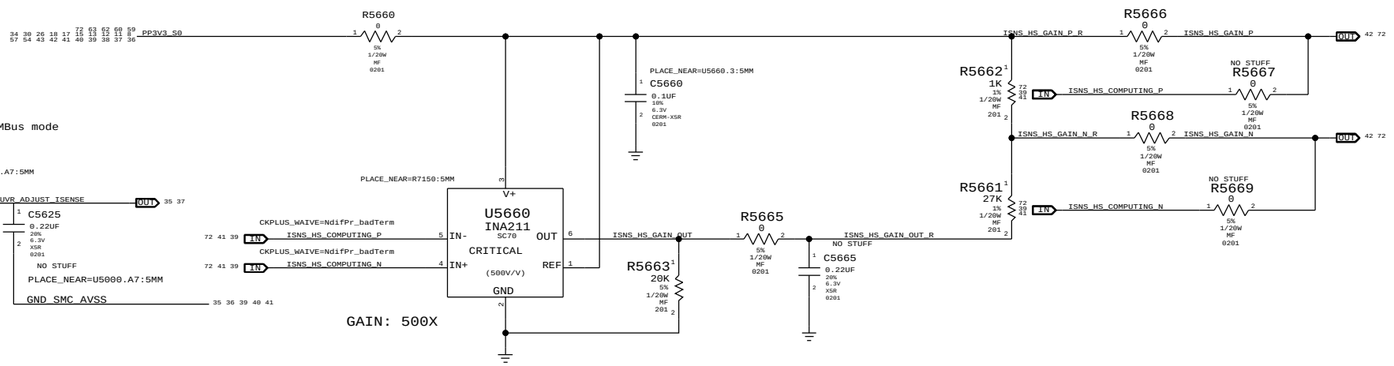
ICS3 : Adjustable Gain CPU VR Current

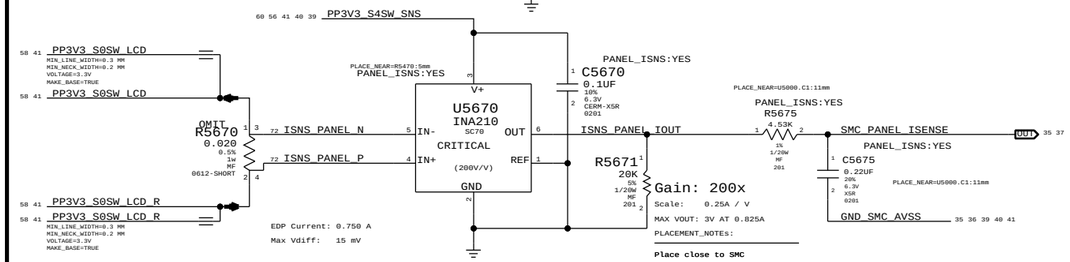


Sense Pins gain stage for U5800 (EMC1704)



GAIN: 500X

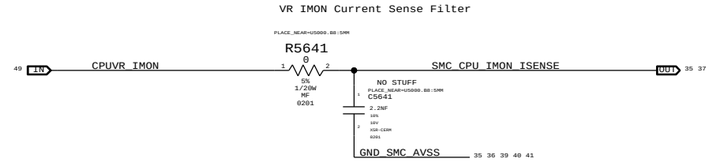
ILDC :LCD Panel Current Sense / Filter



In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

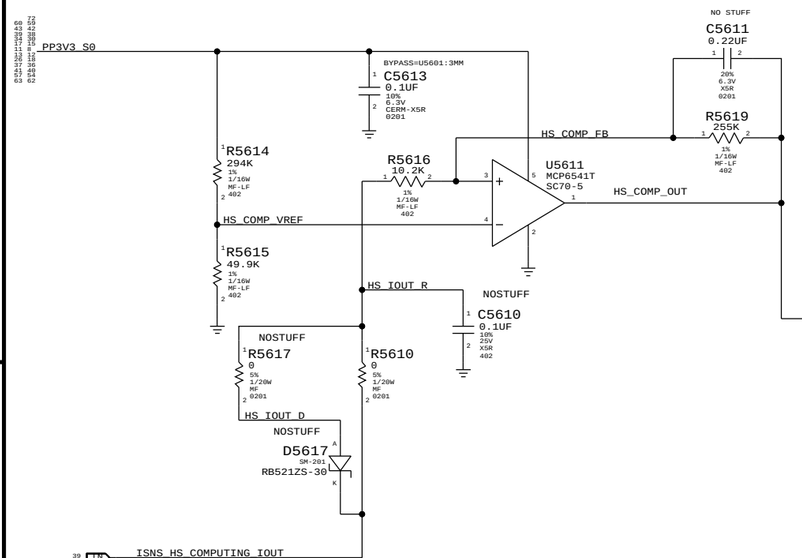
With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

VR IMON Current Sense Filter

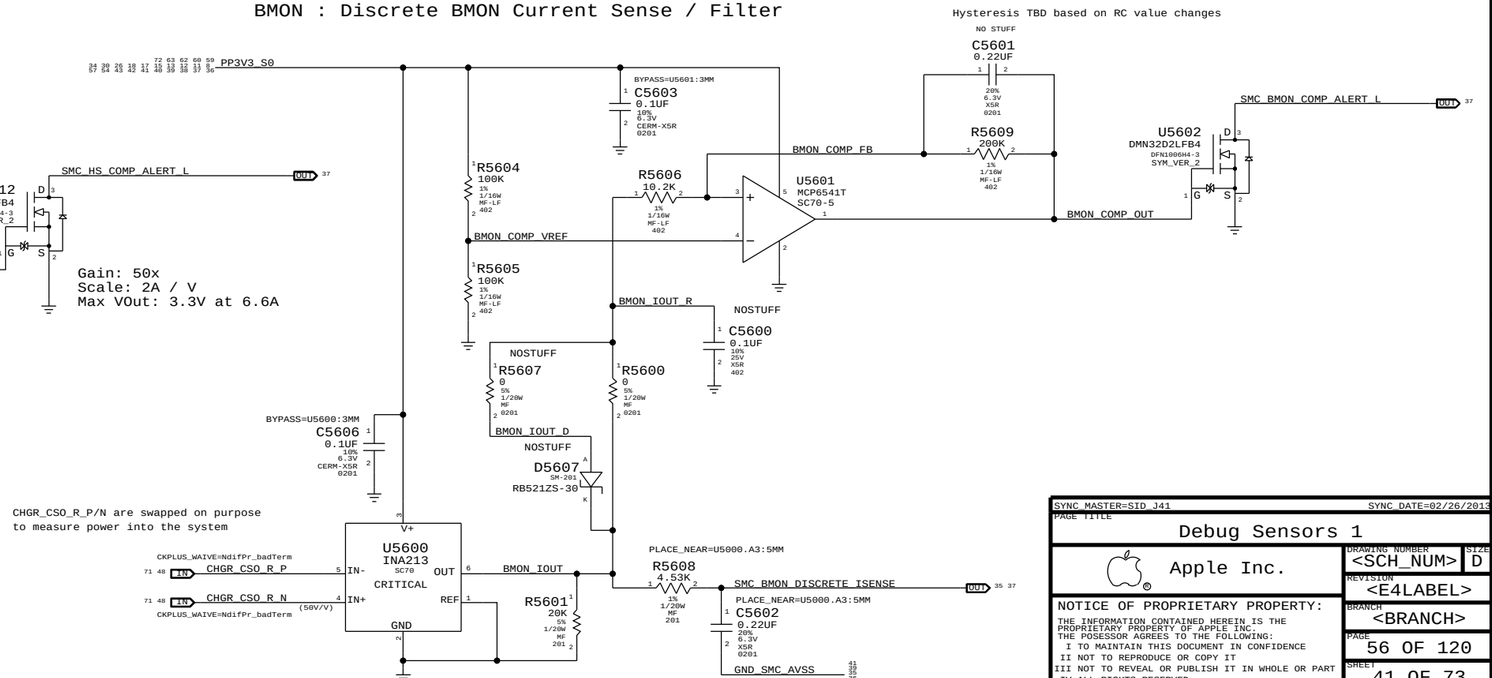


Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Discrete High side Current threshold



BMON : Discrete BMON Current Sense / Filter



Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

CHGR_CSO_R_P/N are swapped on purpose to measure power into the system

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=SID_J41 SYNC_DATE=02/26/2013

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Debug Sensors 1

Apple Inc.

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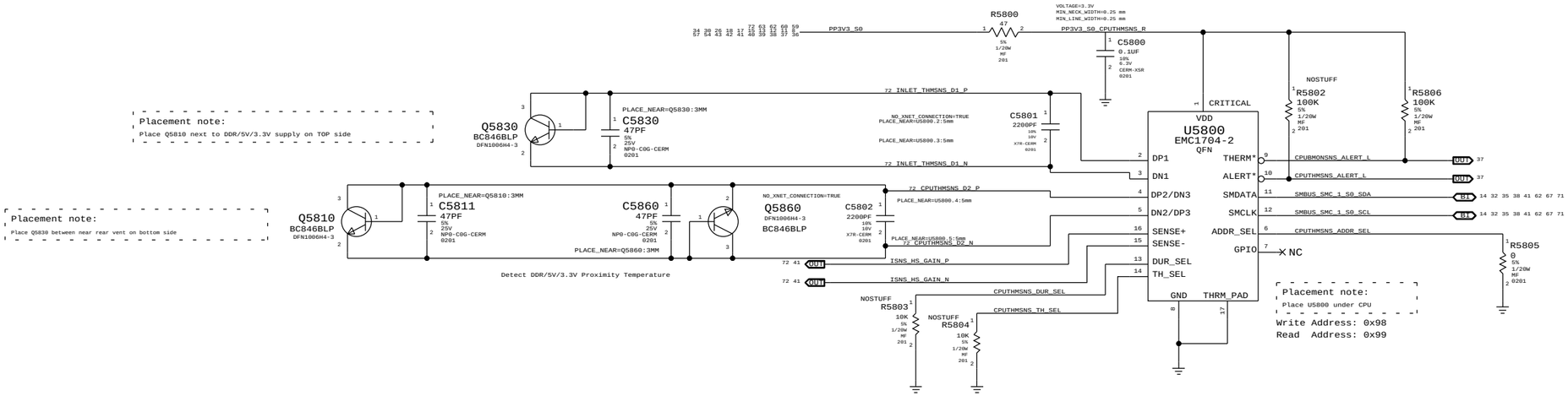
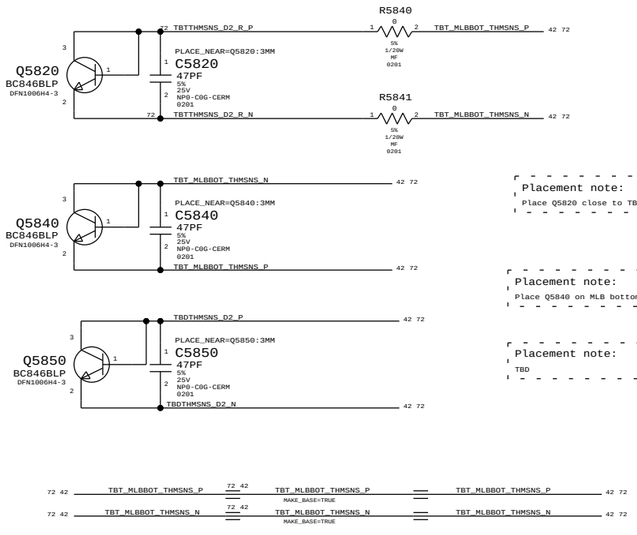
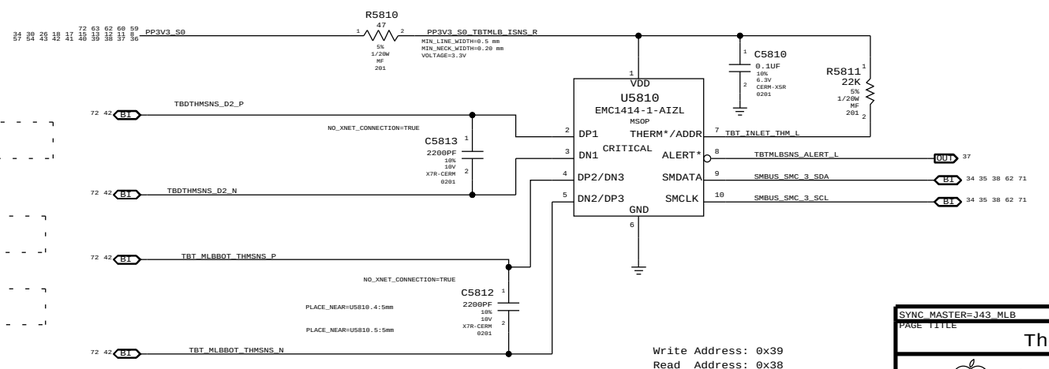
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors



TBT, MLBBOT and TBD Temp Sensor



SYNC_MASTER=J43_MLB	SYNC_DATE=02/20/2013
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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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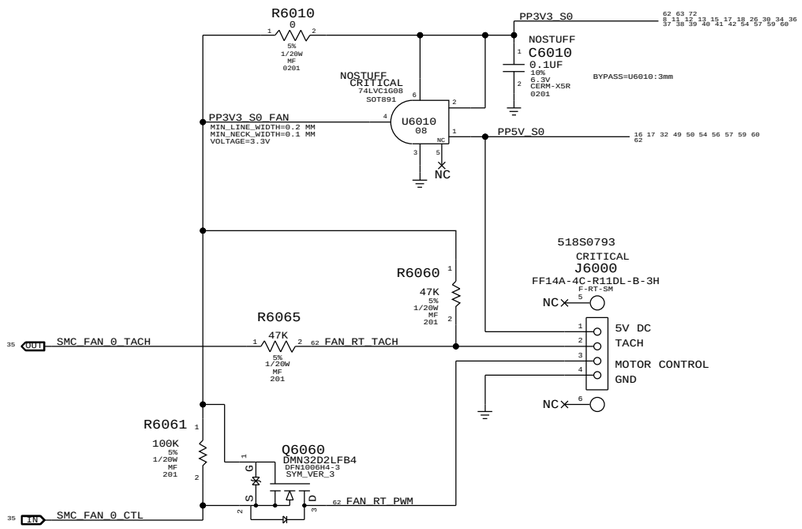
FAN CONNECTOR



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

Fan

Apple Inc.

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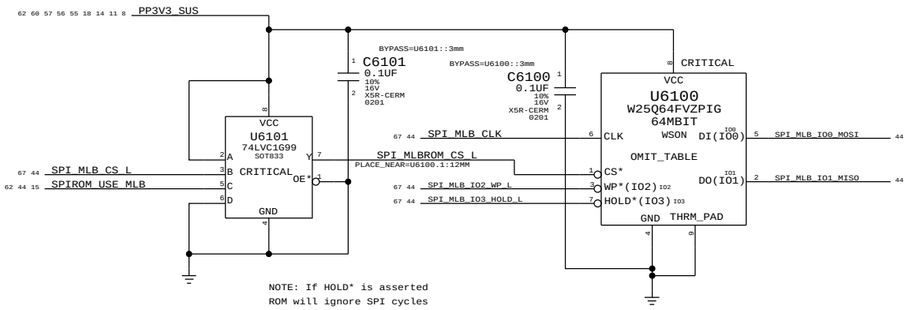
SPI ROM

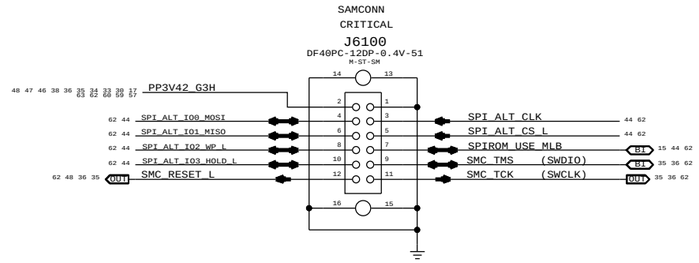
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



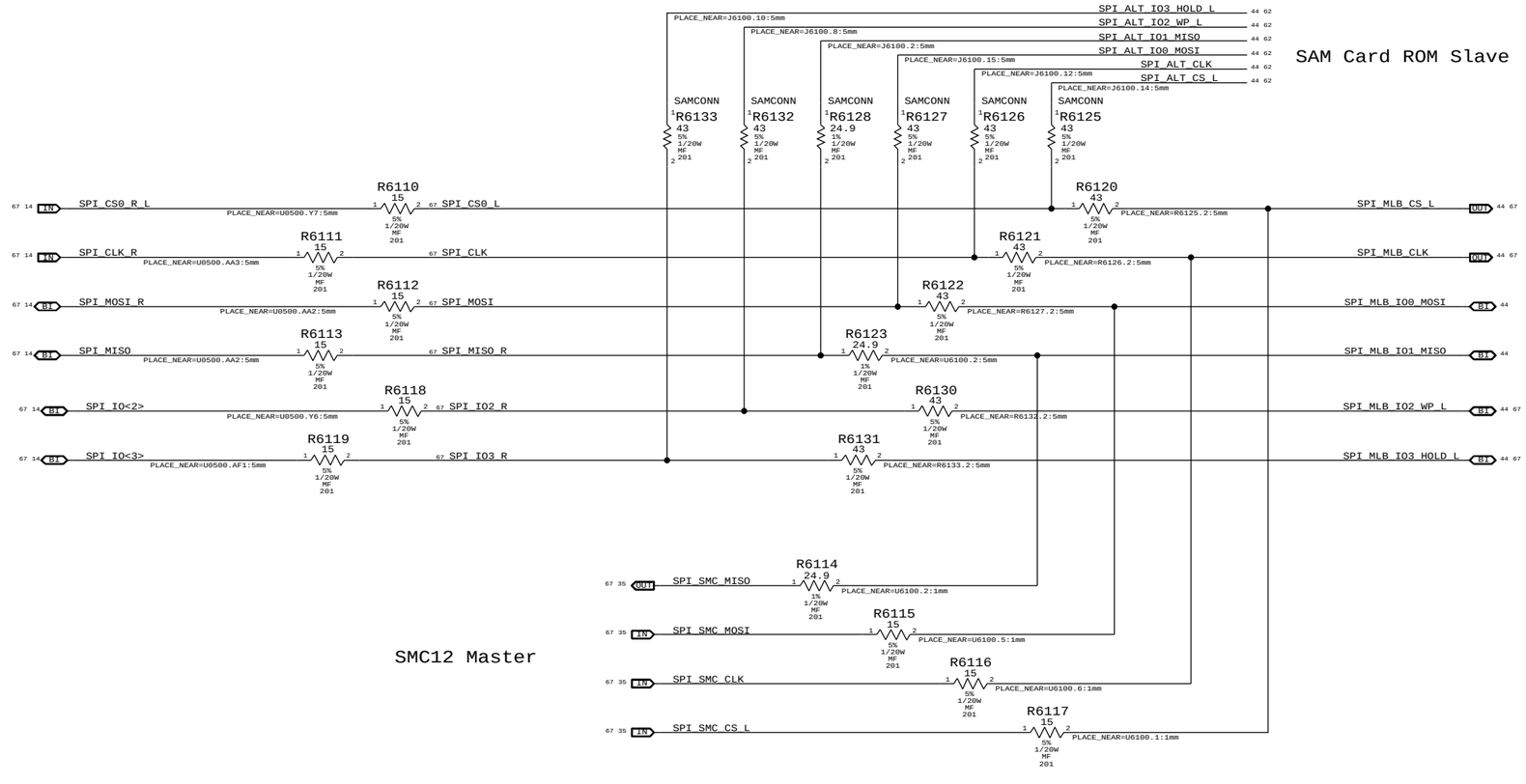
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination



BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE
SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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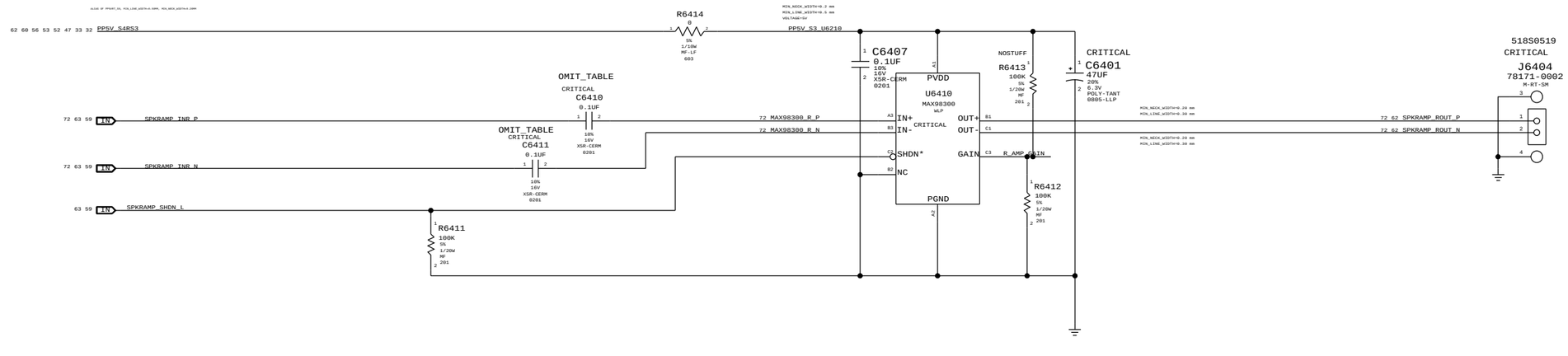
SHEET 44 OF 73

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0460	2	CAP,CER,X5R,0.1UF,10%,16V,0201,MURATA	C6410,C6411	CRITICAL	

SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE: Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

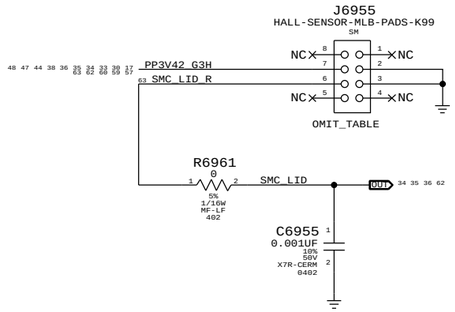
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 64 OF 120

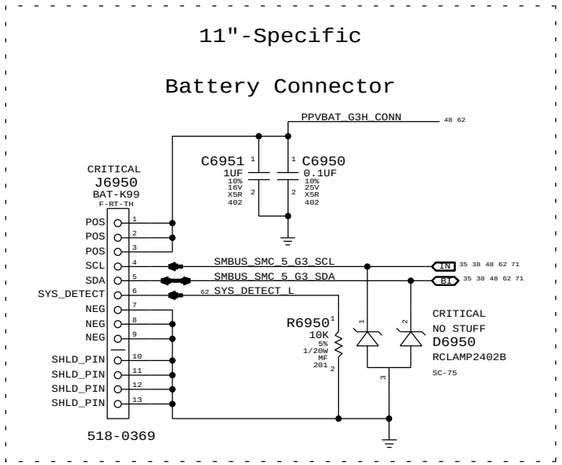
SHEET: 45 OF 73

Hall Effect Sensor



11"-Specific

Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Battery Connector & Hall Effect

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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MLB to LIO Power Cable Connector

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508

62 60 48 PPDCIN_G3H

PP5V_S4RS3
60 62 32 33 45 52 53 56

C7006 0.1UF 10% 16V X5R-CERM 0201

NO STUFF CRITICAL C7007 1UF 10% 35V X5R 603

NO STUFF CRITICAL C7008 1UF 10% 35V X5R 603

NO STUFF C7005 0.1UF 10% 50V X7R 603-1

R7012 68K 1% 1/20W MF 201

Input impedance of 68K meets sparkitecture requirements for detection of B121 (16.5V)

CRITICAL
Q7010
SI5419DU
POWERPAK

R7010 100K 5% 1/20W MF 201

CRITICAL C7012 0.047UF 10% 25V X7R 0402

R7011 10K 1% 1/20W MF 201

DCIN_ISOL_GATE_R

DCIN_ISOL_GATE

62 60 48 40 PPDCIN_G3H_ISOL

CRITICAL
D7012
GDZT2R6.8
GDZ-0201
6.8V Zener

R7006 4.7 5% 1/8W MF-LF 805
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=8.6V

62 60 54 48 40 39 27 PPBUS_G3H

PPBUS_G3H_R

CRITICAL
D7005
BAT30CWFILM
SOT-323

R7005 10 5% 1/8W MF-LF 805
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V

PP18V5_DCIN_ISOL_R

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

CRITICAL C7091 1UF 10% 25V X5R 402

CRITICAL C7090 1UF 10% 25V X5R 402

CRITICAL C7092 5.6UF 20% 25V POLY-TANT CASE-B2-SM

R7080 0 5% 1/20W MF 0201

NO STUFF R7081 49.9K 1% 1/20W MF 201

NO STUFF C7080 1000PF 5% 25V CERM 0402

P3V42G3H_SHDN_L

CRITICAL
U7090
LT3470AED
DFN

VIN BOOST SHDN* SW BIAS NC FB GND THRM PAD

P3V42G3H_BOOST
DIDT=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

C7094 0.22UF 10% 10V CERM 402

CRITICAL L7095 10UH-20%-0.85A-0.46OHM 2520

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

C7095 22PF 5% 50V NP0-C0G-CERM 0201

P3V42G3H_FB
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

<Ra> R7095 348K 1% 1/20W MF 201

<Rb> R7096 200K 1% 1/20W MF 201

CRITICAL C7099 10UF 20% 10V X5R-CERM 0402-1

CRITICAL C7098 10UF 20% 10V X5R-CERM 0402-1

PP3V42_G3H 17 39 33 34 35 36 38 44 46 46 57 58 60 62 63

Vout = 3.425V
300mA Max Output
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE
DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Reverse-Current Protection

Need to stuff R7192 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!

Inrush Limiter

FROM ADAPTER

62 60 47 _PPDCIN_G3H

R7185 470K 1/20W MF 201

C7185 0.1UF 10% 25V X5R 402

CRITICAL Q7180 IRF9395TRPBF DIRECTFET-MC

CHGR_AGATE_DIV

R7186 332K 1% 1/20W MF 201

PPDCIN_G3H_INRUSH

R7180 100K 5% 1/20W MF 201

C7184 4.7UF 10% 25V X5R-CERM 0603

CHGR_SGATE_DIV

R7181 62K 5% 1/20W MF 201

62 60 47 49 _PPDCIN_G3H_ISOL

CRITICAL D7105 BAT30CWFILM SOT-323

PP5V5_DCIN:NO

R7105 20 5% 1/10W MF-LF 603

48 PPCHGR_DCIN_D_R

(CHGR_DCIN)

(CHGR_AGATE)

(CHGR_SGATE)

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 13.55V

30mA max load

PP5V1_CHGR_VDD

R7101 4.7 5% 1/10W MF-LF 402

48 PP5V1_CHGR_VDDP

C7101 1UF 10% 10V X5R 402

47 46 44 38 36 35 34 33 30 17 63 62 60 59 57 PP3V42_G3H

R7110 130K 1% 1/20W MF 201

NO STUFF R7102 100K 5% 1/20W MF 201

R7100 0 5% 1/20W MF 0201

62 44 36 35 1.8V SMC_RESET_L

CHGR_RST_L

46 38 29 71 62 1.8V SMBUS_SMC_5_G3_SCL

46 38 29 71 62 3.3V SMBUS_SMC_5_G3_SDA

57 1.8V CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

71 CHGR_CSO_P

71 CHGR_CSO_N

CRITICAL U7100 ISL6259 TQFN

VDD	19	
VDDP	20	
VHST	12	
SMB_RST_N	13	CHGR_RST_L
SCL	11	SMBUS_SMC_5_G3_SCL
SDA	10	SMBUS_SMC_5_G3_SDA
VFRQ	4	CHGR_VFRQ
CELL	6	CHGR_CELL
ACIN	3	CHGR_ACIN
ICOMP	5	CHGR_ICOMP
VCOMP	7	CHGR_VCOMP
VNEG	8	CHGR_VNEG
CSOP	18	CHGR_CSO_P
CSON	17	CHGR_CSO_N
THRM_PAD (AGND)	29	
PGND (PGND)	22	
DCIN	2	CHGR_DCIN
SGATE	26	CHGR_SGATE
AGATE	1	CHGR_AGATE
CSIP	28	71 CHGR_CSI_P
CSIN	27	71 CHGR_CSI_N
BOOT	25	CHGR_BOOT
UGATE	24	CHGR_UGATE
PHASE	23	CHGR_PHASE
LGATE	21	CHGR_LGATE
BGATE	16	CHGR_BGATE
20V/V AMON	9	CHGR_AMON OUT 39
36V/V BMON	15	CHGR_BMON OUT 39
ACOK	14	SMC_BC_ACOK OUT 35 36 59 63

R7113 100 5% 1/20W MF 201

R7115 255K 1% 1/20W MF 201

R7111 46.4K 1% 1/20W MF 201

CHGR_VCOMP_R

C7115 470PF 10% 16V X5R-X7R-CERM 0201

R7142 1K 5% 1/20W MF 201

CHGR_ICOMP_R

R7116 10K 1% 1/20W MF 201

CHGR_VNEG_R

C7116 470PF 10% 16V X5R-X7R-CERM 0201

C7150 0.47UF 10% 10V X5R 0402

C7102 1UF 10% 10V X5R 402

XW7100 SM PLACE_NEAR=U7100.22:1mm

(GND)

C7142 0.1UF 10% 6.3V CERM-X5R 0201

C7111 0.01UF 10% 10V X5R-CERM 0201

C7100 1UF 10% 10V X5R 402-1

C7105 0.22UF 10% 50V X5R-CERM 0603-1

C7126 1000PF 10% 16V X7R-CERM 0201

GND_CHGR_AGND

R7120 0.020 0.5% 1W MF-LF 0612

71 CHGR_CSI_R_P

71 CHGR_CSI_R_N

R7121 10 5% 1/20W MF 201

R7122 10 5% 1/20W MF 201

C7120 0.047UF 10% 16V X7R-CERM 0402

C7122 0.1UF 10% 25V X5R 402

C7121 0.1UF 10% 25V X5R 402

PPDCIN_G3H_CHGR

C7125 0.22UF 10% 10V CERM 402

CRITICAL Q7130 NTMFD4902NF DFN

Max Current = 8A

f = 400 kHz

CRITICAL L7130 4.7UH-17A PIMC104T4R7MN-SM

SWITCH_NODE=TRUE

CRITICAL C7130 33UF-0.060OHM 20% 25V POLY-TANT CASE-D3L

CRITICAL C7131 33UF-0.060OHM 20% 25V POLY-TANT CASE-D3L

C7135 1UF 10% 25V X5R 603-1

C7136 1UF 10% 25V X5R 603-1

BYPASS=Q7130:1.5mm C7137 0.001UF 10% 50V X7R-CERM 0402

TO SYSTEM

CRITICAL F7140 8AMP-24V 1206

PPBUS_G3H 27 39 40 47 54 60 62

PPVBAT_G3H_CHGR_REG

C7140 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S

C7141 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S

C7143 62UF-0.023OHM 20% 11V TANT-POLY CASE-B2S

BYPASS=L7130:Q7130:1.5mm C7145 1000PF 10% 16V X7R-CERM 0201

CRITICAL Q7155 SI7137DP SO-8

TO/FROM BATTERY

PPVBAT_G3H_CONN 46 62

R7150 0.01 1% 1W MF 2512-4

PPVBAT_G3H_CHGR_R

R7151 2.2 5% 1/20W MF 201 71 41 CHGR_CSO_R_P

R7152 0 5% 1/20W MF 0201 71 41 CHGR_CSO_R_N

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

* R7151 HAS 2.20HM TO COMPENSATE UNBALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

C7117 10UF 10% 25V X5R 805

C7114 1UF 10% 25V X5R 603-1

C7113 0.1UF 10% 25V X5R 402

C7112 0.01UF 10% 25V X7R 402

5.5v "G3Hot" Supply

For Erp Lot6 spec

NO STUFF R7192 0

NO STUFF C7190 4.7UF 10% 25V X5R-CERM 0603

CRITICAL U7190 LT3470A DFN

VIN BOOST SHDN* SW BIAS NC FB THRM GND PAD

PP5V1_BOOST

SWITCH_NODE=TRUE

PP5V1_SW

NO STUFF C7194 0.22UF 10% 16V CERM 402

CRITICAL NO STUFF L7195 10UH-20%-0.85A-0.46OHM 2520

NO STUFF C7195 22PF 5% 50V NP0-C0G-CERM 0201

PP5V1_FB

NO STUFF <Ra> R7195 681K 1% 1/10W MF 603

NO STUFF <Rb> R7196 200K 1% 1/10W MF 603

Vout = 1.25V * (1 + Ra / Rb)

NO STUFF CRITICAL C7198 10UF 20% 10V X5R 603

CRITICAL C7199 10UF 20% 10V X5R 603

PP5V5_DCIN:YES

R7190 0 5% 1/10W MF-LF 402 CHGR_DCIN 48

PP5V5_VDDP

R7191 0 5% 1/10W MF-LF 402 PP5V1_CHGR_VDDP 48

PP5V5_CHGR_VDDP

Vout = 5.50V
200MA MAX OUTPUT
(Switcher limit)

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

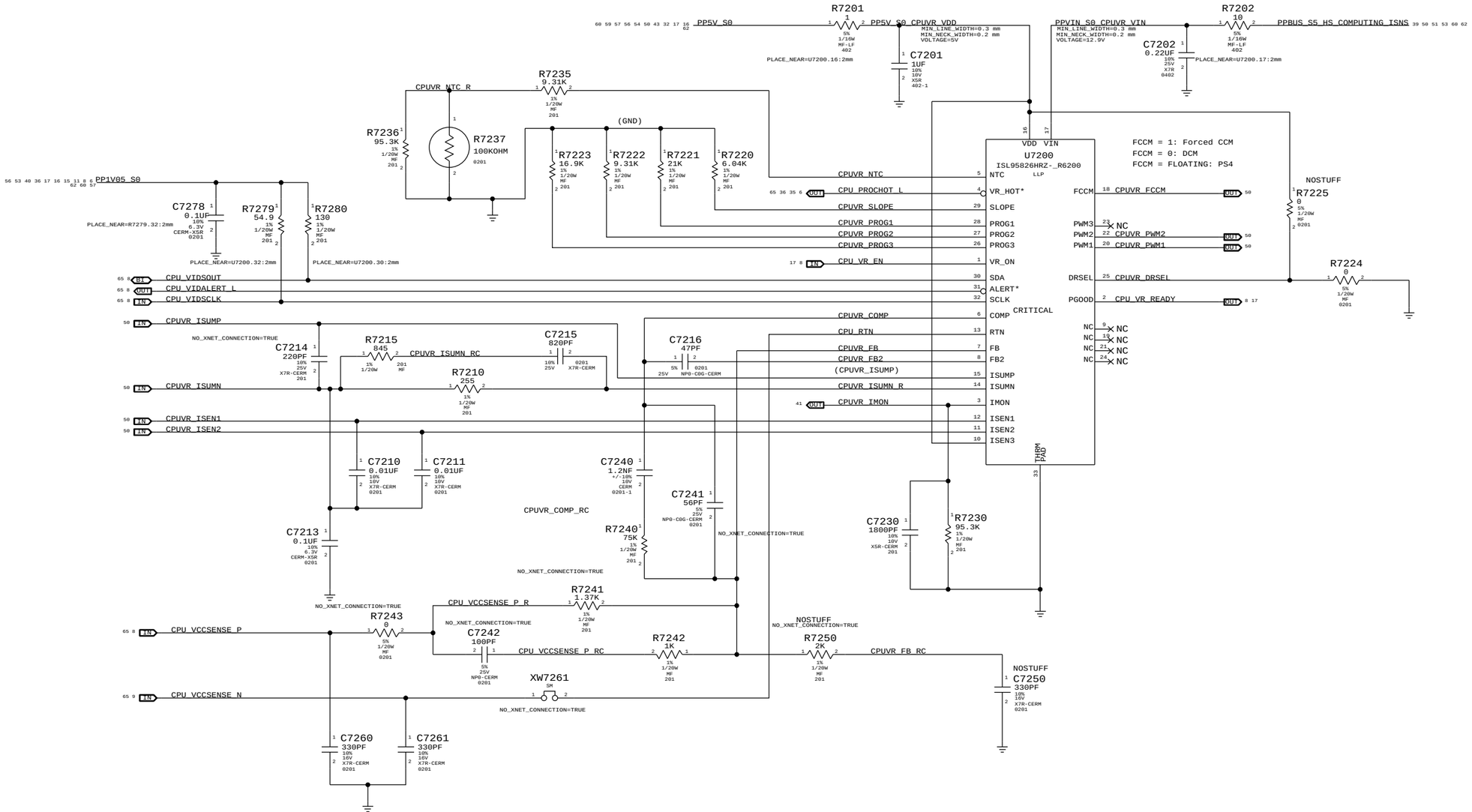
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

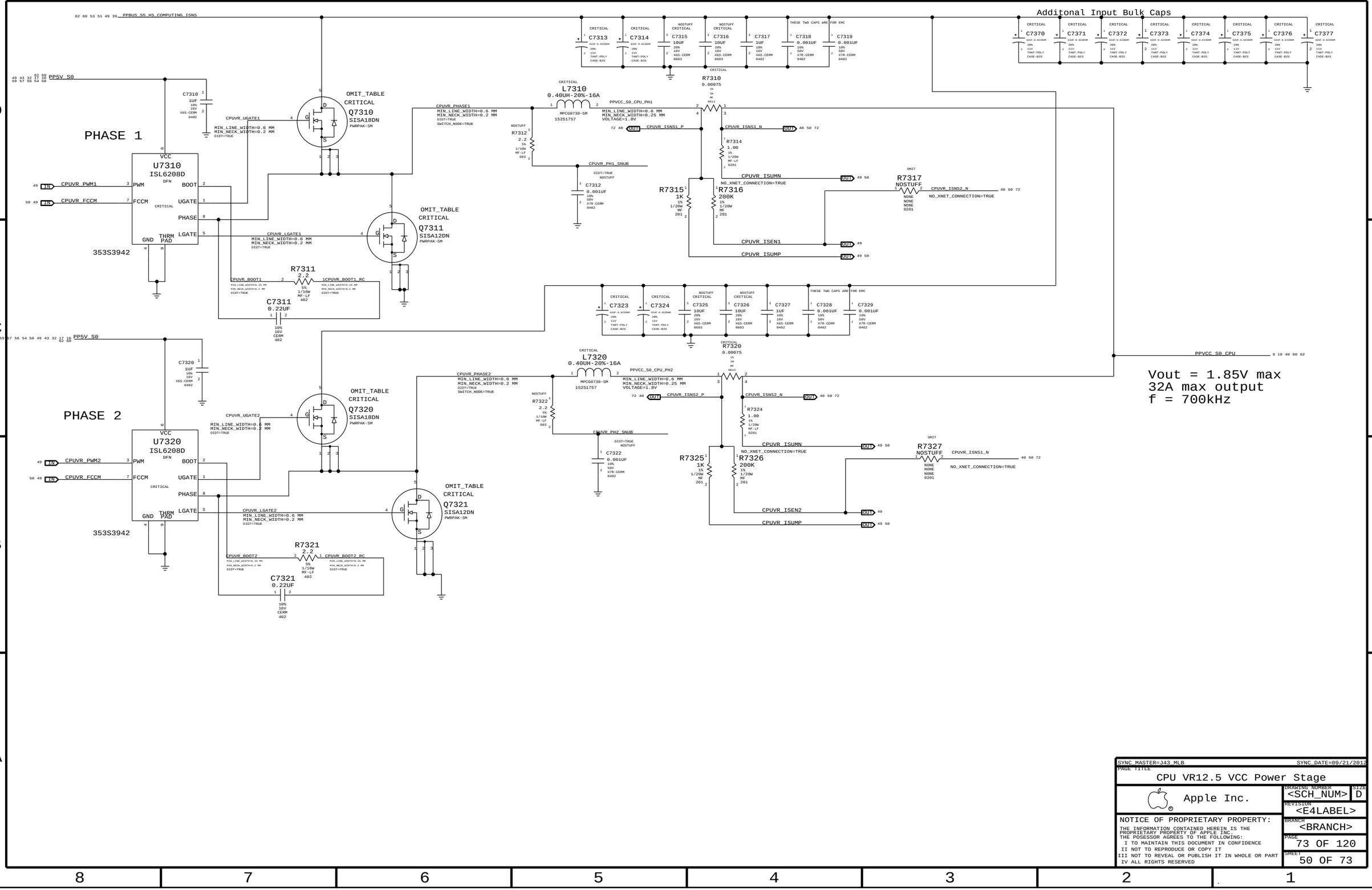
BRANCH: <BRANCH>

PAGE: 71 OF 120

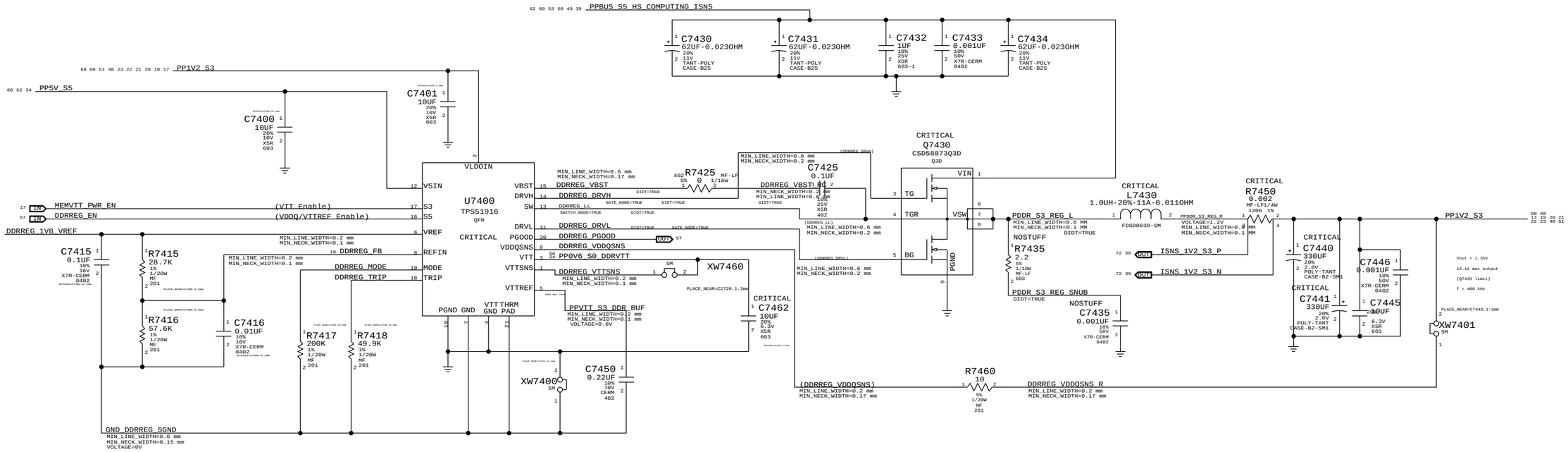
SHEET: 48 OF 73



SYNC_MASTER=J43_MLB	SYNC_DATE=10/09/2012
PAGE TITLE	CPU VR12.6 VCC Regulator IC
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 72 OF 120
	SHEET: 49 OF 73



SYNC_MASTER=J43_MLB	SYNC_DATE=09/21/2012
PAGE TITLE: CPU VR12.5 VCC Power Stage	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 73 OF 120
	SHEET: 50 OF 73



SYNC_MASTER=J43_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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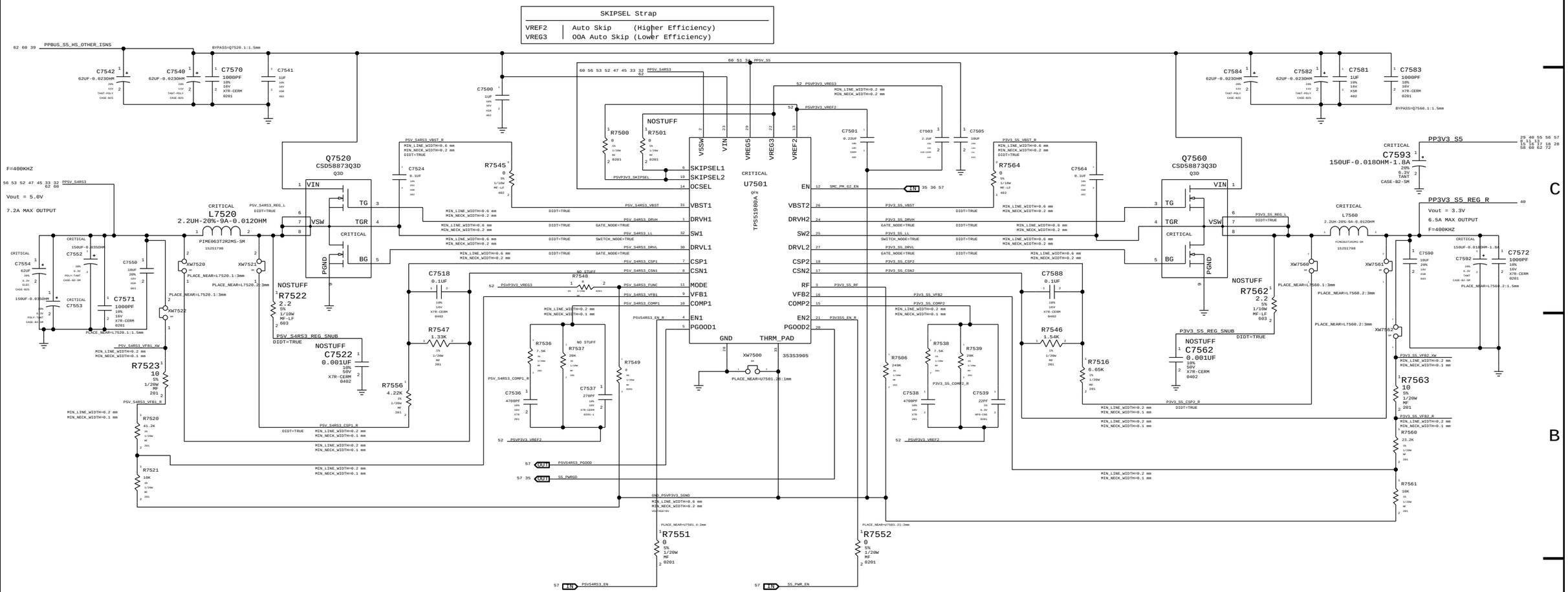
SKIPSEL Strap	
VREF2	Auto Skip (Higher Efficiency)
VREG3	OOA Auto Skip (Lower Efficiency)



SYNC_MASTER=J43_MLB	SYNC_DATE=10/02/2012
PAGE TITLE	5V S4RS3 / 3.3V S5 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 75 OF 120
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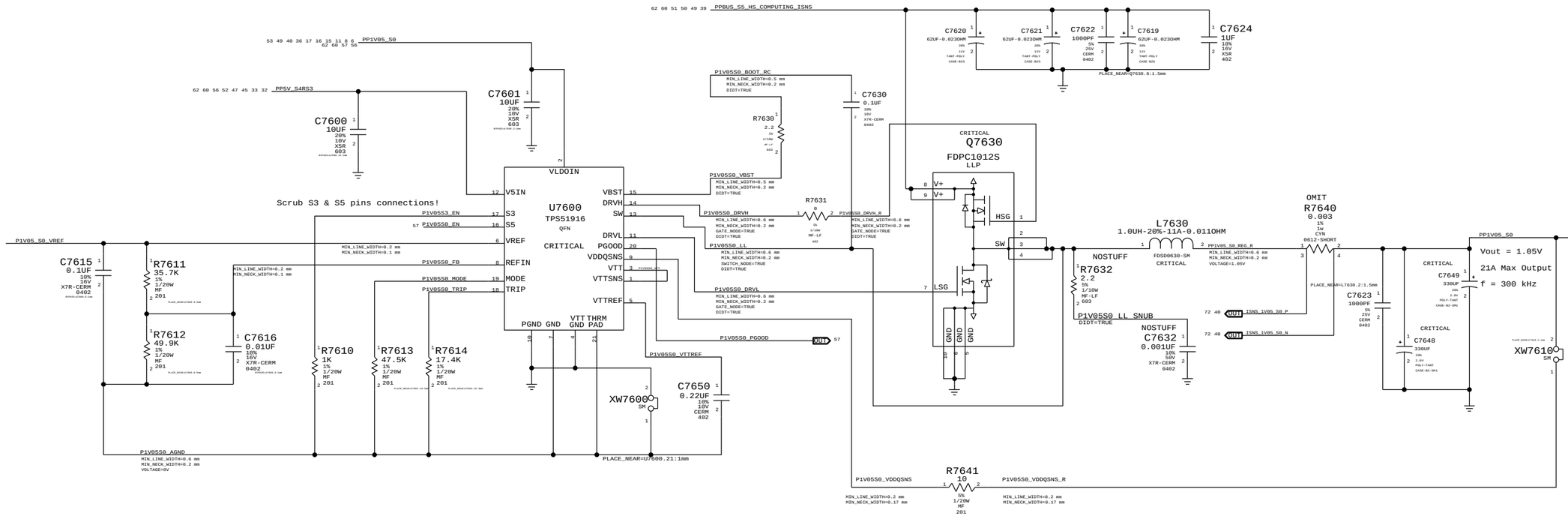
1.05V S0 Regulator



SYNC_MASTER=J43_MLB	SYNC_DATE=09/10/2012
PAGE TITLE	1.05V S0 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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PPBUS S0 LCDBklt FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

F7700 3AMP-32V-467 603-HF PLACE_SIDE=BOTTOM
PPBUS_G3H
PPVIN_S0SW_LCDBKLTFET
R7788 301K 1% 1/20W MF 201
C7782 0.1UF 10% 16V X7R-CERM 0402
LCDBKLT_EN_DIV_L
R7789 147K 1% 1/20W MF 201
LCDBKLT_EN_L
Q7706 FDC638APZ_SBMS001 SSOT6-HF
PPVIN_S0SW_LCDBKLT_FET
PPVIN_S0SW_LCDBKLT
CRITICAL L7701 15UH-2.8A PIMB053T-SM
CRITICAL C7712 10UF 10% 25V X5R 805
CRITICAL C7713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L7701.1:3mm
LCDBKLT_BOOST
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.150 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE
PLACE_NEAR=L7701.2:3mm
CRITICAL D7701 SOD-123 RB160M-60G
PPHV_S0SW_LCDBKLT
C7796 220PF 10% 50V X7R-CERM 0402
CRITICAL C7797 10UF 10% 50V X5R 1210-1
CRITICAL C7799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=U7701.A5:3mm
PLACE_NEAR=D7701.2:5mm
PLACE_NEAR=D7701.2:3mm
XW7720 SM
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
MIN_LINE_WIDTH=0.1 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=C7797.1:5mm

Q7707 DMN5L06VK-7 SOT563 VER 3
EDP_BKLT_EN
LCDBKLT_DISABLE
Q7707 DMN5L06VK-7 SOT563 VER 3
BKLT_PLT_RST_L

PP5V_S0
C7710 1UF 10% 25V X5R 603-1
BYPASS=U7701.D1:5mm
C7714 0.01UF 10% 10V X5R-CERM 0201
BYPASS=U7701.D1:3mm
PP3V3_S0
C7711 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U7701.C4:4mm
(GND_BKL_SGND)

U7701 25-BUMP-MICRO LP8550
VDDIO VLDO VIN
VSYNC FILTER ISET FSET SCLK SDA PWM EN FAULT
SW_0 SW_1 FB
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
BKL_ISEN1 BKL_ISEN2 BKL_ISEN3 BKL_ISEN4 BKL_ISEN5 BKL_ISEN6
GND_S GND_L GND_SW GND_SW

R7741 10K 5% 1/20W MF 201
R7753 0 5% 1/20W MF 0201
SMBUS_PCH_CLK
R7757 0 5% 1/20W MF 0201
SMBUS_PCH_DATA
Addr: 0x58(Wr)/0x59(Rd)
R7731 200K 1% 1/20W MF 201
R7715 100K 1% 1/20W MF 201
PPVIN_S0SW_LCDBKLT
R7704 33 5% 1/20W MF 201
EDP_BKLT_PWM
C7704 33PF 5% 25V NPO-C0G 0201
TP7701 TP-P6 PLACE_SIDE=BOTTOM
I_LED=17.1mA
Fpwm=9.62kHz
see spec for others
R7755 10K 5% 1/20W MF 201
R7714 21.5K 1% 1/20W MF 201
R7716 90.9K 1% 1/20W MF 201
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)
GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
CRITICAL XW7710 SM

10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R771B,R7719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

R7717 0 5% 1/16W MF-LF 402 LED_RETURN_1 OUT
R7718 0 5% 1/16W MF-LF 402 LED_RETURN_2 OUT
R7719 0 5% 1/16W MF-LF 402 LED_RETURN_3 OUT
R7720 0 5% 1/16W MF-LF 402 LED_RETURN_4 OUT
R7721 0 5% 1/16W MF-LF 402 LED_RETURN_5 OUT
R7722 0 5% 1/16W MF-LF 402 LED_RETURN_6 OUT
BKLT:PROD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
MIN_NECK_WIDTH=0.20 mm
PLACE_NEAR=U7701.E5:10mm
PLACE_NEAR=U7701.D5:10mm
PLACE_NEAR=U7701.C5:10mm
PLACE_NEAR=U7701.E3:10mm
PLACE_NEAR=U7701.E2:10mm
PLACE_NEAR=U7701.E1:10mm

PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

Keyboard Backlight Driver & Detection

PP5V_S0
BYPASS=U7750.1:2:2 MM
CRITICAL L7750 10UH-0.58A-0.35OHM 1098AS-SM
KBDLED_SW
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.225 MM
SWITCH_NODE=TRUE
DIDT=TRUE
C7750 1UF 10% 10V X5R 402-1
U7750 SPN0350076 MLF
VIN
SMC_SYS_KBDLED
EN SW FB OUT NC GND THRM PAD
CRITICAL
KBDLED_FB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=40V
KBDLED_ANODE
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=40V
R7700 4.7 5% 1/16W MF-LF 402
C7755 0.22UF 10% 50V X5R-CERM 0603-1
C7756 0.22UF 10% 50V X5R-CERM 0603-1

Keyboard Backlight Connector

CRITICAL J7715 FF14A-4C-R11DL-B-3H F-RT-SM
NC NC
518S0793

SYNC_MASTER=J43_MLB	SYNC_DATE=09/13/2012
PAGE TITLE	LCD/KBD Backlight Driver
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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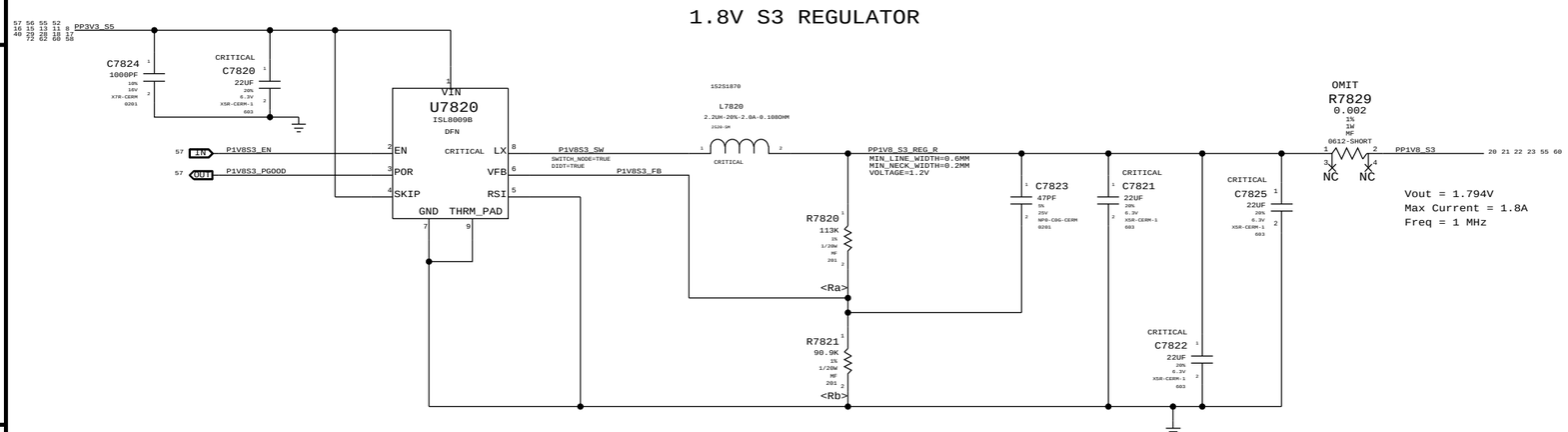
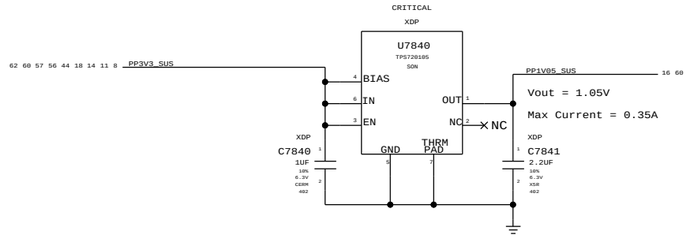
1.8V S3 REGULATOR

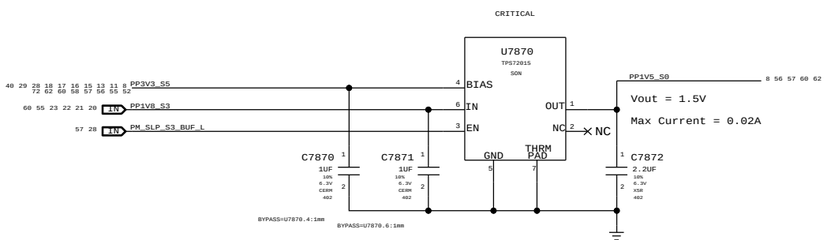


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE

Misc Power Supplies

Apple Inc.

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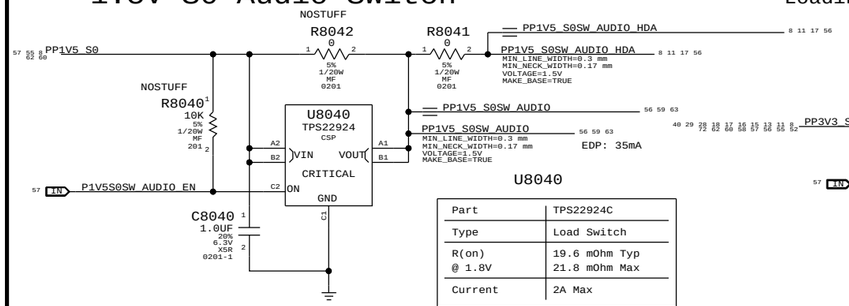
1.5V S0 Audio Switch

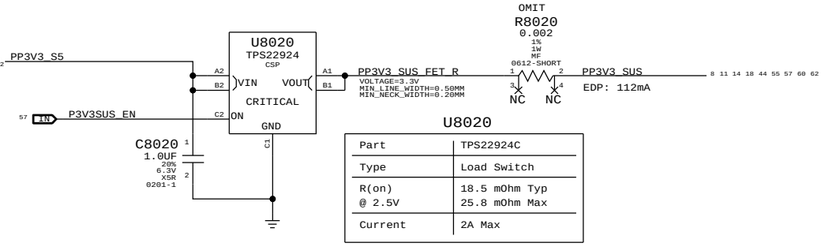
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

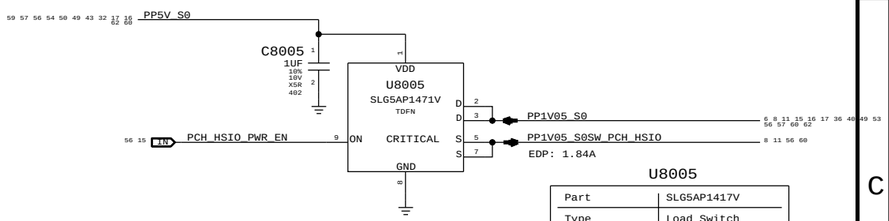
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.05V PCH HSIO Switch

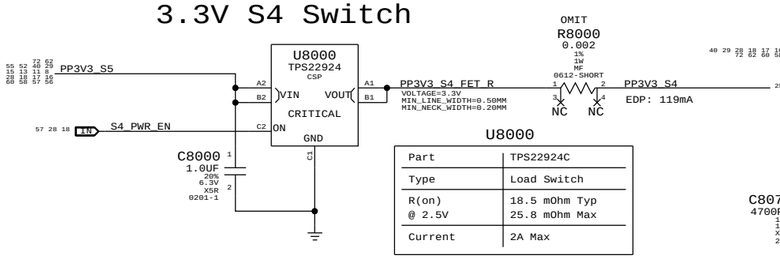


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

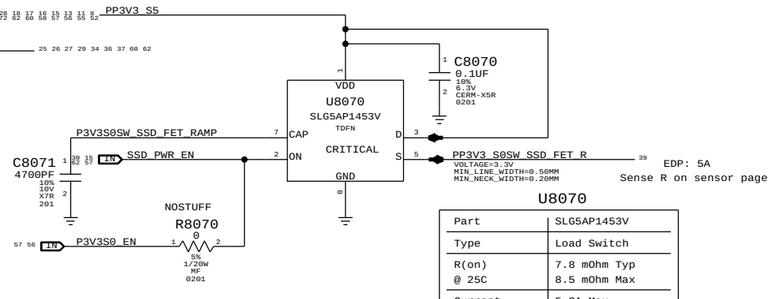
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

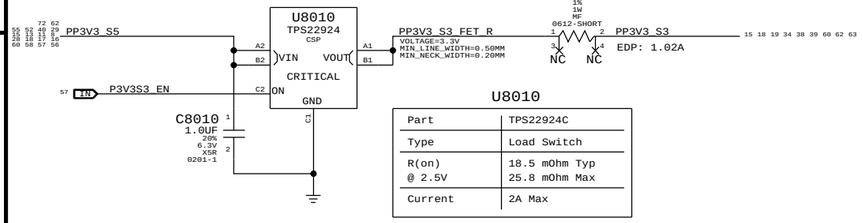
3.3V SSD Switch



U8070

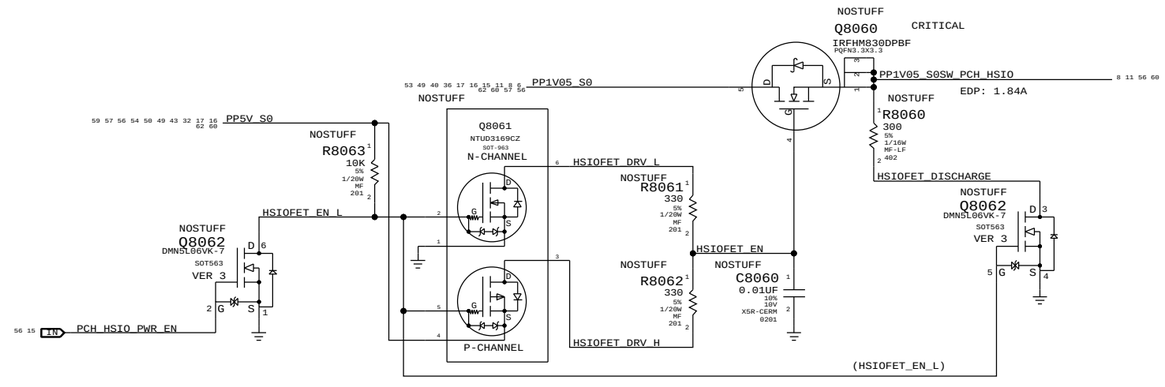
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

3.3V S3 Switch

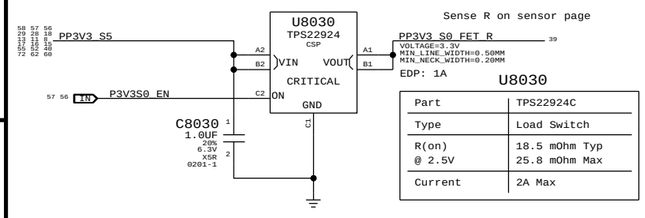


U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max



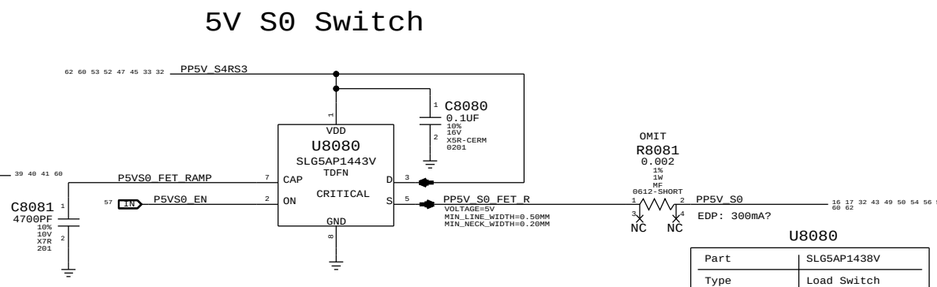
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

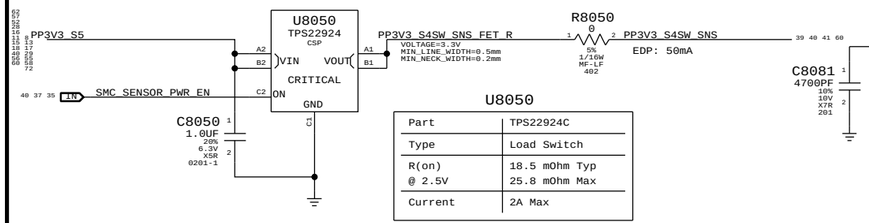
5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

3.3V Sensor Switch



U8050

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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S5 Enables

SMC_PM_G2_EN (OUT) → R8140 100 5% 1/20W MF 201 → S5_PWR_EN (MAKE_BASE=TRUE) → S5_PWR_EN (OUT)
SMC_PM_G2_EN (IN)
NOSTUFF C8142 0.47UF 10% 6.3V CERM-X5R 402
PLACE_NEAR=U7501.21:7mm

S5 Power Good

PP3V42_G3H
PLACE_NEAR=U7501.20:7mm
R8141 100K 5% 1/20W MF 201
S5_PWRGD-->SMC
SMC-->PM_DSW_PWRGD
S5_PWRGD → S5_PWRGD (MAKE_BASE=TRUE) (OUT)

SSD Enable

SSD_PWR_EN (IN) → SSD_PWR_EN (MAKE_BASE=TRUE) (OUT)

Standby Enables

PP3V3_S5
NOSTUFF C8170 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U8170.6:2.3mm
NOSTUFF U8170 74LVC1G32 SOT891
PM_SLP_S5_L (IN)
SMC_S4_WAKESRC_EN (IN)
S4_PWR_EN (MAKE_BASE=TRUE) → S4_PWR_EN (OUT)
R8115 0 5% 1/20W MF 0201

S3 Enables

PM_SLP_S4_L (IN)
R8111 20K 5% 1/20W MF 201
R8116 0 5% 1/20W MF 0201
R8112 0 5% 1/20W MF 0201
C8111 0.1UF 20% 10V CERM 402
NO STUFF C8116 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C8112 0.47UF 10% 6.3V CERM-X5R 402
P3V3S3_EN (MAKE_BASE=TRUE) → P3V3S3_EN (OUT)
P1V8S3_EN (MAKE_BASE=TRUE) → P1V8S3_EN (OUT)
DDRREG_EN (MAKE_BASE=TRUE) → DDRREG_EN (OUT)

USB_PWR:STBY / USB_PWR:S3

USB_PWR:STBY R8114 100 5% 1/20W MF 201
USB_PWR:S3 R8117 100 5% 1/20W MF 201
USB_PWR_EN (MAKE_BASE=TRUE) → USB_PWR_EN (OUT)
NO STUFF C8114 0.47UF 10% 6.3V CERM-X5R 402

USB_PWR:STBY

R8177 0 5% 1/20W MF 0201
S4_PWR_EN (IN)

USB_PWR:S3

R8179 0 5% 1/20W MF 0201
PM_SLP_S4_L (IN)

P5VS4RS3_EN_RC
NO STUFF D8175 SM-201 RB521ZS-30
R8175 0 5% 1/20W MF 0201
NO STUFF R8176 240 5% 1/20W MF 201
P5VS4RS3_EN_D
P5VS4RS3_EN (OUT)
NO STUFF C8175 2.2UF 10% 6.3V X5R 402

5V needs to be held up
so 1.05V can fall after 1.5V

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESMC_EN	PM_SUS_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	1	0	0	0	0
Battery Off (S3monAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (S3mon)	1	0	0	0	0	0	0

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K 1% 1/20W MF 201 → VMON_5V_DIV (5.0V Divider: 1.07V) → R8152 15K 1% 1/20W MF 201
PP3V3_S0 → R8158 15K 1% 1/20W MF 201 → VMON_3V3_DIV (3.3V Divider: 1.07V) → R8159 7.15K 1% 1/20W MF 201
PP1V5_S0 → R8155 1K 5% 1/20W MF 201 → VMON_Q4_BASE
R8153 1K 5% 1/20W MF 201
C8159 1UF 10% 10V X5R 402 (9ms RC delay)
R8154 1K 5% 1/20W MF 201 → VMON_Q3_BASE
R8156 150K 1% 1/20W MF 201 → S0PGD_C
VMON_Q2_BASE
NC
NC
CRITICAL Q8150 ASMCC0179 DFN2015H4-8 376S0854 (Q1 Q2 Q3 Q4)
S0PGD_BJT_GND_R
R8157 100 5% 1/20W MF 201
ALL_SYS_PWRGD

Vbe 0.7V max @ 2mA
Vce(sat) 0.1V max @ 1mA
Q1 Vth 0.7~1V @Id 250uA

1.5V Codec Enable

PLACE_NEAR=U8040.2:C7mm
AUD_PWR_EN (IN) → R8145 100K 5% 1/20W MF 201 → P1V5S0SW_AUDIO_EN (OUT)
D8146 SM-201 RB521ZS-30 (P1V5CODEC_EN_D)
R8146 1K 5% 1/20W MF 201
C8146 0.1UF 10% 25V X5R 402
PLACE_NEAR=U8040.C2:7mm

3.3V SUS Detect

PP3V3_S5
BYPASS=U8130.6:2.3mm
C8130 0.1UF 10% 6.3V CERM-X5R 0201
No stuff C8131, 12ms Min delay time
U8130 Sense input threhold is 3.07V
PP3V3_SUS → R8133 100K 5% 1/20W MF 201
PP3V3_SUS
CRITICAL U8130 TPS3808G33 QFN (VDD SENSE CT GND THRM PAD RESET* MR*)
PM_RSMRST_L (OUT)
TP_SUS_PGOOD_MR_L
SUS_PGOOD_CT
NO STUFF C8131 1000PF 10% 16V X7R-CERM 0201

CHGR VFRQ Generation

PP3V42_G3H
R8131 330K 5% 1/20W MF 201
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency
CHGR_VFRQ (OUT)
Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (D G S)
PM_SLP_S3_R_L

S0 Rail PGOOD Circuitry

(ISL version used for development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

PP1V05_S0 → R8160 6.04K 1% 1/20W MF 201 → P5V_DIV_VMON (5V Divider: 3.19V @ 4.5Vmin)
R8170 15K 1% 1/20W MF 201
R8172 6.04K 1% 1/20W MF 201 → P1V5_DIV_VMON (1.5V Divider: 0.718V @ 1.45Vmin)
R8161 15K 1% 1/20W MF 201
R8171 15K 1% 1/20W MF 201
R8173 15K 1% 1/20W MF 201 → P1V05_DIV_VMON (1.05V Divider: 0.723V @ 1.02Vmin)
S0PGOOD_ISL
PP3V3_S0 → C8160 0.1UF 10% 6.3V CERM-X5R 0201
U8160 ISL88042IRTEZ TDFN (VDD V2MON V3MON V4MON MR* RST* GND THRM_PAD)
353S2310 (IPU)
NC
ALL_SYS_PWRGD_R → R8162 330 5% 1/20W MF 201 → ALL_SYS_PWRGD (OUT)

PM_SLP_S3_BUF_L
R8167 10K 5% 1/20W MF 201
P1V8S3_PGOOD (IN) → R8166 100 5% 1/20W MF 201
P5VS4RS3_PGOOD (IN) → R8165 100 5% 1/20W MF 201
P1V05S0_PGOOD (IN) → R8164 100 5% 1/20W MF 201
DDRREG_PGOOD (IN) → R8168 100 5% 1/20W MF 201

S0 Enables

PP3V3_S5
BYPASS=U8180.6:3mm
C8180 0.1UF 10% 6.3V CERM-X5R 0201
PM_SLP_S3_L (IN) → R8178 100 5% 1/20W MF 201 → PM_SLP_S3_R_L
U8180 MC74VHC1G08 SC70-HF
PM_SLP_S3_BUF_L (MAKE_BASE=TRUE)
NOSTUFF R8180 330K 5% 1/20W MF 201

P1V05_EN_D
NO STUFF D8185 SM-201 RB521ZS-30
NO STUFF R8138 820 5% 1/20W MF 201
R8185 0 5% 1/20W MF 0201
P3V3S0_EN_D
R8184 330 5% 1/20W MF 201
D8184 SM-201 RB521ZS-30
R8186 20K 5% 1/20W MF 201
R8187 0 5% 1/20W MF 0201
PM_SLP_S3_BUF_L (OUT)
P5VS0_EN (MAKE_BASE=TRUE) → P5VS0_EN (OUT)
P3V3S0_EN (MAKE_BASE=TRUE) → P3V3S0_EN (OUT)
P1V05S0_EN (MAKE_BASE=TRUE) → P1V05S0_EN (OUT)
NO STUFF C8185 0.22UF 10% 10V CERM 402
C8186 0.1UF 20% 10V CERM 402
NO STUFF C8187 0.68UF 10% 6.3V CERM 402

SUS Enables

PM_SLP_SUS_L (IN) → PM_SLP_SUS_L (MAKE_BASE=TRUE) → PM_SLP_SUS_L (OUT)
R8190 0 5% 1/20W MF 0201
P3V3SUS_EN (MAKE_BASE=TRUE) → P3V3SUS_EN (OUT)
NO STUFF C8190 0.1UF 10% 25V X5R 402

SYNC_MASTER=J43_MLB SYNC_DATE=09/16/2013
PAGE TITLE: Power Control
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
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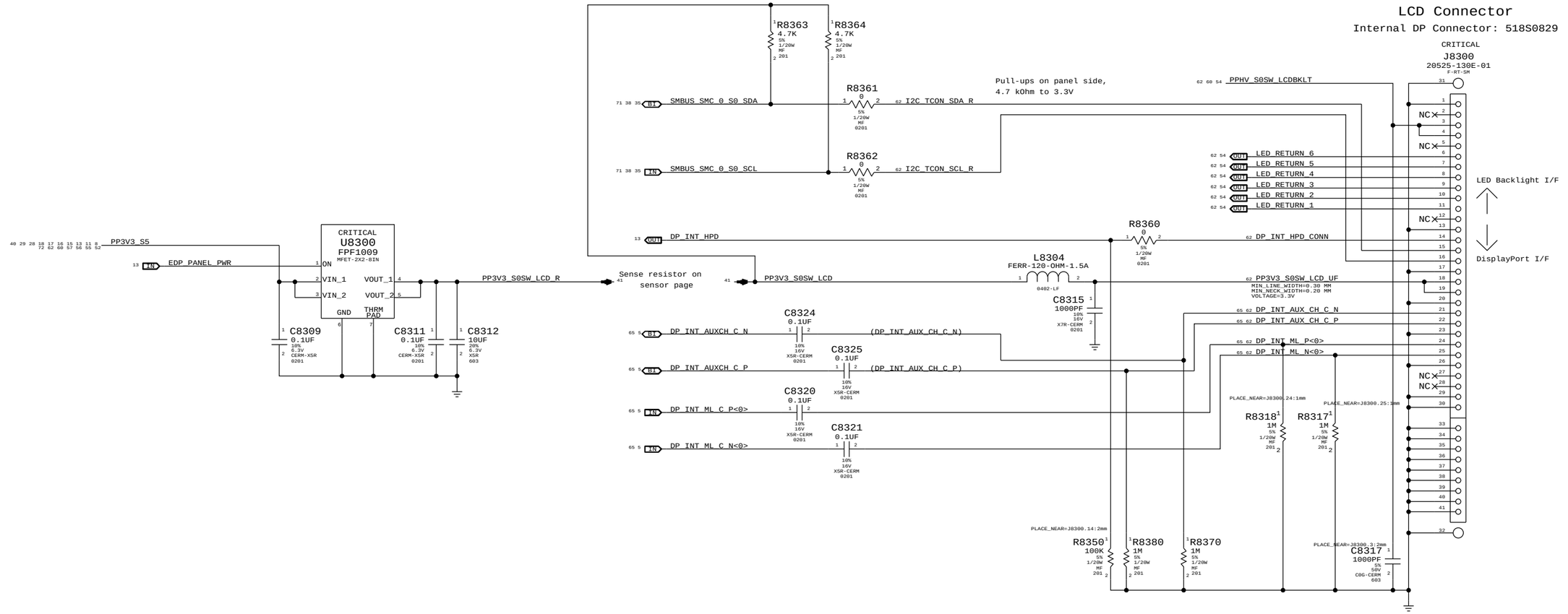

SYNC_MASTER=J43_MLB SYNC_DATE=09/11/2012

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

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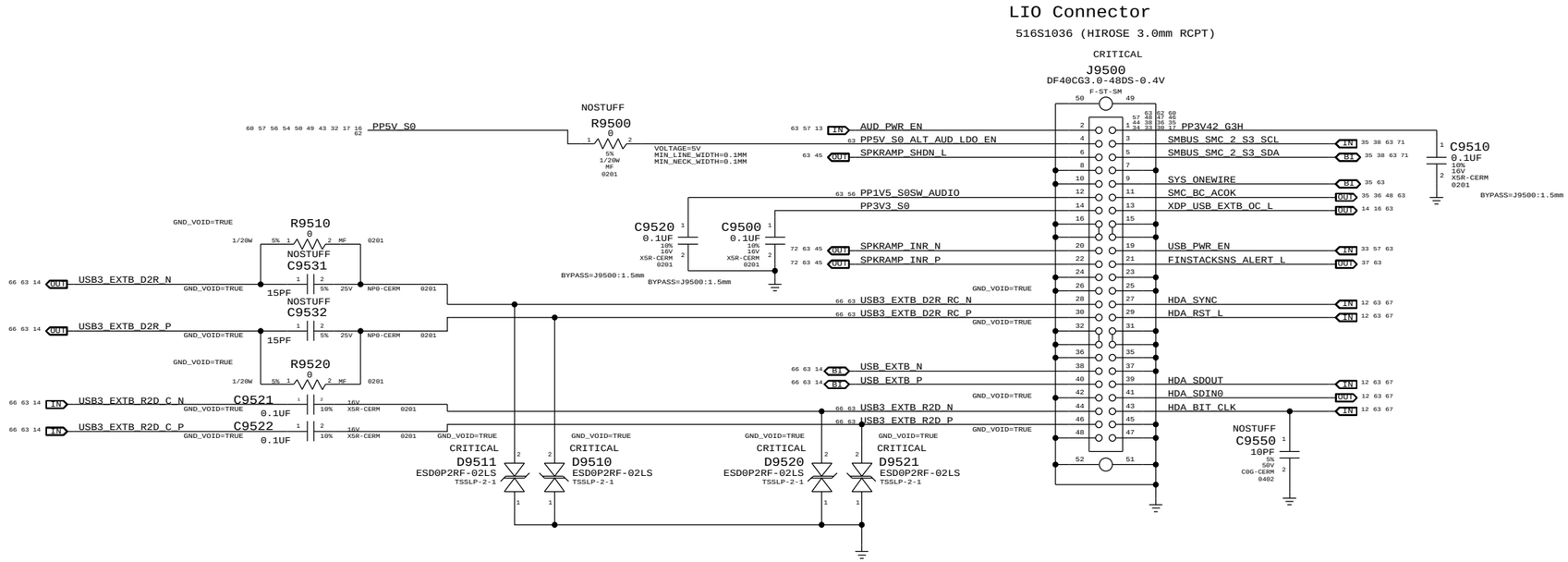

SYNC_MASTER=CLEAN_J41	SYNC_DATE=11/13/2012
PAGE TITLE	LIO Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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8 7 6 5 4 3 2 1

D C B A

"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS

PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_OTHER_ISNS

PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H

PP3V42_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H

PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE

PPVRTC_G3H

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S5
PP5V_S5

PP5V_S4RS3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4RS3
PP5V_S4RS3
PP5V_S4RS3
PP5V_S4RS3
PP5V_S4RS3
PP5V_S4RS3

PP5V_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S5 ×30

PP3V3_S4
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4 ×10

PP3V3_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SUS ×15

PP3V3_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3 ×15

PP3V3_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0 ×30

PP3V3_S45W_SNS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S45W_SNS ×20

PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_SSD
PP3V3_S0SW_SSD

PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4_TBTAPWR

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V8_S3
PP1V8_S3

PP1V2_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3 ×8

PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_SUS
PP1V05_SUS

PP1V05_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V05_S0 ×5

PP1V05_S0SW_PCH_HSIO
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0SW_PCH_HSIO
PP1V05_S0SW_PCH_HSIO

PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V6_S0_DDRVTT
PP0V6_S0_DDRVTT

LCDBKLT Rail

PPHV_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=16V
MAKE_BASE=TRUE

PPHV_S0SW_LCDBKLT
PPHV_S0SW_LCDBKLT

TBT Rails (off when no cable)

PP15V_TBT
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE

PP15V_TBT
PP15V_TBT

PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_TBTLC
PP3V3_TBTLC

PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVIN_S4SW_TBTBST_FET
VOLTAGE=8.6V

PPVIN_SW_TBTBST
VOLTAGE=12.8V

CPU "VCORE" RAILS

PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCC_S0_CPU
PPVCC_S0_CPU

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

2A max supply
1.84A

SYNC_MASTER=WILL J43	SYNC_DATE=12/17/2012
PAGE TITLE	Power Aliases
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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	SHEET 60 OF 73

LPDDR3 Command/Address

		MAKE_BASE			
7	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>		20 24 68
7	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>		20 24 68
7	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>		20 24 68
7	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>		20 24 68
7	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>		20 24 68
7	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>		20 24 68
68 61 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>		7 20 24 61 68
7	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>		20 24 68
7	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>		20 24 68
7	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>		20 24 68
7	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>		21 24 68
7	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>		21 24 68
7	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>		21 24 68
7	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>		21 24 68
7	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>		21 24 68
7	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>		21 24 68
68 61 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>		7 21 24 61 68
7	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>		21 24 68
7	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>		21 24 68
7	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>		21 24 68
68 61 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>		7 20 21 24 61 68
61 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1		7 61
61 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2		7 61
7	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>		22 24 68
7	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>		22 24 68
7	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>		22 24 68
7	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>		22 24 68
7	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>		22 24 68
7	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>		22 24 68
68 61 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>		7 22 24 61 68
7	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>		22 24 68
7	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>		22 24 68
7	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>		22 24 68
7	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>		23 24 68
7	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>		23 24 68
7	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>		23 24 68
7	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>		23 24 68
7	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>		23 24 68
7	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>		23 24 68
68 61 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>		7 23 24 61 68
7	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>		23 24 68
7	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>		23 24 68
7	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>		23 24 68
68 61 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>		7 22 23 24 61 68
61 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3		7 61
61 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4		7 61

Memory Bit/Byte Swizzle

		MAKE_BASE			
20	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<9>		7 68
20	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<12>		7 68
20	=MEM_A_DQ<2>	TRUE	MEM_A_DQ<10>		7 68
20	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<11>		7 68
20	=MEM_A_DQ<4>	TRUE	MEM_A_DQ<8>		7 68
20	=MEM_A_DQ<5>	TRUE	MEM_A_DQ<13>		7 68
20	=MEM_A_DQ<6>	TRUE	MEM_A_DQ<14>		7 68
20	=MEM_A_DQ<7>	TRUE	MEM_A_DQ<15>		7 68
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20	=MEM_A_DQ<9>	TRUE	MEM_A_DQ<1>		7 68
20	=MEM_A_DQ<10>	TRUE	MEM_A_DQ<2>		7 68
20	=MEM_A_DQ<11>	TRUE	MEM_A_DQ<7>		7 68
20	=MEM_A_DQ<12>	TRUE	MEM_A_DQ<4>		7 68
20	=MEM_A_DQ<13>	TRUE	MEM_A_DQ<5>		7 68
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20	=MEM_A_DQ<15>	TRUE	MEM_A_DQ<6>		7 68
20	=MEM_A_DQ<16>	TRUE	MEM_A_DQ<29>		7 68
20	=MEM_A_DQ<17>	TRUE	MEM_A_DQ<28>		7 68
20	=MEM_A_DQ<18>	TRUE	MEM_A_DQ<27>		7 68
20	=MEM_A_DQ<19>	TRUE	MEM_A_DQ<31>		7 68
20	=MEM_A_DQ<20>	TRUE	MEM_A_DQ<24>		7 68
20	=MEM_A_DQ<21>	TRUE	MEM_A_DQ<25>		7 68
20	=MEM_A_DQ<22>	TRUE	MEM_A_DQ<26>		7 68
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20	=MEM_A_DQ<24>	TRUE	MEM_A_DQ<18>		7 68
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20	=MEM_A_DQ<26>	TRUE	MEM_A_DQ<16>		7 68
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20	=MEM_A_DQ<29>	TRUE	MEM_A_DQ<19>		7 68
20	=MEM_A_DQ<30>	TRUE	MEM_A_DQ<22>		7 68
20	=MEM_A_DQ<31>	TRUE	MEM_A_DQ<17>		7 68
21	=MEM_A_DQ<32>	TRUE	MEM_A_DQ<41>		7 68
21	=MEM_A_DQ<33>	TRUE	MEM_A_DQ<44>		7 68
21	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<46>		7 68
21	=MEM_A_DQ<35>	TRUE	MEM_A_DQ<47>		7 68
21	=MEM_A_DQ<36>	TRUE	MEM_A_DQ<40>		7 68
21	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<45>		7 68
21	=MEM_A_DQ<38>	TRUE	MEM_A_DQ<42>		7 68
21	=MEM_A_DQ<39>	TRUE	MEM_A_DQ<43>		7 68
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21	=MEM_A_DQ<41>	TRUE	MEM_A_DQ<37>		7 68
21	=MEM_A_DQ<42>	TRUE	MEM_A_DQ<34>		7 68
21	=MEM_A_DQ<43>	TRUE	MEM_A_DQ<39>		7 68
68 61 21 7	MEM_A_DQ<32>	TRUE	MEM_A_DQ<32>		7 21 61 68
21	=MEM_A_DQ<45>	TRUE	MEM_A_DQ<33>		7 68
21	=MEM_A_DQ<46>	TRUE	MEM_A_DQ<35>		7 68
21	=MEM_A_DQ<47>	TRUE	MEM_A_DQ<38>		7 68
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20	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<1>		7 68
20	=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<0>		7 68
20	=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<0>		7 68
20	=MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<3>		7 68
20	=MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<3>		7 68
20	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<2>		7 68
20	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<2>		7 68
21	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<5>		7 68
21	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<5>		7 68
21	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<4>		7 68
21	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<4>		7 68
68 61 21 7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>		7 21 61 68
68 61 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>		7 21 61 68
21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>		7 68
21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>		7 68

		MAKE_BASE			
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22	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<13>		7 68
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22	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<14>		7 68
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68 61 23 7	MEM_B_DQ<33>	TRUE	MEM_B_DQ<33>		7 23 61 68
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22	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<1>		7 68
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23	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<7>		7 68
68 61 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>		7 23 61 68
68 61 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<7>		7 68
68 61 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>		7 23 61 68

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN	(Need 6 TPs)	29 35 36 37 39
TRUE	WIFI_EVENT_L		29 35 36
TRUE	PCIE_AP_R2D_N		29 67
TRUE	PCIE_AP_R2D_P		29 67
TRUE	PCIE_CLK100M_AP_N		12 29 67
TRUE	PCIE_CLK100M_AP_P		12 29 67
TRUE	PCIE_AP_D2R_P		14 29 67
TRUE	PCIE_AP_D2R_N		14 29 67
TRUE	PCIE_WAKE_L		13 29 31
TRUE	AP_RESET_CONN_L		29
TRUE	AP_CLKREQ_O_L		29
TRUE	USB_BT_CONN_P		29 66
TRUE	USB_BT_CONN_N		29 66
TRUE	PP3V3_S4		25 26 27 29 34 36 37 60 60 62

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST

TRUE	PP3V3_S0SW_SSD_FLT	(Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>		30 65
TRUE	PCIE_SSD_R2D_P<3..0>		30 65
TRUE	PP3V3_S0		40 41 42 43 54 57 59 60 62 63 72
TRUE	SSD_RESET_CONN_L		30
TRUE	SSD_CLKREQ_CONN_L		30
TRUE	SMC_OOB1_R2D_CONN_L		30
TRUE	SMC_OOB1_D2R_CONN_L		30
TRUE	SSD_PCIE_SEL_L		30
TRUE	SSD_SR_EN_L		15 30
TRUE	SMC_PWRFAIL_WARN_L		30 35
TRUE	SSD_PWR_EN		15 30 56 57
TRUE	PCIE_SSD_D2R_N<3..0>		12 30 65
TRUE	PCIE_SSD_D2R_P<3..0>		12 30 65
TRUE	PCIE_CLK100M_SSD_N		12 30 65
TRUE	PCIE_CLK100M_SSD_P		12 30 65

(Need to add 6 GND TPs)

J4002: Camera Connector

FUNC_TEST

TRUE	MIPI_CLK_CONN_N		32 70
TRUE	MIPI_CLK_CONN_P		32 70
TRUE	CAM_SENSOR_WAKE_L_CONN		32
TRUE	MIPI_DATA_CONN_N		32 70
TRUE	MIPI_DATA_CONN_P		32 70
TRUE	SMBUS_SMC_1_S0_SDA		14 32 35 38 41 42 67 71
TRUE	SMBUS_SMC_1_S0_SCL		14 32 35 38 41 42 67 71
TRUE	I2C_CAM_SCK		31 32
TRUE	I2C_CAM_SDA		31 32
TRUE	PP5V_S3RS0_ALSCAM_F	(Need TBD TPs)	32

(Need to add TBD GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST

TRUE	SPI_ALT_IO3_HOLD_L	44
TRUE	SPI_ALT_IO2_WP_L	44
TRUE	LPC_AD<3..0>	14 35 67
TRUE	SPI_ALT_IO0_MOSI	44
TRUE	XDP_LPCPLUS_GPIO	15 16
TRUE	LPCPLUS_RESET_L	67
TRUE	SMC_TDO	35 36
TRUE	TP_SMC_TRST_L	
TRUE	TP_SMC_MD1	
TRUE	SMC_TX_L	35 36
TRUE	SPI_ALT_IO1_MISO	44
TRUE	LPC_FRAME_L	14 35 67
TRUE	SPIROM_USE_MLB	15 44
TRUE	PM_CLKRUN_L	13 35
TRUE	SPI_ALT_CLK	44
TRUE	SPI_ALT_CS_L	44
TRUE	LPC_SERIRQ	15 35
TRUE	LPC_PWRDWN_L	13 35
TRUE	SMC_TDI	35 36
TRUE	SMC_TCK	35 36 44
TRUE	SMC_RESET_L	35 36 44 48
TRUE	SMC_ROMBOOT	
TRUE	SMC_RX_L	35 36
TRUE	SMC_TMS	35 36 44

(Need to add 6 GND TPs)

TP93	TRUE	GND

J6000: Fan Connector

FUNC_TEST

TRUE	PP5V_S0	16 17 32 43 49 50 54 56 57 59 60
TRUE	FAN_RT_TACH	43
TRUE	FAN_RT_PWM	43

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST

TRUE	SMC_LID	34 35 36 46
TRUE	TPAD_SPI_MISO_R	34
TRUE	USB_TPAD_P	14 34 66
TRUE	USB_TPAD_N	14 34 66
TRUE	TPAD_SPI_CLK_R	34
TRUE	TPAD_WAKE_L	34
TRUE	TPAD_SPI_MOSI_R	34
TRUE	PP3V3_S4_IPD	34
TRUE	TPAD_SPI_CS_R_L	34
TRUE	TPAD_SPI_IF_EN_CONN	34
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN	34
TRUE	PP5V_S4_IPD	34
TRUE	TPAD_USB_IF_EN_CONN	34
TRUE	SMBUS_SMC_3_SDA	34 35 38 42 71
TRUE	SMBUS_SMC_3_SCL	34 35 38 42 71
TRUE	SMC_LSOC_RST_L	34 36
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMC_ONOFF_L	34 35 36

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST

TRUE	PPDCIN_G3H	(Need 4 TPs)	47 48 60 62
TRUE	PP5V_S4RS3	(Need 3 TPs)	32 33 45 47 52 53 56 60

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	45 72
TRUE	SPKRAMP_ROUT_N	45 72

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	(Need 4 TPs)	46 48
TRUE	SMBUS_SMC_5_G3_SCL		35 38 46 48 71
TRUE	SMBUS_SMC_5_G3_SDA		35 38 46 48 71
TRUE	SYS_DETECT_L		46

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST

TRUE	PPHV_S0SW_LCDBKLT	(Need 2 TPs)	54 58 60
TRUE	LED_RETURN_6		54 58
TRUE	LED_RETURN_5		54 58
TRUE	LED_RETURN_4		54 58
TRUE	LED_RETURN_3		54 58
TRUE	LED_RETURN_2		54 58
TRUE	LED_RETURN_1		54 58
TRUE	DP_INT_HPD_CONN		58
TRUE	I2C_TCON_SDA_R		58
TRUE	I2C_TCON_SCL_R		58
TRUE	PP3V3_S0SW_LCD_UF	(Need 2 TPs)	58
TRUE	DP_INT_AUX_CH_C_N		58 65
TRUE	DP_INT_AUX_CH_C_P		58 65
TRUE	DP_INT_ML_P<0>		58 65
TRUE	DP_INT_ML_N<0>		58 65

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_ANODE	54
TRUE	KBDLED_FB	54

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST

TP76	TRUE	XDP_CPU_TCK	6 16 65
TP77	TRUE	XDP_PCH_TCK	12 16 67
TP78	TRUE	XDP_CPU_TDI	6 16 65
TP79	TRUE	XDP_CPU_TDO	6 16 65
TP80	TRUE	XDP_CPUPCH_TRST_L	6 12 16 65
TP81	TRUE	XDP_CPU_TMS	6 16 65
TP82	TRUE	XDP_PCH_TMS	12 16 67
TP83	TRUE	XDP_PCH_TDI	12 16 67
TP84	TRUE	XDP_PCH_TDO	12 16 67
TP85	TRUE	XDP_CPU_PREQ_L	6 16 65
TP86	TRUE	XDP_CPU_PRDY_L	6 16 65
TP87	TRUE	XDP_CPU_VCCST_PWRGD	16
TP88	TRUE	PM_RSMRST_L	13 57
TP89	TRUE	XDP_SYS_PWROK	16
TP90	TRUE	PM_SYSRST_L	13 17 35
TP91	TRUE	CPU_CFG<3>	6 16 65
TP92	TRUE	PP1V05_S0	6 9 11 15 16 17 36 40 49 53 56 57 60 62

(Need to add 2 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	27 39 40 47 48 54 60
TRUE	PPVIN_S4SW_TBTBST_FET	27 60
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	39 49 50 51 53 60
TRUE	PPDCIN_G3H	47 48 60 62
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	PPVRTC_G3H	8 12 13 17 60
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 72
TRUE	PP3V3_SUS	8 11 14 18 44 55 56 57 60
TRUE	PP3V3_S3	15 18 19 34 38 39 56 60 63
TRUE	PP3V3_S0	60 62 63 72
TRUE	PP3V3_S0SW_SSD	8 12 13 14 15 16 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	PP1V5_S0	30 39 60
TRUE	PP1V05_S0	8 55 56 57 60
TRUE	PP15V_TBT	6 9 11 15 16 17 36 40 49 53 56 57 60 62
TRUE	PP3V3_TBTLC	27 28 60
TRUE	PP1V05_TBT	17 18 25 26 60
TRUE	PPVCC_S0_CPU	26
TRUE	PP1V05_TBTCIO	8 10 40 50 60
TRUE	PPBUS_S5_HS_OTHER_ISNS	26 60
TRUE	PPDCIN_G3H_ISOL	39 52 60
TRUE	PP3V3_S4	40 47 48 60

(Need to add 27 GND TPs)

NO_TEST Nets

NO_TEST

MAKE_BASE

62	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	62	
62	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	62	
62 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 62	
62 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 62	
62 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 62	
62 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 62	
62 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 62	
62 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 62	
62 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 62	
62 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 62	CPU/PCH
62 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 62	
62 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 62	
62 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 62	
62 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 62	
65	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5	
65	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5	
62 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 62	
62 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 62	
62 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 62	
62 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 62	
62 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 62	
62 35	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	35 62	
62	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	62	
62	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	62	
62	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	62	
62 35	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	35 62	
62 35	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	35 62	
62 35	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	35 62	
62 35	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	35 62	
62 35	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	35 62	
62	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	62	SMC
62	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	62	
62	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	62	
62 35	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	35 62	
62 35	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	35 62	
62 35	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	35 62	
62 35	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	35 62	
62 35	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	35 62	
69	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25	
69	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25	
69	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25	
69	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25	
62 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 62	
69 62	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	62 69	
69 62	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	62 69	
69 62 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 62 69	
69 62 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 62 69	TBT
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>		
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>		
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>		
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>		
62 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 62	
62 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 62	
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>		
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>		
62 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 62	
62 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 62	

Unused nets with offpage

(Nets with offpages not used on this project)

PCH_BT_UART_D2R	15	
PCH_BT_UART_R2D	15	
PCH_BT_UART_RTS_L	15	
PCH_BT_UART_CTS_L	15	
AUD_SPI_CS_L	15	
AUD_SPI_CLK	15	
AUD_SPI_MISO	15	
AUD_SPI_MOSI	15	
HDMITBTMUX_LATCH	13	
HDD_PWR_EN	15	
WOL_EN	14	
BT_PWRRST_L	15	
HDMITBTMUX_FLAG	13	
FW_PWR_EN		
FW_PME_L		
ENET_MEDIA_SENSE	15	
LCD_PSR_EN	15	
LCD_IRQ_L	15	
ODD_PWR_EN_L	13	
ENET_LOW_PWR	13	
AUD_IP_PERIPHERAL_DET		
AUD_I2C_INT_L		
AP_PCIE_DEV_WAKE	13	

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

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Func Test / No Test

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Functional Test Points

J9500: LIO Connector

FUNC_TEST

TRUE	AUD_PWR_EN	13 57 59
TRUE	PP5V_S0_ALT_AUD_LDO_EN	59
TRUE	SPKRAMP_SHDN_L	45 59
TRUE	PP1V5_S0SW_AUDIO	56 59
TRUE	PP3V3_S0	60 62 72 5 11 12 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	SPKRAMP_INR_N	45 59 72
TRUE	SPKRAMP_INR_P	45 59 72
TRUE	USB3_EXTB_D2R_RC_N	59 63 66
TRUE	USB3_EXTB_D2R_RC_P	59 63 66
TRUE	USB_EXTB_N	14 59 66
TRUE	USB_EXTB_P	14 59 66
TRUE	USB3_EXTB_R2D_N	59 63 66
TRUE	USB3_EXTB_R2D_P	59 63 66
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMBUS_SMC_2_S3_SCL	35 38 59 71
TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71
TRUE	SYS_ONEWIRE	35 59
TRUE	SMC_BC_ACOK	35 36 48 59
TRUE	XDP_USB_EXTB_OC_L	14 16 59
TRUE	USB_PWR_EN	33 57 59
TRUE	FINSTACKSNS_ALERT_L	37 59
TRUE	HDA_SYNC	12 59 67
TRUE	HDA_RST_L	12 59 67
TRUE	HDA_SDOUT	12 59 67
TRUE	HDA_SDIN0	12 59 67
TRUE	HDA_BIT_CLK (Need to add 5 GND TPs)	12 59 67

J6955: HALL EFFECT Connector

FUNC_TEST

TRUE	SMC_LID_R	46
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63

Power Aliases

63 62 60 56 39 38 34 19 18 15 PP3V3_S3 = PP3V3_S3 15 18 19 34 38 39 56 60 62 63

NO_TEST Nets

NO_TEST MAKE_BASE

66 63 14	NC_USB3RPCIE_SD_D2RP	TRUE	TRUE	NC_USB3RPCIE_SD_D2RP	14 63 66	
66 63 14	NC_USB3RPCIE_SD_D2RN	TRUE	TRUE	NC_USB3RPCIE_SD_D2RN	14 63 66	
66 63 14	NC_USB3RPCIE_SD_R2D_CP	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CP	14 63 66	CPU/PCH
66 63 14	NC_USB3RPCIE_SD_R2D_CN	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CN	14 63 66	
63 37 35	NC_SMC_ADC16	TRUE	TRUE	NC_SMC_ADC16	35 37 63	SMC

Bead Probes

66 59 14	USB3_EXTB_D2R_N	BEAD-PROBE	BPA511
66 59 14	USB3_EXTB_D2R_P	BEAD-PROBE	BPA510
66 63 59	USB3_EXTB_D2R_RC_N	BEAD-PROBE	BPA520
66 63 59	USB3_EXTB_D2R_RC_P	BEAD-PROBE	BPA521
66 59 14	USB3_EXTB_R2D_C_N	BEAD-PROBE	BPA513
66 59 14	USB3_EXTB_R2D_C_P	BEAD-PROBE	BPA512
66 63 59	USB3_EXTB_R2D_N	BEAD-PROBE	BPA523
66 63 59	USB3_EXTB_R2D_P	BEAD-PROBE	BPA522

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
XDP_SDCONN_STATE_CHANGE_L	15 16
SD_PWR_EN	15

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 36
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 16 62
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16 62
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_45S	CPU_ITP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 35
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 35 36 49
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_RMTL	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	
	CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
(ESB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 49
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 49
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

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CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 62
	USB_80D	USB	USB_BT_CONN_N	29 62
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 34 62
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 34 62
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 34
	SPI_45S	SPI	TPAD_SPI_MISO	15 34
	SPI_45S	SPI	TPAD_SPI_CLK	15 34
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 33
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 33
	UART_45S	UART	SMC_DEBUGPRT_TX_L	33 35 36
	UART_45S	UART	SMC_DEBUGPRT_RX_L	33 35 36
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	33
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 33
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 33
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 59 63
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 59 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP	14 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN	14 63
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 35 62
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 35 62
	LPC_45S	LPC	LPCPLUS_RESET_L	62
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 35
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 19 38 54
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 19 38 54
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 38
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 38
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 71
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 71
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 59 63
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 59 63
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 59 63
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 59 63
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 59 63
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 36
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	35 36
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 44
	SPI_45S	SPI	SPI_CLK	44
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 44
	SPI_45S	SPI	SPI_MOSI	44
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 44
	SPI_45S	SPI	SPI_MISO_R	44
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 44
	SPI_45S	SPI	SPI_CS0_L	44
	SPI_45S	SPI	SPI_SMC_CLK	35 44
	SPI_45S	SPI	SPI_SMC_MOSI	35 44
	SPI_45S	SPI	SPI_SMC_MISO	35 44
	SPI_45S	SPI	SPI_SMC_CS_L	35 44
	SPI_45S	SPI	SPI_MLB_CLK	44
	SPI_45S	SPI	SPI_MLB_IO2_WP_L	44
	SPI_45S	SPI	SPI_MLB_IO3_HOLD_L	44
	SPI_45S	SPI	SPI_MLB_CS_L	44
	SPI_45S	SPI	SPI_IO<2>	14 44
	SPI_45S	SPI	SPI_IO2_R	44
	SPI_45S	SPI	SPI_IO<3>	14 44
	SPI_45S	SPI	SPI_IO3_R	44
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	29 62
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	29 62
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 29 62
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 29 62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16 62
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16 62
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16 62
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16 62
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 21 24 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 24 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 21 24 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 21 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 21 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 21 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 22 23 24 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 22 24 61
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 23 24 61
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 61
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 23 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 23 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 23 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 61
	MEM_PWR		PP1V2_S3	17 19 20 21 22 23 40 61 69
	MEM_PWR		PP0V6_S3_MEM_VREFCA_A	18 19 20 21
	MEM_PWR		PP0V6_S3_MEM_VREFDQ_A	18 19 20 21
	MEM_PWR		PP0V6_S3_MEM_VREFCA_B	18 19 22 23
	MEM_PWR		PP0V6_S3_MEM_VREFDQ_B	18 19 22 23

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	62
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	62
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2>	62
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2>	62
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	62
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP	25 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN	25 62
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 62
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 62
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 62
		S2_MEM_PWR	PP1V35_CAM	31 32
		S2_MEM_PWR	PP0V675_CAM_VREF	31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SCL	35 38 58
SMBUS_SMC_0_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SDA	35 38 58
SMBUS_SMC_1_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 67
SMBUS_SMC_1_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 67
SMBUS_SMC_2_S3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SCL	35 38 59 63
SMBUS_SMC_2_S3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SDA	35 38 59 63
SMBUS_SMC_3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_3_SCL	34 35 38 42 62
SMBUS_SMC_3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_3_SDA	34 35 38 42 62
SMBUS_SMC_5_G3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SCL	35 38 46 48 62
SMBUS_SMC_5_G3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SDA	35 38 46 48 62

SMBus Charger Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SENSE_DIFFPAIR			CHGR_CSI_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	48
	2TO1_DIFFPAIR		CHGR_CSI_R_P	48
	2TO1_DIFFPAIR		CHGR_CSI_R_N	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	48
	2TO1_DIFFPAIR		CHGR_CSO_R_P	41 48
	2TO1_DIFFPAIR		CHGR_CSO_R_N	41 48

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	40 50
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	40 41
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	40 41
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	40
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	39
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	40 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	40 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	41 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	41 42
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	45 59 63
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	45 59 63
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	45
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	45
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	45 62
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	45 62
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 49 52 60 62 63
		SB_POWER	PP3V3_S0	8 11 13 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
	GND		GND	

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<rdar://component/512995> J41 HW EE Schematic | Pre Proto 1
<rdar://component/508412> J41 HW EE Schematic | Proto 1
<rdar://component/508413> J41 HW EE Schematic | EVT
<rdar://component/508414> J41 HW EE Schematic | DVT

Kismet:

afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

<rdar://component/497591> MobileMac HW | Task
<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
<rdar://component/497588> MobileMac HW | Layout
<rdar://component/497590> MobileMac HW | Investigation
<rdar://component/497589> MobileMac HW | Architecture

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