

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J44 MLB-4GB SCHEMATIC

08/20/2013

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ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0052	1	SCHEM,MLB-4GB,J44	SCH	CRITICAL	
820-3536	1	PCBF,MLB-4GB,J44	PCB	CRITICAL	

DRAWING TITLE <PART_DESCRIPTION>		DRAWING NUMBER <SCH_NUM>	SIZE D
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BOM Groups

BOM GROUP	BOM OPTIONS
J44_COMMON	ALTERNATE , COMMON , J44_COMMON1 , J44_COMMON2 , J44_COMMON3 , J44_COMMON4 , J44_PROGPARTS
J44_COMMON1	TBTHV:P15V, SKIP_5V3V3: AUDIBLE, SPI: DUAL_IO
J44_COMMON2	EDP, EDP_LS_CAP, CAMERA_3V3: S0, CAM_WAKE: NO, CAM_XTAL: NO, MEM_ODT: PU, VCORE_FETS
J44_COMMON3	XDP, LPCPLUS, BKLT: PROD, CPUTHRM: ALRT, LOADRC: NO, OTHERRC: NO, DDRRC: NO, TBTRC: NO, BMONRC: NO
J44_PROGPARTS	SMC_PROG: PVT, BOOTROM: PVT, TBTRM: PVT, TPAD_PSOC: PROG
ENGISNS	LOADISNS, OTHERISNS, DDRISNS, TBTISNS, BMONISNS

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3918	1	EPROM, FALCON RIDGE (V13.7) J44	U2890	CRITICAL	TBTROM: PVT

SMC

341S3922	1	IC, SMC-B1, EXT(V2.16F39), PVT, J44	U5000	CRITICAL	SMC_PROG: PVT
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EFI ROM

341S3924	1	IC, EFI ROM (V0116), PVT, J44	U6100	CRITICAL	BOOTROM: PVT
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PSOC

341S3862	1	IC, TRKPD/KYBD PSOC, CU ONLY (V224) J44	U4801	CRITICAL	TPAD_PSOC: PROG
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Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4596	1	HSWULT, SR18A, PRQ, CO, 2.4, 28W, 2+3, 3M, BGA	U0500	CRITICAL	CPU_HSW: 2.4G
337S4597	1	HSWULT, SR189, PRQ, CO, 2.6, 28W, 2+3, 3M, BGA	U0500	CRITICAL	CPU_HSW: 2.6G
337S4598	1	HSWULT, SR188, PRQ, CO, 2.8, 28W, 2+3, 4M, BGA	U0500	CRITICAL	CPU_HSW: 2.8G
338S1247	1	IC, TBT, FR-4C, A0, PRQ, CIO, SR1JC, FCBGA288	U2800	CRITICAL	
338S1186	1	IC, BCM15700A2, S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
376S1194	2	MOSFET, N-CH, 30V, 15.3A, 12M, 8P 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET: VSHY
376S1193	2	MOSFET, N-CH, 30V, 22A, 6.0M, 8P 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET: VSHY
376S0964	2	MOSFET, N-CH, 25V, 30A, 9.6M, 8P 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET: REN
376S1104	2	MOSFET, N-CH, 25V, 30A, 6.1M, 8P 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET: REN

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson alt to NDK
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
138S0725	138S0724		ALL	Samsung alt to Murata
376S1032	376S0855		ALL	Toshiba alt for Diodes Dual
376S1129	376S0855		ALL	NXP Alt for Diodes Dual
376S1089	376S1128		ALL	NXP Alt for Diodes Single
353S3452	353S1286		ALL	Maxim alt to Microchip
376S1180	376S0761		ALL	Renesas alt to Vishay
128S0364	128S0264		ALL	Sanyo 2nd Factory alt
107S0254	107S0241		ALL	Cyntec alt to TFT
138S0843	138S0674		ALL	Samsung alt to Murata (BKLT)
138S0803	138S0639		ALL	Samsung alt to Murata (BKLT)
138S0846	138S0811		ALL	Samsung alt to Murata (BKLT)
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
127S0164	127S0162		ALL	Rohm alt to Vishay
353S4070	353S4069		ALL	Pericom alt to TI DP Mux U9750
353S4068	353S4069		ALL	NXP alt to TI DP Mux U9750
353S3814	353S3812		ALL	TI alt to NXP
311S0649	311S0541		ALL	ONsemi alt to Toshiba
128S0436	128S0392		ALL	Kemet alt to Sanyo

SYMC MASTER: J44 SYMC DATE: 08/20/2013

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BOM Configuration

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0054	COMMON,MLB-4GB,J44	J44_COMMON
985-0053	DEV,MLB-4GB,J44	XDP_CONN
639-4878	PCBA,MLB-4GB,2.4G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-4879	PCBA,MLB-4GB,2.4G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G-ELPIDA,CAMDRAM:ELPIDA
639-4880	PCBA,MLB-4GB,2.4G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G-MICRON,CAMDRAM:MICRON
639-5272	PCBA,MLB-4GB,2.6G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5273	PCBA,MLB-4GB,2.6G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G-ELPIDA,CAMDRAM:ELPIDA
639-5274	PCBA,MLB-4GB,2.6G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G-MICRON,CAMDRAM:MICRON
639-5275	PCBA,MLB-4GB,2.8G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5276	PCBA,MLB-4GB,2.8G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G-ELPIDA,CAMDRAM:ELPIDA
639-5277	PCBA,MLB-4GB,2.8G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G-MICRON,CAMDRAM:MICRON
685-0074	VCORE,FET,VSHY,J44	VCORE_FET:VSHY
685-0075	VCORE,FET,REN,J44	VCORE_FET:REN

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0054	1	J44 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-0053	1	J44 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SUB-BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0074	1	VCORE,FET,VSHY,J44	VCOREFETS	CRITICAL	VCORE_FETS

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0075	685-0074		ALL	RENDSAS ALT TO VSHY

DRAM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0704	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,P,DIE,96FBGA	U4000	CRITICAL	4G-ELPIDA
333S0700	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,HUMA,96FBGA	U4000	CRITICAL	4G_HYNIX_H
333S0698	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,REV E,96FBGA	U4000	CRITICAL	4G-MICRON
333S0715	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,P,DIE,96FBGA	U4000	CRITICAL	4G-ELPIDA_1866
333S0717	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,HUMA,96FBGA	U4000	CRITICAL	4G_HYNIX_H_1866
333S0720	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,REV E,96FBGA	U4000	CRITICAL	4G-MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G-ELPIDA	4G-ELPIDA, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L, PPDDR:1V35
RAM_4G-HYNIX_H	4G-HYNIX_H, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H, PPDDR:1V35
RAM_4G-MICRON	4G-MICRON, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L, PPDDR:1V35
RAM_4G-ELPIDA_1866	4G-ELPIDA_1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L, PPDDR:1V5
RAM_4G-HYNIX_H_1866	4G-HYNIX_H_1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H, PPDDR:1V5
RAM_4G-MICRON_1866	4G-MICRON_1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L, PPDDR:1V5

NOTE: 1866 PARTS BEING STRAPPED TO RUN AT 1600

13" MBP VARIABLE BOM GROUPS

BOM GROUP	BOM OPTIONS
J44_COMMON4	SMCBOARDID:8

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	1C,SDRAM,4GBIT,DDR3L-1600,HUMA,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:HYNIX_H
333S0704	1	1C,SDRAM,4GBIT,DDR3L-1600,DIE P,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:ELPIDA
333S0698	1	1C,SDRAM,4GBIT,DDR3L-1600,REV E,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:MICRON

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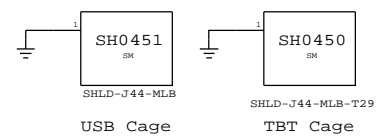
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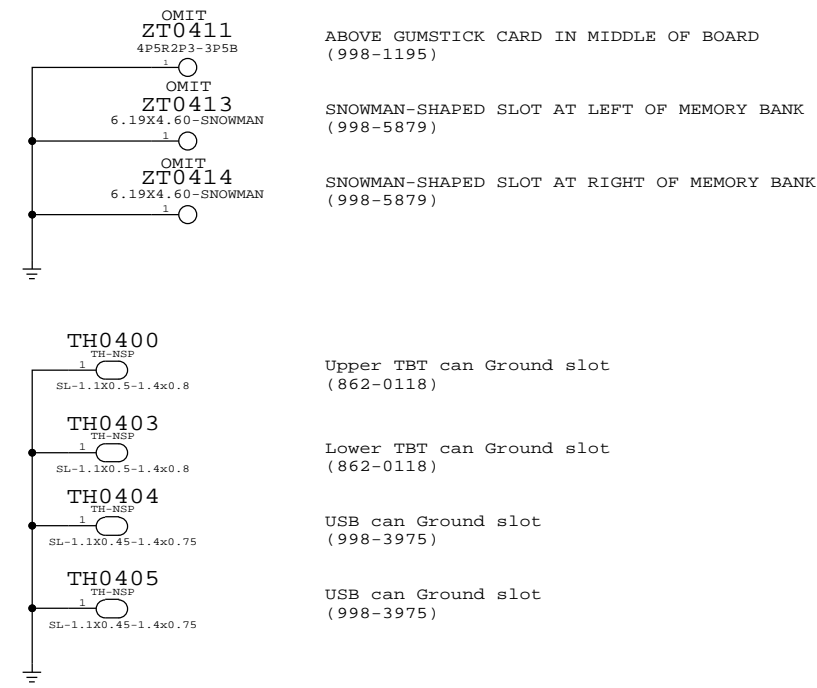
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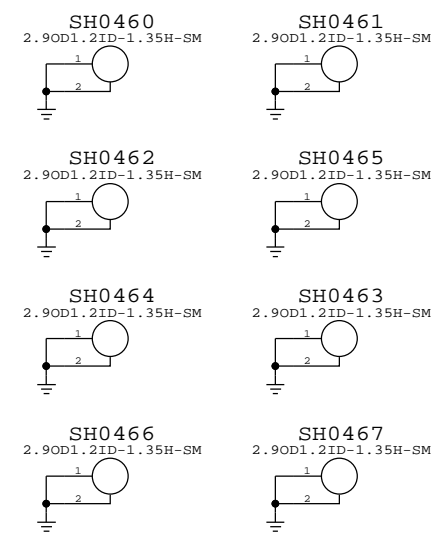
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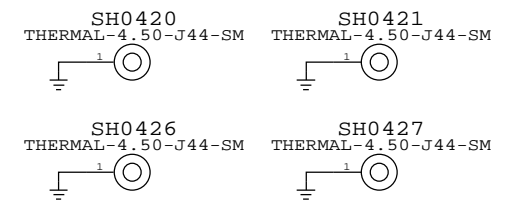
Mounting Holes & Slots



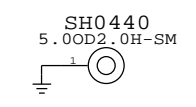
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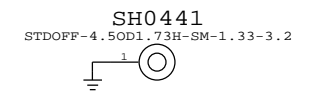
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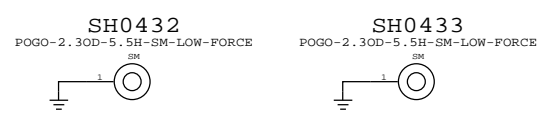
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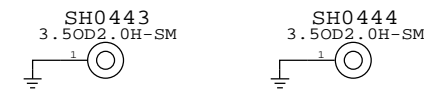
FAN STANDOFF (806-5376)



POGO PINS (870-2451)
SH0435 & SH0436 removed.



RIO FLEX BRACKET BOSSES (860-2354)



D
C
B
A

D
C
B
A

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PD Parts			
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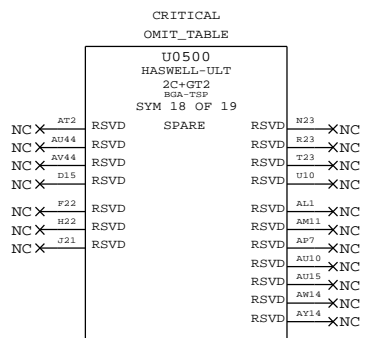
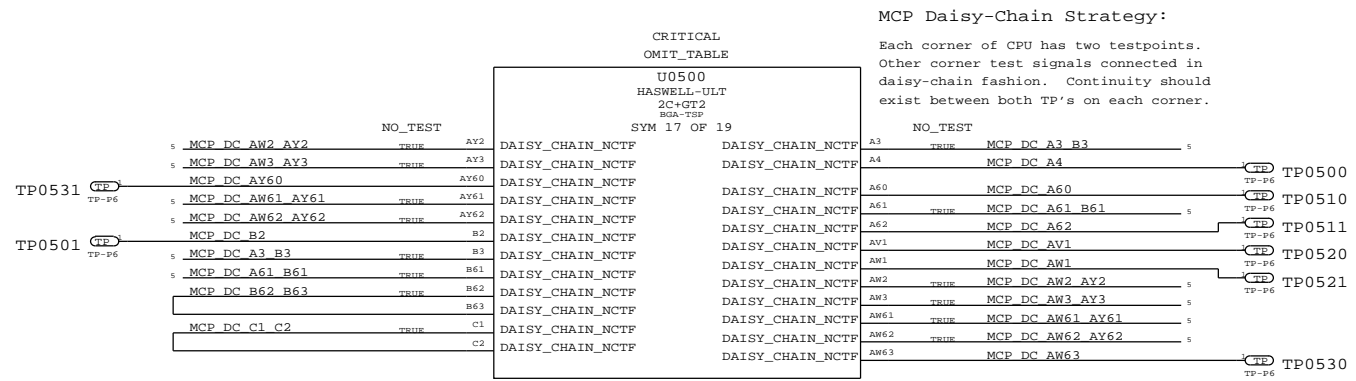
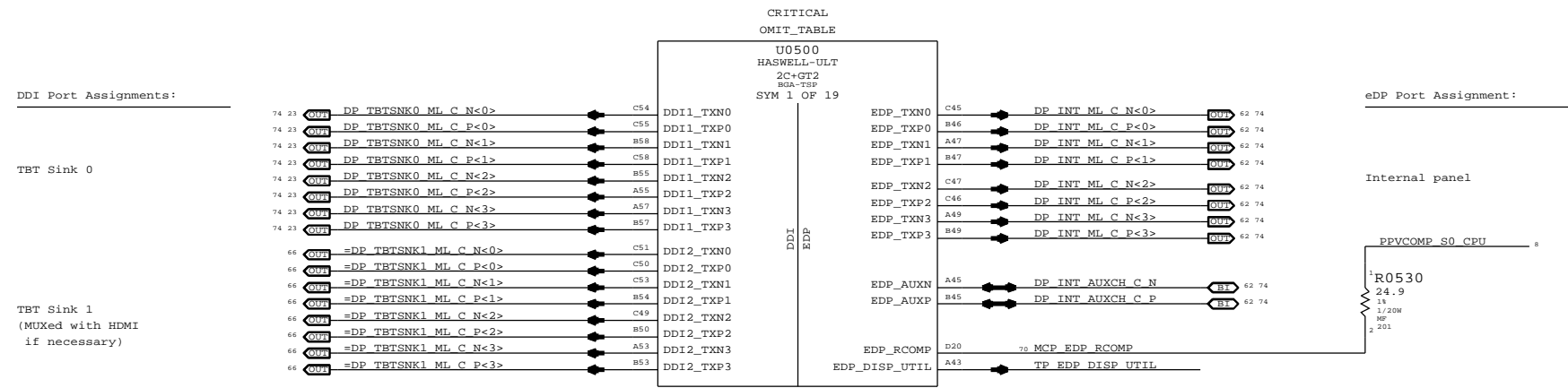
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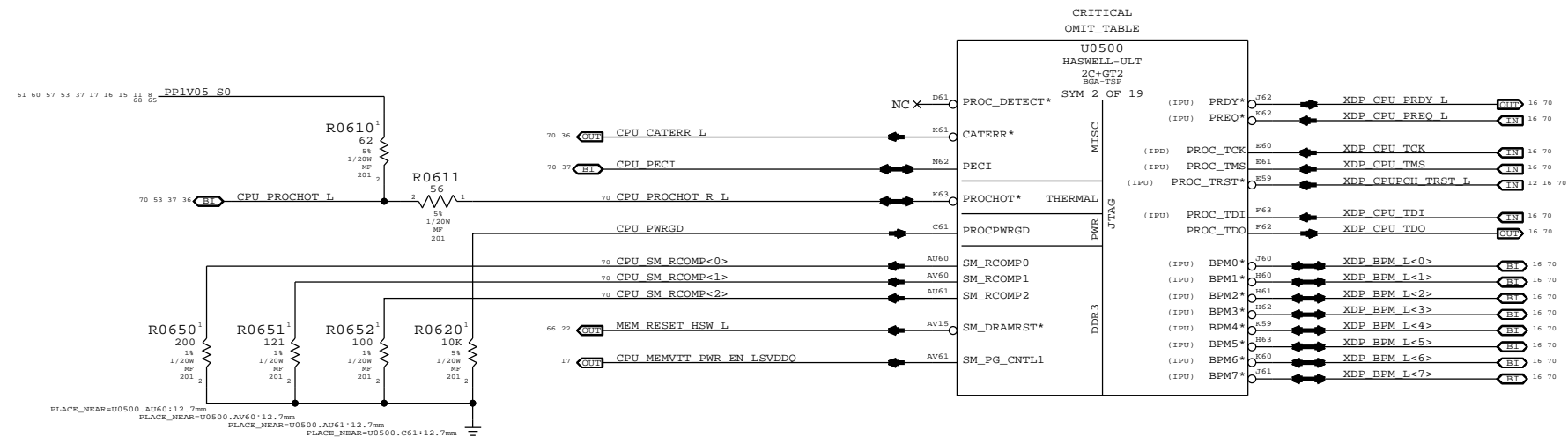
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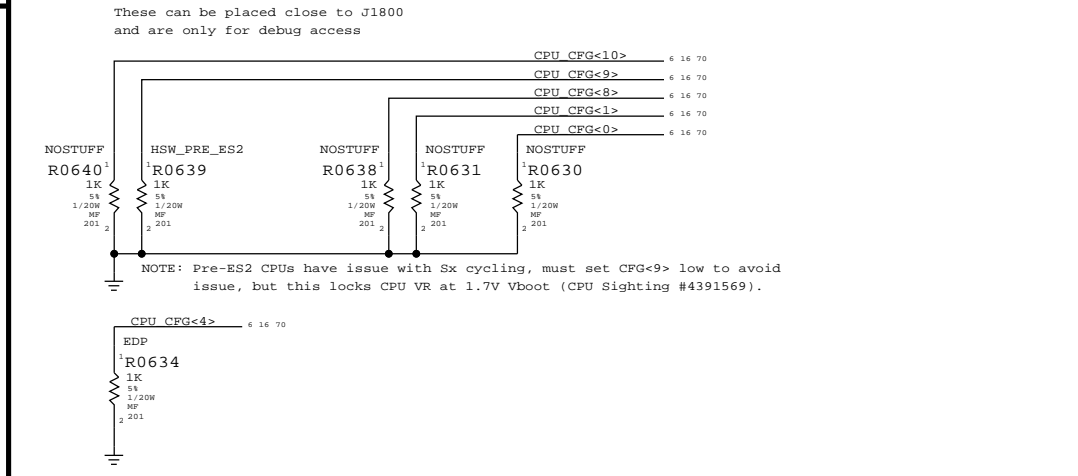
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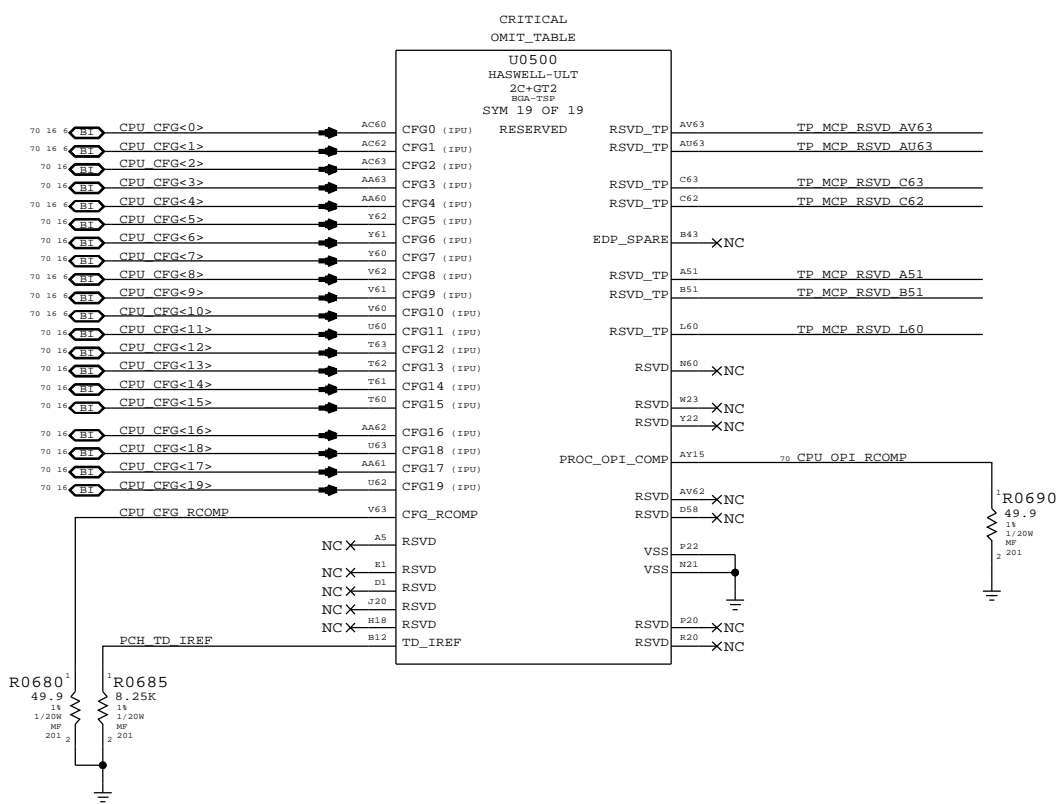
B

CFG<10>:SAFE MODE BOOT 1 = NORMAL OPERATION 0 = POWER FEATURES NOT ACTIVE
 CFG<9> :NO SVID-CAPABLE VR 1 = VR SUPPORTS SVID 0 = VR DOES NOT SUPPORT SVID
 CFG<8> :ALLOW NOA ON LOCKED UNITS 1 = NORMAL OPERATION 0 = NOA ALWAYS UNLOCKED
 CFG<4> :EDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
 CFG<1> :PCH-LESS MODE 1 = NORMAL OPERATION 0 = PCH-LESS MODE
 CFG<0> :RESET SEQUENCE STALL 1 = NORMAL OPERATION 0 = STALL AFTER PCU PLL LOCK

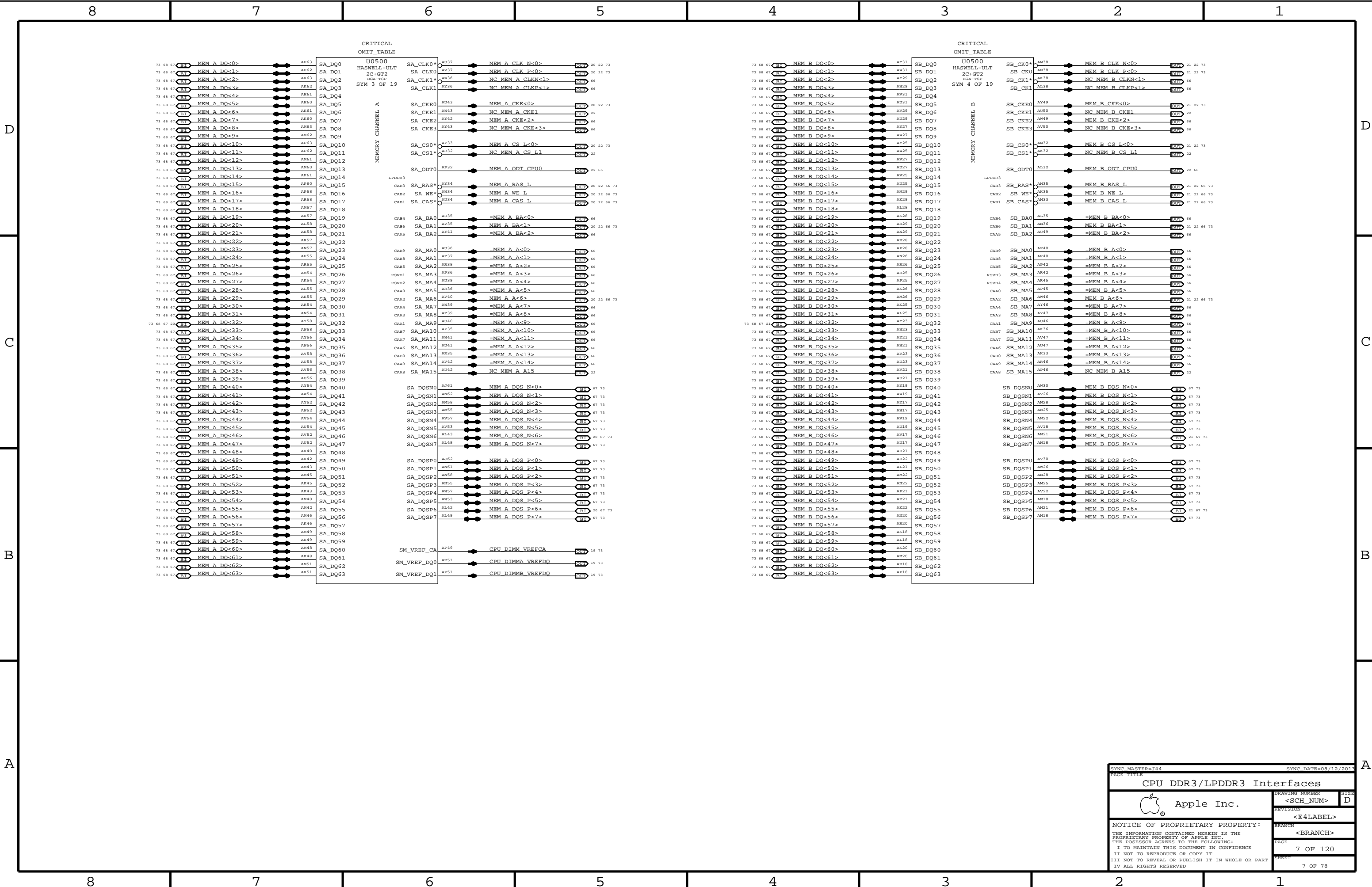


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PAGE TITLE			
CPU DDR3/LPDDR3 Interfaces			
DRAWING NUMBER		SIZE	
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SHEET		7 OF 78	

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
 LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
 Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

D

C

B

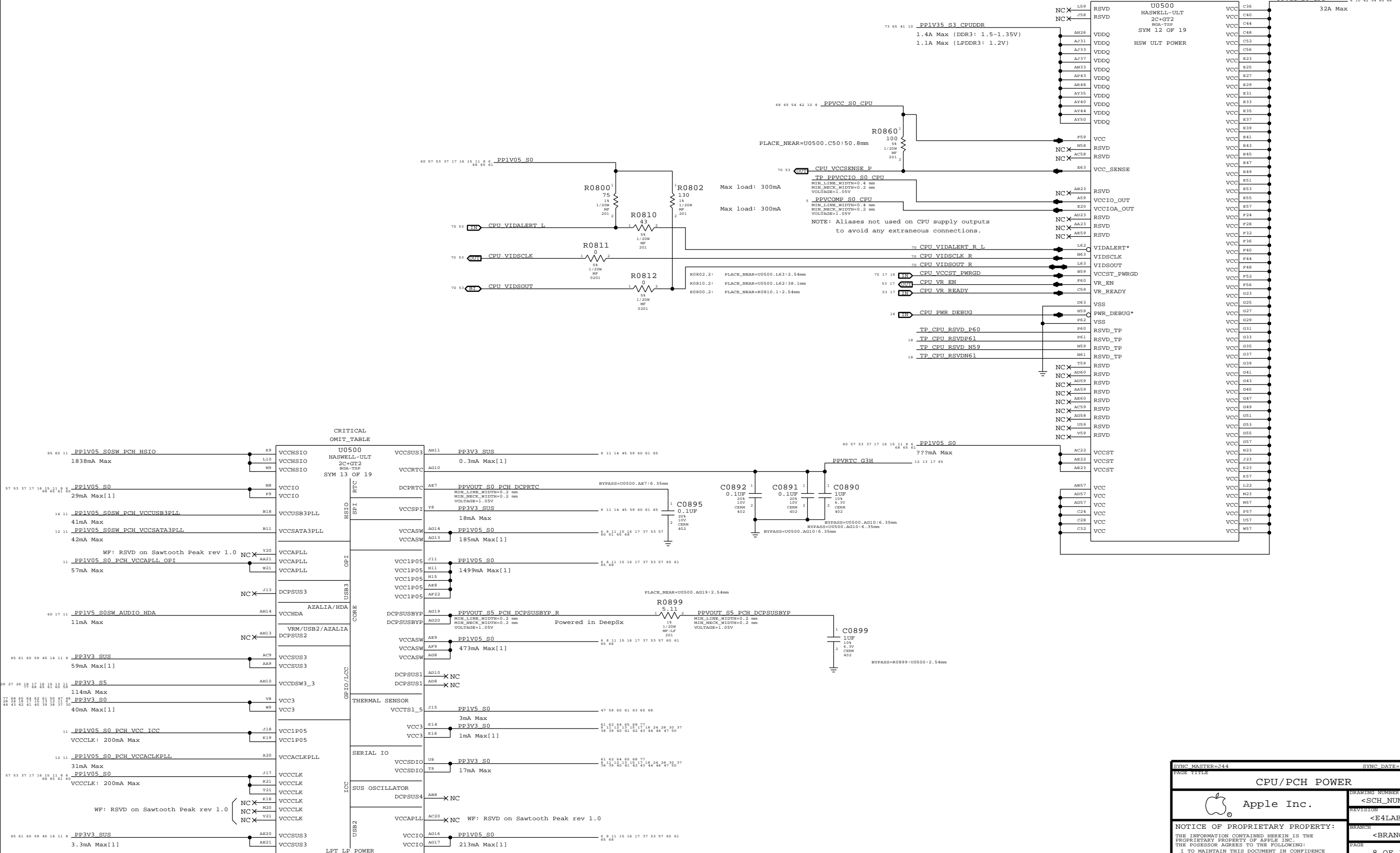
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A



CRITICAL OMIT_TABLE

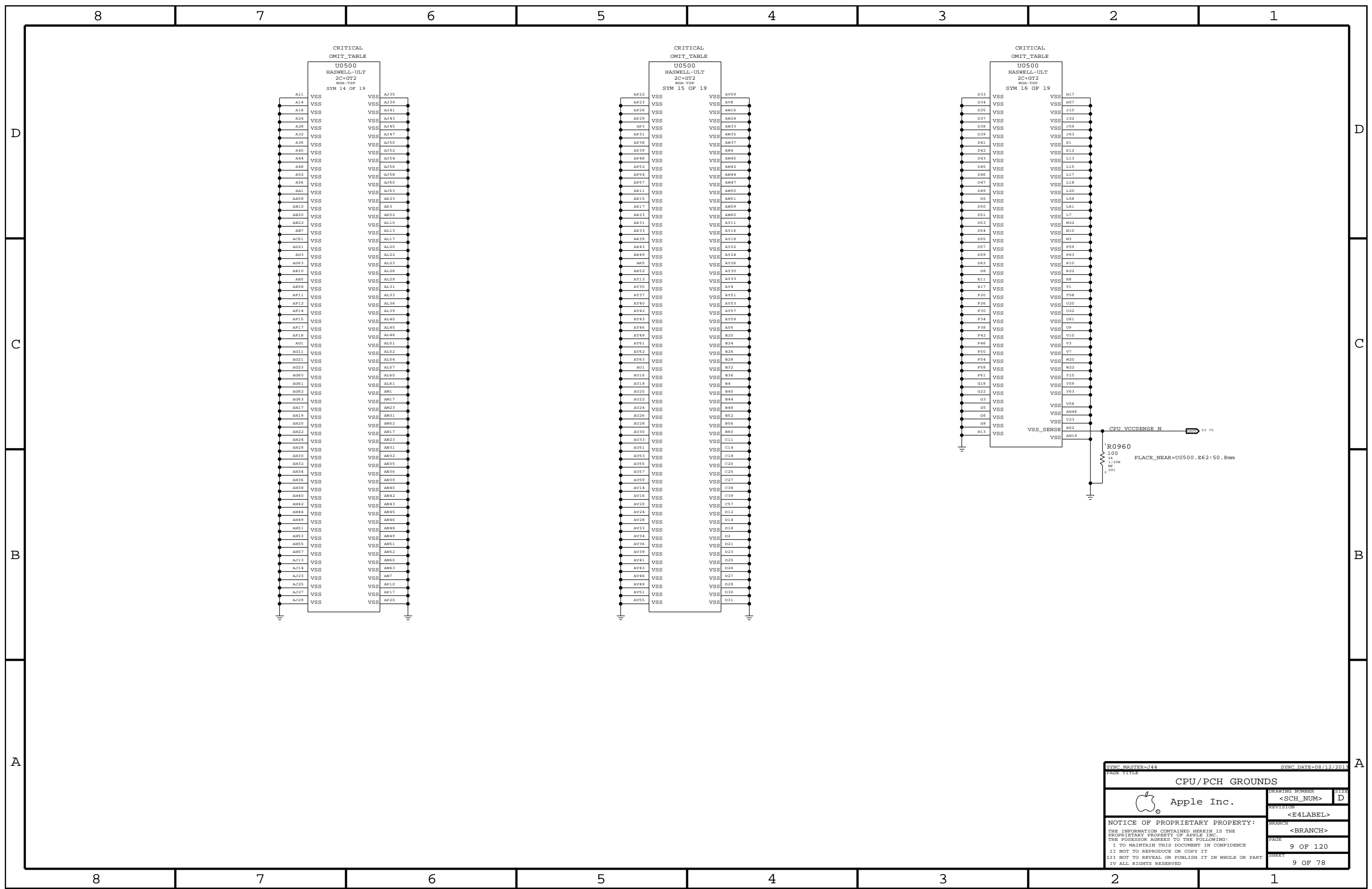
Signal	Current	Notes
PP1V05_S0SW_PCH_HSIO	1838mA Max	
PP1V05_S0	29mA Max[1]	
PP1V05_S0SW_PCH_VCCUSB3PLL	41mA Max	
PP1V05_S0SW_PCH_VCCSATA3PLL	42mA Max	
PP1V05_S0_PCH_VCCAPLL_OPI	57mA Max	WF: RSVD on Sawtooth Peak rev 1.0
PP1V5_S0SW_AUDIO_HDA	11mA Max	
PP3V3_S0	59mA Max[1]	
PP3V3_S5	114mA Max	
PP3V3_S0	40mA Max[1]	
PP1V05_S0_PCH_VCC_ICC	VCCCLK: 200mA Max	
PP1V05_S0_PCH_VCCACKPLL	31mA Max	
PP1V05_S0	VCCCLK: 200mA Max	
PP3V3_S0	3.3mA Max[1]	

CRITICAL OMIT_TABLE

Signal	Current	Notes
VCC36		
VCC40		
VCC44		
VCC48		
VCC52		
VCC56		
VCC60		
VCC64		
VCC68		
VCC72		
VCC76		
VCC80		
VCC84		
VCC88		
VCC92		
VCC96		
VCC100		
VCC104		
VCC108		
VCC112		
VCC116		
VCC120		
VCC124		
VCC128		
VCC132		
VCC136		
VCC140		
VCC144		
VCC148		
VCC152		
VCC156		
VCC160		
VCC164		
VCC168		
VCC172		
VCC176		
VCC180		
VCC184		
VCC188		
VCC192		
VCC196		
VCC200		
VCC204		
VCC208		
VCC212		
VCC216		
VCC220		
VCC224		
VCC228		
VCC232		
VCC236		
VCC240		
VCC244		
VCC248		
VCC252		
VCC256		
VCC260		
VCC264		
VCC268		
VCC272		
VCC276		
VCC280		
VCC284		
VCC288		
VCC292		
VCC296		
VCC300		
VCC304		
VCC308		
VCC312		
VCC316		
VCC320		
VCC324		
VCC328		
VCC332		
VCC336		
VCC340		
VCC344		
VCC348		
VCC352		
VCC356		
VCC360		
VCC364		
VCC368		
VCC372		
VCC376		
VCC380		
VCC384		
VCC388		
VCC392		
VCC396		
VCC400		
VCC404		
VCC408		
VCC412		
VCC416		
VCC420		
VCC424		
VCC428		
VCC432		
VCC436		
VCC440		
VCC444		
VCC448		
VCC452		
VCC456		
VCC460		
VCC464		
VCC468		
VCC472		
VCC476		
VCC480		
VCC484		
VCC488		
VCC492		
VCC496		
VCC500		
VCC504		
VCC508		
VCC512		
VCC516		
VCC520		
VCC524		
VCC528		
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VCC564		
VCC568		
VCC572		
VCC576		
VCC580		
VCC584		
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VCC620		
VCC624		
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VCC680		
VCC684		
VCC688		
VCC692		
VCC696		
VCC700		
VCC704		
VCC708		
VCC712		
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VCC724		
VCC728		
VCC732		
VCC736		
VCC740		
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VCC884		
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VCC908		
VCC912		
VCC916		
VCC920		
VCC924		
VCC928		
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VCC936		
VCC940		
VCC944		
VCC948		
VCC952		
VCC956		
VCC960		
VCC964		
VCC968		
VCC972		
VCC976		
VCC980		
VCC984		
VCC988		
VCC992		
VCC996		
VCC1000		

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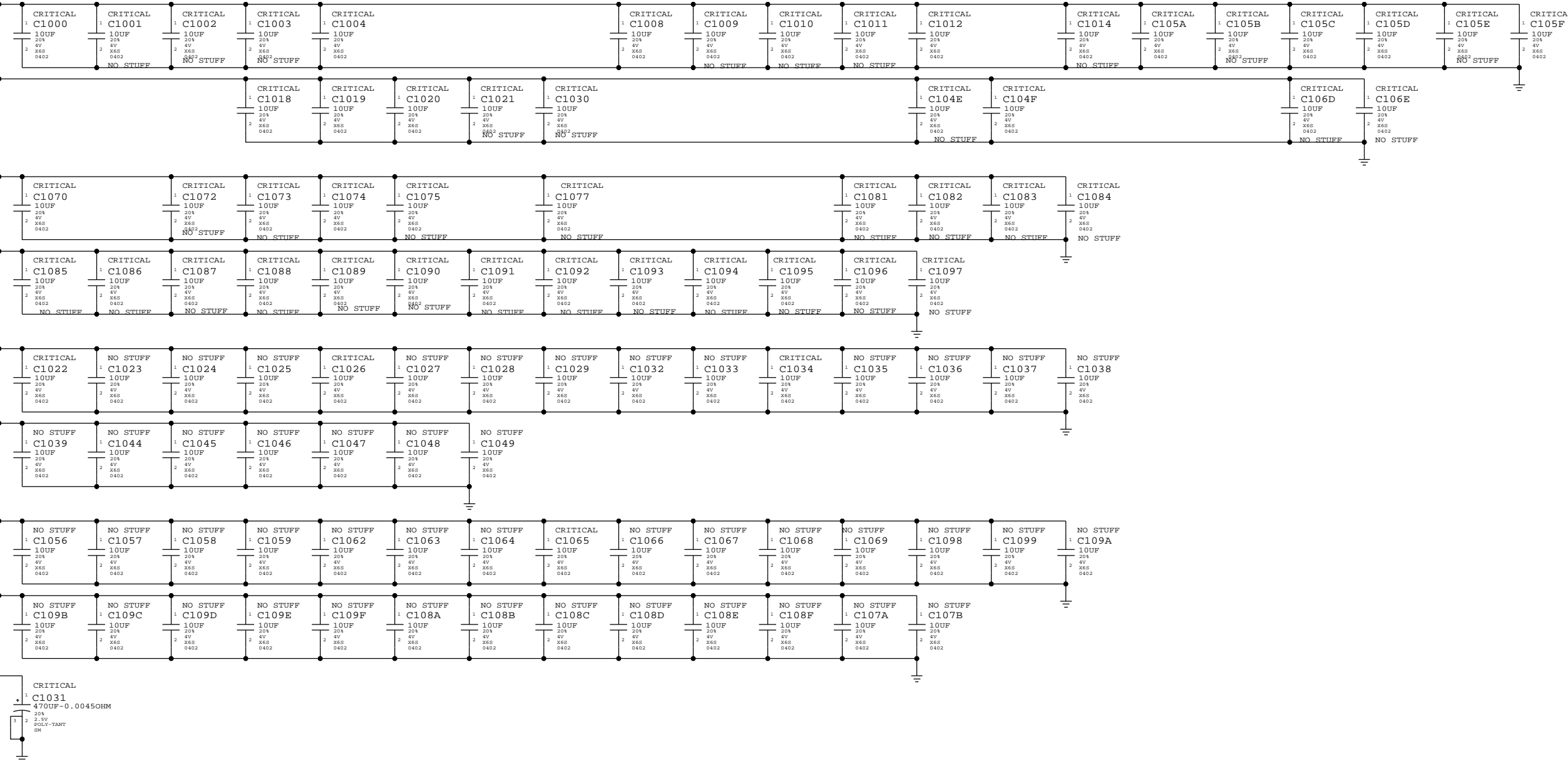


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CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
 Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

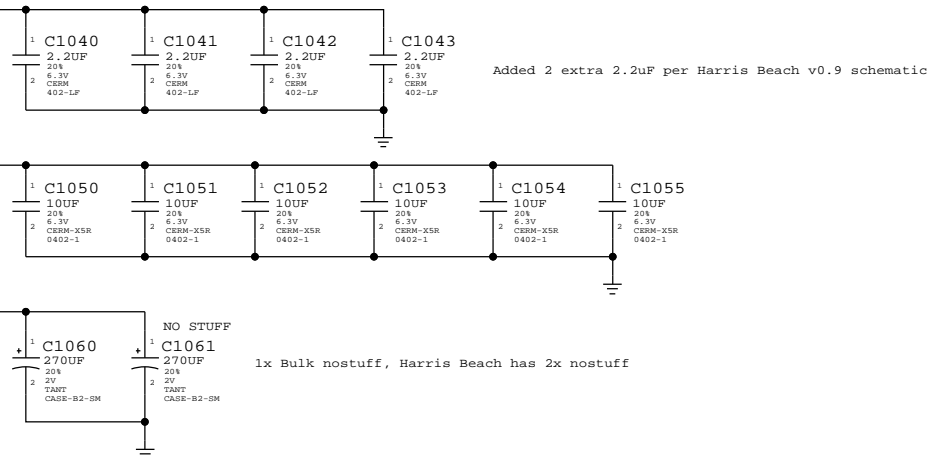
68 65 54 42 8_PPVCC_S0_CPU



CPU VDDQ DECOUPLING

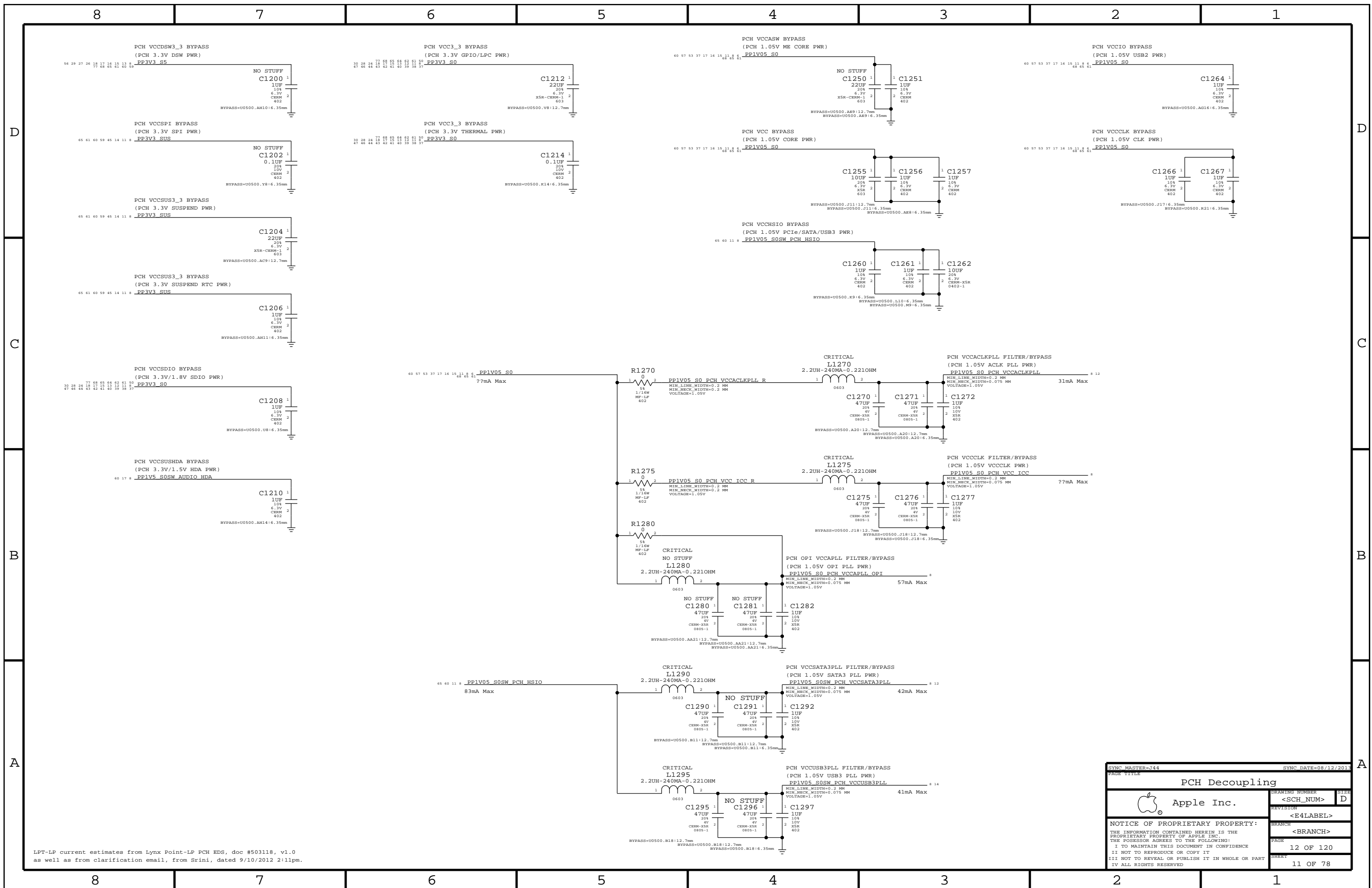
Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
 Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

73 65 41 8_PP1V35_S3_CPUDDR



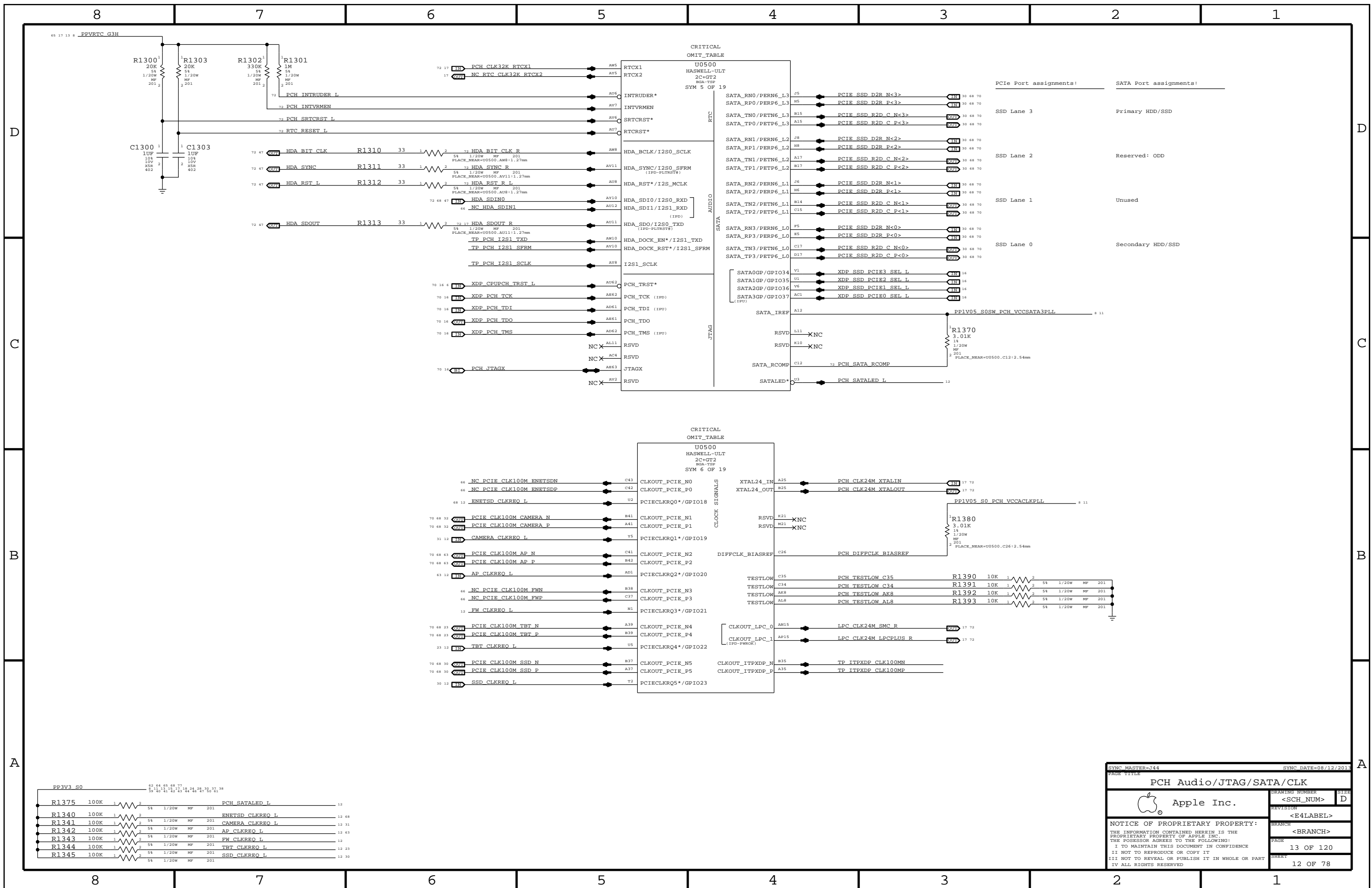
CPU VCC Decoupling

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CPU Decoupling			
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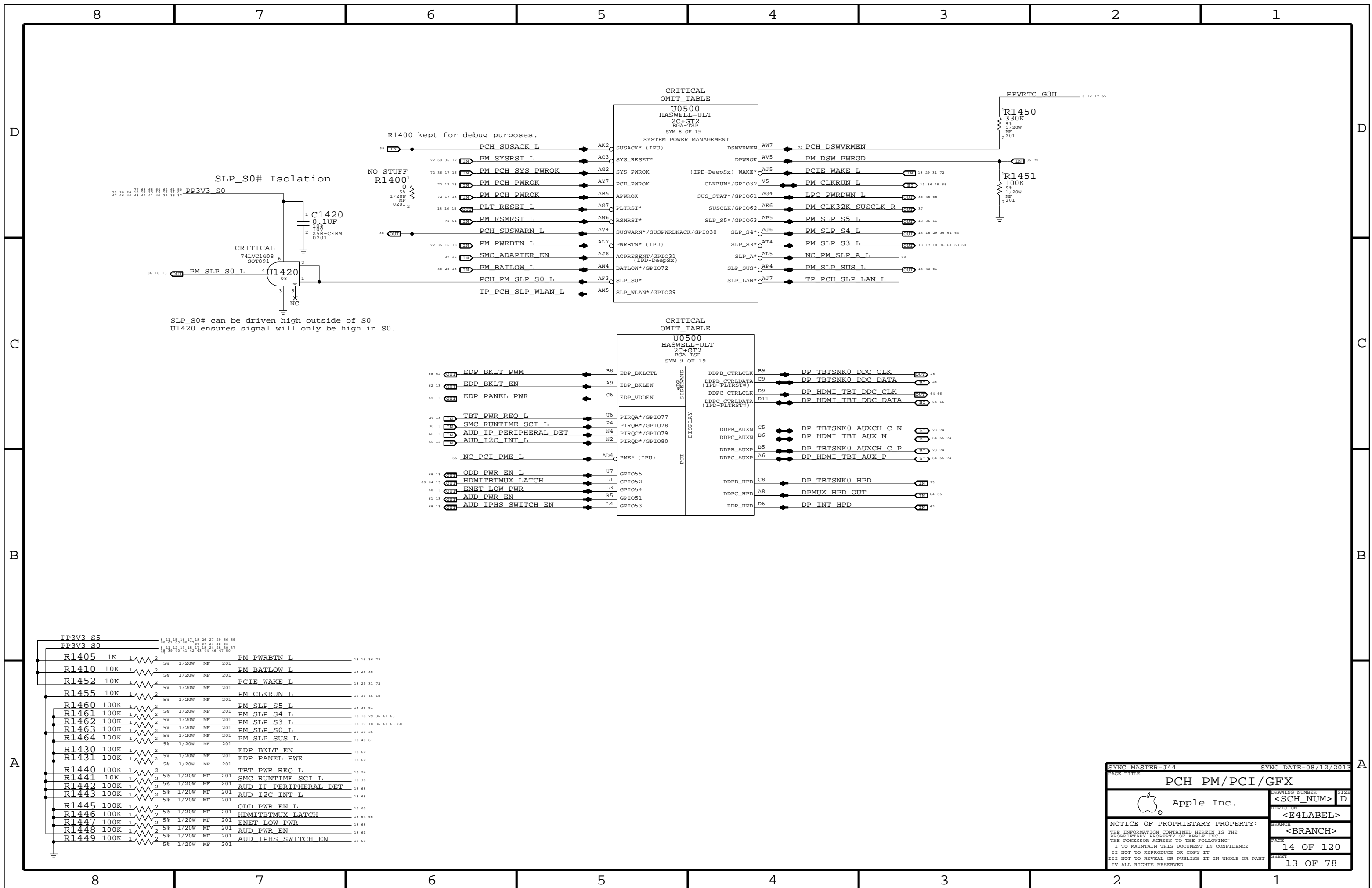


LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

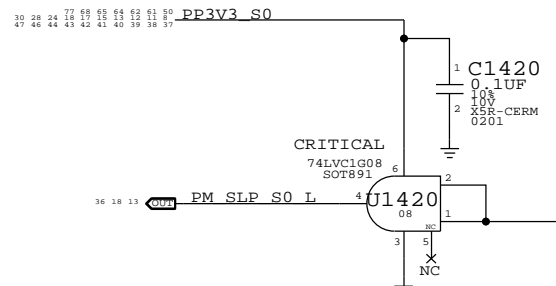
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Apple Inc.		<SCH_NUM>	D
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SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
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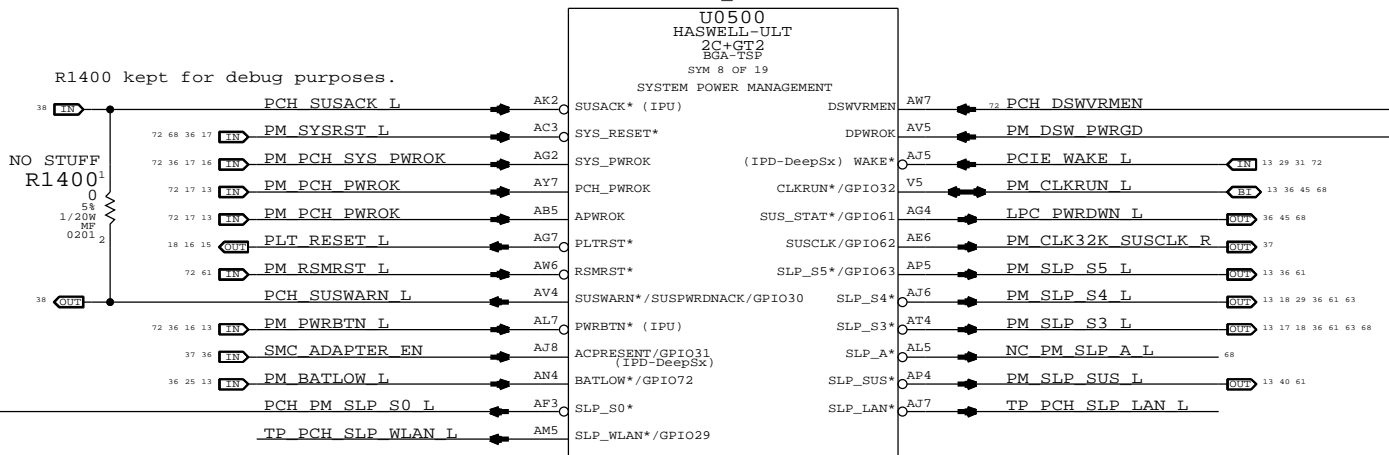


SLP_S0# Isolation

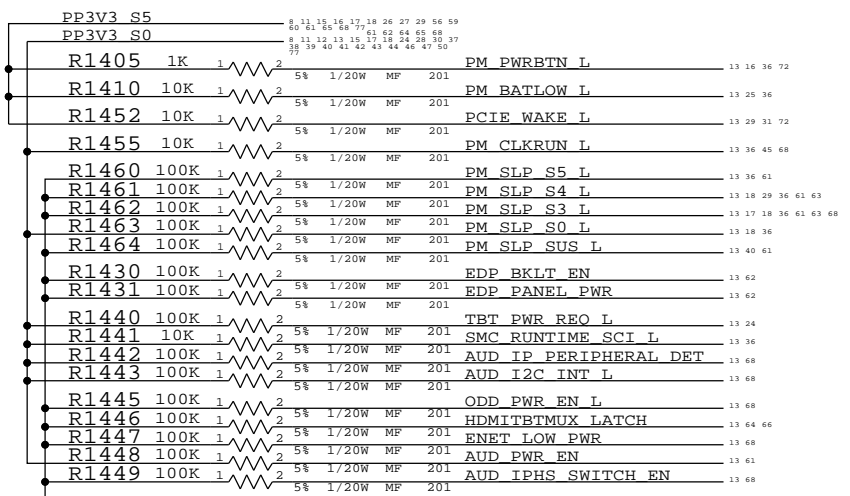
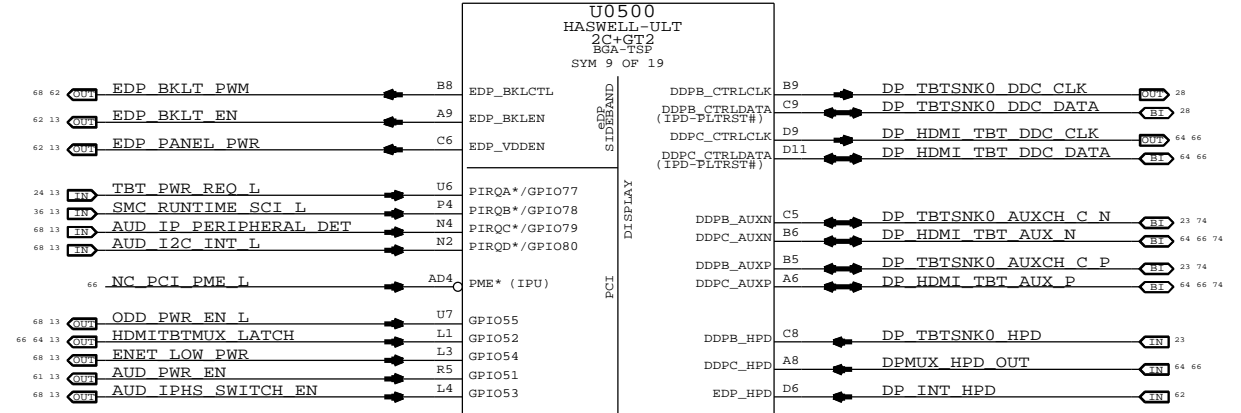


SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.

CRITICAL OMIT_TABLE



CRITICAL OMIT_TABLE



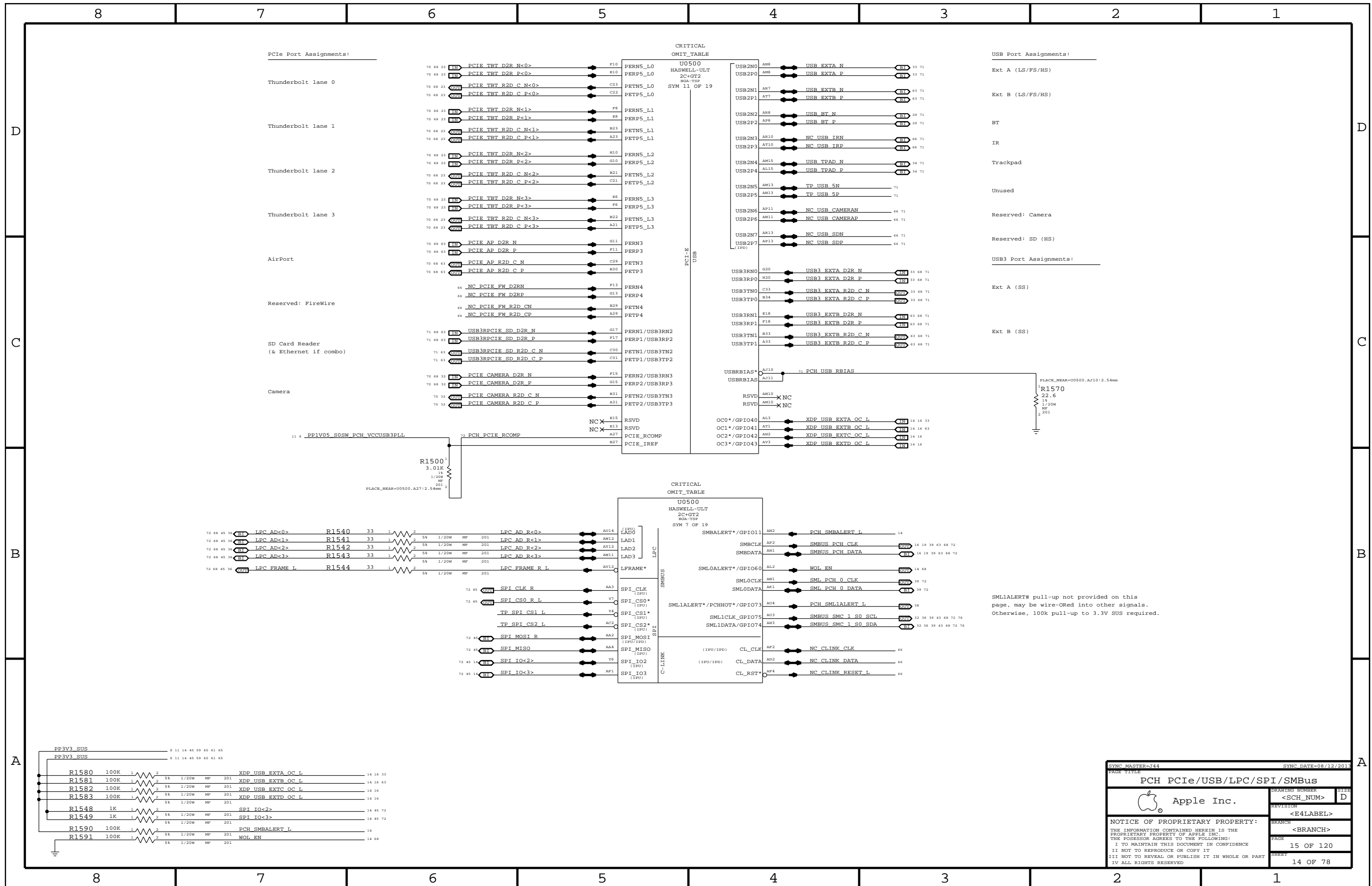
SYNC_MASTER=J44 SYNC_DATE=08/12/2013

PCH PM/PCI/GFX

Apple Inc.

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PCH PCIe/USB/LPC/SPI/SMBus			
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H



Pull-up/down on chipset support page (depends on TBT controller)
 Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
 Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

Pull-up on TBT page
 Requires connection to SMC via 1K series R

R1616 should also be stuffed if platform does not use SD card

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PCH GPIO/MISC/LPIO			
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Extra BPM Testpoints

- 70 6 XDP BPM L<2> TP1802
- 70 6 XDP BPM L<3> TP1803
- 70 6 XDP BPM L<4> TP1804
- 70 6 XDP BPM L<5> TP1805
- 70 6 XDP BPM L<6> TP1806
- 70 6 XDP BPM L<7> TP1807

Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

- 70 16 XDP CPU TDO R1810 51 1 XDP
 - 70 16 XDP CPU TCK R1813 51 2 XDP
- TDI and TMS are terminated in CPU.

D

D

C

C

B

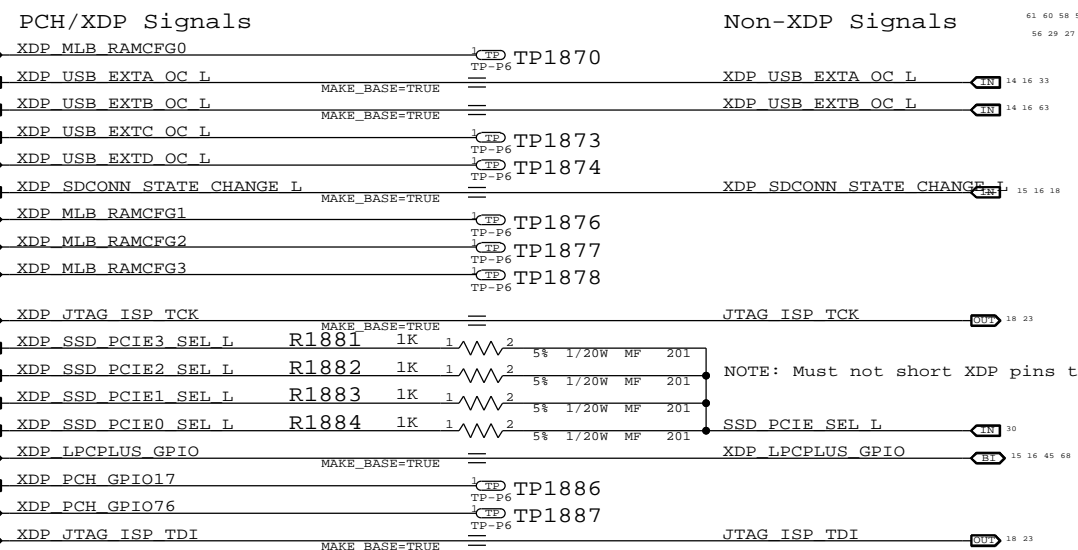
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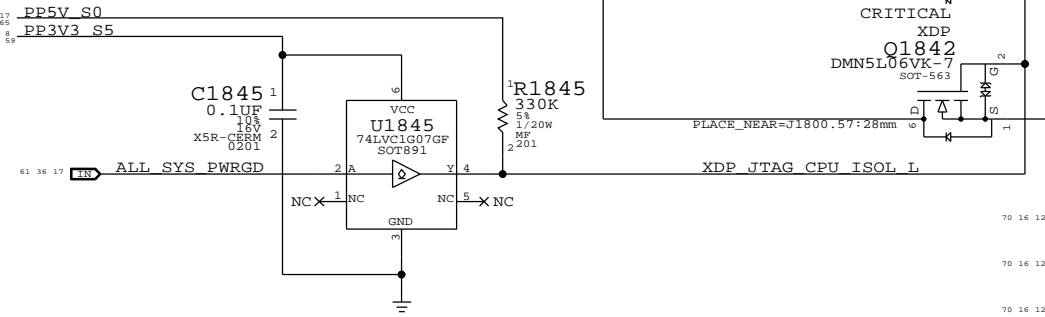
PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.



Unused & MLB_RAMCFGx GPIOs have TPs.
 USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
 SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
 JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
 NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
 SSD_PCIEx_SEL_L straps are connected via 1K to common net.
 LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation



- 70 16 PCH JTAGX R1899 1K 2 NO STUFF
- 70 16 XDP PCH TDO R1890 51 2 XDP
- 70 16 XDP PCH TDI R1891 51 2 XDP
- 70 16 XDP PCH TMS R1892 51 2 XDP
- 70 16 XDP PCH TCK R1896 51 2 NO STUFF
- 70 16 XDP CPUPCH TRST R1897 51 2 NO STUFF

SYNC MASTER=J44		SYNC DATE=08/12/2013	
CPU/PCH Merged XDP			
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		PAGE	18 OF 120
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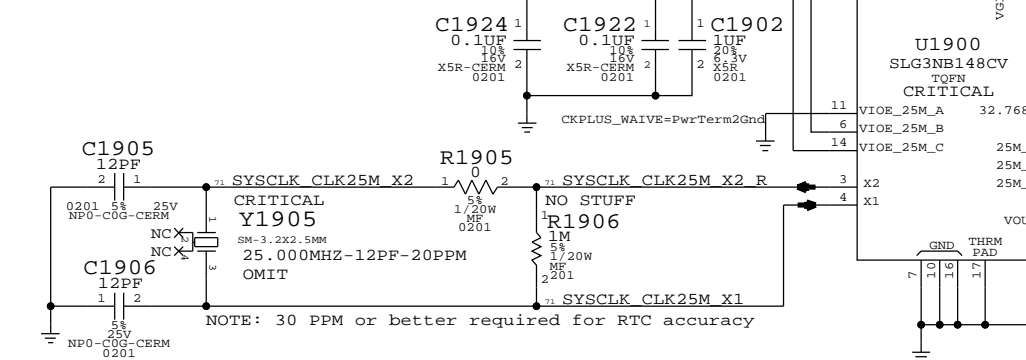
System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

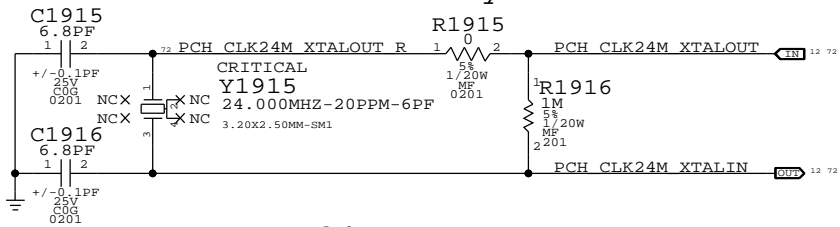
GreenCLK 25MHz Power Must be powered if any VDDIO is powered.

CAM XTAL Power
TBT XTAL Power

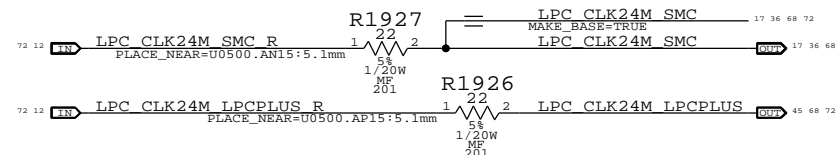


NOTE: 30 PPM or better required for RTC accuracy

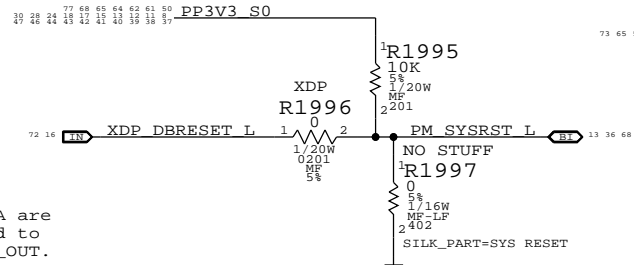
PCH 24MHz Crystal



PCH 24MHz Outputs



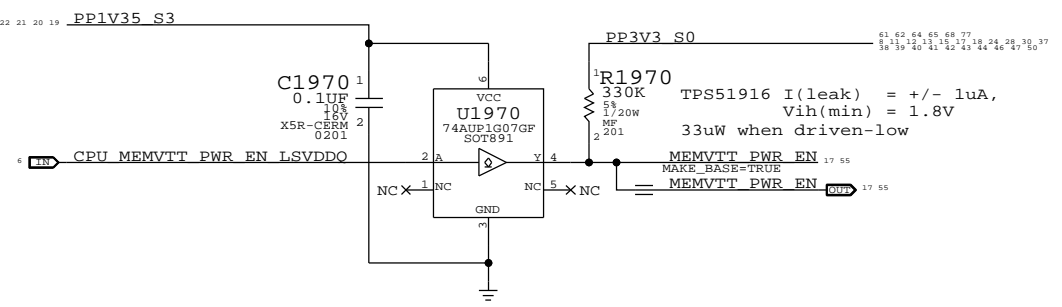
PCH Reset Button



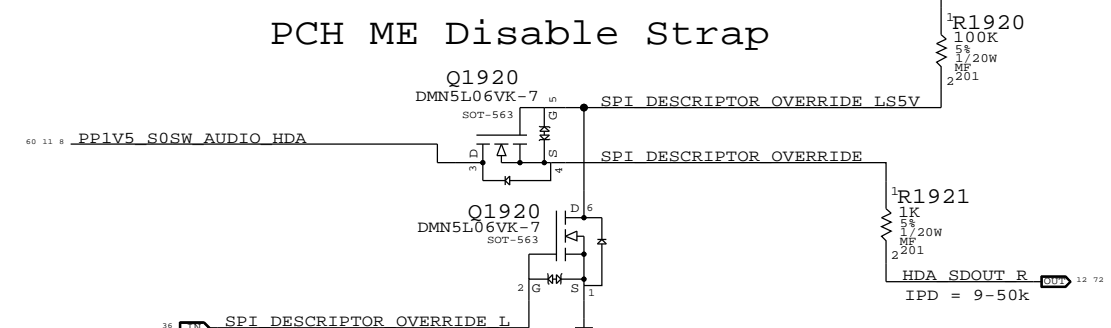
VBAT and +V3.3A are internally ORED to create VDD_RTC_OUT. +V3.3A should be first available ~3.3V power to reduce VBAT draw.

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

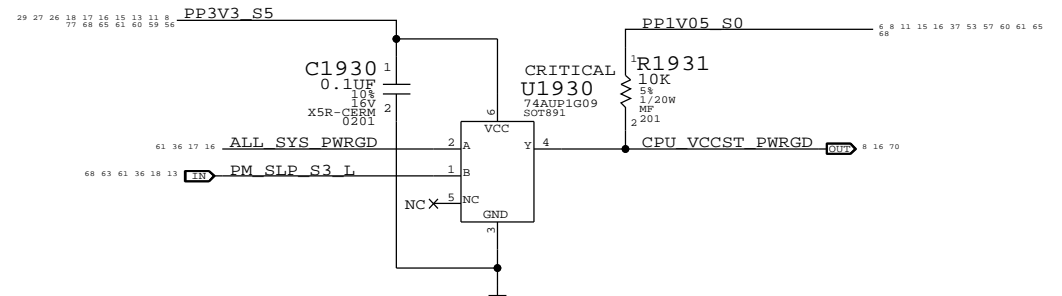


PCH ME Disable Strap

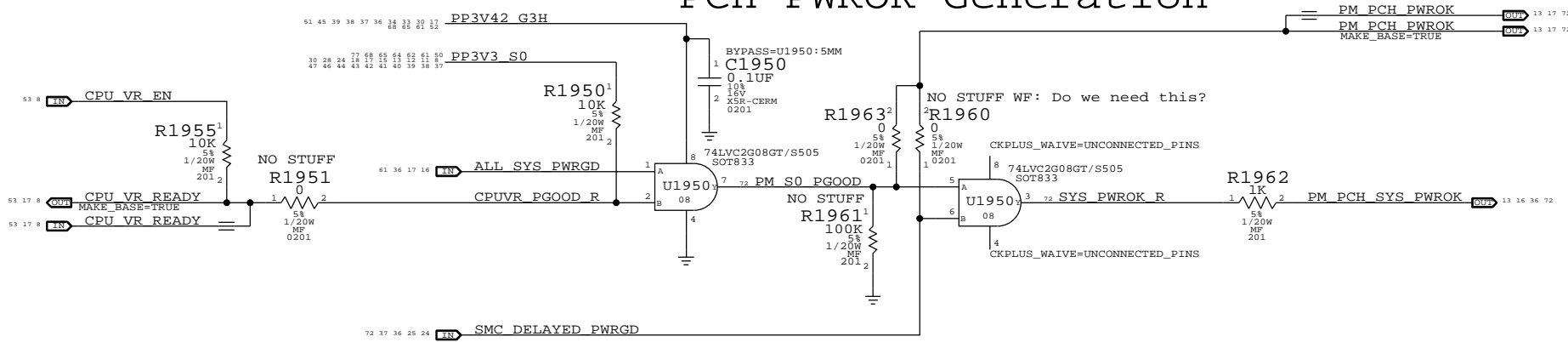


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD



PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL, 25MHZ, 20PPM, 12PF, 3.2X2.5X.6MM, 85C	Y1905		

SYNC MASTER=J44 SYNC DATE=08/12/2013

Chipset Support

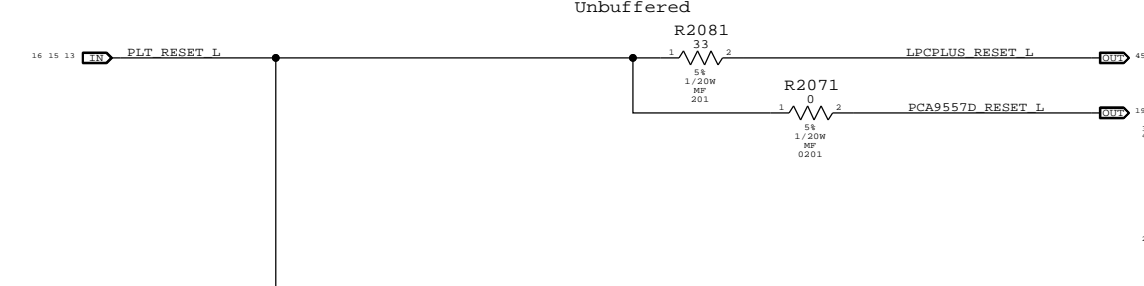
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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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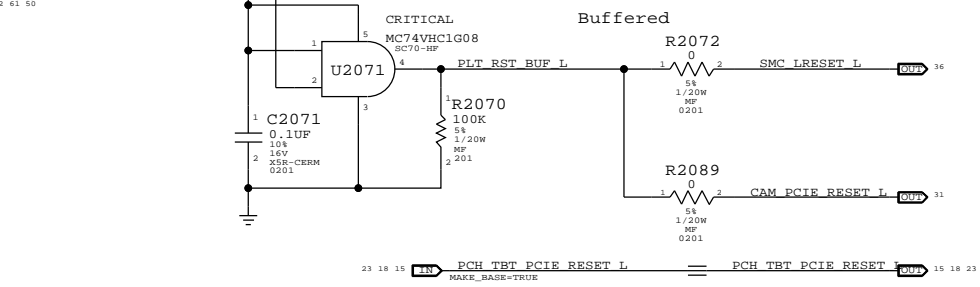
Platform Reset Connections

Unbuffered



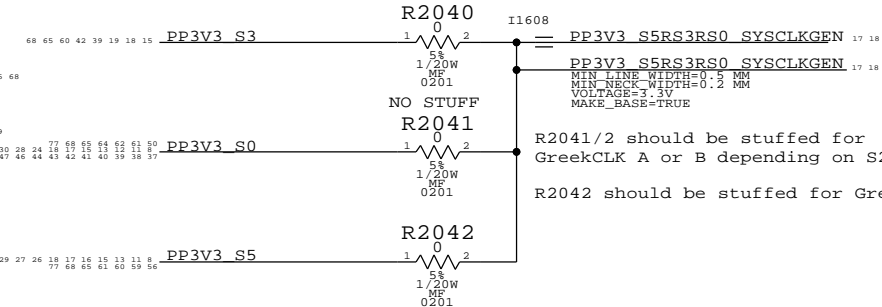
Scrub for Layout Optimization

Buffered



GreenCLK 25MHz Power

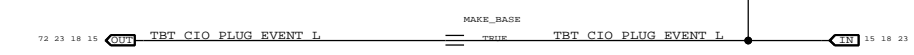
NO STUFF



R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail
R2042 should be stuffed for GreenCLK C

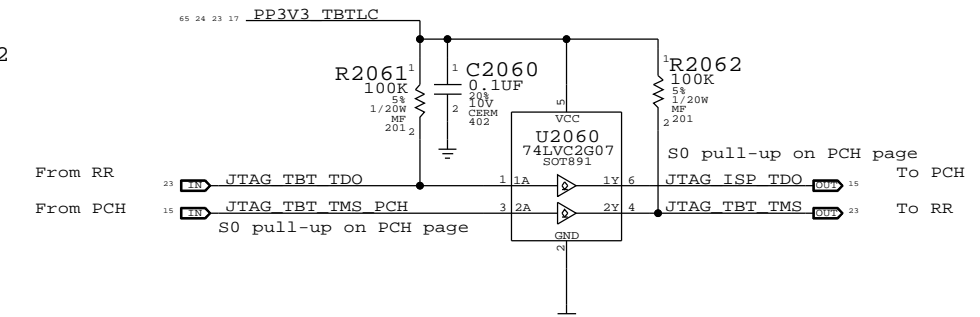
THUNDERBOLT PULL-UP

REDWOOD RIDGE PLUG_EVENT IS ACTIVE-LOW, ALWAYS DRIVEN (PULL-UP)



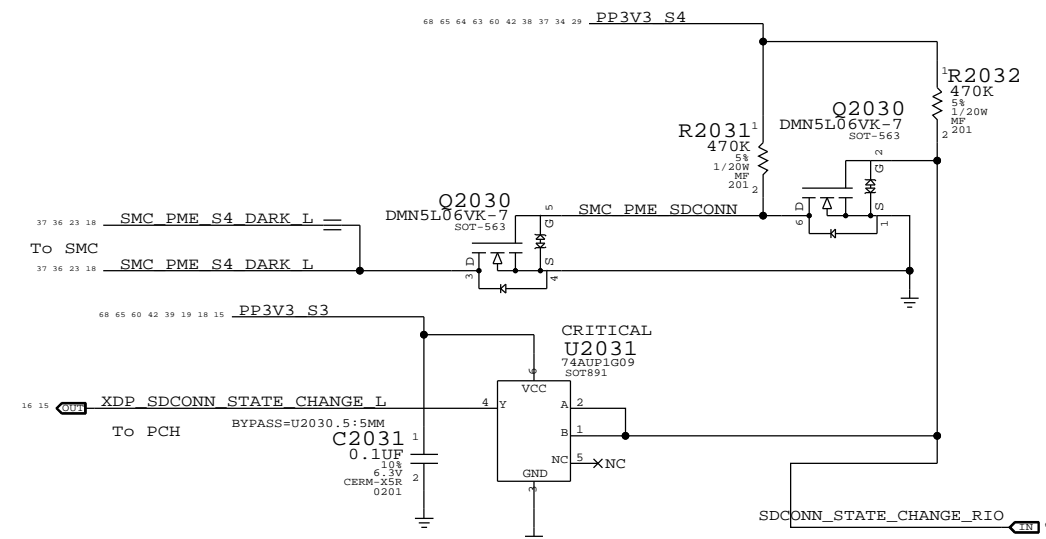
Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH



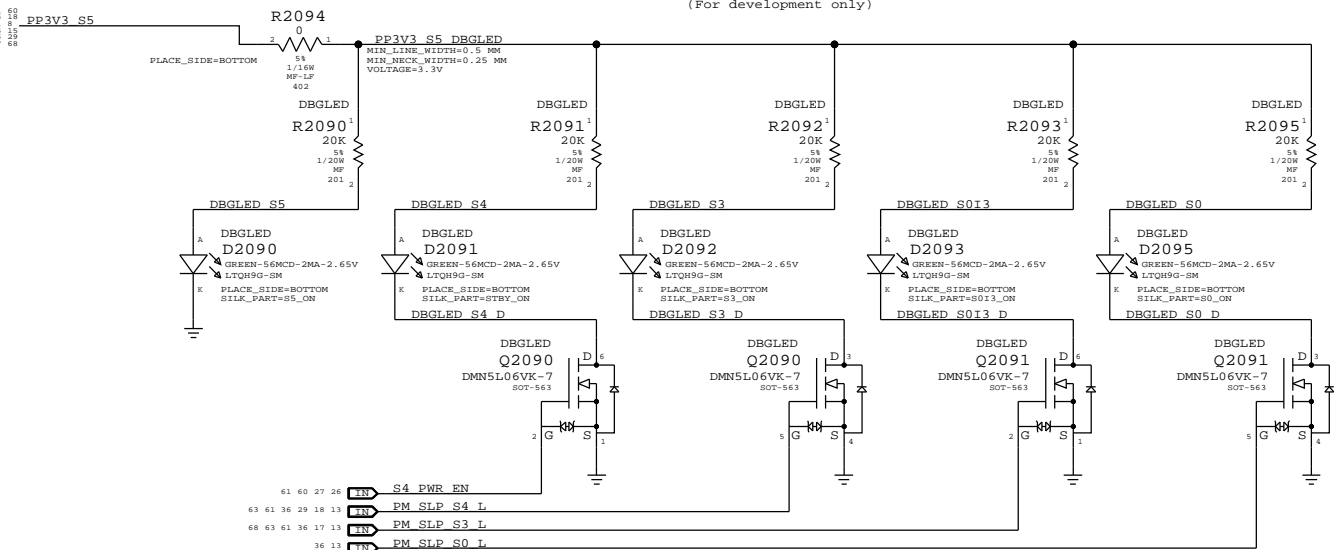
NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.
NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.

SDCONN_STATE_CHANGE Isolation

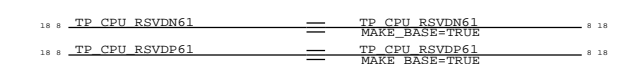


Power State Debug LEDs

(For development only)

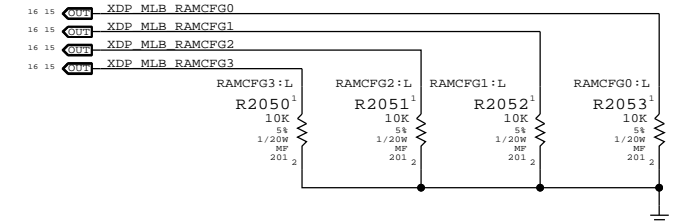


Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property



RAM Configuration Straps

Pull-downs for chip-down RAM systems



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
Project Chipset Support			
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		<E4LABEL>	
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Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

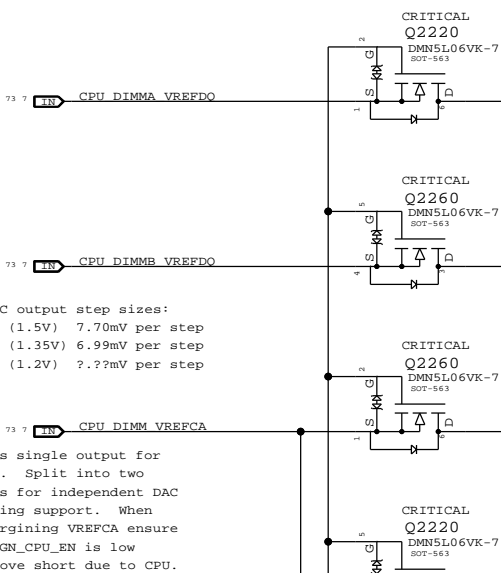
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining



NOTE: CPU DAC output step sizes:
 DDR3 (1.5V) 7.70mV per step
 DDR3L (1.35V) 6.99mV per step
 LPDDR3 (1.2V) 7.77mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT

R2218

PP3V3_S3

SHORT

PP3V3_S3_VREFMRGN_DAC

MIN_LINE_WIDTH=0.3 mm

MIN_NECK_WIDTH=0.2 mm

VOLTAGE=3.3V

DDR3L

DDR3

LPDDR3

MEMVREF

MEMVREF

MEMVREF

MEMVREF

MEMVREF

MEMVREF

MEMVREF

MEMVREF

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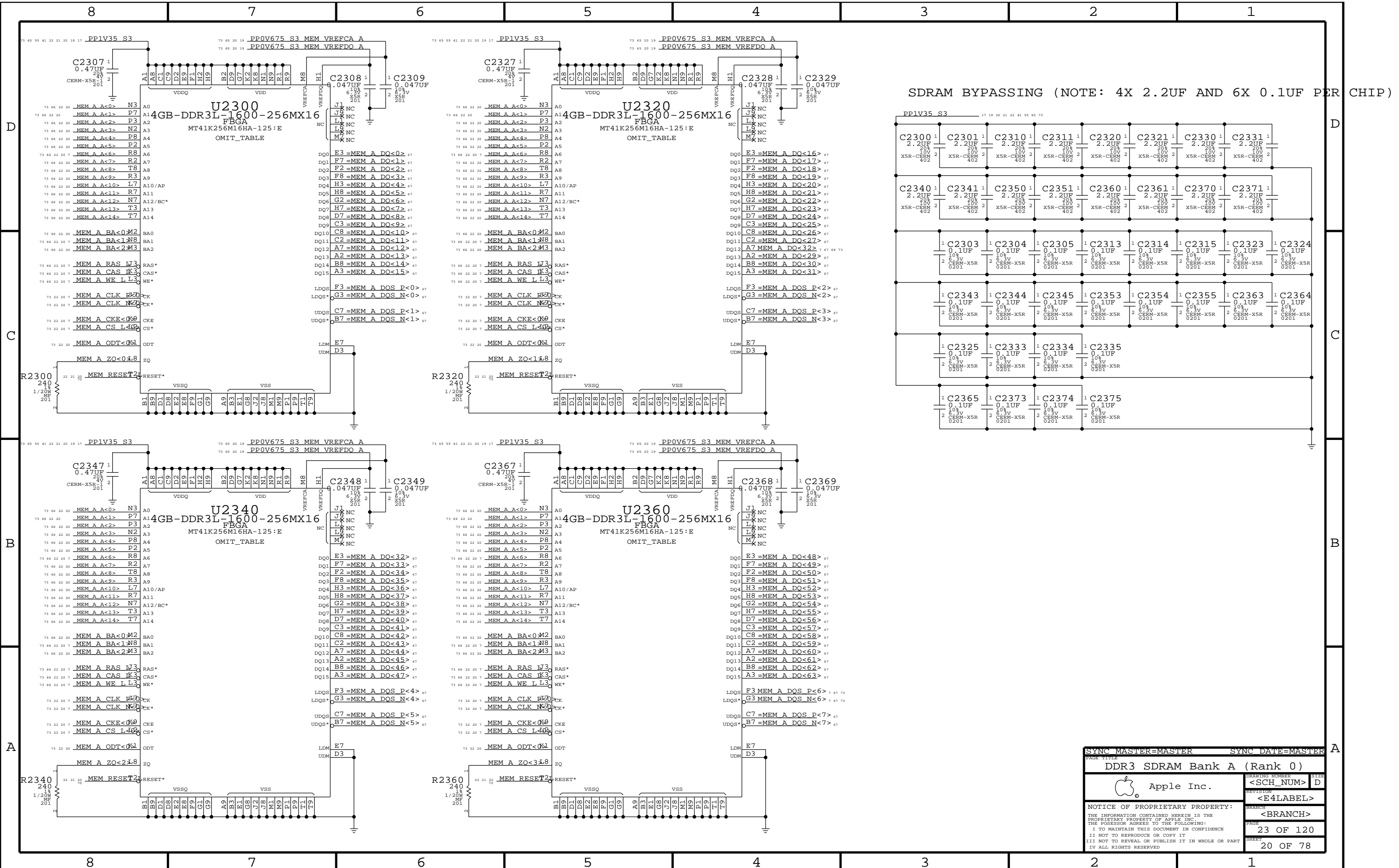
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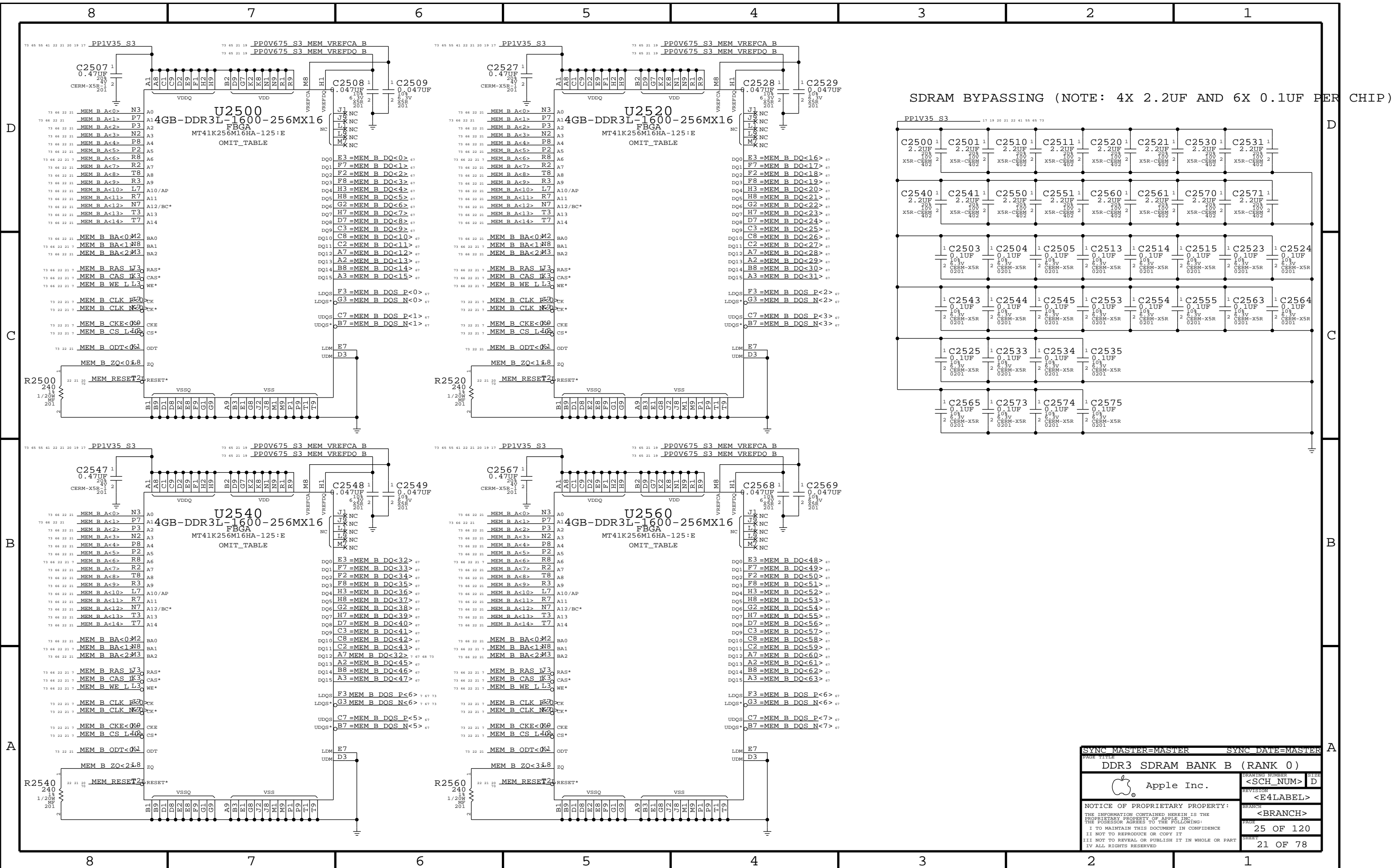
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MEMVREF



SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

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DDR3 SDRAM Bank A (Rank 0)			
DRAWING NUMBER		SIZE	
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REVISION		<E4LABEL>	
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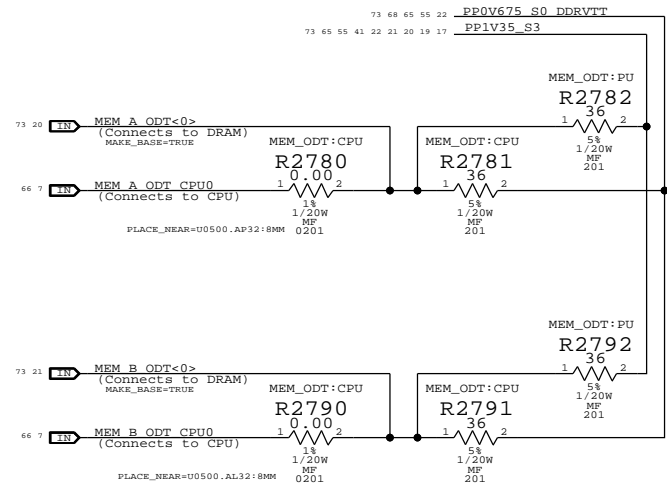


SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

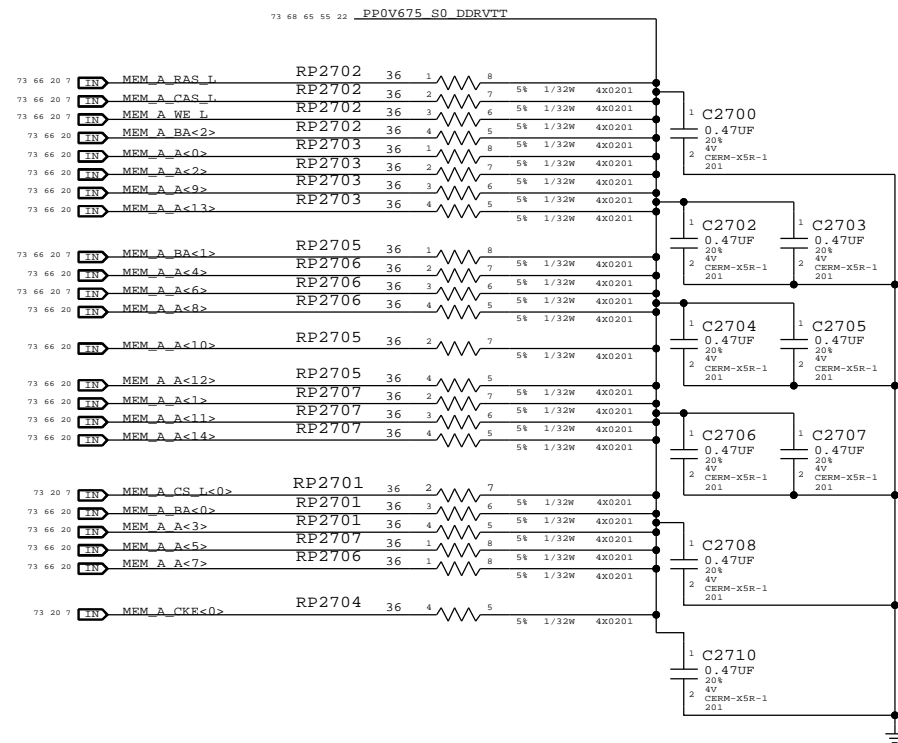
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DDR3 SDRAM BANK B (RANK 0)			
Apple Inc.		BRANCH NUMBER	SHEET
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Memory ODT Option

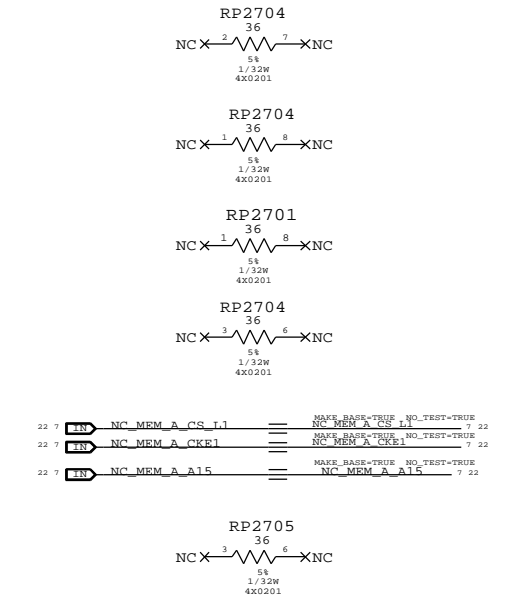
MEM_ODT:CPU drives ODT from CPU, terminated to 0.675V VTT.
MEM_ODT:PU disconnect ODT from CPU, ODT pins on DRAM pulled up to 1.35V VDDQ.



Memory CMD/CTL Termination - Channel A

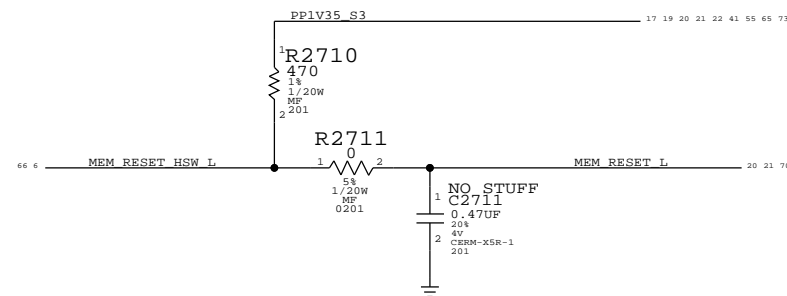


MEMORY RPACK SPARES

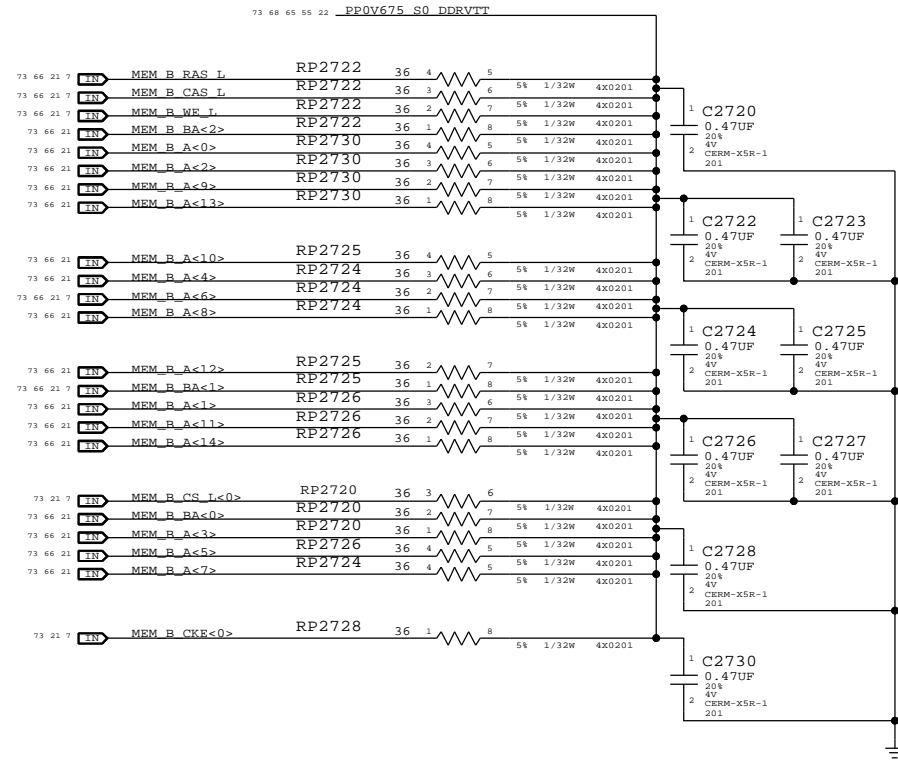


Memory Reset Pull Up

Reset is an open drain in Haswell ULT and needs pull up

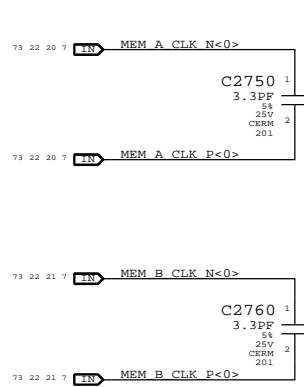


Memory CMD/CTL Termination - Channel B



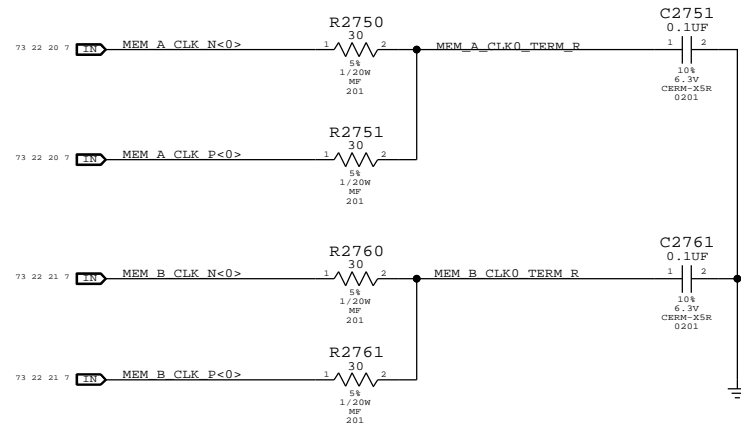
Memory Clock Near-End Termination

Place source C termination before first DRAM



Memory Clock Far-End Termination

Place RC end termination after last DRAM



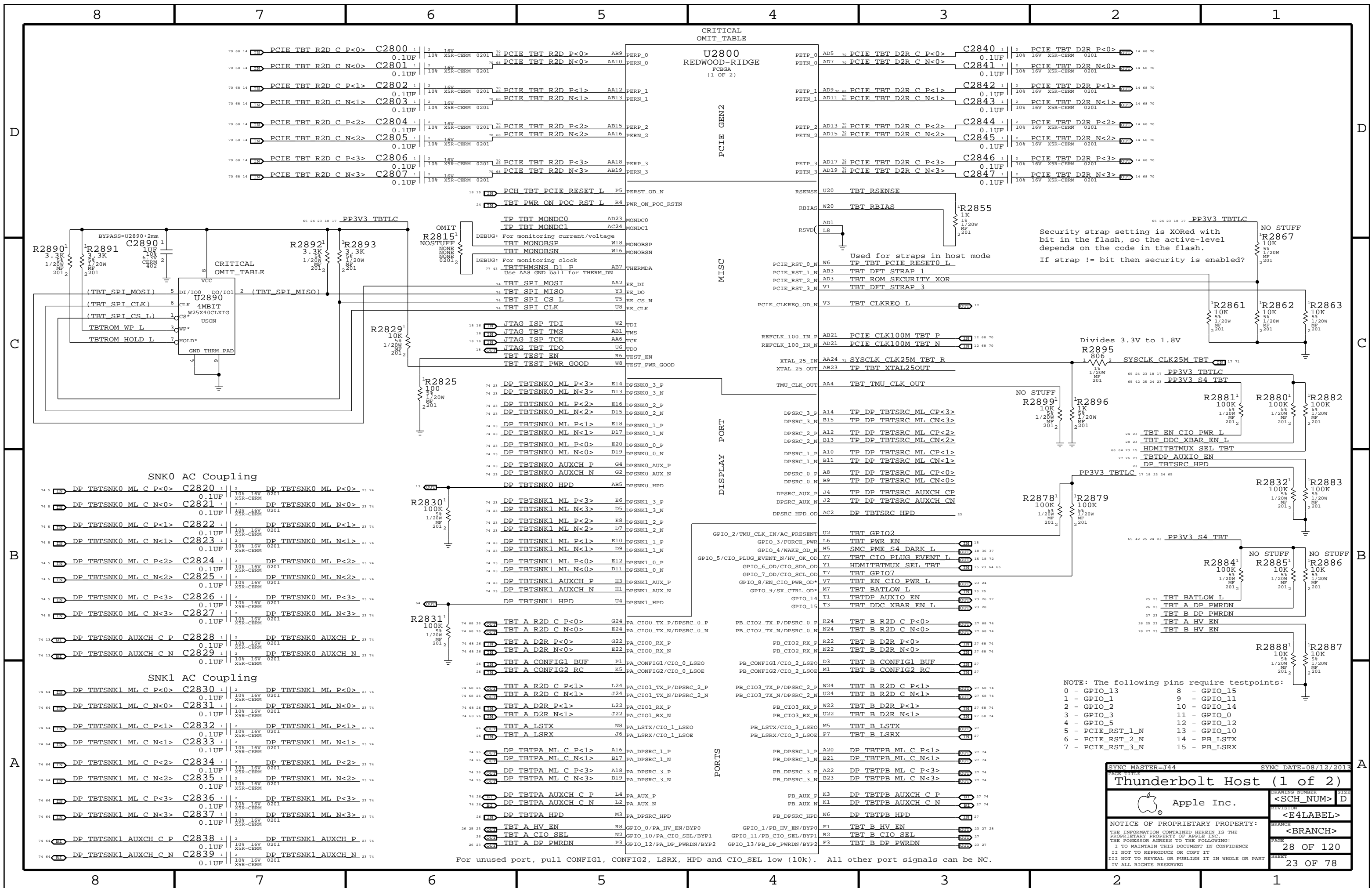
SYNC MASTER=J44 YONAS-4GB SYNC DATE=04/02/2013

DDR3 Termination

Apple Inc.

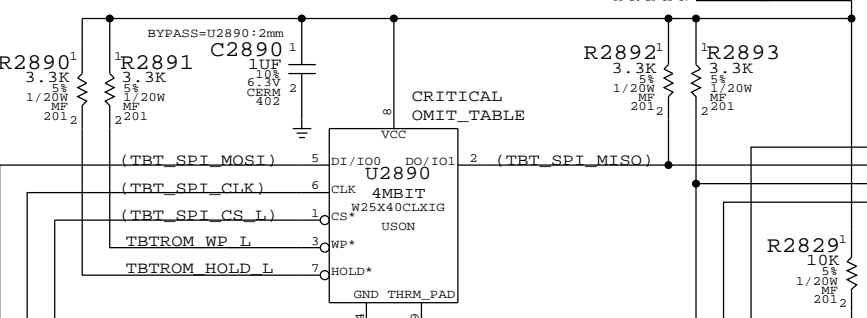
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PAGE	27 OF 120
SHEET	22 OF 78



CRITICAL OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)



SNK0 AC Coupling

74 5	DP TBTSNK0 ML C P<0>	C2820	DP TBTSNK0 ML P<0>	23 74
74 5	DP TBTSNK0 ML C N<0>	C2821	DP TBTSNK0 ML N<0>	23 74
74 5	DP TBTSNK0 ML C P<1>	C2822	DP TBTSNK0 ML P<1>	23 74
74 5	DP TBTSNK0 ML C N<1>	C2823	DP TBTSNK0 ML N<1>	23 74
74 5	DP TBTSNK0 ML C P<2>	C2824	DP TBTSNK0 ML P<2>	23 74
74 5	DP TBTSNK0 ML C N<2>	C2825	DP TBTSNK0 ML N<2>	23 74
74 5	DP TBTSNK0 ML C P<3>	C2826	DP TBTSNK0 ML P<3>	23 74
74 5	DP TBTSNK0 ML C N<3>	C2827	DP TBTSNK0 ML N<3>	23 74
74 13	DP TBTSNK0 AUXCH C P	C2828	DP TBTSNK0 AUXCH P	23 74
74 13	DP TBTSNK0 AUXCH C N	C2829	DP TBTSNK0 AUXCH N	23 74

SNK1 AC Coupling

74 64	DP TBTSNK1 ML C P<0>	C2830	DP TBTSNK1 ML P<0>	23 74
74 64	DP TBTSNK1 ML C N<0>	C2831	DP TBTSNK1 ML N<0>	23 74
74 64	DP TBTSNK1 ML C P<1>	C2832	DP TBTSNK1 ML P<1>	23 74
74 64	DP TBTSNK1 ML C N<1>	C2833	DP TBTSNK1 ML N<1>	23 74
74 64	DP TBTSNK1 ML C P<2>	C2834	DP TBTSNK1 ML P<2>	23 74
74 64	DP TBTSNK1 ML C N<2>	C2835	DP TBTSNK1 ML N<2>	23 74
74 64	DP TBTSNK1 ML C P<3>	C2836	DP TBTSNK1 ML P<3>	23 74
74 64	DP TBTSNK1 ML C N<3>	C2837	DP TBTSNK1 ML N<3>	23 74
74 64	DP TBTSNK1 AUXCH C P	C2838	DP TBTSNK1 AUXCH P	23 74
74 64	DP TBTSNK1 AUXCH C N	C2839	DP TBTSNK1 AUXCH N	23 74

CRITICAL OMIT_TABLE

104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201
104	X5R-CERM	0201	104	X5R-CERM	0201

DP TBTSNK0 ML

74 23	DP TBTSNK0 ML P<3>	E14	DPSNK0_3_P
74 23	DP TBTSNK0 ML N<3>	D13	DPSNK0_3_N
74 23	DP TBTSNK0 ML P<2>	E16	DPSNK0_2_P
74 23	DP TBTSNK0 ML N<2>	D15	DPSNK0_2_N
74 23	DP TBTSNK0 ML P<1>	E18	DPSNK0_1_P
74 23	DP TBTSNK0 ML N<1>	D17	DPSNK0_1_N
74 23	DP TBTSNK0 ML P<0>	E20	DPSNK0_0_P
74 23	DP TBTSNK0 ML N<0>	D19	DPSNK0_0_N
74 23	DP TBTSNK0 AUXCH P	G4	DPSNK0_AUX_P
74 23	DP TBTSNK0 AUXCH N	G2	DPSNK0_AUX_N

DP TBTSNK1 ML

74 23	DP TBTSNK1 ML P<3>	E6	DPSNK1_3_P
74 23	DP TBTSNK1 ML N<3>	D5	DPSNK1_3_N
74 23	DP TBTSNK1 ML P<2>	E8	DPSNK1_2_P
74 23	DP TBTSNK1 ML N<2>	D7	DPSNK1_2_N
74 23	DP TBTSNK1 ML P<1>	E10	DPSNK1_1_P
74 23	DP TBTSNK1 ML N<1>	D9	DPSNK1_1_N
74 23	DP TBTSNK1 ML P<0>	E12	DPSNK1_0_P
74 23	DP TBTSNK1 ML N<0>	D11	DPSNK1_0_N
74 23	DP TBTSNK1 AUXCH P	H3	DPSNK1_AUX_P
74 23	DP TBTSNK1 AUXCH N	H1	DPSNK1_AUX_N

DP TBTPA ML

74 26	DP TBTPA ML C P<1>	A16	PA_DPSRC_1_P
74 26	DP TBTPA ML C N<1>	B17	PA_DPSRC_1_N
74 26	DP TBTPA ML C P<3>	A18	PA_DPSRC_3_P
74 26	DP TBTPA ML C N<3>	B19	PA_DPSRC_3_N
74 26	DP TBTPA AUXCH C P	L4	PA_AUX_P
74 26	DP TBTPA AUXCH C N	L2	PA_AUX_N
26	DP TBTPA HPD	M3	PA_DPSRC_HPD
26 23	TBT A HV EN	R8	GPIO_0/PA_HV_EN/BYP0
26 23	TBT A CIO SEL	N2	GPIO_10/PA_CIO_SEL/BYP1
26 23	TBT A DP PWRDN	P3	GPIO_12/PA_DP_PWRDN/BYP2

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash. If strap != bit then security is enabled?

Divides 3.3V to 1.8V

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LISTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC MASTER=J44 SYNC DATE=08/12/2013

Thunderbolt Host (1 of 2)

Apple Inc.

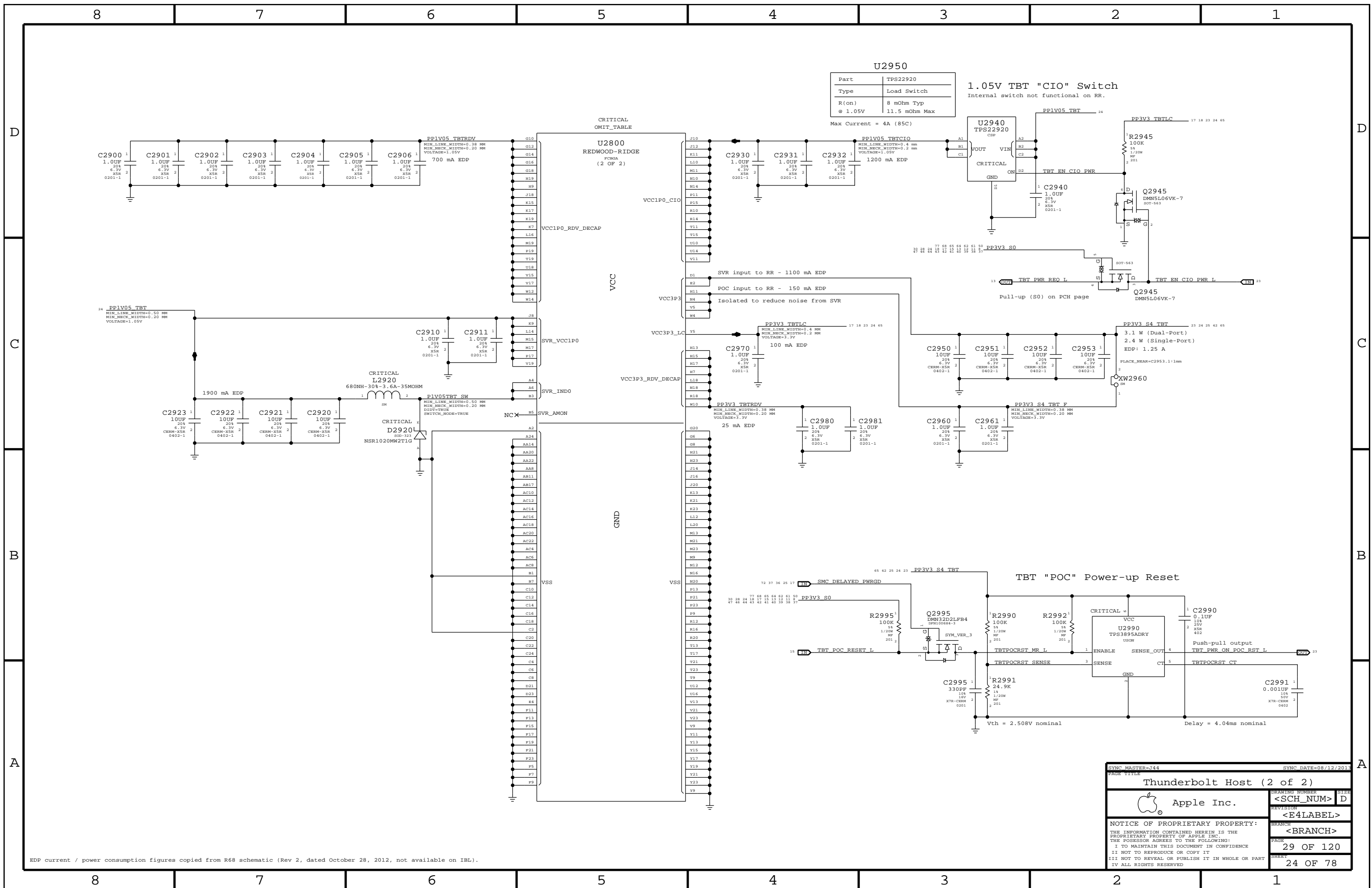
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PAGE: 28 OF 120 SHEET: 23 OF 78



U2950

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch
Internal switch not functional on RR.

3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A
PLACE_NEAR=C2953.1:1mm

TBT "POC" Power-up Reset

Vth = 2.508V nominal
Delay = 4.04ms nominal

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
Thunderbolt Host (2 of 2)			
Apple Inc.		DRAWING NUMBER	SIZE
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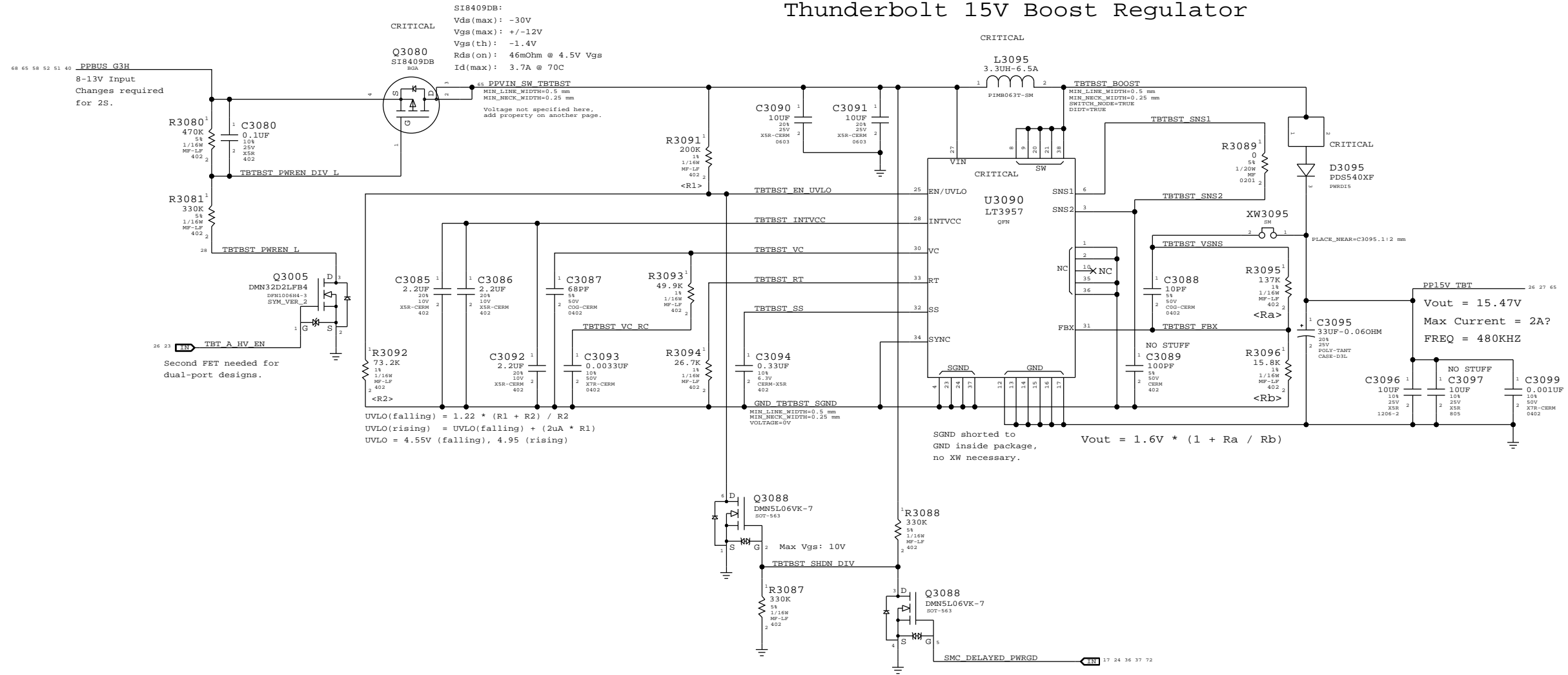
Page Notes

Power aliases required by this page:
 - =PPVIN_SW_TBTBST (8-13V Boost Input)
 - =PP15V_TBT_REG (15V Boost Output)

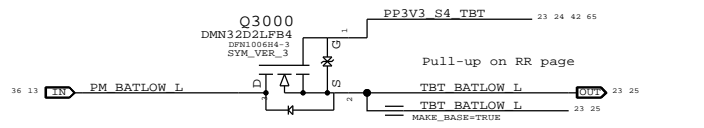
Signal aliases required by this page:
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BOM options provided by this page:
 (NONE)

Thunderbolt 15V Boost Regulator



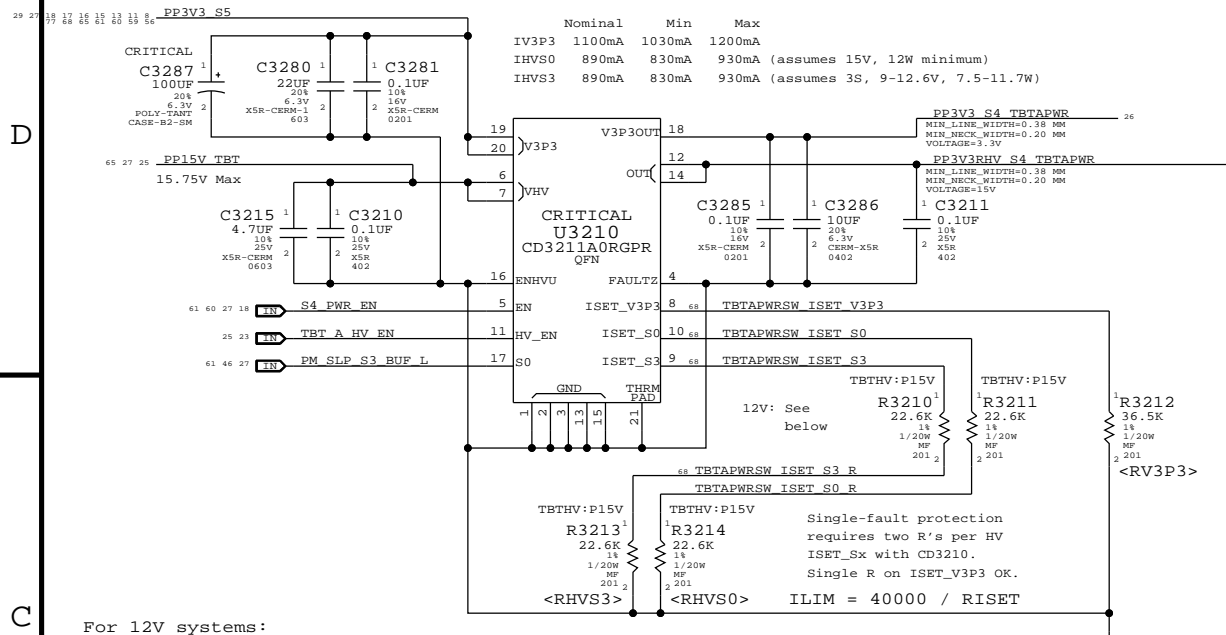
BATLOW# Isolation



SYNC MASTER=144		SYNC DATE=08/12/2013	
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

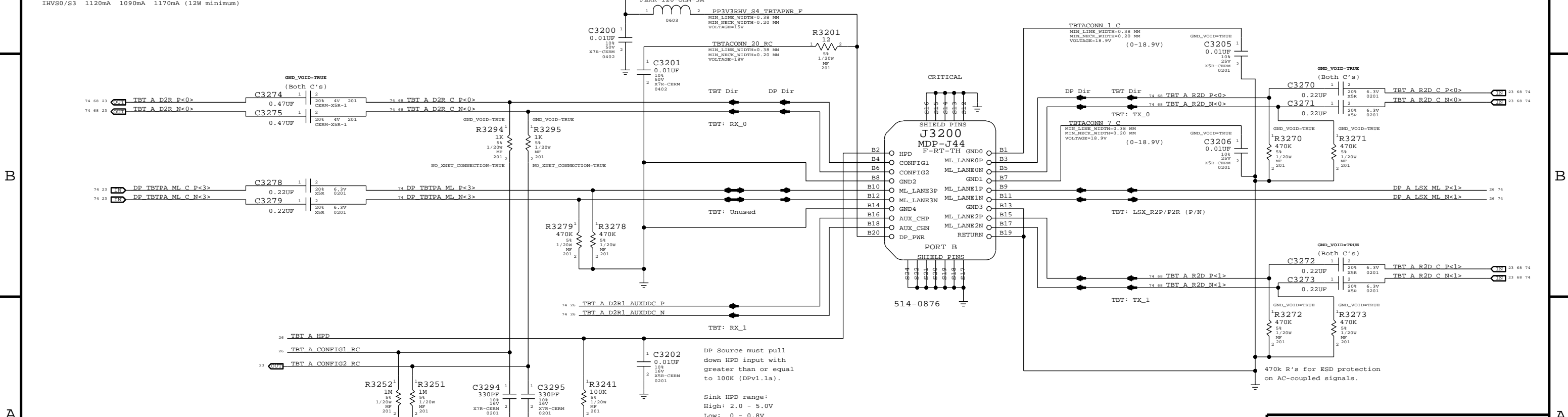


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES_MTL FILM,1/20W,17.8K,1.0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES_MTL FILM,1/20W,17.8K,1.0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal	Min	Max
IHV50/S3	1120mA	1090mA
		1170mA (12W minimum)

Thunderbolt Connector A



SYNC MASTER=144 SYNC DATE=08/12/2013

Thunderbolt Connector A

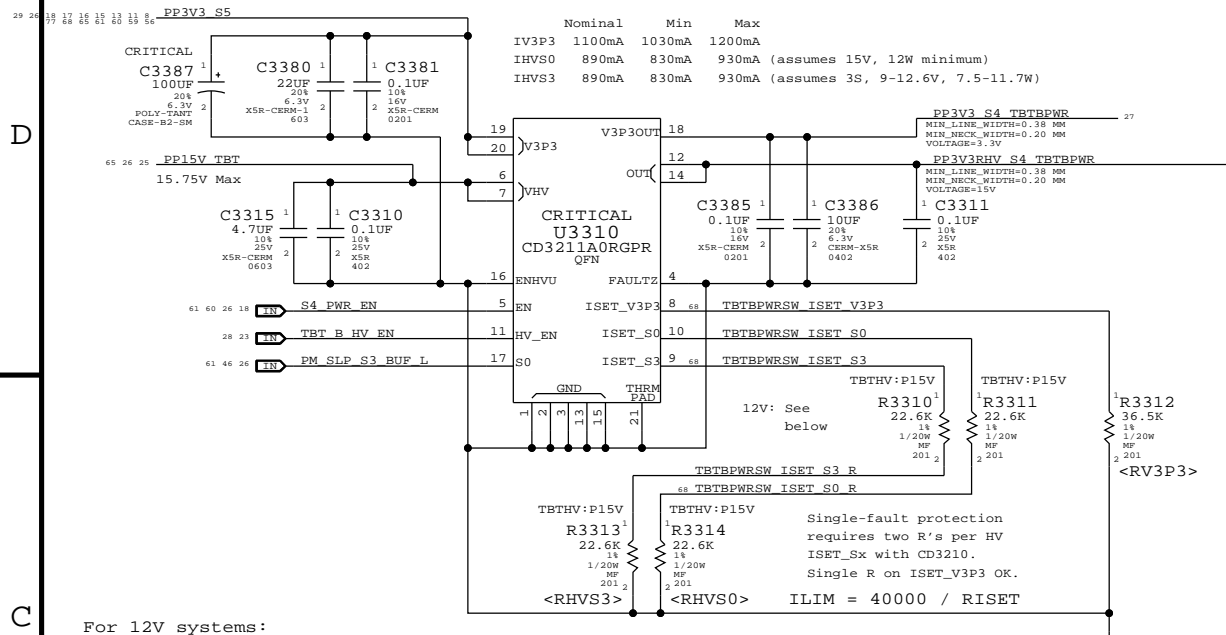
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

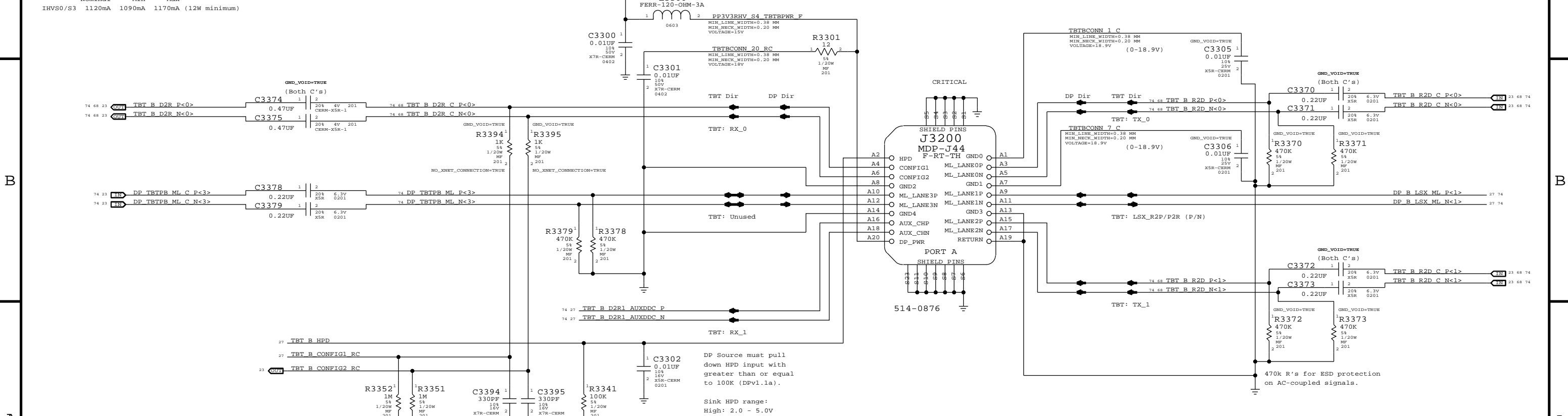


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES_MTL_FILM,1/20W,17.8K,1.0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES_MTL_FILM,1/20W,17.8K,1.0201,SMD,LF	R3311,R3314		TBTHV:P12V

Nominal	Min	Max	
IHV50/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B



SYNC MASTER=144 SYNC DATE=08/12/2013

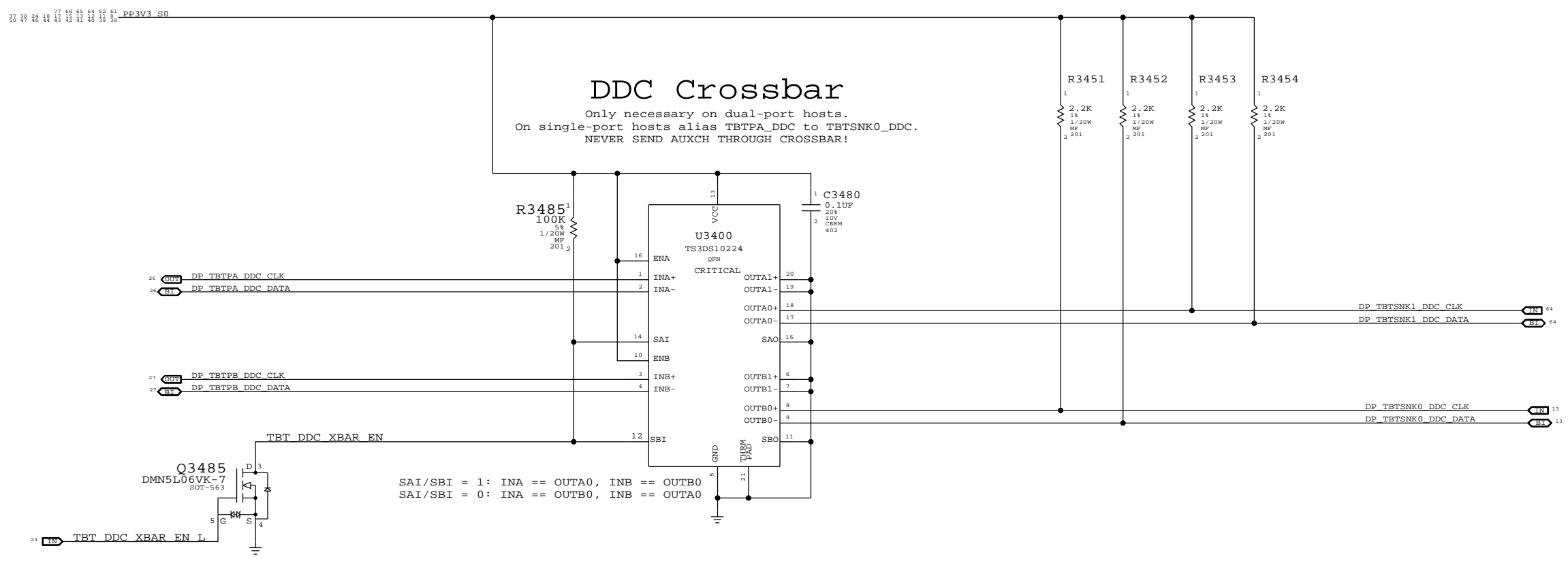
Thunderbolt Connector B

Apple Inc.

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REVISION	
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PAGE	33 OF 120
SHEET	27 OF 78

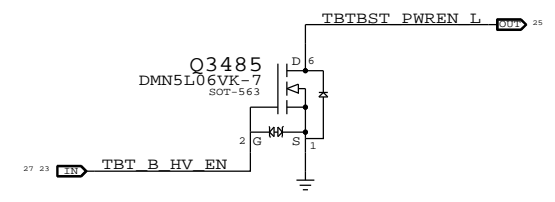
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DDC Pull-Ups
 2.2k pull-ups are required by PCH to indicate active display interface.
 DP++ spec violation, should remove!
 NOTE: Only DDC_DATA is sensed, so DDC_CLK pull-ups are unstuffed.

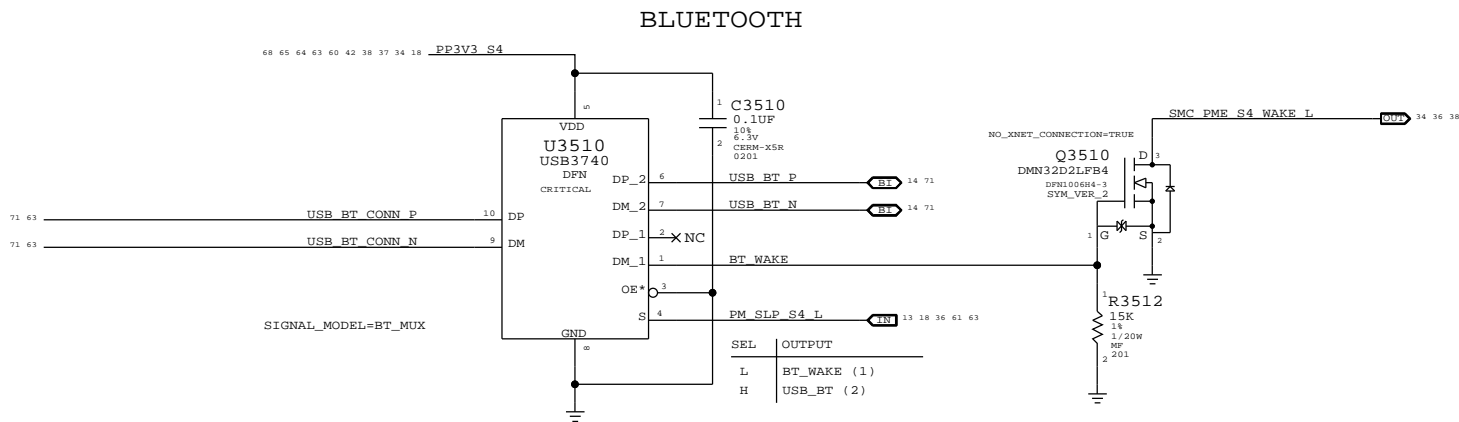
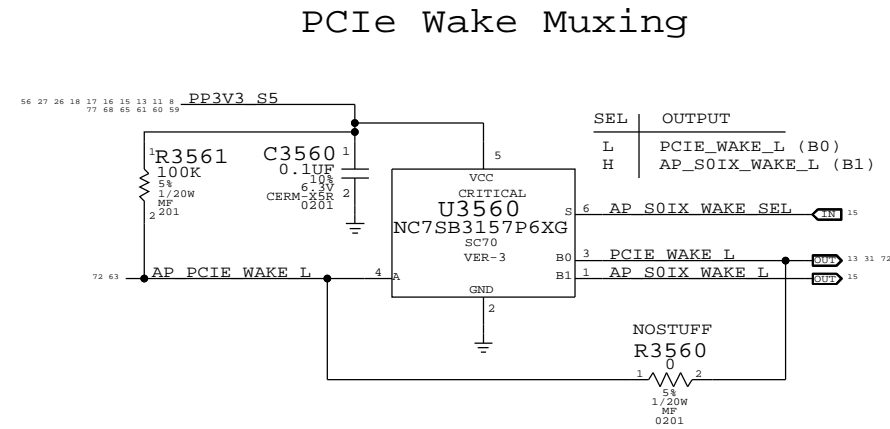


SAI/SBI = 1: INA == OUTA0, INB == OUTB0
 SAI/SBI = 0: INA == OUTB0, INB == OUTA0

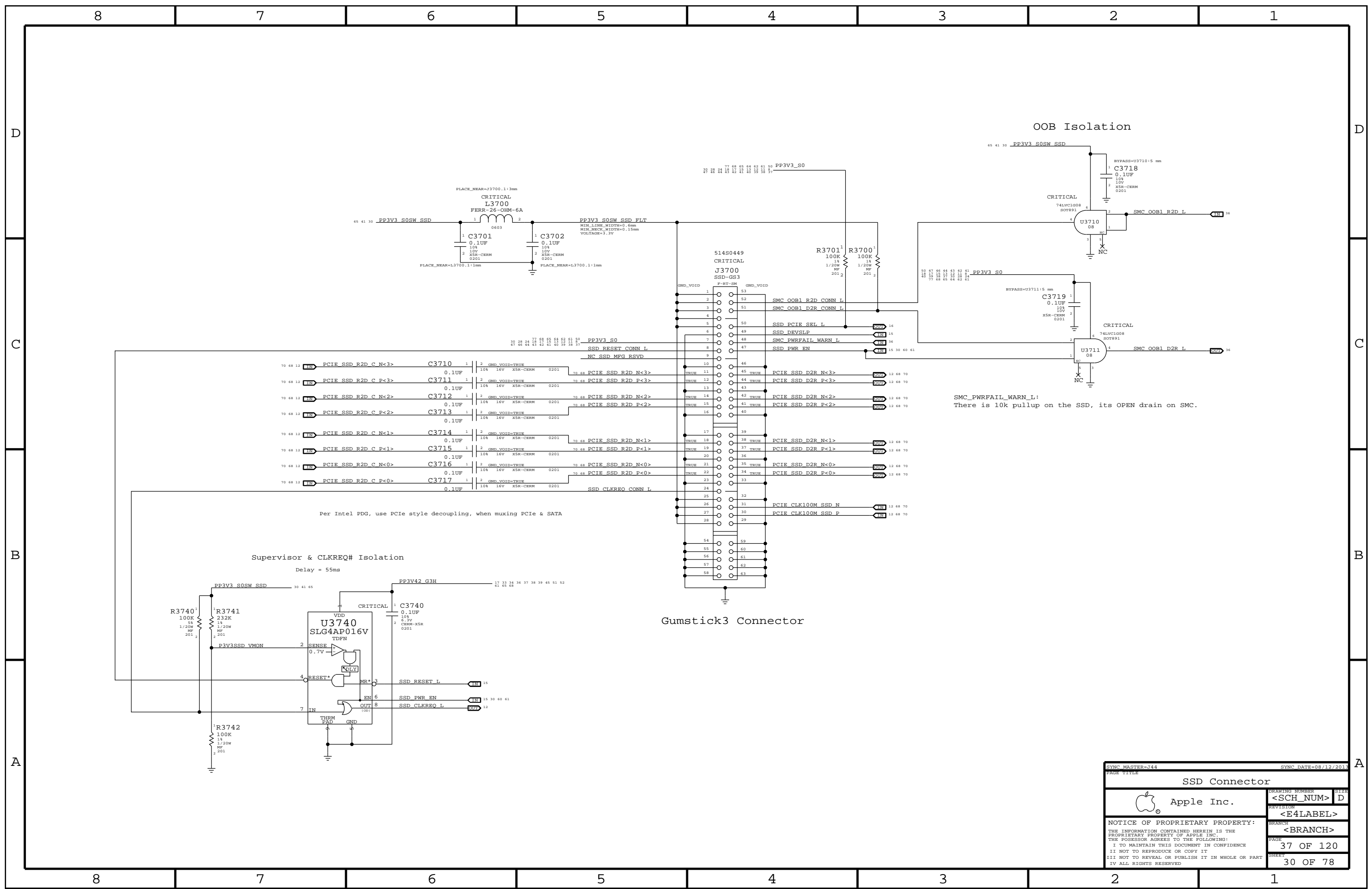
Second FET needed for dual-port designs.
 CONNECTS TO TBTBTS_PWREN_L ON PAGE 30.



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
DDC Crossbar			
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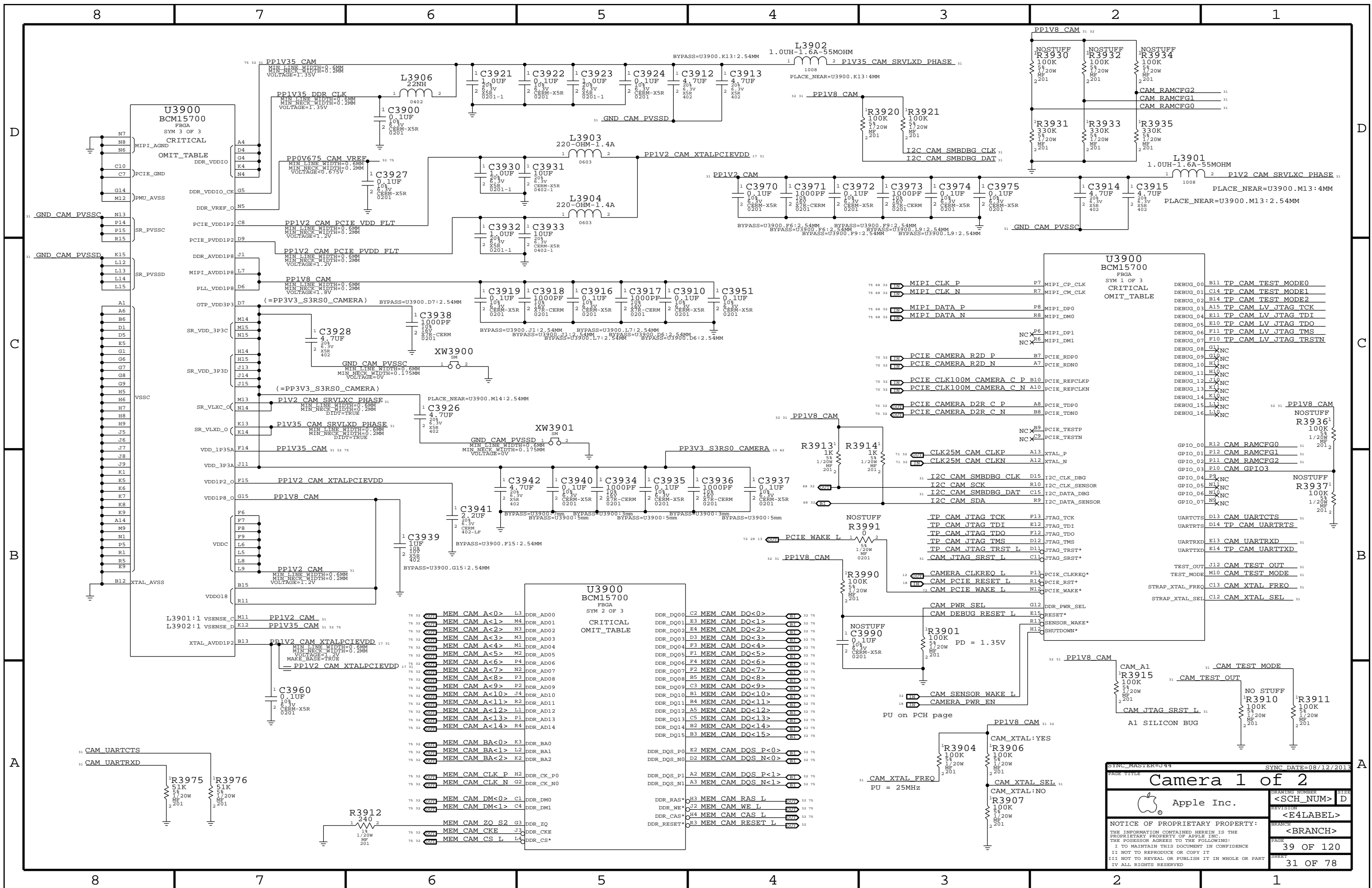


SMC_PWRFAIL_WARN_L:
There is 10k pullup on the SSD, its OPEN drain on SMC.

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

Supervisor & CLKREQ# Isolation
Delay = 55ms

SYNC MASTER=144		SYNC DATE=08/12/2013	
SSD Connector			
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		PAGE	37 OF 120
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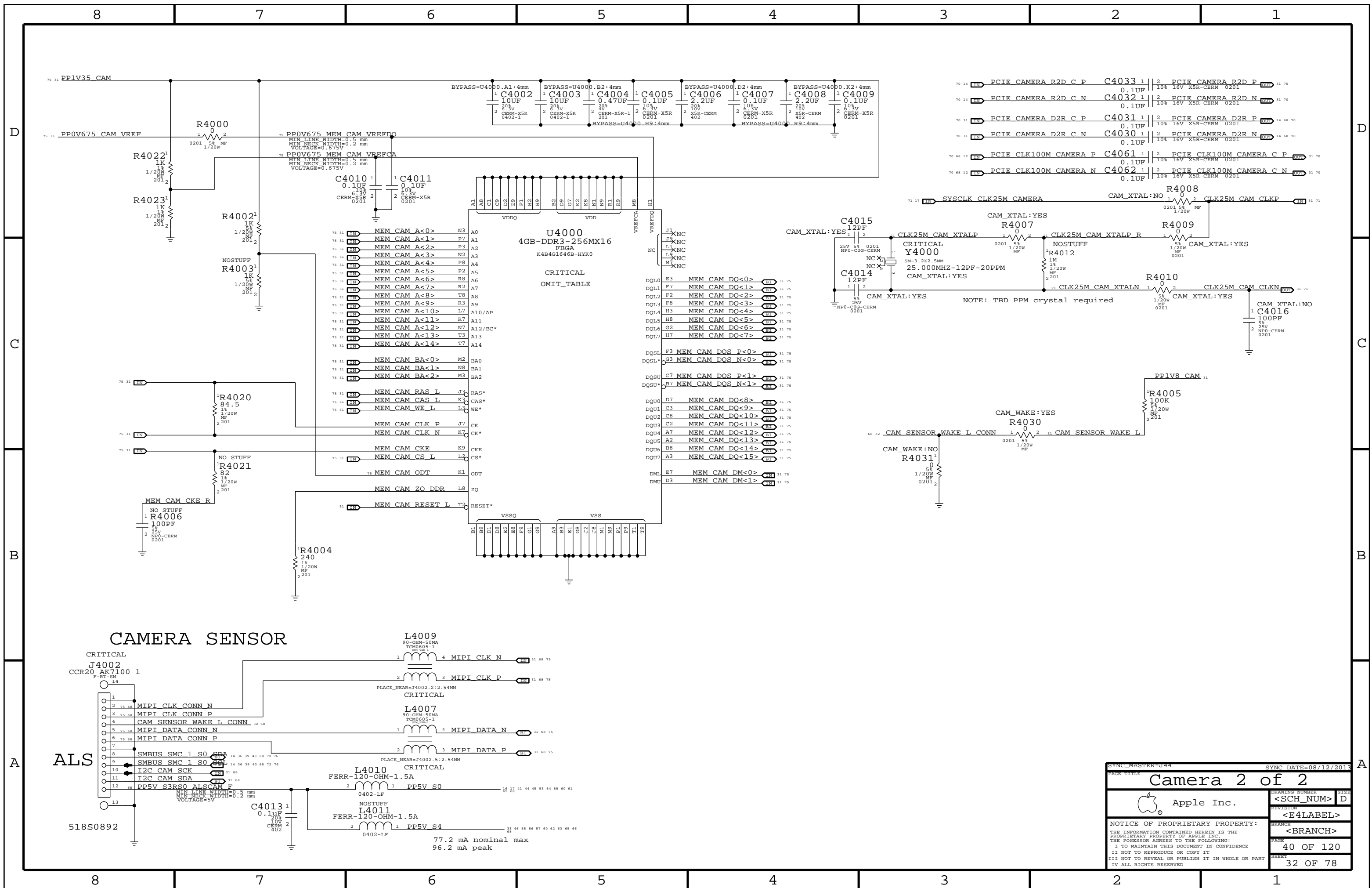
Camera 1 of 2

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 SYNC_DATE=08/12/2013

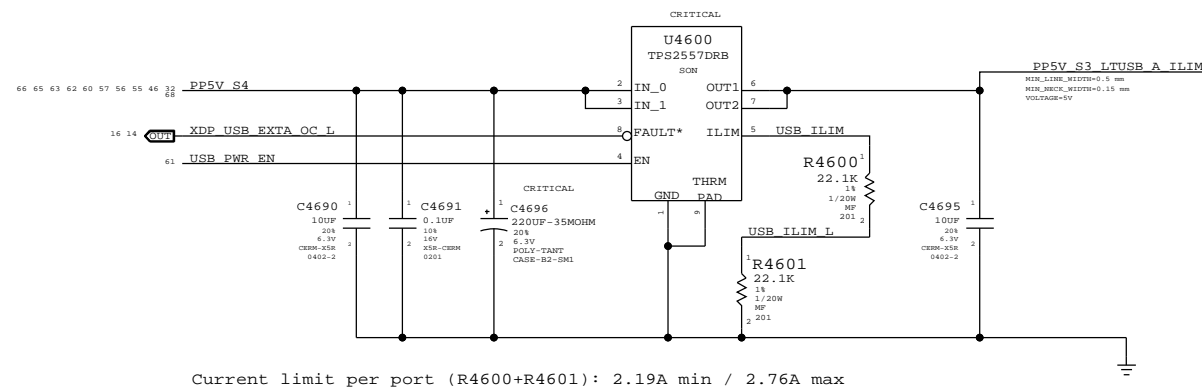
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PAGE TITLE		SYNC DATE=08/12/2013	
Camera 2 of 2		DRAWING NUMBER	SIZE
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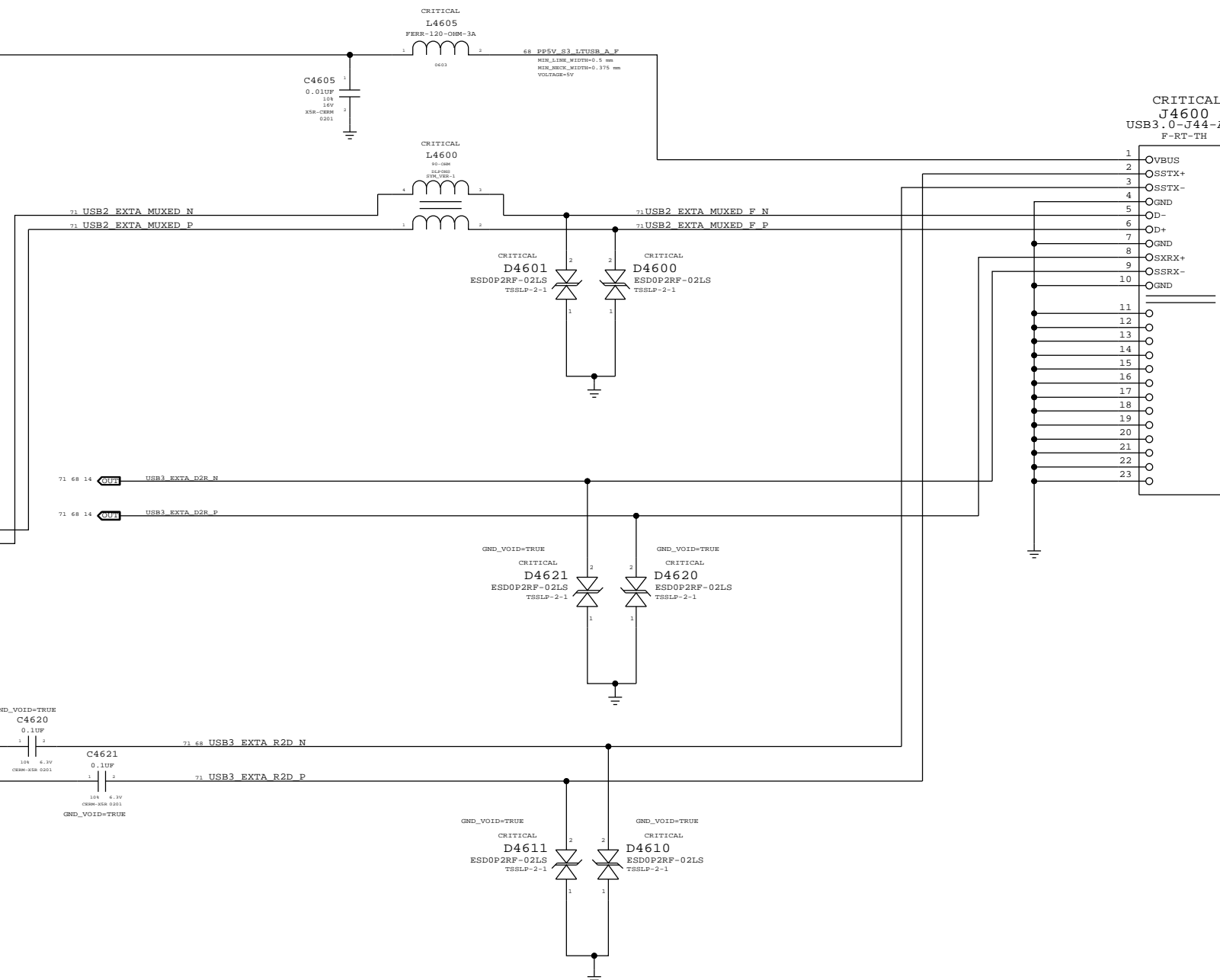
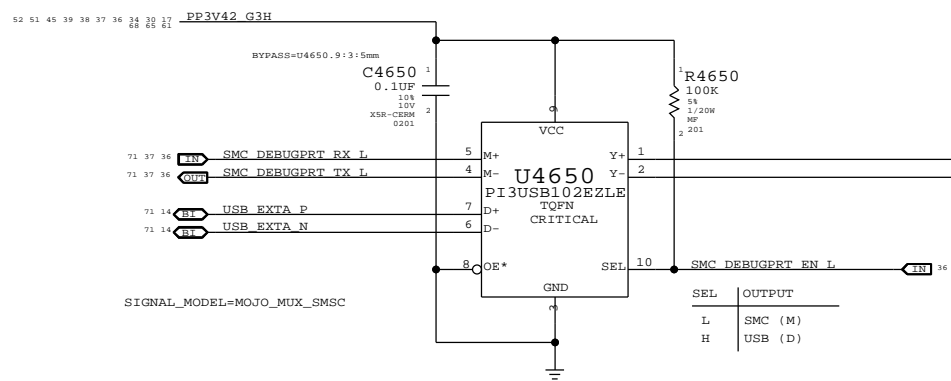
RIGHT USB PORT A

USB Port Power Switch



Mojo SMC Debug Mux

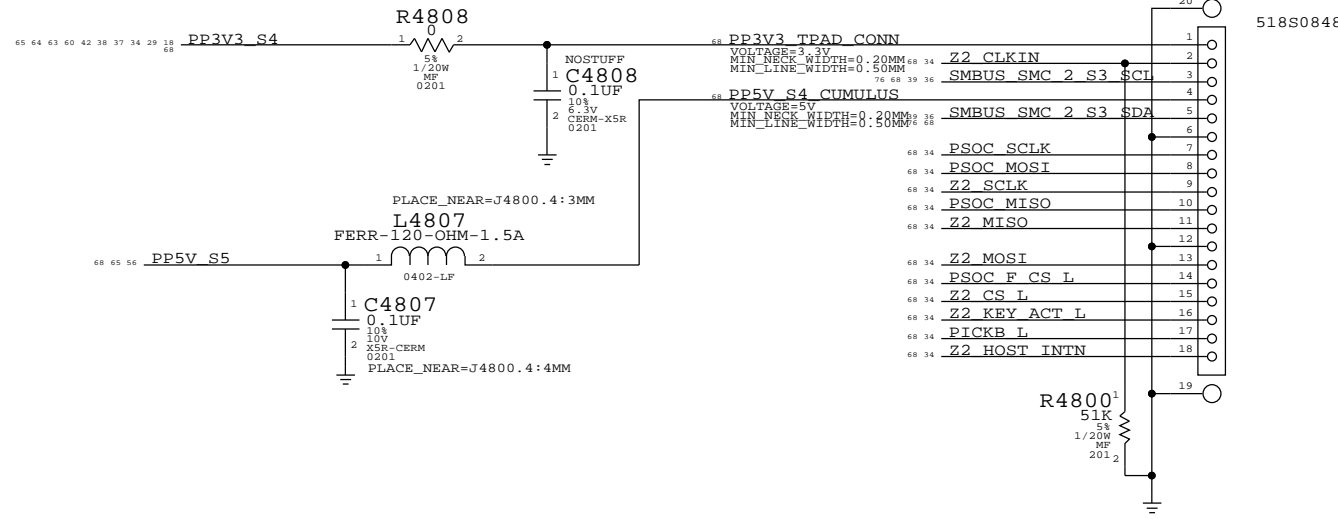
THE PI3USB102E CAN CLAMP VOLTAGE IN THE INTERNAL USB PINS



SYNC MASTER=J44		SYNC DATE=08/12/2013	
External A USB3 Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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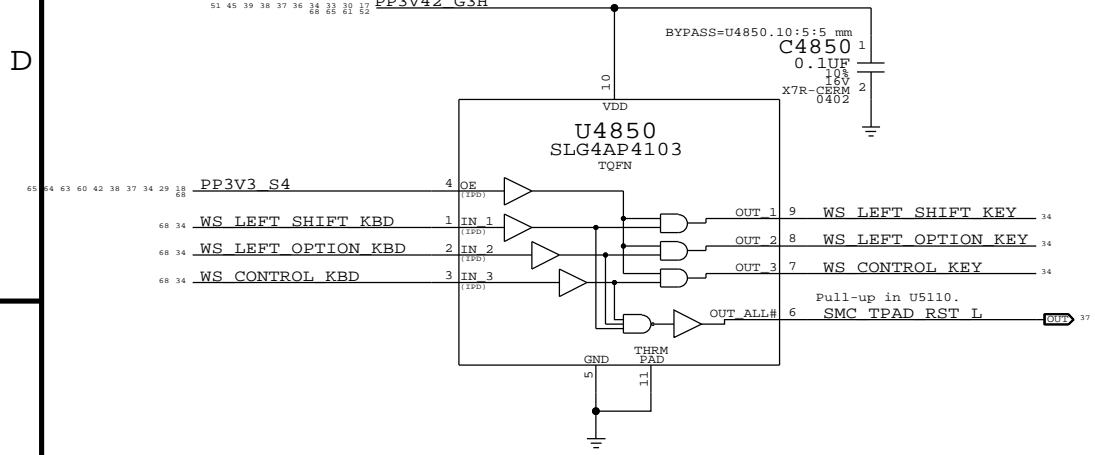
IPD Flex Connector

CRITICAL
J4800
FF14-18C-R11DL
F-RT-SM



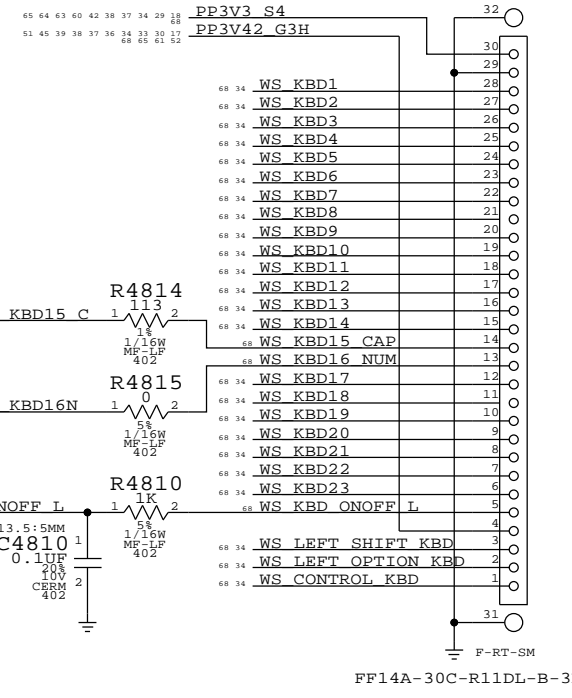
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



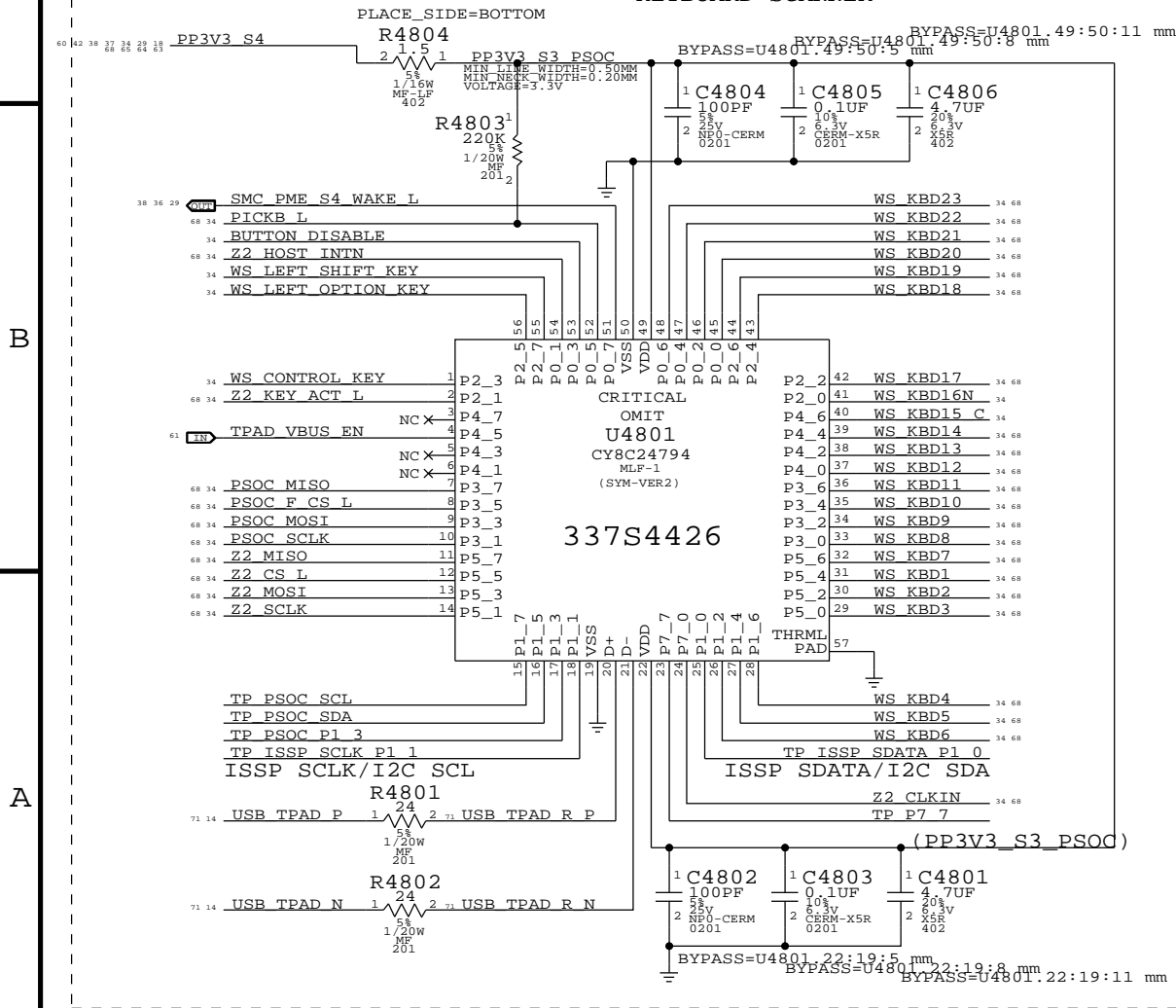
Keyboard Connector

518S0752
CRITICAL
J4813



PSOC USB CONTROLLER

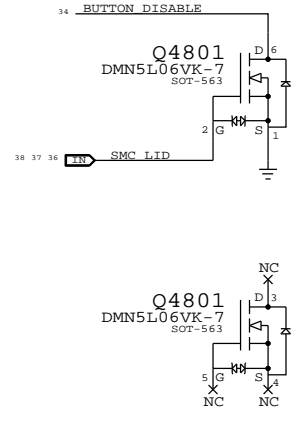
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

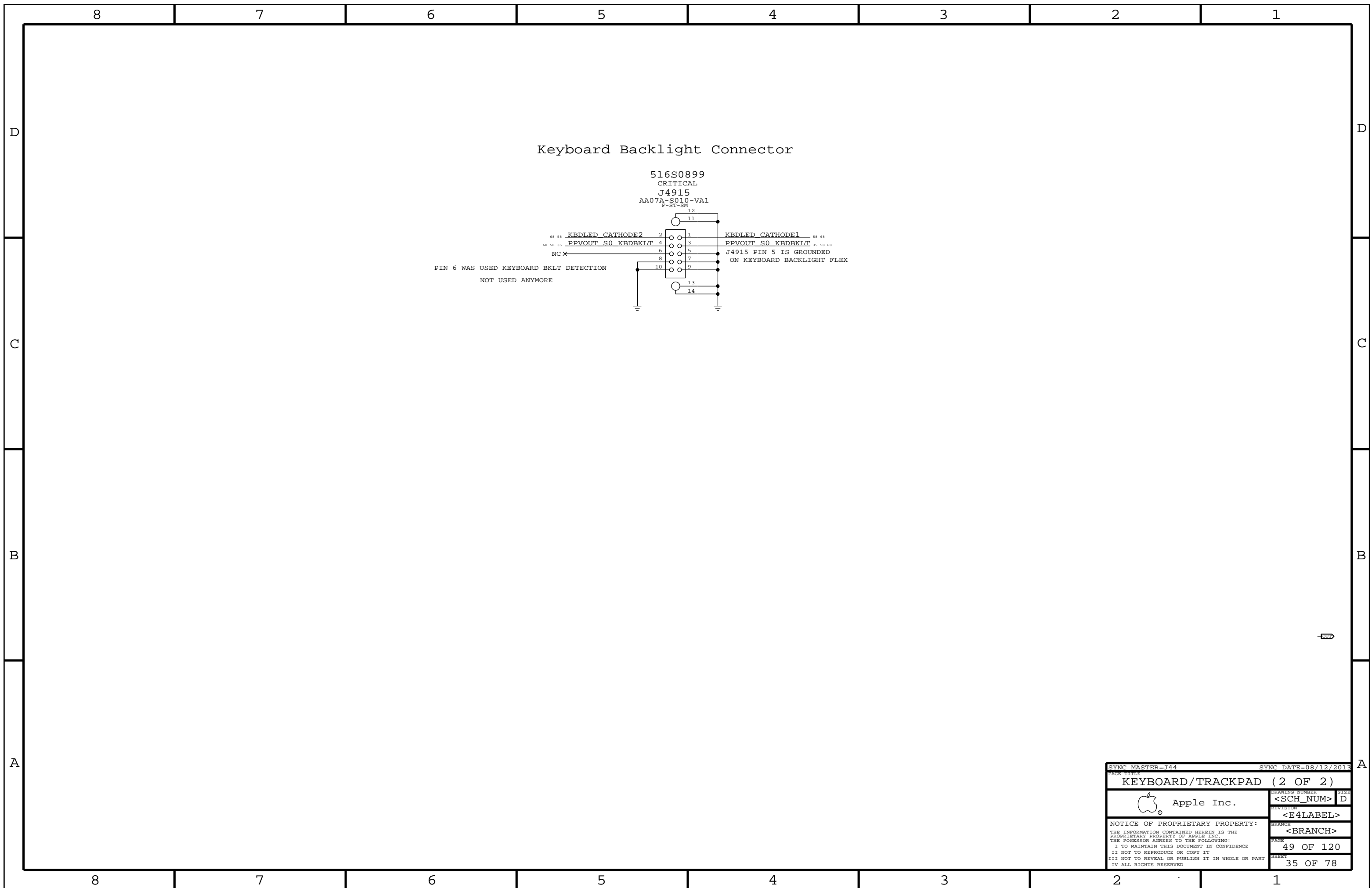
PLACE THESE COMPONENTS CLOSE TO J4800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

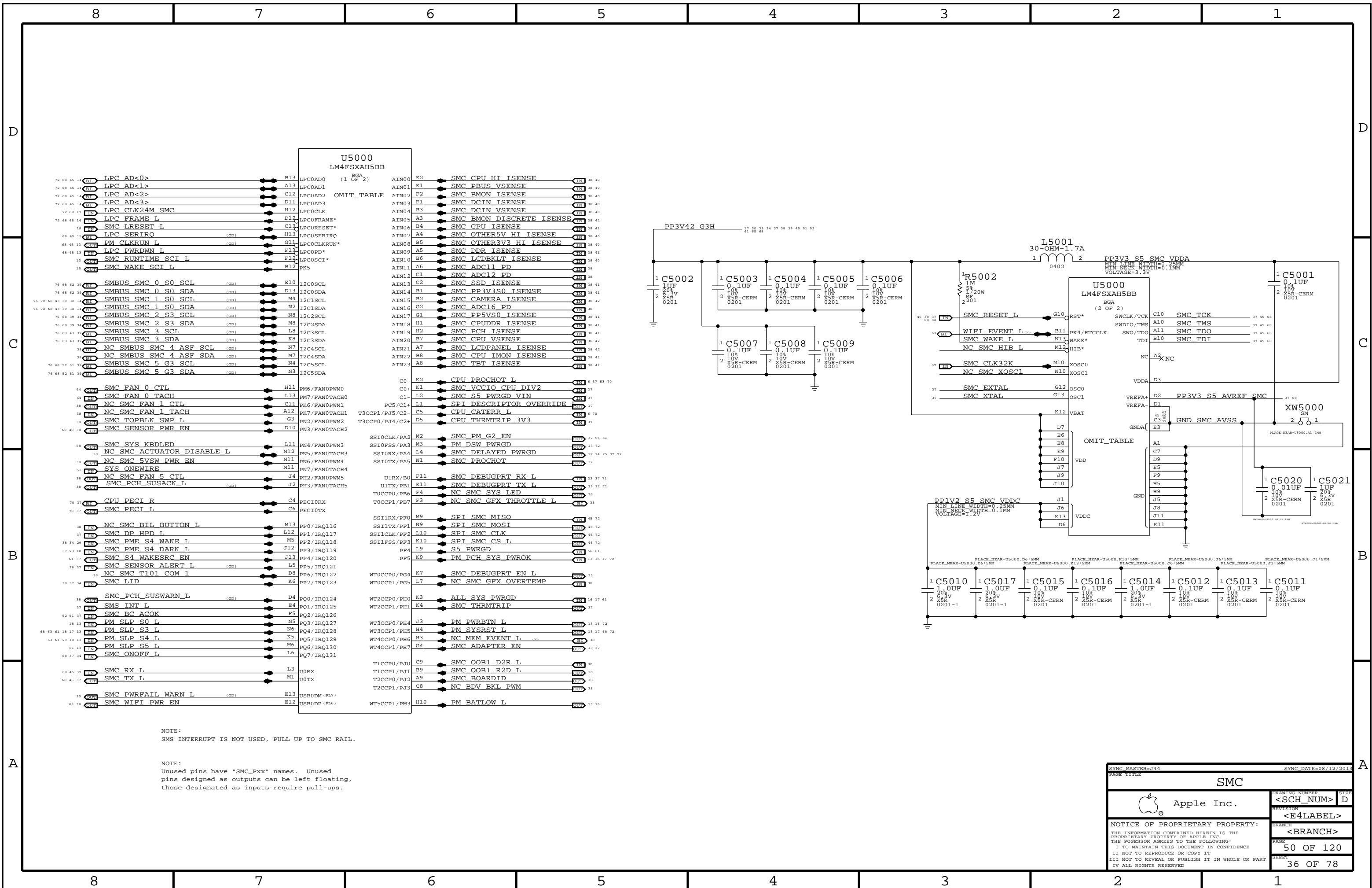


IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W	
		80UA		0.204 V	16.32E-6 W	
		60MA (MAX)	10 OHM	0.6 V	36E-3 W	
3V3 LDO	VDD	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W	
		8MA (TYP)	1.5 OHM	0.012 V	96E-6 W	
PSOC	VDD	14MA (MAX)		0.021 V	294E-6 W	
		4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W	

SYNC MASTER=144 SYNC DATE=08/12/2013
PAGE TITLE
KEYBOARD/TRACKPAD (1 OF 2)
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PAGE TITLE KEYBOARD/TRACKPAD (2 OF 2)			
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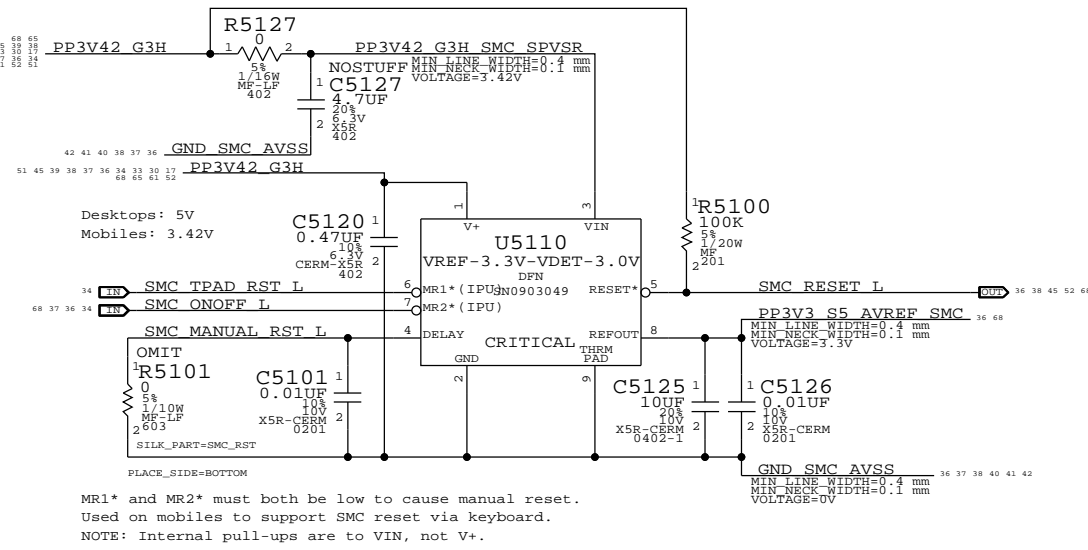


NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

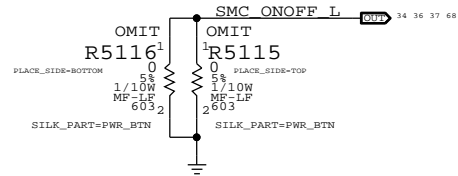
NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=144		SYNC DATE=08/12/2013	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
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SMC Reset "Button", Supervisor & AVREF Supply

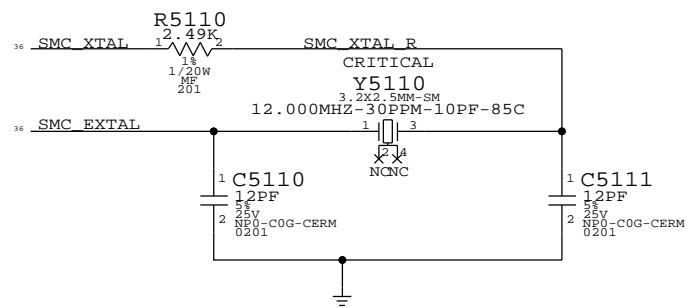


Debug Power "Buttons"

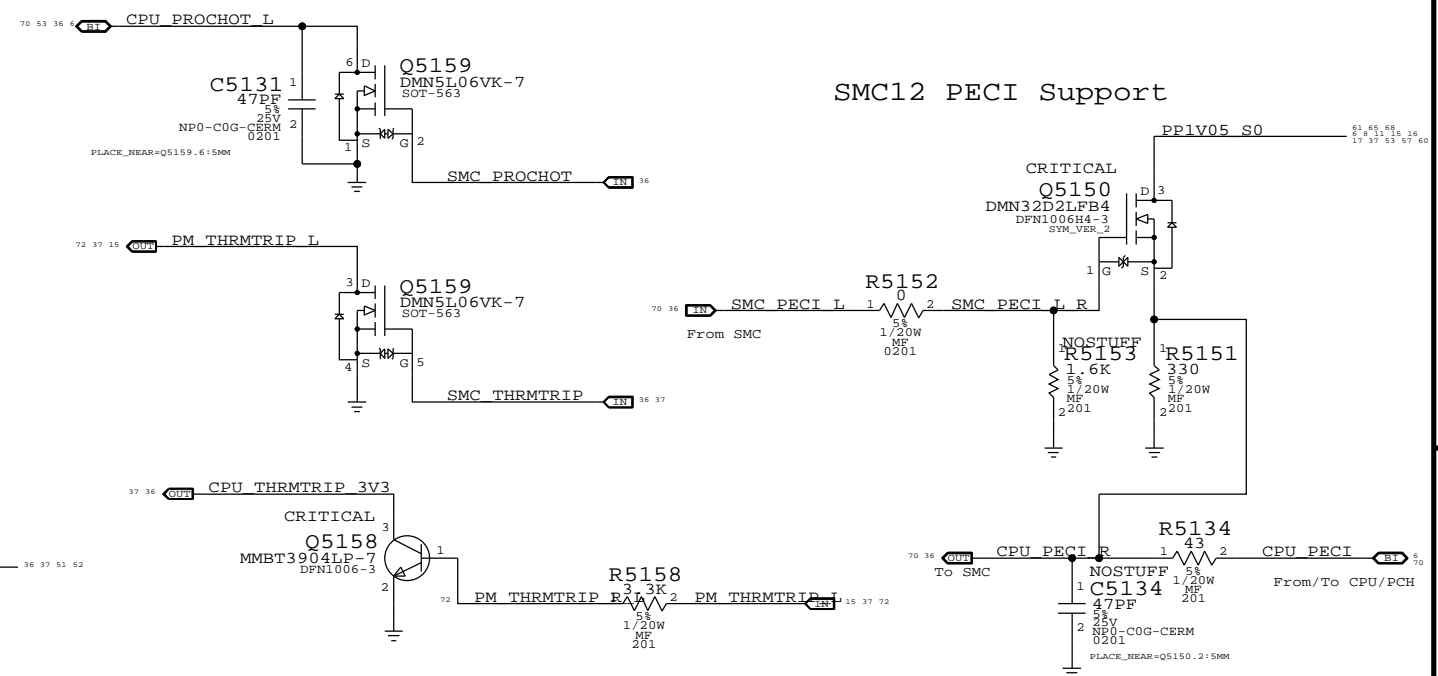


SMC Crystal Circuit

SMC USB Clock require these crystal values: 5, 6, 8, 10, 12, 16, 18, 20, 24, 25 Mhz



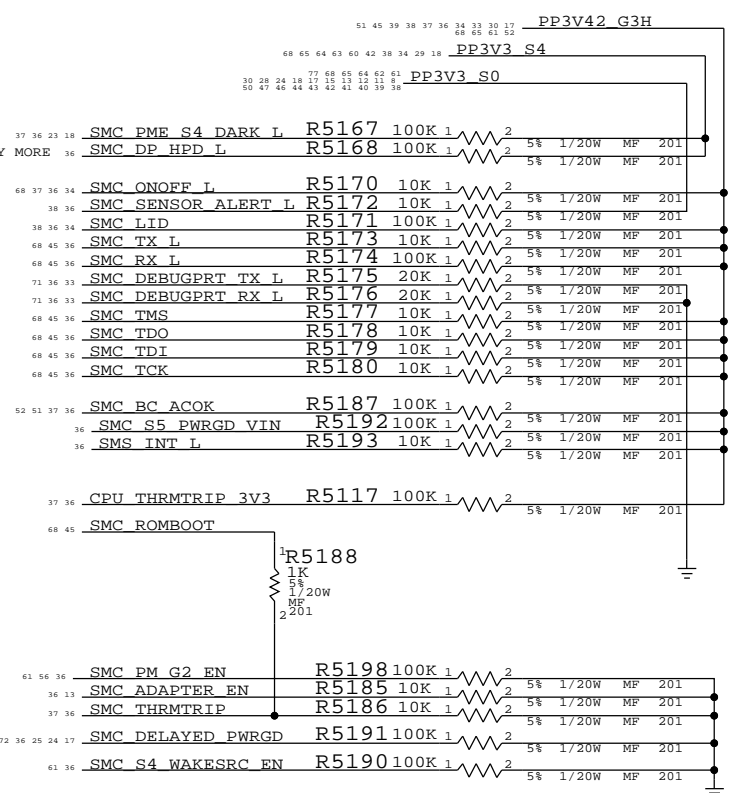
SMC12 PECI Support



SMC BC ACOK == SMC BC ACOK MAKE_BASE=TRUE

SMC PME S4 DARK L == SMC PME S4 DARK L MAKE_BASE=TRUE

PM CLK32K SUSCLK R1 == SMC CLK32K MAKE_NEAR=10550_A615_1mm

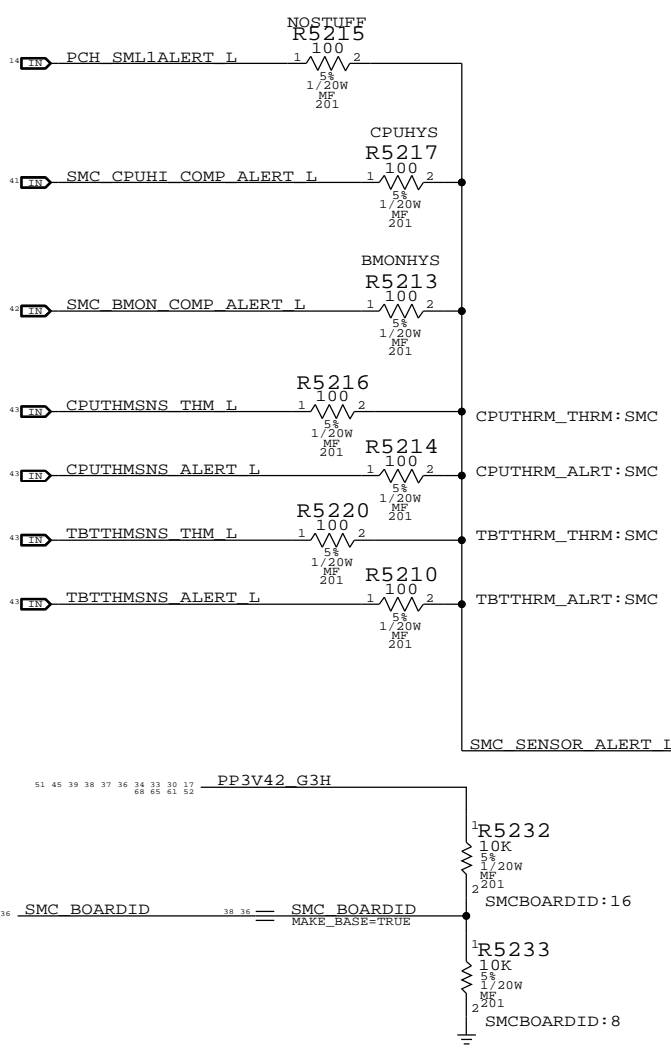


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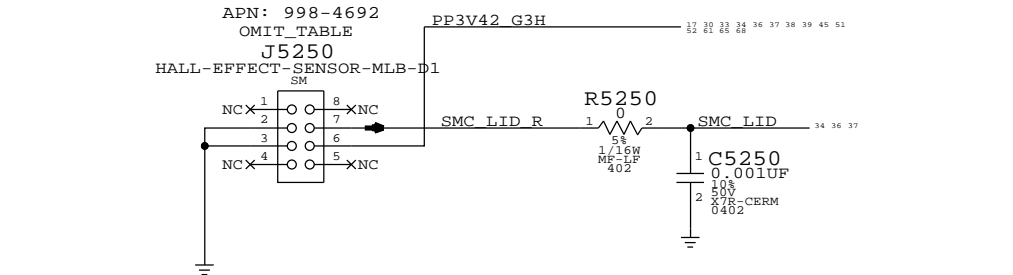
SMC12 ADC Assignments

40 38 36	SMC CPU HI ISENSE	=	SMC CPU HI ISENSE	36 38 40
40 38 36	SMC PBUS VSENSE	=	SMC PBUS VSENSE	36 38 40
40 38 36	SMC BMON ISENSE	=	SMC BMON ISENSE	36 38 40
40 38 36	SMC DCIN ISENSE	=	SMC DCIN ISENSE	36 38 40
40 38 36	SMC DCIN VSENSE	=	SMC DCIN VSENSE	36 38 40
40 38 36	SMC BMON DISCRETE ISENSE	=	SMC BMON DISCRETE ISENSE	36 38 42
41 38 36	SMC CPU ISENSE	=	SMC CPU ISENSE	36 38 41
40 38 36	SMC OTHER5V HI ISENSE	=	SMC OTHER5V HI ISENSE	36 38 40
40 38 36	SMC OTHER3V3 HI ISENSE	=	SMC OTHER3V3 HI ISENSE	36 38 40
41 38 36	SMC DDR ISENSE	=	SMC DDR ISENSE	36 38 41
40 38 36	SMC LCDBKLT ISENSE	=	SMC LCDBKLT ISENSE	36 38 40
38 36	SMC ADC11 PD	=	SMC ADC11 PD	36 38
38 36	SMC ADC12 PD	=	SMC ADC12 PD	36 38
41 38 36	SMC SSD ISENSE	=	SMC SSD ISENSE	36 38 41
41 38 36	SMC PP3V3S0 ISENSE	=	SMC PP3V3S0 ISENSE	36 38 41
42 38 36	SMC CAMERA ISENSE	=	SMC CAMERA ISENSE	36 38 42
38 36	SMC ADC16 PD	=	SMC ADC16 PD	36 38
41 38 36	SMC PP5V50 ISENSE	=	SMC PP5V50 ISENSE	36 38 41
41 38 36	SMC CPUDDR ISENSE	=	SMC CPUDDR ISENSE	36 38 41
41 38 36	SMC PCH ISENSE	=	SMC PCH ISENSE	36 38 41
42 38 36	SMC CPU VSENSE	=	SMC CPU VSENSE	36 38 42
42 38 36	SMC LCDPANEL ISENSE	=	SMC LCDPANEL ISENSE	36 38 42
42 38 36	SMC CPU IMON ISENSE	=	SMC CPU IMON ISENSE	36 38 42
42 38 36	SMC TBT ISENSE	=	SMC TBT ISENSE	36 38 42

Thermal Alerts



Hall Effect Pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-0912	1	SUBASSY,PCBA HALL EFFECT,J44	J5250	CRITICAL	

639-4502 (J44 HALL EFFECT BOARD) REPORTS TO 677-0912

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM: BOTH	CPUTHRM_THRM: SMC, CPUTHRM_ALERT: SMC
CPUTHRM: THRM	CPUTHRM_THRM: SMC, CPUTHRM_ALERT: PU
CPUTHRM: ALERT	CPUTHRM_THRM: PU, CPUTHRM_ALERT: SMC
CPUTHRM: NONE	CPUTHRM_THRM: PU, CPUTHRM_ALERT: PU

Specify one of these BOM GROUPs.

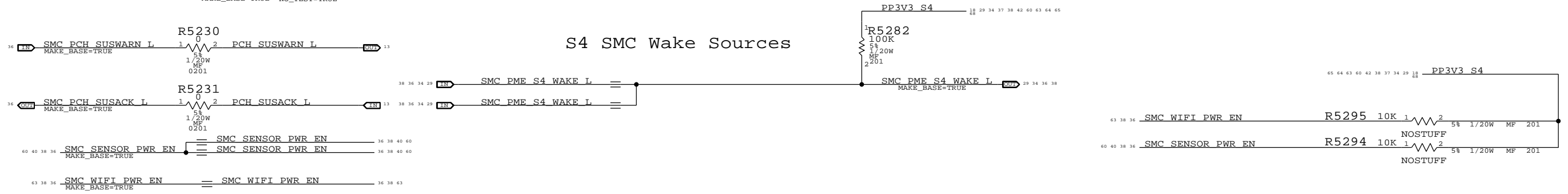
BOM GROUP	BOM OPTIONS
TBTHRM: BOTH	TBTHRM_THRM: SMC, TBTHRM_ALERT: SMC
TBTHRM: THRM	TBTHRM_THRM: SMC, TBTHRM_ALERT: PU
TBTHRM: ALERT	TBTHRM_THRM: PU, TBTHRM_ALERT: SMC
TBTHRM: NONE	TBTHRM_THRM: PU, TBTHRM_ALERT: PU
TBTHRM: GONE	

Requires EM1412-1 or EM1412-2 instead of EM1412-A, new APN needs to be created.

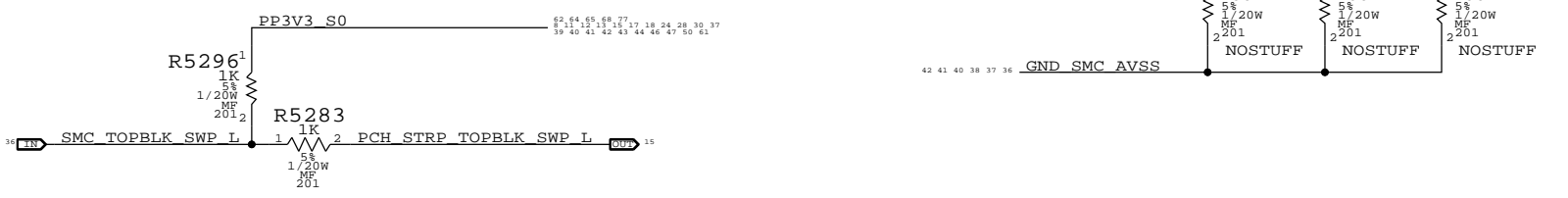
SMC12 Pin Assignments

38 36	NC SMBUS SMC 4 ASF SCL	=	NC SMBUS SMC 4 ASF SCL	36 38
38 36	NC SMBUS SMC 4 ASF SDA	=	NC SMBUS SMC 4 ASF SDA	36 38
38 36	NC BDV BKL PWM	=	NC BDV BKL PWM	36 38
38 36	NC SMC SYS LED	=	NC SMC SYS LED	36 38
38 36	NC SMC GFX THROTTLE L	=	NC SMC GFX THROTTLE L	36 38
38 36	NC SMC GFX OVERTEMP	=	NC SMC GFX OVERTEMP	36 38
38 36	NC SMC FAN 1 CTL	=	NC SMC FAN 1 CTL	36 38
38 36	NC SMC FAN 1 TACH	=	NC SMC FAN 1 TACH	36 38
38 36	NC SMC 5VSW PWR EN	=	NC SMC 5VSW PWR EN	36 38
38 36	NC SMC FAN 5 CTL	=	NC SMC FAN 5 CTL	36 38
38 36	NC SMC BIL BUTTON L	=	NC SMC BIL BUTTON L	36 38
38 36	NC MEM EVENT L	=	NC MEM EVENT L	36 38
38 36	NC SMC T101 COM 1	=	NC SMC T101 COM 1	36 38
38 36	NC SMC ACTUATOR DISABLE L	=	NC SMC ACTUATOR DISABLE L	36 38

S4 SMC Wake Sources



Top Block Swap

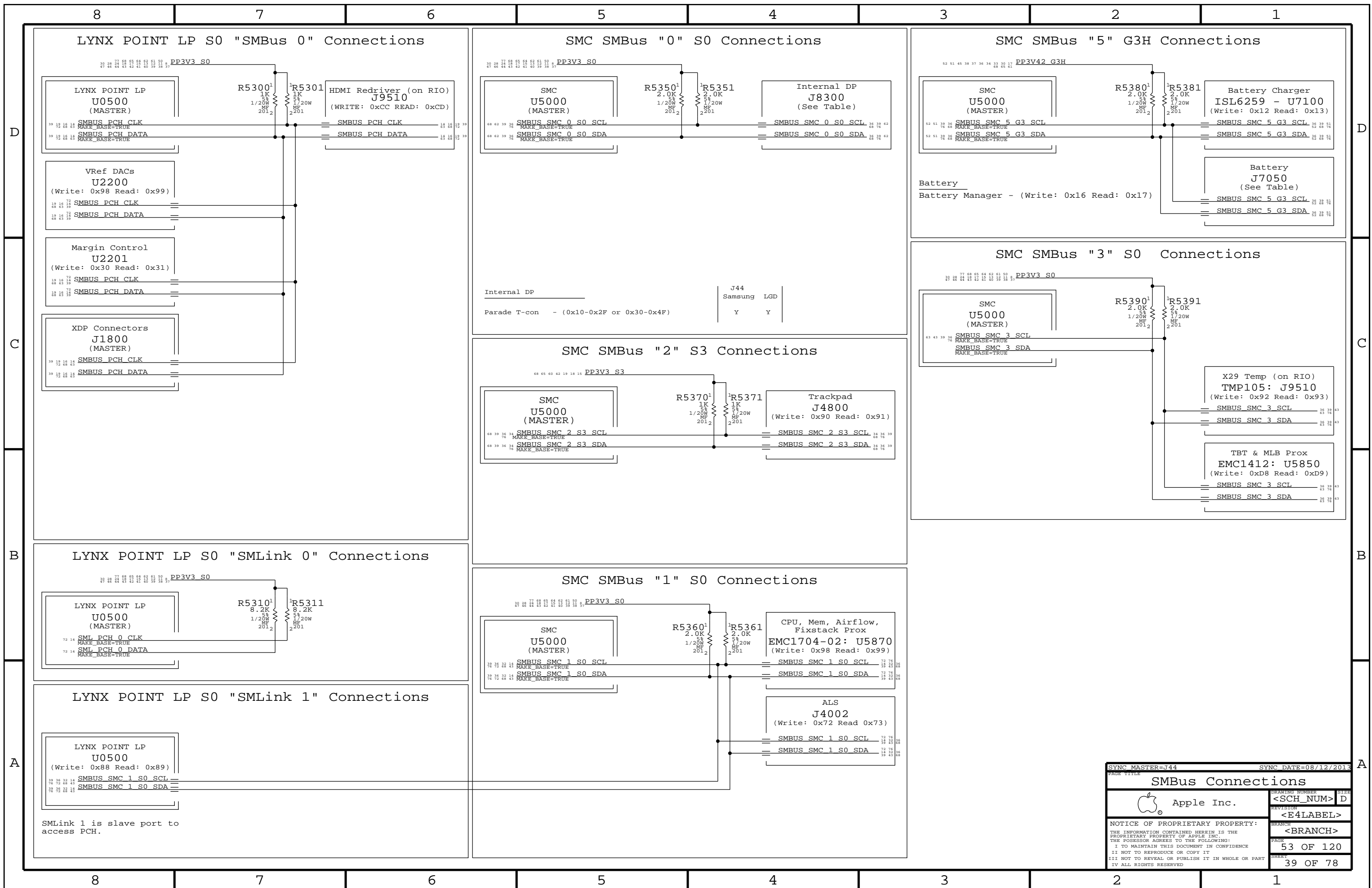


SMC Project Support

Apple Inc.

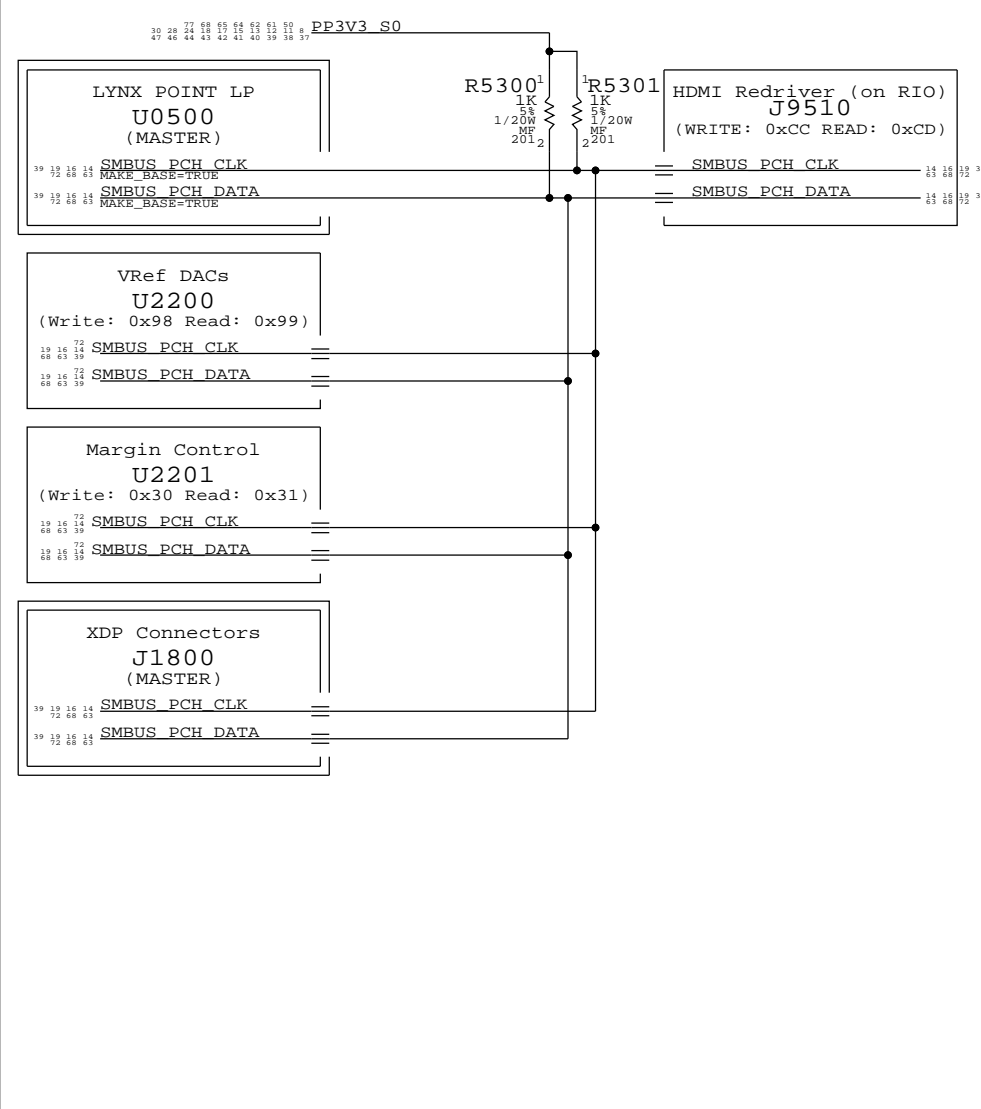
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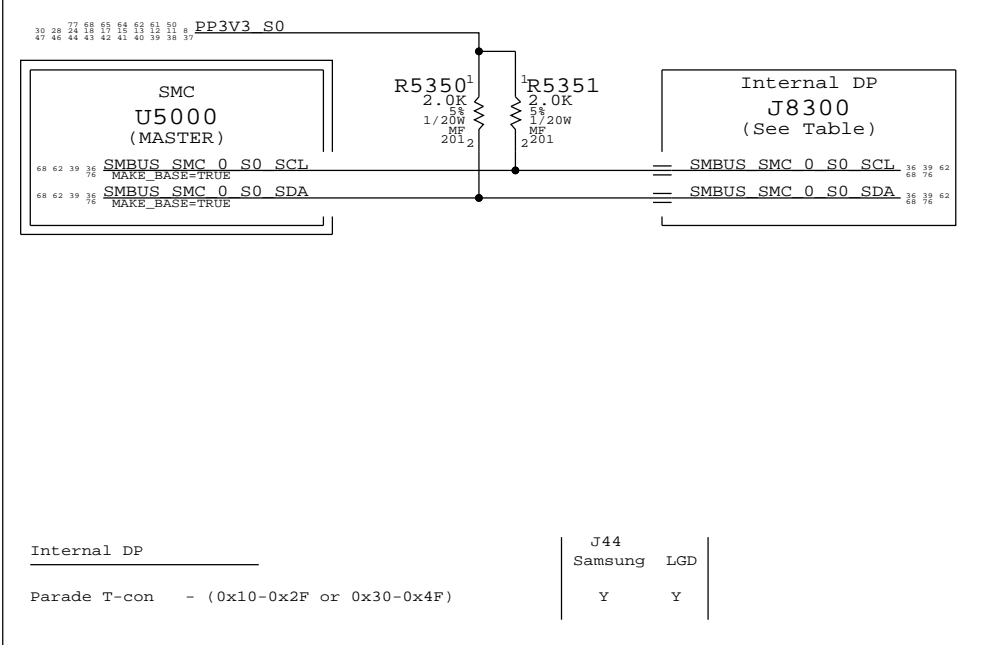


SYNC MASTER=J44		SYNC DATE=08/12/2013	
SMBus Connections			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	53 OF 120
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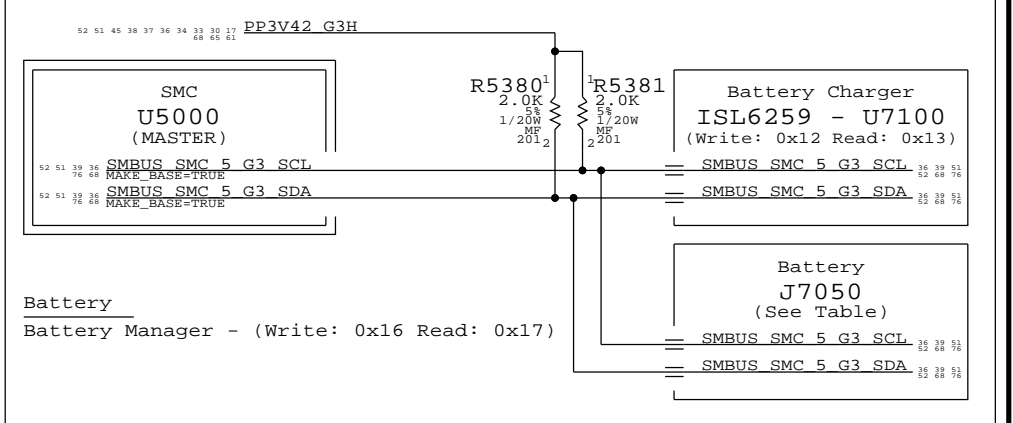
LYNX POINT LP S0 "SMBus 0" Connections



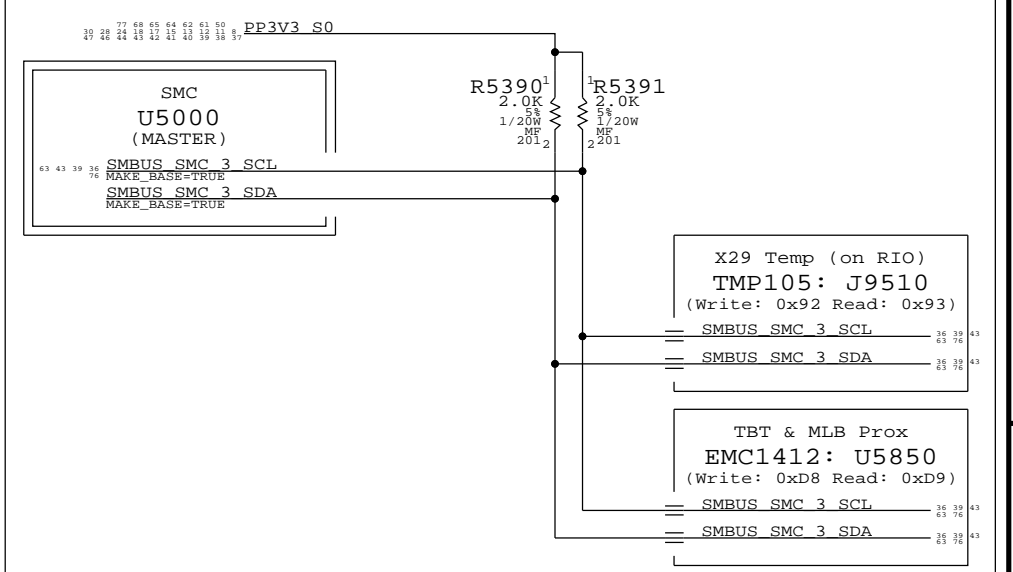
SMC SMBus "0" S0 Connections



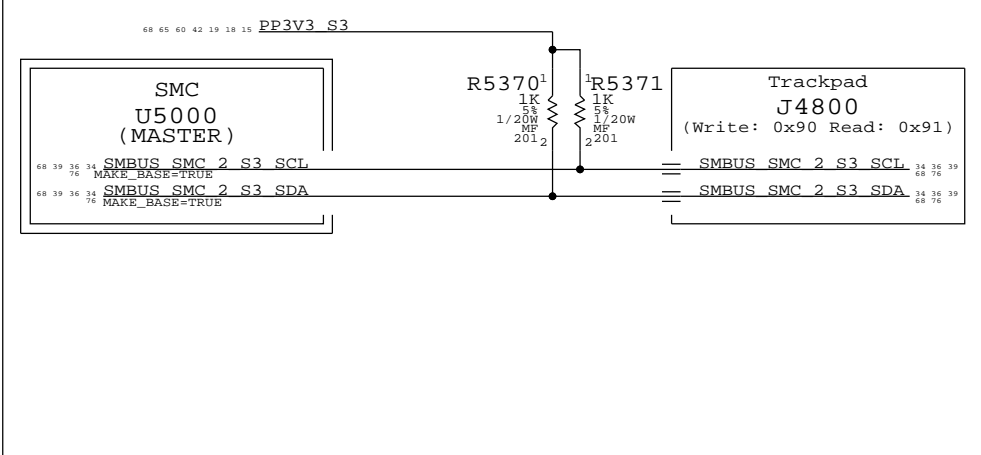
SMC SMBus "5" G3H Connections



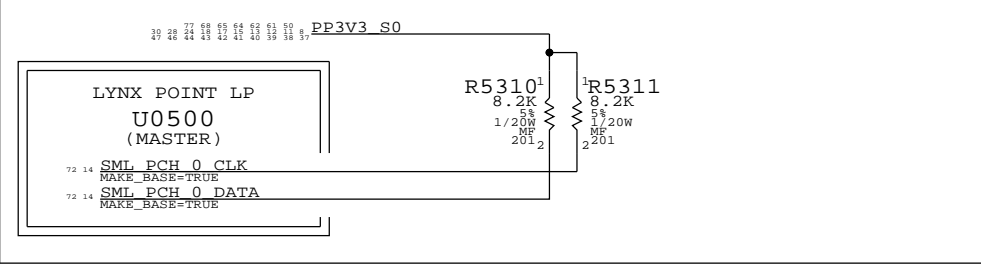
SMC SMBus "3" S0 Connections



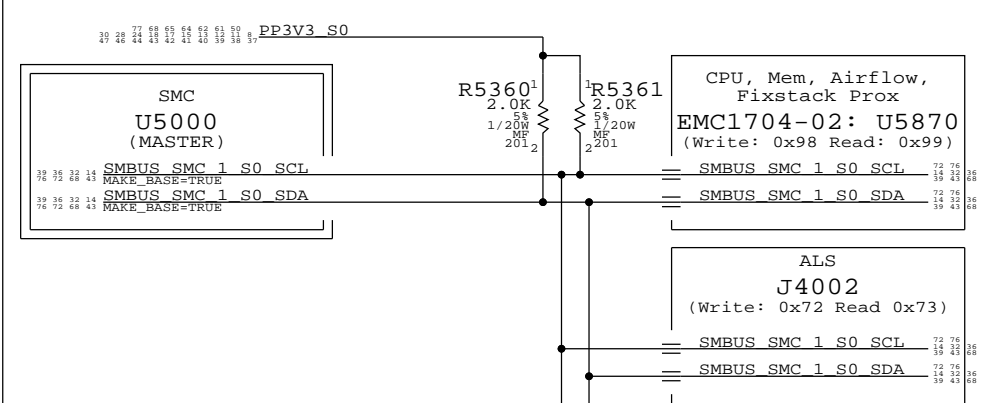
SMC SMBus "2" S3 Connections



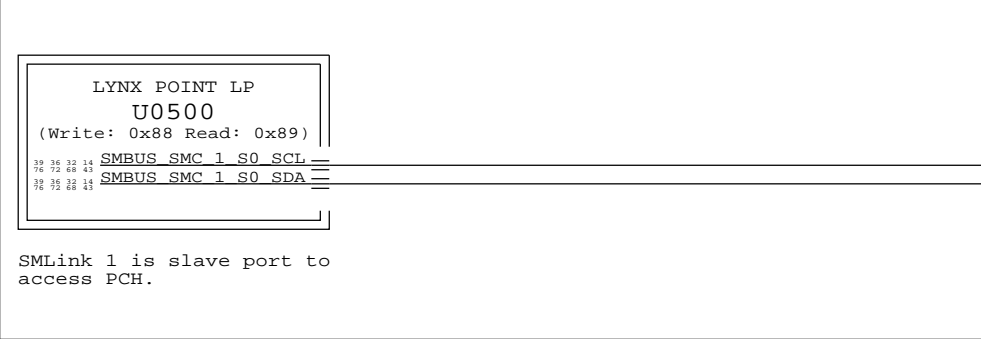
LYNX POINT LP S0 "SMLink 0" Connections



SMC SMBus "1" S0 Connections

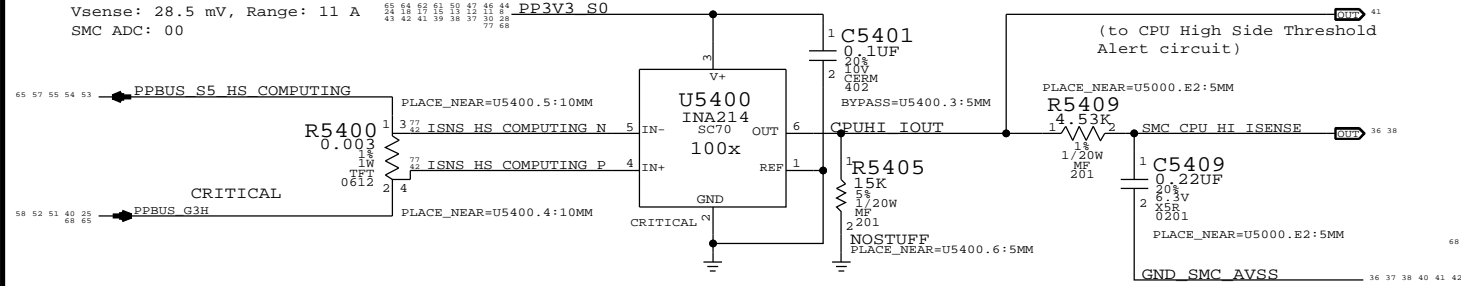


LYNX POINT LP S0 "SMLink 1" Connections



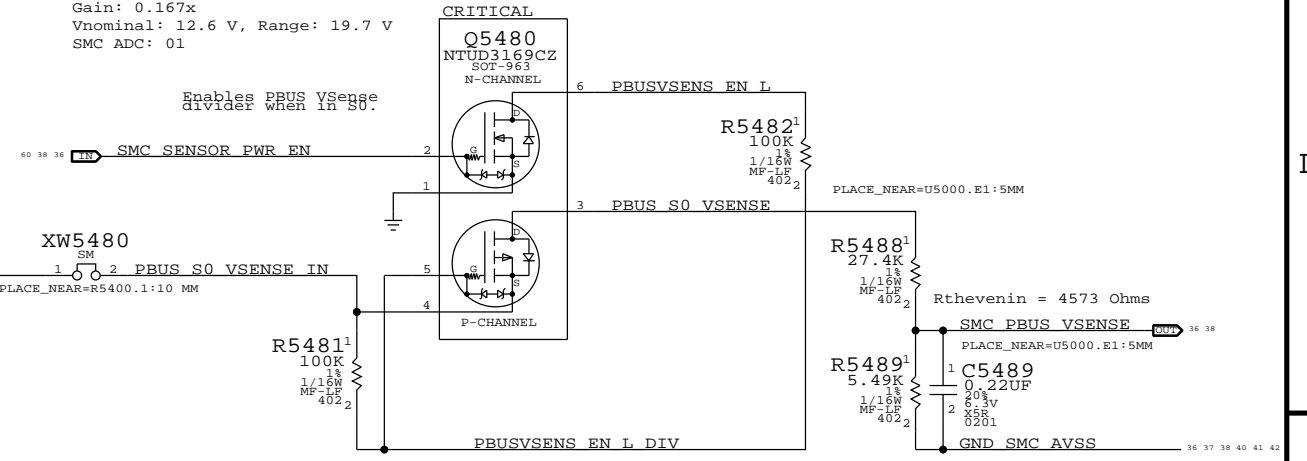
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 9.5 A
 Rsense: 0.003 (R5400)
 Vsense: 28.5 mV, Range: 11 A
 SMC ADC: 00



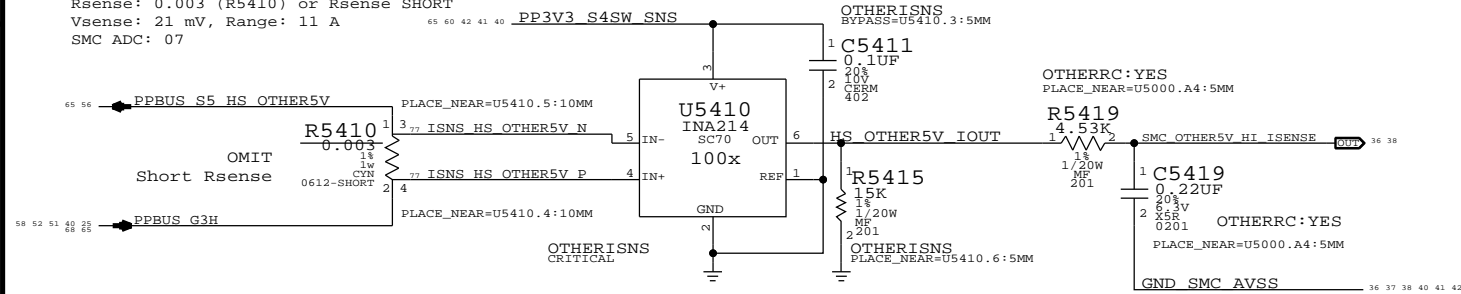
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
 Vnominal: 12.6 V, Range: 19.7 V
 SMC ADC: 01



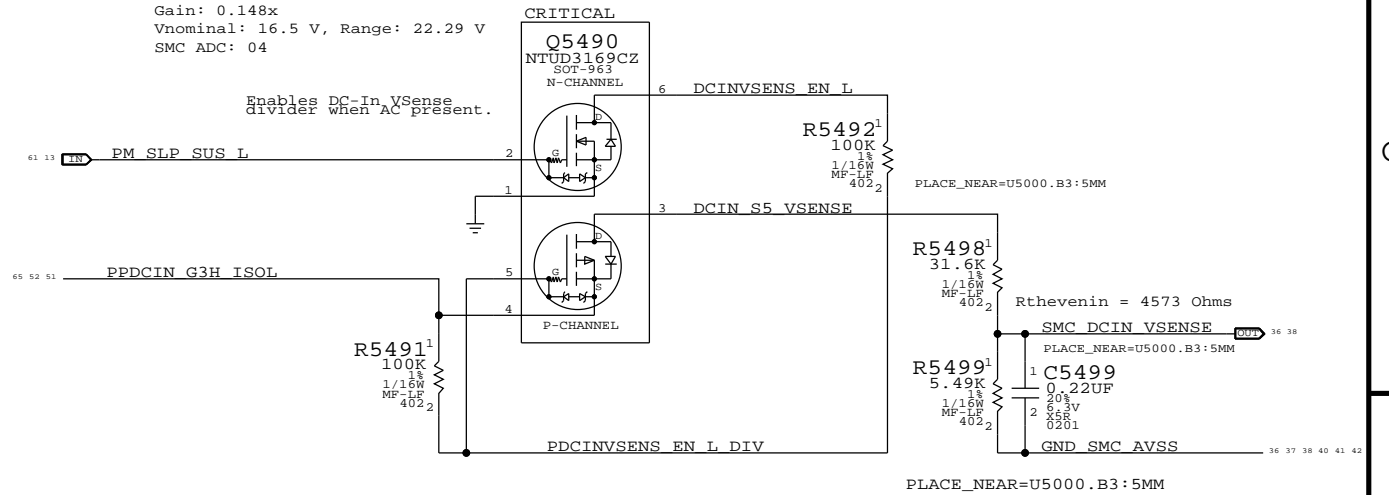
OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 7 A
 Rsense: 0.003 (R5410) or Rsense SHORT
 Vsense: 21 mV, Range: 11 A
 SMC ADC: 07



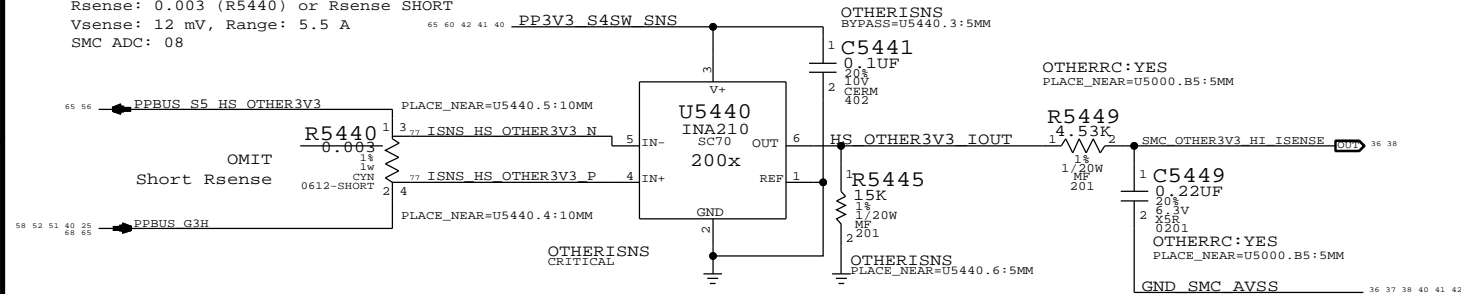
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
 Vnominal: 16.5 V, Range: 22.29 V
 SMC ADC: 04



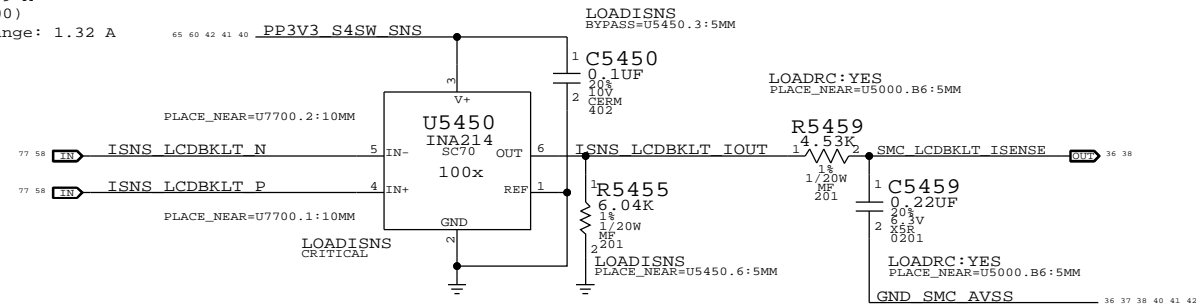
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A
 Rsense: 0.003 (R5440) or Rsense SHORT
 Vsense: 12 mV, Range: 5.5 A
 SMC ADC: 08



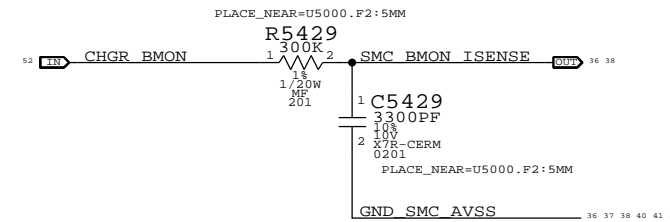
LCD Backlight Current Sense (IBLC)

Gain: 100x, EDP: 0.9 A
 Rsense: 0.025 (R7700)
 Vsense: 22.5 mV, Range: 1.32 A
 SMC AD: 10



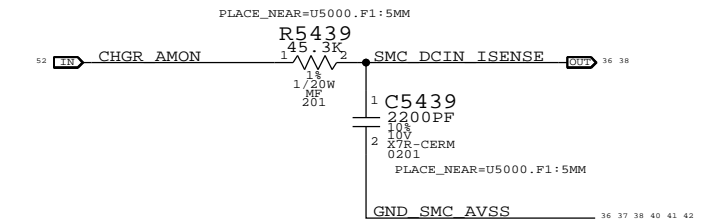
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
 Rsense: 0.005 (R7150)
 SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
 Rsense: 0.020 (R7120)
 SMC ADC: 03



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449	CRITICAL	OTHERRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO

SYNC MASTER=J44 SYNC DATE=08/12/2013

Power Sensors: High Side

Apple Inc.

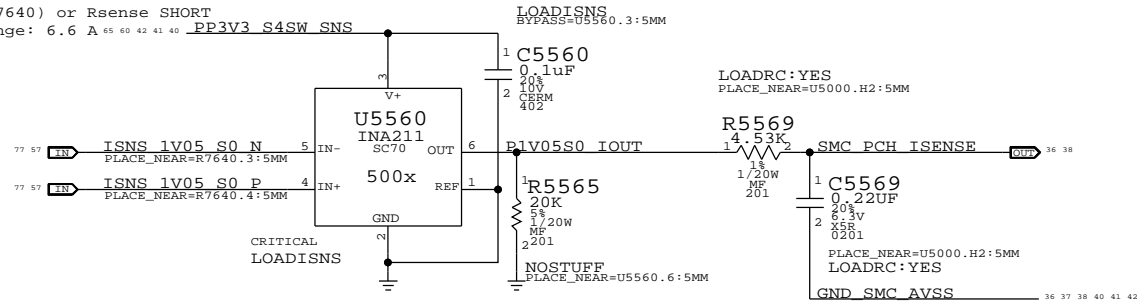
Apple logo

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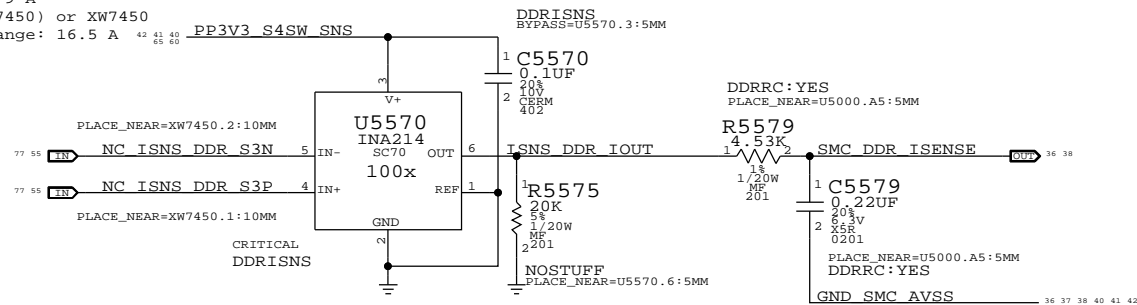
PCH 1.05V Current Sense (IC1C)

Gain: 500x, EDP: 5 A
 Rsense: 0.001 (R7640) or Rsense SHORT
 Vsense: 5 mV, Range: 6.6 A
 SMC ADC: 19



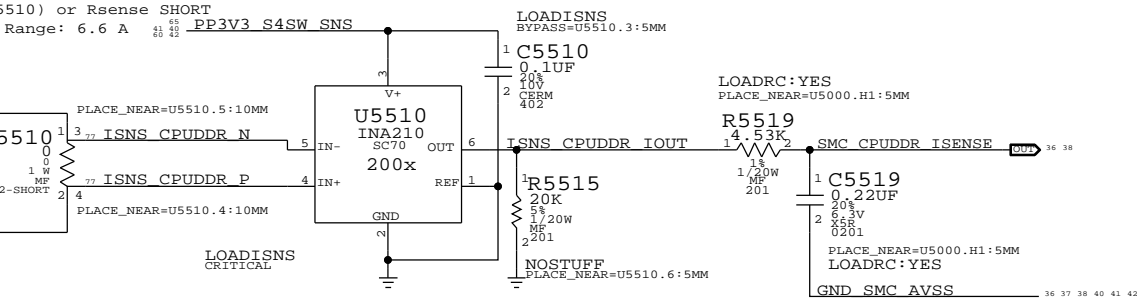
DDR 1.35V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9 A
 Rsense: 0.002 (R7450) or XW7450
 Vsense: 21 mV, Range: 16.5 A
 SMC ADC: 09



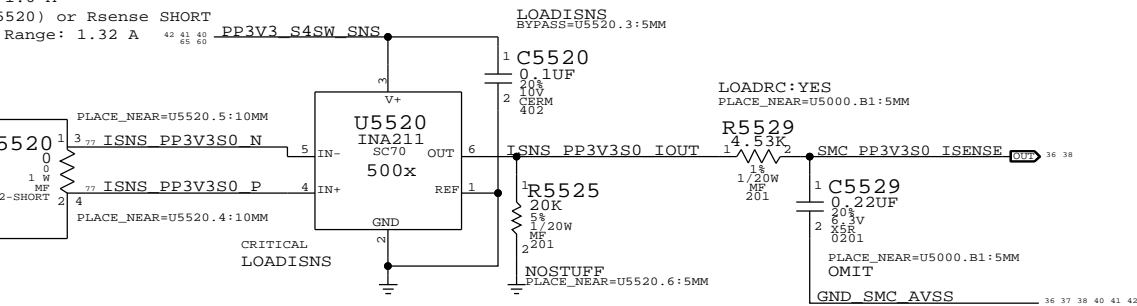
CPU DDR 1.35V S3 (CPU Only) Current Sense (IM1C)

Gain: 200x, EDP: 2.5 A
 Rsense: 0.005 (R5510) or Rsense SHORT
 Vsense: 12.5 mV, Range: 6.6 A
 SMC ADC: 18



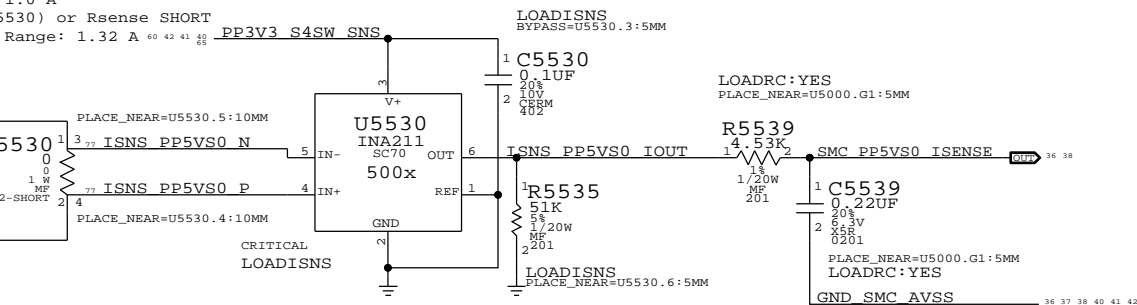
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.0 A
 Rsense: 0.005 (R5520) or Rsense SHORT
 Vsense: 21.5 mV, Range: 1.32 A
 SMC ADC: 14



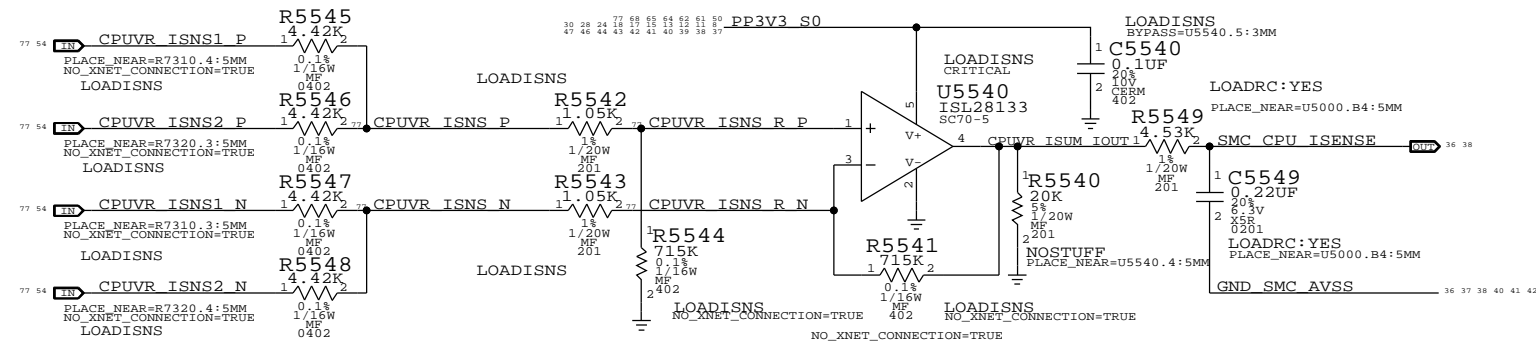
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
 Rsense: 0.005 (R5530) or Rsense SHORT
 Vsense: 23.5 mV, Range: 1.32 A
 SMC ADC: 17



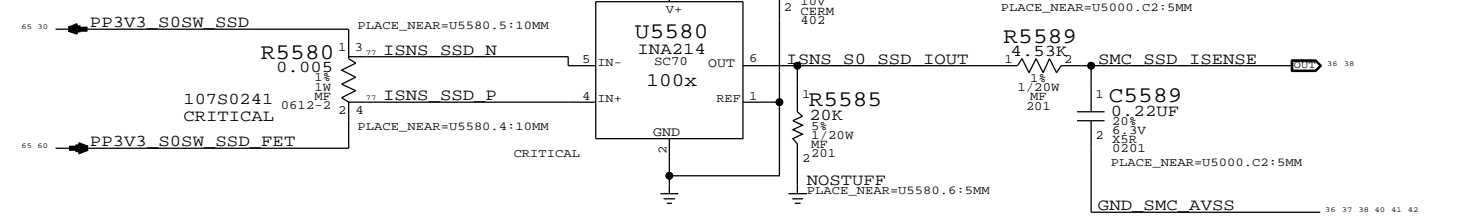
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
 Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
 Vsense: 15 mV, Range: 40.12 A
 SMC ADC: 06



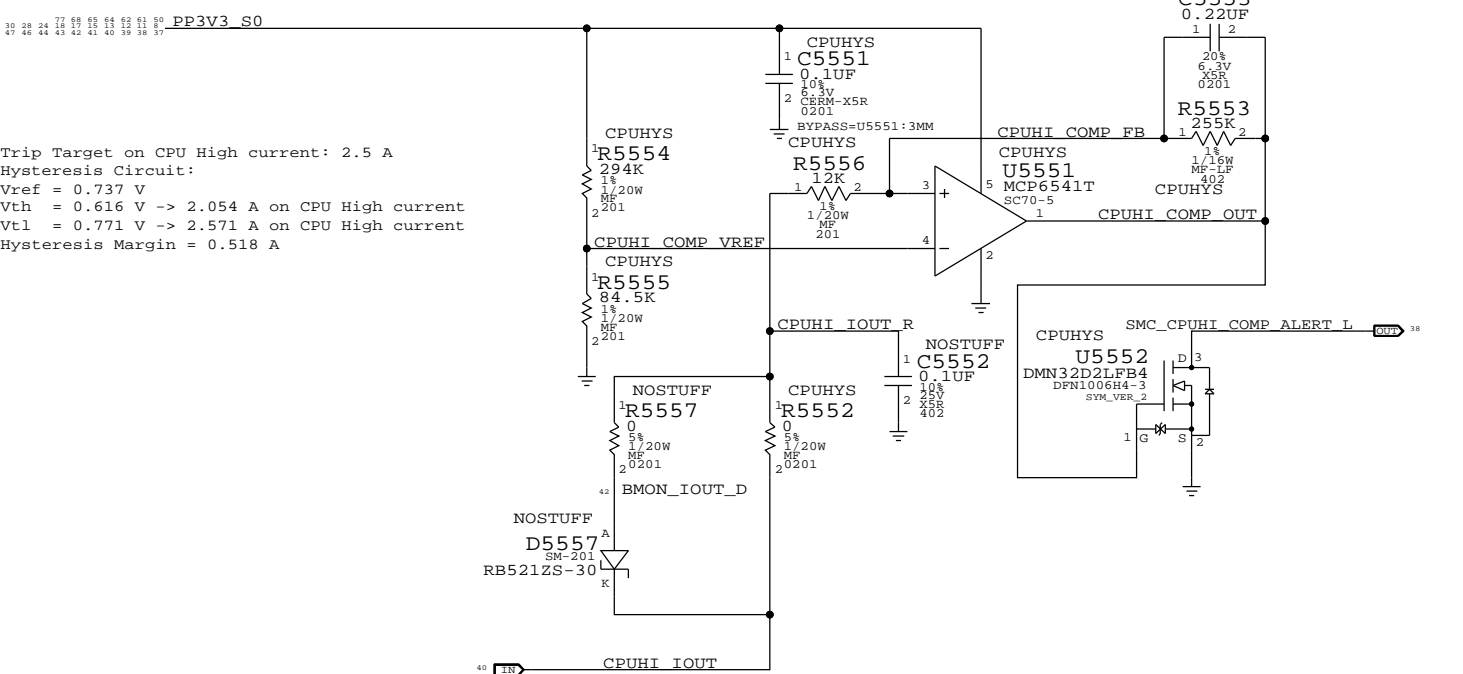
SSD Current Sense (ISDC)

Gain: 100x, EDP: 5 A (16.5 W)
 Rsense: 0.005 (R5580)
 Vsense: 25 mV, Range: 6.6 A
 SMC ADC: 13



CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
 Rsense: 0.003 (R5400)



Trip Target on CPU High current: 2.5 A
 Hysteresis Circuit:
 Vref = 0.737 V
 Vth = 0.616 V -> 2.054 A on CPU High current
 Vtl = 0.771 V -> 2.571 A on CPU High current
 Hysteresis Margin = 0.518 A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

SYNC MASTER=J44 SYNC DATE=08/12/2013

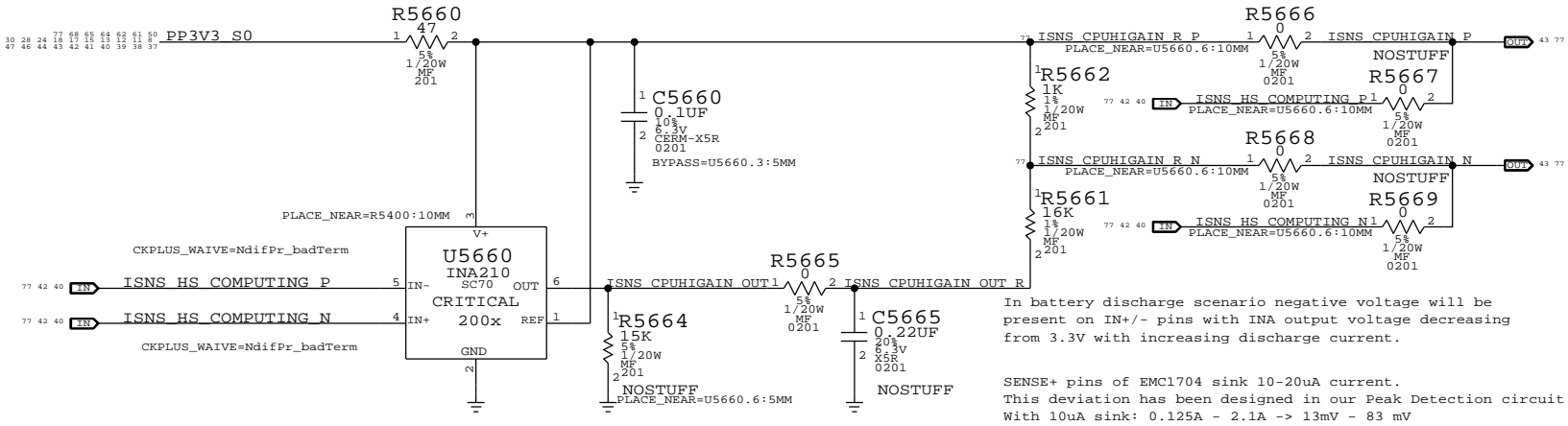
Power Sensors: Load Side

Apple Inc.

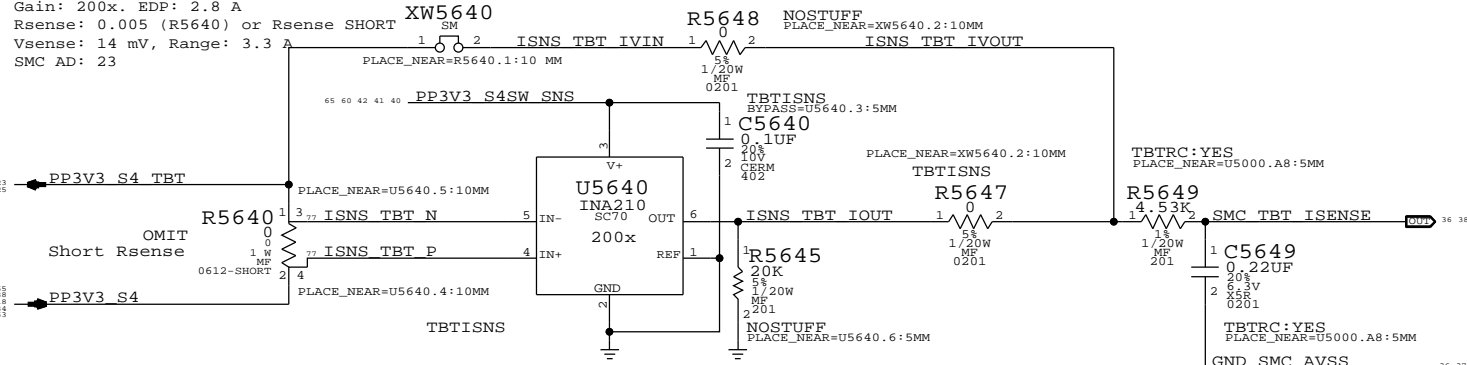
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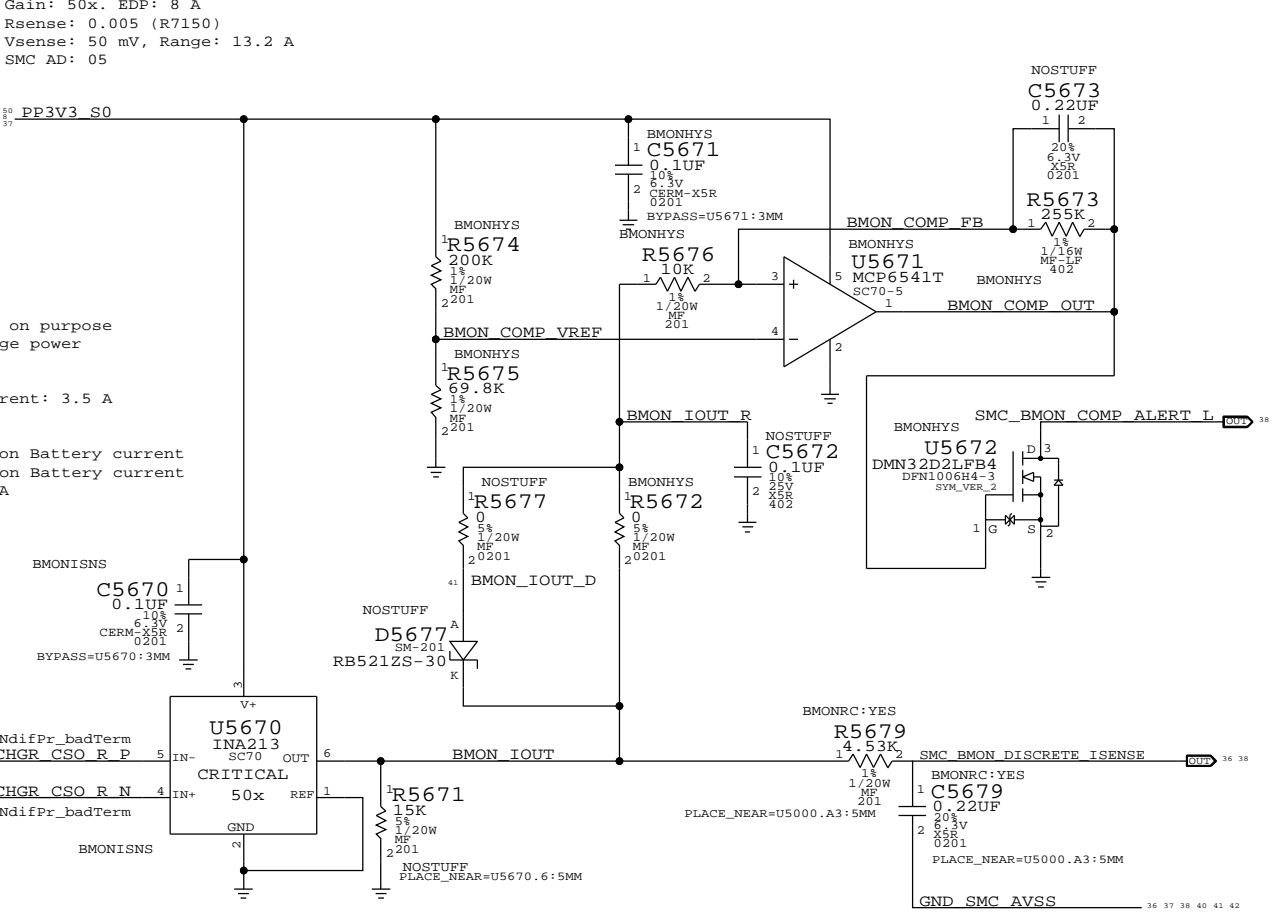
CPU High Side (IC0R) Peak Detection Support



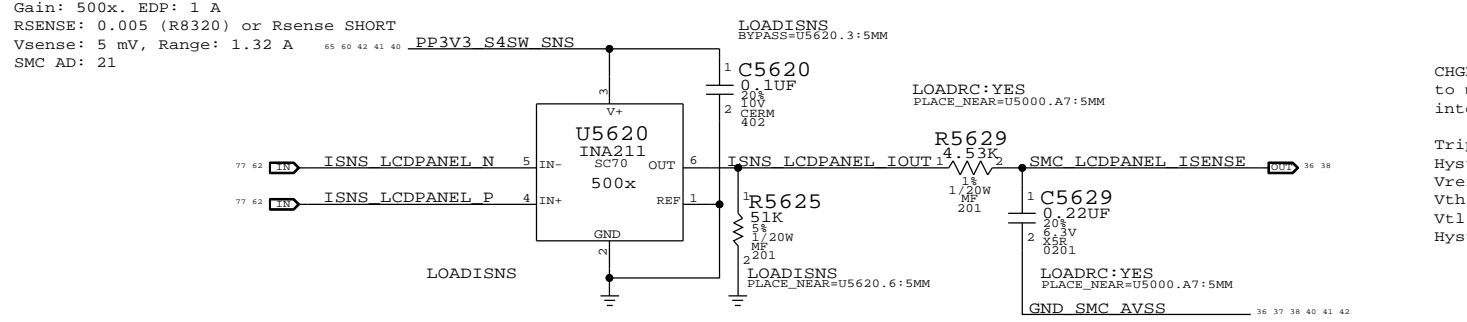
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)



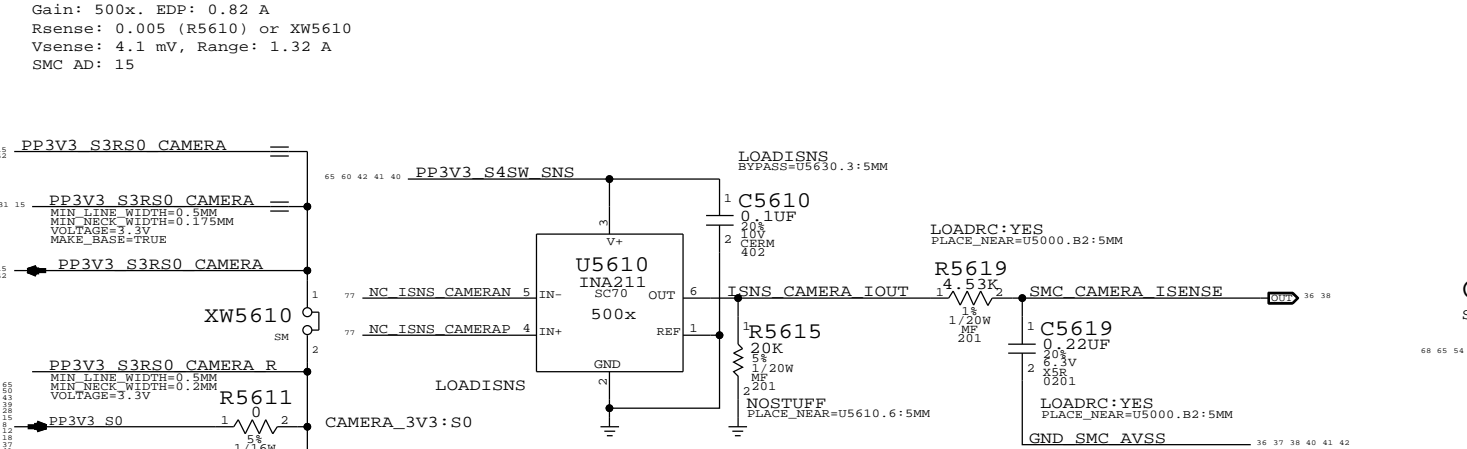
Battery BMON Discrete Current Sense (IP0R) & Threshold Alert



LCD Panel Current Sense (ILDC)

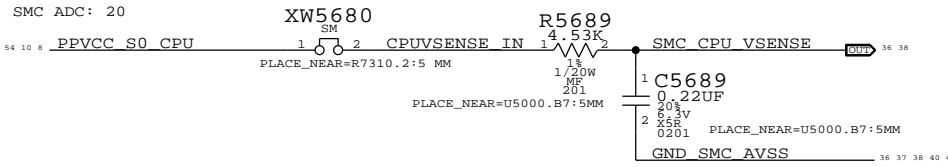


Camera (S2 Controller) Current Sense (ICMC)

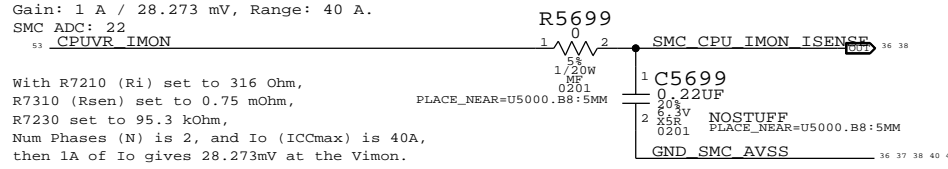


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		

CPU Core Voltage Sense (VC0C)



CPU Core IMON Current Sense (IC2C)



SYNC MASTER=144 SYNC DATE=08/12/2013

Power Sensors: Extended

Apple Inc.

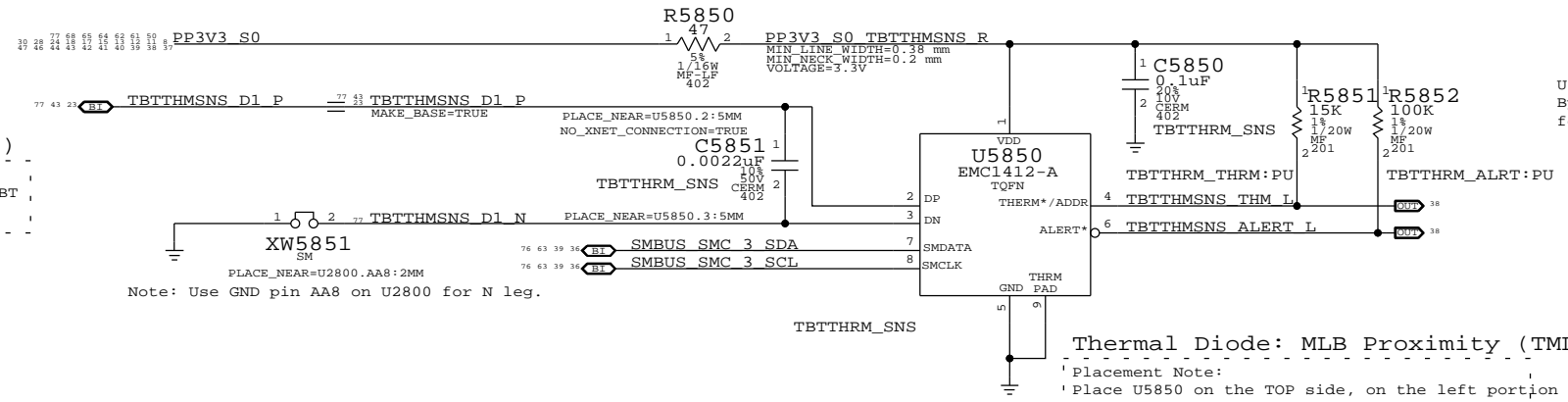
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**Thermal Sensor A:
Thunderbolt Die, MLB Proximity**

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (THSP)
 Placement Note:
 The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.



U5850 I2C Address:
 By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

Thermal Diode: MLB Proximity (TMLB)
 Placement Note:
 Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

**Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity**

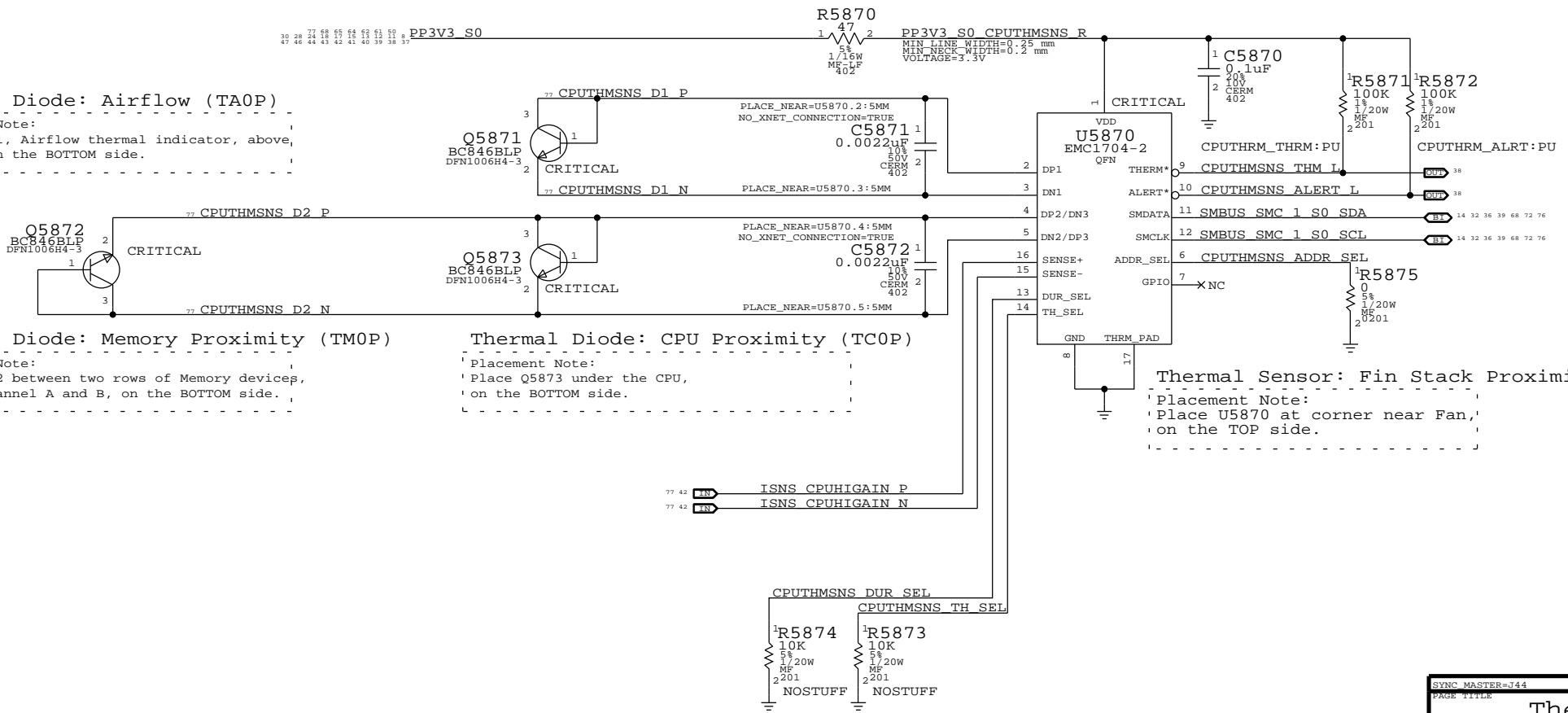
I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: Airflow (TA0P)
 Placement Note:
 Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)
 Placement Note:
 Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Diode: CPU Proximity (TC0P)
 Placement Note:
 Place Q5873 under the CPU, on the BOTTOM side.

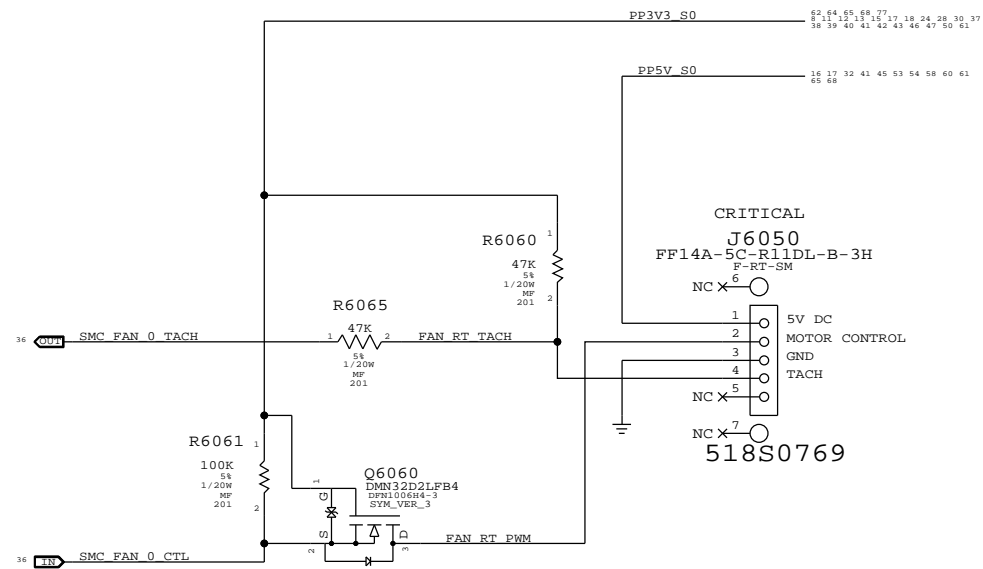
Thermal Sensor: Fin Stack Proximity (Th1H)
 Placement Note:
 Place U5870 at corner near Fan, on the TOP side.



SYNC MASTER=144		SYNC DATE=08/12/2013	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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FAN CONNECTOR

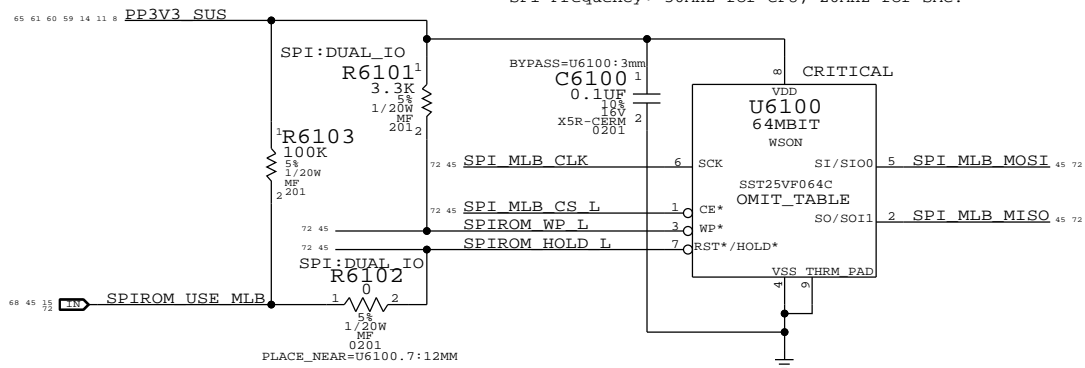
KEEP THE 5 PIN CONNECTOR FROM D1



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE: Fan			
DRAWING NUMBER: <SCH_NUM>		SIZE: D	
REVISION: <E4LABEL>		BRANCH: <BRANCH>	
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SPI ROM

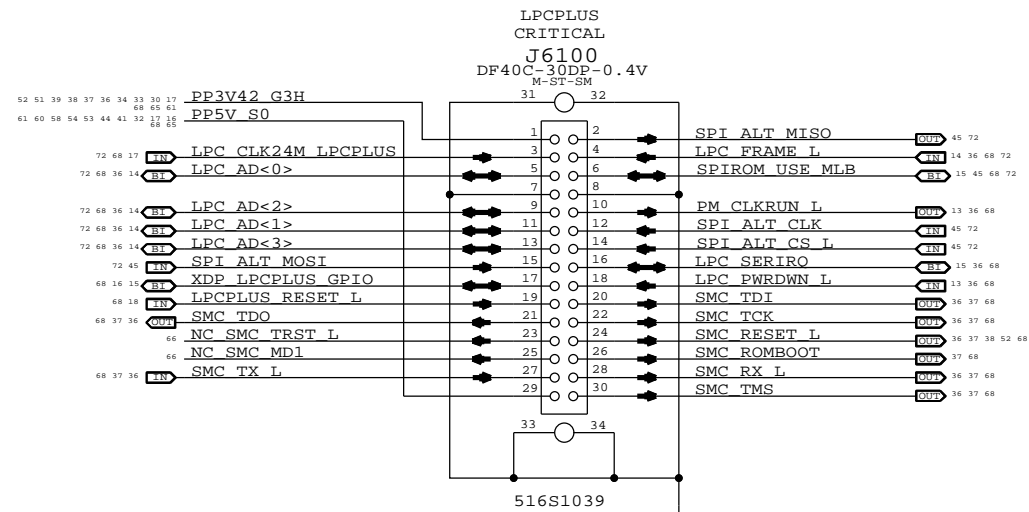
Dual-IO Mode (Mode 0 & 3) supported.
 SPI Frequency: 50MHz for CPU, 20MHz for SMC.



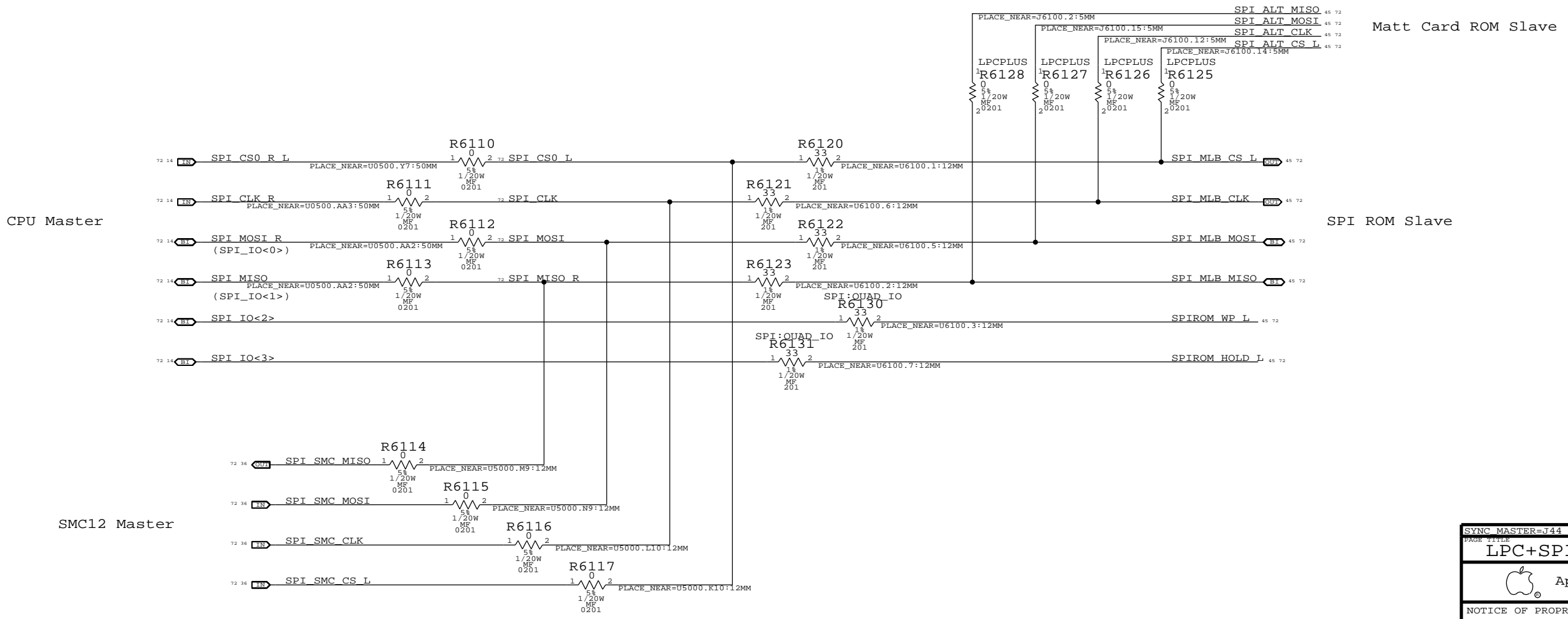
NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and Dual-IO modes.

NOTE: Not all ROM APNs currently used support Quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

LPC+SPI Connector (Matt Card Connector)



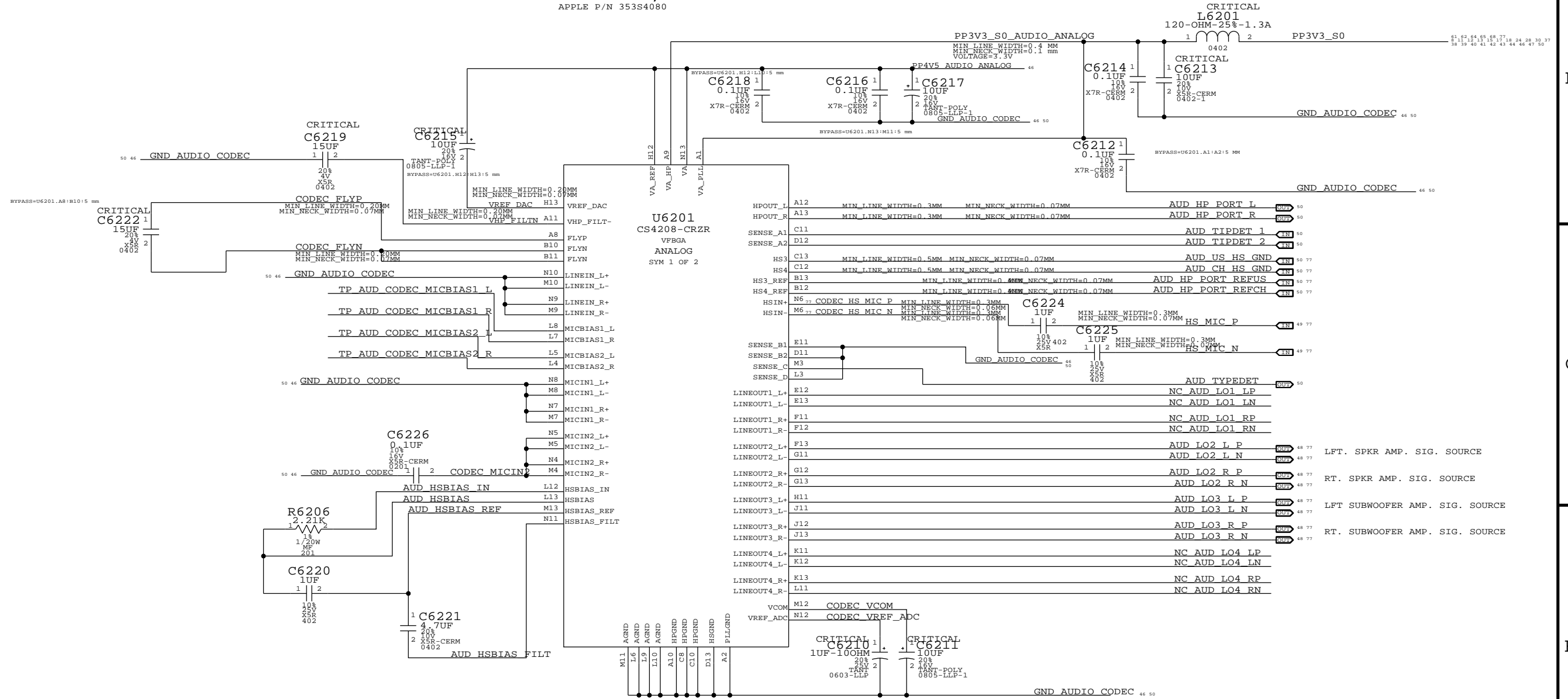
SPI Bus Series Termination



SYNC MASTER=J44		SYNC DATE=08/12/2013	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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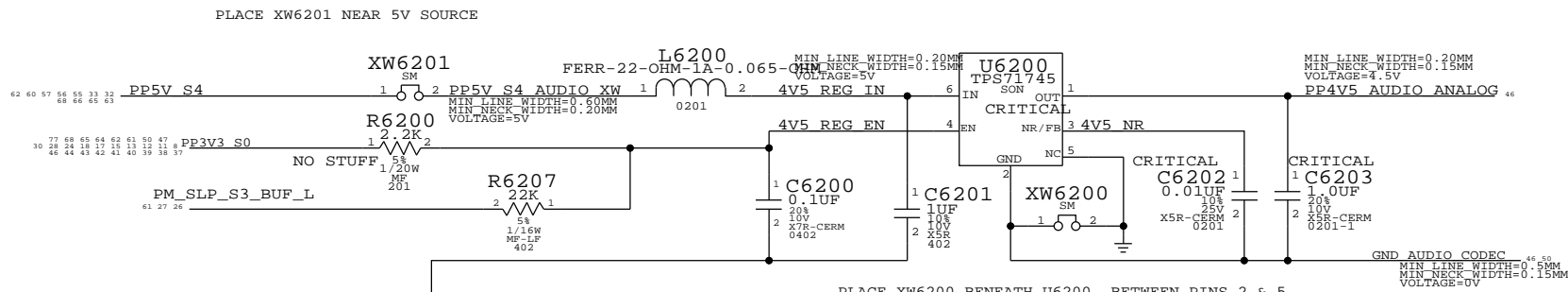
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



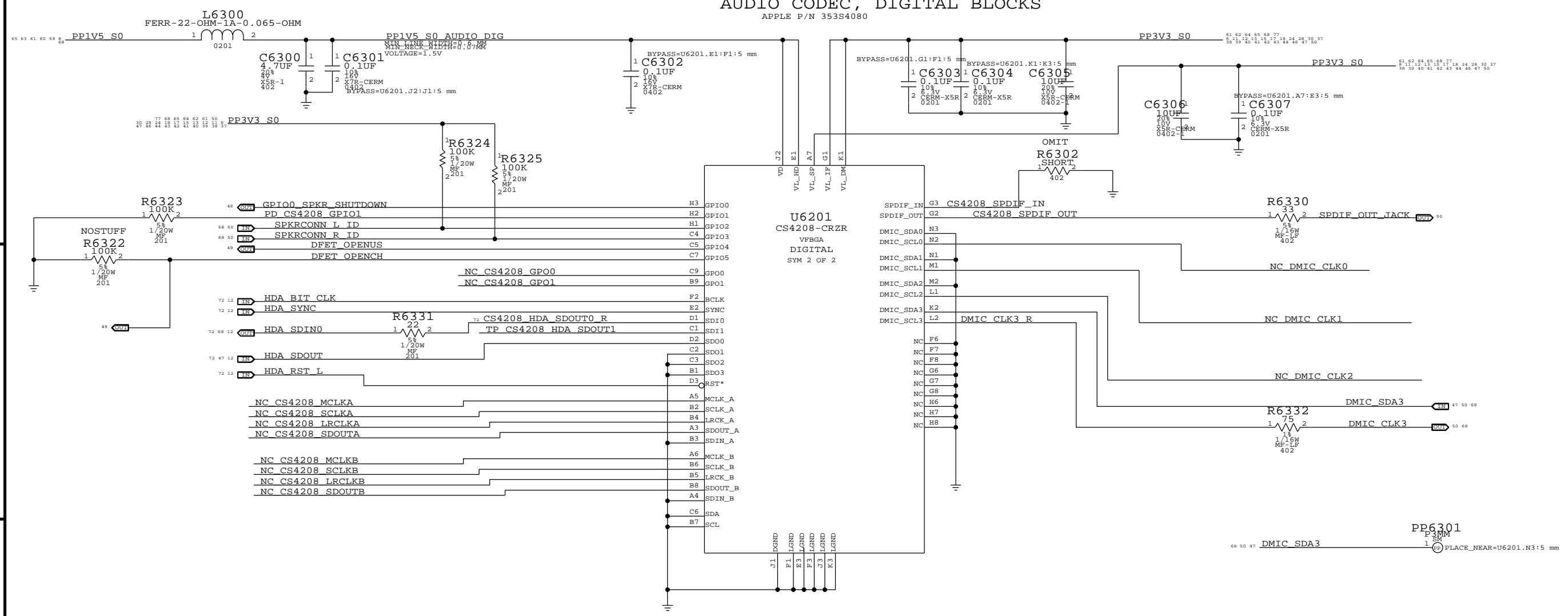
4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
AUDIO:CODEC, ANALOG		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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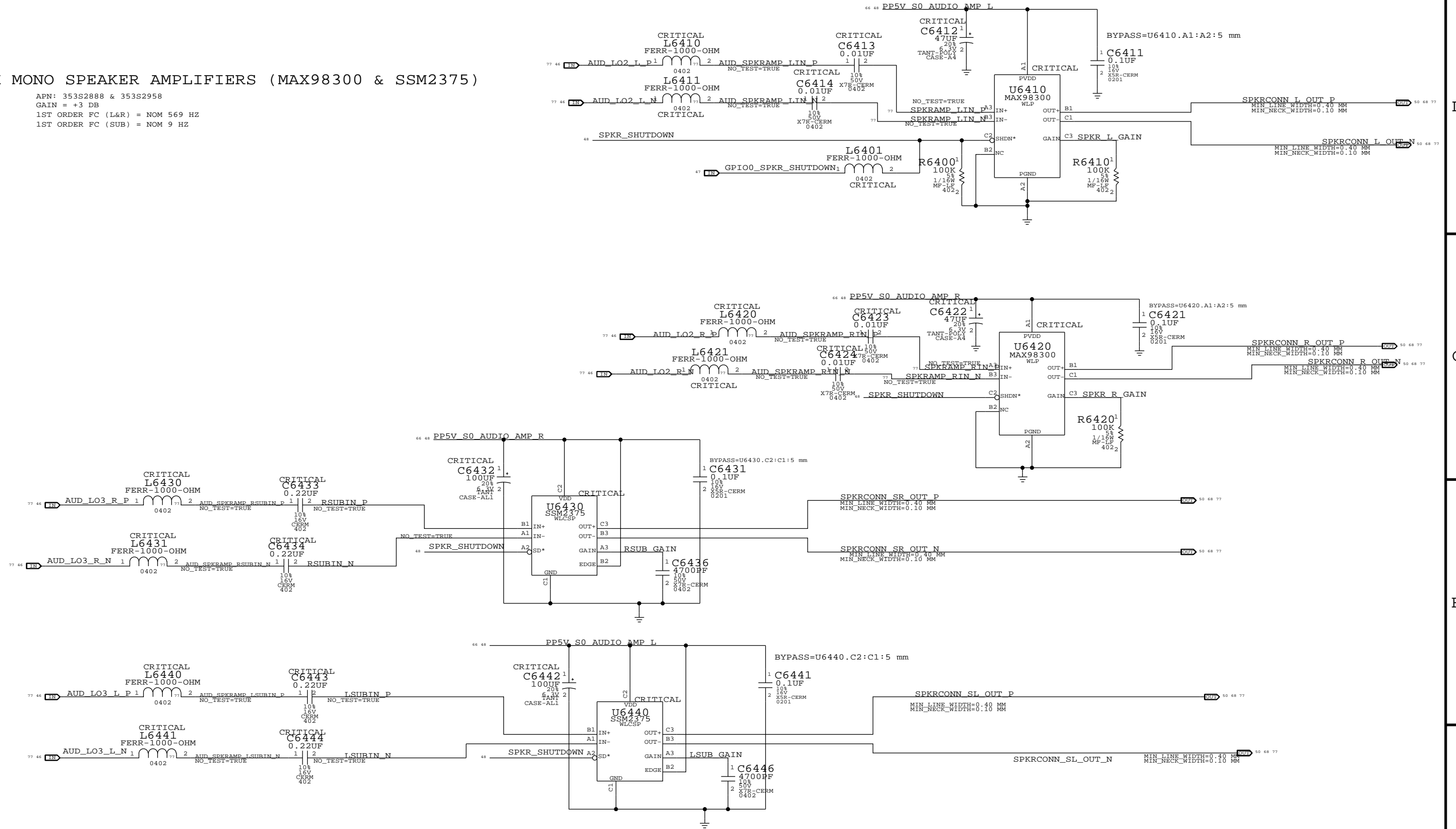
AUDIO CODEC, DIGITAL BLOCKS
APPLE P/N 353S4080



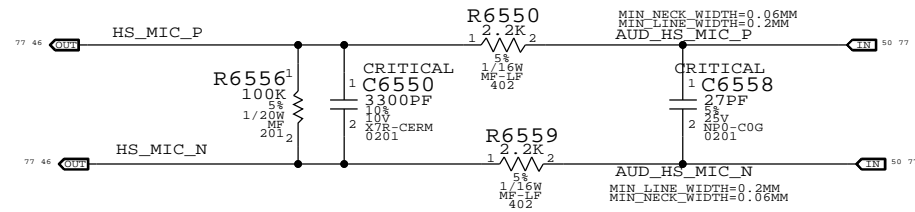
SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
AUDIO:CODEC, DIGITAL			
Apple Inc.		DRAWING NUMBER	SIZE
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4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

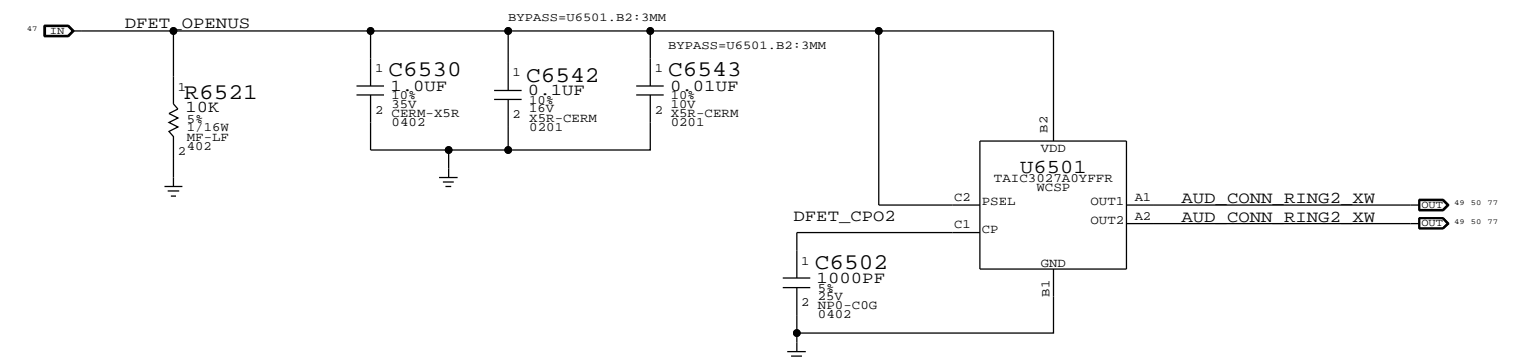
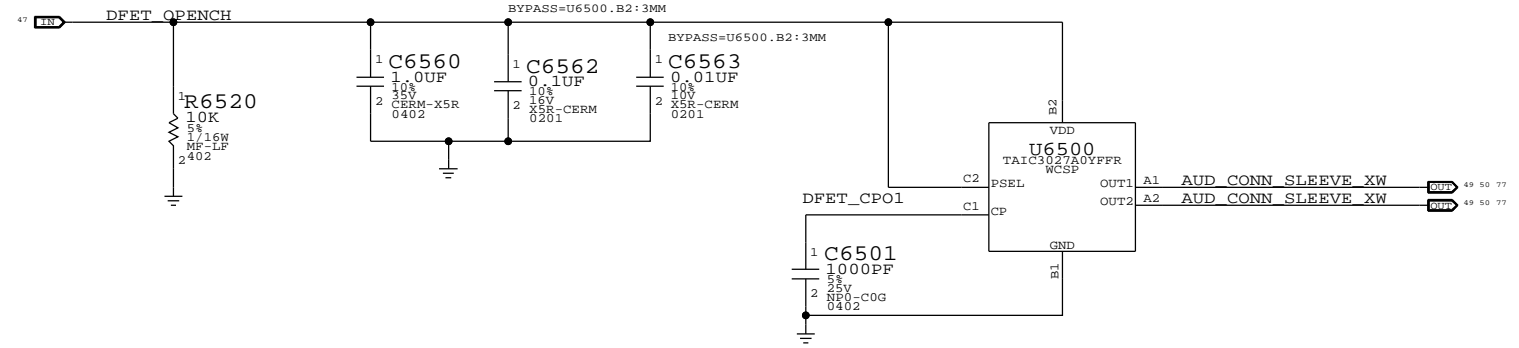
APN: 353S2888 & 353S2958
 GAIN = +3 DB
 1ST ORDER FC (L&R) = NOM 569 HZ
 1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=144		SYNC DATE=08/12/2013	
AUDIO: SPEAKER AMP			
		DRAWING NUMBER	SIZE
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R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)



SYNC MASTER=144		SYNC DATE=08/12/2013	
AUDIO: JACK			
Apple Inc.		DRAWING NUMBER	SIZE
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		<BRANCH>	
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETS OPEN

SPEAKER CONNECTOR

HP=80HZ
APN: 518S0672

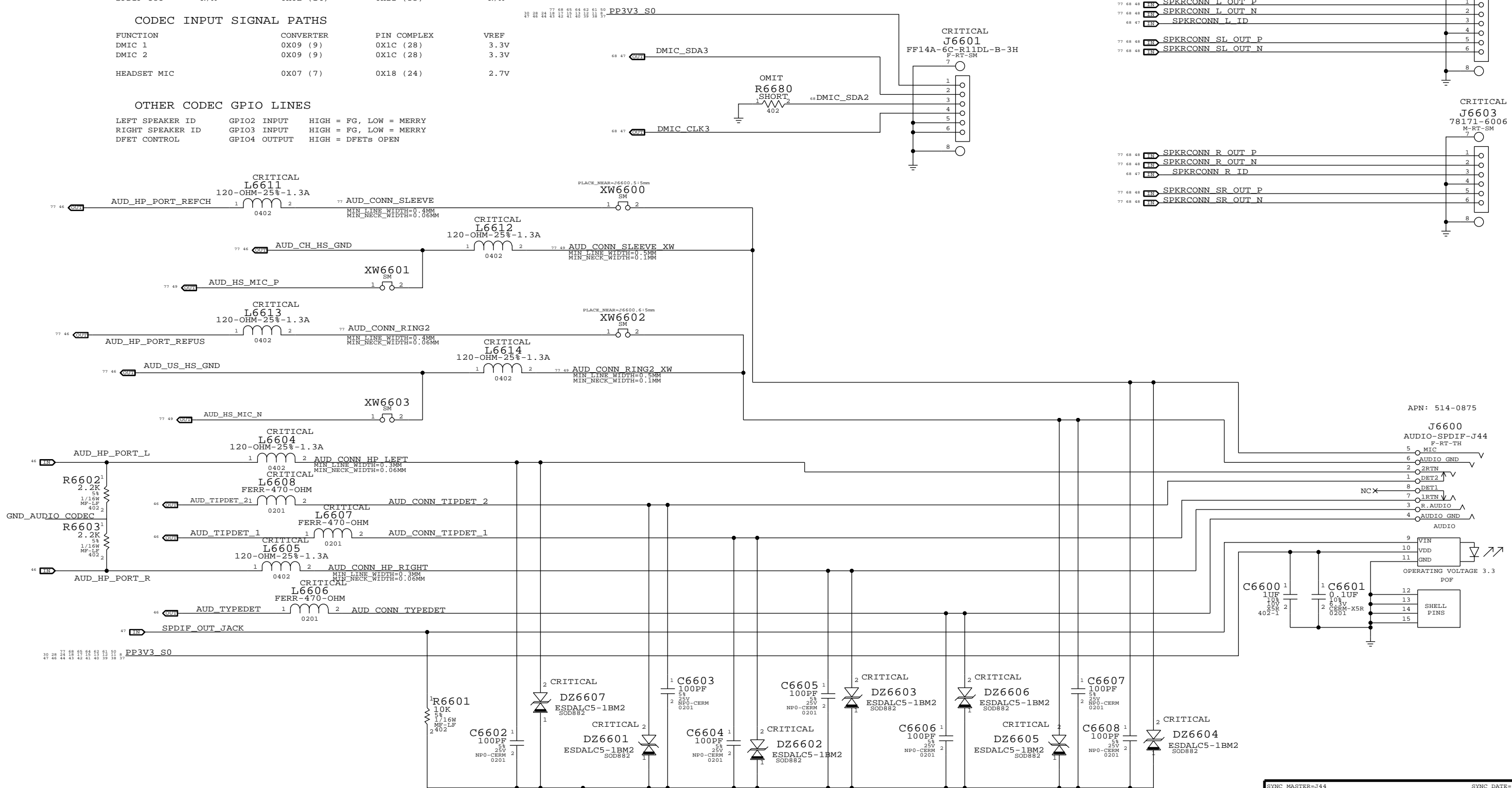
CRITICAL
J6602
78171-6006
M-RT-SM

2-MIC CONNECTOR

APN: 518S0818

CRITICAL
J6601
FF14A-6C-R11DL-B-3H
F-RT-SM

CRITICAL
J6603
78171-6006
M-RT-SM



SYNC MASTER=144 SYNC DATE=08/12/2013
PAGE TITLE

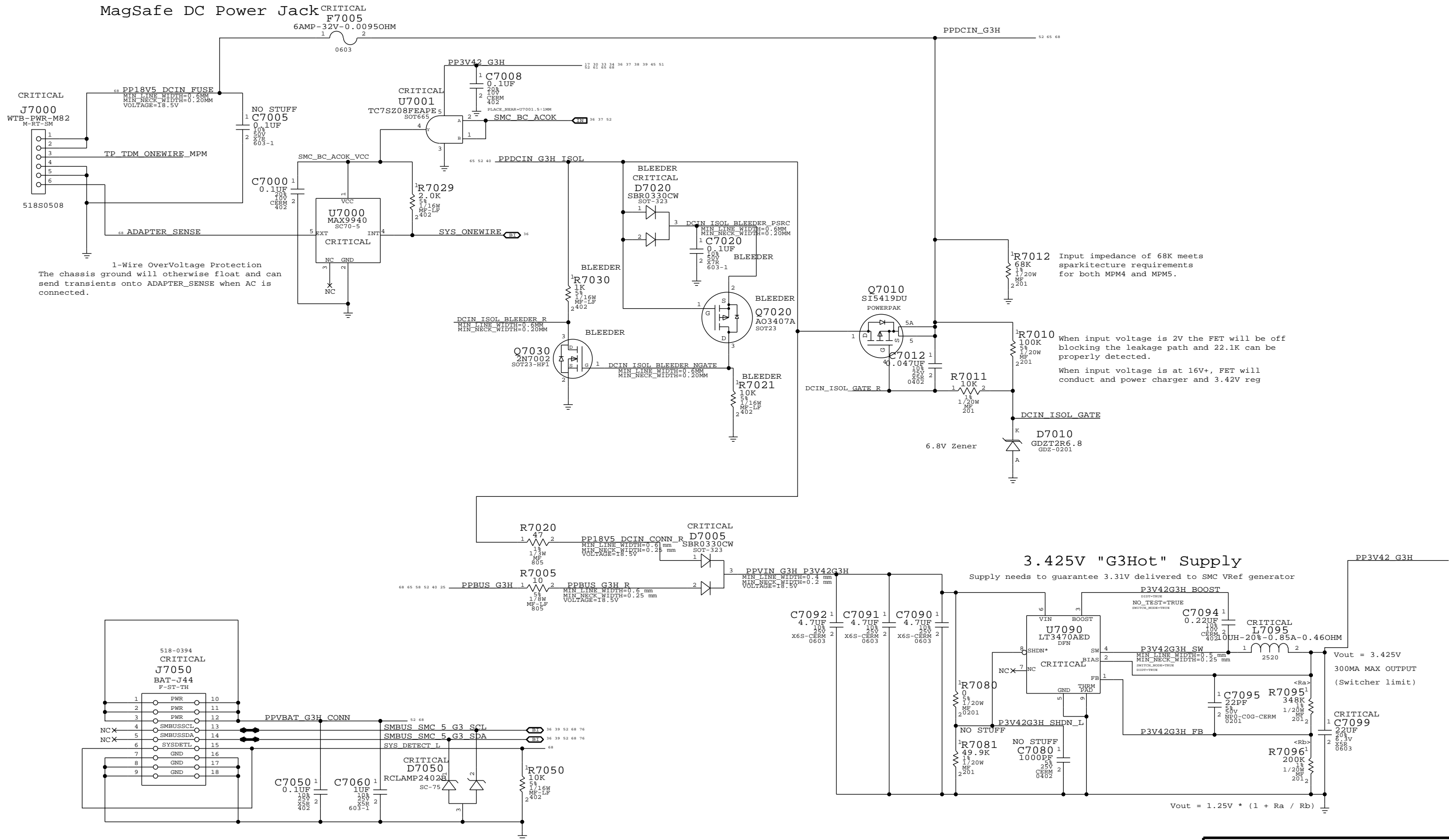
AUDIO: JACK TRANSLATORS

Apple Inc.

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MagSafe DC Power Jack



1-Wire OverVoltage Protection
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

Input impedance of 68K meets sparkitechure requirements for both MPM4 and MPM5.

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.
When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER <SCH_NUM> D
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Reverse-Current Protection

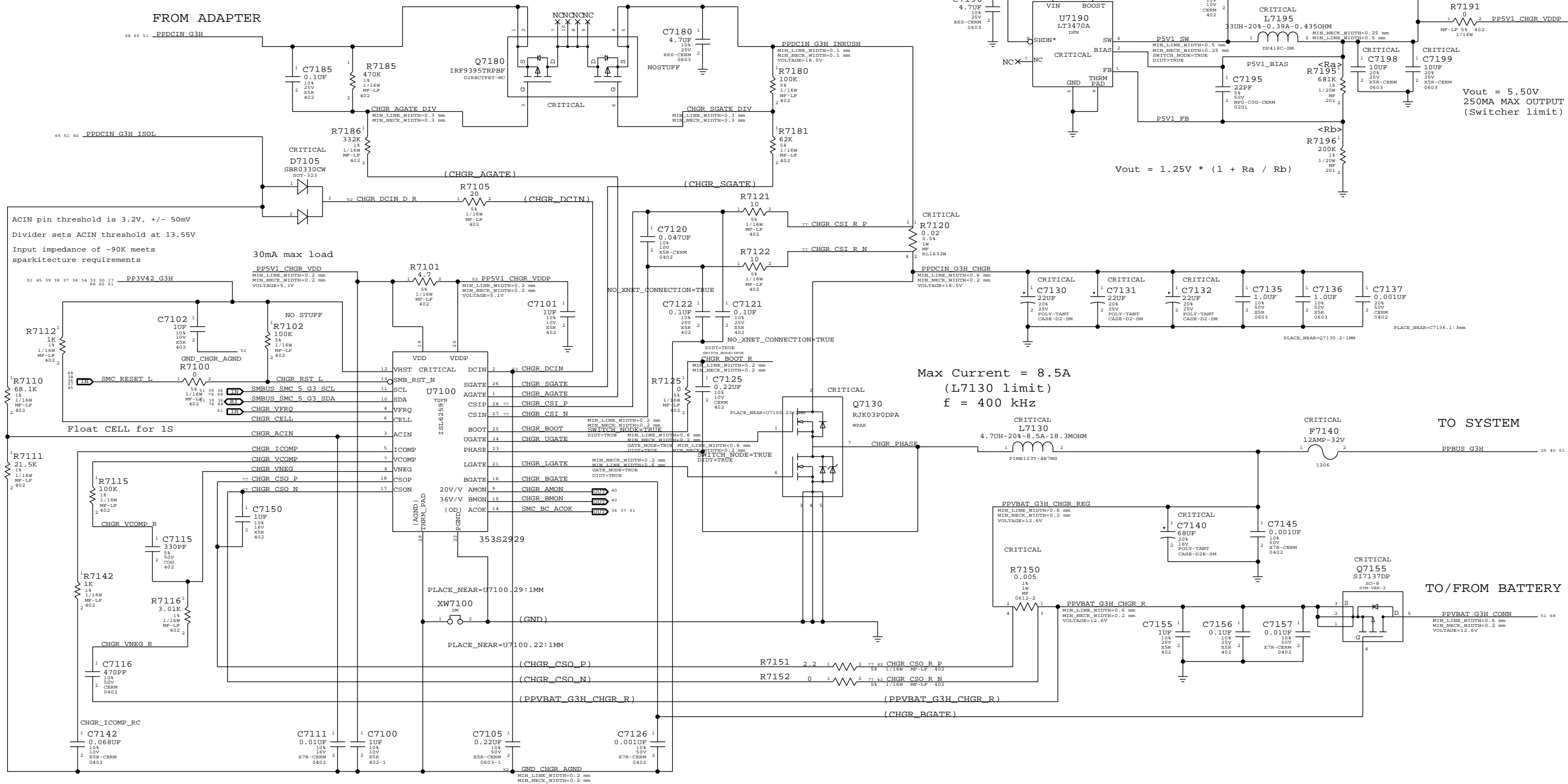
Inrush Limiter

For Exp Lot6 spec

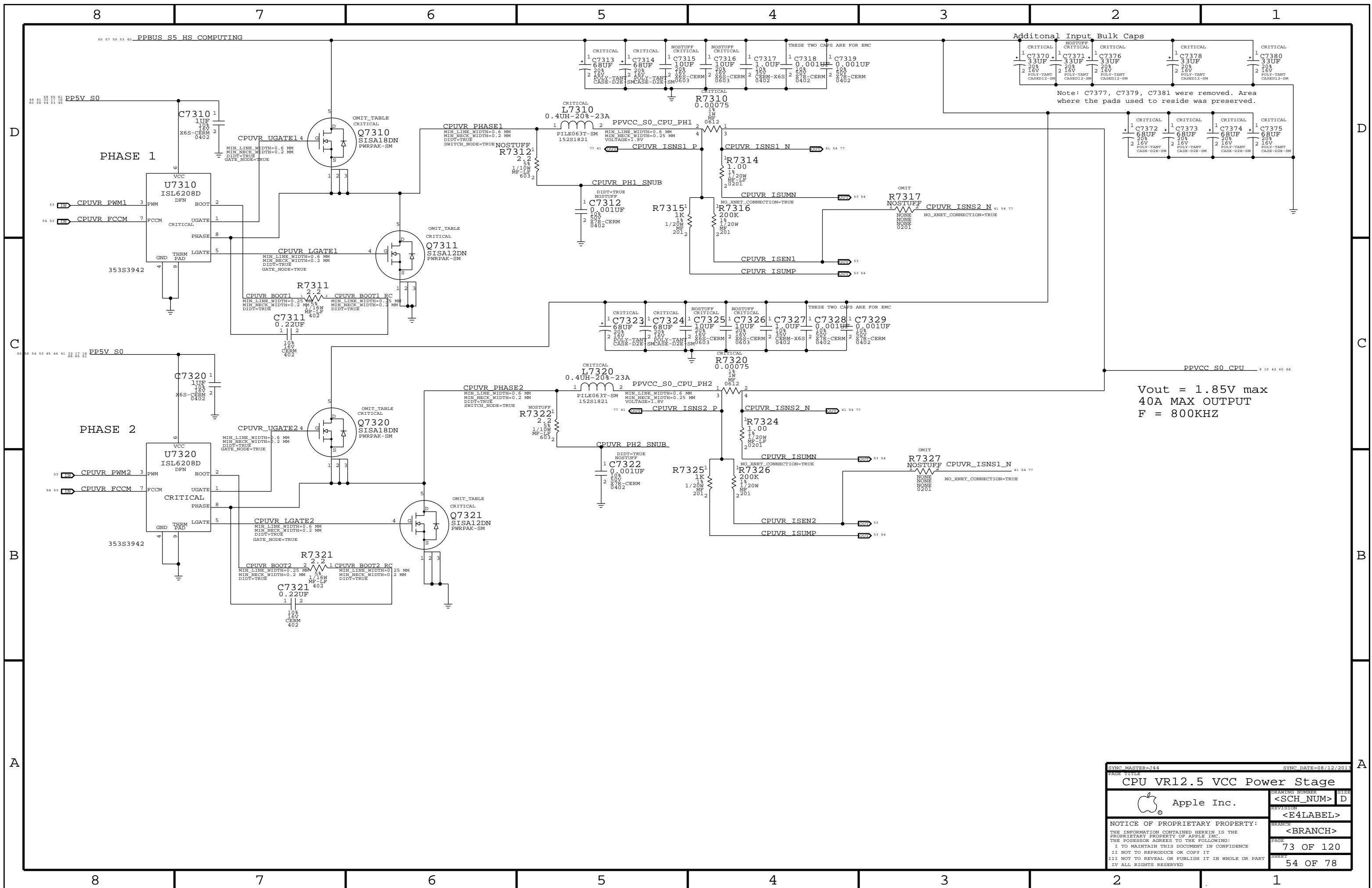
NOSTUFF

D
C
B
A

D
C
B
A



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	SIZE
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Additional Input Bulk Caps

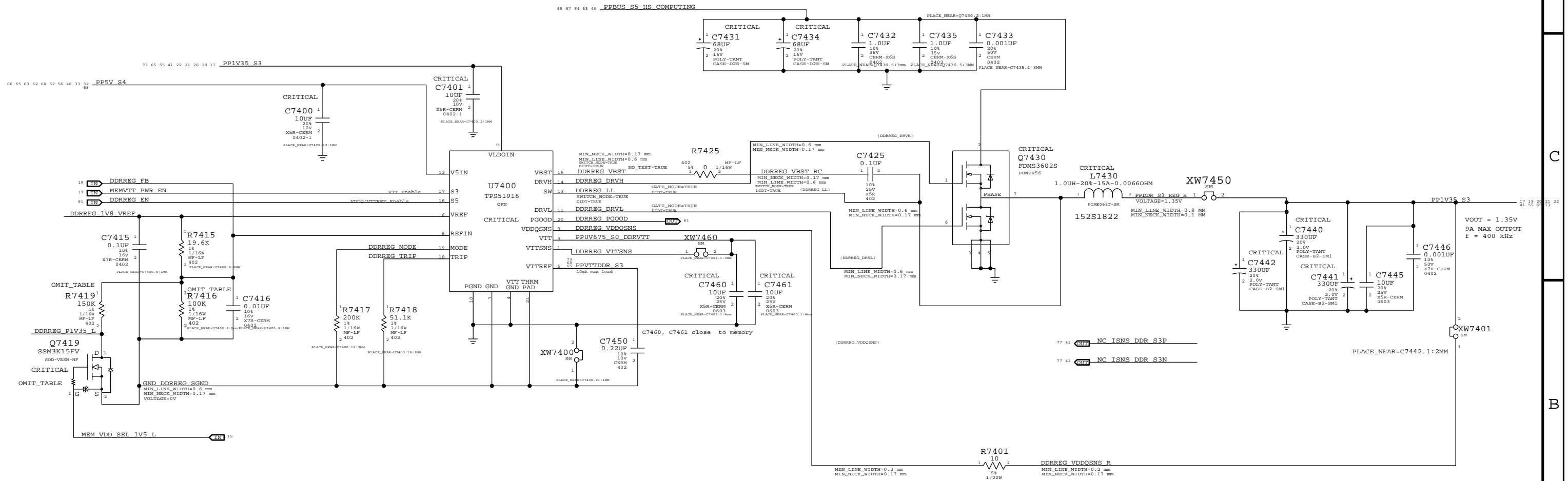
Note: C7377, C7379, C7381 were removed. Area where the pads used to reside was preserved.

C7372 68UF
C7373 68UF
C7374 68UF
C7375 68UF

Vout = 1.85V max
40A MAX OUTPUT
F = 800KHZ

SYNCH MASTER=144		SYNCH DATE=08/12/2013	
CPU VR12.5 VCC Power Stage			
Apple Inc.		DRAWING NUMBER	SIZE
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DDR3L (1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.00HM,SOT-723,HP	Q7419	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7419	CRITICAL	PPDDR:1V5

SYMC: WATERS-144
SYMC: DATE: 08/12/2015

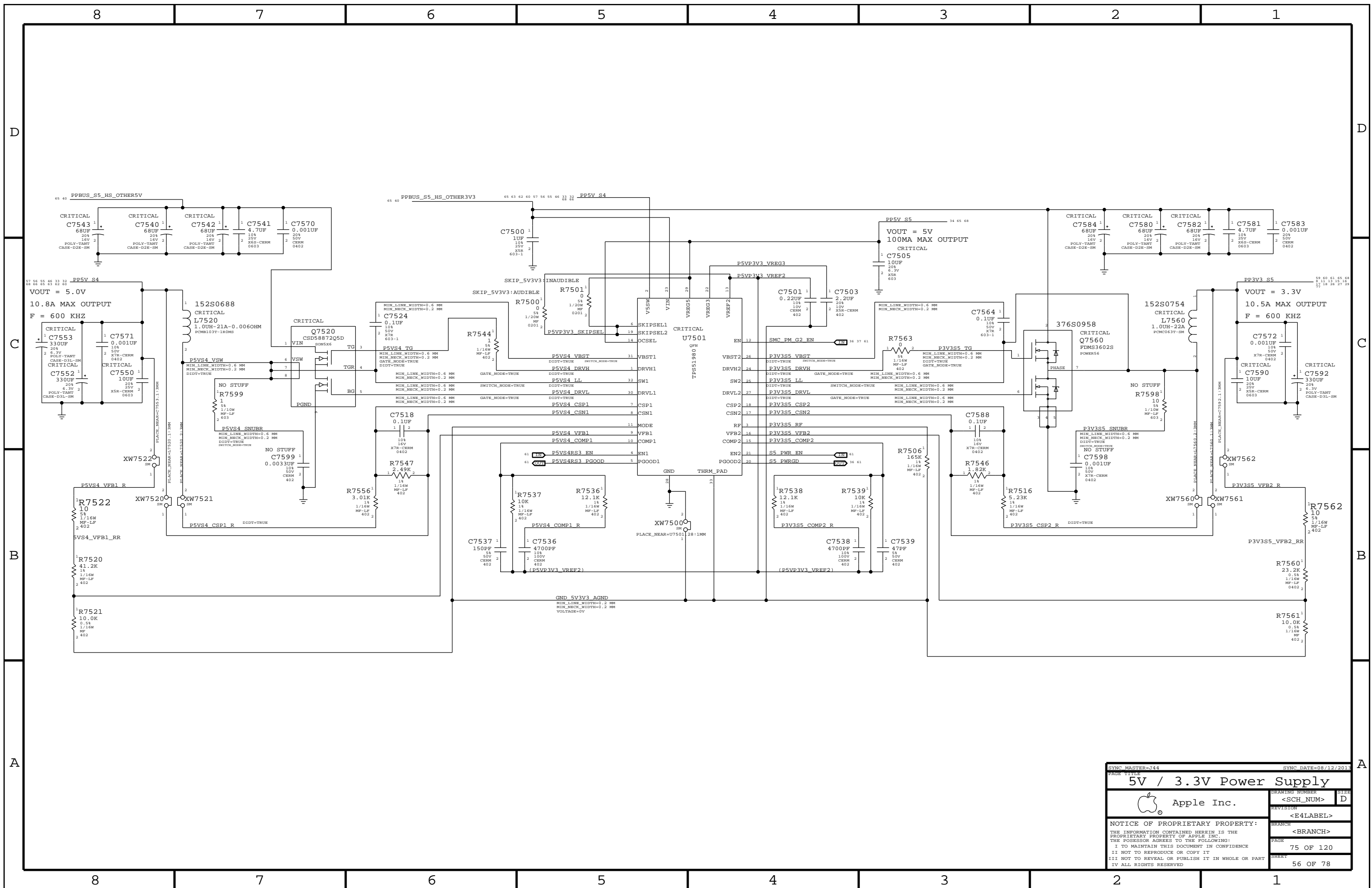
1.35V DDR3 SUPPLY

Apple Inc.

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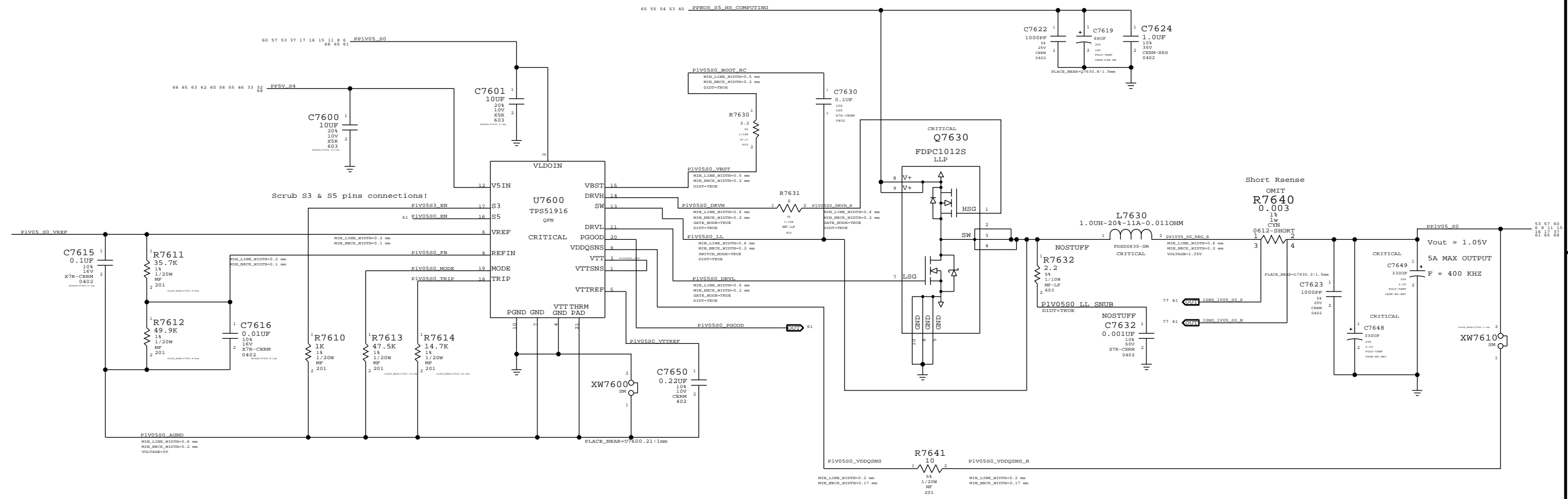
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PAGE TITLE			
5V / 3.3V Power Supply			
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1.05V S0 Regulator



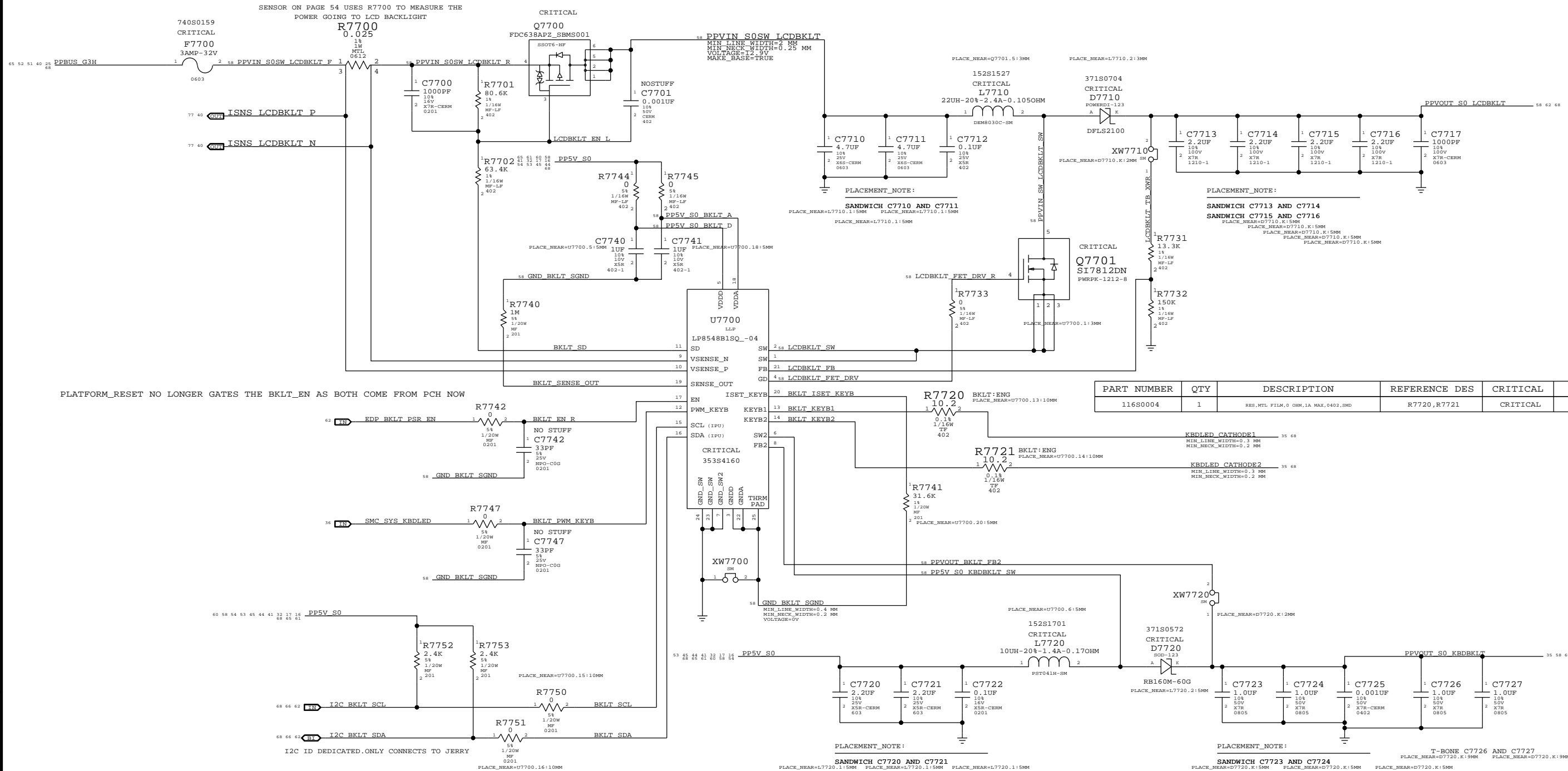
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PAGE TITLE 1.05V S0 Power Supply			
DRAWING NUMBER <SCH_NUM>		SIZE D	
REVISION <E4LABEL>		BRANCH <BRANCH>	
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Page Notes

Power aliases required by this page:
 - =PPVIN_S0SW_LCDBKLT FET (9-12.6V LCD BACKLIGHT INPUT)
 - =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
 - =PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:
 BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
 BKLT:PROD - Stuffs 0 ohm series R for production

SENSOR ON PAGE 54 USES R7700 TO MEASURE THE POWER GOING TO LCD BACKLIGHT



PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL,PT1M,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL,PT1M,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PBUS LINE WIDTHS

LCD BKLT LINE WIDTHS

KBD BKLT LINE WIDTHS

- PP5V_S0_BKLT_A 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
- PP5V_S0_BKLT_D 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
- PPVIN_S0SW_LCDBKLT F 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT R 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT FET 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
- PPVIN_S0SW_LCDBKLT 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- LCDBKLT FET DRV R 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
GATE_MODE=TRUE
DIDT=TRUE
- LCDBKLT FET DRV 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
GATE_MODE=TRUE
DIDT=TRUE
- LCDBKLT SW 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
SWITCH_MODE=TRUE
DIDT=TRUE
- PPVIN_SW_LCDBKLT SW 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
SWITCH_MODE=TRUE
DIDT=TRUE
- PP5V_S0_KBDBKLT SW 58
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=40V
SWITCH_MODE=TRUE
DIDT=TRUE
- PP5V_S0_KBDBKLT 35 58 68
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=40V
- PP5V_S0_BKLT_FB2 58
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=40V
- PP5V_S0_BKLT_FB 58
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V

SYNC MASTER=144 SYNC DATE=08/12/2013

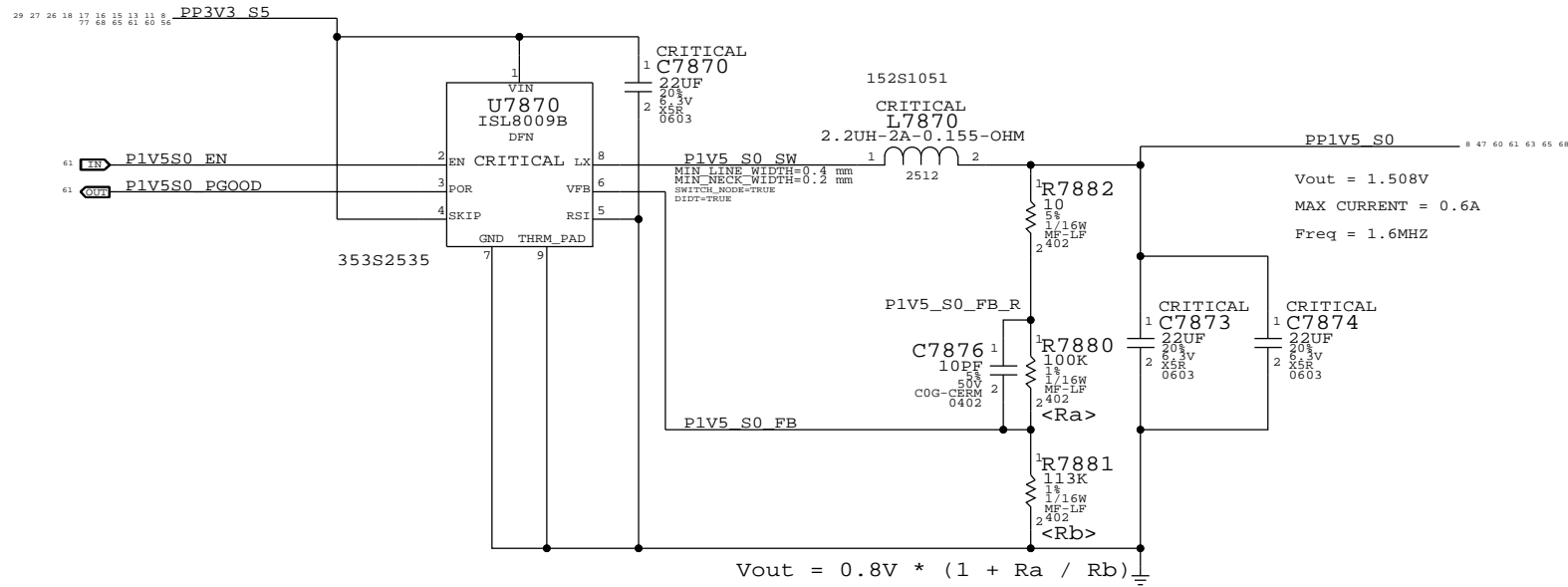
LCD AND KBD BKLT DRIVER

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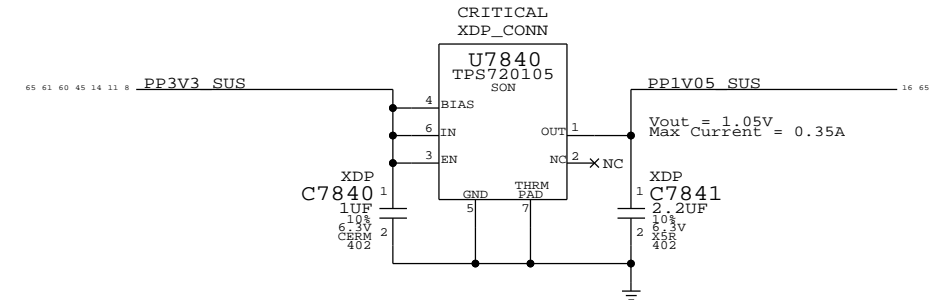
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1.5V S0 Switcher



1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

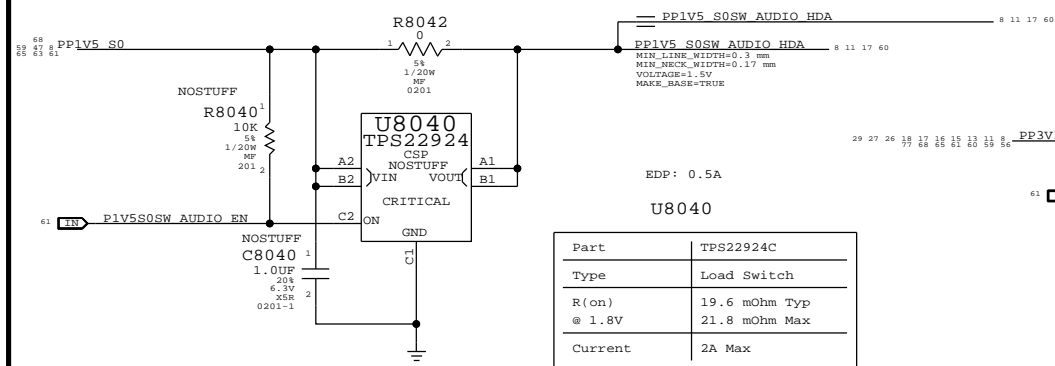


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PAGE TITLE: Misc Power Supplies			
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REVISION: <E4LABEL>		BRANCH: <BRANCH>	
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1.5V S0 Audio Switch (BYPASSED)

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

3.3V SUS Switch



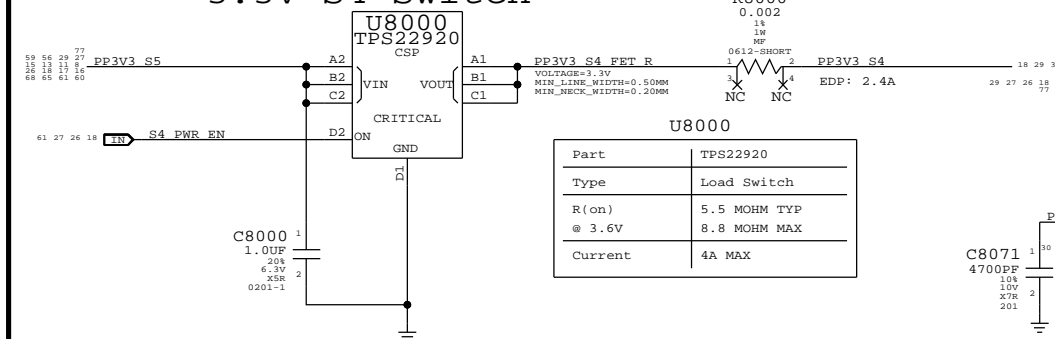
Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

3.3V S4 Switch

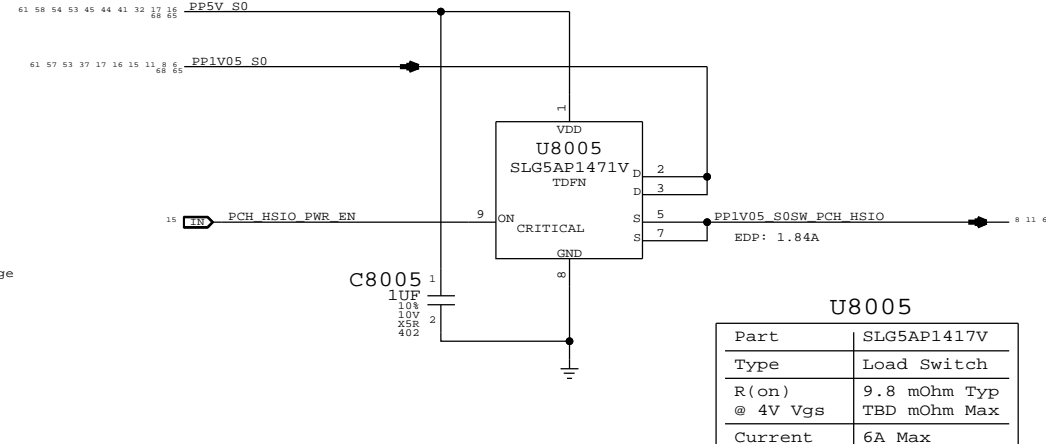
3.3V SSD Switch

1.05V PCH HSIO Switch



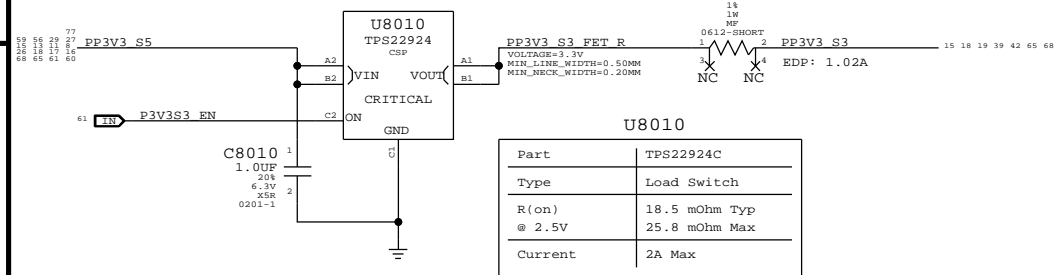
Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.5 MOHM TYP 8.8 MOHM MAX
Current	4A MAX

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max



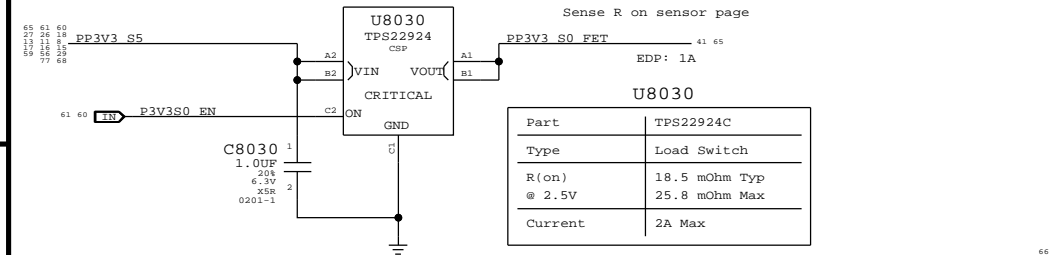
Part	SLG5AP1471V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

3.3V S3 Switch



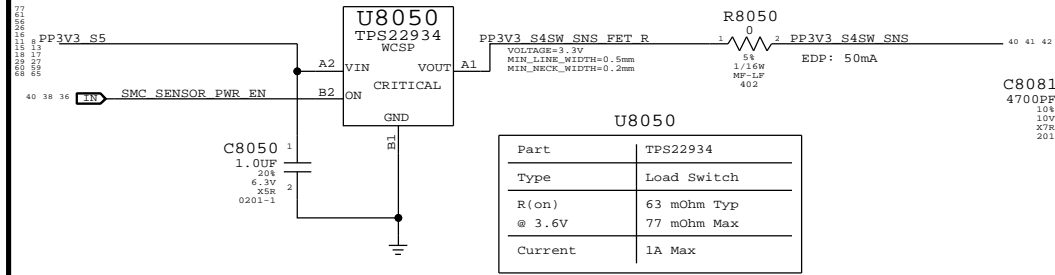
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V S0 Switch



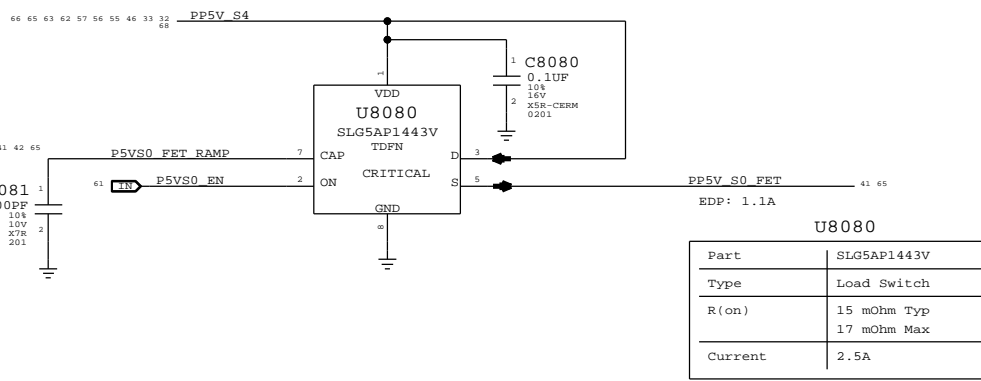
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V Sensor Switch



Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

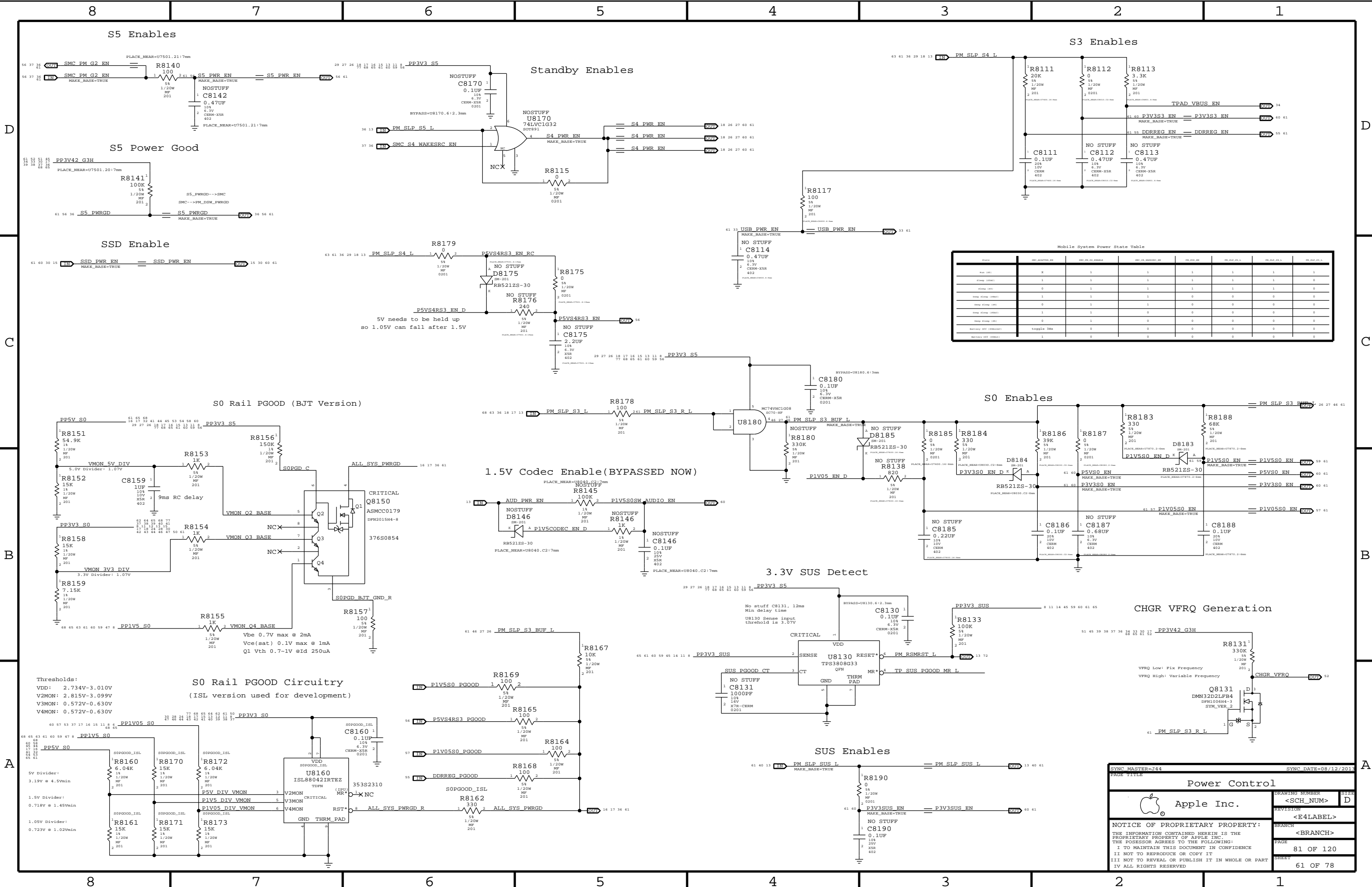
5V S0 Switch



Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
Power FETs		DRAWING NUMBER	SIZE
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Mobile System Power State Table

State	PM_SLP_S3	PM_SLP_S4	PM_SLP_S5	PM_SLP_S0	PM_SLP_S1	PM_SLP_S2
Power Off	0	0	0	0	0	0
Standby (S3)	1	0	0	0	0	0
Standby (S4)	0	1	0	0	0	0
Standby (S5)	0	0	1	0	0	0
Deep Standby (S3)	1	0	0	0	0	0
Deep Standby (S4)	0	1	0	0	0	0
Deep Standby (S5)	0	0	1	0	0	0
Deep Standby (S0)	0	0	0	1	0	0
Battery Off (Suspend)	0	0	0	0	0	0
Battery Off (Normal)	1	0	0	0	0	0

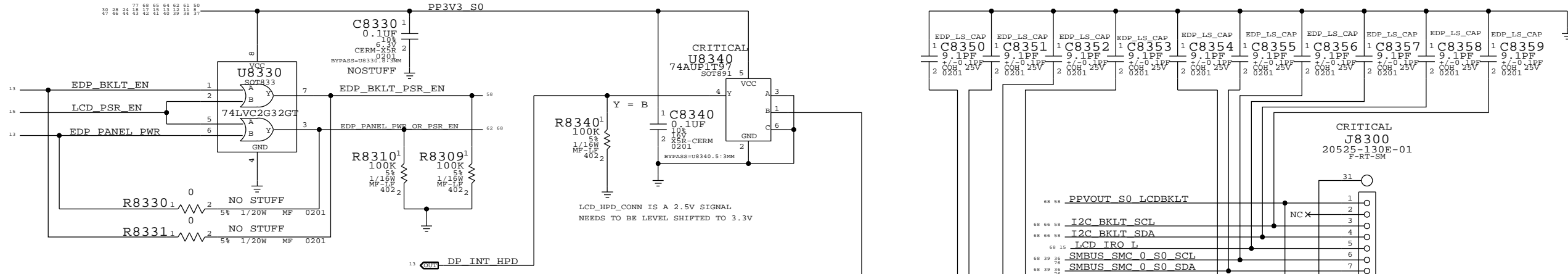
Power Control

Apple Inc.

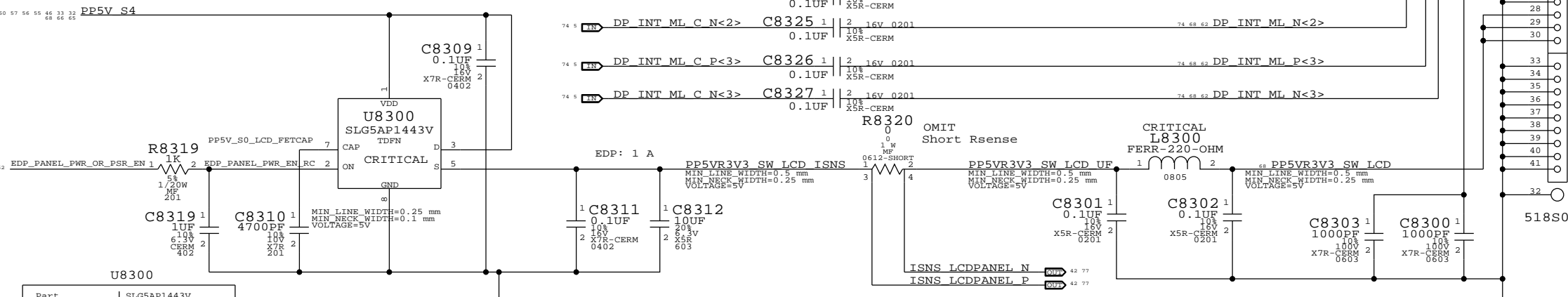
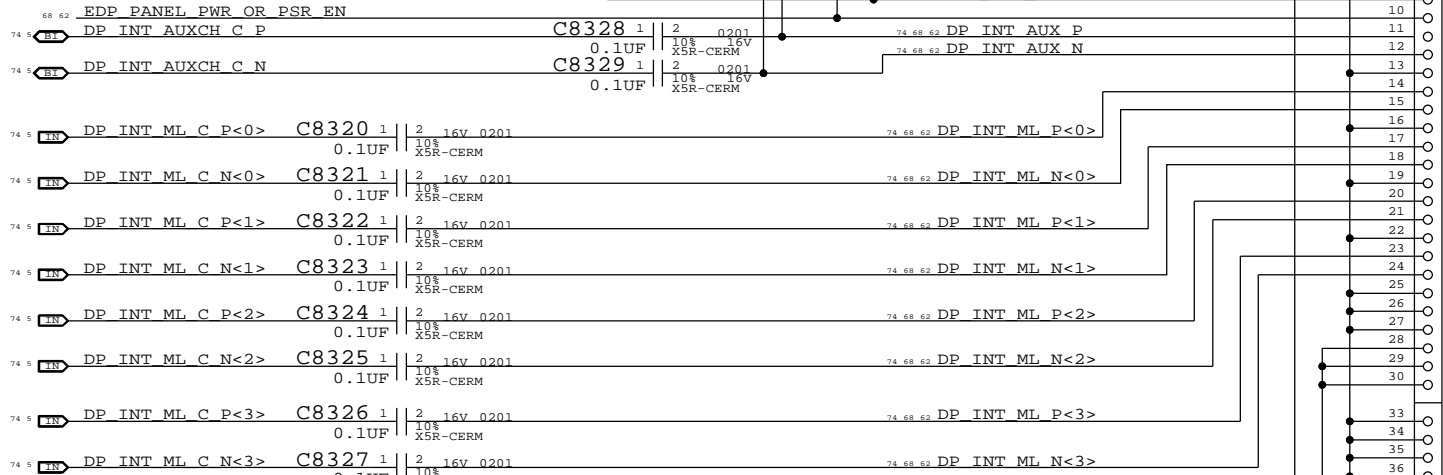
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LCD PANEL INTERFACE (eDP)
NEEDS FINAL CHECK AGAINST UPDATE FOR NEW PANEL

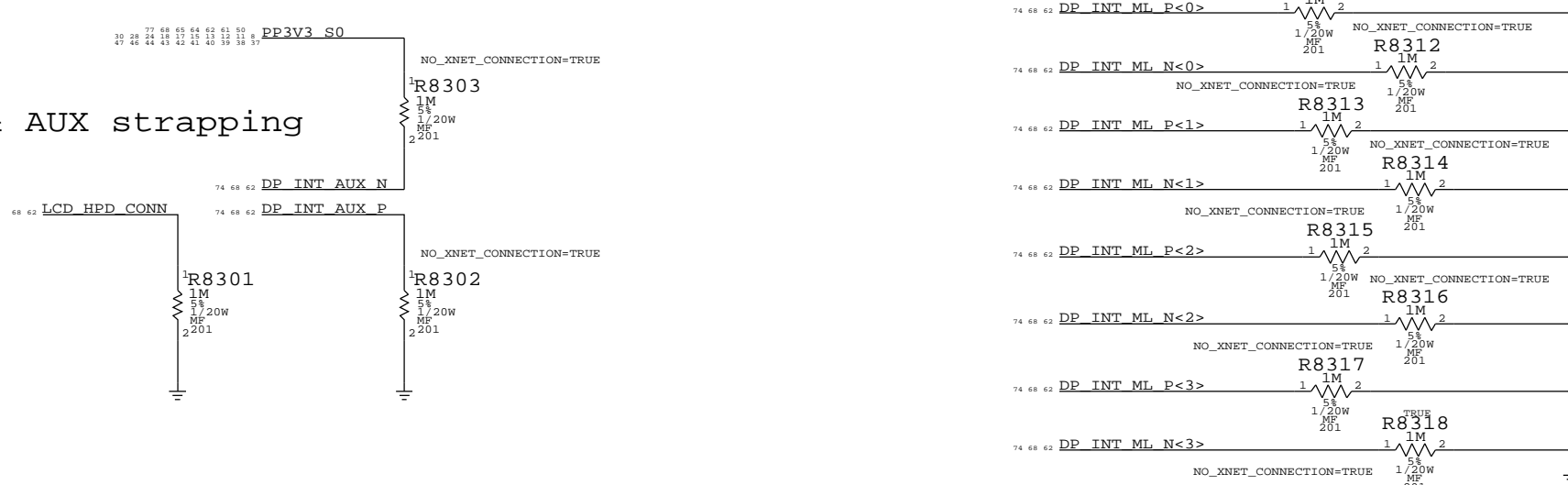


PANEL USES EDP_PANEL_PWR_PSR_EN TO DISCHARGE THE LCD BEFORE POWER GOES AWAY



Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

LCD Panel HPD & AUX strapping



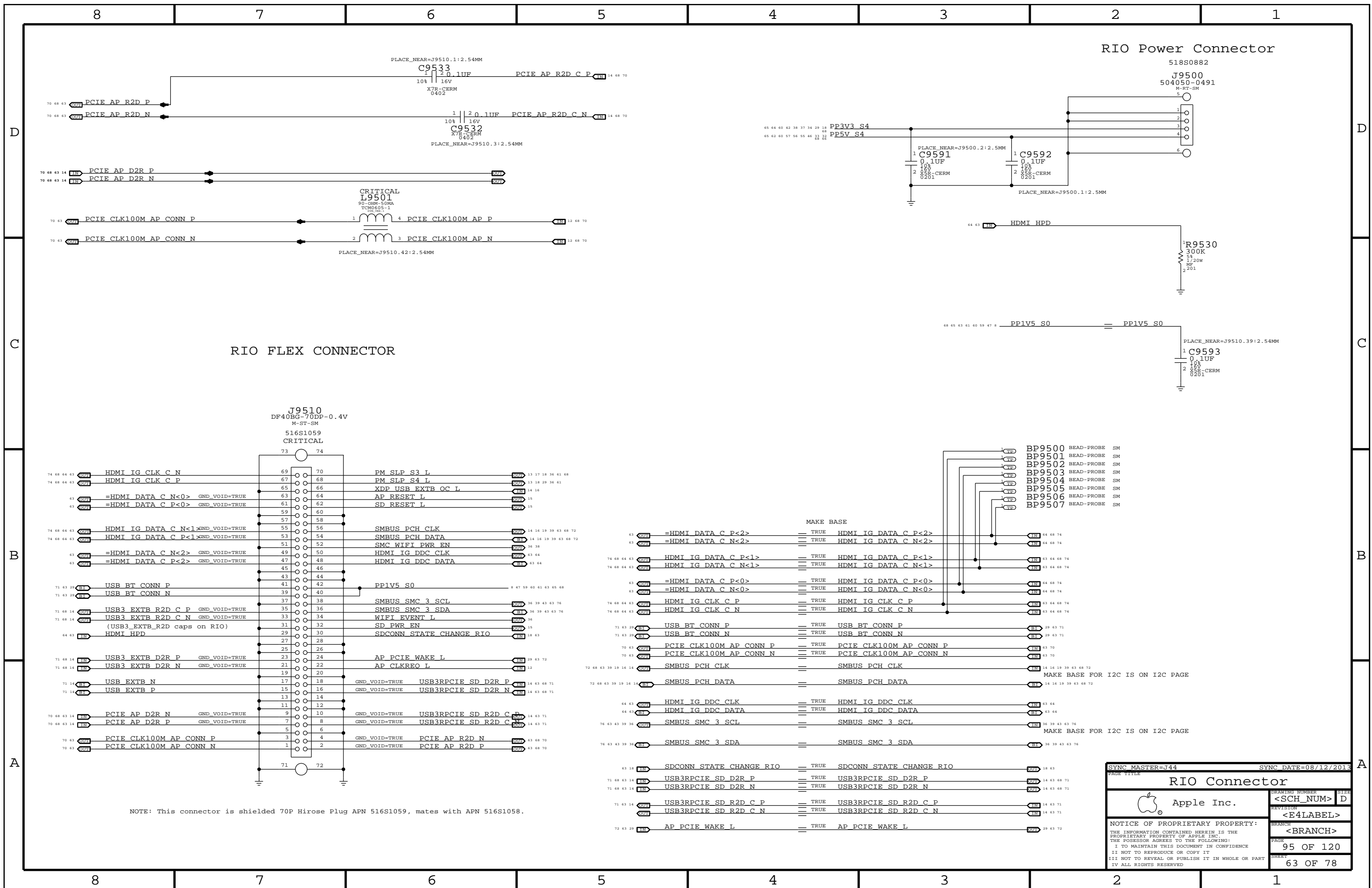
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eDP Display Connector

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RIO FLEX CONNECTOR

RIO Power Connector

J9510
DF40BG-70DP-0.4V
M-ST-SM

516S1059
CRITICAL

518S0882

J9500

504050-0491
M-ST-SM

NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

Pin	Signal Name	Direction	Internal Signal	Direction	Internal Signal
73	HDMI IG CLK C N	IN	PM SLP S3 L	OUT	33 17 18 36 61 68
74	HDMI IG CLK C P	IN	PM SLP S4 L	OUT	33 17 18 36 61 68
63	=HDMI DATA C N<0>	IN	XDP USB EXTB OC L	OUT	14 14
64	=HDMI DATA C P<0>	IN	AP RESET L	OUT	15
65	=HDMI DATA C N<1>	IN	SD RESET L	OUT	15
66	=HDMI DATA C P<1>	IN			
67	HDMI IG DATA C N<1>	IN	SMBUS PCH CLK	OUT	14 16 19 39 63 68 72
68	HDMI IG DATA C P<1>	IN	SMBUS PCH DATA	OUT	14 16 19 39 63 68 72
69	=HDMI DATA C N<2>	IN	SMC WIFI PWR EN	OUT	36 38
70	=HDMI DATA C P<2>	IN	HDMI IG DDC CLK	OUT	63 64
71	HDMI IG DATA C N<2>	IN	HDMI IG DDC DATA	OUT	63 64
72	HDMI IG DATA C P<2>	IN			
39	USB BT CONN P	IN	PPIV5 S0	OUT	8 47 59 60 61 63 65 68
40	USB BT CONN N	IN			
37	USB3 EXTB R2D C P	IN	SMBUS SMC 3 SCL	OUT	36 39 43 63 76
38	USB3 EXTB R2D C N	IN	SMBUS SMC 3 SDA	OUT	36 39 43 63 76
31	USB3 EXTB R2D caps on RIO	IN	WIFI EVENT L	OUT	36
30	HDMI HPD	IN	SD PWR EN	OUT	15
29			SDCONN STATE CHANGE RIO	OUT	18 63
27					
26					
25					
24	USB3 EXTB D2R P	IN	AP PCIE WAKE L	OUT	29 63 72
23	USB3 EXTB D2R N	IN	AP CLKREQ L	OUT	32
22					
21					
20					
19					
18	USB EXTB N	IN	GND VOID=TRUE	USB3RPCIE SD D2R P	14 63 68 71
17	USB EXTB P	IN	GND VOID=TRUE	USB3RPCIE SD D2R N	14 63 68 71
16					
15					
14					
13					
12					
11					
10	PCIE AP D2R N	IN	GND VOID=TRUE	USB3RPCIE SD R2D C P	14 63 71
9	PCIE AP D2R P	IN	GND VOID=TRUE	USB3RPCIE SD R2D C N	14 63 71
8					
7					
6					
5					
4					
3					
2					
1					

- BP9500 BEAD-PROBE SM
- BP9501 BEAD-PROBE SM
- BP9502 BEAD-PROBE SM
- BP9503 BEAD-PROBE SM
- BP9504 BEAD-PROBE SM
- BP9505 BEAD-PROBE SM
- BP9506 BEAD-PROBE SM
- BP9507 BEAD-PROBE SM

SYNC MASTER=J44 SYNC DATE=08/12/2013

RIO Connector

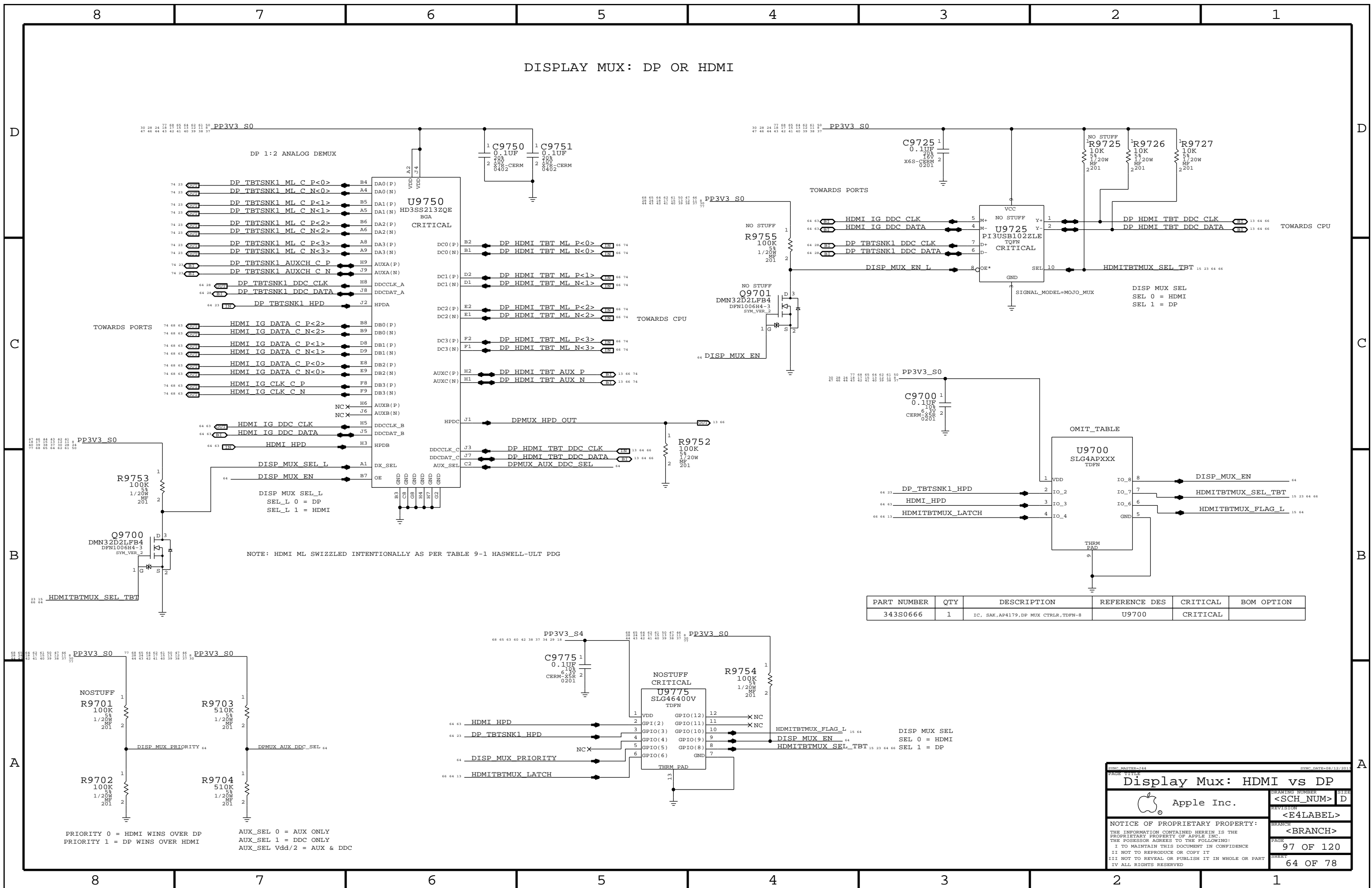
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DISPLAY MUX: DP OR HDMI

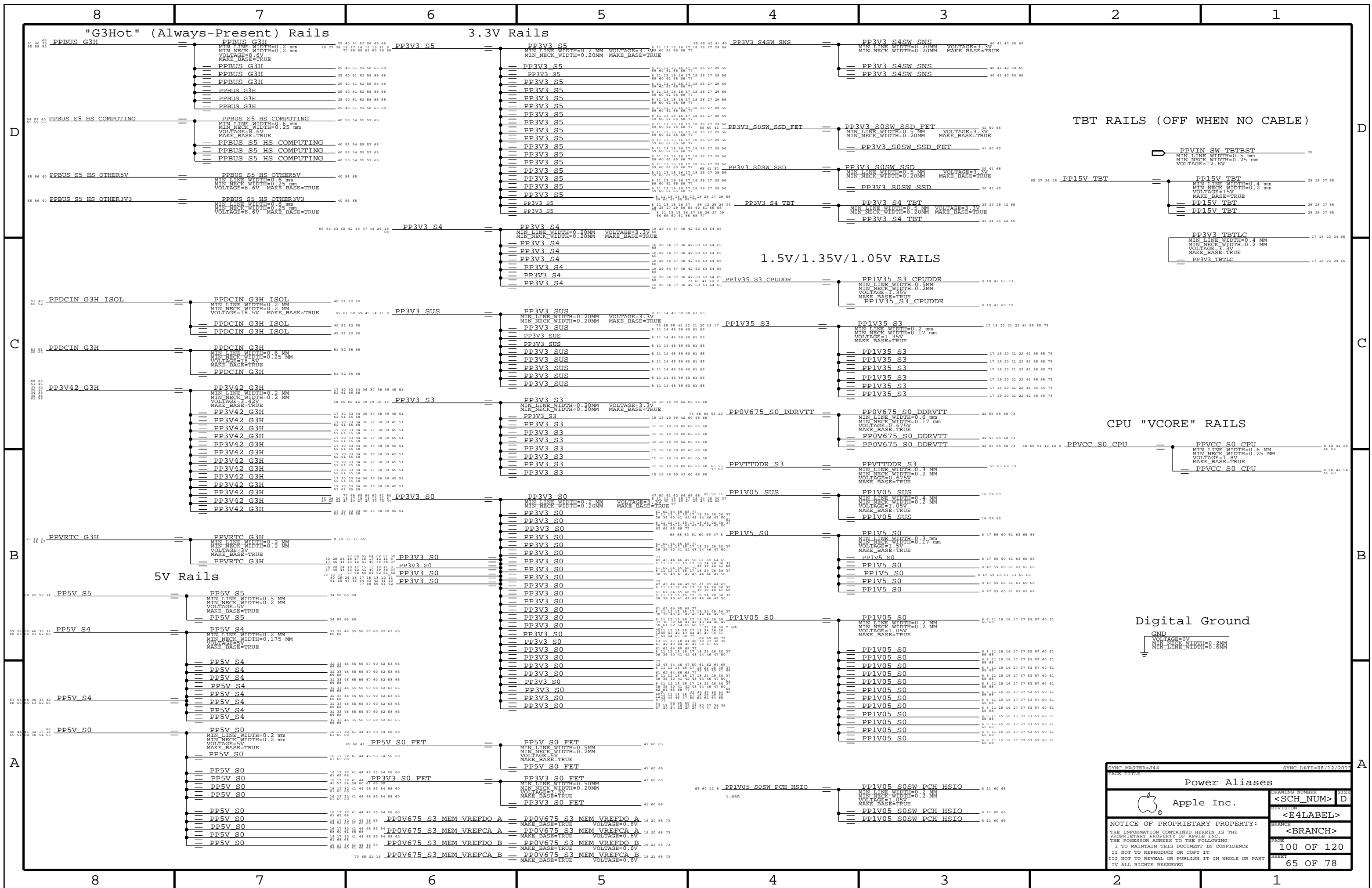


Display Mux: HDMI vs DP

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TBT RAILS (OFF WHEN NO CABLE)

CPU "V CORE" RAILS

Digital Ground

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE		DRAWING NUMBER	
		Apple Inc.	
		<SCH_NUM> D REVISION <E4LABEL>	
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		PAGE 100 OF 120	
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MEMORY ADDRESS/CTRL

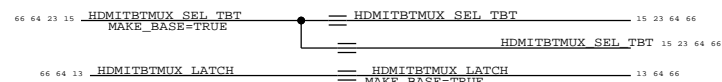
HDMI VS TBT

D

D

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7	=MEM A A<1>
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7	=MEM A A<5>
66 22 20	=MEM A A<6>
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7	=MEM A A<14>

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5	=DP TBTSNK1 ML C N<1>
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5	=DP TBTSNK1 ML C P<3>
5	=DP TBTSNK1 ML C N<3>
74 66 64 13	DP HDMI TBT AUX P
74 66 64 13	DP HDMI TBT AUX N
66 64 13	DP HDMI TBT DDC CLK
66 64 13	DP HDMI TBT DDC DATA
66 64 13	DPMUX HPD OUT



EPD PANEL

MAKE_BASE	
68 66 62 58	I2C BKLT_SCL
68 66 62 58	I2C BKLT_SDA

C

C

MAKE_BASE	
66 22 7	MEM A ODT_CPU0
66 22 20 7	MEM A_RAS_L
66 22 20 7	MEM A_WE_L
66 22 20 7	MEM A_CAS_L
7	=MEM A BA<0>
66 22 20 7	MEM A BA<1>
7	=MEM A BA<2>

UNUSED SIGNALS

MAKE_BASE	
66 12	NC_PCIE_CLK100M_FWP
66 12	NC_PCIE_CLK100M_FWN
66 14	NC_PCIE_FW_D2RP
66 14	NC_PCIE_FW_D2RN
66 14	NC_PCIE_FW_R2D_CP
66 14	NC_PCIE_FW_R2D_CN
66 12	NC_PCIE_CLK100M_ENETSDP
66 12	NC_PCIE_CLK100M_ENETSDN
71 66 14	NC_USB_IRP
71 66 14	NC_USB_IRN
71 66 14	NC_USB_CAMERAP
71 66 14	NC_USB_CAMERAN
71 66 14	NC_USB_SDP
71 66 14	NC_USB_SDN
66 12	NC_HDA_SDIN1
66 13	NC_PCI_PME_L
66 14	NC_CLINK_CLK
66 14	NC_CLINK_DATA
66 14	NC_CLINK_RESET_L

B

B

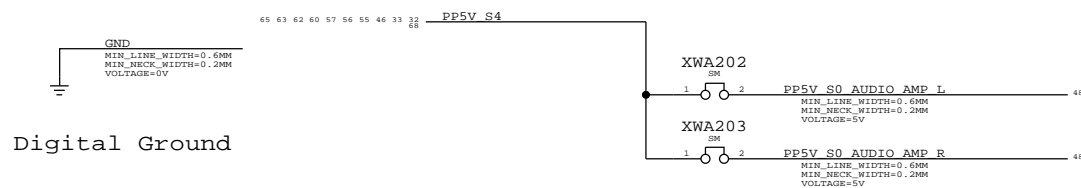
MAKE_BASE	
66 22 7	MEM B ODT_CPU0
66 22 21 7	MEM B_RAS_L
66 22 21 7	MEM B_WE_L
66 22 21 7	MEM B_CAS_L
7	=MEM B BA<0>
66 22 21 7	MEM B BA<1>
7	=MEM B BA<2>

UNUSED MEMORY SIGNALS

NO_TEST	
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7	MEM_A_CKE<2>
66 7	NC_MEM_A_CKE<3>
66 7	NC_MEM_B_CLKN<1>
66 7	NC_MEM_B_CLKP<1>
66 7	MEM_B_CKE<2>
66 7	NC_MEM_B_CKE<3>

A

A



SYNC_MASTER=MASTER		SYNC_DATE=MASTER	
PAGE TITLE			
Signal Aliases			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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Memory Bit/Byte Swizzle

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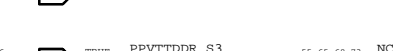
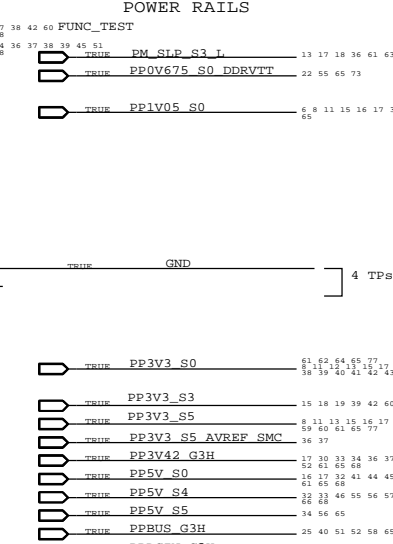
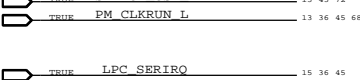
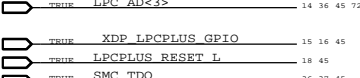
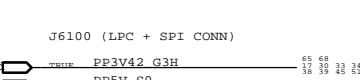
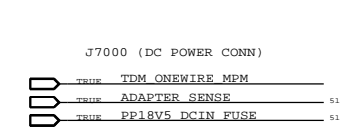
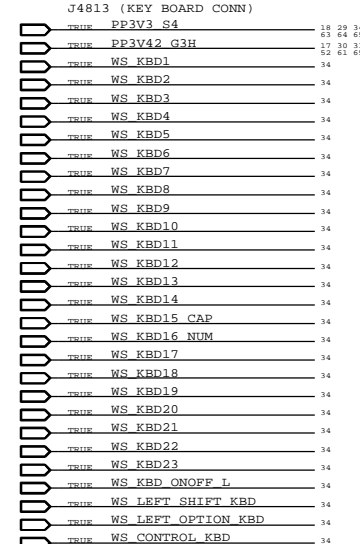
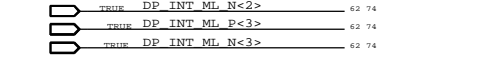
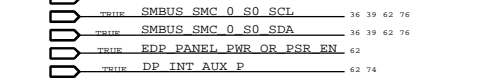
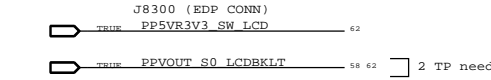
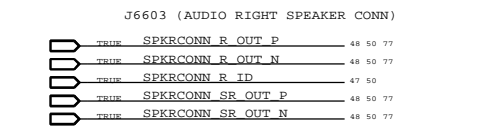
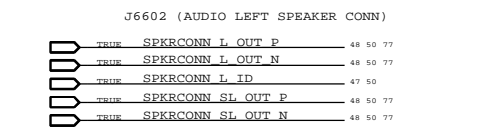
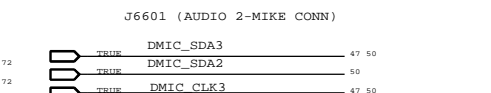
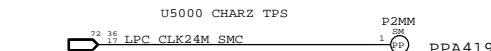
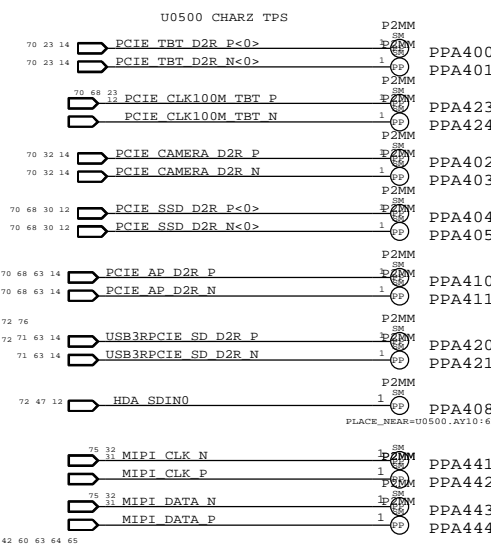
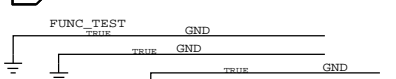
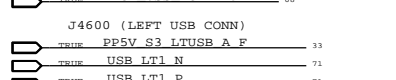
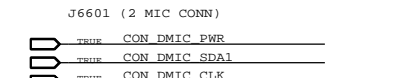
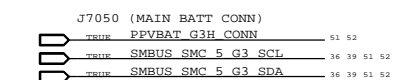
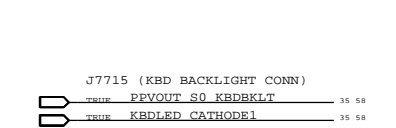
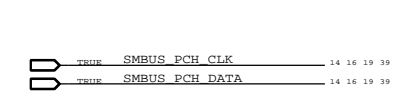
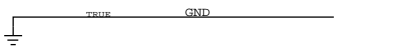
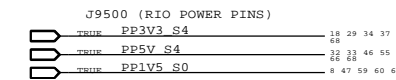
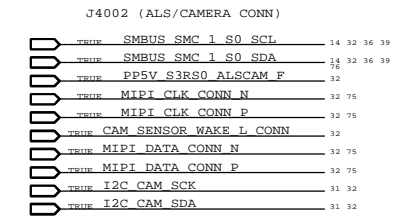
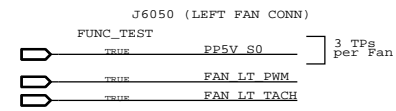
Memory Bit/Byte Swizzle

Apple Inc.

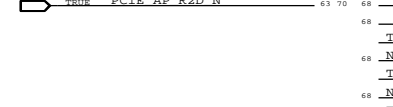
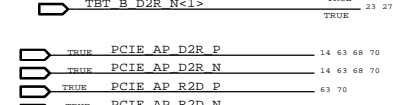
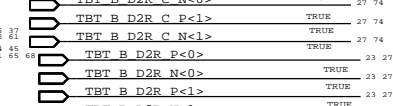
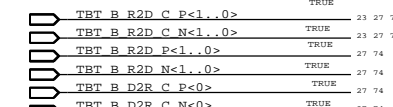
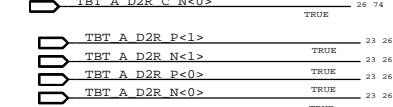
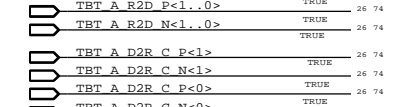
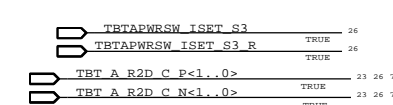
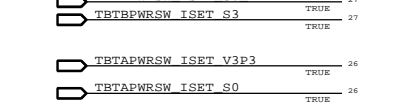
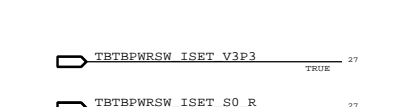
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Functional Test Points



NO_TESTS



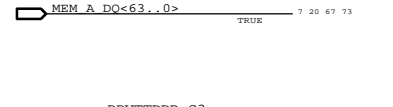
ICT Test Points



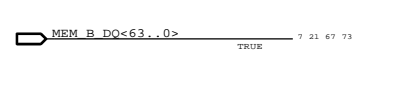
MEM A DQ<63..0>



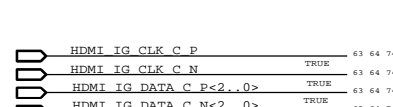
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HDMI IG CLK C P



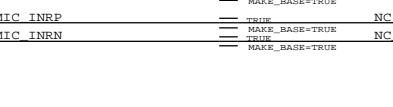
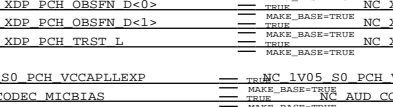
NC_XDP_PCH_HOOK4



NC_XDP_PCH_HOOK5



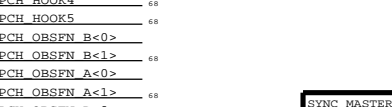
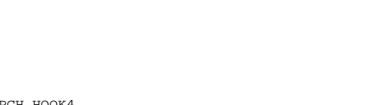
NC_XDP_PCH_OBSFN_B<0>



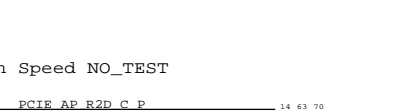
NC NO_TEST



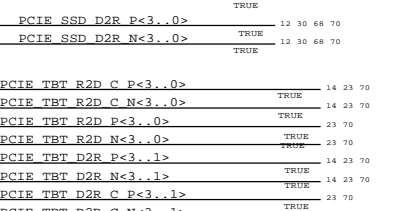
High Speed NO_TEST



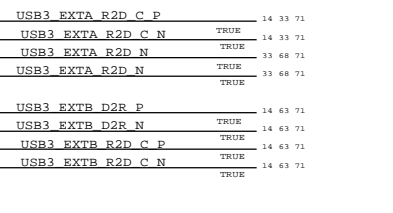
Unused nets with offpage



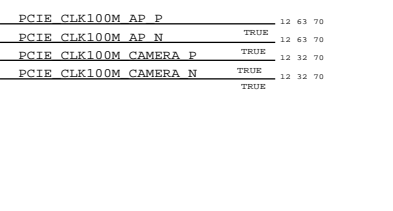
Unused nets with offpage



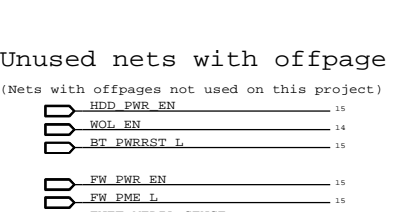
Unused nets with offpage



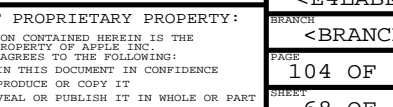
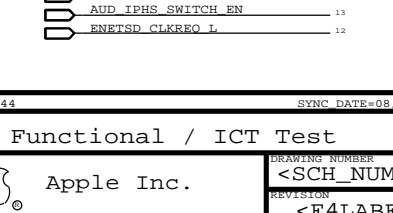
Unused nets with offpage



Unused nets with offpage



Unused nets with offpage



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J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, P65BGA, BGA_MEM			MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL11, ISL7, ISL8, ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PCB Rule Definitions			
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK *	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
XDP_TCK0	CPU_45S	CPU_18MIL	XDP CPU TCK	6 16
XDP_TCK0	CPU_45S	CPU_18MIL	PCH JTAGX	12 16
XDP_TCK1	CPU_45S	CPU_18MIL	XDP PCH TCK	12 16
XDP_TDO	CPU_45S		XDP CPU TDO	6 16
XDP_TDO	CPU_45S		XDP PCH TDO	12 16
XDP_TDI	CPU_45S		XDP CPU TDI	6 16
XDP_TDI	CPU_45S		XDP PCH TDI	12 16
XDP_TMS	CPU_45S		XDP CPU TMS	6 16
XDP_TMS	CPU_45S		XDP PCH TMS	12 16
XDP_TRST_L	CPU_45S		XDP TRST L	16
XDP_TRST_L	CPU_45S		XDP CPUPCH TRST L	6 12 16
XDP_PRDY_L	CPU_45S		XDP CPU PRDY L	6 16
XDP_PREQ_L	CPU_45S		XDP CPU PREQ L	6 16
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	CPU VCCST_PWRGD	6 16 17
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	XDP CPU VCCST_PWRGD	16
CPU_BPM	CPU_45S	CPU_08MIL	XDP BPM L<1..0>	6 16
CPU_BPM_TP	CPU_45S		XDP BPM L<7..2>	6 16
CPU_RCOMP_SM	CPU_27P4S	CPU_25MIL	CPU SM RCOMP<2..0>	6
CPU_RCOMP_FDP	CPU_27P4S	CPU_25MIL	MCP FDP RCOMP	6
CPU_RCOMP_OPT	CPU_27P4S	CPU_12MIL	CPU OPT RCOMP	6
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU PROCHOT L	6 16 17 53
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU PROCHOT R L	6
CPU_CATERR	CPU_45S	CPU_08MIL	CPU CATERR L	6 16
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU VIDALERT L	8 53
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU VIDALERT R L	8
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU VIDSCLK	8 53
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU VIDSCLK R	8
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU VIDSOUT	8 53
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU VIDSOUT R	8
CPU_PECI	CPU_45S	CPU_18MIL	CPU PECI	6 37
CPU_PECI	CPU_45S	CPU_18MIL	CPU PECI R	16 37
CPU_PECT_SMC	CPU_45S	CPU_18MIL	SMC PECT L	16 37
CPU_PECT_SMC	CPU_45S	CPU_18MIL	SMC PECT L R	37
CPU_CFG	CPU_45S		CPU CFG<19..11>	6 16
CPU_CFG_PD	CPU_45S		CPU CFG<10..8>	6 16
CPU_CFG	CPU_45S		CPU CFG<7..5>	6 16
CPU_CFG_PD	CPU_45S		CPU CFG<4>	6 16
CPU_CFG_3	CPU_45S		CPU CFG<3>	6 16
CPU_CFG	CPU_45S		CPU CFG<2>	6 16
CPU_CFG_PD	CPU_45S		CPU CFG<1..0>	6 16
CPU_MEM_RESET	CPU_45S	CPU_08MIL	MEM RESET L	20 21 22
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	8 53
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	8 53

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE SSD D2R P<3..1>	12 30 68
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE SSD D2R N<3..1>	12 30 68
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE SSD D2R P<0>	12 30 68
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE SSD D2R N<0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D C P<3..0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D C N<3..0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D P<3..0>	30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D N<3..0>	30 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R P<0>	14 23 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R N<0>	14 23 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R C P<0>	23
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R C N<0>	23
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R P<3..1>	14 23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R N<3..1>	14 23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R C P<3..1>	23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R C N<3..1>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D P<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D N<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D C P<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D C N<3..0>	14 23 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D P	63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D N	63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D C P	14 63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D C N	14 63 68
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE AP D2R P	14 63 68
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE AP D2R N	14 63 68
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN P	63
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN N	63
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP P	12 63 68
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP N	12 63 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA P	12 32 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA N	12 32 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C P	31 32
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C N	31 32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD P	12 30 68
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD N	12 30 68
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT P	12 23 68
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT N	12 23 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R P	14 32 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R N	14 32 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R C P	31 32
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R C N	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D P	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D N	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D C P	14 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D C N	14 32

SYNC MASTER=144 SYNC DATE=08/12/2013

CPU & PCIe Constraints

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAIS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAIS	*	=6X_DIELECTRIC	?	USB_RBIAIS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
USB_BT	USB_85D	USB	USB BT P	14 29
USB_BT	USB_85D	USB	USB BT N	14 29
USB_BT	USB_85D	USB	USB BT CONN P	29 63
USB_BT	USB_85D	USB	USB BT CONN N	29 63
USB_EXTA	USB_85D	USB	USB EXTA P	14 33
USB_EXTA	USB_85D	USB	USB EXTA N	14 33
DEFAULT	DEFAULT	DEFAULT	SMC DEBUGPRT RX L	33 36 37
DEFAULT	DEFAULT	DEFAULT	SMC DEBUGPRT TX L	33 36 37
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED P	33
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED N	33
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED F P	33
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED F N	33
USB_EXTA	USB_85D	USB	USB LT1 P	68
USB_EXTA	USB_85D	USB	USB LT1 N	68
USB_EXTB	USB_85D	USB	USB EXTB P	14 63
USB_EXTB	USB_85D	USB	USB EXTB N	14 63
USB_TPAD	USB_85D	USB	USB TPAD P	14 34
USB_TPAD	USB_85D	USB	USB TPAD N	14 34
USB_TPAD	USB_85D	USB	USB TPAD R P	34
USB_TPAD	USB_85D	USB	USB TPAD R N	34
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3 EXTA D2R P	14 33 68
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3 EXTA D2R N	14 33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D P	33
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D N	33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D C P	14 33 68
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D C N	14 33 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3 EXTB D2R P	14 63 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3 EXTB D2R N	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3 EXTB R2D C P	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3 EXTB R2D C N	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE SD D2R P	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE SD D2R N	14 63 68
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE SD R2D C P	14 63
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE SD R2D C N	14 63
USB_NC	USB_85D	USB	NC USB IRP	14 66
USB_NC	USB_85D	USB	NC USB IRN	14 66
USB_NC	USB_85D	USB	TP USB 5P	14
USB_NC	USB_85D	USB	TP USB 5N	14
USB_NC	USB_85D	USB	NC USB SDP	14 66
USB_NC	USB_85D	USB	NC USB SDN	14 66
USB_NC	USB_85D	USB	NC USB CAMERAP	14 66
USB_NC	USB_85D	USB	NC USB CAMERAN	14 66
PCH_USB_RBIAIS	PCH_USB_RBIAIS	USB_RBIAIS	PCH USB RBIAIS	14
SATA_85D	SATA_85D	SATA_RX	DUMMY SATA D2R P	
SATA_85D	SATA_85D	SATA_RX	DUMMY SATA D2R N	
SATA_85D	SATA_85D	SATA_TX	DUMMY SATA R2D P	
SATA_85D	SATA_85D	SATA_TX	DUMMY SATA R2D N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2 R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK CLK25M CAMERA	17 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM CLKP	31 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP R	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALN	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT	17 23
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R	23

Notes:
This is here to keep the SATA rules.

SYNC MASTER=144		SYNC DATE=08/12/2013	
USB Constraints			
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?


PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 36 45 68
LPC_AD	LPC_45S	LPC	LPC_FRAME L	14 36 45 68
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC R	12 17
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 36 68
LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 45 68
LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS R	12 17
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	14 16 19 39 63 68
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	14 16 19 39 63 68
SML_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	14 39
SML_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	14 39
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 12 36 39 63 68 76
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 12 36 39 63 68 76
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 47
HDA_BIT_CLK_R	HDA_45S	HDA	HDA_BIT_CLK R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 47
HDA_SYNC_R	HDA_45S	HDA	HDA_SYNC R	12
HDA_RST	HDA_45S	HDA	HDA_RST R L	12
HDA_RST_L	HDA_45S	HDA	HDA_RST L	12 47
HDA_SDIN	HDA_45S	HDA	HDA_SDIN	12 47 68
HDA_SDIN	HDA_45S	HDA	CS4208 HDA_SDOUT0 R	47
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 47
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT R	12 17
SPI_ALT_CLK	SPT_45S	SPT	SPI_ALT_CLK	45
SPI_CLK	SPT_45S	SPT	SPI_CLK	45
SPI_CLK_R	SPT_45S	SPT	SPI_CLK R	14 45
SPI_MLB_CLK	SPT_45S	SPT	SPI_MLB_CLK	45
SPI_SMC_CLK	SPT_45S	SPT	SPI_SMC_CLK	36 45
SPI_ALT_CS_L	SPT_45S	SPT	SPI_ALT_CS L	45
SPI_CS0_L	SPT_45S	SPT	SPI_CS0 L	45
SPI_CS0_R_L	SPT_45S	SPT	SPI_CS0 R L	14 45
SPI_MLB_CS_L	SPT_45S	SPT	SPI_MLB_CS L	45
SPI_SMC_CS_L	SPT_45S	SPT	SPI_SMC_CS L	36 45
SPI_ALT_MISO	SPT_45S	SPT	SPI_ALT_MISO	45
SPI_MISO	SPT_45S	SPT	SPI_MISO	14 45
SPI_MISO_R	SPT_45S	SPT	SPI_MISO R	45
SPI_MLB_MISO	SPT_45S	SPT	SPI_MLB_MISO	45
SPI_SMC_MISO	SPT_45S	SPT	SPI_SMC_MISO	36 45
SPI_ALT_MOSI	SPT_45S	SPT	SPI_ALT_MOSI	45
SPI_MOSI	SPT_45S	SPT	SPI_MOSI	45
SPI_MOSI_R	SPT_45S	SPT	SPI_MOSI R	14 45
SPI_MLB_MOSI	SPT_45S	SPT	SPI_MLB_MOSI	45
SPI_SMC_MOSI	SPT_45S	SPT	SPI_SMC_MOSI	36 45
SPI_IO<2>	SPT_45S	SPT	SPI_IO<2>	14 45
SPIROM_WP_L	SPT_45S	SPT	SPIROM_WP L	45
SPI_IO<3>	SPT_45S	SPT	SPI_IO<3>	14 45
SPIROM_HOLD_L	SPT_45S	SPT	SPIROM_HOLD L	45
SPIROM_USE_MLB	SPT_45S	SPT	SPIROM_USE_MLB	15 45 68
PCH_CLK32K_RTCX1	PCH_45S	PCH_15MTL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCST	PCH_45S	PCH_15MTL	PCH_SRTCST L	12
PCH_RTCRST	PCH_45S	PCH_15MTL	RTC RESET L	12
PM_THRMTRIP_L	PCH_45S	PCH_18MTL	PM_THRMTRIP L	15 37
PM_THRMTRIP_R_L	PCH_45S	PCH_18MTL	PM_THRMTRIP R L	37
PCH_INTRUDER_L	PCH_45S	PCH_15MTL	PCH_INTRUDER L	12
PCH_INTVRMEN	PCH_45S	PCH_15MTL	PCH_INTVRMEN	12
PCH_DSWVRMEN	PCH_45S	PCH_15MTL	PCH_DSWVRMEN	13
PM_RSMRST_L	PCH_45S	PCH_15MTL	PM_RSMRST L	13 61
PM_SYSRST_L	PCH_45S	PCH_15MTL	PM_SYSRST L	13 17 36 68
XDP_DBRESET_L	PCH_45S	PCH_15MTL	XDP_DBRESET L	16 17
PM_PCH_SYS_PWROK	PCH_45S	PCH_15MTL	PM_PCH_SYS_PWROK	13 16 17 36
XDP_SYS_PWROK	PCH_45S	PCH_15MTL	XDP_SYS_PWROK	16
SYS_PWROK_R	PCH_45S	PCH_15MTL	SYS_PWROK R	17
PM_PCH_PWROK	PCH_45S	PCH_15MTL	PM_PCH_PWROK	13 17
PM_S0_PGOOD	PCH_45S	PCH_15MTL	PM_S0_PGOOD	17
SMC_DELAYED_PWRGD	PCH_45S	PCH_15MTL	SMC_DELAYED_PWRGD	17 24 25 36 37
PM_DSW_PWRGD	PCH_45S	PCH_15MTL	PM_DSW_PWRGD	13 36
PM_PWRBTN_L	PCH_45S	PCH_15MTL	PM_PWRBTN L	13 16 36
XDP_CPU_PWRBTN_L	PCH_45S	PCH_15MTL	XDP_CPU_PWRBTN L	16
PCIE_WAKE_L	PCH_45S	PCH_15MTL	PCIE_WAKE L	13 29 31
AP_PCIE_WAKE_L	PCH_45S	PCH_15MTL	AP_PCIE_WAKE L	29 63
CAM_PCIE_WAKE_L	PCH_45S	PCH_15MTL	CAM_PCIE_WAKE L	31
TBT_CIO_PLUG_EVENT_L	PCH_45S	PCH_15MTL	TBT_CIO_PLUG_EVENT L	15 18 23
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT R	17
PCH_PCIE_RCOMP	PCH_27P4S	PCH_12MTL	PCH_PCIE_RCOMP	14
PCH_OPI_COMP	PCH_27P4S	PCH_12MTL	PCH_OPI_COMP	15
PCH_SATA_RCOMP	PCH_27P4S	PCH_12MTL	PCH_SATA_RCOMP	12

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PCH Constraints			
 Apple Inc.		DRAWING NUMBER	SIZE
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTL	*	=2x_DIELECTRIC	?
MEM_CTL2CTL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=2x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=2x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

Haswell ULT Memory Down DDR3L 1x8 Length Matching

DDR3 Signal Group	Unit	Min Length	Max Length
CTLmax - CTLmin	mils	0	100
CTL to CLK	mils	CLK - 500	CLK + 500
CMDi to CMDj	mils	CMDj - 100	CMDj + 100
CMD to CLK	mils	CLK - 500	CLK + 500
(DQmax - DQmin) per byte	mils	0	250
(DQS - DQmax) per byte	mils	-100	150
DQS to DQS#	mils	-5	5
DQS to CLK (Rule 1)	mils	CLK - 6500	CLK + 500
Max(CLK-DQS) - Min(CLK-DQS)	mils	0	5500
CLK to CLK#	mils	-5	5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE		MEM A CLK P<0>	7 20 22
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<0>	7 20 22
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM A CKE<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM A CS L<0>	7 20 22
MEM_A_ODT0	MEM_40S	MEM_CTL	MEM A ODT<0>	20 22
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	7 20 22 66
MEM_A_DQBYTE0	MEM_45S	MEM_A_DQBYTE_0	MEM A DQ<7..0>	7 67 68
MEM_A_DQBYTE1	MEM_45S	MEM_A_DQBYTE_1	MEM A DQ<15..8>	7 67 68
MEM_A_DQBYTE2	MEM_45S	MEM_A_DQBYTE_2	MEM A DQ<23..16>	7 67 68
MEM_A_DQBYTE3	MEM_45S	MEM_A_DQBYTE_3	MEM A DQ<31..24>	7 67 68
MEM_A_DQBYTE4	MEM_45S	MEM_A_DQBYTE_4	MEM A DQ<39..32>	7 20 67 68
MEM_A_DQBYTE5	MEM_45S	MEM_A_DQBYTE_5	MEM A DQ<47..40>	7 67 68
MEM_A_DQBYTE6	MEM_45S	MEM_A_DQBYTE_6	MEM A DQ<55..48>	7 67 68
MEM_A_DQBYTE7	MEM_45S	MEM_A_DQBYTE_7	MEM A DQ<63..56>	7 67 68
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<0>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<1>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<1>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<2>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<2>	7 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<3>	7 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<3>	7 67
MEM_A_DQS8	MEM_80D	MEM_A_DQS_8	MEM A DQS P<4>	7 67
MEM_A_DQS9	MEM_80D	MEM_A_DQS_9	MEM A DQS N<4>	7 67
MEM_A_DQS10	MEM_80D	MEM_A_DQS_10	MEM A DQS P<5>	7 67
MEM_A_DQS11	MEM_80D	MEM_A_DQS_11	MEM A DQS N<5>	7 67
MEM_A_DQS12	MEM_80D	MEM_A_DQS_12	MEM A DQS P<6>	7 20 67
MEM_A_DQS13	MEM_80D	MEM_A_DQS_13	MEM A DQS N<6>	7 20 67
MEM_A_DQS14	MEM_80D	MEM_A_DQS_14	MEM A DQS P<7>	7 67
MEM_A_DQS15	MEM_80D	MEM_A_DQS_15	MEM A DQS N<7>	7 67
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<0>	7 21 22
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM B CKE<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM B CS L<0>	7 21 22
MEM_B_ODT0	MEM_40S	MEM_CTL	MEM B ODT<0>	21 22
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	7 21 22 66
MEM_B_DQBYTE0	MEM_45S	MEM_B_DQBYTE_0	MEM B DQ<7..0>	7 67 68
MEM_B_DQBYTE1	MEM_45S	MEM_B_DQBYTE_1	MEM B DQ<15..8>	7 67 68
MEM_B_DQBYTE2	MEM_45S	MEM_B_DQBYTE_2	MEM B DQ<23..16>	7 67 68
MEM_B_DQBYTE3	MEM_45S	MEM_B_DQBYTE_3	MEM B DQ<31..24>	7 67 68
MEM_B_DQBYTE4	MEM_45S	MEM_B_DQBYTE_4	MEM B DQ<39..32>	7 21 67 68
MEM_B_DQBYTE5	MEM_45S	MEM_B_DQBYTE_5	MEM B DQ<47..40>	7 67 68
MEM_B_DQBYTE6	MEM_45S	MEM_B_DQBYTE_6	MEM B DQ<55..48>	7 67 68
MEM_B_DQBYTE7	MEM_45S	MEM_B_DQBYTE_7	MEM B DQ<63..56>	7 67 68
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<0>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<1>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<1>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<2>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<2>	7 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<3>	7 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<3>	7 67
MEM_B_DQS8	MEM_80D	MEM_B_DQS_8	MEM B DQS P<4>	7 67
MEM_B_DQS9	MEM_80D	MEM_B_DQS_9	MEM B DQS N<4>	7 67
MEM_B_DQS10	MEM_80D	MEM_B_DQS_10	MEM B DQS P<5>	7 67
MEM_B_DQS11	MEM_80D	MEM_B_DQS_11	MEM B DQS N<5>	7 67
MEM_B_DQS12	MEM_80D	MEM_B_DQS_12	MEM B DQS P<6>	7 21 67
MEM_B_DQS13	MEM_80D	MEM_B_DQS_13	MEM B DQS N<6>	7 21 67
MEM_B_DQS14	MEM_80D	MEM_B_DQS_14	MEM B DQS P<7>	7 67
MEM_B_DQS15	MEM_80D	MEM_B_DQS_15	MEM B DQS N<7>	7 67
MEM_PWR			PP1V35 S3	17 19 20 21 22 41 55 65
MEM_PWR			PP1V35 S3 CPUDDR	8 10 41 65
MEM_PWR			PP0V675 S0 DDRVTT	22 55 65 68
MEM_PWR			PPVTDDR S3	55 65 68
MEM_12MIL			CPU DIMMA VREFD0	7 19
MEM_12MIL			CPU DIMMA VREFD0 A ISOL	19
MEM_12MIL			CPU DIMMB VREFD0	7 19
MEM_12MIL			CPU DIMMB VREFD0 B ISOL	19
MEM_12MIL			CPU DIMM VREFCA	7 19
MEM_12MIL			CPU DIMM VREFCA A ISOL	19
MEM_12MIL			CPU DIMM VREFCA B ISOL	19
MEM_12MIL			PP0V675 S3 MEM VREFD0 A	19 20 65
MEM_12MIL			PP0V675 S3 MEM VREFD0 B	19 21 65
MEM_12MIL			PP0V675 S3 MEM VREFCA A	19 20 65
MEM_12MIL			PP0V675 S3 MEM VREFCA B	19 21 65

SYNC MASTER=144 SYNC DATE=01/03/2013

Apple Inc.

Memory Constraints

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
 DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
 SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
 MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

ELECTRICAL CONST SET	PHYSICAL	SPACING	NET TYPE
	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N
	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
	TBT_SPI_45S	TBT_SPI	TBT SPI CS L
	DP_85D	DISPLAYPORT	DP HDMI TBT ML P<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT ML N<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX P
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX N
	HDMI_85D	HDMI_CLK	HDMI IG CLK C P
	HDMI_85D	HDMI_CLK	HDMI IG CLK C N
	HDMI_85D	HDMI_DATA	HDMI IG DATA C P<2..0>
	HDMI_85D	HDMI_DATA	HDMI IG DATA C N<2..0>

Only used on hosts supporting Thunderbolt video-in

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	PHYSICAL	SPACING	NET TYPE
	TBTDP_85D	TBTDP_TX	TBT A R2D C P<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D C N<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D P<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D N<1..0>
	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>
	DP_85D	DISPLAYPORT	DP A LSX ML P<1>
	DP_85D	DISPLAYPORT	DP A LSX ML N<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>
	TBTDP_85D	TBTDP_RX	TBT A D2R C P<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R C N<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R P<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R N<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R C P<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R C N<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R P<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R N<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R1 AUXDDC P
	TBTDP_85D	TBTDP_RX	TBT A D2R1 AUXDDC N
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH P
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH N
	TBTDP_85D	TBTDP_TX	TBT B R2D C P<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D C N<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D P<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D N<1..0>
	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML P<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML N<1>
	DP_85D	DISPLAYPORT	DP B LSX ML P<1>
	DP_85D	DISPLAYPORT	DP B LSX ML N<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML P<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML N<3>
	TBTDP_85D	TBTDP_RX	TBT B D2R C P<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R C N<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R P<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R N<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R C P<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R C N<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R P<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R N<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R1 AUXDDC P
	TBTDP_85D	TBTDP_RX	TBT B D2R1 AUXDDC N
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH P
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH N
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH P
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH N
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH P
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH N
	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>
	DP_85D	DISPLAYPORT	DP INT ML P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML N<3..0>
	DP_85D	DISPLAYPORT	DP INT AUXCH C P
	DP_85D	DISPLAYPORT	DP INT AUXCH C N
	DP_85D	DISPLAYPORT	DP INT AUXCH P
	DP_85D	DISPLAYPORT	DP INT AUXCH N

Notes:
 AUX and DDC was removed from DISPLAYPORT or TBTDP_RX/TX because it's not high speed, and to save routing space.

Only used on dual-port hosts.

SYNC MASTER=144 SYNC DATE=08/12/2013
 PAGE TITLE
TBT,DP,HDMI Constraints
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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?	MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?	MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?	MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2X_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2X_DIELECTRIC	?	S2_DQS2OWNDATA	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CTRL	*	=2X_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CTRL2CTRL	*	=2X_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_2OTHERMEM	*	=4X_DIELECTRIC	?	S2_2OTHERMEM	TOP,BOTTOM	=6X_DIELECTRIC	?
S2MEM_2PWR	*	=2X_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2GND	*	=2X_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2OTHER	*	=6X_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N 31 32
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE 31 32
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DO<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DO<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P 31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N 31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK P 31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK N 31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN P 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN N 32 68
		S2_MEM_PWR	PP1V35 CAM 31 32
		S2_MEM_PWR	PP0V675 CAM VREF 31 32
		S2_MEM_PWR	PP0V675 MEM CAM VREFCA 32
		S2_MEM_PWR	PP0V675 MEM CAM VREFDO 32

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SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE		SMBUS_SMC_2_S3_SCL	34 36 39 68
	PHYSICAL	SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	34 36 39 68
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 72
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 72
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 39 62 68
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 39 62 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	36 39 51 52 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	36 39 51 52 68
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	36 39 43 63
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	36 39 43 63

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