1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J92 MLB NEWARK - DVT

11/21/2014

ALIASES RESOLVED

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00107	1	SCHEM,MLB-NEWARK,J92	SCH	CRITICAL	
820-00045	1	PCBF,MLB-NEWARK,J92	PCB	CRITICAL	

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,CCSAK,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS,EQ:4CH
MLB_MISC	CAM_FREQ:24M,CAM_XTAL:NO,EDP,RSMRST:SMC,PGOOD8:SLP_S4,SSD_LPSR:S3
MLB_DEBUG:ENG	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PVT	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PROD	XDP

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAM:HYN_2GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_2GB
DRAM:HYN_4GB_QDP	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB_QDP
DRAM:HYN_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_4GB
DRAM:HYN_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:HYNIX_8GB
DRAM:ELP_2GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_2GB
DRAM:ELP_4GB_QDP	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB_QDP
DRAM:ELP_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_4GB
DRAM:ELP_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4638	1	IC,MCU,LPC11U37,128KB/12KB,TFBGA48	U4600	CRITICAL	HPM:BLANK
341S00190	1	IC,HPM (VXXX) DVT,X261	U4600	CRITICAL	HPM:PROG
338S1231	1	IC,SMC12-B1,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00031	1	IC,SMC-B1,EXTERNAL (VXXXX) PROTO2A, J92	U5000	CRITICAL	SMC:PROG
335S1009	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_WIN:BLANK
335S1010	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S1029	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MIC:BLANK
341S00191	1	EFI ROM,MLB (VXXX) DVT,X261	U6100	CRITICAL	BOOTROM:PROG
335S0948	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLBGA	U8800	CRITICAL	SSDROM_WIN:BLANK
335S0966	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLCSP	U8800	CRITICAL	SSDROM_MAC:BLANK
341S00091	1	S1-X SSD BOOTROM, U164	U8800	CRITICAL	SSDROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00054	1	IC,CPU,BW,QGKE,QS,E0,2/2,0.8,4.5W,.8,B1234	U0500	CRITICAL	CPU:0.8GHZ
337S00099	1	IC,CPU,BW,QH2Z,PRQ,F0,2/2,1.1,5W,.85,B1234	U0500	CRITICAL	CPU:1.1GHZ
337S00098	1	IC,CPU,BW,QH2V,PRQ,F0,2/2,1.2,5W,.9,B1234	U0500	CRITICAL	CPU:1.2GHZ
337S00097	1	IC,CPU,BW,QH2R,PRQ,F0,2/2,1.3,5W,.9,B1234	U0500	CRITICAL	CPU:1.3GHZ
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7995	1	LABEL,BARCODE,2D,1D,CONFIG,MLB,X261	LABEL		

SSD POP Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S0243	1	POP,S1-X CONTROLLER+4GBITS ELP,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_ELP
339S0244	1	POP,S1-X CONTROLLER+4GBITS HYN,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_HYN
685-00003	1	POP,MLB,S1X-A1,ELP-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_ELP
685-00004	1	POP,MLB,S1X-A1,HYN-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_HYN
338S1288	1	IC,S1-X,CONTROLLER,A1,841(312)B,FCCSP	SSD_CTRL	CRITICAL	S1X:A1
338S00055	1	IC,S1-X,CONTROLLER,A2,841(312)B,FCBGA	SSD_CTRL	CRITICAL	S1X:A2
333S0733	1	IC,LPDDR2,128MX32,1.2V,ELPIDA 28NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:ELPIDA
333S0694	1	IC,LPDDR2,128MX32,1.2V,HYNIX 29NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:HYNIX
870-00878	1	TAPE,CONDUCTIVE,SSD,REEL,X261	SSD_TAPE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-6486	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S00028	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB_QDP
998-6453	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_2GB
998-6454	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB_QDP
333S0730	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0731	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0740	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0741	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_8GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
2GB	0	0
4GB QDP	0	1
4GB DDP	1	0
8GB	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00074	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
128S0393	128S0334		ALL	Kemet alt to Sanyo
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
197S0590	197S0588		ALL	Epson alt to TXC
197S0591	197S0588		ALL	NDK alt to TXC
107S0249	107S0251		ALL	TFT alt to Cyntec
138S0789	138S0941		ALL	Samsung alt to Murata
333S0700	333S0704		ALL	Hynix CAM DRAM alt to Elpida
333S00016	333S0704		ALL	Elpida new die CAM DRAM alt
333S00030	333S0704		ALL	Hynix new die CAM DRAM alt
339S0243	339S0244		ALL	Elpida SSD DRAM alt to Hynix
335S0948	335S0966		ALL	Winbond alt to Macronix
128S0631	128S0351		ALL	NEC alt to Sanyo
128S00008	128S0380		ALL	NEC alt to Sanyo
311S00007	311S0426		ALL	Sanyo alt to NEC
311S00008	311S0271		ALL	Samsung alt to Murata
311S00018	311S0409		ALL	Diodes alt to NXP
740S00004	740S0134		ALL	Kemet alt to Sanyo
740S00005	740S0190		ALL	Polytronics alt to Wayon
128S0296	128S0487		ALL	Sanyo alt to NEC
128S00012	128S0487		ALL	ROHM alt to NEC
128S00025	128S0469		ALL	Kemet alt to Sanyo
128S0374	128S0469		ALL	NEC alt to Sanyo
376S00007	376S1179		ALL	AOS alt to Vishay
376S1080	376S0820		ALL	Diodes alt to Onsemi
376S00036	376S1194		ALL	Vishay alt to Onsemi
376S00037	376S1193		ALL	Vishay alt to Onsemi
685-00004	685-00003	SSDRAM:A1_ELP	ALL	Hynix SSD DRAM alt to Elpida
337S00061	337S00054	CPU:0.8GHZ	ALL	2.4G turbo CPU alt to 2.0G

SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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Top level BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-6568	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6569	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6570	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6571	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6572	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6573	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6574	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6575	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6576	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6577	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6578	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6579	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6580	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6581	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6582	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6583	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6584	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6585	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6586	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6587	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6588	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6589	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6590	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6591	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6592	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6593	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6594	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6595	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6596	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6597	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6598	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6599	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6600	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6601	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6602	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6603	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6604	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6605	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6606	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6607	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6608	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6609	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6610	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6611	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6612	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6613	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6614	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6615	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP

Partial & development BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00014	CMN PTS,PCBA,MLB-NEWARK,J92	MLB_COMMON
685-00003	POP,MLB,S1X-A2,ELP-4GBIT,X261	S1X:A2,S1X_DRAM:ELPIDA
685-00004	POP,MLB,S1X-A2,HYN-4GBIT,X261	S1X:A2,S1X_DRAM:HYNIX
939-00043	PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261	ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG

Common BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00014	1	CMN PTS,PCBA,MLB-NEWARK,J92	CMNPTS	CRITICAL	CMN

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00196	1	BT ROM (VXX) DVT,2MBIT,X261	U3570	CRITICAL	BT:PROG
341S00197	1	WIFI ROM (PXXXX) DVT,WW1,X261	U3580	CRITICAL	WIFI:FCC
341S00198	1	WIFI ROM (PXXXX) DVT,WW2,X261	U3580	CRITICAL	WIFI:ETSI
341S00199	1	WIFI ROM (PXXXX) DVT,WW3,X261	U3580	CRITICAL	WIFI:APAC
341S00200	1	WIFI ROM (PXXXX) DVT,IND,X261	U3580	CRITICAL	WIFI:IND

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J92 BOM Variants

Apple Inc.

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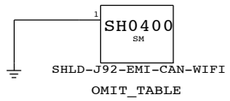
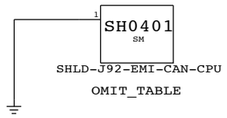
WIFI EMI CAN



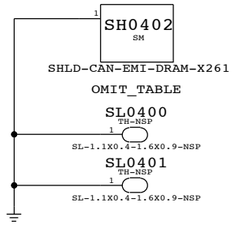
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-7064	1	CAN,EMI,WIFI,X261	SH0400	CRITICAL	

CPU EMI CAN



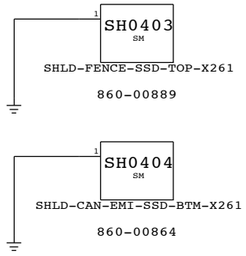
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00112	1	CAN,EMI,CPU,X261	SH0401	CRITICAL	

DRAM EMI CAN & SLOTs

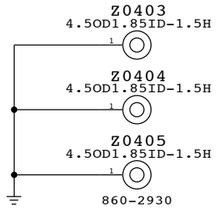


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00400	1	CAN,EMI,DRAM,TALL,X261	SH0402	CRITICAL	

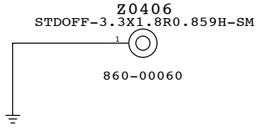
SSD EMI FENCE & CAN



CPU Heat Spreader Bosses



E85 BTB Connector Boss



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PD PARTS

Apple Inc.

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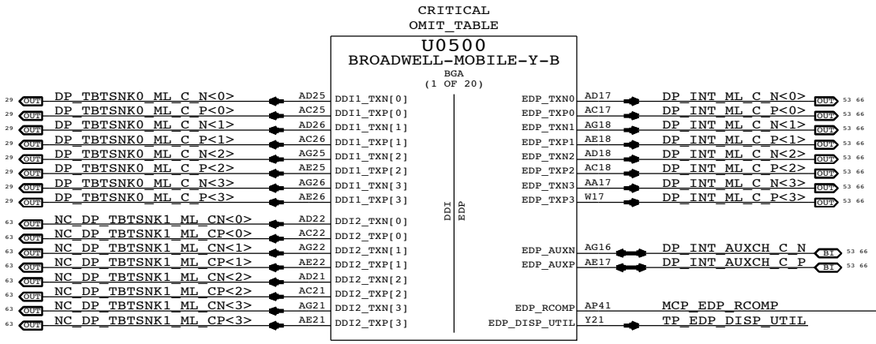
DDI Port Assignments:

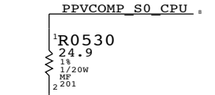
TBT Sink 0

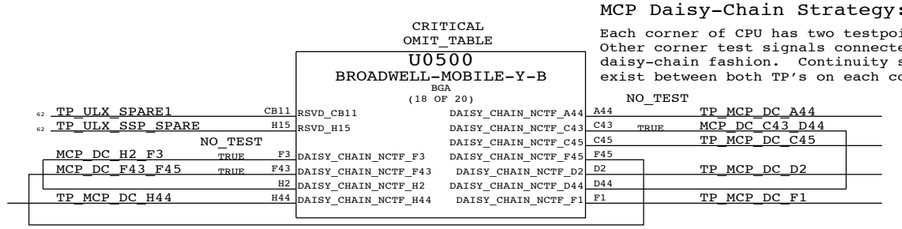
TBT Sink 1
(MUXed with HDMI
if necessary)



eDP Port Assignment:

Internal panel





MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

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Apple Inc.

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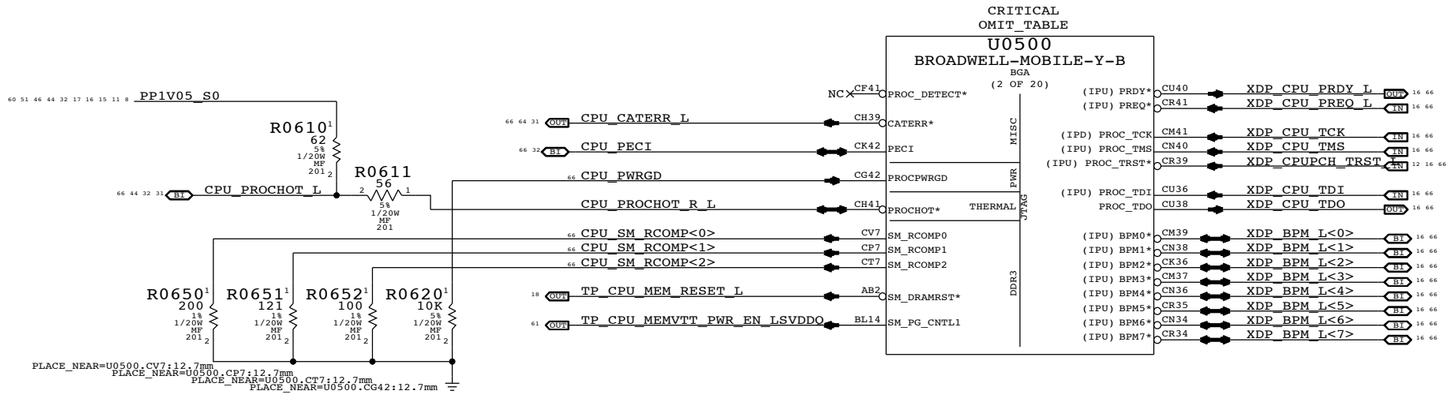
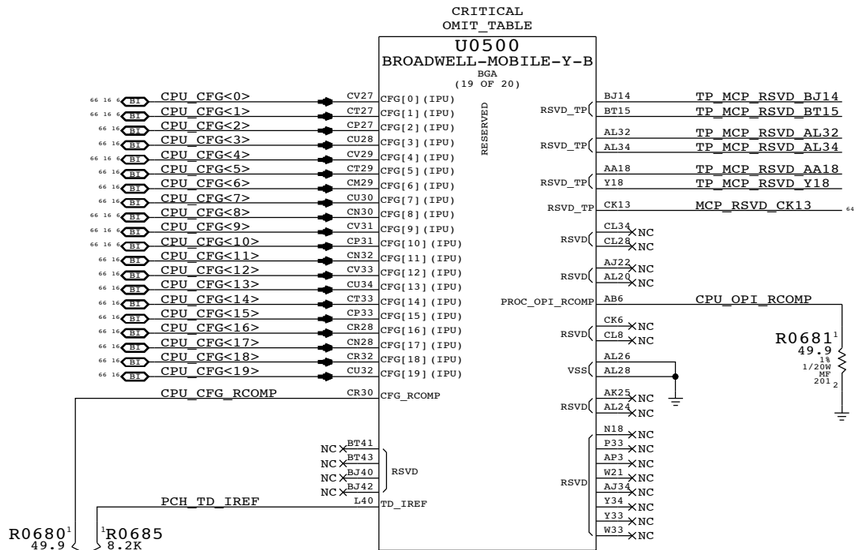
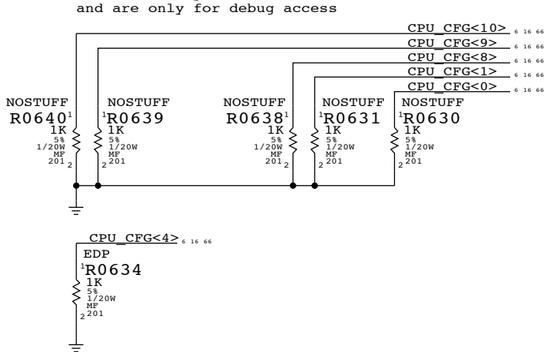




TBD: Confirm w/ Intel which still apply for BDW-Y

CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 =	POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 =	VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 =	NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 =	ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 =	PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 =	STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



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CPU Misc/JTAG/CFG/RSVD

Apple Inc.

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CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
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MEMORY CHANNEL A

MEM_A_DQ<0>	CT17	SA_DQ0	SA_CLK0*	CG4	MEM_A_CLK_N<0>	OUT 20 69
MEM_A_DQ<1>	CV17	SA_DQ1	SA_CLK0	CG2	MEM_A_CLK_P<0>	OUT 20 69
MEM_A_DQ<2>	CN14	SA_DQ2	SA_CLK1*	CC4	MEM_A_CLK_N<1>	OUT 20 69
MEM_A_DQ<3>	CP15	SA_DQ3	SA_CLK1	CC6	MEM_A_CLK_P<1>	OUT 20 69
MEM_A_DQ<4>	CN16	SA_DQ4				
MEM_A_DQ<5>	CR16	SA_DQ5	SA_CKE0	CH11	MEM_A_CKE<0>	OUT 20 69
MEM_A_DQ<6>	CM13	SA_DQ6	SA_CKE1	CH9	MEM_A_CKE<1>	OUT 20 69
MEM_A_DQ<7>	CV15	SA_DQ7	SA_CKE2	CA12	MEM_A_CKE<2>	OUT 20 69
MEM_A_DQ<8>	CT13	SA_DQ8	SA_CKE3	CA10	MEM_A_CKE<3>	OUT 20 69
MEM_A_DQ<9>	CP13	SA_DQ9				
MEM_A_DQ<10>	CP10	SA_DQ10	SA_CS0*	CA4	MEM_A_CS_L<0>	OUT 20 69
MEM_A_DQ<11>	CM10	SA_DQ11	SA_CS1*	CA2	MEM_A_CS_L<1>	OUT 20 69
MEM_A_DQ<12>	CN12	SA_DQ12				
MEM_A_DQ<13>	CV13	SA_DQ13	SA_ODT0	CA6	MEM_A_ODT<0>	OUT 20 61 69
MEM_A_DQ<14>	CV10	SA_DQ14				
MEM_A_DQ<15>	CT10	SA_DQ15	SA_CAB3	CE2	=MEM_A_RAS_L	OUT 61
MEM_A_DQ<16>	CT25	SA_DQ16	SA_CAB2	CE4	=MEM_A_WE_L	OUT 61
MEM_A_DQ<17>	CP25	SA_DQ17	SA_CAB1	CC8	=MEM_A_CAS_L	OUT 61
MEM_A_DQ<18>	CN22	SA_DQ18				
MEM_A_DQ<19>	CP23	SA_DQ19	SA_CAB4	CB5	=MEM_A_BA<0>	OUT 61
MEM_A_DQ<20>	CN24	SA_DQ20	SA_CAB6	CC2	MEM_A_CAB<6>	OUT 20 61 69
MEM_A_DQ<21>	CV25	SA_DQ21	SA_CAA5	CF11	=MEM_A_BA<2>	OUT 61
MEM_A_DQ<22>	CV23	SA_DQ22				
MEM_A_DQ<23>	CT23	SA_DQ23	SA_CAB9	CE8	=MEM_A_A<0>	OUT 61
MEM_A_DQ<24>	CN20	SA_DQ24	SA_CAB8	CE12	=MEM_A_A<1>	OUT 61
MEM_A_DQ<25>	CN18	SA_DQ25	SA_CAB5	CF5	=MEM_A_A<2>	OUT 61
MEM_A_DQ<26>	CT21	SA_DQ26		CE10	TP_LPDDR3_RSVD1	OUT 61
MEM_A_DQ<27>	CT19	SA_DQ27	NOTUSED	CG8	TP_LPDDR3_RSVD2	OUT 61
MEM_A_DQ<28>	CP19	SA_DQ28	SA_CAA0	CG6	=MEM_A_A<5>	OUT 61
MEM_A_DQ<29>	CP21	SA_DQ29	SA_CAA2	CH3	=MEM_A_A<6>	OUT 61
MEM_A_DQ<30>	CV19	SA_DQ30	SA_CAA4	CE6	=MEM_A_A<7>	OUT 61
MEM_A_DQ<31>	CV21	SA_DQ31	SA_CAA3	CB9	=MEM_A_A<8>	OUT 61
MEM_A_DQ<32>	BU2	SA_DQ32	SA_CAA1	CC12	=MEM_A_A<9>	OUT 61
MEM_A_DQ<33>	BW2	SA_DQ33	SA_CAB7	CF3	=MEM_A_A<10>	OUT 61
MEM_A_DQ<34>	BW6	SA_DQ34	SA_CAA7	CG12	=MEM_A_A<11>	OUT 61
MEM_A_DQ<35>	BU4	SA_DQ35	SA_CAA6	CH5	MEM_A_CAA<6>	OUT 20 61 69
MEM_A_DQ<36>	BW4	SA_DQ36	SA_CAB0	CB3	=MEM_A_A<13>	OUT 61
MEM_A_DQ<37>	BT3	SA_DQ37	SA_CAA9	CF9	=MEM_A_A<14>	OUT 61
MEM_A_DQ<38>	BU6	SA_DQ38	SA_CAA8	CG10	=MEM_A_A<15>	OUT 61
MEM_A_DQ<39>	BT5	SA_DQ39				
MEM_A_DQ<40>	BN2	SA_DQ40	SA_DQSN0	CU16	MEM_A_DQS_N<0>	BI 61 69
MEM_A_DQ<41>	BR2	SA_DQ41	SA_DQSN1	CR12	MEM_A_DQS_N<1>	BI 61 69
MEM_A_DQ<42>	BN6	SA_DQ42	SA_DQSN2	CR24	MEM_A_DQS_N<2>	BI 61 69
MEM_A_DQ<43>	BN4	SA_DQ43	SA_DQSN3	CR20	MEM_A_DQS_N<3>	BI 61 69
MEM_A_DQ<44>	BR6	SA_DQ44	SA_DQSN4	BV3	MEM_A_DQS_N<4>	BI 61 69
MEM_A_DQ<45>	BR4	SA_DQ45	SA_DQSN5	BP3	MEM_A_DQS_N<5>	BI 61 69
MEM_A_DQ<46>	BM5	SA_DQ46	SA_DQSN6	BV9	MEM_A_DQS_N<6>	BI 20 61 69
MEM_A_DQ<47>	BM3	SA_DQ47	SA_DQSN7	BP9	MEM_A_DQS_N<7>	BI 61 69
MEM_A_DQ<48>	BT11	SA_DQ48				
MEM_A_DQ<49>	BU10	SA_DQ49	SA_DQSP0	CT15	MEM_A_DQS_P<0>	BI 61 69
MEM_A_DQ<50>	BW12	SA_DQ50	SA_DQSP1	CU12	MEM_A_DQS_P<1>	BI 61 69
MEM_A_DQ<51>	BW10	SA_DQ51	SA_DQSP2	CU24	MEM_A_DQS_P<2>	BI 61 69
MEM_A_DQ<52>	BW8	SA_DQ52	SA_DQSP3	CU20	MEM_A_DQS_P<3>	BI 61 69
MEM_A_DQ<53>	BU8	SA_DQ53	SA_DQSP4	BV5	MEM_A_DQS_P<4>	BI 61 69
MEM_A_DQ<54>	BU12	SA_DQ54	SA_DQSP5	BP5	MEM_A_DQS_P<5>	BI 61 69
MEM_A_DQ<55>	BT9	SA_DQ55	SA_DQSP6	BV11	MEM_A_DQS_P<6>	BI 20 61 69
MEM_A_DQ<56>	BN8	SA_DQ56	SA_DQSP7	BP11	MEM_A_DQS_P<7>	BI 61 69
MEM_A_DQ<57>	BR8	SA_DQ57				
MEM_A_DQ<58>	BN12	SA_DQ58	SM_VREF_CA	AP13	CPU_DIMM_VREFCA	OUT 19
MEM_A_DQ<59>	BN10	SA_DQ59	SM_VREF_DQ0	AU14	CPU_DIMMA_VREFDQ	OUT 19
MEM_A_DQ<60>	BR12	SA_DQ60	SM_VREF_DQ1	AT13	CPU_DIMMB_VREFDQ	OUT 19
MEM_A_DQ<61>	BR10	SA_DQ61	SM_VCCDDQG	CC14	TP_ULX_DDR_VCCDDQG	64
MEM_A_DQ<62>	BM11	SA_DQ62				
MEM_A_DQ<63>	BM9	SA_DQ63				

CRITICAL
OMIT_TABLE

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BROADWELL-MOBILE-Y-B
BGA
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MEMORY CHANNEL B

MEM_B_DQ<0>	BK3	SB_DQ0	SB_CK0*	AW6	MEM_B_CLK_N<0>	OUT 21 64 69
MEM_B_DQ<1>	BK5	SB_DQ1	SB_CK0	AW4	MEM_B_CLK_P<0>	OUT 21 64 69
MEM_B_DQ<2>	BG6	SB_DQ2	SB_CK1*	AP11	MEM_B_CLK_N<1>	OUT 21 69
MEM_B_DQ<3>	BJ2	SB_DQ3	SB_CK1	AP9	MEM_B_CLK_P<1>	OUT 21 69
MEM_B_DQ<4>	BJ4	SB_DQ4				
MEM_B_DQ<5>	BJ6	SB_DQ5	SB_CKE0	BA2	MEM_B_CKE<0>	OUT 21 69
MEM_B_DQ<6>	BG2	SB_DQ6	SB_CKE1	BA4	MEM_B_CKE<1>	OUT 21 64 69
MEM_B_DQ<7>	BG4	SB_DQ7	SB_CKE2	AR8	MEM_B_CKE<2>	OUT 21 69
MEM_B_DQ<8>	BF3	SB_DQ8	SB_CKE3	AP5	MEM_B_CKE<3>	OUT 21 69
MEM_B_DQ<9>	BF5	SB_DQ9				
MEM_B_DQ<10>	BC6	SB_DQ10	SB_CS0*	AR10	MEM_B_CS_L<0>	OUT 21 64 69
MEM_B_DQ<11>	BE2	SB_DQ11	SB_CS1*	AT11	MEM_B_CS_L<1>	OUT 21 64 69
MEM_B_DQ<12>	BE4	SB_DQ12				
MEM_B_DQ<13>	BE6	SB_DQ13	SB_ODT0	AU10	MEM_B_ODT<0>	OUT 21 61 69
MEM_B_DQ<14>	BC2	SB_DQ14				
MEM_B_DQ<15>	BC4	SB_DQ15	SB_CAB3	BA10	=MEM_B_RAS_L	OUT 61
MEM_B_DQ<16>	BE10	SB_DQ16	SB_CAB2	AW12	=MEM_B_WE_L	OUT 61
MEM_B_DQ<17>	BC10	SB_DQ17	SB_CAB1	AW10	=MEM_B_CAS_L	OUT 61
MEM_B_DQ<18>	BE8	SB_DQ18				
MEM_B_DQ<19>	BC8	SB_DQ19	SB_CAB4	AY11	=MEM_B_BA<0>	OUT 61
MEM_B_DQ<20>	BF11	SB_DQ20	SB_CAB6	BA12	MEM_B_CAB<6>	OUT 21 61 69
MEM_B_DQ<21>	BC12	SB_DQ21	SB_CAA5	AU2	=MEM_B_BA<2>	OUT 61
MEM_B_DQ<22>	BE12	SB_DQ22				
MEM_B_DQ<23>	BF9	SB_DQ23	SB_CAB9	AT9	=MEM_B_A<0>	OUT 61
MEM_B_DQ<24>	BJ12	SB_DQ24	SB_CAB8	AR4	=MEM_B_A<1>	OUT 61
MEM_B_DQ<25>	BG12	SB_DQ25	SB_CAB5	AU8	=MEM_B_A<2>	OUT 61
MEM_B_DQ<26>	BJ8	SB_DQ26		AR6	TP_LPDDR3_RSVD3	OUT 61
MEM_B_DQ<27>	BJ10	SB_DQ27	NOTUSED	AT5	TP_LPDDR3_RSVD4	OUT 61
MEM_B_DQ<28>	BG8	SB_DQ28	SB_CAA0	AT3	=MEM_B_A<5>	OUT 61
MEM_B_DQ<29>	BG10	SB_DQ29	SB_CAA2	BA8	=MEM_B_A<6>	OUT 61
MEM_B_DQ<30>	BK9	SB_DQ30	SB_CAA4	AY3	=MEM_B_A<7>	OUT 61
MEM_B_DQ<31>	BK11	SB_DQ31	SB_CAA3	AW2	=MEM_B_A<8>	OUT 61
MEM_B_DQ<32>	AM1	SB_DQ32	SB_CAA1	AY5	=MEM_B_A<9>	OUT 61
MEM_B_DQ<33>	AH2	SB_DQ33	SB_CAB7	AY9	=MEM_B_A<10>	OUT 61
MEM_B_DQ<34>	AJ3	SB_DQ34	SB_CAA7	AU4	=MEM_B_A<11>	OUT 61
MEM_B_DQ<35>	AM5	SB_DQ35	SB_CAA6	AU6	MEM_B_CAA<6>	OUT 21 61 69
MEM_B_DQ<36>	AM3	SB_DQ36	SB_CAB0	AW8	=MEM_B_A<13>	OUT 61
MEM_B_DQ<37>	AJ1	SB_DQ37	SB_CAA9	BA6	=MEM_B_A<14>	OUT 61
MEM_B_DQ<38>	AJ5	SB_DQ38	SB_CAA8	AR2	=MEM_B_A<15>	OUT 61
MEM_B_DQ<39>	AH4	SB_DQ39				
MEM_B_DQ<40>	AG3	SB_DQ40	SB_DQSN0	BH5	MEM_B_DQS_N<0>	BI 61 64 69
MEM_B_DQ<41>	AG1	SB_DQ41	SB_DQSN1	BD5	MEM_B_DQS_N<1>	BI 61 69
MEM_B_DQ<42>	AD2	SB_DQ42	SB_DQSN2	BD11	MEM_B_DQS_N<2>	BI 61 69
MEM_B_DQ<43>	AE3	SB_DQ43	SB_DQSN3	BH11	MEM_B_DQS_N<3>	BI 61 69
MEM_B_DQ<44>	AE1	SB_DQ44	SB_DQSN4	AK2	MEM_B_DQS_N<4>	BI 61 69
MEM_B_DQ<45>	AG5	SB_DQ45	SB_DQSN5	AF2	MEM_B_DQS_N<5>	BI 61 69
MEM_B_DQ<46>	AD4	SB_DQ46	SB_DQSN6	AK8	MEM_B_DQS_N<6>	BI 21 61 69
MEM_B_DQ<47>	AE5	SB_DQ47	SB_DQSN7	AF8	MEM_B_DQS_N<7>	BI 61 69
MEM_B_DQ<48>	AM9	SB_DQ48				
MEM_B_DQ<49>	AM7	SB_DQ49	SB_DQSP0	BH3	MEM_B_DQS_P<0>	BI 61 64 69
MEM_B_DQ<50>	AH8	SB_DQ50	SB_DQSP1	BD3	MEM_B_DQS_P<1>	BI 61 69
MEM_B_DQ<51>	AJ9	SB_DQ51	SB_DQSP2	BD9	MEM_B_DQS_P<2>	BI 61 69
MEM_B_DQ<52>	AM11	SB_DQ52	SB_DQSP3	BH9	MEM_B_DQS_P<3>	BI 61 69
MEM_B_DQ<53>	AJ7	SB_DQ53	SB_DQSP4	AK4	MEM_B_DQS_P<4>	BI 61 69
MEM_B_DQ<54>	AJ11	SB_DQ54	SB_DQSP5	AF4	MEM_B_DQS_P<5>	BI 61 69
MEM_B_DQ<55>	AH10	SB_DQ55	SB_DQSP6	AK10	MEM_B_DQS_P<6>	BI 21 61 69
MEM_B_DQ<56>	AE11	SB_DQ56	SB_DQSP7	AF10	MEM_B_DQS_P<7>	BI 61 69
MEM_B_DQ<57>	AG7	SB_DQ57				
MEM_B_DQ<58>	AE7	SB_DQ58				
MEM_B_DQ<59>	AE9	SB_DQ59				
MEM_B_DQ<60>	AG11	SB_DQ60				
MEM_B_DQ<61>	AG9	SB_DQ61				
MEM_B_DQ<62>	AD8	SB_DQ62				
MEM_B_DQ<63>	AD10	SB_DQ63				

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PAGE TITLE
CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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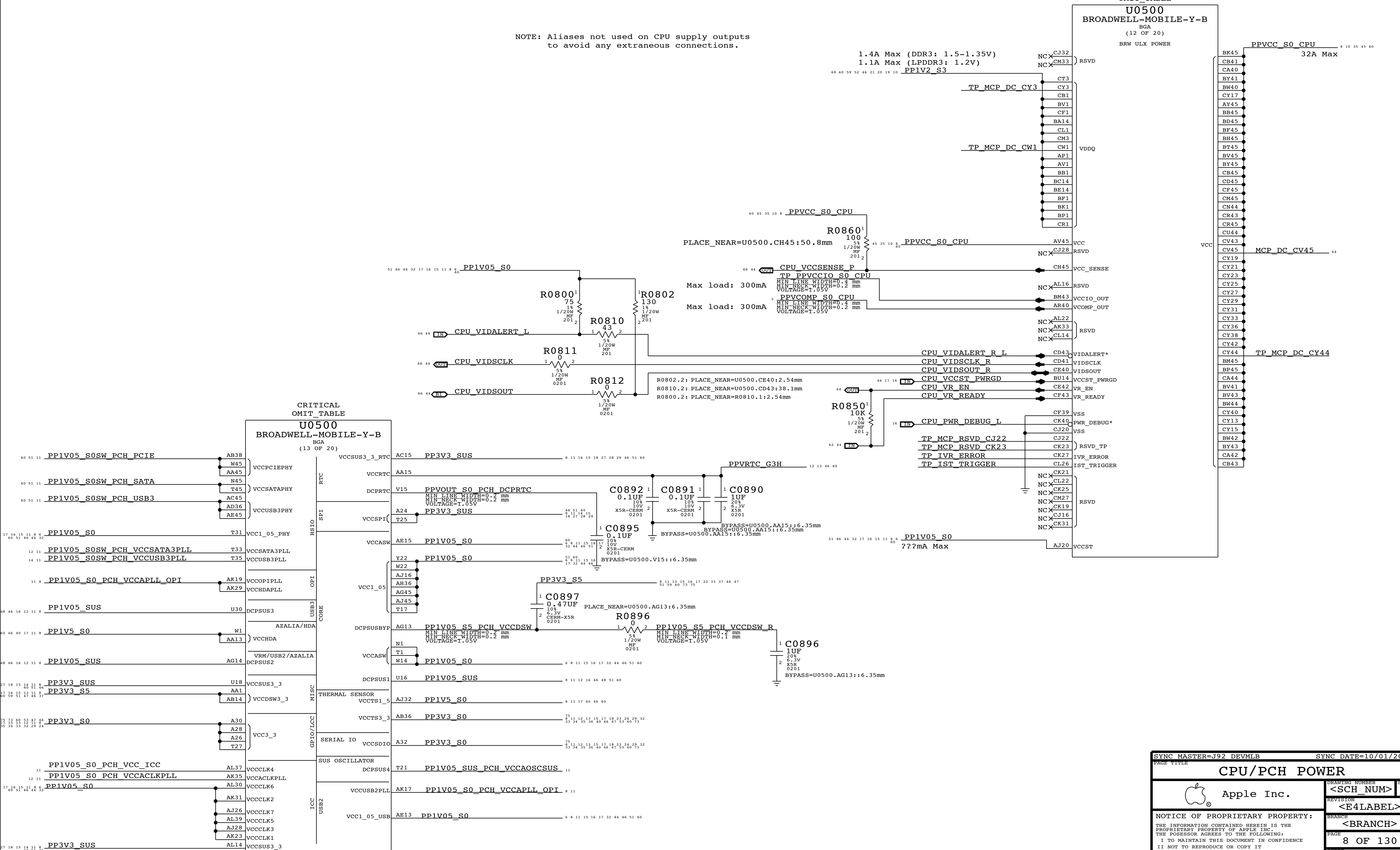
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.



CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(12 OF 20)
BRW ULX POWER
1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)
PP1V2_S3
TP_MCP_DC_CY3
TP_MCP_DC_CW1
VDDQ
RSVD
PPVCC_S0_CPU
32A Max
MCP_DC_CV45
TP_MCP_DC_CY44
VCC
R0860
100
PLACE_NEAR=U0500.CH45:50.8mm
CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
PPVCOMP_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
VCC_SENSE
VCCIO_OUT
VCOMP_OUT
PP1V05_S0
R0800
75
R0802
130
R0810
43
R0811
0
R0812
0
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0802.2: PLACE_NEAR=U0500.CE40:2.54mm
R0810.2: PLACE_NEAR=U0500.CD43:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
R0850
10K
CPU_PWR_DEBUG_L
TP_MCP_RSVD_CJ22
TP_MCP_RSVD_CK23
TP_IVR_ERROR
TP_IST_TRIGGER
VIDALERT*
VIDSCLK
VIDSOUT
VCCST_PWRGD
VR_EN
VR_READY
VSS
PWR_DEBUG*
RSVD_TP
IVR_ERROR
IST_TRIGGER
???mA Max
VCCST
CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(13 OF 20)
WPT LP POWER
PP1V05_S0SW_PCH_PCIE
PP1V05_S0SW_PCH_SATA
PP1V05_S0SW_PCH_USB3
PP1V05_S0SW_PCH_VCCSATA3PLL
PP1V05_S0SW_PCH_VCCUSB3PLL
PP1V05_S0_PCH_VCCAPLL_OPI
PP1V05_SUS
PP1V5_S0
PP3V3_SUS
PP3V3_S5
PP3V3_S0
PP1V05_S0_PCH_VCC_ICC
PP1V05_S0_PCH_VCCACLKPLL
PPVRTC_G3H
PPVOUT_S0_PCH_DCPRTC
C0892
0.1UF
C0891
0.1UF
C0890
1UF
C0895
0.1UF
BYPASS=U0500.AA15::6.35mm
BYPASS=U0500.V15::6.35mm
C0897
0.47UF
PLACE_NEAR=U0500.AG13:6.35mm
R0896
0
PP1V05_S5_PCH_VCCDSW
PP1V05_S5_PCH_VCCDSW_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
C0896
1UF
BYPASS=U0500.AG13::6.35mm
PP1V05_SUS_PCH_VCCAOSCSUS
PP1V05_S0_PCH_VCCAPLL_OPI

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/01/2013

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CPU/PCH POWER

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CRITICAL
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U0500
BROADWELL-MOBILE-Y-B
BGA
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AH29			AY13
AM19			AY15
AH6			AY39
AH31			BA44
AH30			BB3
AH33			BB5
AH32			BB7
AH34			BB9
AH44			BB11
AJ39			BB13
AJ30			BB15
AJ37			BB39
AK6			BC44
AJ18			BD1
AM17			BD7
AN6			BD13
AR42			BD15
AK12			BD39
AK21			BE40
AK27			BE42
BE44			BF7
AM13			BF13
BL8			BF15
CJ18			BF39
CJ24			BG14
AM21			BG44
AM23			BH1
AM25			BH7
AM27			BH13
AM29			BH15
AM31	VSS	VSS	BH39
AM35			BH41
CJ30			BH43
AM45			BJ44
CL5			BK7
AN2			BK13
AN4			BK15
CL24			BK39
AN8			BL2
AN10			BL4
AN12			BL6
AN14			BL10
AN40			BL12
AN42			BL40
AN44			BL42
AP7			BL44
AP15			BM1
AP43			BM7
CN1			BM13
AT1			BM39
AT7			BN44
AT15			BP13
AT39			CH1
AT45			CH15
AU44			CV39
AV13			CV41
AV15			CW12
AV39			CW14
AW44			CW16
CU1			CW18
AY1			AJ24
AY7			AP39
CV3			

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(15 OF 20)

L24		CW20
L16		AM39
H10		L32
H36		CN42
CN26		CP3
BP7		CP17
BP39		CP29
BR44		CR8
BT1		CR14
BT7		CR18
BT13		CR22
J16		CR26
BT39		CR37
BU44		CT31
BV7		CU8
BV13		CU14
BV15		CU18
BV39		CU22
BY1		CU26
BY3		CU42
BY5		CV35
BY7		CV37
BY9		CW5
BY11		CW8
BY13		CW22
BY15		CW24
BY39		CW26
C16		CW28
C20		CW32
C24		CW34
C28		CY7
C32	VSS	CY10
C36		D10
CB7		G28
CB13		J24
CB15		J28
CB39		CD9
CC40		CD5
CC42		CD3
CC44		CC10
CD1		CA8
CD7		AW14
CD13		AR14
CD15		AG39
CD39		BU40
CE44		BU42
CF7		L2
CF13		L20
CF15		L28
CG44		CD11
CH13		G32
CJ26		CW30
CK3		J20
CK10		J32
CK38		
CK44		
CL12		
CM15		
CM17		
CM19		
CM21		
CM23		
CM25		
CM31		
CM35		
CM43		
CN8		

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(20 OF 20)

T23		AD32
AR12		AH14
AU12		AH12
AV3		AG37
AV5		AG35
AV9		AG32
AC1		AG28
AC24		AG24
AC19		AG19
AH15		AF44
AB16		AF16
AB15		AF14
AB12		AF12
AB8		AF6
AA37		AE37
AA35		AE35
AC13		AE32
AA34		AE28
AA33		AE24
AA32		AE19
AA30		AE16
AA29		AD44
AA28		AD28
AB40		AD24
AA26		AD19
AA25	VSS	AD16
AA24		AD12
AA22		AD6
AA21		AC43
AA19		AC41
AA7		AC37
AA5		AC35
AA39		AC9
AA3		AC7
A40		AC3
A36		AB44
A20		AC28
A10		AD14
BM15		AC11
BP15		AC5
CN5		W18
CR5		W16
CU5		V44
W28		U20
W24		U14
W19		T19
AH22		AH28
AH21		AH27
AH20		AH26
AH19		AH25
AH17		AH23
		AV11
		AH16
		H4
		A16
		T29

CRITICAL
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U0500
BROADWELL-MOBILE-Y-B
BGA
(16 OF 20)

U22		CH7
G20		V2
E20		E16
N24		U24
N28		R30
N32		N20
P35		AK15
R2		AM33
R4		AK44
R6		CA14
R8		U28
R10	VSS	U32
E24		V17
R16		V40
R22		R44
E28		T15
R24		F5
R26		G16
R28		R18
AV7		U26
E32		U34
E36		G24
R20		N16
		AJ13
		AC32
	VSS_SENSE	CH43

CPU_VCCSENSE_N OUT

R0960
100
5% 1/20W MF 201
PLACE_NEAR=U0500.CH43:50.8mm

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(17 OF 20)

J43		CL32
J1		CL30
D42		CK33
A42		CK29
Y44		CJ34
W32		CG14
W35		CE14
Y2		BW14
Y12		BR14
Y14	VSS	BN14
Y16		AF36
W34		AA11
W30		Y19
T13		Y24
L38		Y28
Y42		Y32
A6		Y40
D4		J3
H42		J45

SYNC_MASTER=J92_WILL SYNC_DATE=04/10/2013

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CPU/PCH GROUNDS

Apple Inc.

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 16x 10uF 0402 stuff, 12x 10uF 0402 nostuff

60 45 35 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402-1
CRITICAL C1001 10UF 20% 4V X6S 0402-1
CRITICAL C1002 10UF 20% 4V X6S 0402-1
CRITICAL C1003 10UF 20% 4V X6S 0402-1
CRITICAL C1004 10UF 20% 4V X6S 0402-1
NO STUFF C1005 10UF 20% 4V X6S 0402-1
NO STUFF C1006 10UF 20% 4V X6S 0402-1
CRITICAL C1007 10UF 20% 4V X6S 0402-1
NO STUFF C1008 10UF 20% 4V X6S 0402-1
CRITICAL C1009 10UF 20% 4V X6S 0402-1
C1011 10UF 20% 4V X6S 0402-1
C1012 10UF 20% 4V X6S 0402-1
NO STUFF C1013 10UF 20% 4V X6S 0402-1
C1014 10UF 20% 4V X6S 0402-1

NO STUFF C1015 10UF 20% 4V X6S 0402-1
CRITICAL C1016 10UF 20% 4V X6S 0402-1
NO STUFF C1017 10UF 20% 4V X6S 0402-1
CRITICAL C1018 10UF 20% 4V X6S 0402-1
CRITICAL C1019 10UF 20% 4V X6S 0402-1
CRITICAL C1020 10UF 20% 4V X6S 0402-1
NO STUFF C1021 10UF 20% 4V X6S 0402-1
CRITICAL C1022 10UF 20% 4V X6S 0402-1
CRITICAL C1023 10UF 20% 4V X6S 0402-1
NO STUFF C1025 10UF 20% 4V X6S 0402-1
C1026 10UF 20% 4V X6S 0402-1
NO STUFF C1027 10UF 20% 4V X6S 0402-1
NO STUFF C1028 10UF 20% 4V X6S 0402-1
NO STUFF C1029 10UF 20% 4V X6S 0402-1
C1030 12PF 5% 25V CERM 0201

CRITICAL C1031 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1032 210UF 20% 2.5V POLY-TANT CASE-B2S

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

59 52 46 21 20 19 8 69 60 PP1V2_S3

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

Added 2 extra 2.2uF per Harris Beach v0.9 schematic

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/01/2013

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Apple Inc.

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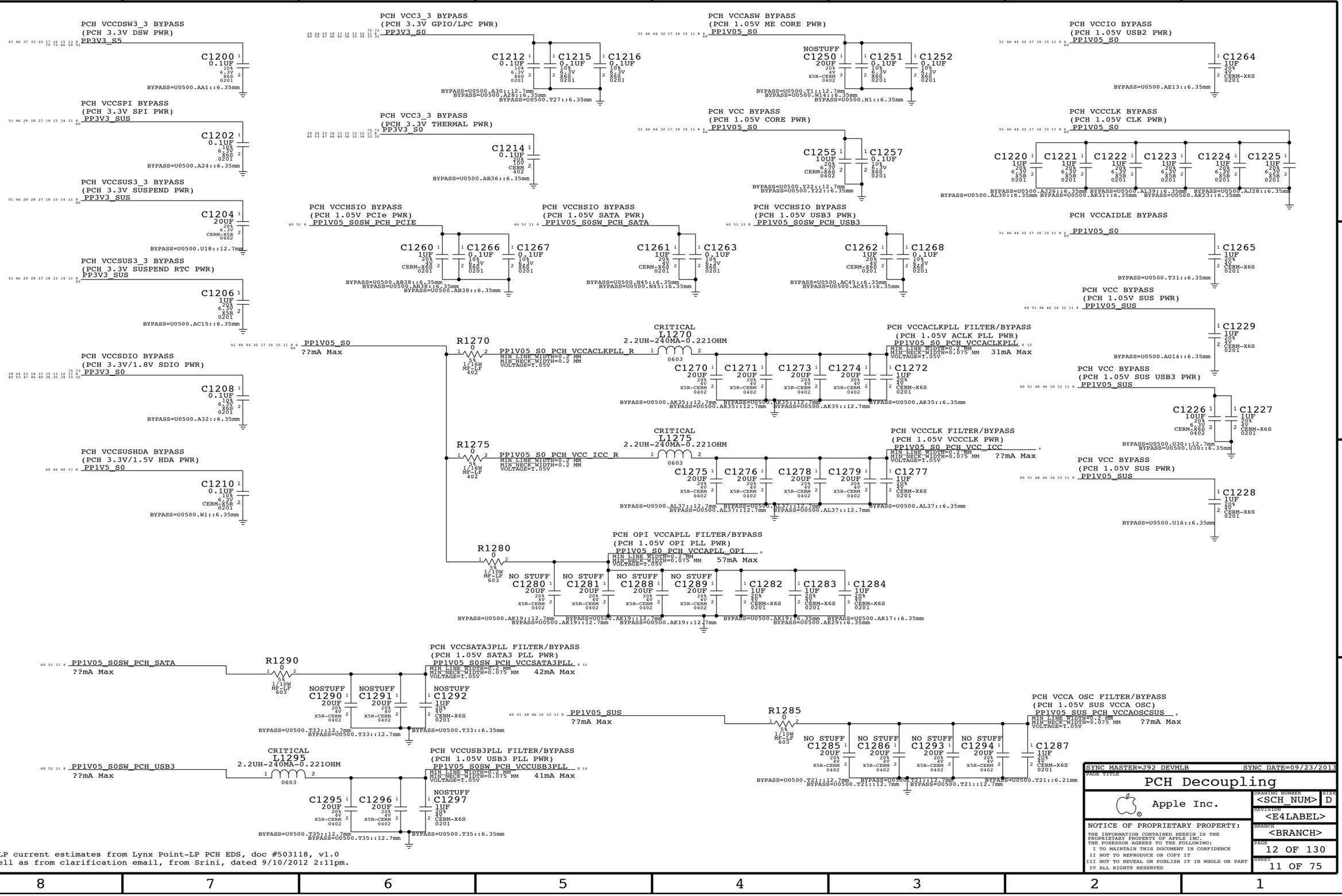
PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
C1200 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA1::6.35mm
PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
C1202 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A24::6.35mm
PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.U18::12.7mm
PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AC15::6.35mm
PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A32::6.35mm
PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0
C1210 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U0500.W1::6.35mm
PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 0.1UF 10% 6.3V X6S 0201
C1215 0.1UF 10% 6.3V X6S 0201
C1216 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A30::12.7mm
BYPASS=U0500.A28::6.35mm
BYPASS=U0500.T27::6.35mm
PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.AB36::6.35mm
PCH VCCHSIO BYPASS
(PCH 1.05V PCIe PWR)
PP1V05_S0SW_PCH_PCIE
C1260 1UF 20% 4V CERM-X6S 0201
C1266 0.1UF 10% 6.3V X6S 0201
C1267 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AB38::6.35mm
BYPASS=U0500.AB38::6.35mm
BYPASS=U0500.AB38::6.35mm
PCH VCCHSIO BYPASS
(PCH 1.05V SATA PWR)
PP1V05_S0SW_PCH_SATA
C1261 1UF 20% 4V CERM-X6S 0201
C1263 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.N45::6.35mm
BYPASS=U0500.N45::6.35mm
PCH VCCHSIO BYPASS
(PCH 1.05V USB3 PWR)
PP1V05_S0SW_PCH_USB3
C1262 1UF 20% 4V CERM-X6S 0201
C1268 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AC45::6.35mm
BYPASS=U0500.AC45::6.35mm
PP1V05_S0
??mA Max
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max
C1270 20UF 20% 4V X5R-CERM 0402
C1271 20UF 20% 4V X5R-CERM 0402
C1273 20UF 20% 4V X5R-CERM 0402
C1274 20UF 20% 4V X5R-CERM 0402
C1272 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::6.35mm
R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
C1275 20UF 20% 4V X5R-CERM 0402
C1276 20UF 20% 4V X5R-CERM 0402
C1278 20UF 20% 4V X5R-CERM 0402
C1279 20UF 20% 4V X5R-CERM 0402
C1277 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::6.35mm
R1280 0 5% 1/10W MF-LF 603
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max
NO STUFF C1280 20UF 20% 4V X5R-CERM 0402
NO STUFF C1281 20UF 20% 4V X5R-CERM 0402
NO STUFF C1288 20UF 20% 4V X5R-CERM 0402
NO STUFF C1289 20UF 20% 4V X5R-CERM 0402
C1282 1UF 20% 4V CERM-X6S 0201
C1283 1UF 20% 4V CERM-X6S 0201
C1284 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::6.35mm
BYPASS=U0500.AK17::6.35mm
BYPASS=U0500.AK29::6.35mm
PP1V05_S0SW_PCH_SATA
??mA Max
R1290 0 5% 1/10W MF-LF 603
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max
NOSTUFF C1290 20UF 20% 4V X5R-CERM 0402
NOSTUFF C1291 20UF 20% 4V X5R-CERM 0402
NOSTUFF C1292 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T33::12.7mm
BYPASS=U0500.T33::12.7mm
BYPASS=U0500.T33::6.35mm
PP1V05_S0SW_PCH_USB3
??mA Max
CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max
C1295 20UF 20% 4V X5R-CERM 0402
C1296 20UF 20% 4V X5R-CERM 0402
NOSTUFF C1297 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T35::12.7mm
BYPASS=U0500.T35::12.7mm
BYPASS=U0500.T35::6.35mm
PP1V05_SUS
??mA Max
R1285 0 5% 1/10W MF-LF 603
PCH VCCA OSC FILTER/BYPASS
(PCH 1.05V SUS VCCA OSC)
PP1V05_SUS_PCH_VCCAOSCSUS
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
NO STUFF C1285 20UF 20% 4V X5R-CERM 0402
NO STUFF C1286 20UF 20% 4V X5R-CERM 0402
NO STUFF C1293 20UF 20% 4V X5R-CERM 0402
NO STUFF C1294 20UF 20% 4V X5R-CERM 0402
C1287 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::6.21mm
PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AE13::6.35mm
PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1220 1UF 20% 6.3V X5R 0201
C1221 1UF 20% 6.3V X5R 0201
C1222 1UF 20% 6.3V X5R 0201
C1223 1UF 20% 6.3V X5R 0201
C1224 1UF 20% 6.3V X5R 0201
C1225 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AJ26::6.35mm
BYPASS=U0500.AL39::6.35mm
BYPASS=U0500.AJ28::6.35mm
BYPASS=U0500.AL30::6.35mm
BYPASS=U0500.AK31::6.35mm
BYPASS=U0500.AK23::6.35mm
PCH VCCAIDLE BYPASS
PP1V05_S0
C1265 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T31::6.35mm
PCH VCC BYPASS
(PCH 1.05V SUS PWR)
PP1V05_SUS
C1229 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AG14::6.35mm
PCH VCC BYPASS
(PCH 1.05V SUS USB3 PWR)
PP1V05_SUS
C1226 10UF 20% 6.3V CERM-X6S 0402
C1227 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.U30::12.7mm
BYPASS=U0500.U30::6.35mm
PCH VCC BYPASS
(PCH 1.05V SUS PWR)
PP1V05_SUS
C1228 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.U16::6.35mm
PCH VCC BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NOSTUFF C1250 20UF 20% 4V X5R-CERM 0402
C1251 0.1UF 10% 6.3V X6S 0201
C1252 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.T1::12.7mm
BYPASS=U0500.W14::6.35mm
BYPASS=U0500.N1::6.35mm
PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V CERM-X6S 0402
C1257 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.Y22::12.7mm
BYPASS=U0500.Y22::6.35mm
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.
SYNC_MASTER=J92_DEVMLB
SYNC_DATE=09/23/2013
PAGE TITLE
PCH Decoupling
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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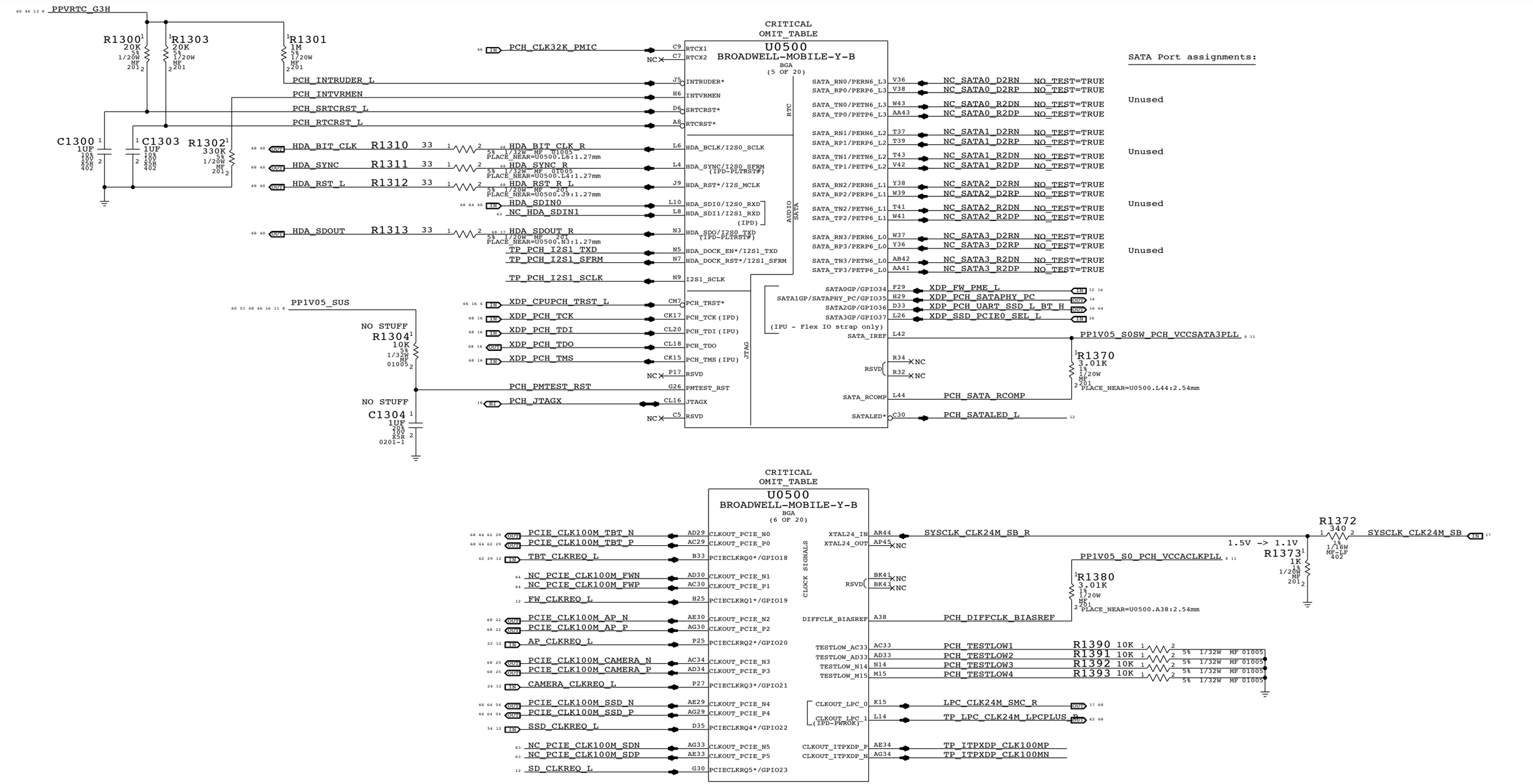

SYNC_MASTER=J92 WILL SYNC_DATE=04/10/2013

PAGE TITLE
PCH Audio/JTAG/SATA/CLK

Apple Inc.

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CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(8 OF 20)
SYSTEM POWER MANAGEMENT

62 31	SMC_PCH_SUSACK_L	D19	SUSACK* (IPU)		
31 17 IN	PM_SYSRST_L	E26	SYS_RESET*		
46 31 16 IN	PM_PCH_SYS_PWROK	A22	SYS_PWROK		
46 IN	PM_PCH_PWROK	F9	PCH_PWROK		
46 IN	PM_PCH_APWROK	J22	APWROK		
18 16 15 OUT	PLT_RESET_L	M23	PLTRST*		
32 IN	PM_RSMRST_L	F7	RSMRST*		
62 31	SMC_PCH_SUSWARN_L	D8	SUSWARN*/SUSPWRDNACK/GPIO30		
31 16 13 IN	PM_PWRBTN_L	M21	PWRBTN* (IPU)		
32 31 IN	SMC_ADAPTER_EN	M17	ACPRESENT/GPIO31 (IPD-DeepSx)		
31 13 IN	PM_BATLOW_L	H17	BATLOW*/GPIO72		
75 46 33 31 13 OUT	PM_SLP_S0_L	G22	SLP_S0*		
	TP_PCH_SLP_WLAN_L	J18	SLP_WLAN*/GPIO29		
				DSWVRMEN G14	PCH_DSWVRMEN
				DPWROK J7	PM_DSW_PWRGD
				(IPD-DeepSx)WAKE* F19	PCIE_WAKE_L IN 13 22
				CLKRUN*/GPIO32 B35	PM_CLKRUN_L BI 13 31
				SUS_STAT*/GPIO61 D25	LPC_PWRDWN_L OUT 31
				SUSCLK/GPIO62 B27	PM_CLK32K_SUSCLK_R OUT 32 68
				SLP_S5*/GPIO63 A18	PM_SLP_S5_L OUT 13 31 51 52
				SLP_S4* H19	PM_SLP_S4_L OUT 13 15 31 46 52
				SLP_S3* N22	PM_SLP_S3_L OUT 13 31 46 52
				SLP_A* G18	PM_SLP_A_L OUT 13 46
				SLP_SUS* D27	PM_SLP_SUS_L OUT 13 46 51 52
				SLP_LAN* K19	TP_PCH_SLP_LAN_L

PPVRTC_G3H 8 12 46 60

R1450 330K 5% 1/32W MF 01005

NO STUFF
R1451 100K 5% 1/32W MF 01005

IN 33 46

NO STUFF
R1400 0.00 0% 1/32W MF 01005

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
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64 53 OUT	EDP_BKLT_PWM	BM41	EDP_BKLCTL	EDP SIDEBAND	DDPB_CTRLCLK BP43	DP_TBTSNK0_DDC_CLK OUT 18
49 13 OUT	EDP_BKLT_EN	BR42	EDP_BKLEN		DDPB_CTRLDATA (IPD-PLTRST#) BN42	DP_TBTSNK0_DDC_DATA BI 18
53 13 OUT	EDP_PANEL_PWR	BN40	EDP_VDDEN		DDPC_CTRLCLK BP41	NC_DP_TBTSNK1_DDC_CLK OUT 63
					DDPC_CTRLDATA (IPD-PLTRST#) BR40	NC_DP_TBTSNK1_DDC_DATA BI 63
64 62 28 13 IN	HPM_I2C_INT_L	K35	PIRQA*/GPIO77	DISPLAY PCI		
31 13 IN	SMC_RUNTIME_SCI_L	F31	PIRQB*/GPIO78			
63 13 IN	HDMITBTMUX_FLAG	J34	PIRQC*/GPIO79			
64 23 13 IN	SSD_BOOT	D38	PIRQD*/GPIO80			
63	NC_PCI_PME_L	B25	PME* (IPU)		DDPB_AUXN Y26	DP_TBTSNK0_AUXCH_C_N BI 29 66
					DDPC_AUXN Y25	NC_DP_TBTSNK1_AUXCH_CN BI 63
63 13 OUT	ODD_PWR_EN_L	M29	GPIO55		DDPB_AUXP W26	DP_TBTSNK0_AUXCH_C_P BI 29 66
63 13 OUT	HDMITBTMUX_LATCH	L30	GPIO52		DDPC_AUXP W25	NC_DP_TBTSNK1_AUXCH_CP BI 63
22 13 OUT	BT_LOW_PWR_L	F35	GPIO54			
64 40 13 OUT	AUD_PWR_EN	H33	GPIO51		DDPB_HPD Y30	DP_TBTSNK0_HPD IN 18
64 22 13 OUT	AP_PCIE_DEV_WAKE	C39	GPIO53		DDPC_HPD Y29	NC_DP_TBTSNK1_HPD IN 63
					EDP_HPD W29	DP_INT_HPD IN 53

PP3V3_S5 8 11 15 16 17 22 33 37 46 47 51 59 60 73 75
PP3V3_S0 8 11 12 15 17 18 23 24 29 32 33 34 35 36 40 46 47 53 60 73 75

R1405	1.00K	5% 1/32W MF 01005	PM_PWRBTN_L	13 16 31
R1410	10K	5% 1/32W MF 01005	PM_BATLOW_L	13 31
R1452	10K	5% 1/32W MF 01005	PCIE_WAKE_L	13 22
R1455	10K	5% 1/32W MF 01005	PM_CLKRUN_L	13 31
R1460	100K	5% 1/32W MF 01005	PM_SLP_S5_L	13 31 51 52
R1461	100K	5% 1/32W MF 01005	PM_SLP_S4_L	13 15 31 46 52
R1462	100K	5% 1/32W MF 01005	PM_SLP_S3_L	13 31 46 52
R1463	100K	5% 1/32W MF 01005	PM_SLP_S0_L	13 31 33 46 75
R1464	100K	5% 1/32W MF 01005	PM_SLP_SUS_L	13 46 51 52
R1465	100K	5% 1/32W MF 01005	PM_SLP_A_L	13 46
R1430	100K	5% 1/32W MF 01005	EDP_BKLT_EN	13 49
R1431	100K	5% 1/32W MF 01005	EDP_PANEL_PWR	13 53
R1440	100K	5% 1/32W MF 01005	HPM_I2C_INT_L	13 28 62 64
R1441	100K	5% 1/32W MF 01005	SMC_RUNTIME_SCI_L	13 31
R1442	100K	5% 1/32W MF 01005	HDMITBTMUX_FLAG	13 63
R1443	100K	5% 1/32W MF 01005	SSD_BOOT	13 23 64
	NO STUFF			
R1444	10K	5% 1/32W MF 01005	BT_LOW_PWR_L	13 22
R1445	100K	5% 1/32W MF 01005	ODD_PWR_EN_L	13 63
R1446	100K	5% 1/32W MF 01005	HDMITBTMUX_LATCH	13 63
R1447	10K	5% 1/32W MF 01005	BT_LOW_PWR_L	13 22
R1448	100K	5% 1/32W MF 01005	AUD_PWR_EN	13 40 64
R1449	100K	5% 1/32W MF 01005	AP_PCIE_DEV_WAKE	13 22 64

SYNC_MASTER=J92_WILL SYNC_DATE=04/10/2013

PAGE TITLE
PCH PM/PCI/GFX

Apple Inc.

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PCIe Port Assignments:

SSD lane 0

SSD lane 1

SSD lane 2

SSD lane 3

AirPort

Camera

Thunderbolt lane 0

Thunderbolt lane 1

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
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PCIE_SSD_D2R_N<0>	AF40	PERN5_L0	
PCIE_SSD_D2R_P<0>	AG41	PERP5_L0	
PCIE_SSD_R2D_C_N<0>	AU40	PETN5_L0	
PCIE_SSD_R2D_C_P<0>	AU42	PETP5_L0	
PCIE_SSD_D2R_N<1>	AD40	PERN5_L1	
PCIE_SSD_D2R_P<1>	AE41	PERP5_L1	
PCIE_SSD_R2D_C_N<1>	AW40	PETN5_L1	
PCIE_SSD_R2D_C_P<1>	AW42	PETP5_L1	
PCIE_SSD_D2R_N<2>	AE43	PERN5_L2	
PCIE_SSD_D2R_P<2>	AD42	PERP5_L2	
PCIE_SSD_R2D_C_N<2>	BA42	PETN5_L2	
PCIE_SSD_R2D_C_P<2>	BA40	PETP5_L2	
PCIE_SSD_D2R_N<3>	AF42	PERN5_L3	
PCIE_SSD_D2R_P<3>	AG43	PERP5_L3	
PCIE_SSD_R2D_C_N<3>	BB41	PETN5_L3	
PCIE_SSD_R2D_C_P<3>	BB43	PETP5_L3	
PCIE_AP_D2R_N	AD38	PERN3	
PCIE_AP_D2R_P	AC39	PERP3	
PCIE_AP_R2D_C_N	AY41	PETN3	
PCIE_AP_R2D_C_P	AY43	PETP3	
PCIE_CAMERA_D2R_N	AH38	PERN4	
PCIE_CAMERA_D2R_P	AH40	PERP4	
PCIE_CAMERA_R2D_C_N	AV41	PETN4	
PCIE_CAMERA_R2D_C_P	AV43	PETP4	
PCIE_TBT_D2R_N<0>	AP38	PERN1/USB3RN3	
PCIE_TBT_D2R_P<0>	AE39	PERP1/USB3RP3	
PCIE_TBT_R2D_C_N<0>	BD41	PETN1/USB3TN3	
PCIE_TBT_R2D_C_P<0>	BD43	PETP1/USB3TP3	
USB3_EXTD_D2R_N	AH42	PERN2/USB3RN4	
USB3_EXTD_D2R_P	AJ43	PERP2/USB3RP4	
USB3_EXTD_R2D_C_N	BC40	PETN2/USB3TN4	
USB3_EXTD_R2D_C_P	BC42	PETP2/USB3TP4	
NC	AT41	RSVD	
NC	AT43		
PCH_PCIE_RCOMP	F41	PCIE_RCOMP	
	C41	PCIE_IREF	

PCI-E
USB

	W12	USB2N0	USB_EXTA_N
	V12	USB2P0	USB_EXTA_P
	T9	USB2N1	NC_USB_EXTBN
	V10	USB2P1	NC_USB_EXTBP
	Y10	USB2N2	USB_BT_N
	Y8	USB2P2	USB_BT_P
	AB10	USB2N3	NC_USB_IRN
	AA9	USB2P3	NC_USB_IRP
	W9	USB2N4	NC_USB_TPADN
	W7	USB2P4	NC_USB_TPADP
	V8	USB2N5	TP_USB_5N
	T7	USB2P5	TP_USB_5P
	V6	USB2N6	NC_USB_CAMERAN
	T5	USB2P6	NC_USB_CAMERAP
	Y6	USB2N7	NC_USB_SDN
	W5	USB2P7	NC_USB_SDP
	V4	USB2N8	TP_USB_8N
	T3	USB2P8	TP_USB_8P
	Y4	USB2N9	TP_USB_9N
	W3	USB2P9	TP_USB_9P
	AJ41	USB3RN1	USB3_EXTA_D2R_N
	AM41	USB3RP1	USB3_EXTA_D2R_P
	BG42	USB3TN1	USB3_EXTA_R2D_C_N
	BG40	USB3TP1	USB3_EXTA_R2D_C_P
	AM43	USB3RN2	NC_USB3_EXTB_D2RN
	AK42	USB3RP2	NC_USB3_EXTB_D2RP
	BF41	USB3TN2	NC_USB3_EXTB_R2D_C_N
	BF43	USB3TP2	NC_USB3_EXTB_R2D_C_P
	B13	USBRBIAS*	PCH_USB_RBIAS
	D13	USBRBIAS	
	H13	RSVD	NC
	F13		NC
	E18	OC0*/GPIO40	XDP_USB_EXTA_OC_L
	E22	OC1*/GPIO41	XDP_USB_EXTB_OC_L
	H21	OC2*/GPIO42	XDP_USB_EXTC_OC_L
	D21	OC3*/GPIO43	XDP_USB_EXTD_OC_L

(IPD)

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

Unused

Unused

USB3 Port Assignments:

Ext A (SS)

Unused

PLACE_NEAR=U0500.B13:2.54mm
R1570 22.6 1% 1/20W MF 201

PP1V05_S0SW_PCH_VCCUSB3PLL

R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.F41:2.54mm

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
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LPC_AD<0>	P13	LAD0	
LPC_AD<1>	M13	LAD1	
LPC_AD<2>	R14	LAD2	
LPC_AD<3>	K13	LAD3	
LPC_FRAME_L	P15	LFRAME*	
SPI_CLK_R	C26	SPI_CLK	
SPI_CS0_R_L	H27	SPI_CS0*	
TP_SPI_CS1_L	M27	SPI_CS1*	
TP_SPI_CS2_L	K27	SPI_CS2*	
SPI_MOSI_R	D31	SPI_MOSI	
SPI_MISO	B23	SPI_MISO	
SPI_IO<2>	F27	SPI_IO2	
SPI_IO<3>	J26	SPI_IO3	

LPC
SMBUS
SPI
C-LINK

K21	SMBALERT*/GPIO11	PCH_SMBALERT_L
P21	SMBCLK	SMBUS_PCH_CLK
B21	SMBDATA	SMBUS_PCH_DATA
F21	SML0ALERT*/GPIO60	WOL_EN
P19	SML0CLK	SML_PCH_0_CLK
B19	SML0DATA	SML_PCH_0_DATA
H8	SML1ALERT*/PCHHOT*/GPIO73	PCH_SML1ALERT_L
C14	SML1CLK/GPIO75	SMBUS_SMC_1_S0_SCL
A14	SML1DATA/GPIO74	SMBUS_SMC_1_S0_SDA
D23	(IPU/IPD) CL_CLK	NC_CLINK_CLK
H23	(IPU/IPD) CL_DATA	NC_CLINK_DATA
K23	CL_RST*	NC_CLINK_RESET_L

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

LPC_AD<0>	R1540	33	LPC_AD_R<0>
LPC_AD<1>	R1541	33	LPC_AD_R<1>
LPC_AD<2>	R1542	33	LPC_AD_R<2>
LPC_AD<3>	R1543	33	LPC_AD_R<3>
LPC_FRAME_L	R1544	33	LPC_FRAME_R_L

5% 1/32W MF 01005 (1/20W MF 201)

PP3V3_SUS
PP3V3_SUS

R1580	100K		XDP_USB_EXTA_OC_L
R1581	100K		XDP_USB_EXTB_OC_L
R1582	100K		XDP_USB_EXTC_OC_L
R1583	100K		XDP_USB_EXTD_OC_L
R1548	1.00K		SPI_IO<2>
R1549	1.00K		SPI_IO<3>
R1590	100K		PCH_SMBALERT_L
R1591	100K		WOL_EN

5% 1/32W MF 01005

SYNC_MASTER=J92_DEVMLB SYNC_DATE=06/28/2013

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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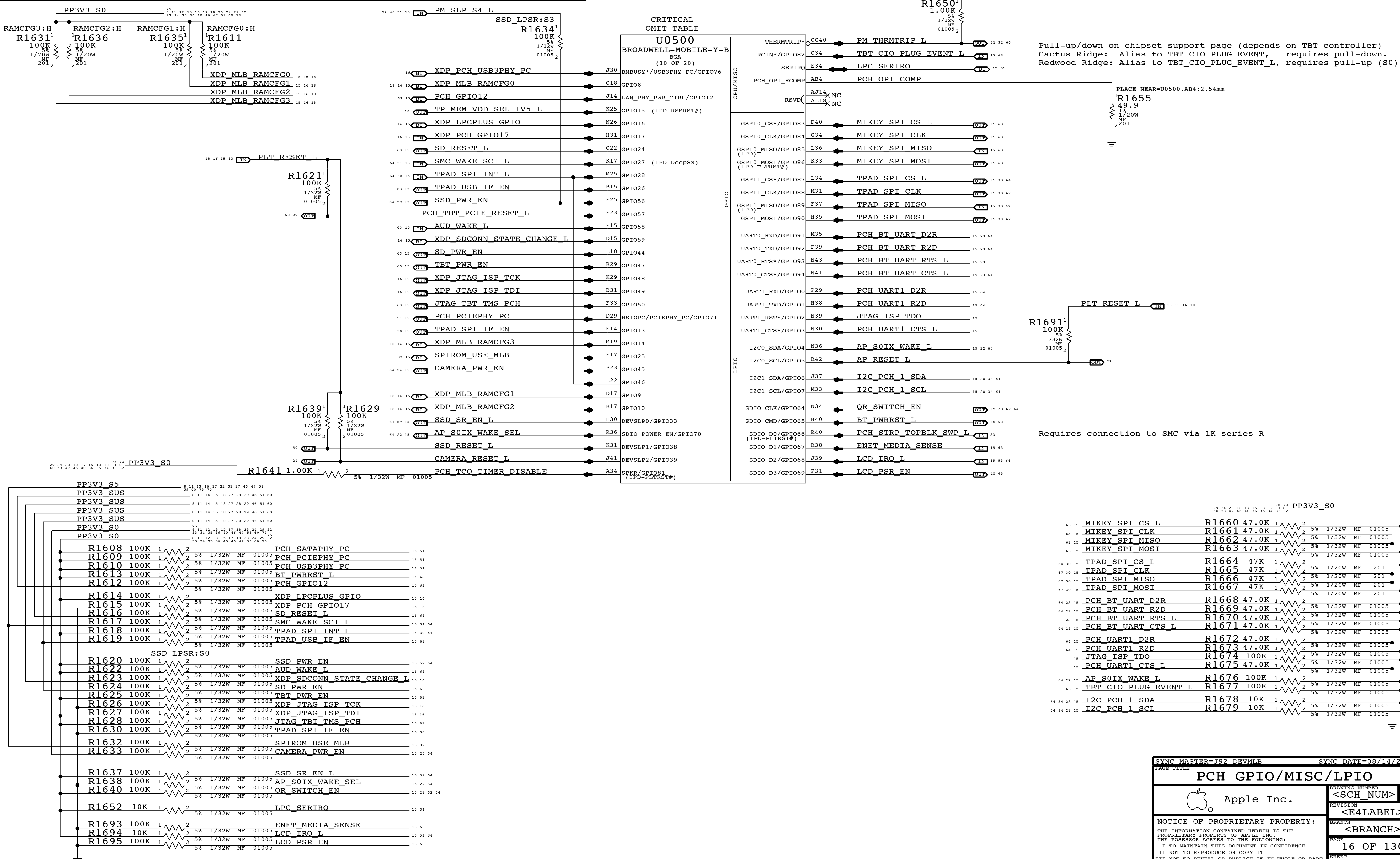
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H



PP3V3_S0
RAMCFG3:H R1631 100K 5% 1/20W MF 201
RAMCFG2:H R1636 100K 5% 1/20W MF 201
RAMCFG1:H R1635 100K 5% 1/20W MF 201
RAMCFG0:H R1611 100K 5% 1/20W MF 201
XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3
PM_SLP_S4_L
SSD_LPSR:S3
R1634 100K 5% 1/32W MF 01005
CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
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XDP_PCH_USB3PHY_PC
XDP_MLB_RAMCFG0
PCH_GPIO12
TP_MEM_VDD_SEL_1V5_L
XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17
SD_RESET_L
SMC_WAKE_SCI_L
TPAD_SPI_INT_L
TPAD_USB_IF_EN
SSD_PWR_EN
PCH_TBT_PCIE_RESET_L
AUD_WAKE_L
XDP_SDCONN_STATE_CHANGE_L
SD_PWR_EN
TBT_PWR_EN
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI
JTAG_TBT_TMS_PCH
PCH_PCIEPHY_PC
TPAD_SPI_IF_EN
XDP_MLB_RAMCFG3
SPIROM_USE_MLB
CAMERA_PWR_EN
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
SSD_SR_EN_L
AP_S0IX_WAKE_SEL
SSD_RESET_L
CAMERA_RESET_L
PCH_TCO_TIMER_DISABLE
PLT_RESET_L
R1621 100K 5% 1/32W MF 01005
R1639 100K 5% 1/32W MF 01005
R1629 100K 5% 1/32W MF 01005
PP3V3_S0
R1641 1.00K 5% 1/32W MF 01005
BMBUSY*/USB3PHY_PC/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15 (IPD-RSMRST#)
GPIO16
GPIO17
GPIO24
GPIO27 (IPD-DeepSx)
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/PCIEPHY_PC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81 (IPD-PLTRST#)
CPU/MISC
GPIO
LPIO
THERMTRIP*
RCIN*/GPIO82
SERIRQ
PCH_OPI_RCOMP
RSVD
GSPI0_CS*/GPIO83
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85 (IPD)
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)
GSPI1_CS*/GPIO87
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89 (IPD)
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS*/GPIO93
UART0_CTS*/GPIO94
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST*/GPIO2
UART1_CTS*/GPIO3
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66 (IPD-PLTRST#)
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
PP1V05_S0
R1650 1.00K 5% 1/32W MF 01005
PM_THRMTRIP_L
TBT_CIO_PLUG_EVENT_L
LPC_SERIRQ
PCH_OPI_COMP
NC
PLACE_NEAR=U0500.AB4:2.54mm
R1655 49.9 1% 1/20W MF 201
MIKEY_SPI_CS_L
MIKEY_SPI_CLK
MIKEY_SPI_MISO
MIKEY_SPI_MOSI
TPAD_SPI_CS_L
TPAD_SPI_CLK
TPAD_SPI_MISO
TPAD_SPI_MOSI
PCH_BT_UART_D2R
PCH_BT_UART_R2D
PCH_BT_UART_RTS_L
PCH_BT_UART_CTS_L
PCH_UART1_D2R
PCH_UART1_R2D
JTAG_ISP_TDO
PCH_UART1_CTS_L
AP_S0IX_WAKE_L
AP_RESET_L
I2C_PCH_1_SDA
I2C_PCH_1_SCL
QR_SWITCH_EN
BT_PWRRST_L
PCH_STRP_TOPBLK_SWP_L
ENET_MEDIA_SENSE
LCD_IRQ_L
LCD_PSR_EN
PLT_RESET_L
R1691 100K 5% 1/32W MF 01005
PP3V3_S5
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_S0
PP3V3_S0
R1608 100K PCH_SATAPHY_PC
R1609 100K PCH_PCIEPHY_PC
R1610 100K PCH_USB3PHY_PC
R1613 100K BT_PWRRST_L
R1612 100K PCH_GPIO12
R1614 100K XDP_LPCPLUS_GPIO
R1615 100K XDP_PCH_GPIO17
R1616 100K SD_RESET_L
R1617 100K SMC_WAKE_SCI_L
R1618 100K TPAD_SPI_INT_L
R1619 100K TPAD_USB_IF_EN
SSD_LPSR:S0
R1620 100K SSD_PWR_EN
R1622 100K AUD_WAKE_L
R1623 100K XDP_SDCONN_STATE_CHANGE_L
R1624 100K SD_PWR_EN
R1625 100K TBT_PWR_EN
R1626 100K XDP_JTAG_ISP_TCK
R1627 100K XDP_JTAG_ISP_TDI
R1628 100K JTAG_TBT_TMS_PCH
R1630 100K TPAD_SPI_IF_EN
R1632 100K SPIROM_USE_MLB
R1633 100K CAMERA_PWR_EN
R1637 100K SSD_SR_EN_L
R1638 100K AP_S0IX_WAKE_SEL
R1640 100K QR_SWITCH_EN
R1652 10K LPC_SERIRQ
R1693 100K ENET_MEDIA_SENSE
R1694 10K LCD_IRQ_L
R1695 100K LCD_PSR_EN
5% 1/32W MF 01005
PP3V3_S0
MIKEY_SPI_CS_L R1660 47.0K
MIKEY_SPI_CLK R1661 47.0K
MIKEY_SPI_MISO R1662 47.0K
MIKEY_SPI_MOSI R1663 47.0K
TPAD_SPI_CS_L R1664 47K
TPAD_SPI_CLK R1665 47K
TPAD_SPI_MISO R1666 47K
TPAD_SPI_MOSI R1667 47K
5% 1/20W MF 201
PCH_BT_UART_D2R R1668 47.0K
PCH_BT_UART_R2D R1669 47.0K
PCH_BT_UART_RTS_L R1670 47.0K
PCH_BT_UART_CTS_L R1671 47.0K
PCH_UART1_D2R R1672 47.0K
PCH_UART1_R2D R1673 47.0K
JTAG_ISP_TDO R1674 100K
PCH_UART1_CTS_L R1675 47.0K
AP_S0IX_WAKE_L R1676 100K
TBT_CIO_PLUG_EVENT_L R1677 100K
I2C_PCH_1_SDA R1678 10K
I2C_PCH_1_SCL R1679 10K

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

Requires connection to SMC via 1K series R

SYNC_MASTER=J92_DEVMLB SYNC_DATE=08/14/2013

PAGE TITLE

PCH GPIO/MISC/LPIO

Apple Inc.

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Extra BPM Probepoints

XDP_BPM_L<2> → PP1802
XDP_BPM_L<3> → PP1803
XDP_BPM_L<4> → PP1804
XDP_BPM_L<5> → PP1805
XDP_BPM_L<6> → PP1806
XDP_BPM_L<7> → PP1807
(P2MM SM)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

R1830 150 5% 1/20W MF 201 2

XDP		XDP
XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0 — CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1 — CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0 — CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1 — CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2 — CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3 — CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0 — CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1 — CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0 — CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1 — CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2 — CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3 — CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4 — NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 — NC
	VCC_OBS_AB	VCC_OBS_CD
CPU_PWR_DEBUG_L	HOOK2	RESET#/HOOK6 — XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7 — XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO — XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn — XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI — XDP_PCH_TDI
	TCK0	TMS — XDP_PCH_TMS
		XDP_PRESENT# — XDP_CPU_PRESENT_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CPU_VCCST_PWRGD — R1800 1K 5% 1/20W MF 201 — XDP
PLACE_NEAR=U0500.BU14:2.54mm

PM_PWRBTN_L — R1802 0 5% 1/20W MF 0201 — XDP
PLACE_NEAR=U5000.K1:2.54mm

PM_PCH_SYS_PWROK — R1804 0 5% 1/20W MF 0201 — XDP

XDP_CPU_TCK

PCH_JTAGX — R1835 0 5% 1/20W MF 0201 — XDP
PLACE_NEAR=J1800.58:28mm

C1804 0.1UF 10% 6.3V CERM-X5R 0201 XDP
R1831 1K 5% 1/20W MF 201 XDP
C1800 0.1UF 10% 6.3V CERM-X5R 0201 XDP
C1801 0.1UF 10% 6.3V CERM-X5R 0201 XDP
C1806 0.1UF 10% 6.3V CERM-X5R 0201 XDP

XDP_CPU_PRESENT_L
NOSTUFF
R1832 0 5% 1/20W MF 0201

R1805 1K 5% 1/20W MF 201 XDP — PLT_RESET_L
PLACE_NEAR=U0500.AG7:2.54mm

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL
Q1840 XDP DMN5L06VK-7 SOT563 VER
PLACE_NEAR=J1800.55:28mm — XDP_CPU_TDO

CRITICAL
Q1840 XDP DMN5L06VK-7 SOT563 VER
PLACE_NEAR=J1800.55:28mm — XDP_CPUPCH_TRST_L
MAKE_BASE=TRUE
XDP_CPUPCH_TRST_L

CRITICAL
Q1842 XDP DMN5L06VK-7 SOT563 VER
PLACE_NEAR=J1800.55:28mm — XDP_CPU_TDI

CRITICAL
Q1842 XDP DMN5L06VK-7 SOT563 VER
PLACE_NEAR=J1800.55:28mm — XDP_CPU_TMS

PP1V05_S0

XDP_CPU_TDO — R1810 51 5% 1/20W MF 201 — XDP
PLACE_NEAR=U0500.CU38:28mm

XDP_CPU_TCK — R1813 51 5% 1/20W MF 201 — XDP
PLACE_NEAR=U0500.CM41:28mm

TDI and TMS are terminated in CPU.

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0		
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	PP1873	
XDP_USB_EXTD_OC_L	PP1874	
XDP_SDCONN_STATE_CHANGE_L	PP1875	
XDP_MLB_RAMCFG1		
XDP_MLB_RAMCFG2		
XDP_MLB_RAMCFG3		
XDP_JTAG_ISP_TCK	PP1879	
XDP_FW_PME_L	PP1880	
XDP_PCH_SATAPHY_PC	R1881 SHORT OMIT NONE NONE NONE 201	PCH_SATAPHY_PC
XDP_PCH_UART_SSD_L_BT_H	R1882 SHORT OMIT NONE NONE NONE 201	PCH_UART_SSD_L_BT_H
XDP_SSD_PCIE0_SEL_L	R1883 1K 5% 1/20W MF 201	
XDP_LPCPLUS_GPIO	PP1884	
XDP_PCH_GPIO17	PP1885	
XDP_PCH_USB3PHY_PC	R1886 SHORT OMIT NONE NONE NONE 201	PCH_USB3PHY_PC
XDP_JTAG_ISP_TDI	PP1887	

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, A, Y, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX — R1899 1K 5% 1/20W MF 201 — NO STUFF
PLACE_NEAR=U0500.CL16:28mm

XDP_PCH_TDO — R1890 51 5% 1/20W MF 201 — XDP
PLACE_NEAR=U0500.CL18:28mm

XDP_PCH_TDI — R1891 51 5% 1/20W MF 201 — XDP
PLACE_NEAR=U0500.CL20:28mm

XDP_PCH_TMS — R1892 51 5% 1/20W MF 201 — XDP
PLACE_NEAR=U0500.CK15:28mm

XDP_PCH_TCK — R1896 51 5% 1/20W MF 201 — NO STUFF
PLACE_NEAR=U0500.CK17:28mm

XDP_CPUPCH_TRST — R1897 51 5% 1/20W MF 201 — NO STUFF
PLACE_NEAR=U0500.CM7:28mm

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/16/2013
PAGE TITLE: CPU/PCH Merged XDP
Apple Inc.
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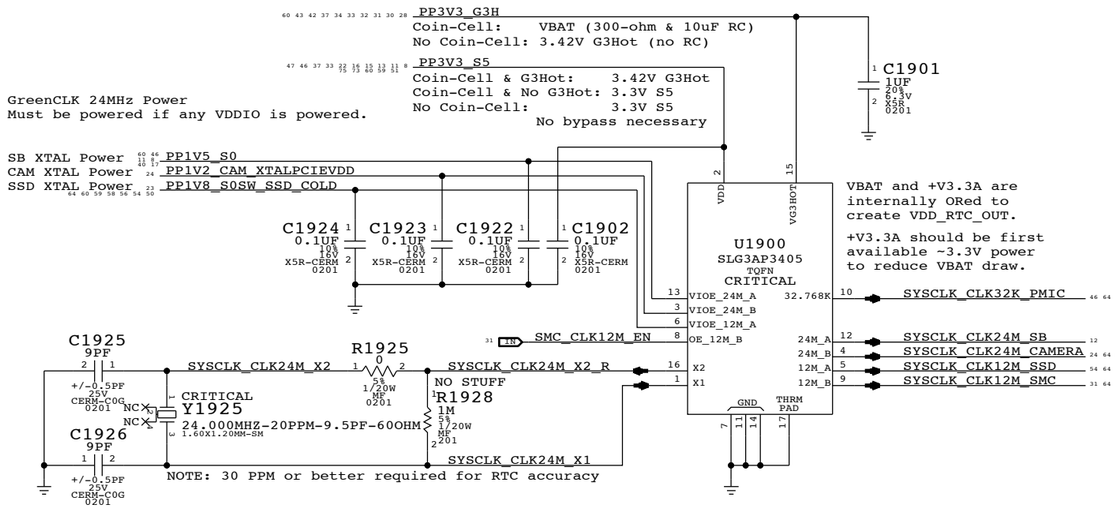
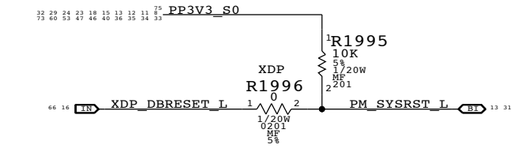
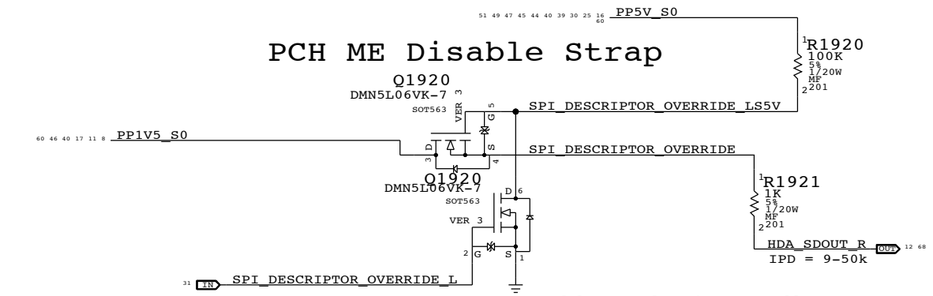
System 32kHz / 12MHz / 24MHz Clock Generator

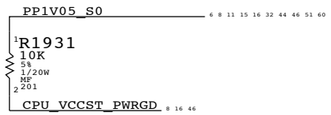




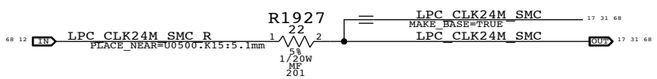
PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



PCH 24MHz Outputs



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PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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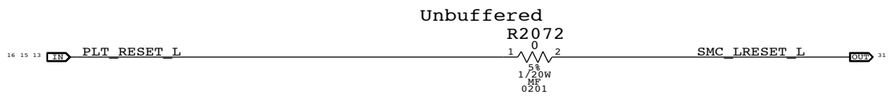
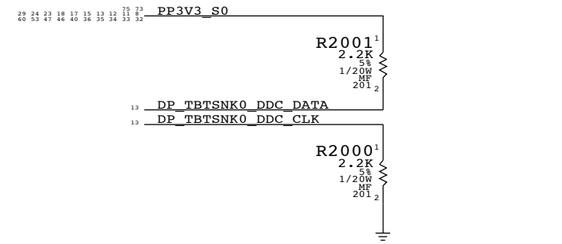
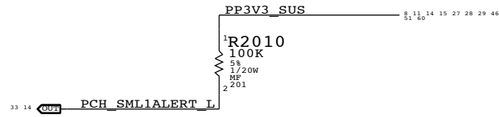
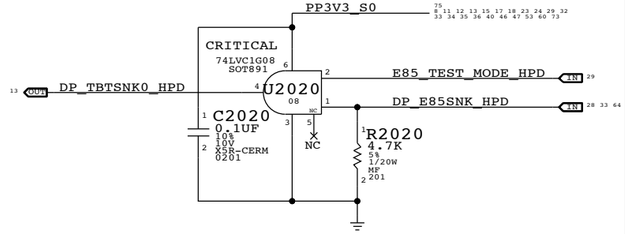
Platform Reset Connections

Unbuffered



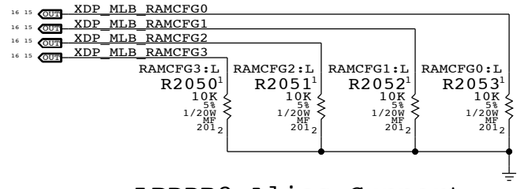




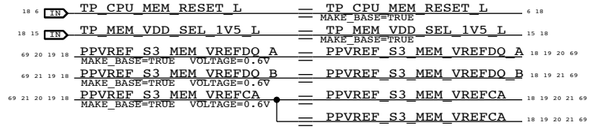


RAM Configuration Straps

Pull-downs for chip-down RAM systems



LPDDR3 Alias Support



SYNC_MASTER=J92_DEVMLB SYNC_DATE=08/01/2013

PAGE TITLE

Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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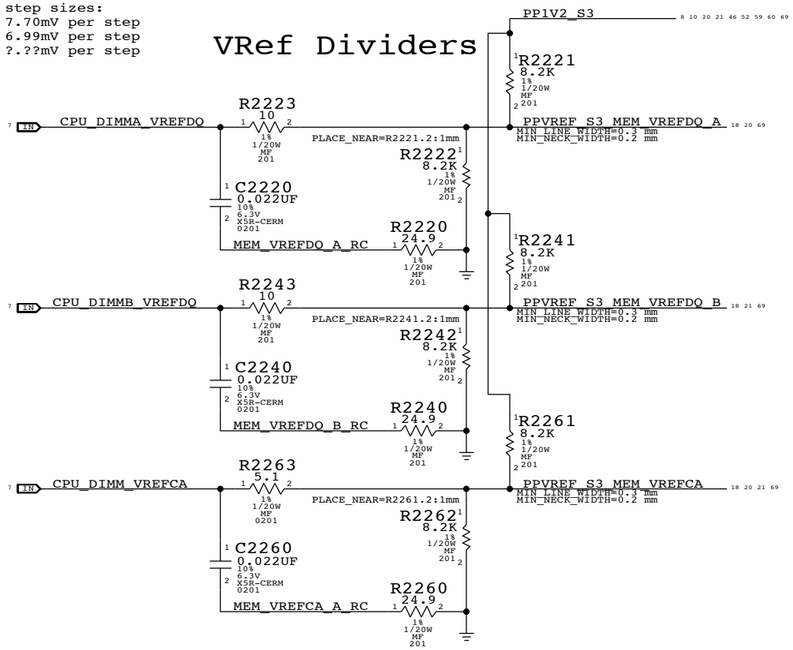
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



SYNC MASTER=J92 DEVMLB SYNC DATE=06/28/2013

PAGE TITLE
LPDDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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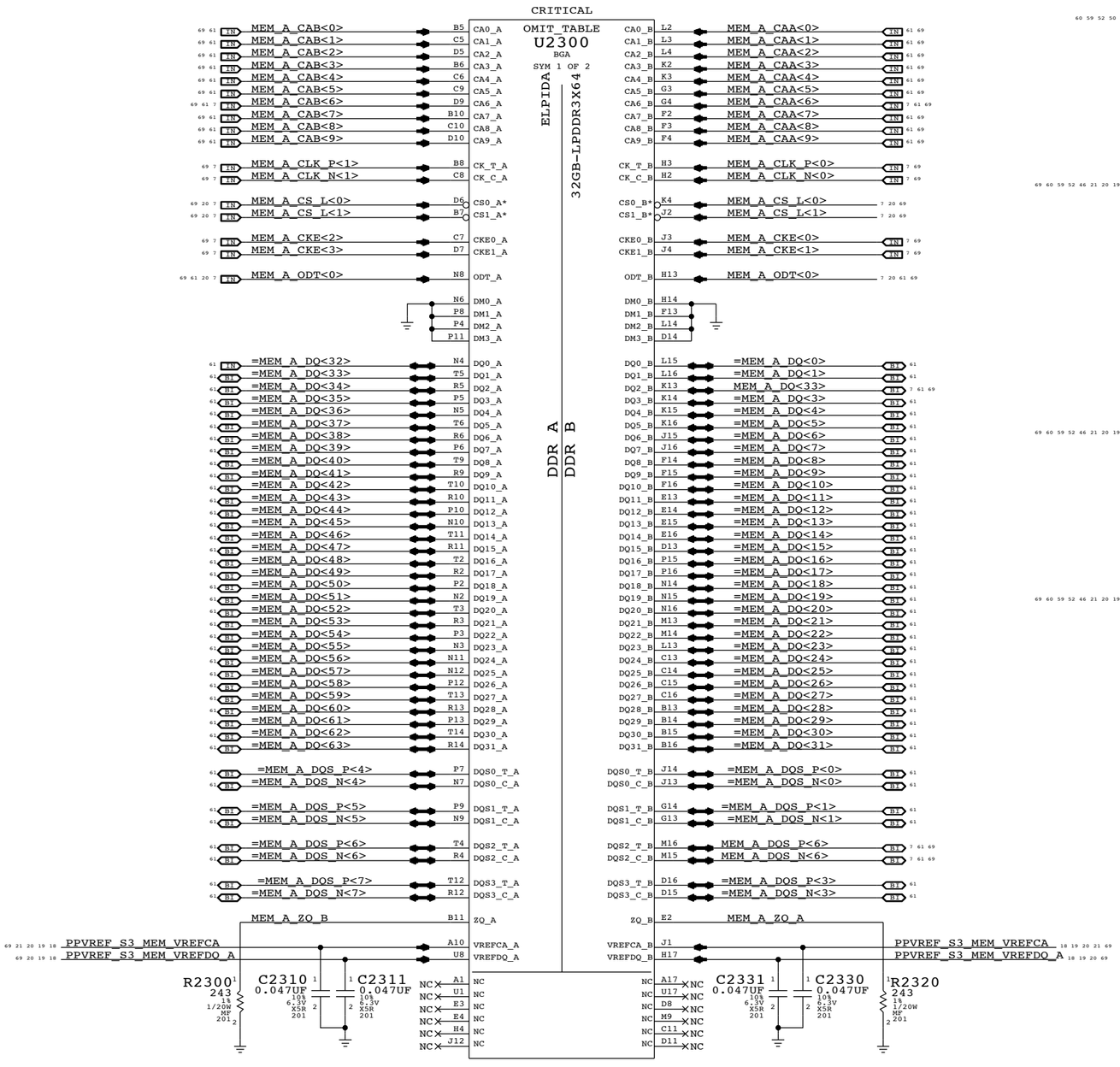

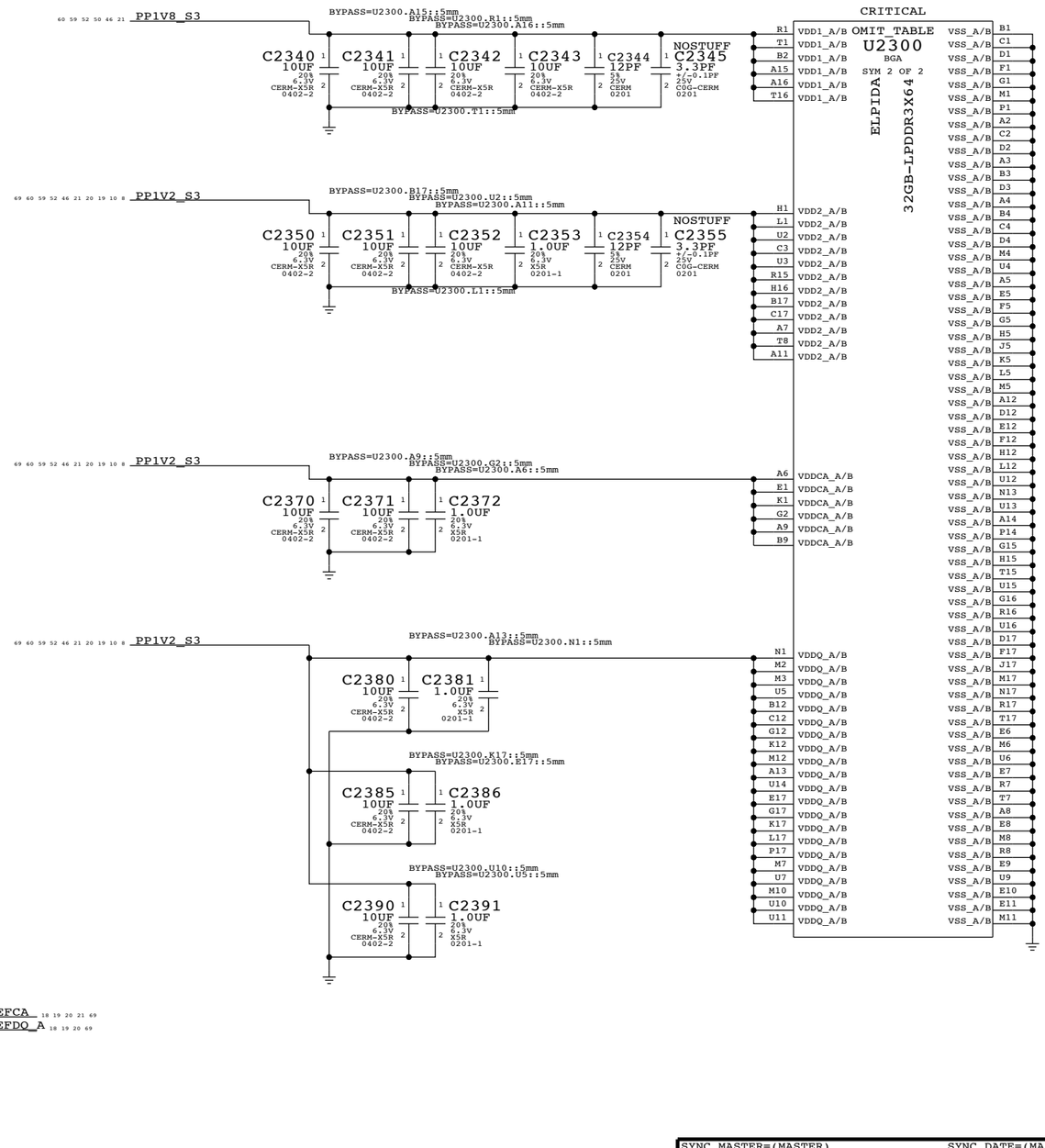

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PAGE TITLE	LPDDR3 DRAM Channel A (0-63)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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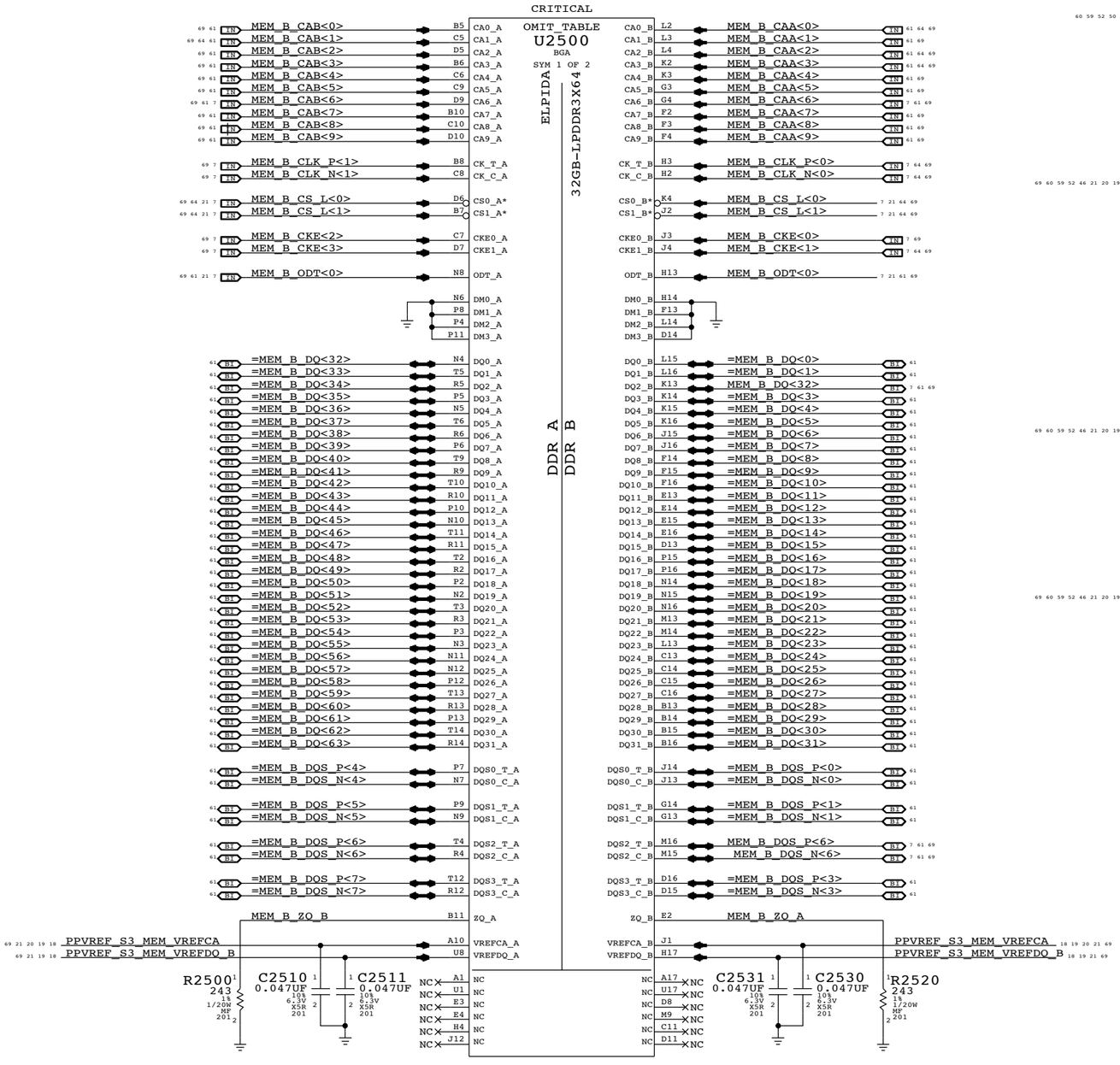

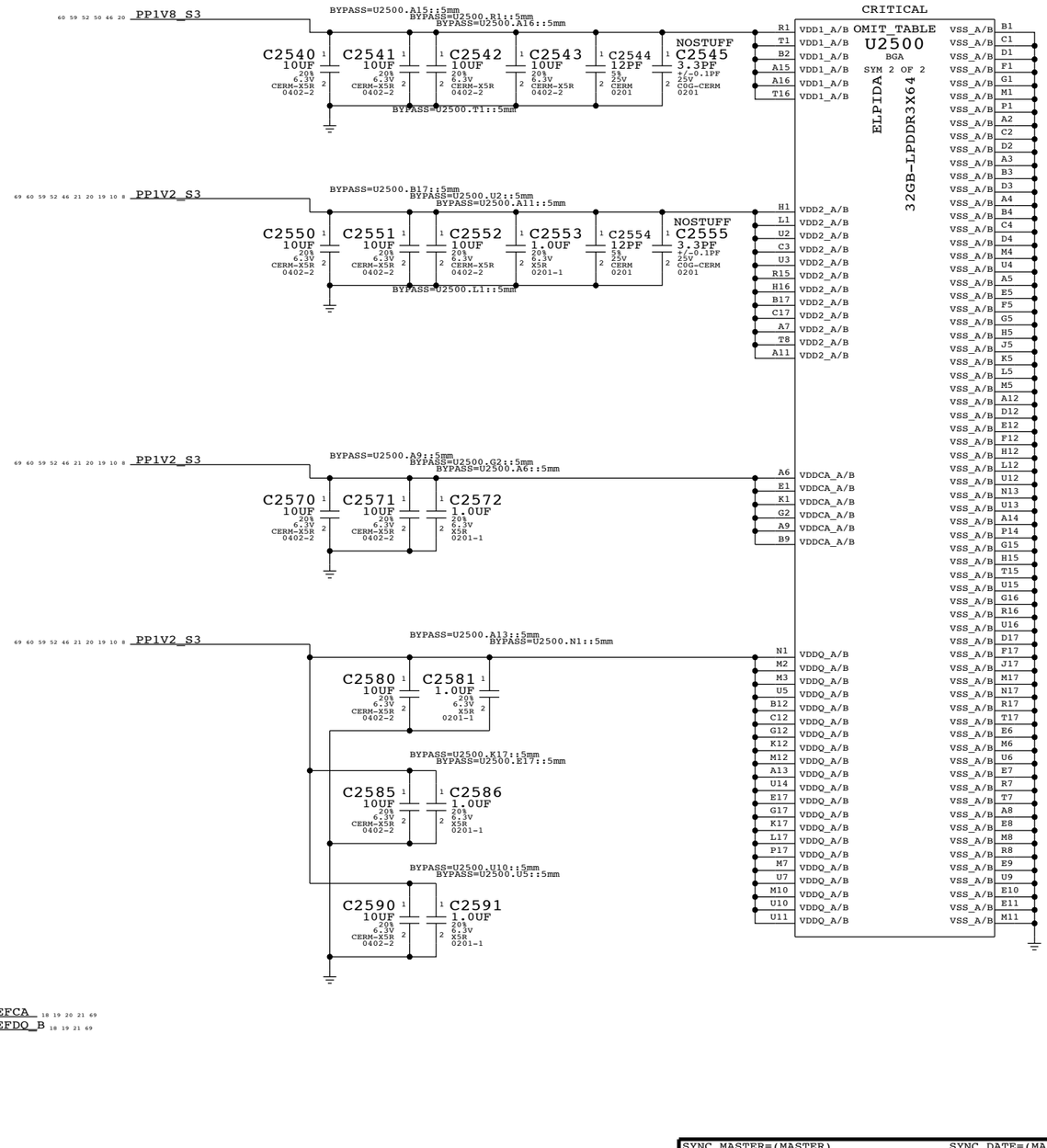

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PAGE TITLE

LPDDR3 DRAM Channel B (0-63)

Apple Inc.

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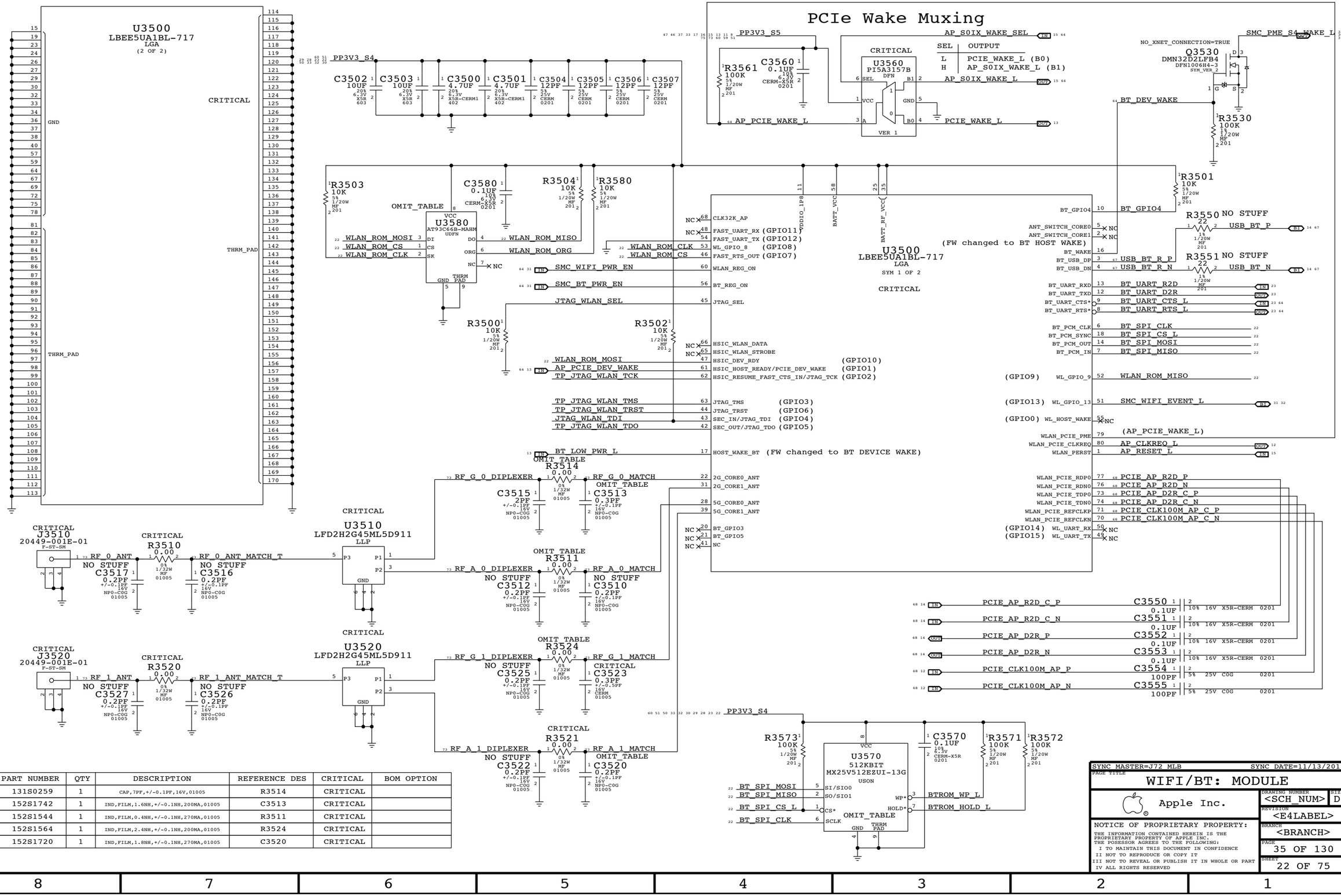
PCIe Wake Muxing



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0259	1	CAP,7PF,+/-0.1PF,16V,01005	R3514	CRITICAL	
152S1742	1	IND,FILM,1.6NH,+/-0.1NH,200MA,01005	C3513	CRITICAL	
152S1544	1	IND,FILM,0.4NH,+/-0.1NH,270MA,01005	R3511	CRITICAL	
152S1564	1	IND,FILM,2.4NH,+/-0.1NH,200MA,01005	R3524	CRITICAL	
152S1720	1	IND,FILM,1.8NH,+/-0.1NH,270MA,01005	C3520	CRITICAL	

SYNC_MASTER=J72_MLB SYNC_DATE=11/13/2012

PAGE TITLE

WIFI/BT: MODULE

Apple Inc.

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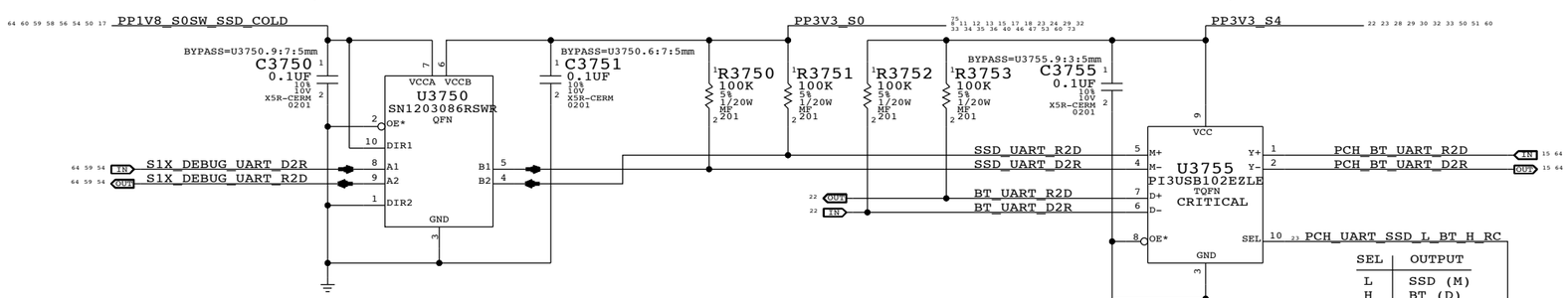
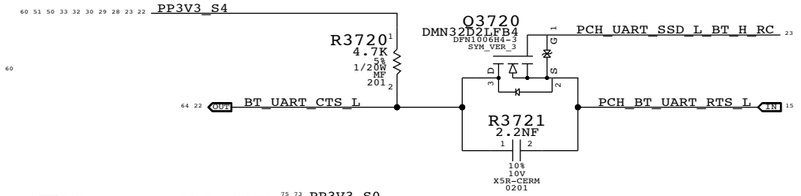
SSD/PCH Level Shifter

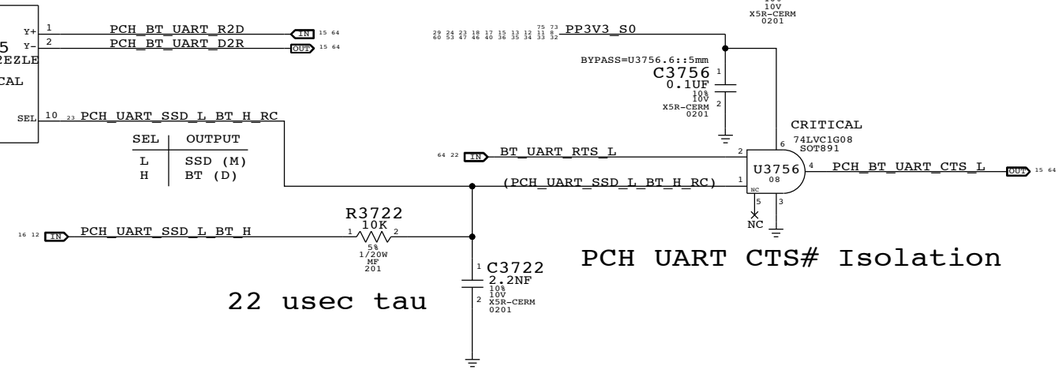


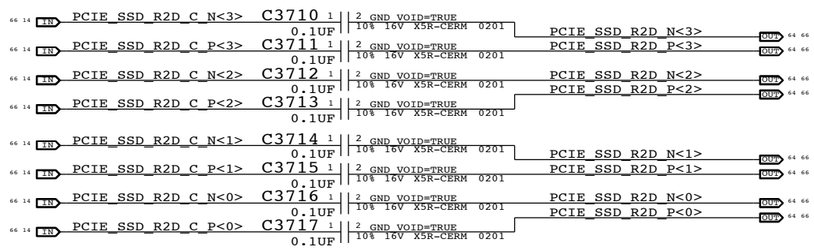
PCH UART BT/SSD MUX

BT UART CTS# Isolation

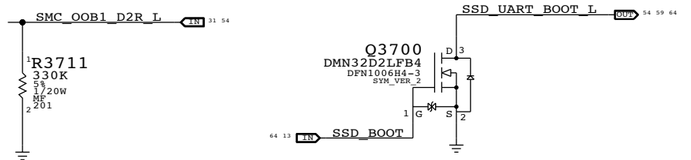


PCH UART CTS# Isolation





Bootloader Enable



SYNC MASTER=J92_DEVMLB SYNC DATE=09/11/2013

PAGE TITLE: SSD Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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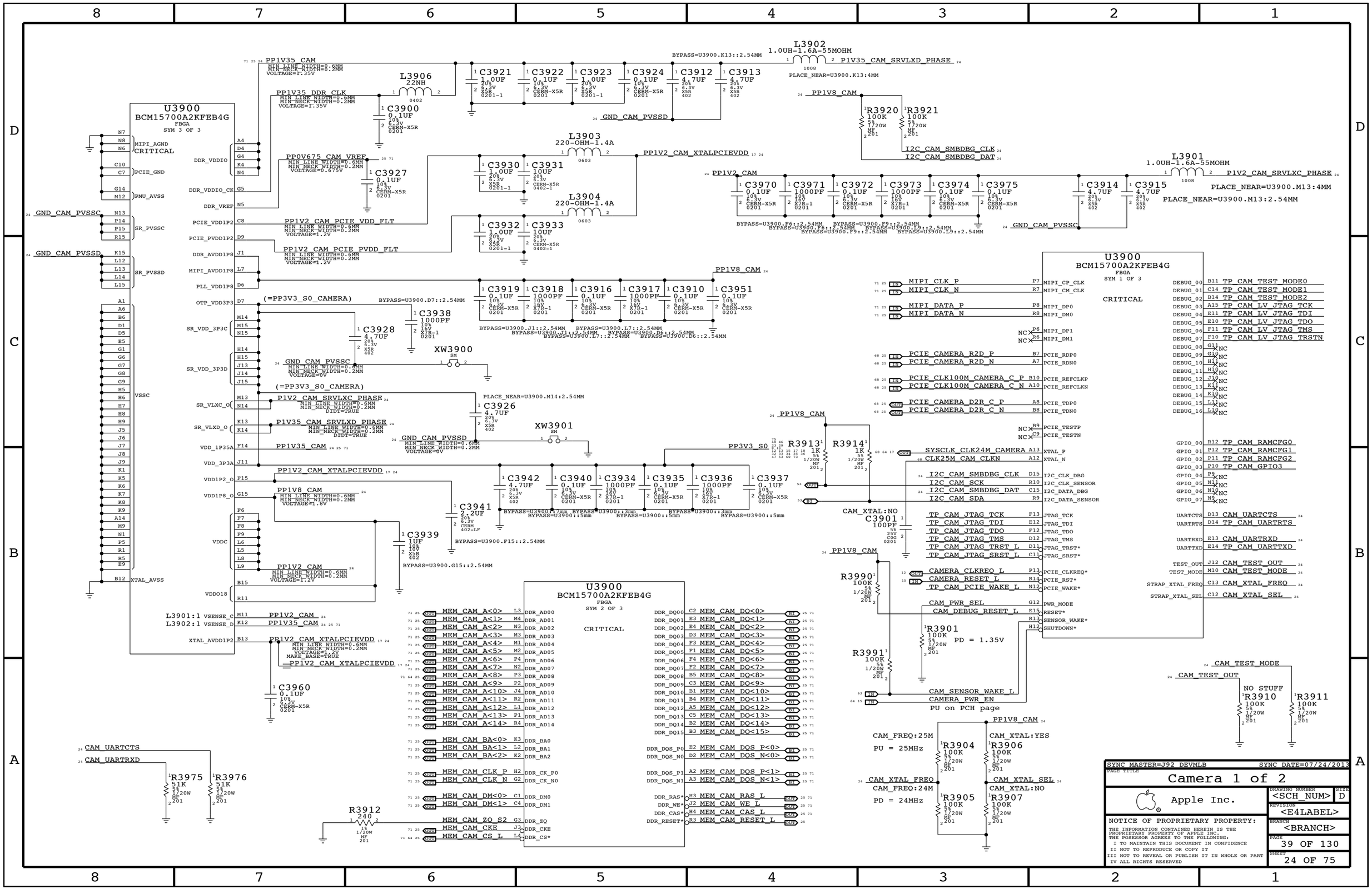
U3900
BCM15700A2KFEB4G
FBGA
SYM 3 OF 3
MIPI_AGND
CRITICAL
PCIE_GND
PMU_AVSS
SR_PVSSC
SR_PVSSD
VSSC
XTAL_AVSS
DDR_VDDIO
DDR_VDDIO_CK
DDR_VREF
PCIE_VDD1P2
PCIE_PVDD1P2
DDR_AVDD1P8
MIPI_AVDD1P8
PLL_VDD1P8
OTP_VDD3P3
SR_VDD_3P3C
SR_VDD_3P3D
SR_VLXC_O
SR_VLXD_O
VDD_1P35A
VDD_3P3A
VDD1P2_O
VDD1P8_O
VDDC
VDDIO18
L3901:1 VSENSE_C
L3902:1 VSENSE_D
XTAL_AVDD1P2
PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
(=PP3V3_S0_CAMERA)
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP1V35_CAM
PP1V8_CAM
PP1V2_CAM
PP1V2_CAM_XTALPCIEVDD
L3906 22NH 0402
L3902 1.0UH-1.6A-55MOHM 1008
L3903 220-OHM-1.4A 0603
L3904 220-OHM-1.4A 0603
L3901 1.0UH-1.6A-55MOHM 1008
P1V35_CAM_SRVLXD_PHASE
P1V2_CAM_SRVLXC_PHASE
PLACE_NEAR=U3900.K13:4MM
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM
PLACE_NEAR=U3900.M14:2.54MM
BYPASS=U3900.K13::2.54MM
GND_CAM_PVSSD
GND_CAM_PVSSC
C3900 0.1UF
C3927 0.1UF
C3928 4.7UF
C3938 1000PF
C3939 1UF
C3941 2.2UF
C3960 0.1UF
C3926 4.7UF
C3921 1.0UF
C3922 0.1UF
C3923 1.0UF
C3924 0.1UF
C3912 4.7UF
C3913 4.7UF
C3930 1.0UF
C3931 10UF
C3932 1.0UF
C3933 10UF
C3970 0.1UF
C3971 1000PF
C3972 0.1UF
C3973 1000PF
C3974 0.1UF
C3975 0.1UF
C3914 4.7UF
C3915 4.7UF
C3919 0.1UF
C3918 1000PF
C3916 0.1UF
C3917 1000PF
C3910 0.1UF
C3951 0.1UF
C3942 4.7UF
C3940 0.1UF
C3934 1000PF
C3935 0.1UF
C3936 1000PF
C3937 0.1UF
R3920 100K
R3921 100K
R3913 1K
R3914 1K
C3901 100PF
R3990 100K
R3991 100K
R3901 100K
PD = 1.35V
R3904 100K
R3905 100K
R3906 100K
R3907 100K
CAM_FREQ:25M
PU = 25MHz
CAM_FREQ:24M
PD = 24MHz
CAM_XTAL:YES
CAM_XTAL:NO
R3910 100K NO STUFF
R3911 100K
R3912 240
R3975 51K
R3976 51K
XW3900 SM
XW3901 SM
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
SYSCLK_CLK24M_CAMERA
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
TP_CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAMERA_RESET_L
TP_CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PU on PCH page
I2C_CAM_SMBDBG_DAT
I2C_CAM_SMBDBG_CLK
CAM_UARTCTS
CAM_UARTRXD
CAM_TEST_MODE
CAM_TEST_OUT
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0>
MEM_CAM_DQ<1>
MEM_CAM_DQ<2>
MEM_CAM_DQ<3>
MEM_CAM_DQ<4>
MEM_CAM_DQ<5>
MEM_CAM_DQ<6>
MEM_CAM_DQ<7>
MEM_CAM_DQ<8>
MEM_CAM_DQ<9>
MEM_CAM_DQ<10>
MEM_CAM_DQ<11>
MEM_CAM_DQ<12>
MEM_CAM_DQ<13>
MEM_CAM_DQ<14>
MEM_CAM_DQ<15>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
TP_CAM_TEST_MODE0
TP_CAM_TEST_MODE1
TP_CAM_TEST_MODE2
TP_CAM_LV_JTAG_TCK
TP_CAM_LV_JTAG_TDI
TP_CAM_LV_JTAG_TDO
TP_CAM_LV_JTAG_TMS
TP_CAM_LV_JTAG_TRSTN
TP_CAM_RAMCFG0
TP_CAM_RAMCFG1
TP_CAM_RAMCFG2
TP_CAM_GPIO3
CAM_UARTCTS
CAM_UARTRTS
CAM_UARTRXD
CAM_UARTTXD
CAM_TEST_OUT
CAM_TEST_MODE
CAM_XTAL_FREQ
CAM_XTAL_SEL
SYNC_MASTER=J92_DEVMLB
SYNC_DATE=07/24/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 39 OF 130
SHEET 24 OF 75
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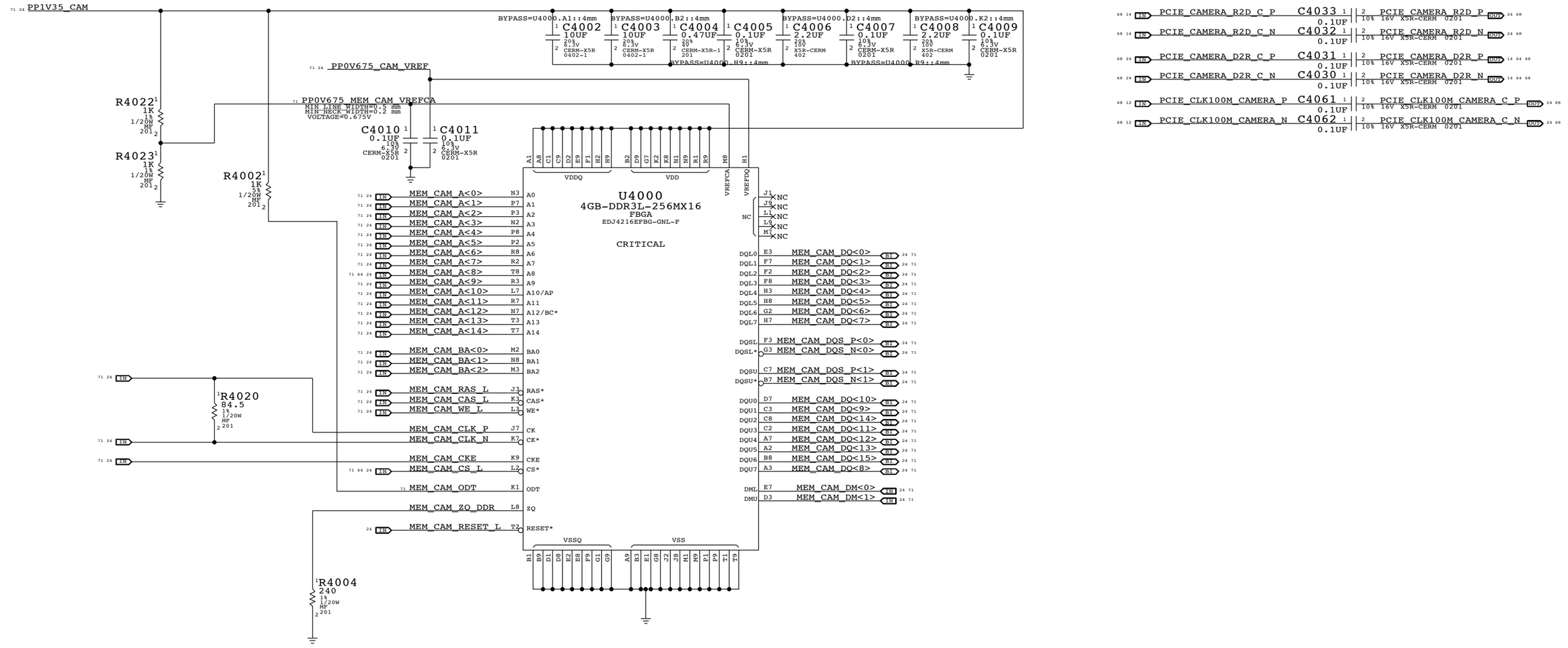

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/10/2013

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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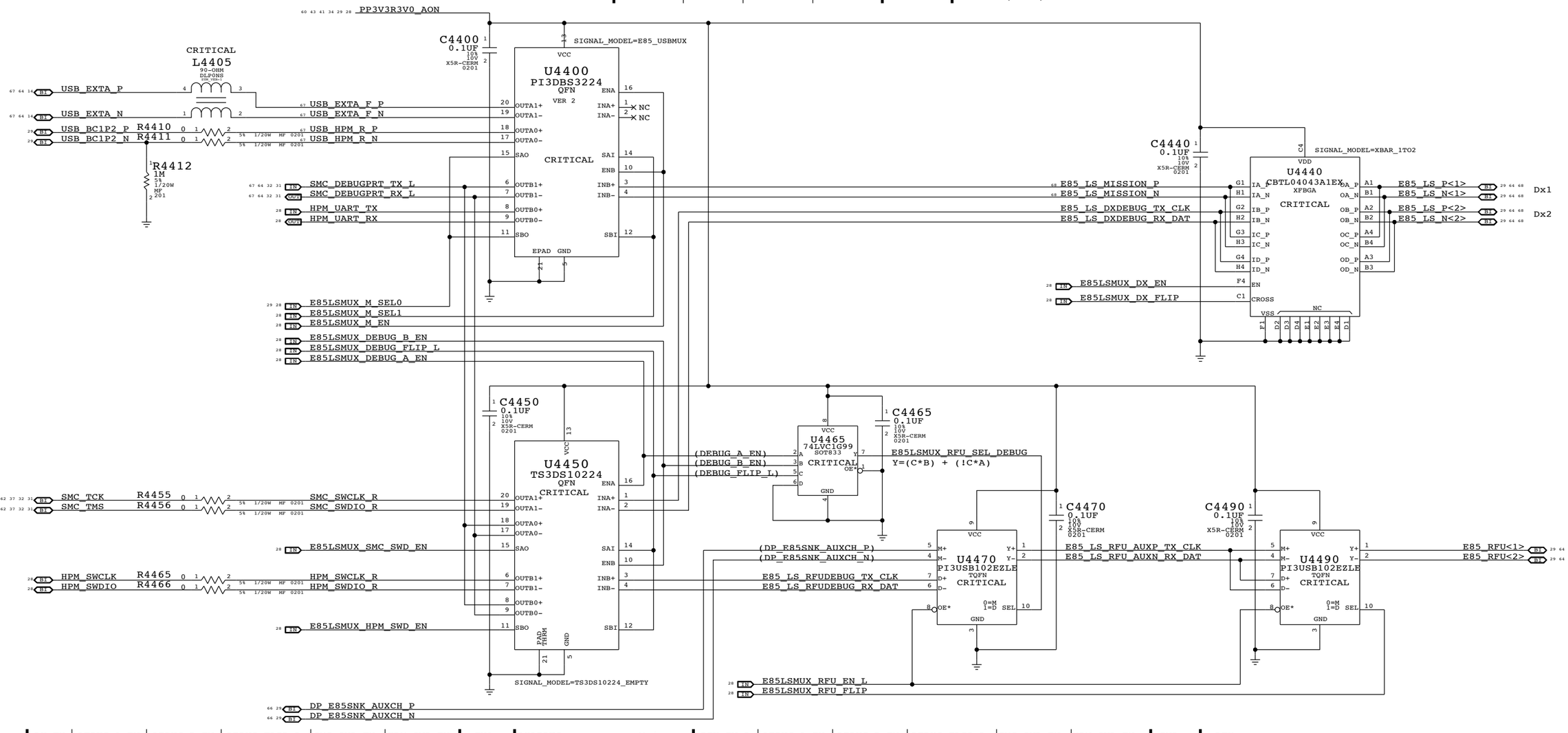
Mode	DX_EN	M_EN	M_SEL0	M_SEL1	INB	Mission
Empty	0	0	X	X	Hi-Z	Hi-Z
Mojo	1	1	1	1	OUTB1	UART (SMC)
USB (Host)	1	1	1	0	OUTA1	USB (PCH)
USB (Device)	1	1	0	0	OUTA0	USB (HPM)
HPM UART	1	1	0	1	OUTB0	UART (HPM)



Mode	DX_EN	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INA	DXDEBUG
Empty	0	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
No Debug	1	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
SMC SWD	1	1	X	1	1	X	OUTA1	SWD (SMC)
Mojo	1	1 X	X 1	1 0	0 X	X 0	OUTA0 OUTB0	UART (SMC)
HPM SWD	1	X	1	0	X	1	OUTB1	SWD (HPM)

Mode	RFU_EN_L	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INB	RFU
Empty	1	X 0	0 X	1 0	X	X	Hi-Z	Hi-Z
DP	0	X 0	0 X	1 0	X	X	Hi-Z	AUX+/HPD
HPM SWD	0	X	1	1	X	1	OUTB1	SWD (HPM)
Mojo	0	X 1	1 X	1 0	X 0	0 X	OUTB0 OUTA0	UART (SMC)
SMC SWD	0	1	X	0	1	X	OUTA1	SWD (SMC)

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE: Low Speed MUXing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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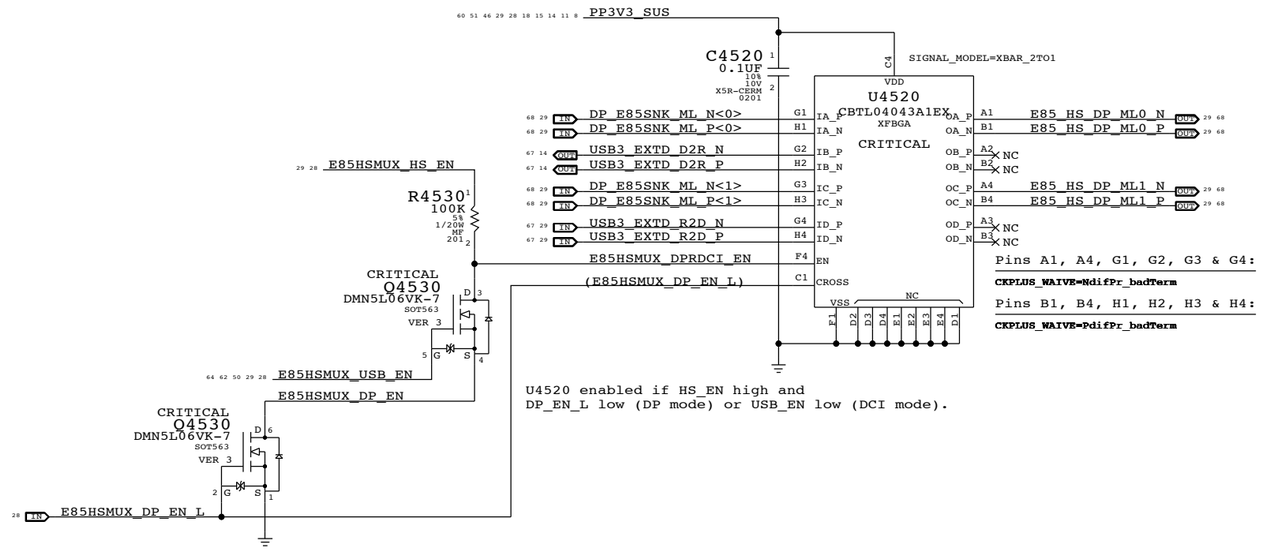

HS_FLIP swaps Tx1/2 and Rx1/2

Mode	HS_EN	DP_EN_L	USB_EN	SSTx1	SSRx1	SSTx2	SSRx2
Empty	0	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
USB3	1	1	1	R2D	D2R	Hi-Z	Hi-Z
USB3/DPx2	1	0	1	R2D	D2R	ML1	ML0
DPx4 (Passive)	1	0	0	ML2	ML3	ML1	ML0
DCI (Debug)	1	1	0	(ML2)	(ML3)	DCI-R2D	DCI-D2R

NOTE: Invert HS_FLIP in DCI mode to put DCI-USB on USB3 pins. USB3 and DP not usable in DCI mode.

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: High Speed MUXing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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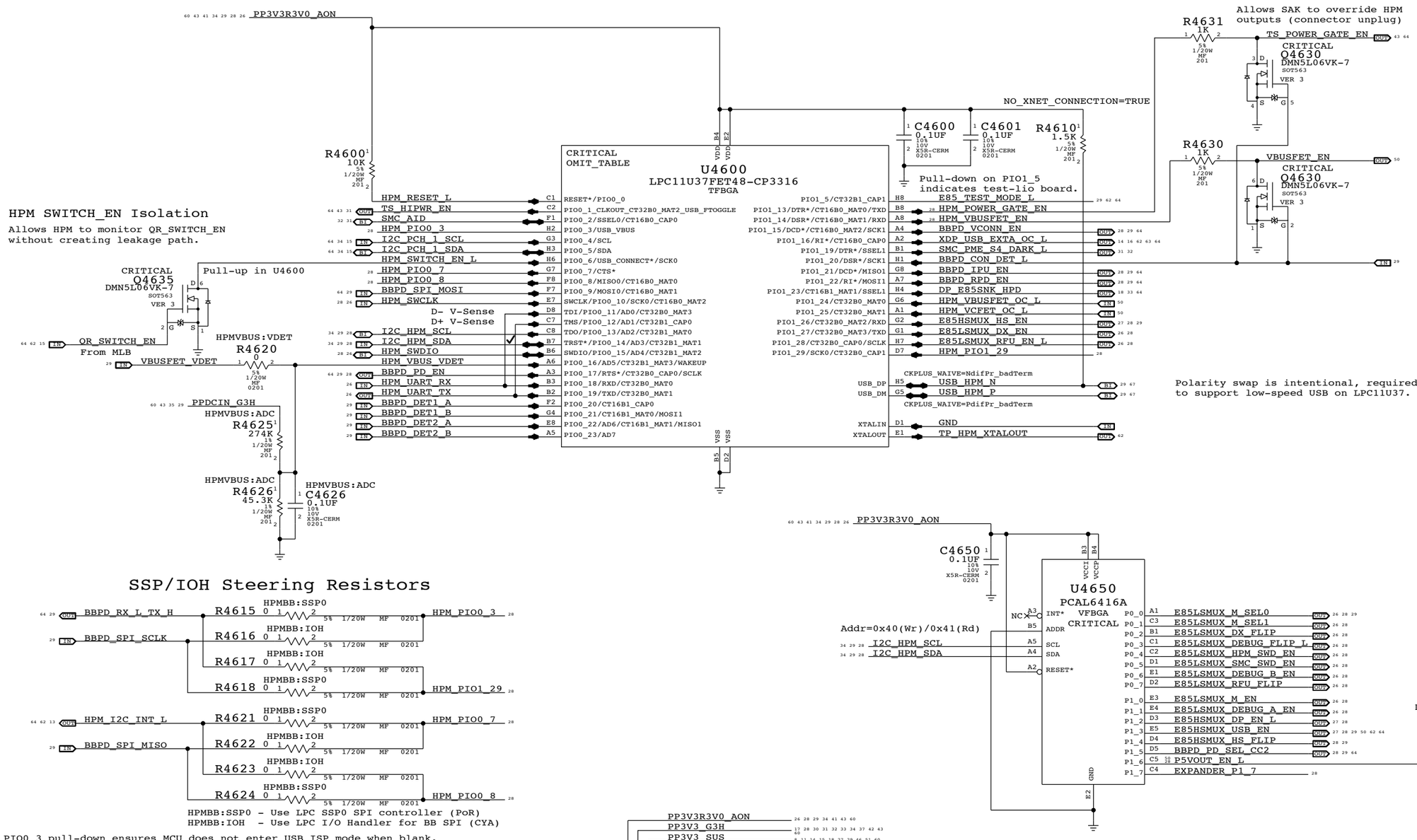

SYNC MASTER=DEV LIO SYNC DATE=04/30/2014

PAGE TITLE

Host Port Micro

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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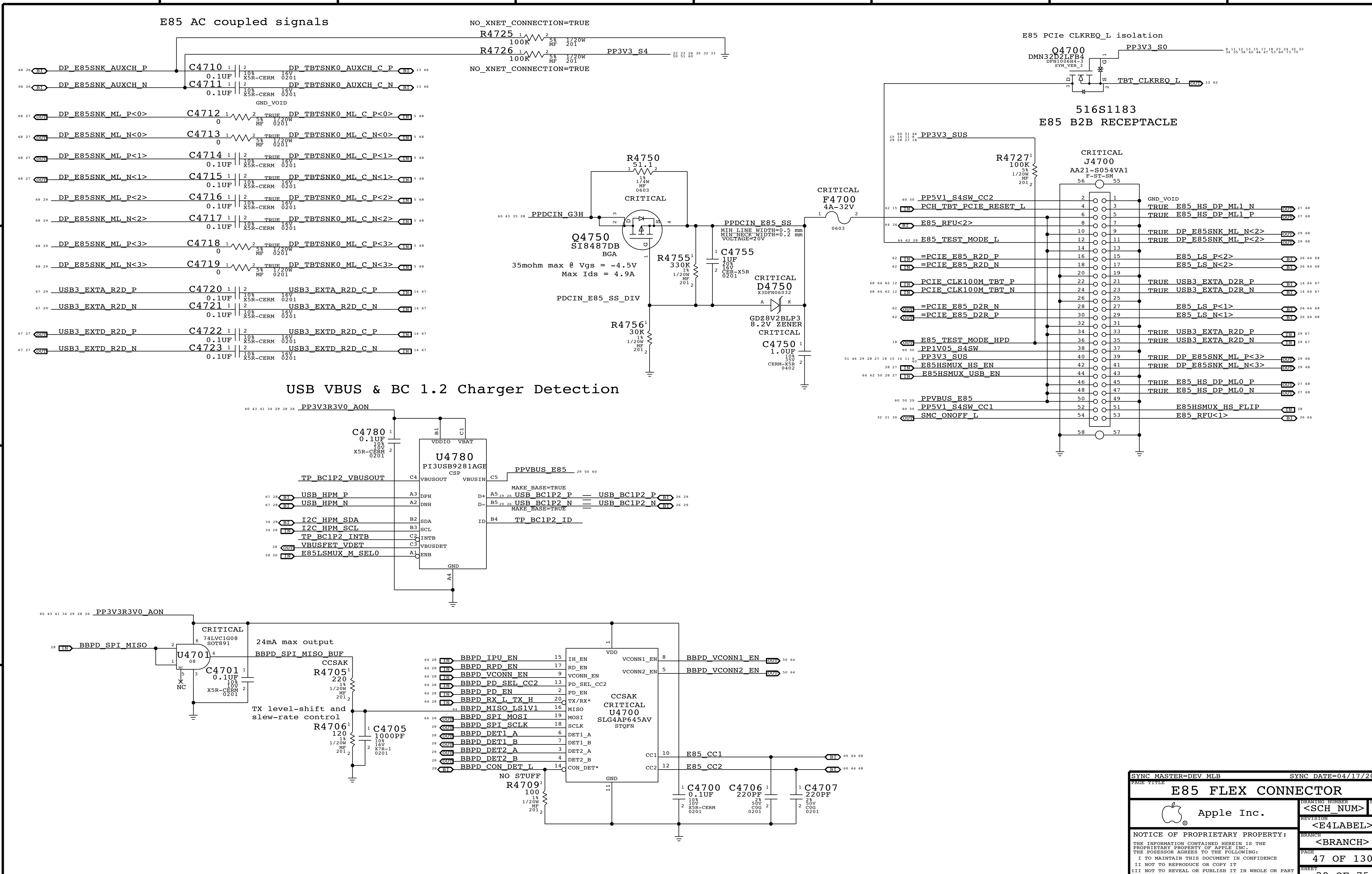

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE

E85 FLEX CONNECTOR

DRAWING NUMBER <SCH_NUM> SIZE D

Apple Inc.

REVISION <E4LABEL>

BRANCH <BRANCH>

IPD ZIF CONNECTOR

Bottom side contacts used
Pinout reversed from flex

518S0854
CRITICAL
J4801
502250-8041
F-RT-SM

TPAD_SPI_CS_L
TPAD_SPI_IF_EN
SMC_PME_S4_WAKE_L
PP3V3_S4_TPAD_F
TP_USB_TPADN
SMC_ACTUATOR_DISABLE_L
SMBUS_SMC_3_SDA
PP3V3_G3H_KBD_F
PP5V_S0_KBD_F

TPAD_SPI_MISO_R
TPAD_SPI_MOSI_R
TPAD_SPI_CLK_R
TPAD_SPI_INT_L
PP3V3_S4_TPAD_F
TP_USB_TPADP
PP5V_S4_TPAD_F
SMBUS_SMC_3_SCL
SMC_LSOC_RST
SMC_ONOFF_L
PP5V_S0_KBD_F
SMC_LID
TP_USB_VBUS_EN

R4802 15 1% 1/20W MF 201 — TPAD_SPI_MISO
R4801 15 1% 1/20W MF 201 — TPAD_SPI_MOSI
R4803 15 1% 1/20W MF 201 — TPAD_SPI_CLK
R4870 100K 5% 1/20W MF 201

CRITICAL
F4800
3A-6A-9V-0.05OHM
0603
PPBUS_G3H — PPBUS_G3H_TPAD_FUSED
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=8.7V

CRITICAL
L4800
30-OHM-5A
0603
PPBUS_G3H_TPAD_FLT
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=8.7V

C4800 0.1uF 20% 10V CERM 402

XW4801
SM
GND_ACTUATOR
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=0V

CRITICAL
L4801
FERR-120-OHM-1.5A
0402-LF
PP3V3_G3H_KBD_F — PP3V3_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C4801 0.1uF 20% 10V CERM 402

CRITICAL
L4802
FERR-120-OHM-1.5A
0402-LF
PP3V3_S4_TPAD_F — PP3V3_S4
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C4802 0.1uF 20% 10V CERM 402

CRITICAL
L4803
FERR-120-OHM-1.5A
0402-LF
PP5V_S4_TPAD_F — PP5V_S4
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4803 0.1uF 20% 10V CERM 402

CRITICAL
L4804
FERR-120-OHM-1.5A
0402-LF
PP5V_S0_KBD_F — PP5V_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4804 0.1uF 20% 10V CERM 402

BYPASS=J4801::1.5MM
BYPASS=J4801::1.5MM
BYPASS=J4801::1.5MM
SMC_LSOC_RST
SMC_ONOFF_L
SMC_LID
C4810 100PF 5% 25V C0G 0201
C4811 100PF 5% 25V C0G 0201
C4812 100PF 5% 25V C0G 0201

SYNC_MASTER=J92_DEVMLB SYNC_DATE=03/26/2014
PAGE TITLE: Keyboard & Trackpad Conn
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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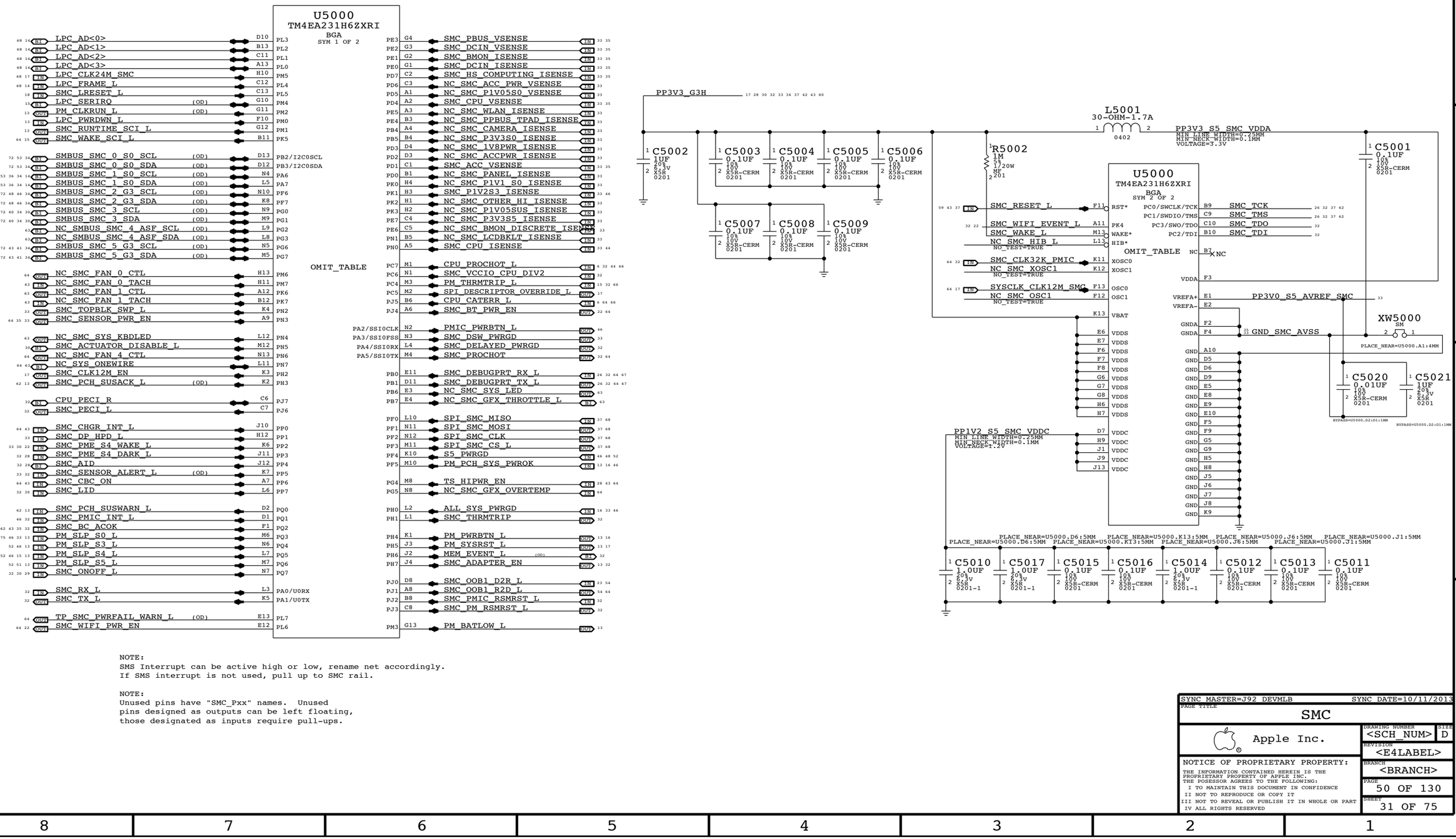

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/11/2013

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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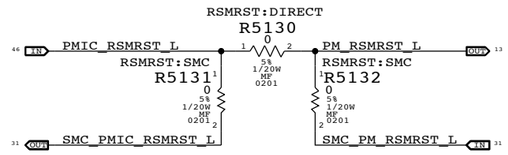

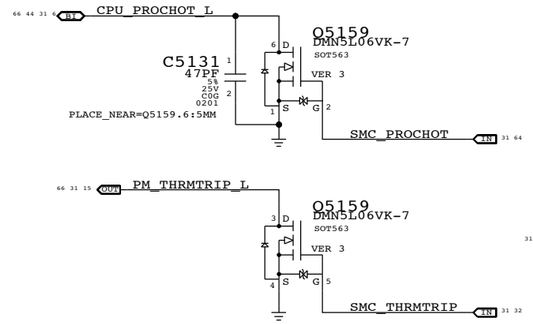

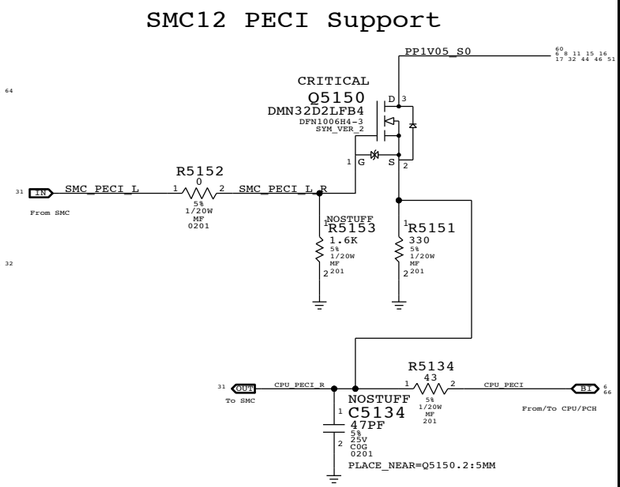

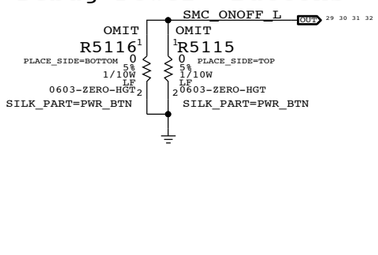

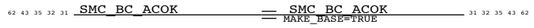

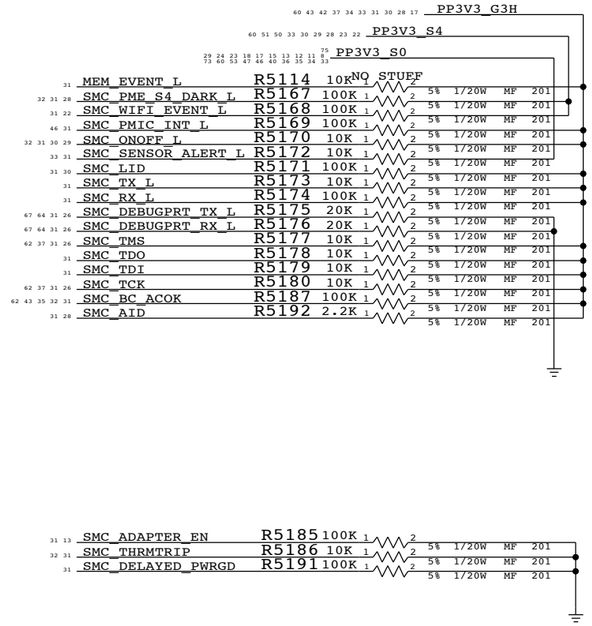

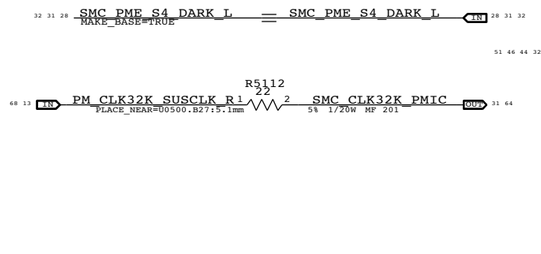

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/11/2013

PAGE TITLE

SMC Shared Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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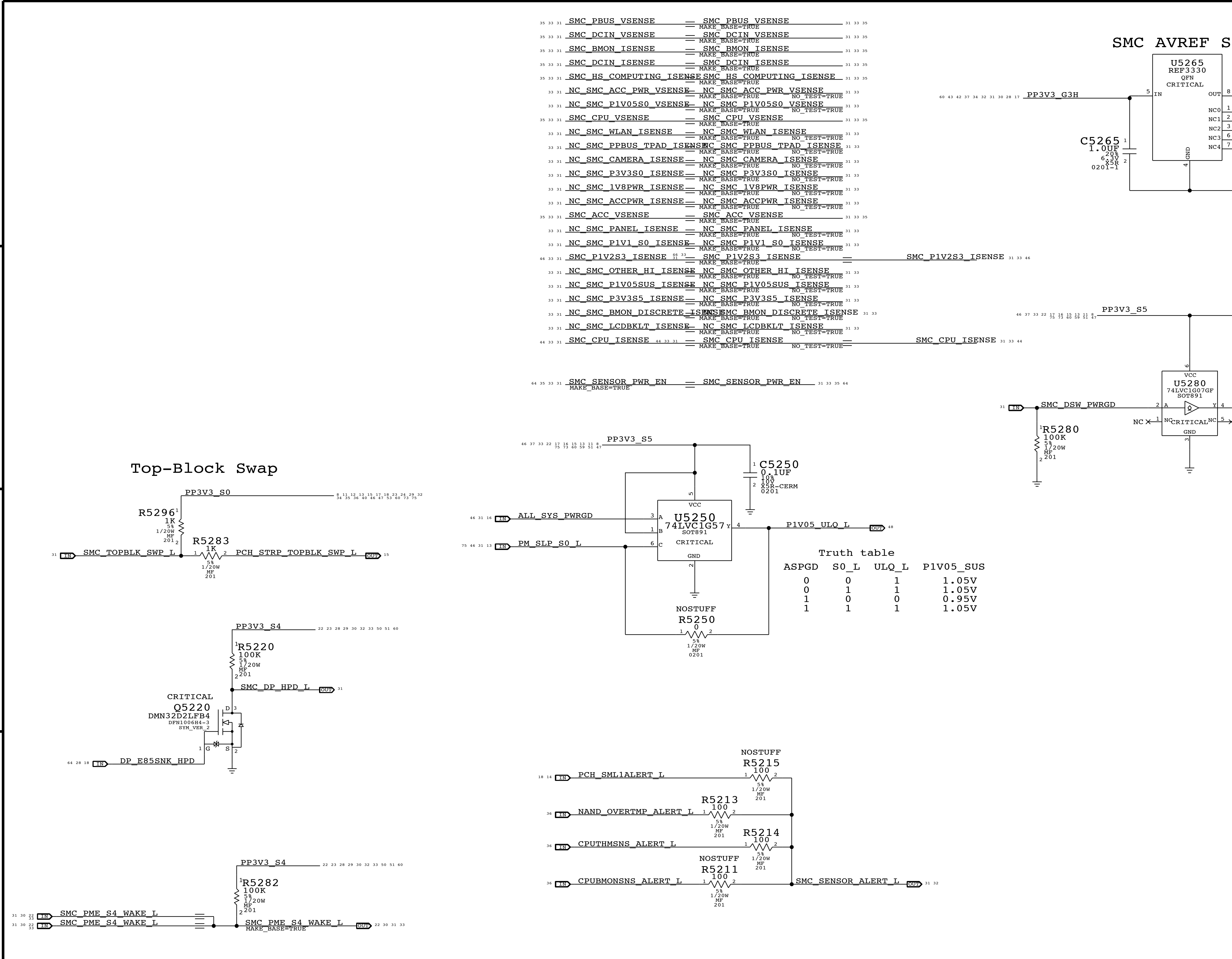

Truth table

ASPGD	S0_L	ULQ_L	P1V05_SUS
0	0	1	1.05V
0	1	1	1.05V
1	0	0	0.95V
1	1	1	1.05V

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE

SMC Project Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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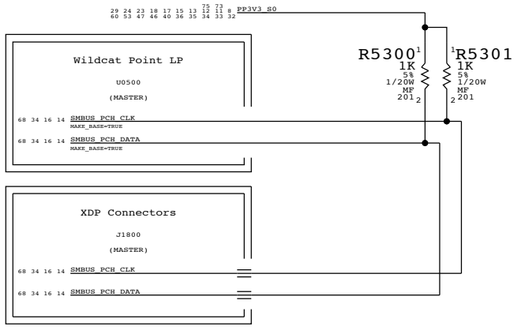
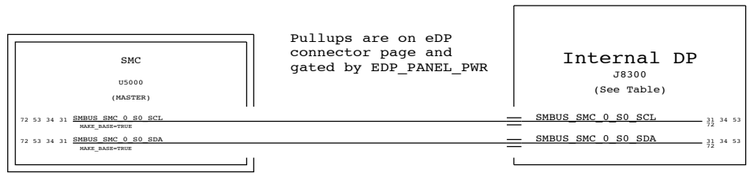
Wildcat Point LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

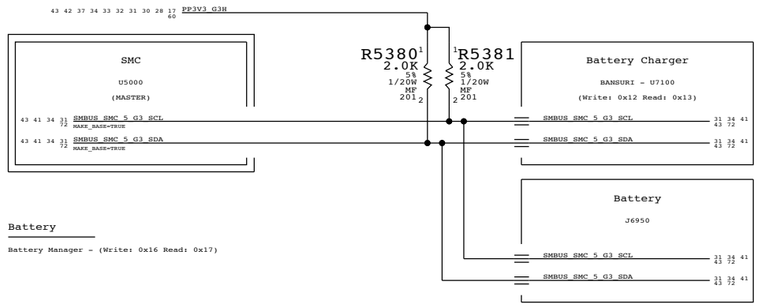


(* = Multiple options)

Internal DP

	J43		J41		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

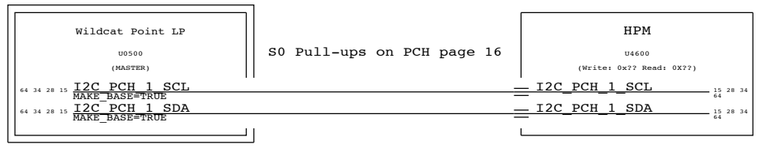
SMC "5" SMBus G3H Connections



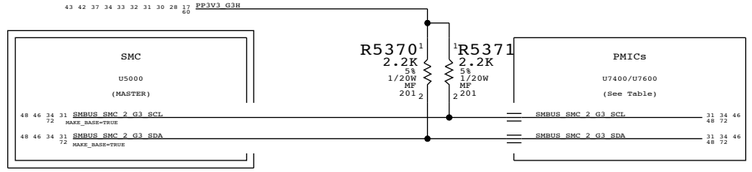
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

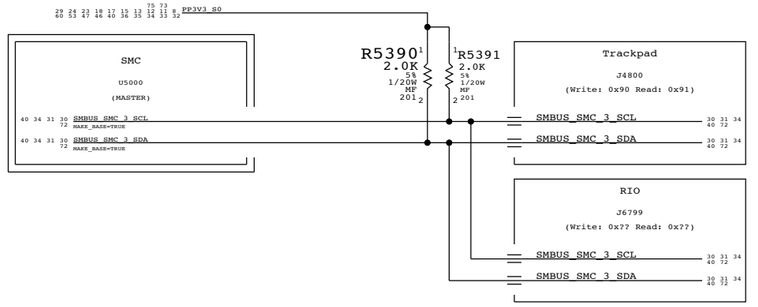
Wildcat Point LP S0 I2C "1" Connections



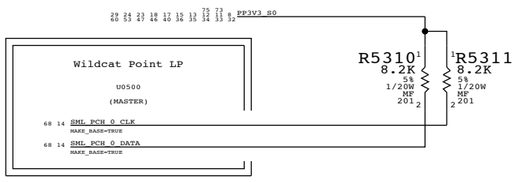
SMC "2" SMBus S3 Connections



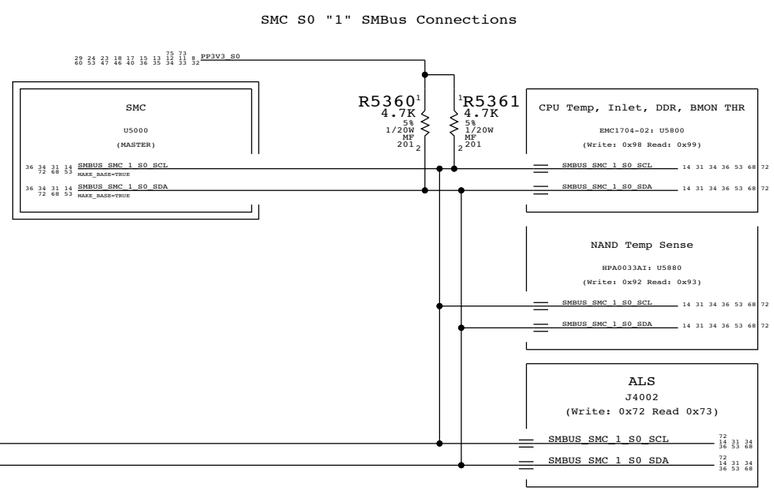
SMC "3" SMBus S0 Connections



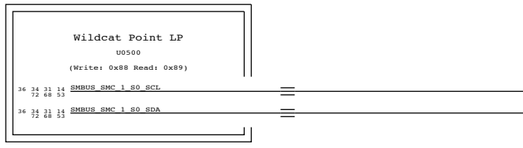
Wildcat Point LP S0 "SMLink 0" Connections



SMC S0 "1" SMBus Connections

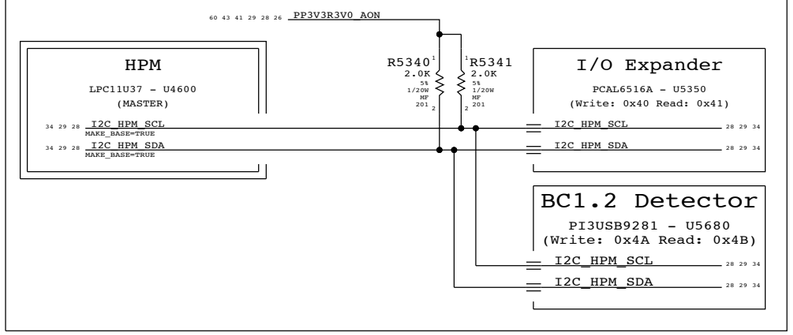


Wildcat Point LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH

HPM Master Bus



SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

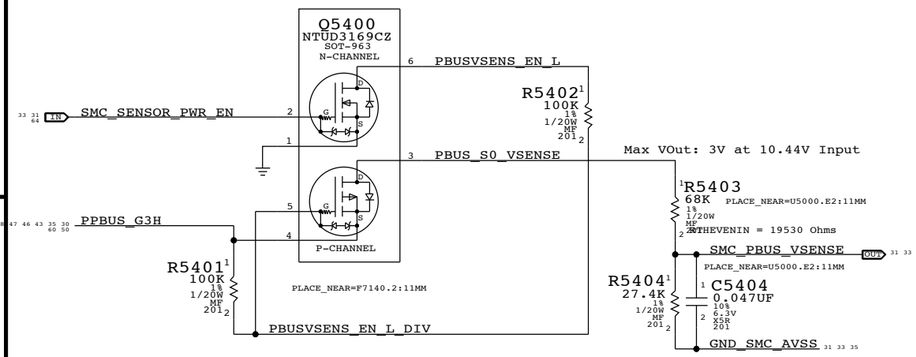
BRANCH: <BRANCH>

PAGE: 53 OF 130

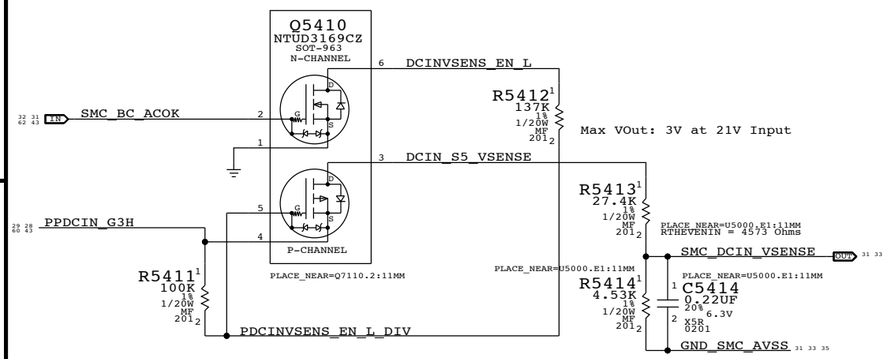
SHEET: 34 OF 75

POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

VP0R: PBUS Voltage Sense Enable & Filter

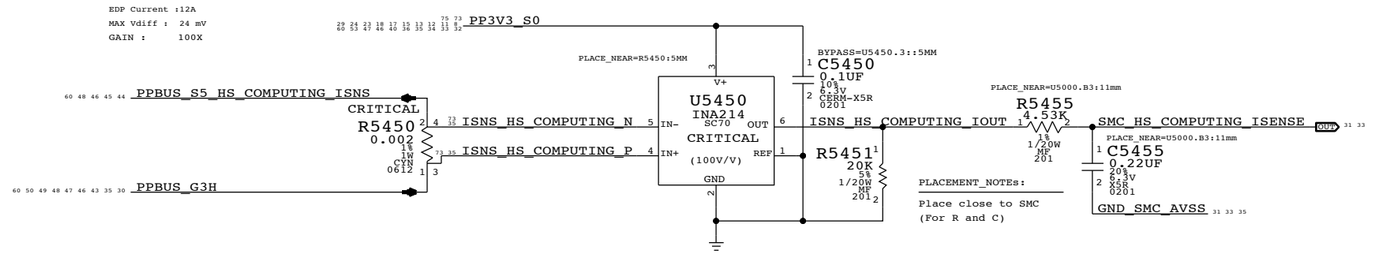


VD0R: DC-In Voltage Sense Enable & Filter



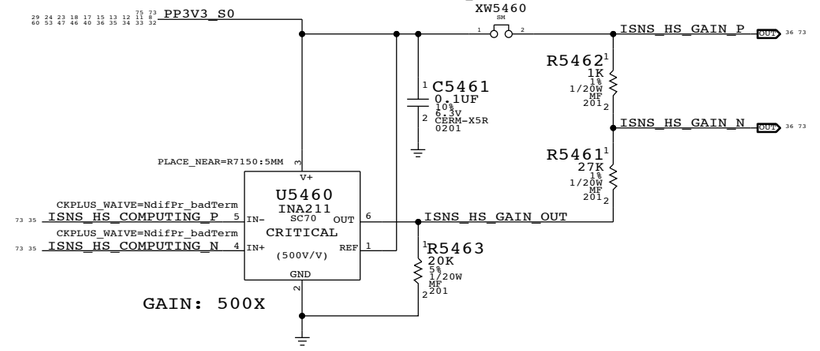
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



Need to set gains for ULX

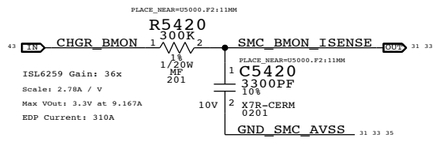
EMC1704 Computing High Side Gain Stage



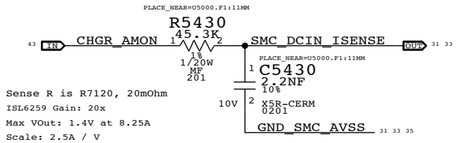
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

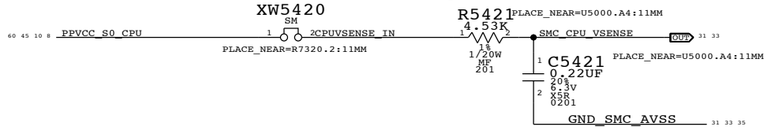
CHARGER BMON High Side Current Sense



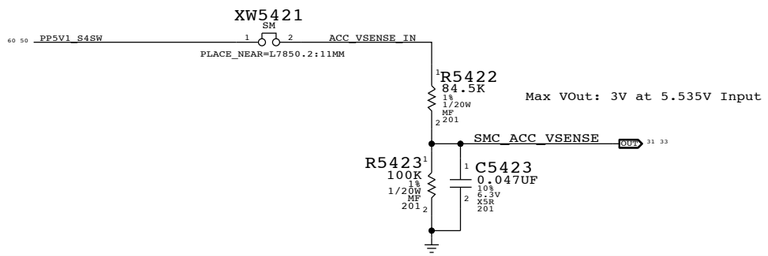
DC-IN (AMON) Current Sense



VCFR CPU Vcore Voltage Sense / Filter



ACC Voltage Sense



SYNC_MASTER=J92_DEVMLB SYNC_DATE=02/07/2014

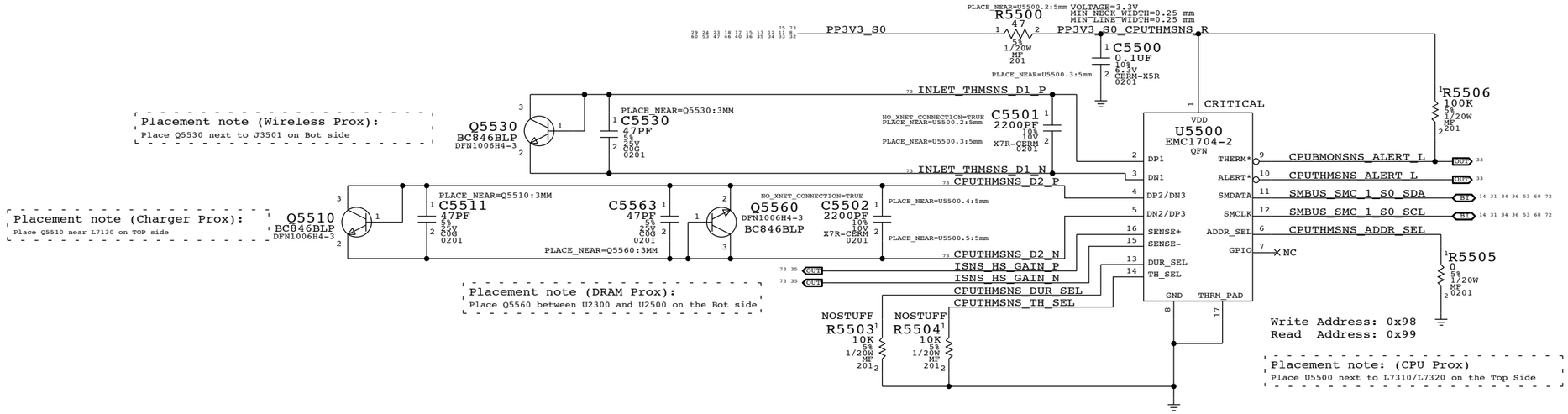
PAGE TITLE: Voltage & Current Sensing

Apple Inc.

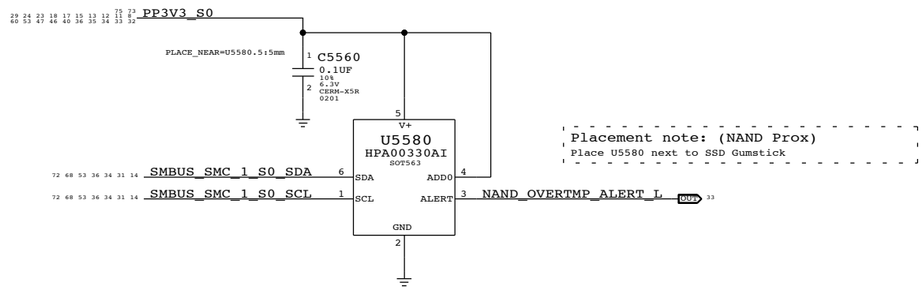
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 130
SHEET: 35 OF 75

POR THERMAL SENSORS : TO BE USED IN PRODUCTION

CPU Proximity, Inlet ,DDR and BMON THR Sensor

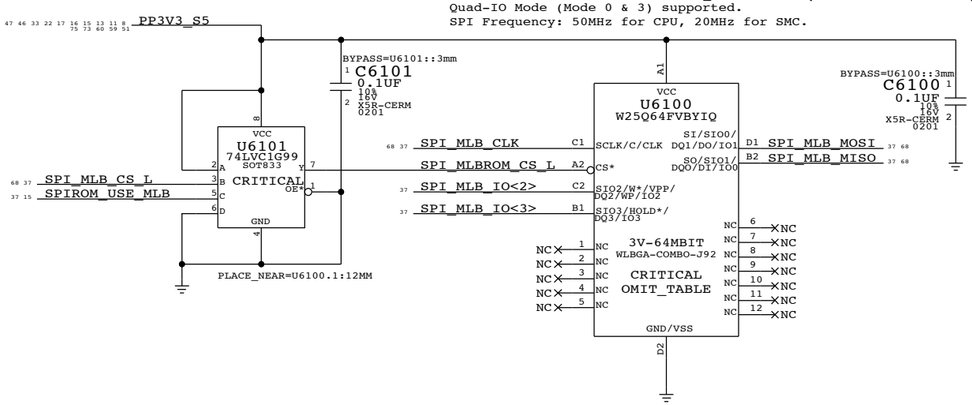


NAND Temp Sensor



SPI ROM - Combo BGA Footprint (3 vendors)

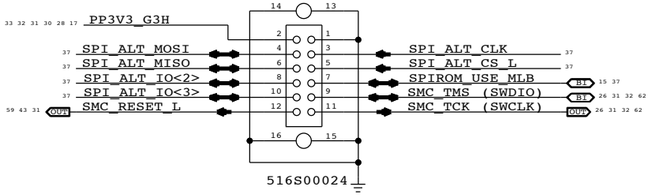
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



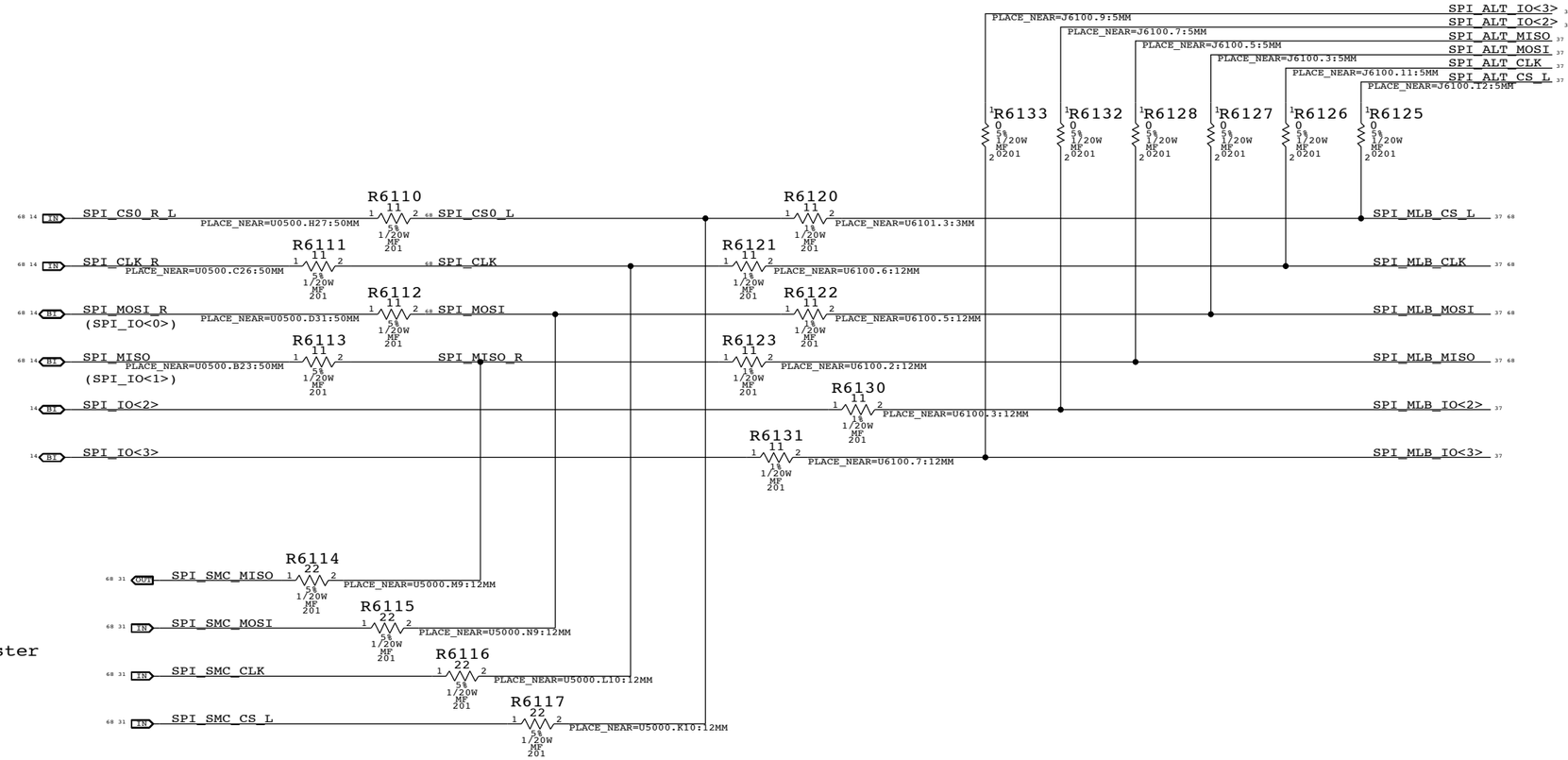
SPI+SWD SAM Connector

CRITICAL

J6100
DF40PC-12DP-0.4V-51
M-ST-SM



BootROM SPI Bus Series Termination



SYNC MASTER=J92 DEVMLB SYNC DATE=07/23/2013

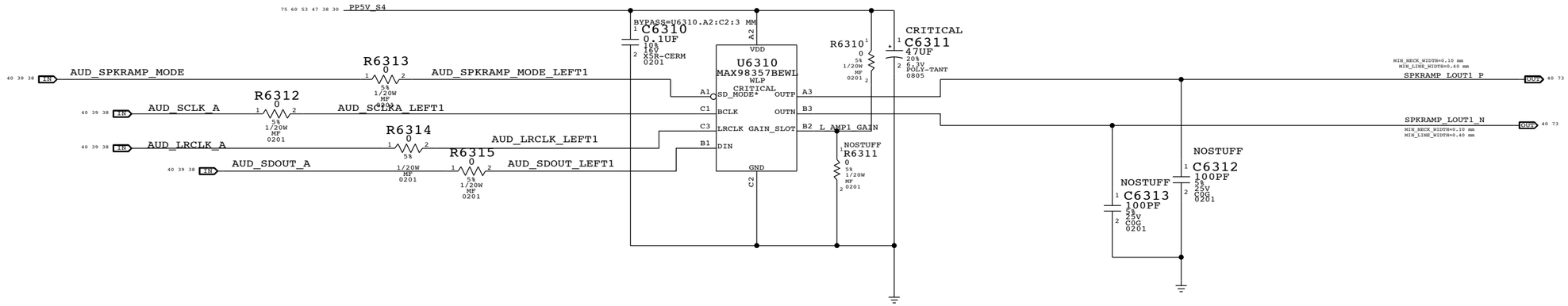
PAGE TITLE
SPI+SWD Debug Connector

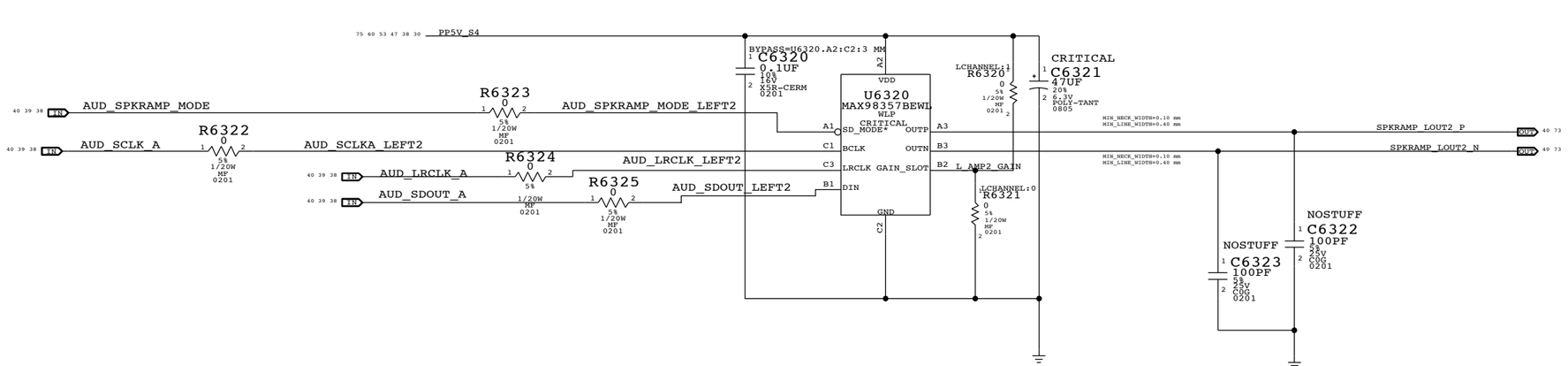
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 61 OF 130
SHEET 37 OF 75

Left Speaker Amps

APPLE P/N 353S4265





SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ:2CH	LCHANNEL:1,RCHANNEL:3
EQ:4CH	LCHANNEL:0,RCHANNEL:4

SYNC MASTER=J92 DEVMLB SYNC DATE=09/19/2013

PAGE TITLE: Audio:Left Speaker Amps

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

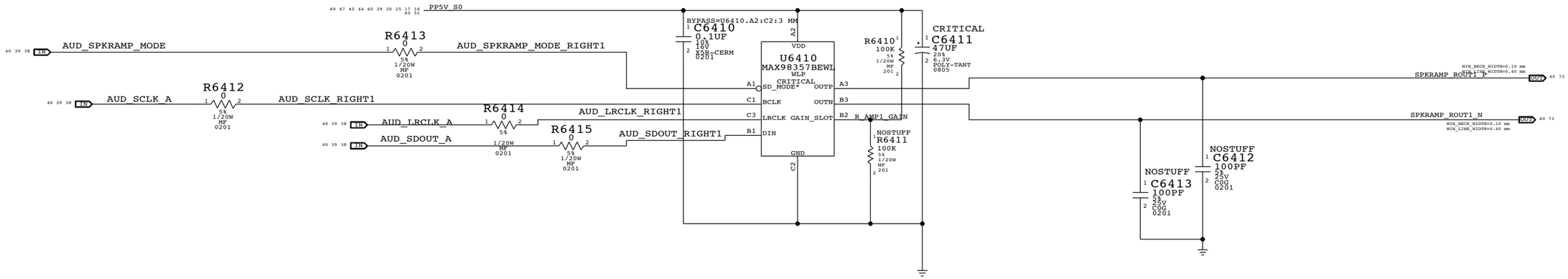
BRANCH: <BRANCH>

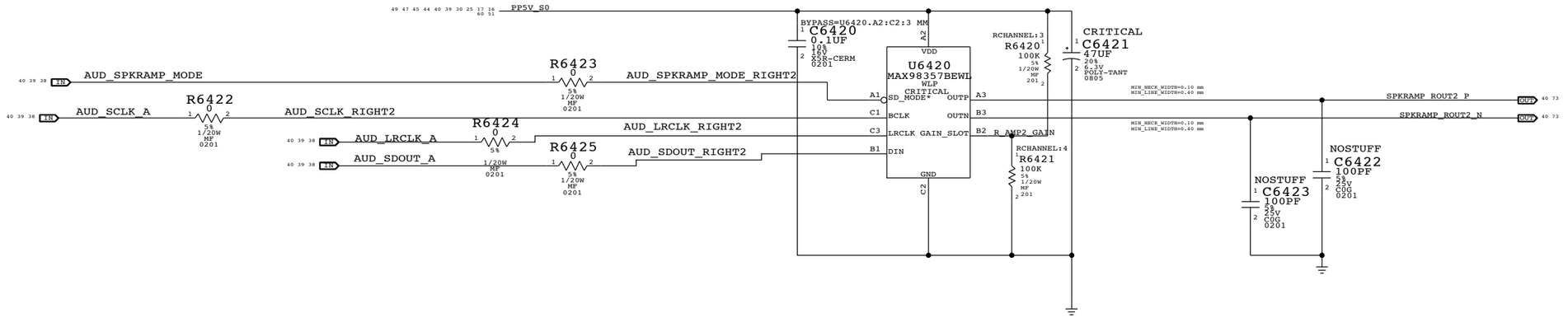
PAGE: 63 OF 130

SHEET: 38 OF 75

Right Speaker Amps

APPLE P/N 353S4265





SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE

Audio:Right Speaker Amps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 64 OF 130

SHEET 39 OF 75

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)		0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

CODEC INPUT SIGNAL PATHS

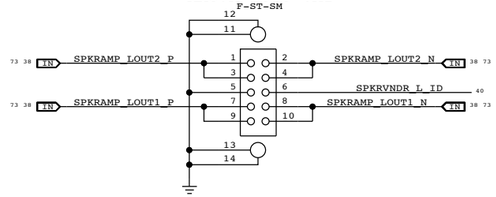
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SOUTHBRIDGE RESOURCE/PIN ALLOCATIONS

FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 3
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 5
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 16
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	BCH SMBUS 0

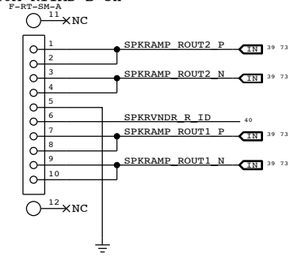
LEFT SPEAKER CONN

516S0899
CRITICAL
J6750
AA07A-S010-VA1
F-ST-SM

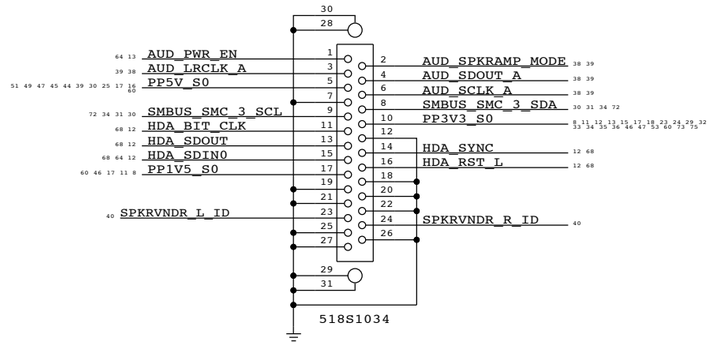


RIGHT SPEAKER CONN

518S00014
CRITICAL
J6751
FF18-10A-R11AD-B-3H
F-RT-SM-A



CRITICAL
J6799
502250-8027
F-RT-SM



RIO FLEX CONN

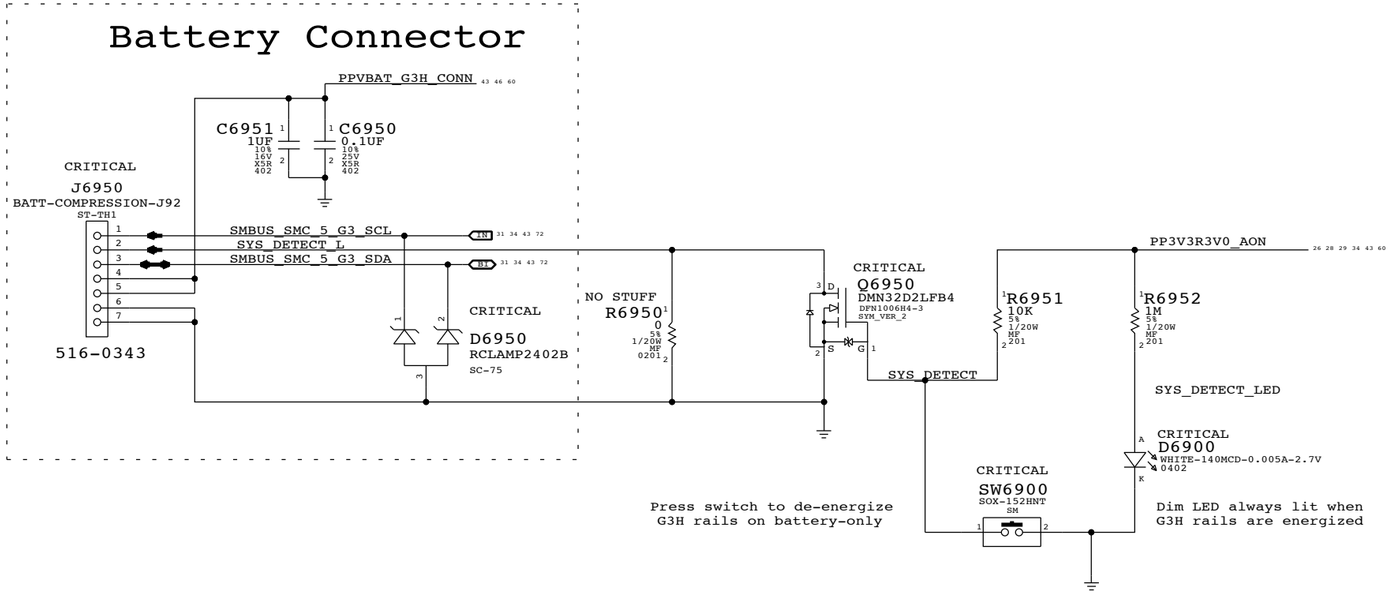
SYNC_MASTER=CARA J92 SYNC_DATE=04/17/2014

PAGE TITLE
AUDIO: CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 67 OF 130
SHEET 40 OF 75

Battery Connector



SYNC MASTER=J43_MLB SYNC DATE=10/24/2012

PAGE TITLE: Battery Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

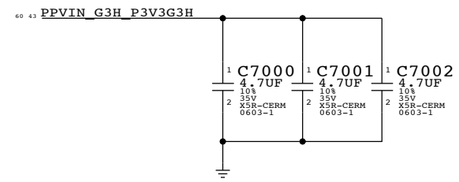
REVISION: <E4LABEL>

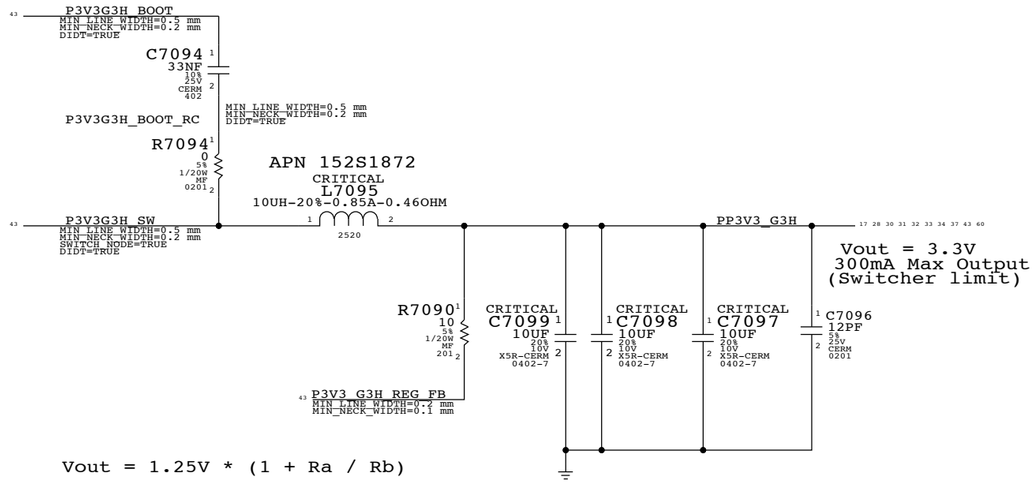
BRANCH: <BRANCH>

PAGE: 69 OF 130

SHEET: 41 OF 75

3.3V G3H VR - Bansuri





Vout = 1.25V * (1 + Ra / Rb)

SYNC MASTER=J92 WILL SYNC DATE=02/04/2013

PAGE TITLE
3.3V G3Hot Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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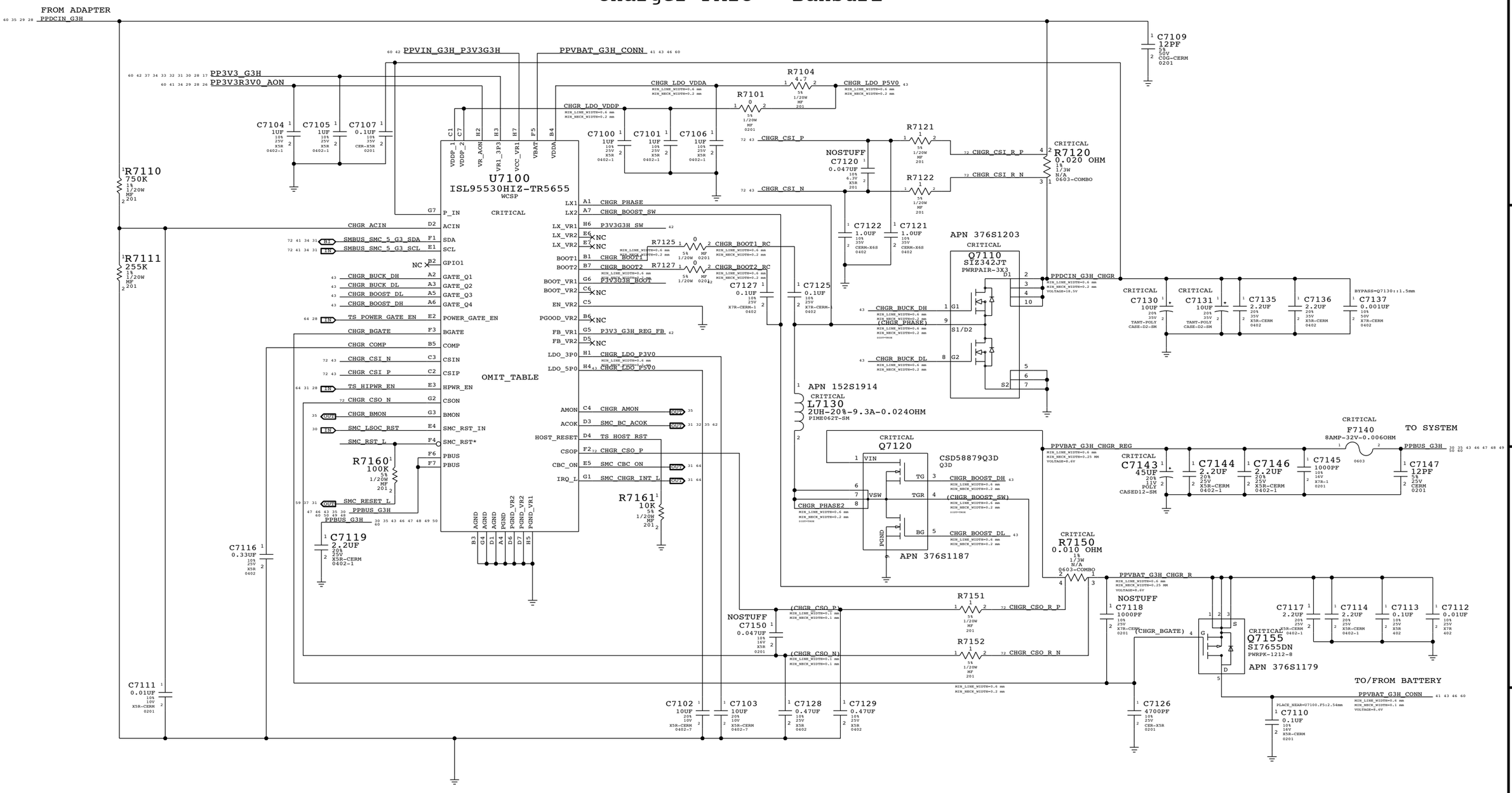
SHEET 42 OF 75

Charger PMIC - Bansuri



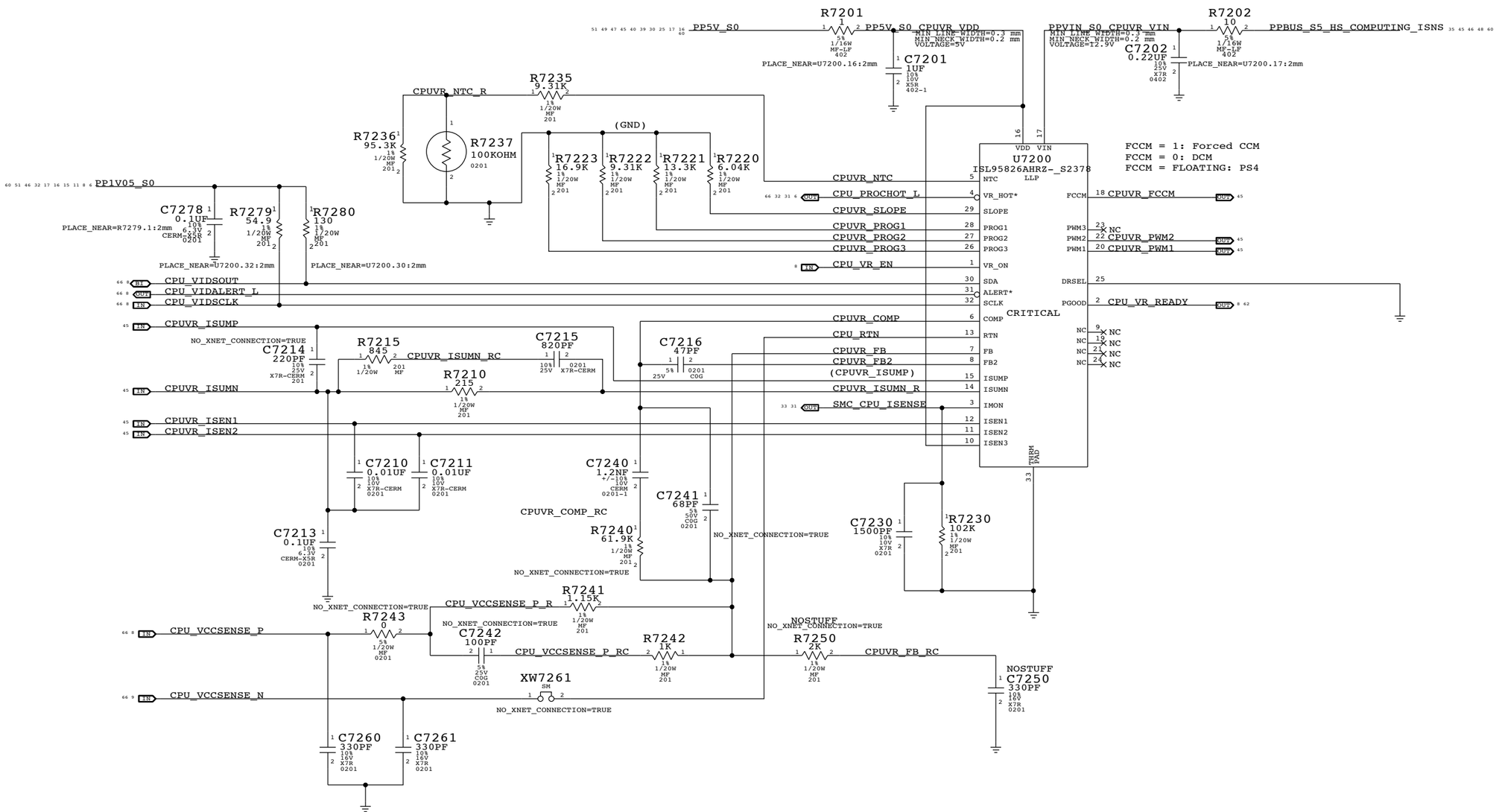
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00347	1	IC,ISL95530B1T11,CHGR PMU,BANSURI,WCSP56	U7100	CRITICAL	

SYNC_MASTER=J92 DEVMLB SYNC_DATE=04/04/2014

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 71 OF 130
SHEET 43 OF 75



SYNC_MASTER=J43_MLB SYNC_DATE=10/09/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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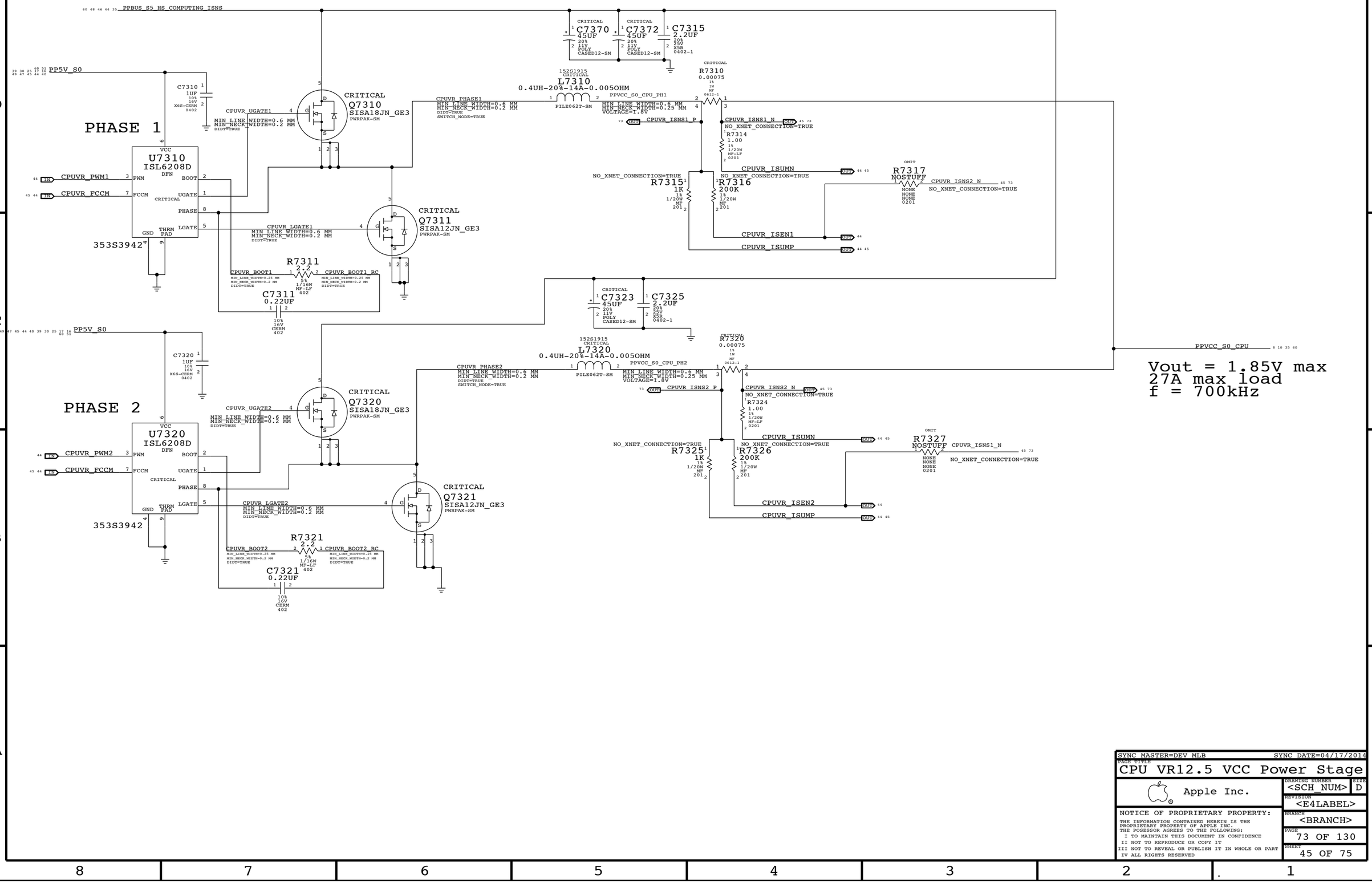
SHEET 44 OF 75



SYNC MASTER=DEV_MLB SYNC DATE=04/17/2014

PAGE TITLE
CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 73 OF 130
SHEET 45 OF 75

TPS650811 (Walrus):

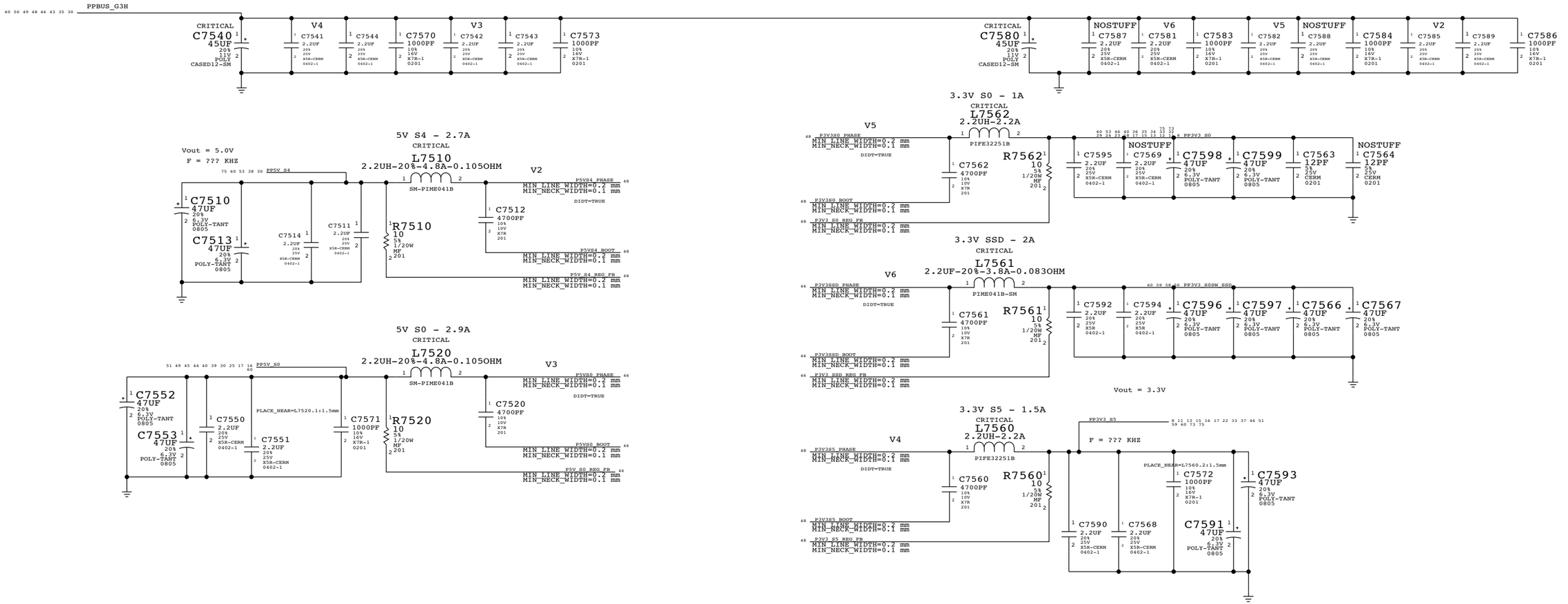
- OTP
- Power-up State Machine
- 32kHz / 24MHz
- RTC Domain
- Coin Cell Charger
- Overtemp V12.6 Interface
- Power Button
- AC/DC Detection
- EC RESET
- Emergency RESET Handler
- V3 Converter (V5Dx_WP)
- V6 Converter (V3.3Dx_SSD)
- V7 Converter (V1.8U)
- V10 Controller (V1.2U)
- V11 LDO (V0.6Dx)
- V12 LDO (2.5V/1.5V)
- Ref Sys
- GPIOs
- ADC
- Power Monitor Unit
- Interrupt Handler
- Battery Detection
- Digital Block
- I2C

- 3V LDO
- 5V LDO

V10 (V1.2U VR)

V12 LDO (1.5V)

SYNC MASTER=J92_DEVMLB	SYNC DATE=04/04/2014
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 130
	SHEET 46 OF 75



SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: 5V & 3.3V Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 75 OF 130

SHEET: 47 OF 75

TPS650801 (Dolphin):
- OTP
- I2C
- LED Drivers
- V2 Converter (V5A_DS3)
- V4 Converter (V3.3A_DSW)
- V5 Converter (V3.3Dx)
- V8 Converter (V1.5S - UNUSED)
- V9 Controller (V1.05A)
- 3V LDO
- 5V LDO
- Digital Block
- Ref Sys

CRITICAL
U7600
SN650801
BGA
SYM 1 OF 2
DEVICE CONTROL
INTERNAL BIASING

PMIC_ADC_EN F3
AGND_PMIC H4
PMIC2_READY H3
PMIC2_CRITTEMP H10
PMIC2_PROCHOT K4
PMIC2_THERMP E10
PMIC2_THERMN F10
PMIC_VREF3V3
PMIC2_VCTRL K6
PMIC2_VCTRL02 G3
PMIC_VREF3V3_RC K1
SMBUS_SMC_2_G3_SCL J8
SMBUS_SMC_2_G3_SDA H8
(Float = 0x34/0x35) NCX
TP_PMIC_LEDDRV1 K9
TP_PMIC_LEDDRV2 J7
TP_PMIC_LEDDRV3 K8
TP_PMIC_LEDDRV4 J6

IMON_EN
VLDO3.3V_EN
RDY
CRITTEMP
HOT
TP
TN
VDDIO A11
VDDIO B10
VIN5V
VCTRL2
VIN3.3VA
SCL
SDA
SLAVEADDR
LEDDRV1
LEDDRV2
LEDDRV3
LEDDRV4

VIN L9
VINLDO3.3V D8
VLDO3.3V B11
VREF1.25V D9
VCTRL0 J2
VCTRL K7
AGND J1
AGND K10
AGND L11
GND F9
GND H2
GND L10
GND D5
GND D6
GND E4
GND E5
GND E6
GND E7
GND E8
GND F4
GND F5
GND F6
GND F7
GND F8
GND G4
GND G5
GND G6
GND G7
GND G8
GND H5
GND H6
GND H7

PPBUS_G3H
PMIC_VREF3V3
PMIC2_VREF1V25
PMIC2_VCTRL02
PMIC2_VCTRL
AGND_PMIC

R7602 10 5% 1/16W MF-LF 402
C7601 0.1UF 10% 10V X5R-CERM 0201
C7602 1.0UF 20% 6.3V X5R 0201-1
C7603 10UF 20% 6.3V CERM-X6S 0402
C7608 10UF 20% 6.3V CERM-X6S 0402
C7607 10UF 20% 6.3V CERM-X6S 0402
C7604 1UF 20% 10V X5R 0201
C7605 1UF 20% 10V X5R 0201
C7606 2.2UF 20% 6.3V X5R-CERM 0201
C7600 2.2UF 20% 25V X5R-CERM 0402-1

XW7699 SM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V

CRITICAL
U7600
SN650801
BGA
SYM 2 OF 2

P5V_S4_EN K5
P5V_S4_MODE J5
P5V_S4_PGOOD J4
P5V_S4_IMON C10
V2_EN
V2_MODE
PGOOD2
V2_IMON
V2-V5A_DS3

VIN2 L6
VIN2 L7
BOOTSTRAP2 L8
LX2 L4
LX2 L5
PGND2 L2
PGND2 L3
VOUT2 K3
FB2 L1
FB2 K2

P5V_S4_REG_FB
P5V_S4_PHASE
P5VS4_BOOT

P3V3_S5_EN G10
P3V3_S5_MODE G9
S5_PWRGD H9
P3V3_S5_IMON E9
V4_EN
V4_MODE
PGOOD4
V4_IMON
V4-V3.3A-DSW

VIN4 E11
VIN4 F11
BOOTSTRAP4 D11
LX4 G11
LX4 H11
PGND4 J11
PGND4 K11
VOUT4 J9
FB4 J10

P3V3_S5_REG_FB
P3V3S5_PHASE
P3V3S5_BOOT

P3V3_S0_EN E3
P3V3_S0_MODE E2
P3V3_S0_PGOOD D3
P3V3_S0_IMON C11
V5_EN
V5_MODE
PGOOD5
V5_IMON
V5-V3.3DX

VIN5 F1
VIN5 G1
BOOTSTRAP5 H1
LX5 D1
LX5 E1
PGND5 B1
PGND5 C1
VOUT5 C2
FB5 A1
FB5 B2

P3V3_S0_REG_FB
P3V3S0_PHASE
P3V3S0_BOOT

V8_EN B7
V8_MODE C8
V8SEL D2
PGOOD8 D7
V8_IMON D10
V8-V1.5S

VIN8 A5
VIN8 A6
BOOTSTRAP8 B6
LX8 A7
LX8 A8
PGND8 A9
PGND8 A10
VOUT8 B9
FB8 C9

NC
NC
NC
NC
NC

P1V05_SUS_EN B8
P1V05_SUS_MODE C7
P1V05_SUS_PGOOD G2
P1V05_SUS_IMON D4
P1V05_ULQ_L F2
P1V05_SUS_ILIM B3
V9_EN
V9_MODE
PGOOD9
V9_IMON
V9_ULQ
ILIMSET9
V9-V1.05A

VBST9 B4
SW9 A4
DRVH9 B5
DRVL9 A2
PGND9 A3
ISP9 C4
ISN9 C5
FB9 C6

ISNS_1V05_SUS_P
ISNS_1V05_SUS_N

R7635 8.66K 1% 1/20W MF 201

V9 (V1.05A VR)

PPBUS_S5_HS_COMPUTING_ISNS
CRITICAL C7620 45UF 20% 11V POLY CASED12-SM
C7622 1000PF 5% 25V CERM 0402
C7624 2.2UF 20% 25V X5R-CERM 0402-1
NOSTUFF C7625 2.2UF 20% 25V X5R-CERM 0402-1

P1V05SUS_BOOT_RC
C7630 0.1UF 10% 16V X7R-CERM 0402
R7630 0 5% 1/16W MF 402
P1V05SUS_VBST
P1V05SUS_DRVH
P1V05SUS_LL
P1V05SUS_DRVL

APN 376S00012
CRITICAL
Q7630
CSD58889Q3D
Q3D
VIN 1
TG 3
TGR 4
VSW 6 7 8
BG 5
PGND 9

APN 152S1913
CRITICAL
L7630
1UH-20%-10.2A-0.014OHM
PIME052T-SM
P1V05_SUS_PHASE
XW7601 SM
P1V05_SUS_PHASE_XW
R7634 121K 1% 1/20W MF 201
XW7600 SM
BB: to 12nF
NO_XNET_CONNECTION=TRUE
C7634 0.015UF 10% 6.3V X5R 0201
ISNS_1V05_SUS_RC
NO_XNET_CONNECTION=TRUE
R7636 0201
100KOHM
ISNS_1V05_SUS_NTC
R7640 31.6K 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
XW7610 SM

R7637 20K 1% 1/20W MF 201
R7641 10 5% 1/20W MF 201
P1V05SUS_VDDQSNS
P1V05SUS_VDDQSNS_R

C7636 0.47UF 10% 6.3V CERM-X5R 0201
AGND_PMIC

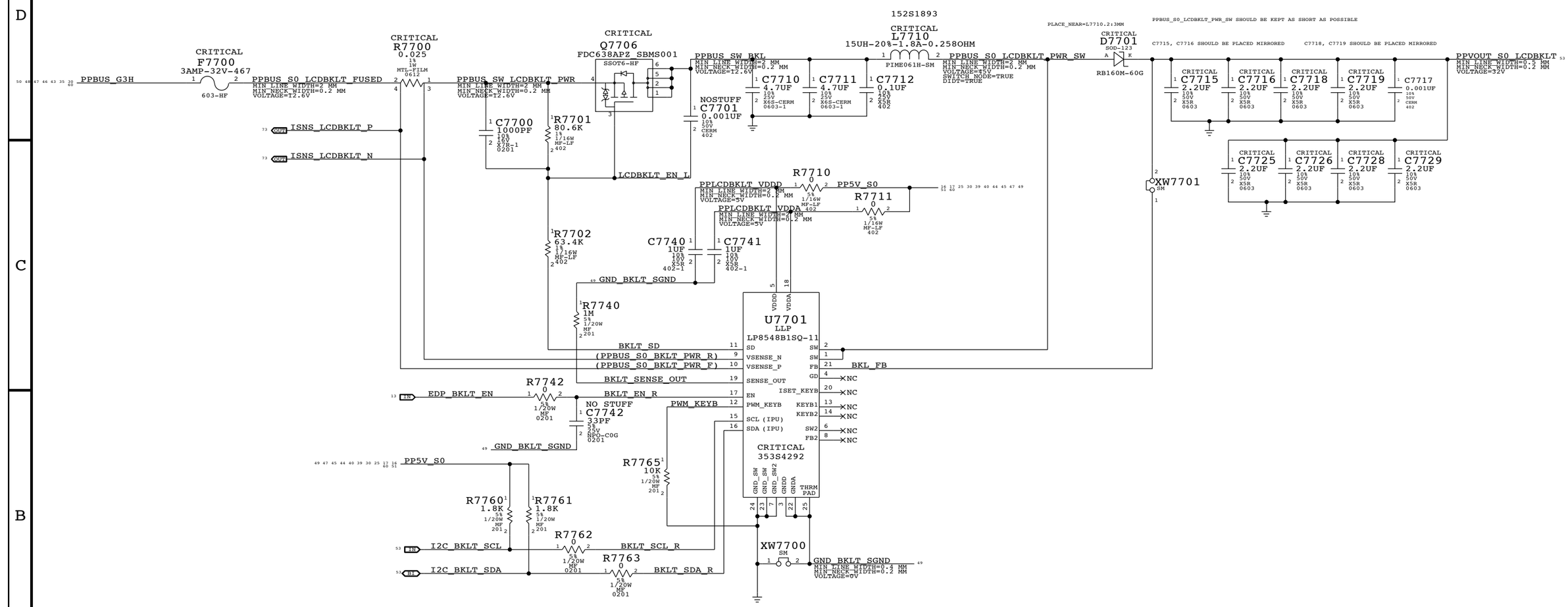
PP1V05_SUS
Vout = 1.05V
5A Max Output
f = ? kHz
C7626 10UF 20% 10V X5R-CERM 0402-1
C7623 10UF 20% 10V X5R-CERM 0402-1
CRITICAL C7648 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C7649 270UF 20% 2V TANT CASE-B2-SM
C7647 12PF 5% 25V CERM 0201

SYNC_MASTER=J92_DEVMLB SYNC_DATE=04/04/2014
PAGE TITLE: 1.05V S0 Power Supply
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 76 OF 130
SHEET: 48 OF 75

Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (6-8.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production



SYNC MASTER=J92 DEVMLB	SYNC DATE=10/01/2013
PAGE TITLE	LCD Backlight Driver
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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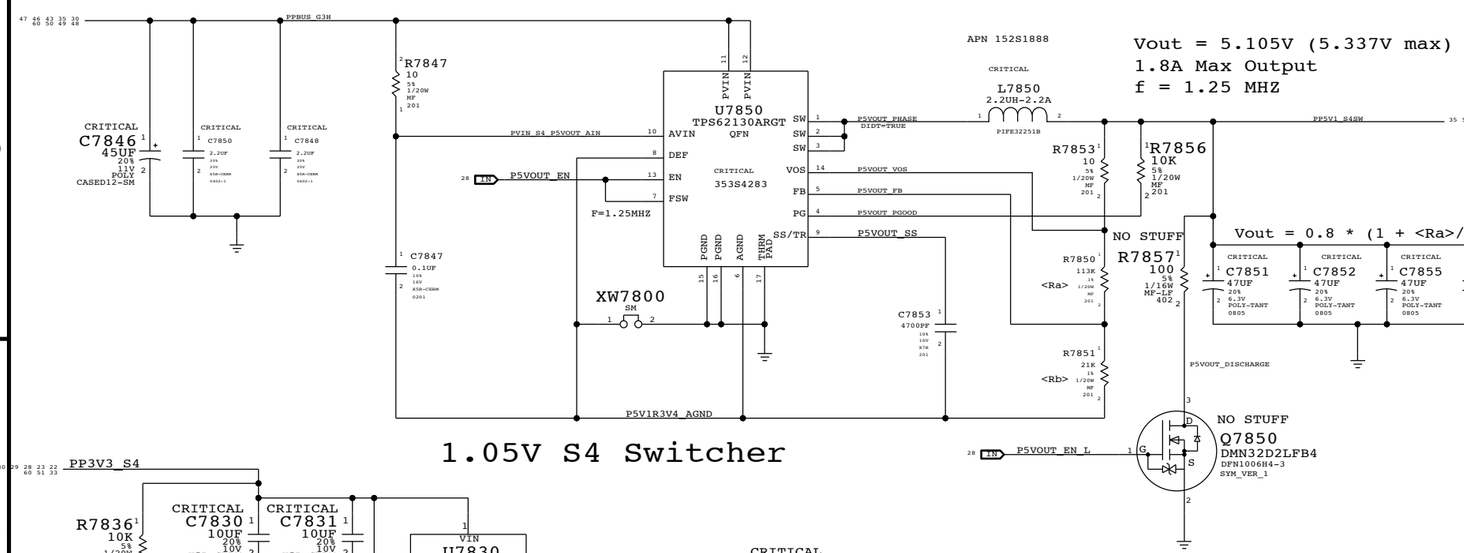
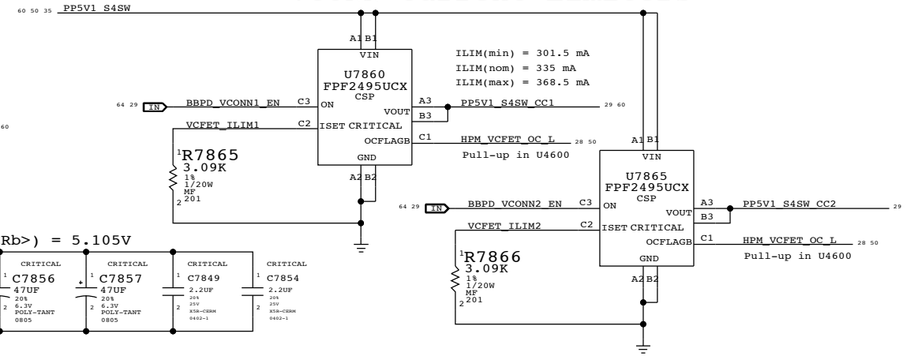
	SHEET 49 OF 75

E85 VBUS/VCONN 5V VR

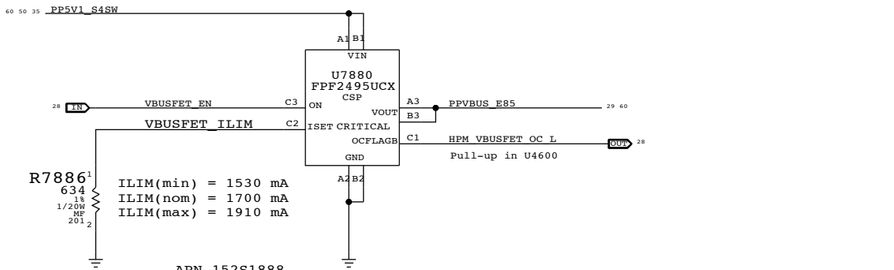


1.05V S4 Switcher

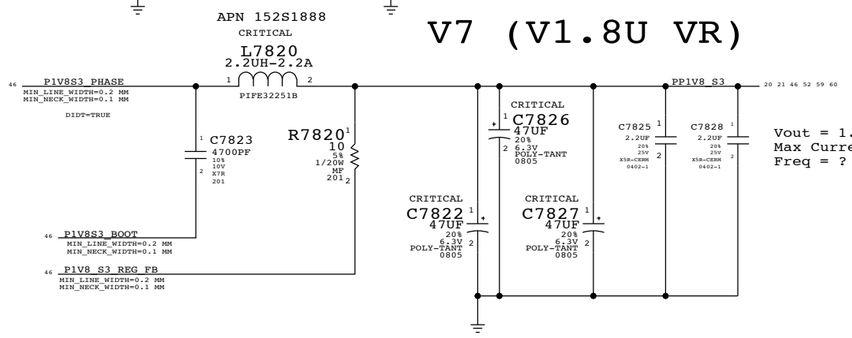
VCONN Current Limiters



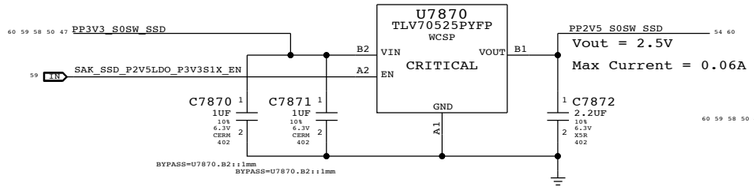
VBUS Current Limiter/OVP IC



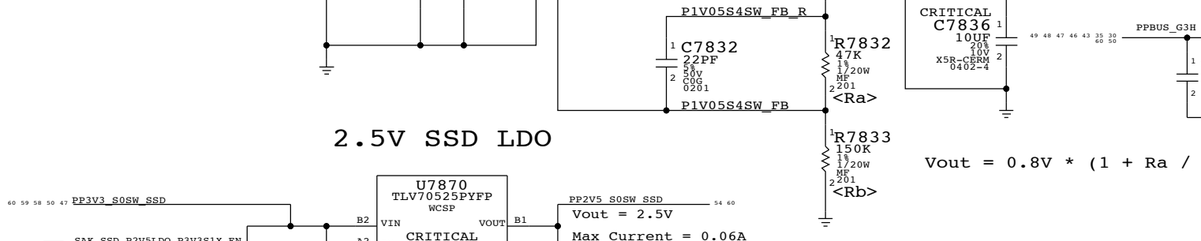
V7 (V1.8U VR)



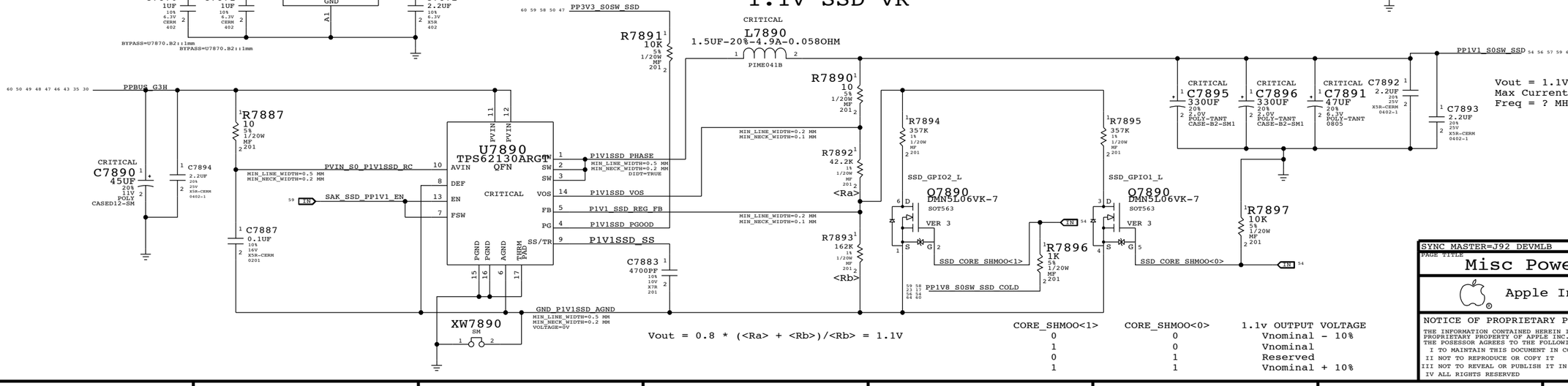
2.5V SSD LDO



2.5V S4 LDO



1.1V SSD VR



CORE_SHMOO<1>	CORE_SHMOO<0>	1.1v OUTPUT VOLTAGE
0	0	Vnominal - 10%
1	0	Vnominal
0	1	Reserved
1	1	Vnominal + 10%

SYNC_MASTER=J92_DEVMLB SYNC_DATE=04/04/2014

PAGE TITLE

Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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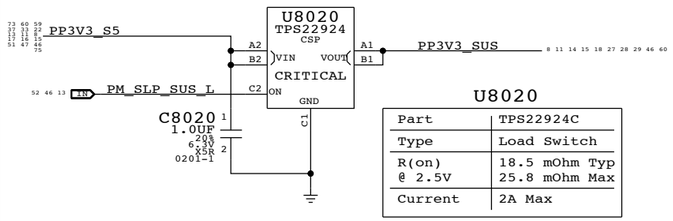
SHEET 50 OF 75

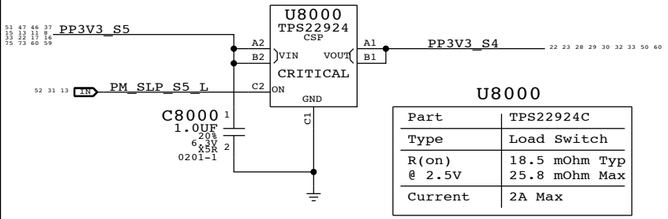
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

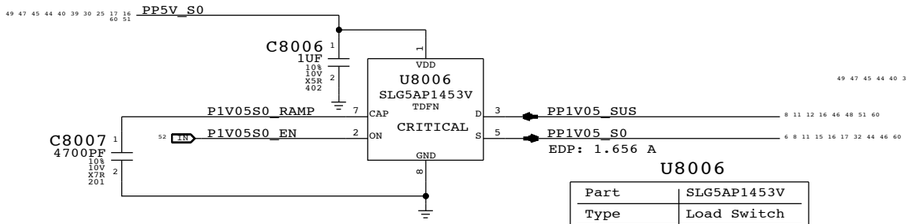
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

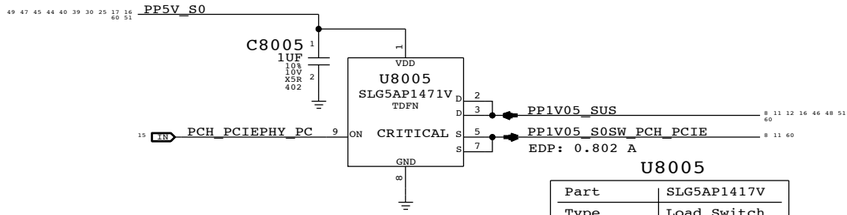
1.05V S0 Switch



U8006

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH PCIe Switch

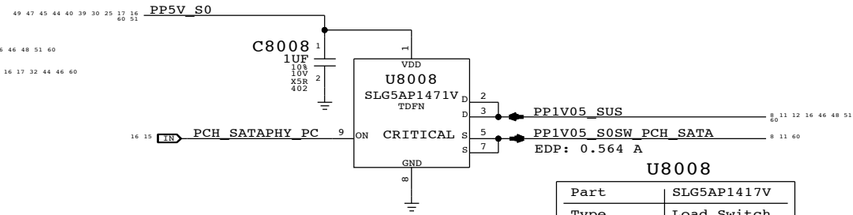


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH SATA Switch

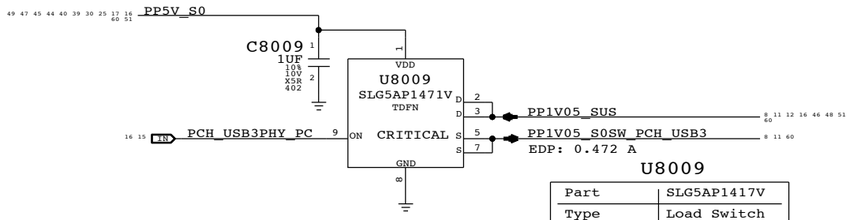


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8008

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH USB3 Switch



HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8009

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/24/2013

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SHEET: 51 OF 75

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S5 Power Good

52 48 46 31 IN S5_PWRGD = S5_PWRGD OUT 31 46 48 52
MAKE_BASE=TRUE

LPDDR power down sequencing support

PP1V8_S3 20 21 46 50 59 60
NO STUFF D8170 SOD-962 PMEG1201AESF
PP1V2_S3 8 10 19 20 21 46 59 60 69

SUS & S4 Enables

52 51 31 13 IN PM_SLP_S5_L = PM_SLP_S5_L OUT 13 31 51 52
MAKE_BASE=TRUE

52 51 46 13 IN PM_SLP_SUS_L = PM_SLP_SUS_L OUT 13 46 51 52
MAKE_BASE=TRUE

S3 Enables

46 IN PMIC_V8_EN
R8117 0 5% 1/20W MF 0201
46 31 15 13 IN PM_SLP_S4_L
NO STUFF D8115 0201 RB521ES-30
P1V8S3_EN_D
NO STUFF R8116 30K 5% 1/20W MF 201
NO STUFF R8115 1K 5% 1/20W MF 201
52 46 P1V8S3_EN = P1V8S3_EN OUT 46 52
MAKE_BASE=TRUE
NO STUFF C8116 0.1UF 10% 6.3V CERM-X5R 0201

S0 Enables

46 31 13 IN PM_SLP_S3_L
D8182 0201 RB521ES-30
D8181 0201 RB521ES-30
D8183 0201 RB521ES-30
P1V5S0_EN_D
P3V3S0_EN_D
P1V05S0_EN_D
R8182 4.99K 1% 1/20W MF 201
R8185 30K 5% 1/20W MF 201
R8181 2.0K 5% 1/20W MF 201
R8186 20K 5% 1/20W MF 201
R8183 1K 5% 1/20W MF 201
R8184 10K 5% 1/20W MF 201
R8187 0 5% 1/20W MF 201
C8185 0.1UF 10% 6.3V CERM-X5R 0201
C8186 0.1UF 10% 6.3V CERM-X5R 0201
C8184 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C8187 0.1UF 10% 6.3V CERM-X5R 0201

52 46 P5VS0_EN = P5VS0_EN OUT 46 52
MAKE_BASE=TRUE
52 51 P1V05S0_EN = P1V05S0_EN OUT 51 52
MAKE_BASE=TRUE
52 46 P3V3S0_EN = P3V3S0_EN OUT 46 52
MAKE_BASE=TRUE
52 46 P1V5S0_EN = P1V5S0_EN OUT 46 52
MAKE_BASE=TRUE

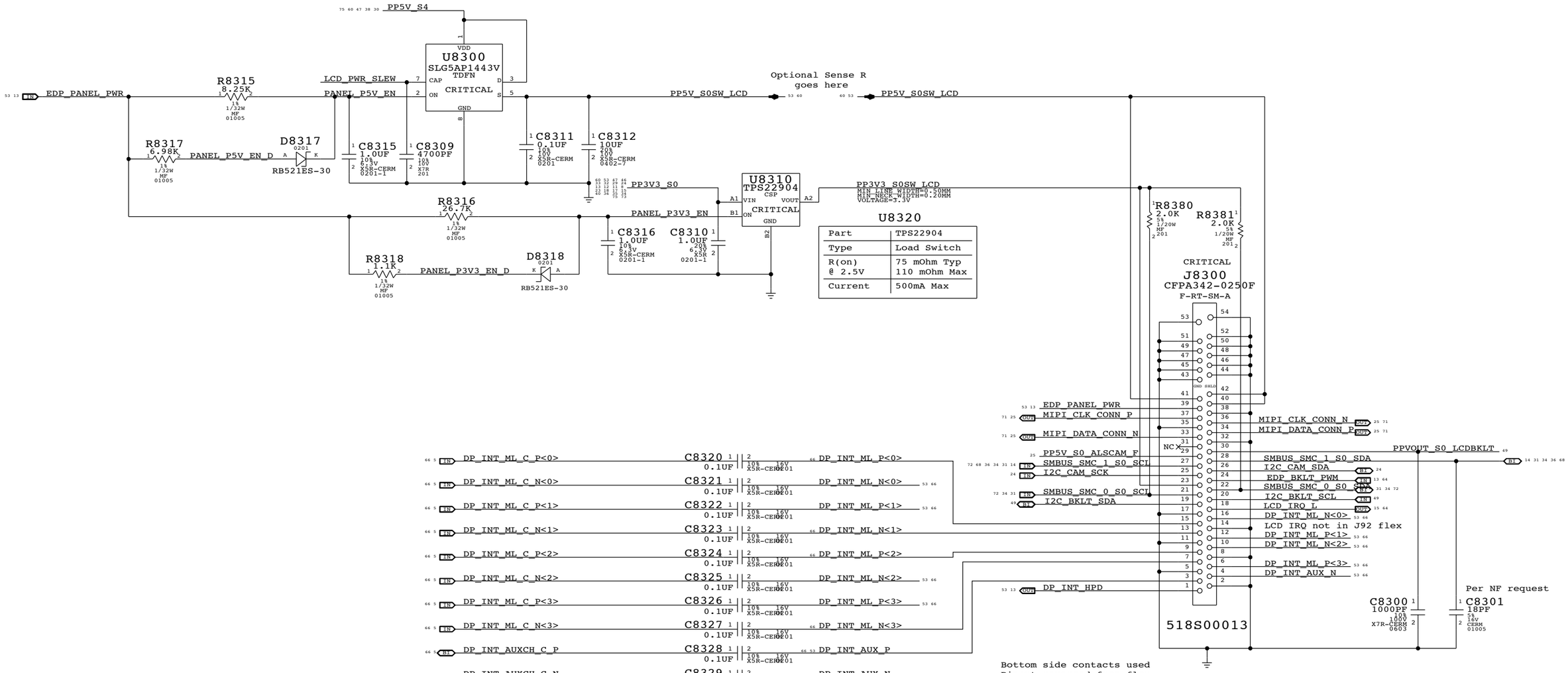
SYNC MASTER=J92 DEVMLB SYNC DATE=09/20/2013

PAGE TITLE: Power Control

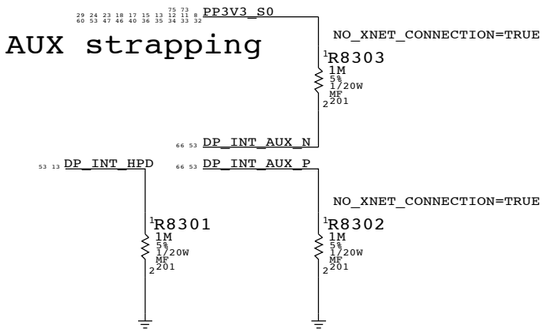
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 81 OF 130
SHEET: 52 OF 75

LCD PANEL INTERFACE (eDP) + Camera (MIPI)



LCD Panel HPD & AUX strapping



SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/25/2013

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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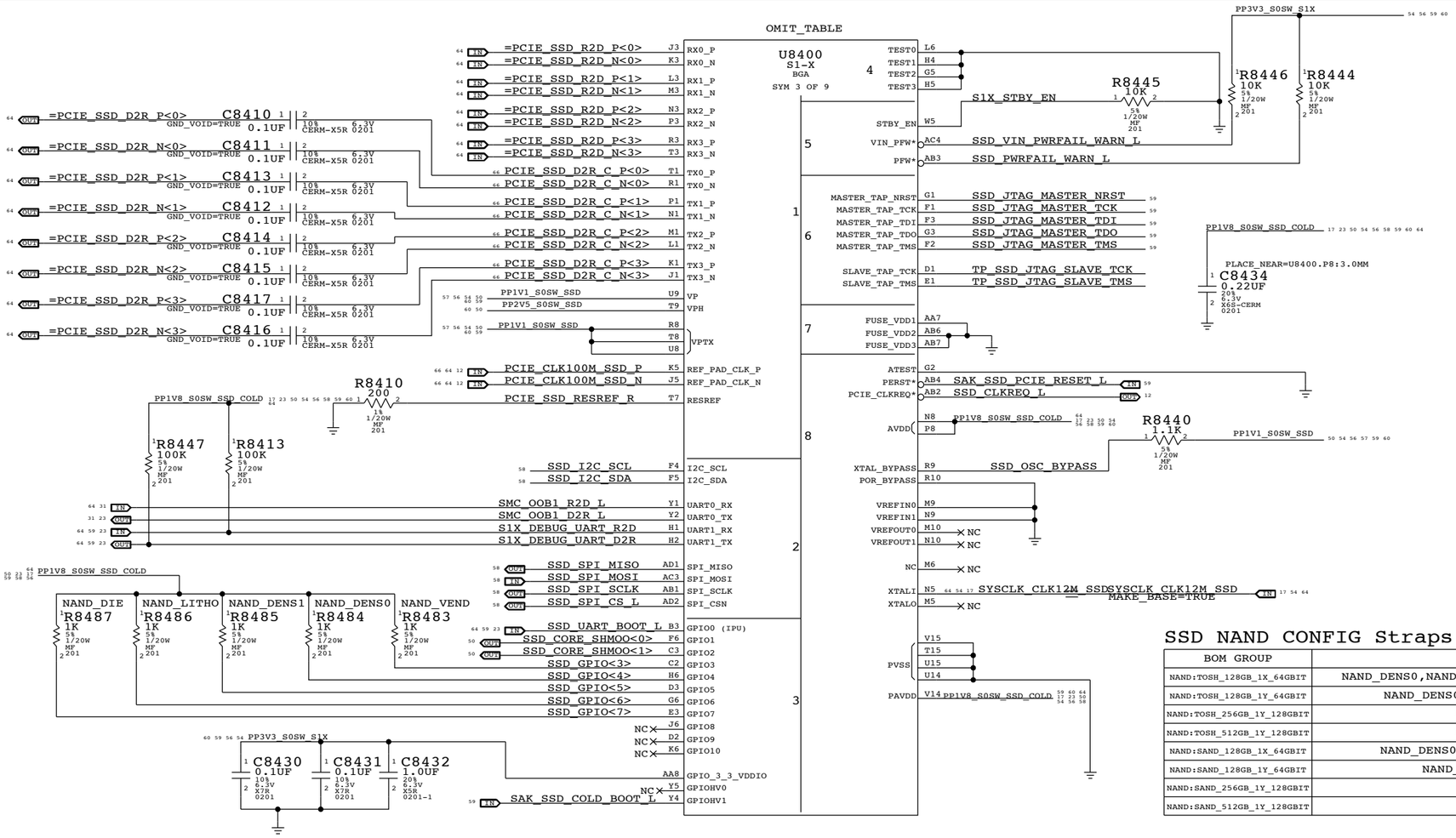
SHEET: 53 OF 75



SSD NAND CONFIG Straps

BOM GROUP	BOM OPTIONS
NAND:TOSH_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_LITHO,NAND_DIE,NAND_TYPE:TOSH_128GB_1X_64GBIT
NAND:TOSH_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_DIE,NAND_TYPE:TOSH_128GB_1Y_64GBIT
NAND:TOSH_256GB_1Y_128GBIT	NAND_VEND,NAND_DENS1,NAND_TYPE:TOSH_256GB_1Y_128GBIT
NAND:TOSH_512GB_1Y_128GBIT	NAND_VEND,NAND_DENS0,NAND_TYPE:TOSH_512GB_1Y_128GBIT
NAND:SAND_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_LITHO,NAND_DIE,NAND_TYPE:SAND_128GB_1X_64GBIT
NAND:SAND_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_DIE,NAND_TYPE:SAND_128GB_1Y_64GBIT
NAND:SAND_256GB_1Y_128GBIT	NAND_DENS1,NAND_TYPE:SAND_256GB_1Y_128GBIT
NAND:SAND_512GB_1Y_128GBIT	NAND_DENS0,NAND_TYPE:SAND_512GB_1Y_128GBIT

SSD NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-7360	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1X_64GBIT
335S00004	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1Y_64GBIT
335S1031	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_256GB_1Y_128GBIT
335S1032	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_512GB_1Y_128GBIT
998-7361	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1X_64GBIT
335S1044	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1Y_64GBIT
335S1041	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_256GB_1Y_128GBIT
335S1045	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_512GB_1Y_128GBIT

S1-X GPIO[10:1] IPD

VENDOR	NAND_VEND(GPIO3)
TOSHIBA	1
SANDISK	0

DENSITY	NAND_DENS0(GPIO4)	NAND_DENS1(GPIO5)
128GB	1	1
256GB	0	1
512GB	1	0

LITHO	NAND_LITHO(GPIO6)
1X	1
1Y	0

DIE SIZE	NAND_DIE(GPIO7)
64Gb	1
128Gb	0

# NAND_CH	(GPIO8)
8 (X56)	1
4 (J92)	0

SYNC MASTER=J92 SSD
SYNC DATE=02/11/2014

PAGE TITLE
SSD Controller (1 of 4)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 84 OF 130
SHEET 54 OF 75

OMIT_TABLE

U8400
S1-X
BGA
SYM 1 OF 9

70 58	OUT	ANI0_ALE	F18	ANI0_ALE	ANI2_ALE	E12	NC
70 58	OUT	ANI0_CLE	D19	ANI0_CLE	ANI2_CLE	D11	NC
70 58	BI	ANI0_DQS_N	B20	ANI0_DQS_N	ANI2_DQS_N	B14	NC
70 58	BI	ANI0_DQS_P	A20	ANI0_DQS_P	ANI2_DQS_P	A14	NC
70 58	BI	ANI0_IO<0>	B22	ANI0_IO0	ANI2_IO0	A16	NC
70 58	BI	ANI0_IO<1>	A23	ANI0_IO1	ANI2_IO1	A11	NC
70 58	BI	ANI0_IO<2>	B21	ANI0_IO2	ANI2_IO2	B16	NC
70 58	BI	ANI0_IO<3>	A22	ANI0_IO3	ANI2_IO3	B11	NC
70 58	BI	ANI0_IO<4>	A21	ANI0_IO4	ANI2_IO4	A12	NC
70 58	BI	ANI0_IO<5>	B18	ANI0_IO5	ANI2_IO5	B12	NC
70 58	BI	ANI0_IO<6>	A18	ANI0_IO6	ANI2_IO6	B15	NC
70 58	BI	ANI0_IO<7>	C18	ANI0_IO7	ANI2_IO7	A15	NC
70 58	OUT	ANI0_NCE<0>	E23	ANI0_NCE0	ANI2_NCE0	E16	NC
70 58	OUT	ANI0_NCE<1>	D22	ANI0_NCE1	ANI2_NCE1	D15	NC
70 58	OUT	ANI0_NCE<2>	E22	ANI0_NCE2	ANI2_NCE2	E15	NC
70 58	OUT	ANI0_NCE<3>	D21	ANI0_NCE3	ANI2_NCE3	D14	NC
		NC	E21	ANI0_NCE4	ANI2_NCE4	E14	NC
		NC	D20	ANI0_NCE5	ANI2_NCE5	D13	NC
		NC	E20	ANI0_NCE6	ANI2_NCE6	E13	NC
		NC	E19	ANI0_NCE7	ANI2_NCE7	D12	NC
70 58	BI	ANI0_NRE_N	B19	ANI0_NRE_N	ANI2_NRE_N	B13	NC
70 58	BI	ANI0_NRE_P	A19	ANI0_NRE_P	ANI2_NRE_P	A13	NC
70 58	OUT	ANI0_NWE	D23	ANI0_NWE	ANI2_NWE	D16	NC
		NC	D18	ANI0_PPM_IN	ANI2_PPM_IN	E11	NC
		NC	E18	ANI0_PPM_OUT	ANI2_PPM_OUT	F11	NC
70 58	OUT	ANI1_ALE	D25	ANI1_ALE	ANI3_ALE	D5	NC
70 58	OUT	ANI1_CLE	D26	ANI1_CLE	ANI3_CLE	E5	NC
70 58	BI	ANI1_DQS_N	E28	ANI1_DQS_N	ANI3_DQS_N	B6	NC
70 58	BI	ANI1_DQS_P	E29	ANI1_DQS_P	ANI3_DQS_P	A6	NC
70 58	BI	ANI1_IO<0>	G28	ANI1_IO0	ANI3_IO0	B4	NC
70 58	BI	ANI1_IO<1>	J29	ANI1_IO1	ANI3_IO1	A7	NC
70 58	BI	ANI1_IO<2>	G29	ANI1_IO2	ANI3_IO2	C4	NC
70 58	BI	ANI1_IO<3>	L29	ANI1_IO3	ANI3_IO3	B9	NC
70 58	BI	ANI1_IO<4>	J28	ANI1_IO4	ANI3_IO4	B8	NC
70 58	BI	ANI1_IO<5>	B26	ANI1_IO5	ANI3_IO5	A9	NC
70 58	BI	ANI1_IO<6>	C26	ANI1_IO6	ANI3_IO6	A4	NC
70 58	BI	ANI1_IO<7>	B25	ANI1_IO7	ANI3_IO7	A8	NC
70 58	OUT	ANI1_NCE<0>	J25	ANI1_NCE0	ANI3_NCE0	D9	NC
70 58	OUT	ANI1_NCE<1>	J26	ANI1_NCE1	ANI3_NCE1	E9	NC
70 58	OUT	ANI1_NCE<2>	H25	ANI1_NCE2	ANI3_NCE2	D8	NC
70 58	OUT	ANI1_NCE<3>	H26	ANI1_NCE3	ANI3_NCE3	E8	NC
		NC	G25	ANI1_NCE4	ANI3_NCE4	D7	NC
		NC	G26	ANI1_NCE5	ANI3_NCE5	E7	NC
		NC	F25	ANI1_NCE6	ANI3_NCE6	D6	NC
		NC	F26	ANI1_NCE7	ANI3_NCE7	E6	NC
70 58	BI	ANI1_NRE_N	D27	ANI1_NRE_N	ANI3_NRE_N	B5	NC
70 58	BI	ANI1_NRE_P	C27	ANI1_NRE_P	ANI3_NRE_P	A5	NC
70 58	OUT	ANI1_NWE	K25	ANI1_NWE	ANI3_NWE	F9	NC
		NC	E26	ANI1_PPM_IN	ANI3_PPM_IN	D4	NC
		NC	E25	ANI1_PPM_OUT	ANI3_PPM_OUT	E4	NC

0 2

1 3

OMIT_TABLE

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NC	AE12	ANI4_ALE	ANI6_ALE	AF25	ANI6_ALE	OUT	58 70
NC	AF11	ANI4_CLE	ANI6_CLE	AF26	ANI6_CLE	OUT	58 70
NC	AH14	ANI4_DQS_N	ANI6_DQS_N	AE28	ANI6_DQS_N	BI	58 70
NC	AJ14	ANI4_DQS_P	ANI6_DQS_P	AE29	ANI6_DQS_P	BI	58 70
NC	AJ11	ANI4_IO0	ANI6_IO0	W29	ANI6_IO<0>	BI	58 70
NC	AJ16	ANI4_IO1	ANI6_IO1	AC29	ANI6_IO<1>	BI	58 70
NC	AH11	ANI4_IO2	ANI6_IO2	AA28	ANI6_IO<2>	BI	58 70
NC	AH16	ANI4_IO3	ANI6_IO3	AG26	ANI6_IO<3>	BI	58 70
NC	AJ15	ANI4_IO4	ANI6_IO4	AH26	ANI6_IO<4>	BI	58 70
NC	AH15	ANI4_IO5	ANI6_IO5	AH25	ANI6_IO<5>	BI	58 70
NC	AJ12	ANI4_IO6	ANI6_IO6	AA29	ANI6_IO<6>	BI	58 70
NC	AH12	ANI4_IO7	ANI6_IO7	AC28	ANI6_IO<7>	BI	58 70
NC	AE16	ANI4_NCE0	ANI6_NCE0	AA25	ANI6_NCE<0>	OUT	58 70
NC	AF15	ANI4_NCE1	ANI6_NCE1	AA26	ANI6_NCE<1>	OUT	58 70
NC	AE15	ANI4_NCE2	ANI6_NCE2	AB25	ANI6_NCE<2>	OUT	58 70
NC	AF14	ANI4_NCE3	ANI6_NCE3	AB26	ANI6_NCE<3>	OUT	58 70
NC	AE14	ANI4_NCE4	ANI6_NCE4	AC25	NC		
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NC	AF12	ANI4_NCE7	ANI6_NCE7	AD26	NC		
NC	AH13	ANI4_NRE_N	ANI6_NRE_N	AF27	ANI6_NRE_N	BI	58 70
NC	AJ13	ANI4_NRE_P	ANI6_NRE_P	AG27	ANI6_NRE_P	BI	58 70
NC	AF16	ANI4_NWE	ANI6_NWE	W25	ANI6_NWE	OUT	58 70
NC	AE11	ANI4_PPM_IN	ANI6_PPM_IN	AE26	NC		
NC	AD11	ANI4_PPM_OUT	ANI6_PPM_OUT	AE25	NC		
NC	AF5	ANI5_ALE	ANI7_ALE	AD18	ANI7_ALE	OUT	58 70
NC	AE5	ANI5_CLE	ANI7_CLE	AF19	ANI7_CLE	OUT	58 70
NC	AH7	ANI5_DQS_N	ANI7_DQS_N	AH21	ANI7_DQS_N	BI	58 70
NC	AJ7	ANI5_DQS_P	ANI7_DQS_P	AJ21	ANI7_DQS_P	BI	58 70
NC	AH5	ANI5_IO0	ANI7_IO0	AJ23	ANI7_IO<0>	BI	58 70
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NC	AF8	ANI5_NCE2	ANI7_NCE2	AE22	ANI7_NCE<2>	OUT	58 70
NC	AE8	ANI5_NCE3	ANI7_NCE3	AF21	ANI7_NCE<3>	OUT	58 70
NC	AF7	ANI5_NCE4	ANI7_NCE4	AE21	NC		
NC	AE7	ANI5_NCE5	ANI7_NCE5	AF20	NC		
NC	AF6	ANI5_NCE6	ANI7_NCE6	AE20	NC		
NC	AE6	ANI5_NCE7	ANI7_NCE7	AE19	NC		
NC	AH6	ANI5_NRE_N	ANI7_NRE_N	AH20	ANI7_NRE_N	BI	58 70
NC	AJ6	ANI5_NRE_P	ANI7_NRE_P	AJ20	ANI7_NRE_P	BI	58 70
NC	AD9	ANI5_NWE	ANI7_NWE	AF23	ANI7_NWE	OUT	58 70
NC	AF4	ANI5_PPM_IN	ANI7_PPM_IN	AF18	NC		
NC	AE4	ANI5_PPM_OUT	ANI7_PPM_OUT	AE18	NC		

4 6

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PP1V8_S0SW_SSD_COLD
PP1V8_S0SW_SSD_HOT
PP1V2_S0SW_SSD_COLD
PP1V2_S0SW_SSD_HOT
DDR_PHY_ZQ
DDR_ZQ
PLACE_NEAR=U8400.V8:3.0MM
PLACE_NEAR=U8400.AA1:2.0MM
NOSTUFF
LPDDR2_CMD_VDDIO
LPDDR2_DATA_VDDIO
AVSS
VDD_DIG
PVDD_DIG
ANI_BOT_VDDIO
ANI_TOP_VDDIO
PP3V3_S0SW_S1X
PP1V1_S0SW_SSD
LPDDR2_CKE0
NO_TEST=TRUE
DDR_VREF_CMD
DDR_VREF_DATA
PLACE_NEAR=U8400.W2:5.0MM
PLACE_NEAR=U8400.R27:5.0MM
S1X_ANI_CALIB
UNUSED_ANI_VREF
ANI_VREF
PLACE_NEAR=U8400.AJ25:2.0MM
PLACE_NEAR=U8400.A25:2.0MM
PP1V8_S0SW_SSD_COLD
PP1V2_S0SW_SSD_COLD
PP1V8_S0SW_SSD_COLD
PP1V8_S0SW_SSD_COLD
PP1V2_S0SW_SSD_COLD
PP1V2_S0SW_SSD_COLD
PP1V8_S0SW_SSD_COLD
PLACE_NEAR=U8400.AA4:2.0MM
PLACE_NEAR=U8400.W2:5.0MM
PLACE_NEAR=U8400.W2:5.0MM
DDR_VREF_CMD
PLACE_NEAR=U8400.R27:5.0MM
DDR_VREF_DATA
ANI_VREF
SYNC MASTER=J92 SSD
SYNC DATE=02/11/2014
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SSD Controller (3 of 4)
Apple Inc.
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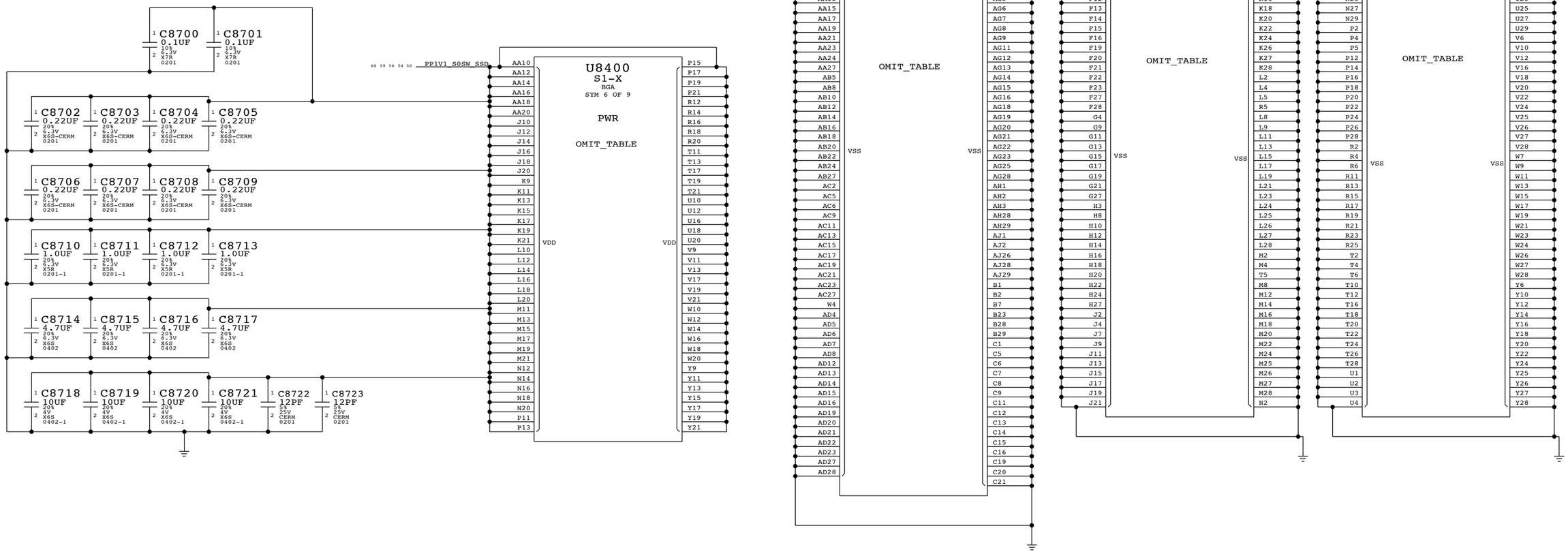

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Apple Inc.

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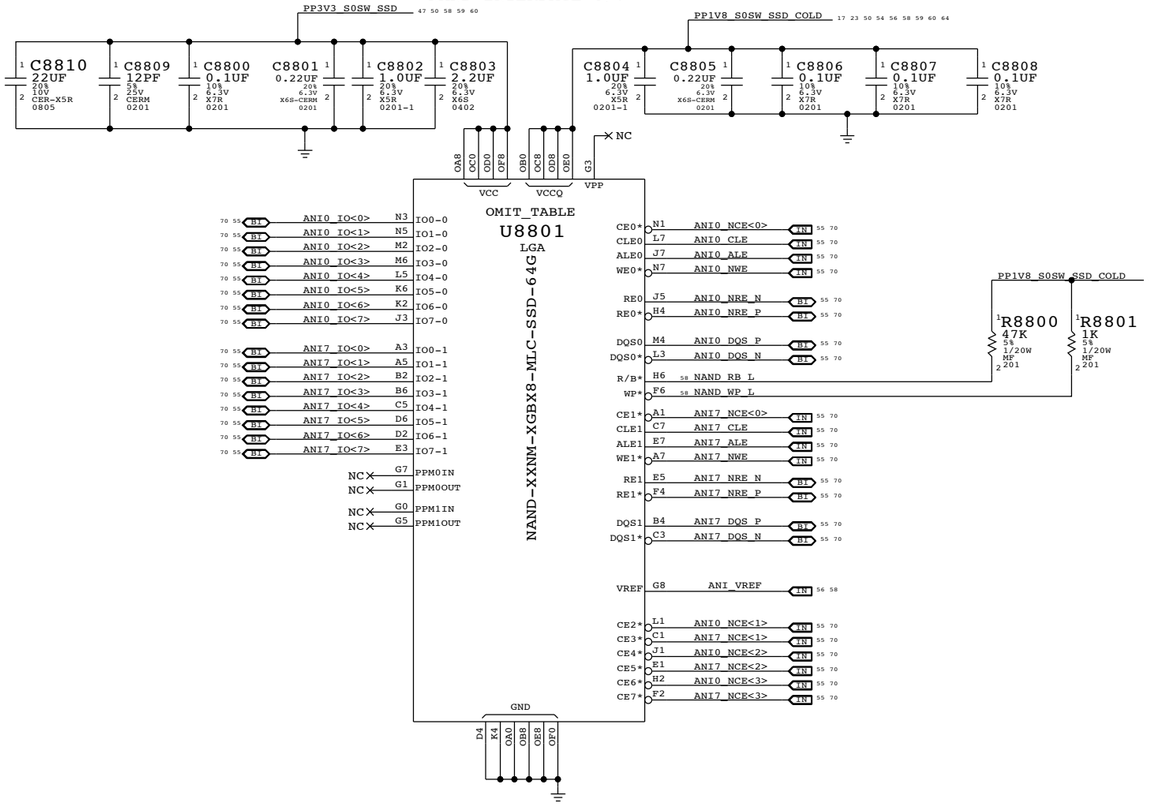
NAND INTERFACE 0/7



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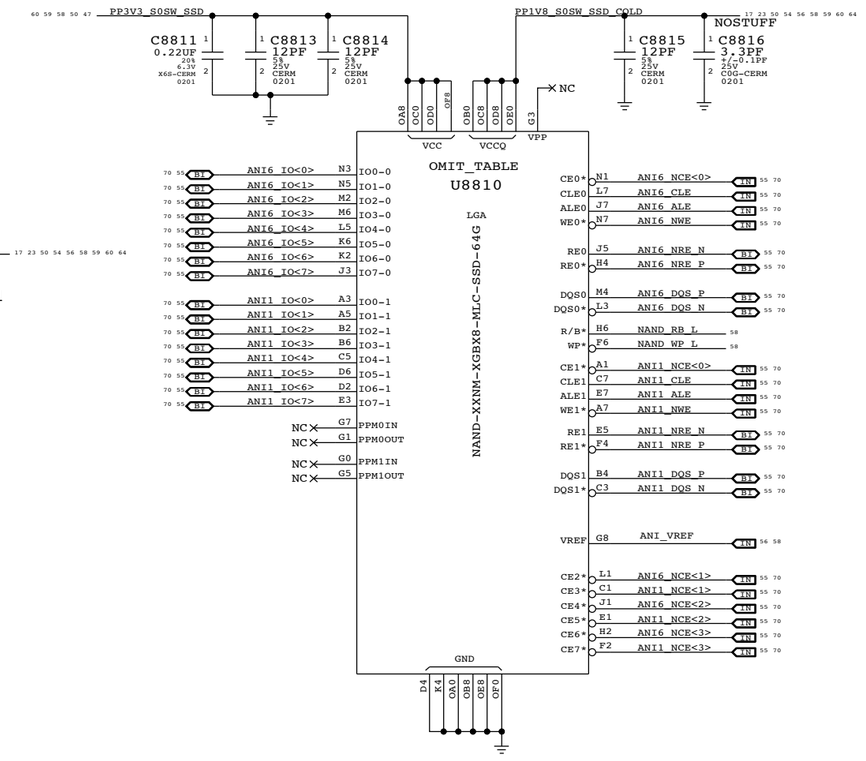

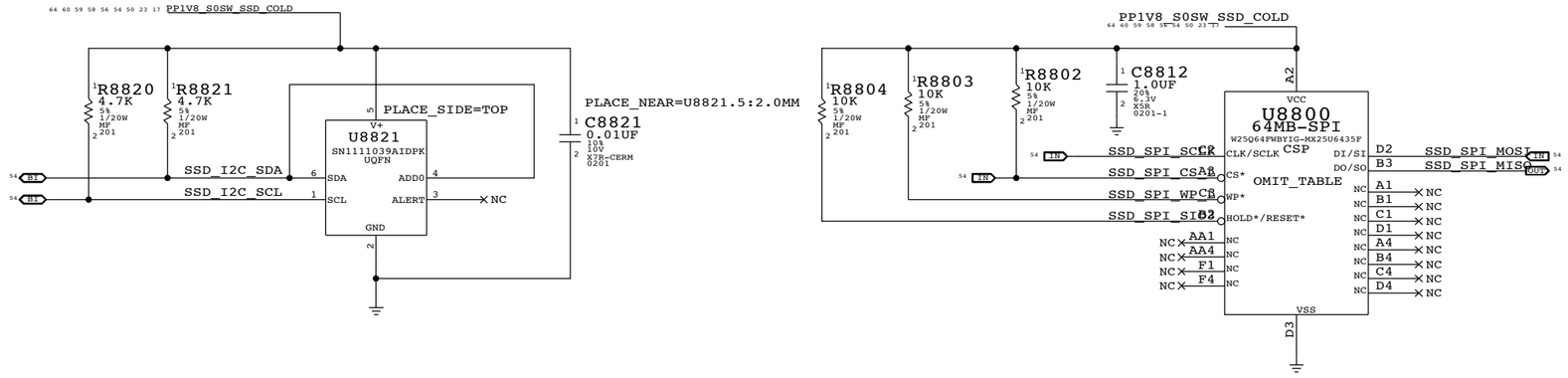

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Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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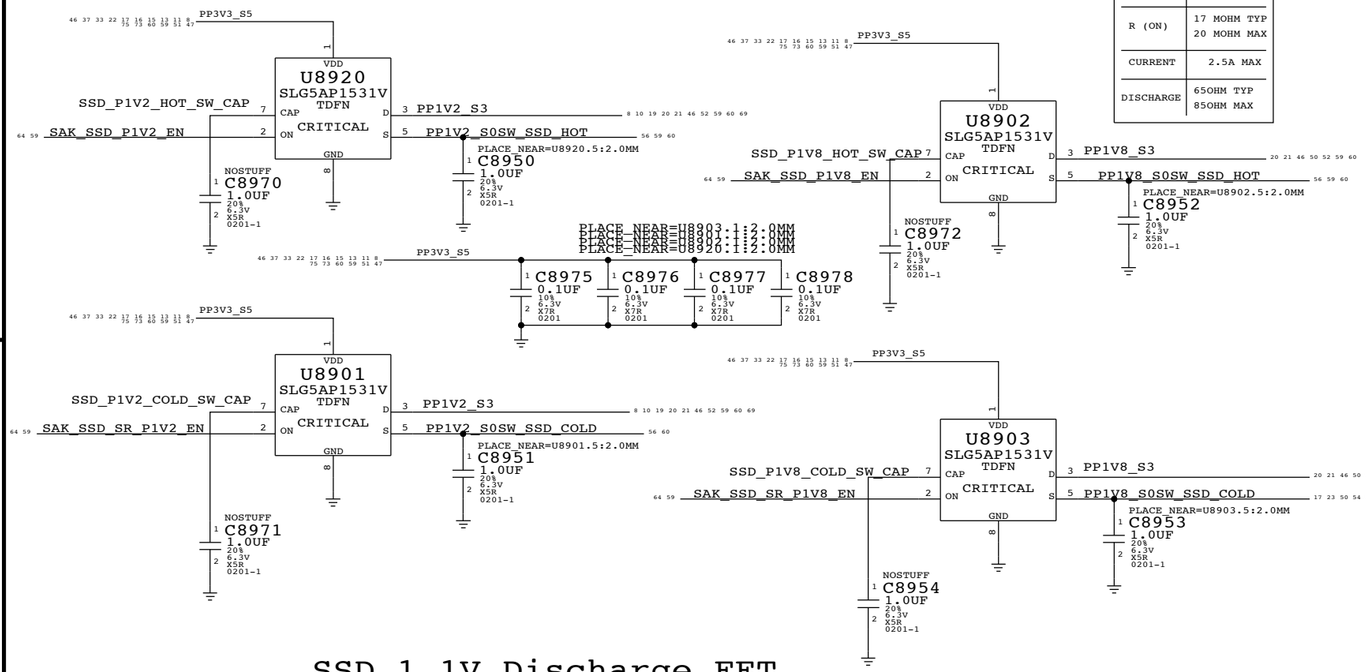
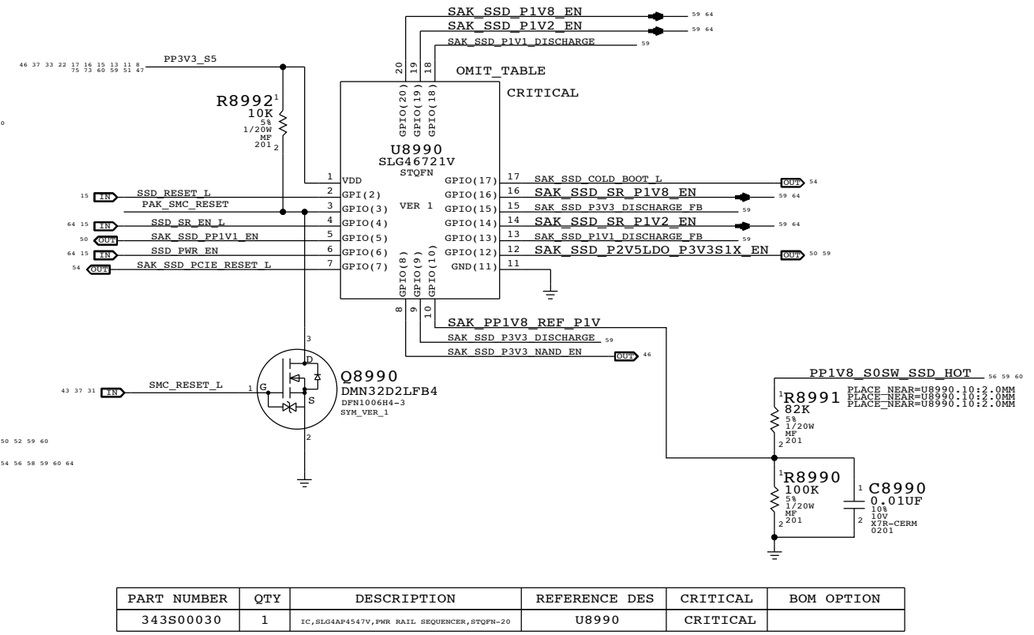
LPDDR2 1.2V & 1.8V LOAD SWITCHES FOR SEQUENCING, SR SUPPORT

PART	SLG5AP1531V
R (ON)	17 MOHM TYP 20 MOHM MAX
CURRENT	2.5A MAX
DISCHARGE	650HM TYP 850HM MAX

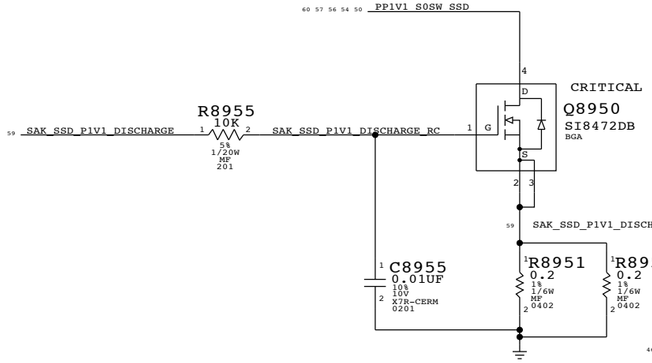


SILEGO GREEN PAK3 FOR POWER SEQUENCING, SR

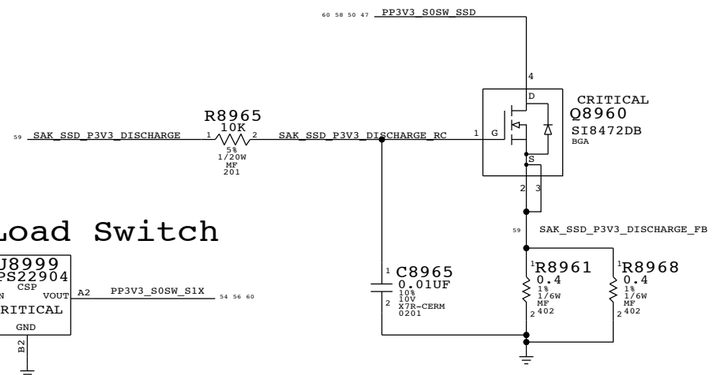


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00030	1	IC,SLG4AP4547V,PWR RAIL SEQUENCER,STQFN-20	U8990	CRITICAL	

SSD 1.1V Discharge FET

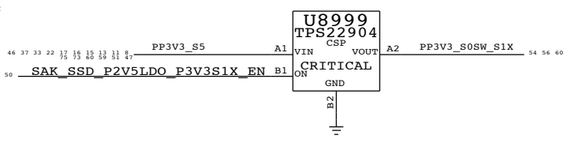


SSD 3.3V Discharge FET

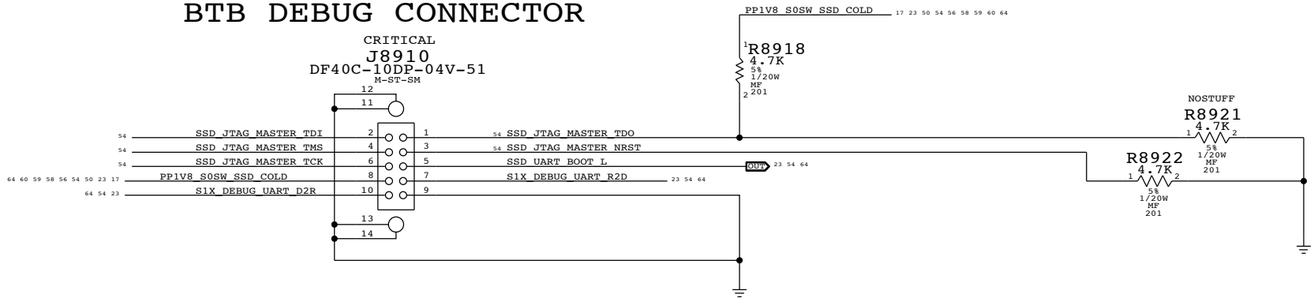


SSD 1.2V/1.8V HOT protection diode

S1X 3.3V Load Switch



BTB DEBUG CONNECTOR



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Apple Inc.

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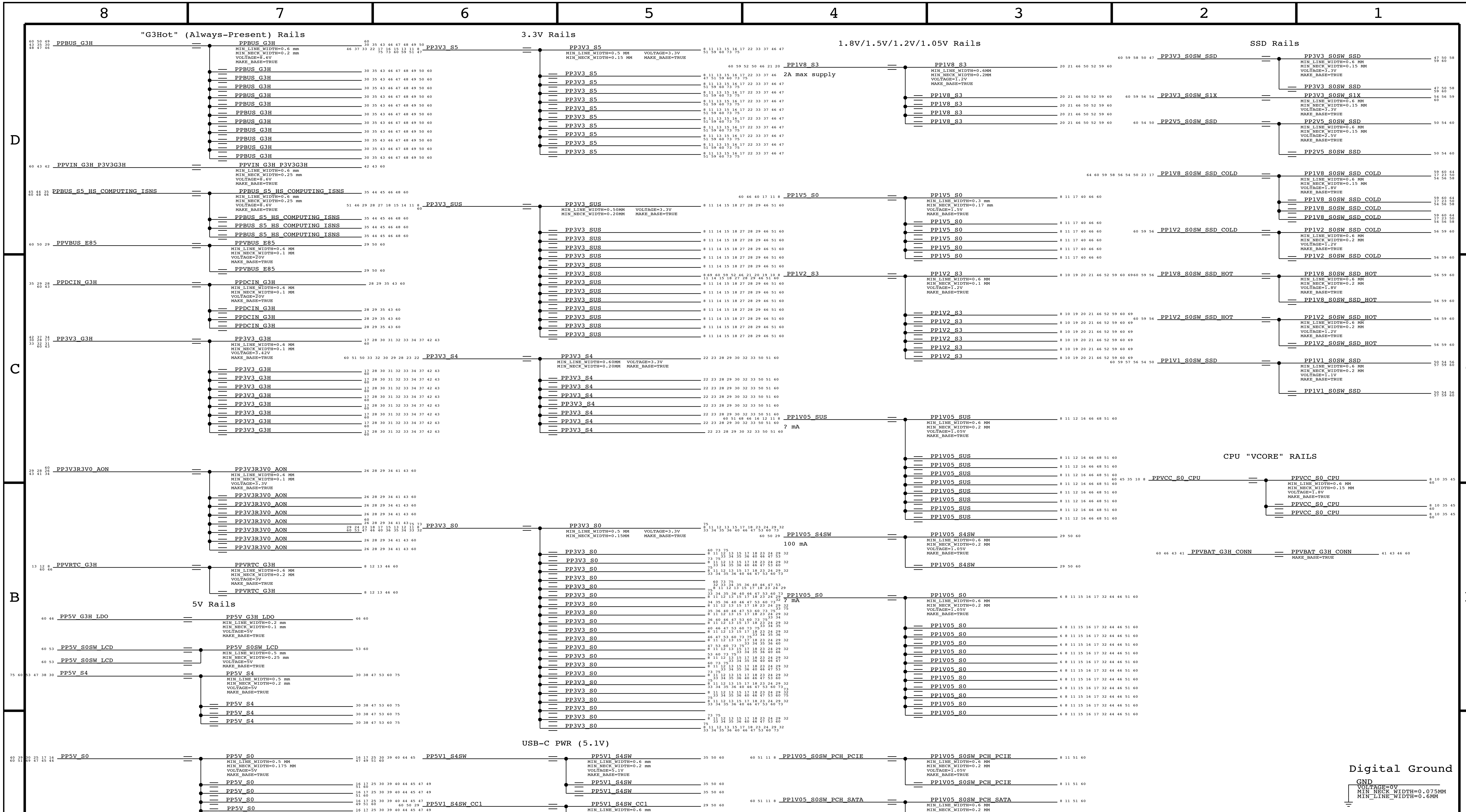

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PAGE TITLE

Power Aliases

Apple Inc.

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Memory Bit/Byte Swizzle

LPDDR3 Command/Address

MAKE_BASE

IN	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	OUT	20 69
IN	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	OUT	20 69
IN	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	OUT	20 69
IN	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	OUT	20 69
IN	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	OUT	20 69
IN	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	OUT	20 69
IN	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	OUT	7 20 61 69
IN	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	OUT	20 69
IN	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	OUT	20 69
IN	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	OUT	20 69
IN	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	OUT	20 69
IN	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	OUT	20 69
IN	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	OUT	20 69
IN	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	OUT	20 69
IN	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	OUT	20 69
IN	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	OUT	20 69
IN	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	OUT	7 20 61 69
IN	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	OUT	20 69
IN	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	OUT	20 69
IN	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	OUT	20 69
IN	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	OUT	7 20 61 69
IN	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1		7 61
IN	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2		7 61
IN	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	OUT	21 64 69
IN	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	OUT	21 69
IN	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	OUT	21 64 69
IN	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	OUT	21 64 69
IN	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	OUT	21 69
IN	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	OUT	21 69
IN	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	OUT	7 21 61 69
IN	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	OUT	21 69
IN	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	OUT	21 69
IN	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	OUT	21 69
IN	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	OUT	21 69
IN	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	OUT	21 64 69
IN	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	OUT	21 69
IN	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	OUT	21 69
IN	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	OUT	21 69
IN	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>	OUT	21 69
IN	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	OUT	7 21 61 69
IN	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	OUT	21 69
IN	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	OUT	21 69
IN	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	OUT	21 69
IN	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	OUT	7 21 61 69
IN	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3		7 61
IN	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4		7 61

MAKE_BASE

B3	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<34>	B1	7 69
B3	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<38>	B1	7 69
B3	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	B1	7 20 61 69
B3	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<36>	B1	7 69
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B3	=MEM_A_DQ<13>	TRUE	MEM_A_DQ<40>	B1	7 69
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B3	=MEM_A_DQ<15>	TRUE	MEM_A_DQ<41>	B1	7 69
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B3	=MEM_A_DQ<17>	TRUE	MEM_A_DQ<48>	B1	7 69
B3	=MEM_A_DQ<18>	TRUE	MEM_A_DQ<54>	B1	7 69
B3	=MEM_A_DQ<19>	TRUE	MEM_A_DQ<53>	B1	7 69
B3	=MEM_A_DQ<20>	TRUE	MEM_A_DQ<49>	B1	7 69
B3	=MEM_A_DQ<21>	TRUE	MEM_A_DQ<51>	B1	7 69
B3	=MEM_A_DQ<22>	TRUE	MEM_A_DQ<50>	B1	7 69
B3	=MEM_A_DQ<23>	TRUE	MEM_A_DQ<52>	B1	7 69
B3	=MEM_A_DQ<24>	TRUE	MEM_A_DQ<61>	B1	7 69
B3	=MEM_A_DQ<25>	TRUE	MEM_A_DQ<60>	B1	7 69
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B3	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<7>	B1	7 69
B3	=MEM_A_DQ<35>	TRUE	MEM_A_DQ<3>	B1	7 69
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B3	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<0>	B1	7 69
B3	=MEM_A_DQ<38>	TRUE	MEM_A_DQ<1>	B1	7 69
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B3	=MEM_A_DQ<50>	TRUE	MEM_A_DQ<19>	B1	7 69
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B3	=MEM_A_DQ<54>	TRUE	MEM_A_DQ<18>	B1	7 69
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B3	=MEM_A_DQ<57>	TRUE	MEM_A_DQ<29>	B1	7 69
B3	=MEM_A_DQ<58>	TRUE	MEM_A_DQ<26>	B1	7 69
B3	=MEM_A_DQ<59>	TRUE	MEM_A_DQ<28>	B1	7 69
B3	=MEM_A_DQ<60>	TRUE	MEM_A_DQ<25>	B1	7 69
B3	=MEM_A_DQ<61>	TRUE	MEM_A_DQ<31>	B1	7 69
B3	=MEM_A_DQ<62>	TRUE	MEM_A_DQ<30>	B1	7 69
B3	=MEM_A_DQ<63>	TRUE	MEM_A_DQ<27>	B1	7 69
B3	=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<4>	B1	7 69
B3	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<4>	B1	7 69
B3	=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<5>	B1	7 69
B3	=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<5>	B1	7 69
B3	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	B1	7 20 61 69
B3	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	B1	7 20 61 69
B3	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<7>	B1	7 69
B3	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<7>	B1	7 69
B3	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<0>	B1	7 69
B3	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<0>	B1	7 69
B3	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<1>	B1	7 69
B3	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<1>	B1	7 69
B3	=MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<2>	B1	7 69
B3	=MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<2>	B1	7 69
B3	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<3>	B1	7 69
B3	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<3>	B1	7 69

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B1	=MEM_B_DQ<0>	TRUE	MEM_B_DQ<35>	B1	7 69
B1	=MEM_B_DQ<1>	TRUE	MEM_B_DQ<38>	B1	7 69
B1	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>	B1	7 21 61 69
B1	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<36>	B1	7 69
B1	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<37>	B1	7 69
B1	=MEM_B_DQ<5>	TRUE	MEM_B_DQ<39>	B1	7 69
B1	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<34>	B1	7 69
B1	=MEM_B_DQ<7>	TRUE	MEM_B_DQ<33>	B1	7 69
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B1	=MEM_B_DQ<9>	TRUE	MEM_B_DQ<43>	B1	7 69
B1	=MEM_B_DQ<10>	TRUE	MEM_B_DQ<46>	B1	7 69
B1	=MEM_B_DQ<11>	TRUE	MEM_B_DQ<45>	B1	7 69
B1	=MEM_B_DQ<12>	TRUE	MEM_B_DQ<47>	B1	7 69
B1	=MEM_B_DQ<13>	TRUE	MEM_B_DQ<44>	B1	7 69
B1	=MEM_B_DQ<14>	TRUE	MEM_B_DQ<42>	B1	7 69
B1	=MEM_B_DQ<15>	TRUE	MEM_B_DQ<40>	B1	7 69
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B1	=MEM_B_DQ<20>	TRUE	MEM_B_DQ<51>	B1	7 69
B1	=MEM_B_DQ<21>	TRUE	MEM_B_DQ<52>	B1	7 69
B1	=MEM_B_DQ<22>	TRUE	MEM_B_DQ<54>	B1	7 69
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B1	=MEM_B_DQ<27>	TRUE	MEM_B_DQ<63>	B1	7 69
B1	=MEM_B_DQ<28>	TRUE	MEM_B_DQ<61>	B1	7 69
B1	=MEM_B_DQ<29>	TRUE	MEM_B_DQ<56>	B1	7 69
B1	=MEM_B_DQ<30>	TRUE	MEM_B_DQ<58>	B1	7 69
B1	=MEM_B_DQ<31>	TRUE	MEM_B_DQ<62>	B1	7 69
B1	=MEM_B_DQ<32>	TRUE	MEM_B_DQ<6>	B1	7 69
B1	=MEM_B_DQ<33>	TRUE	MEM_B_DQ<0>	B1	7 64 69
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B1	=MEM_B_DQ<35>	TRUE	MEM_B_DQ<5>	B1	7 69
B1	=MEM_B_DQ<36>	TRUE	MEM_B_DQ<7>	B1	7 69
B1	=MEM_B_DQ<37>	TRUE	MEM_B_DQ<1>	B1	7 69
B1	=MEM_B_DQ<38>	TRUE	MEM_B_DQ<4>	B1	7 69
B1	=MEM_B_DQ<39>	TRUE	MEM_B_DQ<2>	B1	7 69
B1	=MEM_B_DQ<40>	TRUE	MEM_B_DQ<8>	B1	7 69
B1	=MEM_B_DQ<41>	TRUE	MEM_B_DQ<11>	B1	7 69
B1	=MEM_B_DQ<42>	TRUE	MEM_B_DQ<9>	B1	7 69
B1	=MEM_B_DQ<43>	TRUE	MEM_B_DQ<12>	B1	7 69
B1	=MEM_B_DQ<44>	TRUE	MEM_B_DQ<15>	B1	7 69
B1	=MEM_B_DQ<45>	TRUE	MEM_B_DQ<14>	B1	7 69
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B1	=MEM_B_DQ<52>	TRUE	MEM_B_DQ<20>	B1	7 69
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B1	=MEM_B_DQ<54>	TRUE	MEM_B_DQ<22>	B1	7 69
B1	=MEM_B_DQ<55>	TRUE	MEM_B_DQ<21>	B1	7 69
B1	=MEM_B_DQ<56>	TRUE	MEM_B_DQ<29>	B1	7 69
B1	=MEM_B_DQ<57>	TRUE	MEM_B_DQ<25>	B1	7 69
B1	=MEM_B_DQ<58>	TRUE	MEM_B_DQ<24>	B1	7 69
B1	=MEM_B_DQ<59>	TRUE	MEM_B_DQ<26>	B1	7 69
B1	=MEM_B_DQ<60>	TRUE	MEM_B_DQ<27>	B1	7 69
B1	=MEM_B_DQ<61>	TRUE	MEM_B_DQ<28>	B1	7 69
B1	=MEM_B_DQ<62>	TRUE	MEM_B_DQ<30>	B1	7 69
B1	=MEM_B_DQ<63>	TRUE	MEM_B_DQ<31>	B1	7 69
B1	=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<4>	B1	7 69
B1	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<4>	B1	7 69
B1	=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<5>	B1	7 69
B1	=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<5>	B1	7 69
B1	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	B1	7 21 61 69
B1	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	B1	7 21 61 69
B1	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<7>	B1	7 69
B1	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<7>	B1	7 69
B1	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<0>	B1	7 64 69
B1	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<0>	B1	7 64 69
B1	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<1>	B1	7 69
B1	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<1>	B1	7 69
B1	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<2>	B1	7 69
B1	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<2>	B1	7 69
B1	=MEM_B_DQS_P<7>	TRUE	MEM_B_DQS_P<3>	B1	7 69
B1	=MEM_B_DQS_N<7>	TRUE	MEM_B_DQS_N<3>	B1	7 69

61 6 TP_CPU_MEMVTT_PWR_EN_LSVDDQ — TRUE — TP_CPU_MEMVTT_PWR_EN_LSVDDQ 6 61

MAKE_BASE=TRUE

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE: Memory Signal Swaps

Apple Inc.

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	MAKE_BASE							
64 62 28 15	OR_SWITCH_EN	=	TRUE	OR_SWITCH_EN	15 28 62 64			
62 44 8	CPU_VR_READY	=	TRUE	CPU_VR_READY	8 44 62			
62 31 13	SMC_PCH_SUSWARN_L	=	TRUE	SMC_PCH_SUSWARN_L	13 31 62			
62 31 13	SMC_PCH_SUSACK_L	=	TRUE	SMC_PCH_SUSACK_L	13 31 62			
62 43 35 32 31	SMC_BC_ACOK	=	TRUE	SMC_BC_ACOK	31 32 35 43 62			
62 5	TP_ULX_SPARE1	=	TRUE	TP_ULX_SPARE1	5 62			
62 5	TP_ULX_SSP_SPARE	=	TRUE	TP_ULX_SSP_SPARE	5 62			
68 62 12	TP_LPC_CLK24M_LPCPLUS_R	=	TRUE	TP_LPC_CLK24M_LPCPLUS_R	12 62 68			
64 62 28 13	HPM_I2C_INT_L	=	TRUE	HPM_I2C_INT_L	13 28 62 64			
64 62 28 13	HPM_I2C_INT_L	=						
63 62 28 16 14 64	XDP_USB_EXTA_OC_L	=	TRUE	XDP_USB_EXTA_OC_L	14 16 28 62 63 64			
62 37 32 31 26	SMC_TCK	=	TRUE	SMC_TCK	26 31 32 37 62			
62 37 32 31 26	SMC_TMS	=	TRUE	SMC_TMS	26 31 32 37 62			
62 28	TP_HPM_XTALOUT	=	TRUE	TP_HPM_XTALOUT	28 62			
	GND	=	TRUE	GND				
68 64 62 29 12	PCIE_CLK100M_TBT_P	=	TRUE	PCIE_CLK100M_TBT_P	12 29 62 64 68			
68 64 62 29 12	PCIE_CLK100M_TBT_N	=	TRUE	PCIE_CLK100M_TBT_N	12 29 62 64 68			
29	=PCIE_E85_D2R_P	=	TRUE	PCIE_TBT_D2R_P<0>	14 68			
29	=PCIE_E85_D2R_N	=	TRUE	PCIE_TBT_D2R_N<0>	14 68			
29	=PCIE_E85_R2D_P	=	TRUE	PCIE_TBT_R2D_C_P<0>	14 68			
29	=PCIE_E85_R2D_N	=	TRUE	PCIE_TBT_R2D_C_N<0>	14 68			
62 29 12	TBT_CLKREQ_L	=	TRUE	TBT_CLKREQ_L	12 29 62			
62 29 15	PCH_TBT_PCIE_RESET_L	=	TRUE	PCH_TBT_PCIE_RESET_L	15 29 62			
64 62 29 28	E85_TEST_MODE_L	=	TRUE	E85_TEST_MODE_L	28 29 62 64			

64 62 50 29 28 27 IN E85HSMUX_USB_EN = E85HSMUX_USB_EN OUT 27 28 29 50 62 64

MAKE_BASE=TRUE

SYNC MASTER=J92_DEVMLB SYNC DATE=07/08/2014

PAGE TITLE
J92 Signal Aliases

Apple Inc.

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NO_TEST Nets

		NO_TEST MAKE_BASE				
63 12	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	12 63	
63 12	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	12 63	
63	NC_PCIE_TBT_D2RP<1>	TRUE	TRUE	NC_PCIE_TBT_D2RP<1>	63	
63	NC_PCIE_TBT_D2RN<1>	TRUE	TRUE	NC_PCIE_TBT_D2RN<1>	63	
63	NC_PCIE_TBT_R2D_CP<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CP<1>	63	
63	NC_PCIE_TBT_R2D_CN<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CN<1>	63	
63 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 63	
63 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 63	
63 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 63	
63 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 63	
63 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 63	
63 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 63	CPU/PCH
63 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 63	
63 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 63	
63 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 63	
	=DP_TBTSNK1_ML_C_P<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CP<3..0>	5	
	=DP_TBTSNK1_ML_C_N<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CN<3..0>	5	
63 13	NC_DP_TBTSNK1_DDC_CLK	TRUE	TRUE	NC_DP_TBTSNK1_DDC_CLK	13 63	
63 13	NC_DP_TBTSNK1_DDC_DATA	TRUE	TRUE	NC_DP_TBTSNK1_DDC_DATA	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CP	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CN	13 63	
63 13	NC_DP_TBTSNK1_HPD	TRUE	TRUE	NC_DP_TBTSNK1_HPD	13 63	
63 31	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	31 63	
63	NC_SMC_DEBUGPRT_EN_L	TRUE	TRUE	NC_SMC_DEBUGPRT_EN_L	63	
63 31	NC_SMC_SYS_KBDLED	TRUE	TRUE	NC_SMC_SYS_KBDLED	31 63	
63	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	63	
63 31	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	31 63	
63 31	NC_SMC_FAN_0_TACH	TRUE	TRUE	NC_SMC_FAN_0_TACH	31 63	
63 31	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	31 63	
63 31	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	31 63	
64 63 31	NC_SYS_ONEWIRE	TRUE	TRUE	NC_SYS_ONEWIRE	31 63 64	SMC

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
SD_PWR_EN	15
ENET_MEDIA_SENSE	15
BT_PWRRST_L	15
TPAD_USB_IF_EN	15
PCH_GPIO12	15
TBT_PWR_EN	15
TBT_CIO_PLUG_EVENT_L	15
JTAG_TBT_TMS_PCH	15
ODD_PWR_EN_L	13
HDMITBTMUX_FLAG	13
HDMITBTMUX_LATCH	13
CAM_SENSOR_WAKE_L	24
LCD_PSR_EN	15
XDP_USB_EXTA_OC_L	14 16 28 62 64
AUD_WAKE_L	15
MIKEY_SPI_CS_L	15
MIKEY_SPI_CLK	15
MIKEY_SPI_MISO	15
MIKEY_SPI_MOSI	15

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

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Func Test / No Test

Apple Inc.

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EE Chaz Probe Points

PPA501 P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE)
PPA502 PMIC2_READY
PPA503 P1V05SUS_DRVH
PPA504 SMC_CBC_ON
PPA505 SMC_CHGR_INT_L
PPA506 MEM_B_CAA<0>
PPA507 MEM_B_CLK_P<0>
PPA508 MEM_B_CLK_N<0>
PPA509 MEM_B_CS_L<0>
PPA510 MEM_B_DQ<0>
PPA511 MEM_B_DQS_P<0>
PPA512 MEM_B_DQS_N<0>
PPA513 AP_PCIE_DEV_WAKE
PPA514 AP_S0IX_WAKE_L
PPA515 AP_S0IX_WAKE_SEL
PPA516 E85HSMUX_USB_EN

PPA519 PCH_BT_UART_D2R
PPA520 BT_UART_CTS_L
PPA521 PCH_UART1_R2D
PPA522 PCIE_CAMERA_D2R_P
PPA523 PCIE_CLK100M_SSD_P
PPA524 PCIE_CLK100M_TBT_P

AGND_PMIC — AGND_PMIC (MAKE_BASE=TRUE)
TS_HIPWR_EN — TS_HIPWR_EN (MAKE_BASE=TRUE)
TS_POWER_GATE_EN — TS_POWER_GATE_EN (MAKE_BASE=TRUE)
SSD_PWR_EN — SSD_PWR_EN (MAKE_BASE=TRUE)
SSD_UART_BOOT_L — SSD_UART_BOOT_L (MAKE_BASE=TRUE)
S1X_DEBUG_UART_D2R — S1X_DEBUG_UART_D2R (MAKE_BASE=TRUE)
S1X_DEBUG_UART_R2D — S1X_DEBUG_UART_R2D (MAKE_BASE=TRUE)
PP1V8_S0SW_SSD_COLD — PP1V8_S0SW_SSD_COLD (MAKE_BASE=TRUE)
PCIE_CLK100M_SSD_P — PCIE_CLK100M_SSD_P (MAKE_BASE=TRUE)
PCIE_CLK100M_SSD_N — PCIE_CLK100M_SSD_N (MAKE_BASE=TRUE)
=PCIE_SSD_D2R_P<0..3> — PCIE_SSD_D2R_P<0..3> (MAKE_BASE=TRUE)
=PCIE_SSD_D2R_N<0..3> — PCIE_SSD_D2R_N<0..3> (MAKE_BASE=TRUE)
=PCIE_SSD_R2D_P<0..3> — PCIE_SSD_R2D_P<0..3> (MAKE_BASE=TRUE)
=PCIE_SSD_R2D_N<0..3> — PCIE_SSD_R2D_N<0..3> (MAKE_BASE=TRUE)
P1V1_S0_DLPN_PGOOD — P1V1_S0_DLPN_PGOOD (MAKE_BASE=TRUE)
SYSCLK_CLK24M_CAMERA — SYSCLK_CLK24M_CAMERA (MAKE_BASE=TRUE)
SYSCLK_CLK32K_PMIC — SYSCLK_CLK32K_PMIC (MAKE_BASE=TRUE)
TP_SMC_PWRFAIL_WARN_L — TP_SMC_PWRFAIL_WARN_L (MAKE_BASE=TRUE)

PPA525 E85_RFU<1>
PPA526 E85_RFU<2>
PPA527 E85_CC1
PPA528 E85_CC2
PPA529 AUD_PWR_EN
PPA530 BT_UART_RTS_L
PPA531 CAMERA_PWR_EN
PPA532 HPM_I2C_INT_L
PPA533 EDP_BKLT_PWM
PPA534 HDA_SDIN0
PPA535 I2C_PCH_1_SCL
PPA536 I2C_PCH_1_SDA
PPA537 LCD_IRQ_L
PPA538 MEM_CAM_A<8>
PPA539 MEM_CAM_CS_L

PPA545 PCH_BT_UART_CTS_L
PPA546 PCH_BT_UART_R2D
PPA547 PCH_UART1_D2R
PPA548 PCIE_CAMERA_D2R_N
PPA549 PCIE_CLK100M_SSD_N
PPA550 PCIE_CLK100M_TBT_N
PPA551 PCIE_SSD_D2R_N<0>
PPA552 PCIE_SSD_D2R_P<0>

PPA555 OR_SWITCH_EN
PPA556 SAK_SSD_P1V2_EN
PPA557 SAK_SSD_P1V8_EN
PPA558 SAK_SSD_SR_P1V2_EN
PPA559 SAK_SSD_SR_P1V8_EN
PPA560 SMC_BT_PWR_EN
PPA561 SMC_CLK32K_PMIC
PPA562 SMC_OOB1_R2D_L
PPA563 SMC_PROCHOT
PPA564 SMC_SENSOR_PWR_EN
PPA565 SMC_WAKE_SCI_L
PPA566 SMC_WIFI_PWR_EN
PPA567 AP_PCIE_WAKE_L
PPA568 SSD_BOOT
PPA569 SSD_SR_EN_L
PPA570 SYSCLK_CLK12M_SMC
PPA571 SYSCLK_CLK12M_SSD
PPA572 SYSCLK_CLK24M_CAMERA
PPA573 SYSCLK_CLK32K_PMIC
PPA574 BT_DEV_WAKE
PPA575 TPAD_SPI_CS_L
PPA576 TPAD_SPI_INT_L

PPA577 USB3_EXTA_D2R_N
PPA578 USB3_EXTA_D2R_P
PPA579 CPU_CATERR_L
PPA580 E85_TEST_MODE_L
PPA581 MEM_B_CS_L<1>
PPA582 MEM_B_CKE<1>
PPA583 MEM_B_CAB<1>
PPA584 MEM_B_CAA<2>
PPA585 MCP_RSVD_CK13 — MCP_RSVD_CK13 (MAKE_BASE=TRUE)
PPA586 MCP_DC_CV45 — MCP_DC_CV45 (MAKE_BASE=TRUE)
PPA587 MEM_B_CAA<3>
PPA588 E85_LS_P<1>
PPA589 E85_LS_N<1>
PPA590 E85_LS_P<2>
PPA591 E85_LS_N<2>
PPA592 XDP_PCH_UART_SSD_L_BT_H
PPA593 DP_E85SNK_HPD
PPA594 XDP_USB_EXTA_OC_L
PPA595 XDP_USB_EXTB_OC_L
PPA596 USB_EXTA_P
PPA597 USB_EXTA_N

PPA5A0 BBPD_IPU_EN
PPA5A1 BBPD_MISO_LS1V1
PPA5A2 BBPD_PD_EN
PPA5A3 BBPD_PD_SEL_CC2
PPA5A4 BBPD_RPD_EN
PPA5A5 BBPD_RX_L_TX_H
PPA5A6 BBPD_SPI_MOSI
PPA5A7 BBPD_VCONN1_EN
PPA5A8 BBPD_VCONN2_EN
PPA5A9 BBPD_VCONN_EN

TP_ULX_DDR_VCCDDQG — TRUE — TP_ULX_DDR_VCCDDQG
SMC_DEBUGPRT_TX_L — TRUE — SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L — TRUE — SMC_DEBUGPRT_RX_L

NO_TEST Nets

NO_TEST=MAKE_BASE

NC_USB3_EXTB_D2RP — TRUE TRUE — NC_USB3_EXTB_D2RP
NC_USB3_EXTB_D2RN — TRUE TRUE — NC_USB3_EXTB_D2RN
NC_USB3_EXTB_R2D_CP — TRUE TRUE — NC_USB3_EXTB_R2D_CP
NC_USB3_EXTB_R2D_CN — TRUE TRUE — NC_USB3_EXTB_R2D_CN
NC_USB_IRP — TRUE TRUE — NC_USB_IRP
NC_USB_IRN — TRUE TRUE — NC_USB_IRN
NC_USB_EXTBP — TRUE TRUE — NC_USB_EXTBP
NC_USB_EXTBN — TRUE TRUE — NC_USB_EXTBN
NC_USB_TPADP — TRUE TRUE — NC_USB_TPADP
NC_USB_TPADN — TRUE TRUE — NC_USB_TPADN
NC_PCIE_CLK100M_FWP — TRUE TRUE — NC_PCIE_CLK100M_FWP
NC_PCIE_CLK100M_FWN — TRUE TRUE — NC_PCIE_CLK100M_FWN

CPU/PCH

NC_SYS_ONEWIRE — TRUE TRUE — NC_SYS_ONEWIRE
NC_PMIC_CLK32K_XTALIN — TRUE TRUE — NC_PMIC_CLK32K_XTALIN
NC_SMC_GFX_OVERTEMP — TRUE TRUE — NC_SMC_GFX_OVERTEMP
NC_SMC_FAN_0_CTL — TRUE TRUE — NC_SMC_FAN_0_CTL
NC_SMC_FAN_4_CTL — TRUE TRUE — NC_SMC_FAN_4_CTL

Unused nets with offpage

(Nets with offpages not used on this project)

XDP_USB_EXTB_OC_L

SYNC_MASTER=J41_MLB SYNC_DATE=10/24/2012

PAGE TITLE: Project FCT/NC/Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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J92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL6,ISL8,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL4	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	Y	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.260 MM			
27P4_OHM_SE	ISL6,ISL8,ISL10	Y	0.134 MM	0.134 MM			
27P4_OHM_SE	ISL3,ISL4	Y	0.190 MM	0.190 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.144 MM	0.144 MM			
40_OHM_SE	ISL6	Y	0.070 MM	0.070 MM			
40_OHM_SE	ISL8	Y	0.073 MM	0.073 MM			
40_OHM_SE	ISL10	Y	0.071 MM	0.071 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.095 MM			
45_OHM_SE	ISL6	Y	0.057 MM	0.057 MM			
45_OHM_SE	ISL8	Y	0.058 MM	0.058 MM			
45_OHM_SE	ISL10	Y	0.057 MM	0.057 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
50_OHM_SE_RF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.147 MM	0.060 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL6	Y	0.082 MM	0.082 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL8	Y	0.085 MM	0.085 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL10	Y	0.081 MM	0.081 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
85_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL10	Y	0.057 MM	0.057 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Note: 80ohm copied from 85ohm (pending stack-up calcs)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
80_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL10	Y	0.056 MM	0.056 MM	=STANDARD	0.101 MM	0.101 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.057 MM	?
1x_DIELECTRIC	ISL2,ISL11	0.057 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.057 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.054 MM	?
1x_DIELECTRIC	ISL5,ISL8	0.058 MM	?
1x_DIELECTRIC	ISL6,ISL7	0.051 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE: PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 32
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_TTP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	6 16
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	6 16
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
CPU_CFG	CPU_45S	CPU_TTP	CPU_CFG<2..0>	6 16
CPU_CFG3	CPU_45S	CPU_TTP	CPU_CFG<3>	6 16
CPU_CFG	CPU_45S	CPU_TTP	CPU_CFG<19..4>	6 16
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 31 64
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 31 32 44
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	15 31 32
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	6 16
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	6 16
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	6 16
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	6 16
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPUPCH_TRST_L	6 12 16
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_TTP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 44
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 44
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 44
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 44
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 44
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	14 23
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	14 23
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	23 64
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	23 64
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	54
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	54
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	14 64
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	14 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 54 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 54 64

PCIe SSD

120R	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_P 26 29
120R	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_N 26 29
120R		DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P 13 29
120R		DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N 13 29
120R	DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>
120R	DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>
120R		DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>
120R		DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>
120R	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P
120R	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N
119R		DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P
119R		DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N
	DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0> 53
	DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0> 53
		DP_80D	DP_TX	DP_INT_ML_C_P<3..0> 5 53
		DP_80D	DP_TX	DP_INT_ML_C_N<3..0> 5 53
121R	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P
121R	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N
	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P 5 53
	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N 5 53
		DP_80D	DP_AUX	DP_INT_AUX_P 53
		DP_80D	DP_AUX	DP_INT_AUX_N 53

DP

Note: DisplayPort tables are on Page 113

SYNC_MASTER=J92 DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE: CPU Constraints

Apple Inc.

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

E85 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
E85_HS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
E85_LS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	*	=6x_DIELECTRIC	?
E85_LS	*	=4x_DIELECTRIC	?
E85_CC	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	TOP,BOTTOM	=10x_DIELECTRIC	?
E85_LS	TOP,BOTTOM	=6x_DIELECTRIC	?
E85_CC	TOP,BOTTOM	=6x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_45S	SPI	TPAD_SPI_MOSI	15 30
	SPI_45S	SPI	TPAD_SPI_MISO	15 30
	SPI_45S	SPI	TPAD_SPI_CLK	15 30
USB_BT	USB_80D	USB	USB_BT_P	14 22
USB_BT	USB_80D	USB	USB_BT_N	14 22
	USB_80D	USB	USB_BT_R_P	22
	USB_80D	USB	USB_BT_R_N	22
USB_BT	USB_80D	USB	USB_BT_CONN_P	
USB_BT	USB_80D	USB	USB_BT_CONN_N	
USB_TPAD	USB_80D	USB	NC_USB_TPADP	14 64
USB_TPAD	USB_80D	USB	NC_USB_TPADN	14 64
USB_HPM	USB_85D	USB	USB_HPM_P	28 29
USB_HPM	USB_85D	USB	USB_HPM_N	28 29
	USB_85D	USB	USB_HPM_R_P	26
	USB_85D	USB	USB_HPM_R_N	26
	USB_80D	USB	USB_EXTA_P	14 26 64
	USB_80D	USB	USB_EXTA_N	14 26 64
	USB_85D	USB	USB_EXTA_F_P	26
	USB_85D	USB	USB_EXTA_F_N	26
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 29 64
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 29 64
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_N	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	29
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	29
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 29
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 29
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_P	14 27
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_N	14 27
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_P	27 29
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_N	27 29
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_P	14 29
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_N	14 29
	UART_45S	UART	SMC_DEBUGPRT_TX_L	26 31 32 64
	UART_45S	UART	SMC_DEBUGPRT_RX_L	26 31 32 64
USB_EXTB	USB_80D	USB	NC_USB_EXTBP	14 64
USB_EXTB	USB_80D	USB	NC_USB_EXTBN	14 64
USB_EXTB	USB_80D	USB	USB2_EXTB_F_P	
USB_EXTB	USB_80D	USB	USB2_EXTB_F_N	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RP	14 64
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RN	14 64
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CP	14 64
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CN	14 64
USB_EXTC	USB_80D	USB	USB2_EXTC_P	
USB_EXTC	USB_80D	USB	USB2_EXTC_N	
USB_EXTC	USB_80D	USB	USB2_EXTC_F_P	
USB_EXTC	USB_80D	USB	USB2_EXTC_F_N	
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_P	
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_N	
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_P	
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_N	
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_P	
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_N	
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_P	
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_N	
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_P	
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_N	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

TP SPI

Internal USB

I/O Port Device USB

I/O Port Host USB

I/O Port DCI

USB EXTB nets (Left USB port)

USB EXTC nets (Left USB port)

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE

PCH Constraints 1

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 31
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 31
	LPC_45S	LPC	LPCPLUS_RESET_L	
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 31
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	TP_LPC_CLK24M_LPCPLUS_R	12 62
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 34
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 34
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 34
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 34
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 31 34 36 53 72
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 31 34 36 53 72
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 40
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 40
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 40 64
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 40
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 32
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 37
	SPI_45S	SPI	SPI_CLK	37
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 37
	SPI_45S	SPI	SPI_MOSI	37
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 37
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 37
	SPI_45S	SPI	SPI_CS0_L	37
	SPI_45S	SPI	SPI_SMC_CLK	31 37
	SPI_45S	SPI	SPI_SMC_MOSI	31 37
	SPI_45S	SPI	SPI_SMC_MISO	31 37
	SPI_45S	SPI	SPI_SMC_CS_L	31 37
	SPI_45S	SPI	SPI_MLB_CLK	37
	SPI_45S	SPI	SPI_MLB_MOSI	37
	SPI_45S	SPI	SPI_MLB_MISO	37
	SPI_45S	SPI	SPI_MLB_CS_L	37
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	22
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	22
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 22
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 22
N402	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_P	22
N403	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_N	22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 22
N399	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_P	22
N400	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_N	22
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 62
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 62
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 29 62 64
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 29 62 64
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	24 25
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	24 25
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 25
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 25 64
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 25 64
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	24 25
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	24 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	24 25
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	24 25
PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_P	
PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_N	
DP_TBT_ML	DP_80D	DP_TX	DP_ML_P<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_ML_N<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_P<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_N<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_P<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_N<3..0>	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_P	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_N	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_P	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_N	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_P	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_N	

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK24M_CAMERA	17 24 64
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	24
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

E85 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<0>	5 29
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<0>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<1>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<1>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<3..2>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<3..2>	5 29
	DP_85D	DP_TX	DP_E85SNK_ML_P<3..0>	27 29
	DP_85D	DP_TX	DP_E85SNK_ML_N<3..0>	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_N	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_N	27 29
E85_LS	E85_LS_85D	E85_LS	E85_LS_P<2..1>	26 29 64
E85_LS	E85_LS_85D	E85_LS	E85_LS_N<2..1>	26 29 64
	E85_LS_85D	E85_LS	E85_LS_MISSION_P	26
	E85_LS_85D	E85_LS	E85_LS_MISSION_N	26
		E85_CC	E85_CC1	29 60 64
		E85_CC	E85_CC2	29 60 64

Note: 80ohm constraints are actually 85ohm

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE

PCH Constraints 2

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_70D
MEM_40S	MEM_TERM	MEM_50S

Note: changed MEM_TERM physical rule to MEM_70D from MEM_73D temporarily

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CS0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>
MEM_A_CS1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>
MEM_A_ODT	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CS0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>
MEM_B_CS1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>
MEM_B_ODT	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_70D		MEM_B_DQS_N<7>
		MEM_PWR	PP1V2_S3
		MEM_PWR	PPVREF_S3_MEM_VREFCA
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A
		MEM_PWR	PPVREF_S3_MEM_VREFCA
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_B

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NAND BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
NAND_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
NAND_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NAND_DQS	*	0.100 MM	?
NAND_IO	*	0.100 MM	?
NAND_CMD	*	0.100 MM	?

NAND:

DQS_P/N MAX LENGTH 3"
IO<7..0> SIGNALS SHOULD MATCH +/- 50MIL FROM DQS_P/N
IO<7..0> AND ASSOCIATED DQS_P/N ROUTE ON SAME LAYER. NO MORE THAN 2 VIA TRANSITIONS.
NCE<7..0>,ALE,CLE SHOULD MATCH +/- 250MIL FROM NWE
DQS_P/N & NRE_P/N SHOULD MATCH +/- 100MIL FROM NWE

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ANI0_IO	NAND_45S	NAND_IO	ANI0_IO<7..0>
DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0_DQS_P
DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0_DQS_N
DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0_NRE_P
DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0_NRE_N
ANI0_NWE	NAND_45S	NAND_CMD	ANI0_NWE
ANI0_NCE	NAND_45S	NAND_CMD	ANI0_NCE<3..0>
ANI0_ALE	NAND_45S	NAND_CMD	ANI0_ALE
ANI0_CLE	NAND_45S	NAND_CMD	ANI0_CLE
ANI1_IO	NAND_45S	NAND_IO	ANI1_IO<7..0>
DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1_DQS_P
DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1_DQS_N
DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1_NRE_P
DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1_NRE_N
ANI1_NWE	NAND_45S	NAND_CMD	ANI1_NWE
ANI1_NCE	NAND_45S	NAND_CMD	ANI1_NCE<3..0>
ANI1_ALE	NAND_45S	NAND_CMD	ANI1_ALE
ANI1_CLE	NAND_45S	NAND_CMD	ANI1_CLE
ANI2_IO	NAND_45S	NAND_IO	ANI2_IO<7..0>
DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2_DQS_P
DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2_DQS_N
DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2_NRE_P
DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2_NRE_N
ANI2_NWE	NAND_45S	NAND_CMD	ANI2_NWE
ANI2_NCE	NAND_45S	NAND_CMD	ANI2_NCE<3..0>
ANI2_ALE	NAND_45S	NAND_CMD	ANI2_ALE
ANI2_CLE	NAND_45S	NAND_CMD	ANI2_CLE
ANI3_IO	NAND_45S	NAND_IO	ANI3_IO<7..0>
DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3_DQS_P
DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3_DQS_N
DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3_NRE_P
DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3_NRE_N
ANI3_NWE	NAND_45S	NAND_CMD	ANI3_NWE
ANI3_NCE	NAND_45S	NAND_CMD	ANI3_NCE<3..0>
ANI3_ALE	NAND_45S	NAND_CMD	ANI3_ALE
ANI3_CLE	NAND_45S	NAND_CMD	ANI3_CLE

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ANI4_IO	NAND_45S	NAND_IO	ANI4_IO<7..0>
DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4_DQS_P
DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4_DQS_N
DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4_NRE_P
DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4_NRE_N
ANI4_NWE	NAND_45S	NAND_CMD	ANI4_NWE
ANI4_NCE	NAND_45S	NAND_CMD	ANI4_NCE<3..0>
ANI4_ALE	NAND_45S	NAND_CMD	ANI4_ALE
ANI4_CLE	NAND_45S	NAND_CMD	ANI4_CLE
ANI5_IO	NAND_45S	NAND_IO	ANI5_IO<7..0>
DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5_DQS_P
DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5_DQS_N
DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5_NRE_P
DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5_NRE_N
ANI5_NWE	NAND_45S	NAND_CMD	ANI5_NWE
ANI5_NCE	NAND_45S	NAND_CMD	ANI5_NCE<3..0>
ANI5_ALE	NAND_45S	NAND_CMD	ANI5_ALE
ANI5_CLE	NAND_45S	NAND_CMD	ANI5_CLE
ANI6_IO	NAND_45S	NAND_IO	ANI6_IO<7..0>
DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6_DQS_P
DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6_DQS_N
DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6_NRE_P
DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6_NRE_N
ANI6_NWE	NAND_45S	NAND_CMD	ANI6_NWE
ANI6_NCE	NAND_45S	NAND_CMD	ANI6_NCE<3..0>
ANI6_ALE	NAND_45S	NAND_CMD	ANI6_ALE
ANI6_CLE	NAND_45S	NAND_CMD	ANI6_CLE
ANI7_IO	NAND_45S	NAND_IO	ANI7_IO<7..0>
DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7_DQS_P
DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7_DQS_N
DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7_NRE_P
DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7_NRE_N
ANI7_NWE	NAND_45S	NAND_CMD	ANI7_NWE
ANI7_NCE	NAND_45S	NAND_CMD	ANI7_NCE<3..0>
ANI7_ALE	NAND_45S	NAND_CMD	ANI7_ALE
ANI7_CLE	NAND_45S	NAND_CMD	ANI7_CLE

SYNC MASTER=MASTER SYNC DATE=11/16/2011

PAGE TITLE
NAND CONSTRAINTS

Apple Inc.

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	NET_TYPE			
	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 24 25
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 24 25
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 24 25
E10	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 24 25 64
E10		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 25
E10	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 24 25
E10	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 24 25
E10	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 24 25
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 24 25
E10	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 24 25
E10	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 24 25
E10	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 24 25
E10	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 24 25
E10	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 24 25 64
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 24 25
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 24 25
E12	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 24 25
E12	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 24 25
E12		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 25 53
E12		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 25 53
E13	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 24 25
E13	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 24 25
E13		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 25 53
E13		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 25 53
E14			S2_MEM_PWR	PP1V35_CAM 24 25
E14			S2_MEM_PWR	PP0V675_CAM_VREF 24 25
E14			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 25

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PAGE TITLE: Camera Constraints

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	0.1 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	31 34 53
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	31 34 53
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 31 34 36 53 68
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 31 34 36 53 68
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL	31 34 46 48
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA	31 34 46 48
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL_R	
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA_R	
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	30 31 34 40
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	30 31 34 40
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	31 34 41 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	31 34 41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_P	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_N	43
	1TO1_DIFFPAIR		CHGR_CSI_R_P	43
	1TO1_DIFFPAIR		CHGR_CSI_R_N	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_P	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_N	43
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P3MM	*	=1TO1_DIFFPAIR	0.300 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.400 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

RF Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RF_50S	*	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
RF	*	0.15 MM	?

J92 MLB Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P 35 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N 35 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N 35
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P 35
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P 36
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N 36
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_P 46
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_N 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P 49
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N 49
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_P 48
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_N 48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_P 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_N 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N 36
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_P 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_N 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_P 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_N 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_P 38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_N 38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_P 38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_N 38 40
		SB_POWER	PP3V3_S5 8 11 13 15 16 17 22 33 37 46 47 51 59 60 75
		SB_POWER	PP3V3_S0 8 11 12 13 15 17 18 23 24 29 32 33 34 35 36 40 46 47 53 60 75
		GND	GND
	RF_50S	RF	RF_A_0_DIPLEXER 22
	RF_50S	RF	RF_A_0_MATCH 22
	RF_50S	RF	RF_G_0_DIPLEXER 22
	RF_50S	RF	RF_G_0_MATCH 22
	RF_50S	RF	RF_0_ANT 22
	RF_50S	RF	RF_0_ANT_MATCH_T 22
	RF_50S	RF	RF_A_1_DIPLEXER 22
	RF_50S	RF	RF_A_1_MATCH 22
	RF_50S	RF	RF_G_1_DIPLEXER 22
	RF_50S	RF	RF_G_1_MATCH 22
	RF_50S	RF	RF_1_ANT 22
	RF_50S	RF	RF_1_ANT_MATCH_T 22
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_P<1..0>
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_N<1..0>
	DP_80D	DP_TX	DP_EXT_ML_C_P<1..0>
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USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_N
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_P
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Change List:
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Kismet:
<afp://kismet.apple.com/Kismet-Projects/J92/>

Useful Wiki Links:
Schematic Conventions - <https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions>
Schematic Design Wiki - <https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design>

MobileMac HW Radar:
<radar://component/497591> MobileMac HW | Task
<radar://component/497587> MobileMac HW | Schematic
<radar://component/497585> MobileMac HW | New Bugs
<radar://component/497588> MobileMac HW | Layout
<radar://component/497590> MobileMac HW | Investigation
<radar://component/497589> MobileMac HW | Architecture

Other Info:
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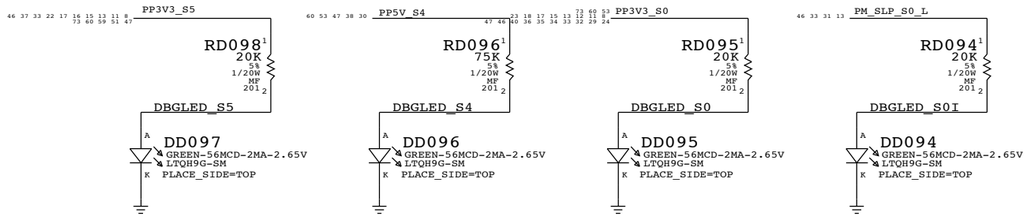
Power State Debug LEDs



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