

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X362 MLB SCHEMATIC

LAST_MODIFICATION= Tue Aug 30 11:06:16 2016


REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
9	0006939272	ENGINEERING RELEASED		2016-08-30

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00515	1	SCHEM,MLB,X362	SCH	CRITICAL	
820-00239	1	PCBF,MLB,X362	PCB	CRITICAL	

DRAWING TITLE		SCHEM,MLB,X362	
 Apple Inc.		DRAWING NUMBER	051-00515
		REVISION	9.0.0
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BOM Groups

Table with BOM GROUP and BOM OPTIONS columns. Rows include X362_COMMON, X362_COMMON1, X362_COMMON2, X362_COMMON3, X362_PROGPARTS, X362_DEVEL:ENG, X362_DEVEL:DVT, and X362_DEVEL:PVT.

Module Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists various CPU, memory, and interface components.

Programmables (All Builds)

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists EFI ROM, SMC ROM, TBT ROMs, and WIFI/BT ROM.

Variable BOM Groups Development/Base BOMs

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists development and base BOM options.

Main DRAM Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists various DRAM components.

Main DRAM SPD Straps

Table with columns: BOM GROUP and BOM OPTIONS. Lists SPD strap options for RAM.

NAND Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists various NAND flash components.

NAND Straps

Table with columns: BOM GROUP and BOM OPTIONS. Lists NAND strap options for SDISK and TSHBA.

Strategic Silicon

Table with columns: PART#, STRATEGIC VALUE, COMMENT. Lists strategic silicon components.

Table with columns: PART#, STRATEGIC VALUE, COMMENT. Lists strategic silicon components.

CPU DRAM CFG Chart

Table with columns: DIE REV, CFG 4, SPEED, CFG 3, CAPACITY, CFG 2. Shows configuration options for CPU and DRAM.

Table with columns: VENDOR, CFG 1, CFG 0. Shows vendor configuration options.

BOM Configuration header with Apple logo, drawing number (051-00515), revision (9.0.0), and page information (2 OF 145).

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00055	COMMON PARTS,MLB,X362	X362_COMMON
985-00070	DEV,MLB,X362	X362_DEVEL:DVT
639-01870	MLB, 2.9G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_256G
639-01871	MLB, 2.9G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_256G
639-01872	MLB, 2.9G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_256G
639-01873	MLB, 2.9G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_256G
639-01984	MLB, 2.9G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01985	MLB, 2.9G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01986	MLB, 2.9G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_512G
639-01987	MLB, 2.9G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_512G
639-02517	MLB, 2.9G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_1T
639-02518	MLB, 2.9G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_1T
639-02519	MLB, 2.9G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_1T
639-02520	MLB, 2.9G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_1T
639-01874	MLB, 3.1G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_256G
639-01875	MLB, 3.1G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_256G
639-01876	MLB, 3.1G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_256G
639-01877	MLB, 3.1G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_256G
639-01883	MLB, 3.1G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01884	MLB, 3.1G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01885	MLB, 3.1G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_512G
639-01886	MLB, 3.1G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_512G
639-01887	MLB, 3.1G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_1T
639-01888	MLB, 3.1G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_1T
639-01889	MLB, 3.1G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_1T
639-01890	MLB, 3.1G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_1T
639-02221	MLB, 3.3G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_256G
639-02222	MLB, 3.3G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_256G
639-02223	MLB, 3.3G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_256G
639-02224	MLB, 3.3G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_256G
639-01891	MLB, 3.3G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01892	MLB, 3.3G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01893	MLB, 3.3G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_512G
639-01894	MLB, 3.3G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_512G
639-01895	MLB, 3.3G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_1T
639-01896	MLB, 3.3G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_1T
639-01897	MLB, 3.3G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_1T
639-01898	MLB, 3.3G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_1T

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01988	MLB,NO CPU,X362	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,SAND_512G
639-01989	MLB,CPU SOCKET,X362	BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_16G_SAMSUNG_2133,SAND_512G
639-02521	MLB, 2.9G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02522	MLB, 2.9G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02523	MLB, 2.9G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_256G
639-02524	MLB, 2.9G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_256G
639-02525	MLB, 2.9G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02526	MLB, 2.9G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02527	MLB, 2.9G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_512G
639-02528	MLB, 2.9G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_512G
639-02529	MLB, 2.9G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02530	MLB, 2.9G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02531	MLB, 2.9G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_1T
639-02532	MLB, 2.9G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_1T
639-02533	MLB, 3.1G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02534	MLB, 3.1G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02535	MLB, 3.1G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_256G
639-02536	MLB, 3.1G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_256G
639-02537	MLB, 3.1G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02538	MLB, 3.1G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02539	MLB, 3.1G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_512G
639-02540	MLB, 3.1G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_512G
639-02541	MLB, 3.1G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02542	MLB, 3.1G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02543	MLB, 3.1G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_1T
639-02544	MLB, 3.1G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_1T
639-02545	MLB, 3.3G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02546	MLB, 3.3G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02547	MLB, 3.3G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_256G
639-02548	MLB, 3.3G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_256G
639-02549	MLB, 3.3G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02550	MLB, 3.3G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02551	MLB, 3.3G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_512G
639-02552	MLB, 3.3G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_512G
639-02553	MLB, 3.3G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02554	MLB, 3.3G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02555	MLB, 3.3G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_1T
639-02556	MLB, 3.3G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_1T

Alternate Parts

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152S00368	152S00269		ALL	Text note to be updated
152S00370	152S00270		ALL	Text note to be updated
353S4068	353S4070		ALL	Text note to be updated
353S00772	353S4070		ALL	Text note to be updated
138S00086	138S0884		ALL	Text note to be updated
107S0248	107S0250		ALL	TFT alt to Cyntec
152S00434	152S1829		ALL	Text note to be updated
371S00019	371S0463		ALL	Rohm alt to Rohm
353S00107	353S3239	ANY	ALL	Onsemi alt to Intersil
353S00231	353S3987		ALL	NXP alt to TI
333S00025	333S00055	POP_4GBIT	ALL	MICRON SSD POP ALT for HYNIX
333S00026	333S00056	POP_8GBIT	ALL	MICRON SSD POP ALT for HYNIX
333S00107	333S00055	POP_4GBIT	ALL	HYNIX SSD POP REPLACEMENT for HYNIX
333S00108	333S00056	POP_8GBIT	ALL	HYNIX SSD POP REPLACEMENT for HYNIX

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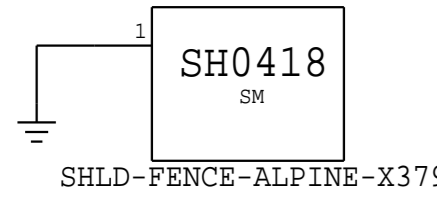
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SHEET		3 OF 119			

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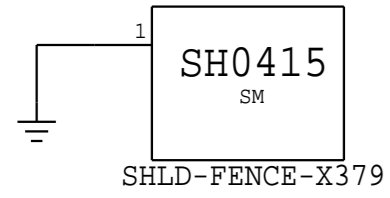
BOARD MECHANICALS

Shield Cans - BOTTOM SIDE

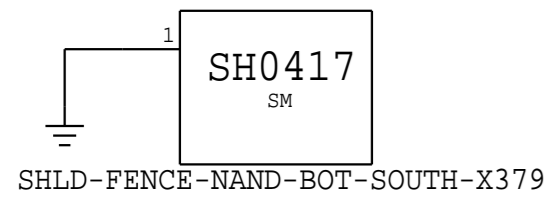
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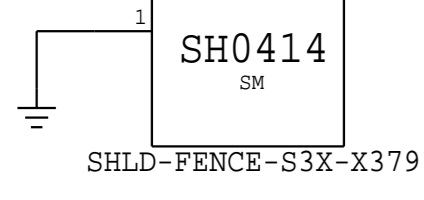
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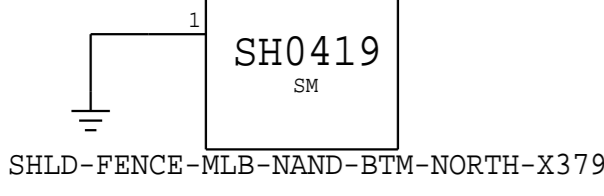
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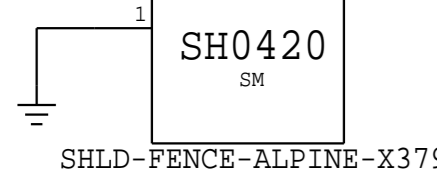
S3X (U8600) - 806-06023



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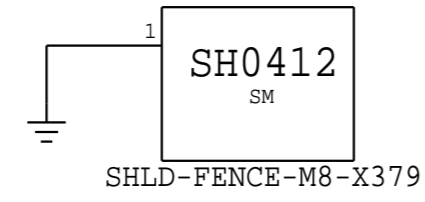


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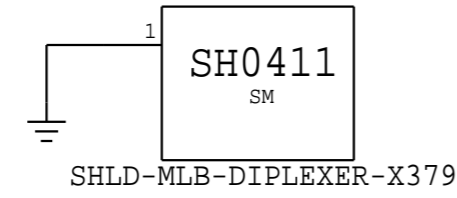


Shield Cans - TOP SIDE

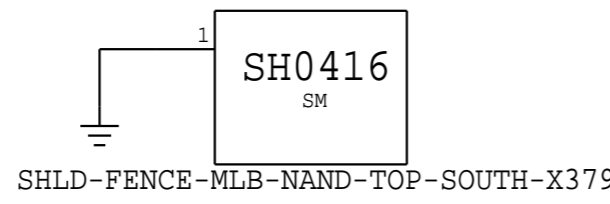
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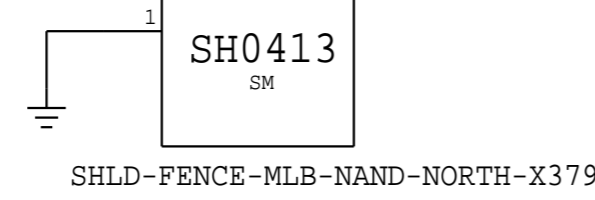
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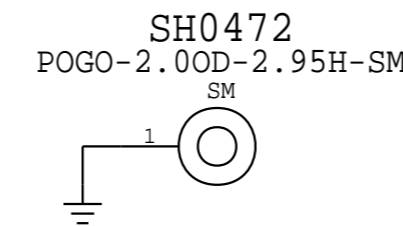
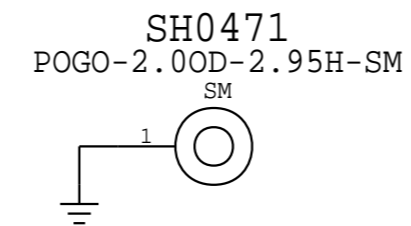


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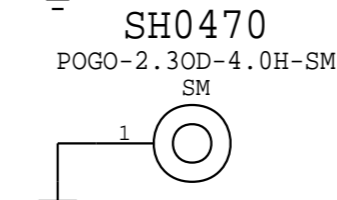
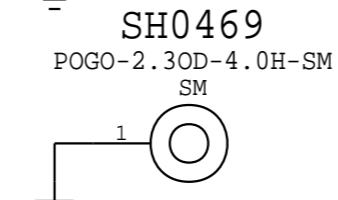
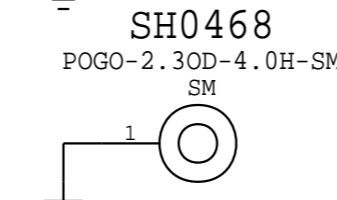
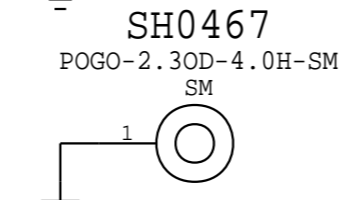
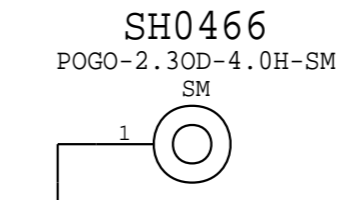
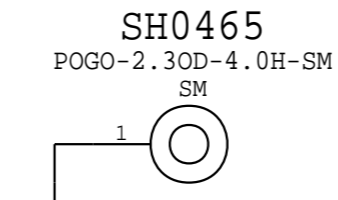
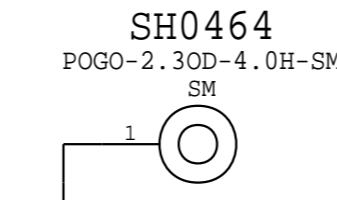
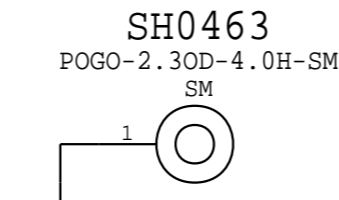


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LIO and RIO -2X (870-5071)

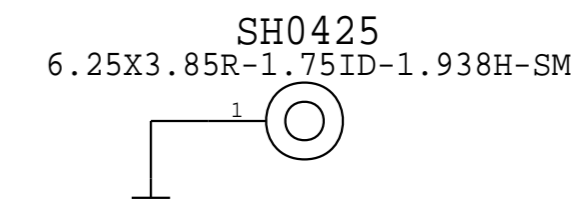


AROUND THE FAN AND CENTER - 8X (870-01518)

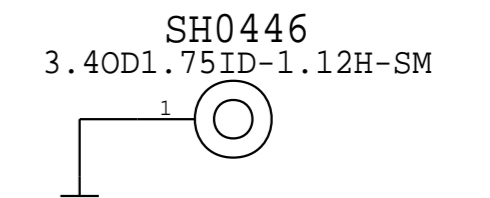
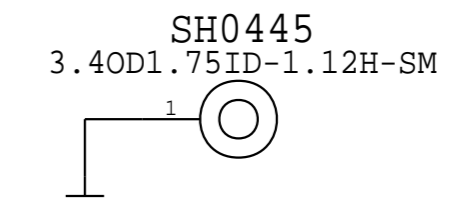


Cowling Bosses - BOTTOM SIDE

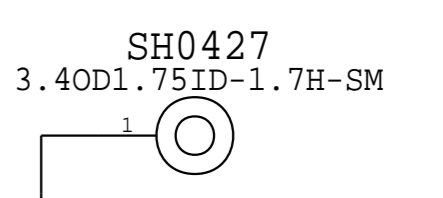
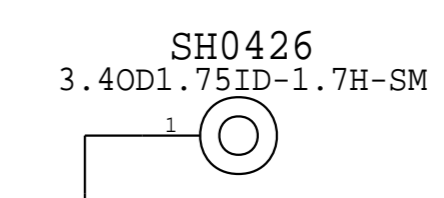
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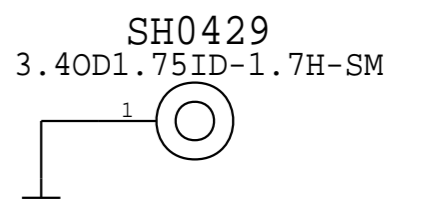
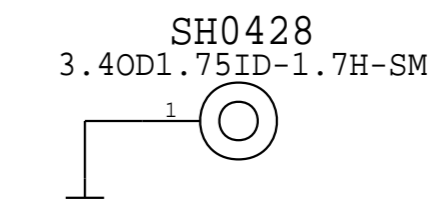
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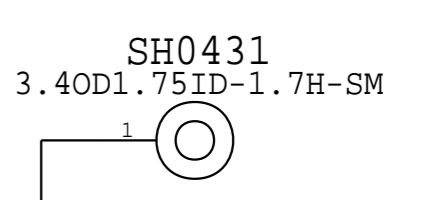
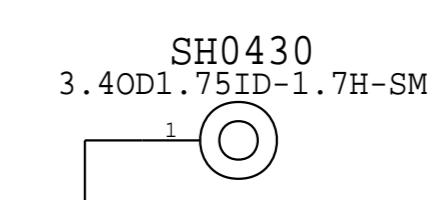
DFR DISPLAY CONN (J4401) - 860-00412



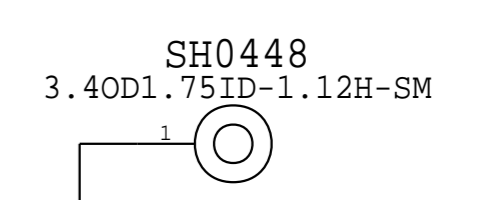
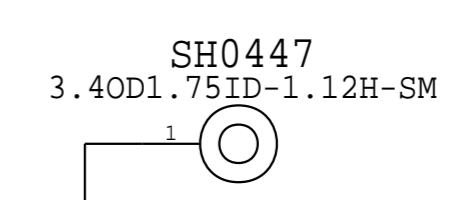
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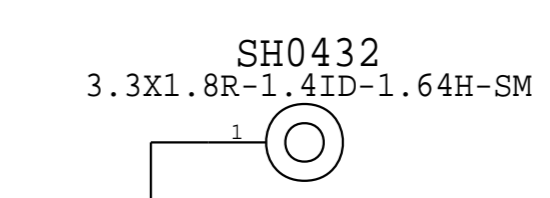
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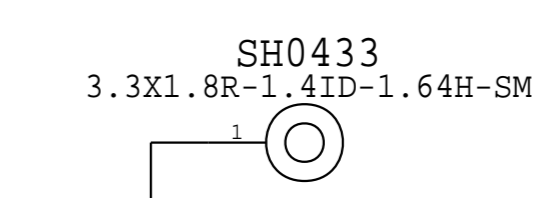
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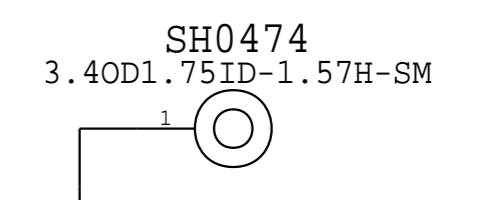
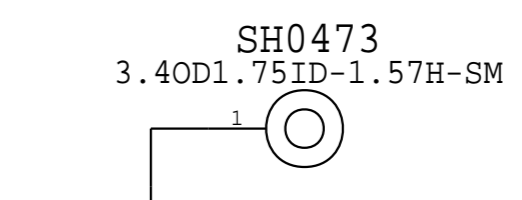
AUDIO JACK CONN (J6600) - 860-00399



MESA CONN (J4900) - 860-00399

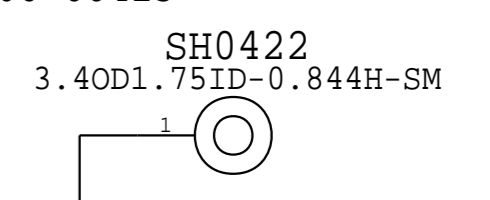
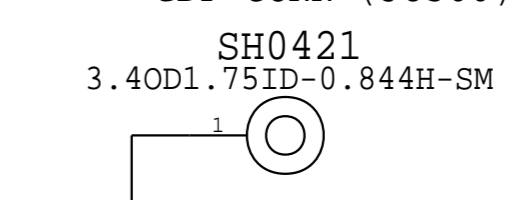


LIFEBOAT CONN (J9600) - 860-00413

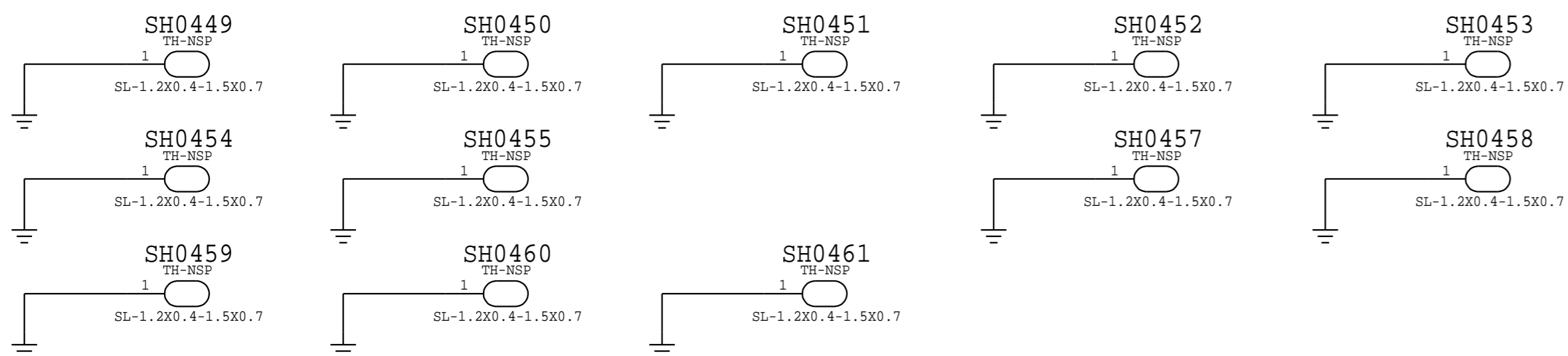


Cowling Bosses - TOP SIDE

eDP CONN (J8500) - 860-00415

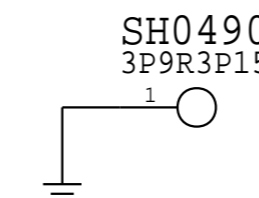


Shield CAN Alignment Slots 14X - 998-04440 (1.2mm X 0.4mm)

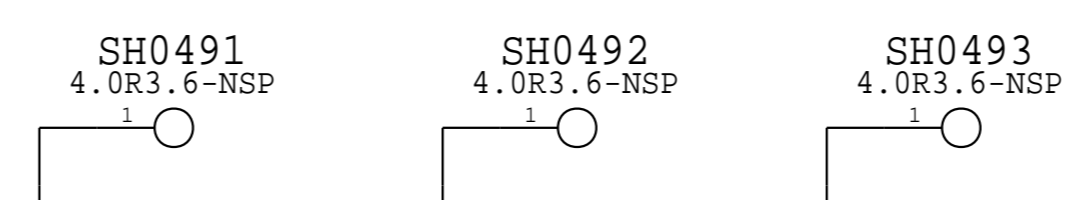


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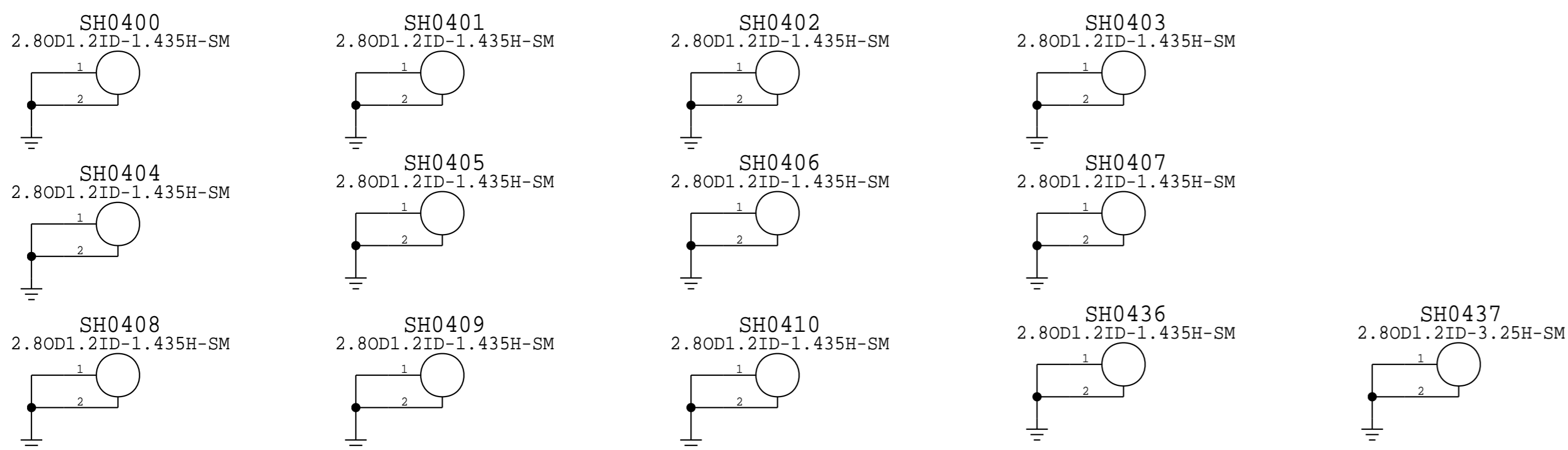
Plated Through Hole - 3.15mm - APN 998-0845



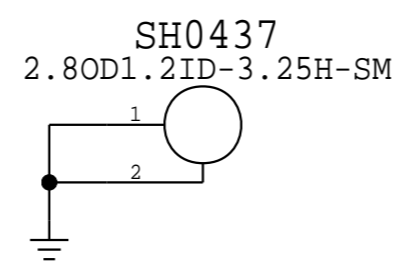
Plated Through Hole - 3.6mm - APN 998-03850



TOP Rubber Mount Standoffs - 12X - (860-00430)



Bottom Rubber Mount Standoffs - 1X - (860-00476)



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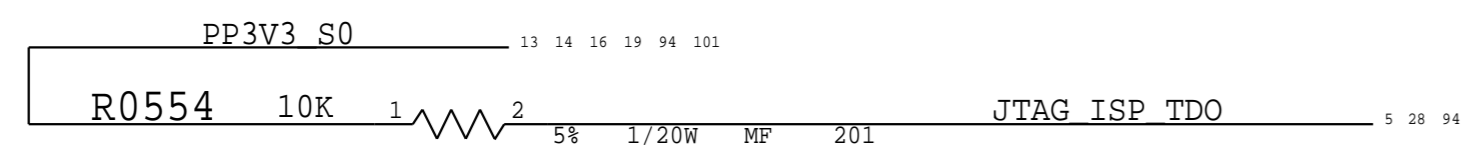
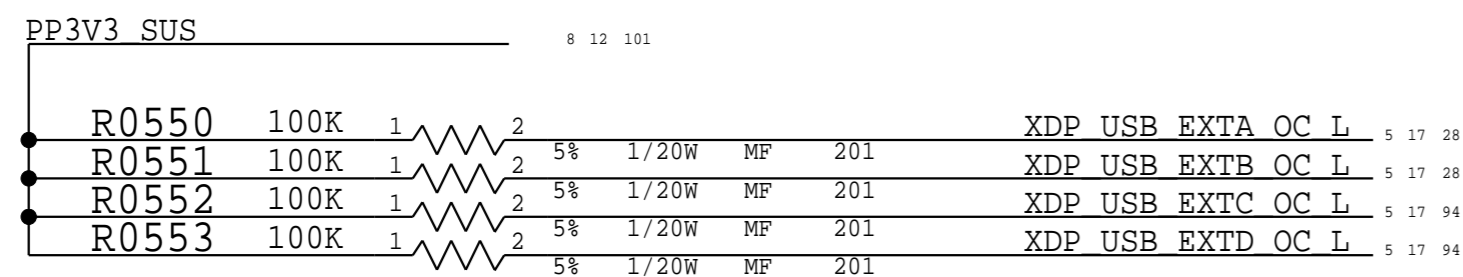
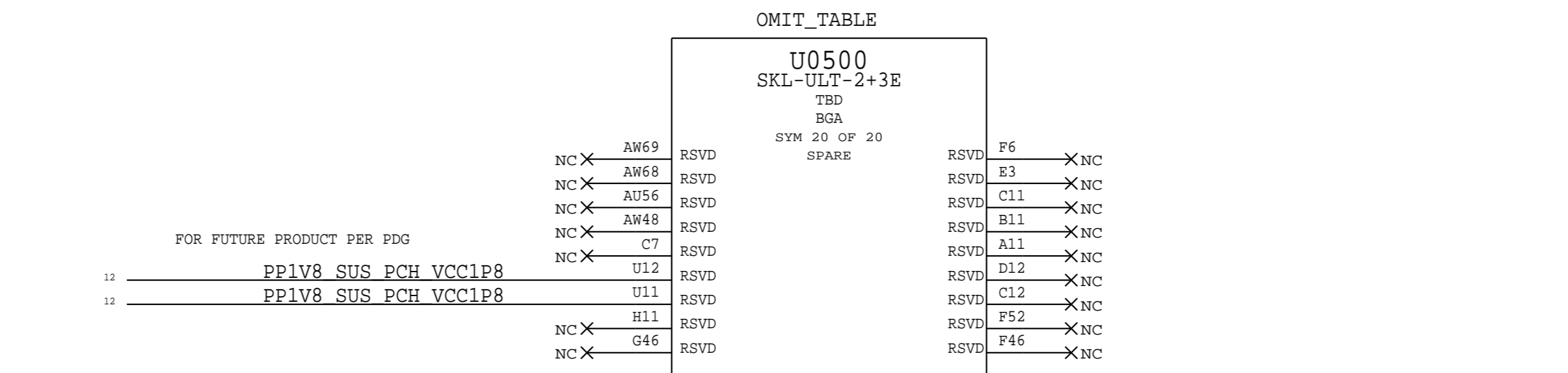
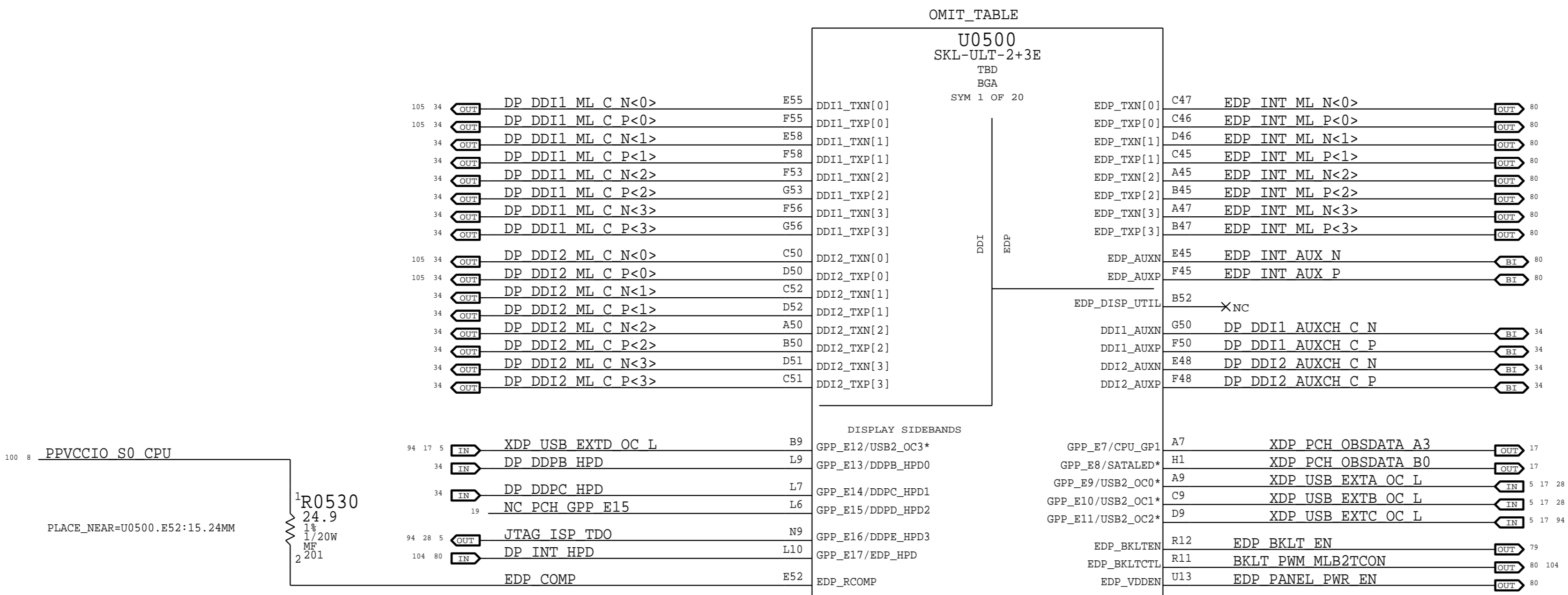
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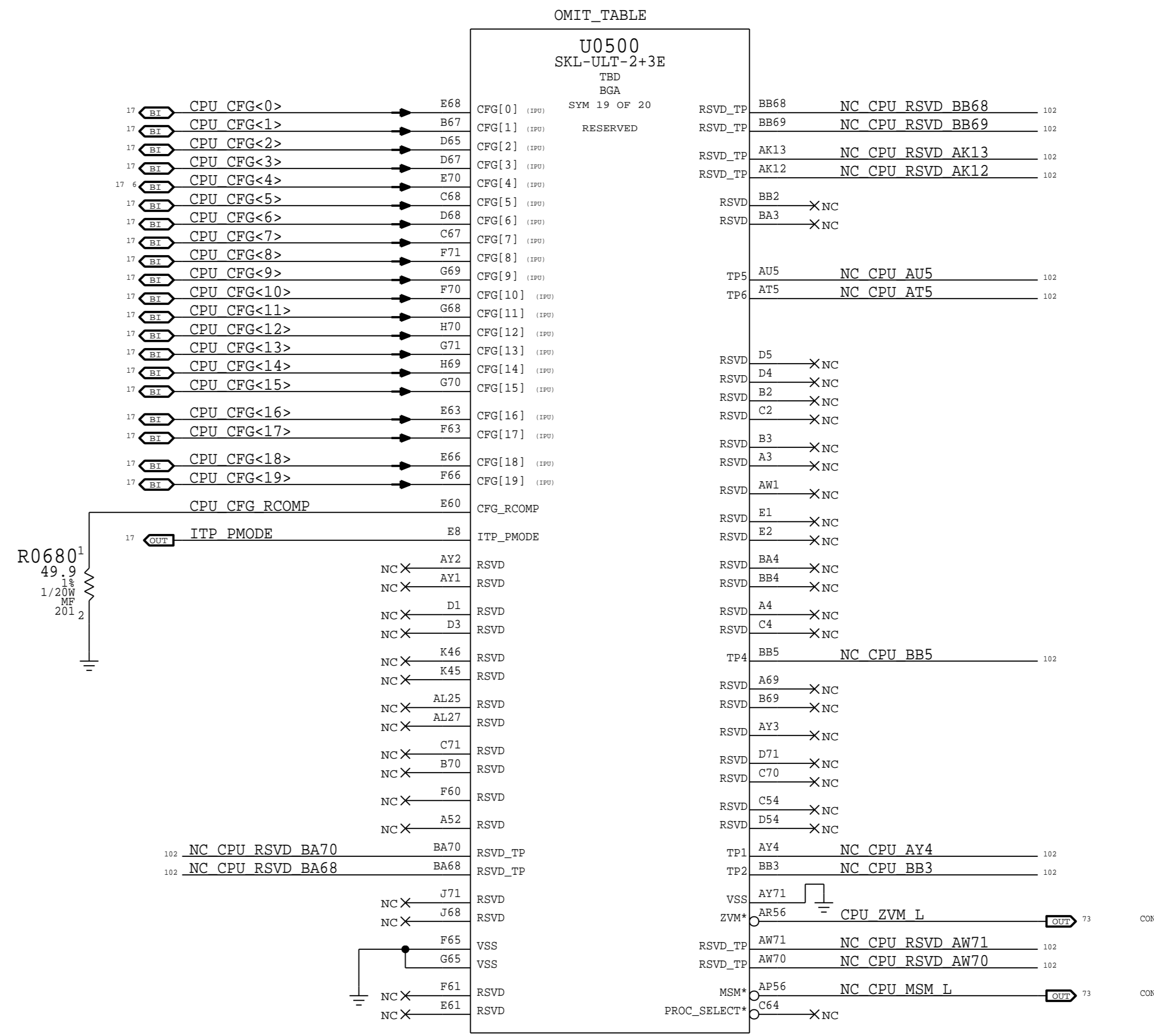
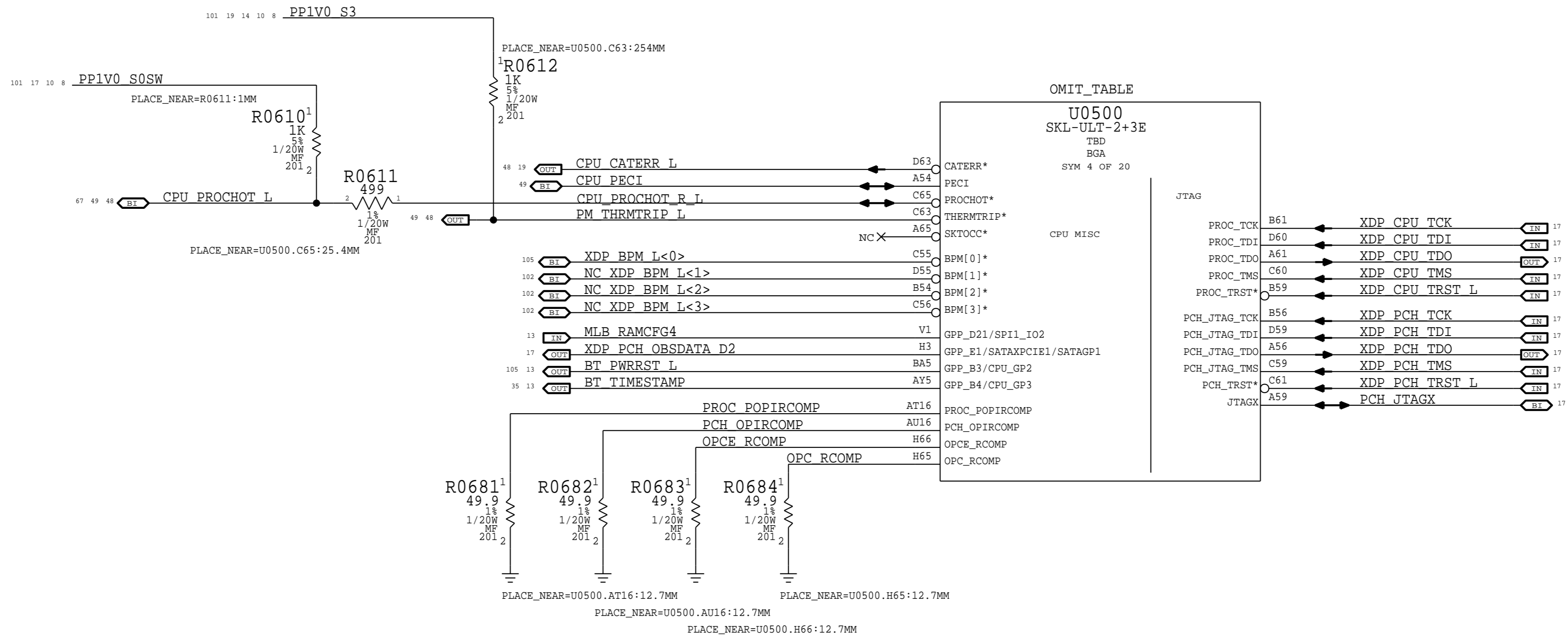
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Apple Inc.

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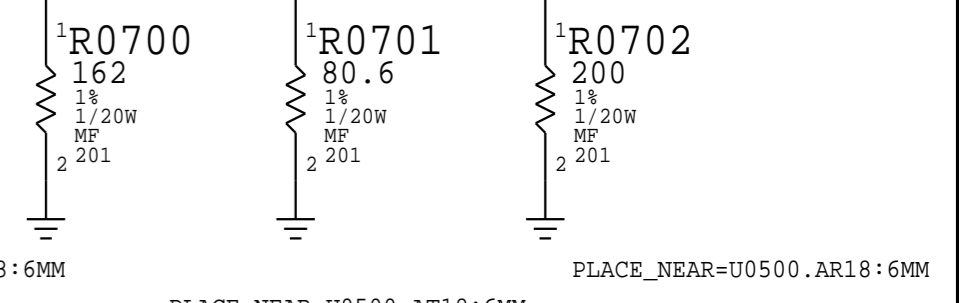
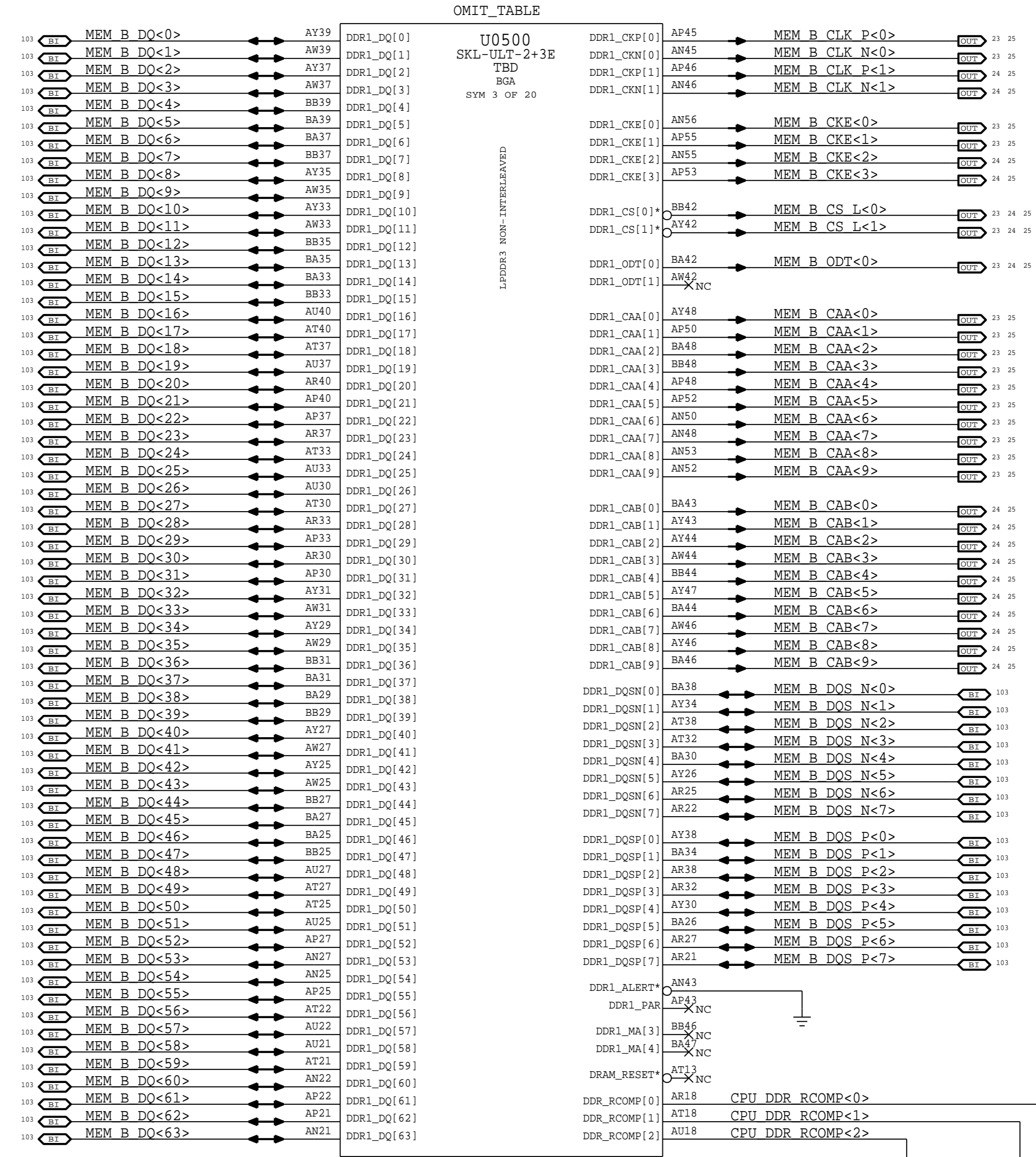
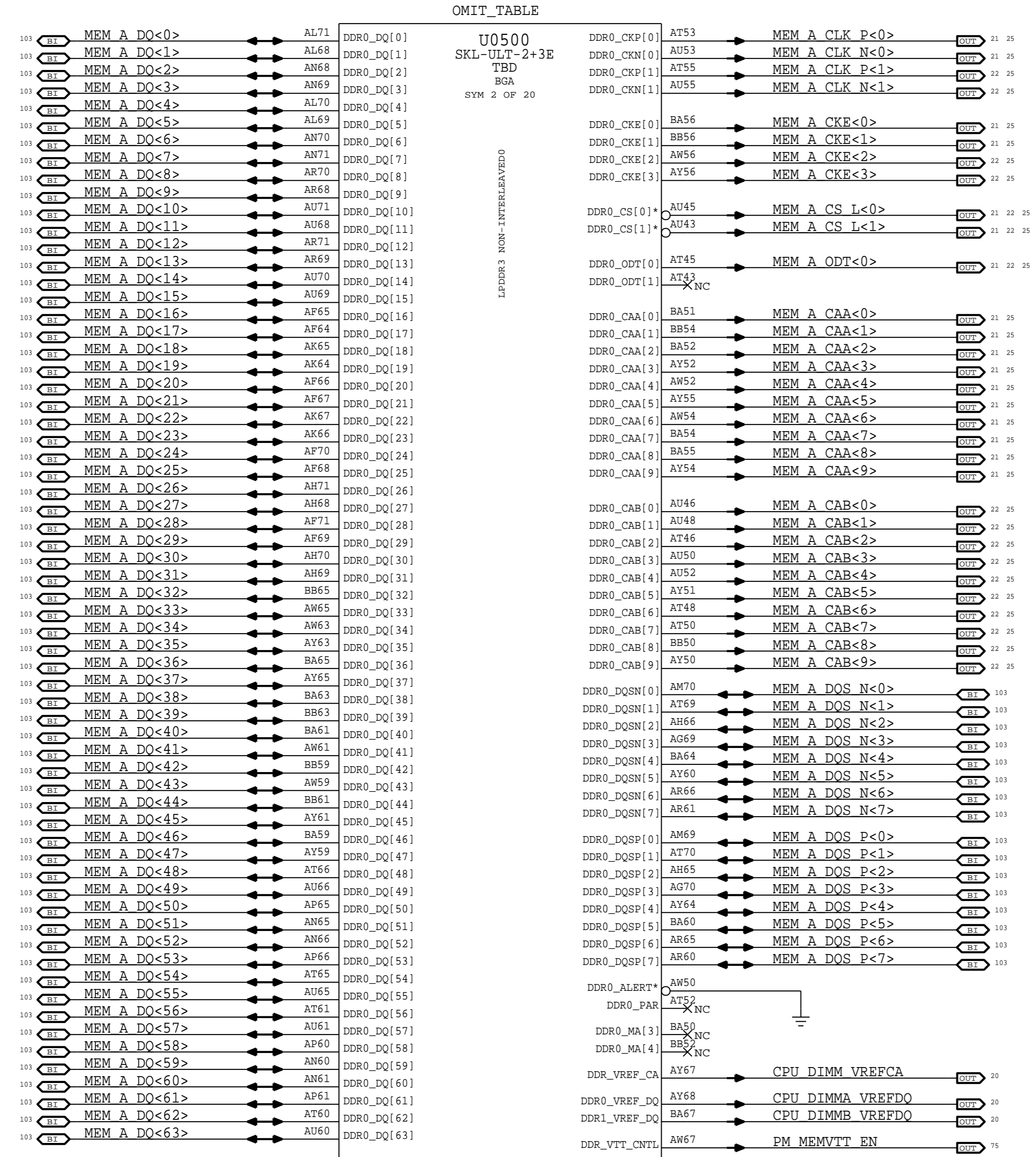
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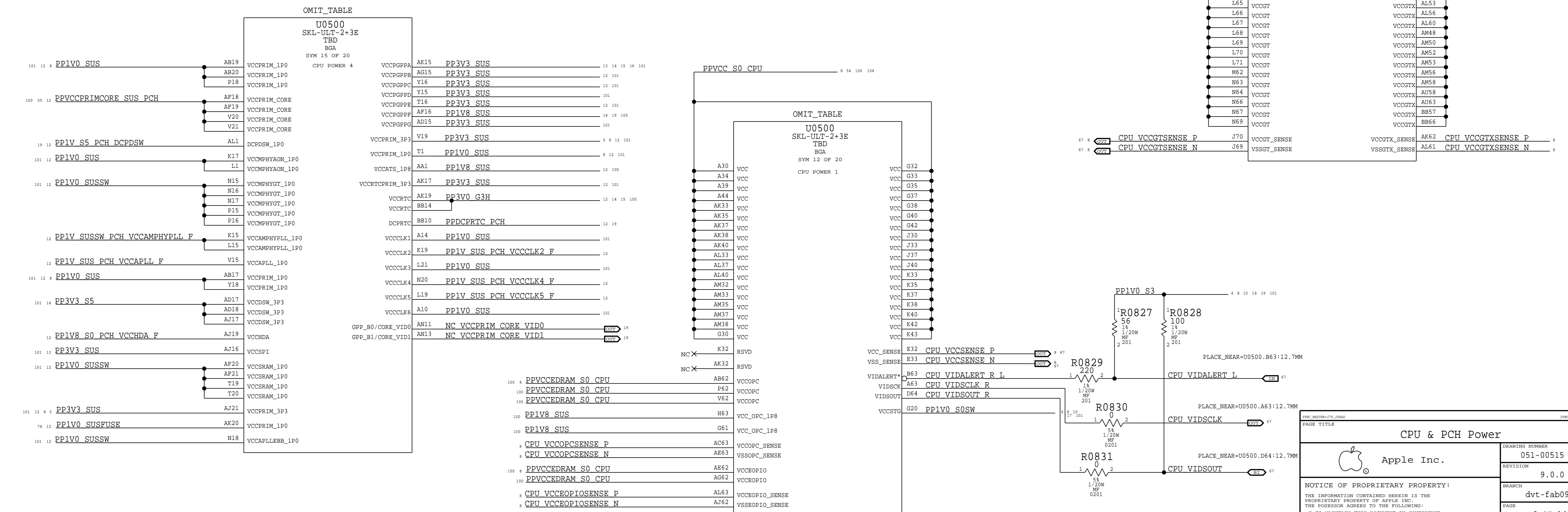
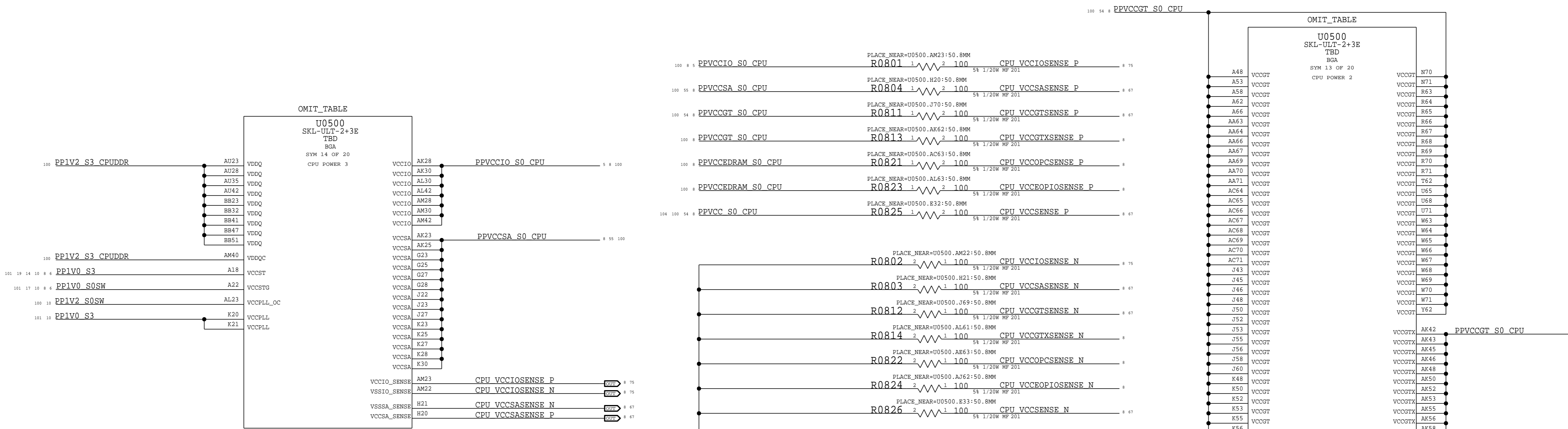
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CPU & PCH Power

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C

B

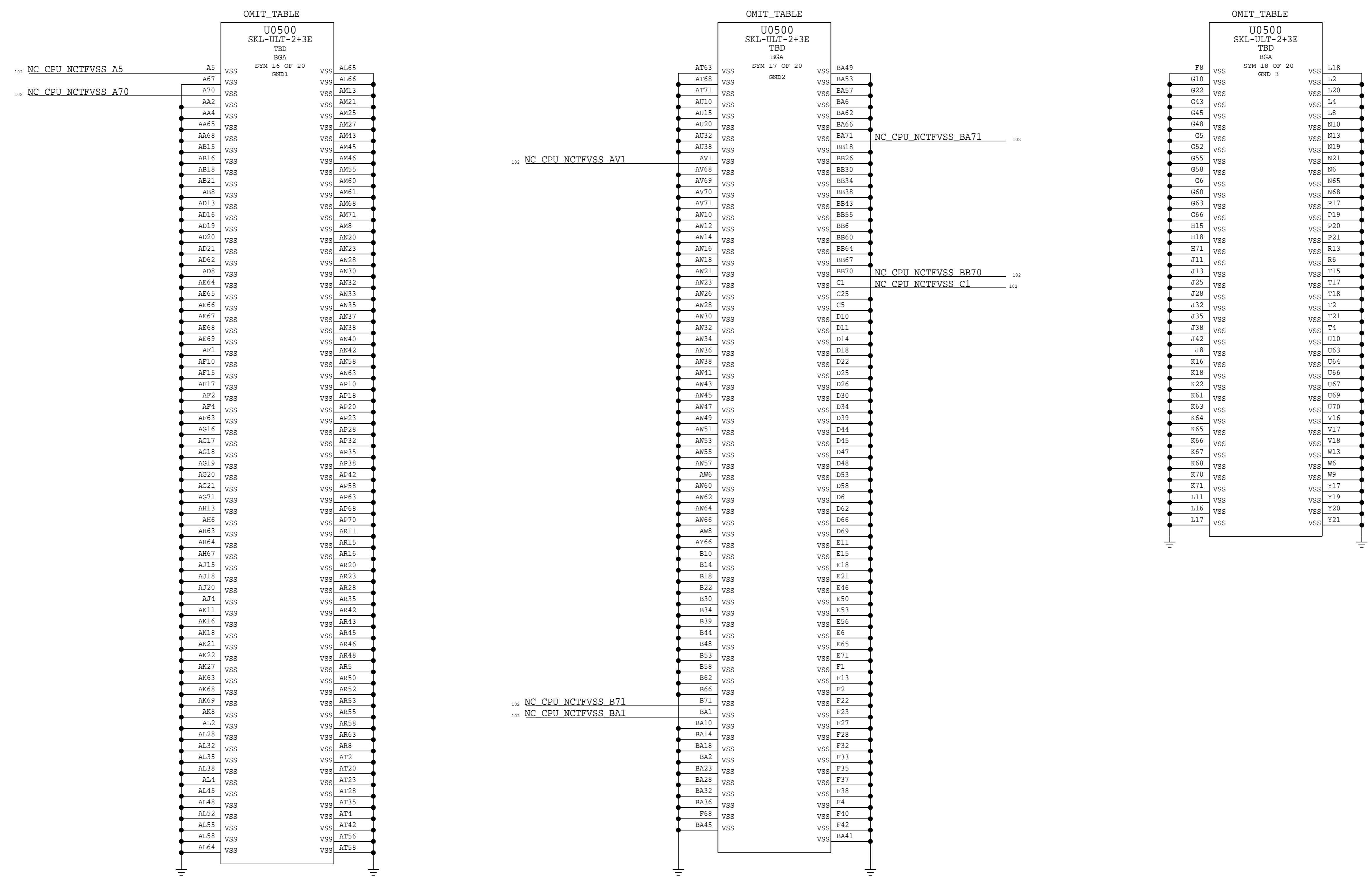
A

D

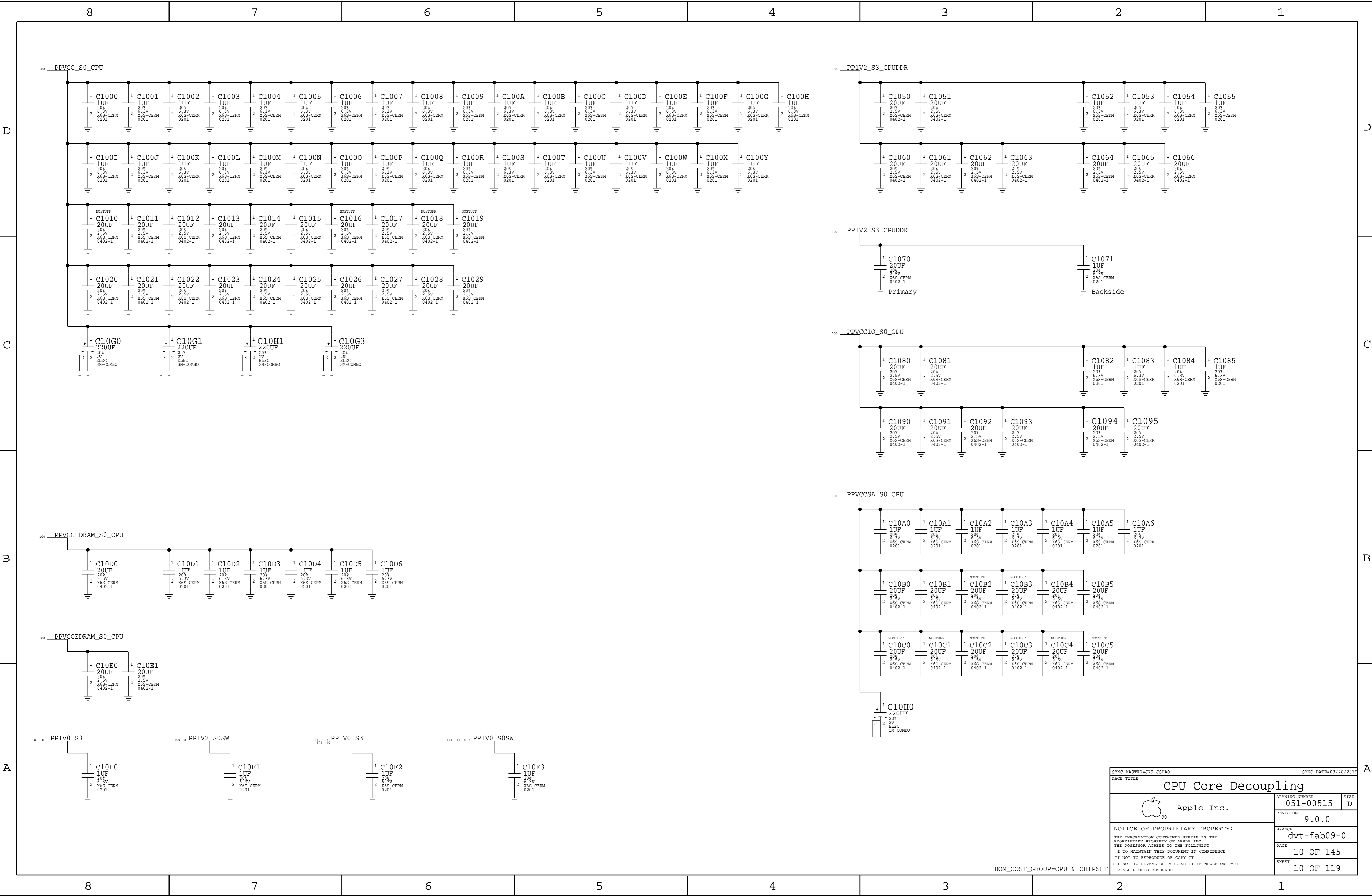
C

B

A



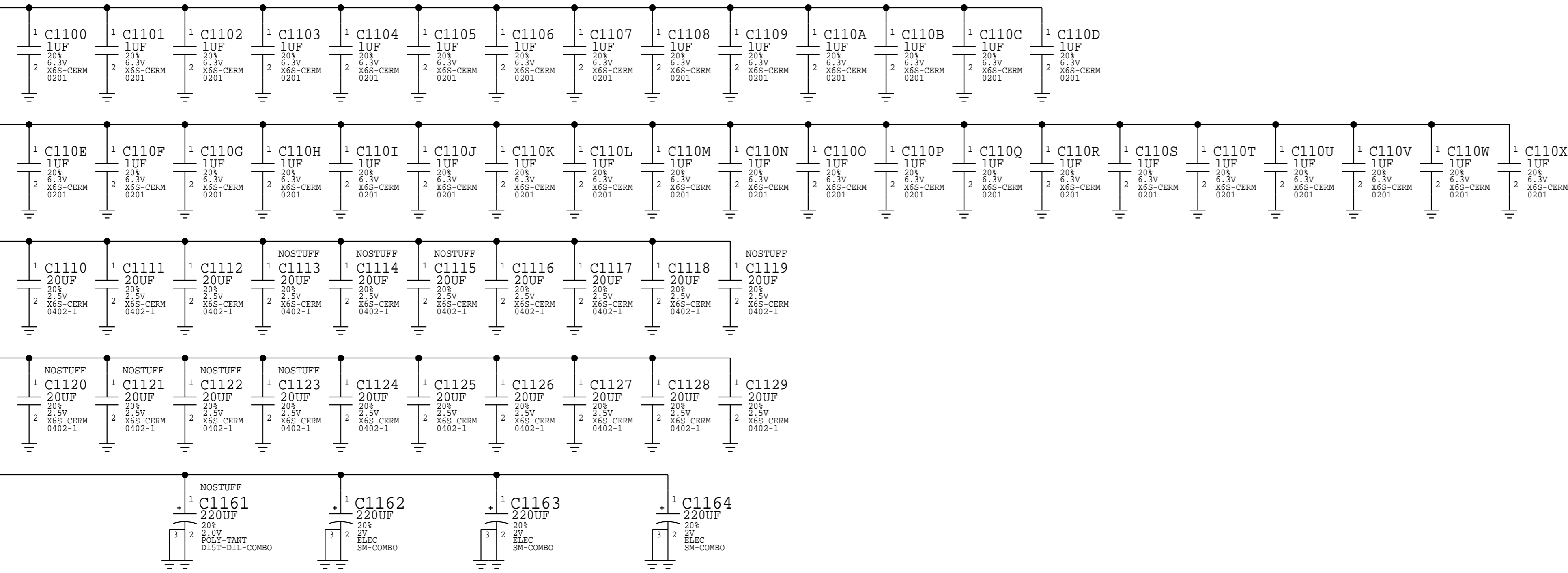
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PAGE TITLE			
CPU & PCH Grounds			
	DRAWING NUMBER	051-00515	STEP
	REVISION	9.0.0	D
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		PAGE	9 OF 145
		SHEET	9 OF 119



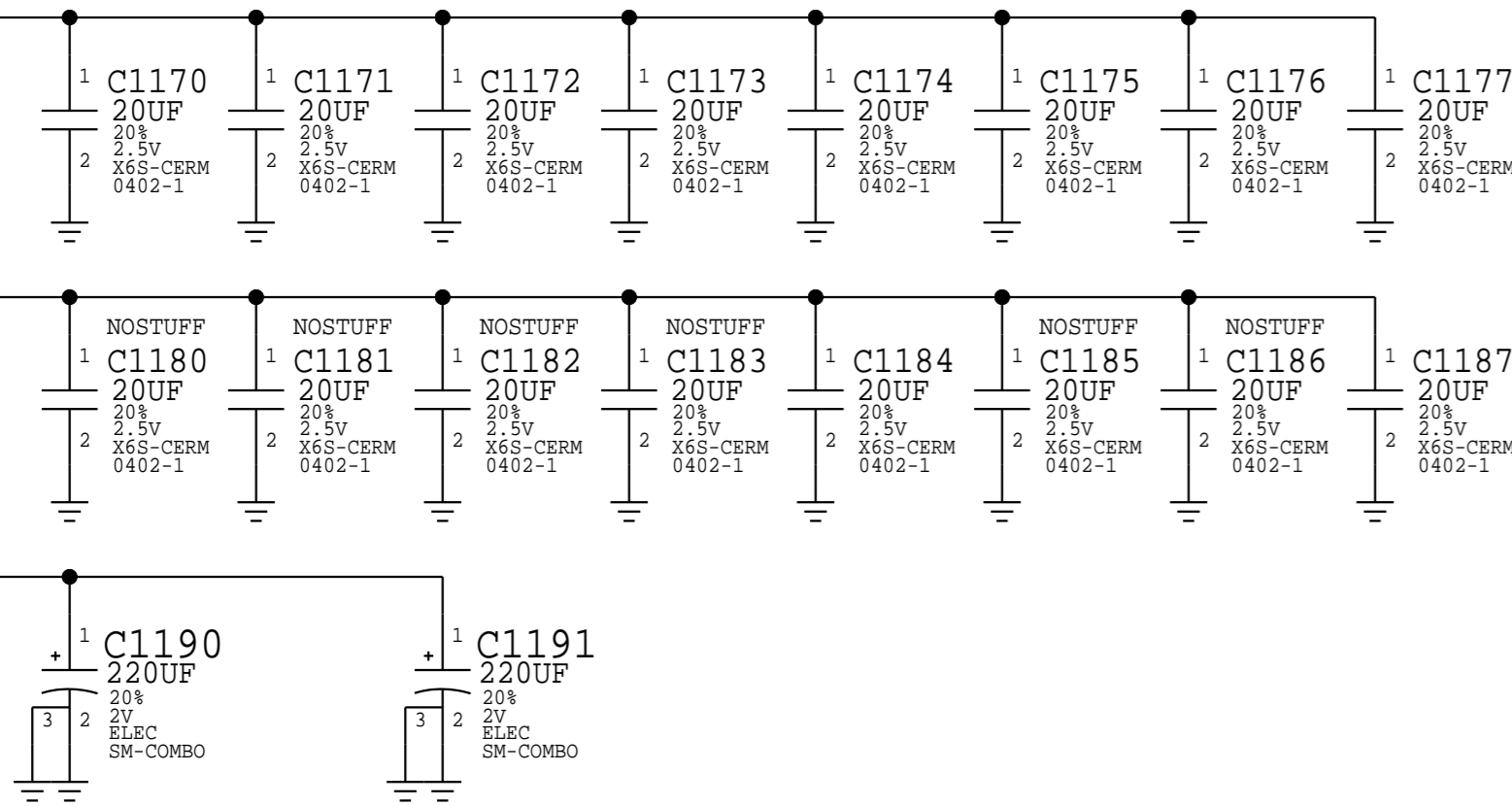
SYNC_MASTER=J79_JSHAO		SYNC_DATE=08/28/2015	
PAGE TITLE CPU Core Decoupling			
	DRAWING NUMBER	051-00515	STR
	REVISION	9.0.0	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED		BRANCH	dvt-fab09-0
		PAGE	10 OF 145
		SHEET	10 OF 119

BOM_COST_GROUP=CPU & CHIPSET

100_PPVCCGT_S0_CPU

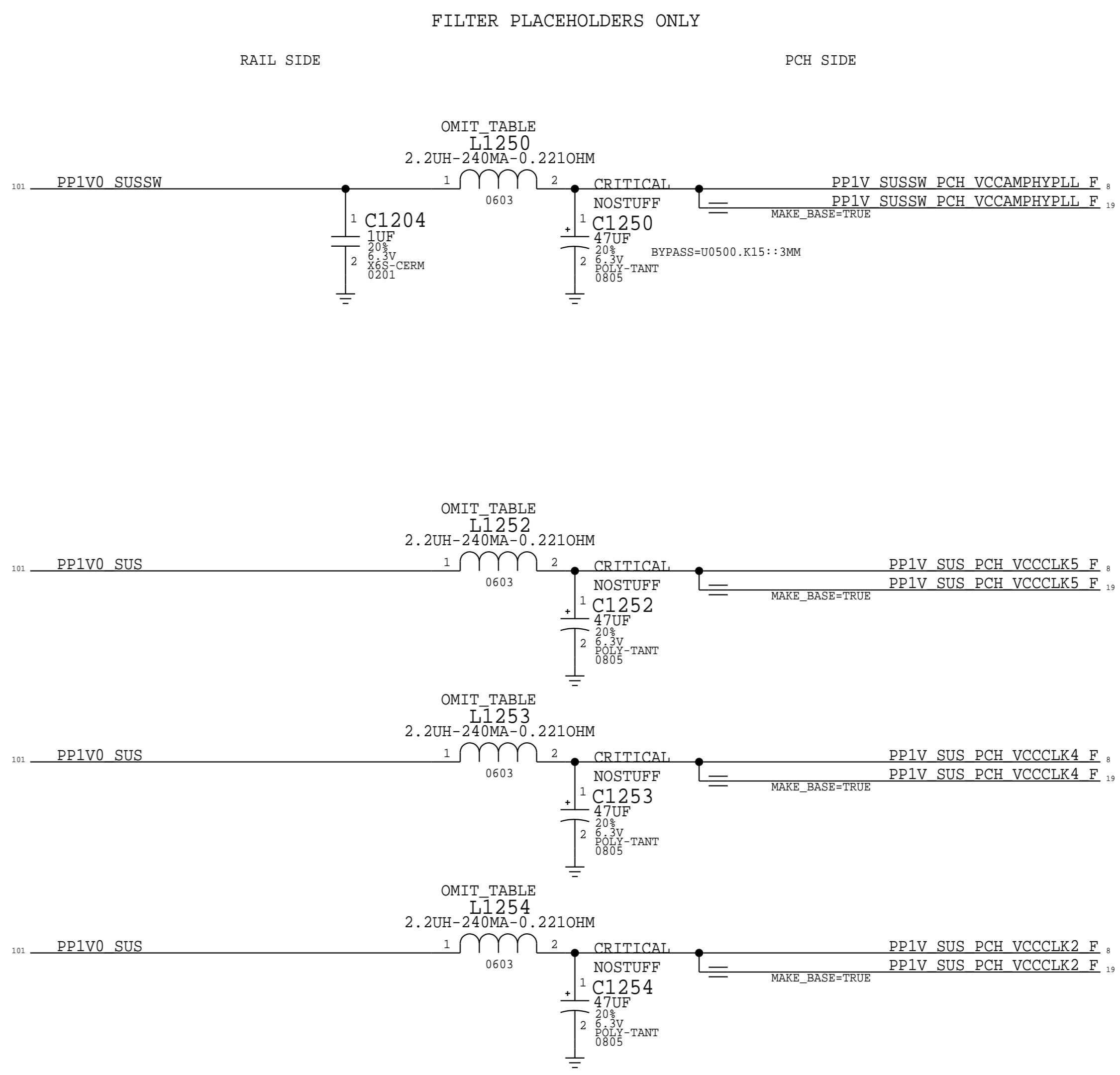
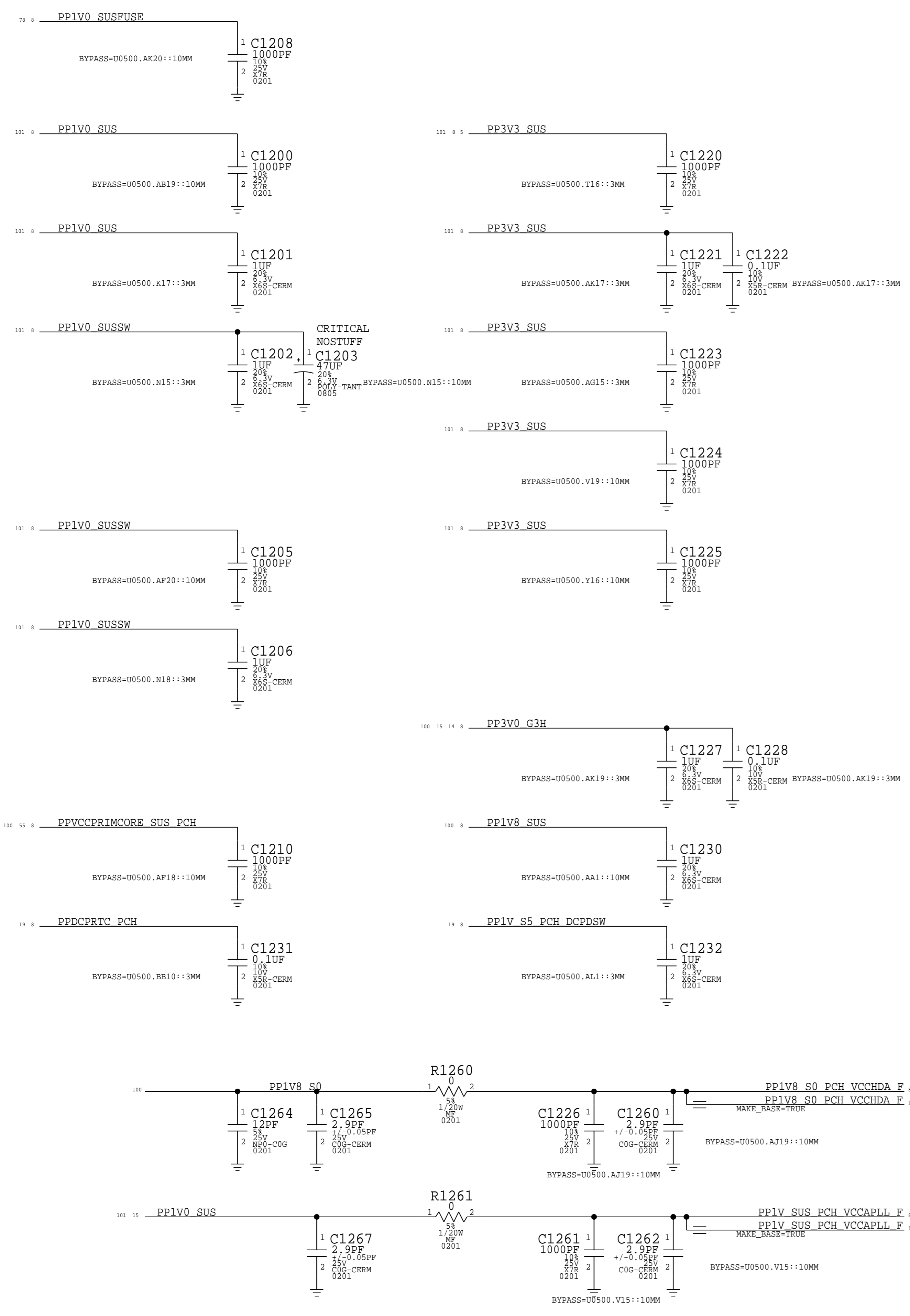


100_PPVCCGT_S0_CPU

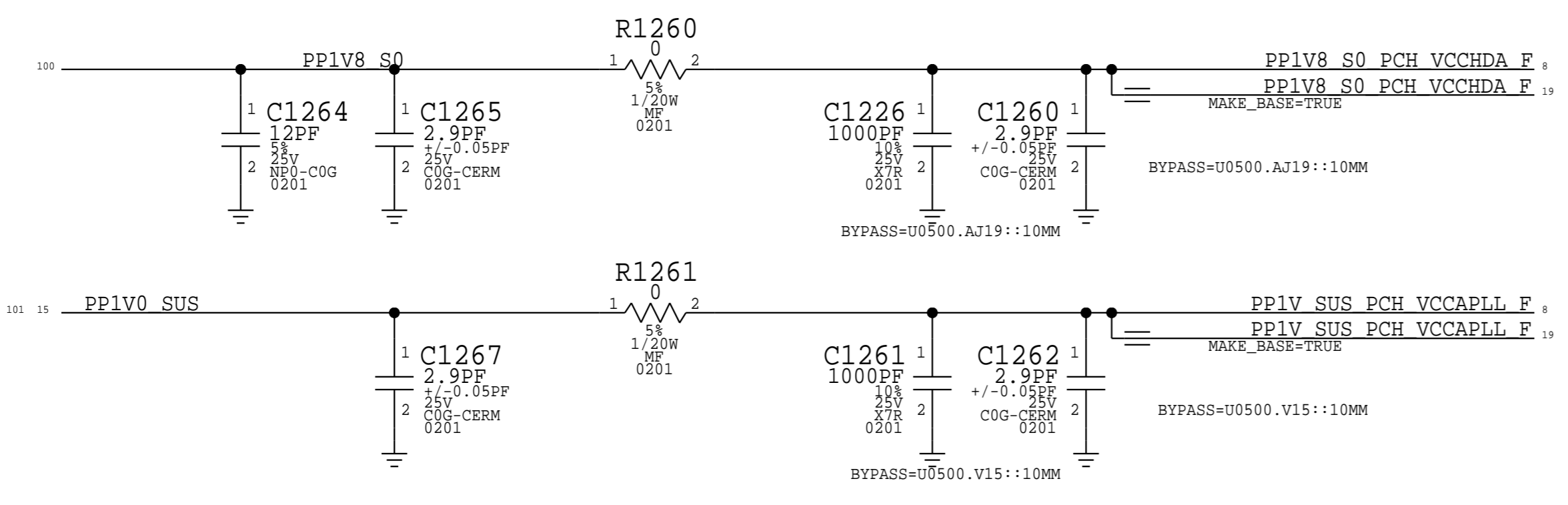
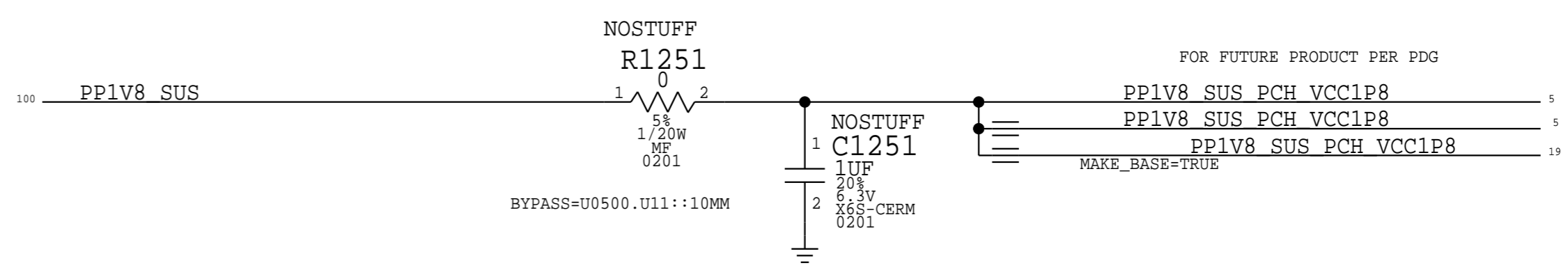


SYNC_MASTER=J79_JSHAO		SYNC_DATE=08/28/2015	
PAGE TITLE			
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DRAWING NUMBER		051-00515	
REVISION		9.0.0	
BRANCH		dvt-fab09-0	
PAGE		11 OF 145	
SHEET		11 OF 119	
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BOM_COST_GROUP=CPU & CHIPSET

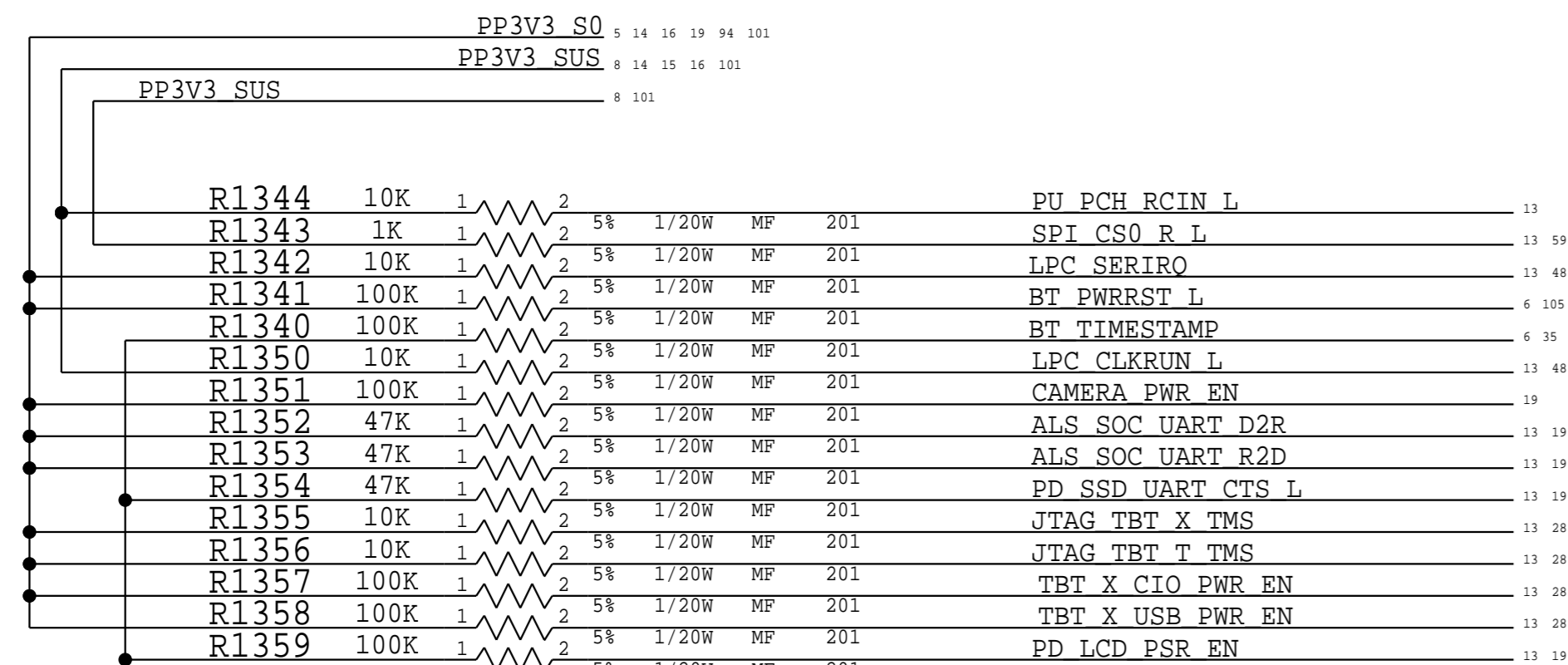
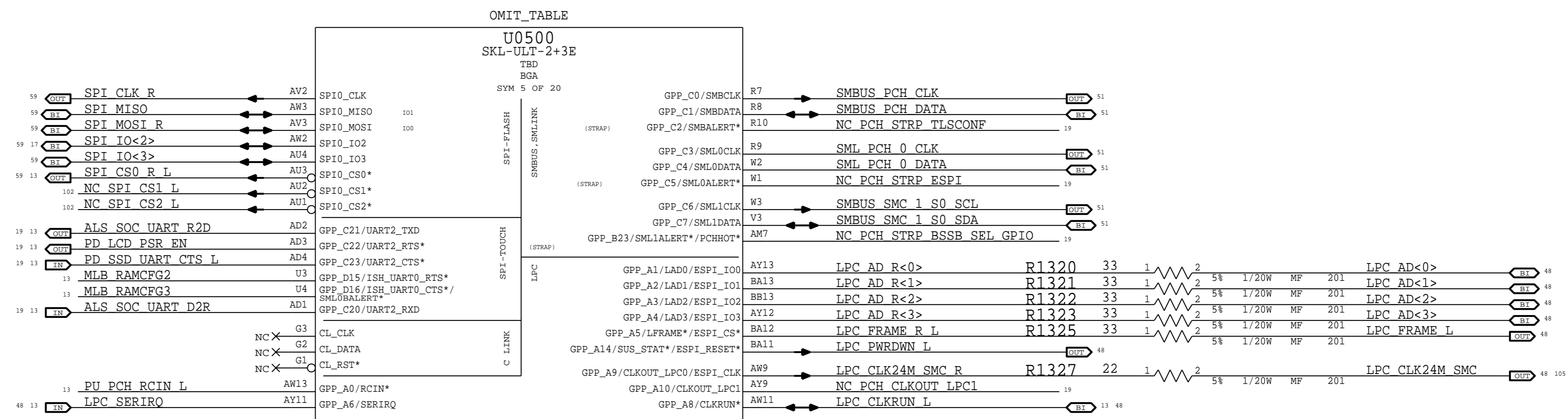
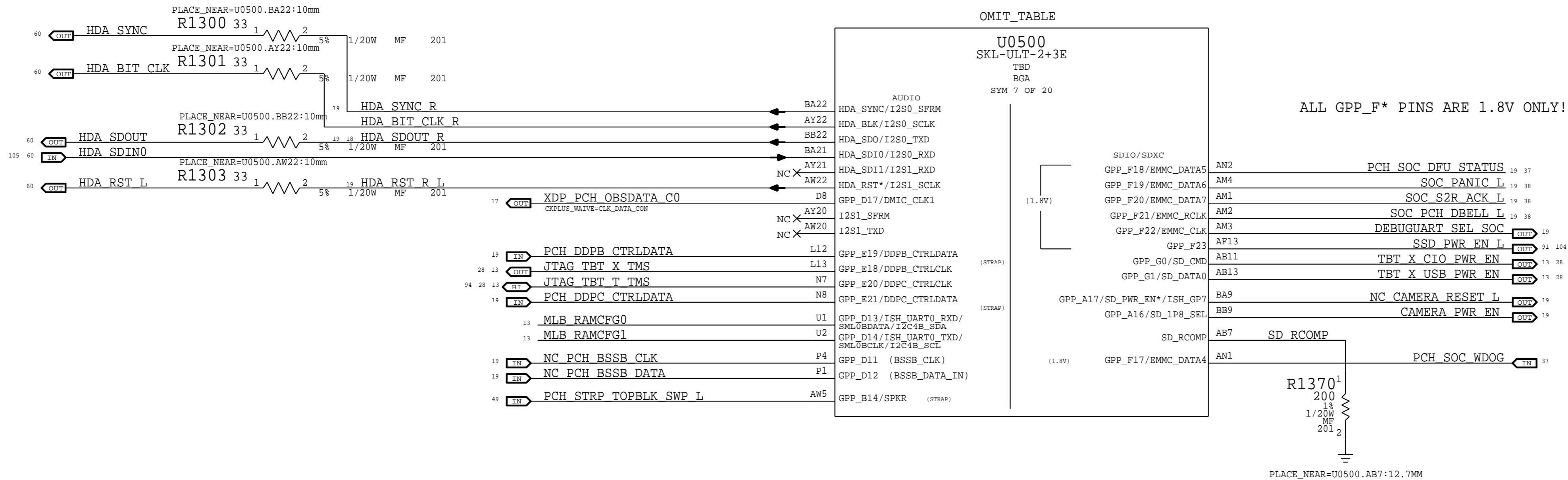


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES, MF, 1A MAX, 0OHM, 5%, 0603	L1250, L1252, L1253, L1254		



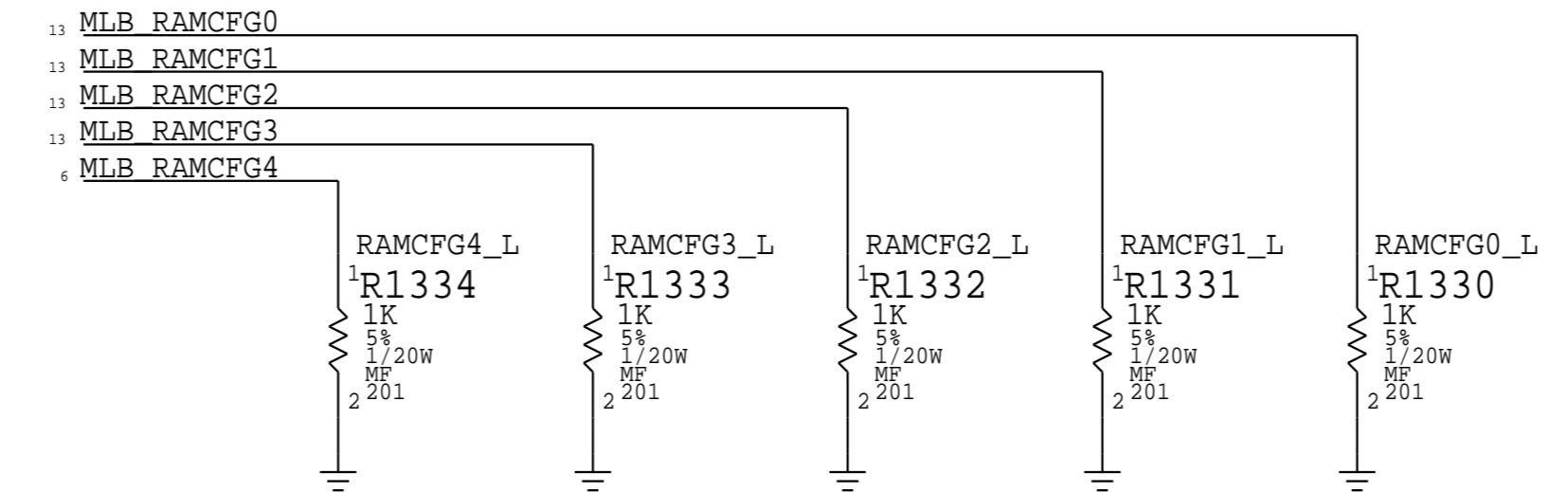
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE PCH Decoupling		
	DRAWING NUMBER 051-00515	SIZE D
	REVISION 9.0.0	
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	SHEET 12 OF 119	



MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.

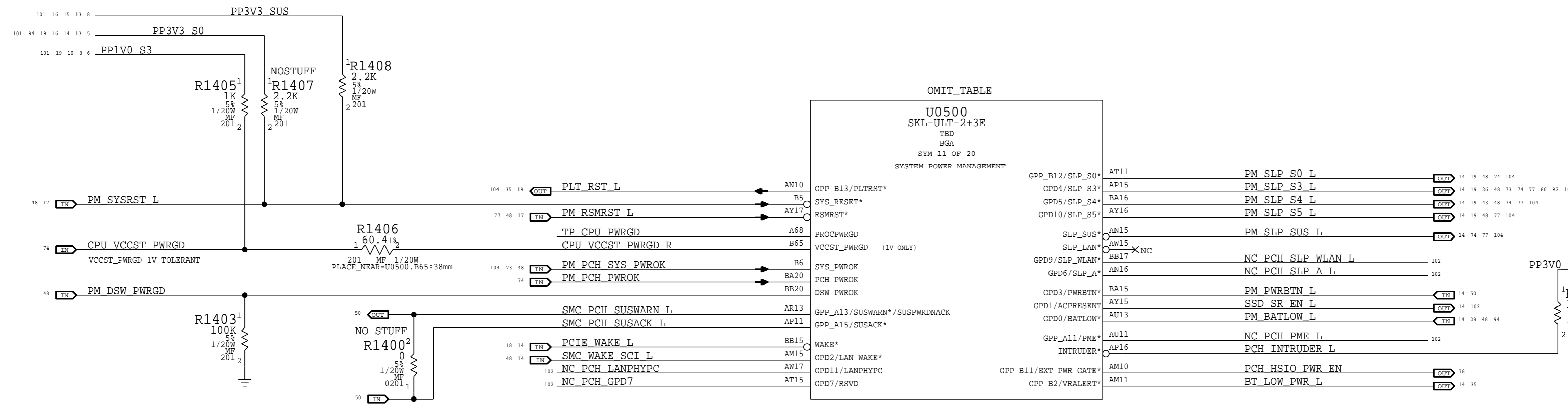


BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L, RAMCFG3_L, RAMCFG2_L, RAMCFG1_L, RAMCFG0_L

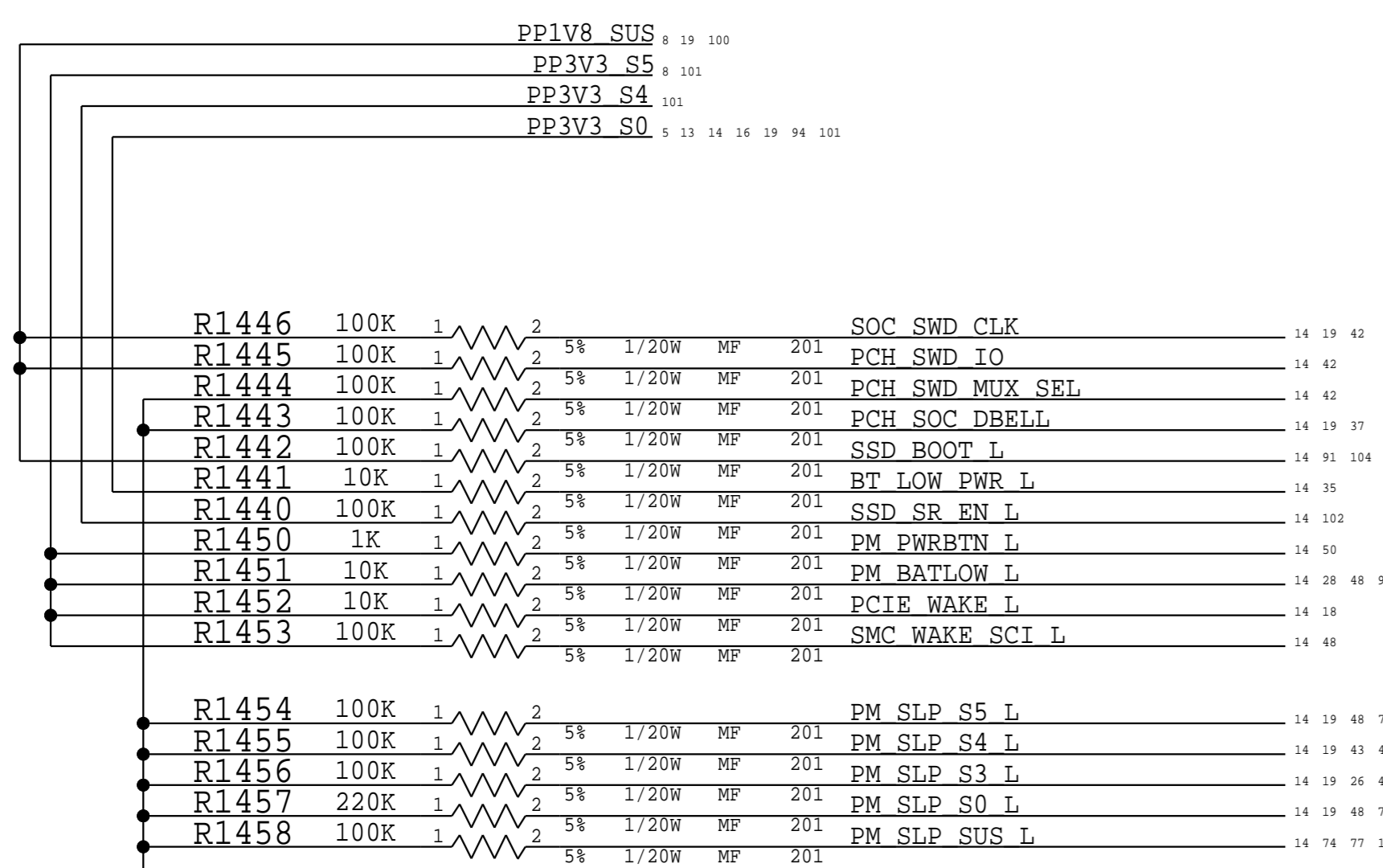
BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB		LAST CHANGE: Tue Feb 2 13:18:21 2016	
PCH Audio/LPC/SPI/SMBus			
Apple Inc.		DRAWING NUMBER 051-00515	SIZE D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 11V ALL RIGHTS RESERVED		REVISION 9.0.0	PAGE 13 OF 145
		BRANCH dvt-fab09-0	SHEET 13 OF 119

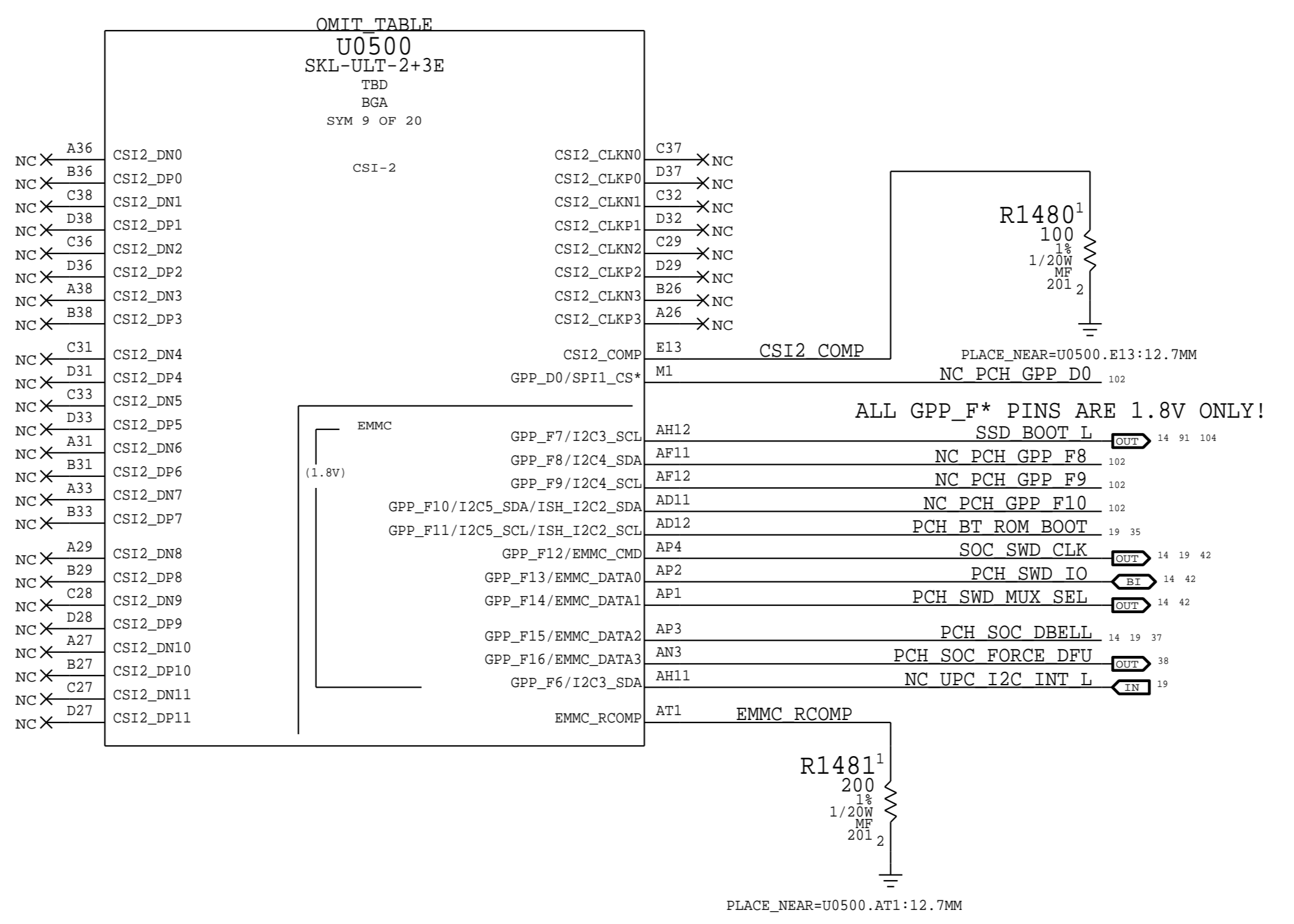
PCH Reset Button



R1400 kept for debug purposes.



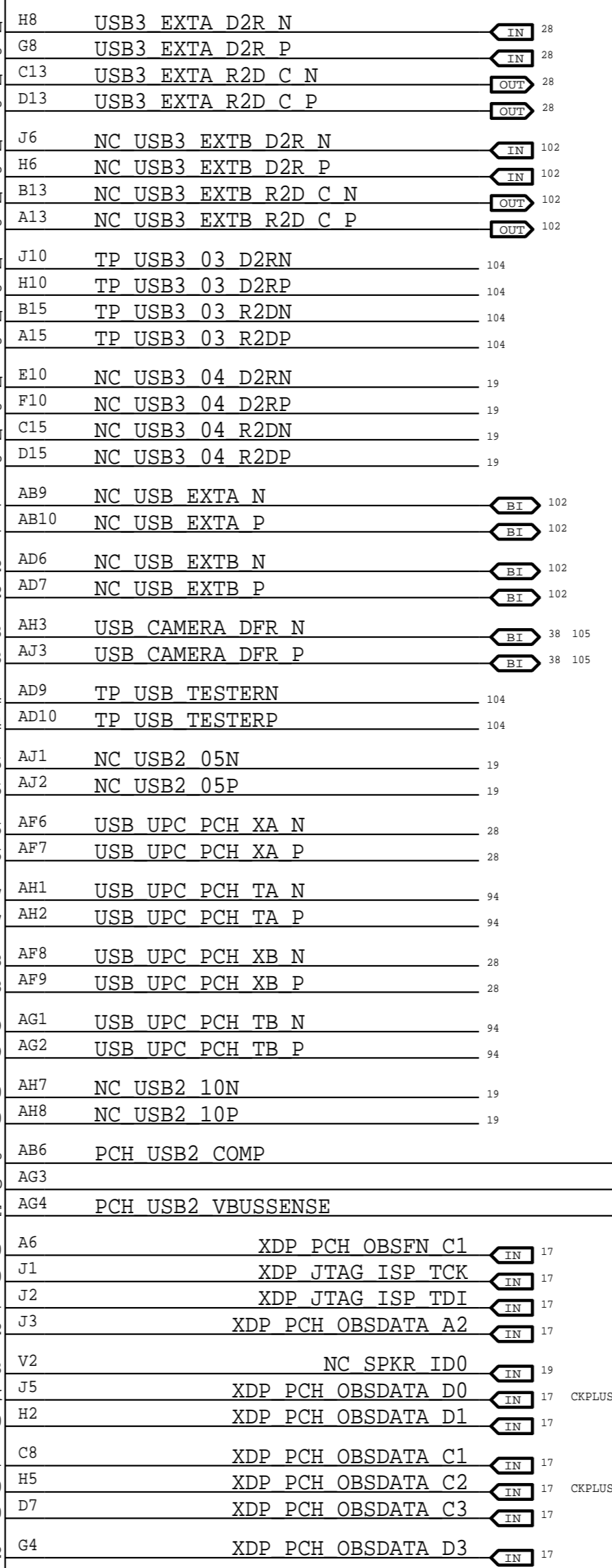
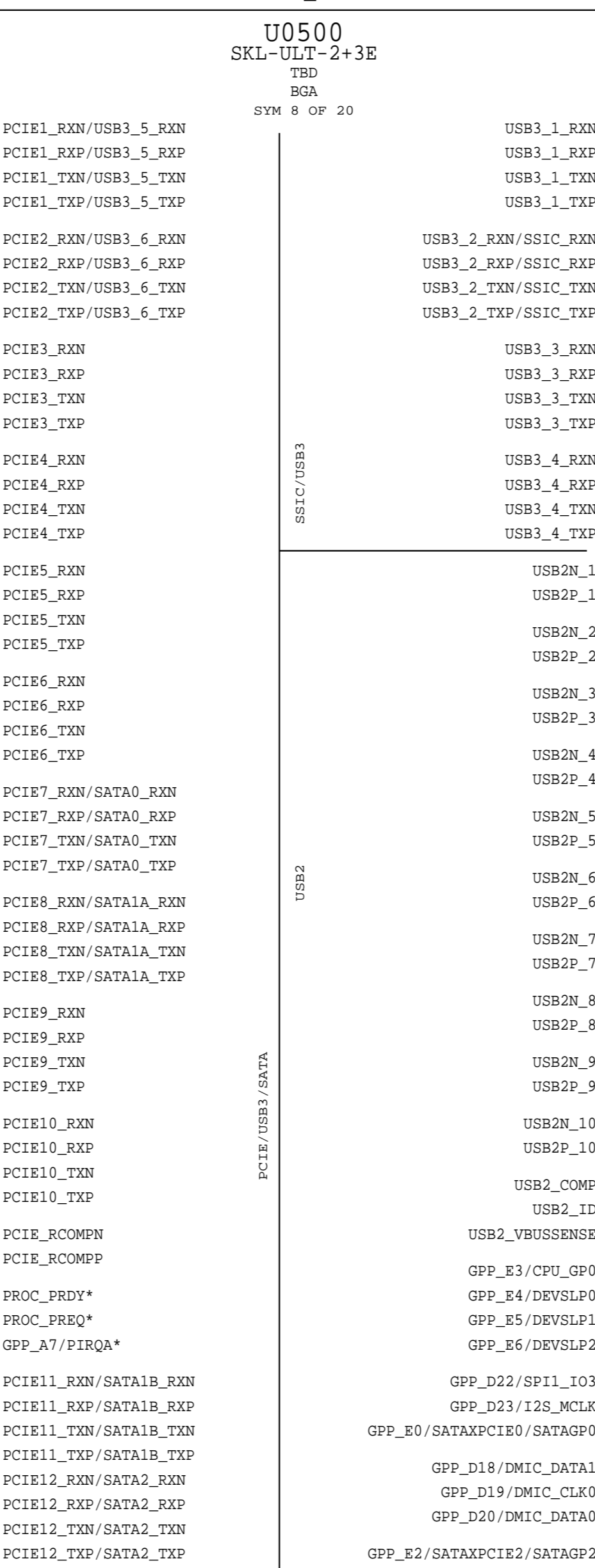
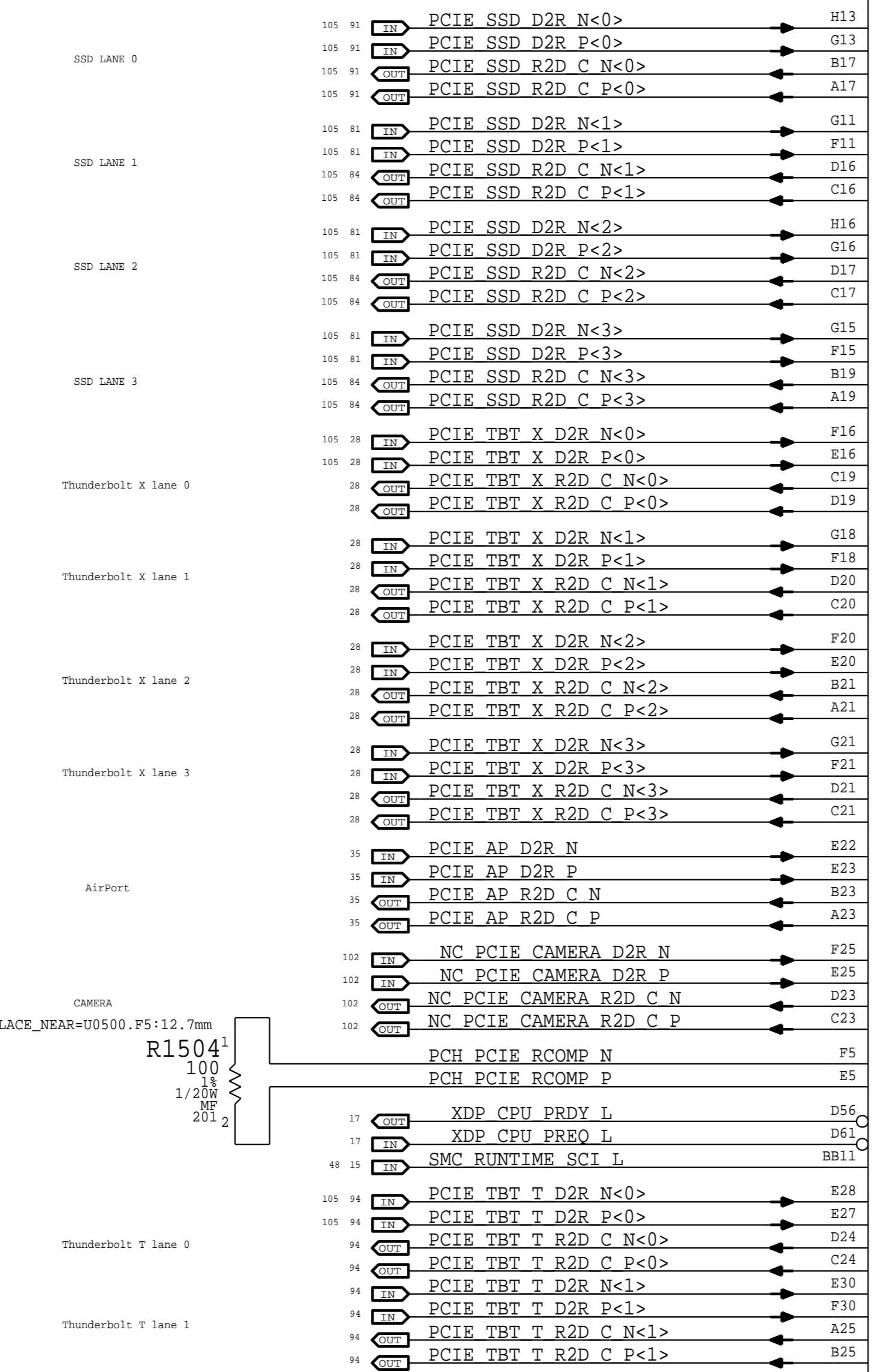
NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED. THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE. THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.



ALL GPP_F* PINS ARE 1.8V ONLY!

DESIGN: X502/MLB	
LAST CHANGE: Tue May 3 17:45:28 2016	
PAGE TITLE	
PCH Power Management	
	DRAWING NUMBER 051-00515
	REVISION 9.0.0
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BRANCH dvt-fab09-0	PAGE 14 OF 145
SHEET 14 OF 119	BOM_COST_GROUP=CPU & CHIPSET

PCIE Port Assignments:

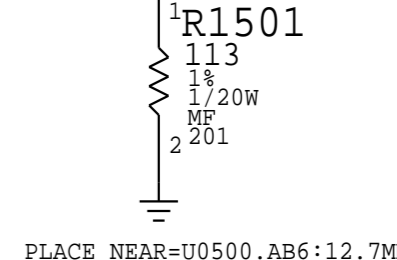
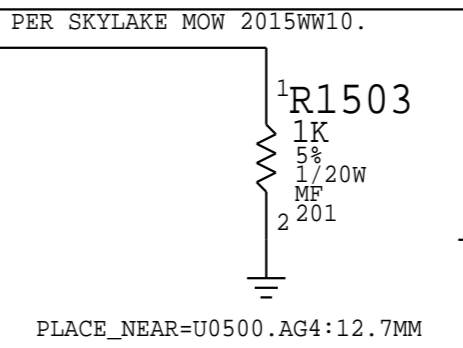
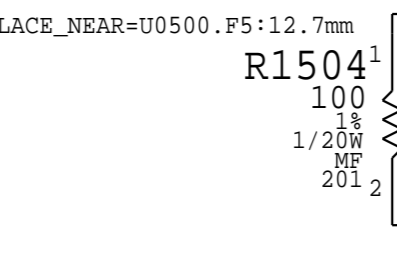


EXT A (SS,DCI)

EXT B (SS)

EXT A (LS/FS/HS)

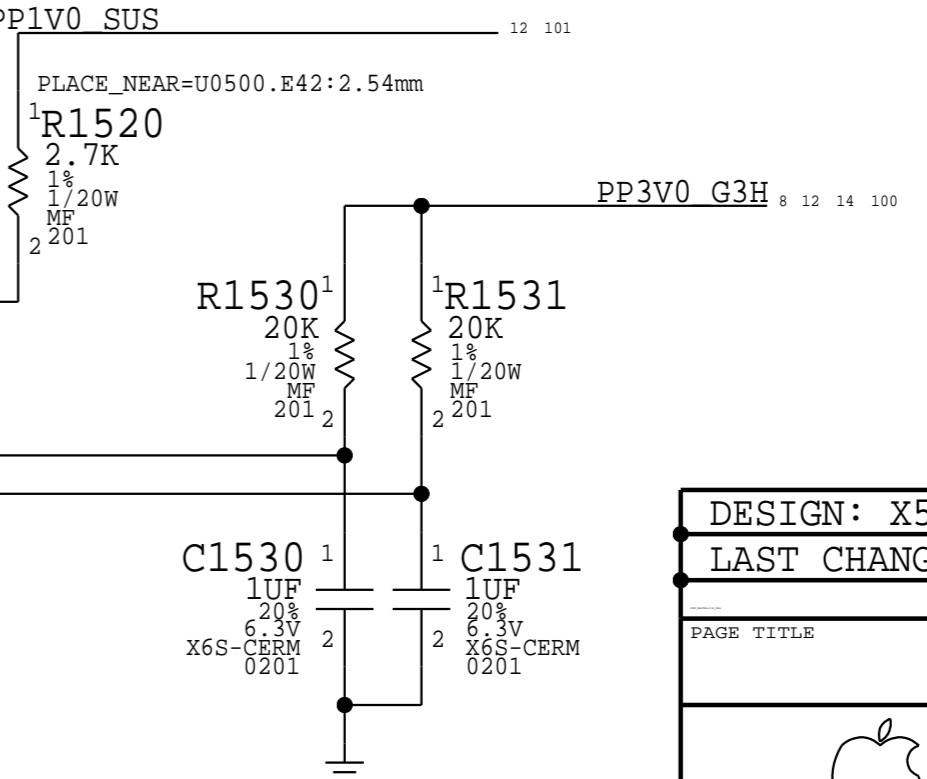
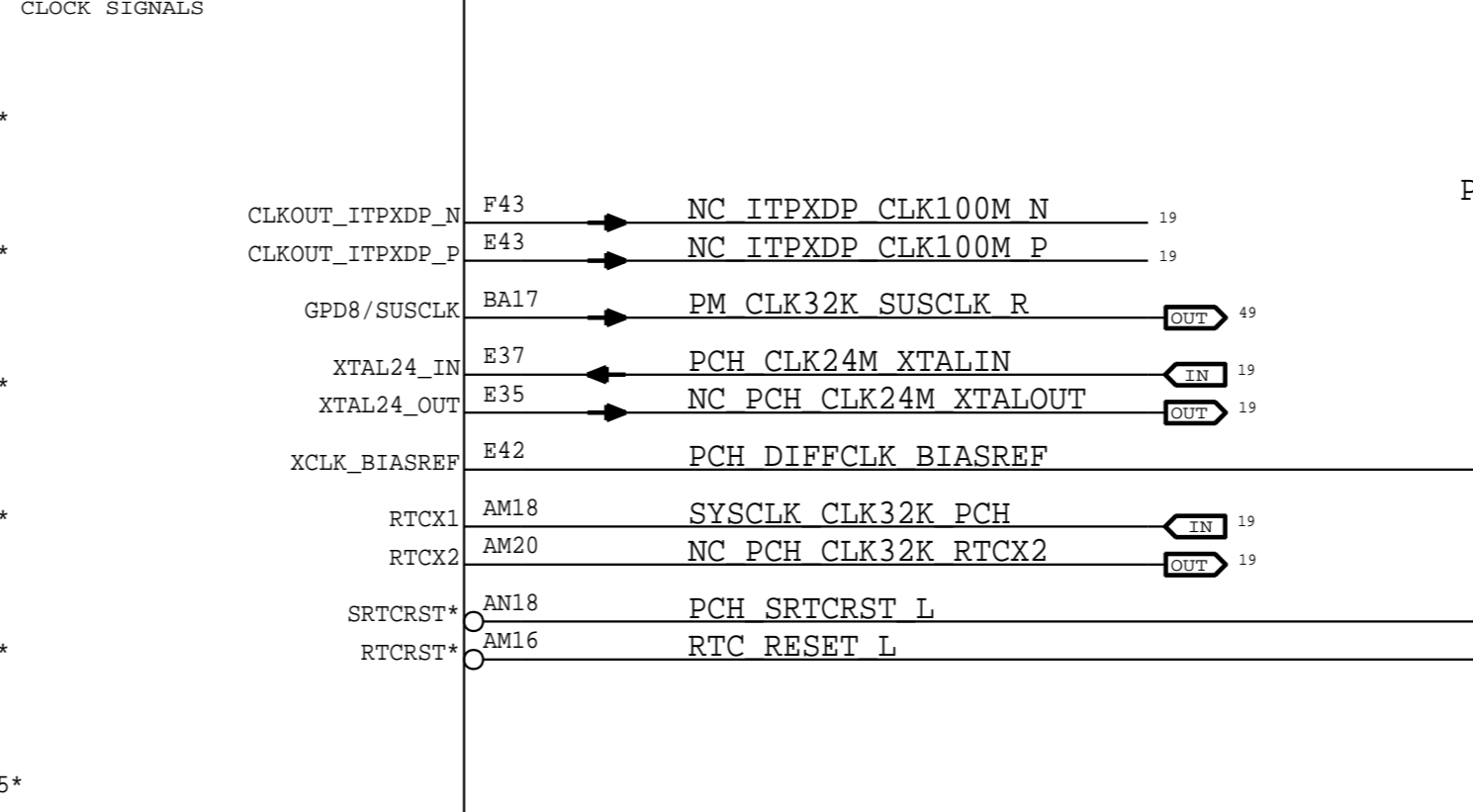
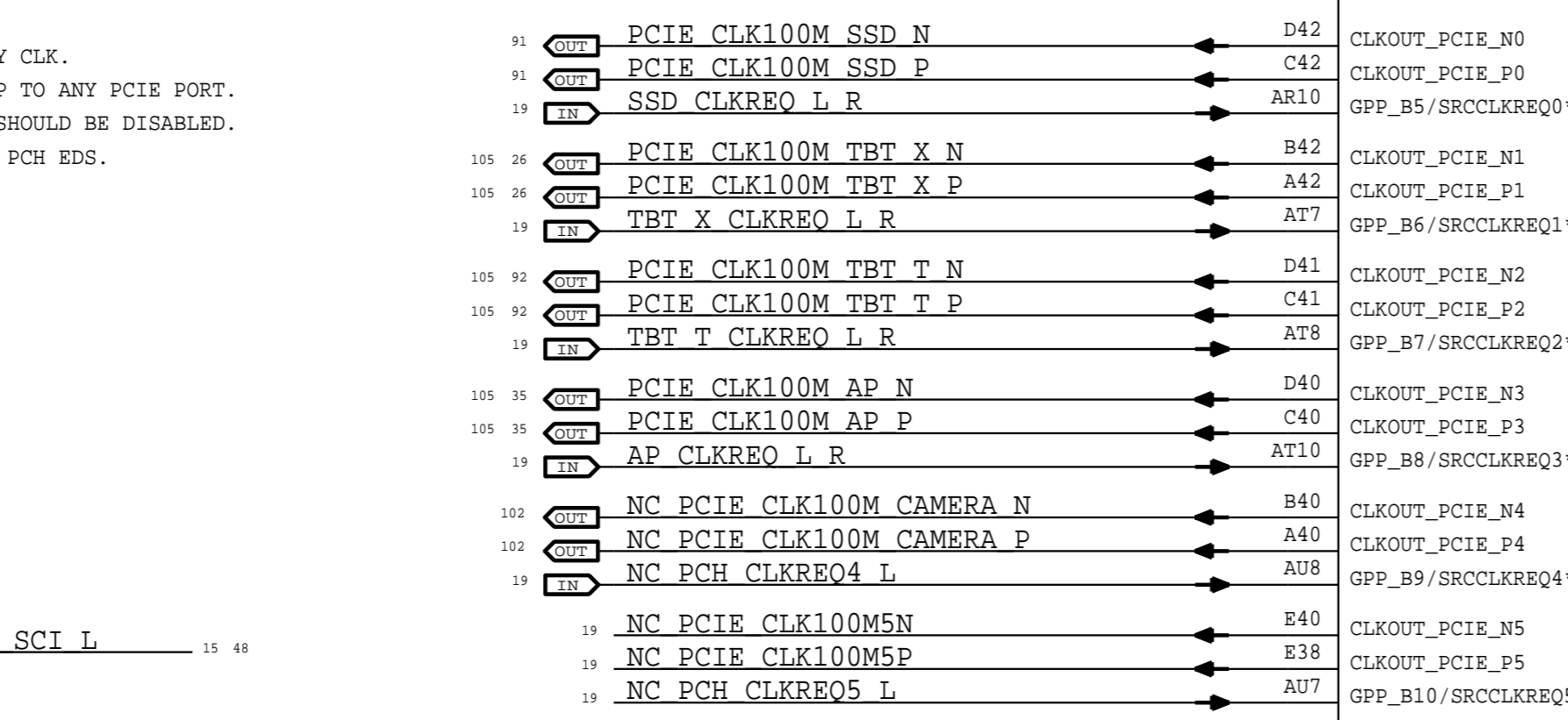
EXT B (LS/FS/HS)



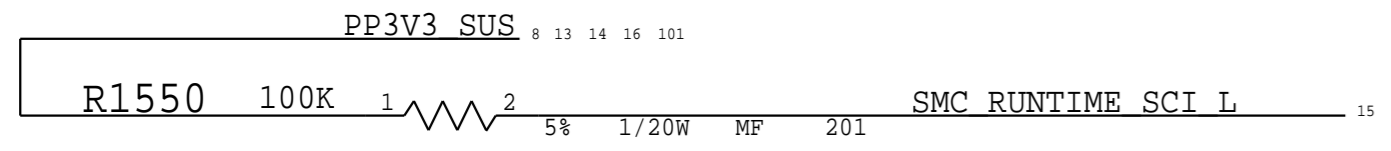
OMIT_TABLE

U0500 SKL-ULT-2+3E TBD BGA SYM 10 OF 20

CLOCK SIGNALS



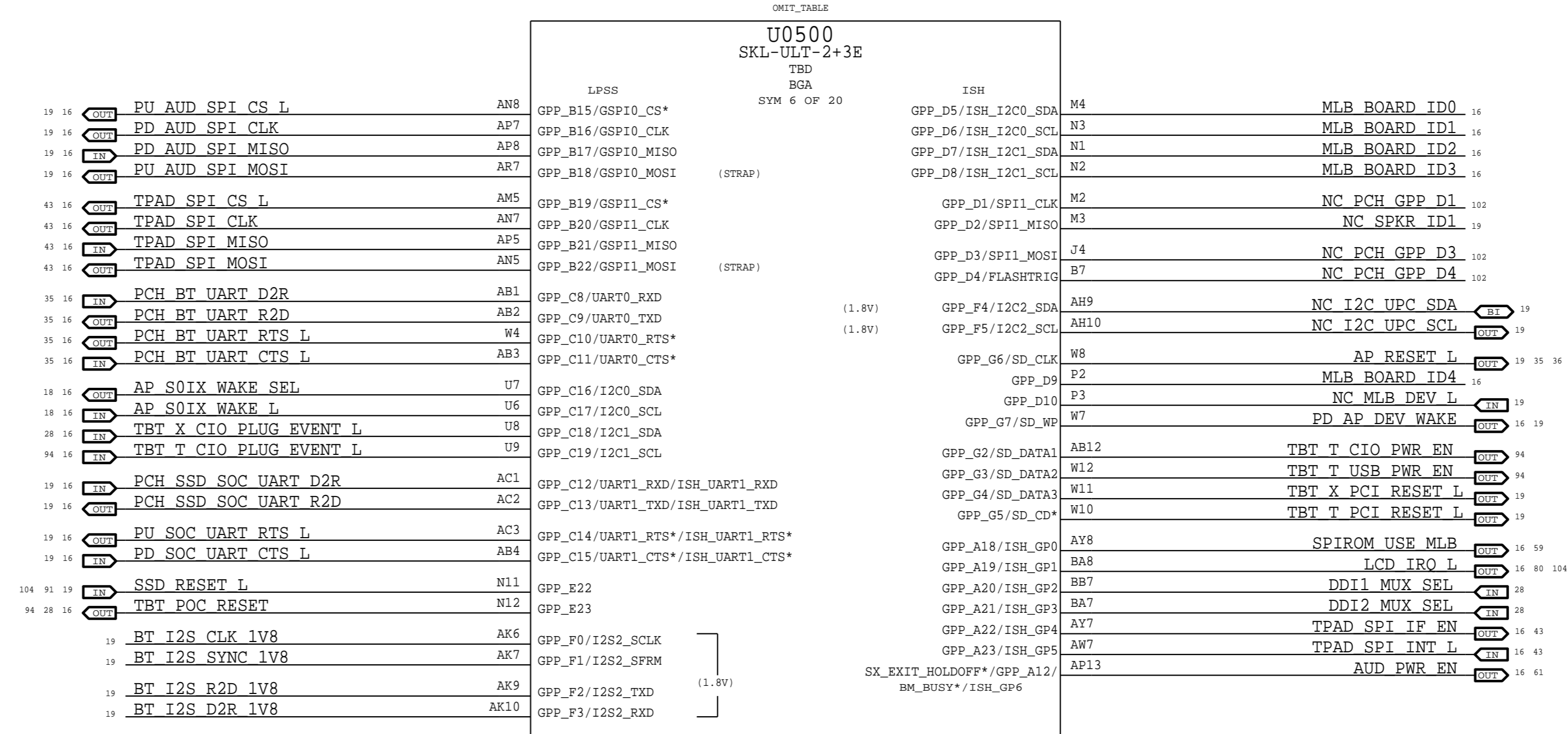
ANY CLKREQ CAN MAP TO ANY CLK.
 ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
 UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
 PER SKYLAKE PDG, SKYLAKE PCH EDS.



DESIGN: X502/MLB		LAST CHANGE: Thu Jun 18 20:05:18 2015	
PAGE TITLE			
PCH PCIE/USB/CLKS			
		DRAWING NUMBER	501-00515
		REVISION	9.0.0
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		PAGE	15 OF 145
		SHEET	15 OF 119

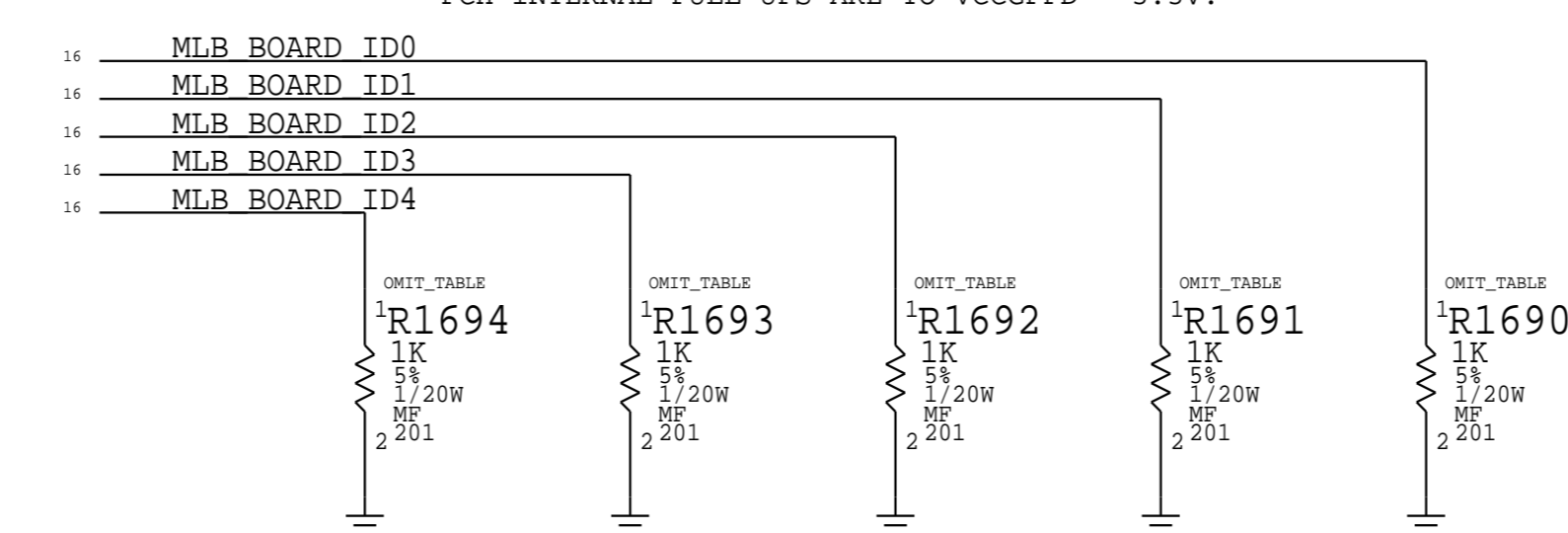
BOM_COST_GROUP=CPU & CHIPSET

ALL GPP_F* PINS ARE 1.8V ONLY!

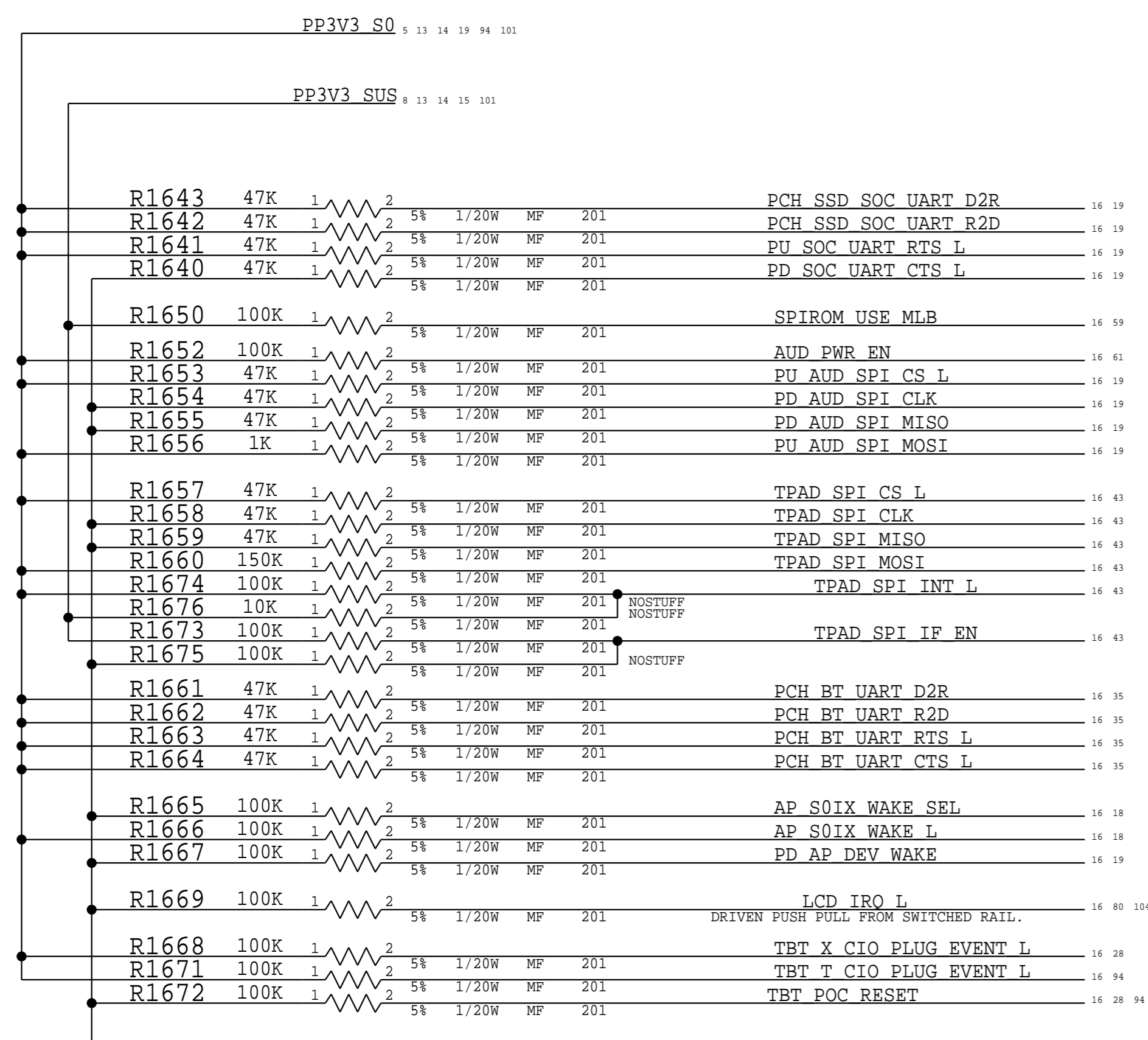


MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES.MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES.MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES.MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES.MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES.MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES.MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES.MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES.MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES.MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES.MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES.MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES.MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES.MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>



BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Wed Oct 28 12:50:22 2015

PAGE TITLE: PCH SPI/UART/GPIO

Apple Inc.

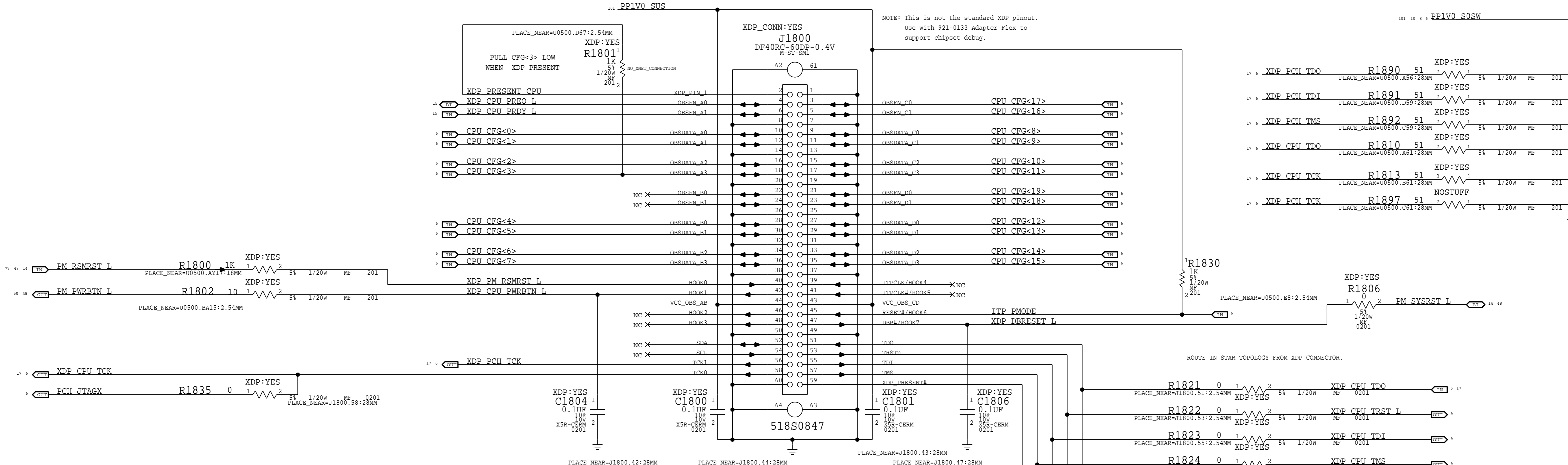
DRAWING NUMBER: 051-00515
REVISION: 9.0.0
BRANCH: dvt-fab09-0

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PAGE: 16 OF 145
SHEET: 16 OF 119

Primary / Merged (CPU/PCH) Micro2-XDP

101 PP1V0 SUS



NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

101 10 8 6 PP1V0 S0SW

PCH XDP Signals

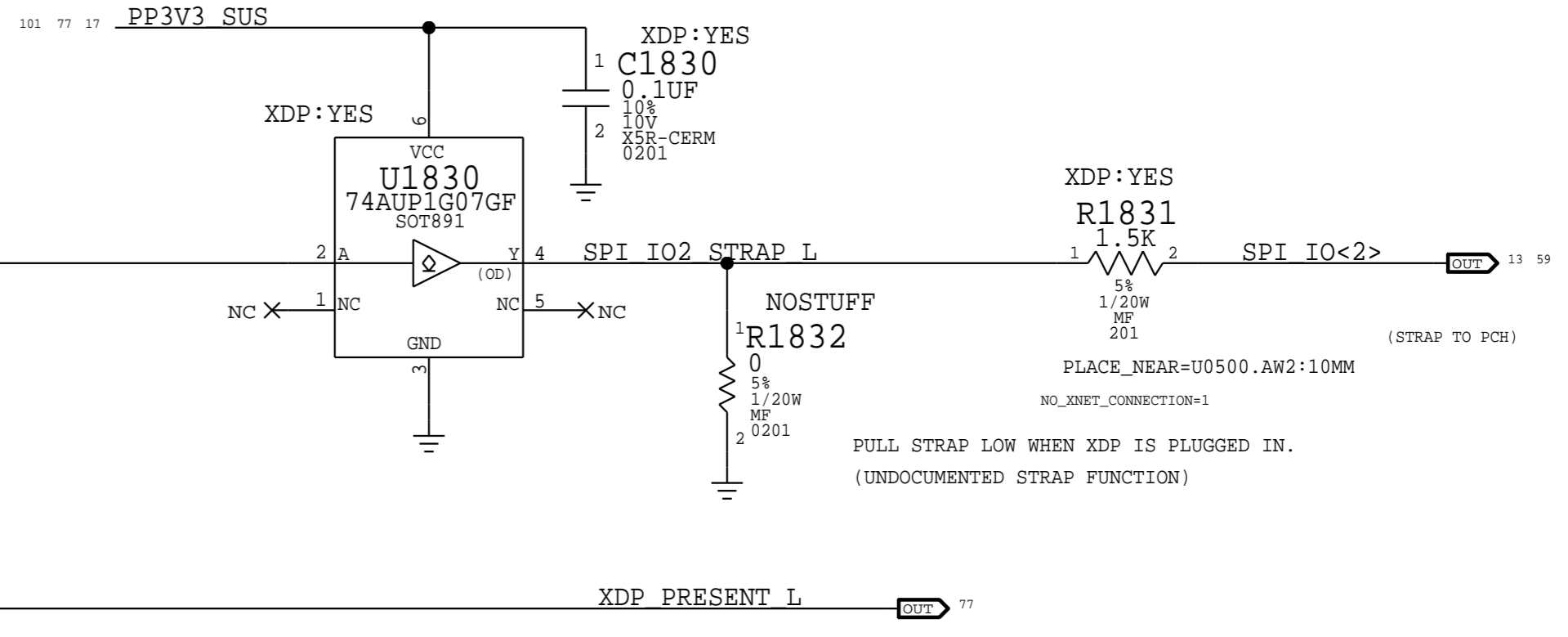
These signals do not connect to the Primary (Merged) XDP connector in this architecture. The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation. They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals

Non-XDP Signals

XDP JTAG ISP TCK	MAKE_BASE=TRUE	XDP JTAG ISP TCK	IN	105
XDP JTAG ISP TDI	MAKE_BASE=TRUE	XDP JTAG ISP TDI	IN	105
XDP PCH OBSDATA A2		TP1870	TP-P6	
XDP PCH OBSDATA A3		TP1871	TP-P6	
XDP PCH OBSDATA B0		TP1872	TP-P6	
XDP PCH OBSDATA C0		TP1873	TP-P6	
XDP PCH OBSDATA C1		TP1874	TP-P6	
XDP PCH OBSDATA C2		TP1875	TP-P6	
XDP PCH OBSDATA C3		TP1876	TP-P6	
XDP PCH OBSDATA D0		TP1877	TP-P6	
XDP PCH OBSDATA D1		TP1878	TP-P6	
XDP PCH OBSDATA D2		TP1879	TP-P6	
XDP PCH OBSDATA D3		TP1880	TP-P6	
XDP PCH OBSFN C1		TP1881	TP-P6	
XDP USB EXT A OC L	MAKE_BASE=TRUE	XDP USB EXT A OC L	IN	105
XDP USB EXT B OC L	MAKE_BASE=TRUE	XDP USB EXT B OC L	IN	105
XDP USB EXT C OC L	MAKE_BASE=TRUE	XDP USB EXT C OC L	IN	105
XDP USB EXT D OC L	MAKE_BASE=TRUE	XDP USB EXT D OC L	IN	105

Unused GPIOs have TPs.
 USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
 JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

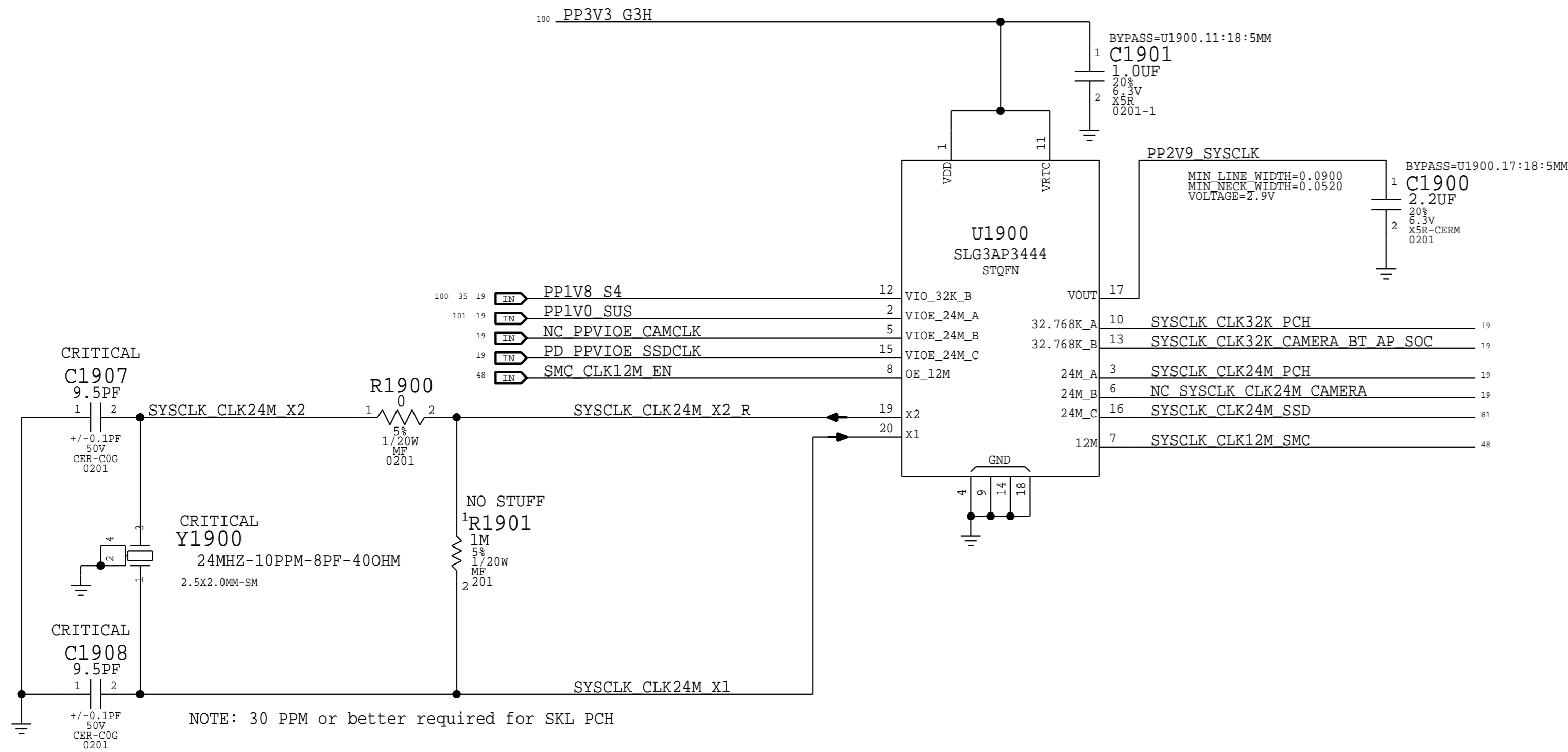


NEED TO CONNECT TO VCCST, *STG POWER LOGIC

DESIGN: X502/MLB		LAST CHANGE: Thu Oct 22 19:53:09 2015	
PAGE TITLE CPU/PCH Merged XDP			
DRAWING NUMBER 051-00515		STEP D	
REVISION 9.0.0		BRANCH dvt-fab09-0	
PAGE 18 OF 145		SHEET 17 OF 119	
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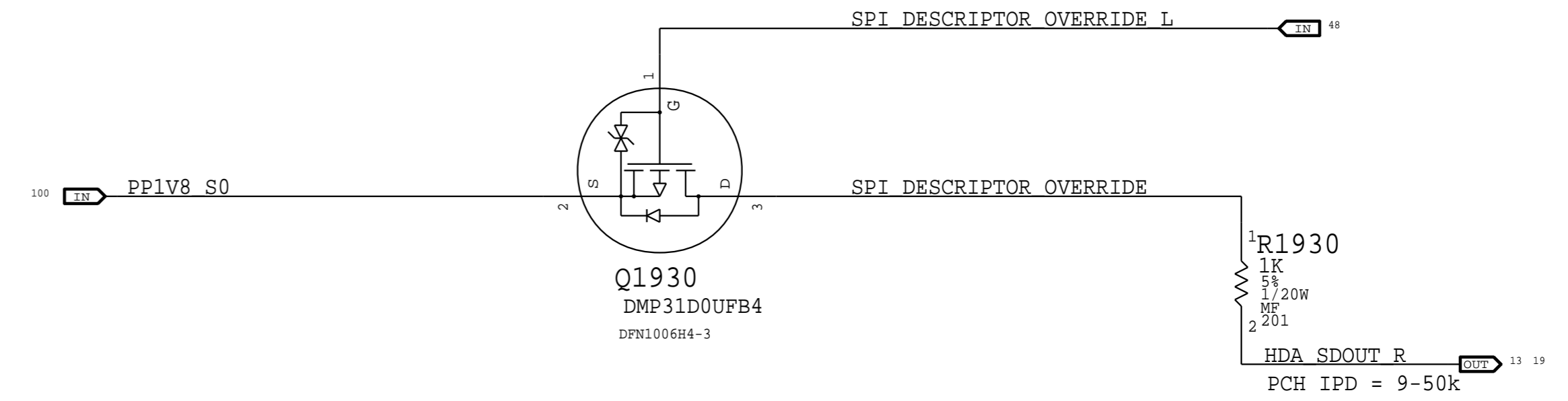
BOM_COST_GROUP=DEBUG

System 32kHz / 12MHz / 24MHz Clock Generator



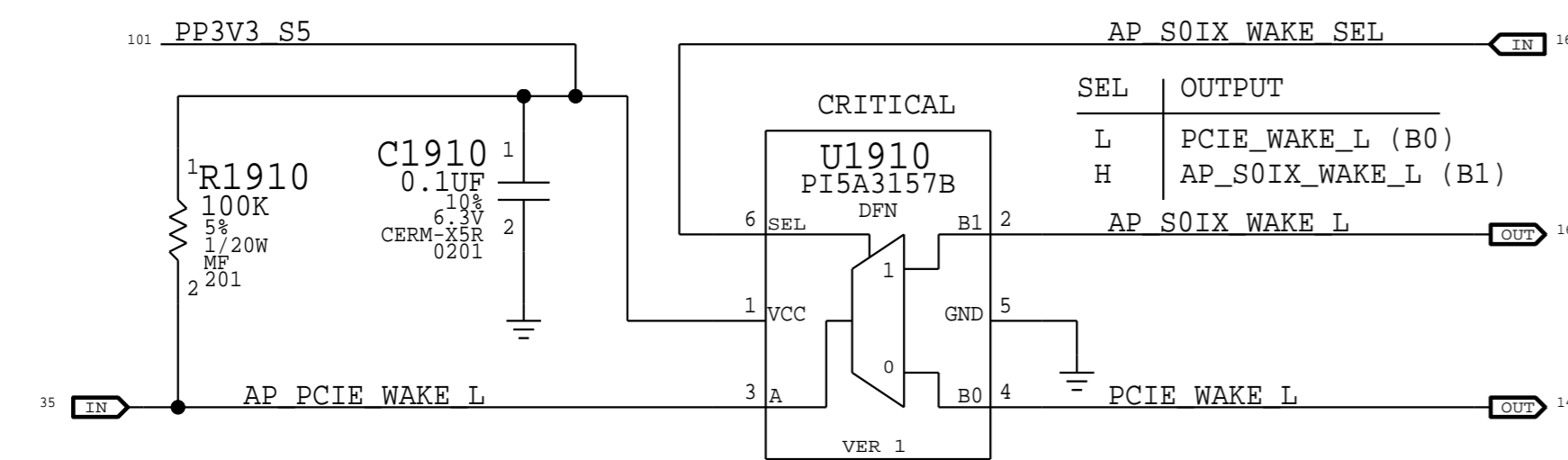
NOTE: 30 PPM or better required for SKL PCH

PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. ***** Circuit does not support HDA voltage >3.3V.

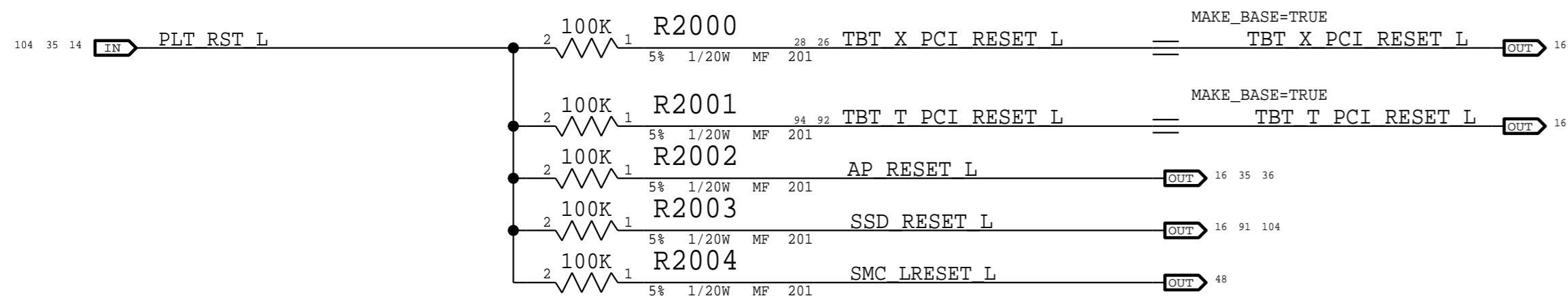
PCIe Wake Muxing



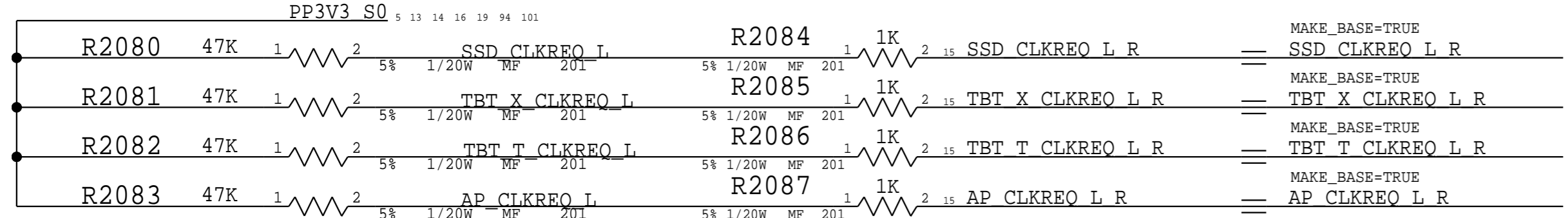
PAGE TITLE Chipset Support 1		
Apple Inc.	DRAWING NUMBER 051-00515	SIZE D
	REVISION 9.0.0	
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	PAGE 19 OF 145	
	SHEET 18 OF 119	

Platform Reset Connections

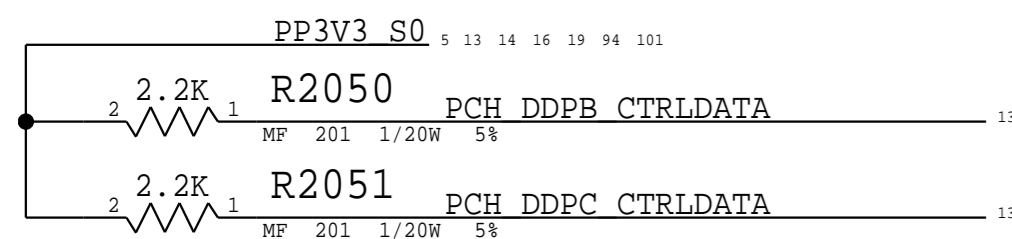
Unbuffered



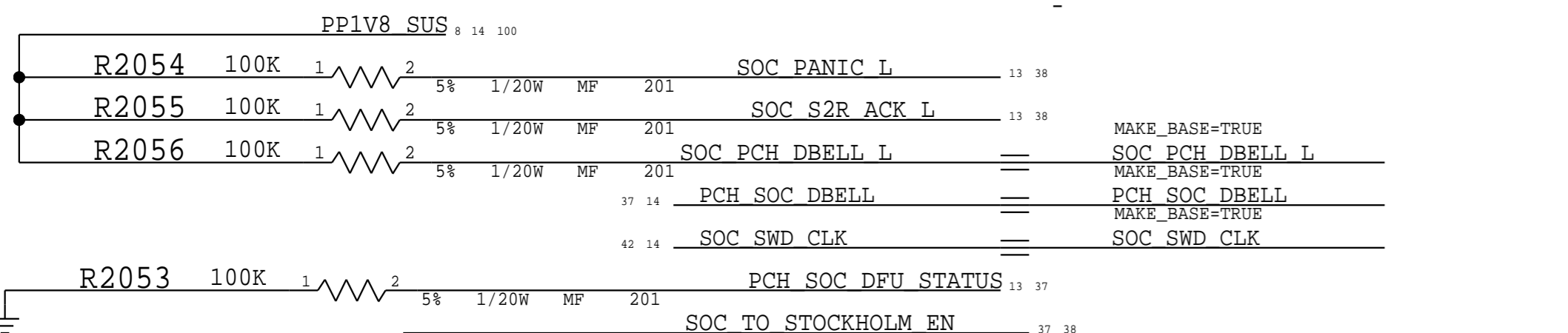
PCIE CLKREQS



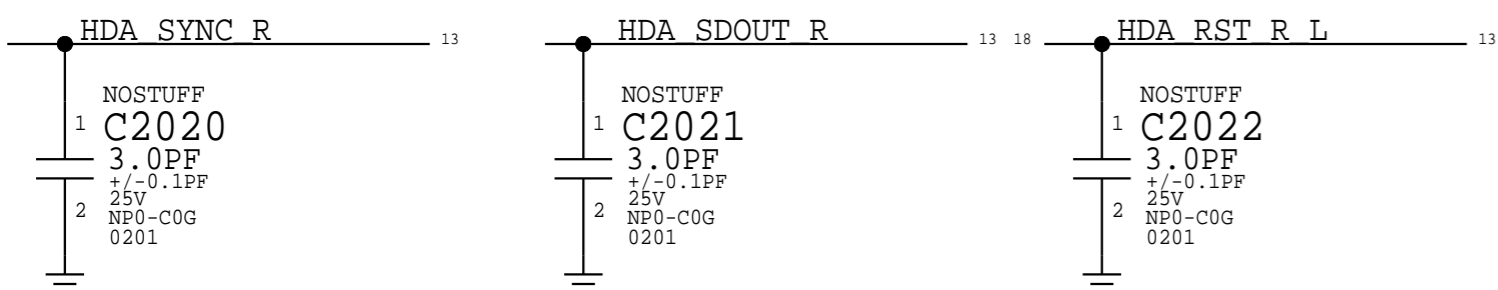
ENABLE DDPB DDPD INTERFACES



T208 PCH GPIO PUs/PDs & ALIASES

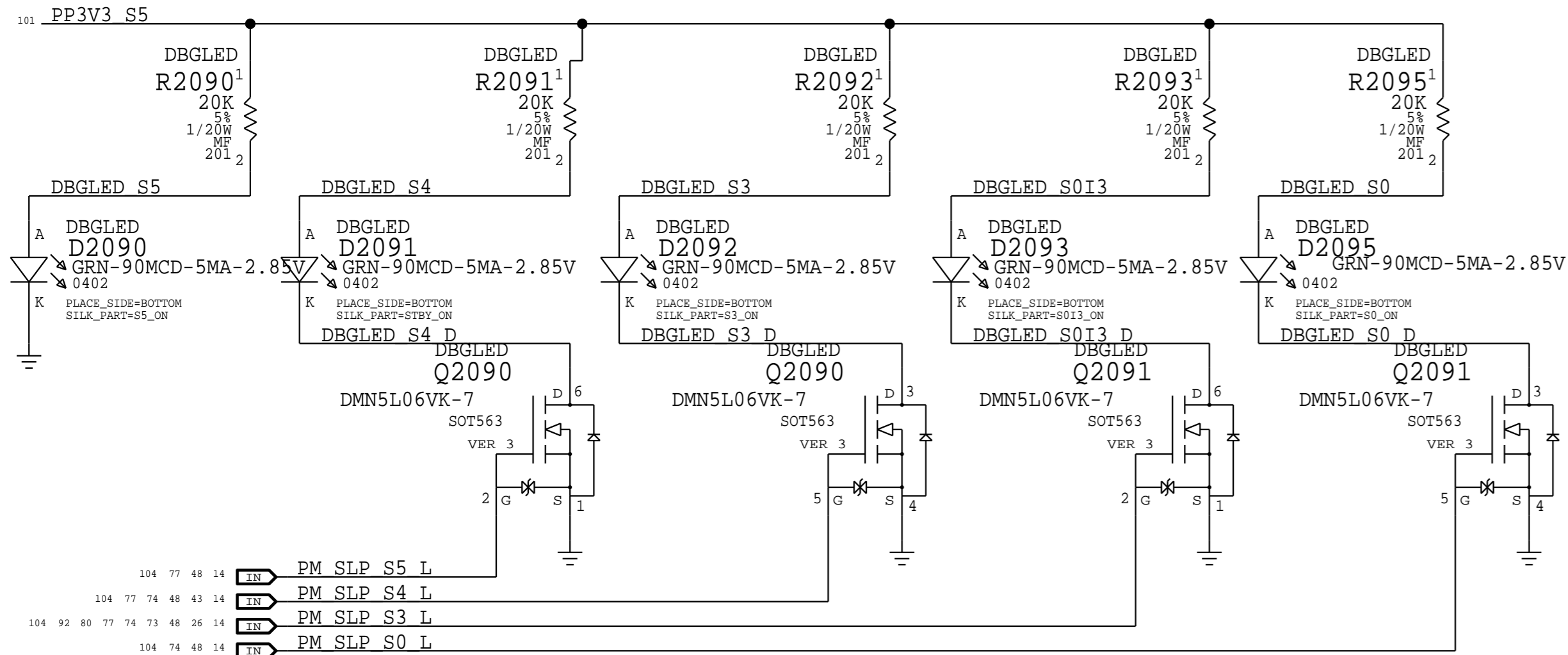


Desense Decoupling Caps on HDA Lines

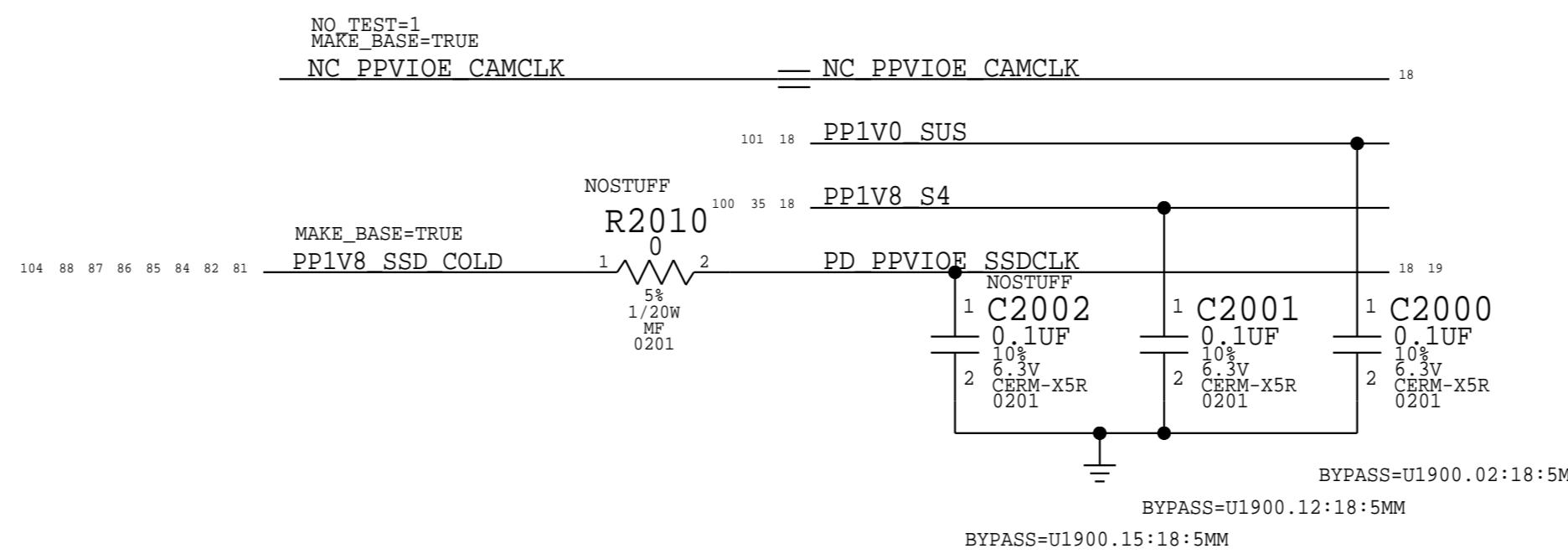


Power State Debug LEDs

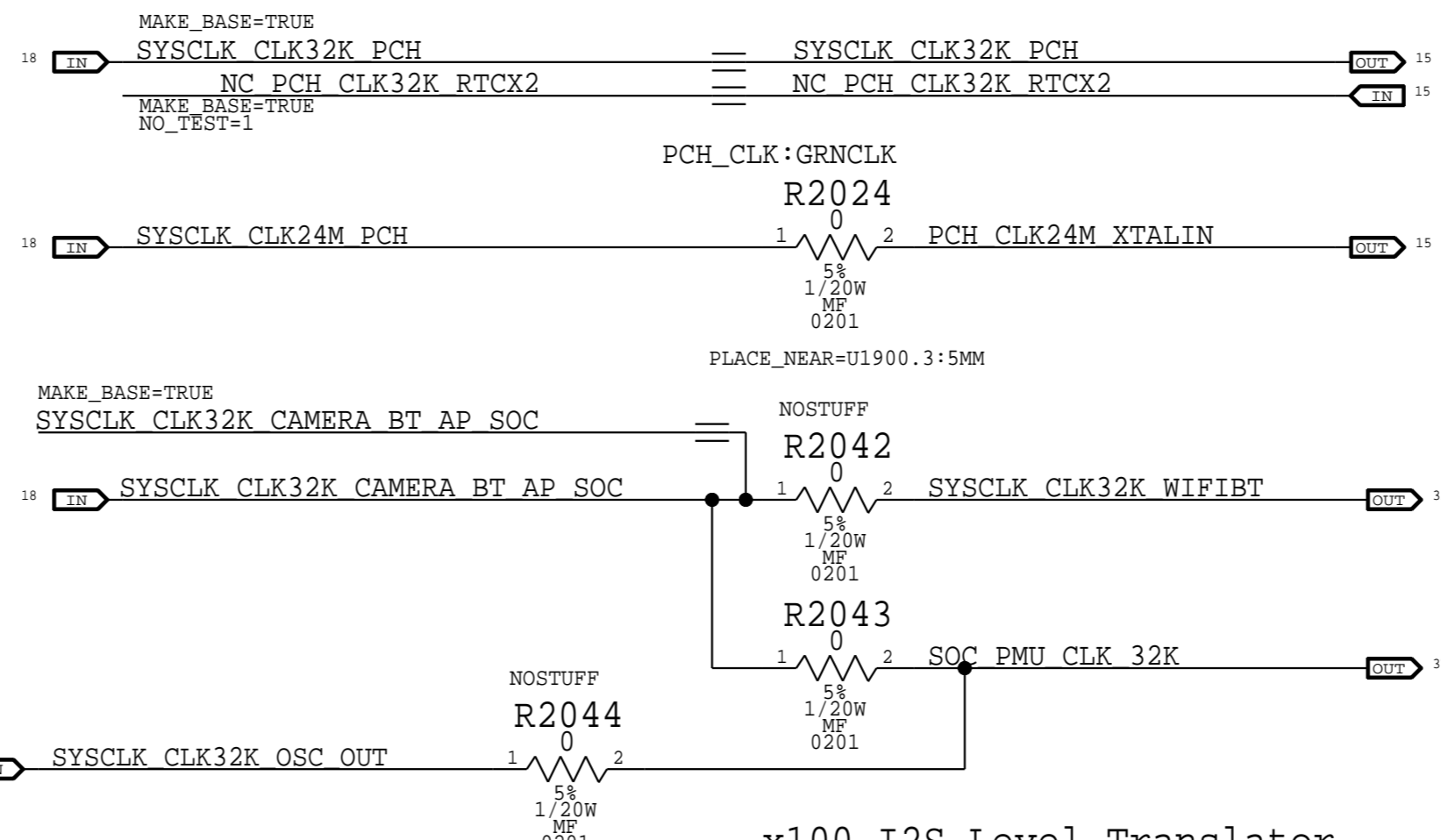
(For development only)



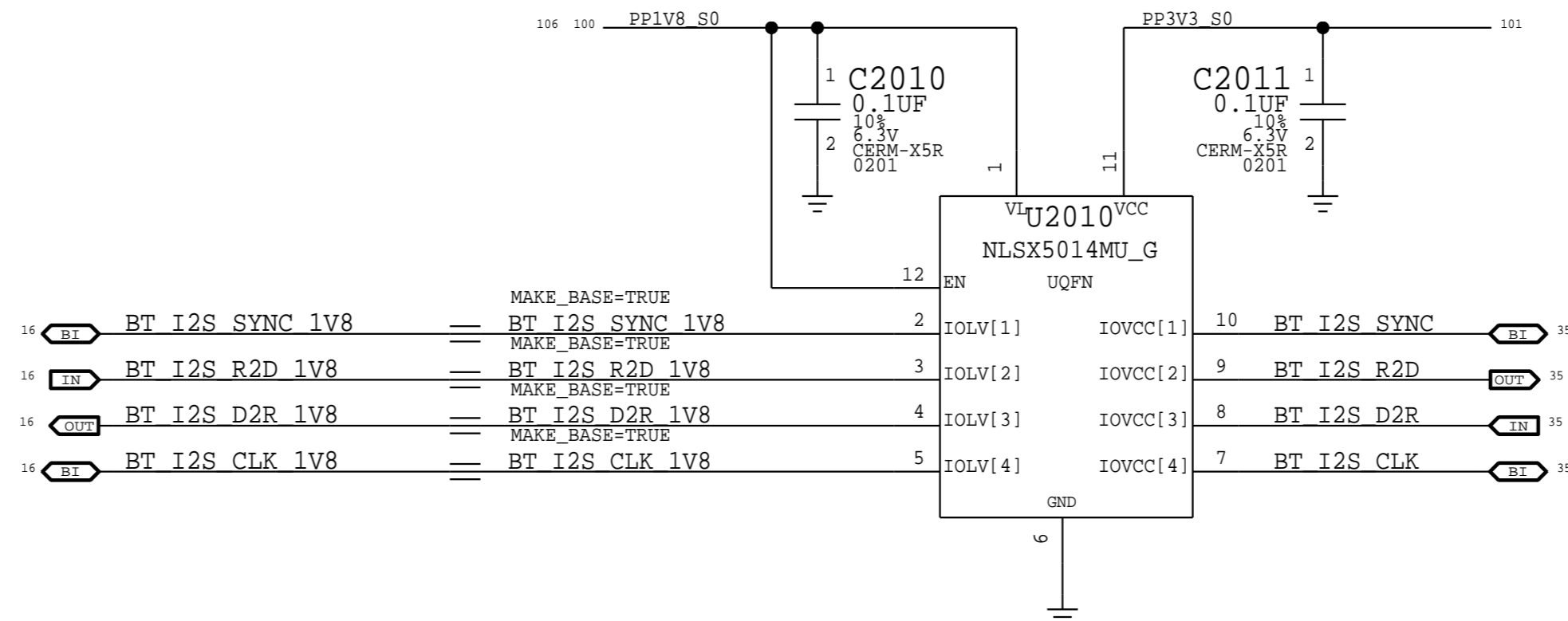
GREENCLK VIOEs



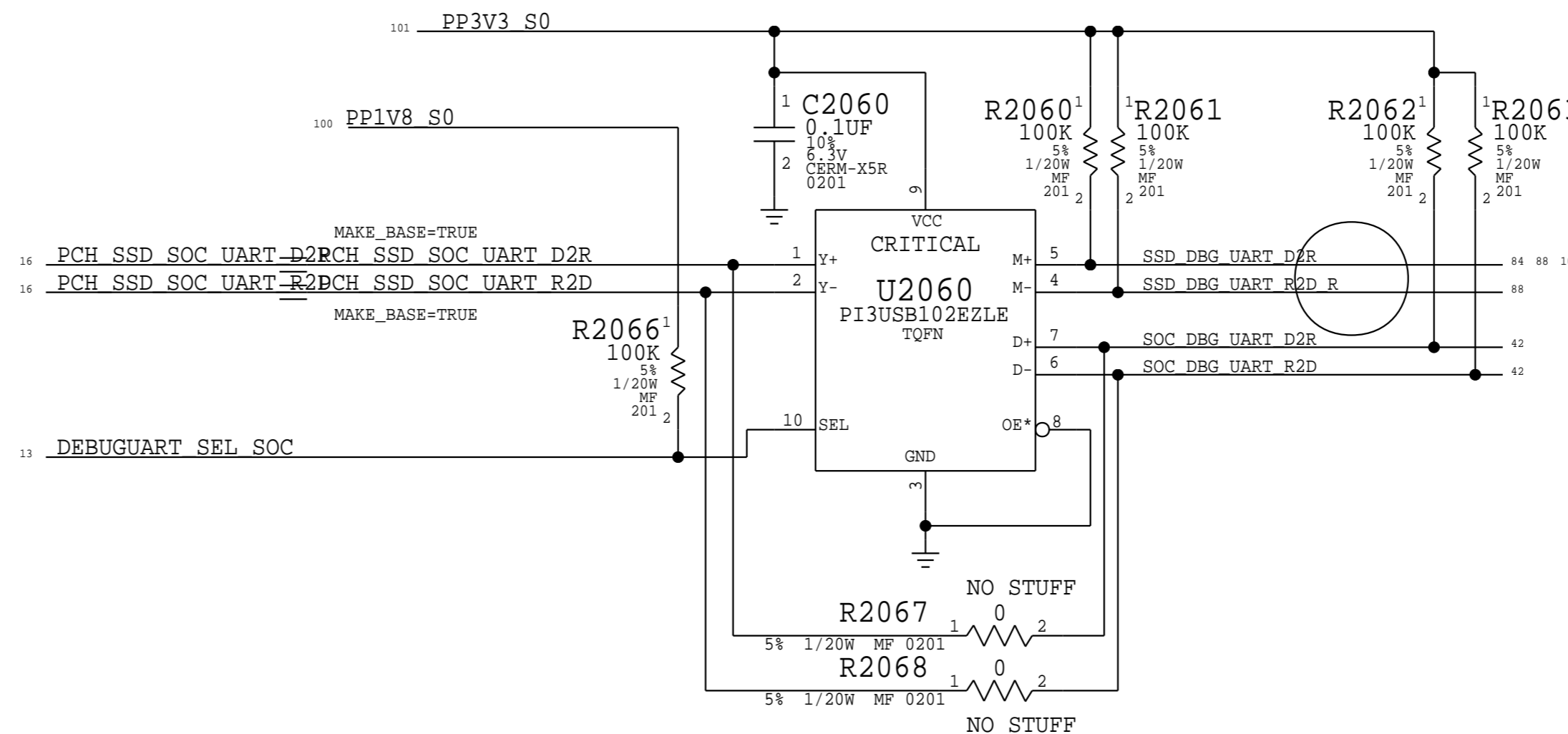
GREENCLK CLOCK OUT ALIASES



x100 I2S Level Translator

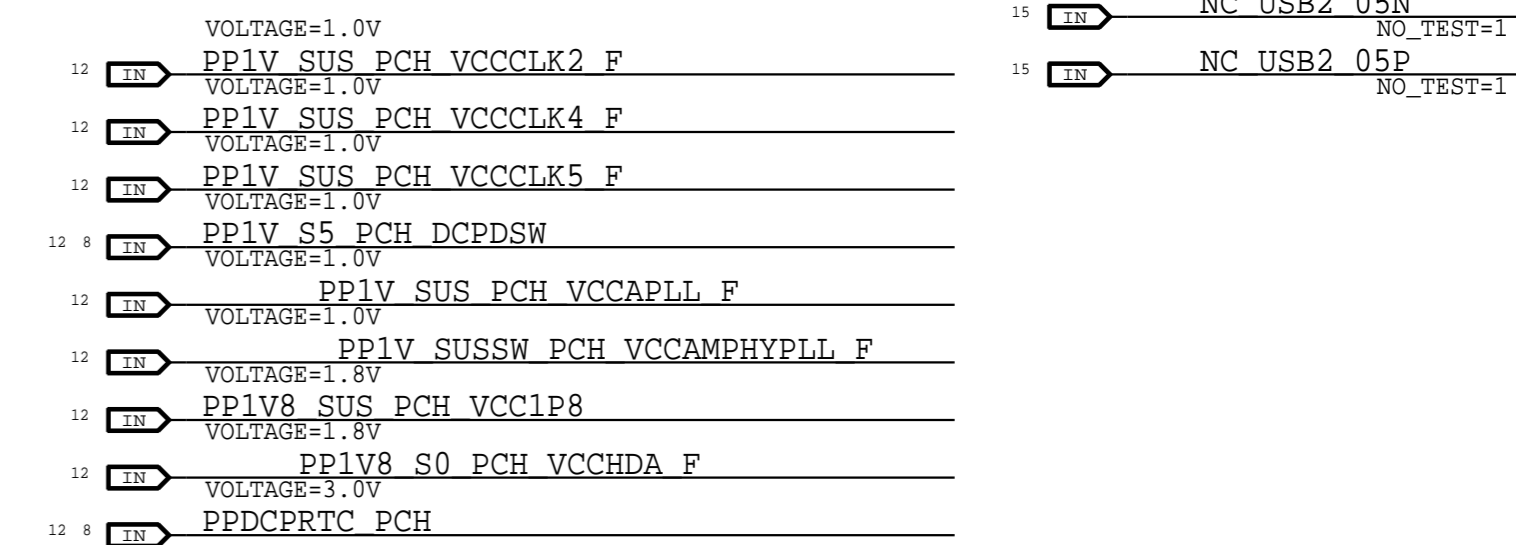


BT/SSD DEBUG UART MUX

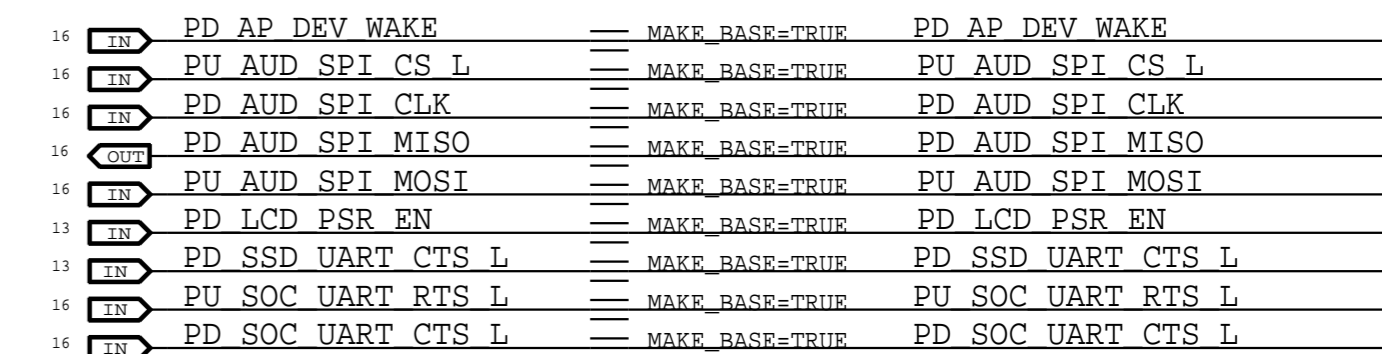


NO TEST

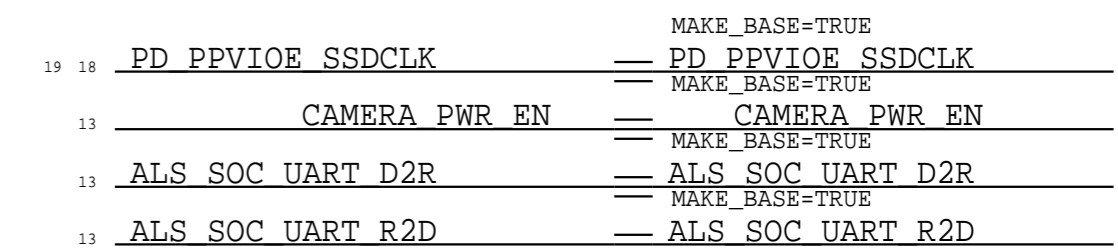
Voltage Props



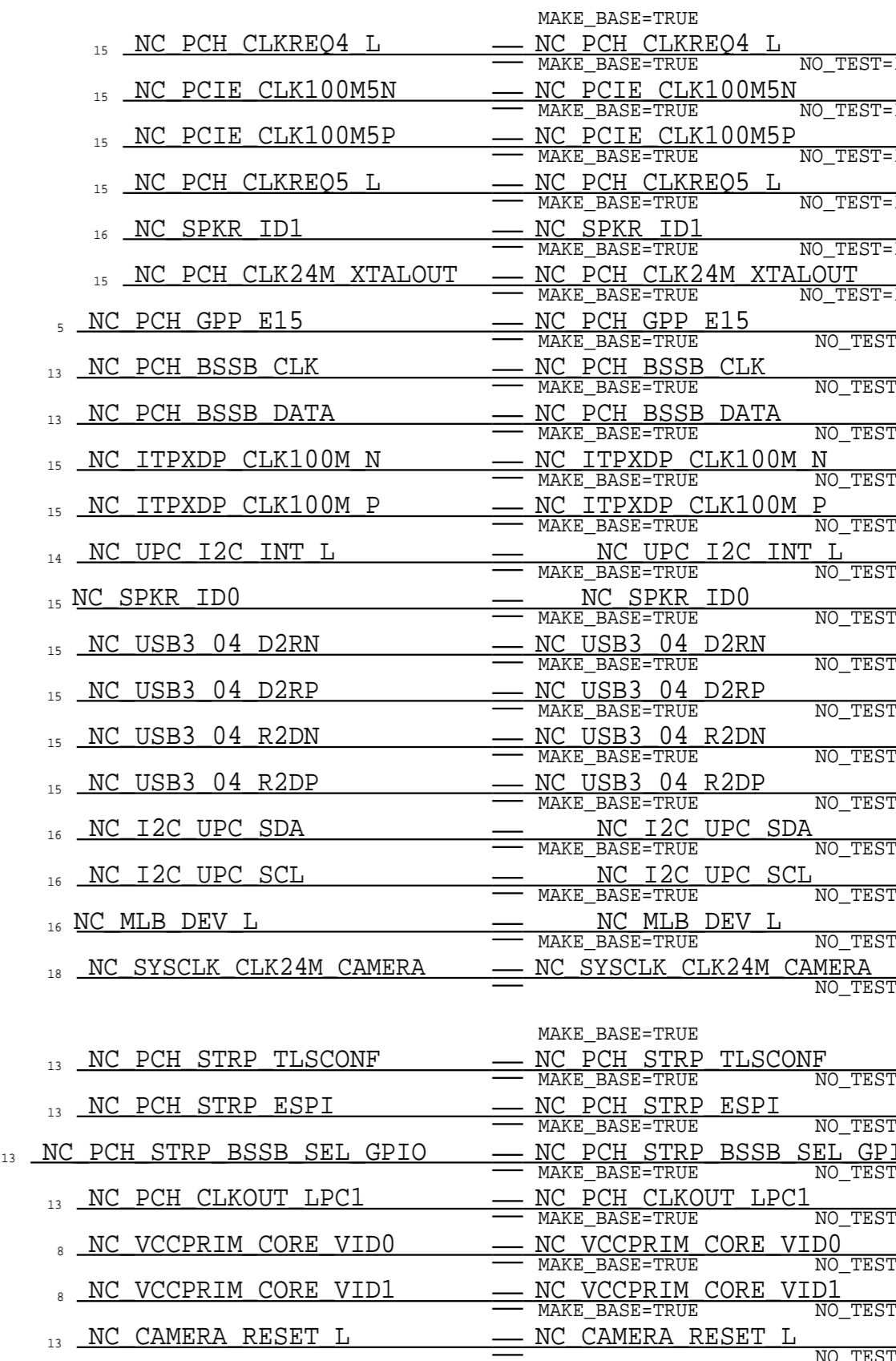
Unused GPIOs with PUs/PDs



SIGNAL ALIASES

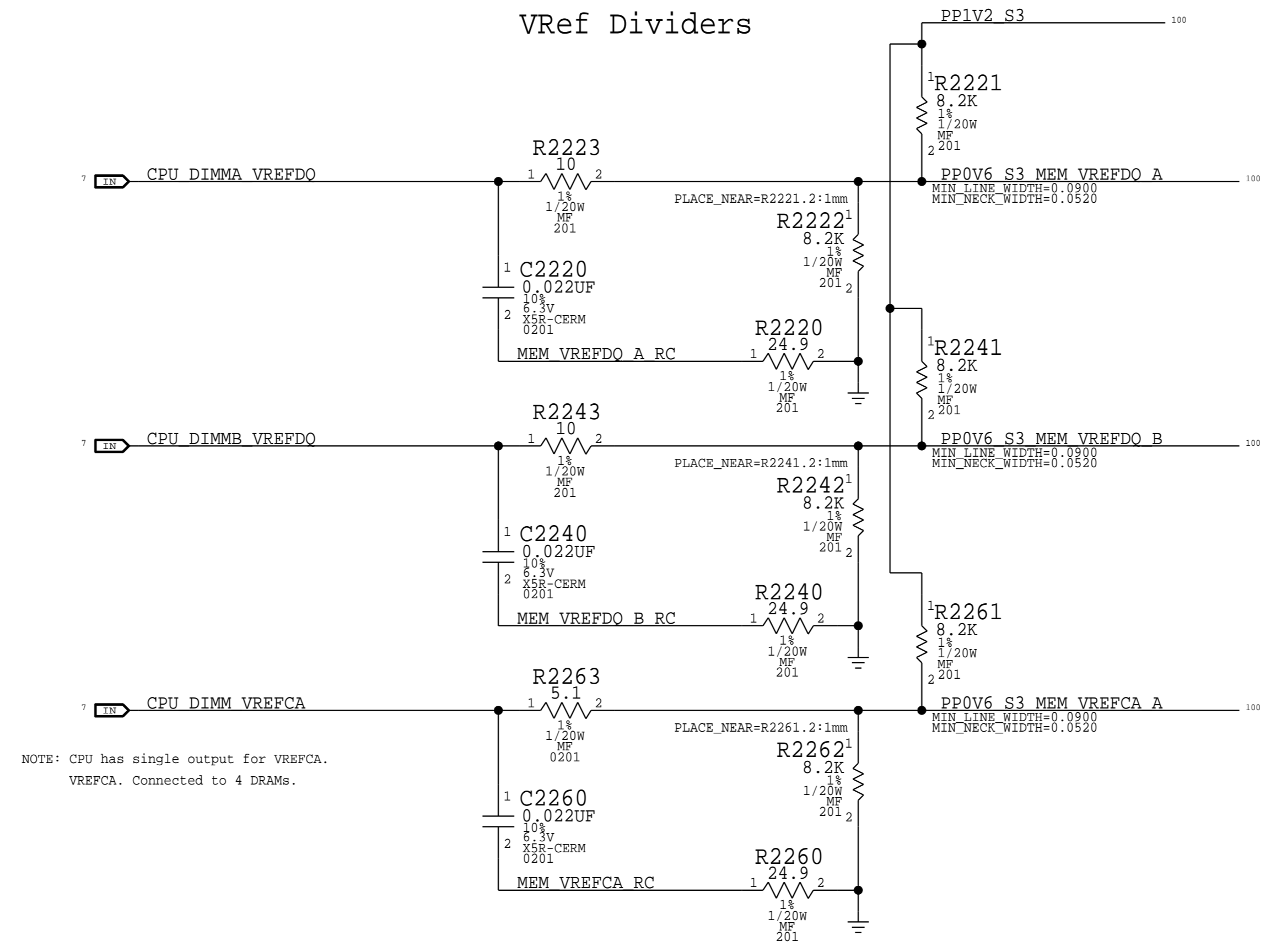


NC SIGNAL ALIASES



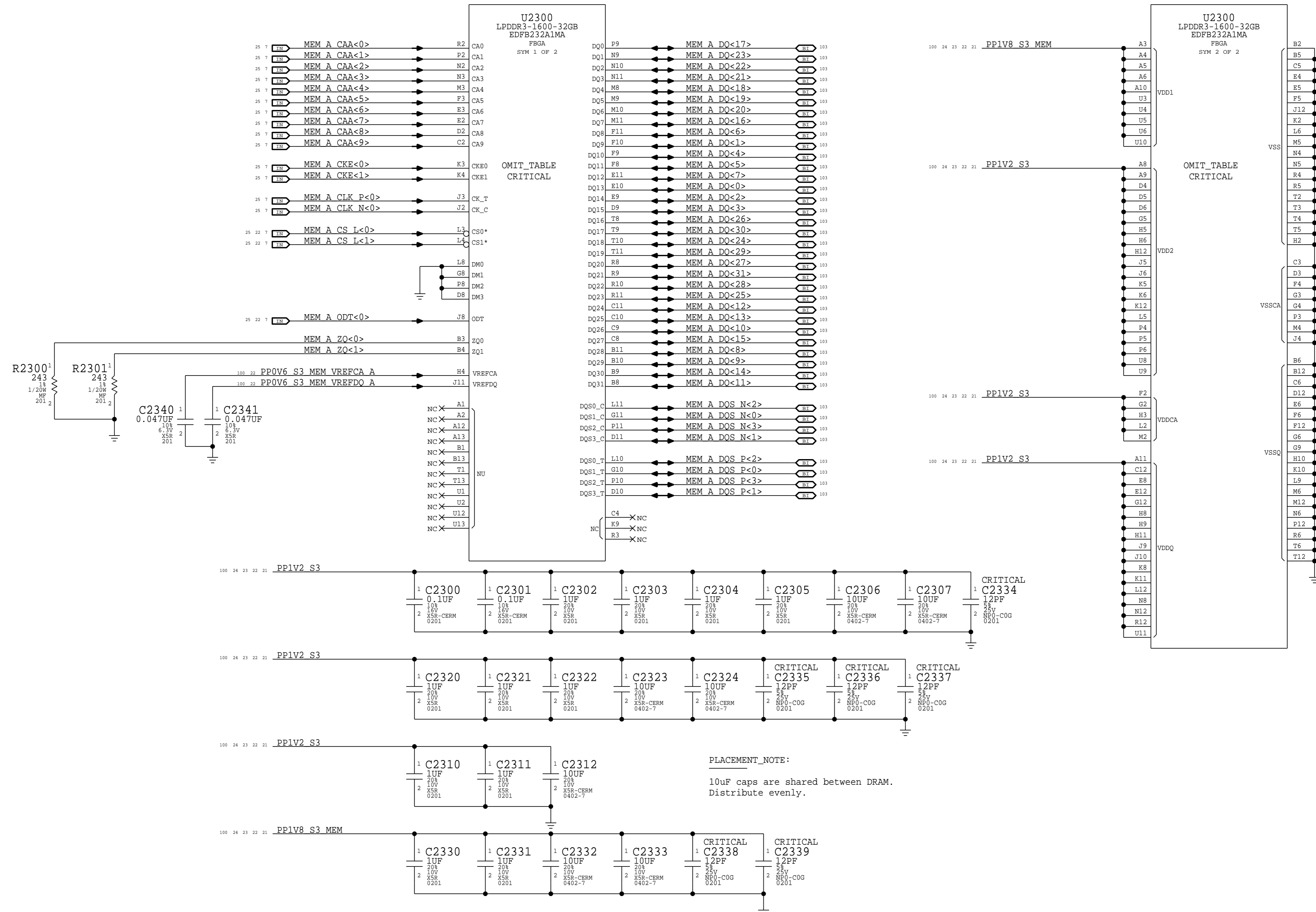
Chipset Support 2
Apple Inc.
DRAWING NUMBER: 051-00515
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 20 OF 145
SHEET: 19 OF 119

CPU-Based Margining



SYNC_MASTER=352_MLB		SYNC_DATE=05/12/2015	
PAGE TITLE			
LPDDR3 VREF Margining			
	DRAWING NUMBER	051-00515	SIZE
	REVISION	9.0.0	D
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		PAGE	22 OF 145
		SHEET	20 OF 119

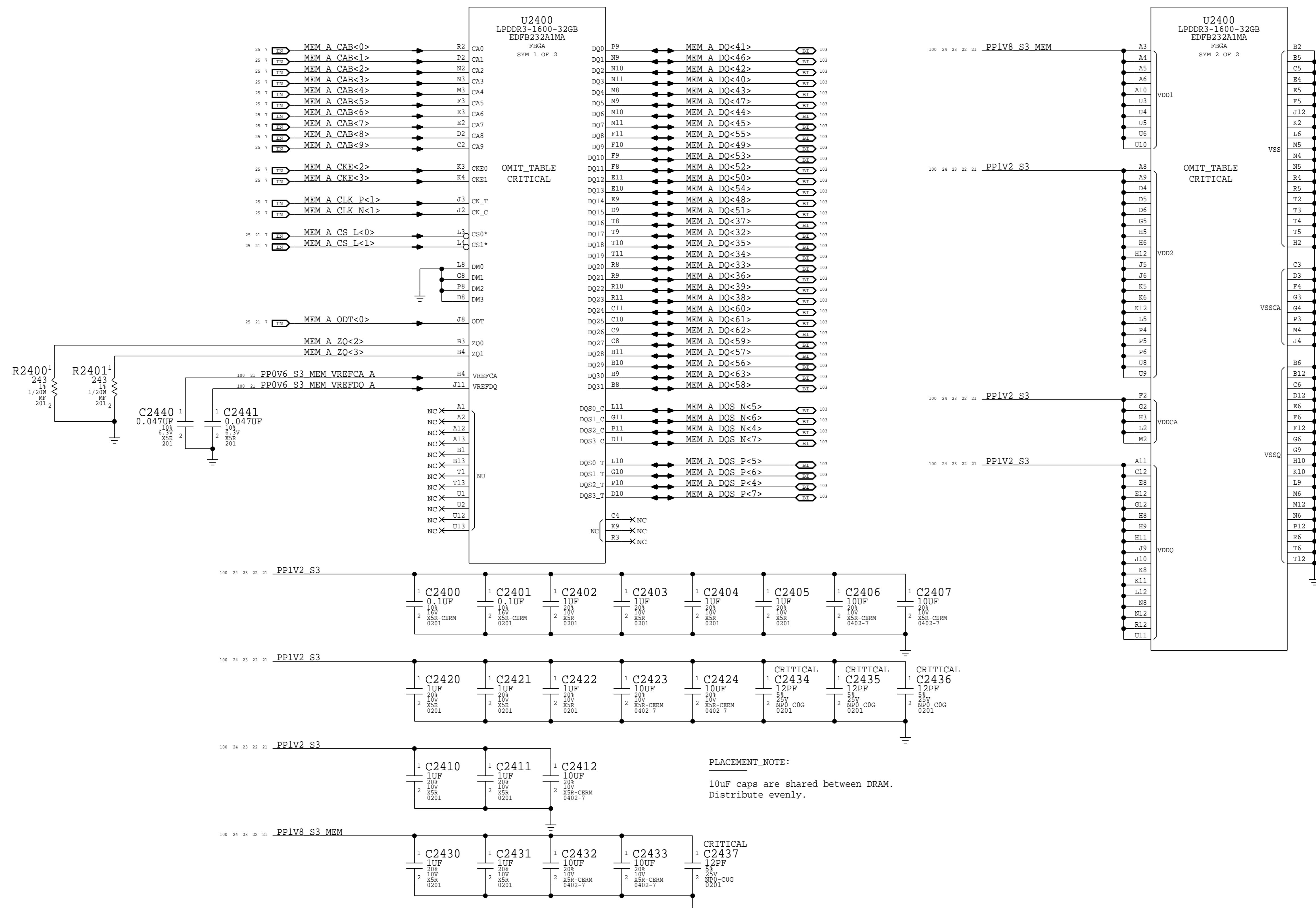
LPDDR3 CHANNEL A (0-31)



BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB		SYNC_DATE=05/12/2015	
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		DRAWING NUMBER	051-00515
		REVISION	9.0.0
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		PAGE	23 OF 145
		SHEET	21 OF 119

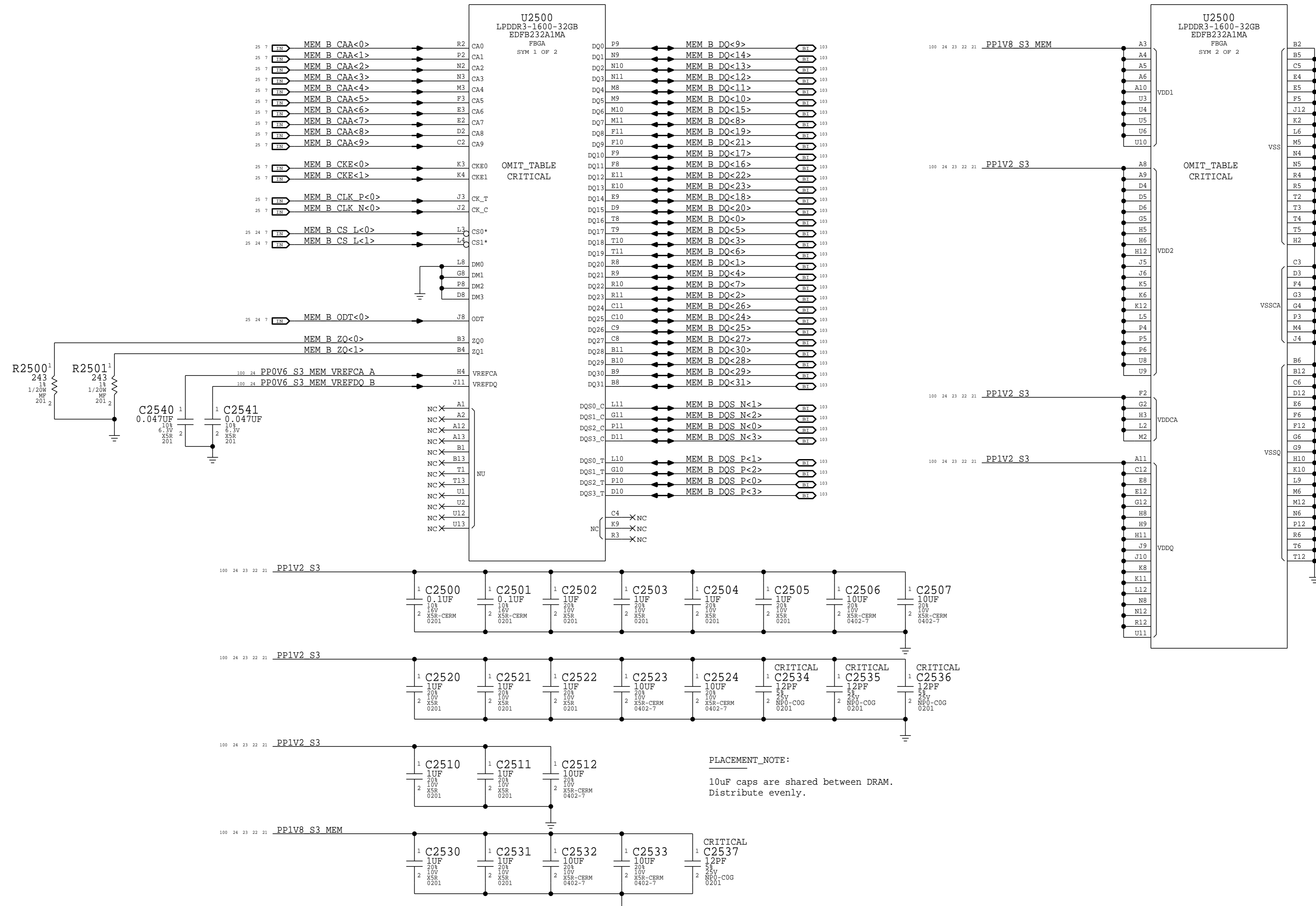
LPDDR3 CHANNEL A (32-63)



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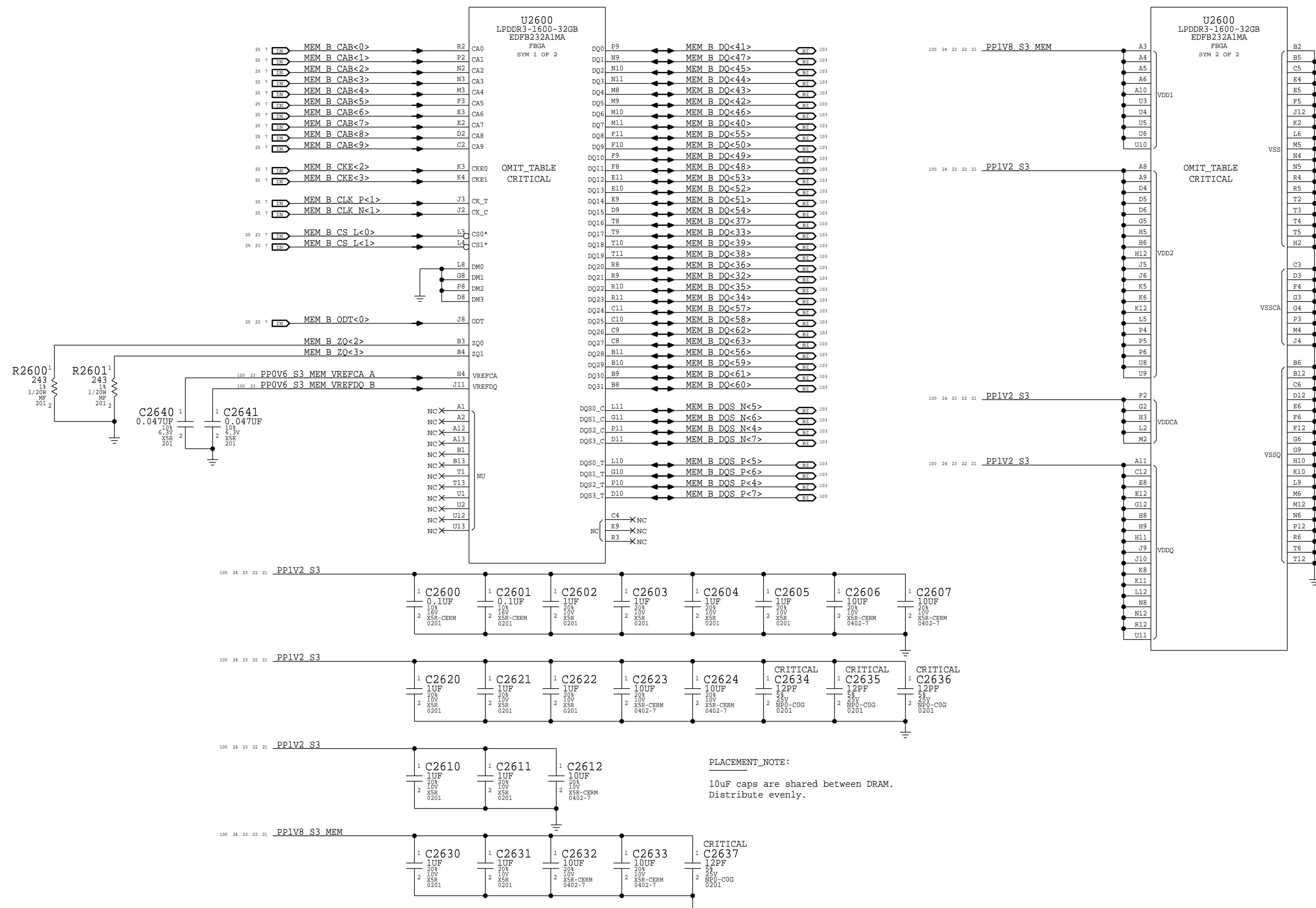
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PAGE TITLE			
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	DRAWING NUMBER	051-00515	STEP
	REVISION	9.0.0	D
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		SHEET	22 OF 119

LPDDR3 CHANNEL B (0-31)



SYNC_MASTER=J52_MLB		SYNC_DATE=05/12/2015	
PAGE TITLE			
LPDDR3 DRAM Channel B (00-31)			
	DRAWING NUMBER	051-00515	STEP
	REVISION	9.0.0	D
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		PAGE	25 OF 145
		SHEET	23 OF 119

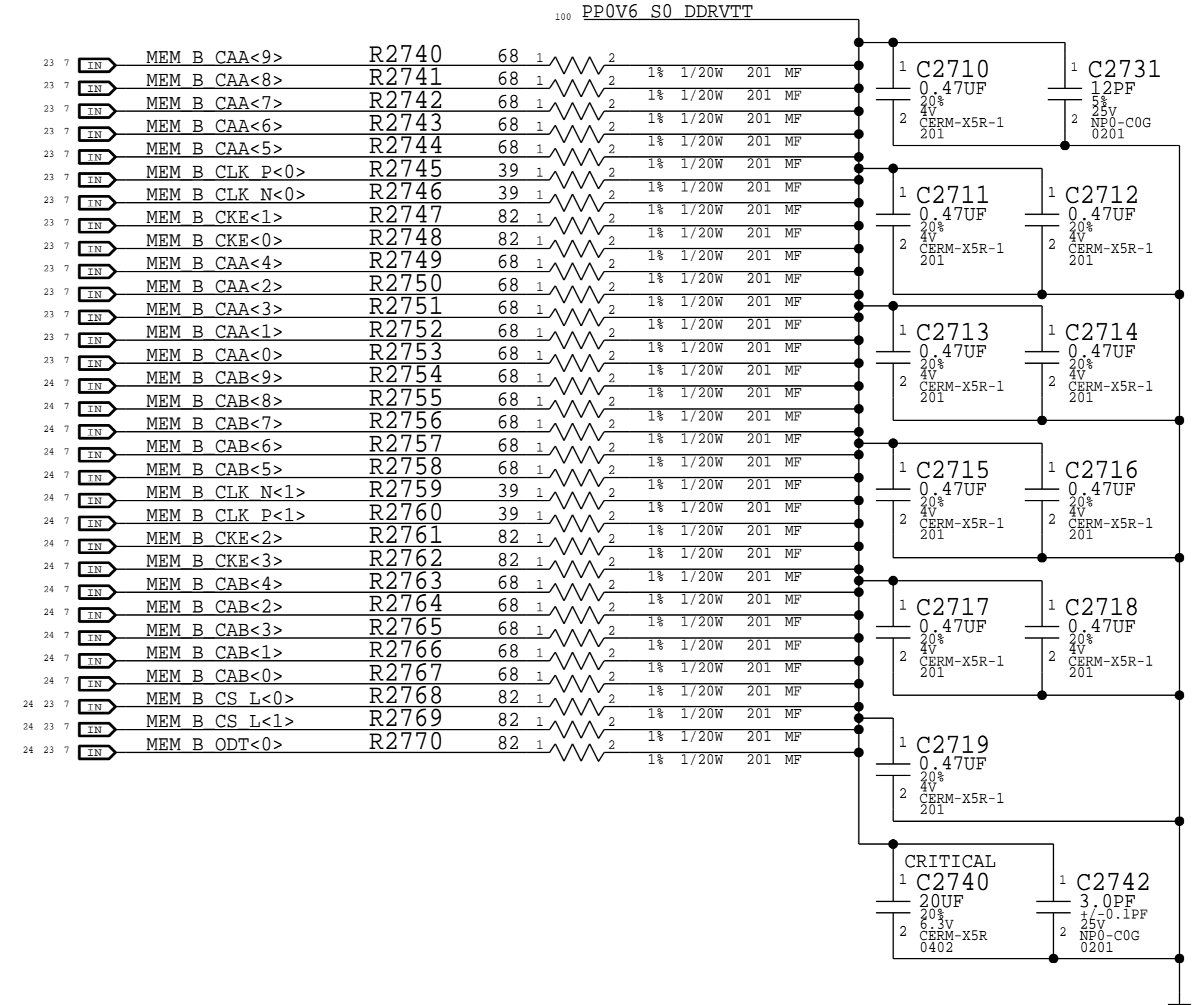
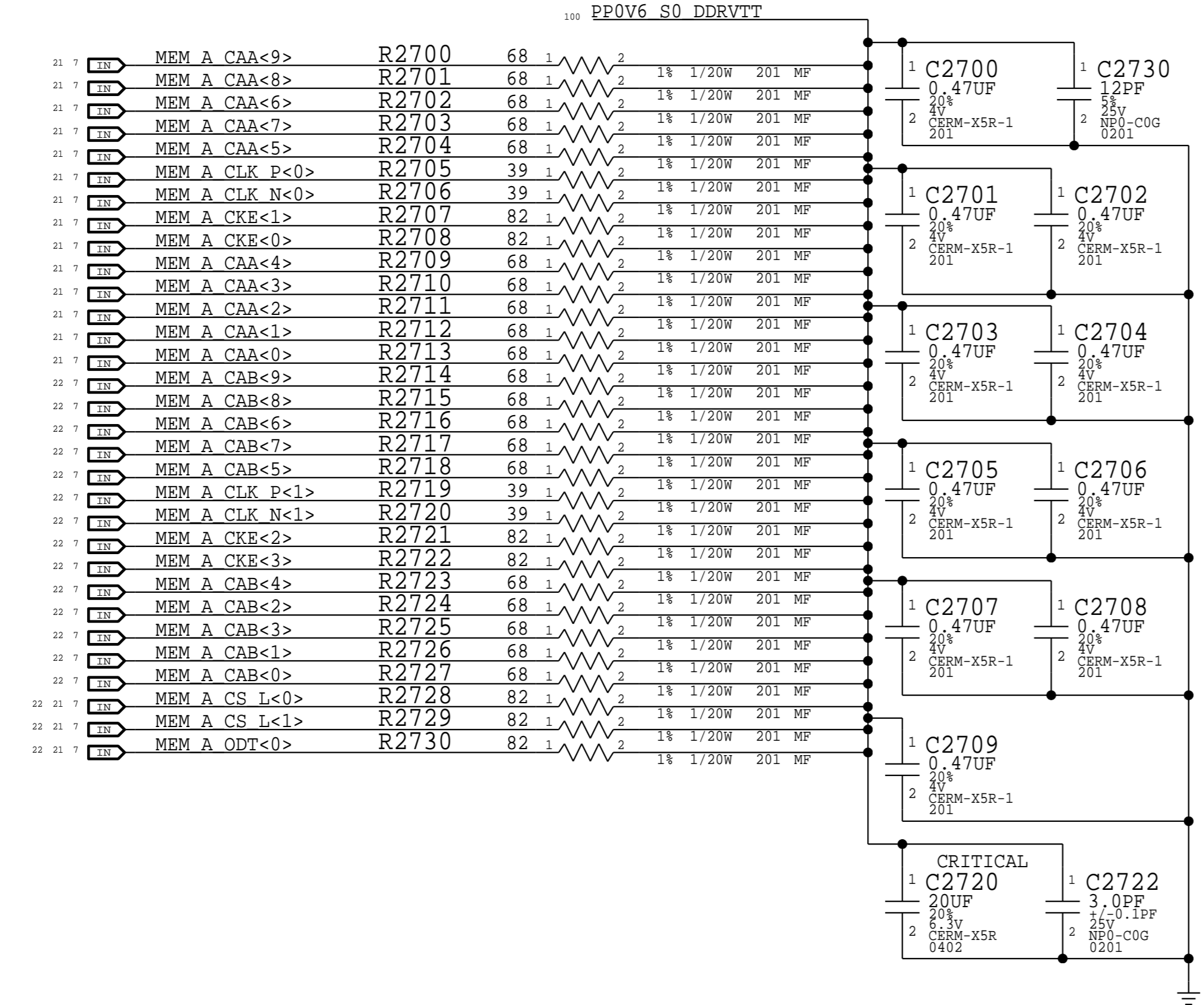
LPDDR3 CHANNEL B (32-63)



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	DRAWING NUMBER	051-00515	STEP
	REVISION	9.0.0	D
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		PAGE	26 OF 145
		SHEET	24 OF 119

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK



BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB		SYNC_DATE=05/12/2015	
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LPDDR3 DRAM Termination			
	DRAWING NUMBER	051-00515	SIZE
	REVISION	9.0.0	D
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		PAGE	27 OF 145
		SHEET	25 OF 119

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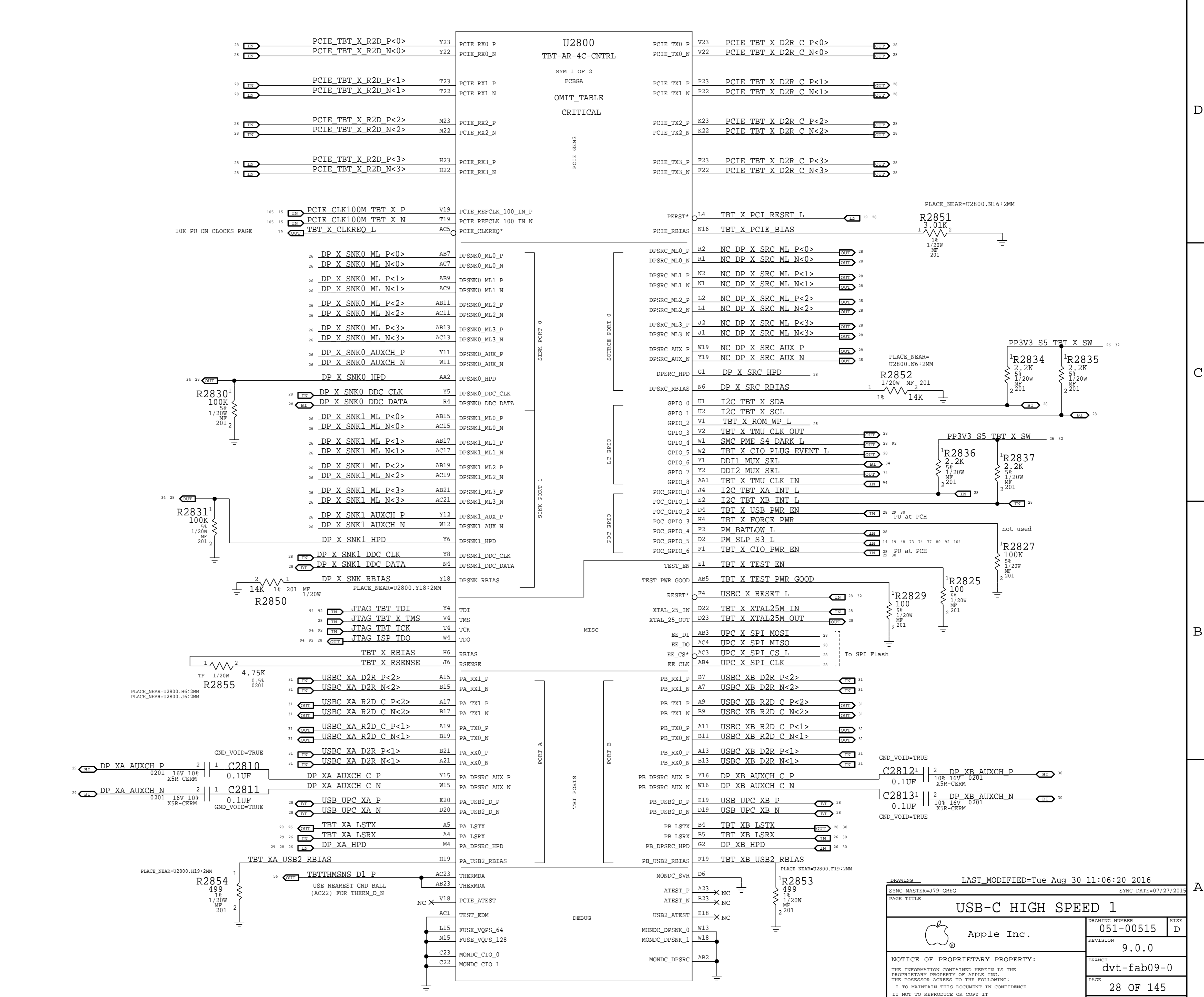
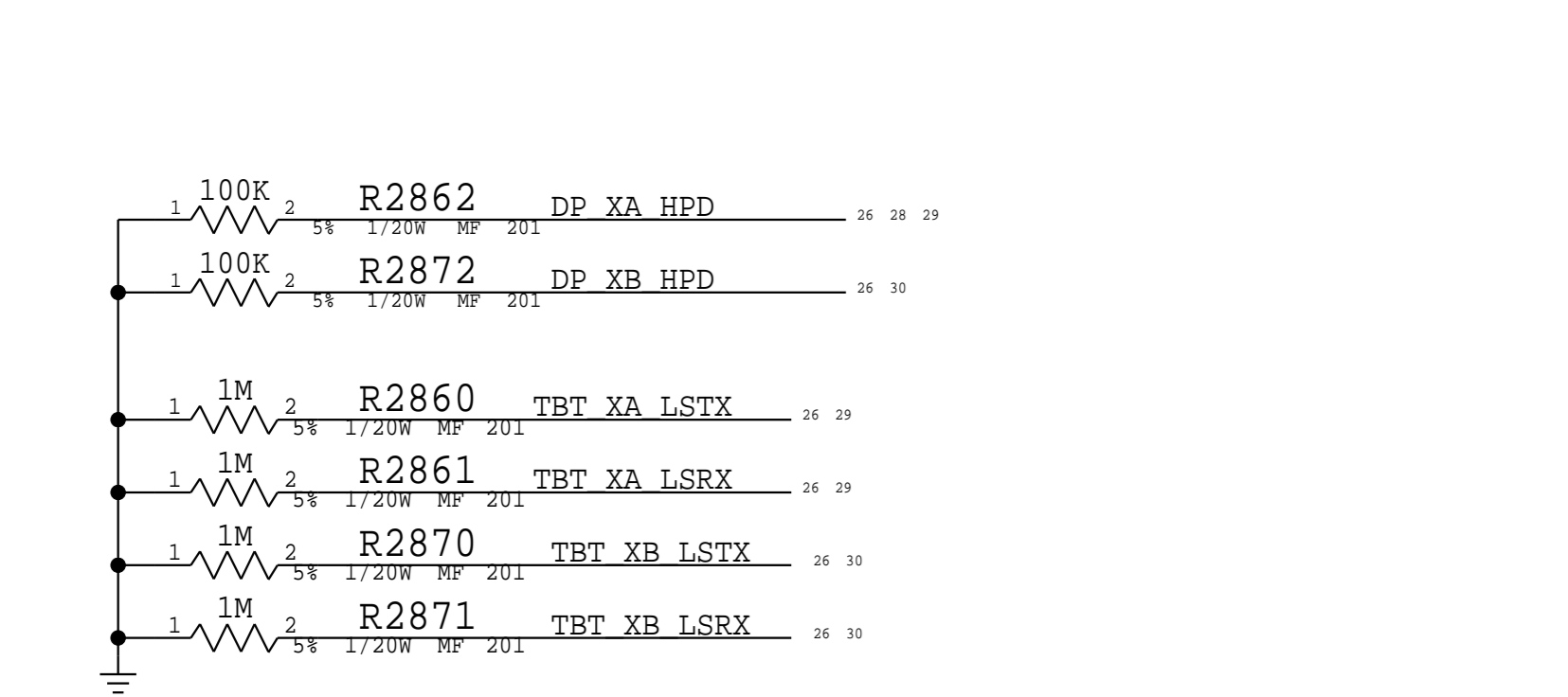
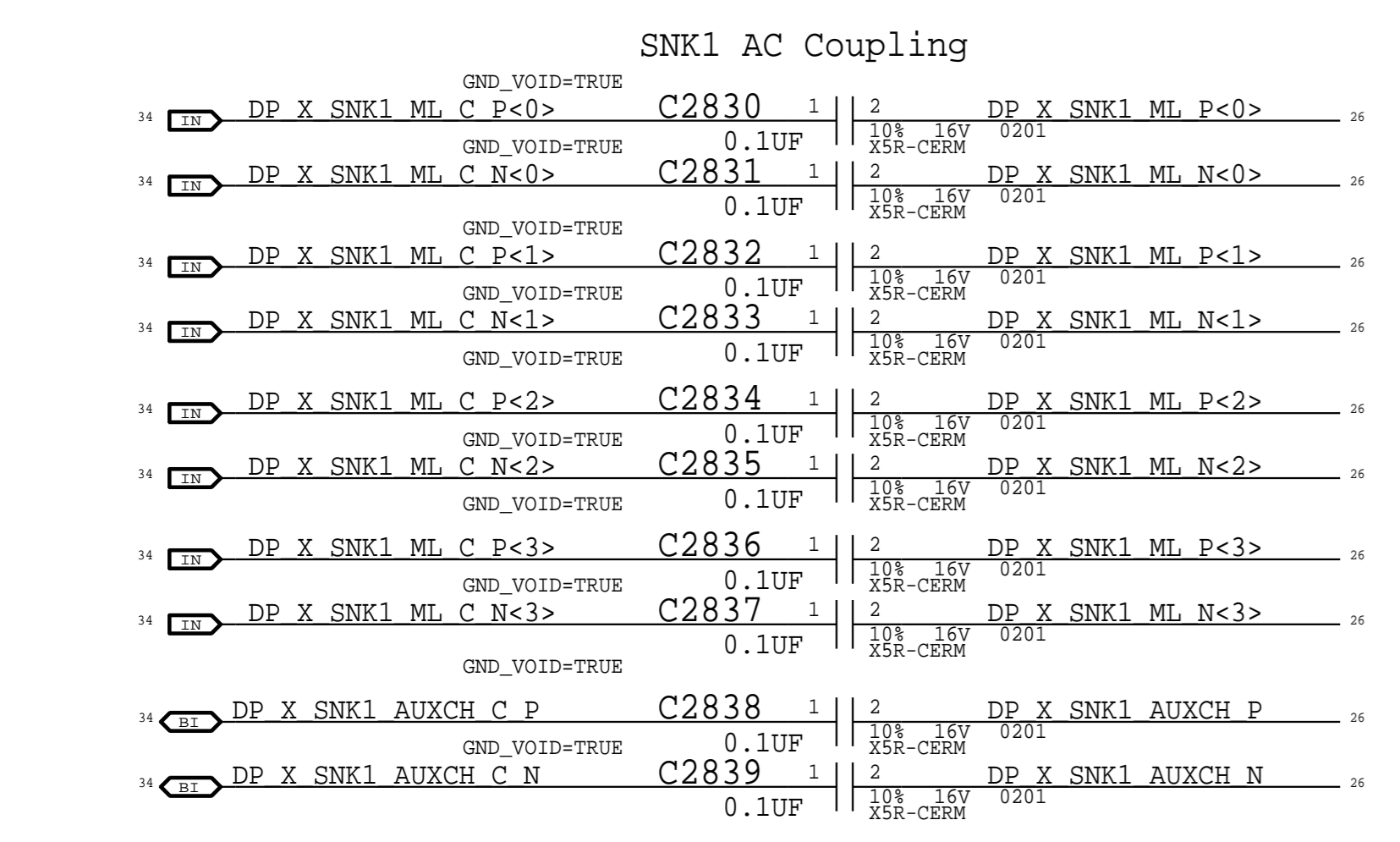
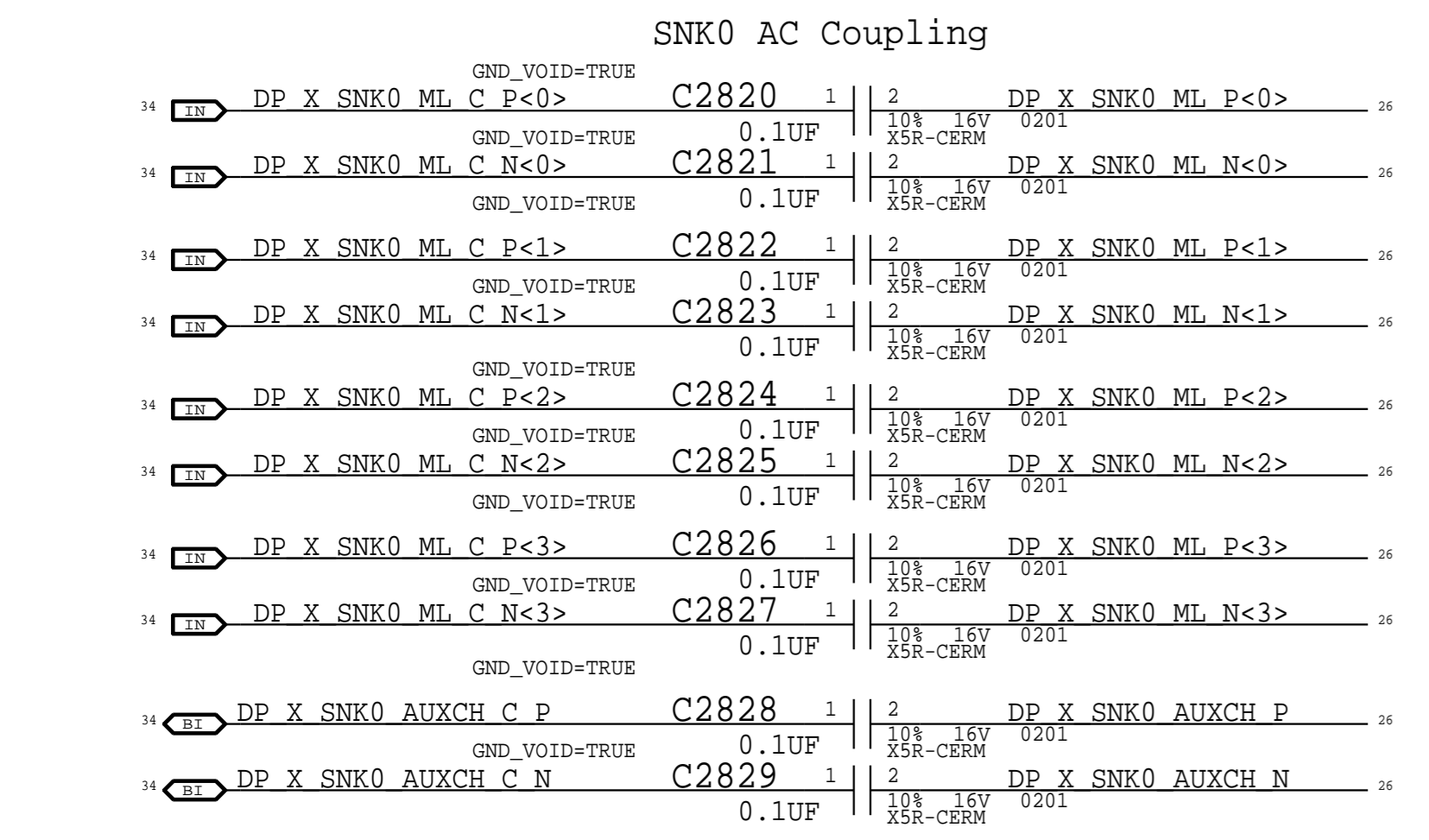
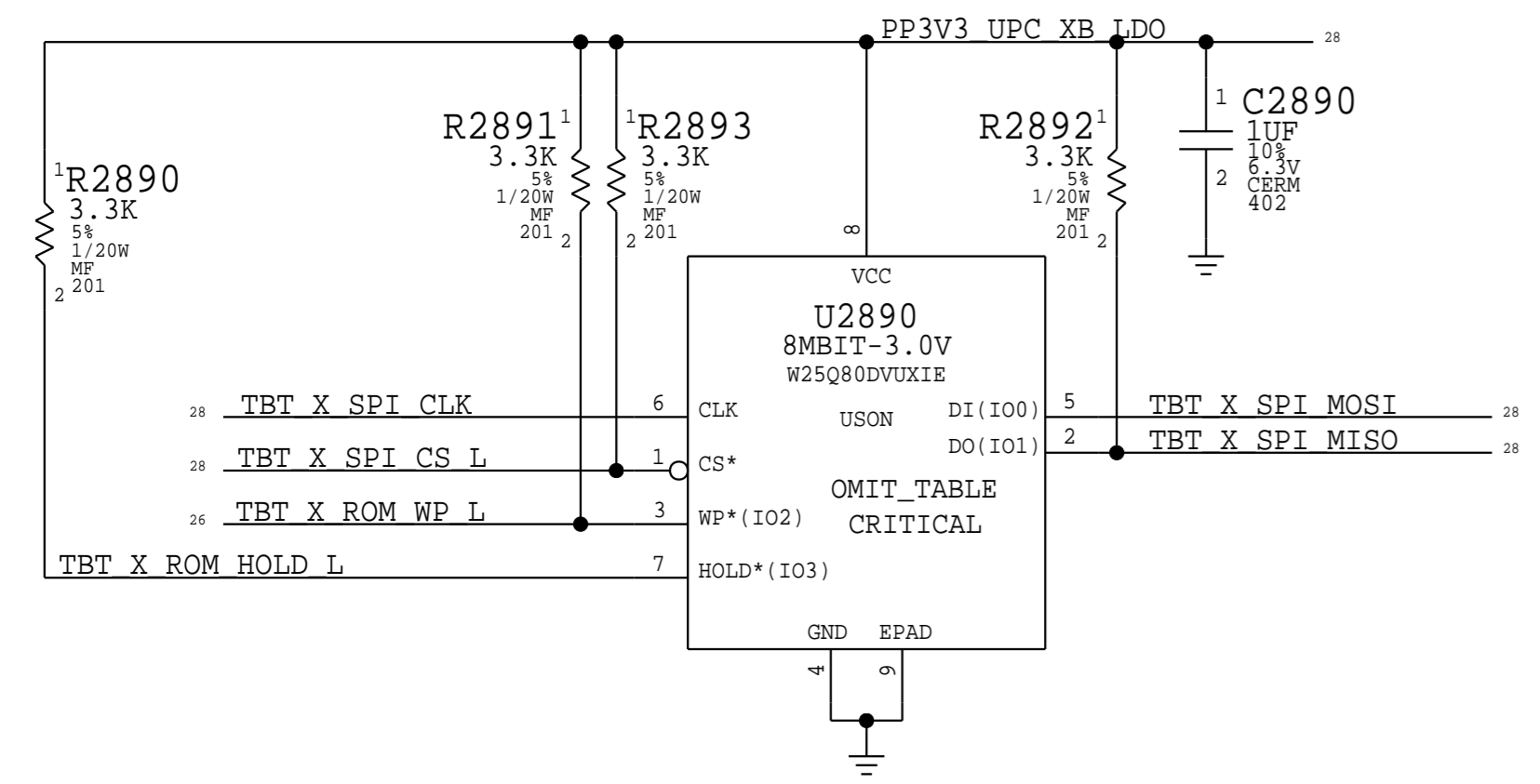
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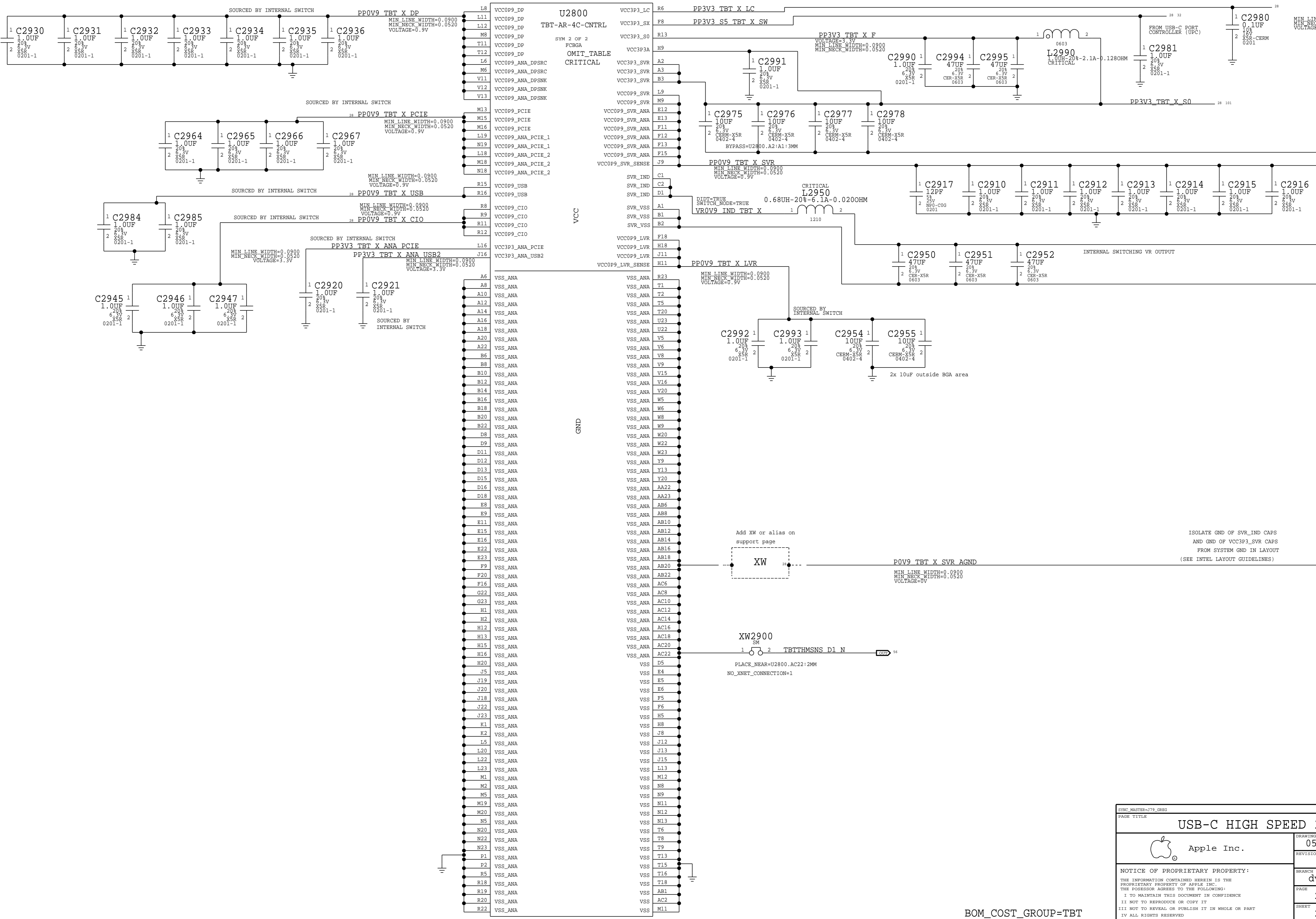
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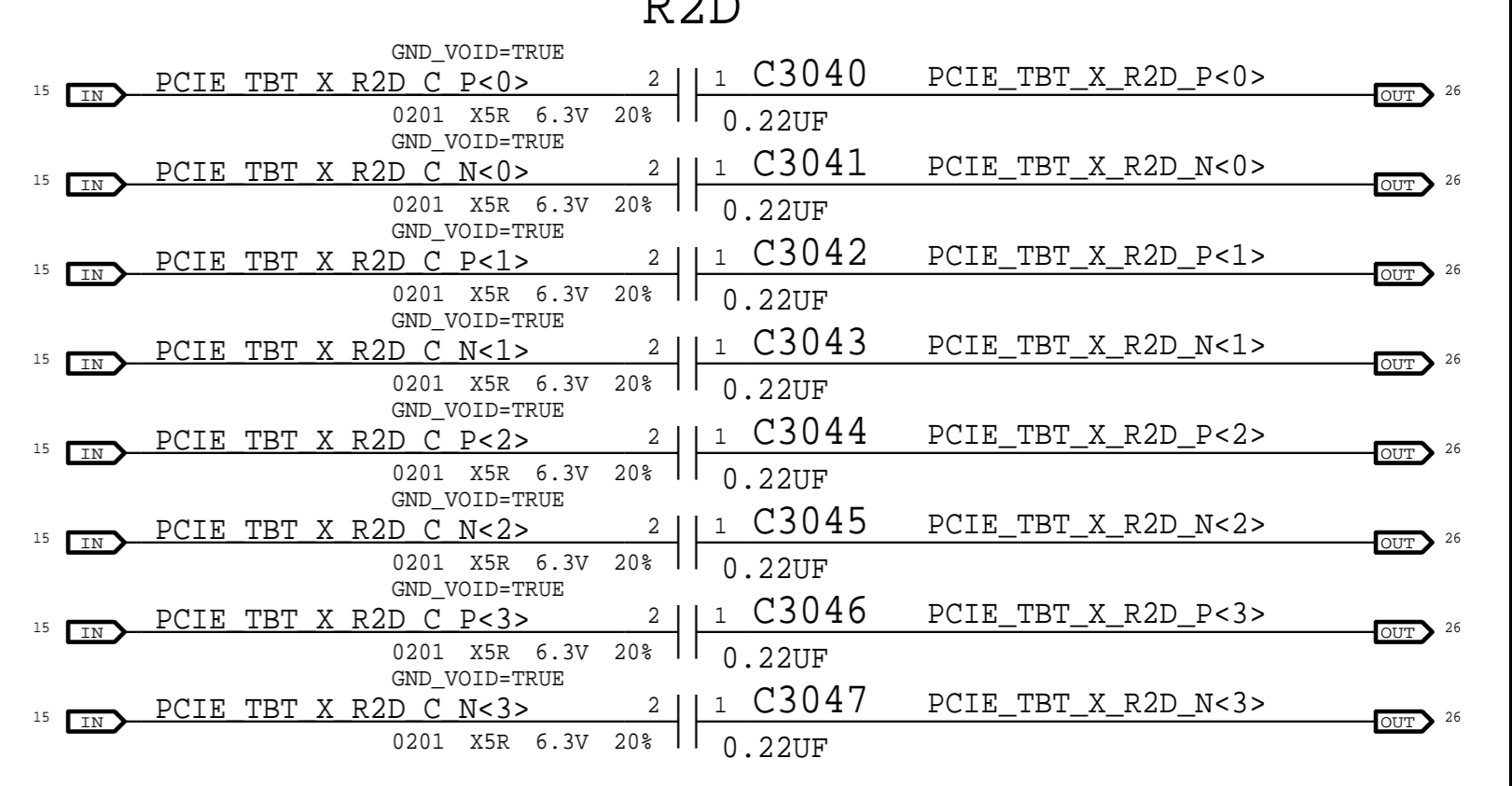
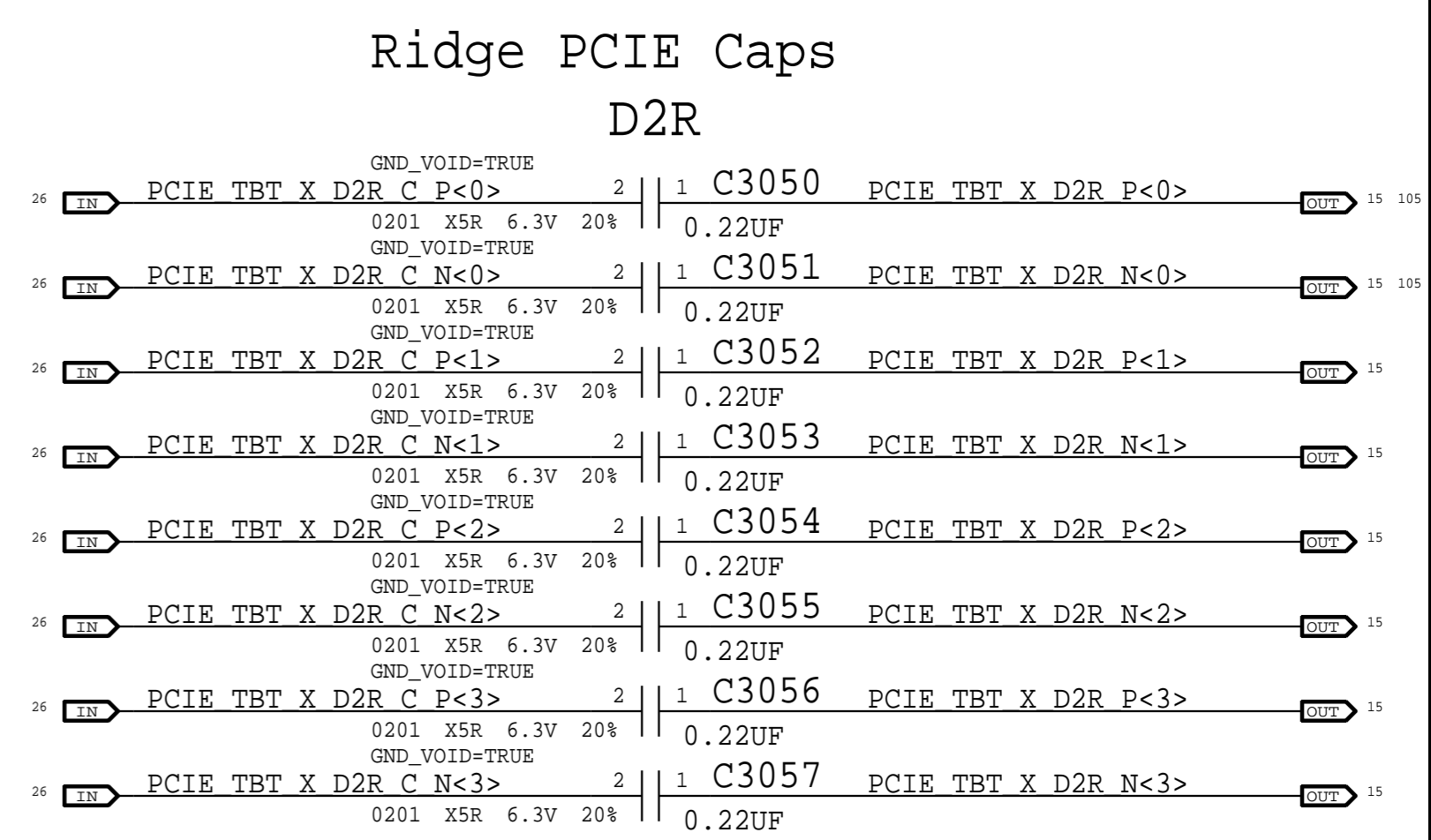
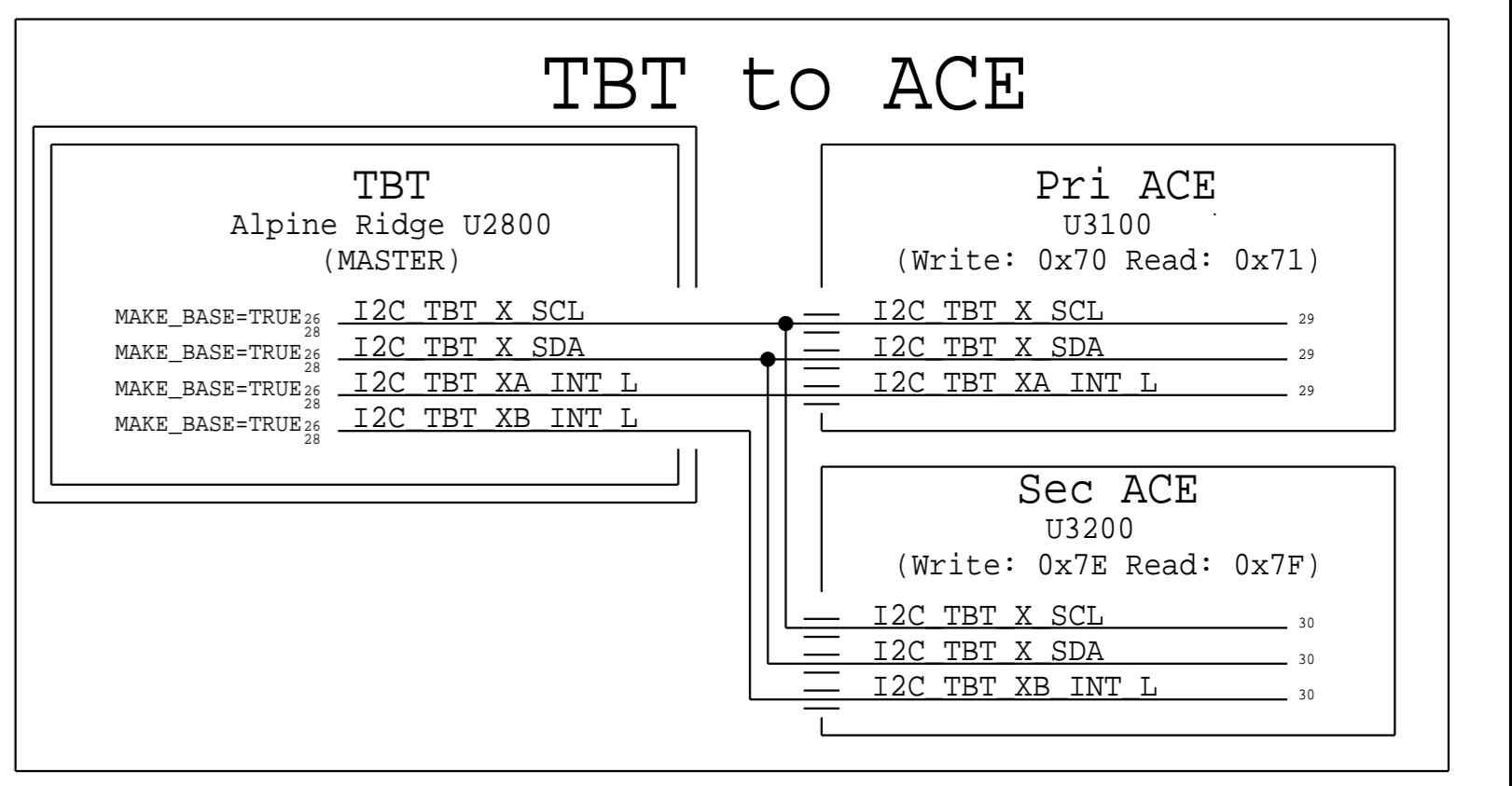
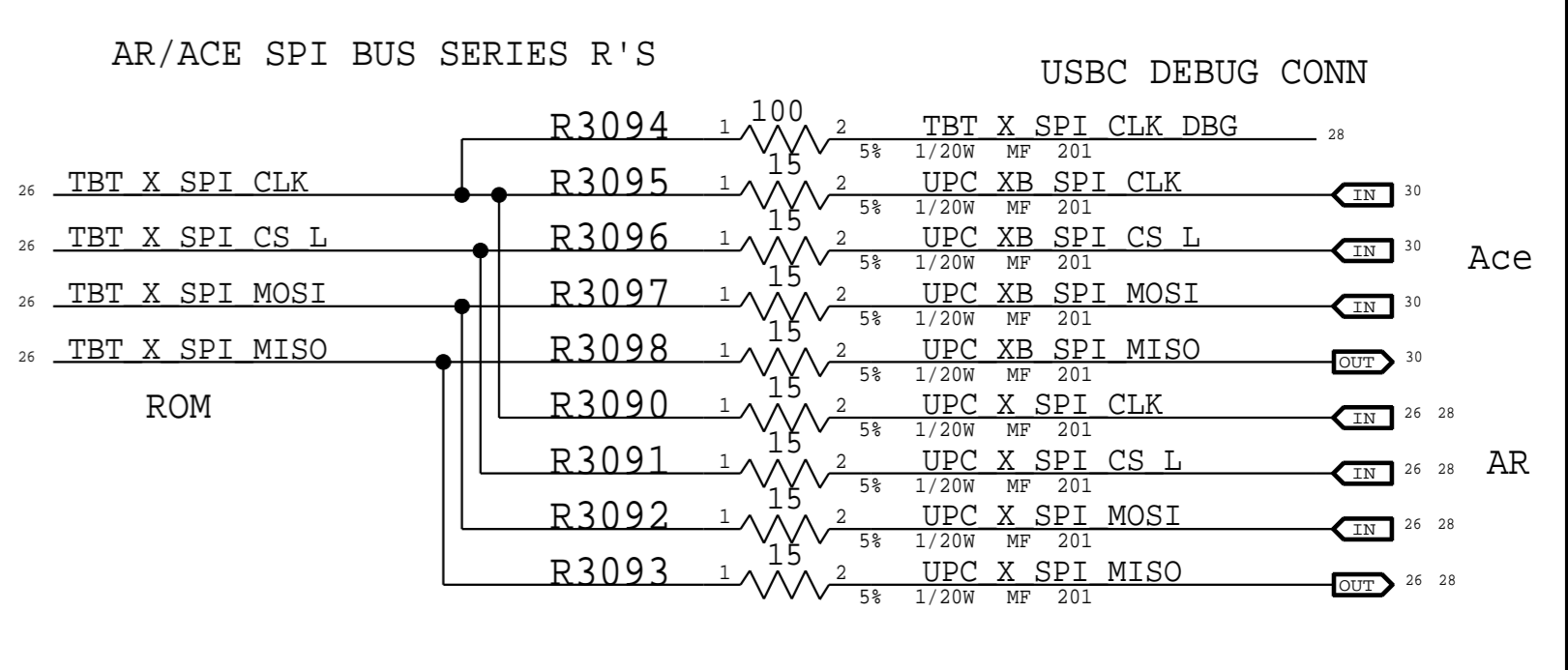
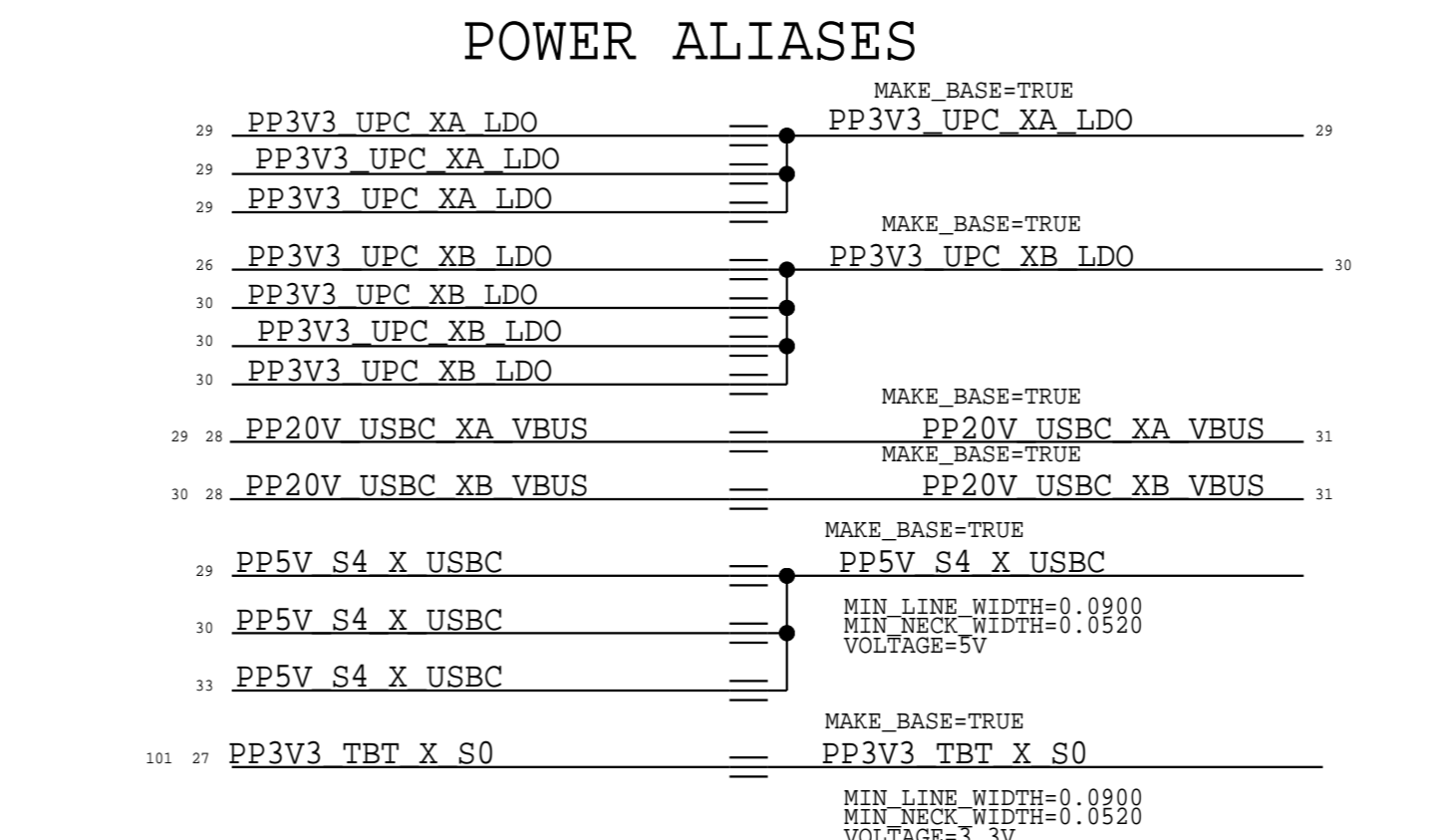
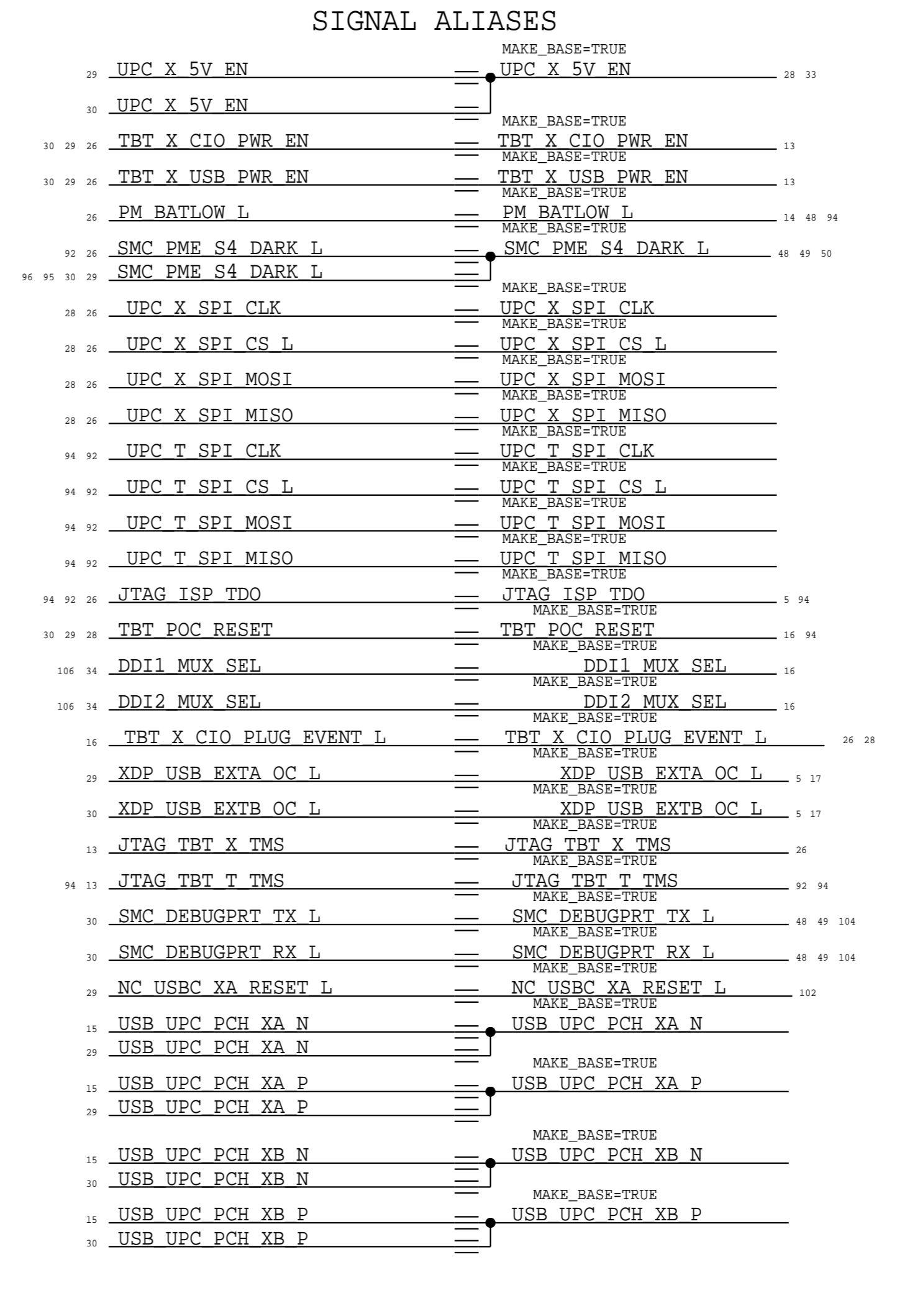
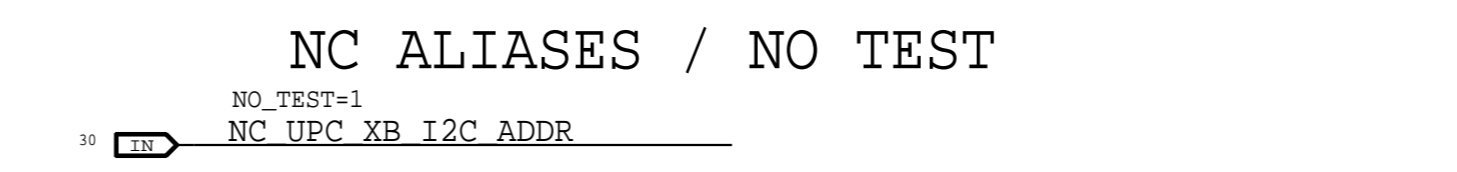
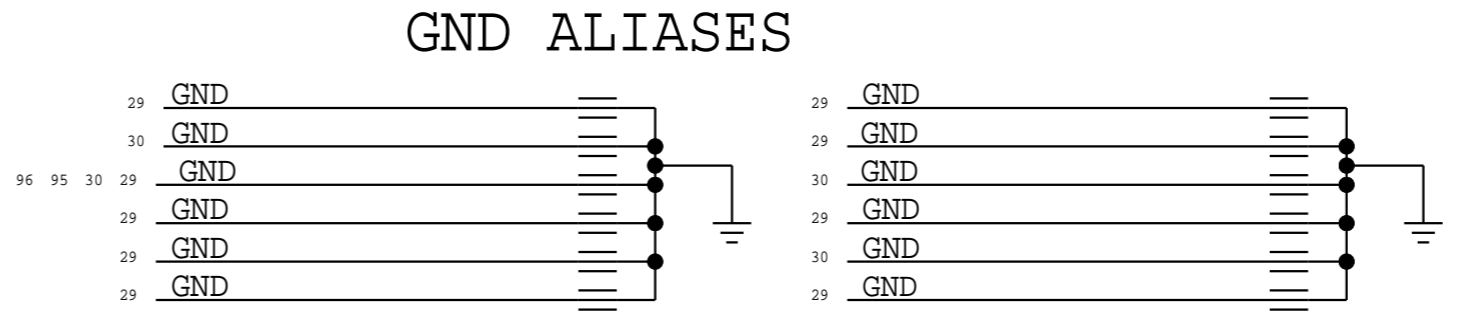
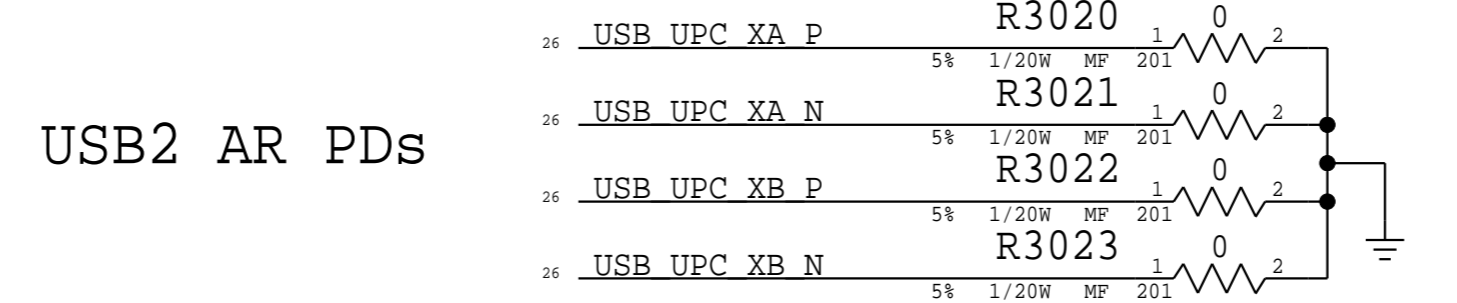
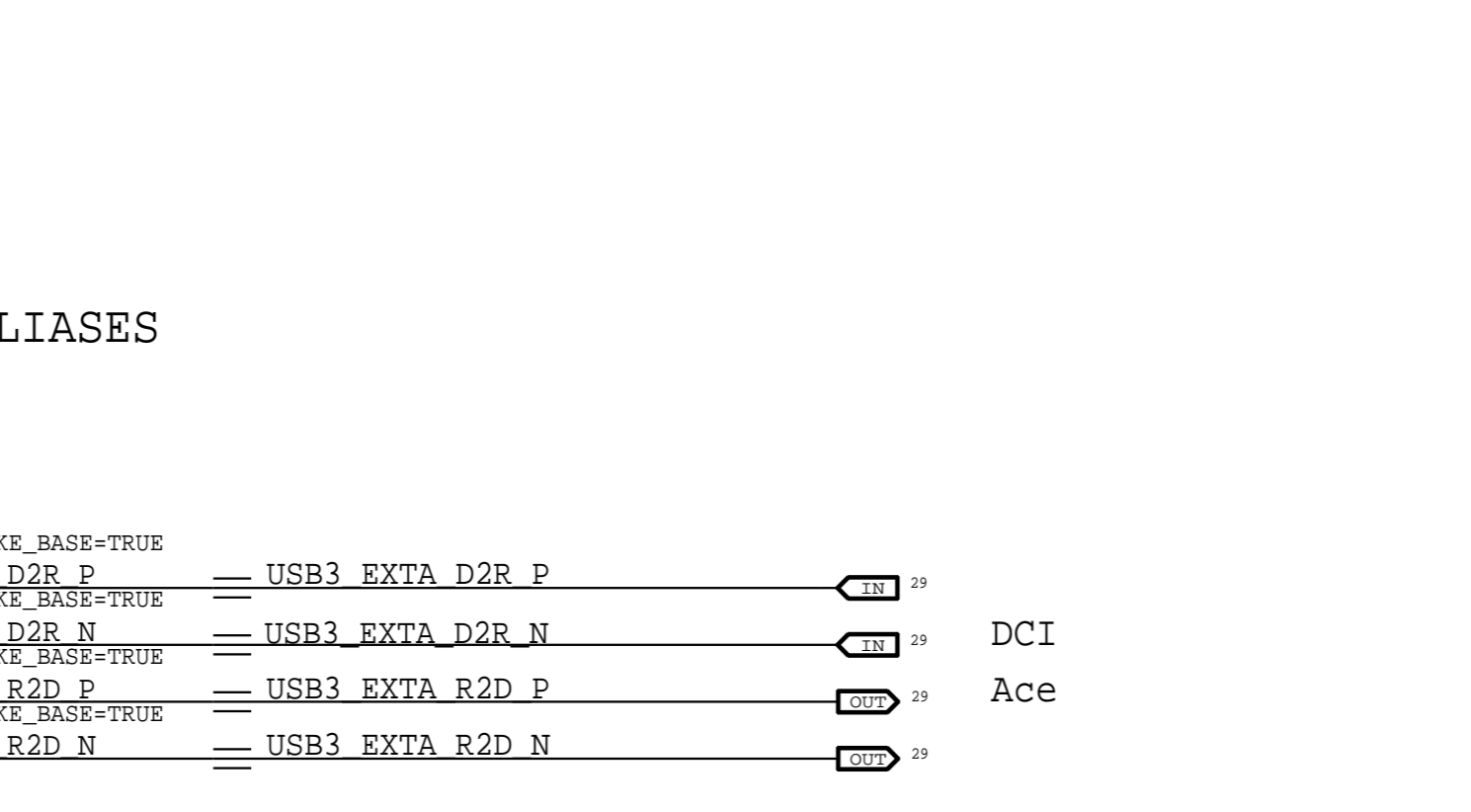
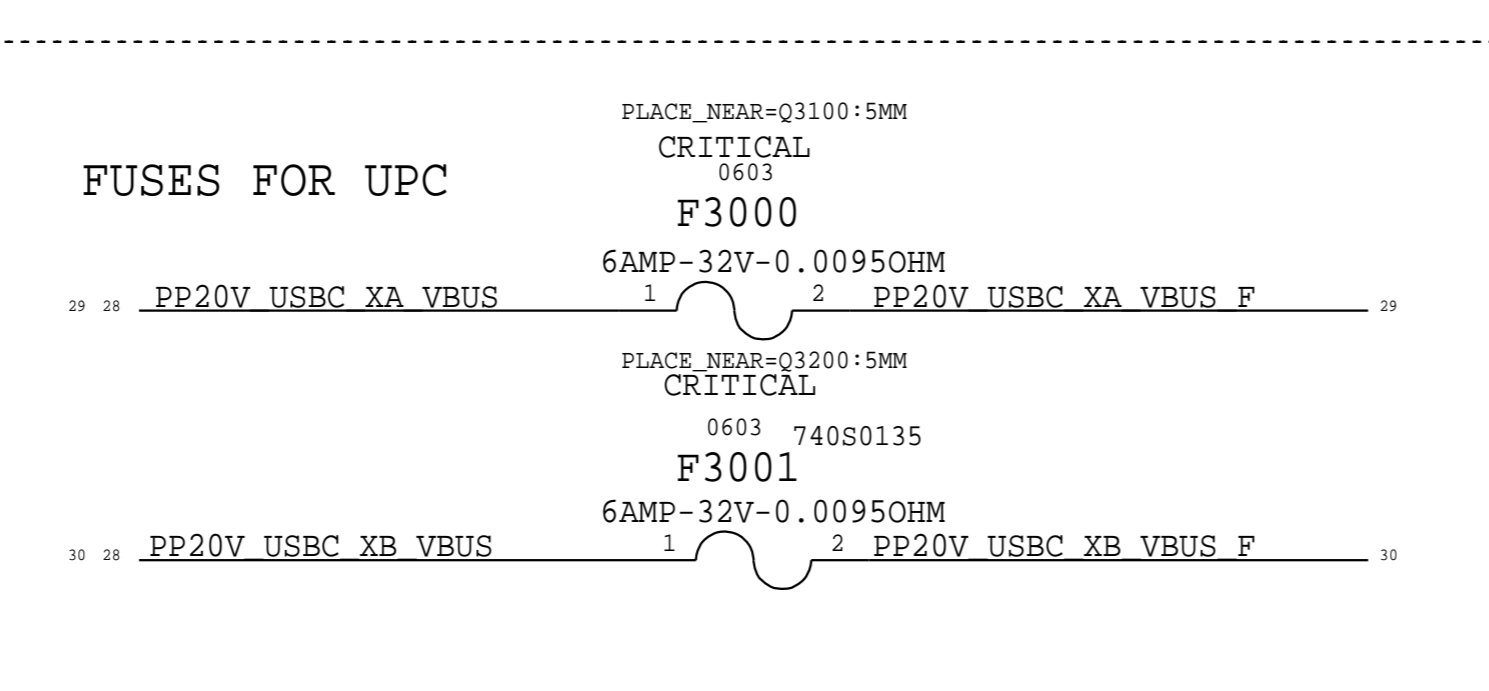
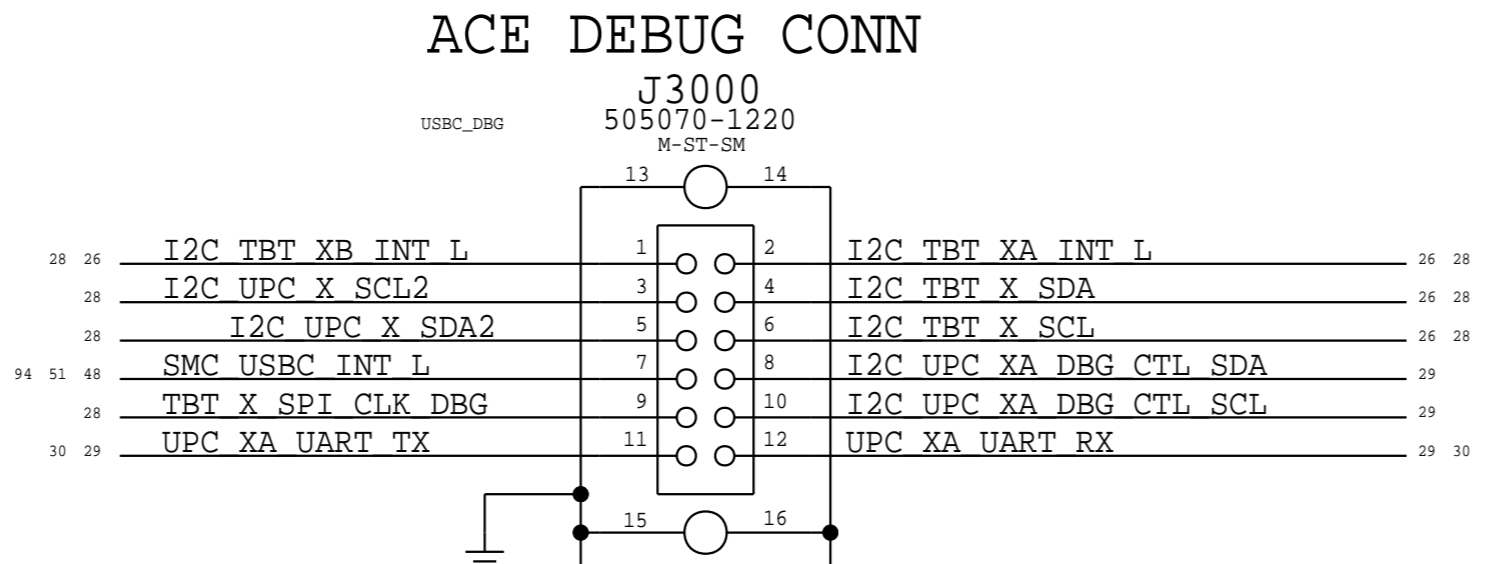
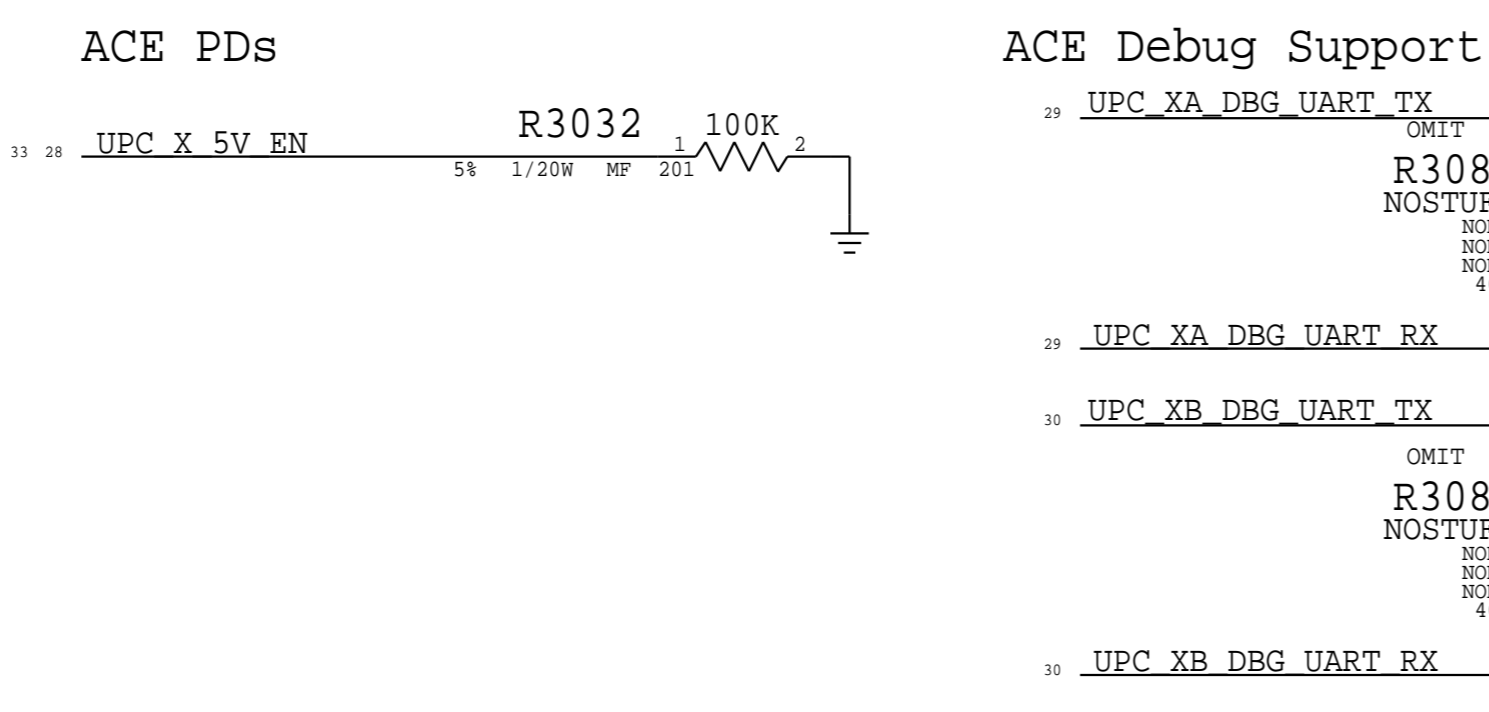
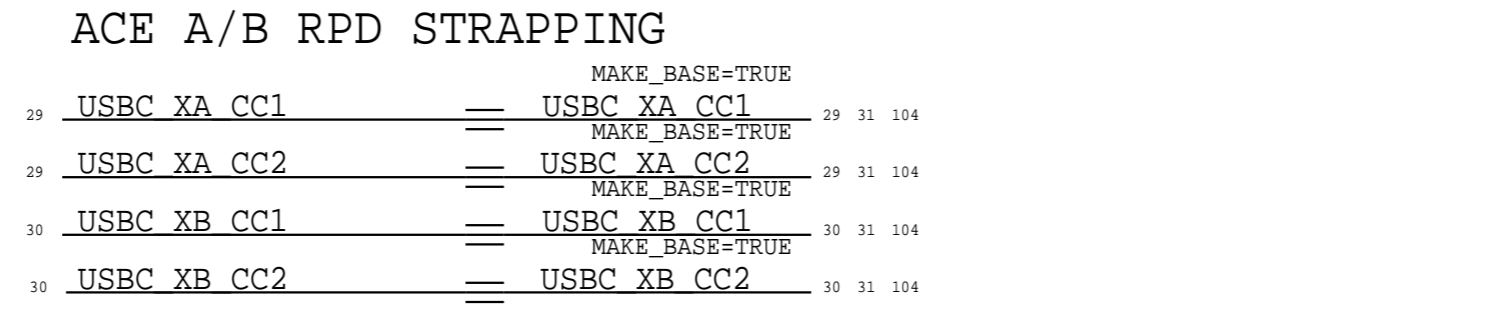
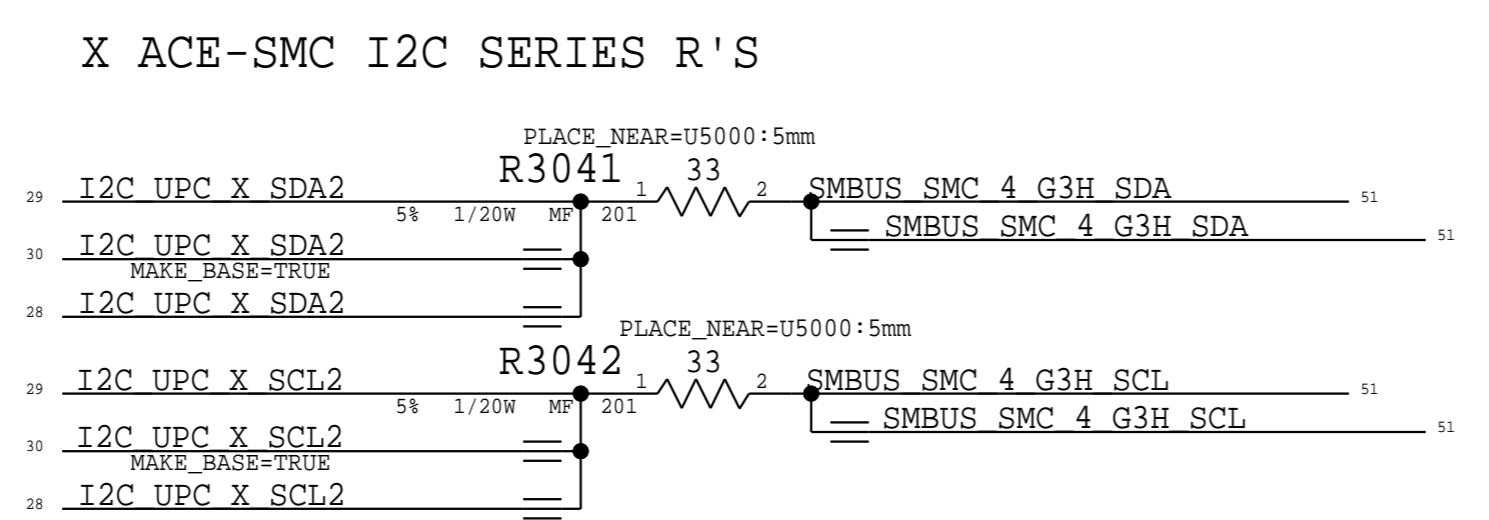
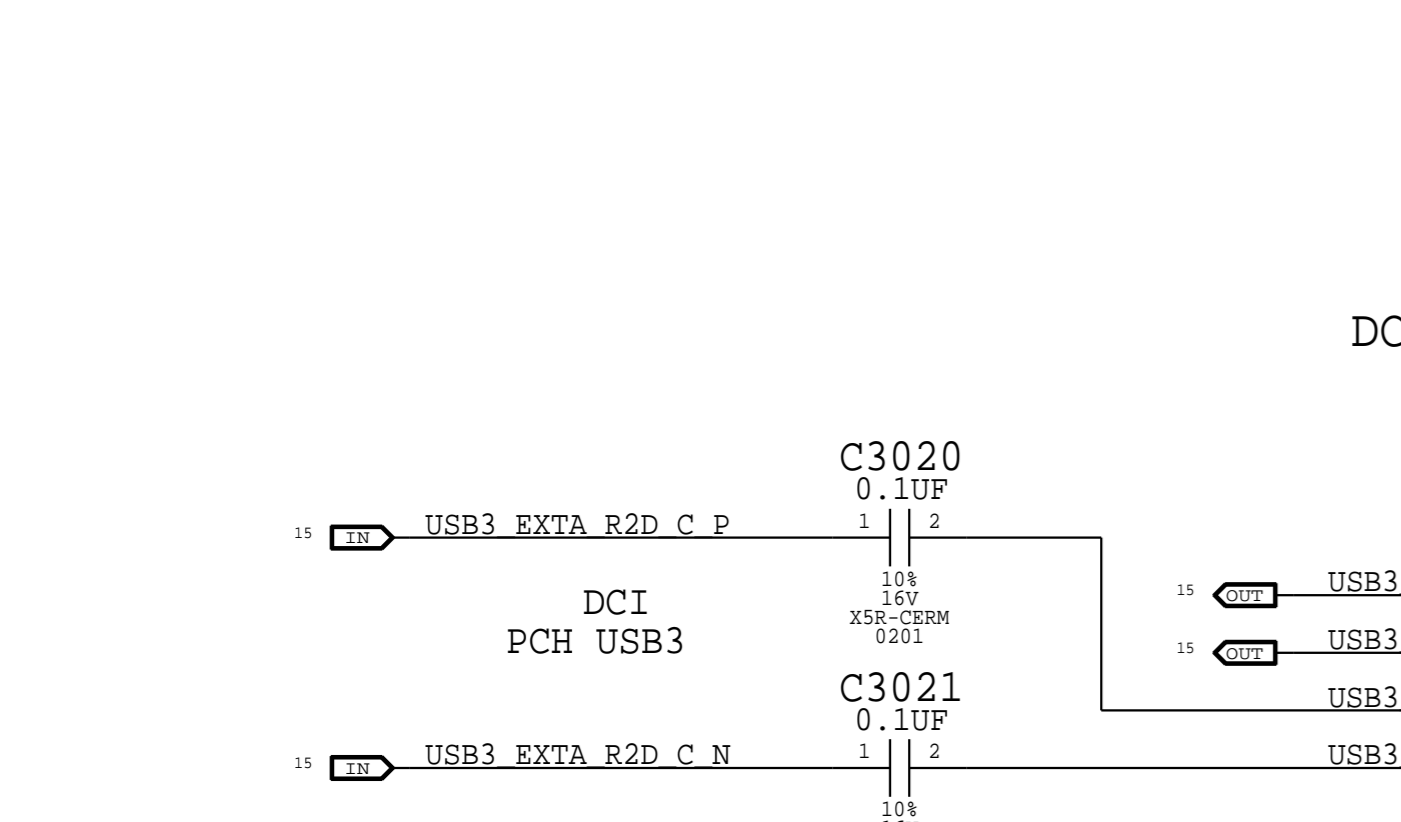
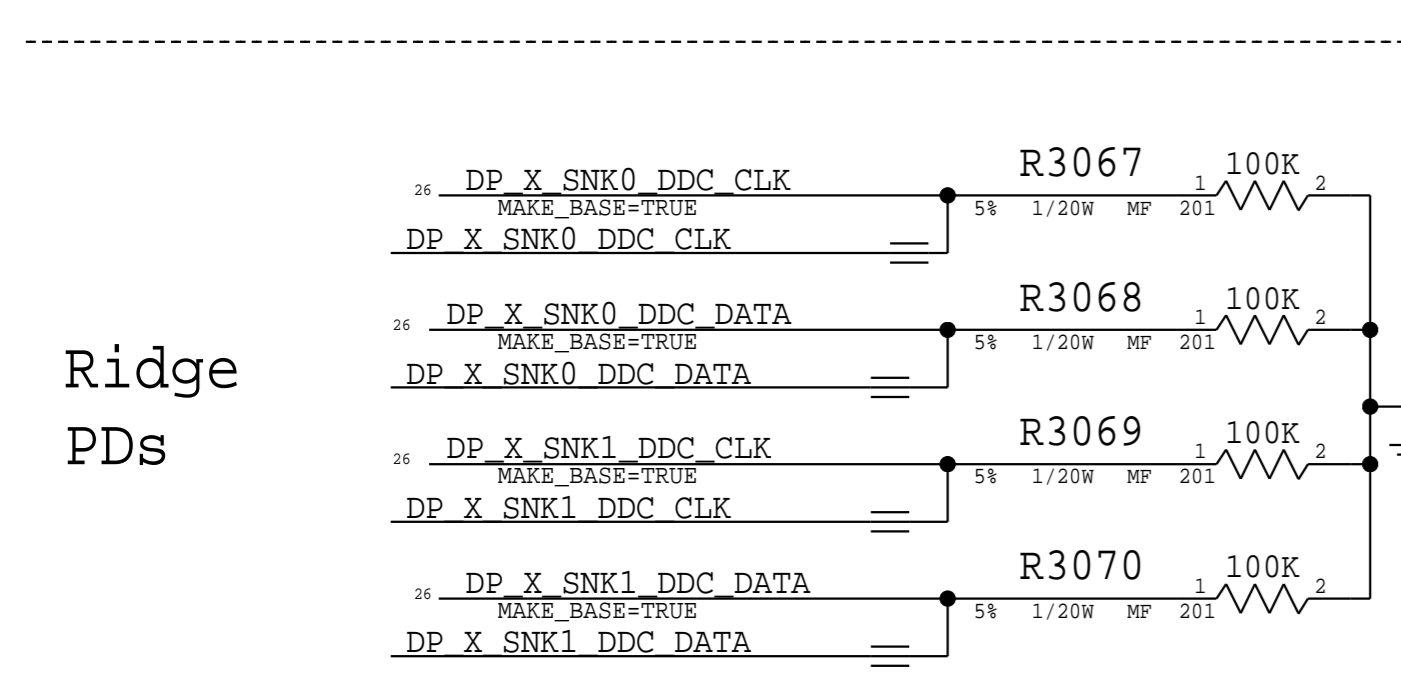
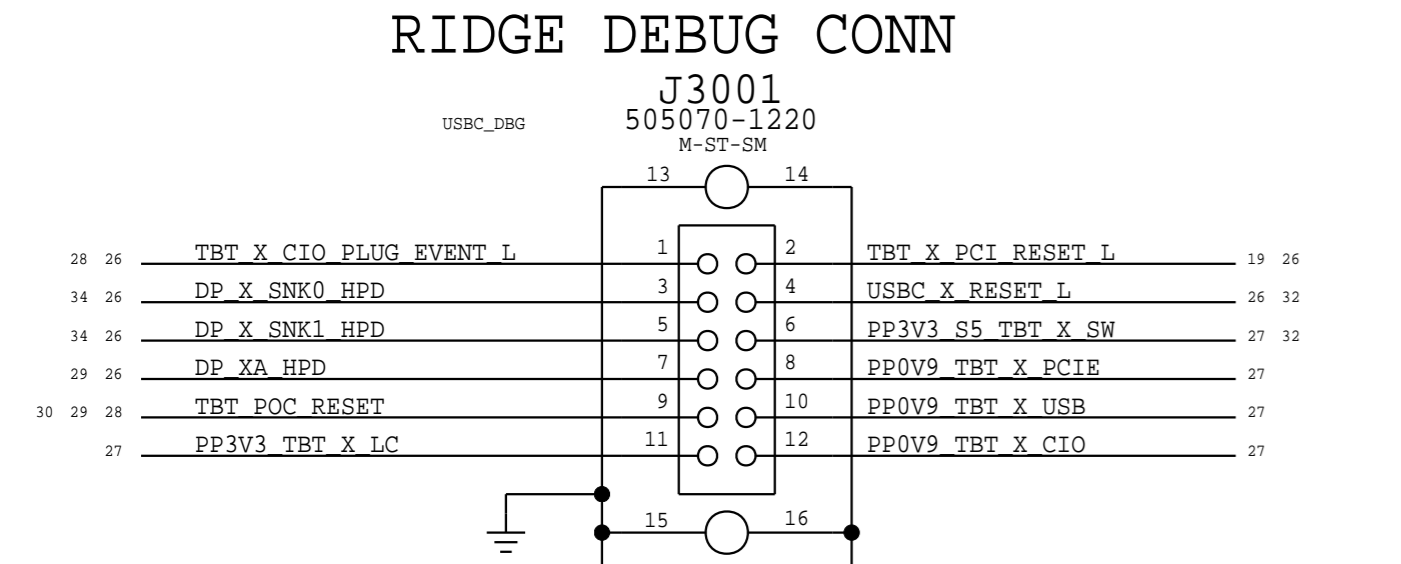
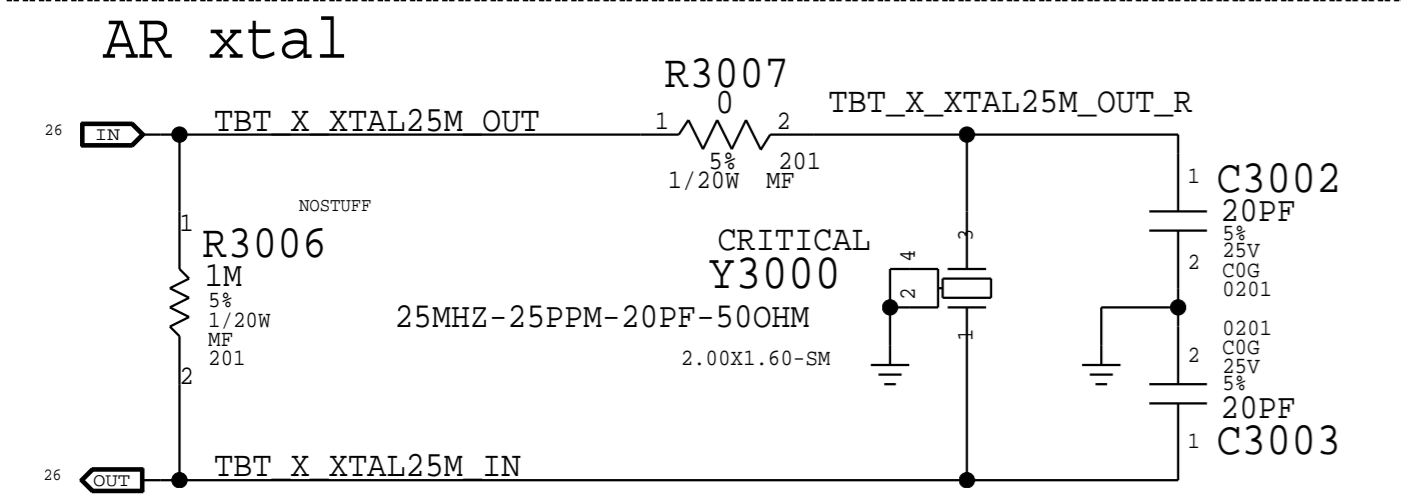
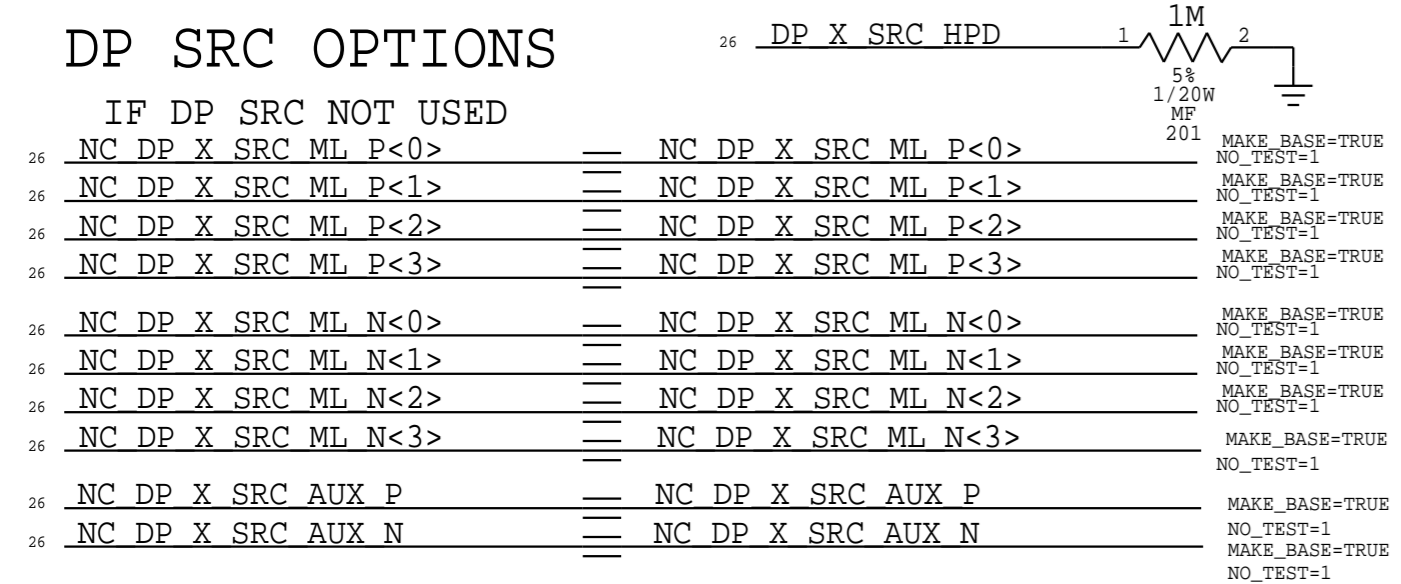
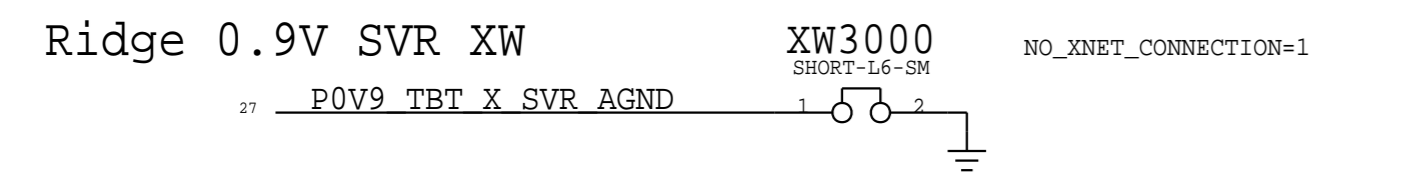
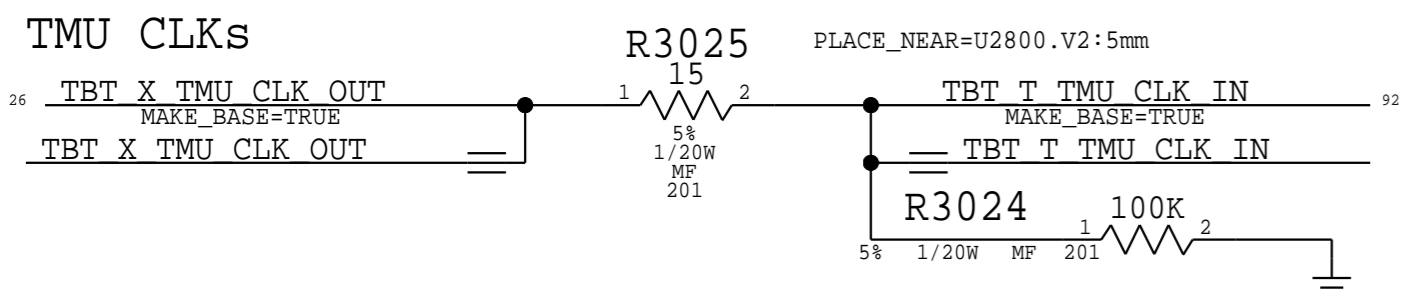
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 PAGE TITLE: USB-C HIGH SPEED 1 REVISION: 9.0.0
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BOM_COST_GROUP=TBT



SYNC_MASTER=779_0REG		SYNC_DATE=09/09/2015	
PAGE TITLE			
USB-C HIGH SPEED 2		DRAWING NUMBER	STAR
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		REVISION	
		9.0.0	
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BOM_COST_GROUP=TBT



USB-C Support

Apple Inc.

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REVISION 9.0.0	BRANCH dvt-fab09-0
PAGE 30 OF 145	SHEET 28 OF 119

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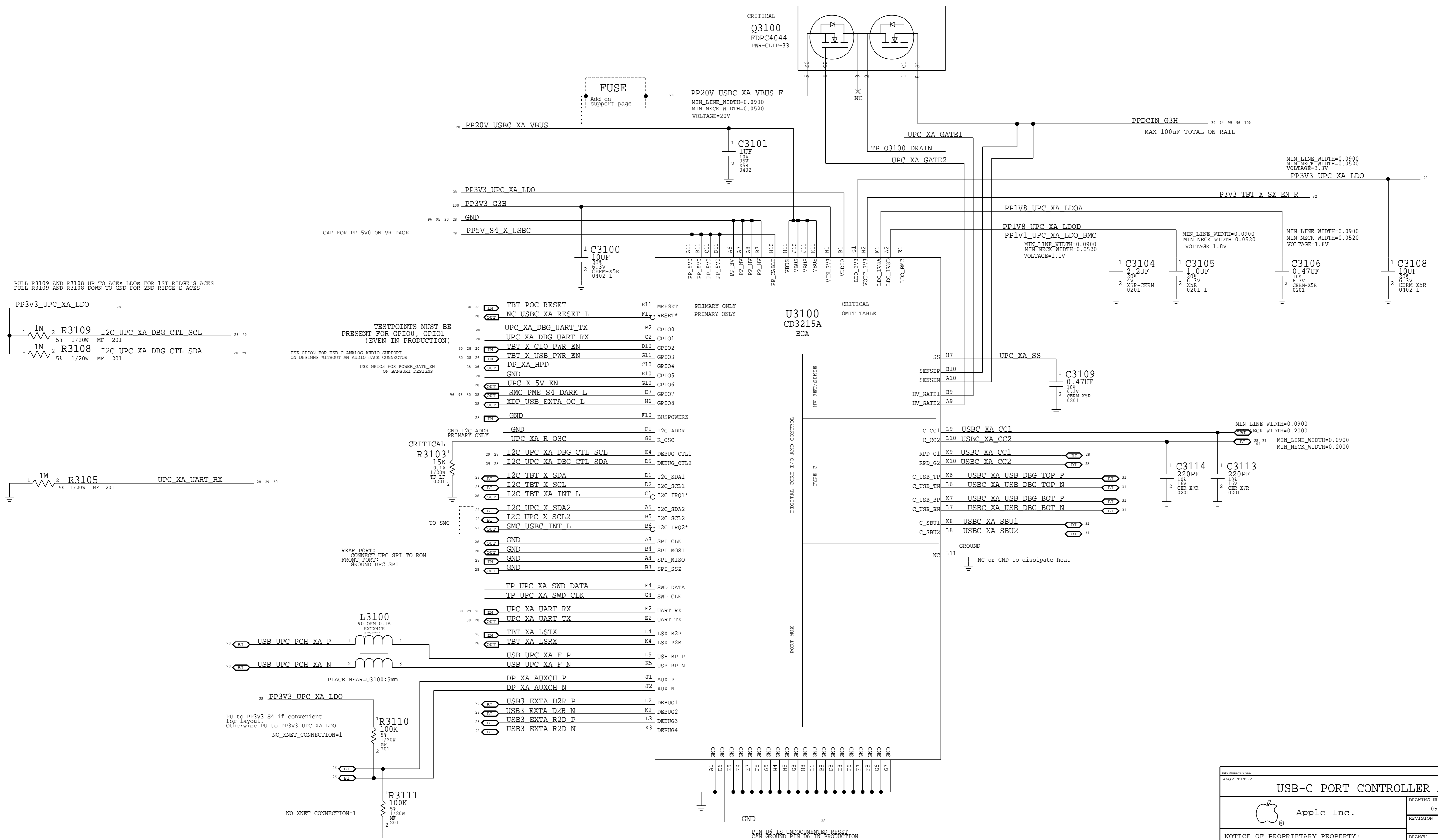
D

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PRIMARY ACE USB-C PORT CONTROLLER (UPC)

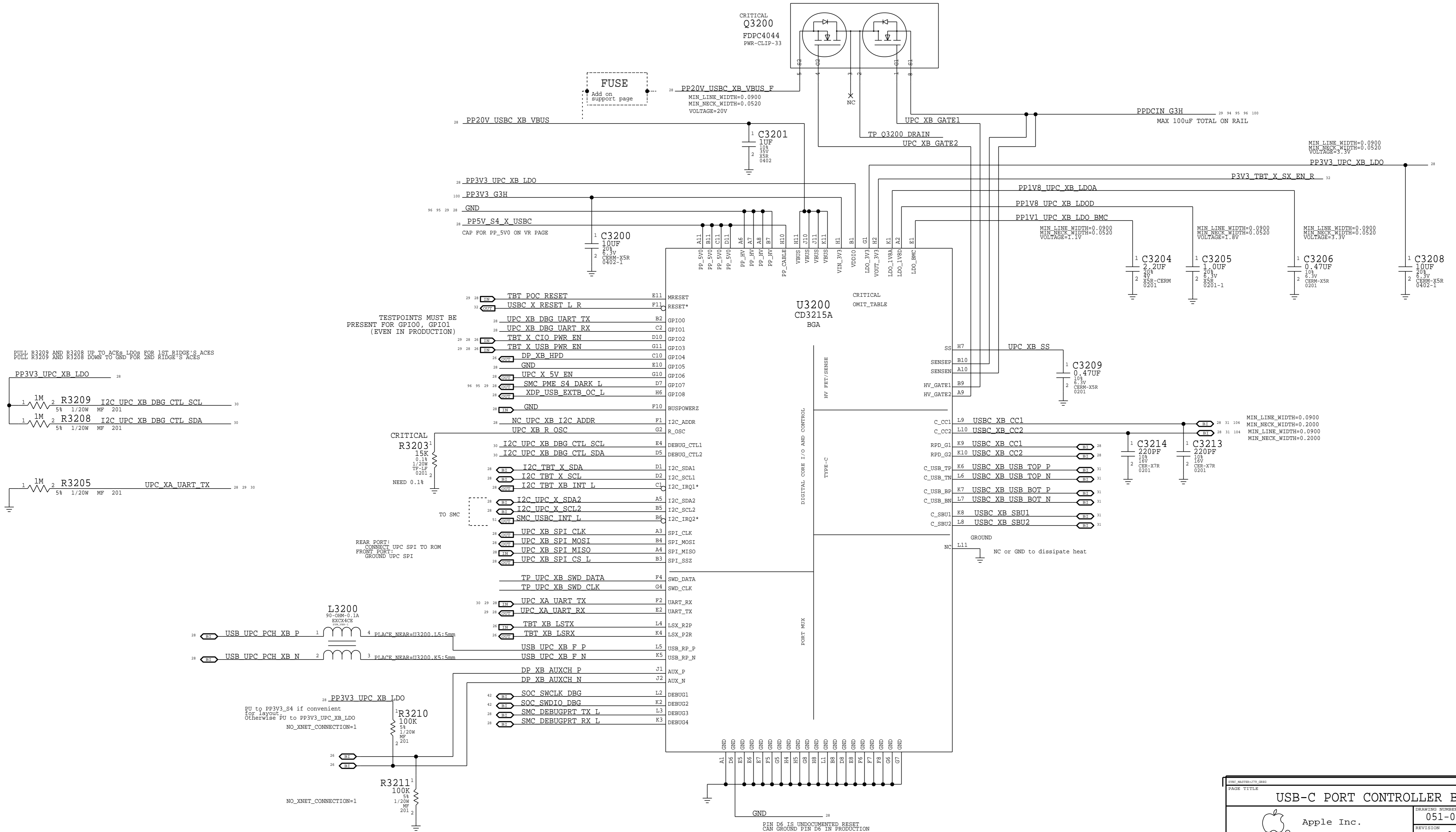


PAGE TITLE		
USB-C PORT CONTROLLER A		
		DRAWING NUMBER 051-00515
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BOM_COST_GROUP=USB-C

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

SECONDARY ACE USB-C PORT CONTROLLER (UPC)



PULL R3209 AND R3208 UP TO ACES_LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

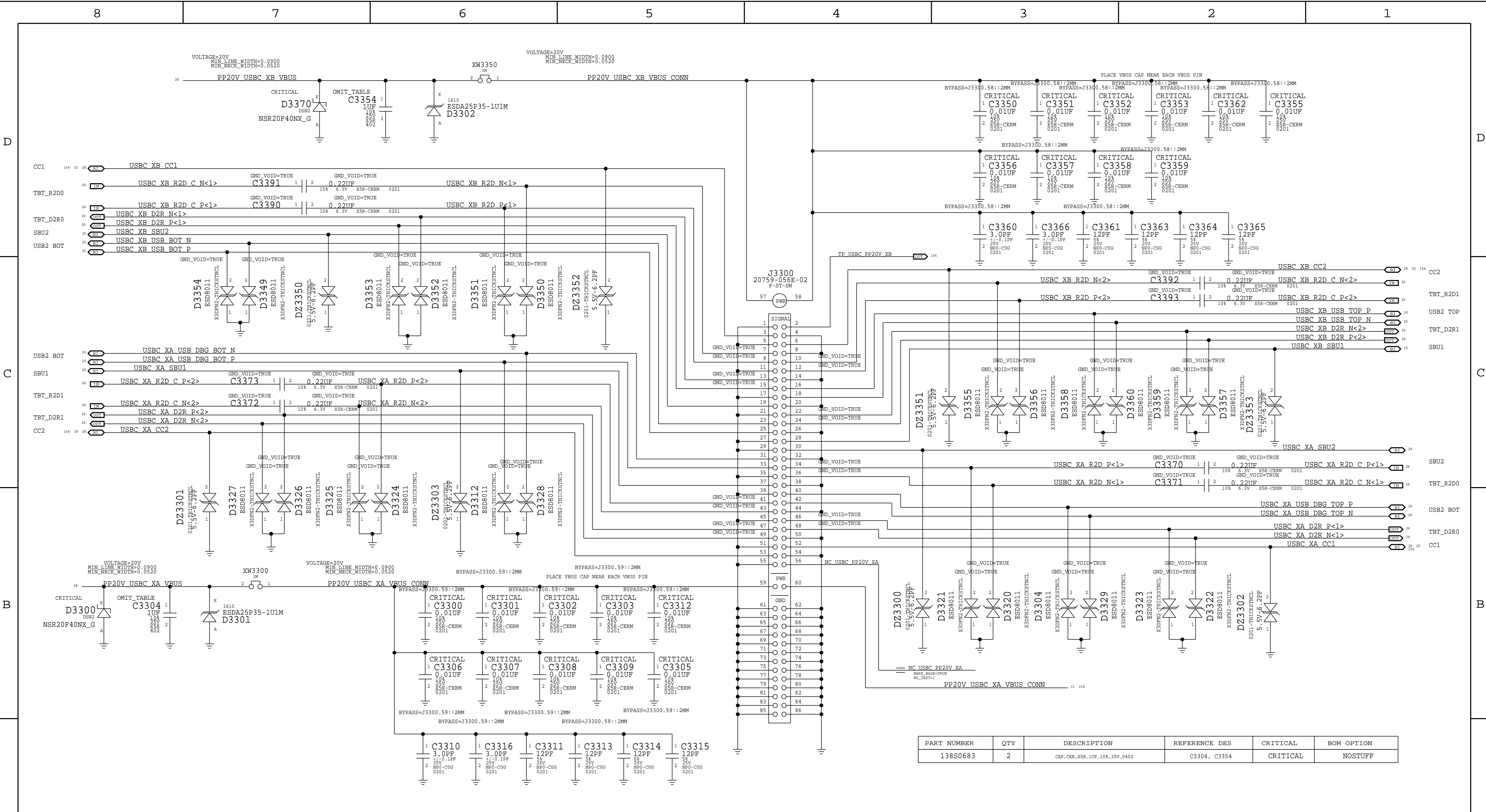
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

DRAWING NUMBER		051-00515	SIZE
REVISION		9.0.0	D
BRANCH		dvt-fab09-0	
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SHEET		30 OF 119	

BOM_COST_GROUP=USB-C




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,XSR,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A



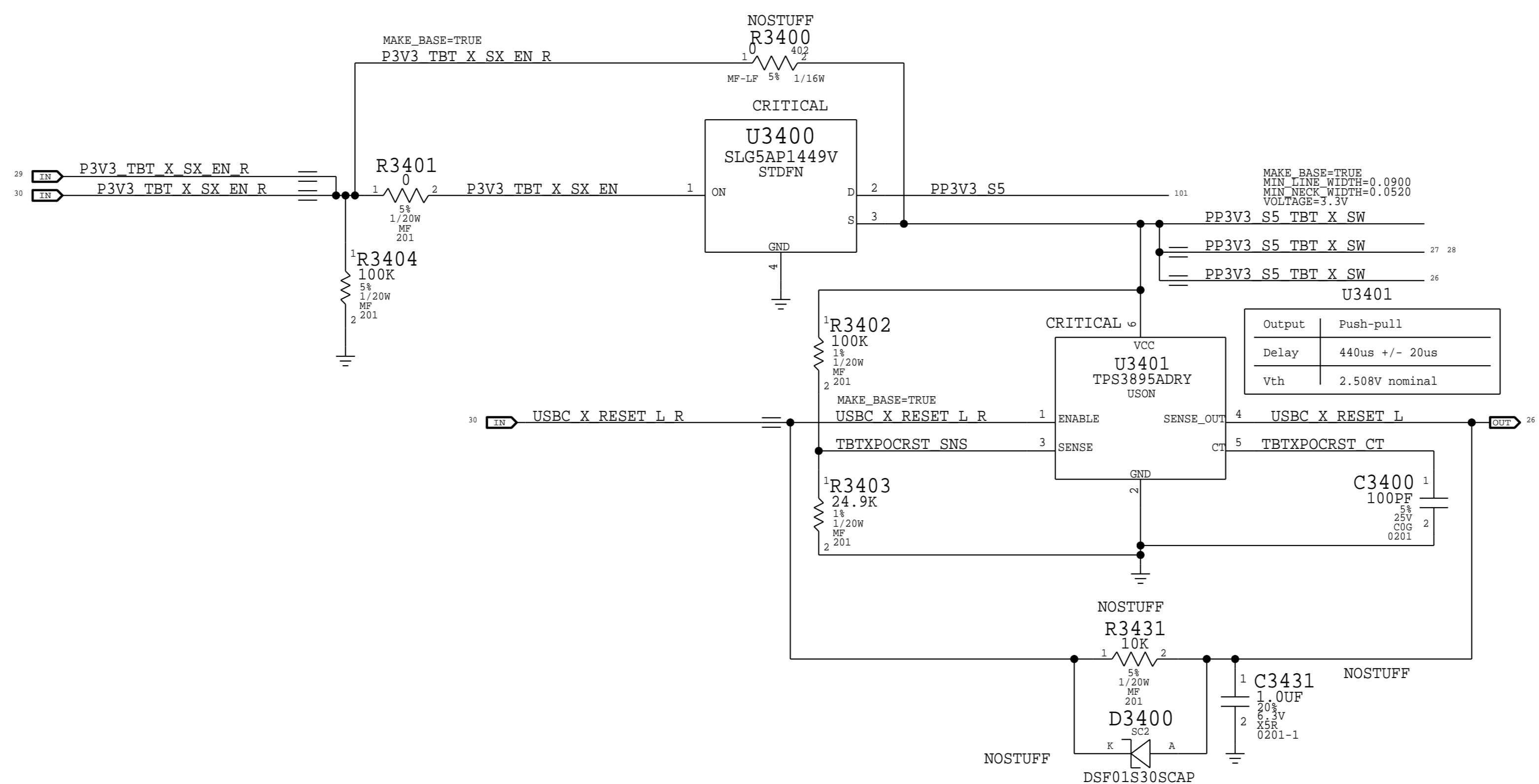
Apple Inc.

DRAWING NUMBER	051-00515	STR	D
REVISION	9.0.0	BRANCH	dvt-fab09-0
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BOM_COST_GROUP=USB-C

TBT X "POC" Power-up Reset



DESIGN: X502/DEV_MLB_U	
LAST CHANGE: Wed Feb 18 17:12:24 2015	
PAGE TITLE	
USB-C CONNECTOR B	
	DRAWING NUMBER 051-00515
	REVISION 9.0.0
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	PAGE 34 OF 145
	SHEET 32 OF 119

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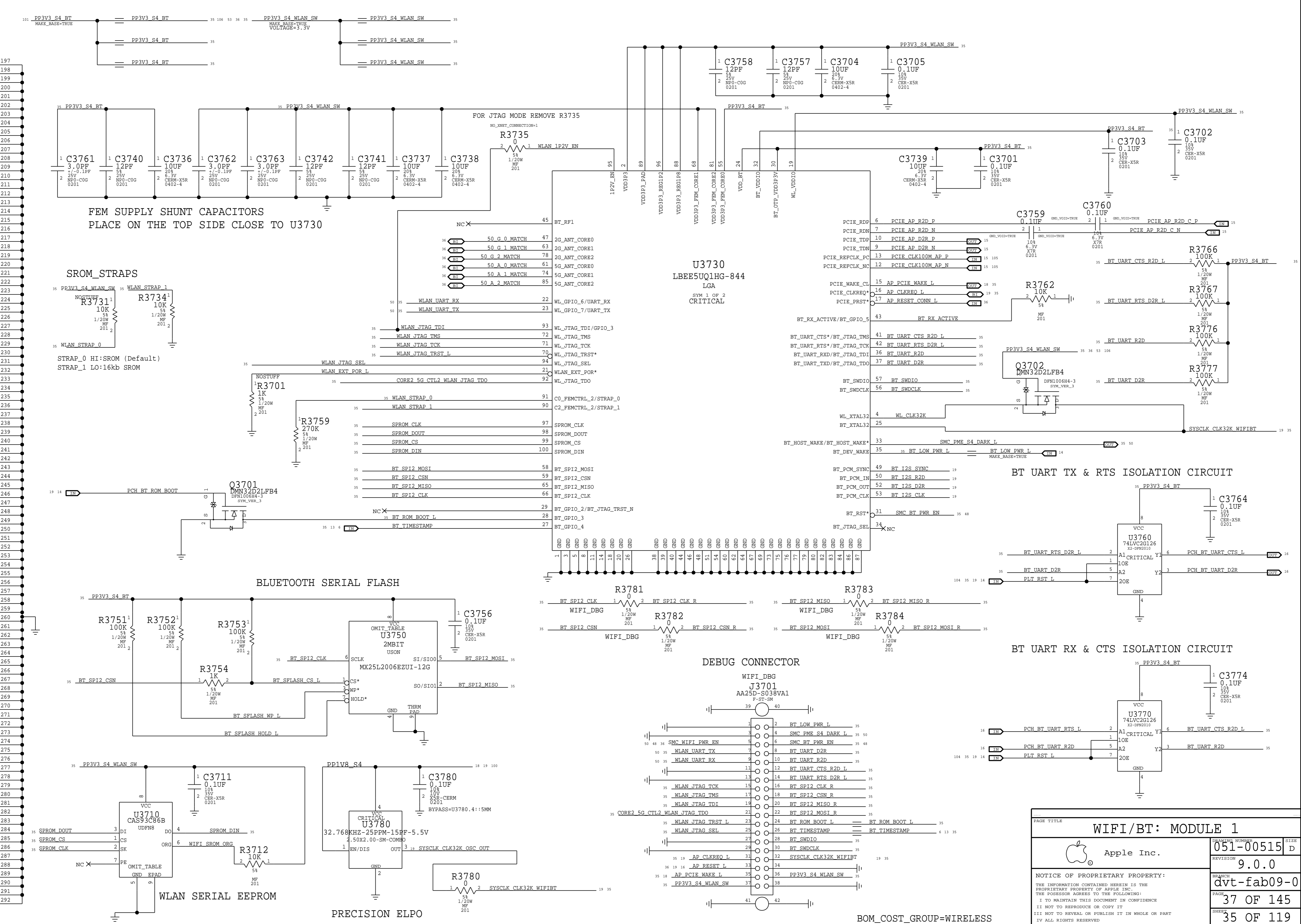
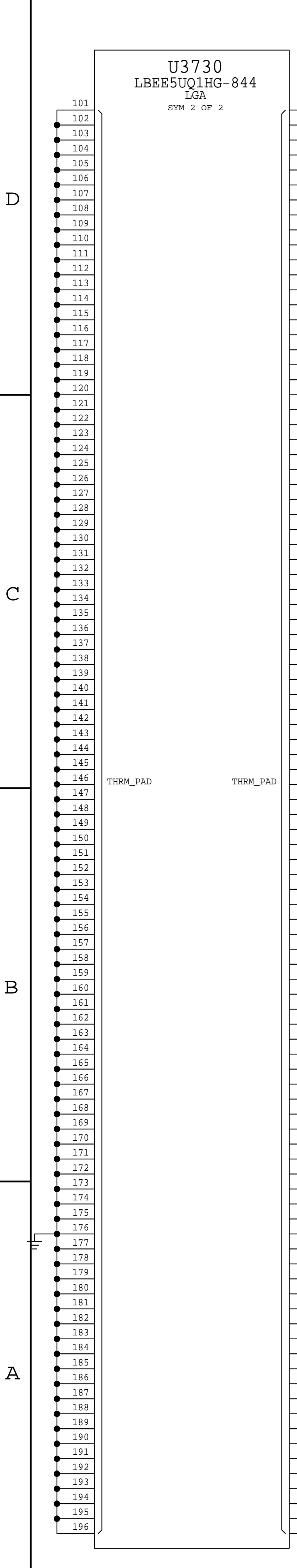
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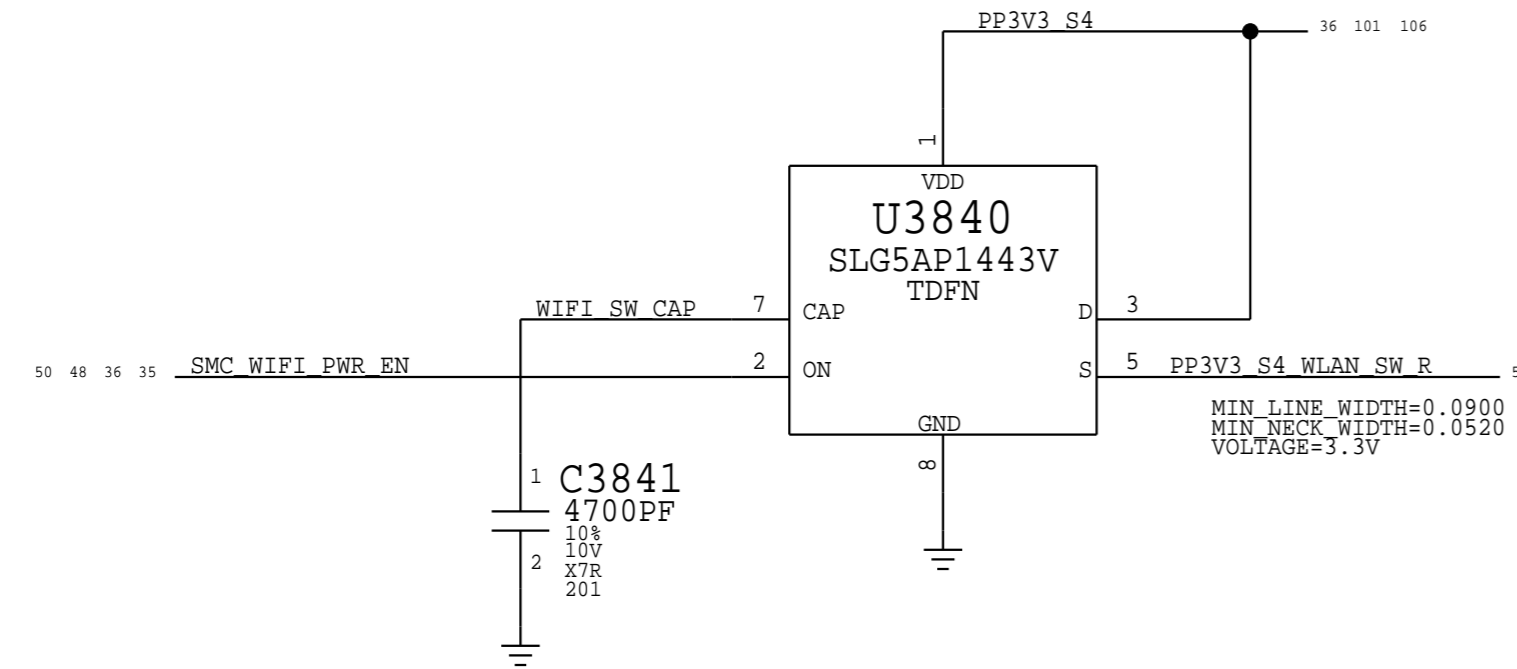
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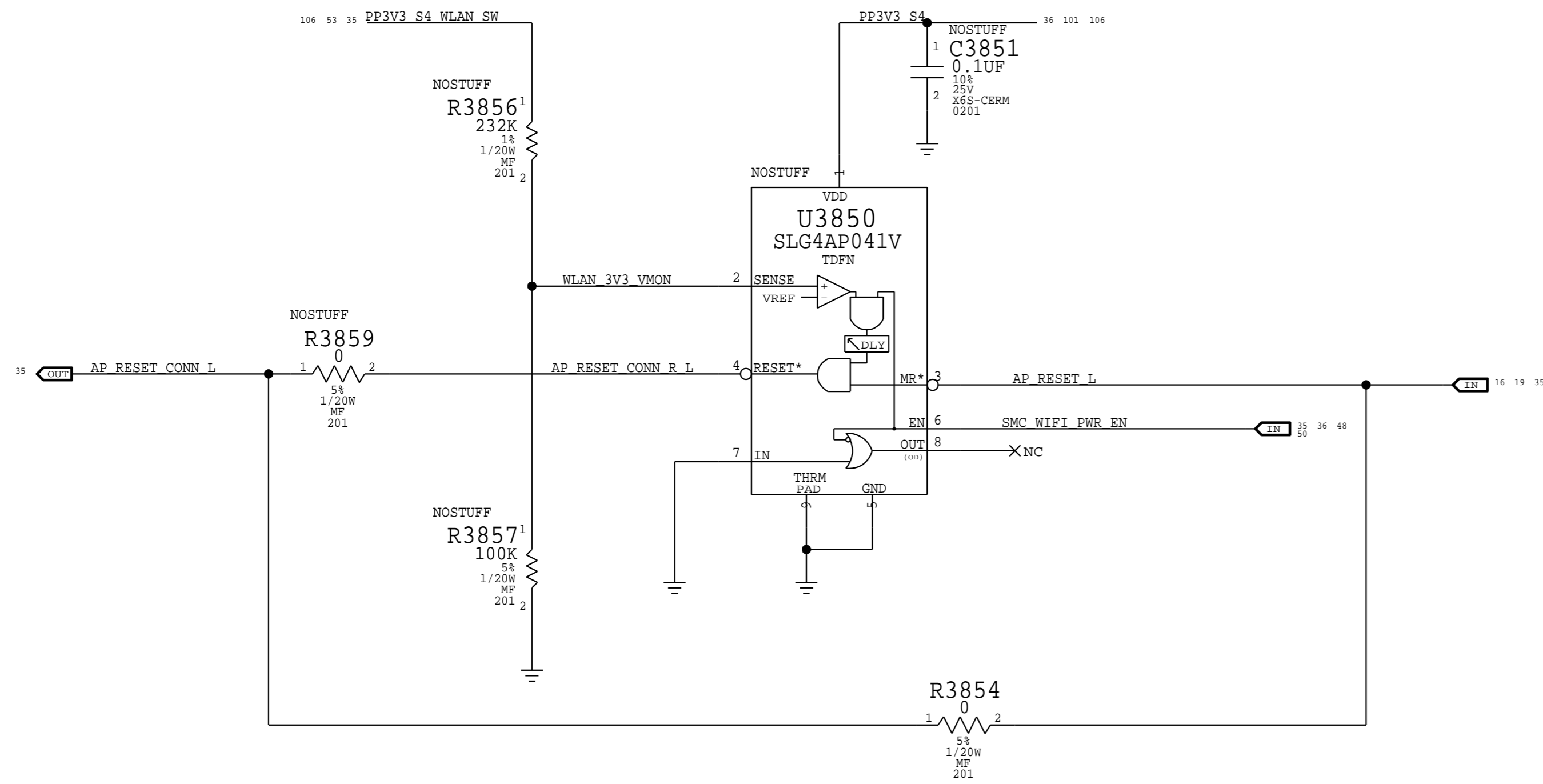


WLAN Power Switch

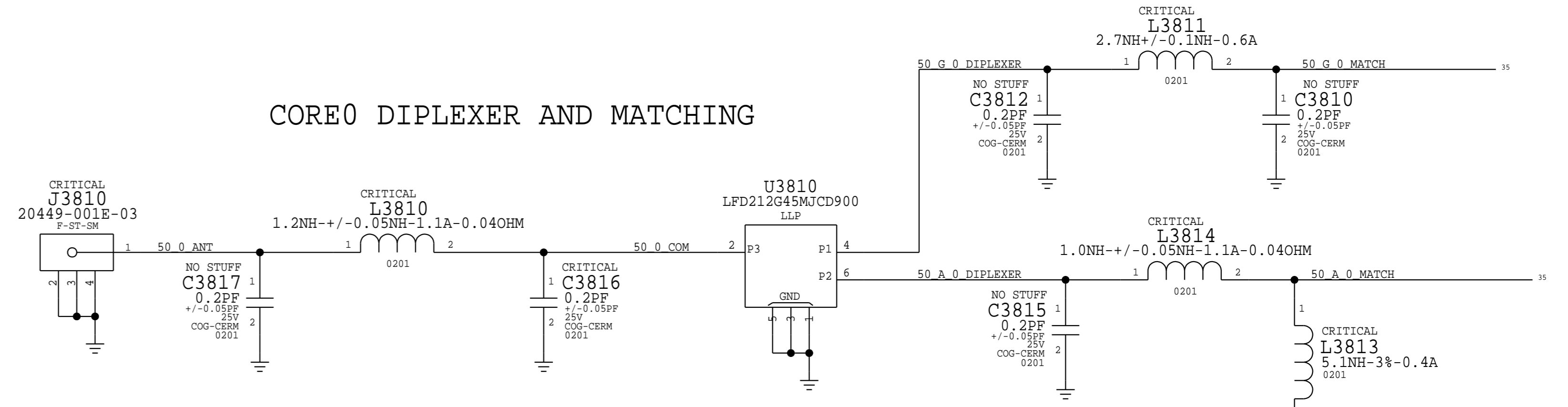


Supervisor & CLKREQ# Isolation

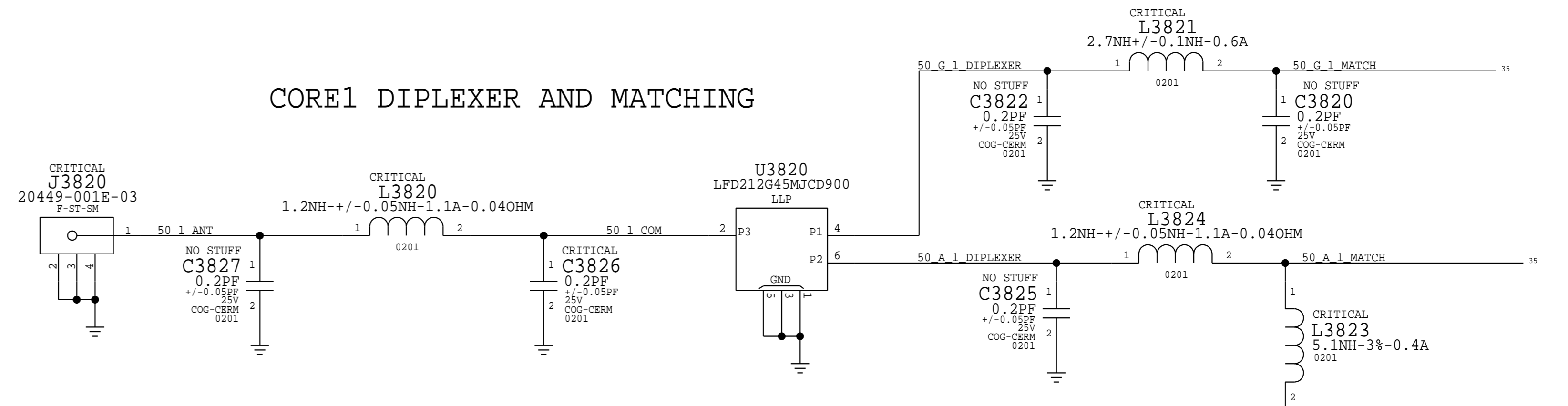
Delay = 130ms +/- 20%



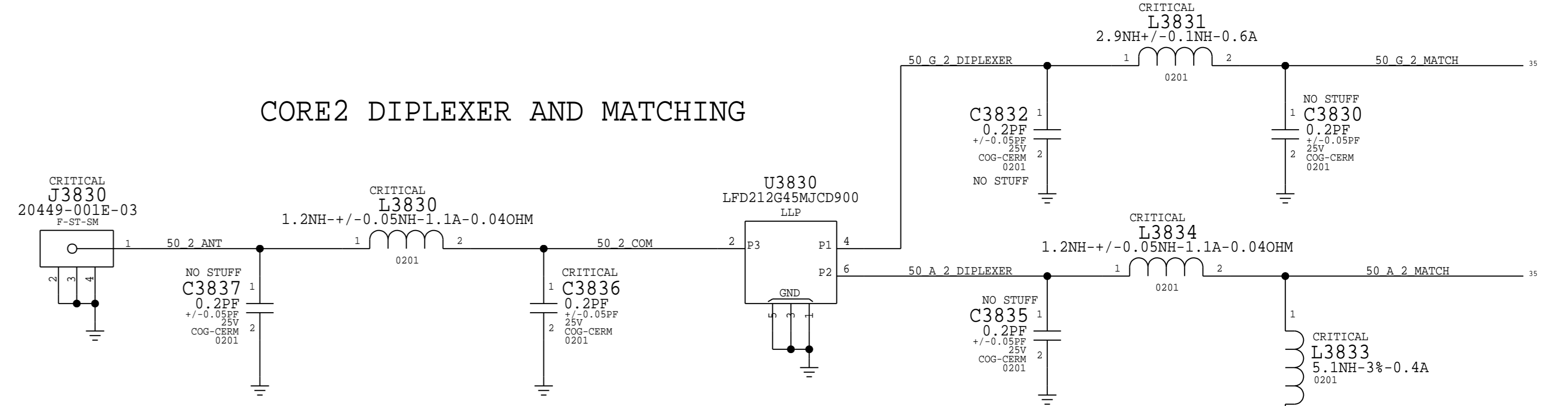
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

WIFI/BT: MODULE 2	
Apple Inc.	051-00515
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343800135	1	IC,M8+512MB 20NM DDR,A12,S,S,CK,BGA700	U3900	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338800147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338800097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD

T208

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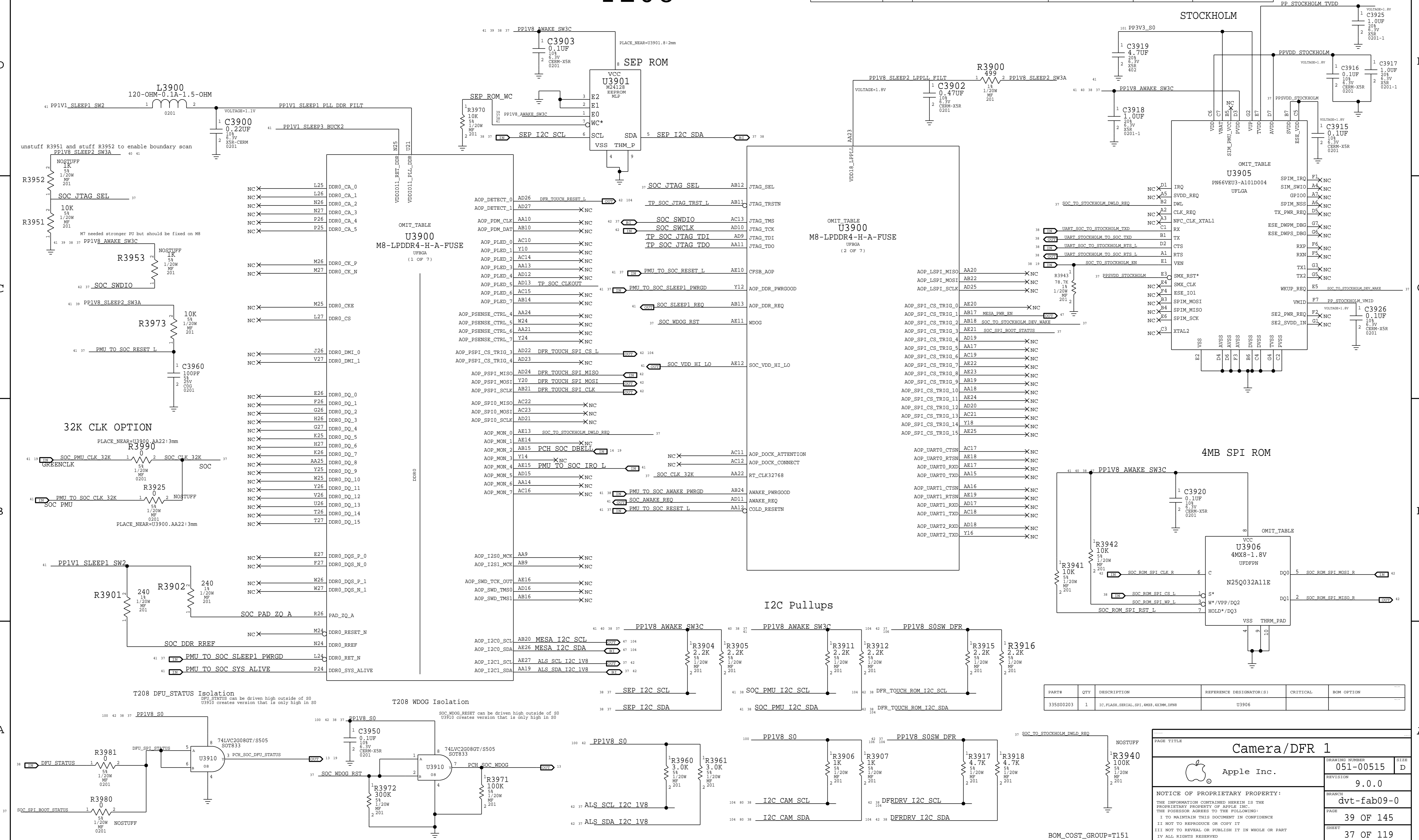
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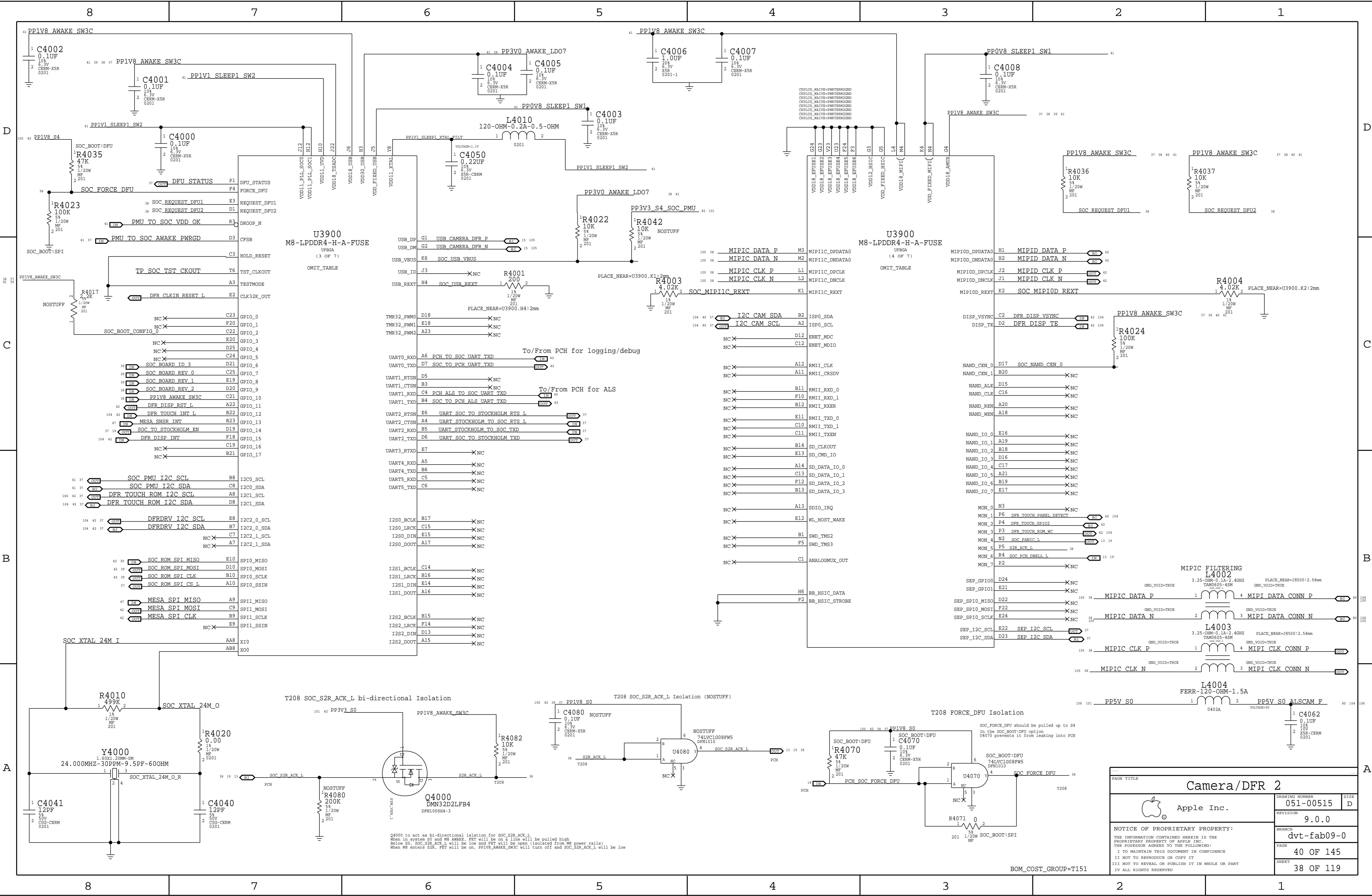
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335800203	1	IC,FLASH,SERIAL,SPI,4MX8,4K3MM,DFNS	U3906		


Camera/DFR 1

Apple Inc.

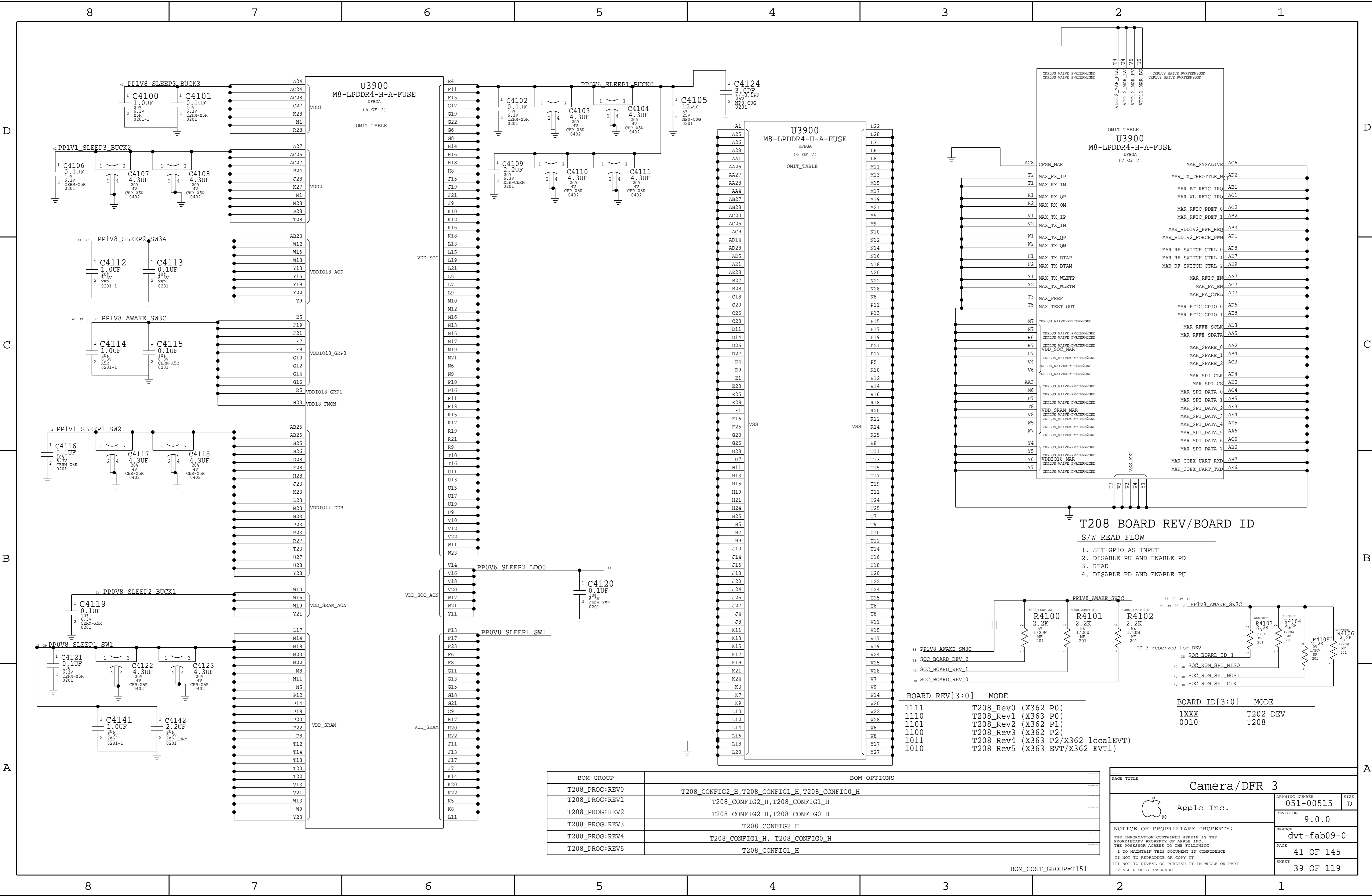
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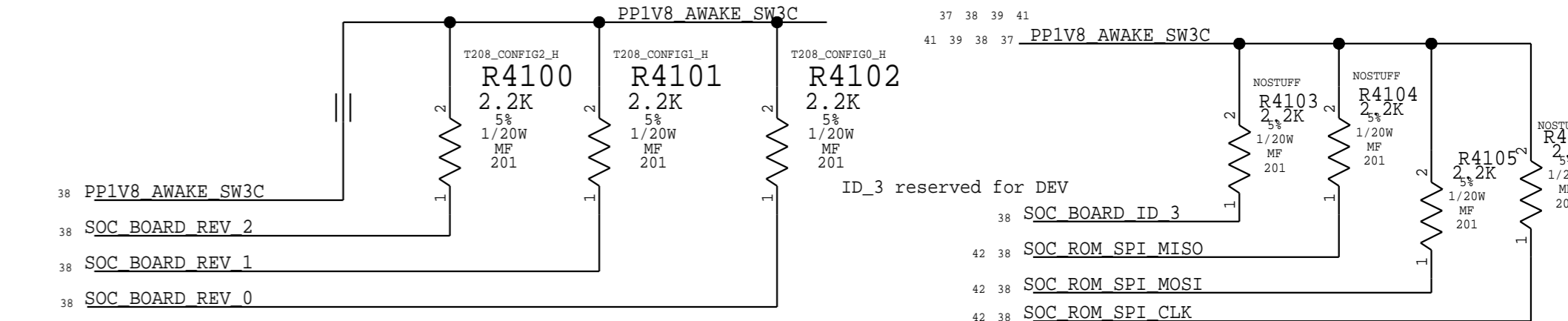
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BOM_COST_GROUP=T151



T208 BOARD REV/BOARD ID
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



BOARD REV[3:0]	MODE
1111	T208_Rev0 (X362 P0)
1110	T208_Rev1 (X363 P0)
1101	T208_Rev2 (X362 P1)
1100	T208_Rev3 (X362 P2)
1011	T208_Rev4 (X363 P2/X362 localEVT)
1010	T208_Rev5 (X363 EVT/X362 EVT1)

BOARD ID[3:0]	MODE
1XXX	T202 DEV
0010	T208

BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

PAGE TITLE: **Camera/DFR 3**

BRANCH: **dvt-fab09-0**

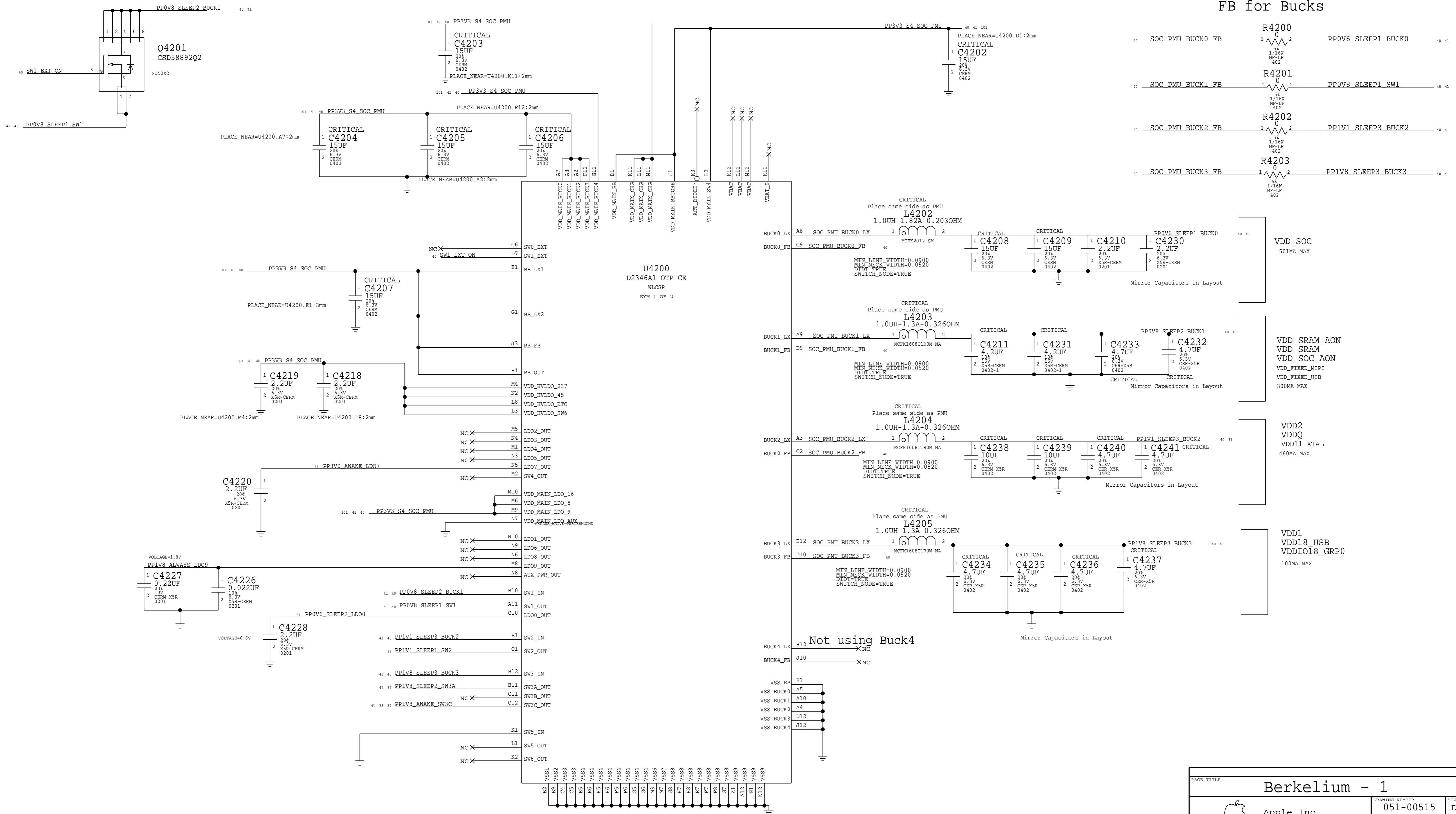
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REVISION: 9.0.0	BRANCH: dvt-fab09-0
PAGE: 41 OF 145	SHEET: 39 OF 119

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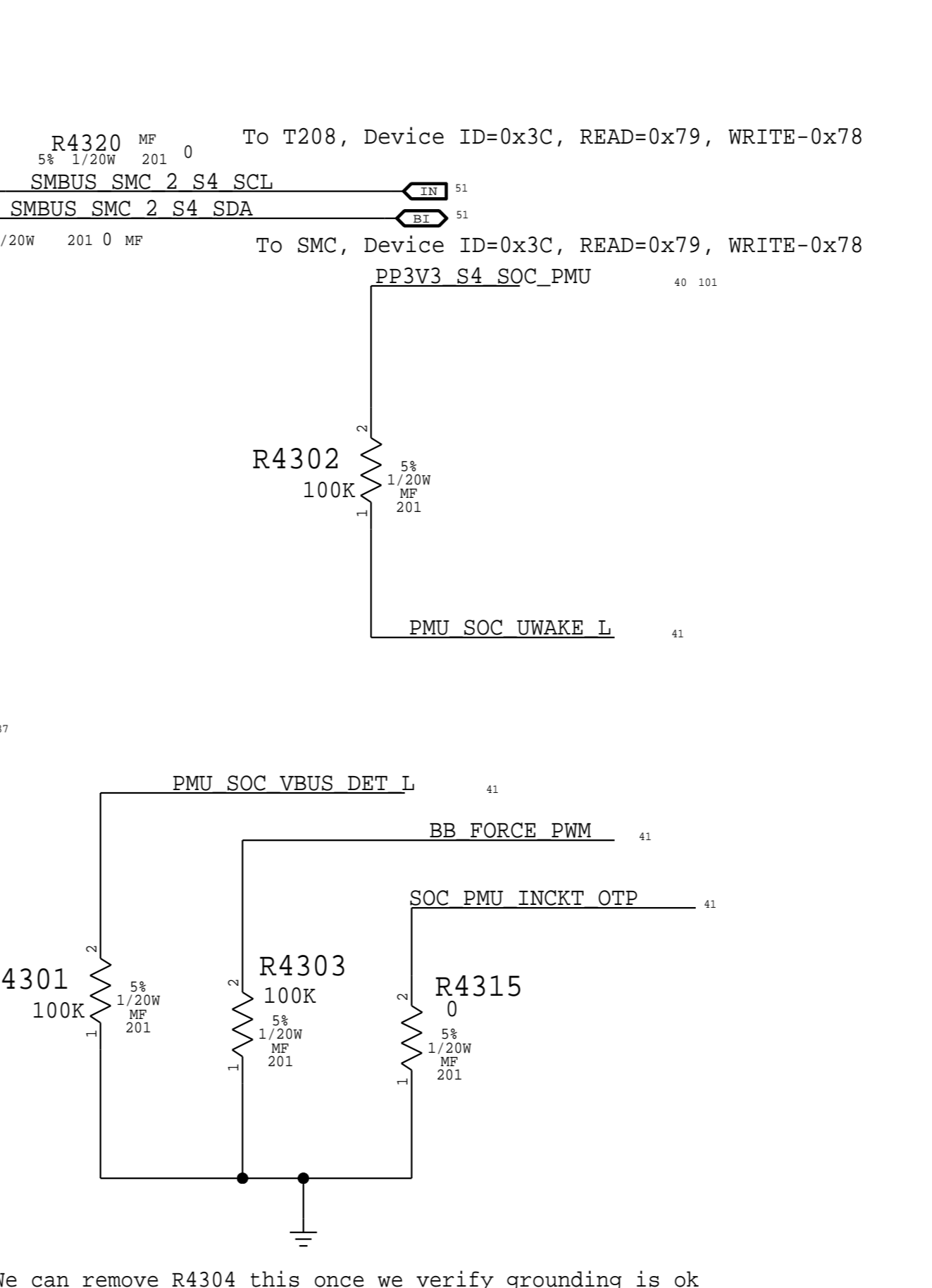
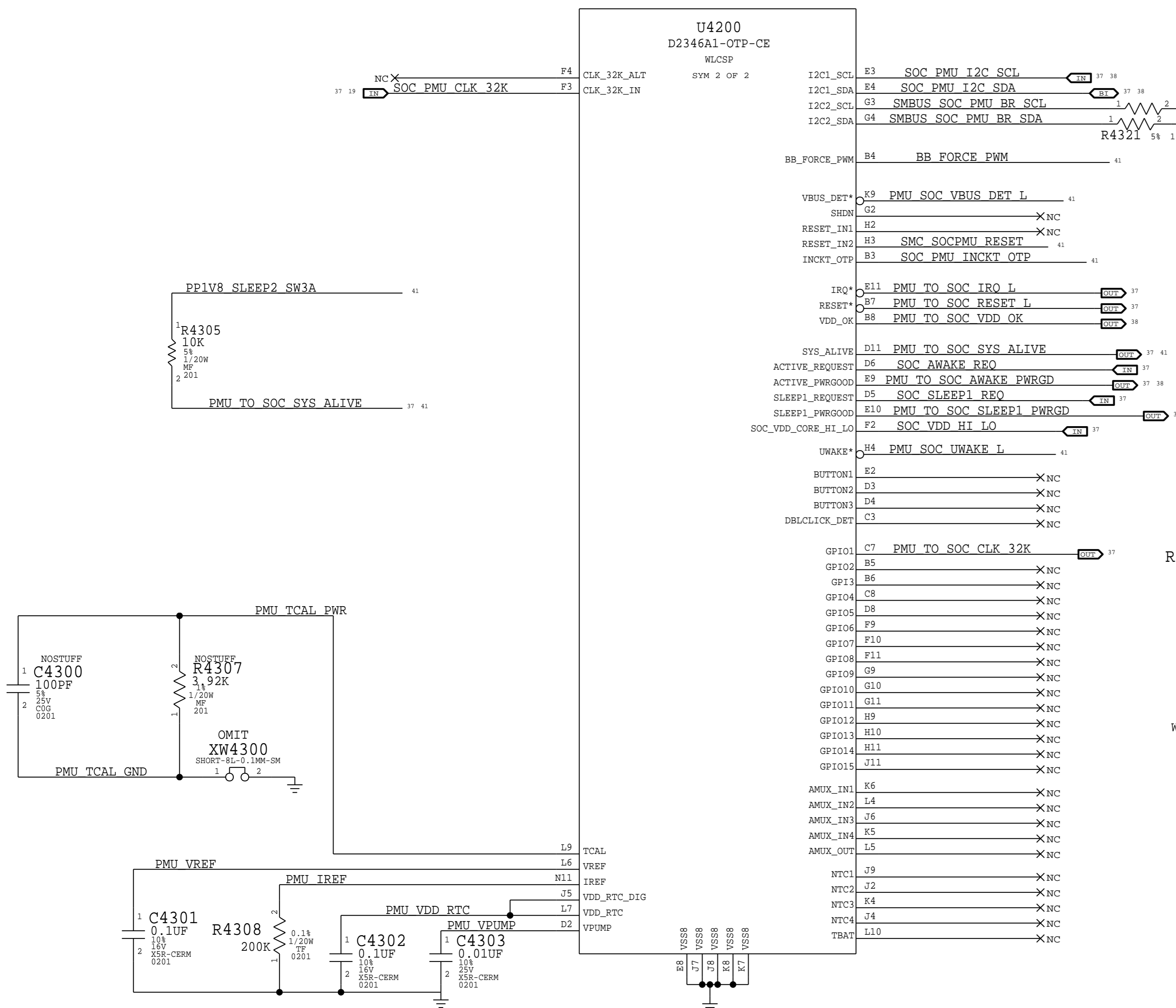
Berkelium

FB for Bucks

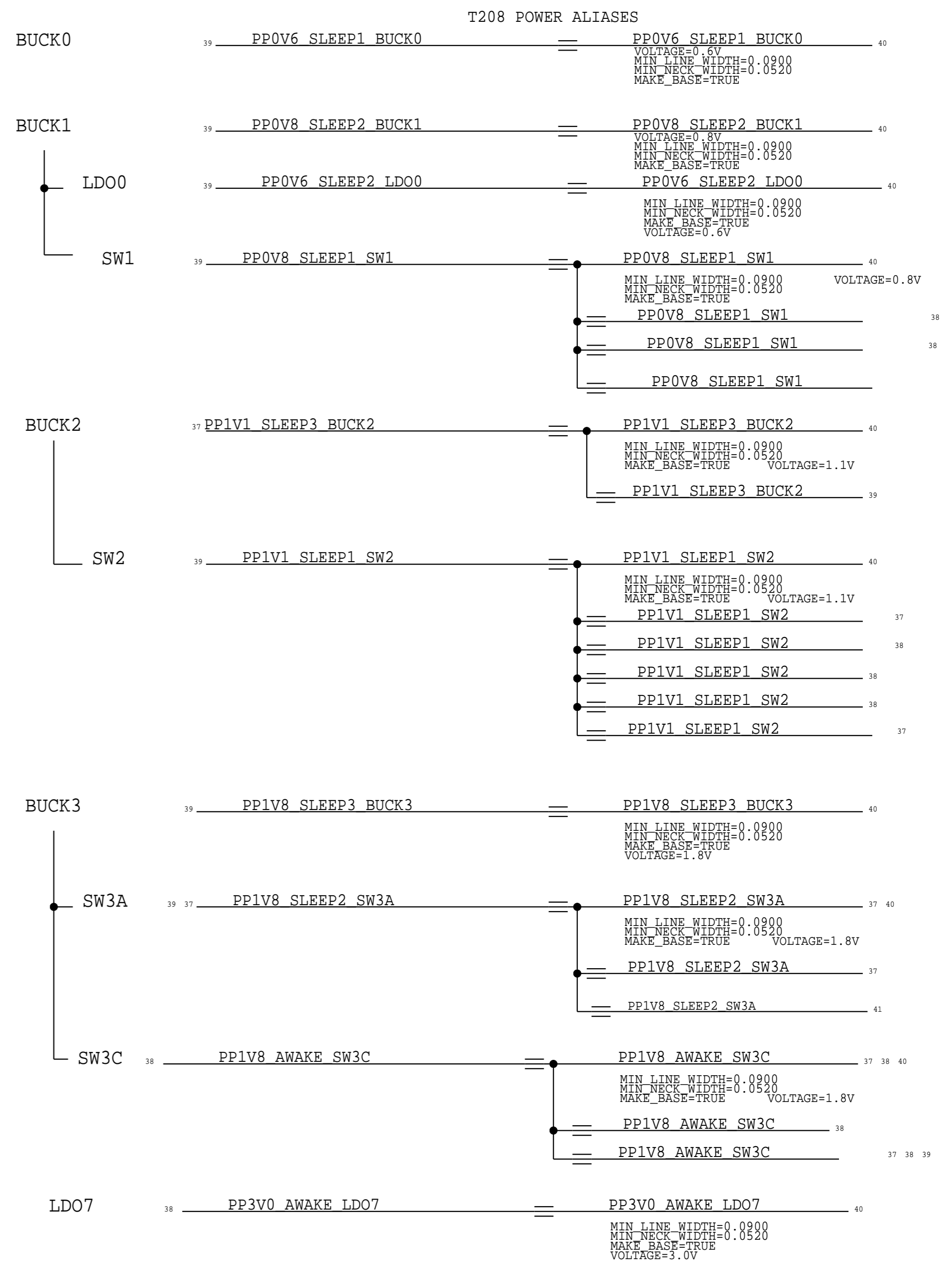


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	SHEET	40 OF 119
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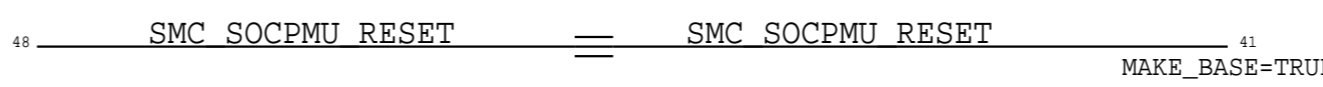
Berkelium - 2



We can remove R4304 this once we verify grounding is ok



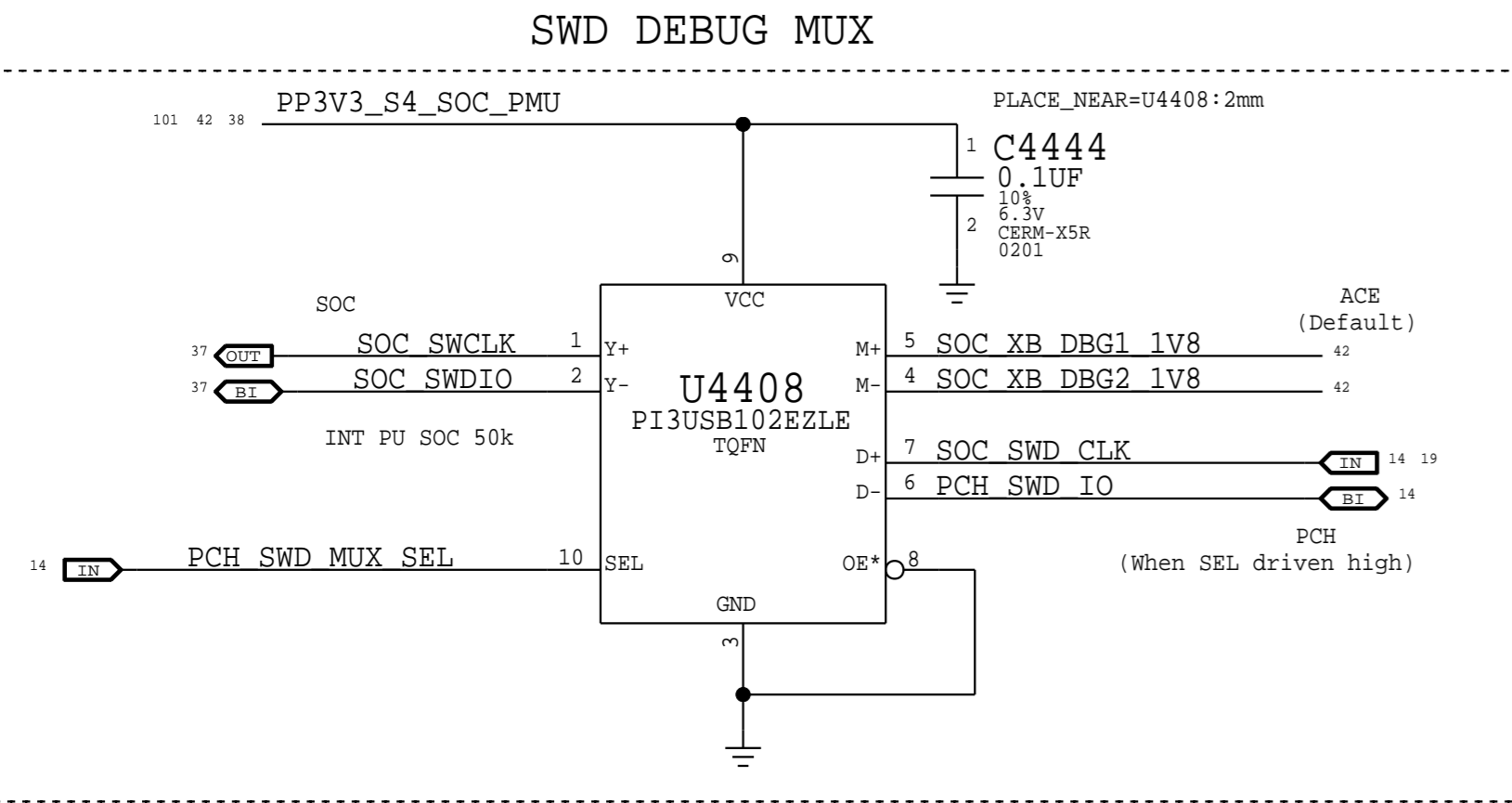
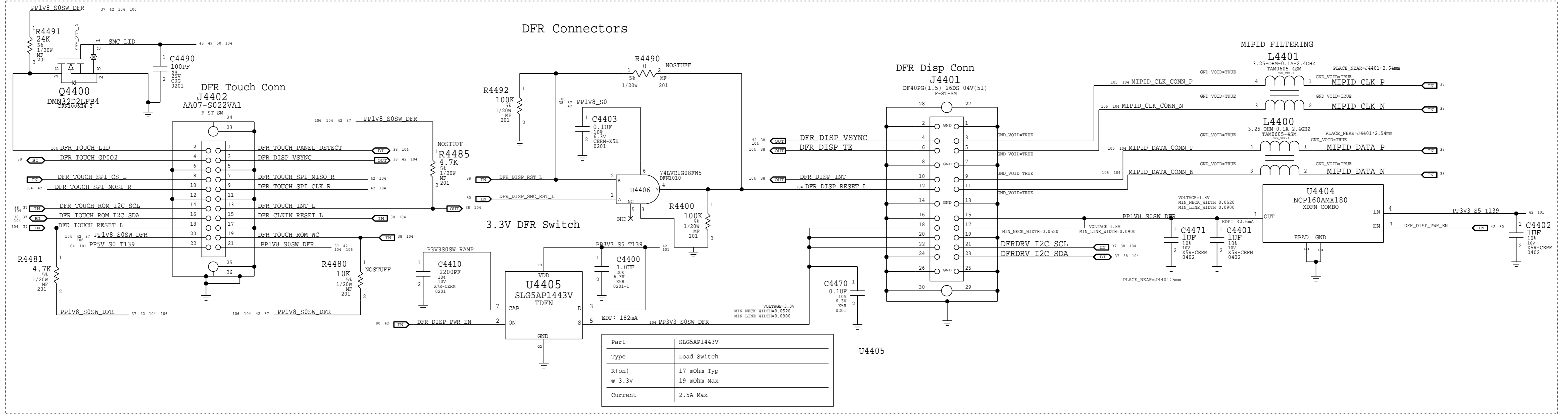
Signal Aliases



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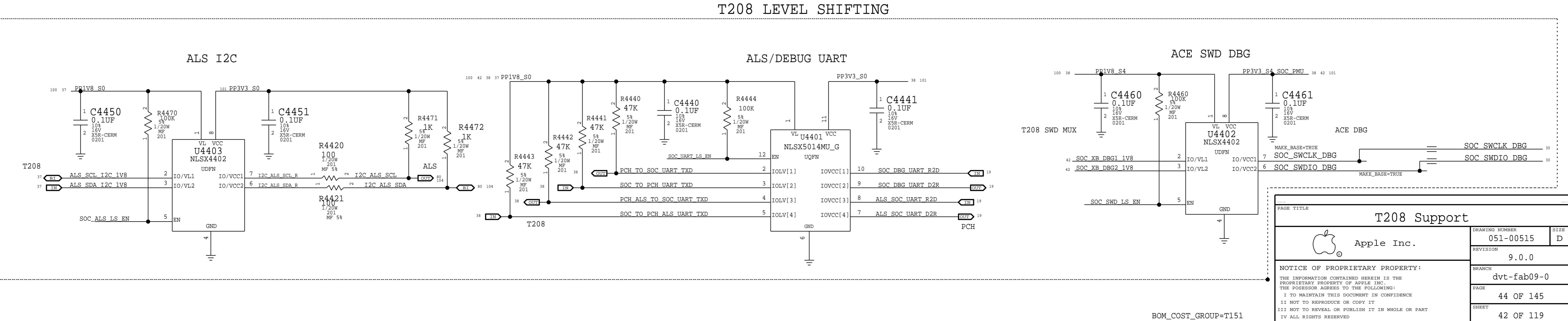
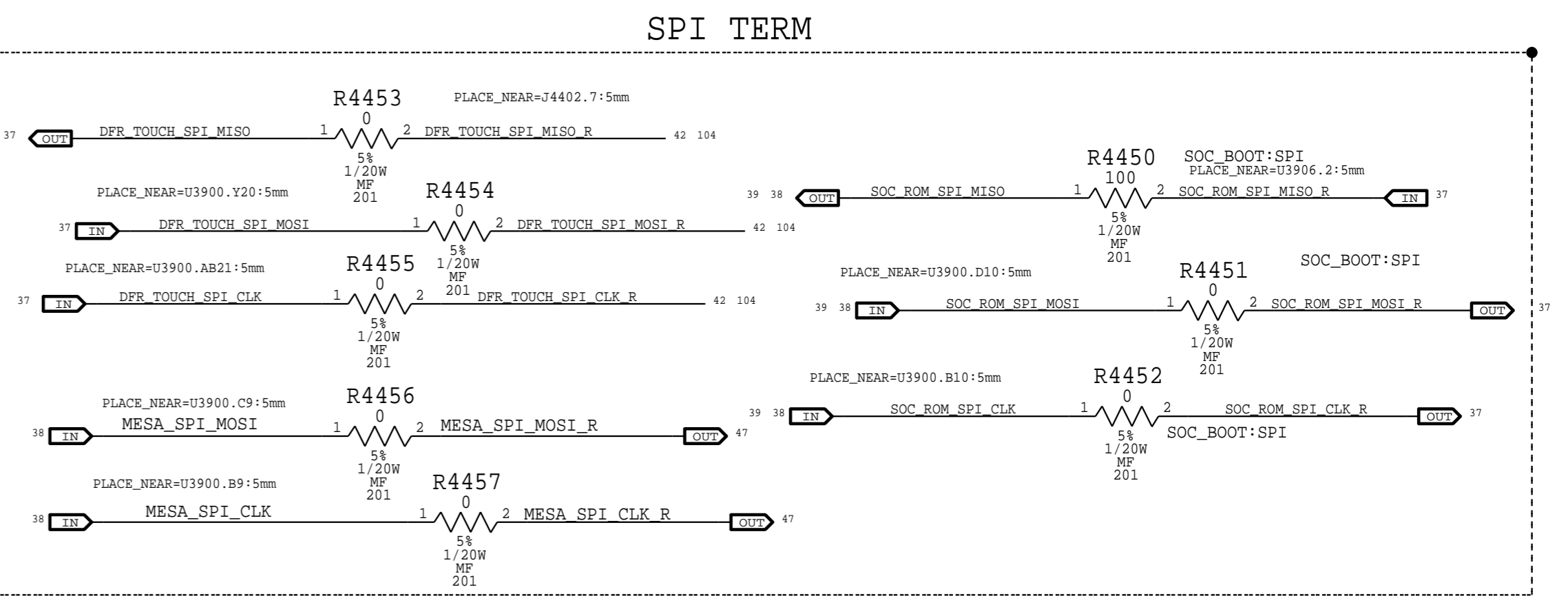
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T208 Support



T208 I2C Mapping

Bus	Device	7-bit Address	8-bit Address	
			Read	Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2



T208 Support

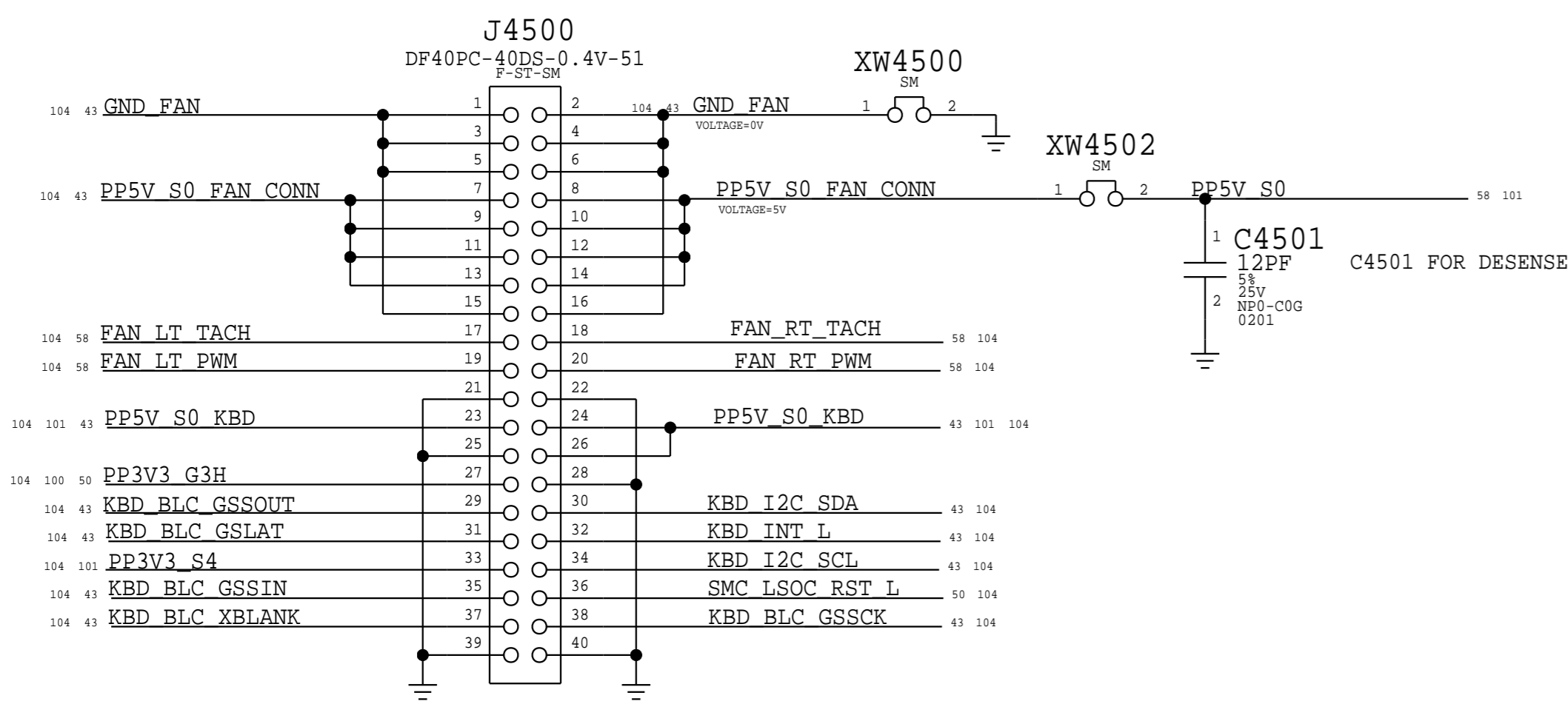
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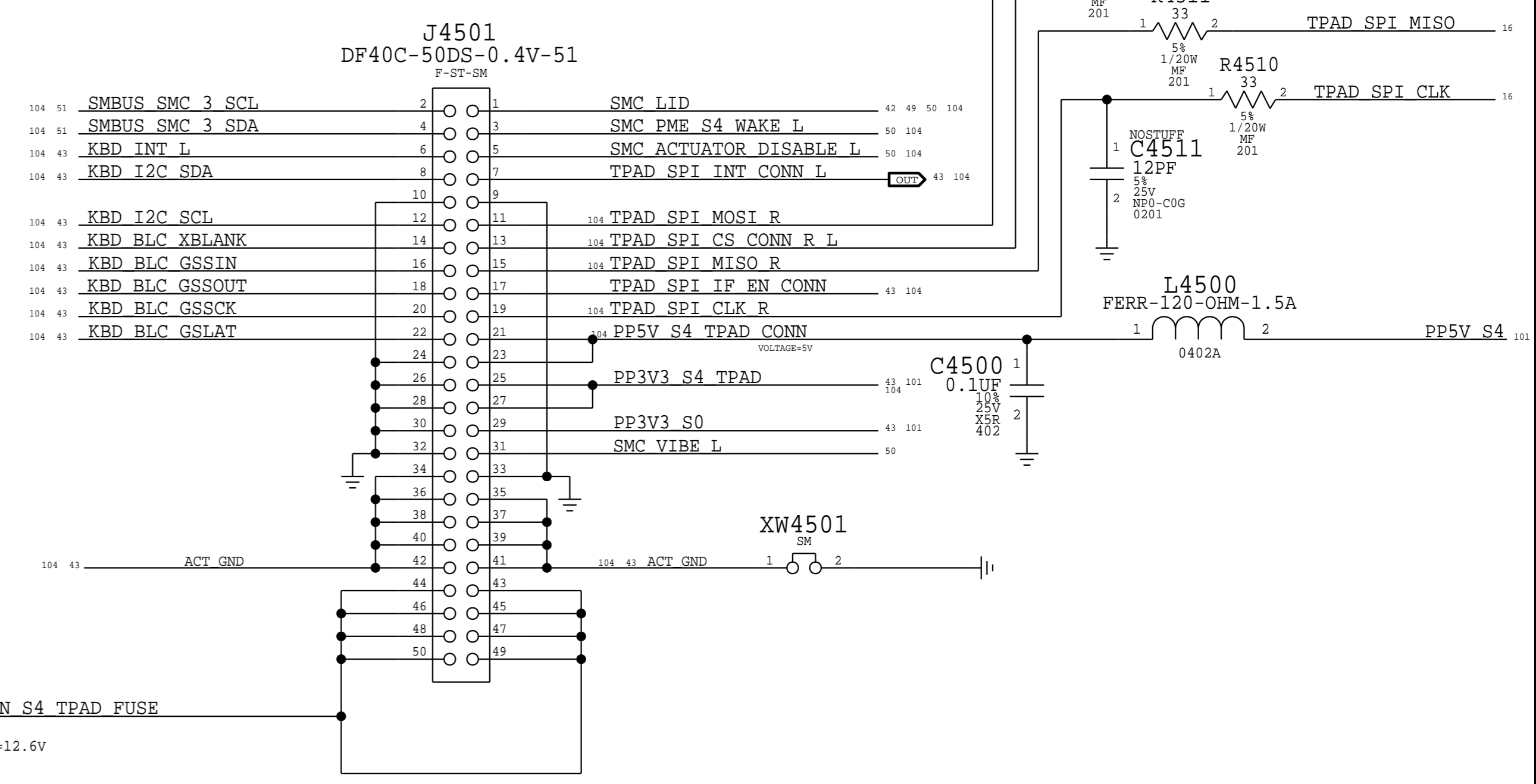
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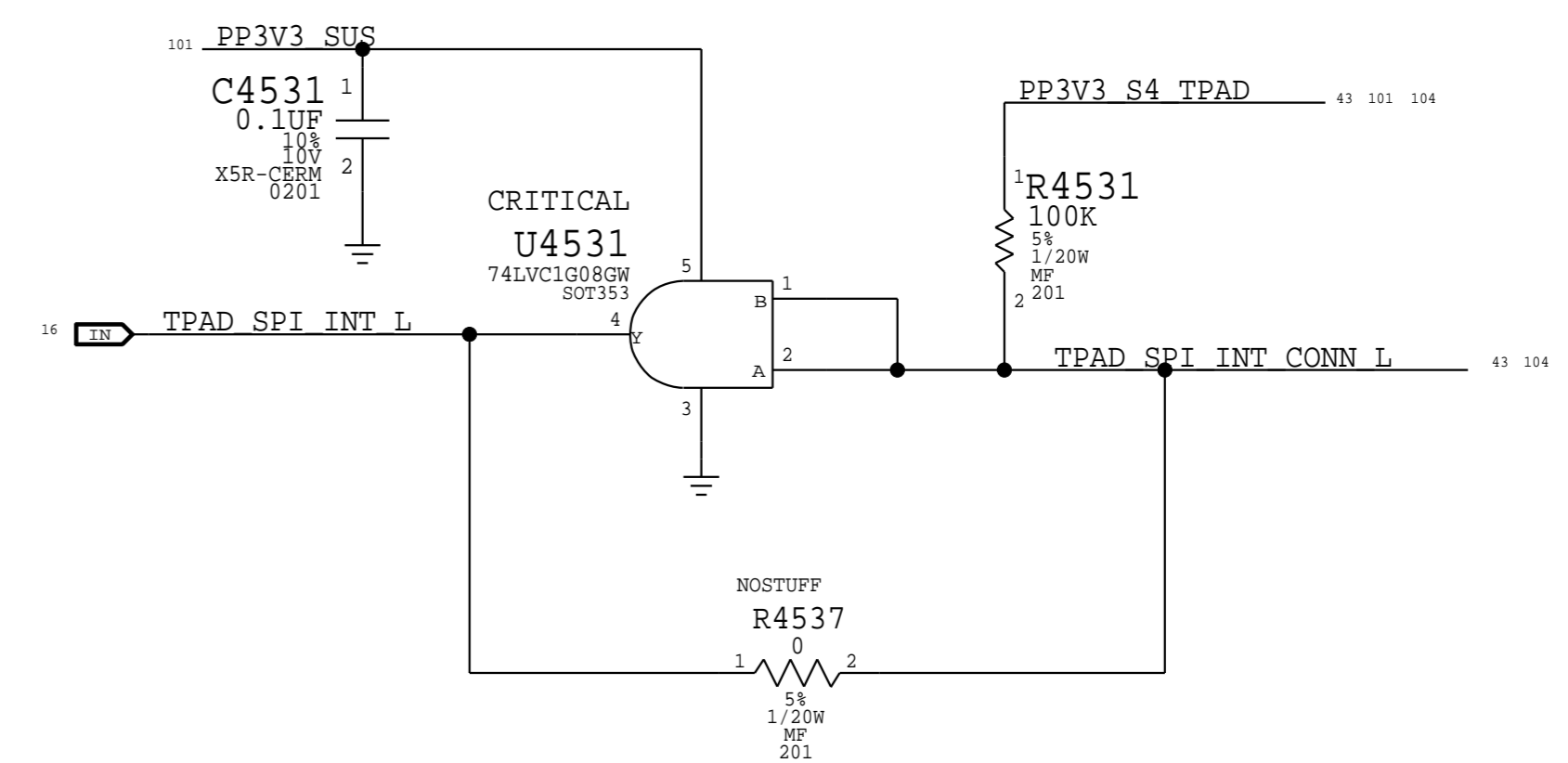
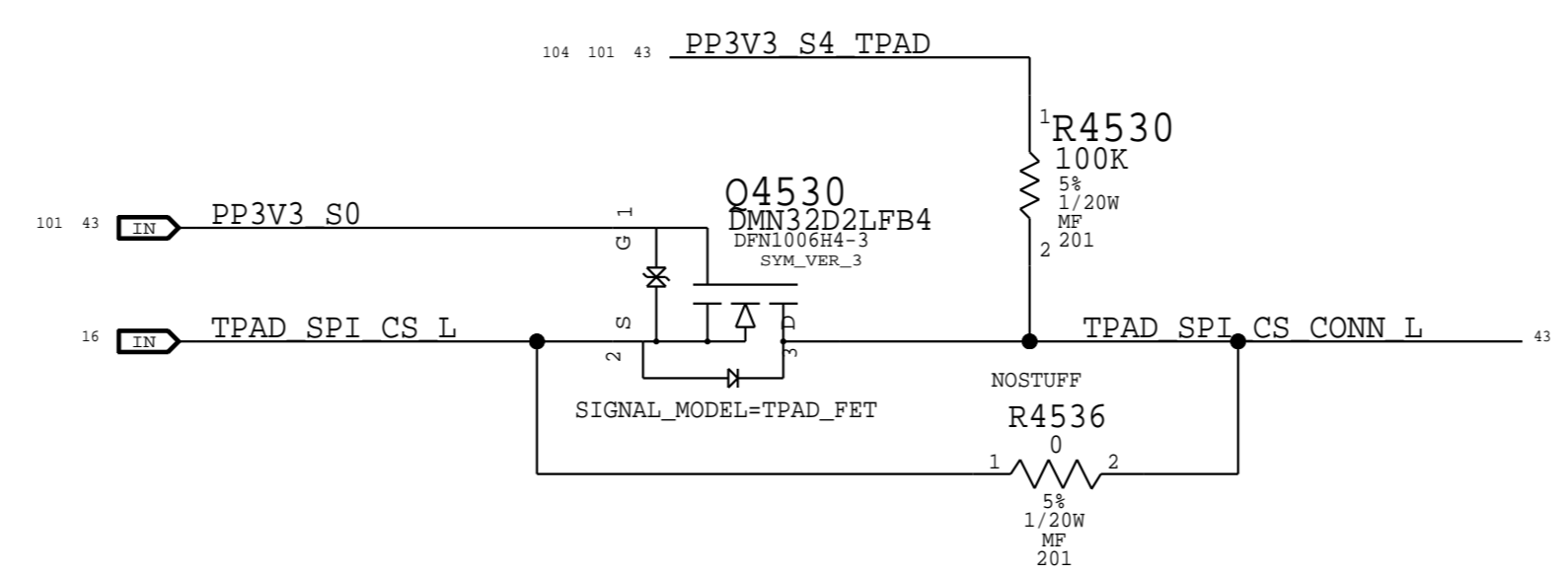
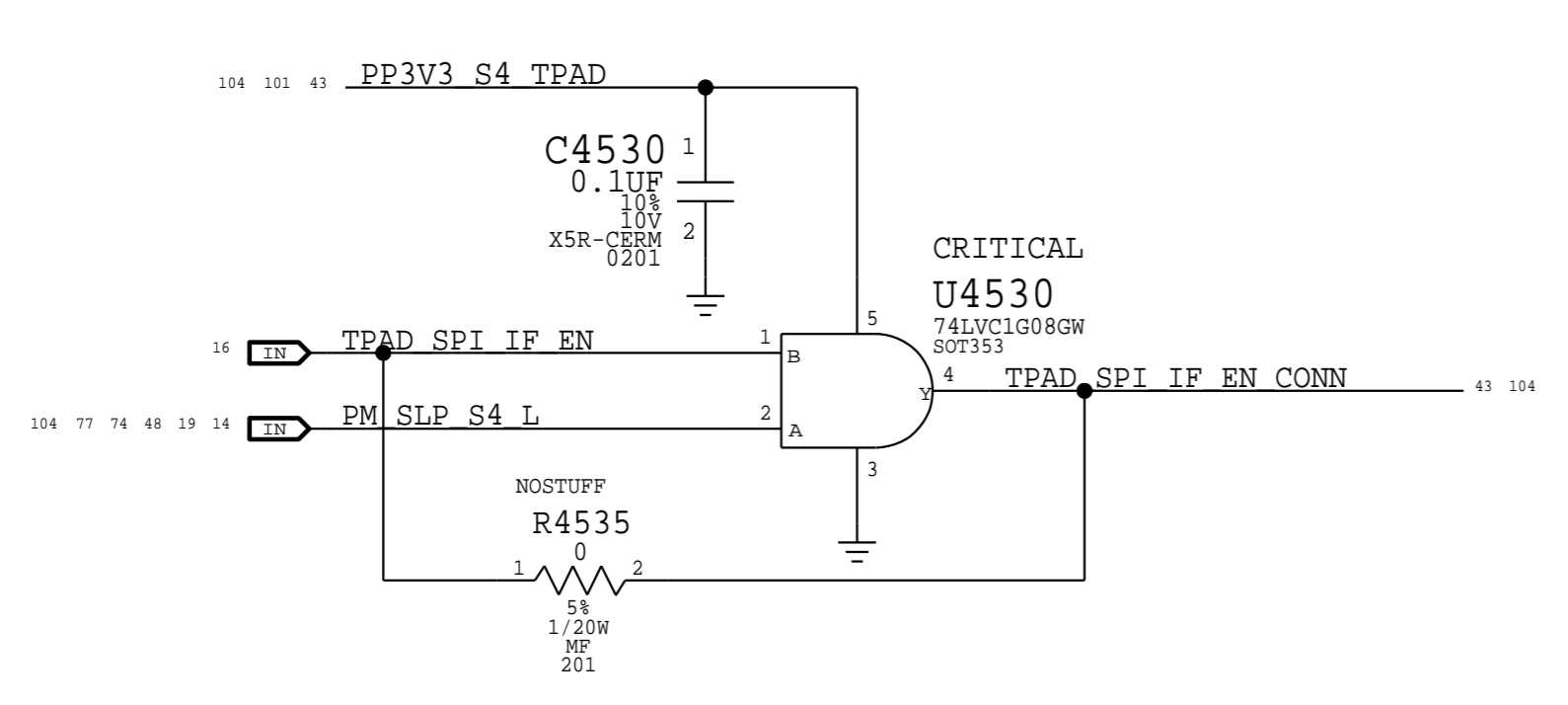
KBD CONNECTOR



TPAD CONNECTOR



TRACKPAD ISOLATION



EYNC_MASTER=79_GABN		EYNC_DATE=11/21/2015	
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Connectors&ESD			
 Apple Inc.	DRAWING NUMBER	051-00515	
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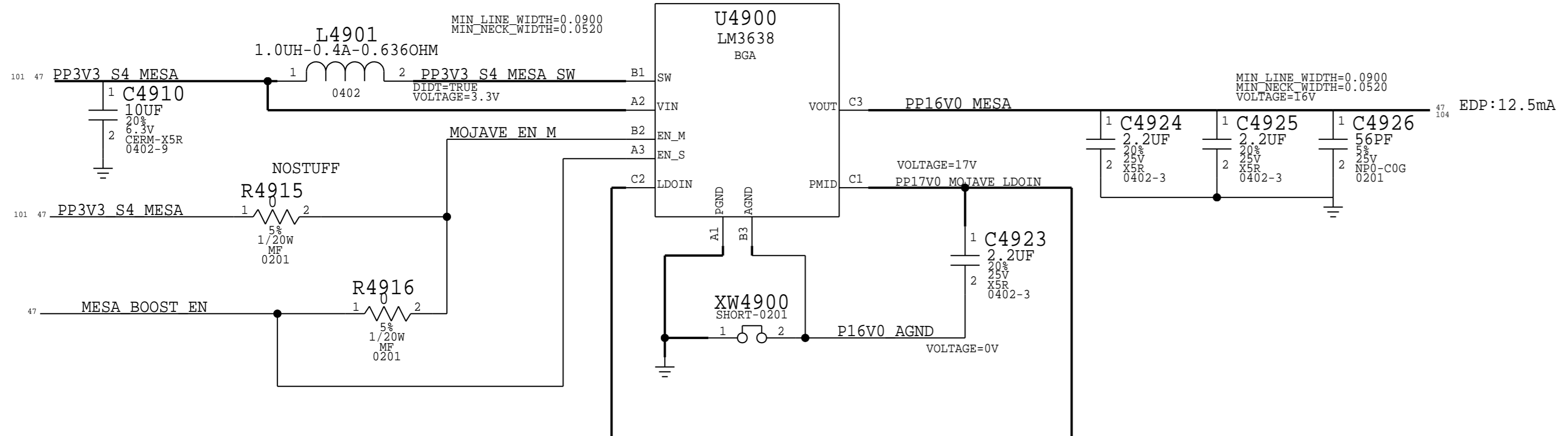
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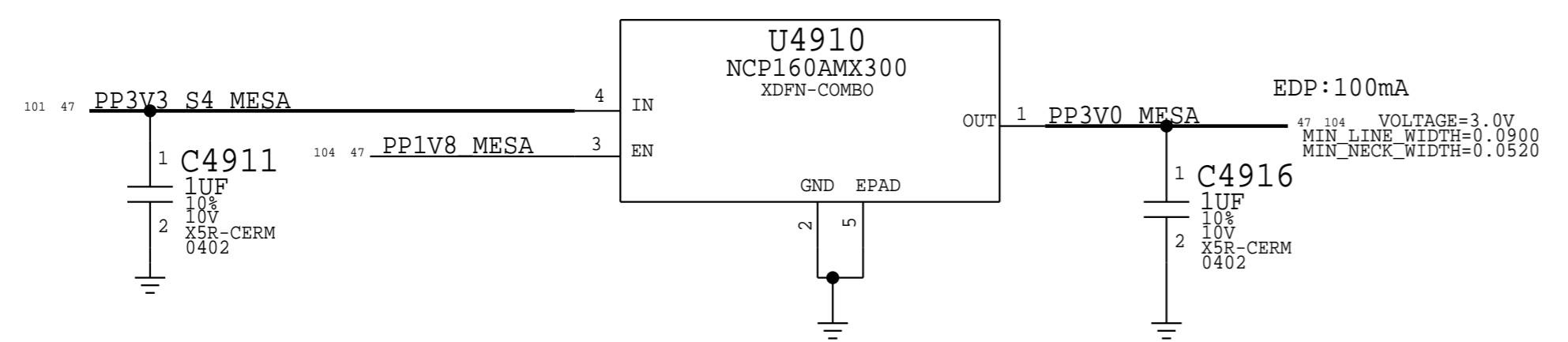
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

MOJAVE 16V BOOST

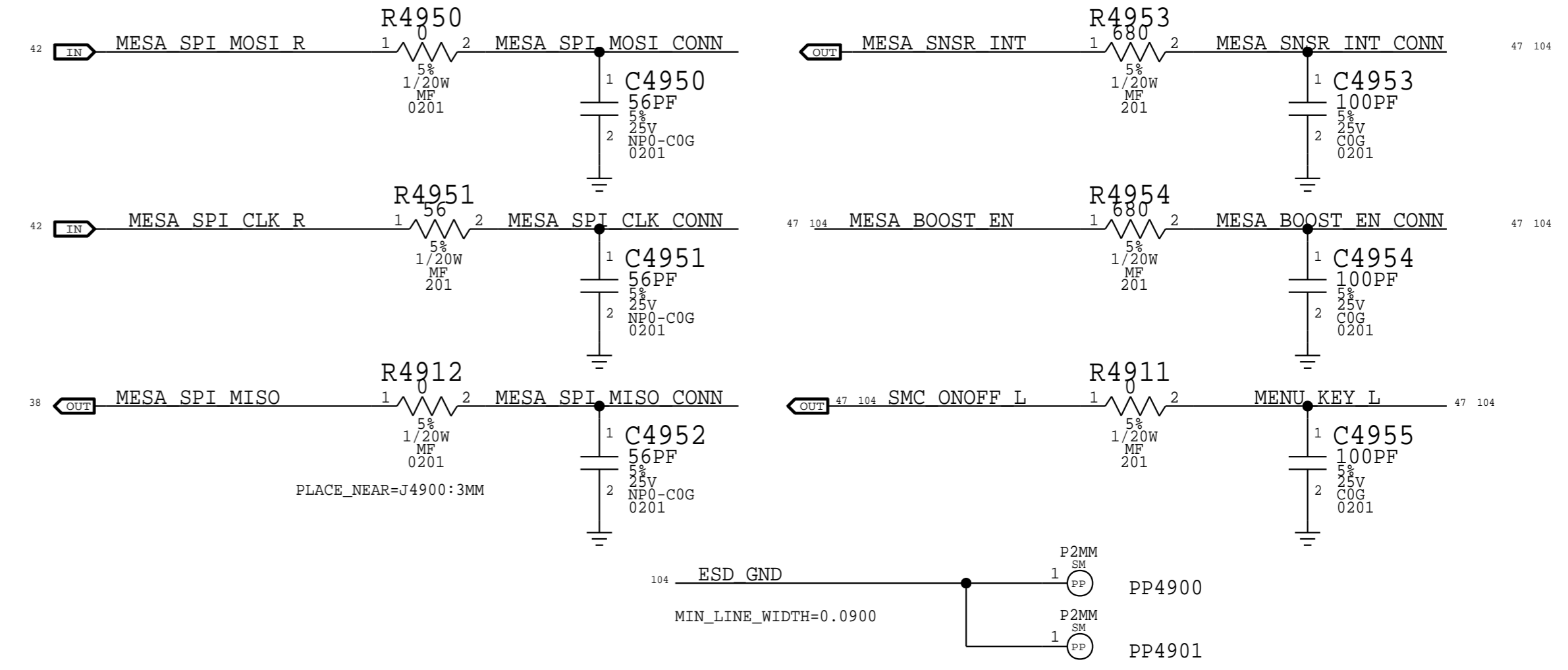
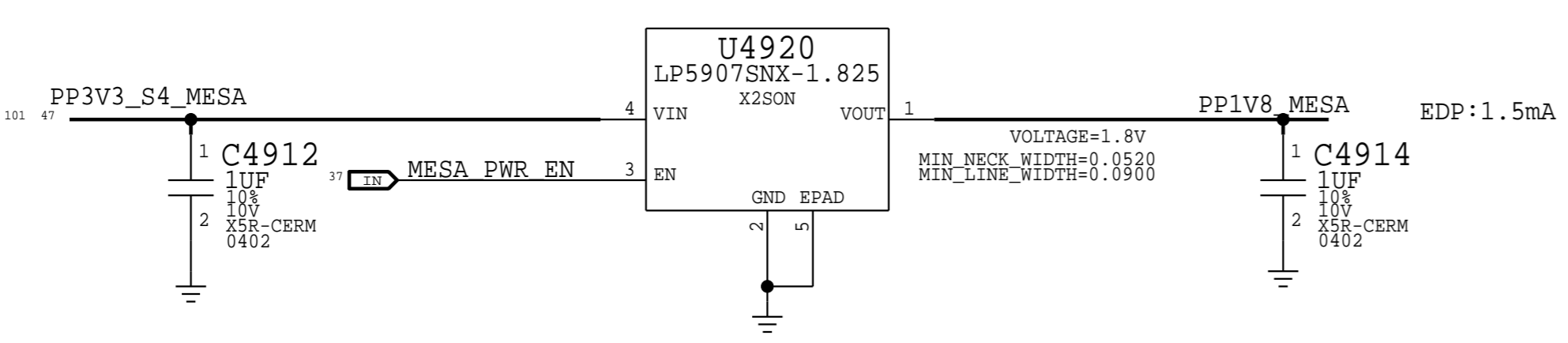


3.0V MESA

Option to feed LDO from 5V in case of dropout issue

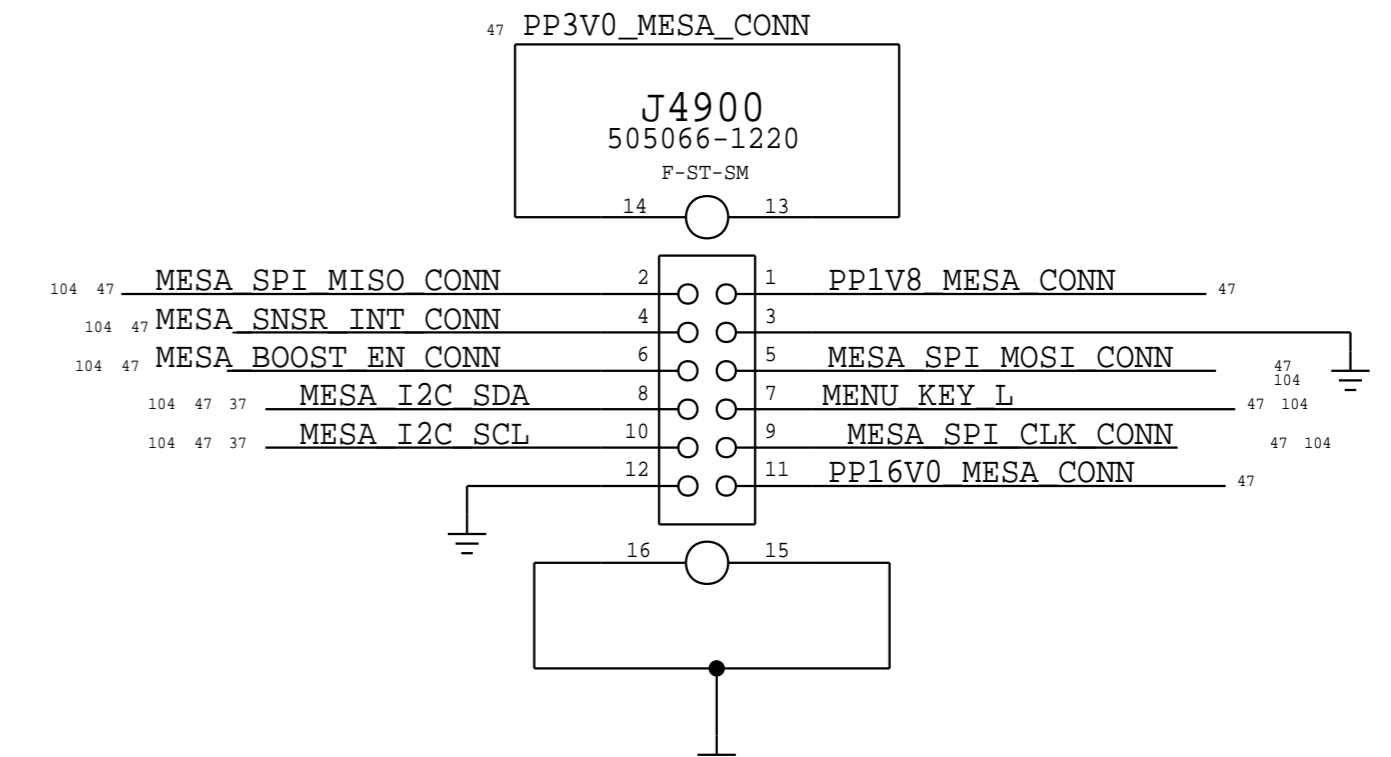


1.8V MESA



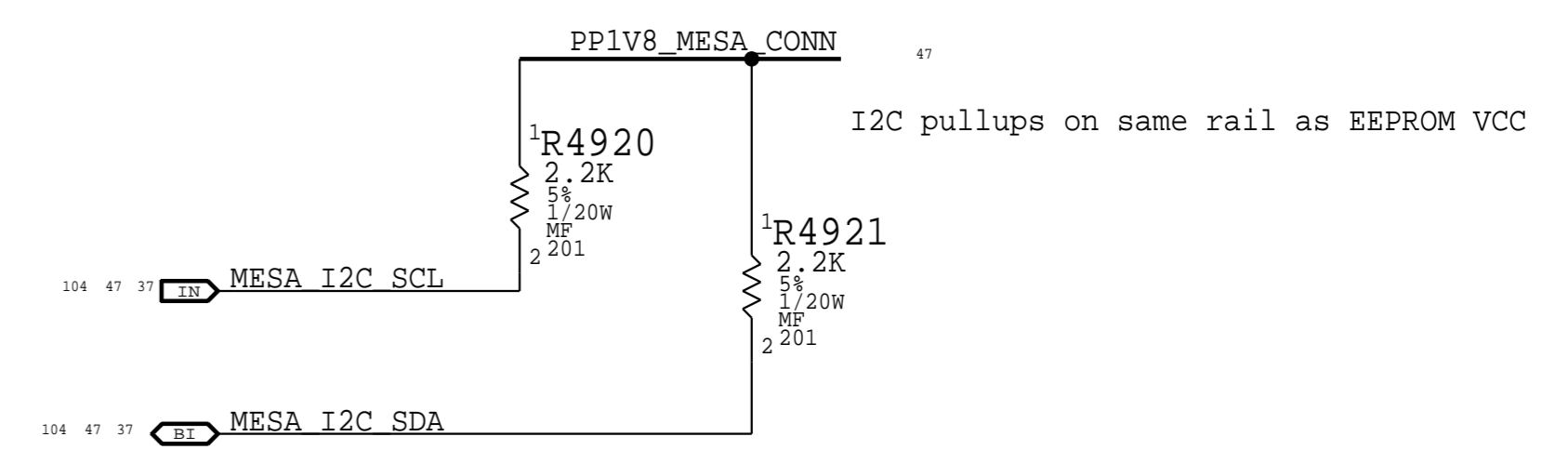
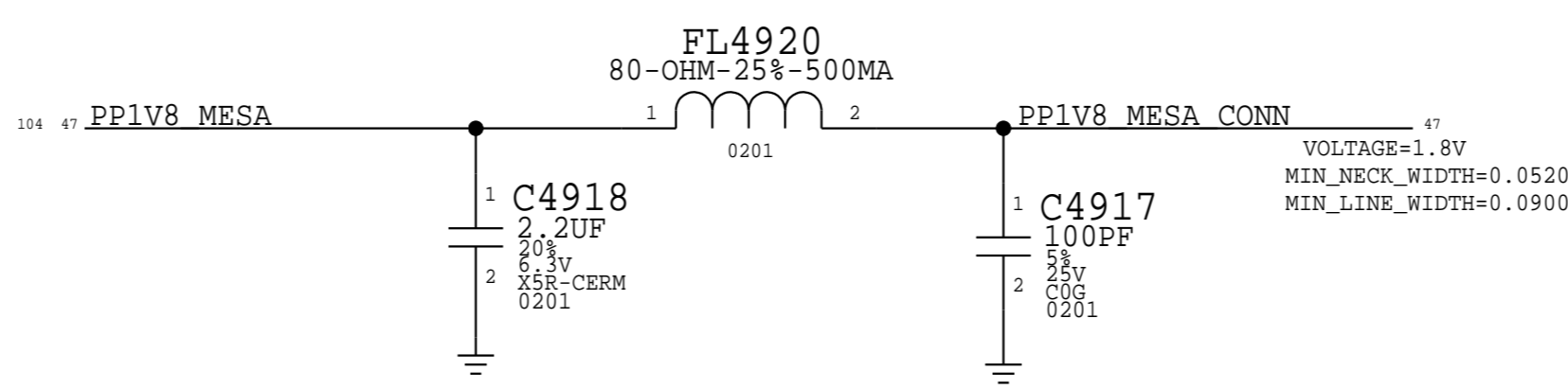
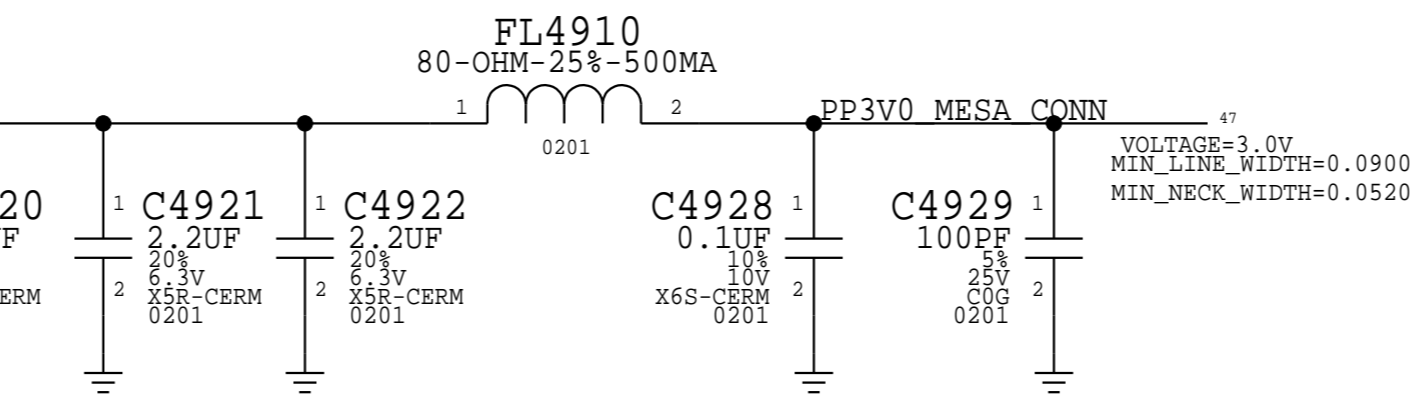
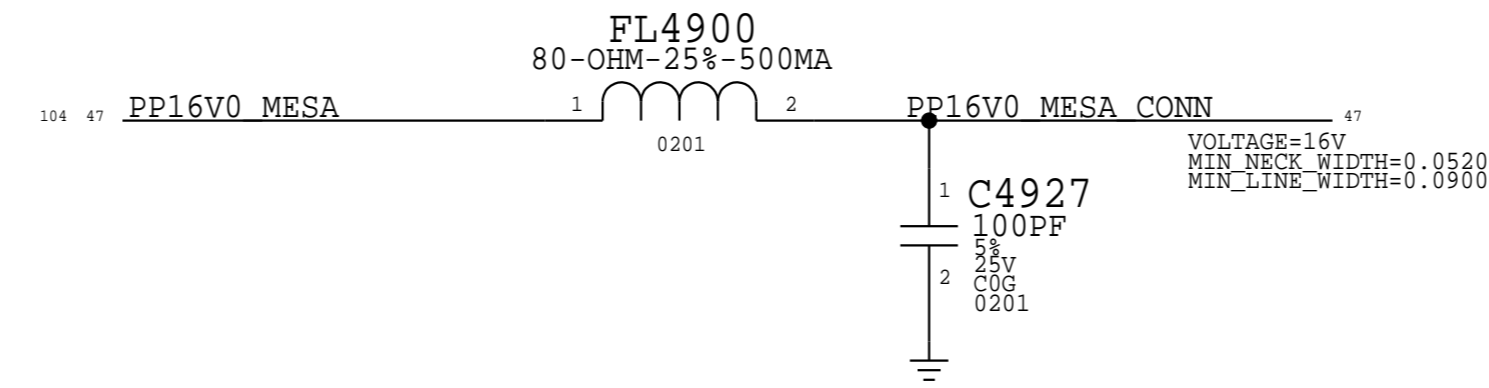
MESA FLEX CONNECTOR

Protol Connector for X434/X435 Support
 PLUG (516S00115) - X434/ X435 Jumper
 Rectacle (516S00203) - X362/X363 MLB



Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0



PAGE TITLE		MESA	
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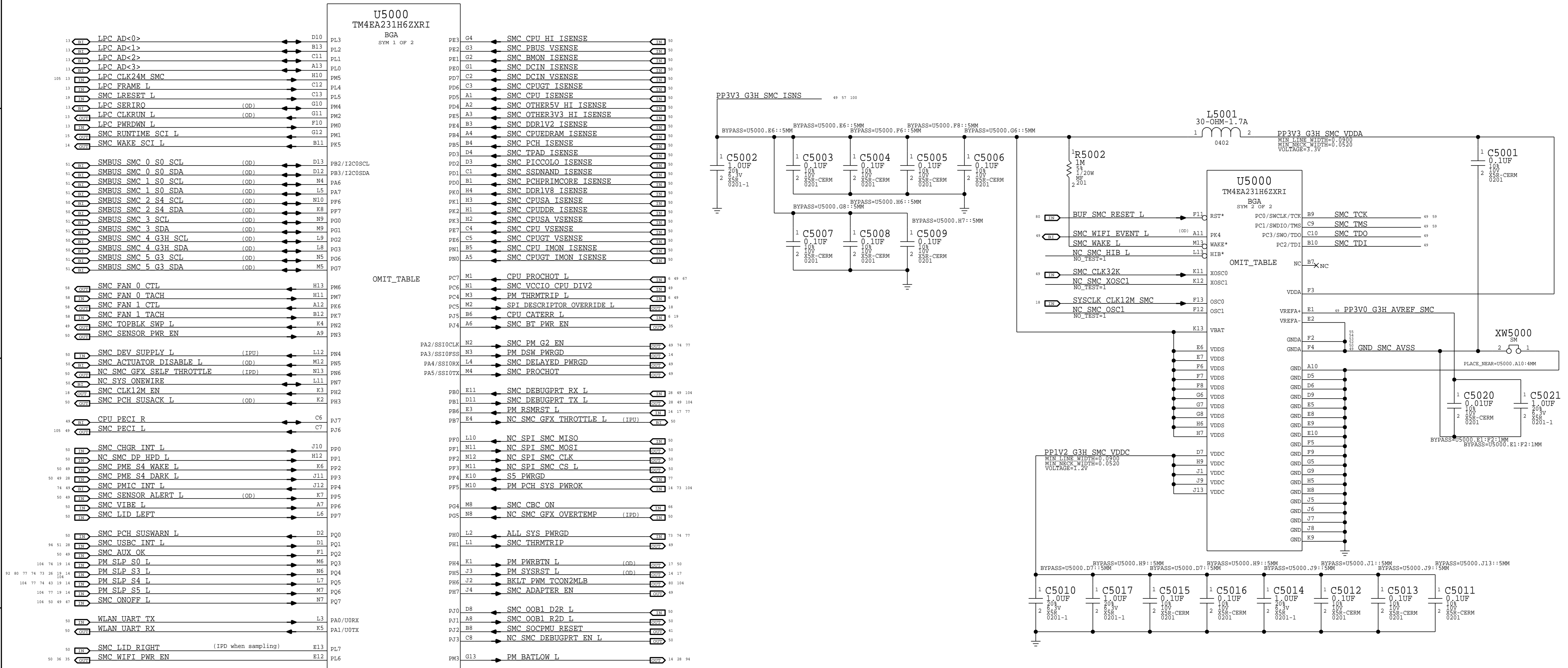
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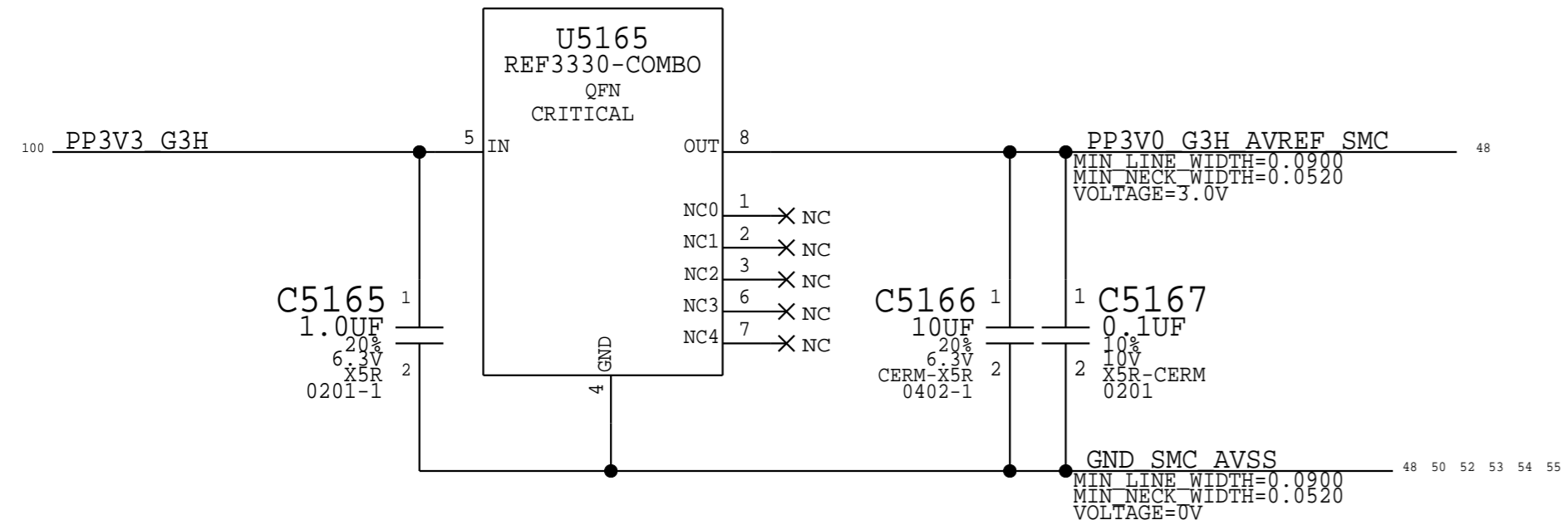
NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

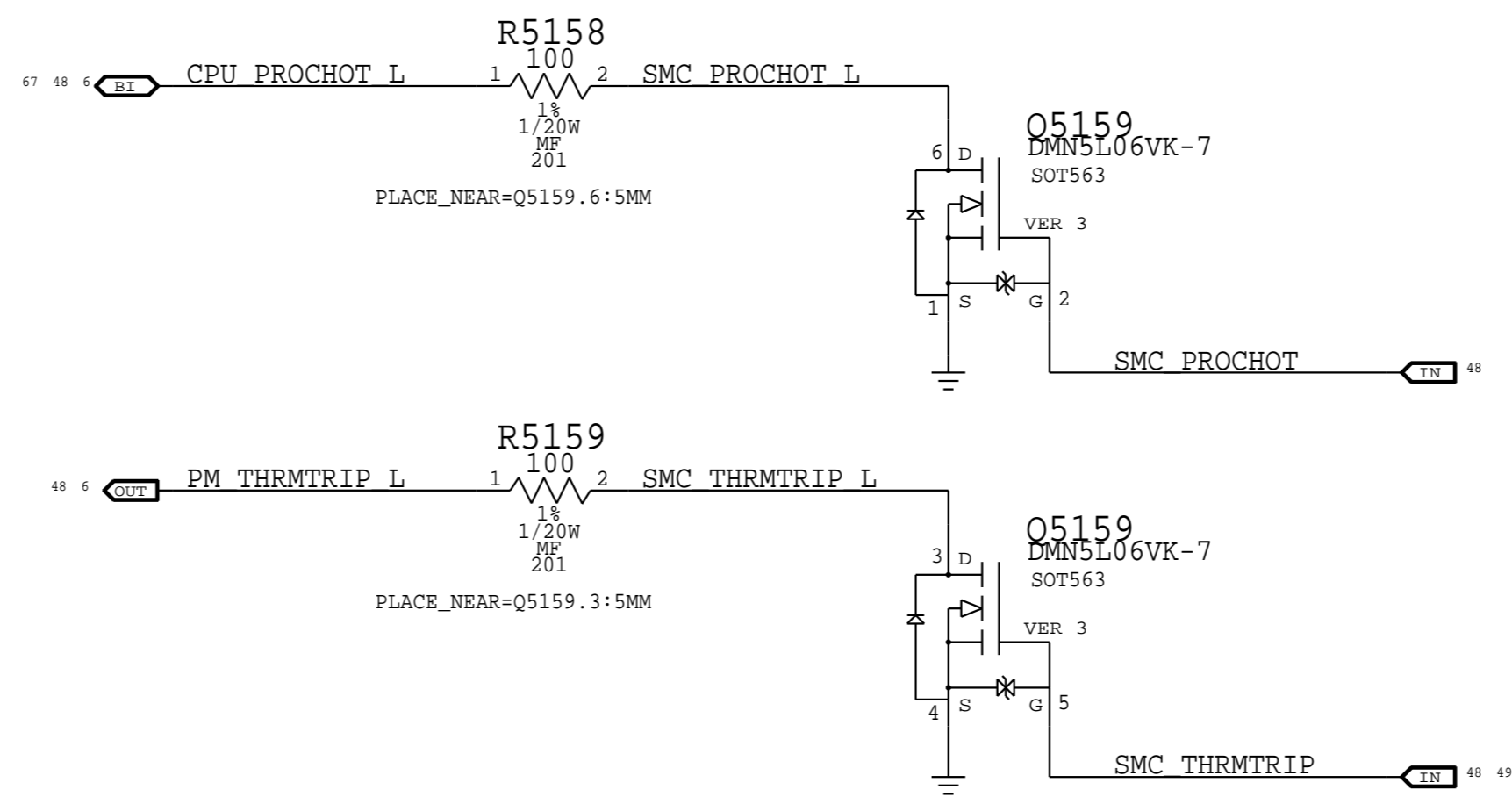
SMC	
	DRAWING NUMBER 051-00515
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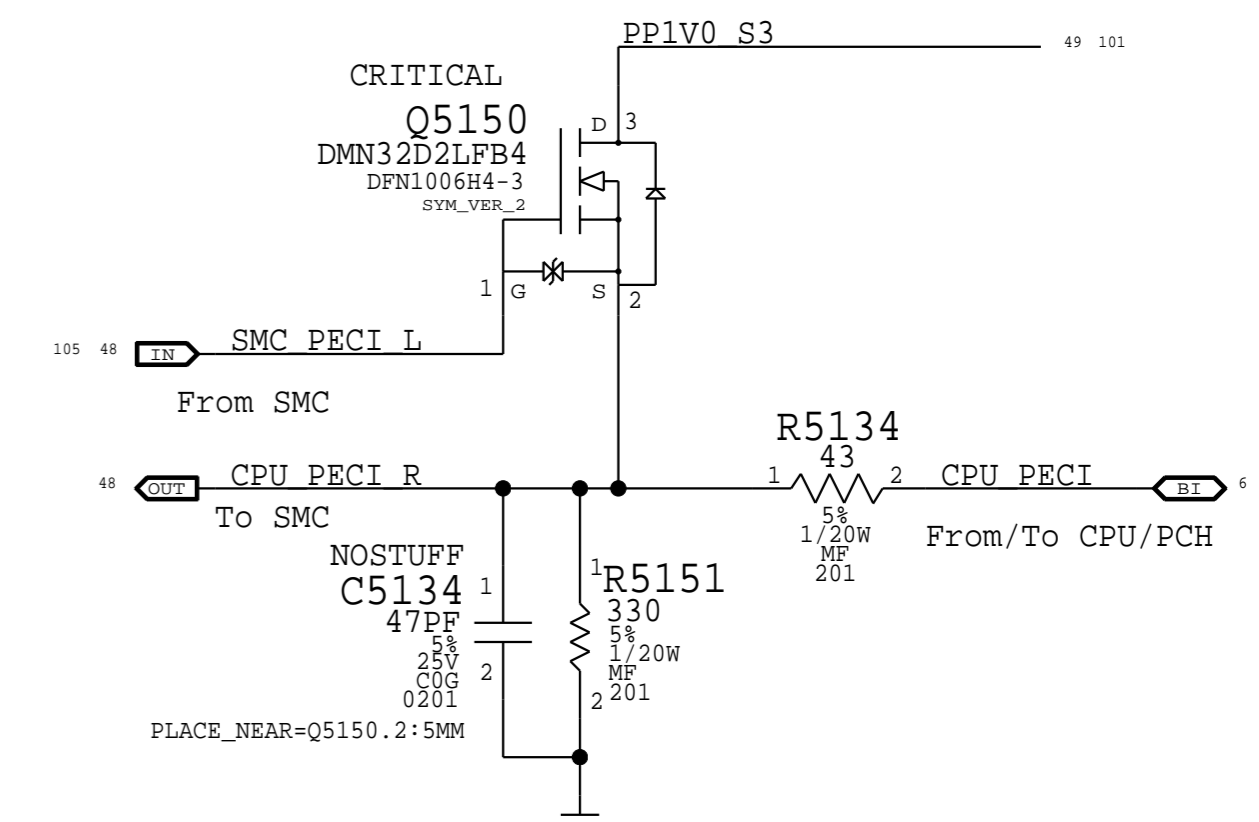
SMC AVREF Supply



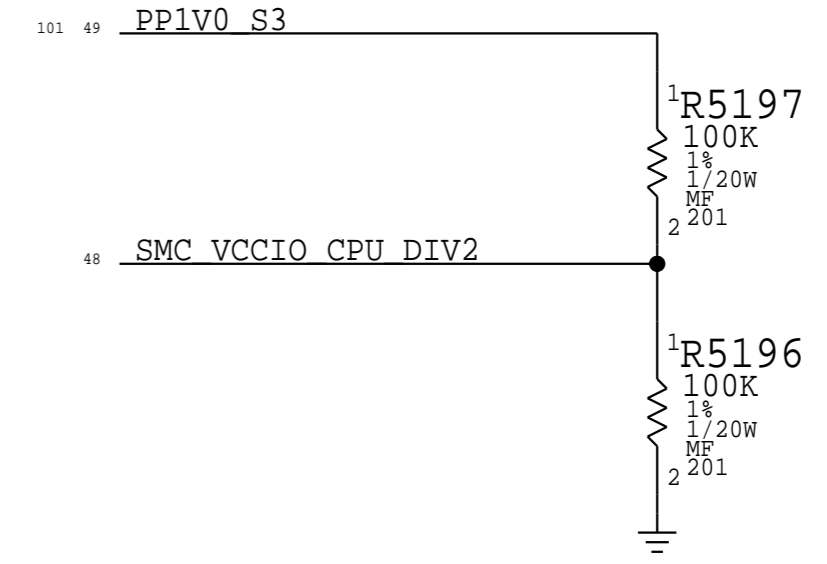
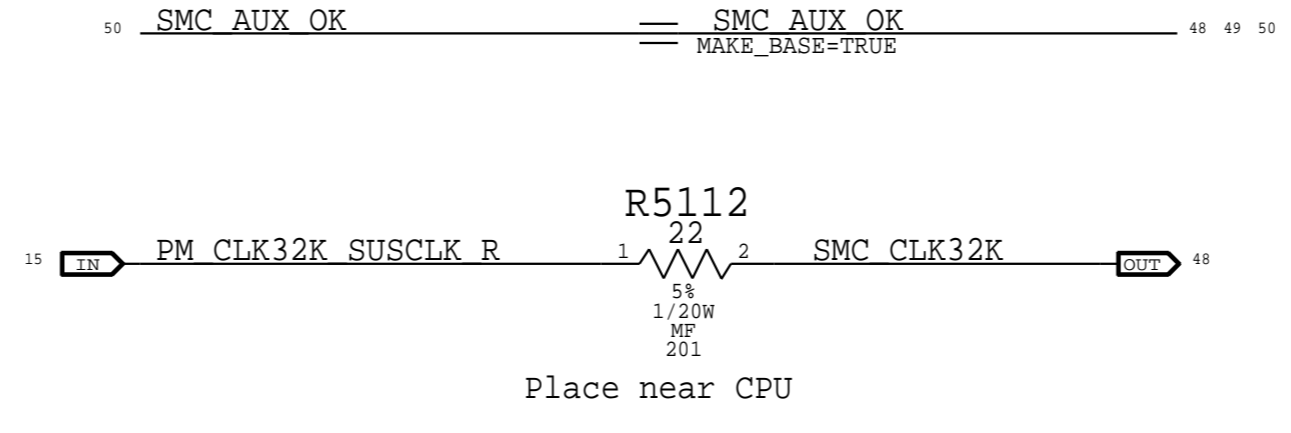
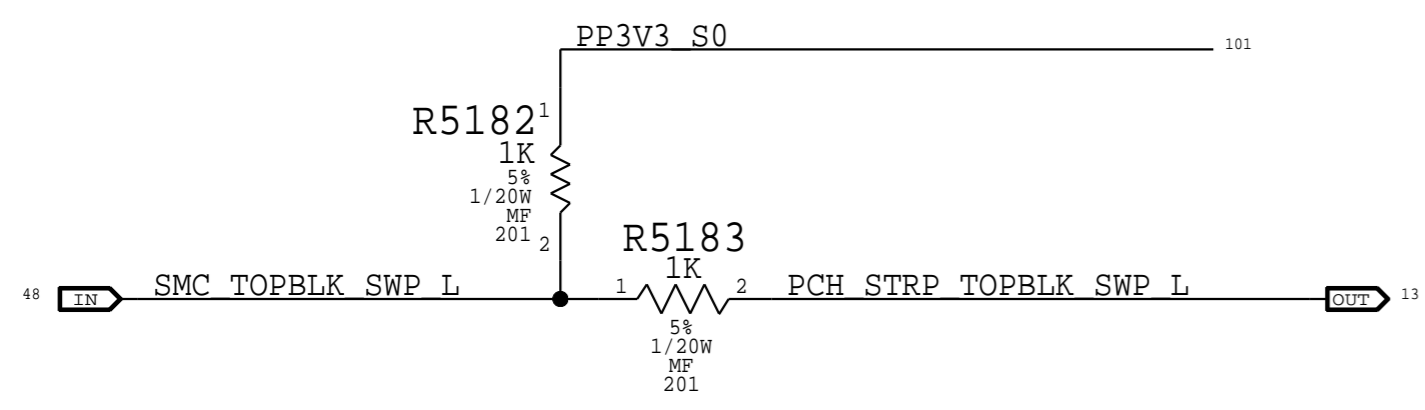
PROCHOT/THRMTRIP Support



PECI Support



Top-Block Swap



Pin	Signal	Value	Notes
100 57 48	PP3V3 G3H SMC ISNS		
101 50	PP3V3 S4		
101	PP3V3 S0		
50 48	SMC PME S4 WAKE L	R5166 100K 1	2 5% 1/20W MF 201
50 48 28	SMC PME S4 DARK L	R5167 100K 1	2 5% 1/20W MF 201
48	SMC WIFI EVENT L	R5168 100K 1	2 5% 1/20W MF 201
74 48	SMC PMIC INT L	R5169 100K 1	2 5% 1/20W MF 201
104 48 47	SMC ONOFF L	R5170 10K 1	2 5% 1/20W MF 201
50 48	SMC SENSOR ALERT L	R5172 10K 1	2 5% 1/20W MF 201
104 50 43 42	SMC LID	R5171 330K 1	2 5% 1/20W MF 201
104 48 28	SMC DEBUGPT TX L	R5175 20K 1	2 5% 1/20W MF 201
104 48 28	SMC DEBUGPT RX L	R5176 20K 1	2 5% 1/20W MF 201
59 48	SMC TMS	R5177 10K 1	2 5% 1/20W MF 201
48	SMC TDO	R5178 10K 1	2 5% 1/20W MF 201
48	SMC TDI	R5179 10K 1	2 5% 1/20W MF 201
59 48	SMC TCK	R5180 10K 1	2 5% 1/20W MF 201
50 48	SMC AUX OK	R5187 100K 1	2 5% 1/20W MF 201
48	SMC ADAPTER EN	R5185 100K 1	2 5% 1/20W MF 201
49 48	SMC THRMTRIP	R5186 10K 1	2 5% 1/20W MF 201
48 48	SMC DELAYED PWRGD	R5191 100K 1	2 5% 1/20W MF 201
77 74 48	SMC PM_G2_EN	R5192 100K 1	2 5% 1/20W MF 201

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SMC Shared Support			
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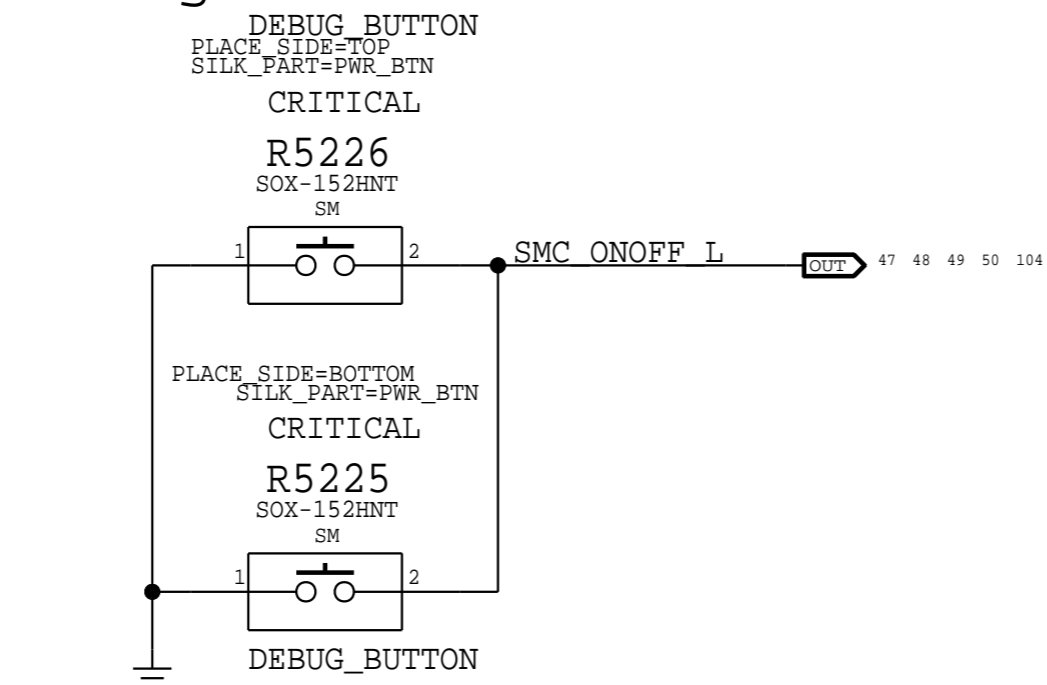
SMC12 ADC Assignments

SMC CPU HI ISENSE	==	SMC CPU HI ISENSE	IN	32
SMC PBUS VSENSE	==	SMC PBUS VSENSE	IN	32
SMC BMON ISENSE	==	SMC BMON ISENSE	IN	32
SMC DCIN ISENSE	==	SMC DCIN ISENSE	IN	32
SMC DCIN VSENSE	==	SMC DCIN VSENSE	IN	32
SMC CPUGT ISENSE	==	SMC CPUGT ISENSE	IN	35
SMC CPU ISENSE	==	SMC CPU ISENSE	IN	33
SMC OTHER5V HI ISENSE	==	SMC OTHER5V HI ISENSE	IN	32
SMC OTHER3V3 HI ISENSE	==	SMC OTHER3V3 HI ISENSE	IN	32
SMC DDR1V2 ISENSE	==	SMC DDR1V2 ISENSE	IN	33
SMC CPUEDRAM ISENSE	==	SMC CPUEDRAM ISENSE	IN	35
SMC PCH ISENSE	==	SMC PCH ISENSE	IN	33
SMC TPAD ISENSE	==	SMC TPAD ISENSE	IN	32
SMC PICCOLO ISENSE	==	SMC PICCOLO ISENSE	IN	32
SMC SSDNAND ISENSE	==	SMC SSDNAND ISENSE	IN	35
SMC PCHPRIMCORE ISENSE	==	SMC PCHPRIMCORE ISENSE	IN	35
SMC DDR1V8 ISENSE	==	SMC DDR1V8 ISENSE	IN	35
SMC CPUSA ISENSE	==	SMC CPUSA ISENSE	IN	35
SMC CPUDDR ISENSE	==	SMC CPUDDR ISENSE	IN	33
SMC CPUSA VSENSE	==	SMC CPUSA VSENSE	IN	35
SMC CPU VSENSE	==	SMC CPU VSENSE	IN	34
SMC CPUGT VSENSE	==	SMC CPUGT VSENSE	IN	34
SMC CPU IMON ISENSE	==	SMC CPU IMON ISENSE	IN	34
SMC CPUGT IMON ISENSE	==	SMC CPUGT IMON ISENSE	IN	34

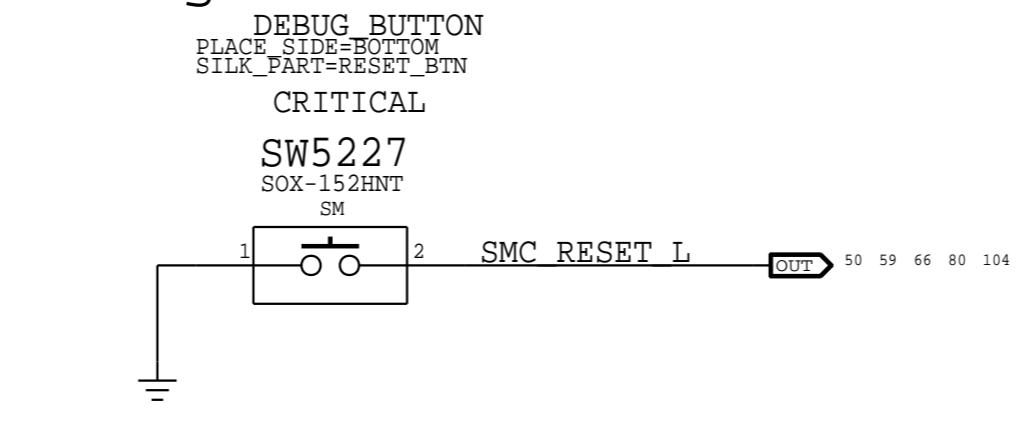
SMC12 Pin Assignments

NC SMC GFX THROTTLE L	==	NC SMC GFX THROTTLE L	NO_TEST=1	
NC SMC GFX OVERTEMP	==	NC SMC GFX OVERTEMP	NO_TEST=1	
NC SMC GFX SELF THROTTLE	==	NC SMC GFX SELF THROTTLE	NO_TEST=1	
NC SMC DP HPD L	==	NC SMC DP HPD L	NO_TEST=1	
NC SYS ONEWIRE	==	NC SYS ONEWIRE	NO_TEST=1	
NC SMC DEBUGPRT EN L	==	NC SMC DEBUGPRT EN L	NO_TEST=1	
SMC LID RIGHT	==	SMC LID RIGHT		50
NC SPI SMC MISO	==	NC SPI SMC MISO	NO_TEST=1	TRUE
NC SPI SMC MOSI	==	NC SPI SMC MOSI	NO_TEST=1	TRUE
NC SPI SMC CLK	==	NC SPI SMC CLK	NO_TEST=1	TRUE
NC SPI SMC CS L	==	NC SPI SMC CS L	NO_TEST=1	TRUE
SMC VIBE L	==	SMC VIBE L		43
SMC PCH SUSWARN L	==	SMC PCH SUSWARN L		14
SMC PCH SUSACK L	==	SMC PCH SUSACK L		14
SMC SENSOR PWR EN	==	SMC SENSOR PWR EN		70
WLAN UART RX	==	WLAN UART RX		35
WLAN UART TX	==	WLAN UART TX		35
SMC AUX OK	==	SMC AUX OK		49
PM PWRBTN L	==	PM PWRBTN L		14
SMC AUX OK	==	SMC AUX OK		52
SMBUS SMC 4 G3H SCL	==	SMBUS SMC 4 G3H SCL		48
SMBUS SMC 4 G3H SDA	==	SMBUS SMC 4 G3H SDA		48
SMBUS SMC 2 S4 SCL	==	SMBUS SMC 2 S4 SCL		48
SMBUS SMC 2 S4 SDA	==	SMBUS SMC 2 S4 SDA		48
SMC OOB1 D2R L	==	SMC OOB1 D2R L		88
SMC OOB1 R2D L	==	SMC OOB1 R2D L		88
SMC ACTUATOR DISABLE L	==	SMC ACTUATOR DISABLE L		43 104
SMC CHGR INT L	==	SMC CHGR INT L		66

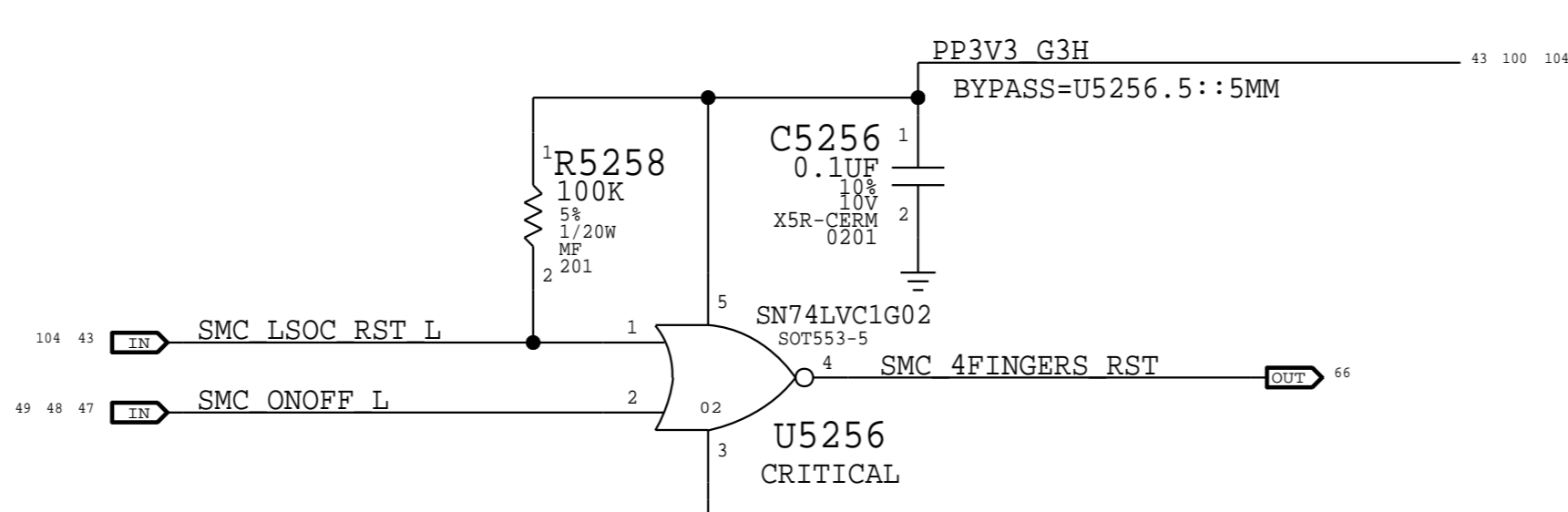
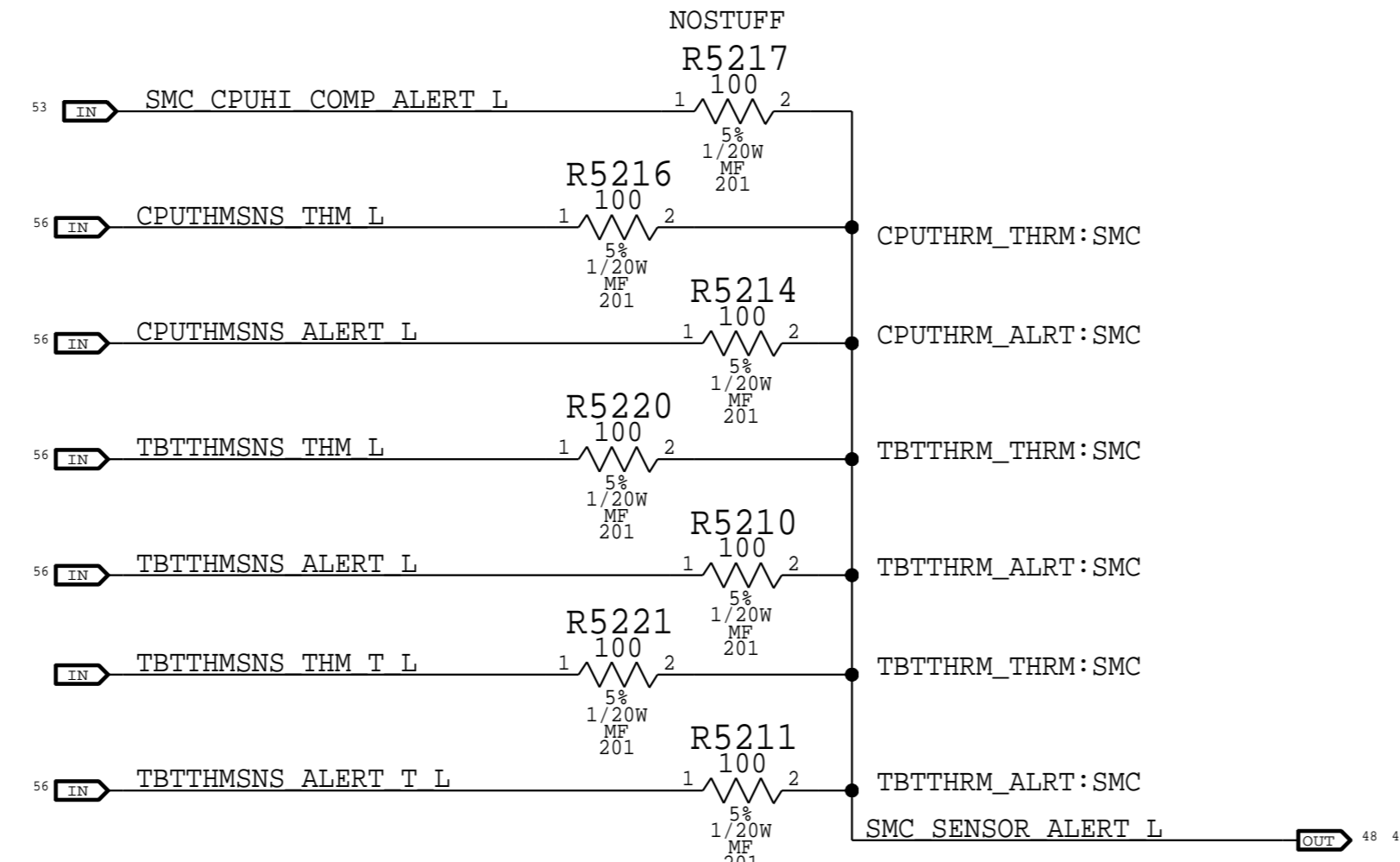
Debug Power "Buttons"



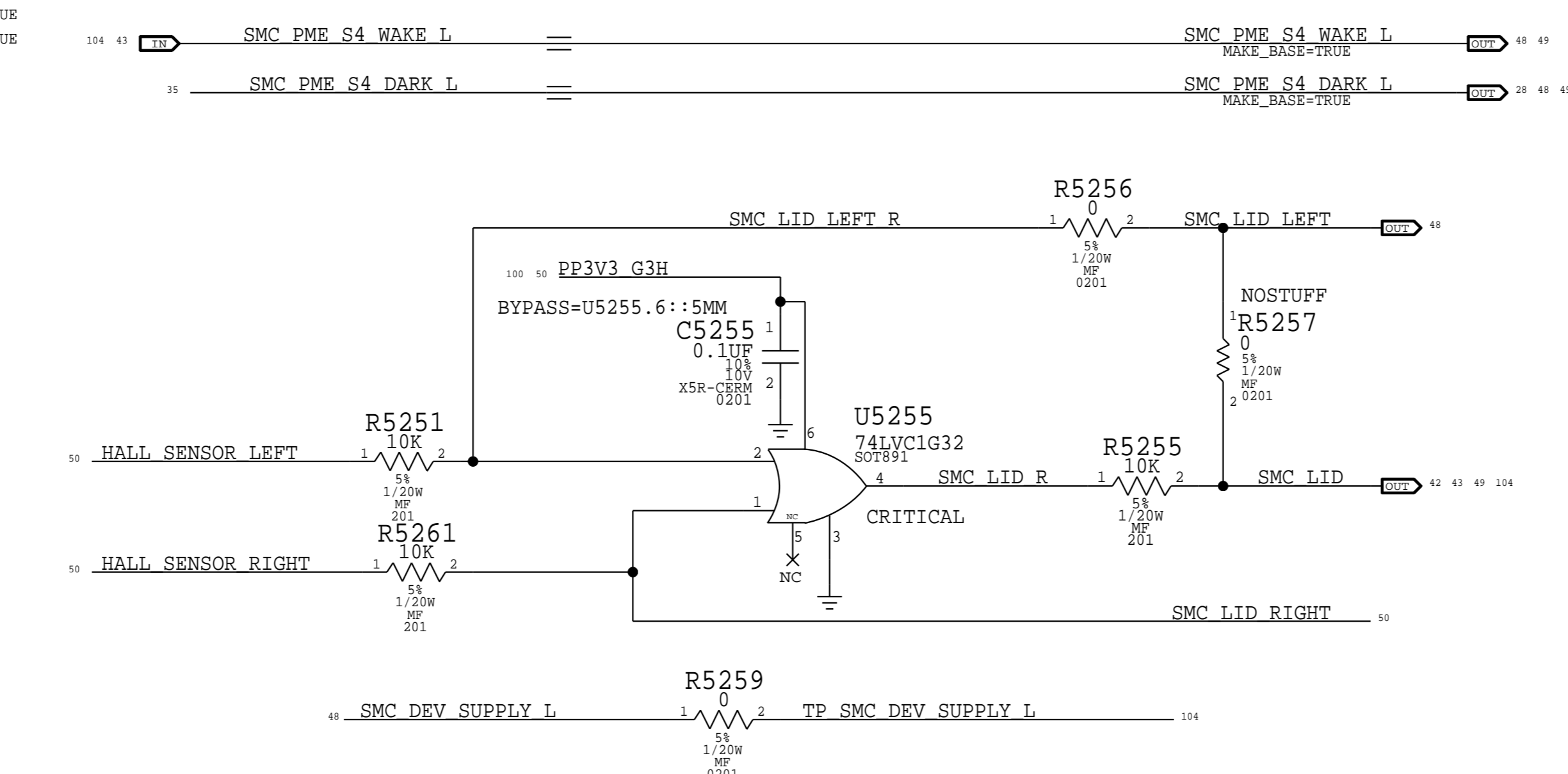
Debug RESET "Buttons"



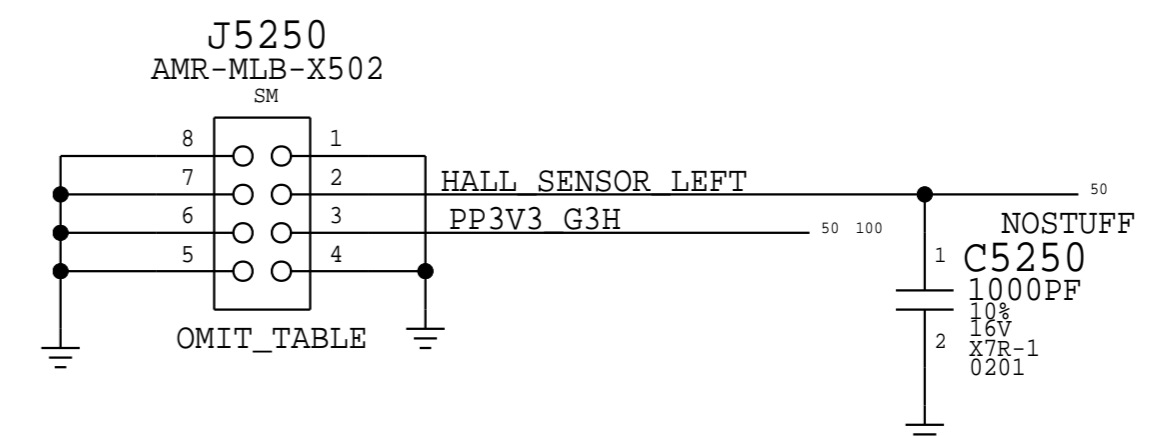
Thermal Alerts



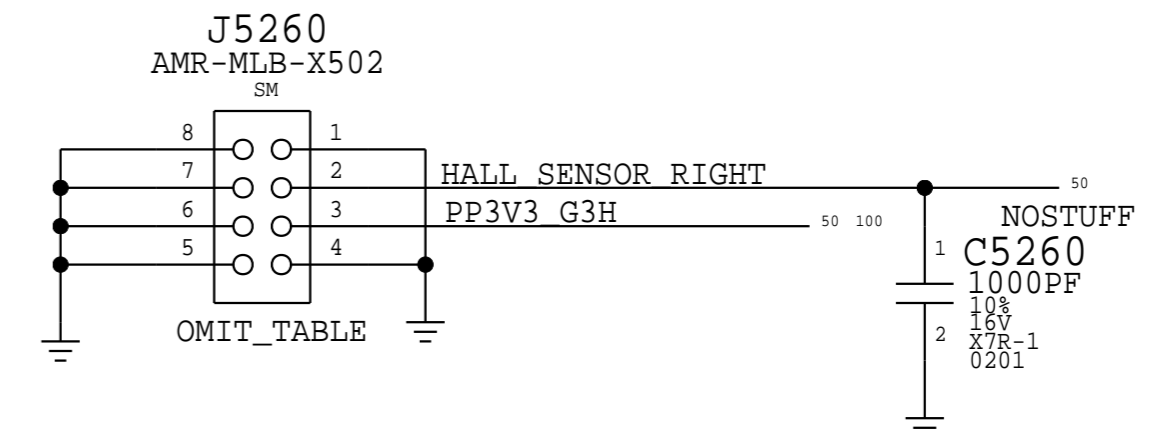
S4 SMC Wake Sources



Hall Effect Pads - Left



Hall Effect Pads - Right



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-04255	2	SUBASSY (T&R) PCBA,HES INTERPOSER,X502	J5250, J5260	CRITICAL	

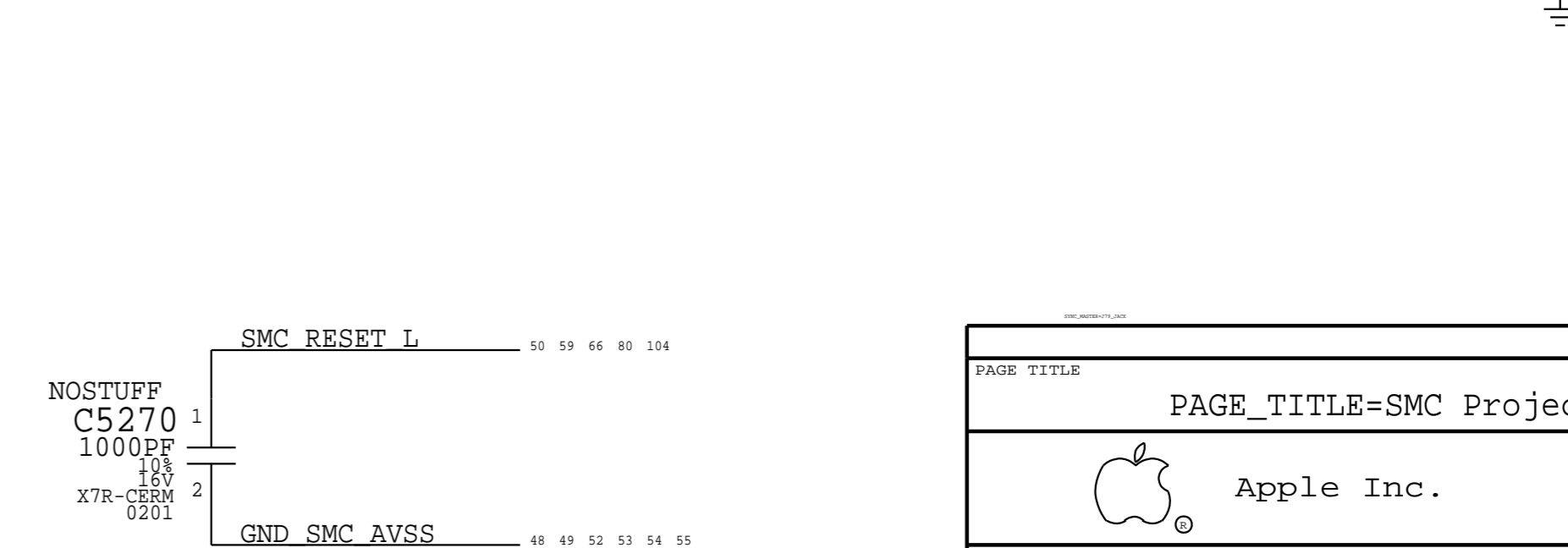
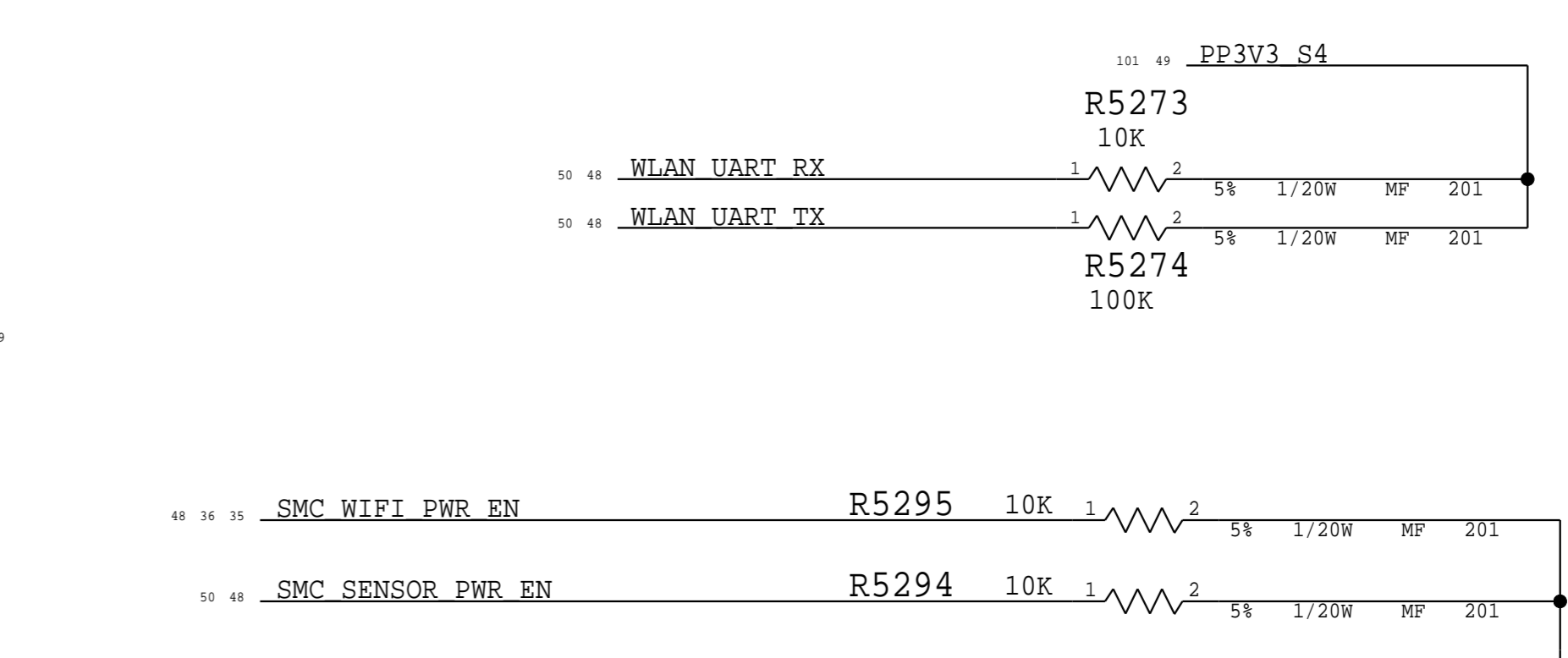
Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM: BOTH	CPUTHRM_THRM: SMC, CPUTHRM_ALRT: SMC
CPUTHRM: THRM	CPUTHRM_THRM: SMC, CPUTHRM_ALRT: PU
CPUTHRM: ALRT	CPUTHRM_ALRT: SMC
CPUTHRM: NONE	CPUTHRM_ALRT: PU

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
TBTTHRM: BOTH	TBTTHRM_THRM: SMC, TBTTHRM_ALRT: SMC
TBTTHRM: THRM	TBTTHRM_THRM: SMC, TBTTHRM_ALRT: PU
TBTTHRM: ALRT	TBTTHRM_THRM: PU, TBTTHRM_ALRT: SMC
TBTTHRM: NONE	TBTTHRM_THRM: PU, TBTTHRM_ALRT: PU

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

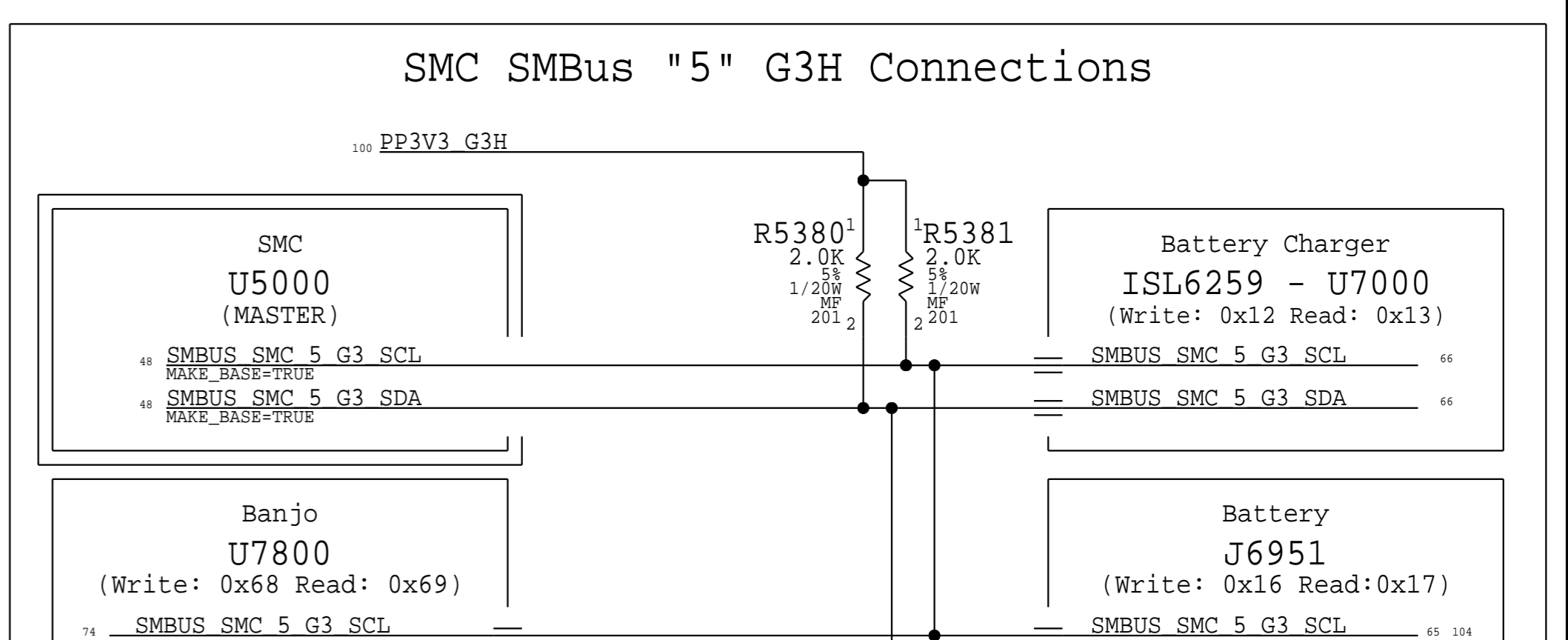
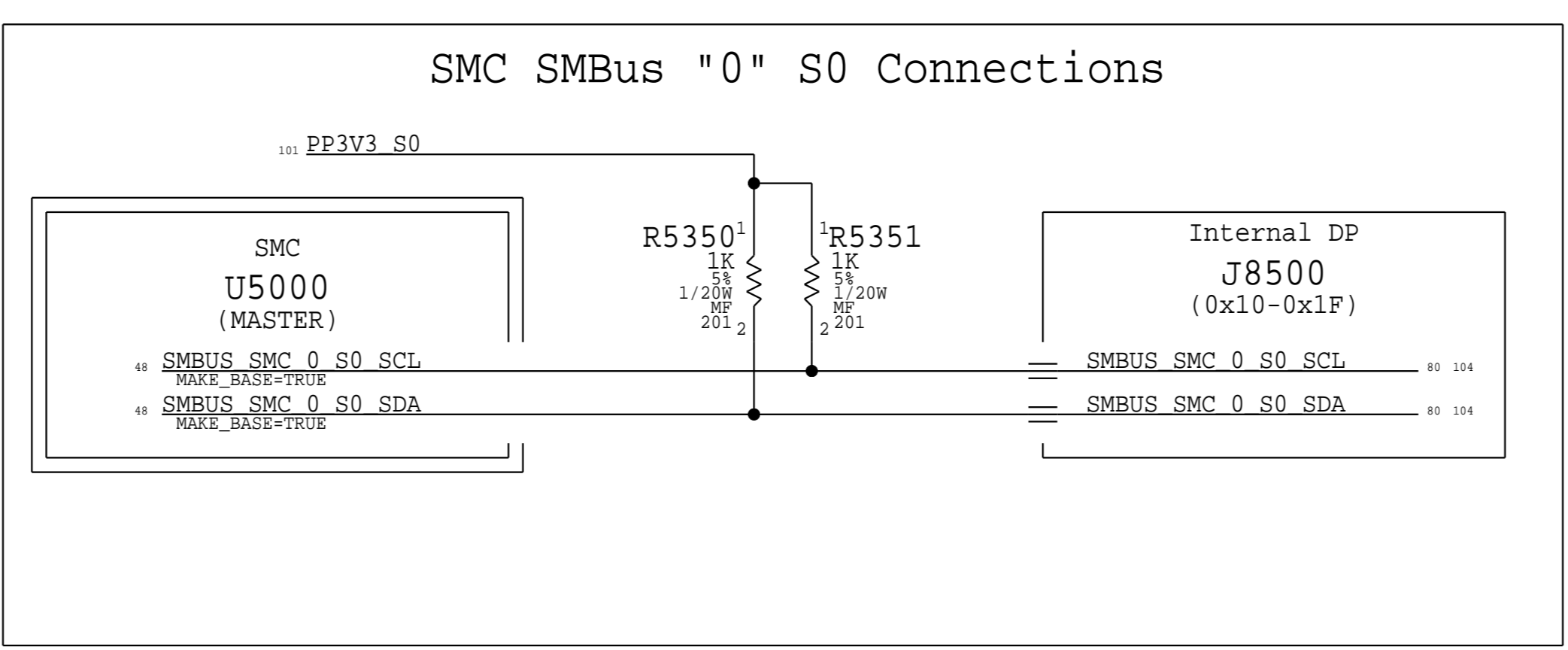
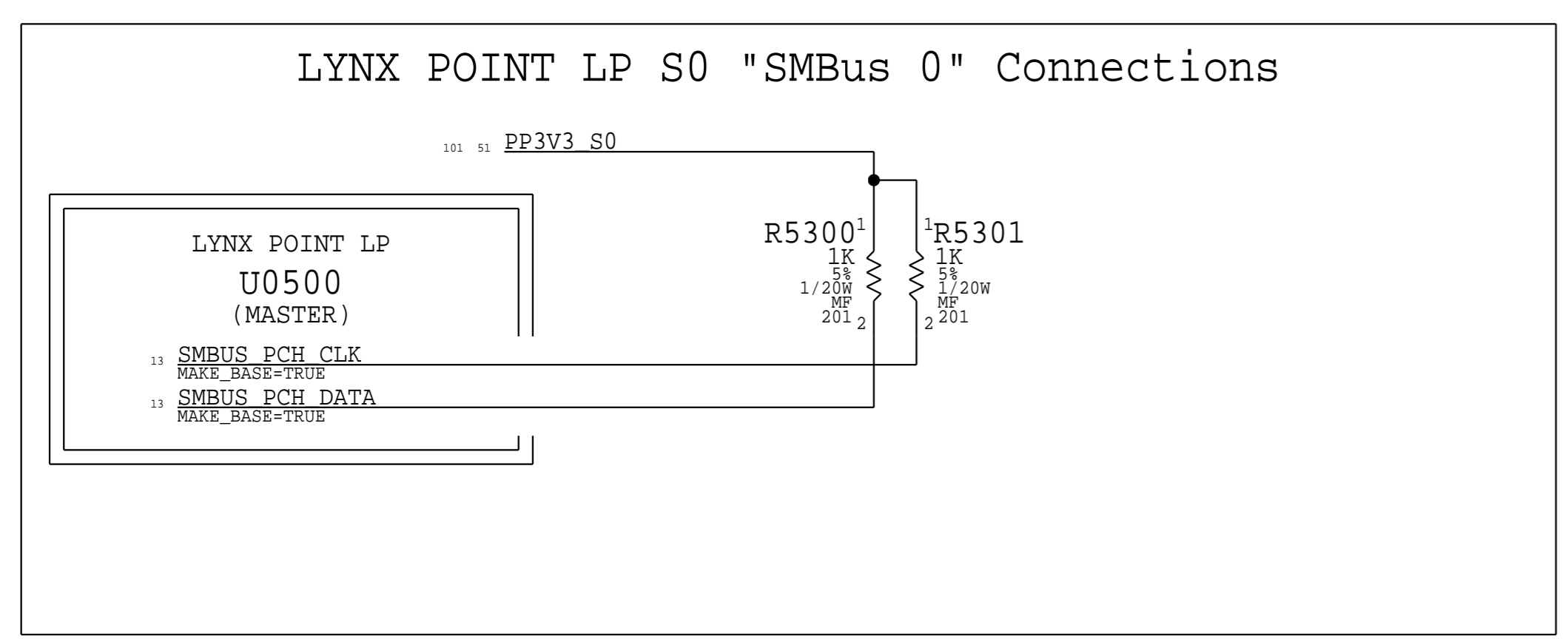


PAGE TITLE		PAGE_TITLE=SMC Project Support	
Apple Inc.		BRANCH NUMBER	051-00515
		REVISION	9.0.0
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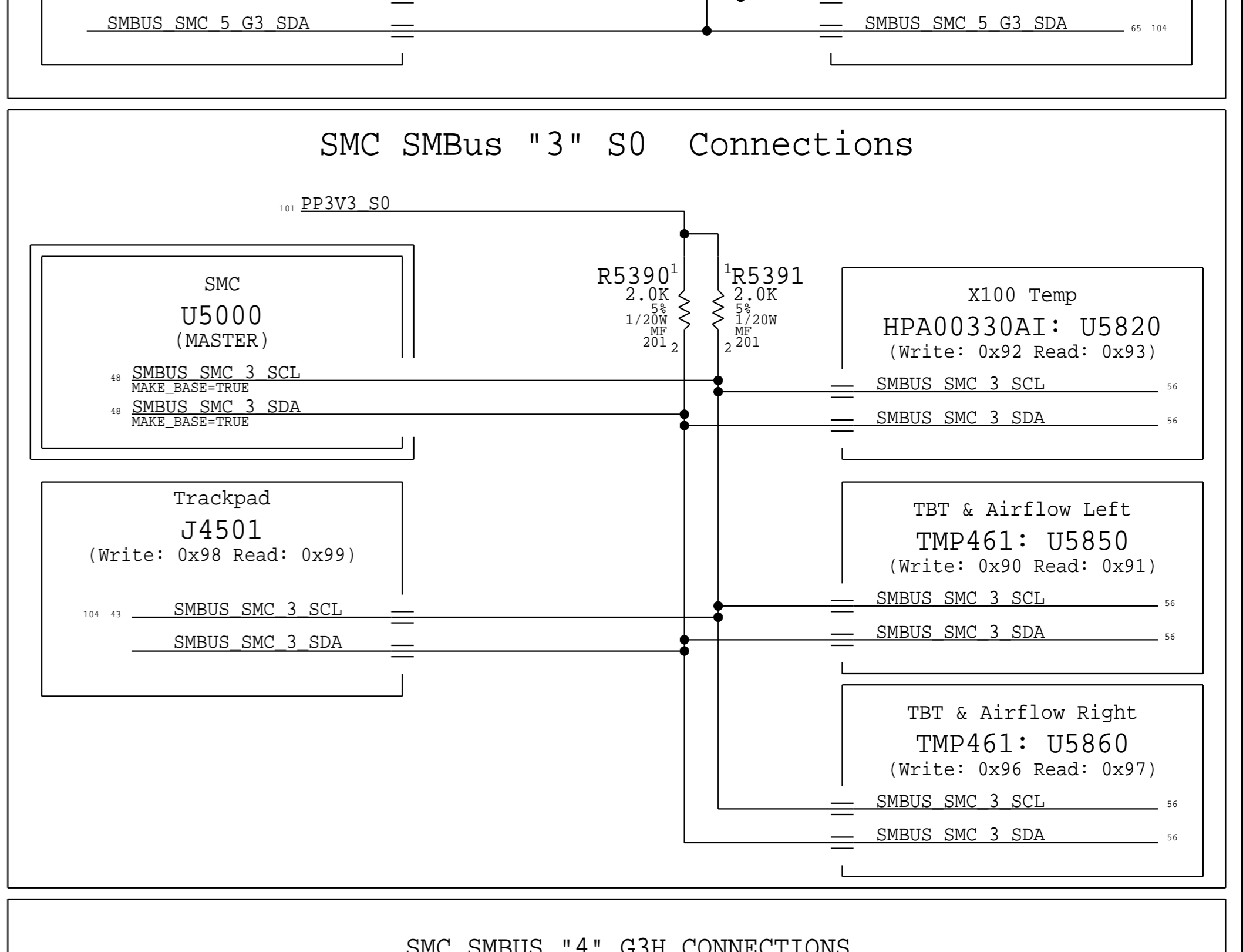
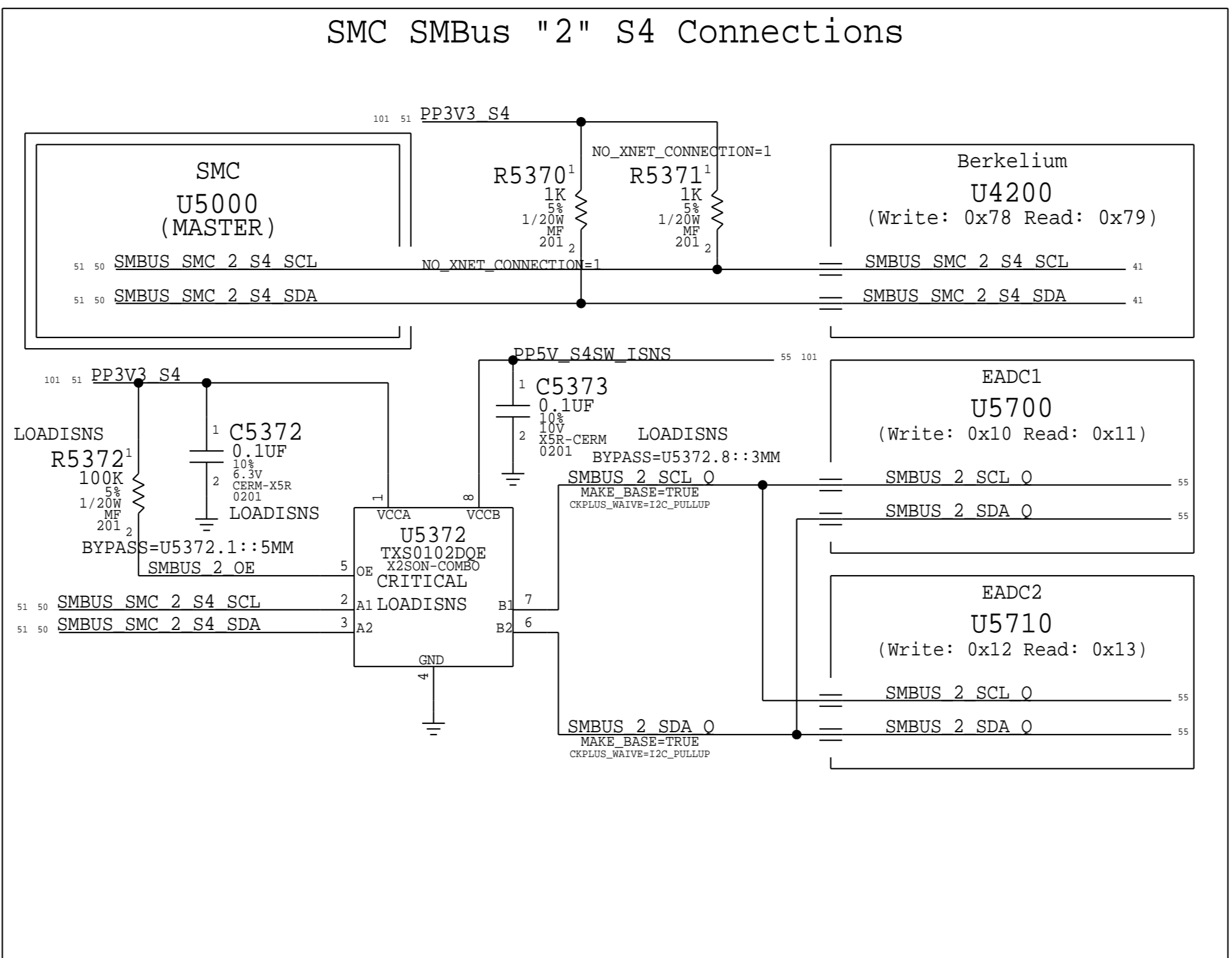
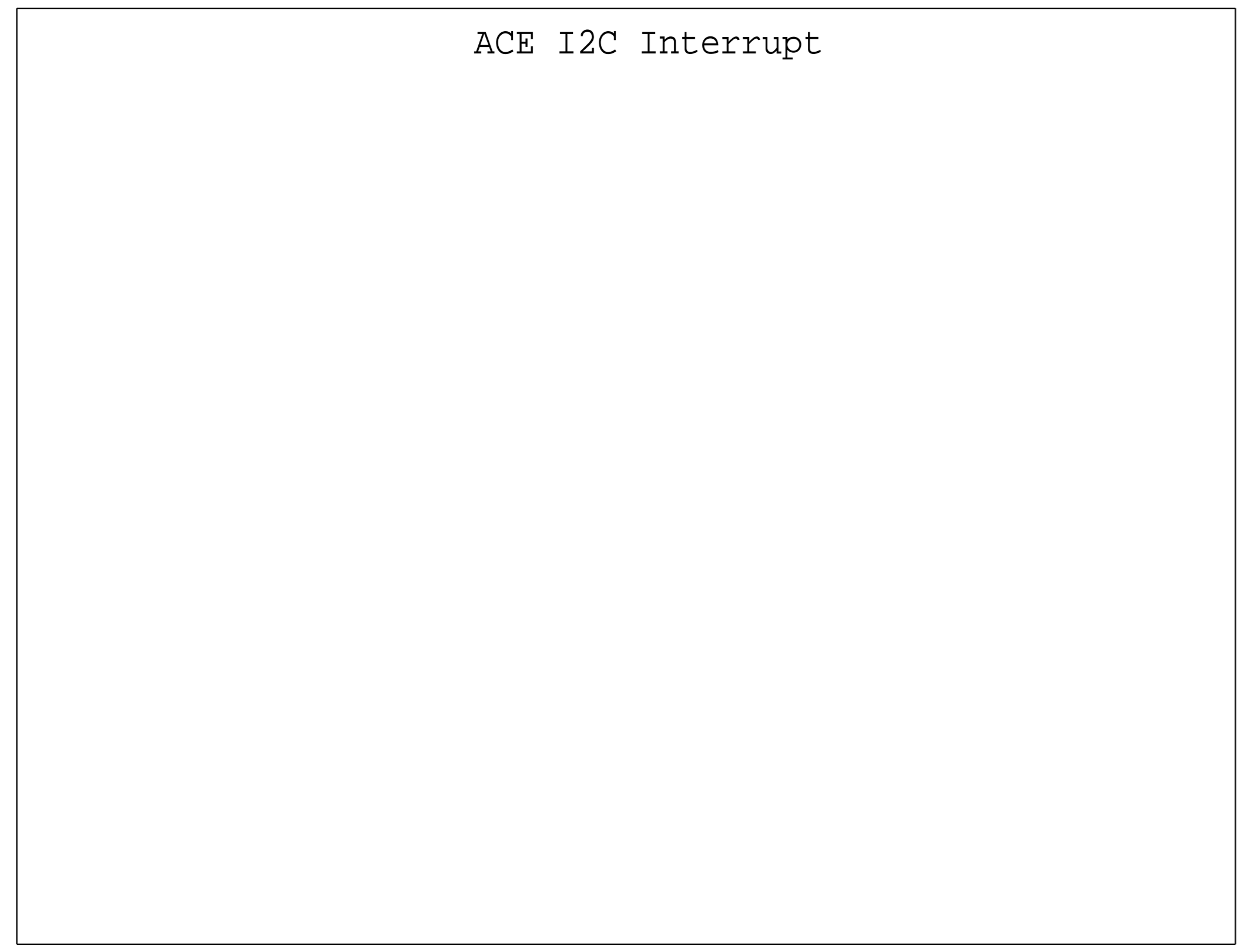
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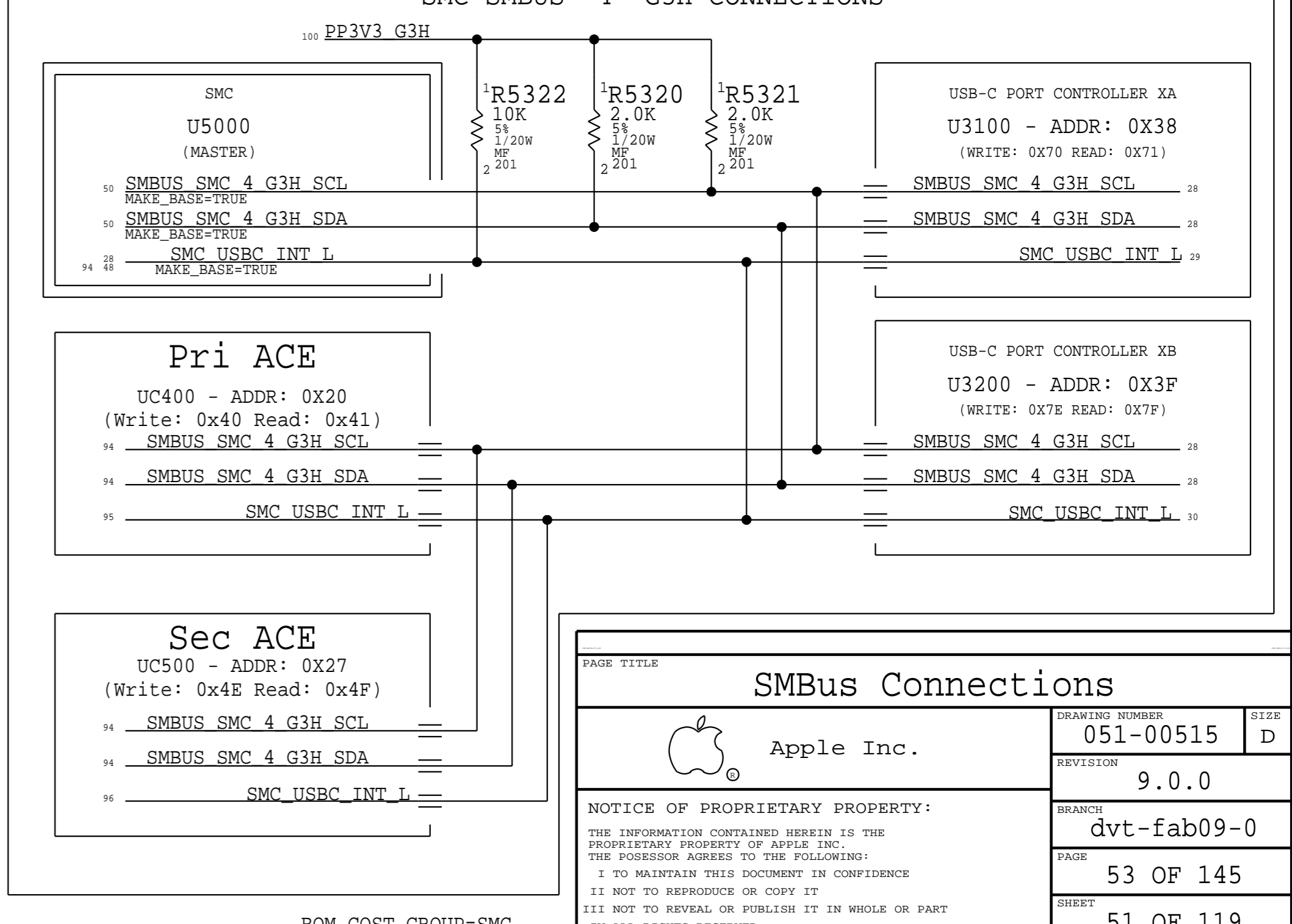
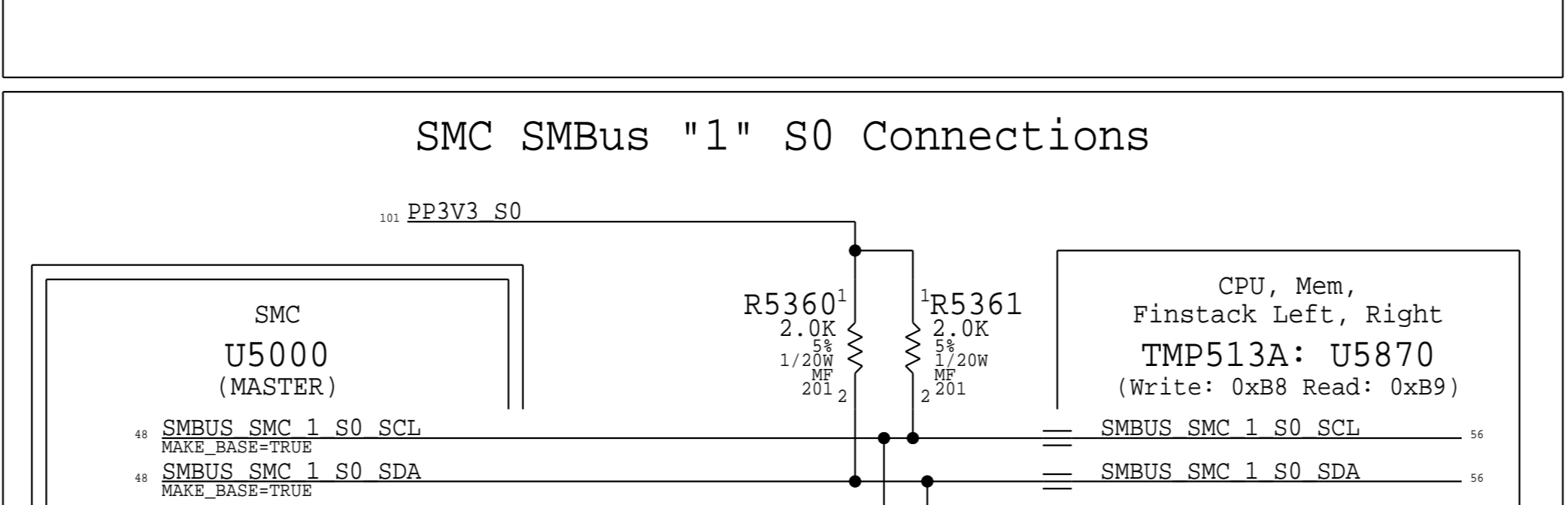
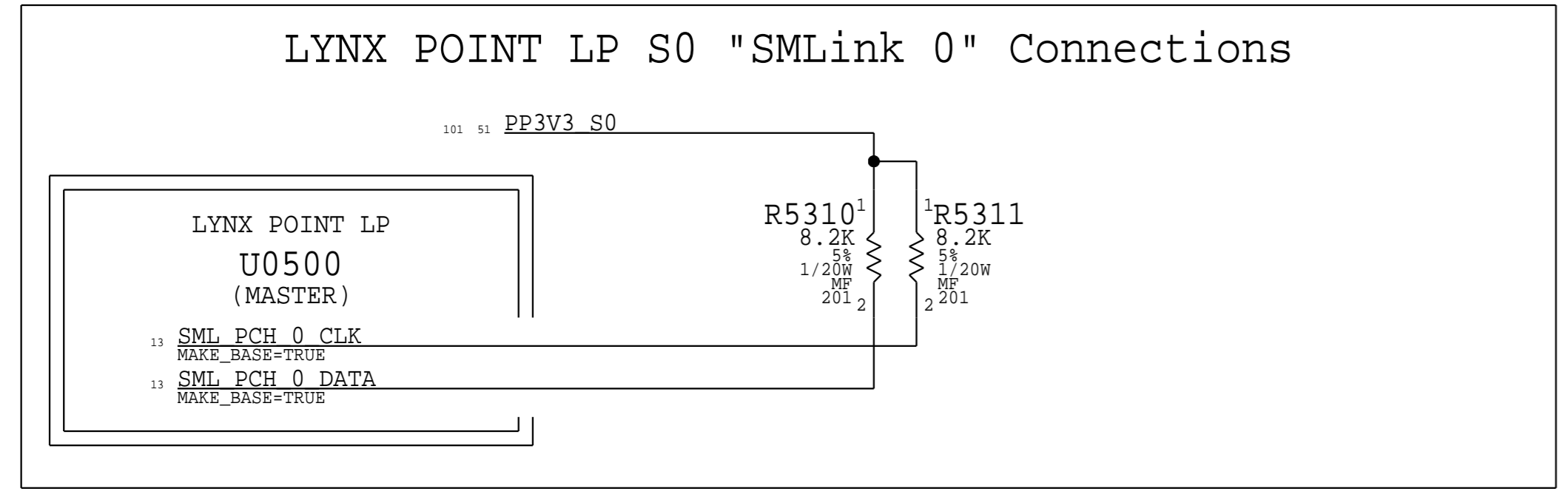
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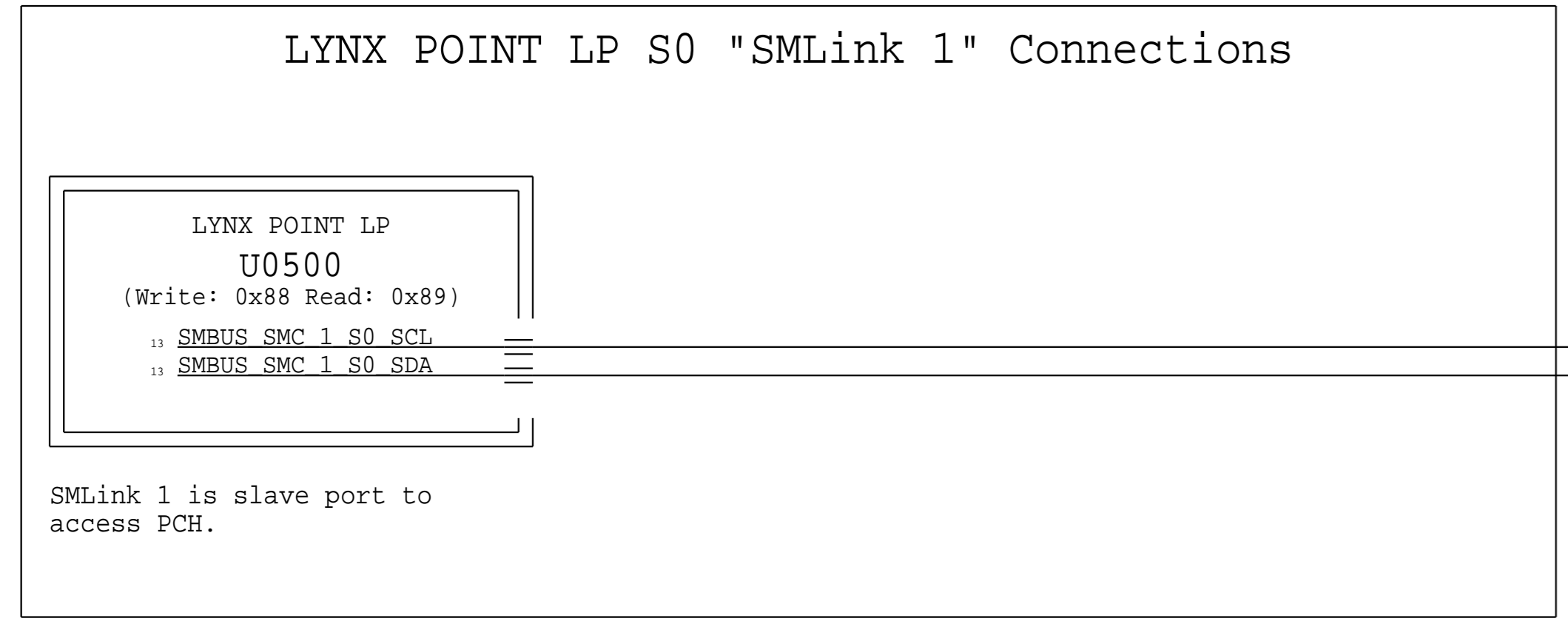
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A

A

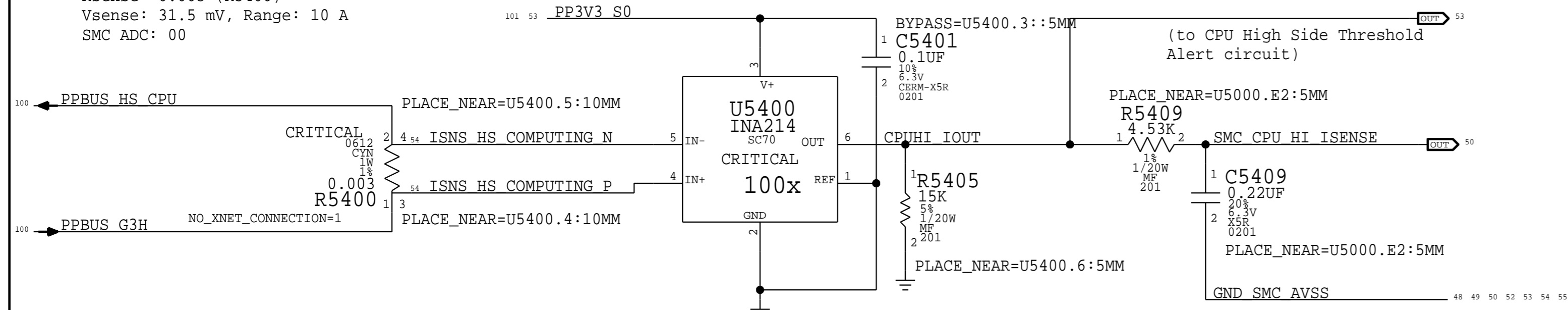


PAGE TITLE		DRAWING NUMBER		STEP
SMBus Connections		051-00515		D
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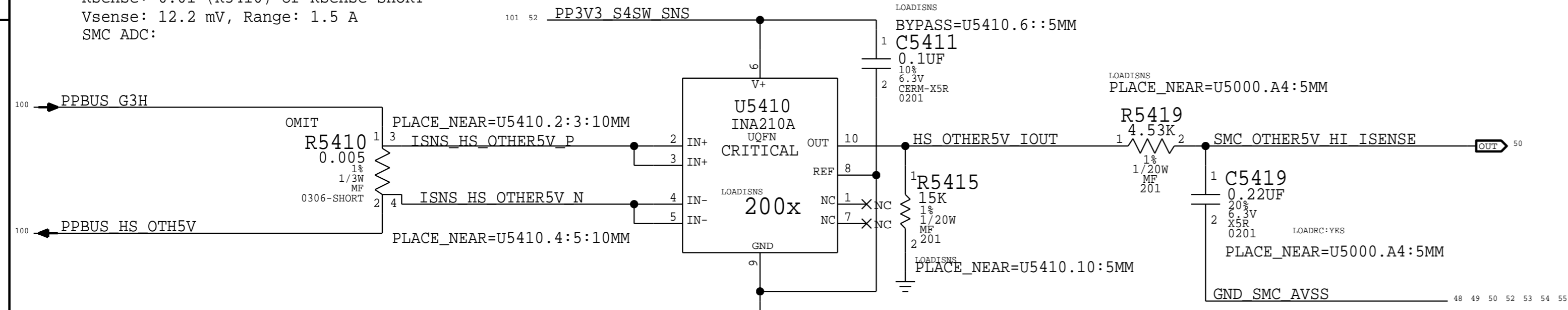
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
 Rsense: 0.003 (R5400)
 Vsense: 31.5 mV, Range: 10 A
 SMC ADC: 00



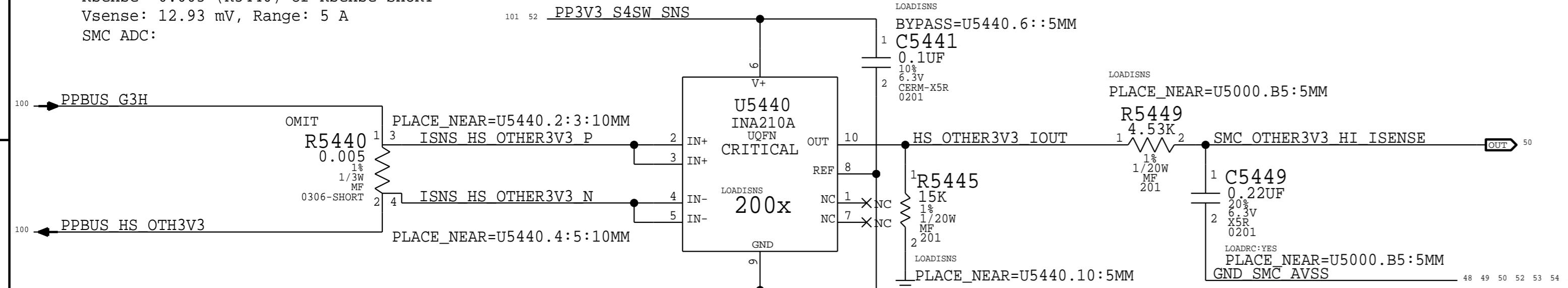
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
 Rsense: 0.01 (R5410) or Rsense SHORT
 Vsense: 12.2 mV, Range: 1.5 A
 SMC ADC:



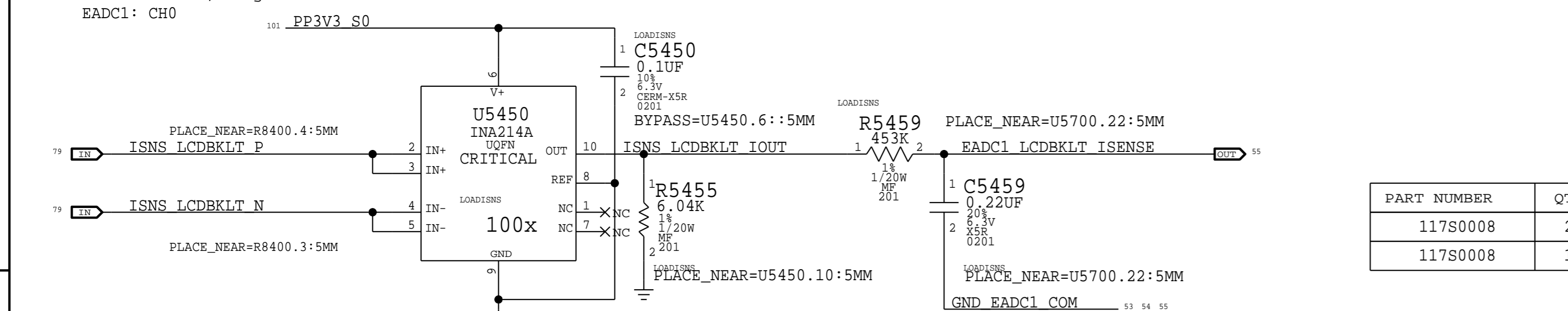
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
 Rsense: 0.003 (R5440) or Rsense SHORT
 Vsense: 12.93 mV, Range: 5 A
 SMC ADC:



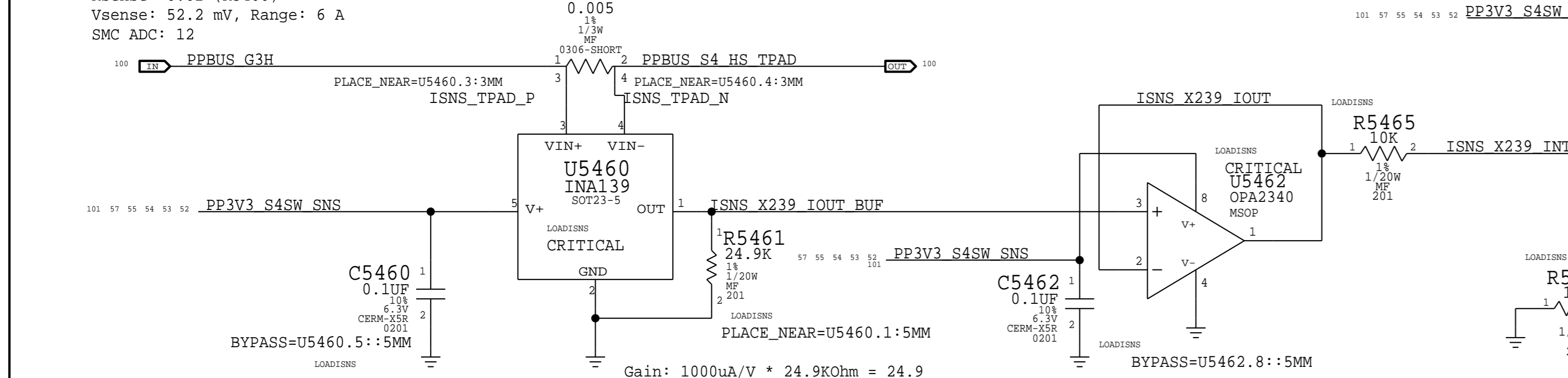
LCD Backlight Current Sense (IBLR)

Gain: 100x, EDP: 1 A
 Rsense: 0.025 (R8400)
 Vsense: 25 mV, Range: 2.4 A
 EADC1: CH0



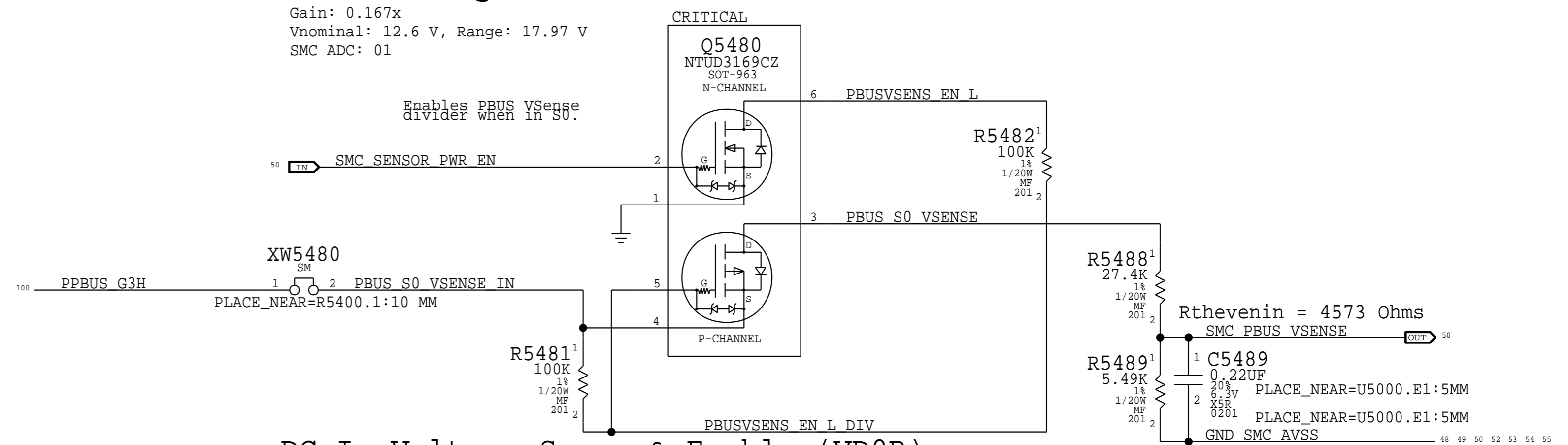
Trackpad Actuator X239 Current Sense (ITAR)

Gain: 24.9x, EDP: 2.61 A (Transient)
 Rsense: 0.02 (R5460)
 Vsense: 52.2 mV, Range: 6 A
 SMC ADC: 12



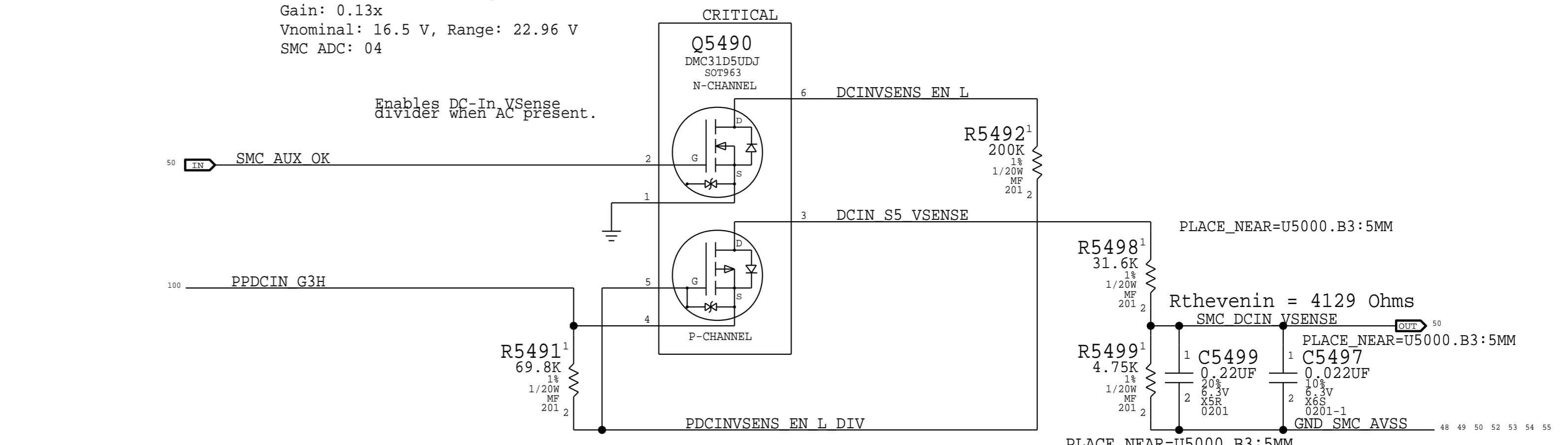
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
 Vnominal: 12.6 V, Range: 17.97 V
 SMC ADC: 01



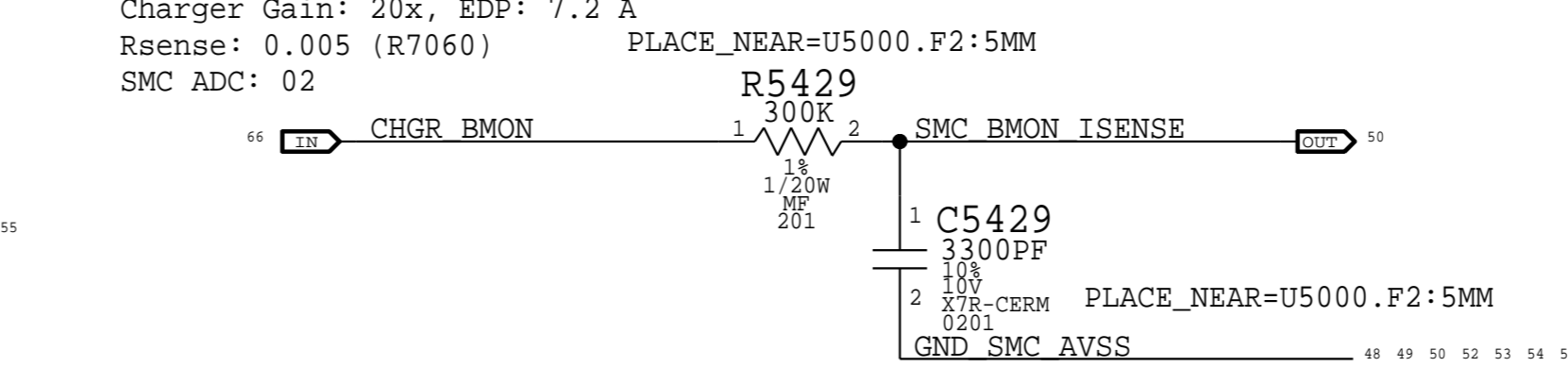
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13x
 Vnominal: 16.5 V, Range: 22.96 V
 SMC ADC: 04



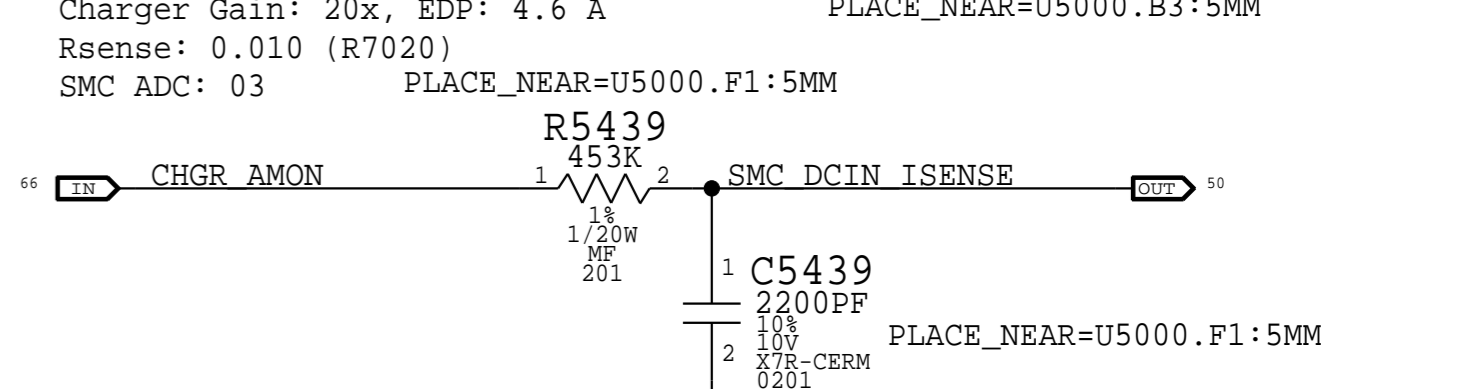
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
 Rsense: 0.005 (R7060)
 SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
 Rsense: 0.010 (R7020)
 SMC ADC: 03



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES_MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		LOADRC:NO
117S0008	1	RES_MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		LOADRC:NO

Power Sensors: High Side

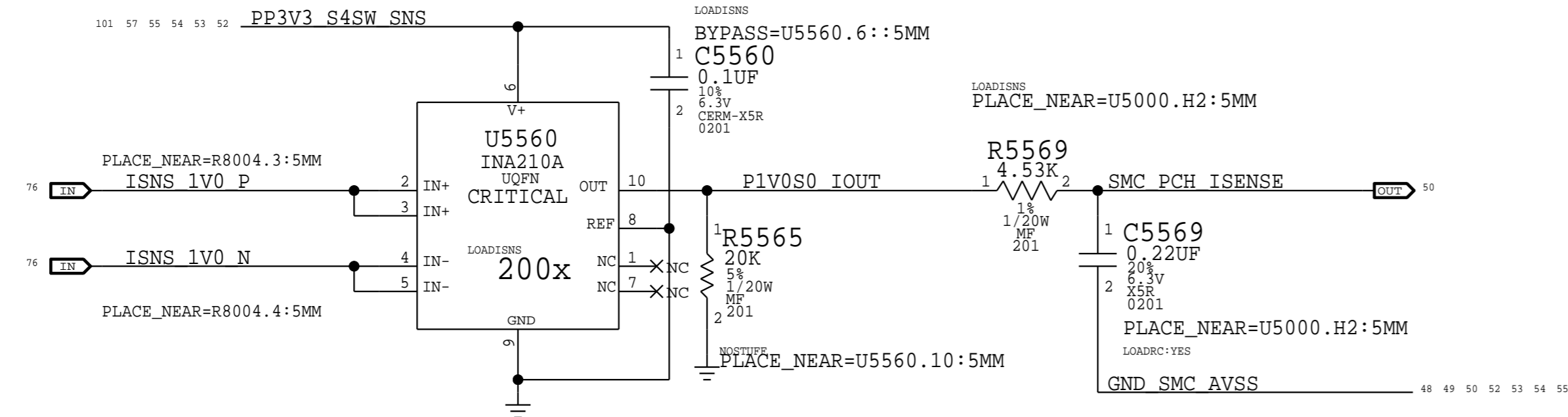
Apple Inc.

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 REVISION: 9.0.0
 BRANCH: dvt-fab09-0
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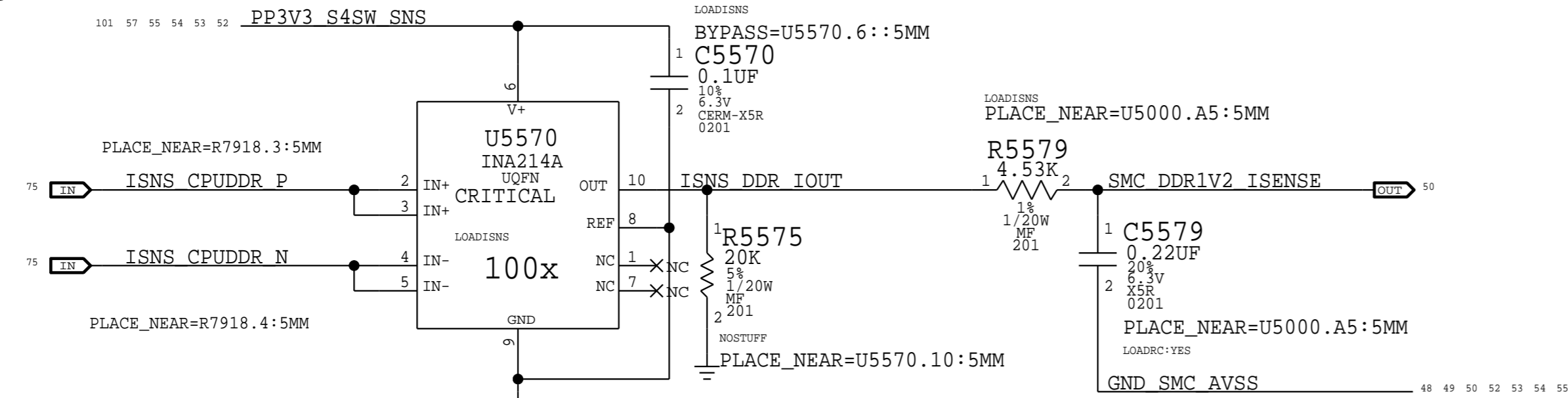
PCH 1.0V Current Sense (IS1C)

Gain: 200x, EDP: 3.29 A
 Rsense: 0.003 (R8004) or Rsense SHORT
 Vsense: 9.87 mV, Range: 5 A
 SMC ADC: 11



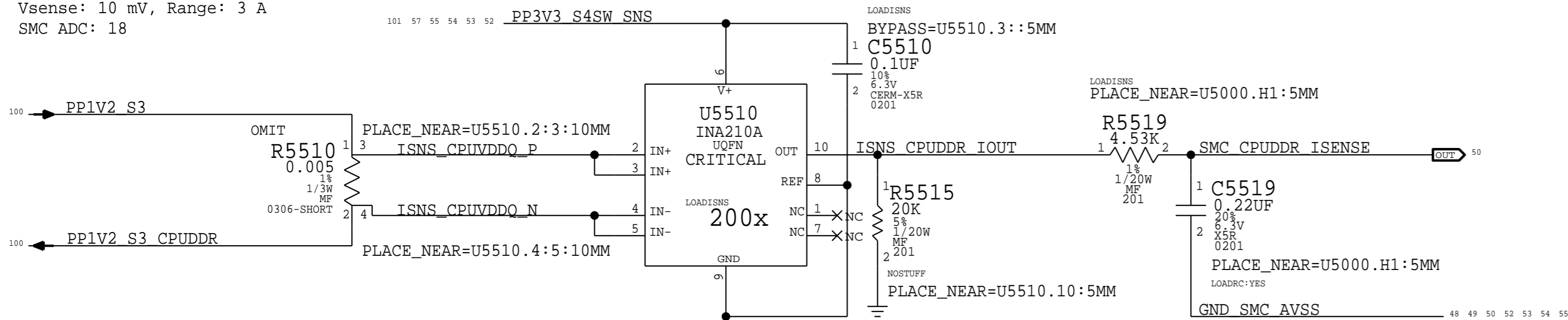
DDR 1.2V S3 (CPU & Memory) Current Sense (IMOC)

Gain: 100x, EDP: 8.21 A
 Rsense: 0.003 (R7918) or XWTBD
 Vsense: 24.63 mV, Range: 10 A
 SMC ADC: 09



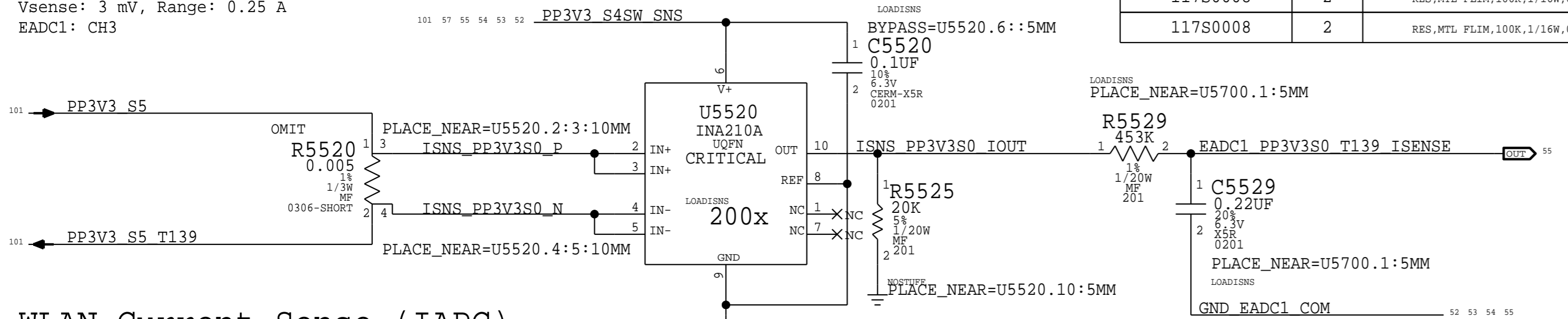
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
 Rsense: 0.005 (R5510) or Rsense SHORT
 Vsense: 10 mV, Range: 3 A
 SMC ADC: 18



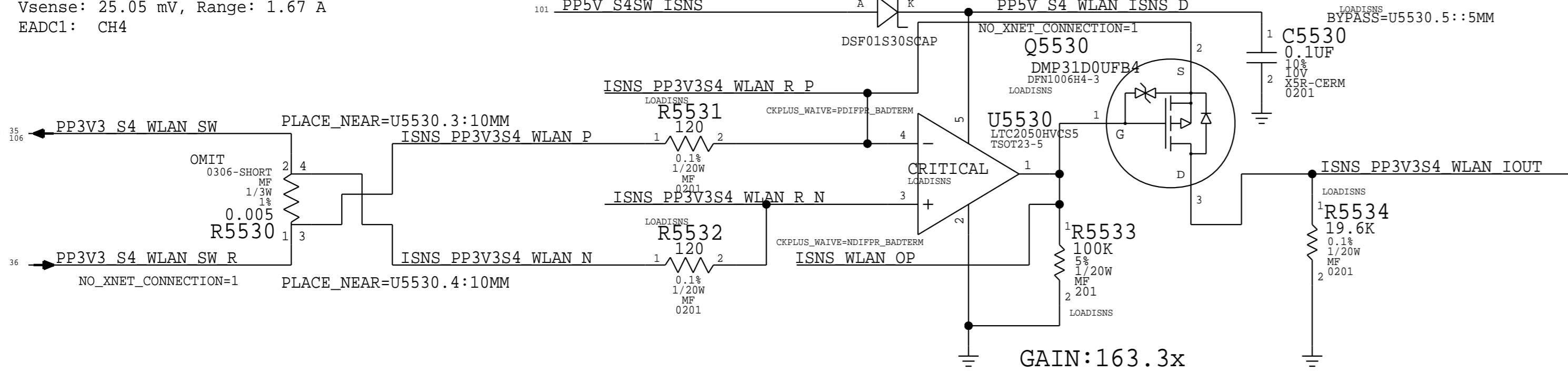
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
 Rsense: 0.05 (R5520) or Rsense SHORT
 Vsense: 3 mV, Range: 0.25 A
 EADC1: CH3



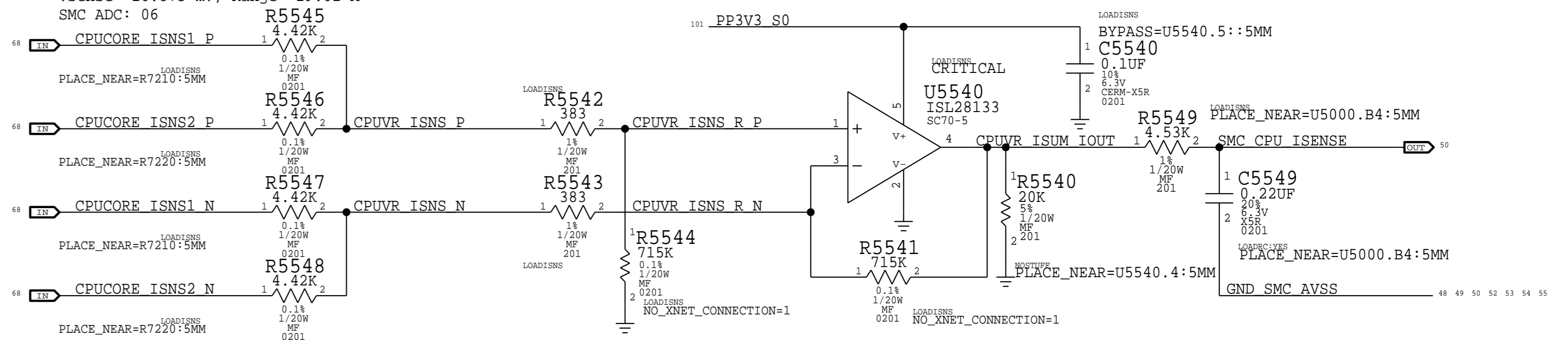
WLAN Current Sense (IAPC)

Gain: 163.3x, EDP: 1.67 A
 Rsense: 0.015 (R5530) or Rsense SHORT
 Vsense: 25.05 mV, Range: 1.67 A
 EADC1: CH4



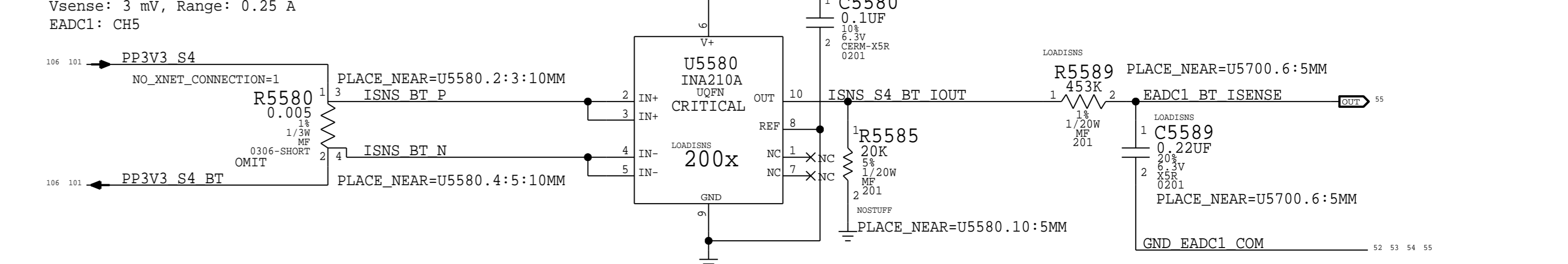
CPU Fixed Current Sense (ICAC)

Gain: 275.74x, EDP: 29 A
 Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
 SMC ADC: 06



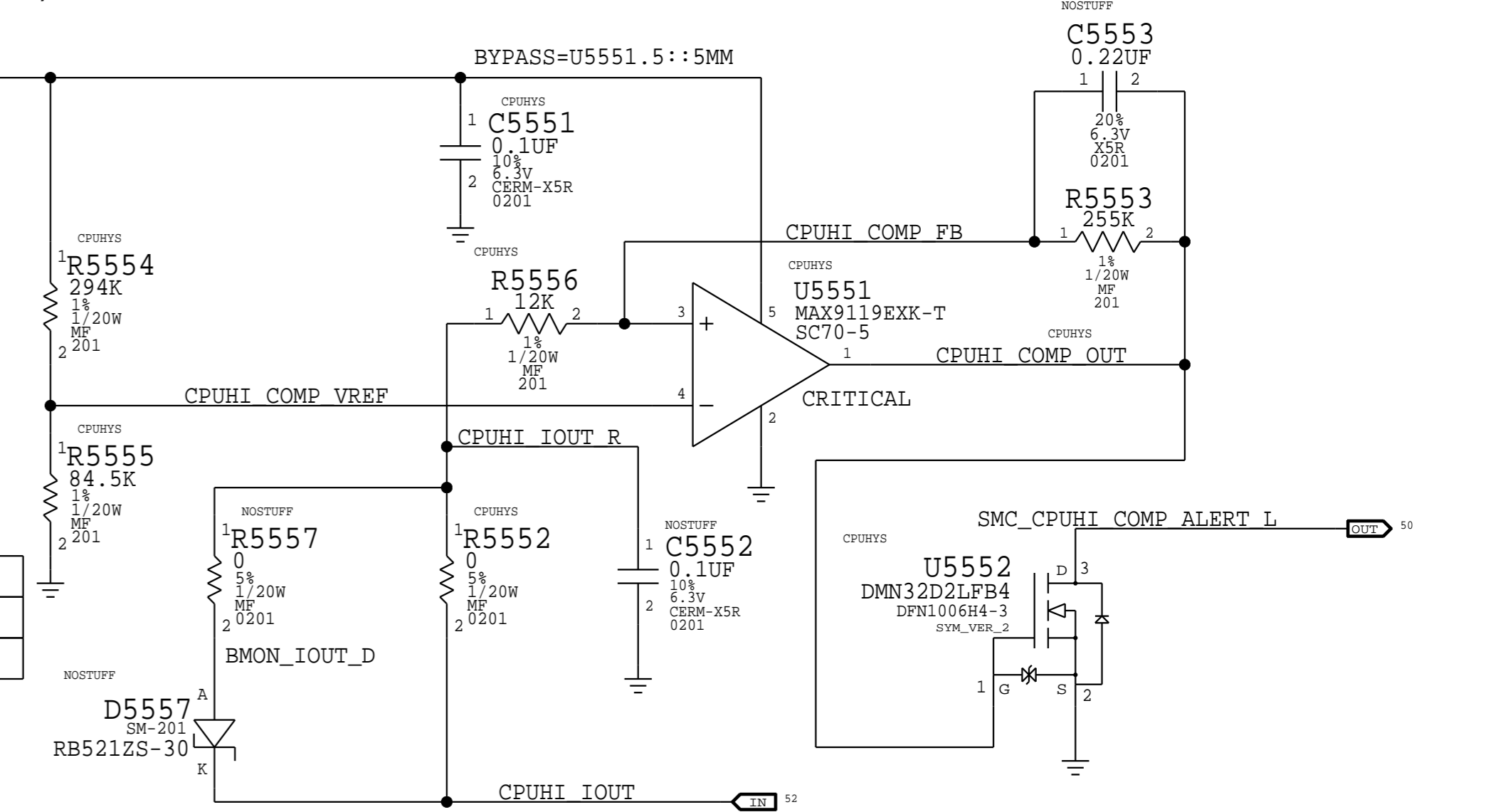
BT Current Sense (IBTC)

Gain: 200x, EDP: 0.06 A
 Rsense: 0.05 (R5580)
 Vsense: 3 mV, Range: 0.25 A
 EADC1: CH5



CPU High Side Current (IC0R) Threshold Alert

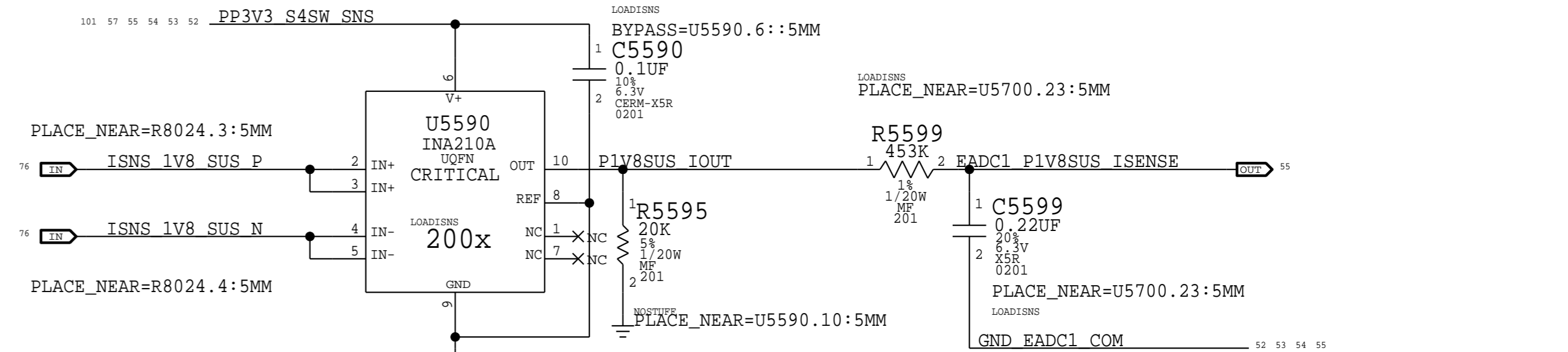
Gain: 100x
 Rsense: 0.003 (R5400)
 Trip Target on CPU High current: 2.5 A
 Hysteresis Circuit:
 Vref = 0.737 V
 Vth = 0.616 V -> 2.054 A on CPU High current
 Vtl = 0.771 V -> 2.571 A on CPU High current
 Hysteresis Margin = 0.518 A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5549,C5579		LOADRC:NO

1.8V Current Sense (I18C)

Gain: 200x, EDP: 0.7 A
 Rsense: 0.025 (R8024) or Rsense SHORT
 Vsense: 17.5 mV, Range: 0.6 A
 SMC ADC: 16



PAGE TITLE: Power Sensors: Load Side

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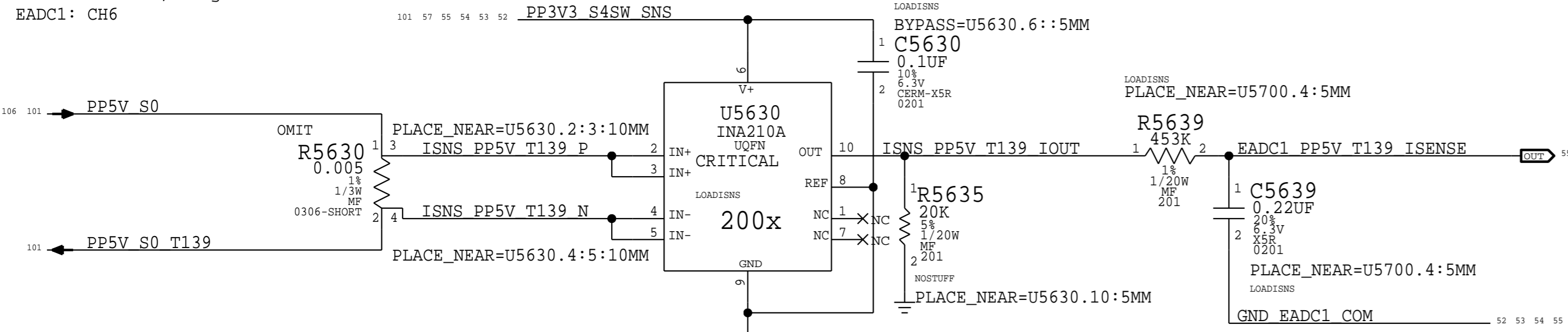
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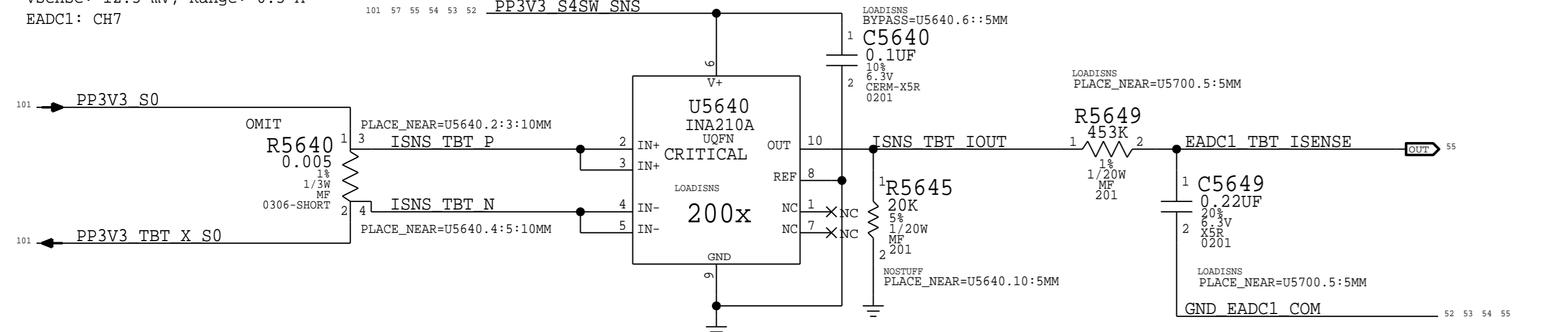
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
 Rsense: 0.05 (R5630) or Rsense SHORT
 Vsense: 0.2 mV, Range: 0.25 A
 EADC1: CH6



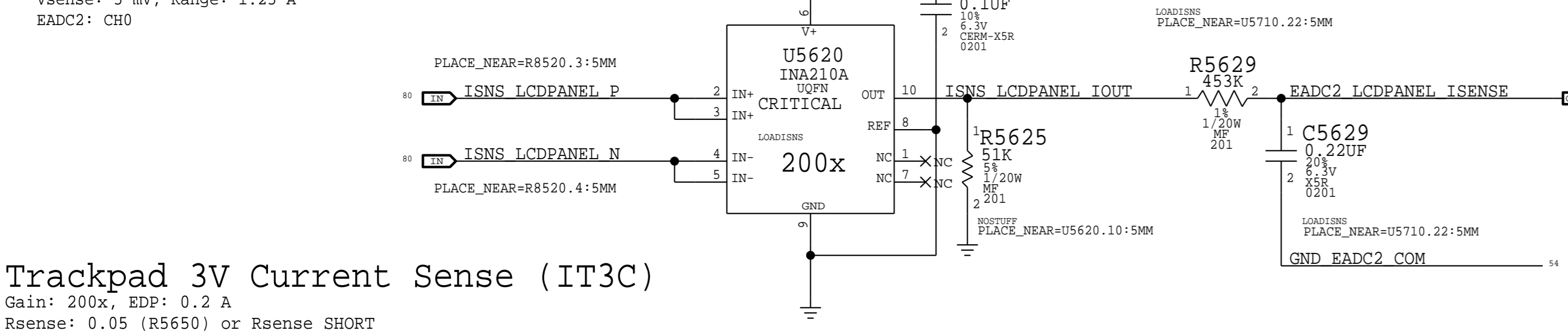
Thunderbolt TBT Current Left (IULC)

Gain: 200x, EDP: 0.5 A
 Rsense: 0.025 (R5640) or Rsense SHORT
 Vsense: 12.5 mV, Range: 0.5 A
 EADC1: CH7



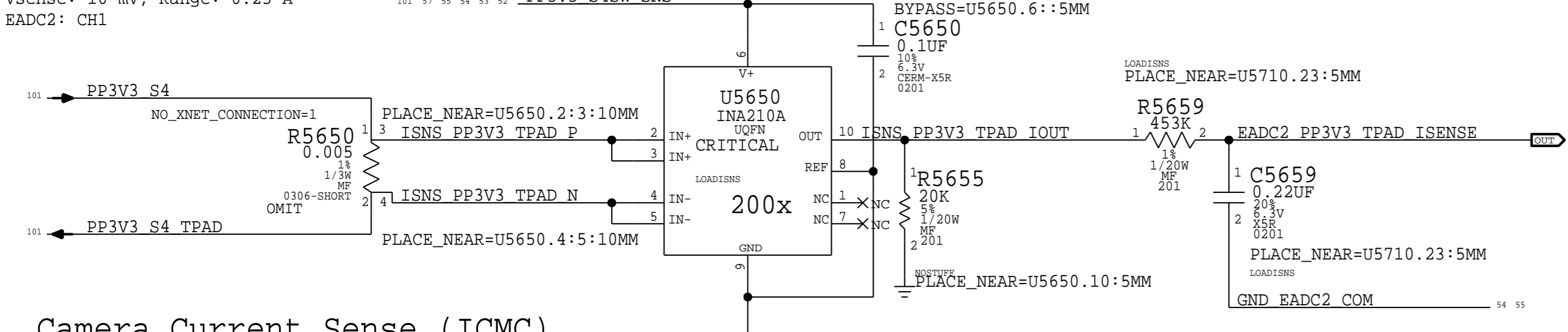
LCD Panel Current Sense (ILDC)

Gain: 200x, EDP: 1 A
 RSENSE: 0.01 (R5620) or Rsense SHORT
 Vsense: 5 mV, Range: 1.25 A
 EADC2: CH0



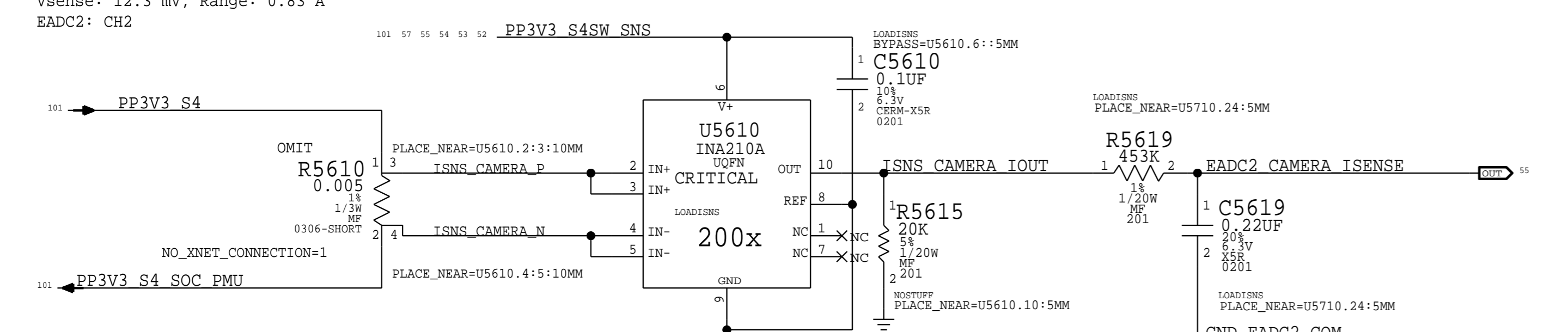
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
 Rsense: 0.05 (R5650) or Rsense SHORT
 Vsense: 10 mV, Range: 0.25 A
 EADC2: CH1

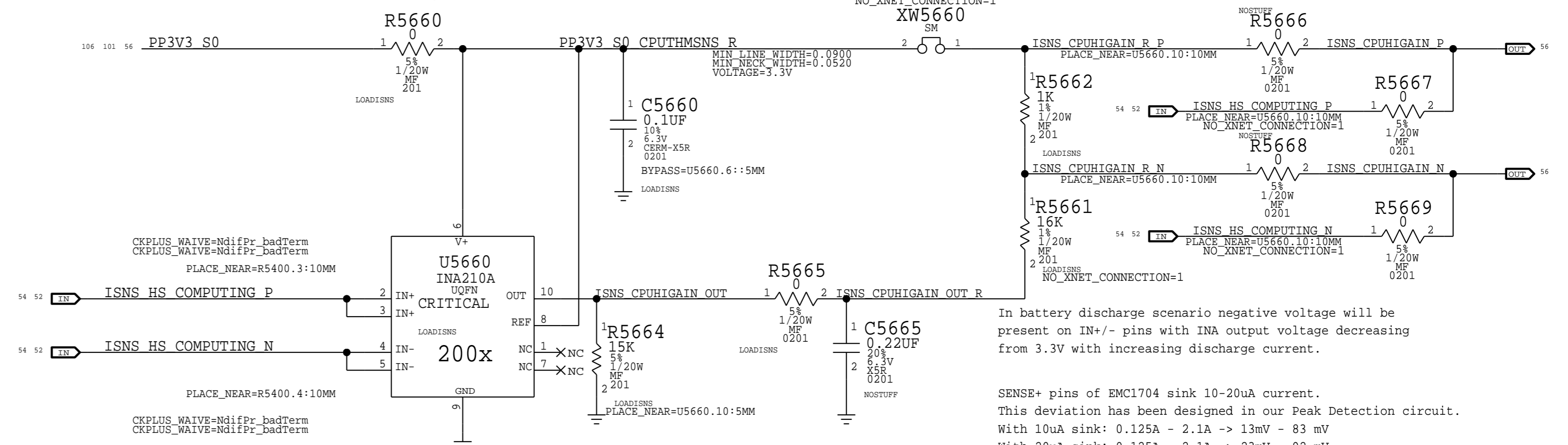


Camera Current Sense (ICMC)

Gain: 200x, EDP: 0.82 A
 Rsense: 0.015 (R5610) or XW5610
 Vsense: 12.3 mV, Range: 0.83 A
 EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

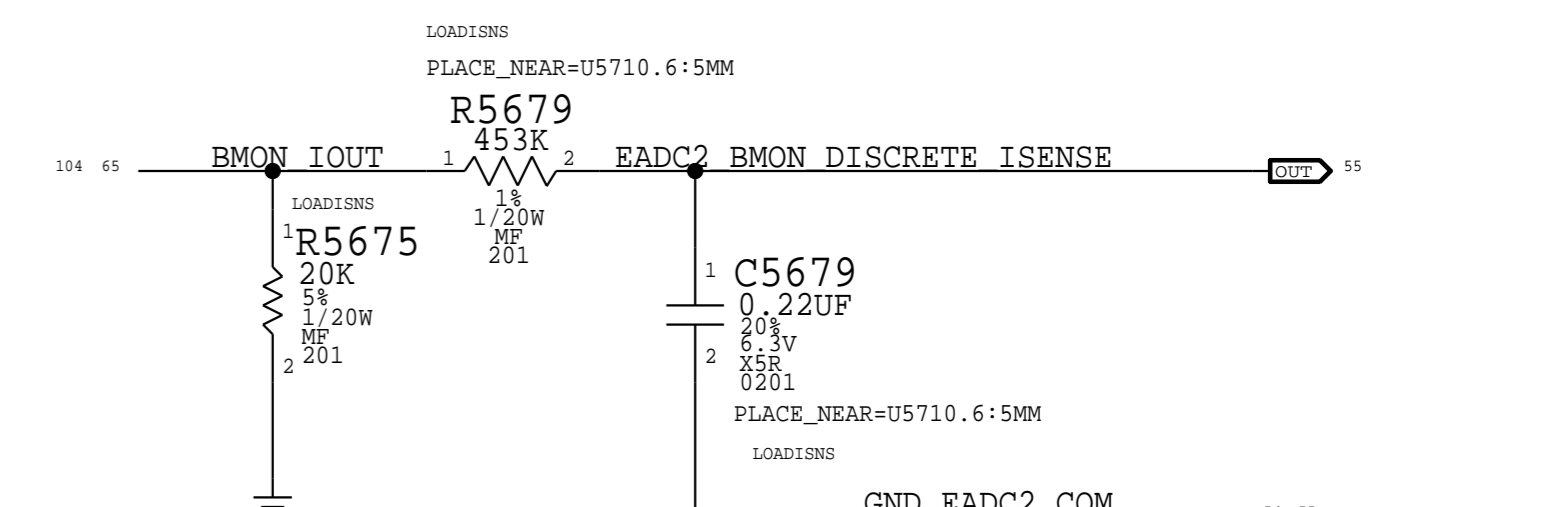


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMCL104 sink 10-20uA current. This deviation has been designed in our Peak Detection circuit. With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

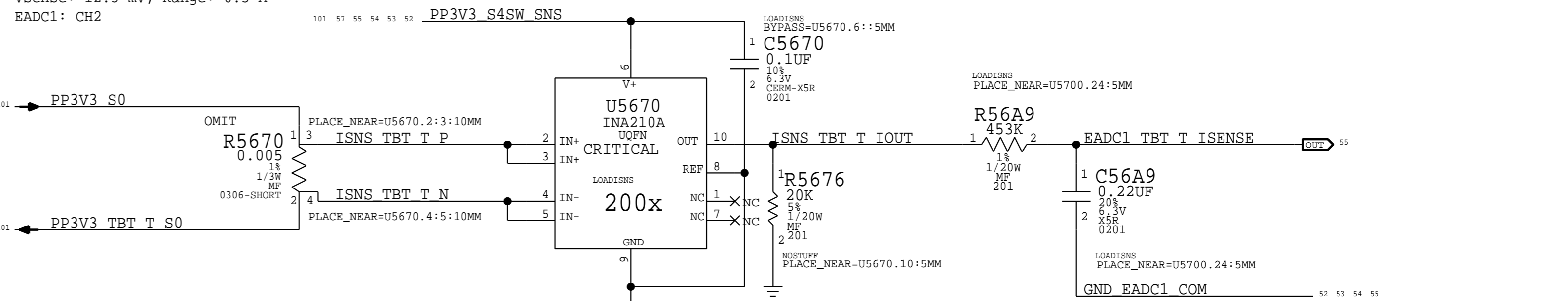
Battery Discrete Current Sense (IB0L)

Gain: 2940x, EDP: 8 A
 Rsense: 0.003 (R501/R502)
 Vsense: 24 mV, Range: 0.28 A
 EADC2: CH5



Thunderbolt TBT Current Right (IURC)

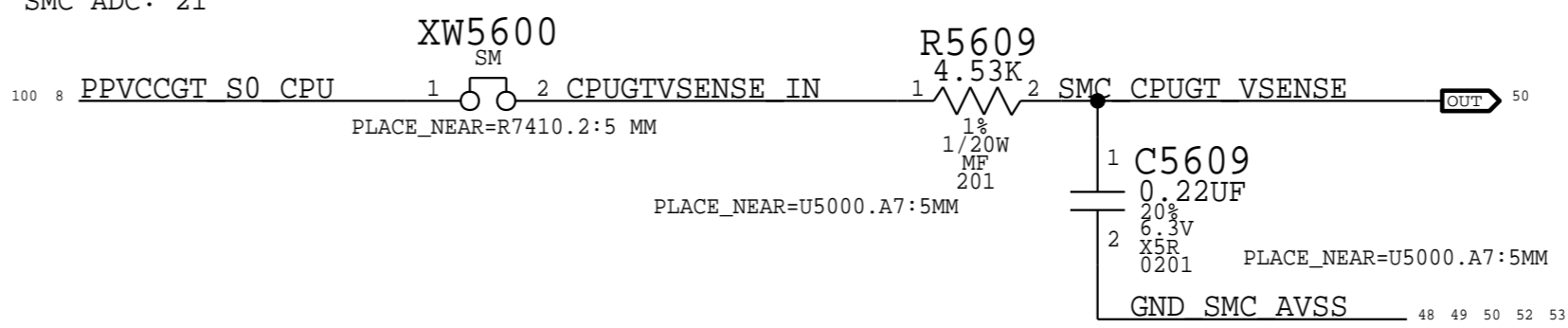
Gain: 200x, EDP: 0.5 A
 Rsense: 0.025 (R5670) or Rsense SHORT
 Vsense: 12.5 mV, Range: 0.5 A
 EADC1: CH2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL,FLM,100K,1/16W,0201,SMD,LF	C5608, C5699		LOADRC:NO

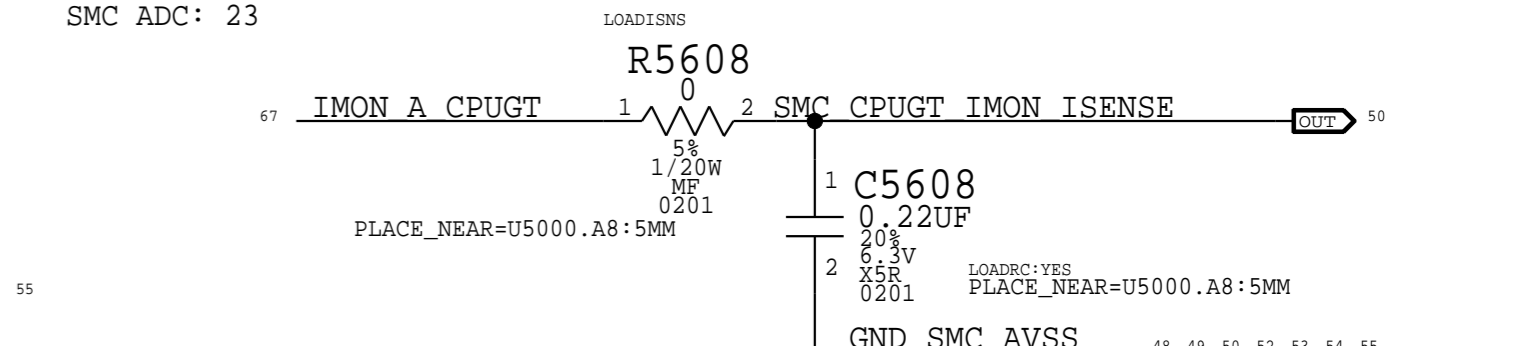
CPU GT Voltage Sense (VCGC)

SMC ADC: 21



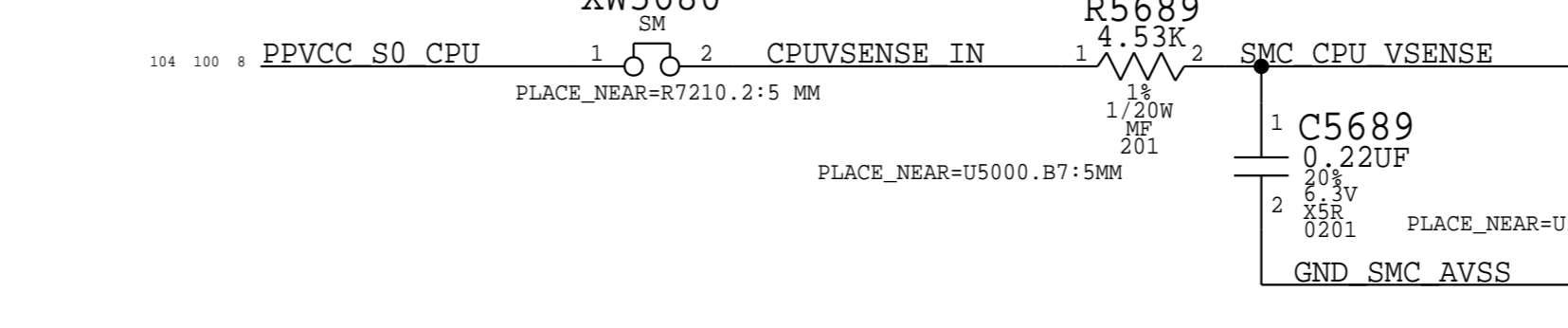
CPU GT IMON Current Sense (ICGM)

Gain: 1 A / 17.963 mV, Range: 64 A.
 SMC ADC: 23



CPU Core Voltage Sense (VCAC)

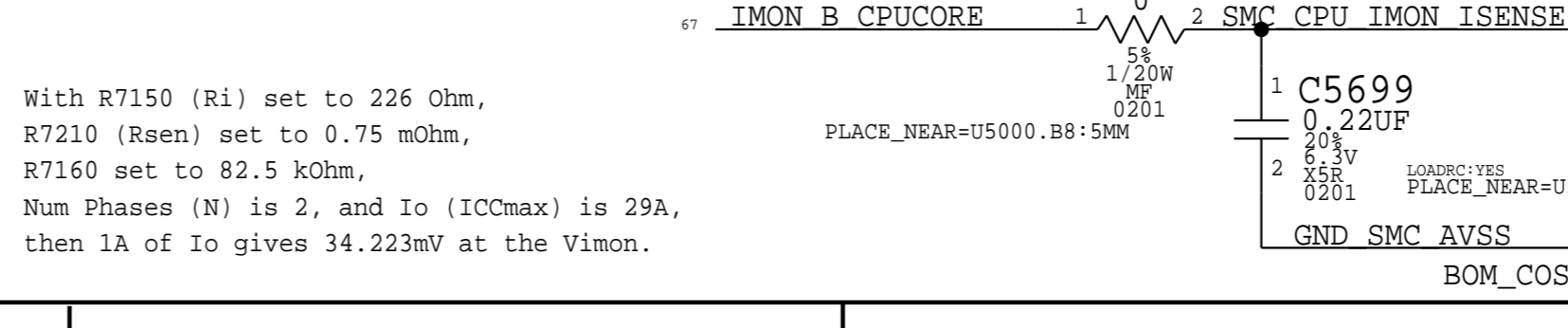
SMC ADC: 20



With R7154 (Ri) set to 294 Ohm, R7410 (Rsen) set to 0.75 mOhm, R7194 set to 84.5 kOhm, Num Phases (N) is 3, and Io (ICmax) is 64A, then 1A of Io gives 17.963mV at the Vimon.

CPU Core IMON Current Sense (ICAM)

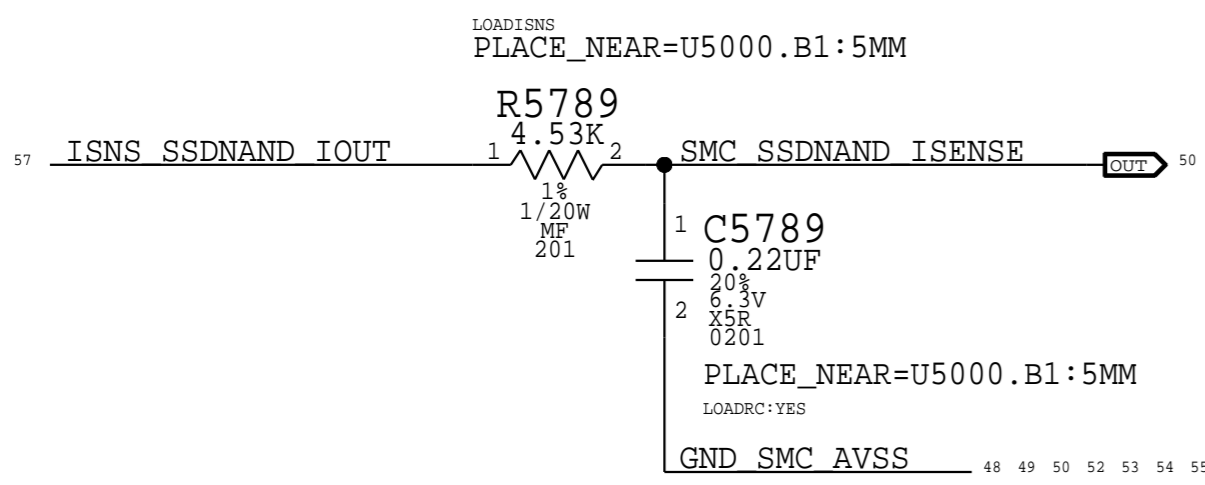
Gain: 1 A / 34.223 mV, Range: 29 A.
 SMC ADC: 22



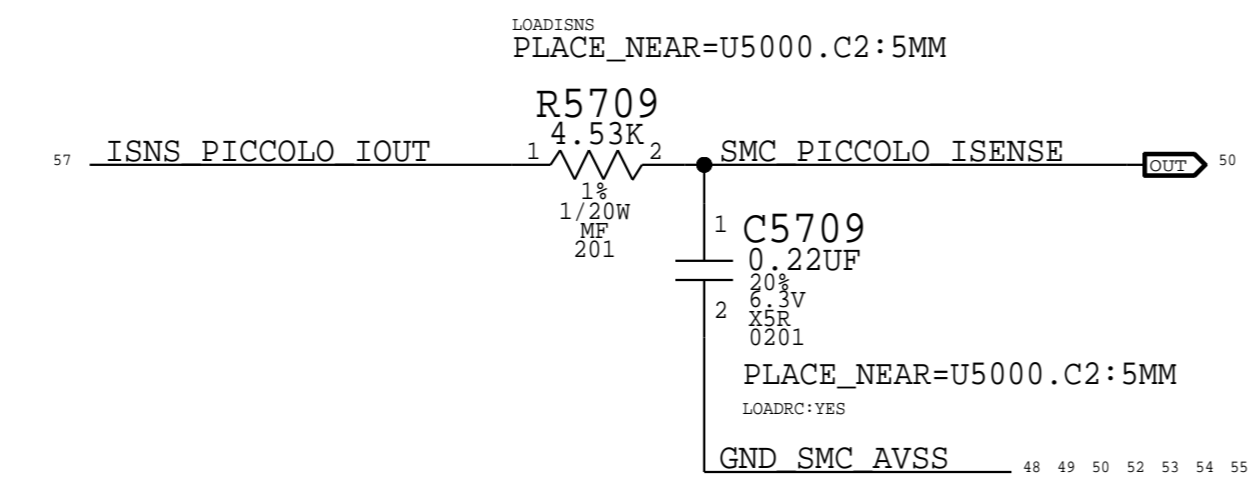
With R7150 (Ri) set to 226 Ohm, R7210 (Rsen) set to 0.75 mOhm, R7160 set to 82.5 kOhm, Num Phases (N) is 2, and Io (ICmax) is 29A, then 1A of Io gives 34.223mV at the Vimon.

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NAND Current Sense (IHNC)

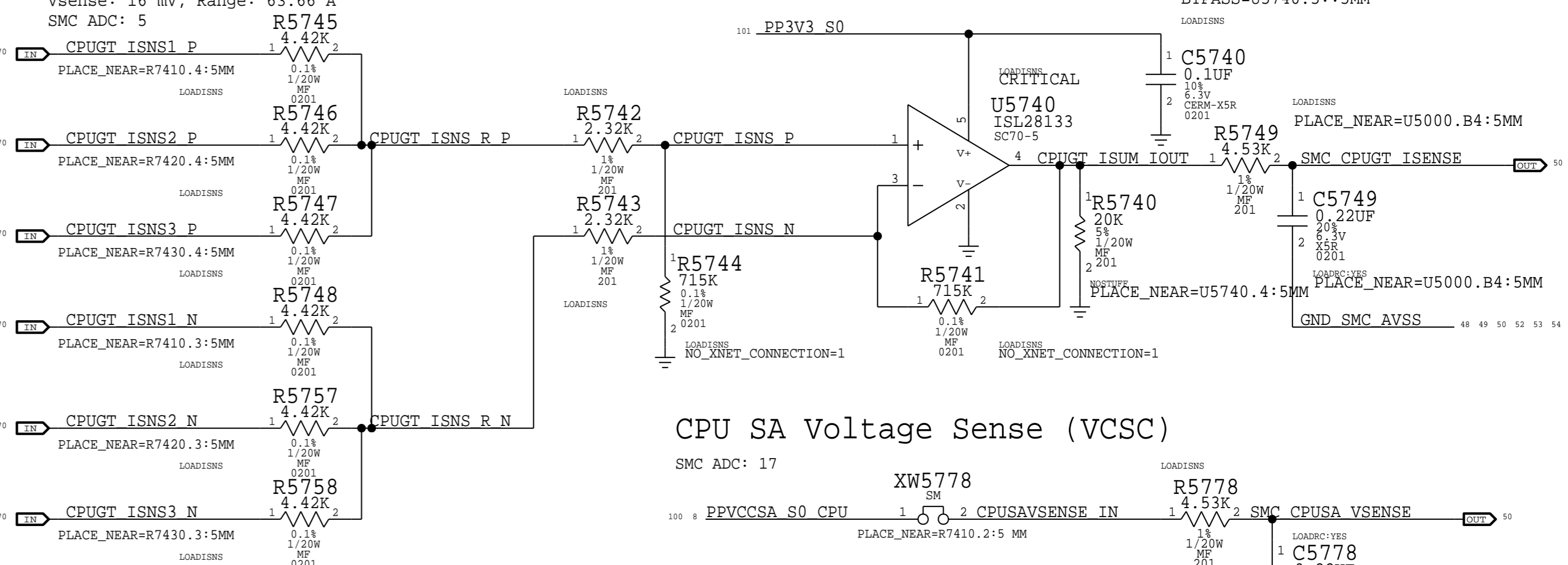


PICCOLO Current Sense (IHCC)



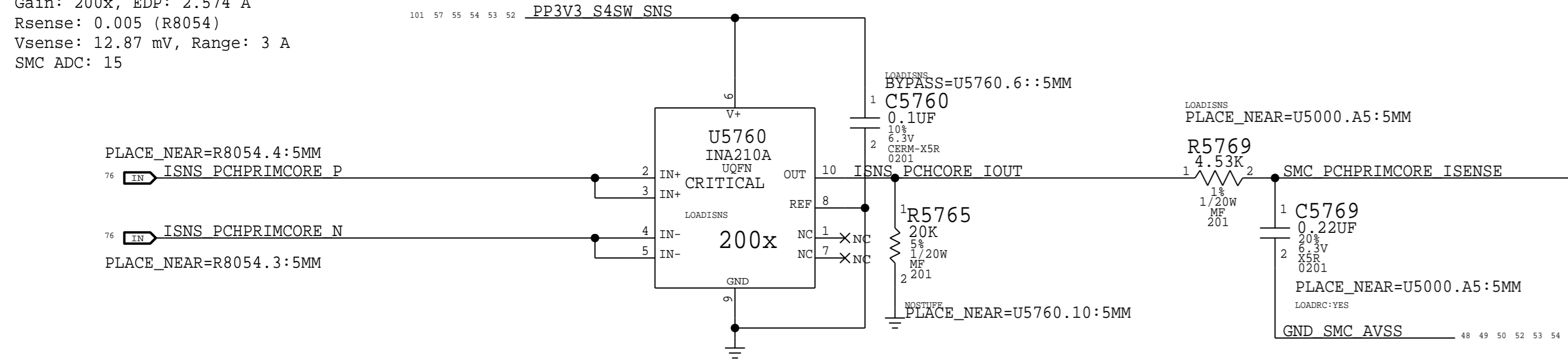
CPU GT+GTX Current Sense (ICGC)

Gain: 188.49x, EDP: 64 A
 Rsense: 3x of 0.00075 (R7410, R7420, R7430), Rsum: 0.00025
 Vsense: 16 mV, Range: 63.66 A
 SMC ADC: 5



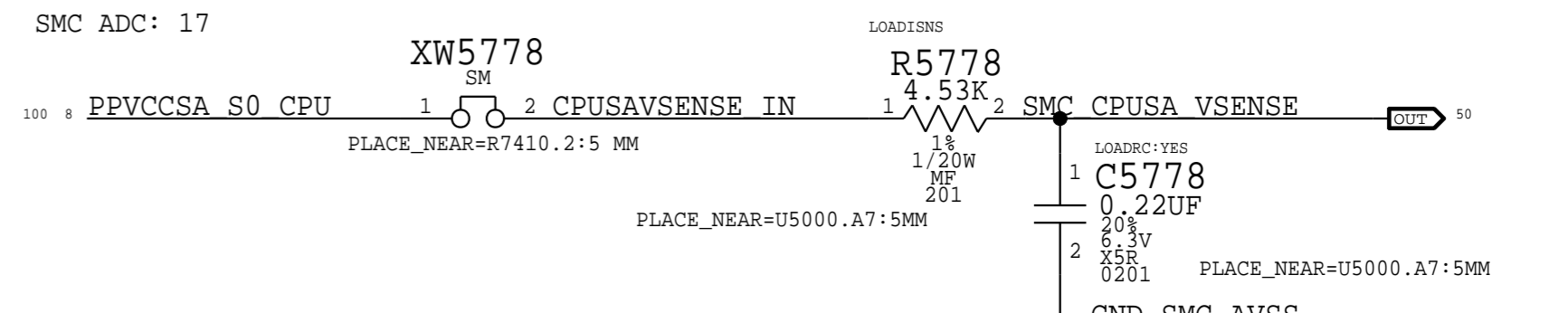
PCH PrimeCore Current Sense (ISCC)

Gain: 200x, EDP: 2.574 A
 Rsense: 0.005 (R8054)
 Vsense: 12.87 mV, Range: 3 A
 SMC ADC: 15



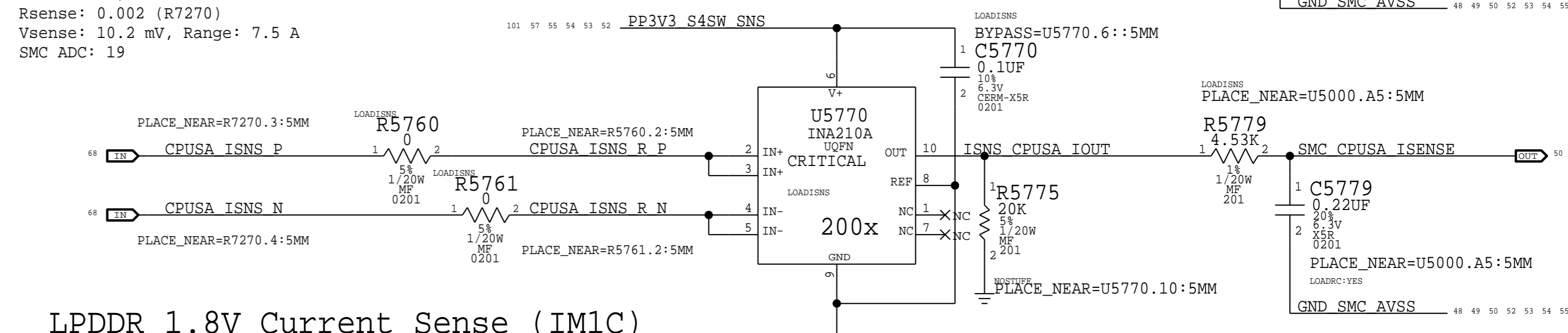
CPU SA Voltage Sense (VCSC)

SMC ADC: 17



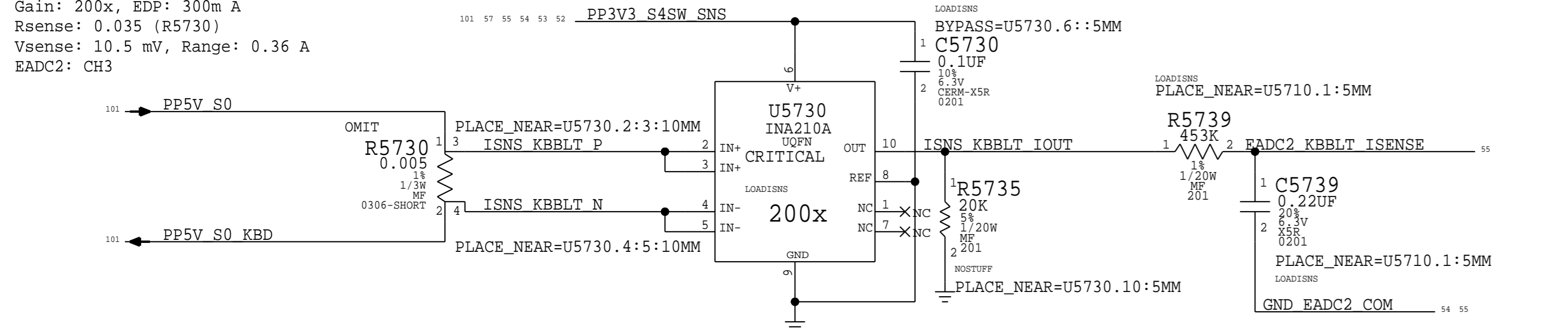
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 5.1 A
 Rsense: 0.002 (R7270)
 Vsense: 10.2 mV, Range: 7.5 A
 SMC ADC: 19



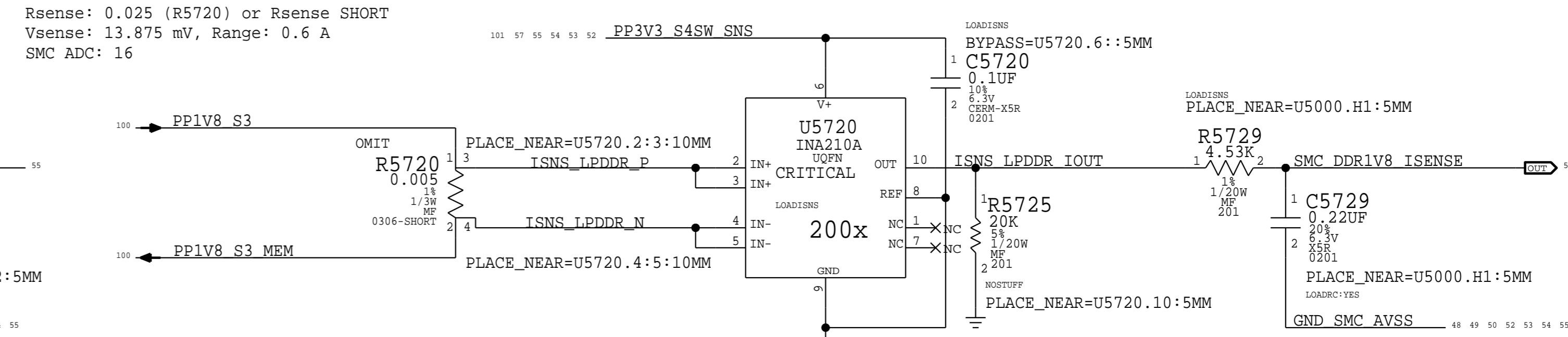
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
 Rsense: 0.035 (R5730)
 Vsense: 10.5 mV, Range: 0.36 A
 EADC2: CH3



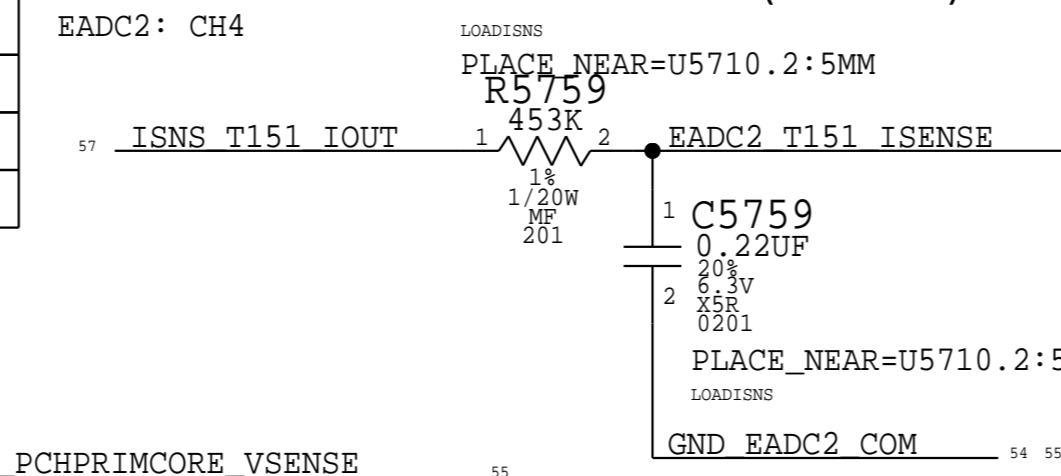
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.555 A
 Rsense: 0.025 (R5720) or Rsense SHORT
 Vsense: 13.875 mV, Range: 0.6 A
 SMC ADC: 16



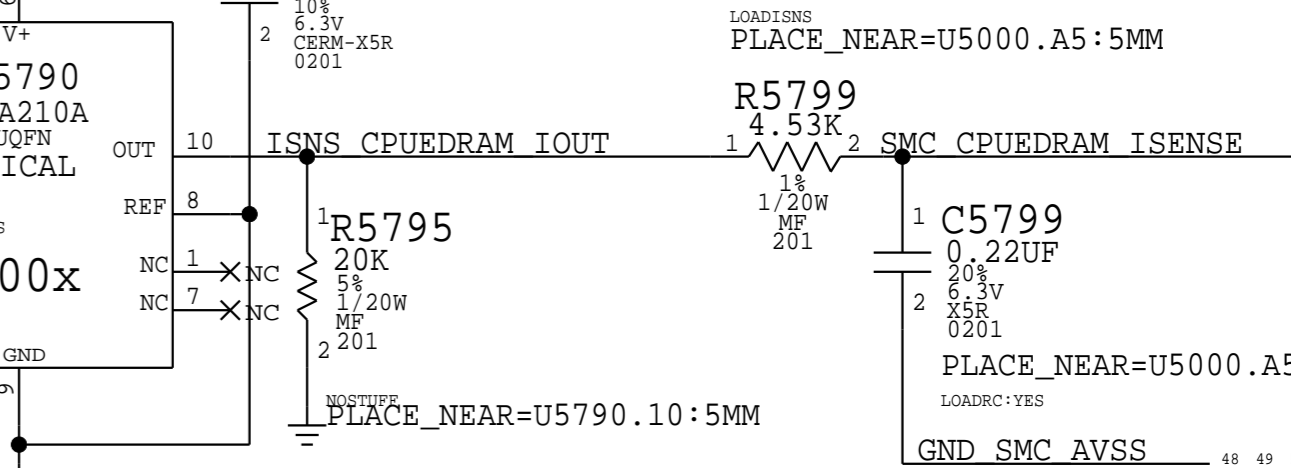
T151 Current Sense (I1DC)

EADC2: CH4

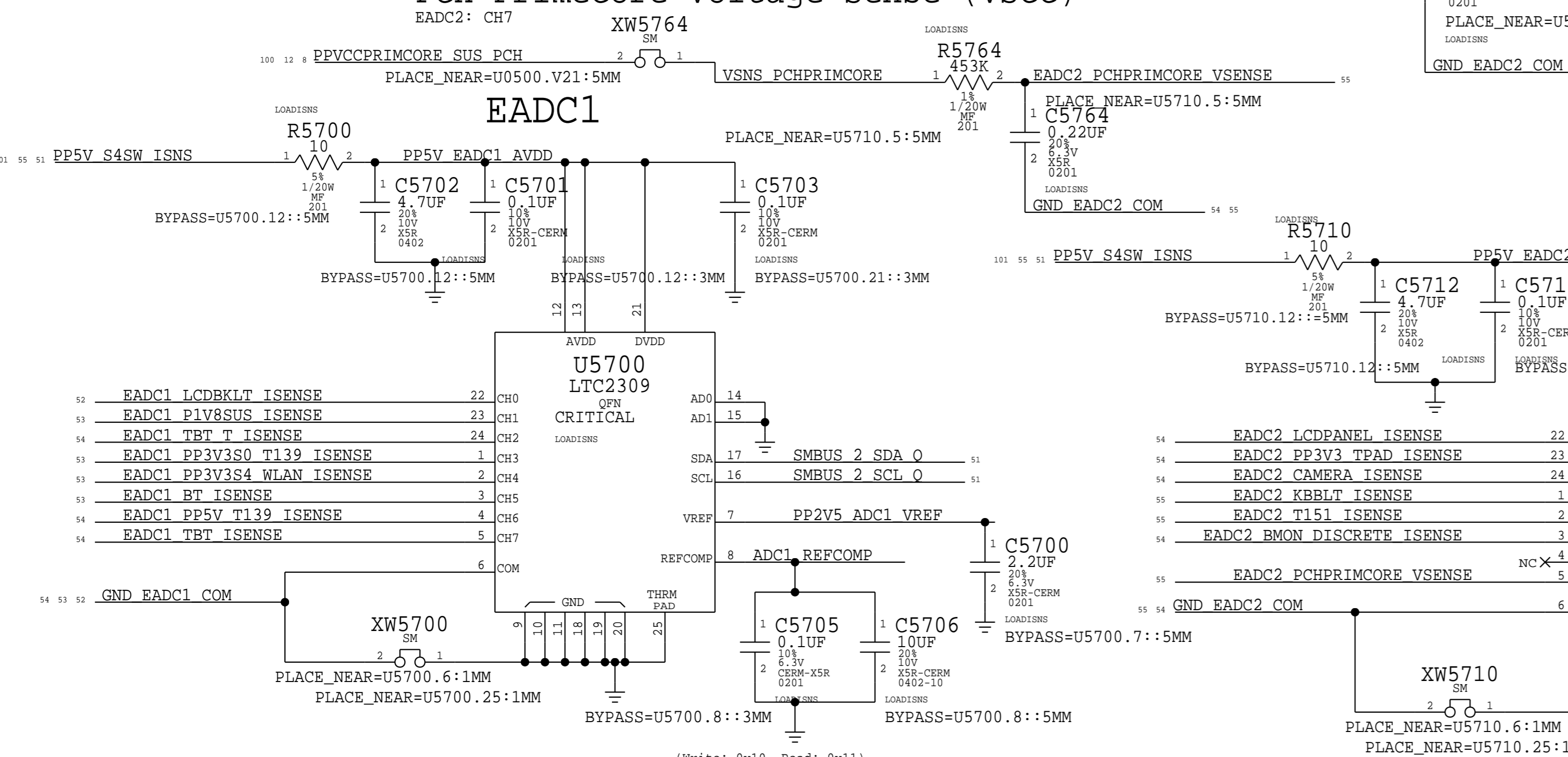


CPU EDRAM Current Sense (ICEC)

Gain: 200x, EDP: 4.5 A
 Rsense: 0.003 (R7718)
 Vsense: 13.5 mV, Range: 5 A
 SMC ADC: 10



PCH PrimeCore Voltage Sense (VSCC)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5769,C5778		LOADRC:NO
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5749,C5779		LOADRC:NO
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5729,C5799		LOADRC:NO
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5709,C5789		LOADRC:NO

EADC2

Power Sensors: Extended 2

Apple Inc.

051-00515

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dvt-fab09-0

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55 OF 119

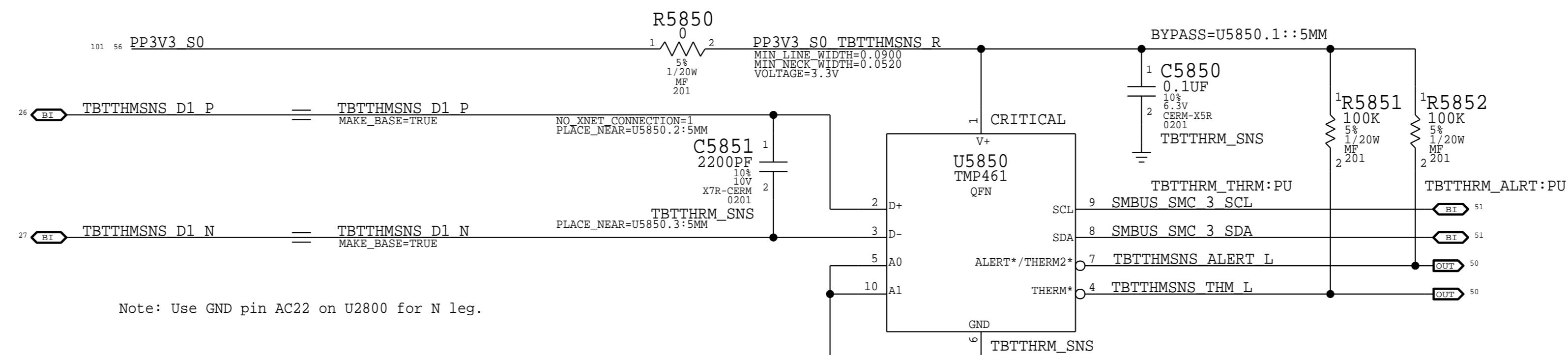
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**Thermal Sensor A:
Thunderbolt Die, Airflow Left**

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TBT1)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



U5850 I2C Address: TMP461 is 0x90/0x91.

Note: Use GND pin AC22 on U2800 for N leg.

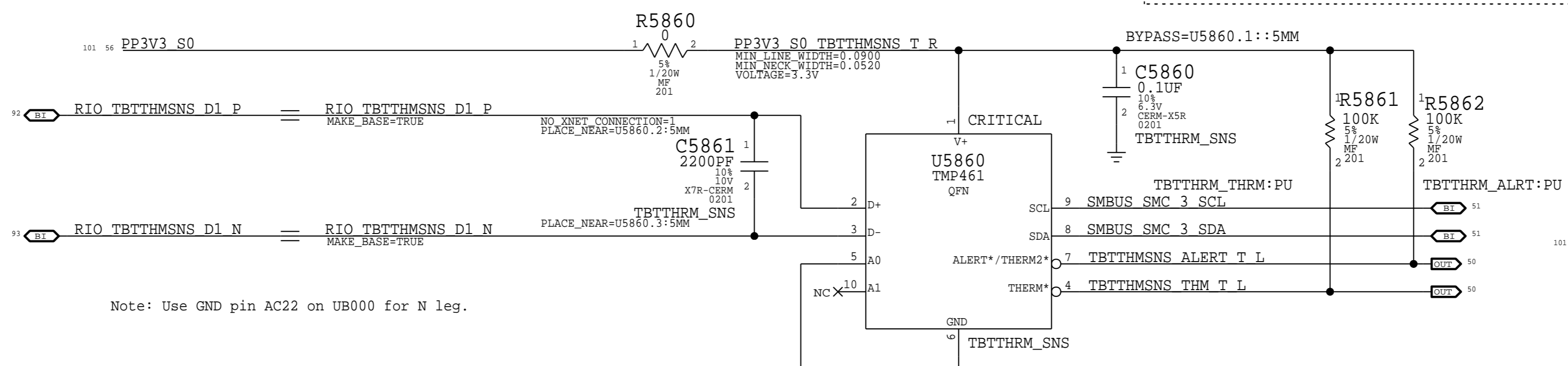
Placement Note:
Place U5850 on the BOTTOM side, on the left portion of the board, 1" to the right of USB connector.

**Thermal Sensor C:
Thunderbolt Die, Air Flow Right**

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: TBT Die (TBT2)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.

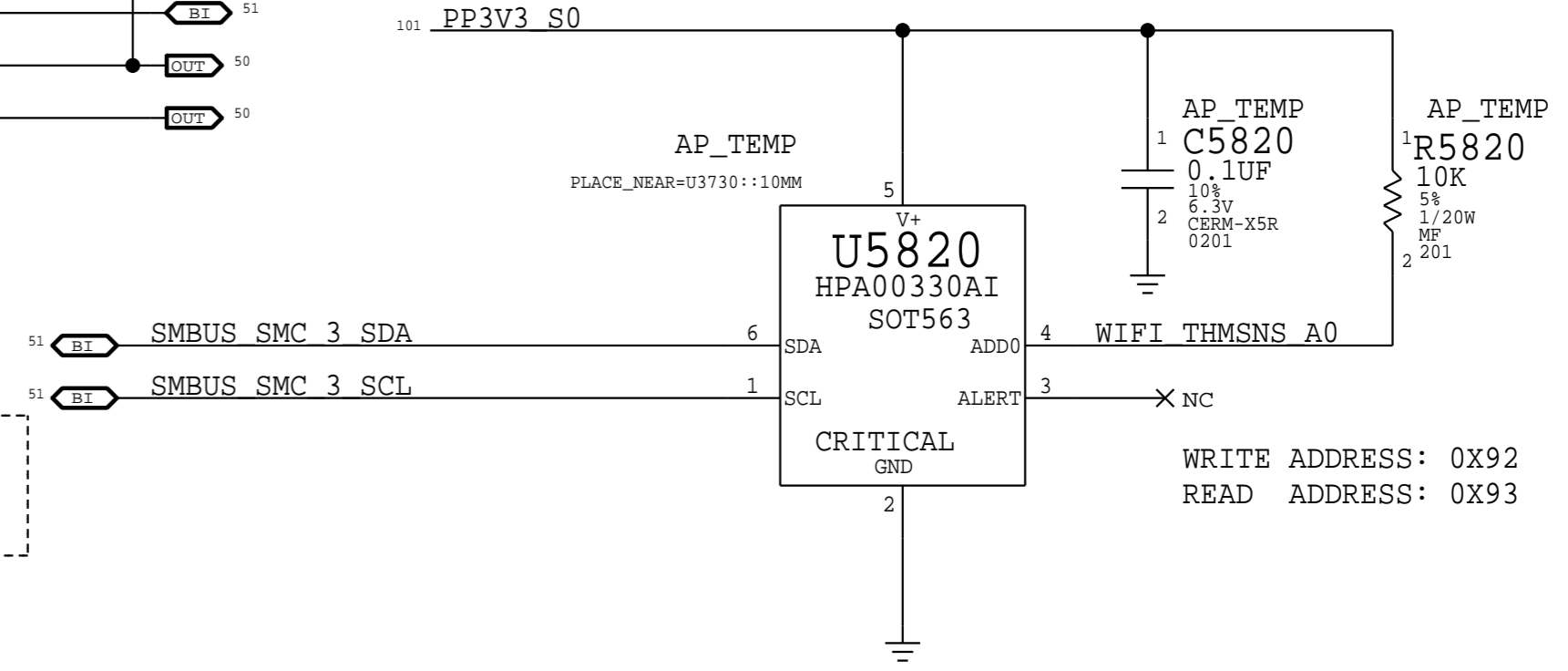


U5860 I2C Address: TMP461 is 0x96/0x97.

Note: Use GND pin AC22 on UB000 for N leg.

Placement Note:
Place U5860 on the BOTTOM side, on the right portion of the board, 1" to the left of USB connector.

X100 PROXIMITY



WRITE ADDRESS: 0x92
READ ADDRESS: 0x93

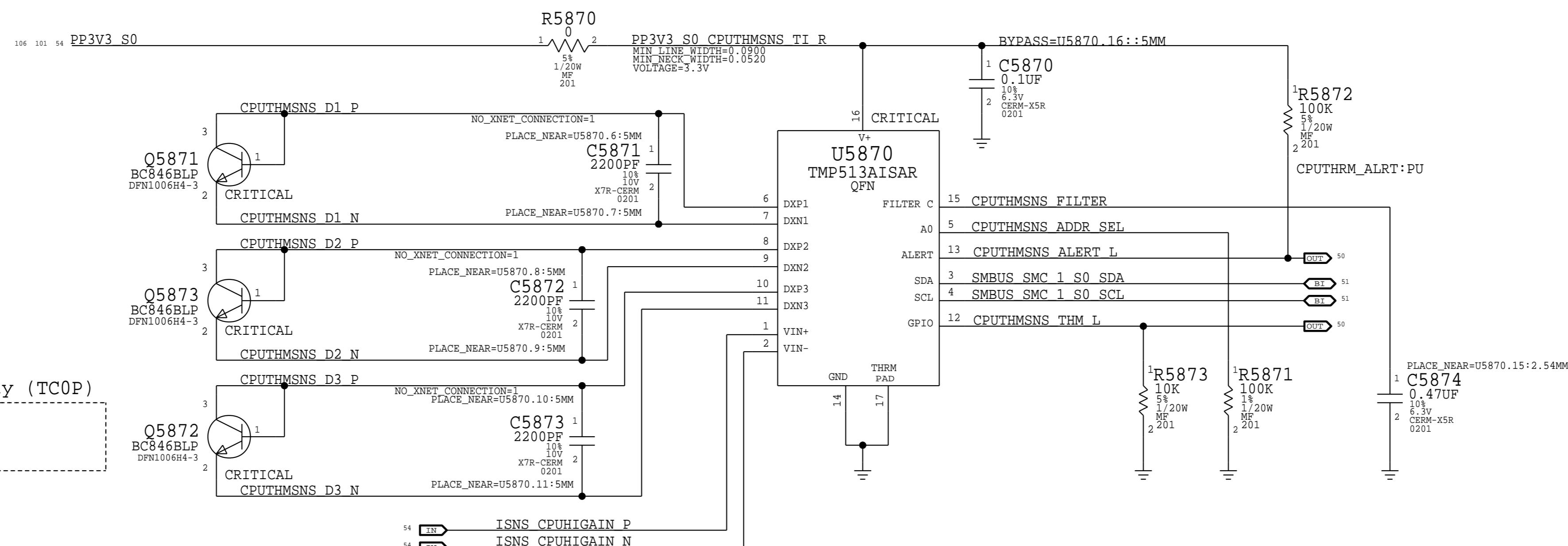
Placement note:
PLACE U5820 ON BOTTOM NEAR X100

**Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right**

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.



Thermal Diode: CPU Proximity (TCOP)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Diode: Memory Proximity (TMOP)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Sensor: Fin Stack Right (Th1H)

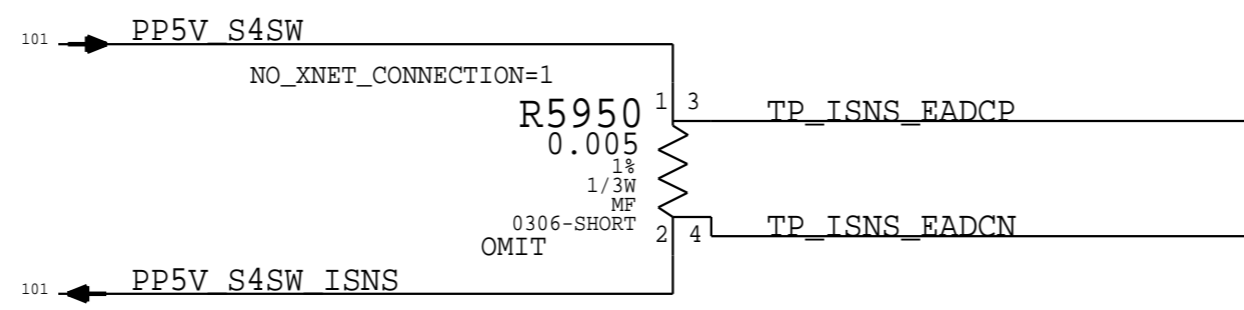
Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

BOM_COST_GROUP=SENSORS

<p>Apple Inc.</p>			<p>DRAWING NUMBER 051-00515</p>	<p>SIZE D</p>
<p>NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED</p>			<p>REVISION 9.0.0</p>	<p>BRANCH dvt-fab09-0</p>
<p>Thermal Sensors</p>			<p>PAGE 58 OF 145</p>	<p>SHEET 56 OF 119</p>

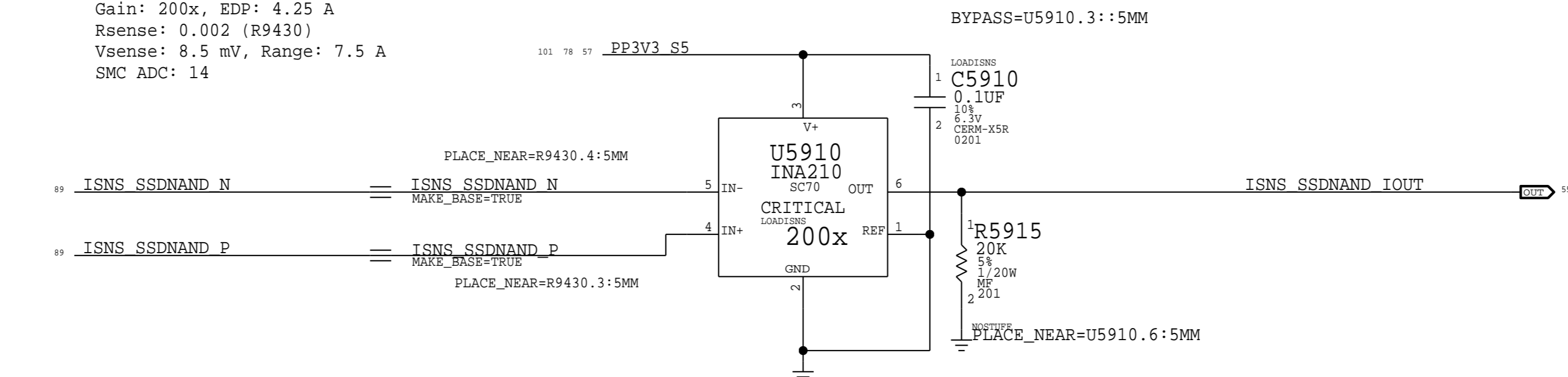
EADC Current Sense (IADC)

Gain: 200x, EDP: 200m A
 Rsense: 0.050 (R5950) or Rsense SHORT
 Vsense: 10 mV, Range: 0.25 A
 EADC2: CH7



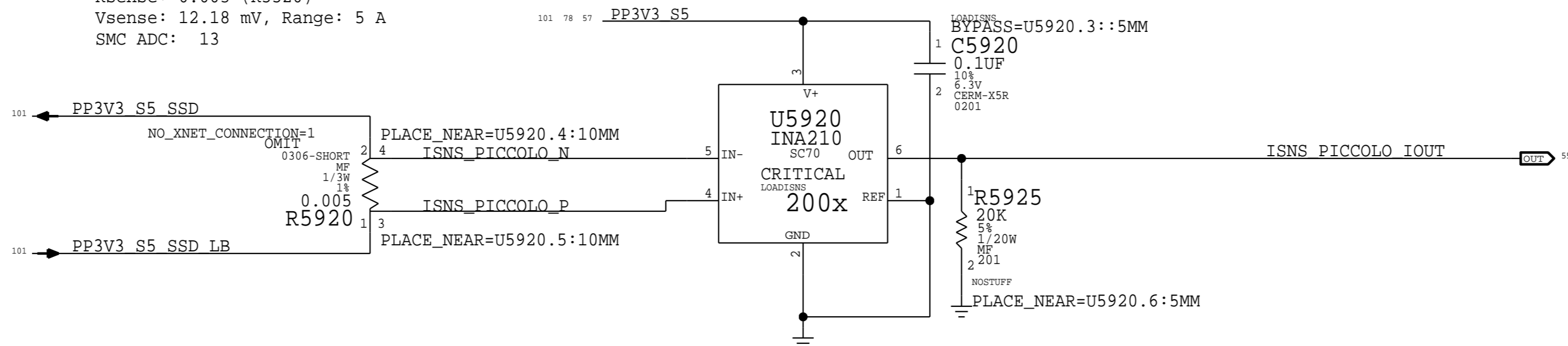
NAND Current Sense (IHNC)

Gain: 200x, EDP: 4.25 A
 Rsense: 0.002 (R9430)
 Vsense: 8.5 mV, Range: 7.5 A
 SMC ADC: 14



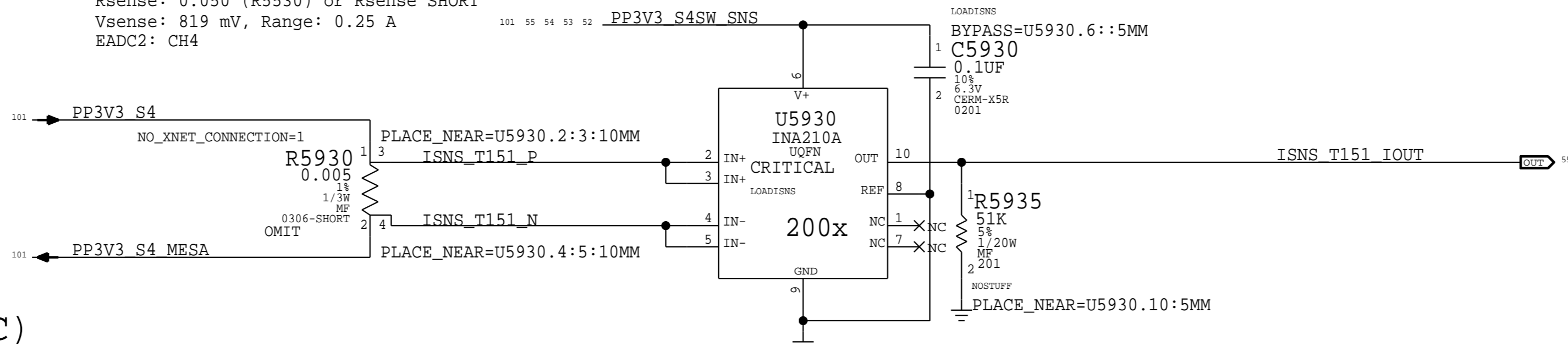
Piccolo Current Sense (IHCC)

Gain: 200x, EDP: 4.06 A
 Rsense: 0.003 (R5520)
 Vsense: 12.18 mV, Range: 5 A
 SMC ADC: 13



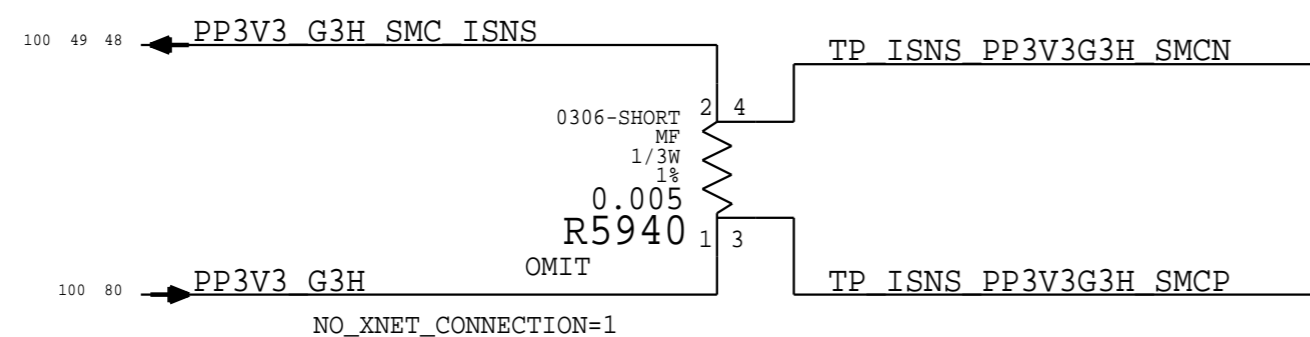
T151 Current Sense (IIDC)

Gain: 200x, EDP: 163.8m A
 Rsense: 0.050 (R5530) or Rsense SHORT
 Vsense: 819 mV, Range: 0.25 A
 EADC2: CH4



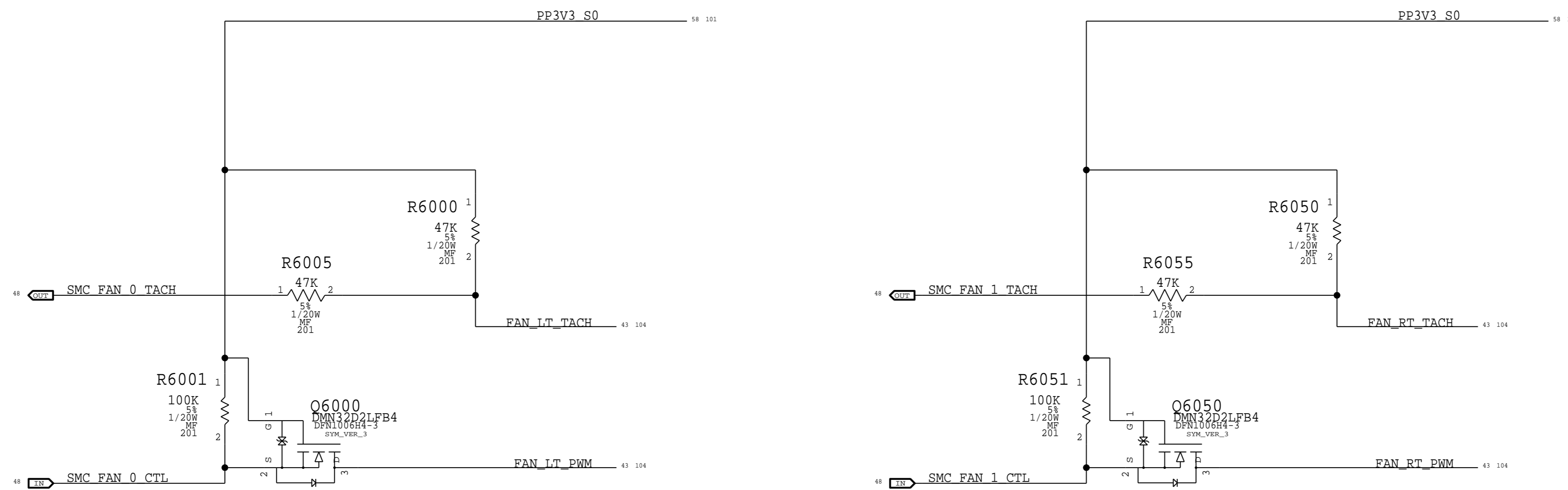
SMC Current Sense (ISMC)

Gain: 391.67x, EDP: 0.2 A
 Rsense: 0.05 (R5940) or Rsense SHORT
 Vsense: 10 mV, Range: 0.21A
 EADC2: CH6

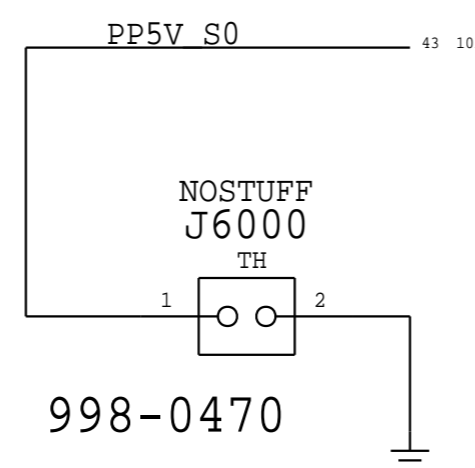


PAGE TITLE Power Sensors:Extended 3		
Apple Inc.	DRAWING NUMBER 051-00515	SIZE D
	REVISION 9.0.0	
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FAN CONTROL



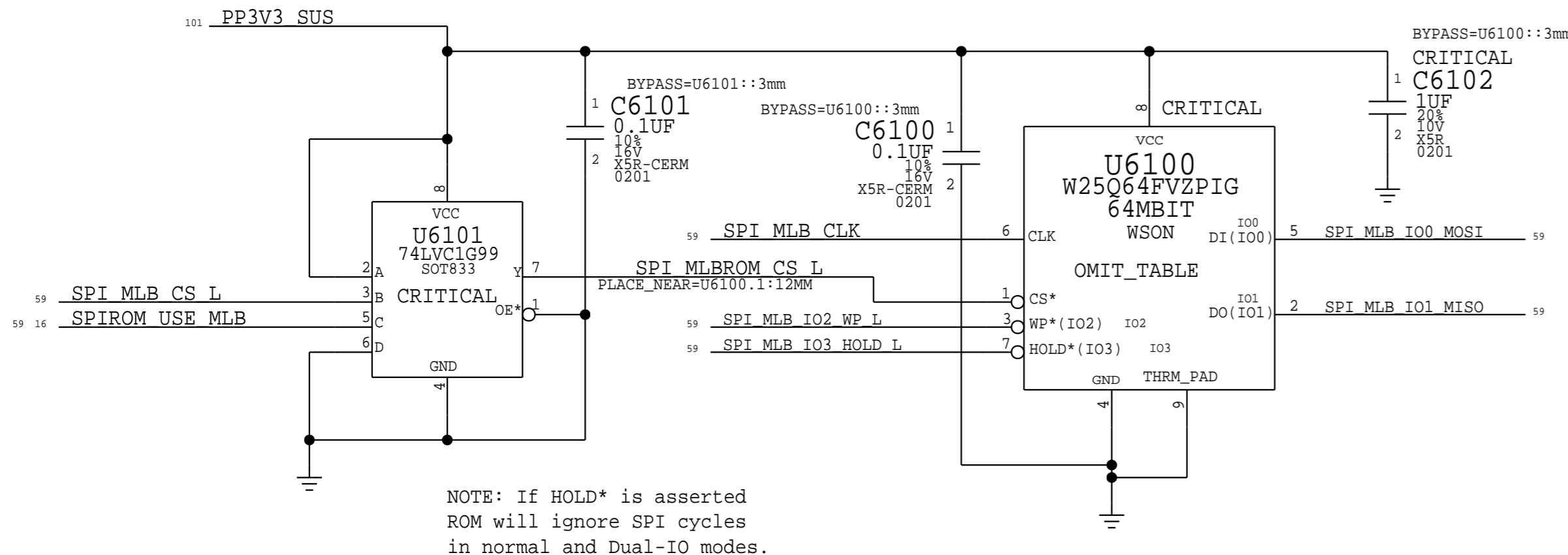
FOR DEBUG FAN POWER



EVMC_MASTER=779_JACK		SYMC_DATE=08/21/2015	
PAGE TITLE			
Fans		DRAWING NUMBER	SIZE
Apple Inc.		051-00515	D
		REVISION	
		9.0.0	
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		dtv-fab09-0	
		PAGE	60 OF 145
		SHEET	58 OF 119

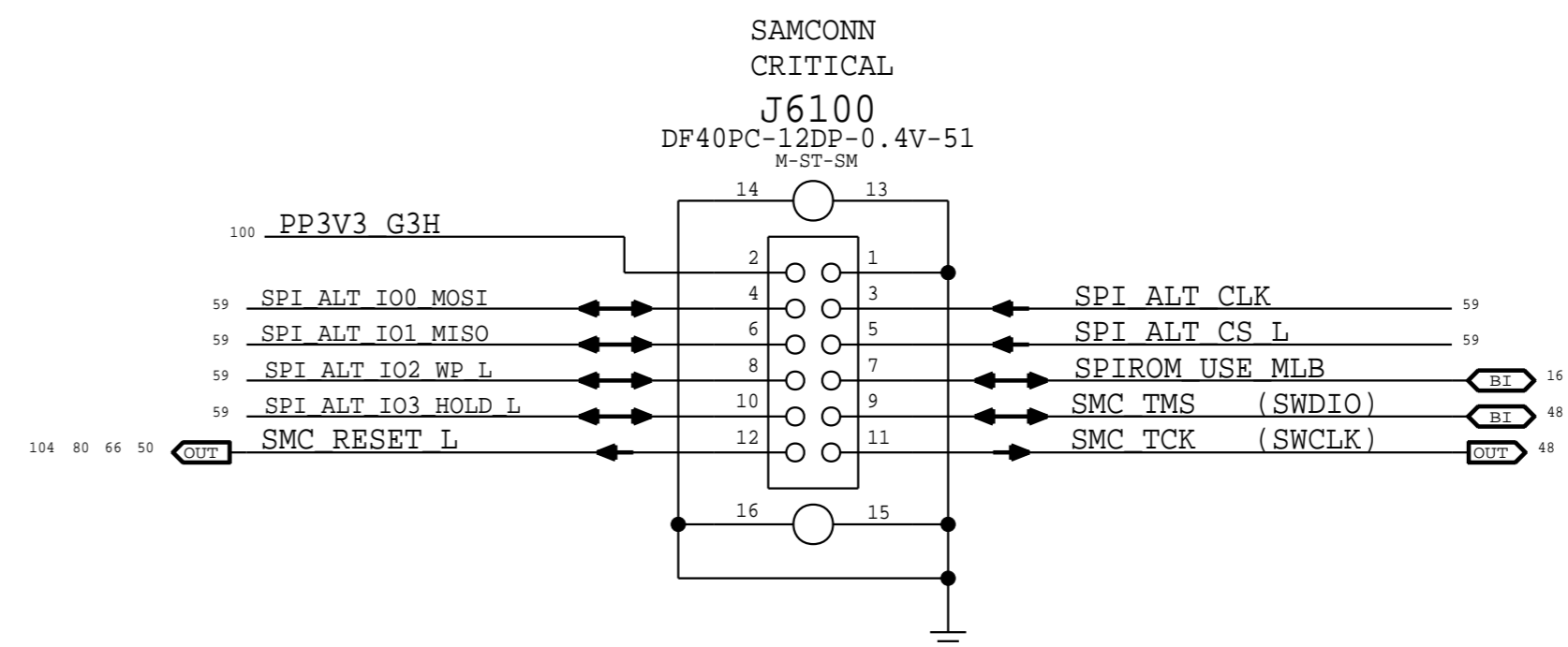
SPI ROM

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

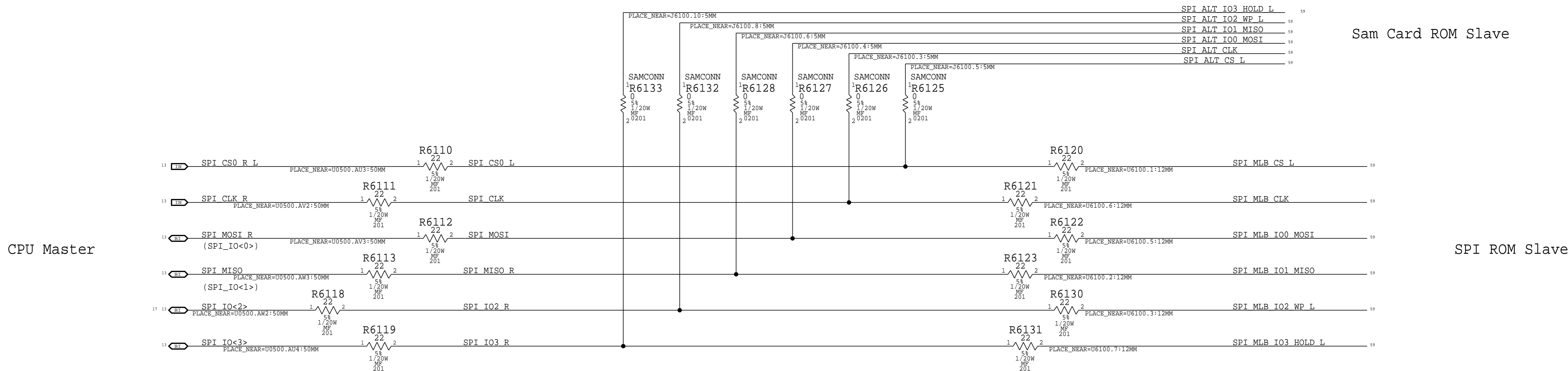


Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)



SYNC_MASTER=J52_MLB		SYNC_DATE=05/12/2015	
PAGE TITLE			
SPI Debug Connector			
	DRAWING NUMBER	051-00515	STEP
	REVISION	9.0.0	D
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		PAGE	61 OF 145
		SHEET	59 OF 119
		BOM_COST_GROUP=CPU & CHIPSET	

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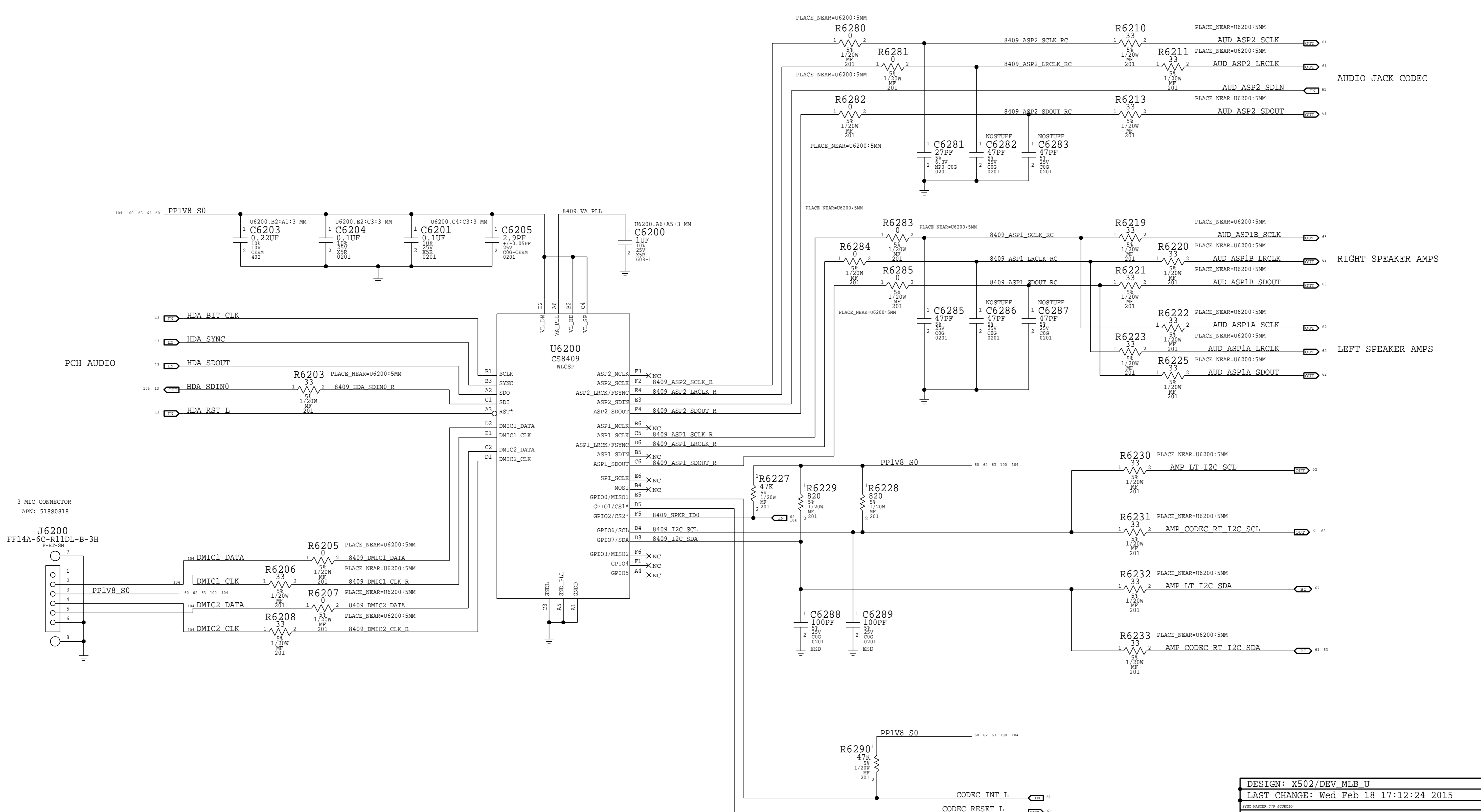
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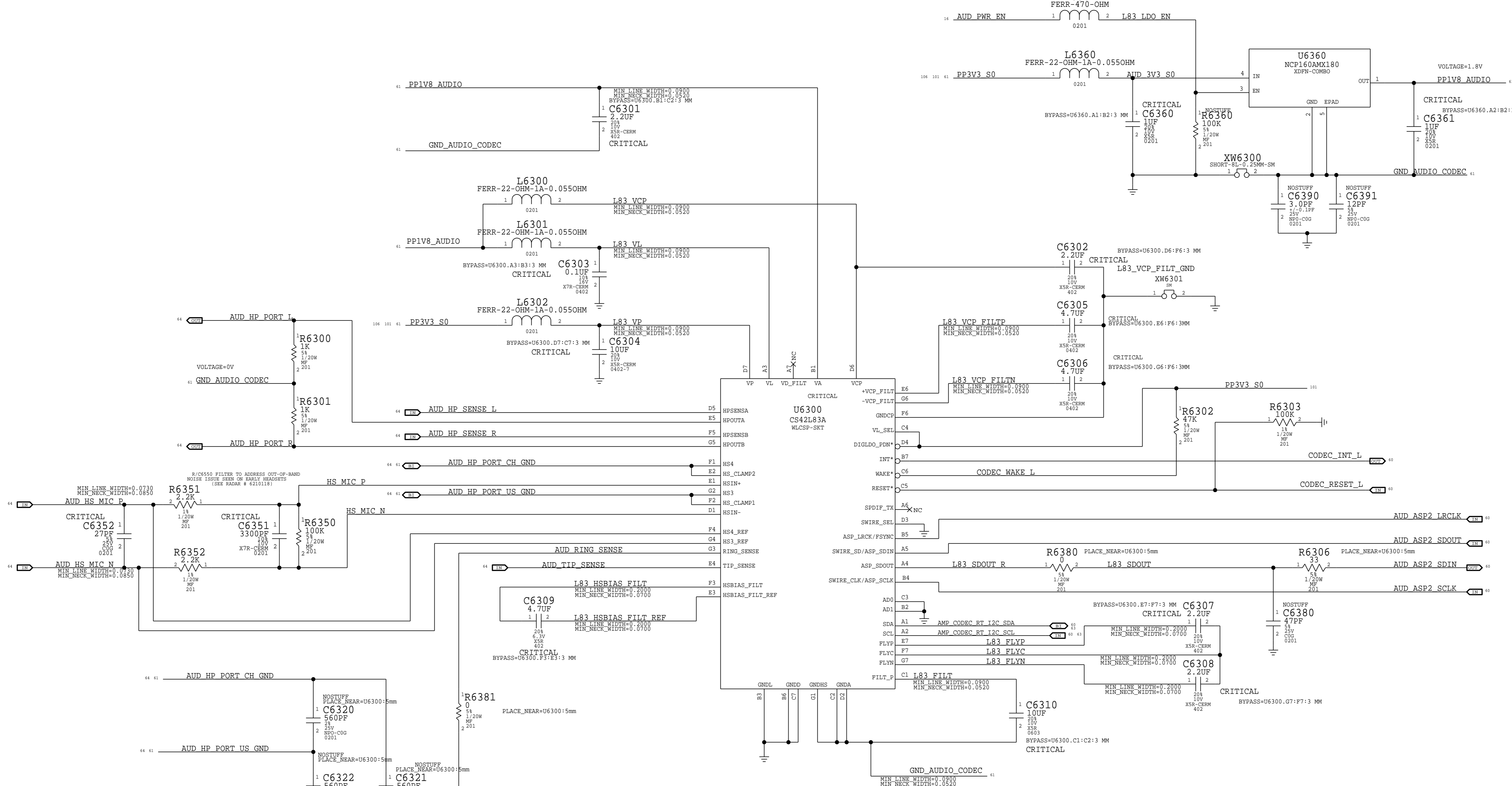
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BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U	
LAST CHANGE: Wed Feb 18 17:12:24 2015	
PAGE TITLE	
HDA Bridge	
	DRAWING NUMBER 051-00515 REVISION 9.0.0 BRANCH dvt-fab09-0 PAGE 62 OF 145 SHEET 60 OF 119
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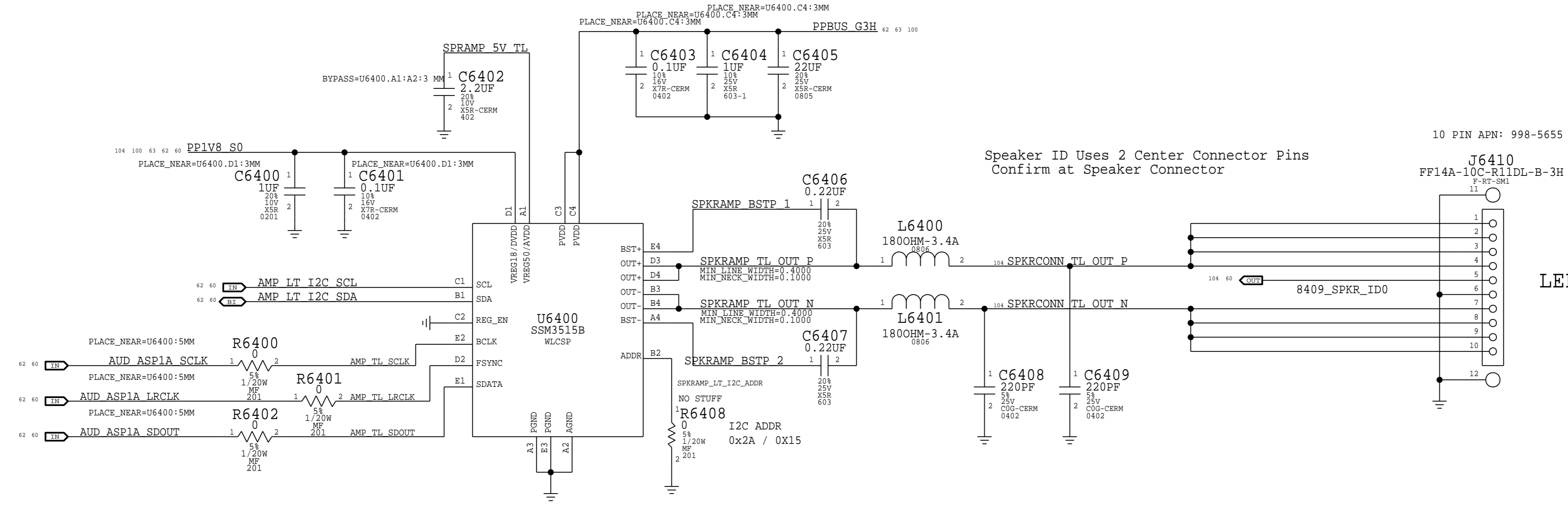
AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0x90 ---
GND	1.8V	0x92
1.8V	GND	0x94
1.8V	1.8V	0x96



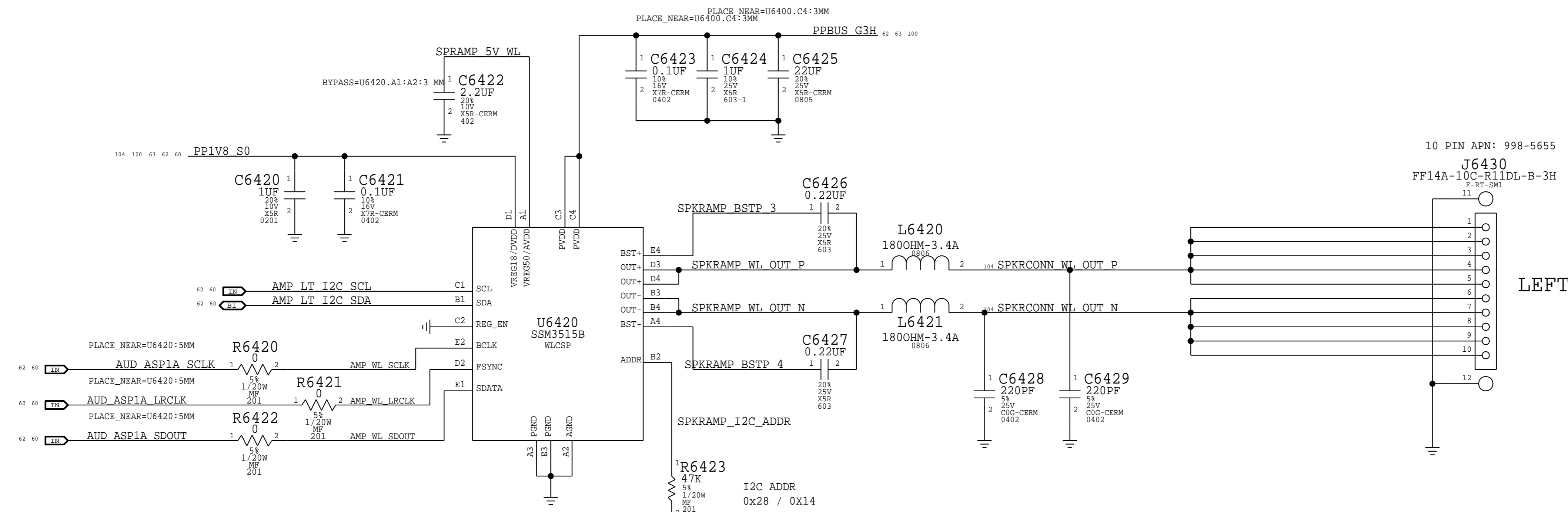
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LAST CHANGE: Wed Feb 18 17:31:01 2015		
PAGE TITLE		
AUDIO JACK CODEC		
	DRAWING NUMBER	051-00515
	REVISION	9.0.0
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	SHEET	61 OF 119

BOM_COST_GROUP=AUDIO

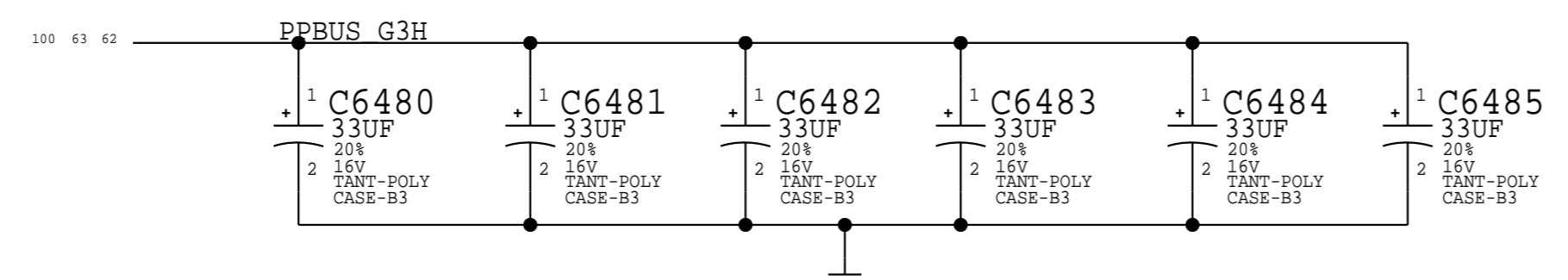
2X MONO SPEAKER AMPLIFIERS
 APN: 35394074
 GAIN = TBD



LEFT TWEETER SPEAKER CONNECTOR



LEFT WOOFER SPEAKER CONNECTOR



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U		
LAST CHANGE: Wed Feb 18 17:12:24 2015		
PAGE TITLE		
Left Speaker Amps & Conn		
	DRAWING NUMBER	051-00515
	REVISION	9.0.0
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2X MONO SPEAKER AMPLIFIERS
 APN: 35384073
 GAIN = TBD

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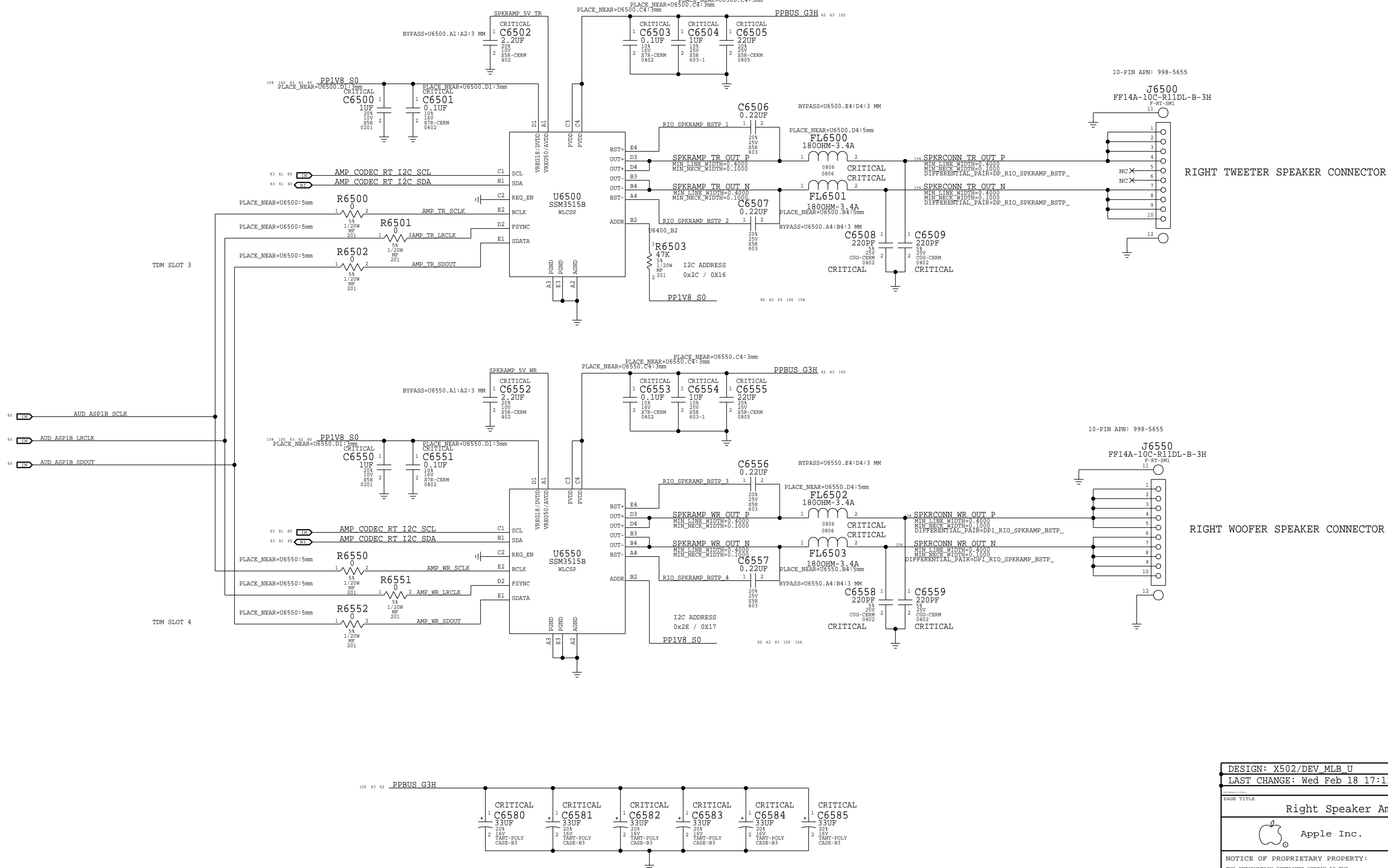
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BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U	
LAST CHANGE: Wed Feb 18 17:12:24 2015	
PAGE TITLE	
Right Speaker Amps & Conn	
	DRAWING NUMBER 051-00515
REVISION 9.0.0	
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BRANCH dvt-fab09-0	PAGE 65 OF 145
SHEET 63 OF 119	STR D

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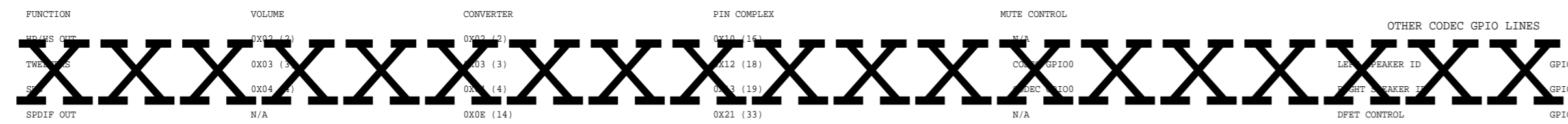
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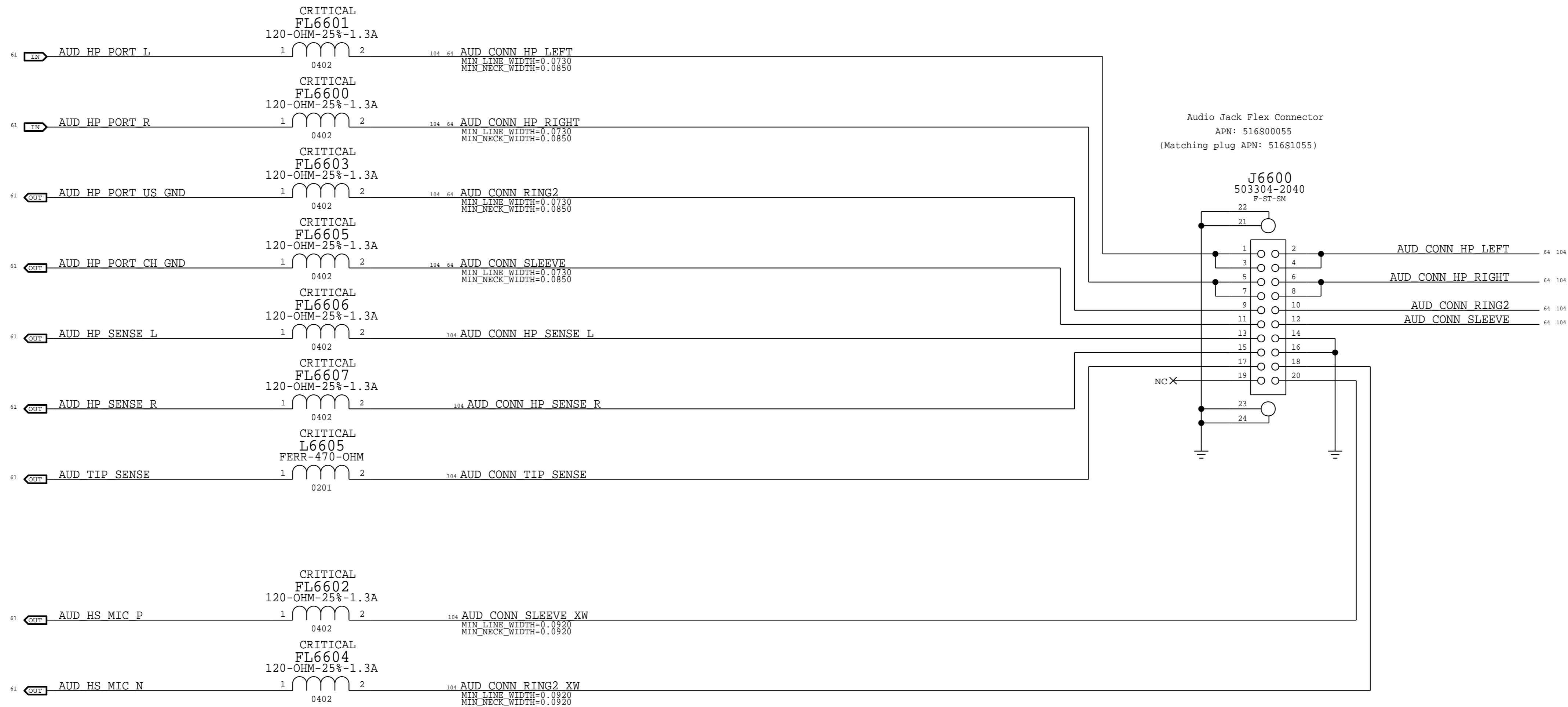
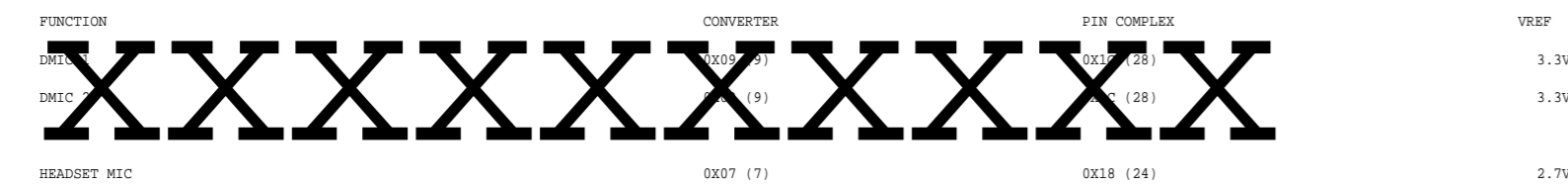
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CODEC OUTPUT SIGNAL PATHS



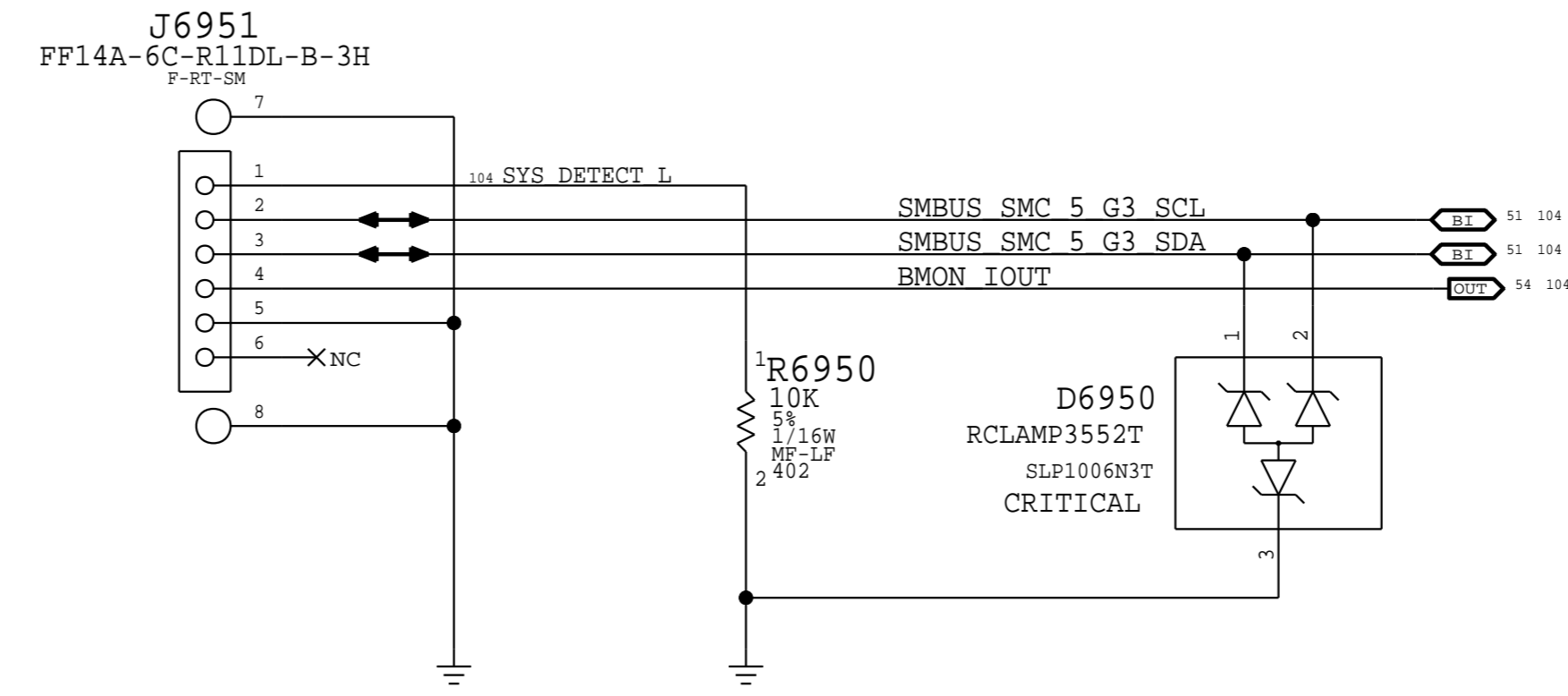
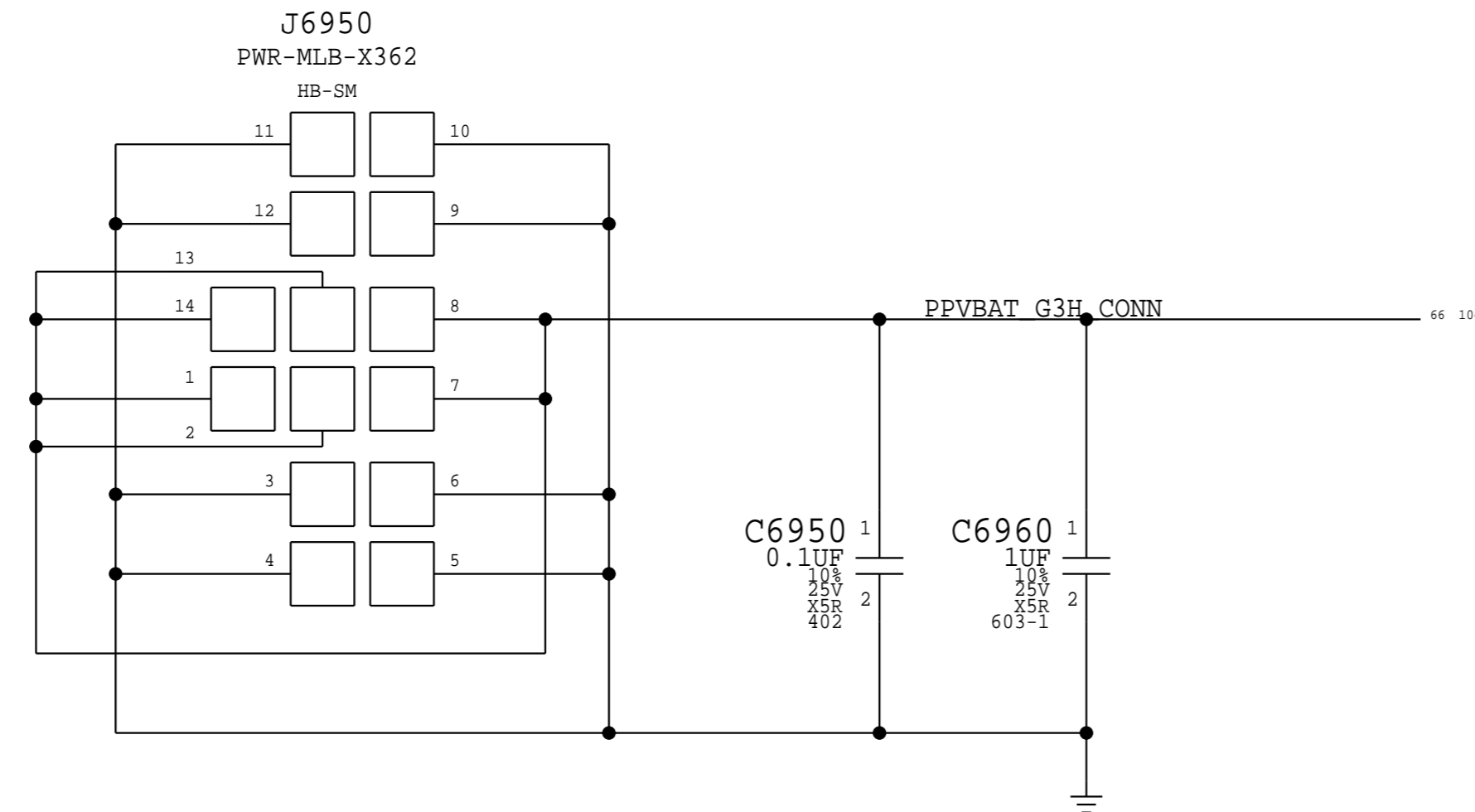
CODEC INPUT SIGNAL PATHS



BOM_COST_GROUP=AUDIO

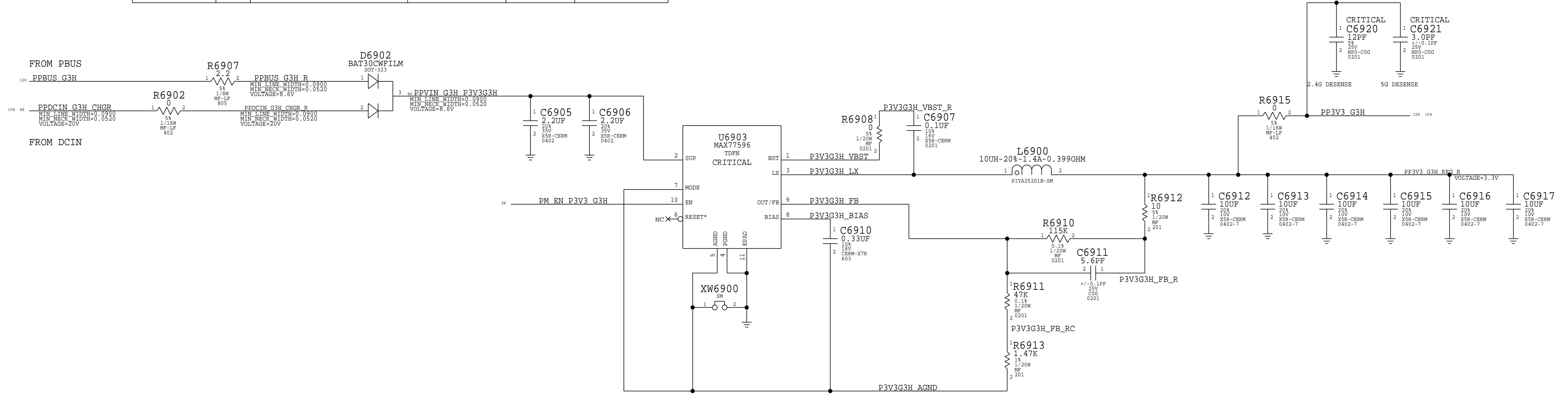
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LAST CHANGE: Wed Feb 18 17:12:24 2015	
PAGE TITLE	
AUDIO JACK CONNECTOR	
	DRAWING NUMBER 051-00515
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J79 Battery Hotbar Flex Pads

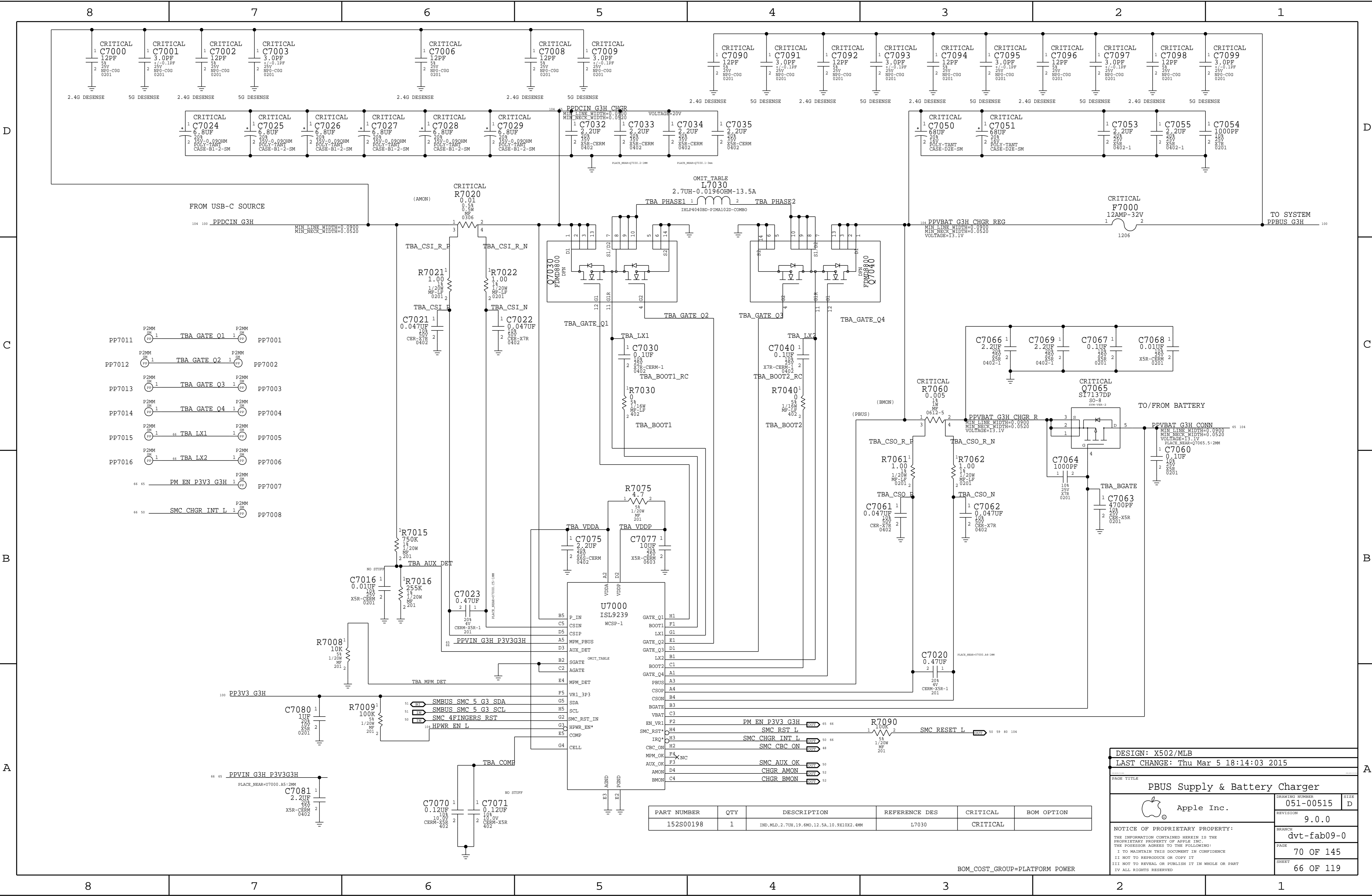


BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00566	1	PCBA, FLEX, BMU PWR, X362	J6950	CRITICAL	



PAGE TITLE		
DC-In & Battery Connectors		
	DRAWING NUMBER	051-00515
	REVISION	9.0.0
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	PAGE	69 OF 145
	SHEET	65 OF 119



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

DESIGN: X502/MLB
 LAST CHANGE: Thu Mar 5 18:14:03 2015

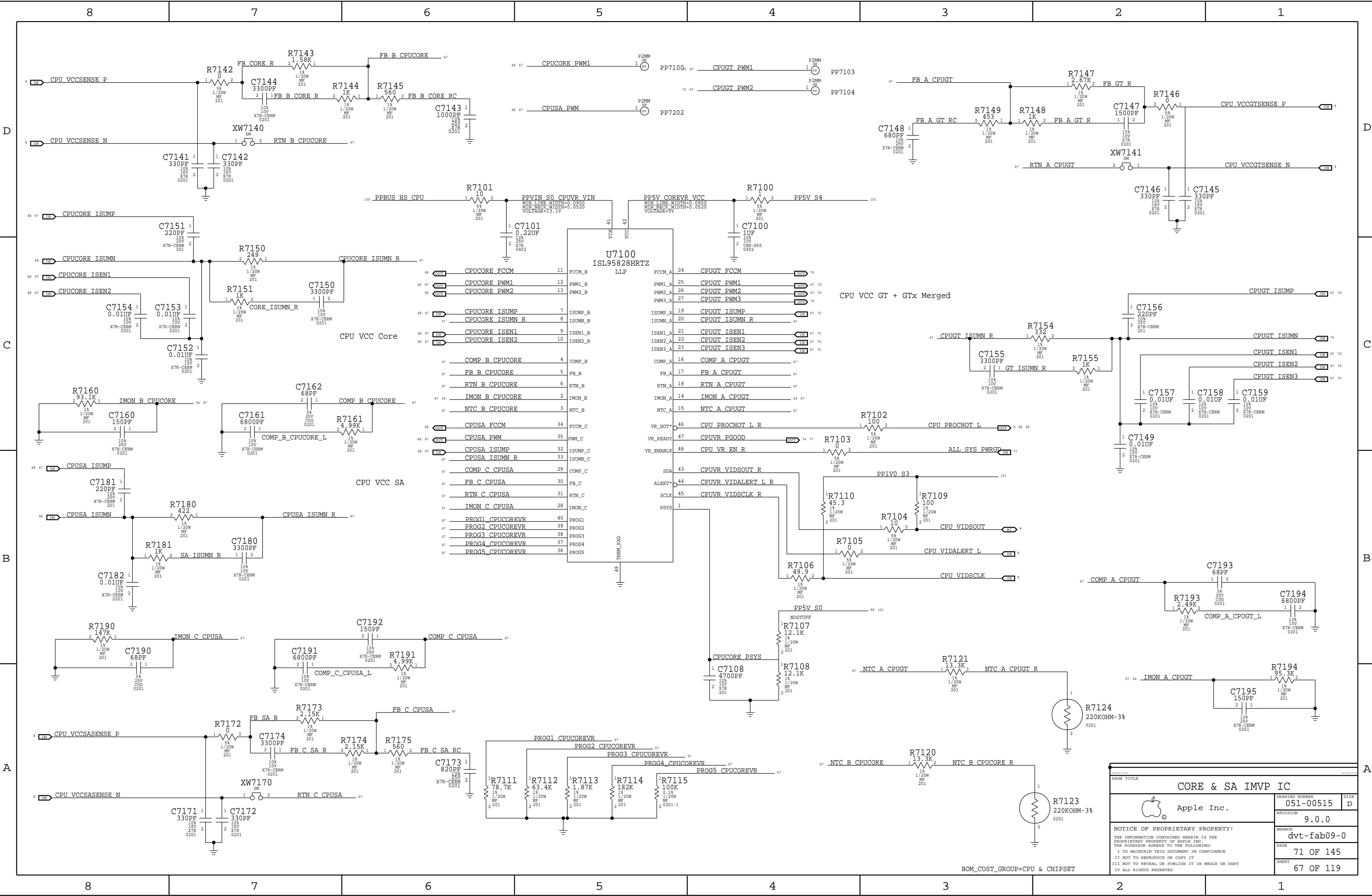
PAGE TITLE
PBUS Supply & Battery Charger


Apple Inc.

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REVISION	9.0.0		
BRANCH	dvt-fab09-0		
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SHEET	66 OF 119		

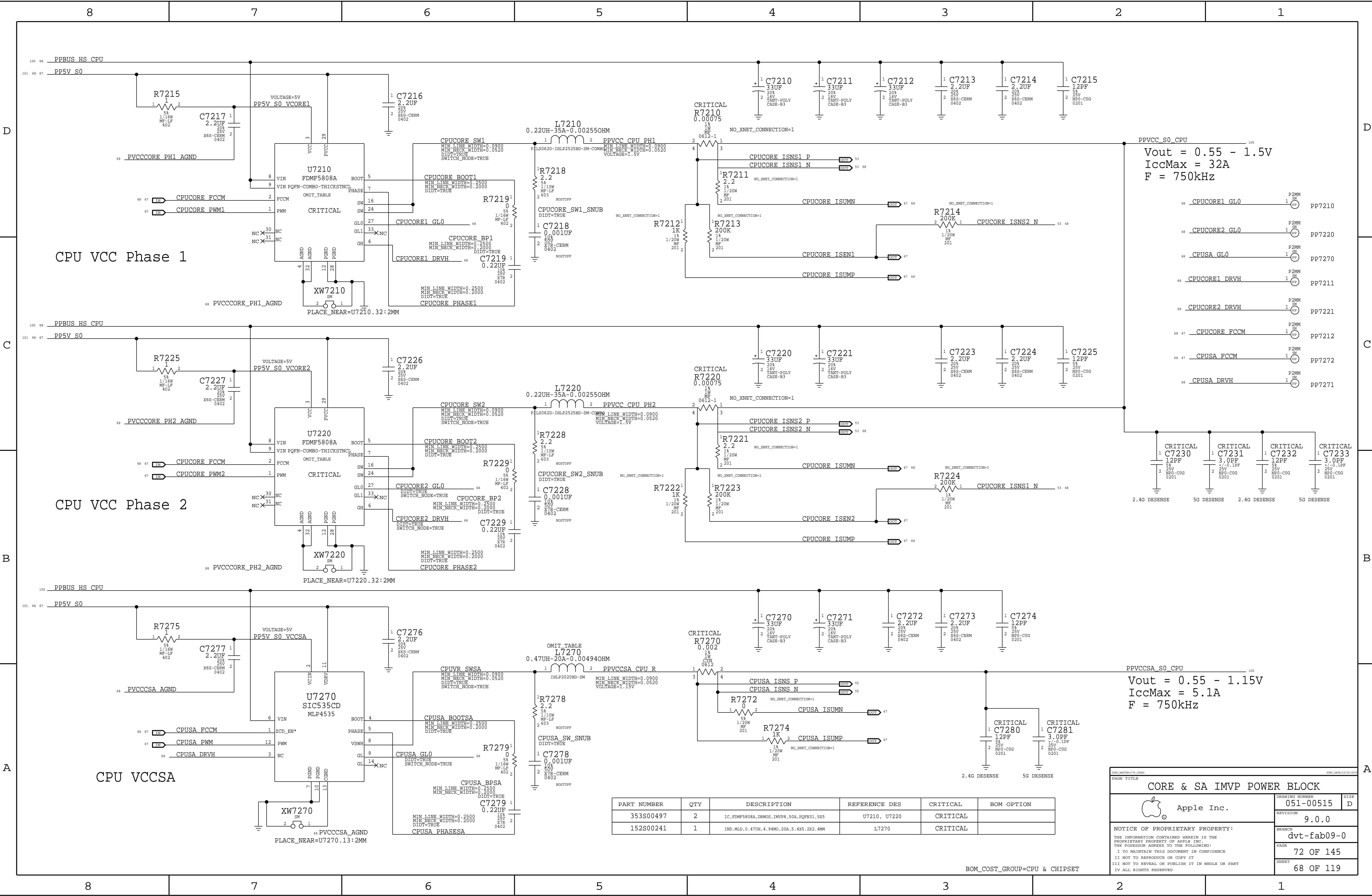
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BOM_COST_GROUP=PLATFORM POWER



PAGE TITLE		
CORE & SA IMVP IC		
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BOM_COST_GROUP=CPU & CHIPSET



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC, FDMF5808A, DRMS, IMVP8, 50A, PQFN31, 5X5	U7210, U7220	CRITICAL	
152S00241	1	IND, MLD, 0.47UH, 4.94MO, 20A, 5, 4X5, 2X2, 4MM	L7270	CRITICAL	

DRWING NUMBER: 051-00515
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 BRANCH: dvt-fab09-0
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BOM_COST_GROUP=CPU & CHIPSET

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SYNC_MASTER=J79_SILUCHEN		SYNC_DATE=04/02/2015	
PAGE TITLE			
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	REVISION	9.0.0	
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	PAGE	73 OF 145	
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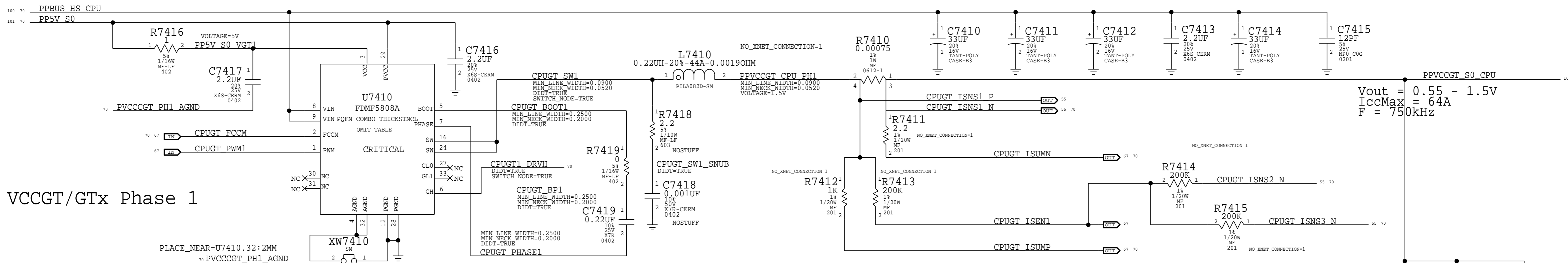
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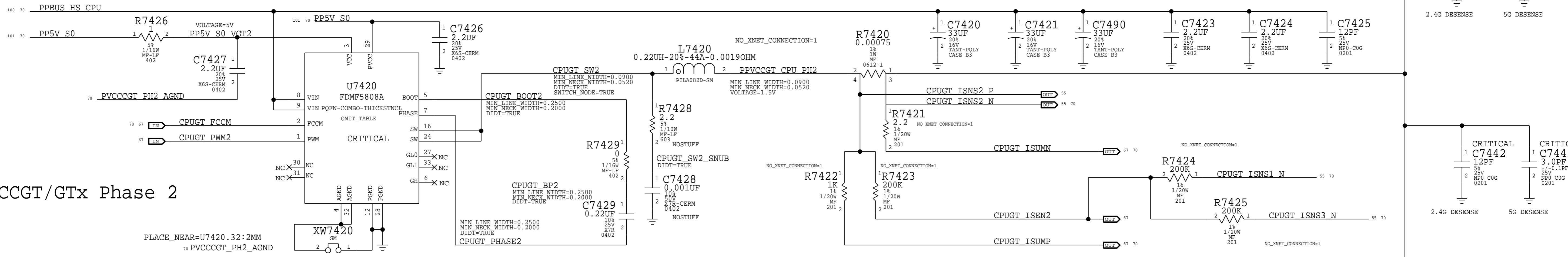
CPU VCCGT/GTx Phase 1



PLACE_NEAR=U7410.32:2MM
PPVCCGT_PH1_AGND

Vout = 0.55 - 1.5V
IccMax = 64A
F = 750kHz

CPU VCCGT/GTx Phase 2

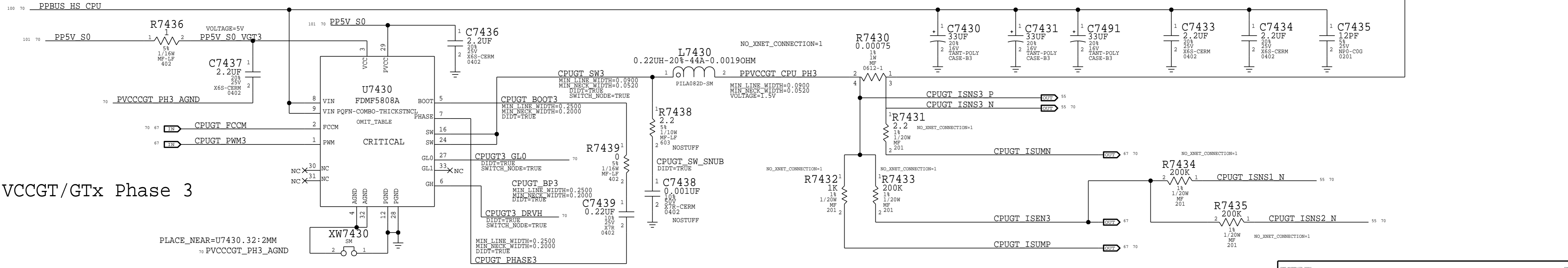


PLACE_NEAR=U7420.32:2MM
PPVCCGT_PH2_AGND

CRITICAL C7440 12PF
CRITICAL C7441 3.0PF
2.4G DESENSE 5G DESENSE

CRITICAL C7442 12PF
CRITICAL C7443 3.0PF
2.4G DESENSE 5G DESENSE

CPU VCCGT/GTx Phase 3



PLACE_NEAR=U7430.32:2MM
PPVCCGT_PH3_AGND

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353500497	3	IC,FDMF5808A,DRMOS,1MWP8,50A,PQFN31,5X5	U7410, U7420, U7430	CRITICAL	

GT & GTX IMVP POWER BLOCK

Apple Inc.

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BRANCH: dvt-fab09-0
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BOM_COST_GROUP=CPU & CHIPSET

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SYNC_MASTER=J79_SILUCHEN		SYNC_DATE=03/27/2015	
PAGE TITLE			
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	SHEET	71 OF 119	

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7

6

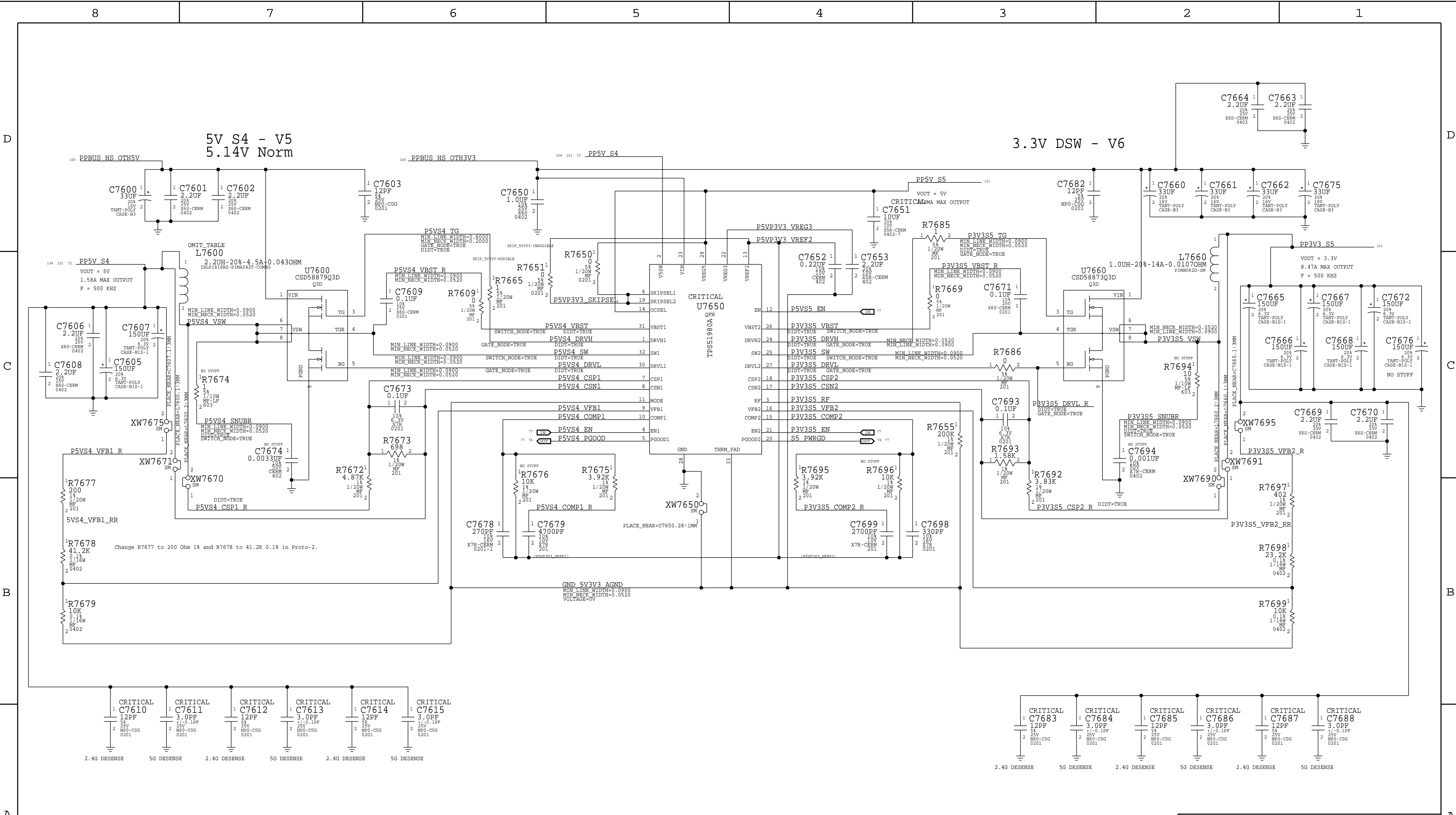
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4

3

2

1

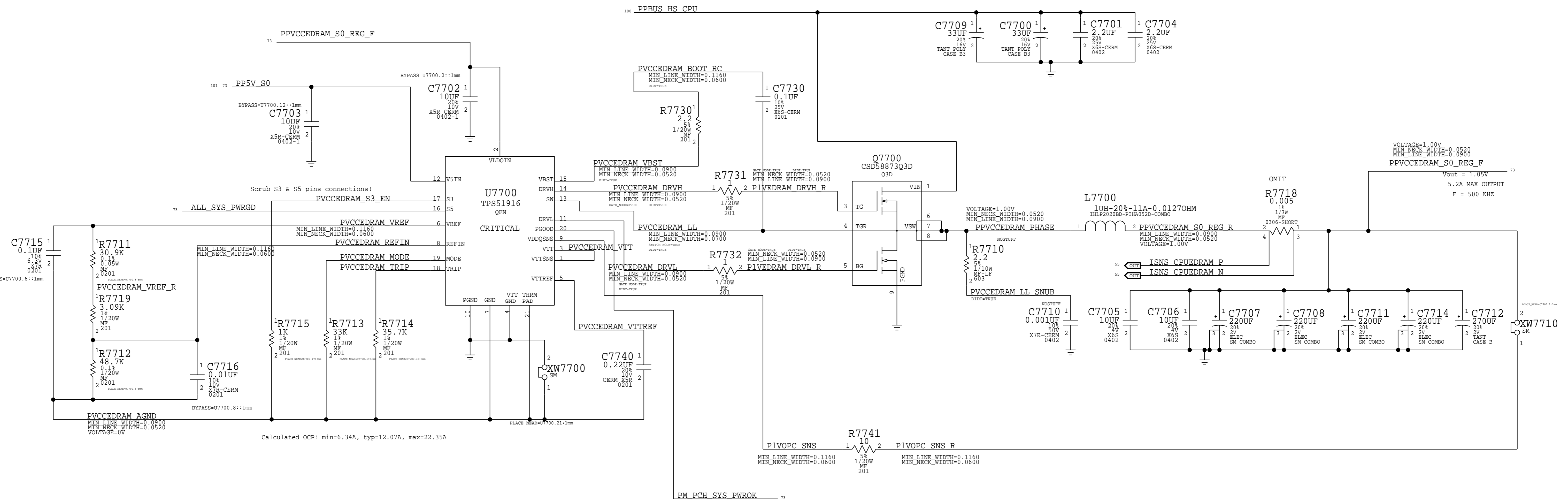


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00182	1	IND, PWR, 2.2UH, 20%, 4.5A, 43MOHM, 4X4MM	L7600	CRITICAL	

PAGE TITLE		
Power - 5V 3.3V Supply		
	BRANCHING NUMBER	051-00515
	REVISION	9.0.0
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	PAGE	76 OF 145
	SHEET	72 OF 119

BOM_COST_GROUP=PLATFORM POWER

1V EDRAM & EOPIO



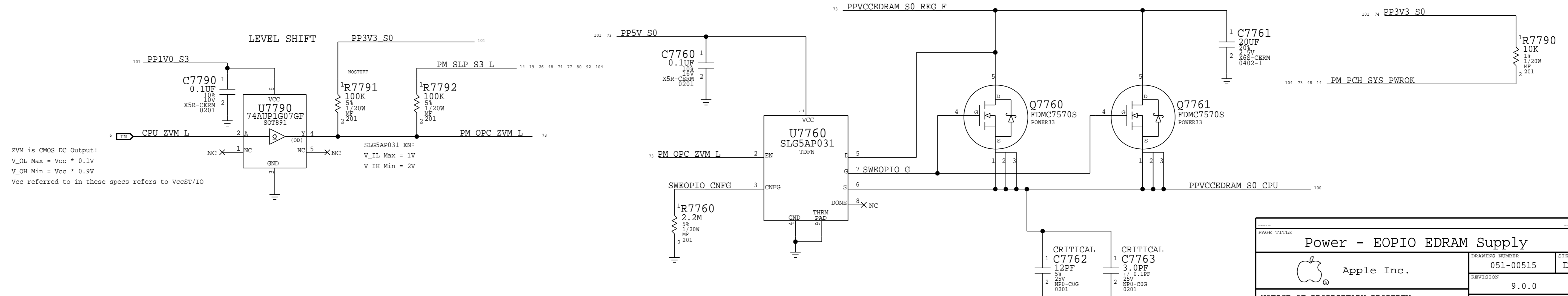
Calculated OCP: min=6.34A, typ=12.07A, max=22.35A

- THE FOLLOWING SHORTCUTS ARE USED:
- OPC (EDRAM) IS POWERED FROM ONE VR.
 - LOAD SWITCHES ARE USED TO MEET THE TURN-ON TIMING.
 - MSM# IS NOT USED.

NC CPU MSM L == NC CPU MSM L
MAKE_BASE=TRUE

PM_PCH_SYS_PWROK == PM_PCH_SYS_PWROK
MAKE_BASE=TRUE

ALL_SYS_PWRGD == ALL_SYS_PWRGD
MAKE_BASE=TRUE



ZVM is CMOS DC Output:
V_{OL} Max = V_{cc} * 0.1V
V_{OH} Min = V_{cc} * 0.9V
V_{cc} referred to in these specs refers to V_{cc}ST/IO

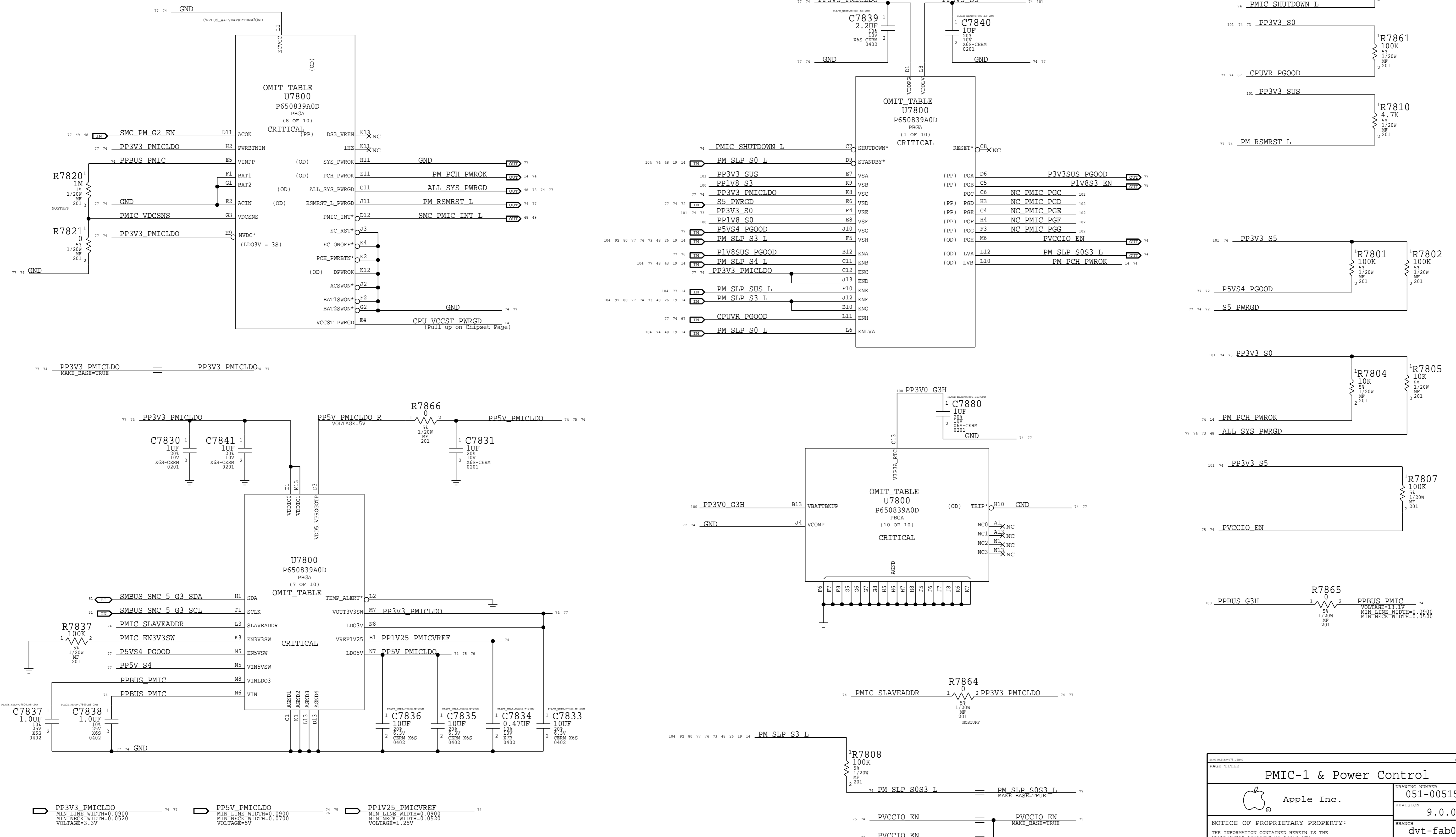
SLG5AP031 EN:
V_{IL} Max = 1V
V_{IH} Min = 2V

CRITICAL C7762 12PF 25V NPO-COG 0201
CRITICAL C7763 3.0PF 1+-0.1PF 25V NPO-COG 0201
2.4G DESENSE 5G DESENSE

PAGE TITLE Power - EOPIO EDRAM Supply		
	DRAWING NUMBER 051-00515	STEP D
	REVISION 9.0.0	
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BRANCH dvt-fab09-0	PAGE 77 OF 145	SHEET 73 OF 119

BOM_COST_GROUP=CPU & CHIPSET

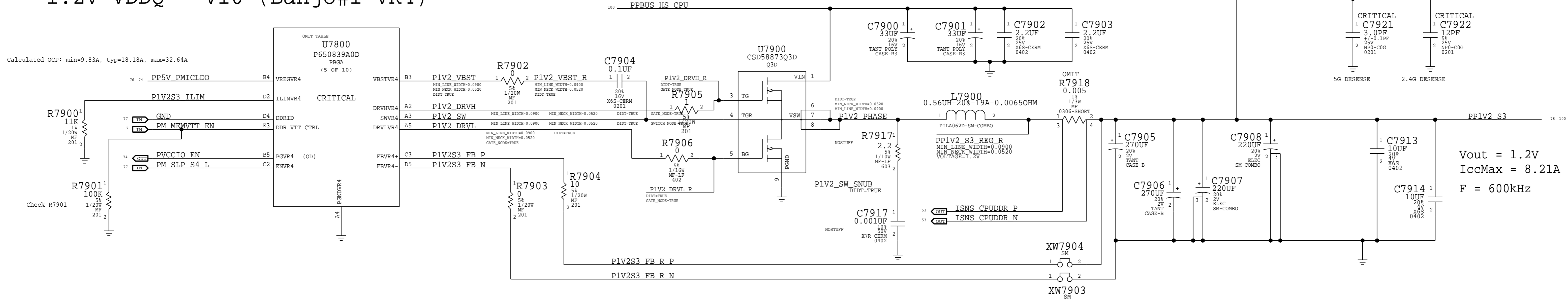
BANJO - PMIC Control



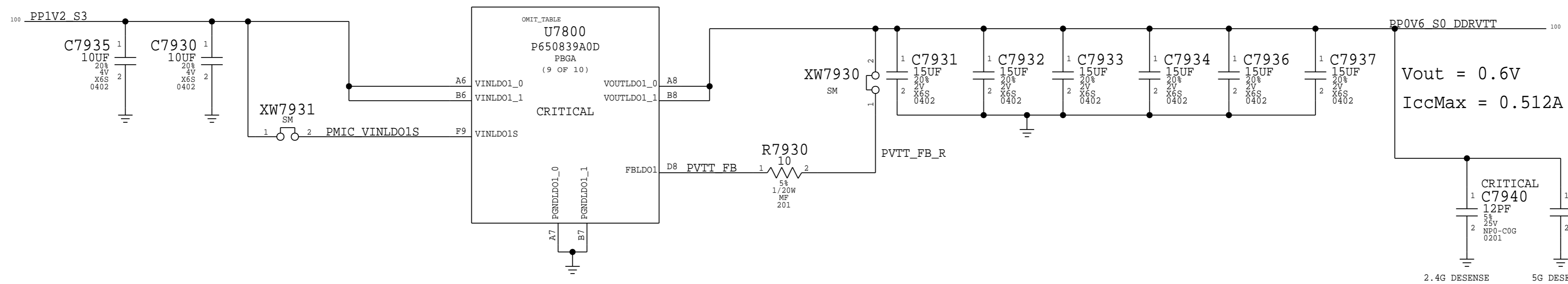
PAGE TITLE		DRAWING NUMBER		STEP
PMIC-1 & Power Control		051-00515		D
Apple Inc.		REVISION		9.0.0
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I I I I ALL RIGHTS RESERVED				

BOM_COST_GROUP=PLATFORM POWER

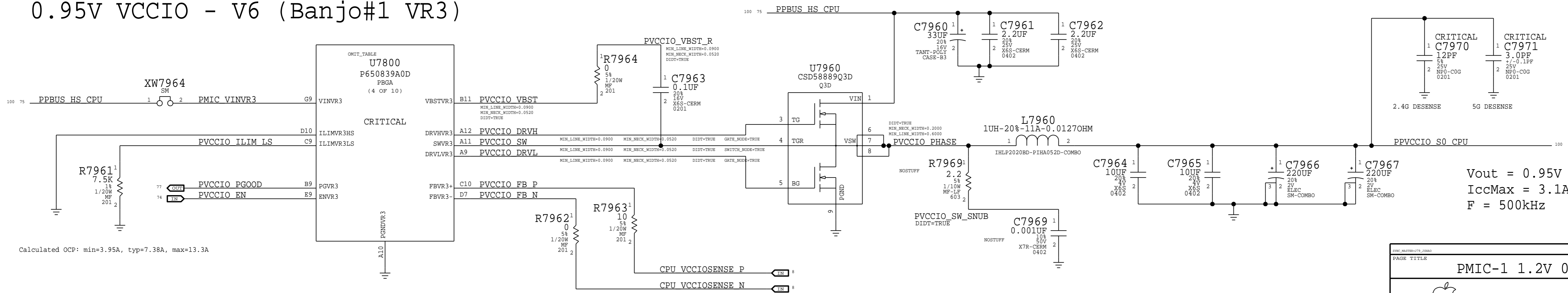
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LD01)

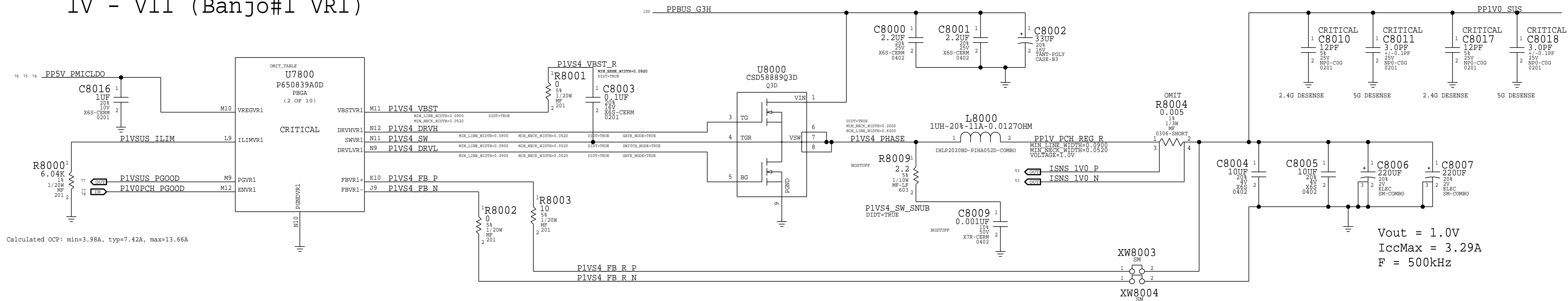


0.95V VCCIO - V6 (Banjo#1 VR3)

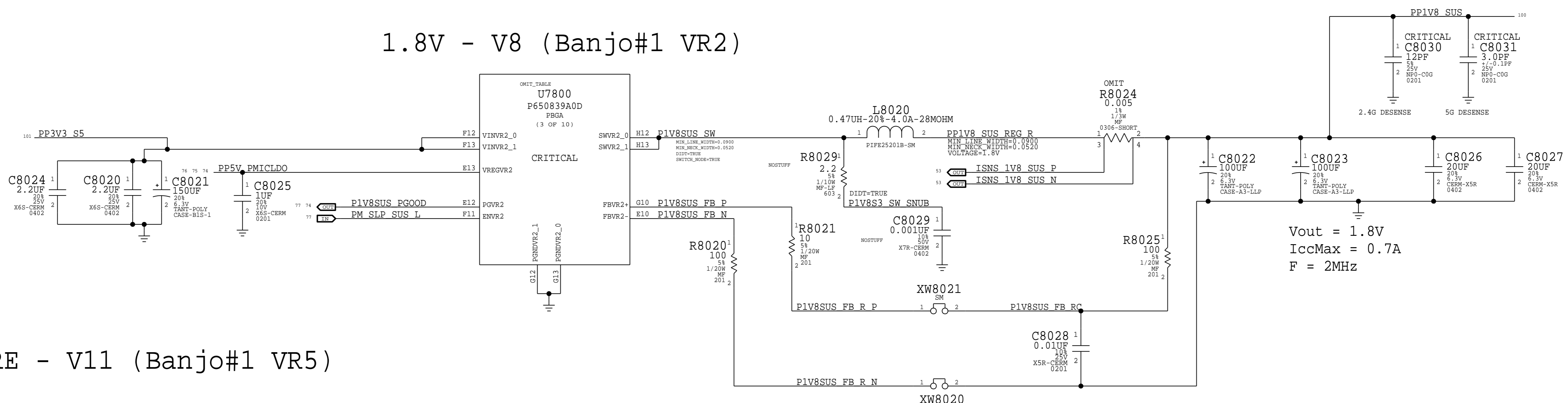


TITLE: PMIC-1 1.2V 0.6V VCCIO DRAWING NUMBER: 051-00515 REVISION: 9.0.0 BRANCH: dvt-fab09-0 PAGE: 79 OF 145 SHEET: 75 OF 119			STEP: D
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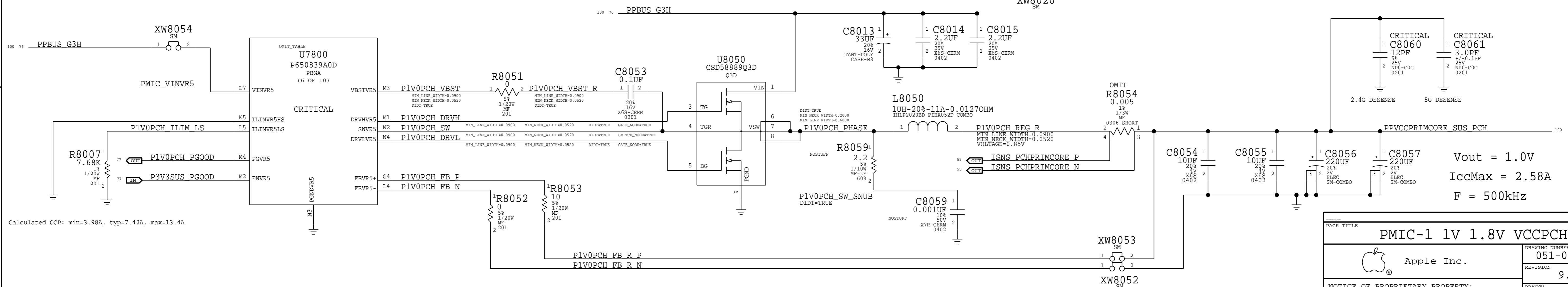
1V - V11 (Banjo#1 VR1)



1.8V - V8 (Banjo#1 VR2)

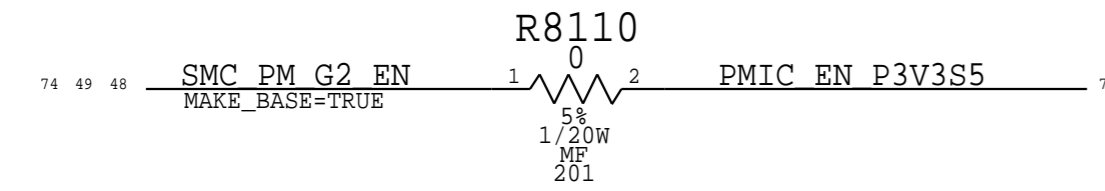


1.0V PCH CORE - V11 (Banjo#1 VR5)
0.7V LPM

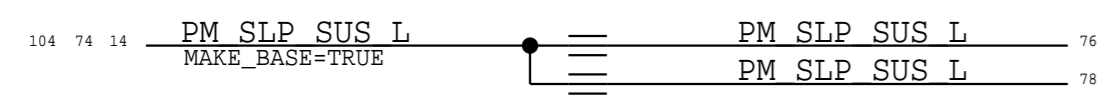


PAGE TITLE		DRAWING NUMBER		STEP
PMIC-1 1V 1.8V VCCPCH		051-00515		D
Apple Inc.		REVISION		9.0.0
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114 ALL RIGHTS RESERVED				

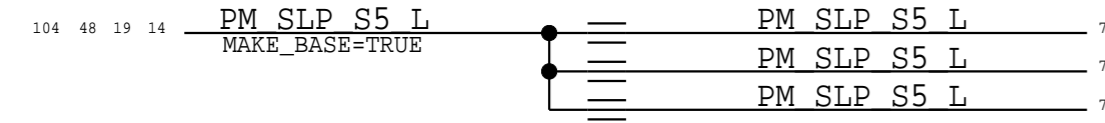
S5 Enables



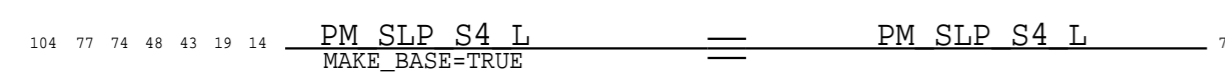
SUS Enables



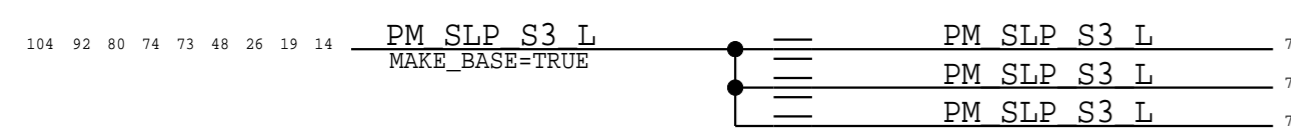
S4 Enables



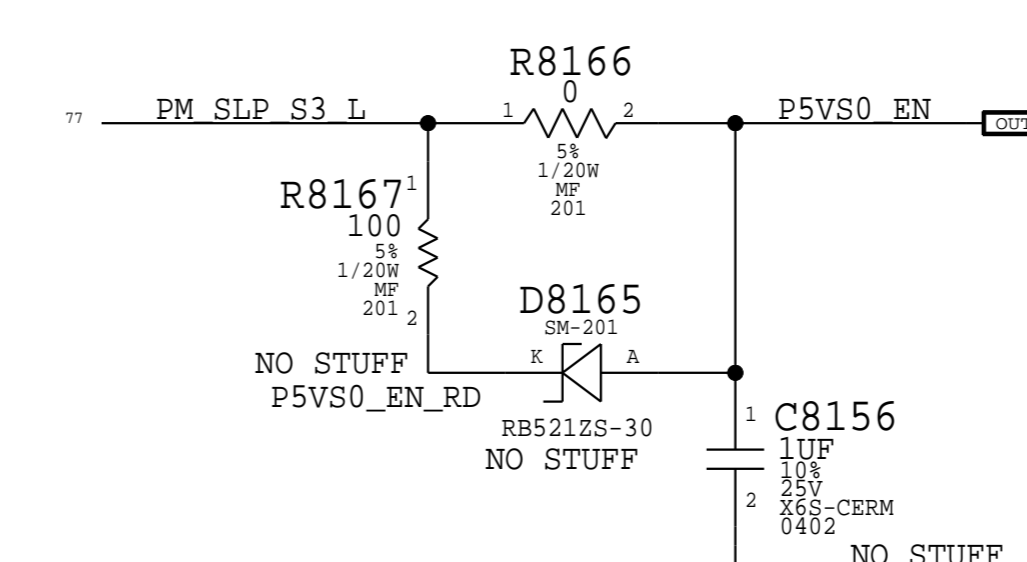
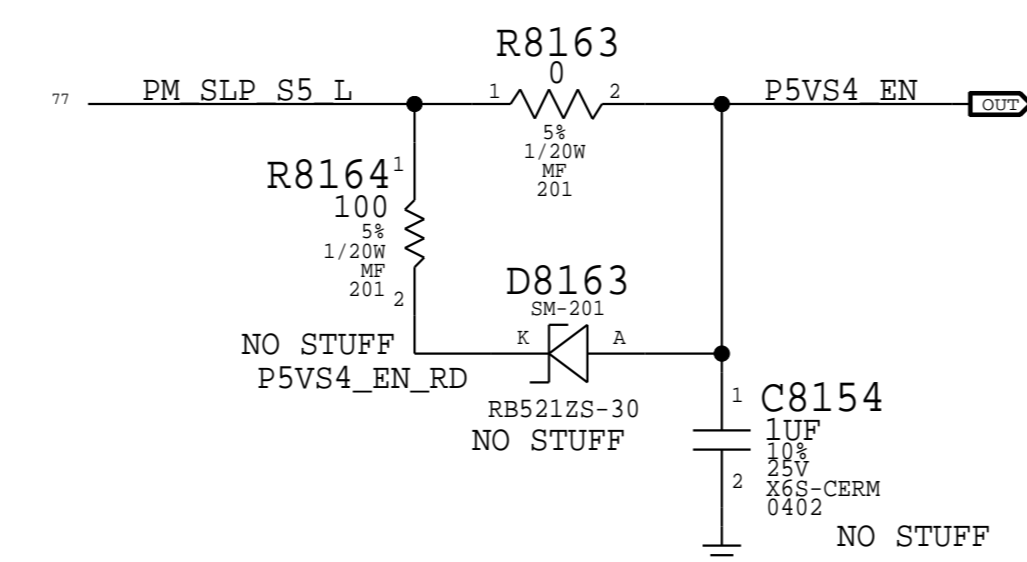
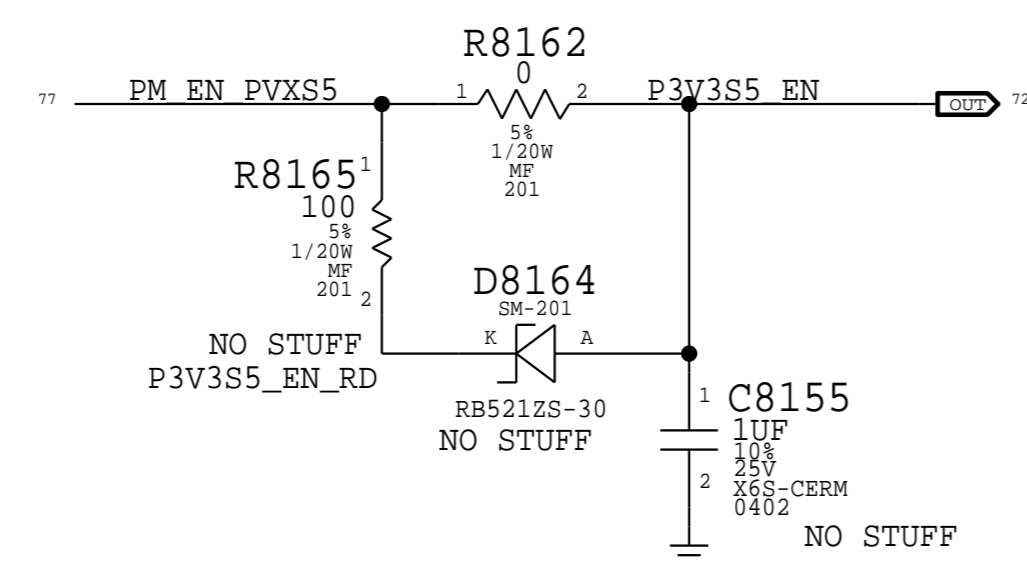
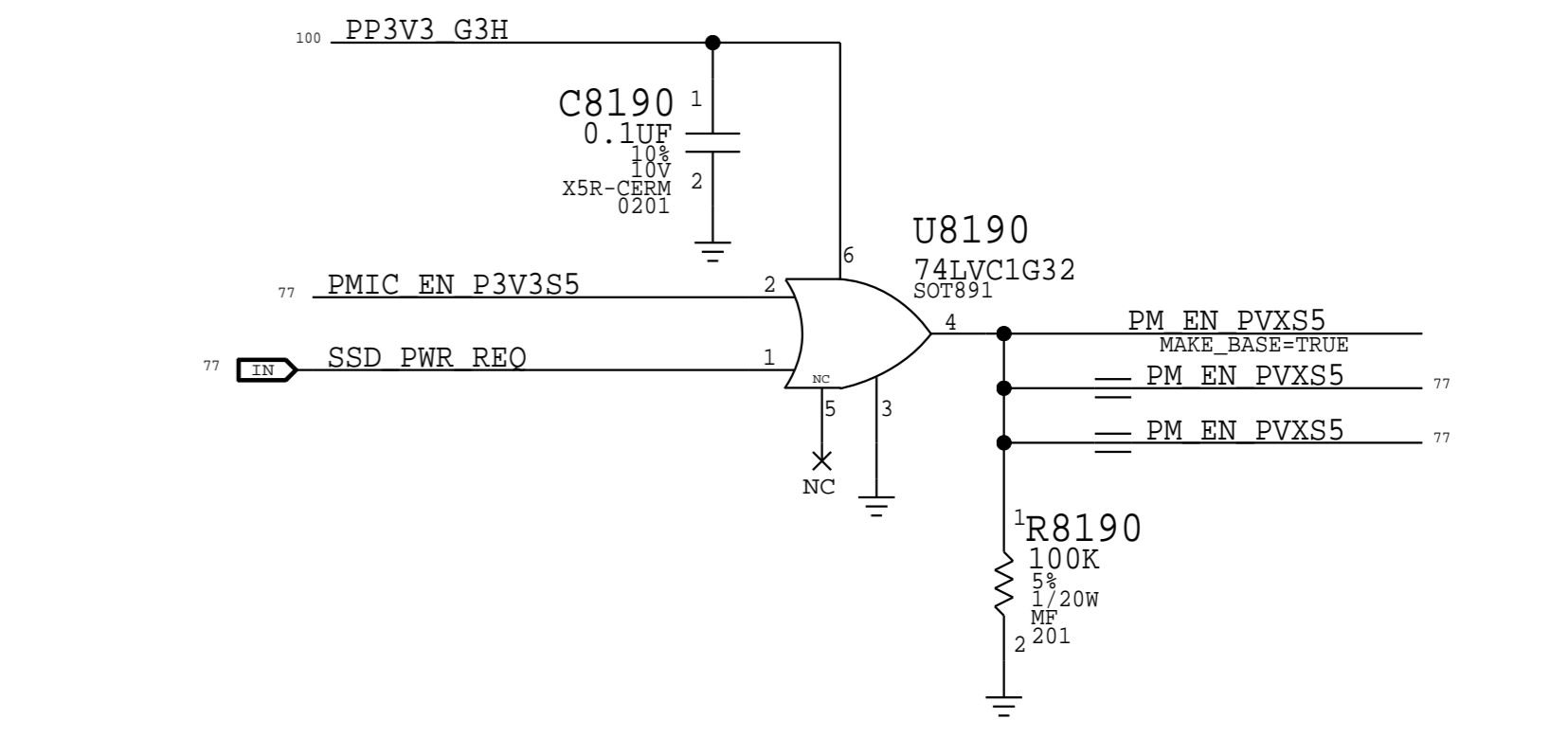
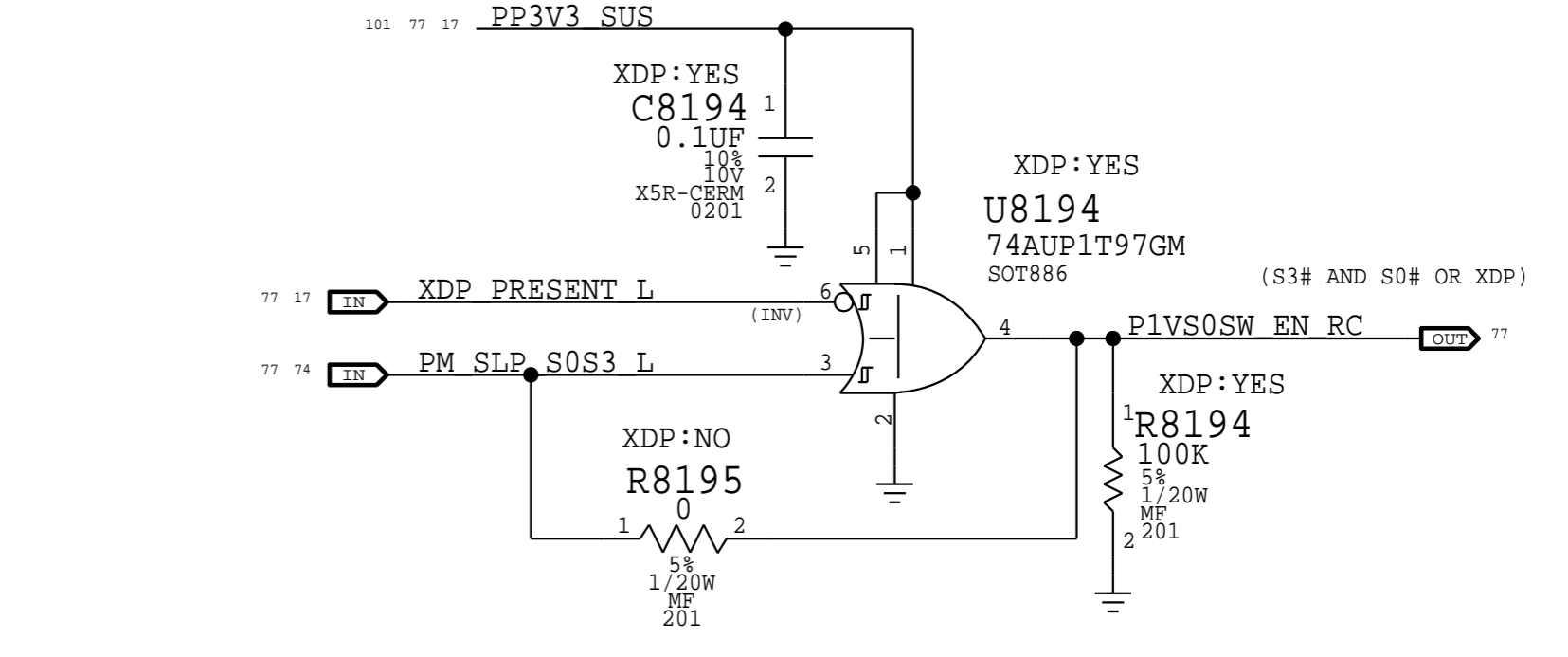
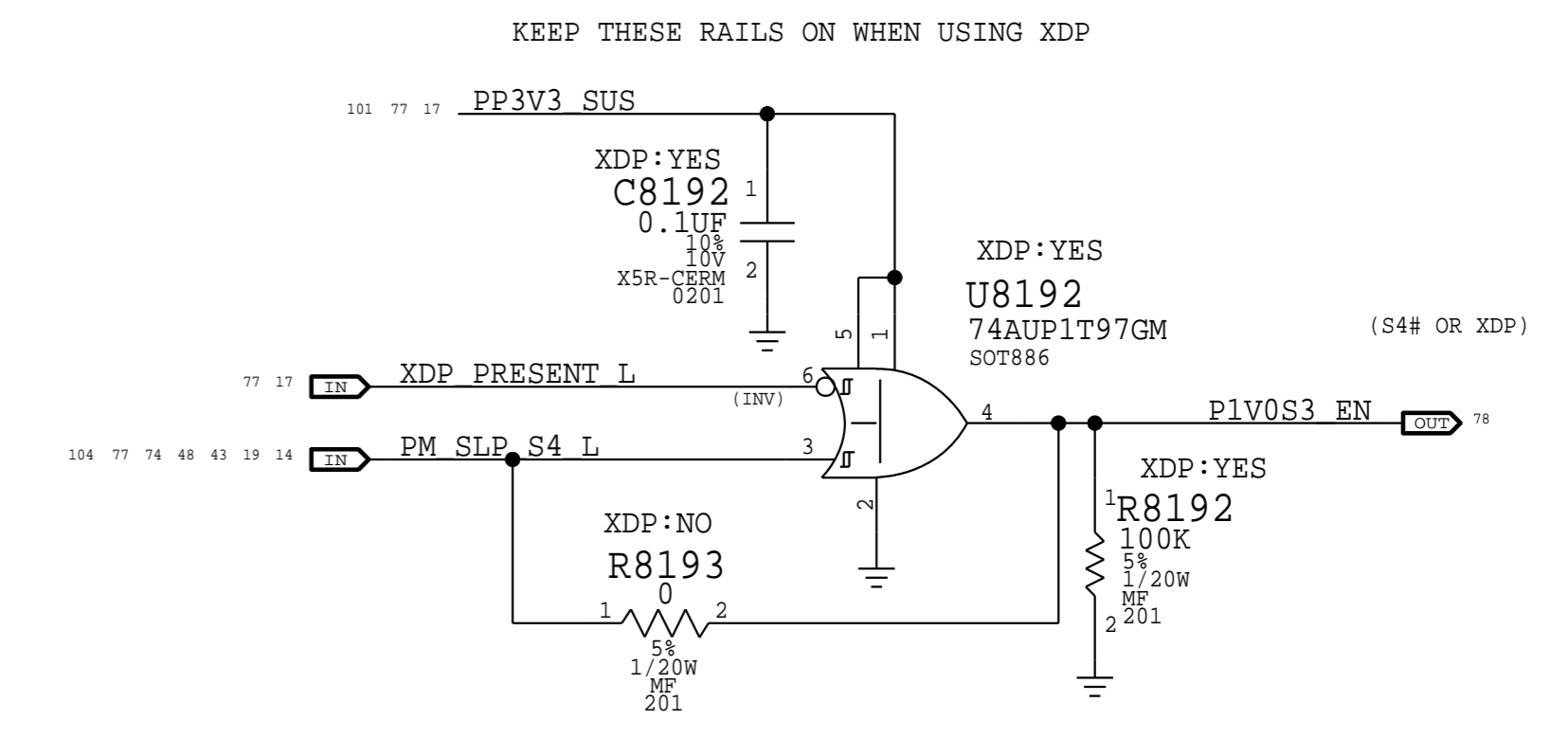
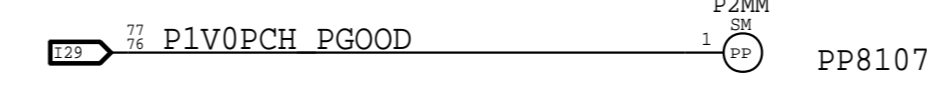
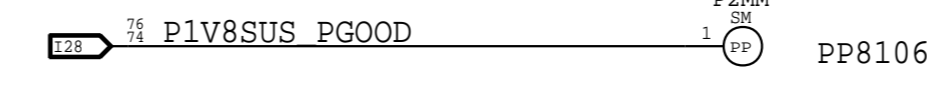
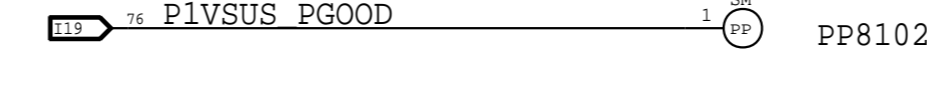
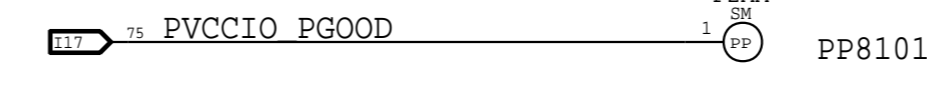
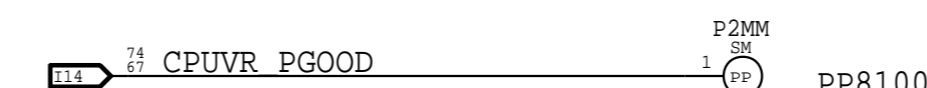
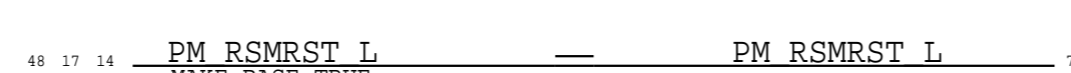
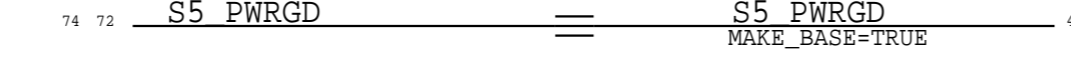
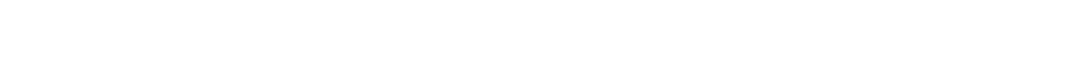
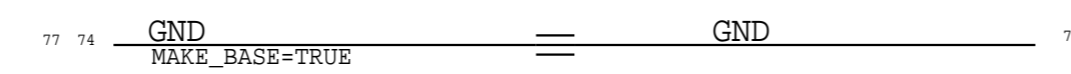
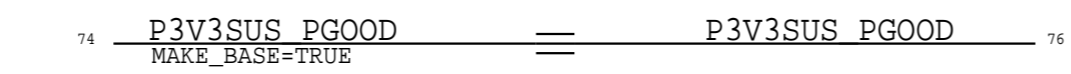
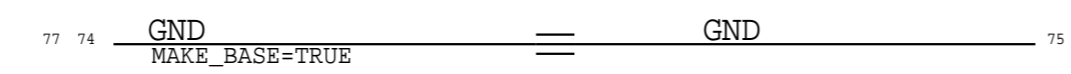
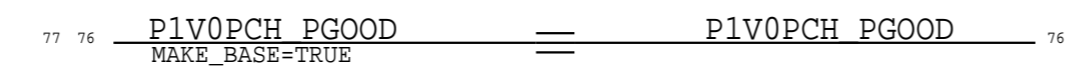
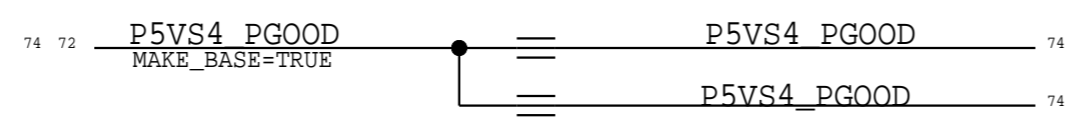
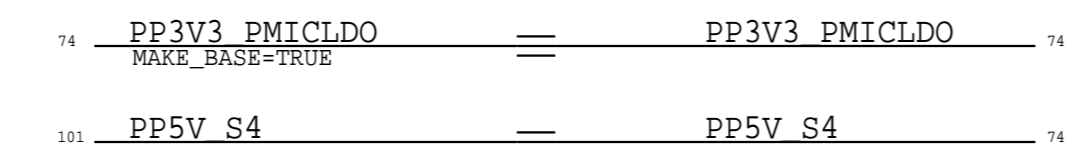
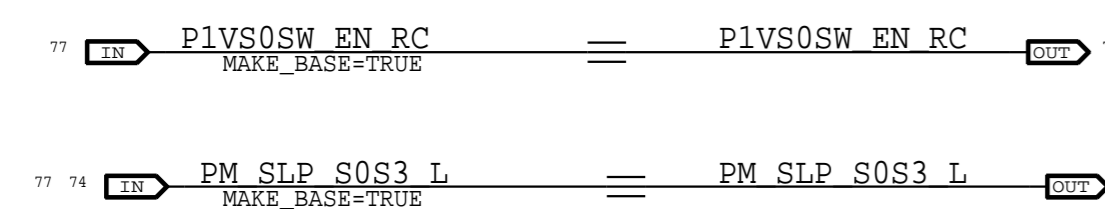
S3 Enables



S0 Enables

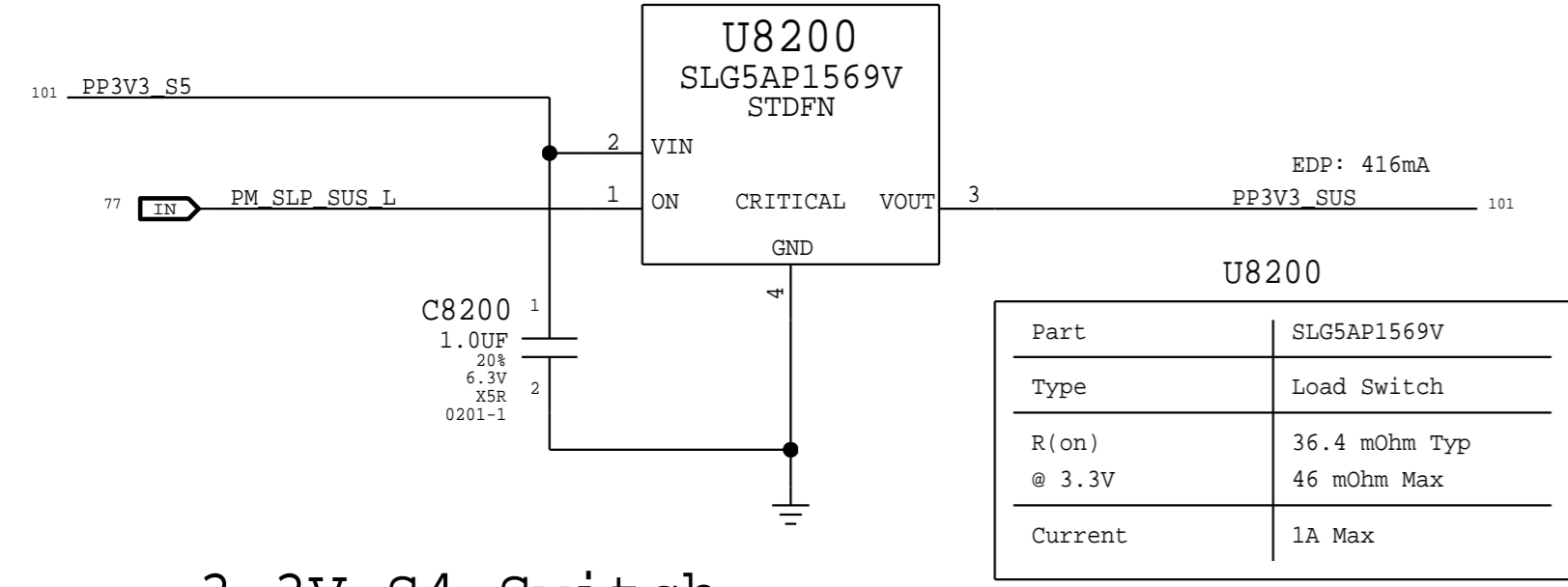


S0i Enables



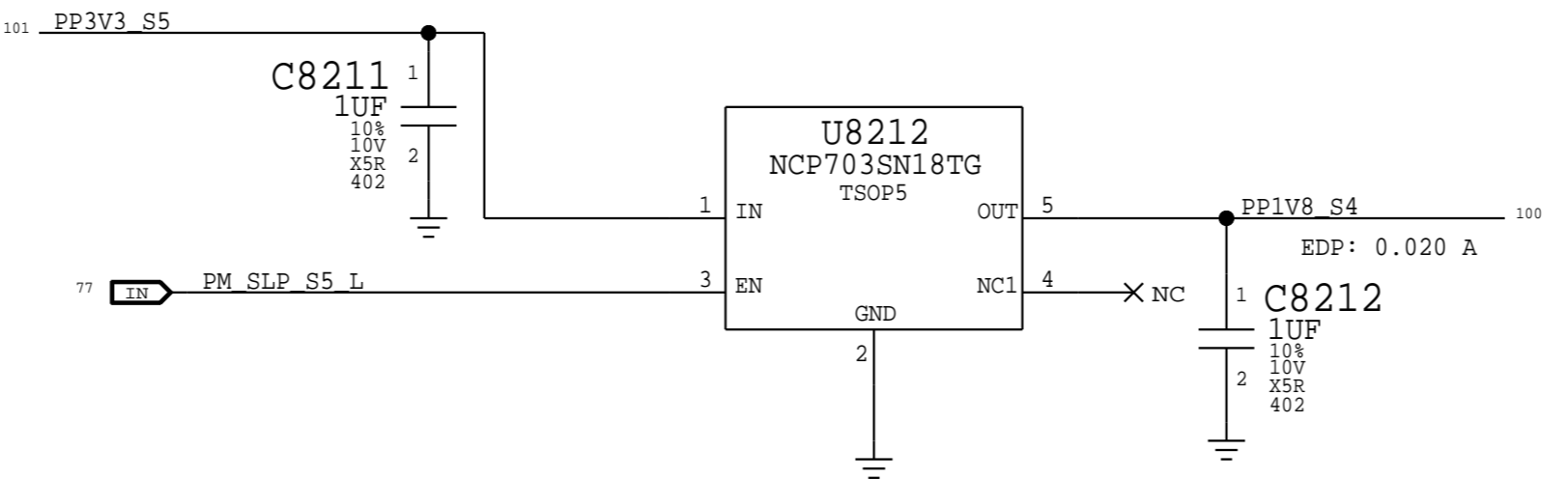
PAGE TITLE PMIC-1 Aliases & TPS		
Apple Inc.	DRAWING NUMBER 051-00515	STEP D
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	PAGE 81 OF 145	
	SHEET 77 OF 119	

3.3V SUS Switch



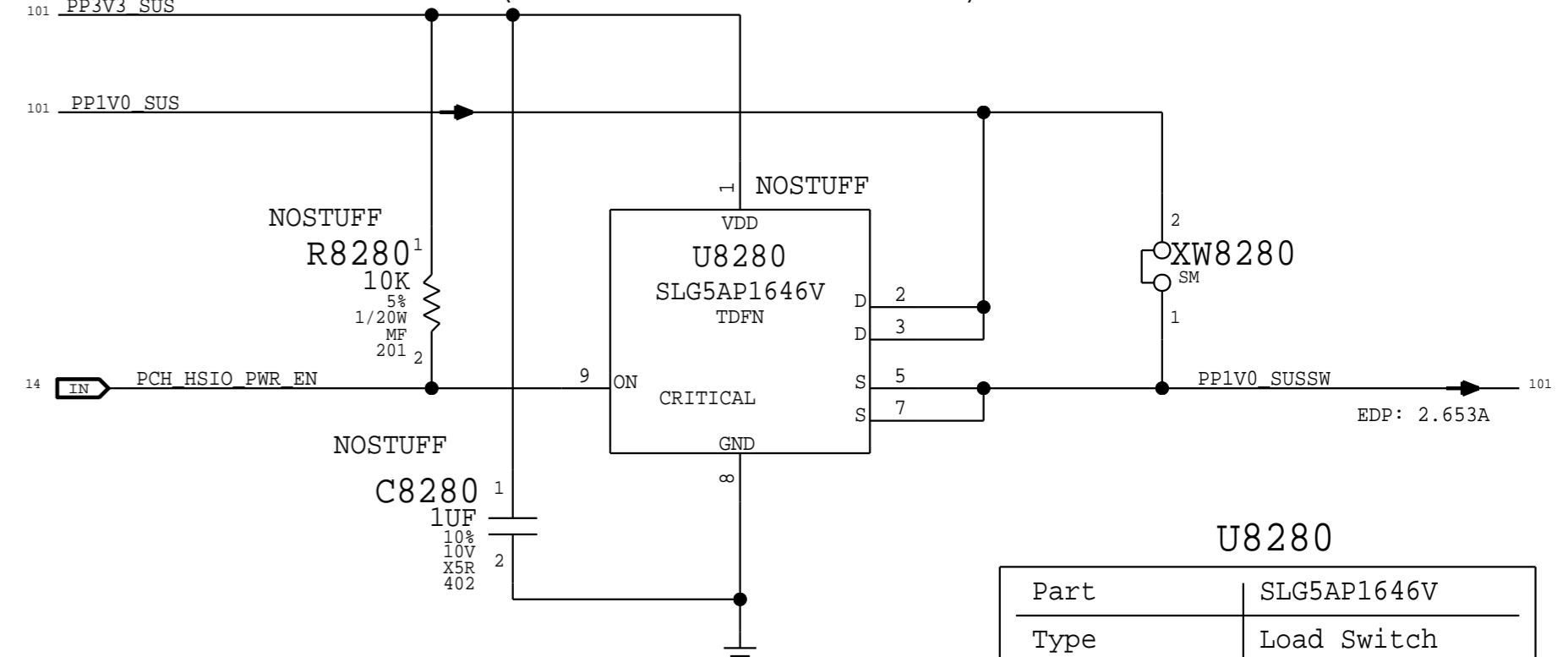
Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.3V	36.4 mOhm Typ 46 mOhm Max
Current	1A Max

1.8V S4 LDO



Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

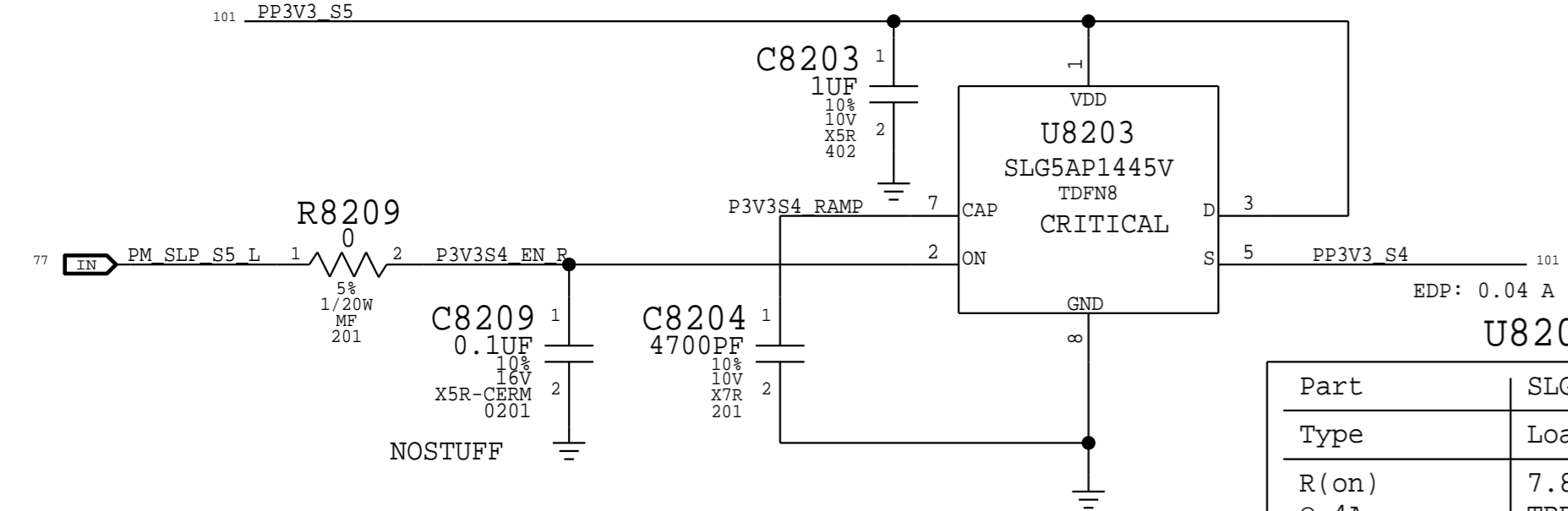
1.0V SUS SW Switch
(CURRENTLY DE-FEATURED)



Part	SLG5AP1646V
Type	Load Switch
R(on) @ 4V Vgs	8.5 mOhm Typ 9.8 mOhm Max
Current	6A Max

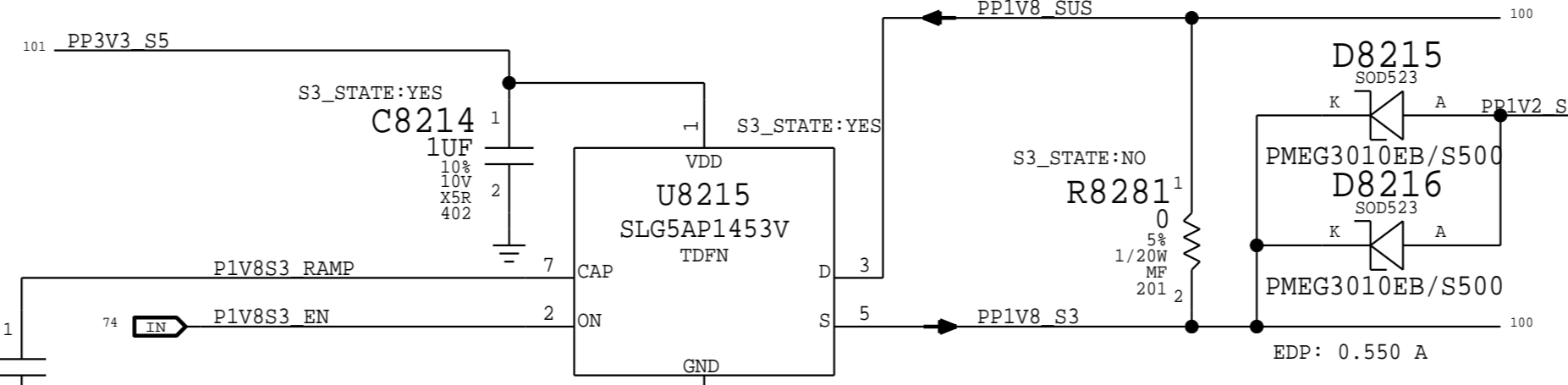
HSIO has turn-on requirement of <0.1V/uS ramp rate and <65uS from EN to 95% (1.05V)

3.3V S4 Switch



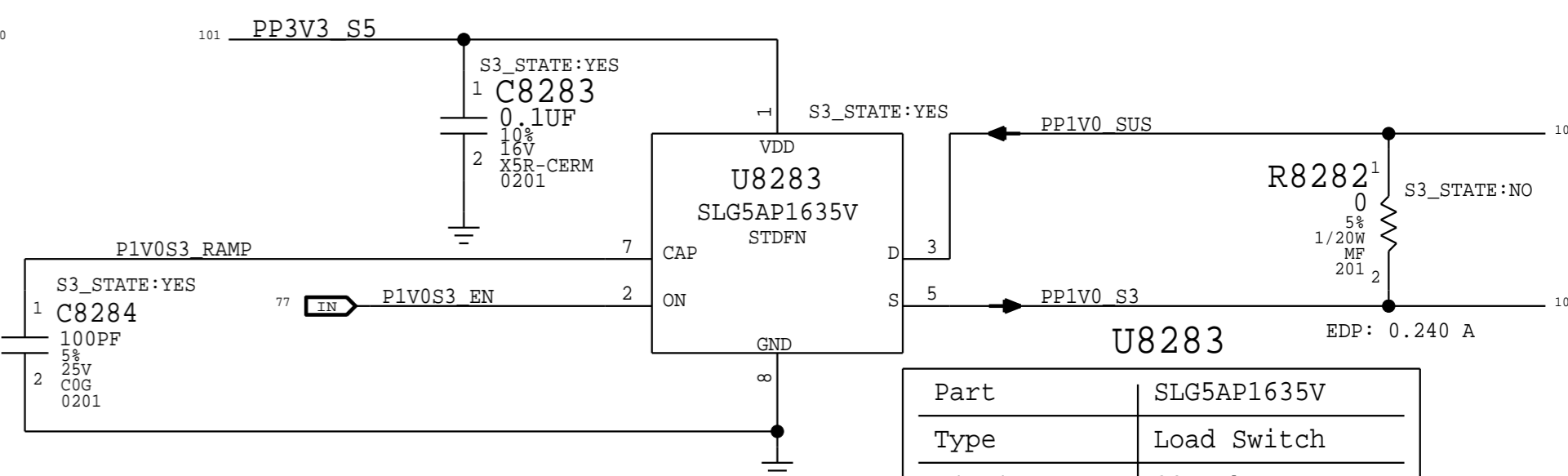
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

1.8V S3 Switch



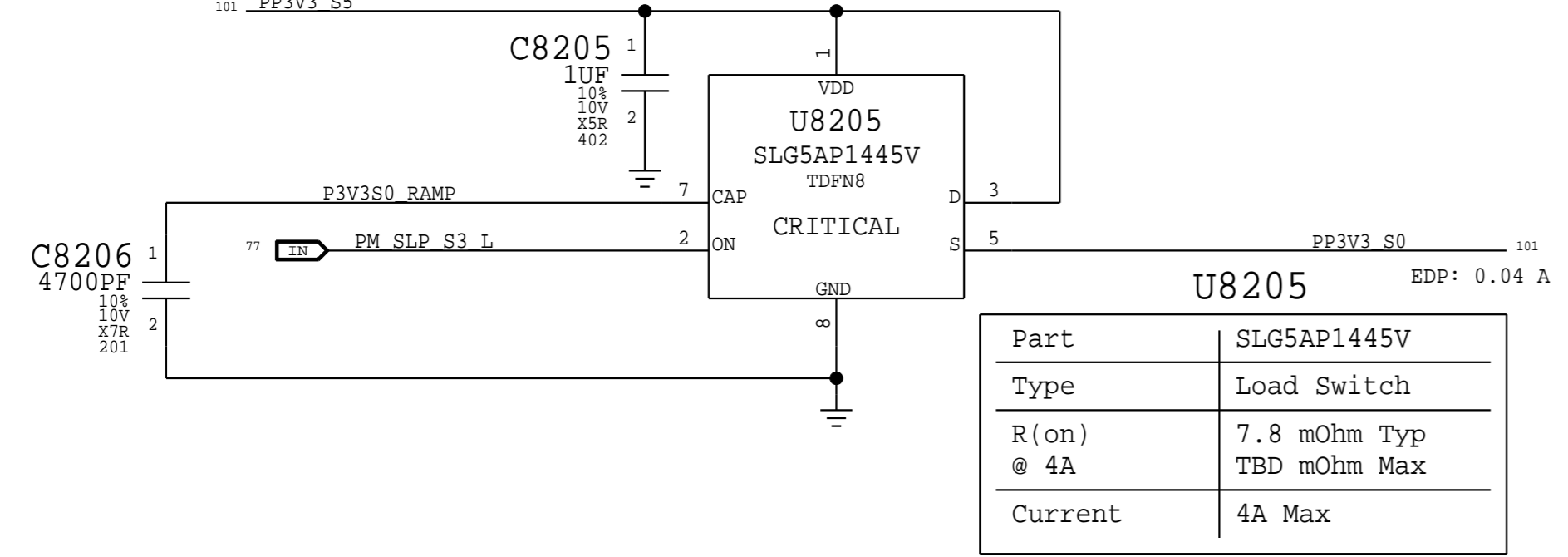
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.0V S3 Switch



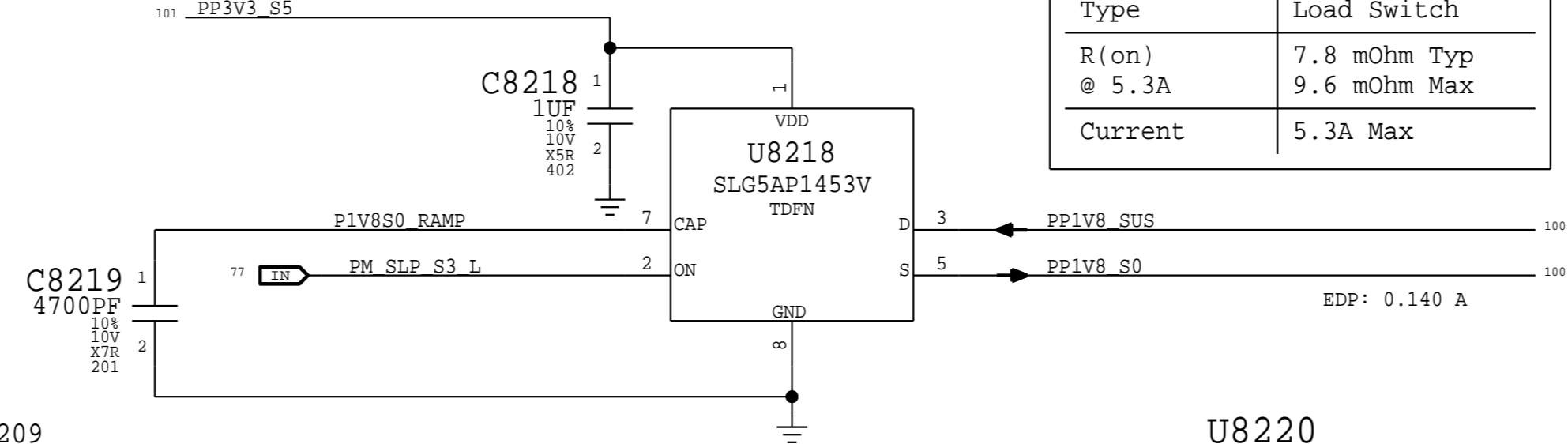
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

3.3V S0 Switch



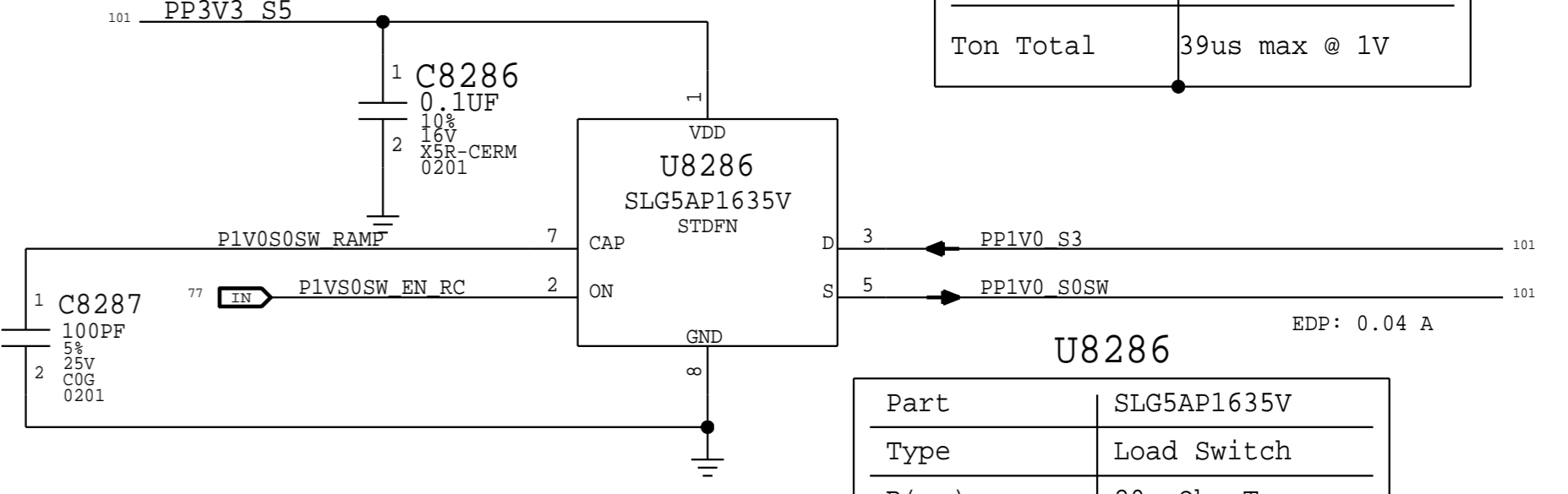
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

1.8V S0 Switch



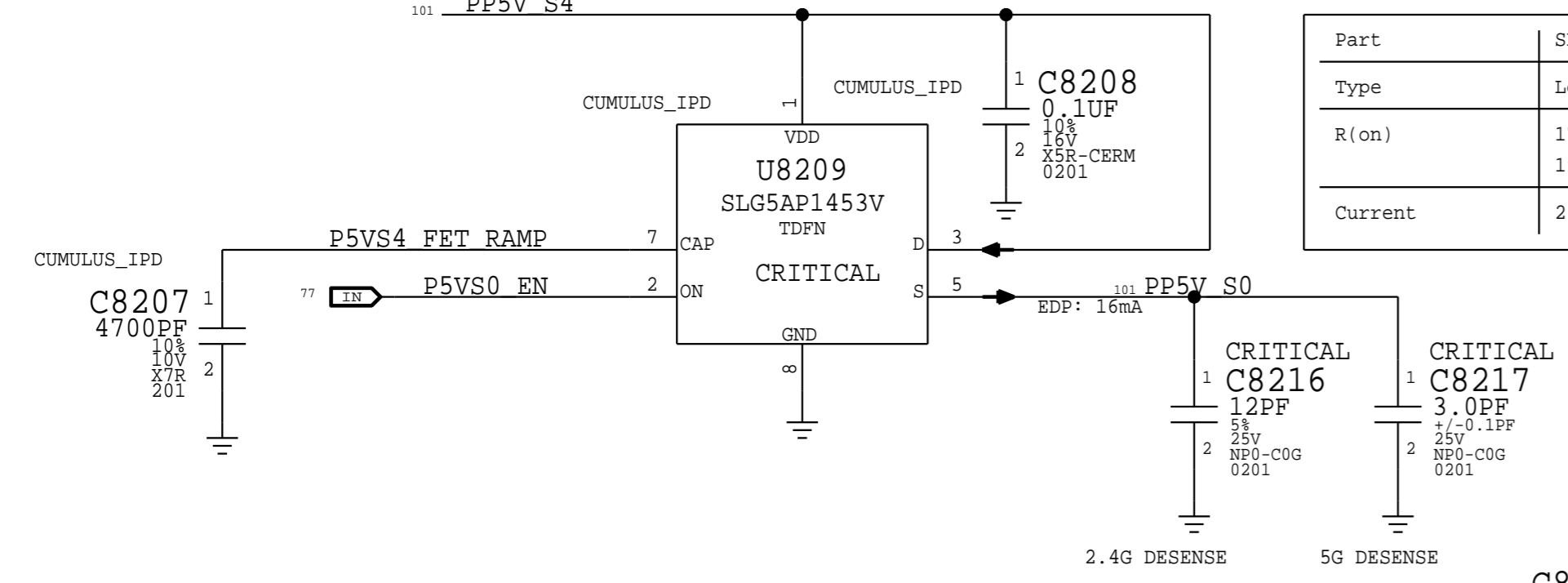
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.0V S0 SW Switch



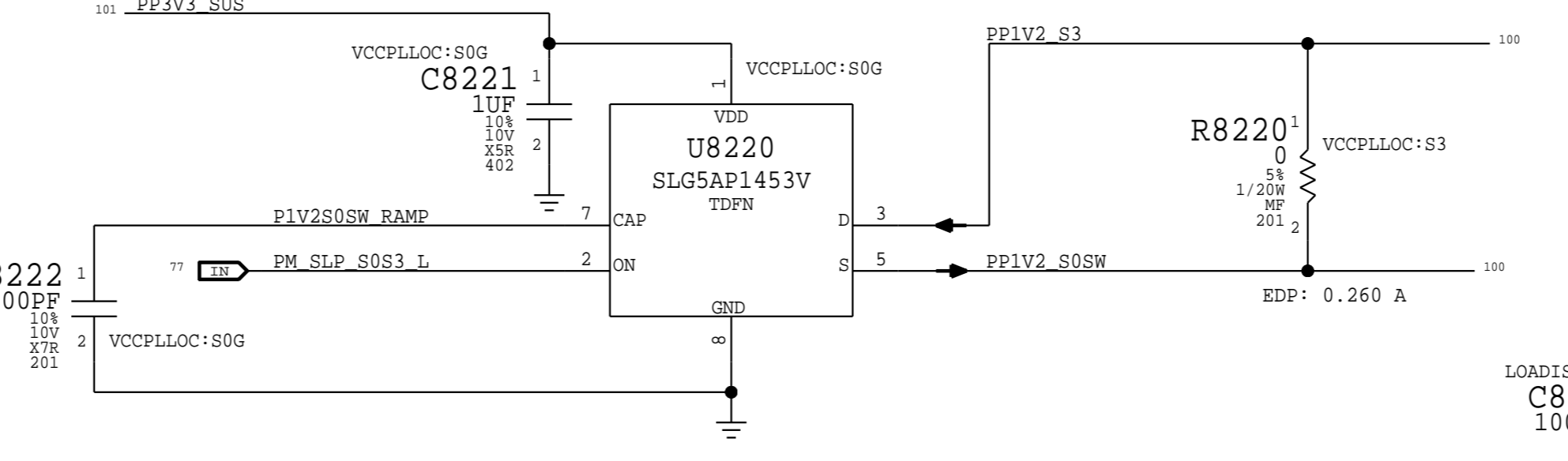
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

5V S0 Switch (Cumulus vs Kona)



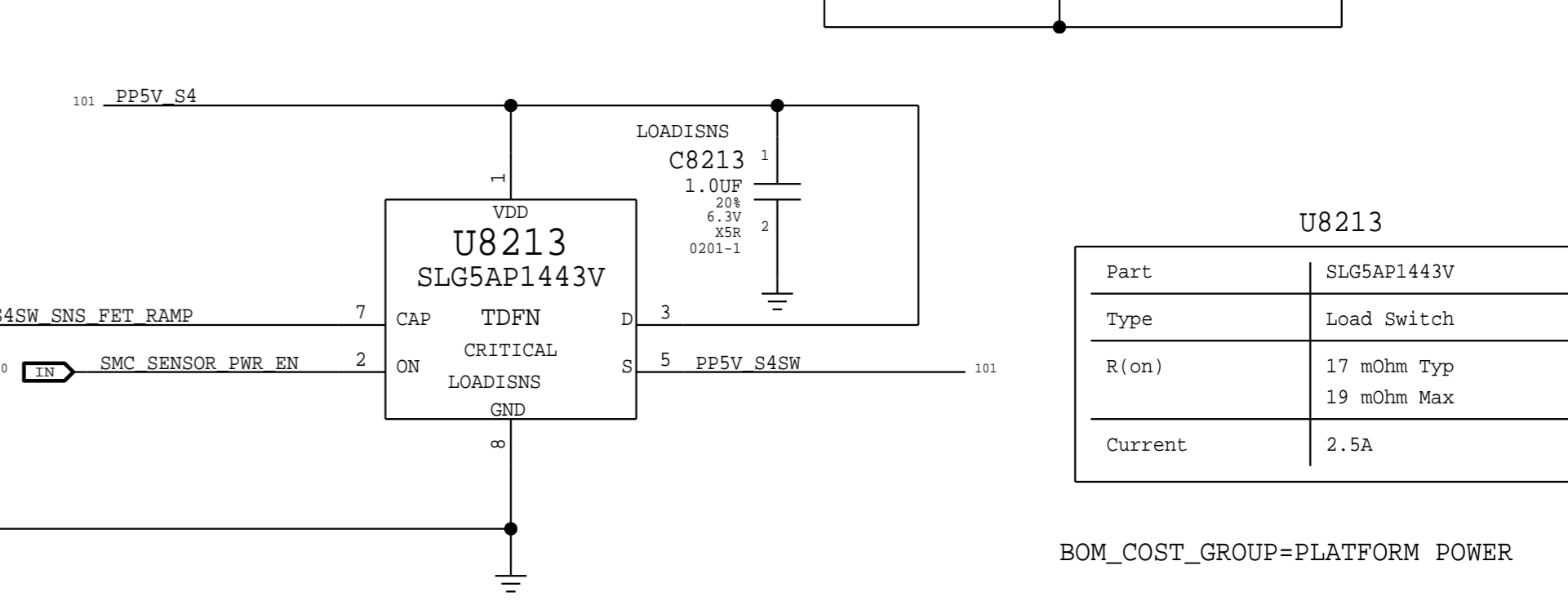
Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

1.2V S0 SW Switch



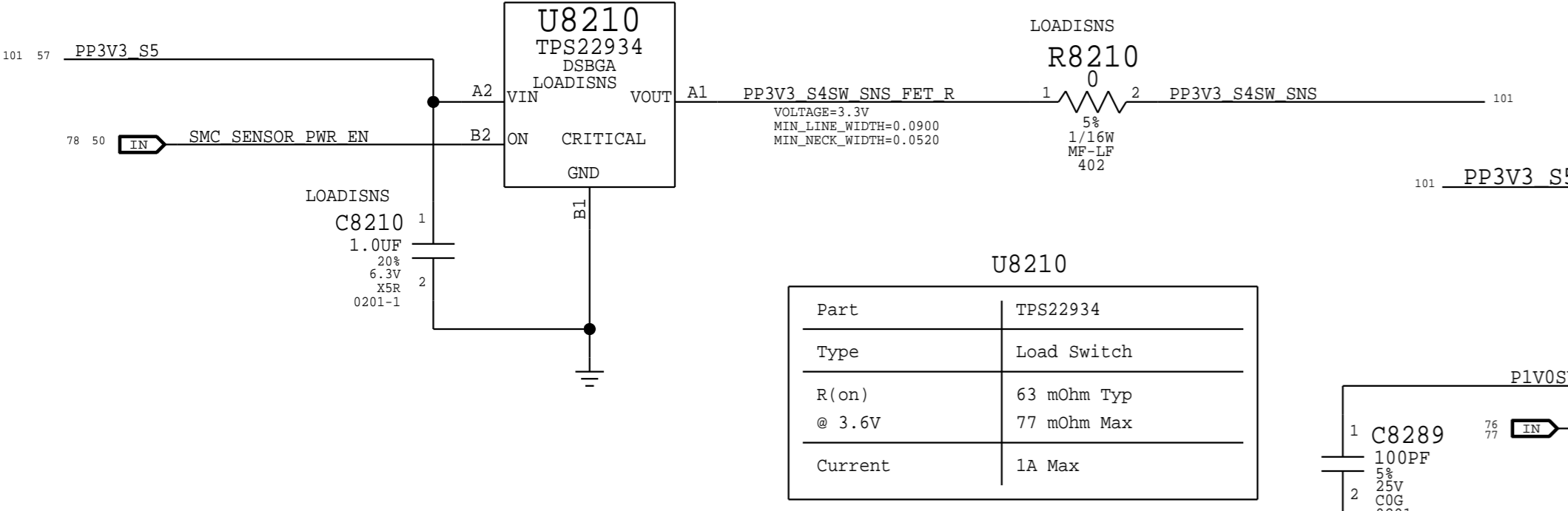
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

5V Sensor Switch



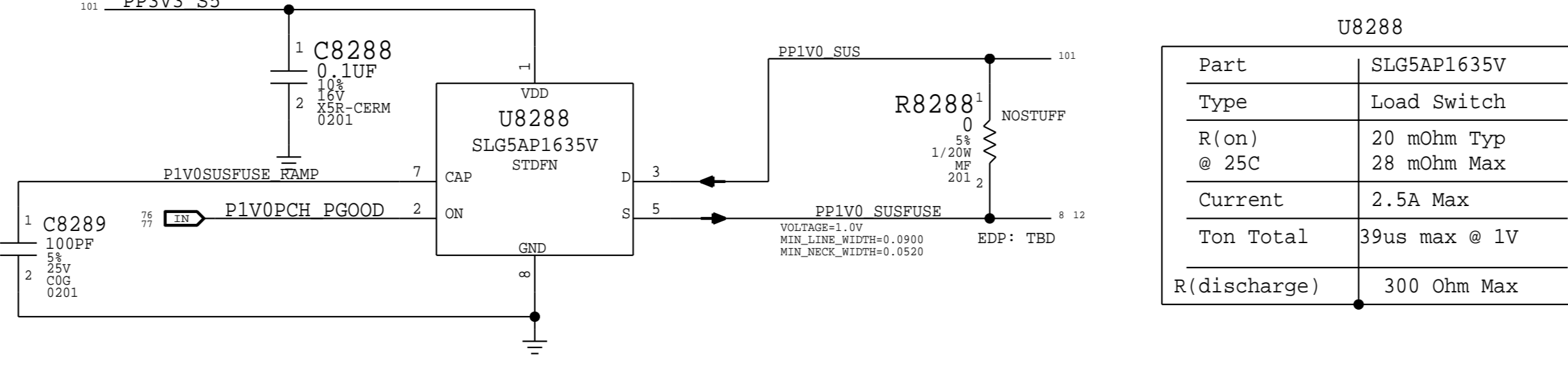
Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

3.3V Sensor Switch



Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

1.0V SUS FUSE Switch



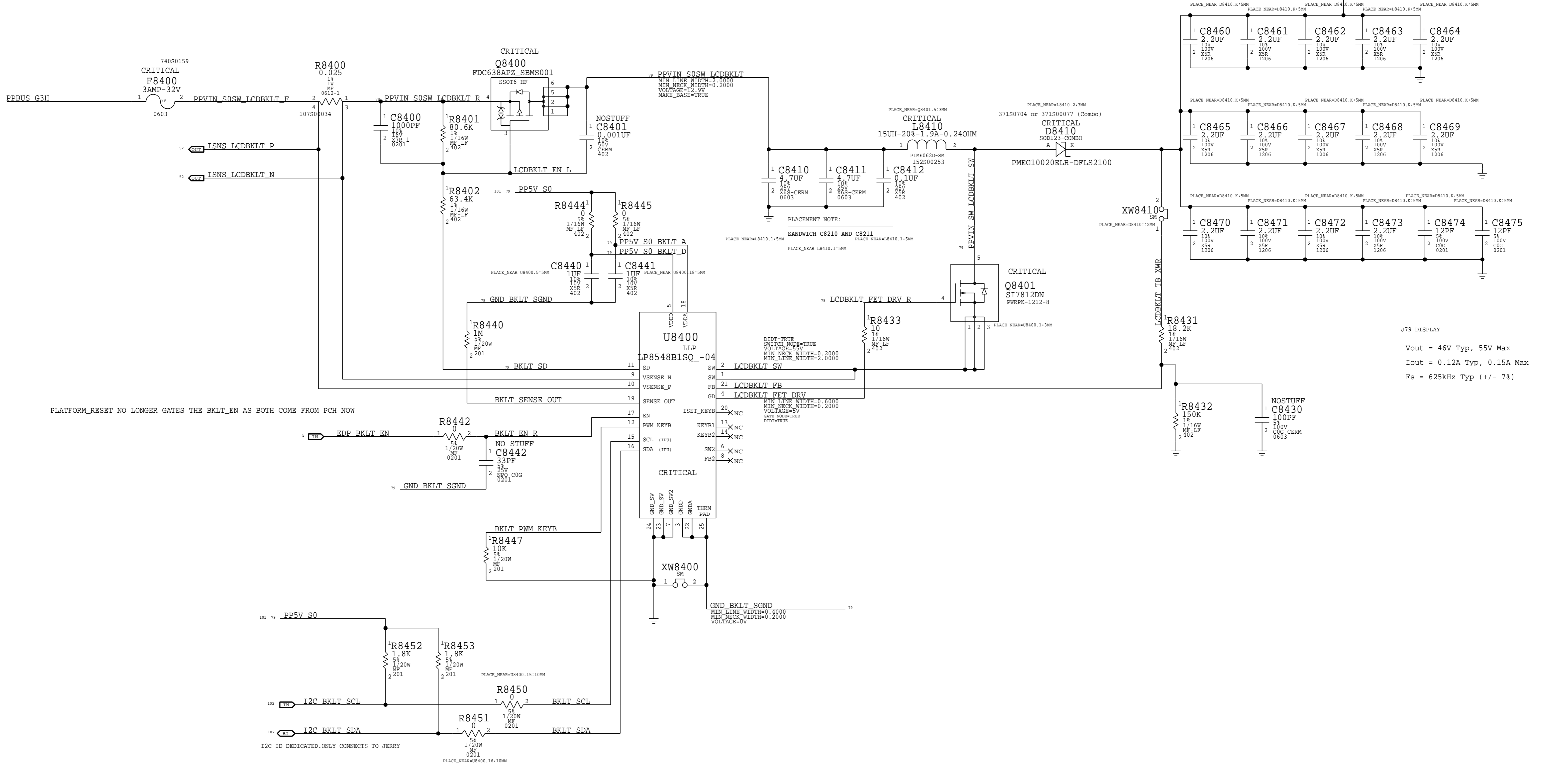
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V
R(discharge)	300 Ohm Max

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE		Power FETs	
Apple Inc.		DRAWING NUMBER	051-00515
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Page Notes

Power aliases required by this page:
 - PPVIN_S0SW_LCDBKLT_FET (9-12.6V LCD BACKLIGHT INPUT)
 - PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

J79 DISPLAY
 Vout = 46V Typ, 55V Max
 Iout = 0.12A Typ, 0.15A Max
 Fs = 625kHz Typ (+/- 7%)

LINE WIDTHS

- PP5V_S0_BKLT_A: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- PP5V_S0_BKLT_D: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- BKLT_SD: MIN_LINE_WIDTH=0.2500, MIN_NECK_WIDTH=0.2000

PBUS LINE WIDTHS

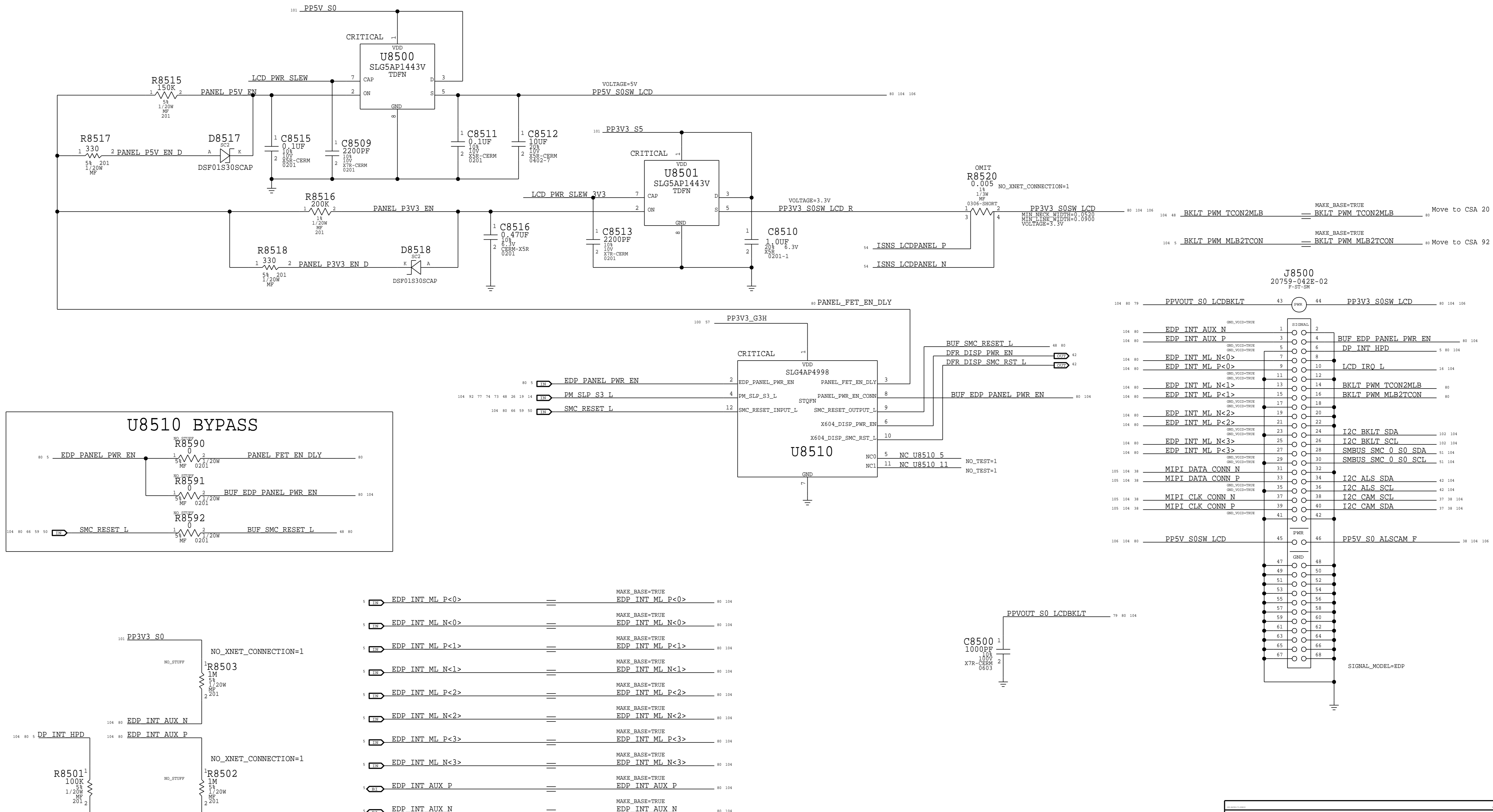
- PPVIN_S0SW_LCDBKLT_F: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_R: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

- LCDBKLT_FET_DRV_R: MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- PPVIN_SW_LCDBKLT_SW: MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- PPVOUT_S0_LCDBKLT: MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1500, VOLTAGE=5V

DRAWING NUMBER: 051-00515 REVISION: 9.0.0 BRANCH: dvt-fab09-0 PAGE: 84 OF 145 SHEET: 79 OF 119			STR: D
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LCD PANEL INTERFACE (eDP) + Camera (MIPI)



PAGE TITLE		
eDP Display Connector		
	DRAWING NUMBER	051-00515
	REVISION	9.0.0
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	PAGE	85 OF 145
	SHEET	80 OF 119

BOM_COST_GROUP=DISPLAY

NAND LANDINGS

CONFIG	LANDING1 R8601	LANDING0 R8660
00 - 2	NOSTUFF	NOSTUFF
01 - 4	NOSTUFF	ASSEMBLE
10 - 8	ASSEMBLE	NOSTUFF
11 - RESERVED	ASSEMBLE	ASSEMBLE

NAND CONFIGURATION

CONFIG	ROMBOOT2 R8617	ROMBOOT1 R8618	ROMBOOT0 R8616
000 - MLC SD/TOS 1Y/1Z (W/ HARD RESET)	NOSTUFF	NOSTUFF	NOSTUFF
001 - MLC SD/TOS 1Y/1Z (W/O HARD RESET)	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	NOSTUFF	NOSTUFF
011 - MLC HYNIX 3D-V2	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	NOSTUFF	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

OPERATION MODE (ODT, CLK FREQ, ETC)

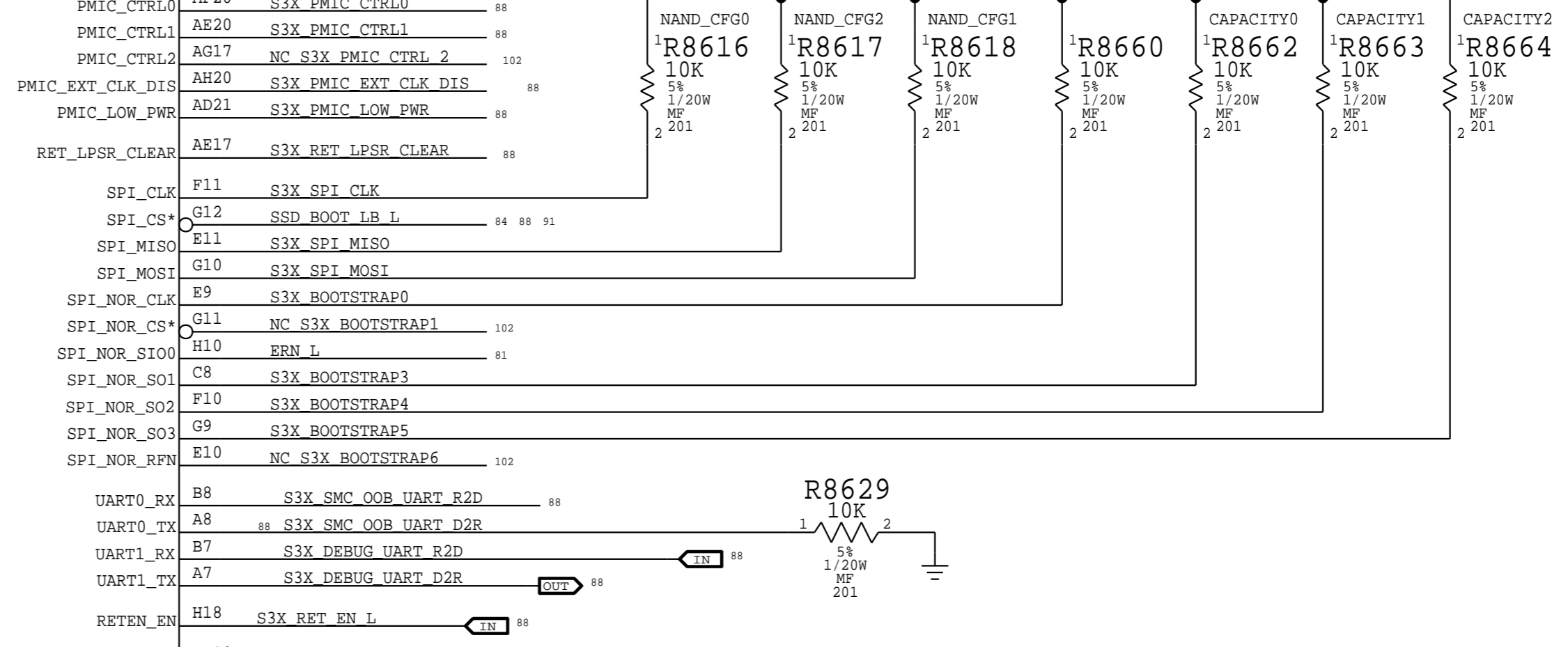
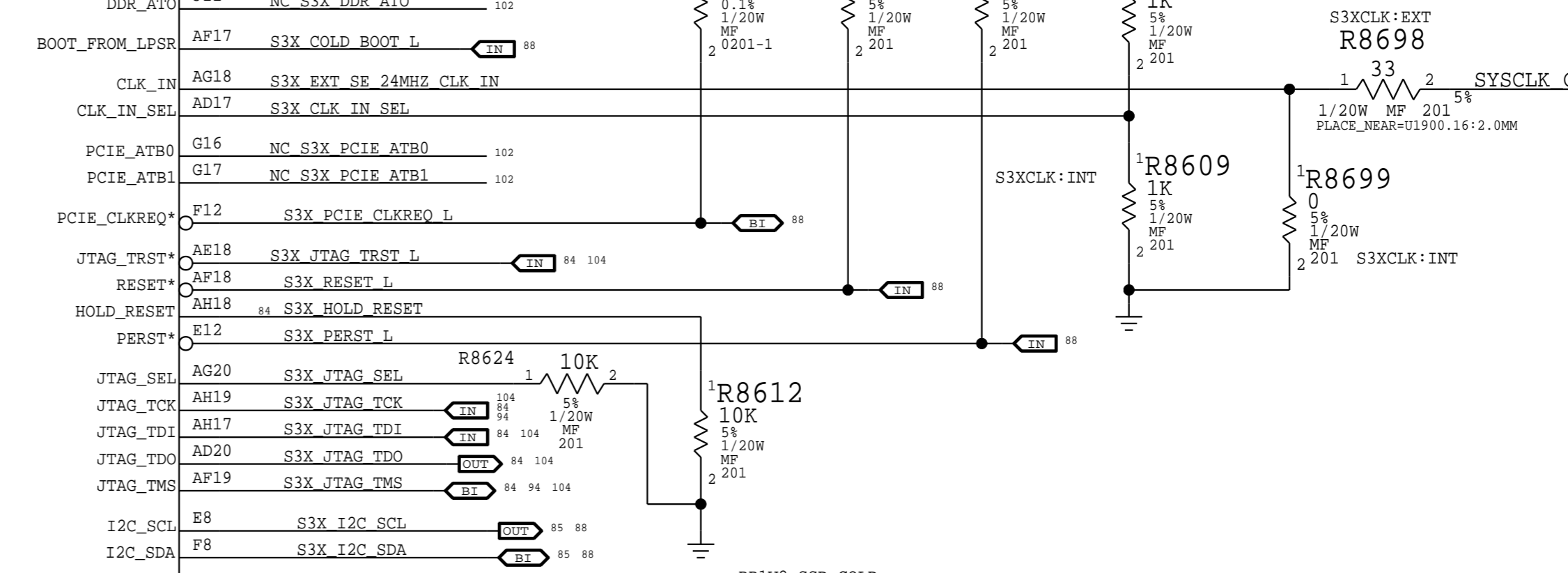
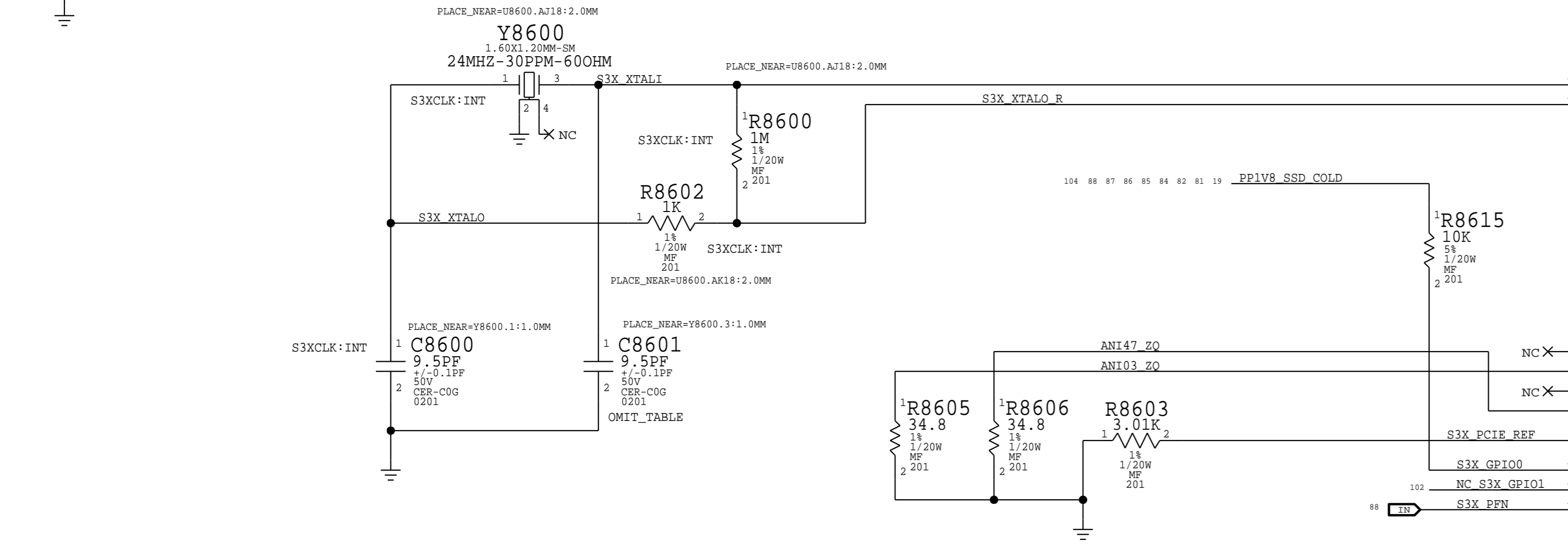
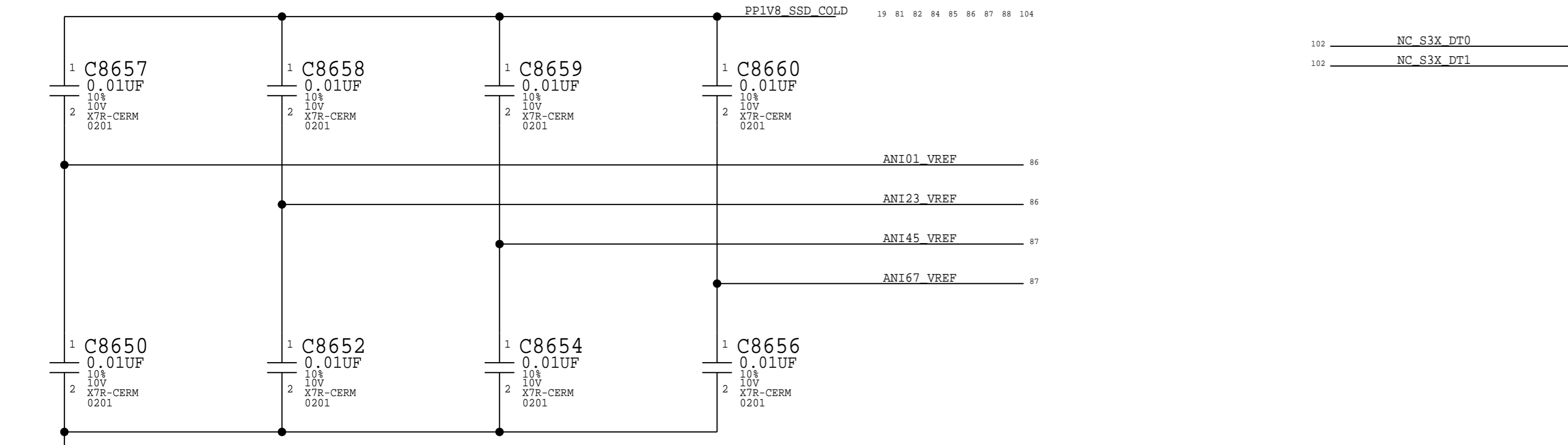
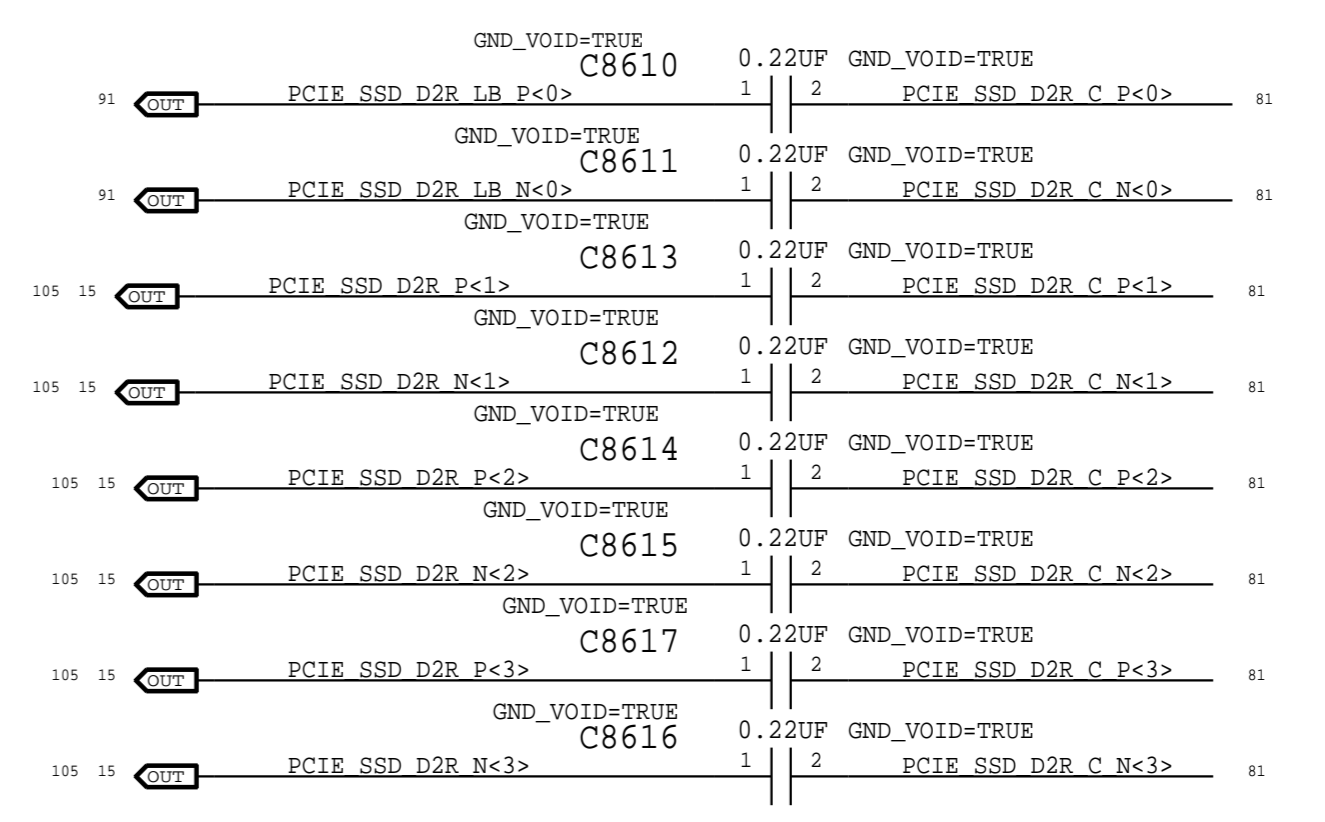
CONFIG	OP_MODE2 R8614	OP_MODE1 R8615	OP_MODE0 R8660
000 - TEABERRY	NOSTUFF	NOSTUFF	NOSTUFF
001 - XB58 GS	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	ASSEMBLE	NOSTUFF
011 - RESERVED	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	ASSEMBLE	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

PRODUCT CAPACITY

CONFIG	CAPACITY2 R8664	CAPACITY1 R8663	CAPACITY0 R8662
000 - 32GB	NOSTUFF	NOSTUFF	NOSTUFF
001 - 64GB	NOSTUFF	NOSTUFF	ASSEMBLE
010 - 128GB	NOSTUFF	ASSEMBLE	NOSTUFF
011 - 256GB	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - 512GB	ASSEMBLE	NOSTUFF	NOSTUFF
101 - 1024GB	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - 2048GB	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

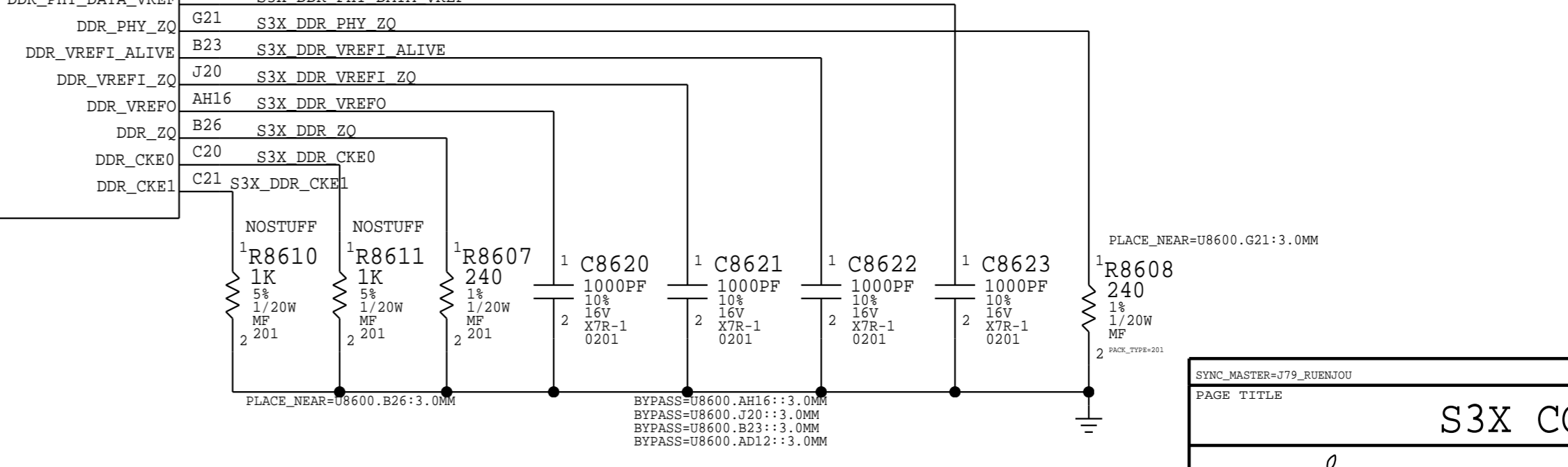
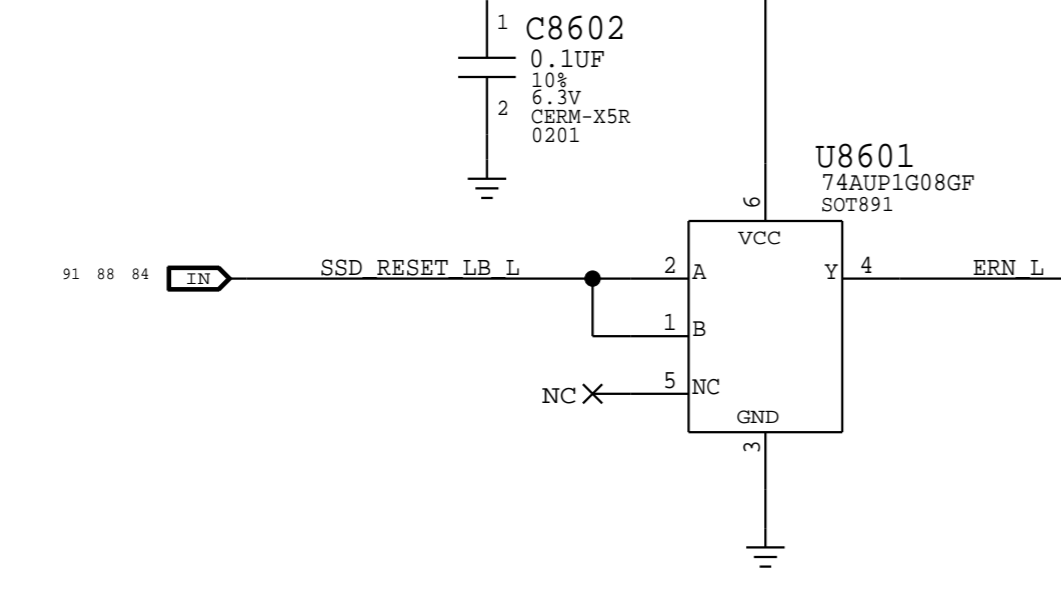
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U8600
S3X
BGA-H1P35
SYM 3 OF 7

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REFCLK_N <td>A18</td> <td>PCIE_CLK100M SSD LB N</td> <td>91 105</td>	A18	PCIE_CLK100M SSD LB N	91 105
PCIE_TX0_P <td>A17</td> <td>PCIE_SSD_D2R_C P<0></td> <td>81</td>	A17	PCIE_SSD_D2R_C P<0>	81
PCIE_TX0_M <td>A16</td> <td>PCIE_SSD_D2R_C N<0></td> <td>81</td>	A16	PCIE_SSD_D2R_C N<0>	81
PCIE_TX1_P <td>A15</td> <td>PCIE_SSD_D2R_C P<1></td> <td>81</td>	A15	PCIE_SSD_D2R_C P<1>	81
PCIE_TX1_M <td>A14</td> <td>PCIE_SSD_D2R_C N<1></td> <td>81</td>	A14	PCIE_SSD_D2R_C N<1>	81
PCIE_TX2_P <td>A13</td> <td>PCIE_SSD_D2R_C P<2></td> <td>81</td>	A13	PCIE_SSD_D2R_C P<2>	81
PCIE_TX2_M <td>A12</td> <td>PCIE_SSD_D2R_C N<2></td> <td>81</td>	A12	PCIE_SSD_D2R_C N<2>	81
PCIE_TX3_P <td>A11</td> <td>PCIE_SSD_D2R_C P<3></td> <td>81</td>	A11	PCIE_SSD_D2R_C P<3>	81
PCIE_TX3_M <td>A10</td> <td>PCIE_SSD_D2R_C N<3></td> <td>81</td>	A10	PCIE_SSD_D2R_C N<3>	81
PCIE_RX0_P <td>C17</td> <td>PCIE_SSD_R2D_LB P<0></td> <td>84</td>	C17	PCIE_SSD_R2D_LB P<0>	84
PCIE_RX0_M <td>C16</td> <td>PCIE_SSD_R2D_LB N<0></td> <td>84</td>	C16	PCIE_SSD_R2D_LB N<0>	84
PCIE_RX1_P <td>C15</td> <td>PCIE_SSD_R2D_P<1></td> <td>84</td>	C15	PCIE_SSD_R2D_P<1>	84
PCIE_RX1_M <td>C14</td> <td>PCIE_SSD_R2D_N<1></td> <td>84</td>	C14	PCIE_SSD_R2D_N<1>	84
PCIE_RX2_P <td>C13</td> <td>PCIE_SSD_R2D_P<2></td> <td>84</td>	C13	PCIE_SSD_R2D_P<2>	84
PCIE_RX2_M <td>C12</td> <td>PCIE_SSD_R2D_N<2></td> <td>84</td>	C12	PCIE_SSD_R2D_N<2>	84
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PCIE_RX3_M <td>C10</td> <td>PCIE_SSD_R2D_N<3></td> <td>84</td>	C10	PCIE_SSD_R2D_N<3>	84



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00077	1	CAP, 9.5PF, 50V, 0201	C8601	CRITICAL	S3XCLK:INT
117S0002	1	RES, MF, 0 OHM, 1/20W, 0201	C8601	CRITICAL	S3XCLK:EXT

Buffered SSD_RESET L to Mitigate EPO Issue

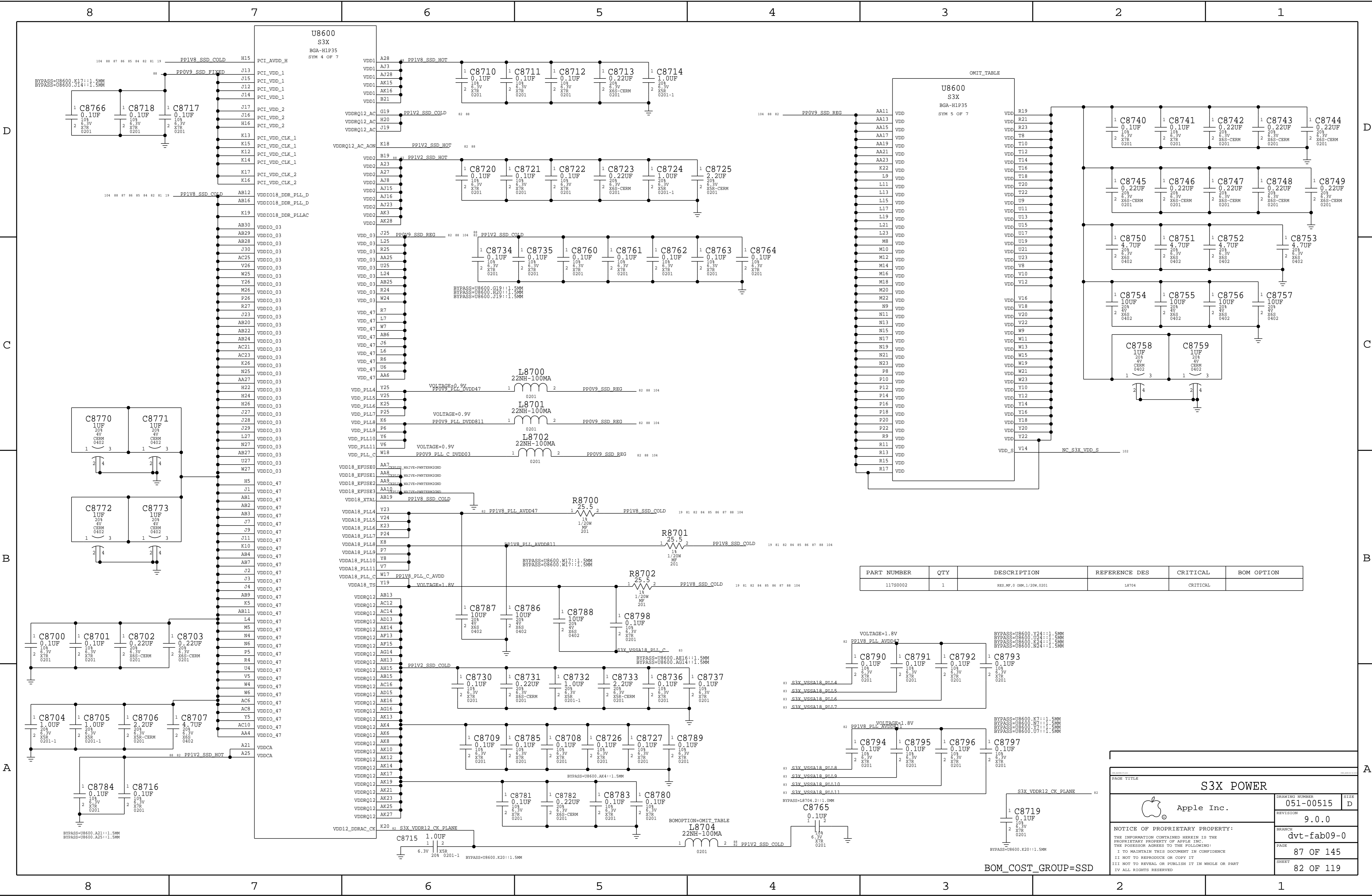


Apple Inc. S3X CORE PCIE

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9.0.0
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BOM_COST_GROUP=SSD



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11750002	1	RES, MF, 0 OHM, 1/20W, 0201	L8704	CRITICAL	

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		DRAWING NUMBER	051-00515
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		PAGE	87 OF 145
		SHEET	82 OF 119

BOM_COST_GROUP=S3X

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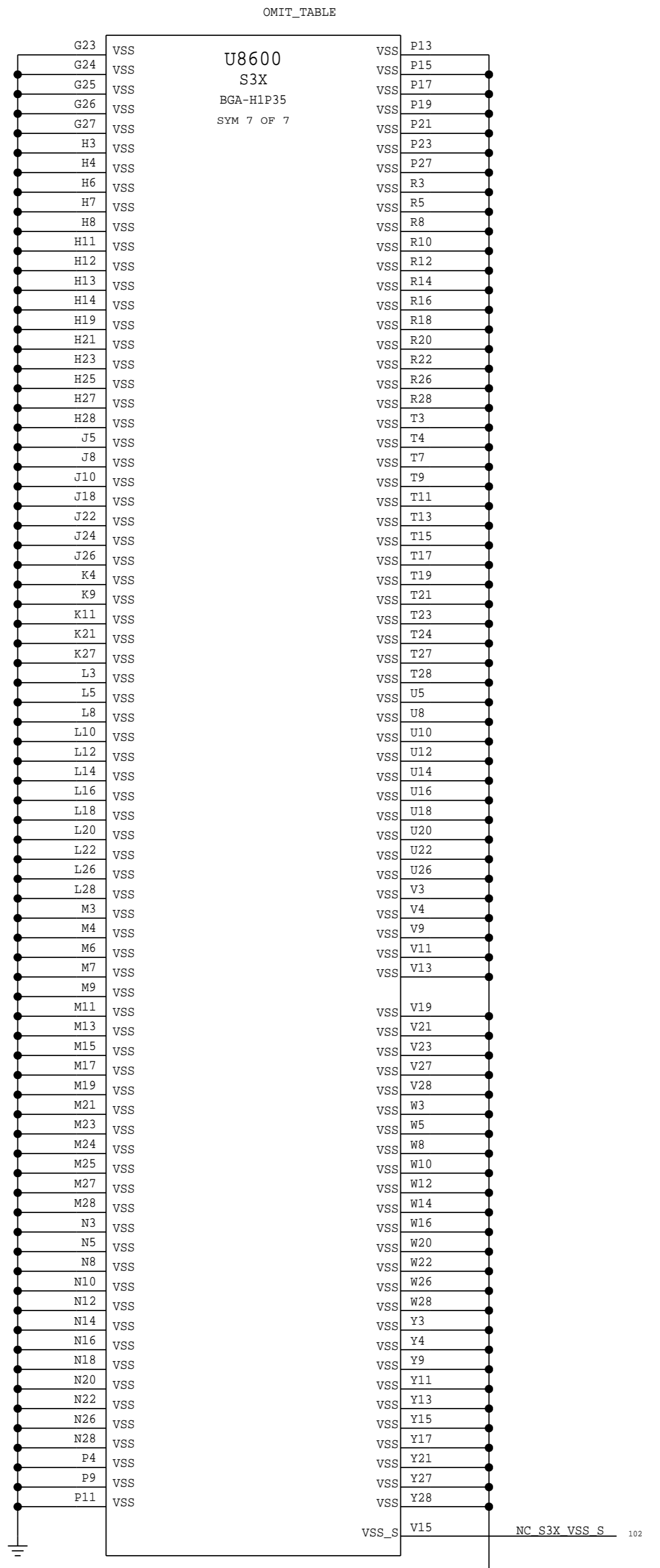
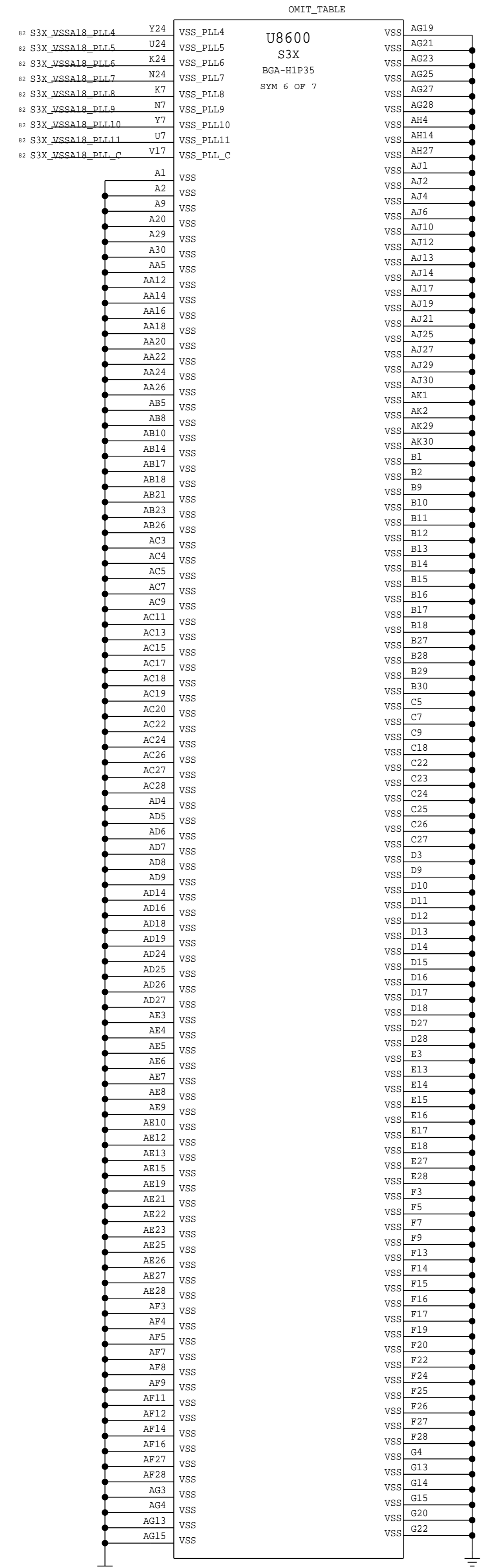
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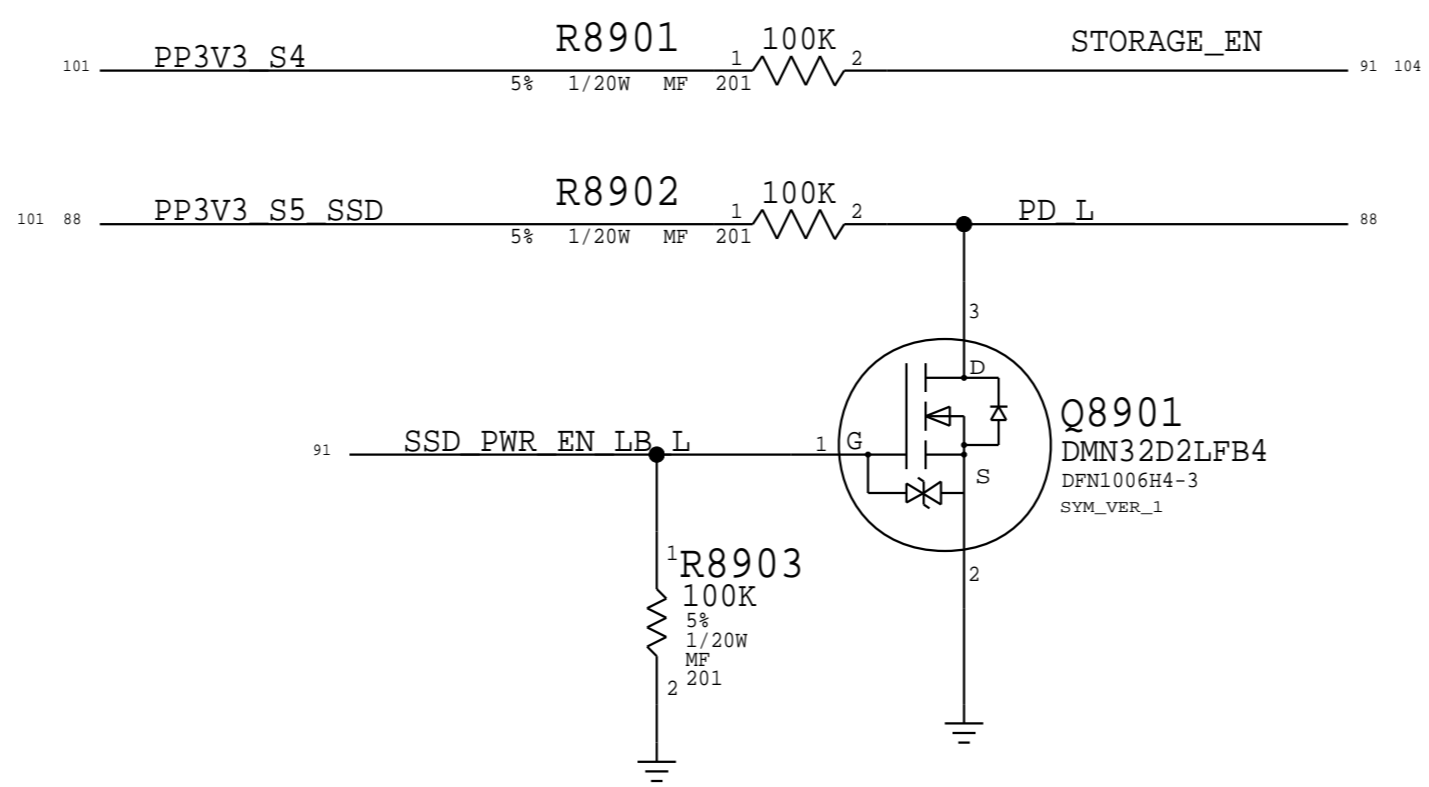
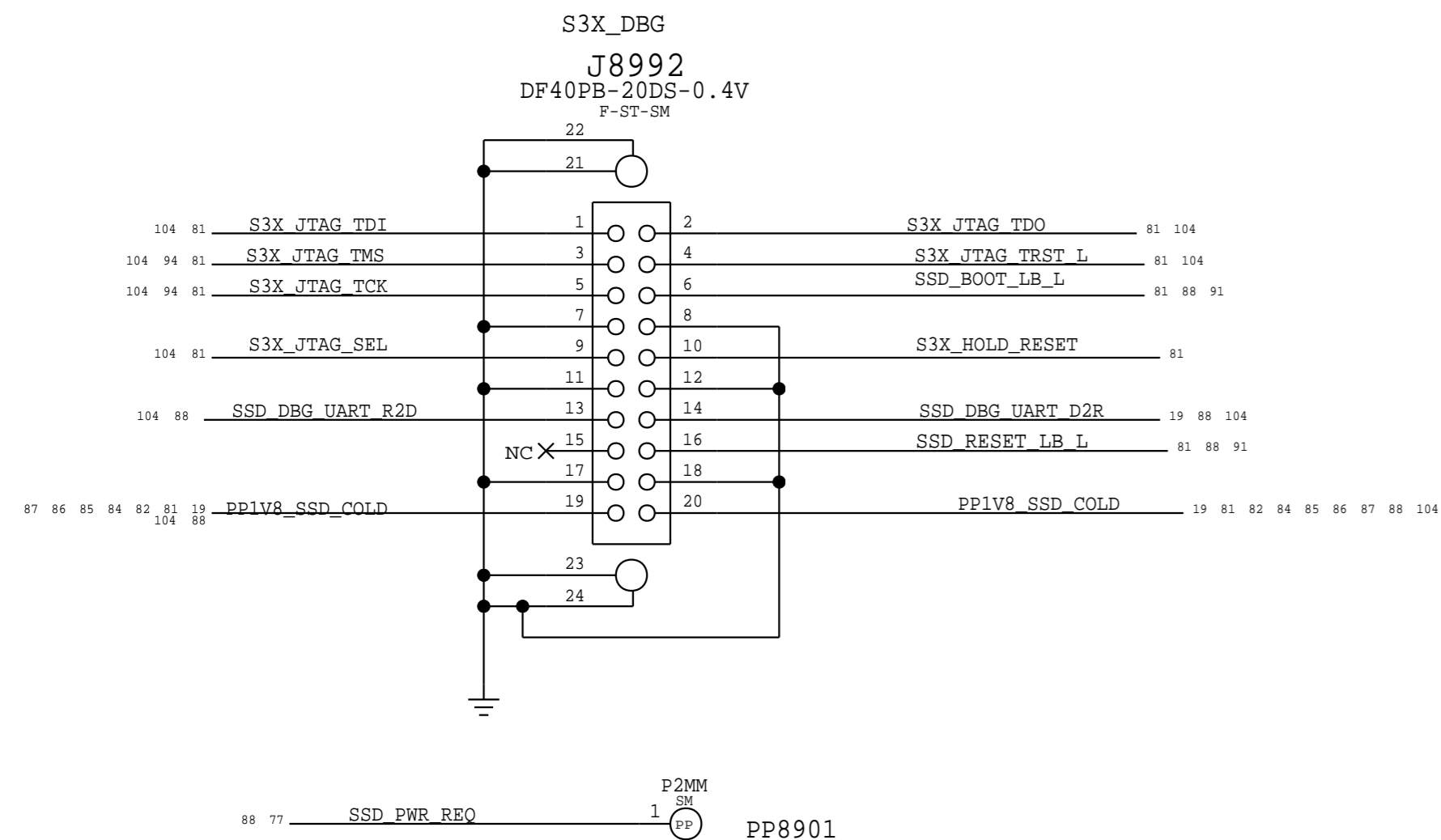
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		REVISION		9.0.0		BRANCH		dvt-fab09-0		PAGE		88 OF 145	
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		SHEET		83 OF 119									

JTAG (DEBUG 1)



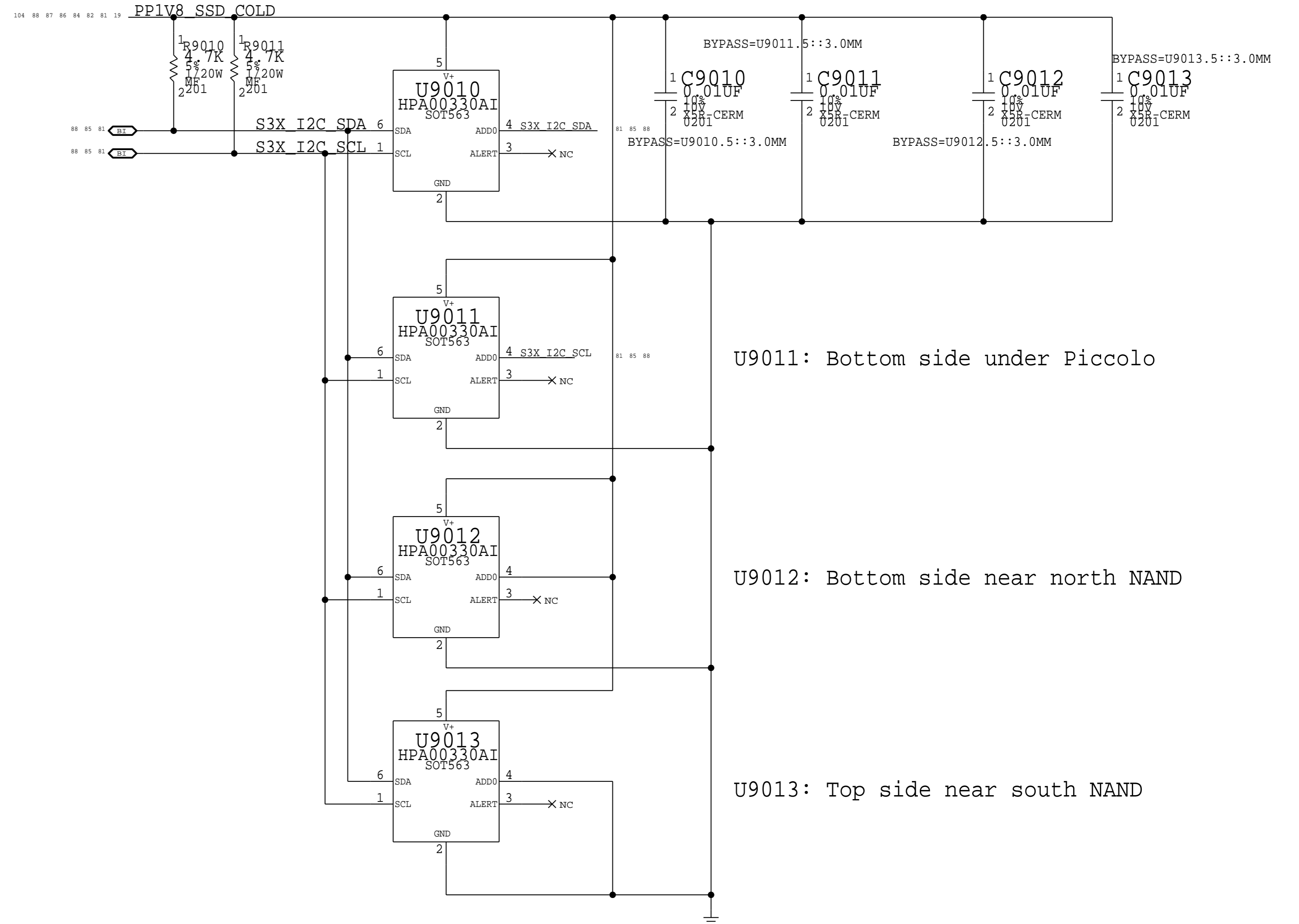
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PAGE TITLE			Connector	
Apple Inc.		DRAWING NUMBER	051-00515	SIZE
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		PAGE	89 OF 145	
		SHEET	84 OF 119	

BOM_COST_GROUP=SSD

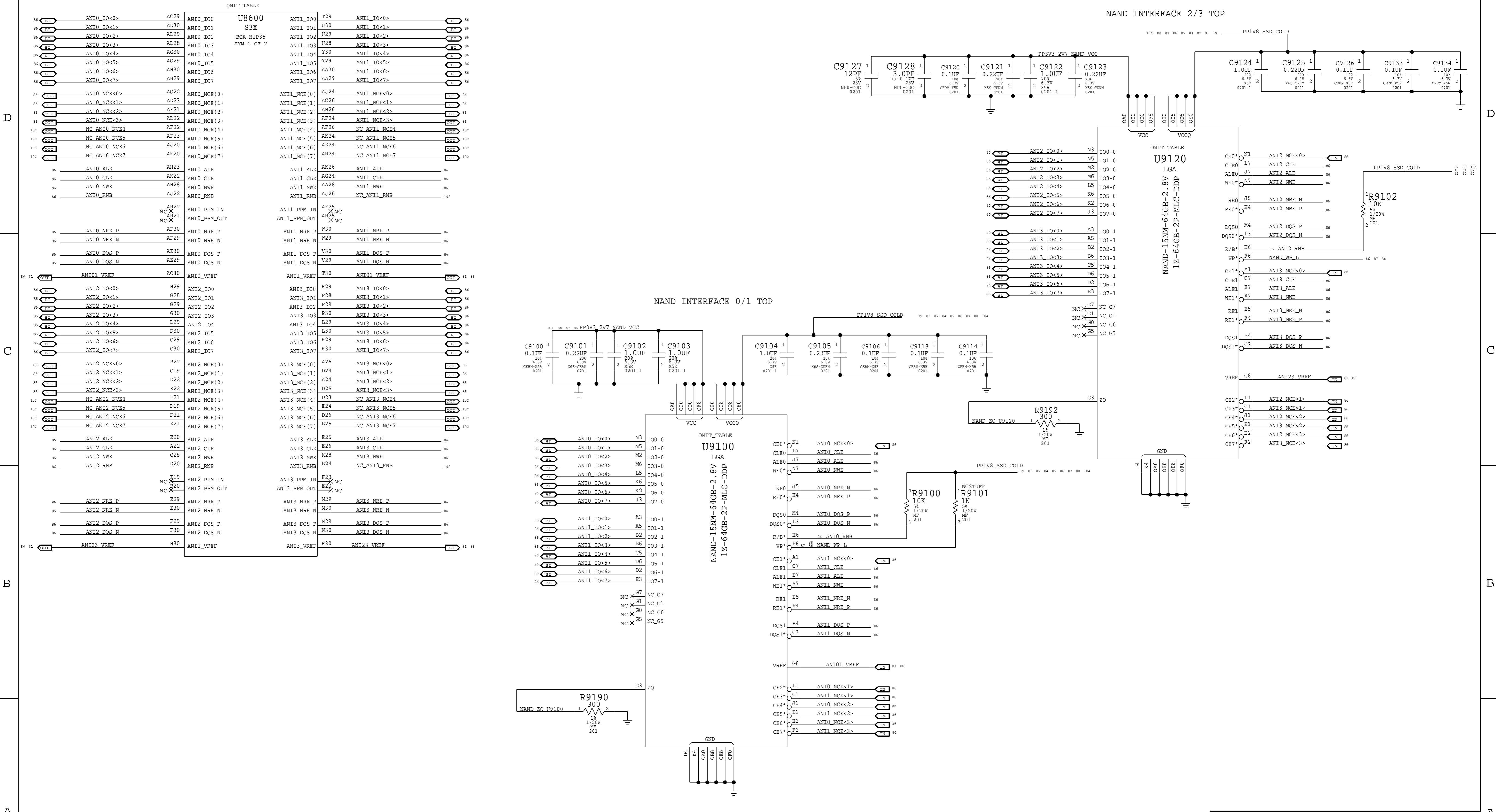
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1001001		V+
1001010		SDA
1001011		SCL

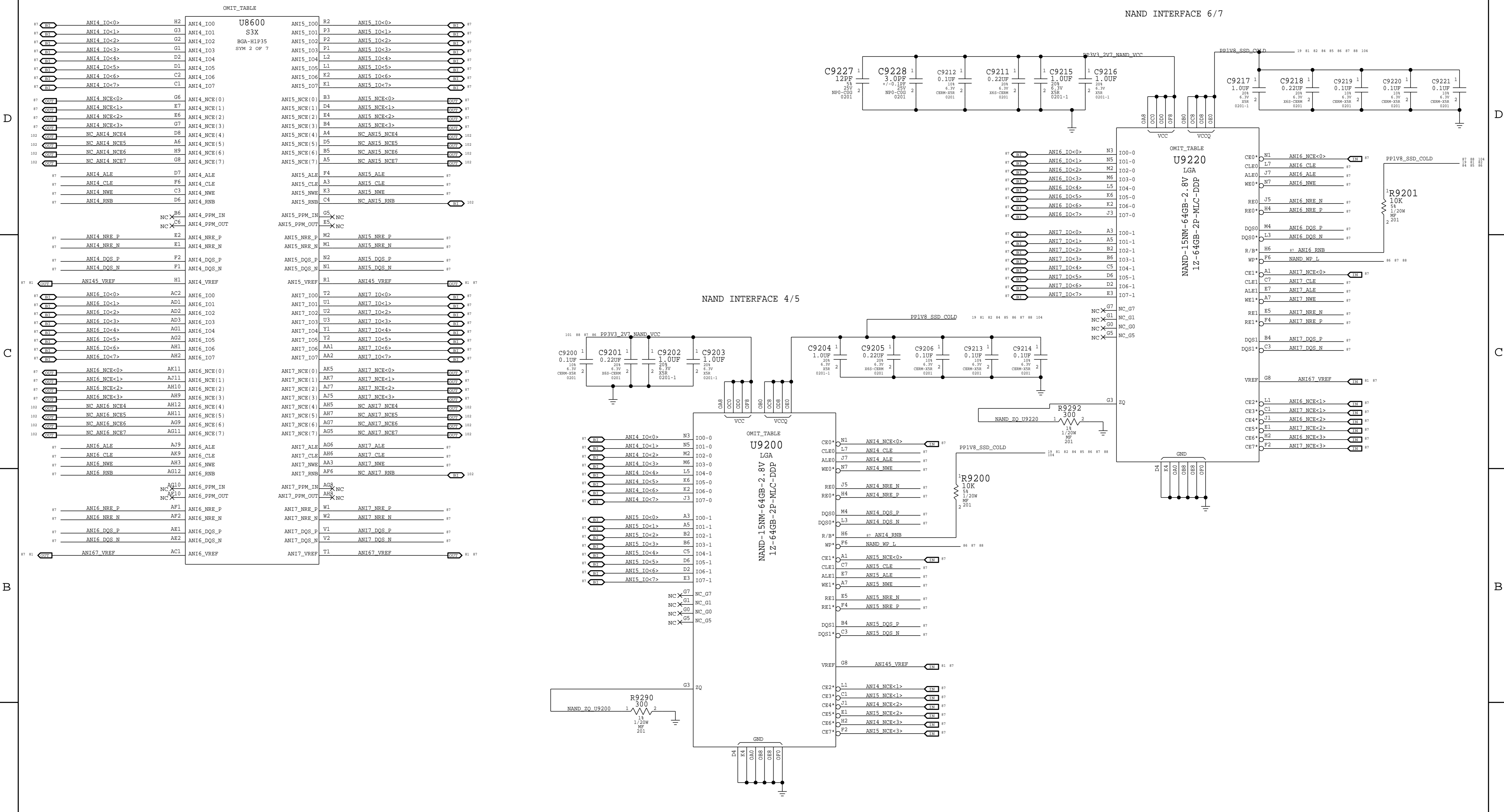
U9010: Top side under S3X



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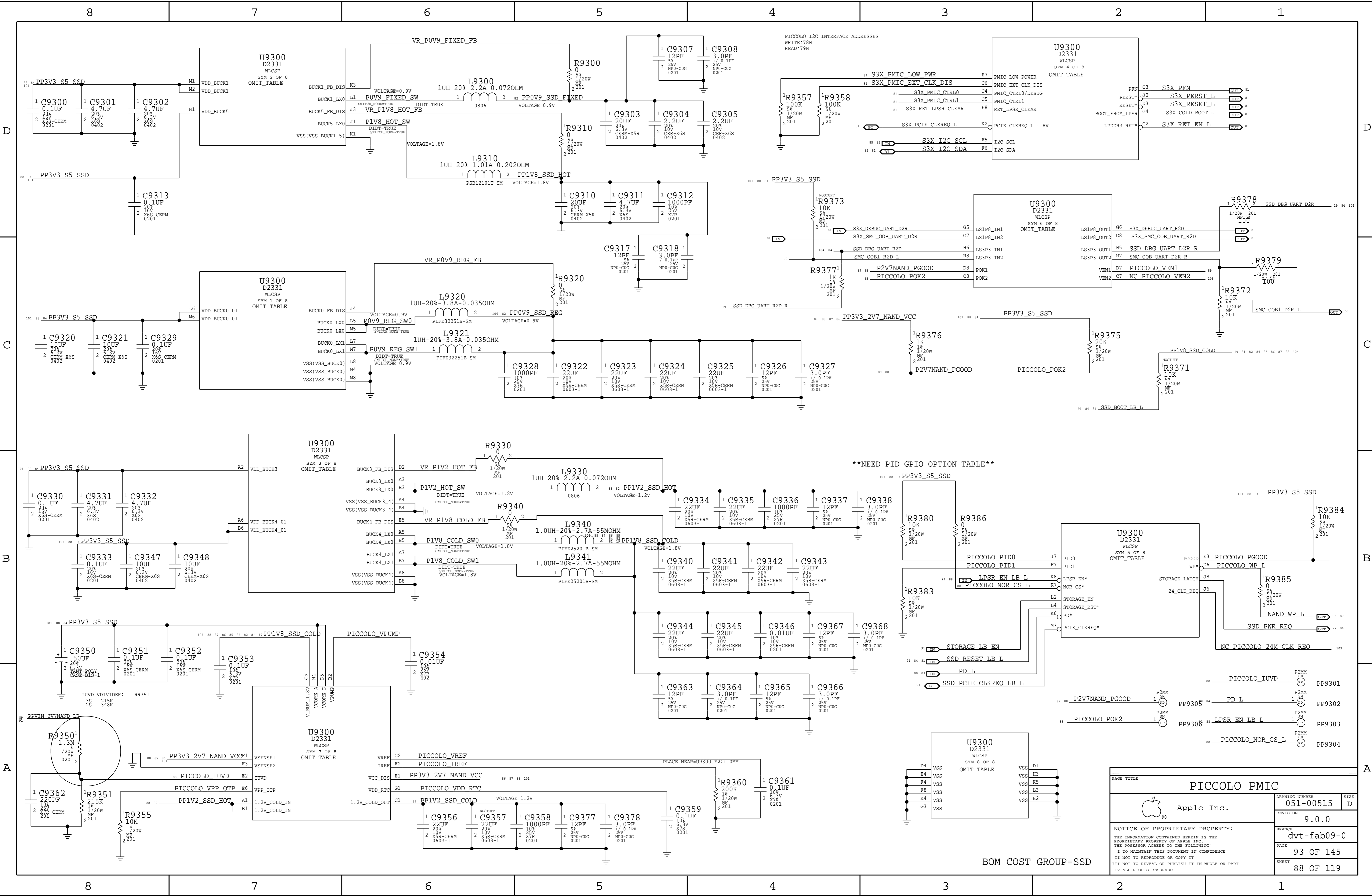
PAGE TITLE NAND VR, I2C ROM, TEMP SENSORS		DRWGNO NUMBER 051-00515	SIZE D
Apple Inc.		REVISION 9.0.0	BRANCH dvt-fab09-0
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		PAGE	92 OF 145
		SHEET	87 OF 119

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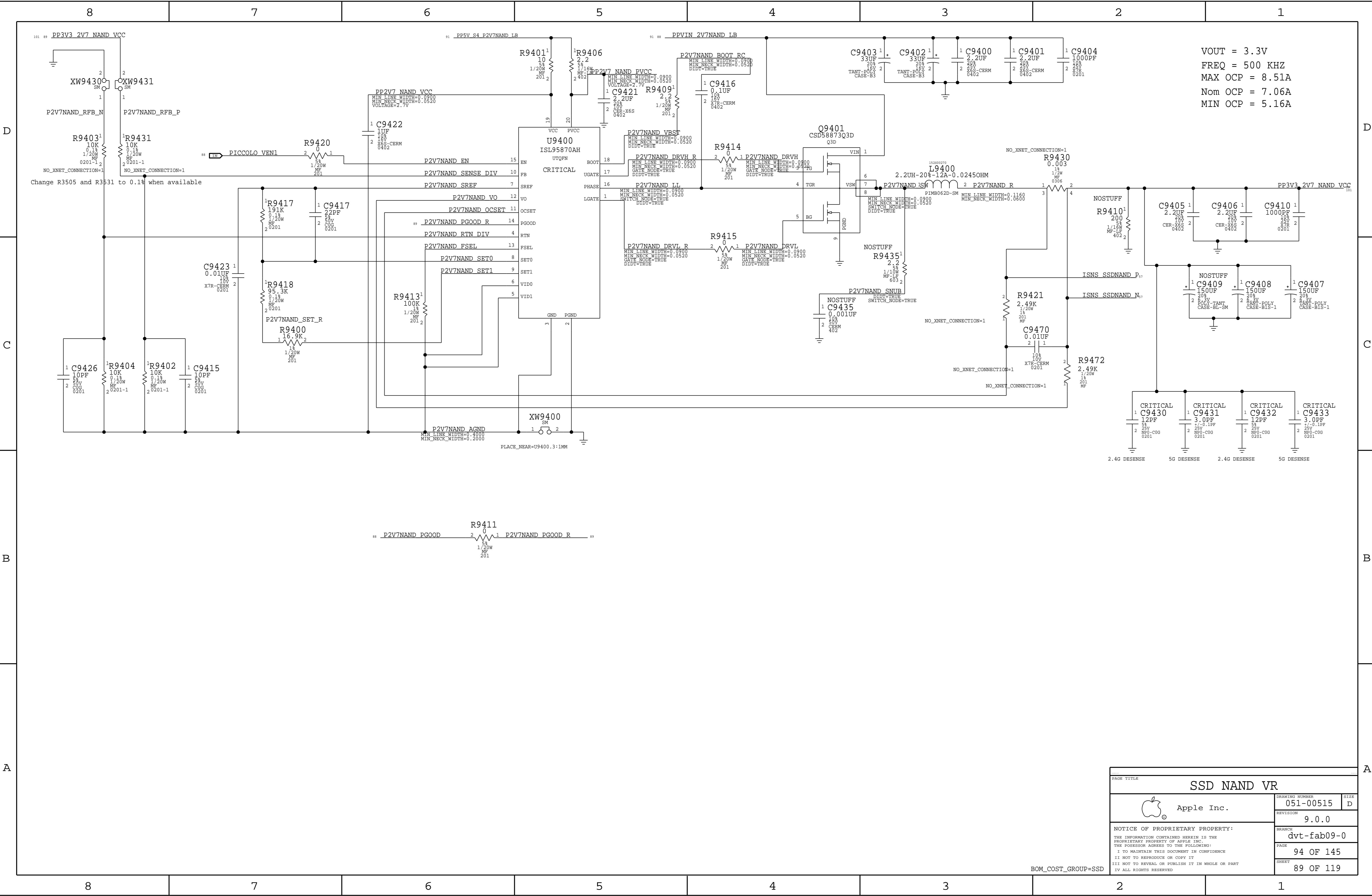


PICCOLO I2C INTERFACE ADDRESSES
 WRITE: 78H
 READ: 79H

****NEED PID GPIO OPTION TABLE****

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Apple Inc.		9.0.0		
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		PAGE	93 OF 145	
		SHEET	88 OF 119	

BOM_COST_GROUP=SSD



PAGE TITLE			SSD NAND VR	
Apple Inc.	DRAWING NUMBER	051-00515	STAR	D
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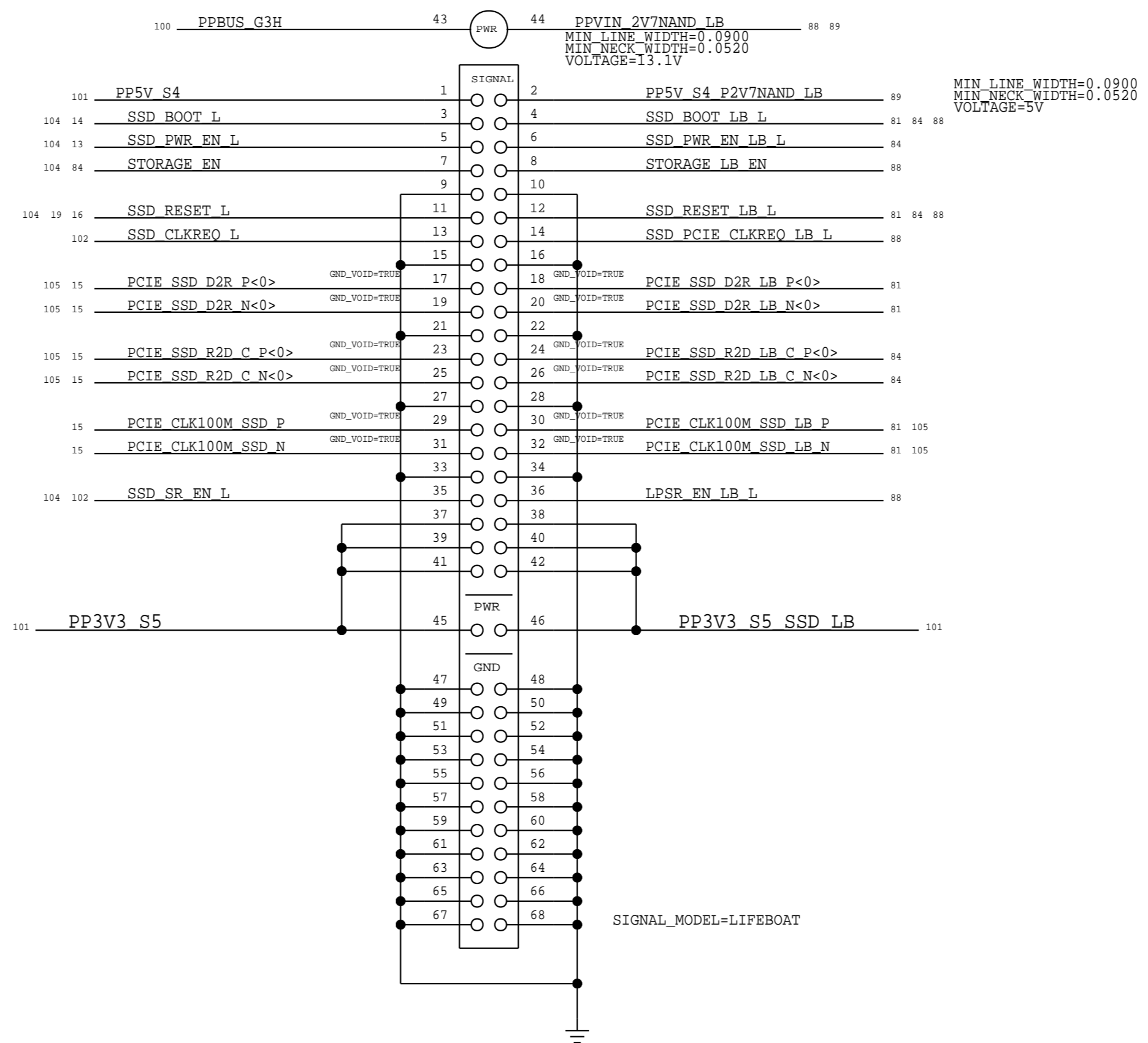
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LIFEBOAT

PCH Side J9600 SSD Side

20759-042E-02
P-ST-SM



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		SHEET	91 OF 119

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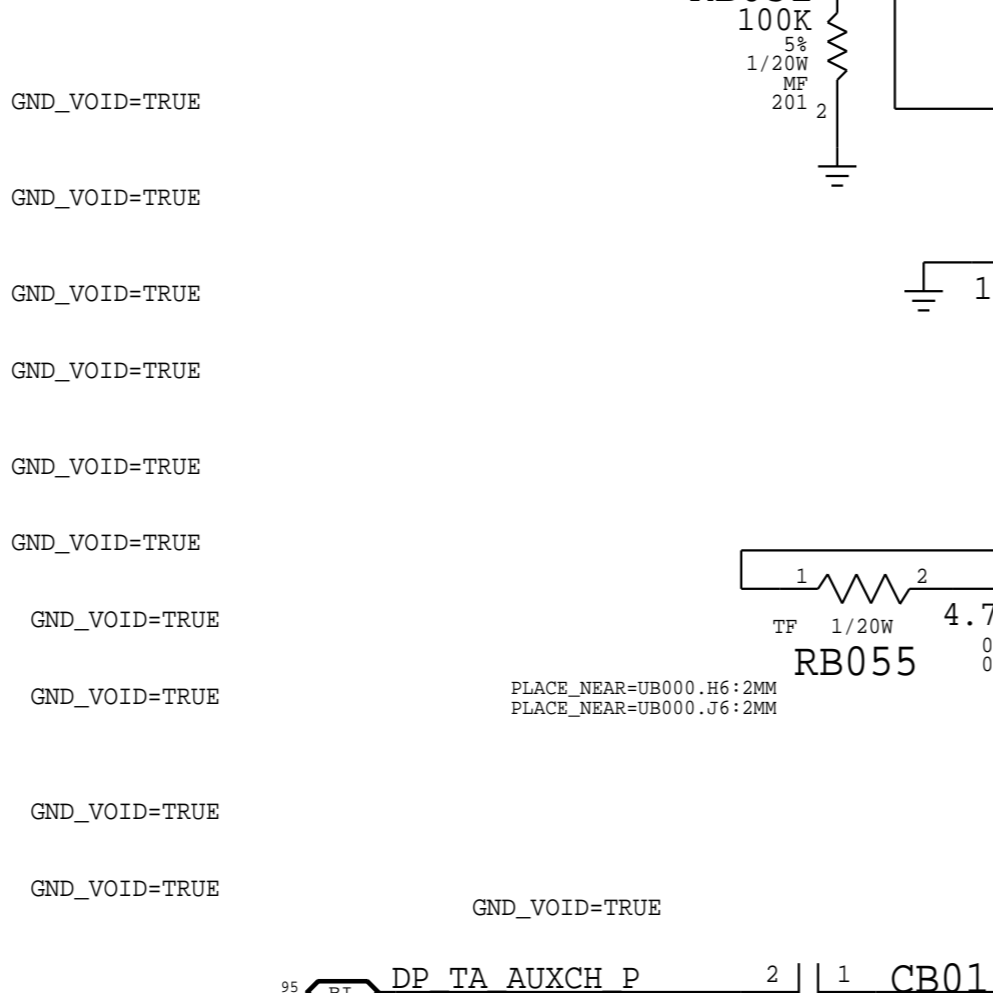
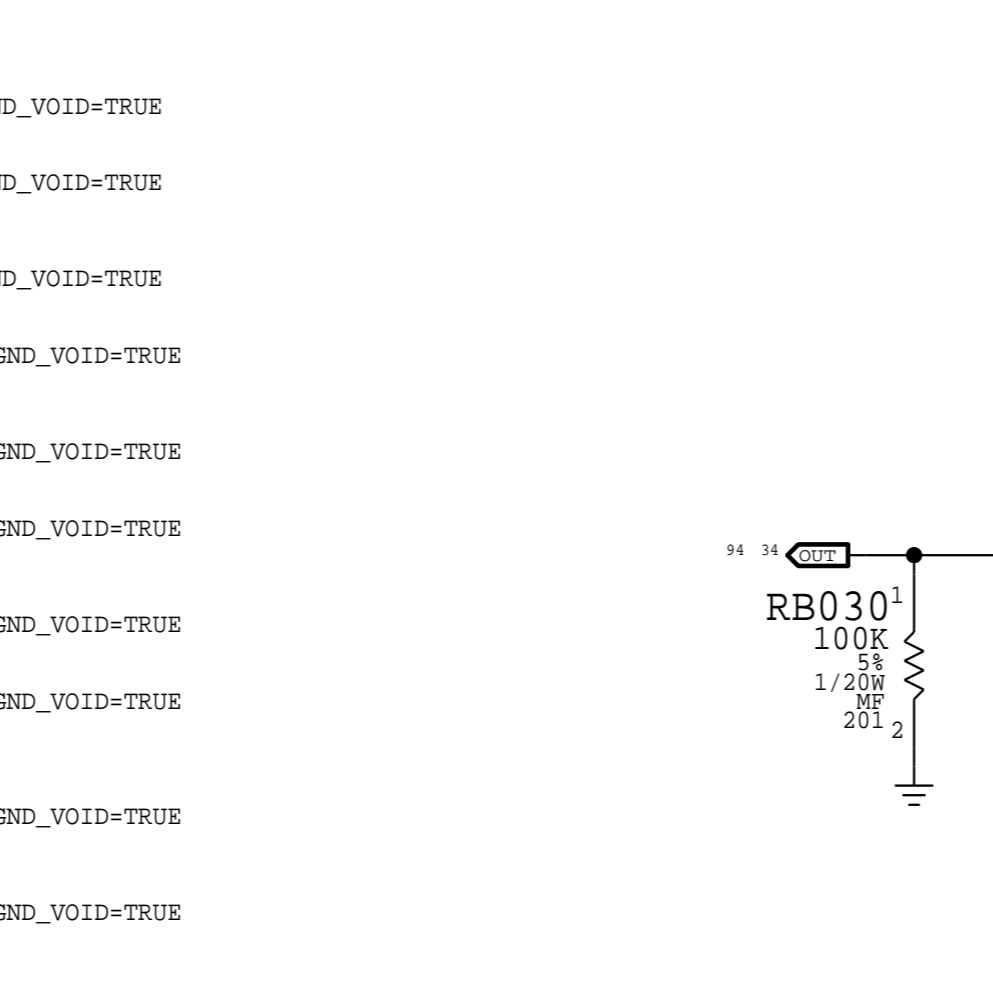
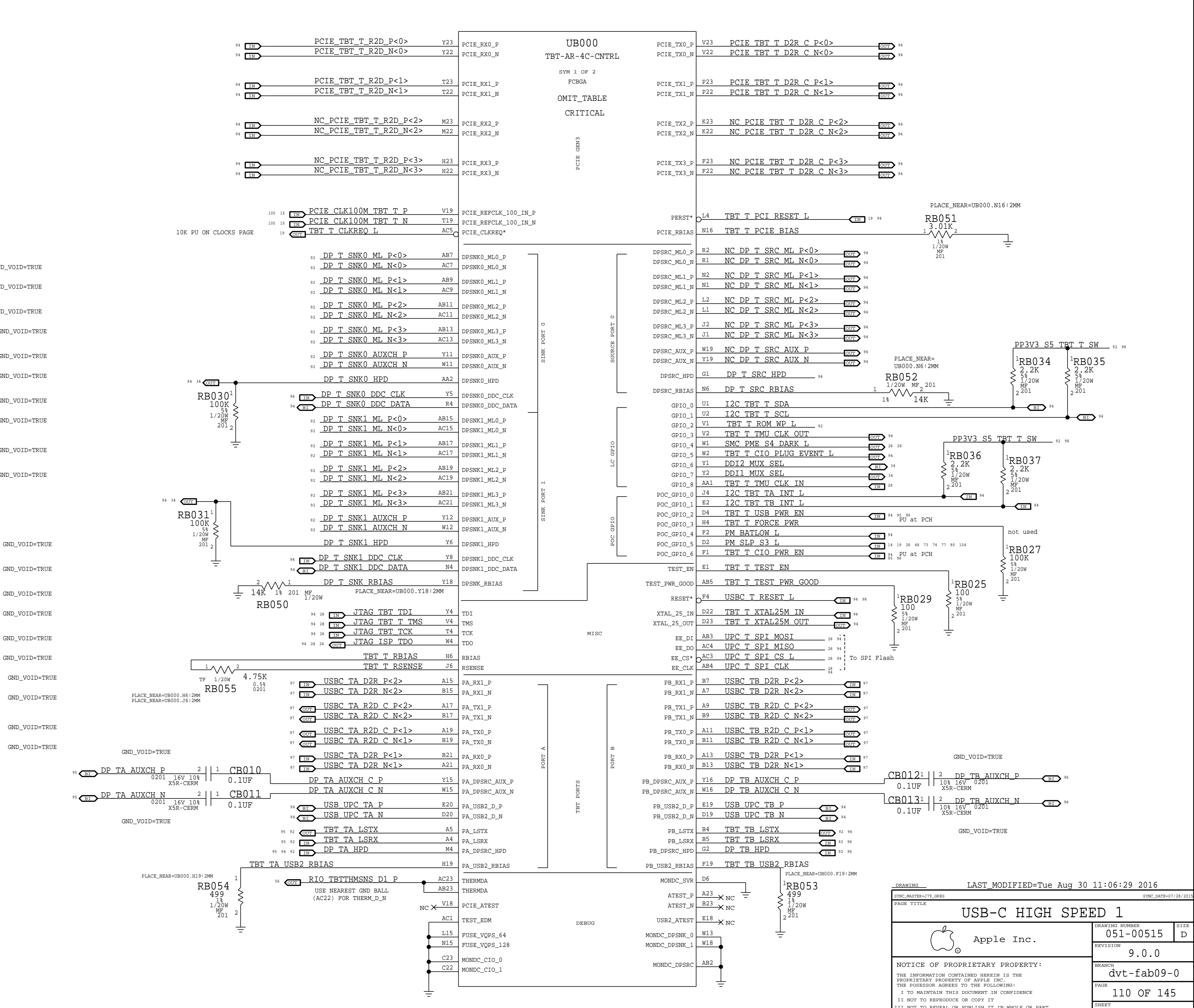
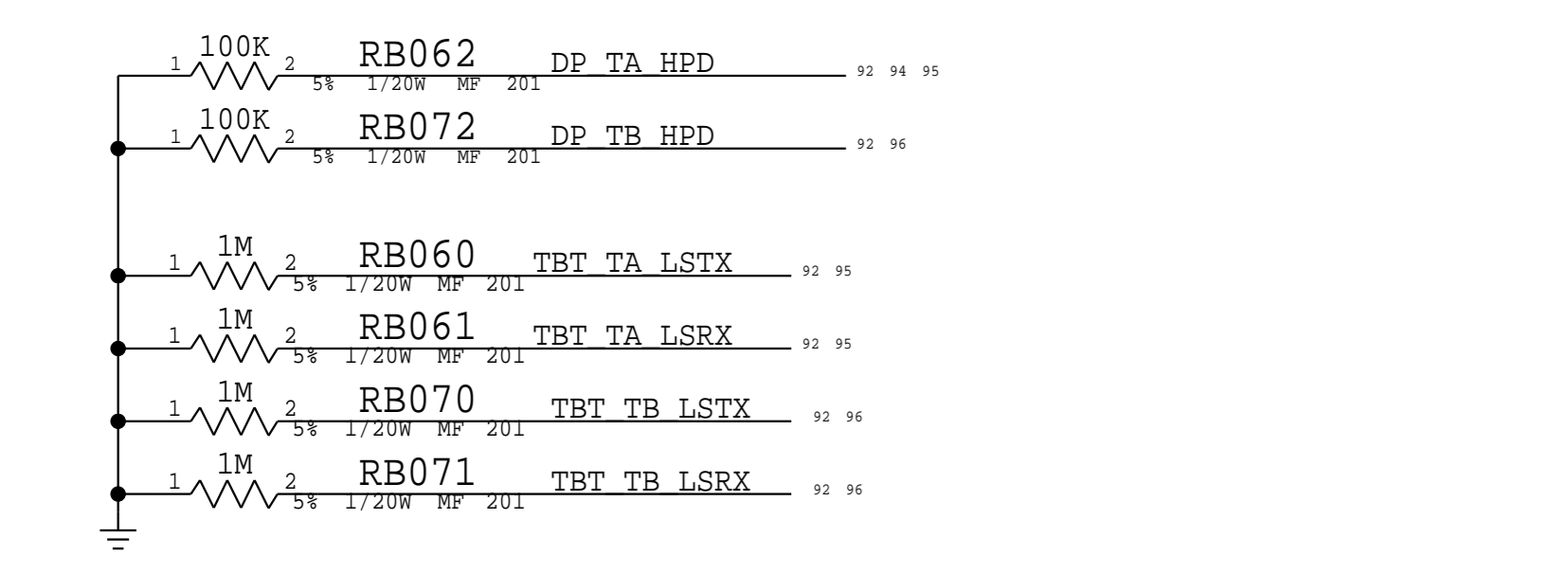
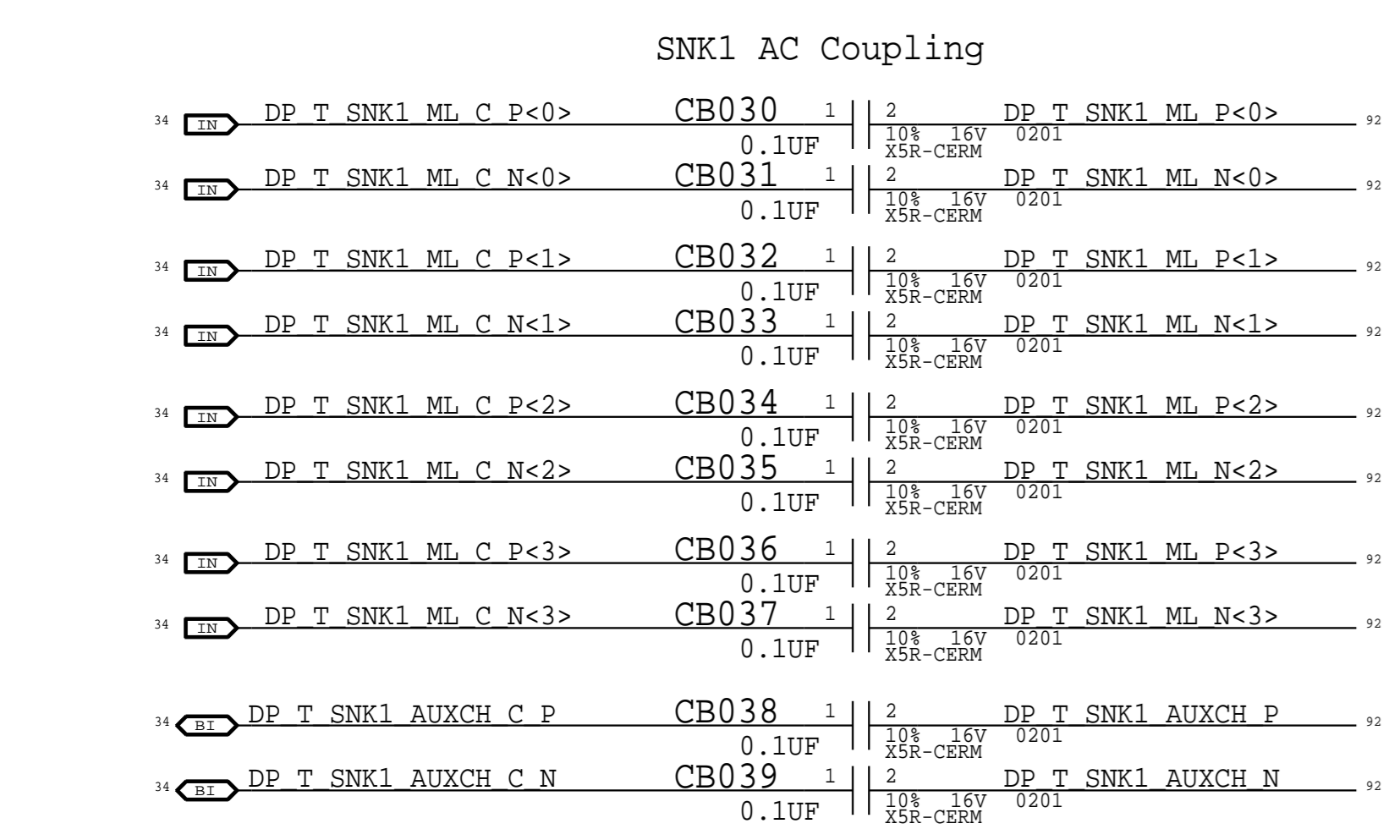
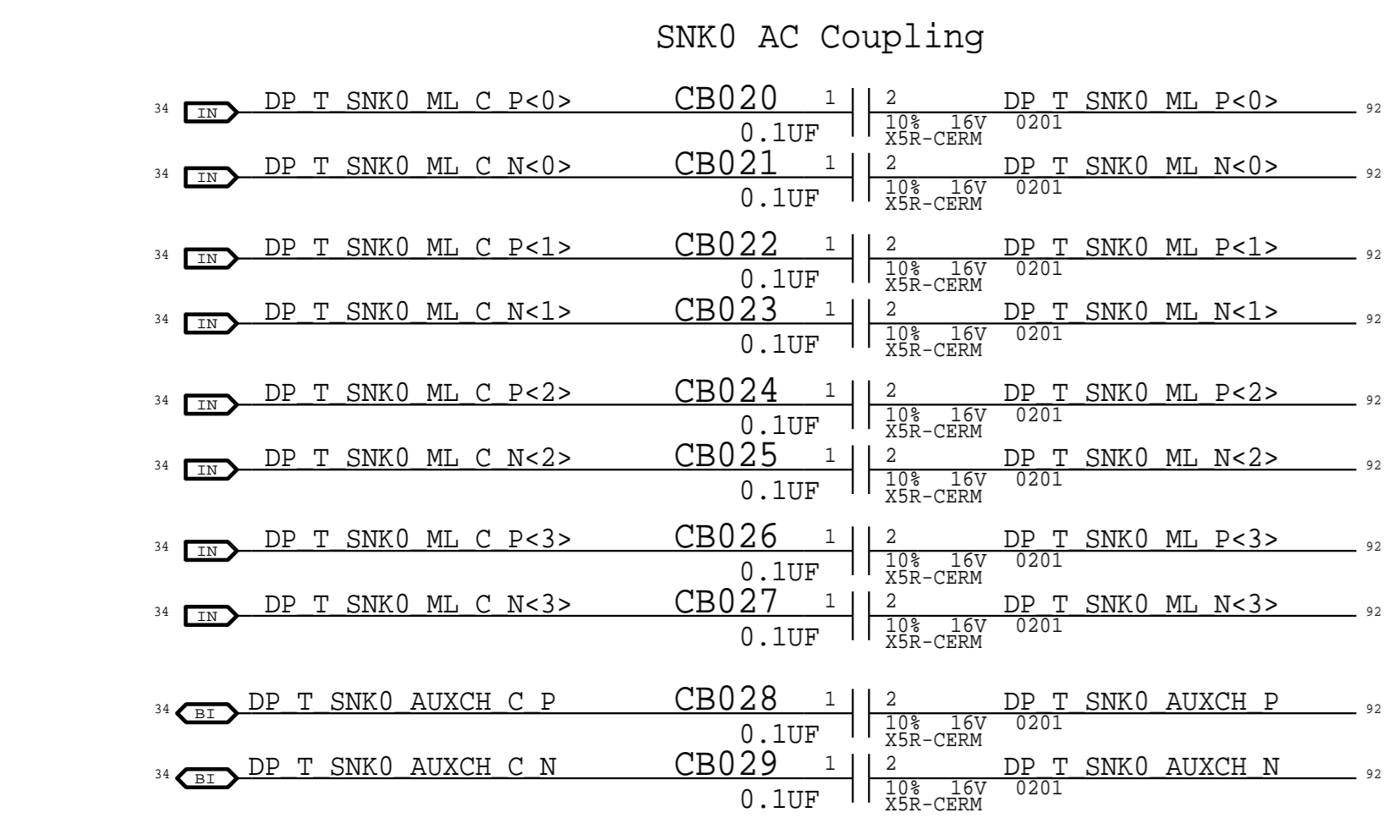
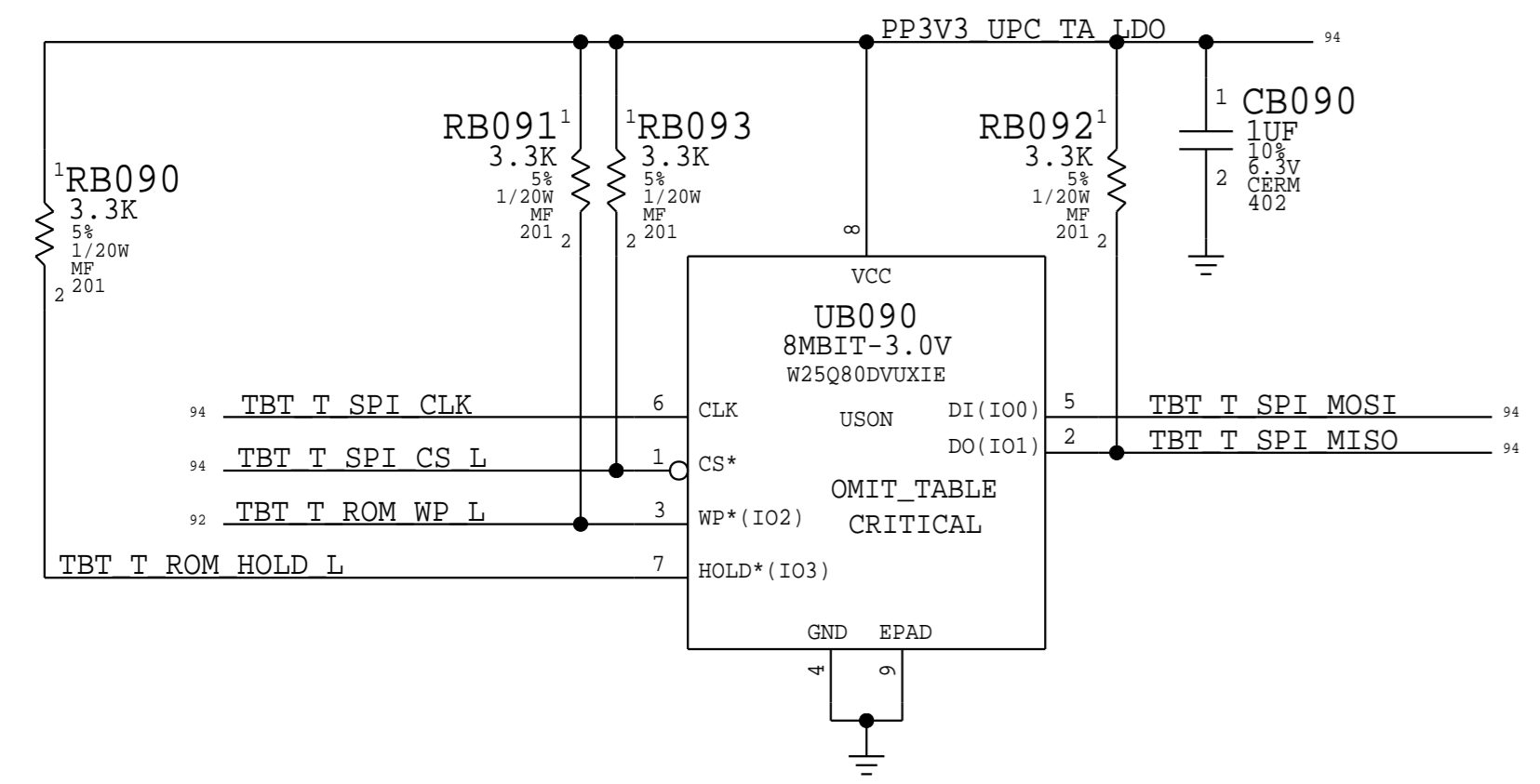
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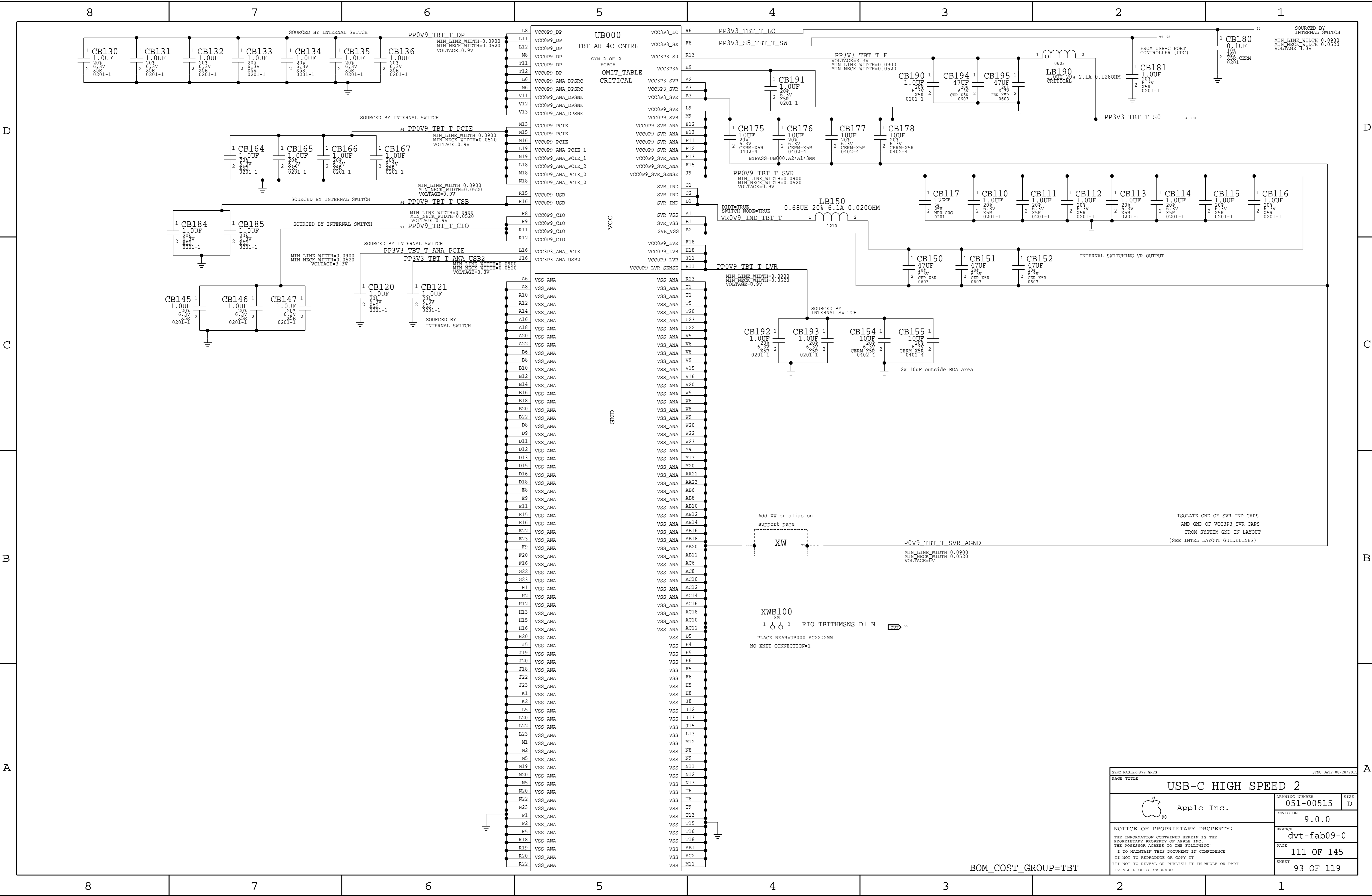
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Apple Inc.

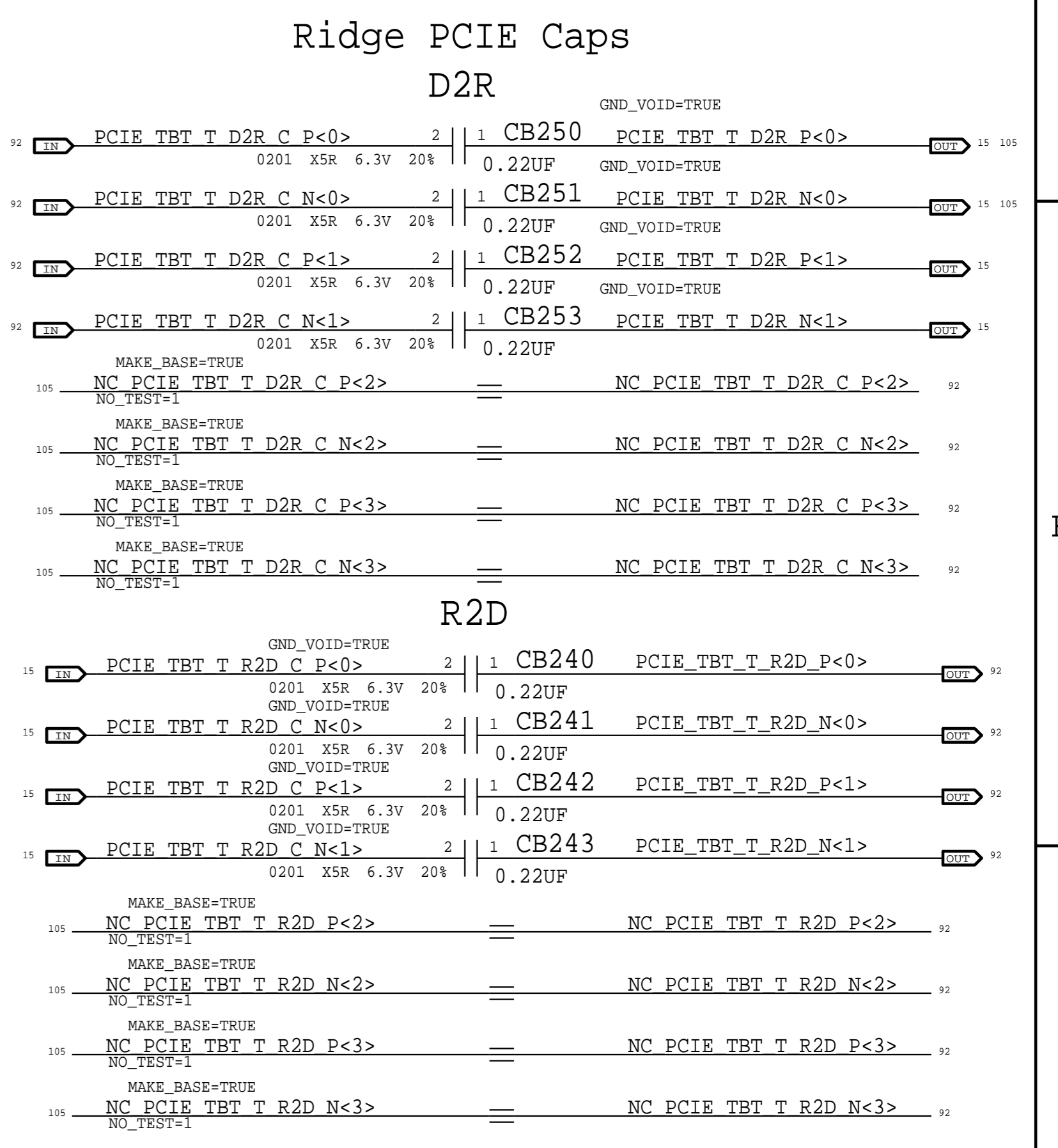
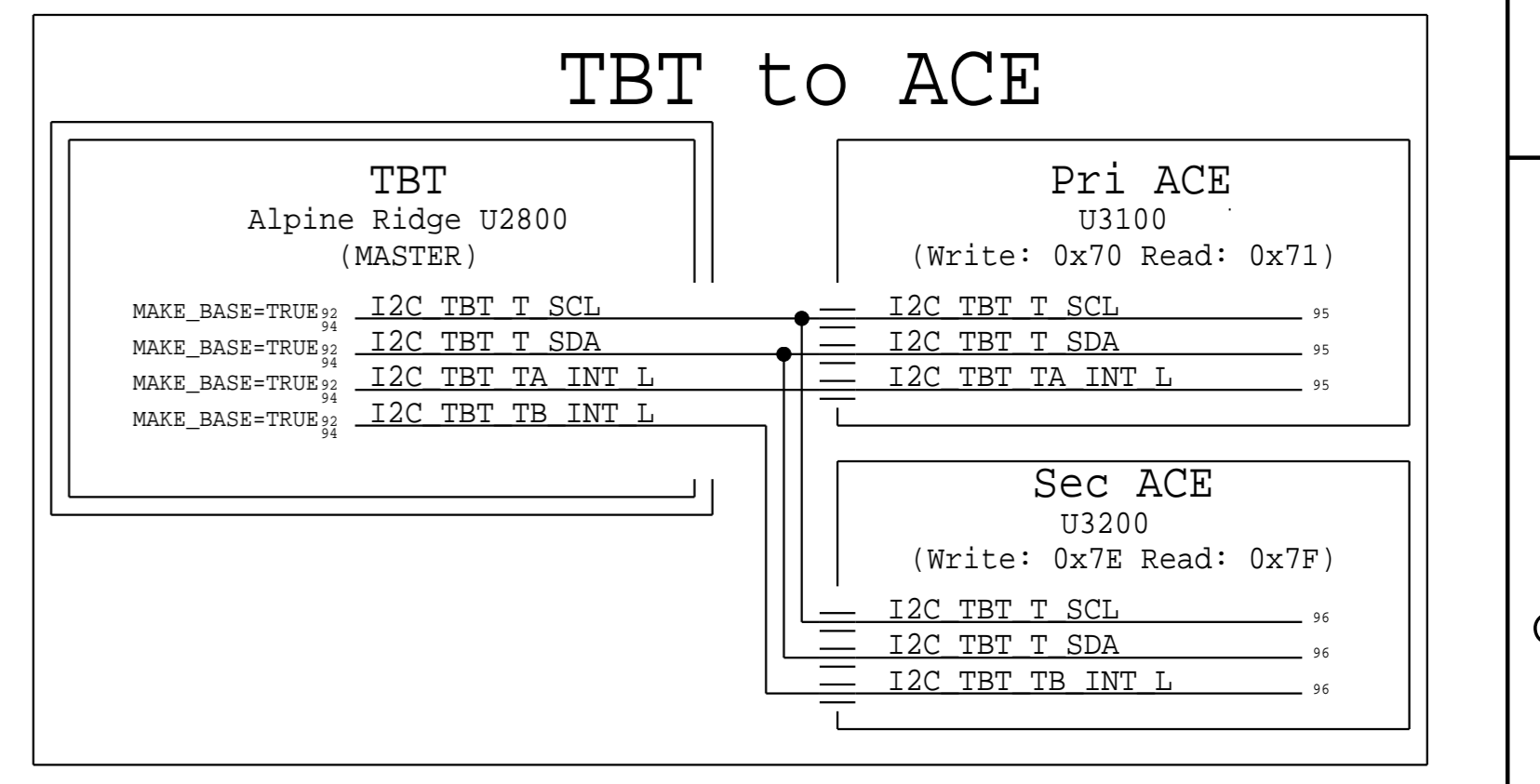
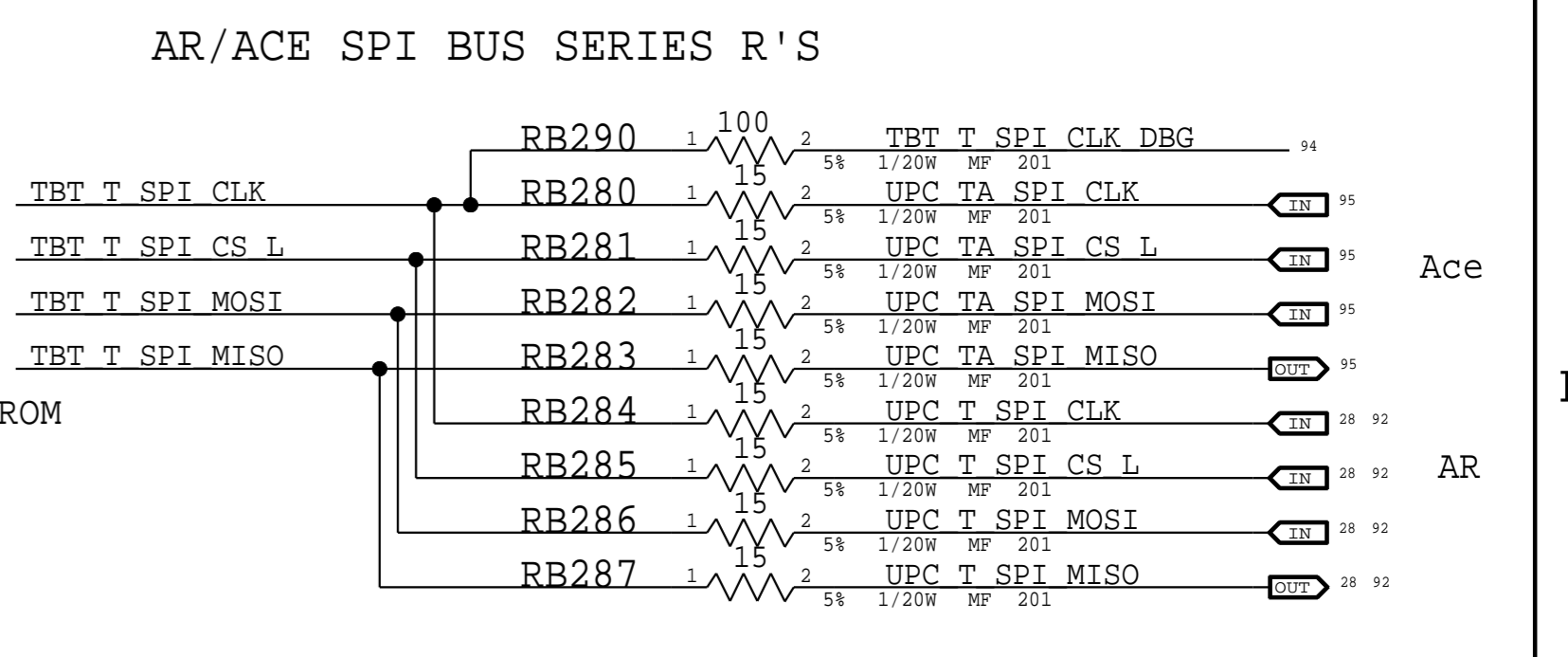
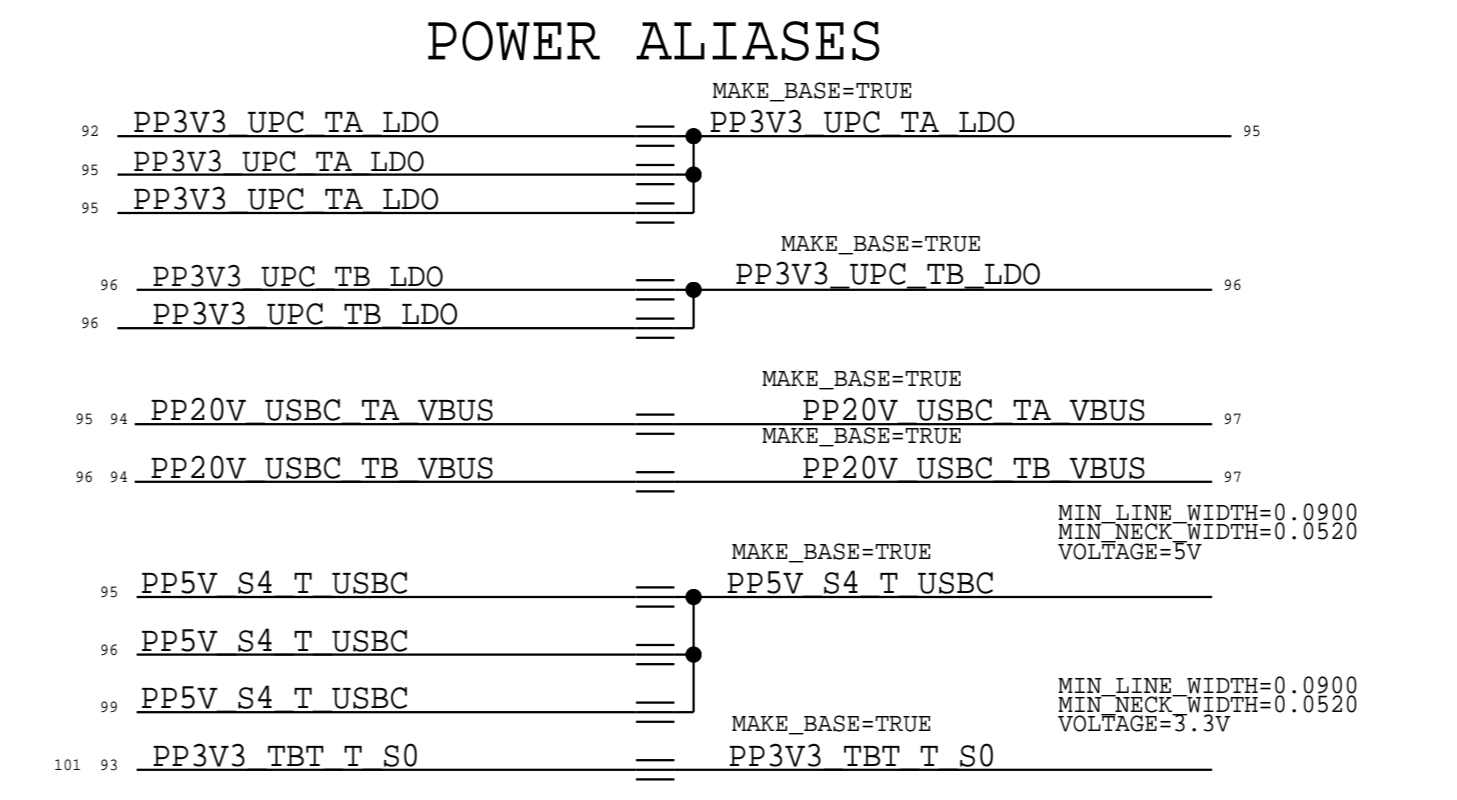
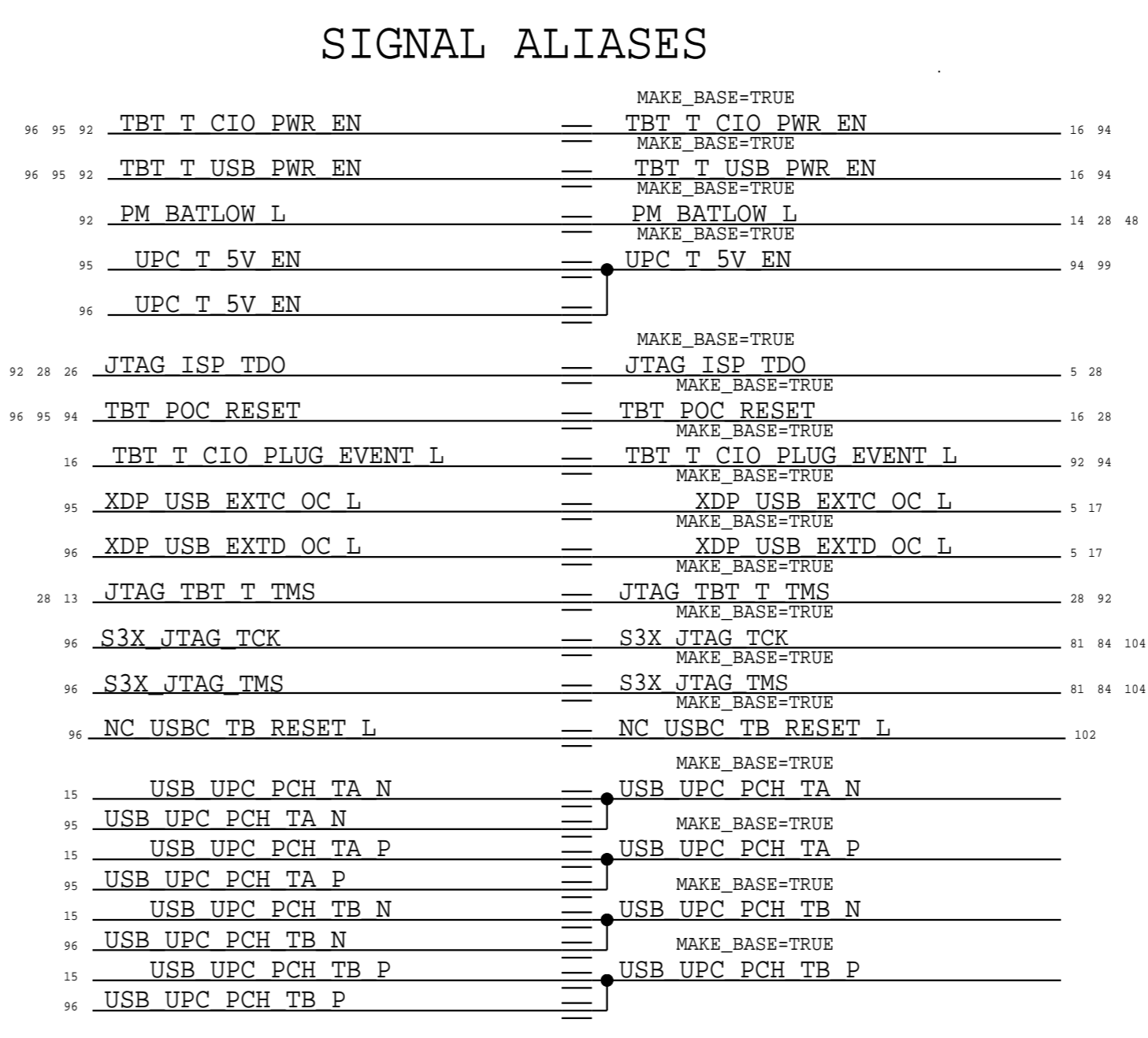
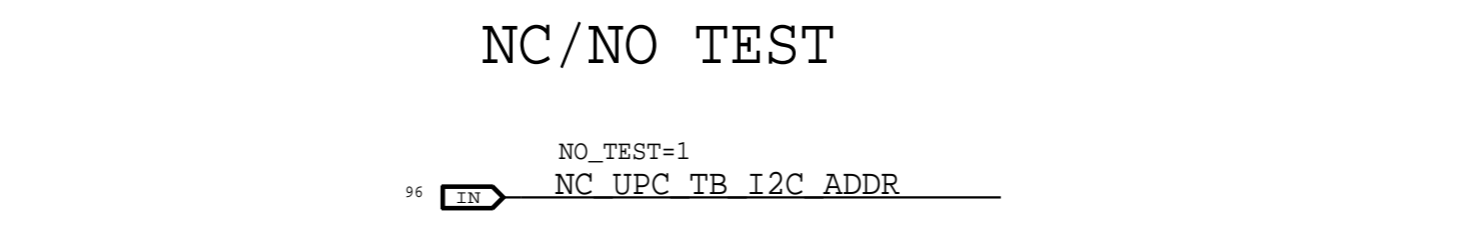
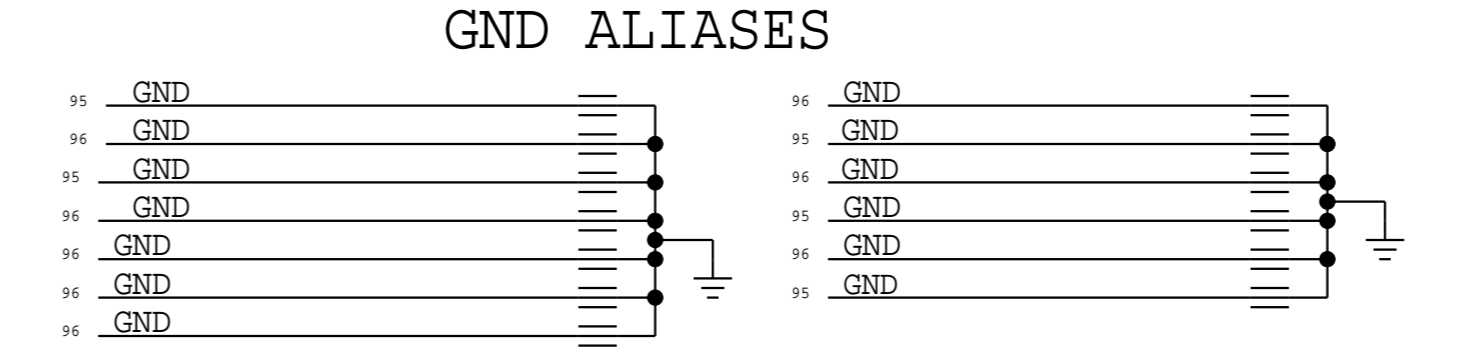
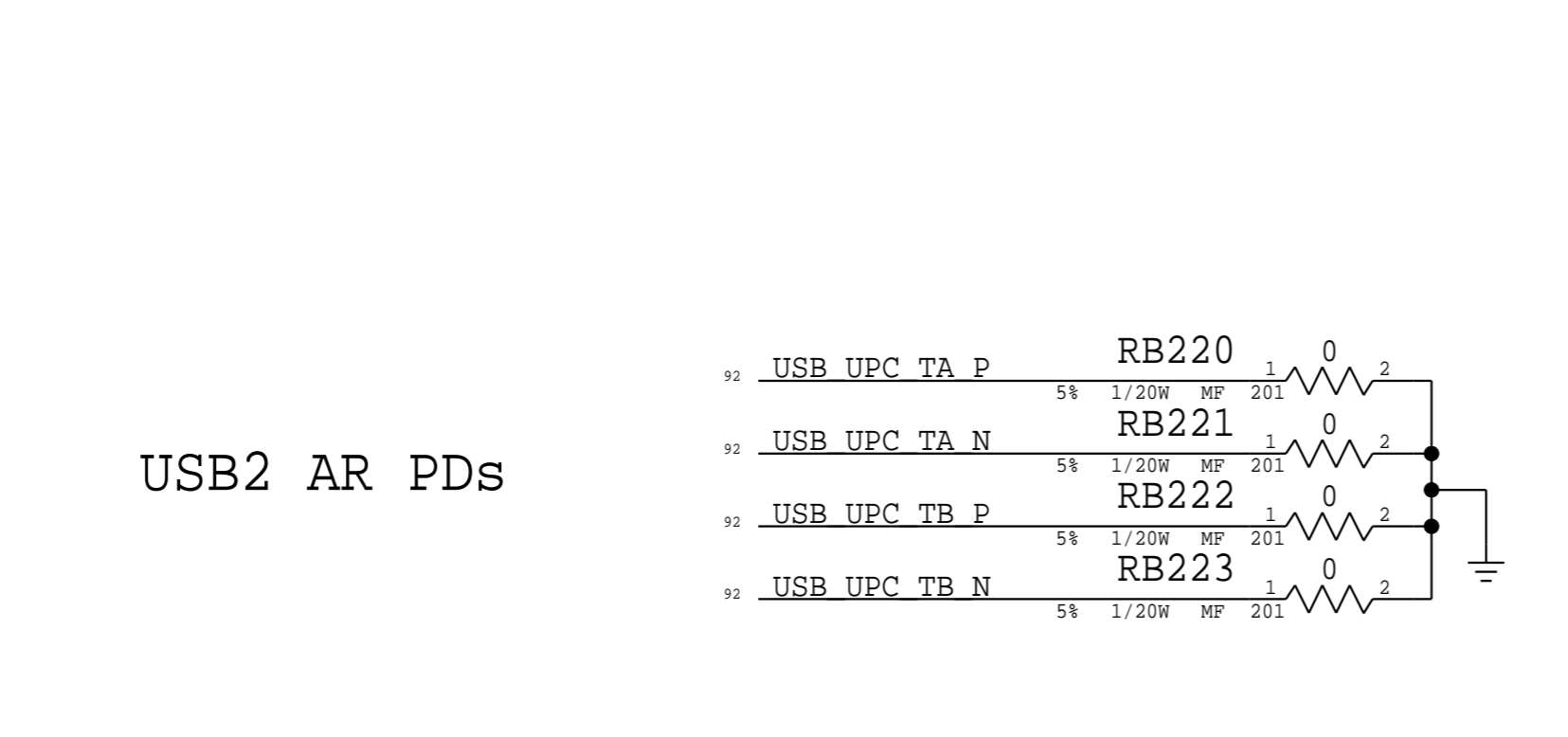
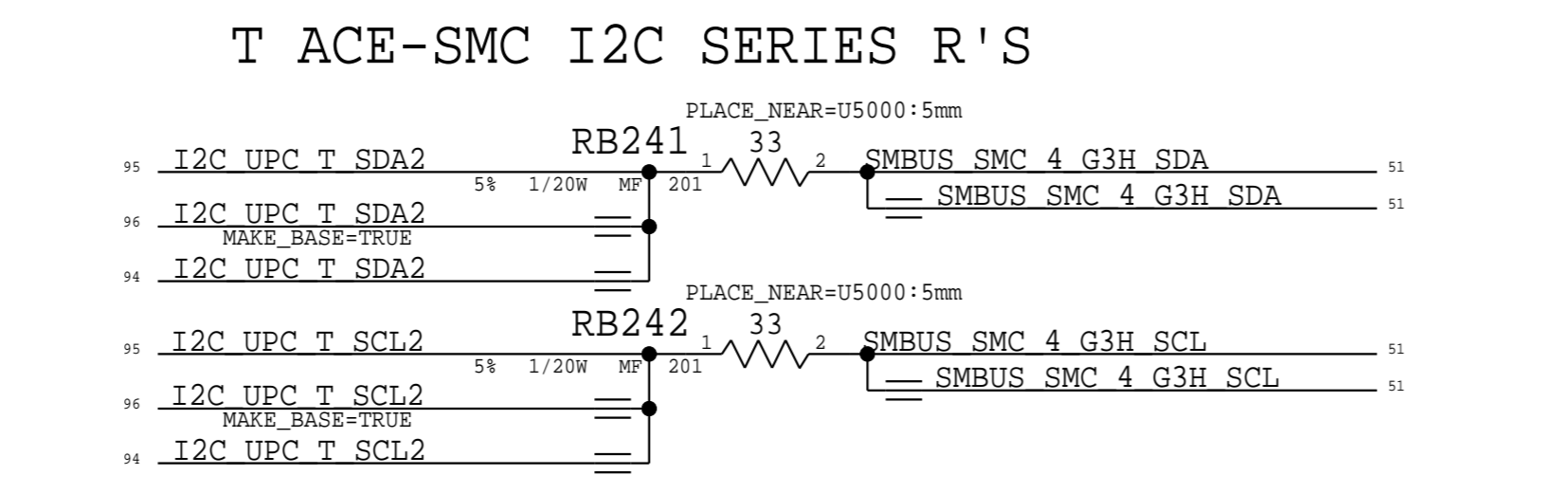
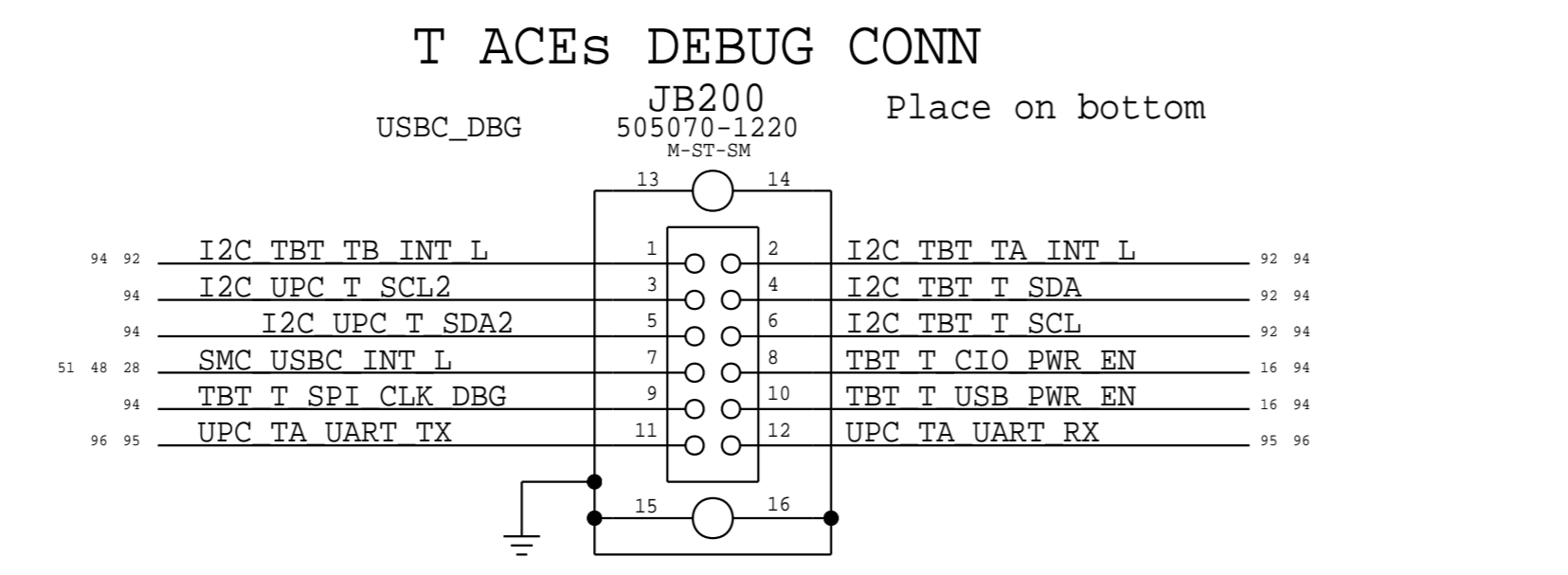
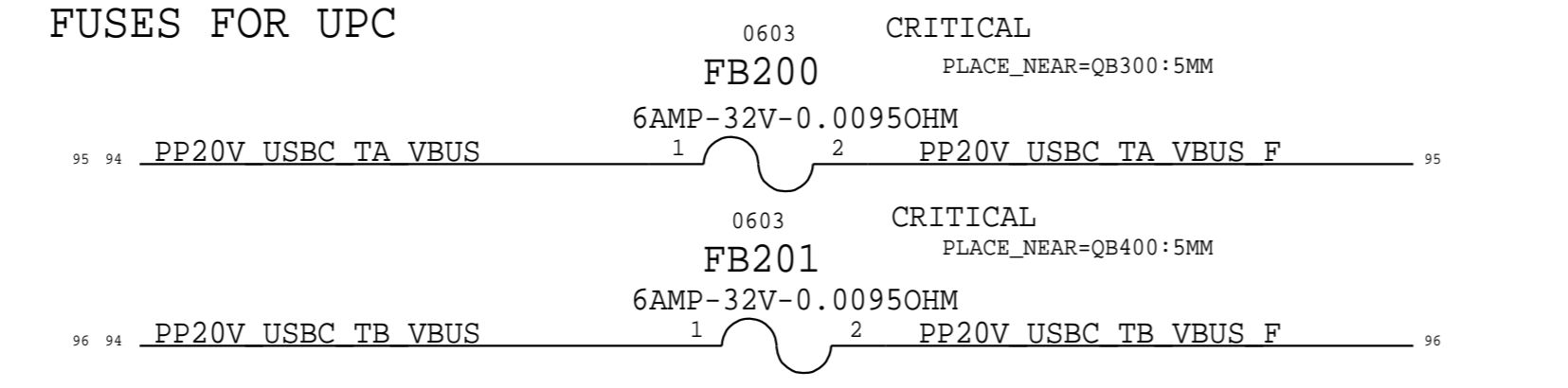
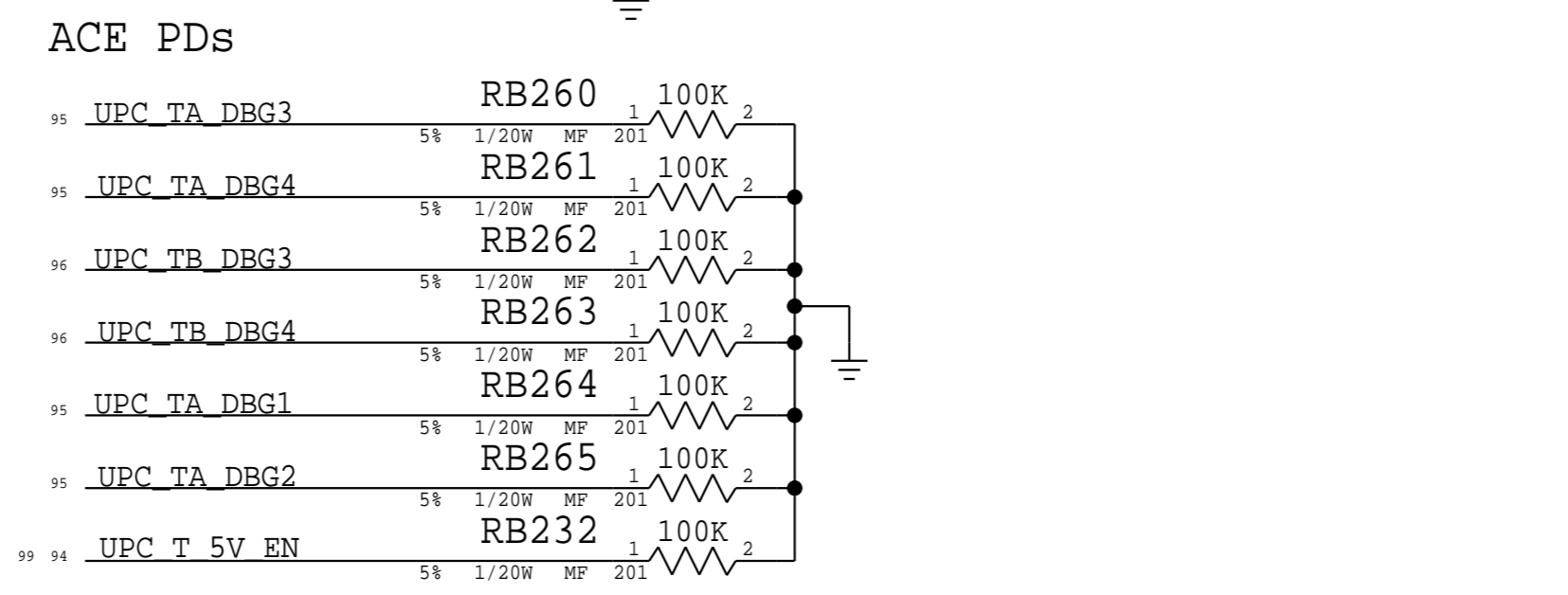
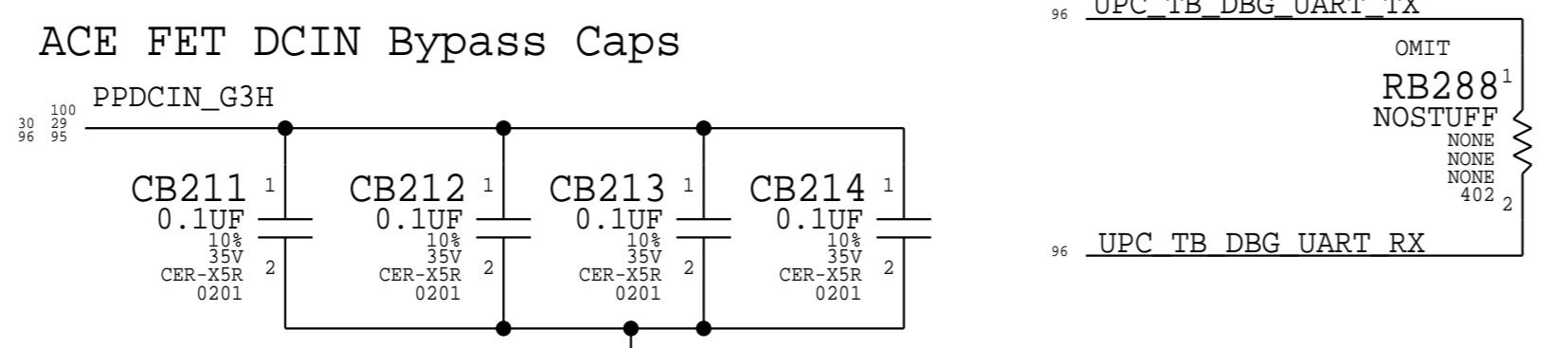
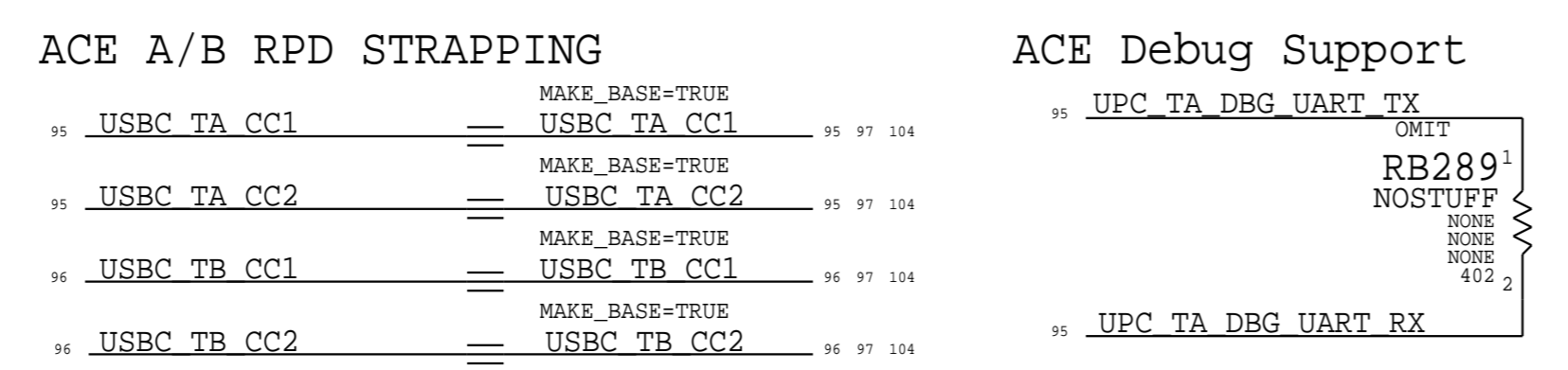
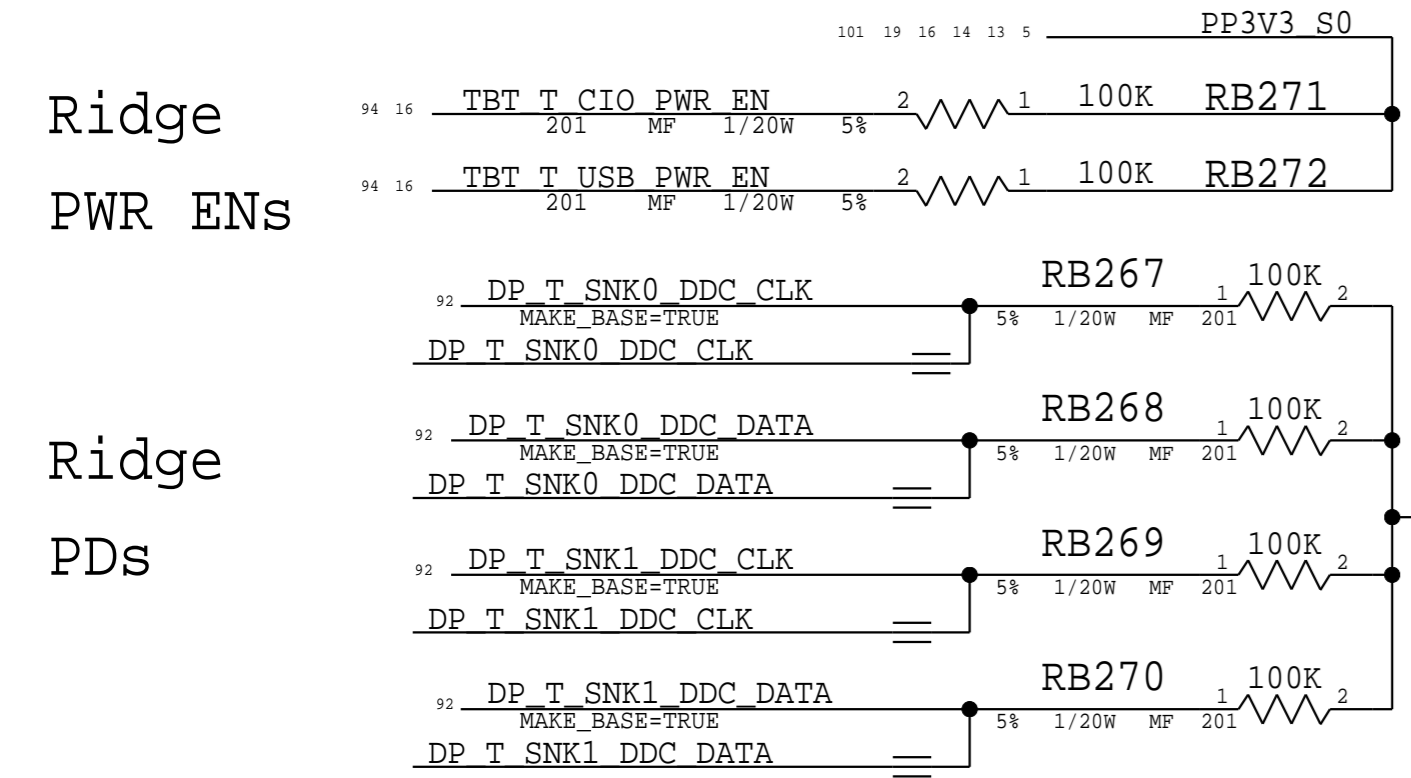
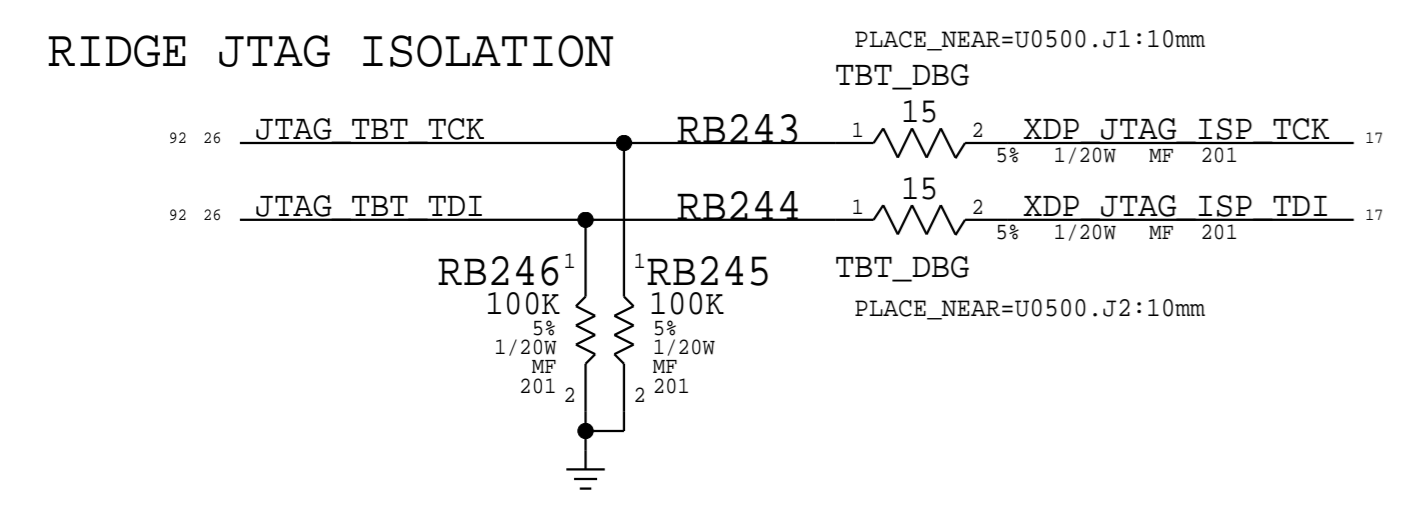
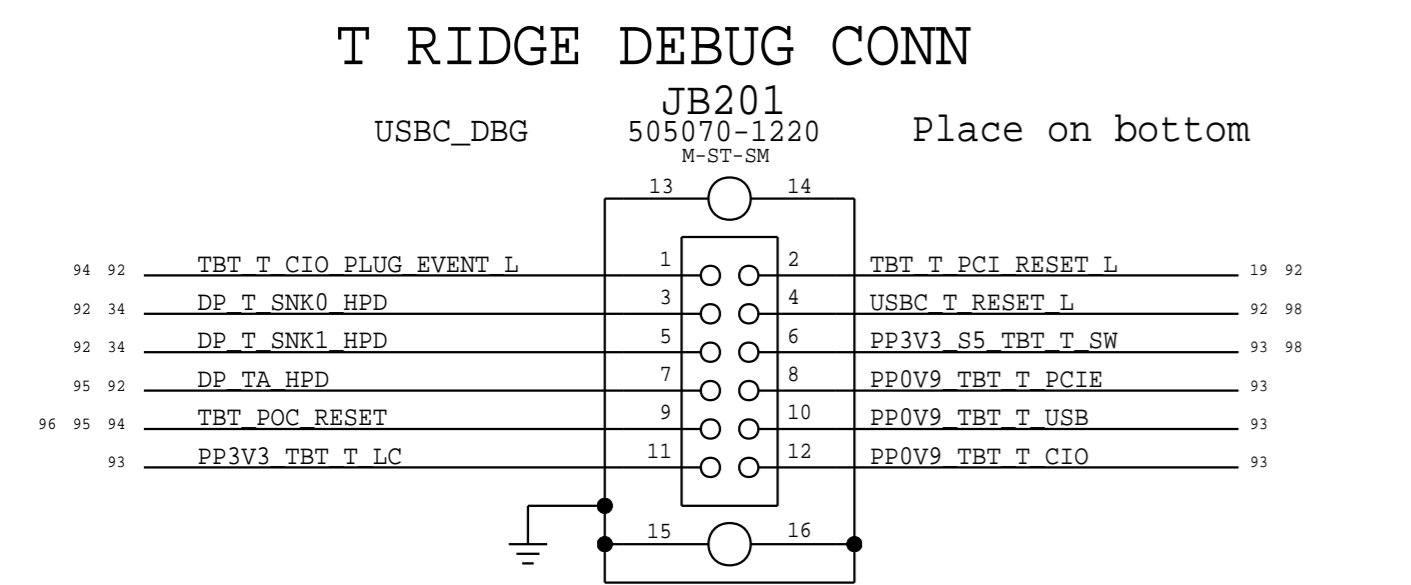
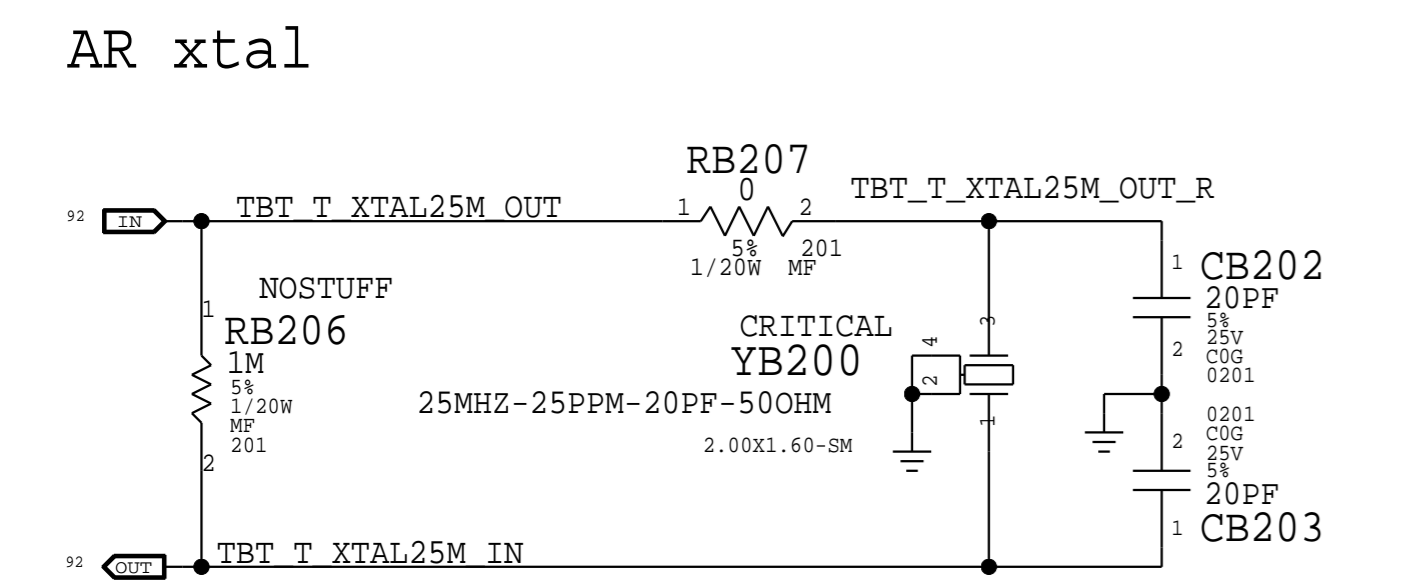
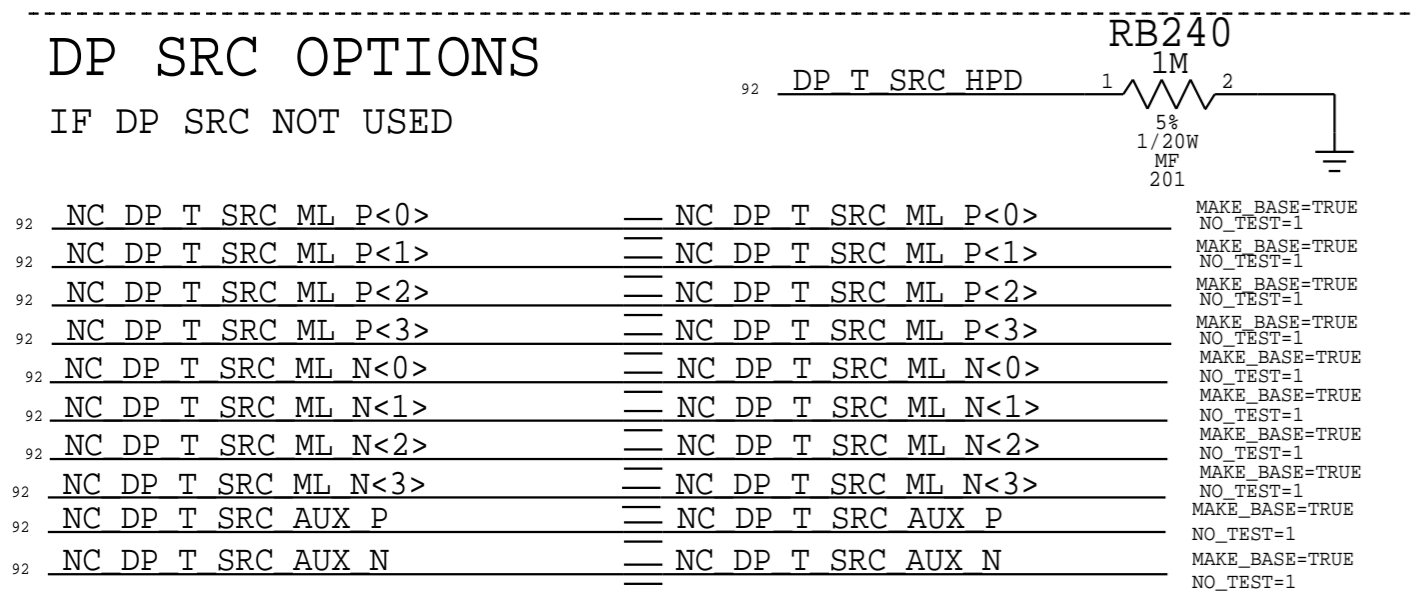
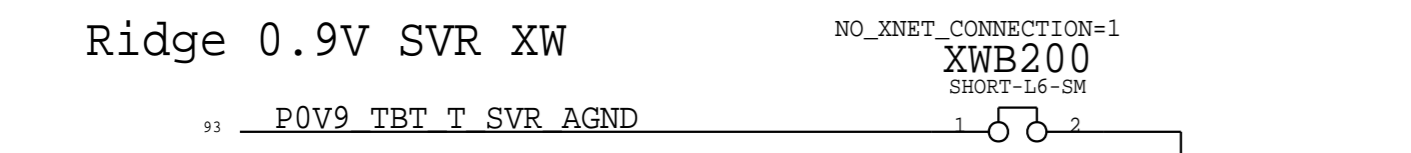
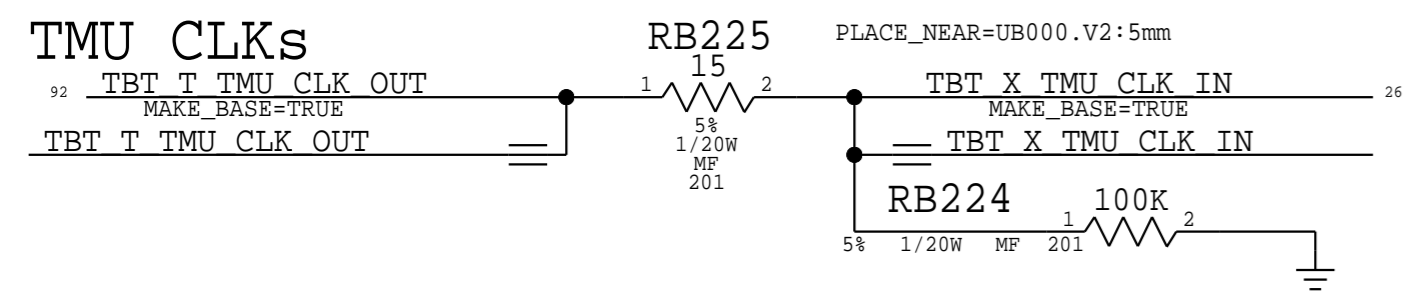
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REVISION	9.0.0	BRANCH	dvt-fab09-0
PAGE	110 OF 145	SHEET	92 OF 119

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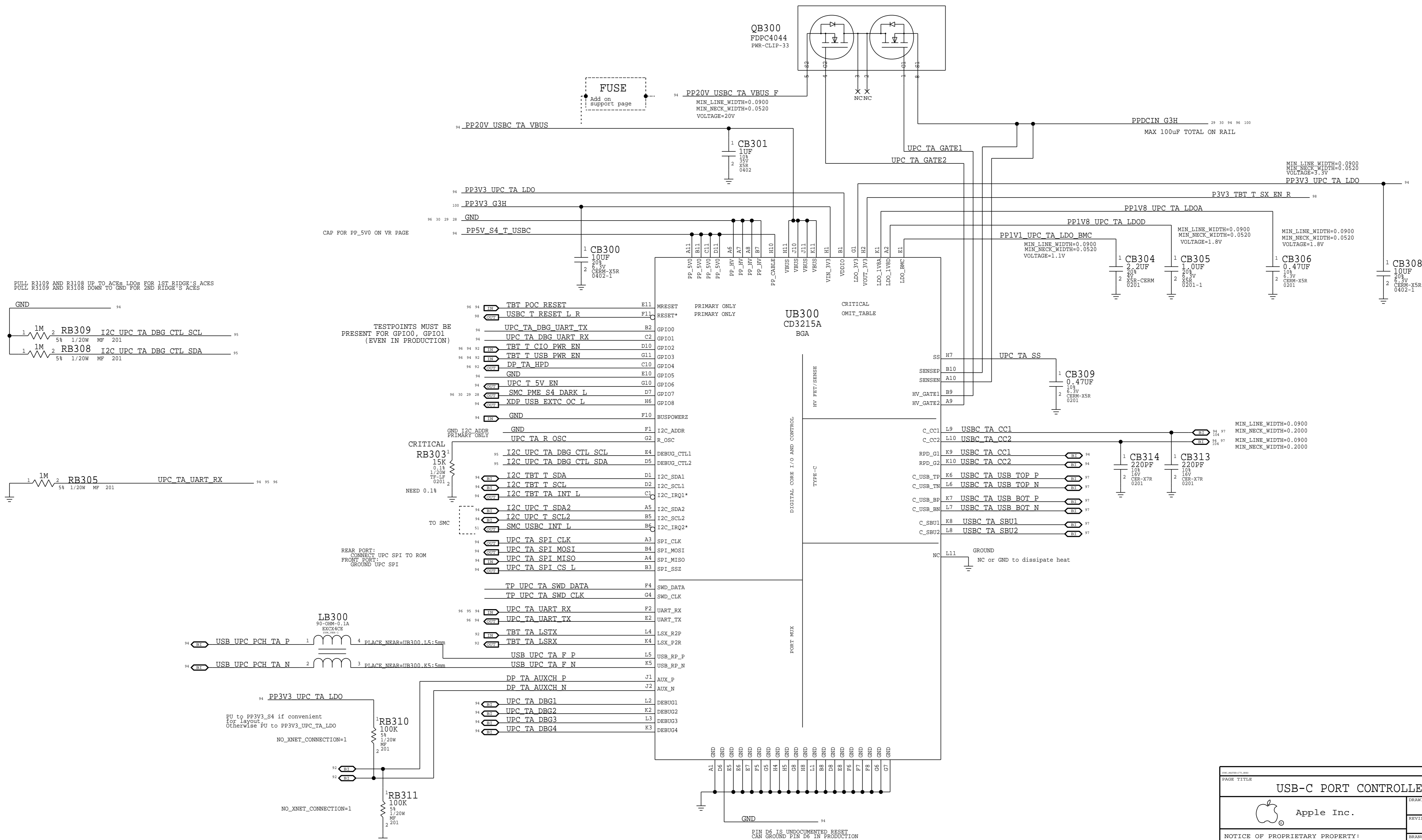
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Apple Inc.		051-00515	D
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		PAGE	111 OF 145
		SHEET	93 OF 119

BOM_COST_GROUP=TBT



PAGE TITLE		USB-C Support	
Apple Inc.		DRAWING NUMBER	051-00515
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		PAGE	112 OF 145
		SHEET	94 OF 119
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PRIMARY ACE USB-C PORT CONTROLLER (UPC)

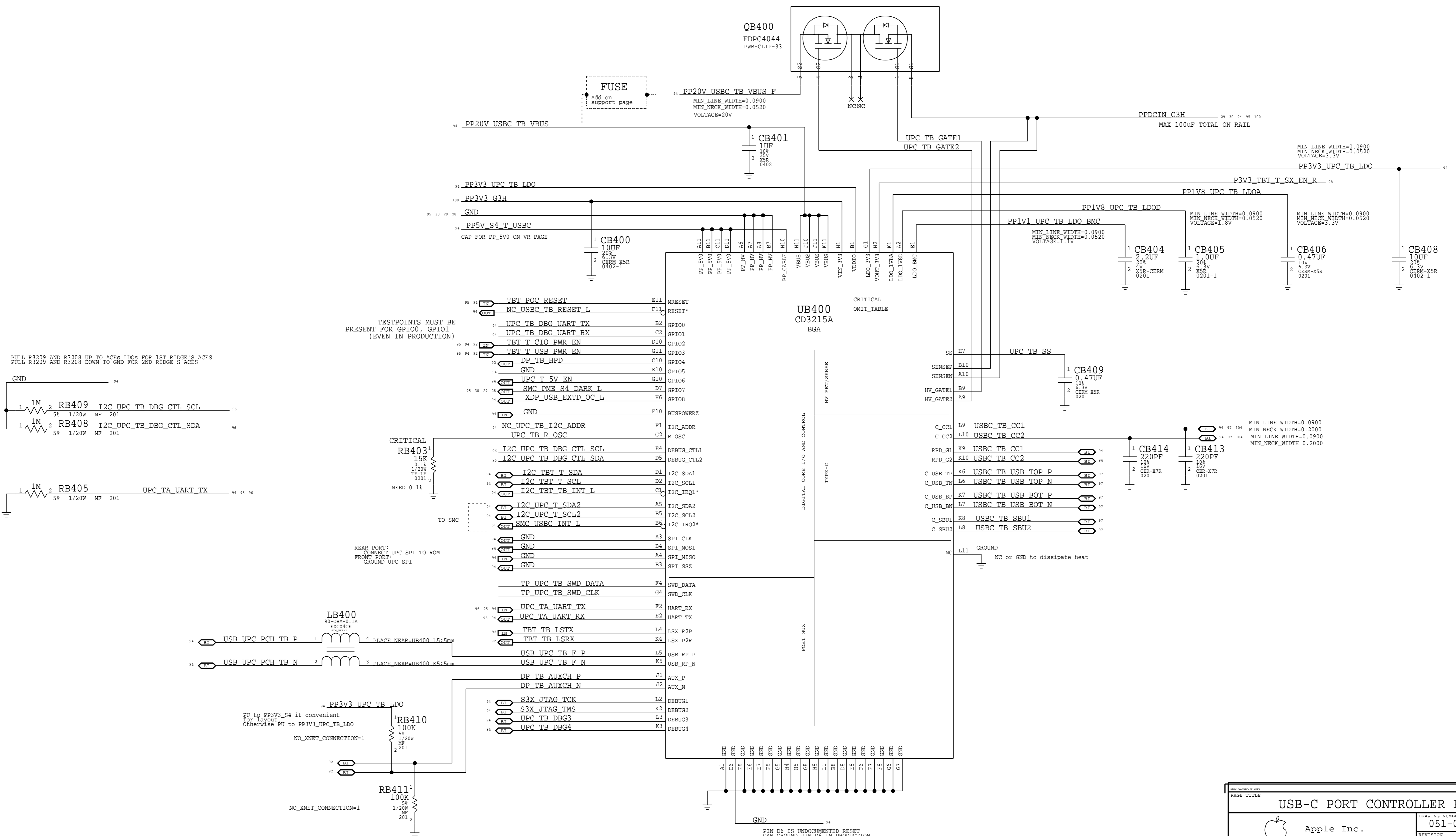


PAGE TITLE		
USB-C PORT CONTROLLER A		
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	PAGE	113 OF 145
	SHEET	95 OF 119

BOM_COST_GROUP=USB-C

PIN D6 IS UNDOCUMENTED RESET CAN GROUND PIN D6 IN PRODUCTION

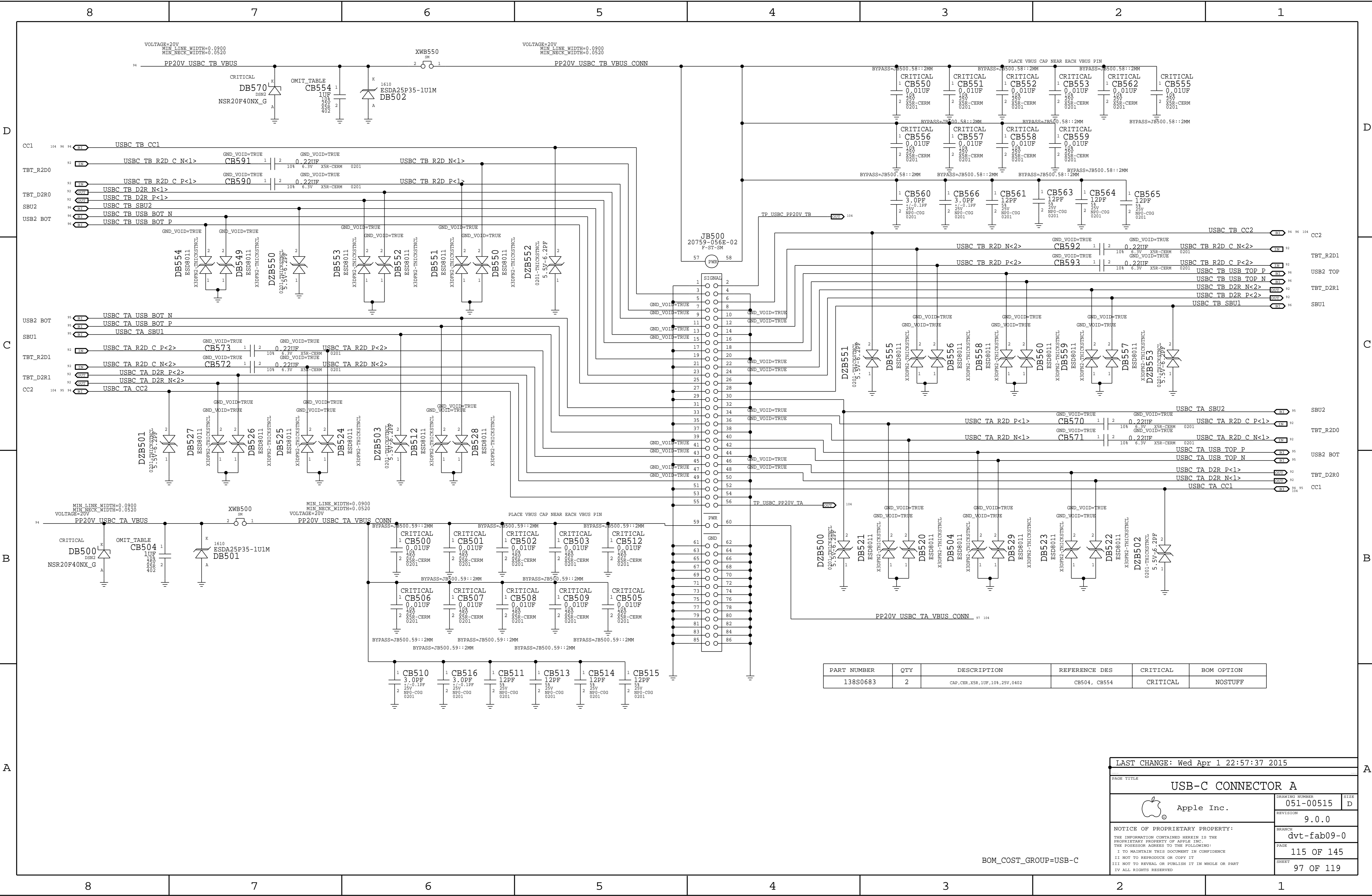
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



USB-C PORT CONTROLLER B		
DRAWING NUMBER 051-00515	SIZE D	
REVISION 9.0.0		
BRANCH dvt-fab09-0		
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BOM_COST_GROUP=USB-C



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP, CER, XSR, 1UF, 10%, 25V, 0402	CB504, CB554	CRITICAL	NOSTUFF

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: **USB-C CONNECTOR A**

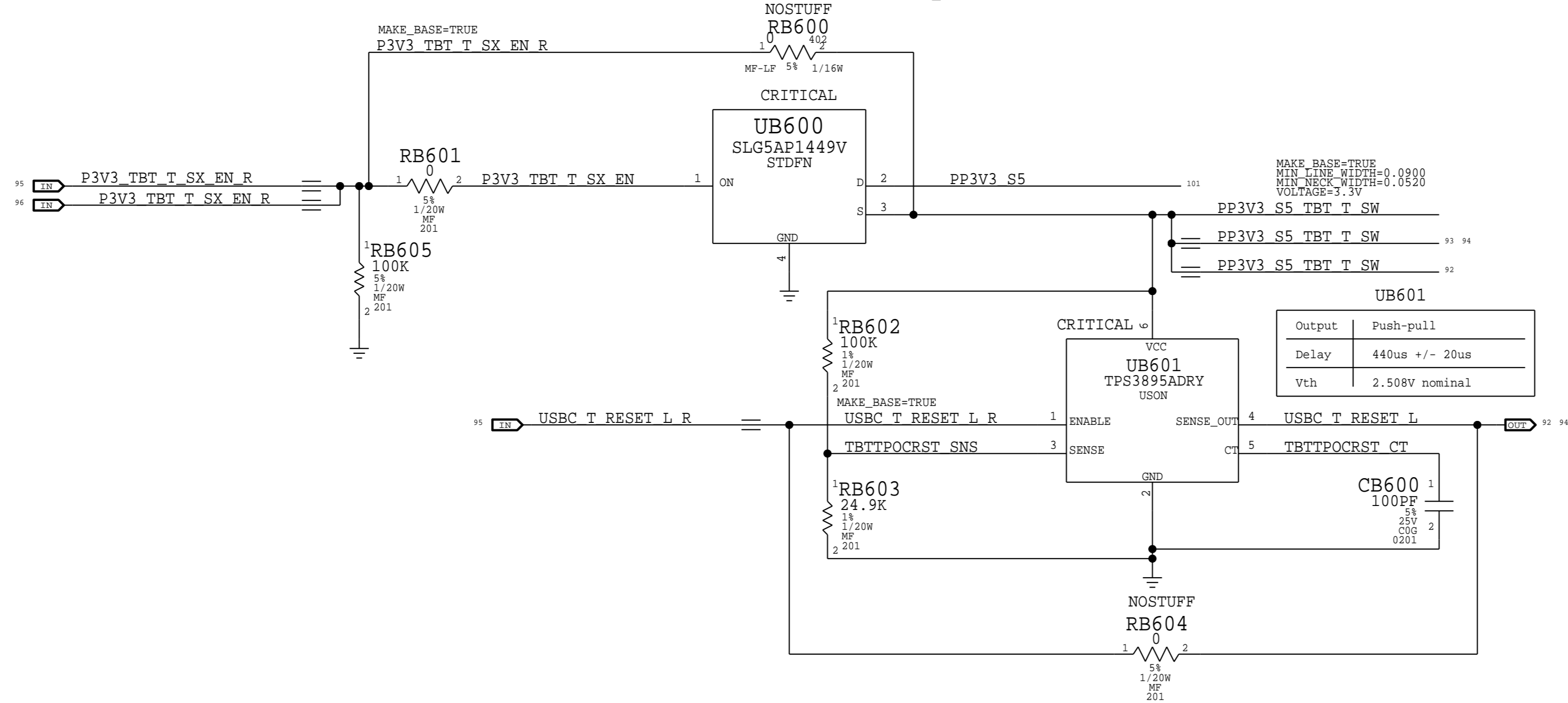
Apple Inc.

DRAWING NUMBER	051-00515	SIZE	D
REVISION	9.0.0	BRANCH	dvt-fab09-0
PAGE	115 OF 145	SHEET	97 OF 119

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BOM_COST_GROUP=USB-C

TBT T "POC" Power-up Reset

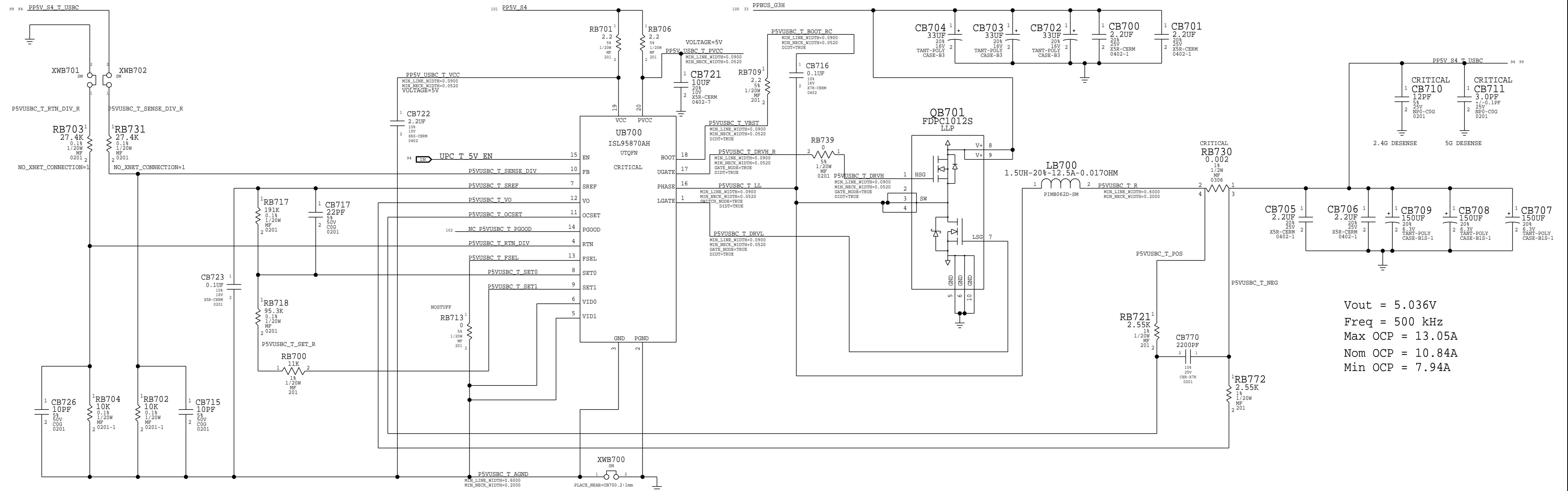


BOM_COST_GROUP=USB-C

DESIGN: j130/dev_mlb_u
 LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: **USB-C CONNECTOR B**

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	PAGE	116 OF 145		
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Vout = 5.036V
 Freq = 500 kHz
 Max OCP = 13.05A
 Nom OCP = 10.84A
 Min OCP = 7.94A

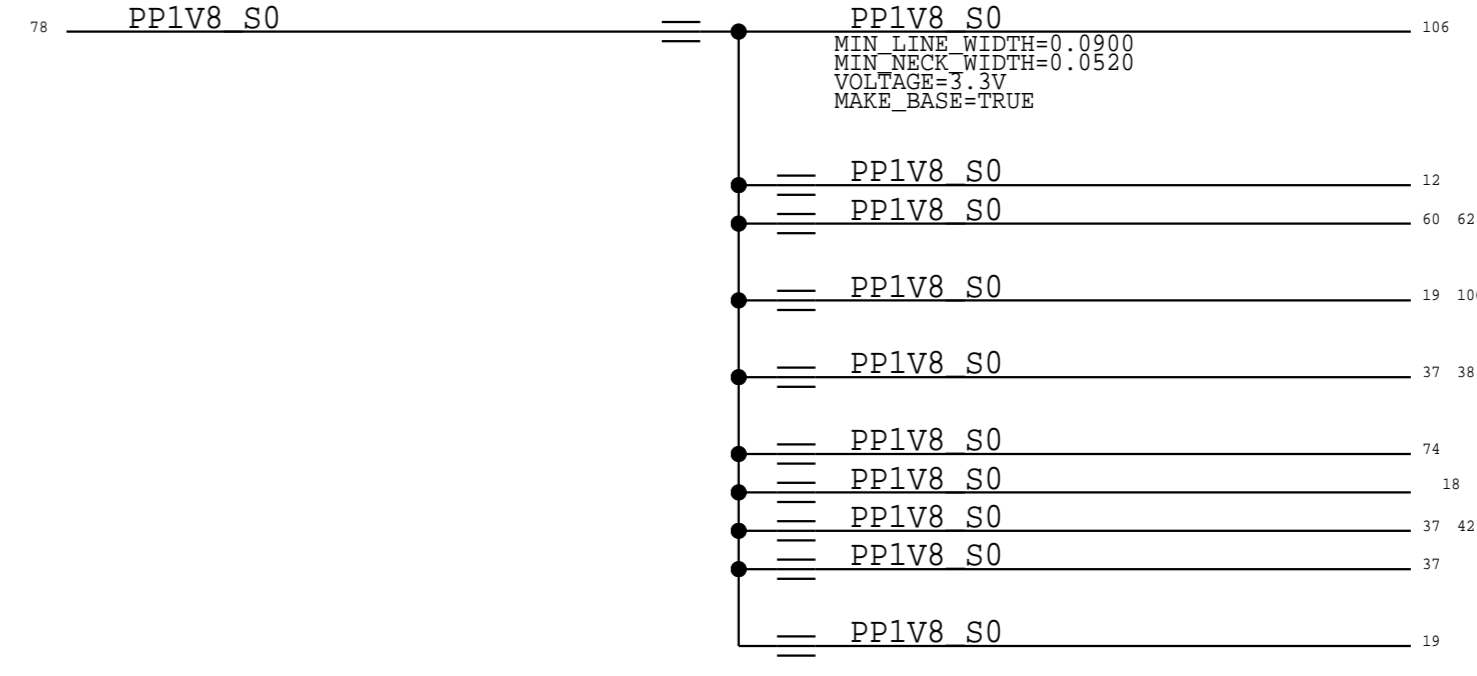
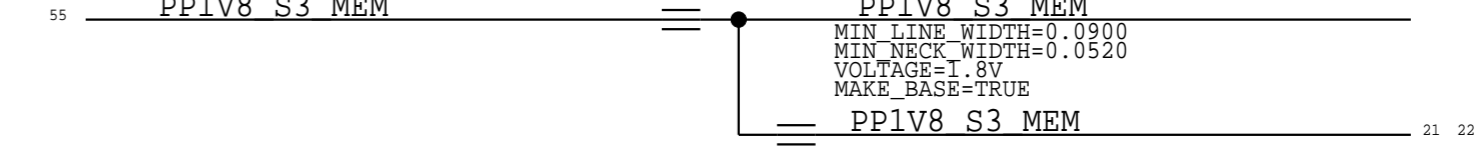
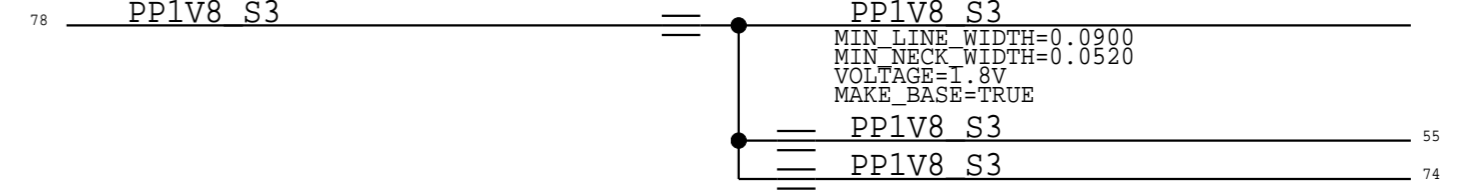
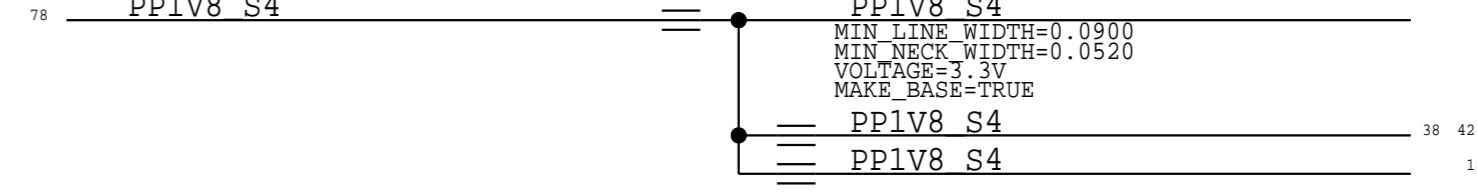
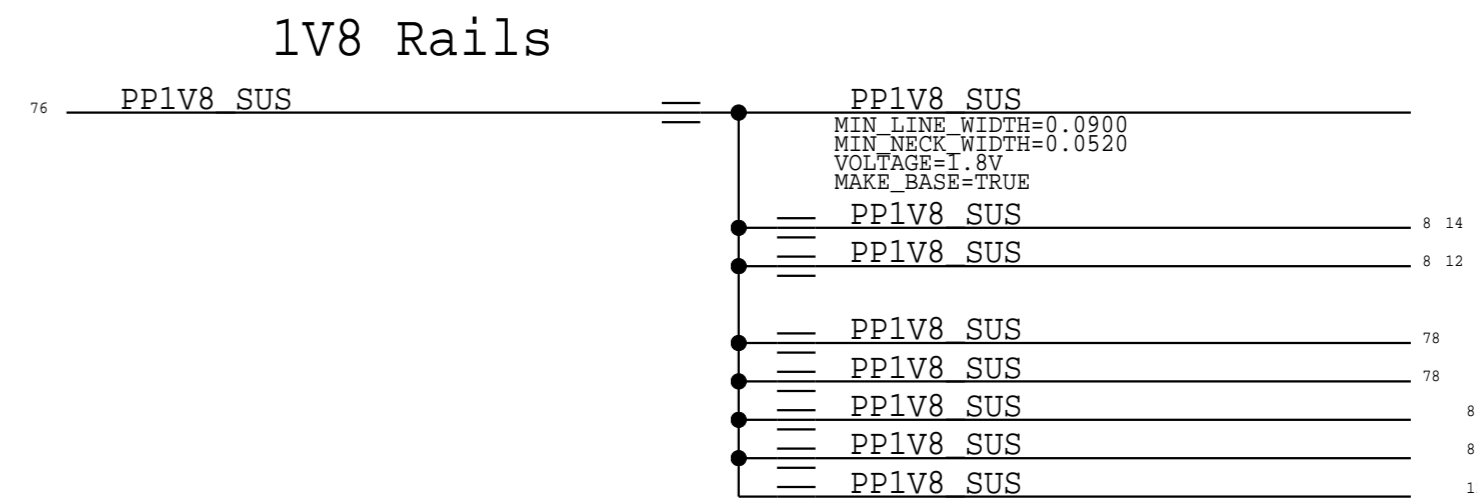
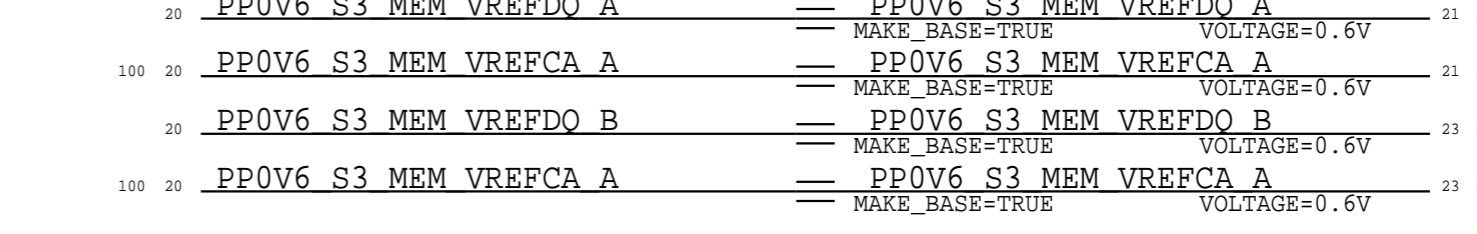
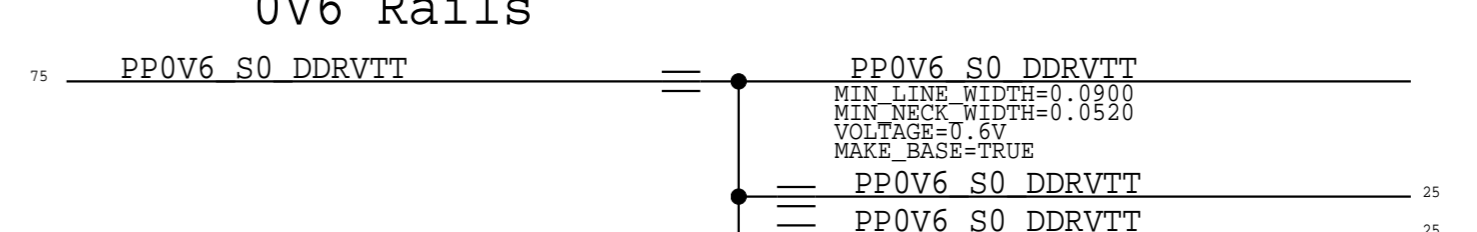
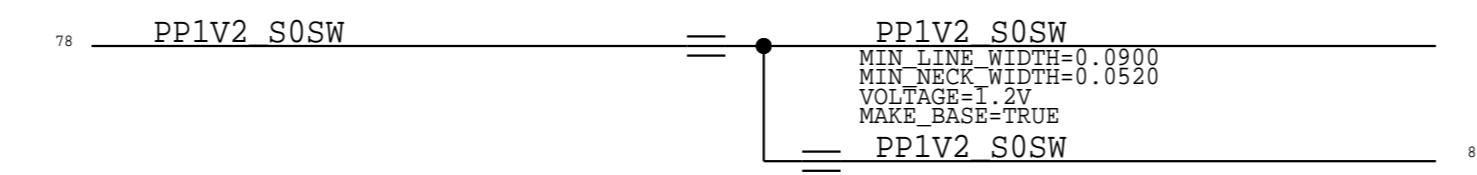
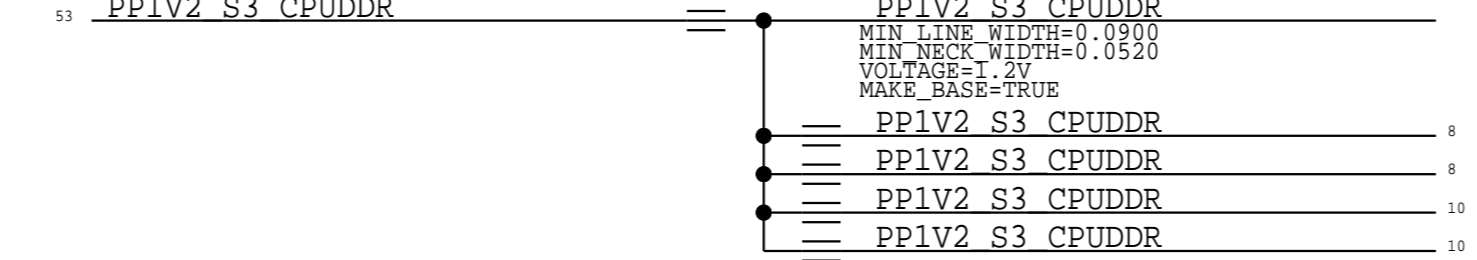
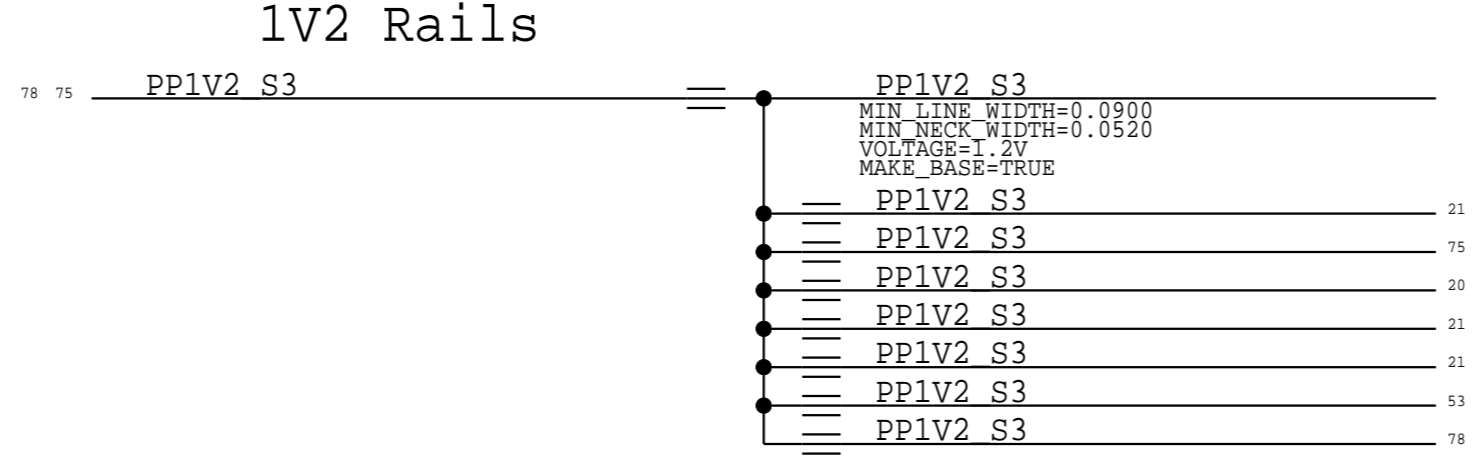
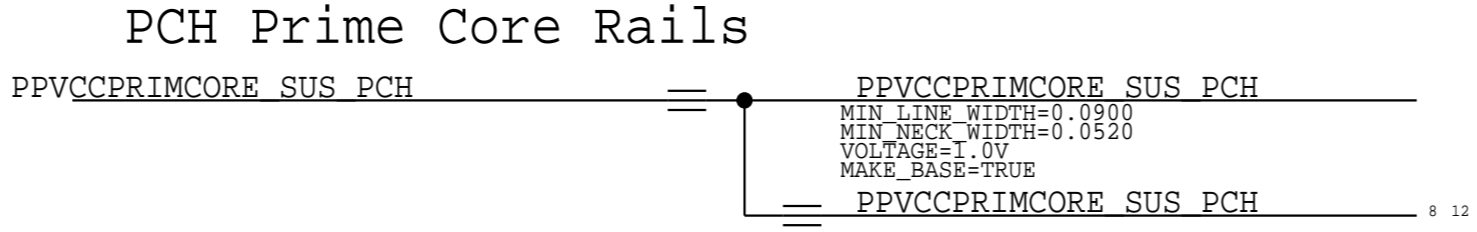
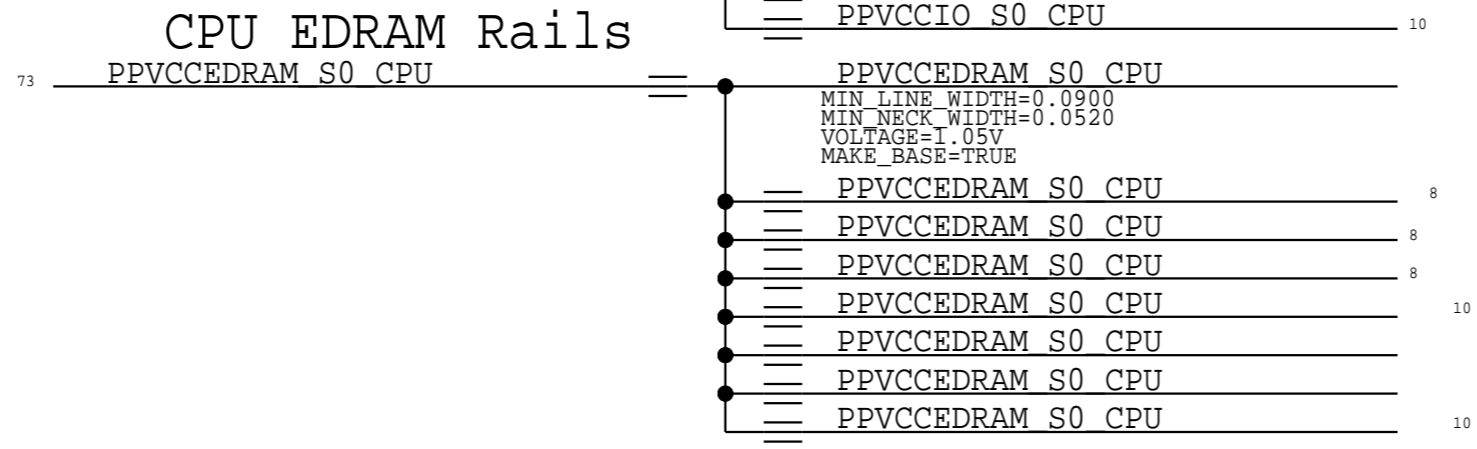
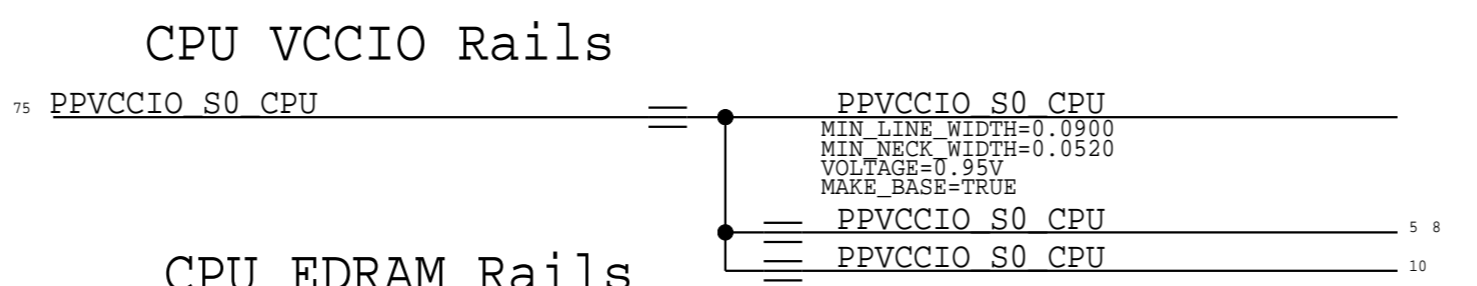
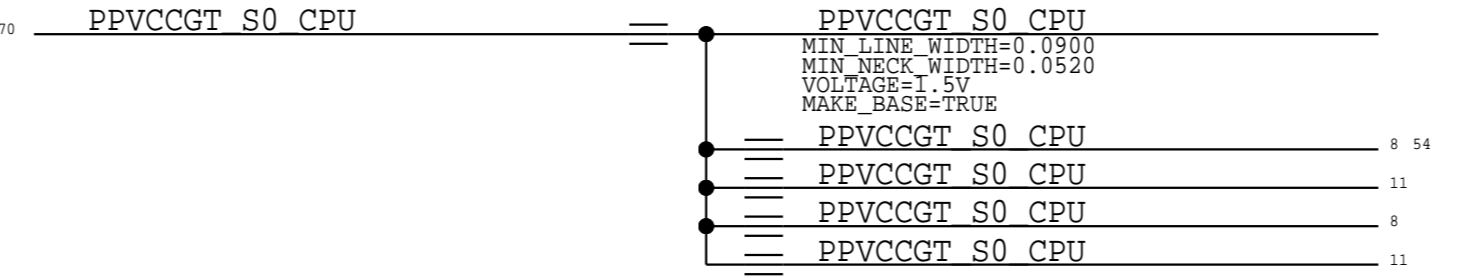
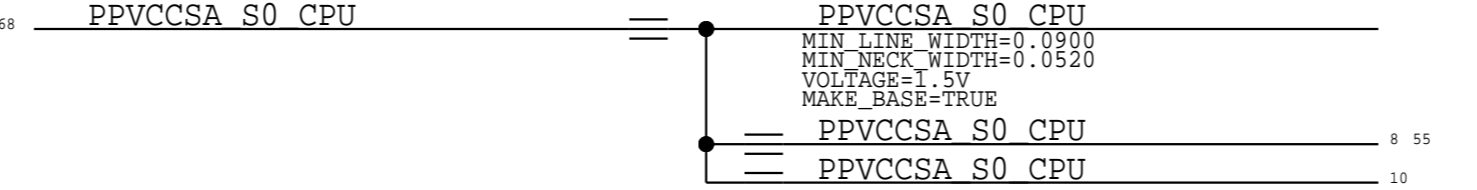
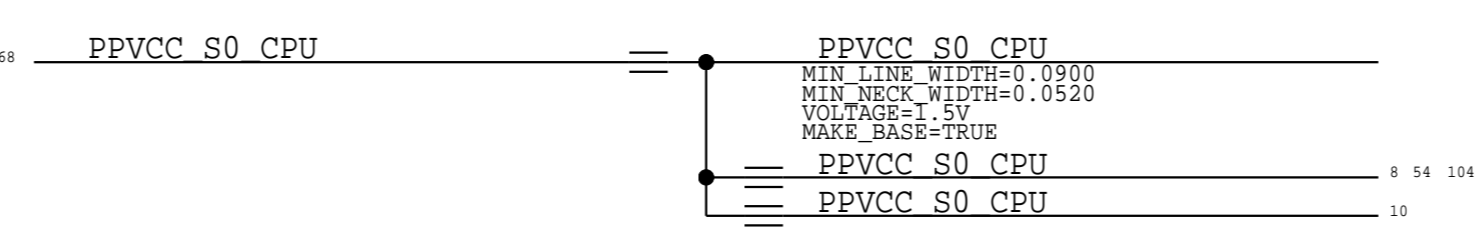
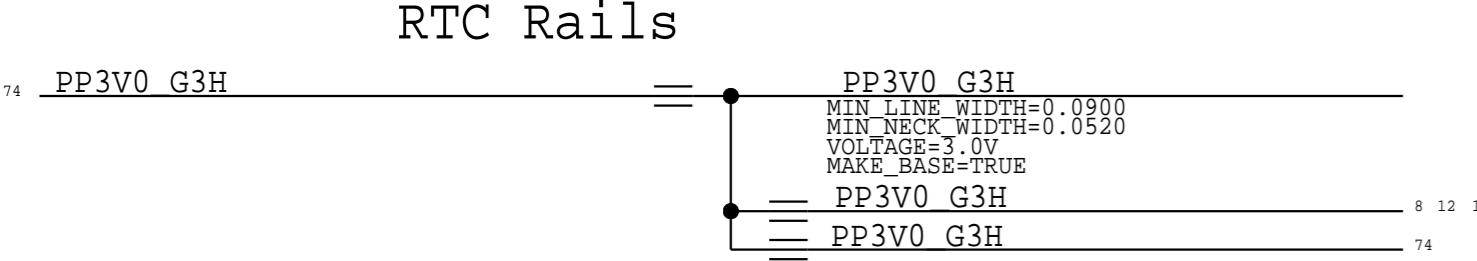
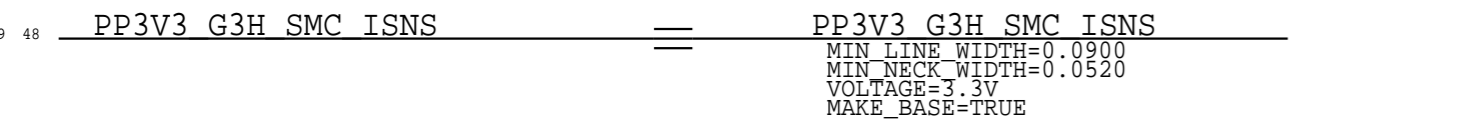
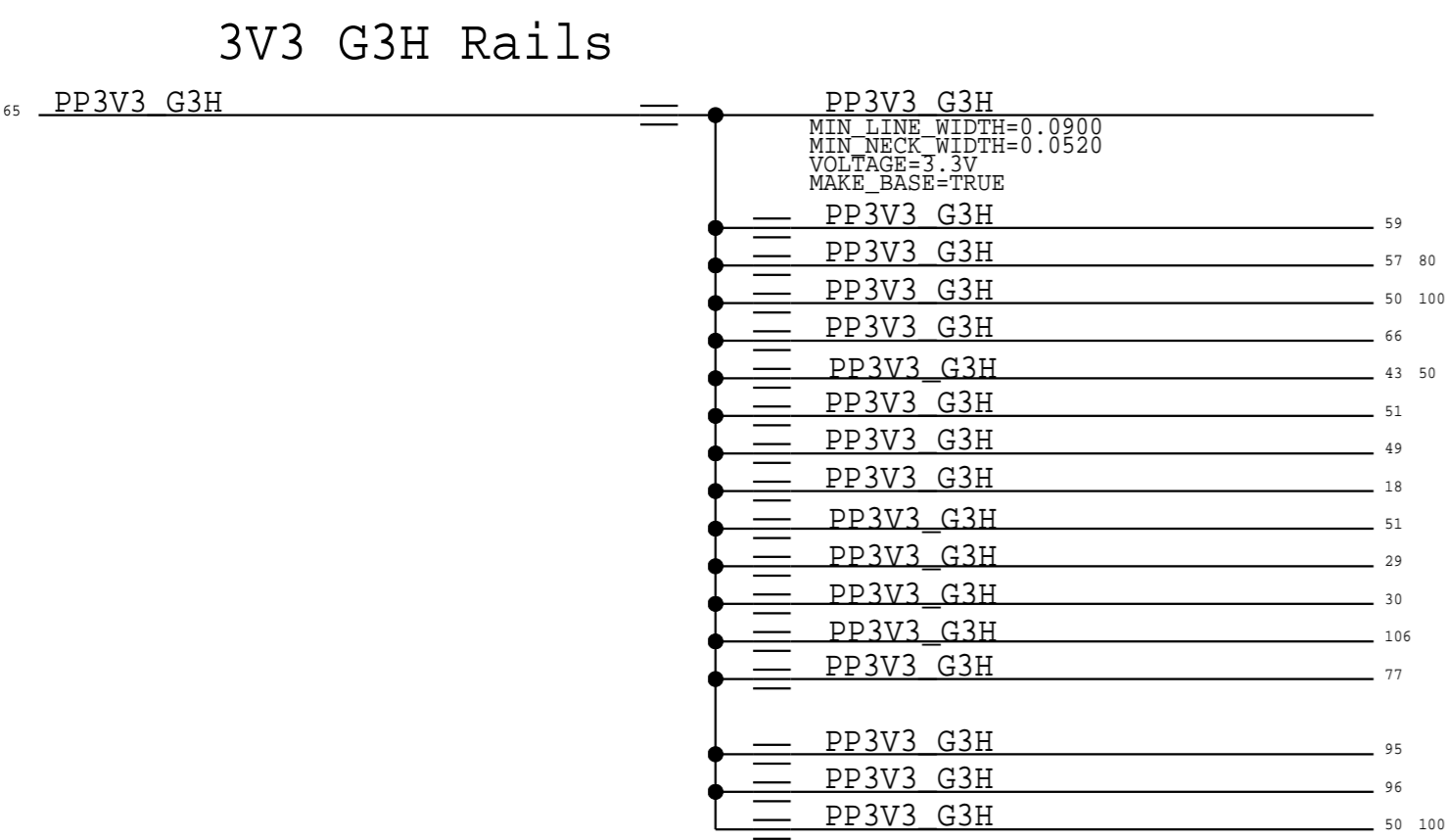
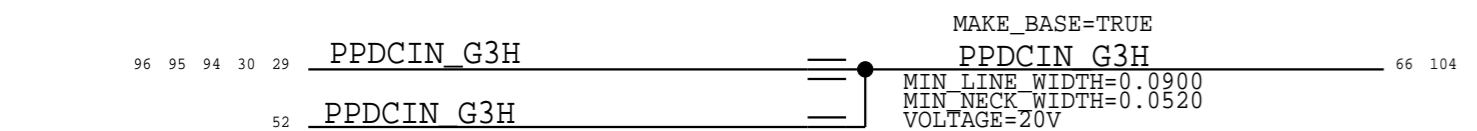
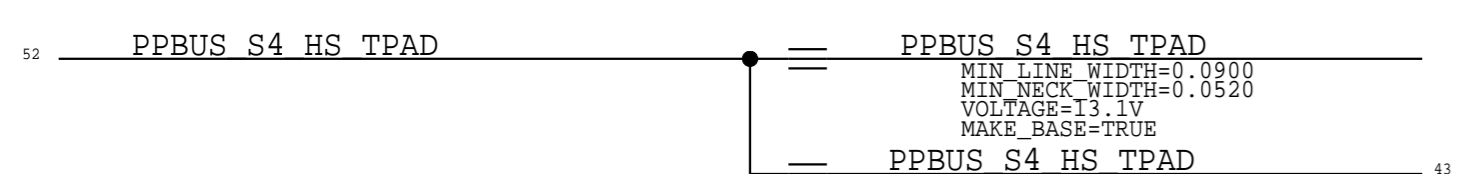
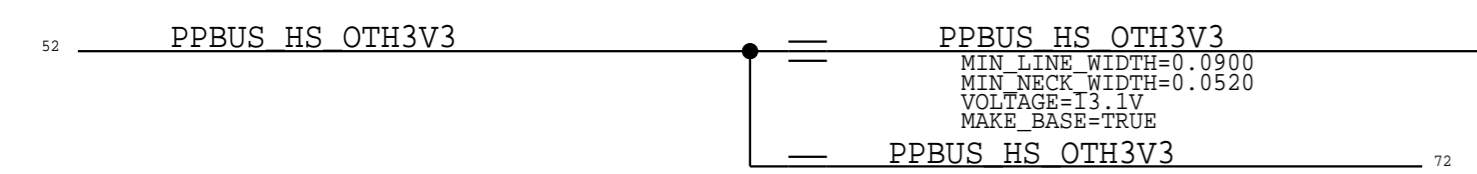
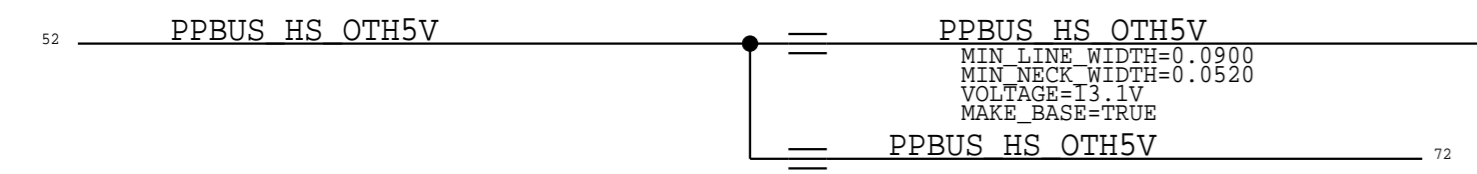
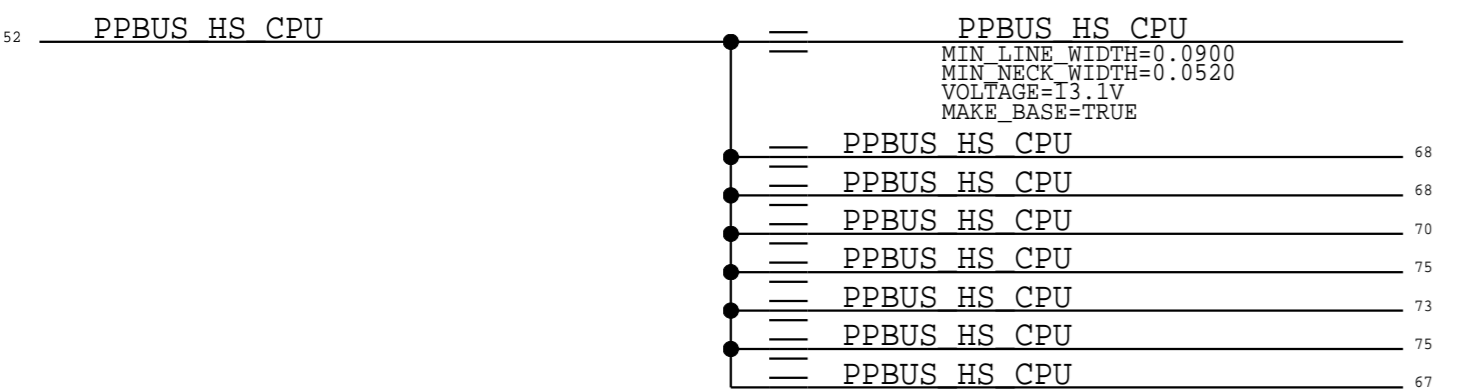
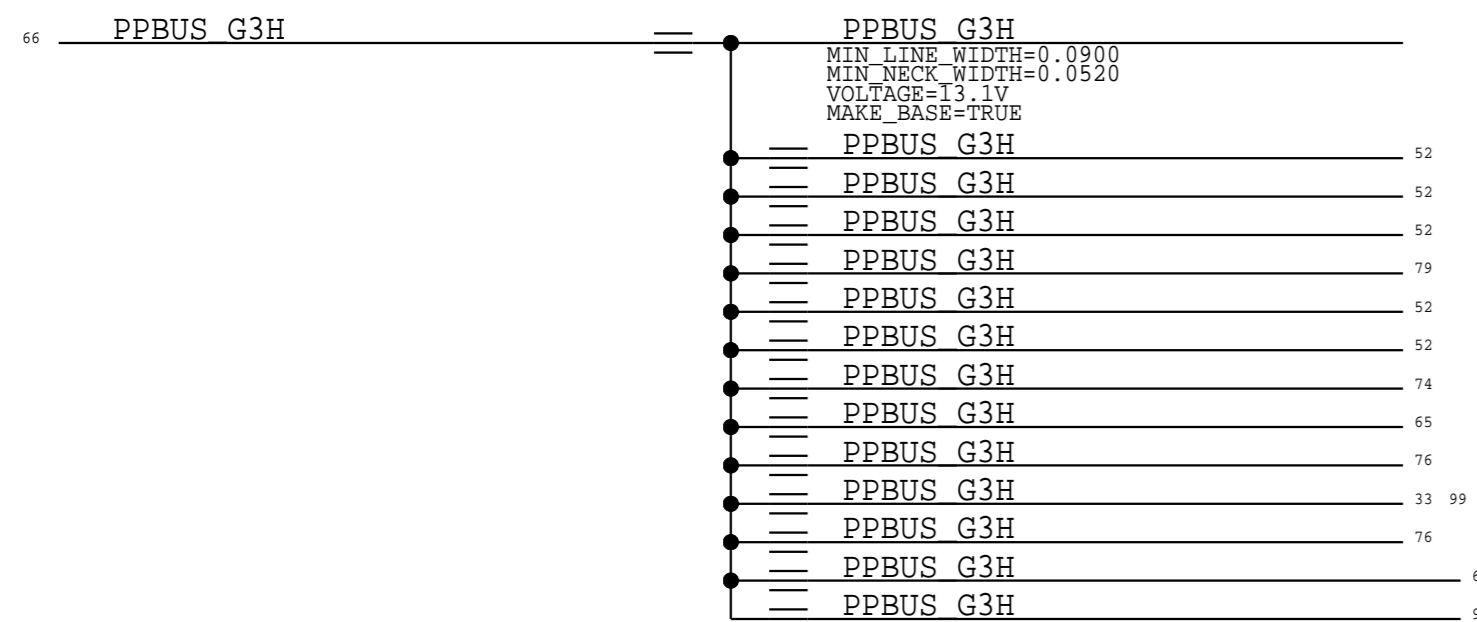
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PAGE TITLE TBT 5V REGULATOR		
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PBUS Rails

IMVP Rails

OV6 Rails



PAGE TITLE Power Aliases - 1		
	DRAWING NUMBER 051-00515	STEP D
	REVISION 9.0.0	
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BRANCH dvt-fab09-0	PAGE 120 OF 145	SHEET 100 OF 119

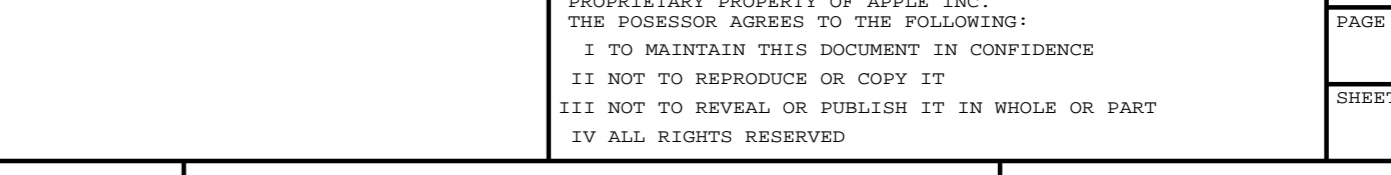
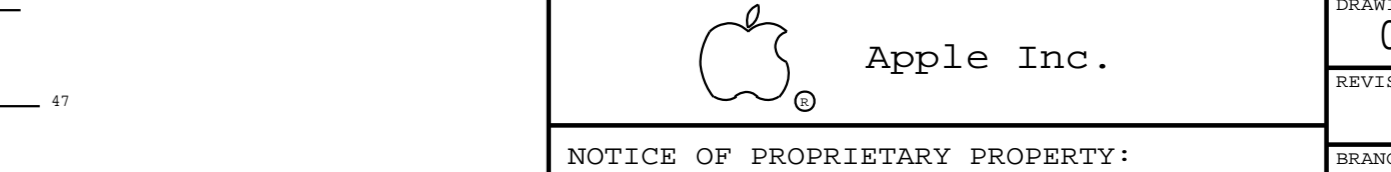
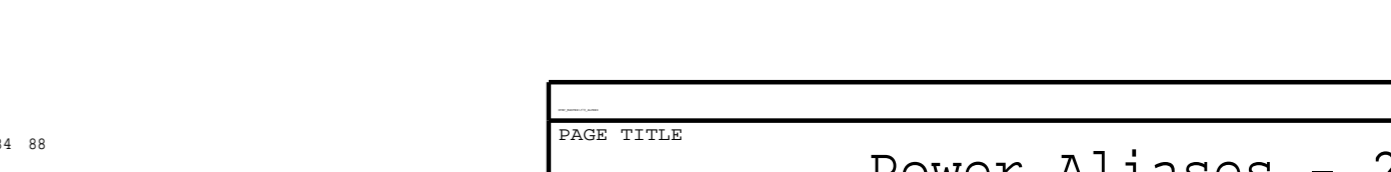
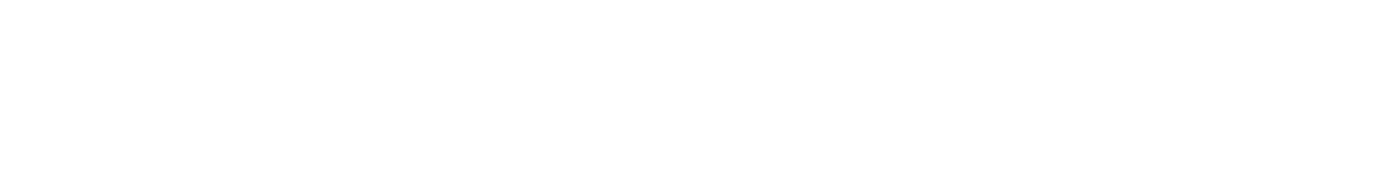
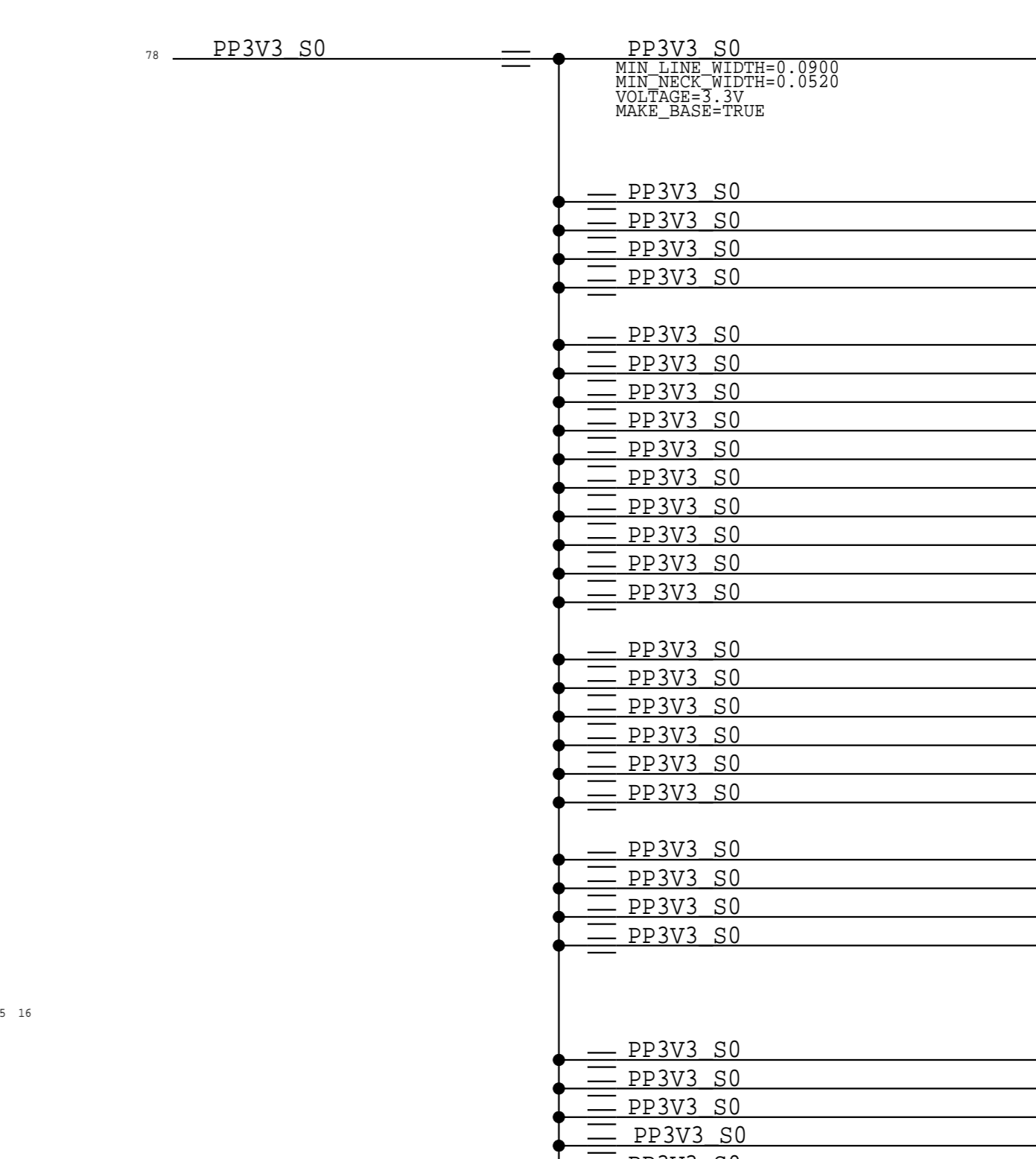
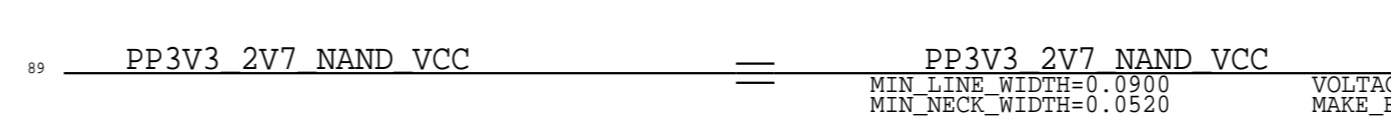
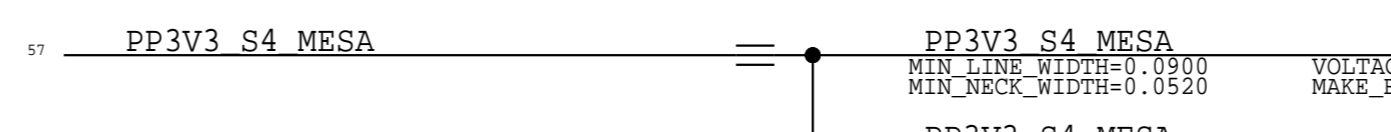
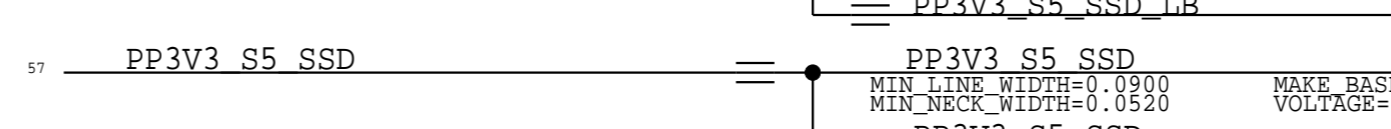
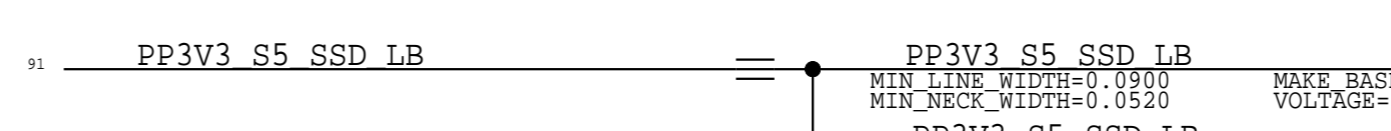
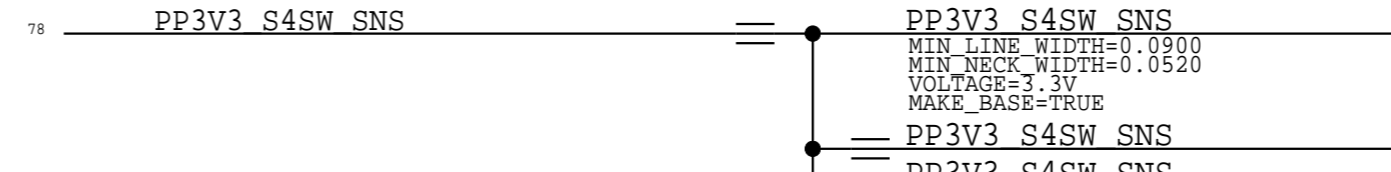
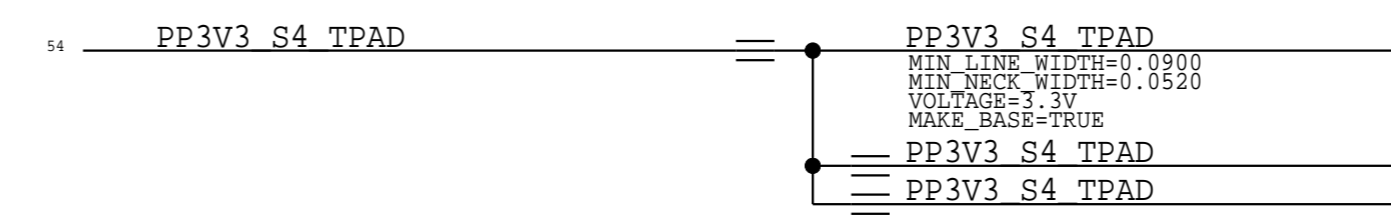
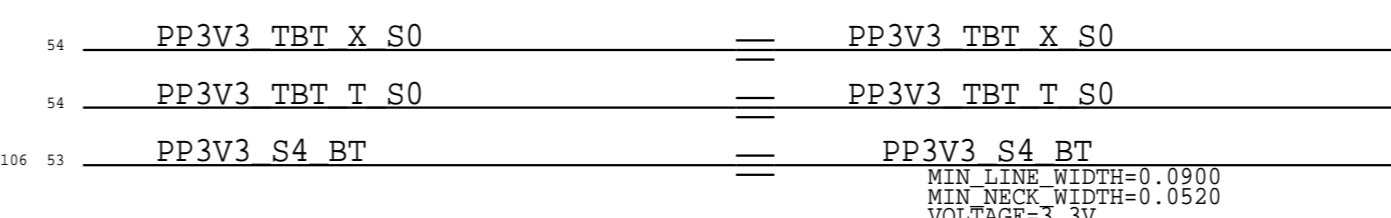
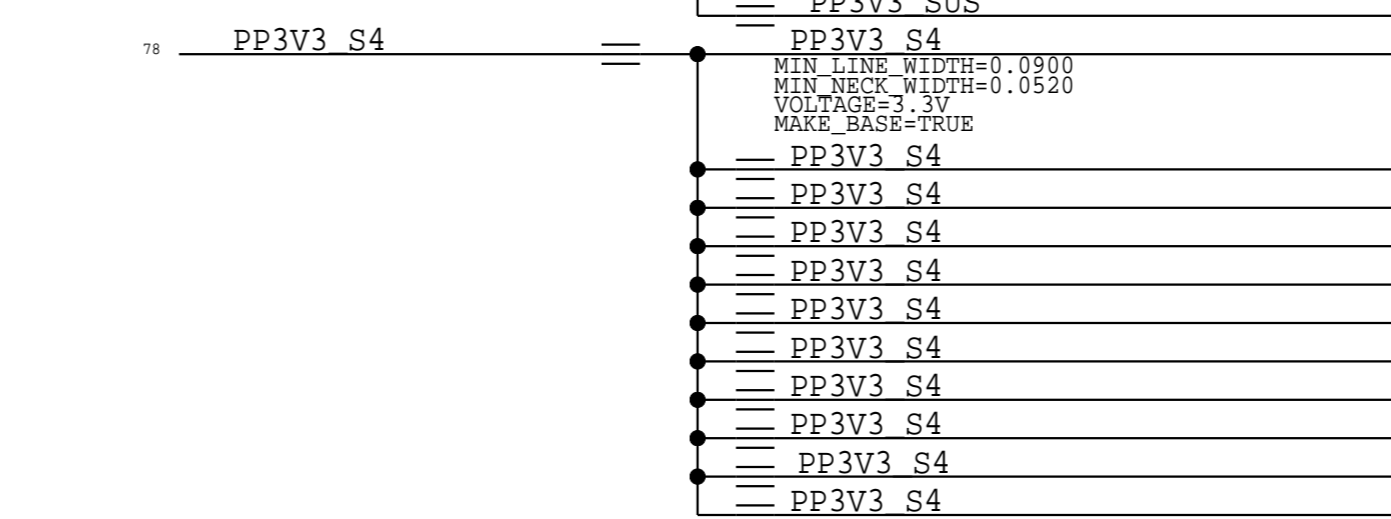
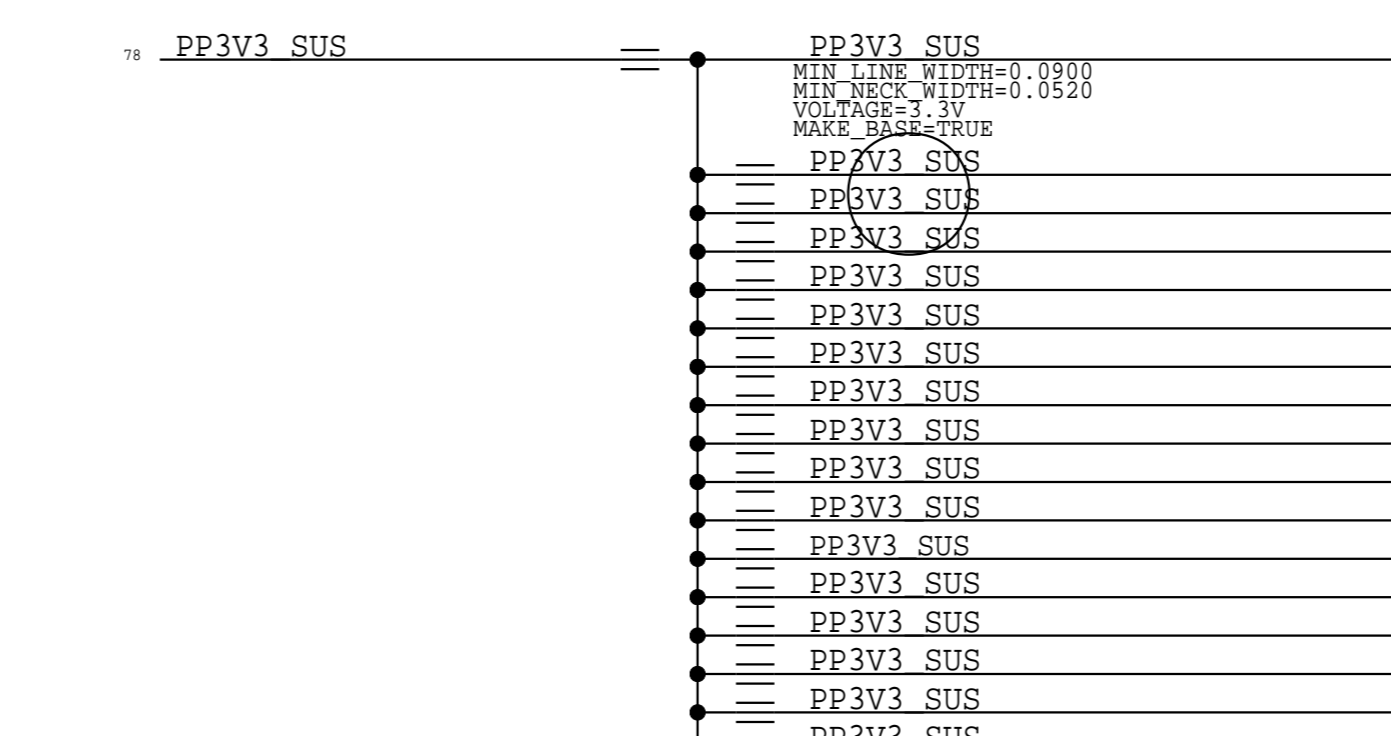
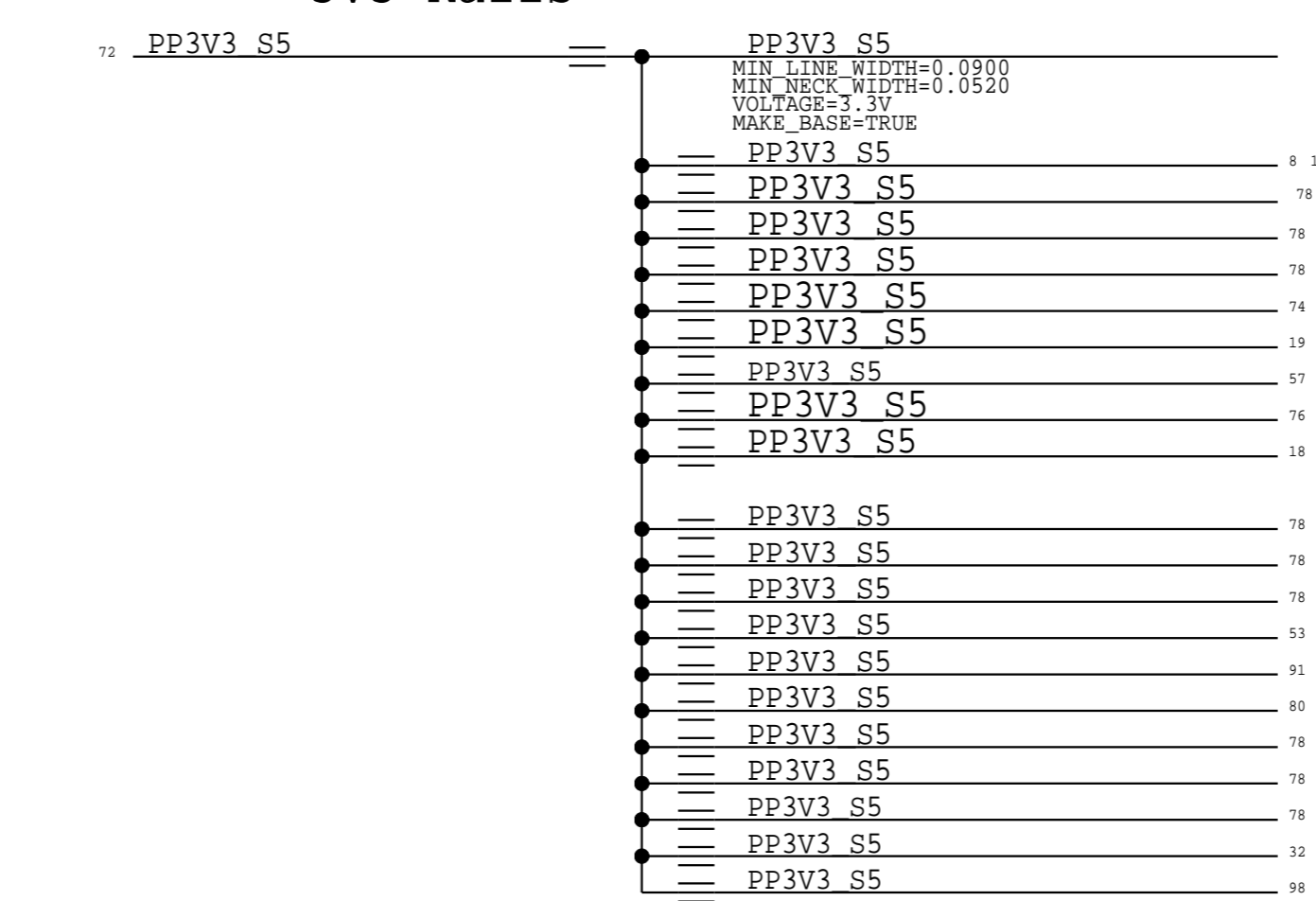
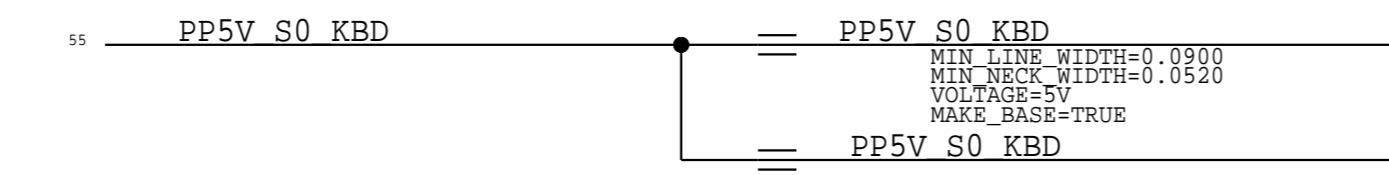
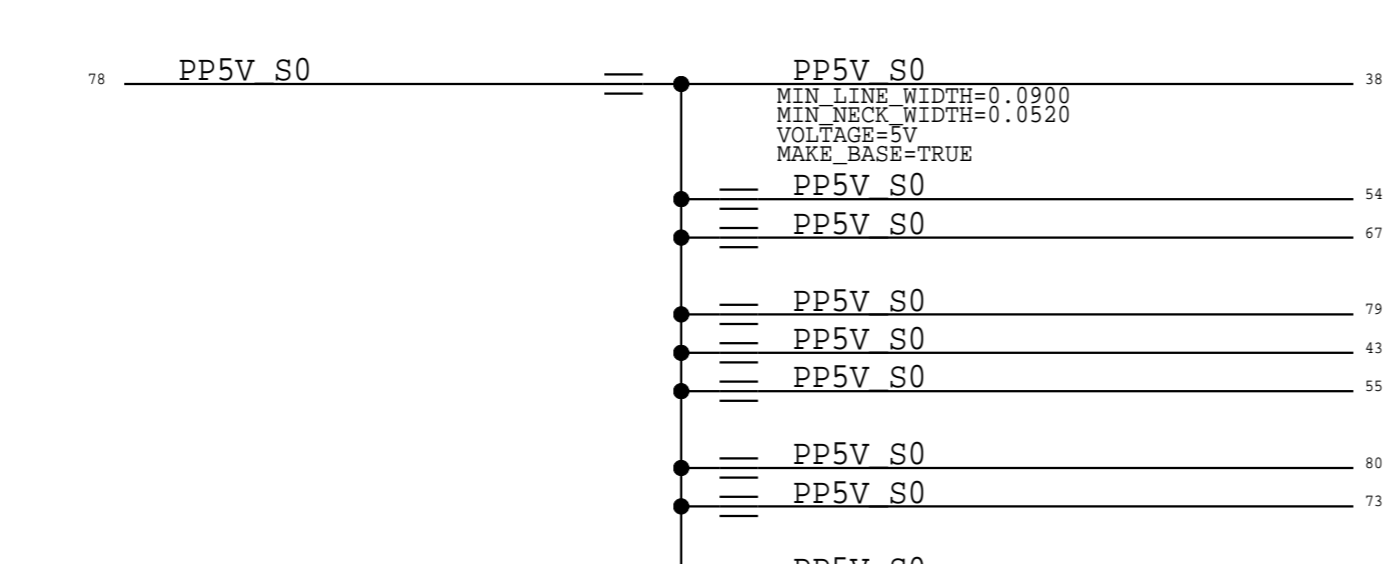
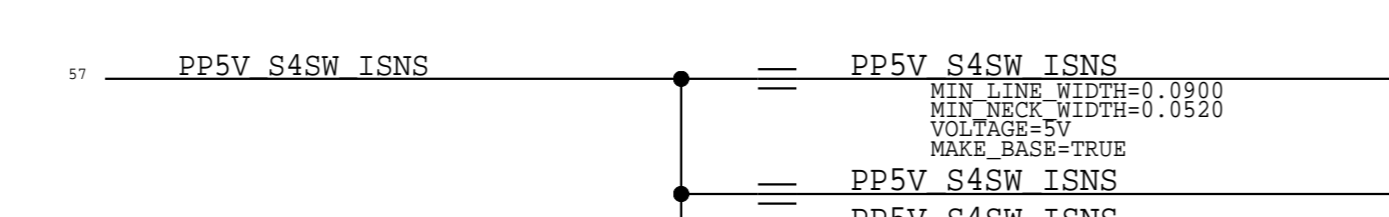
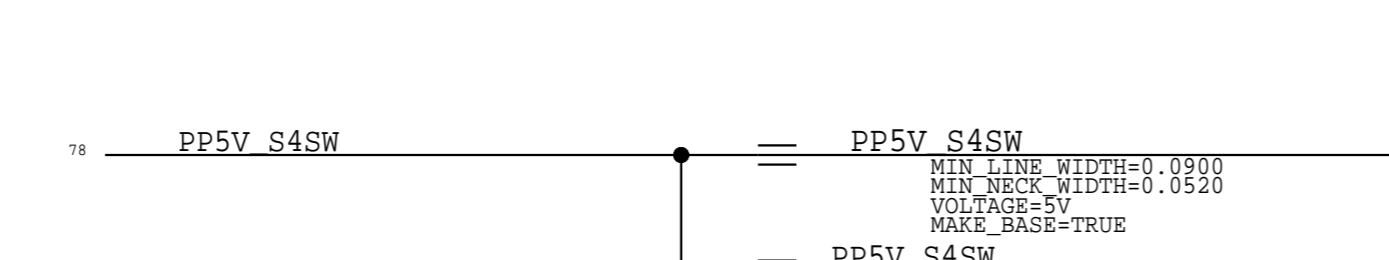
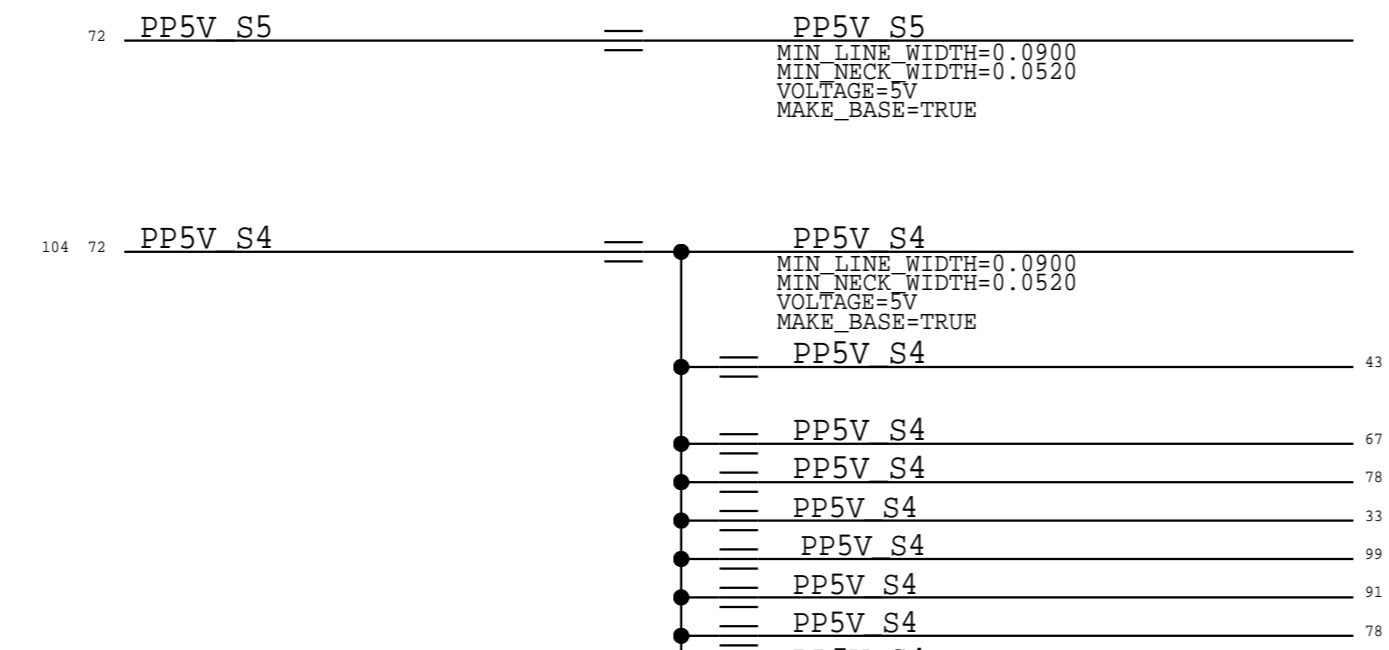
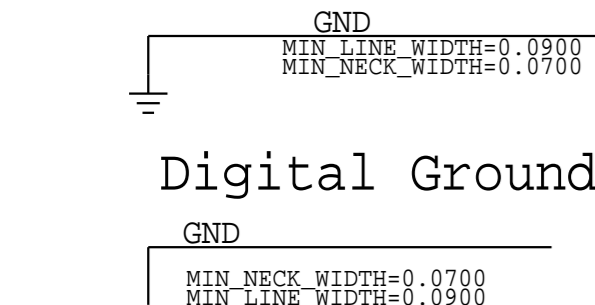
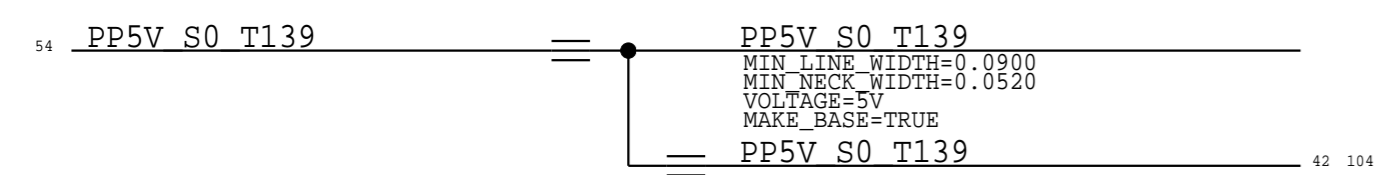
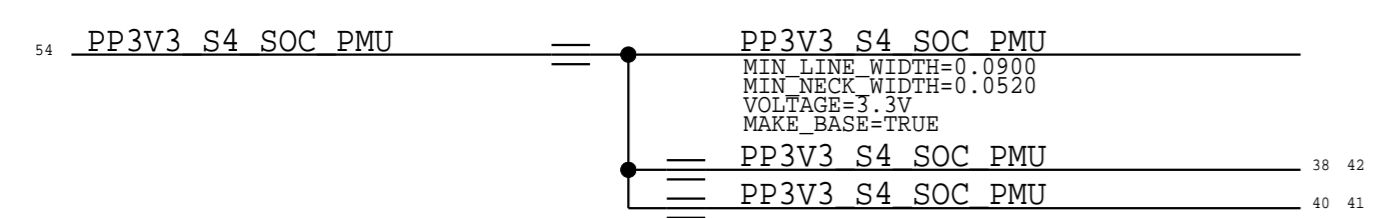
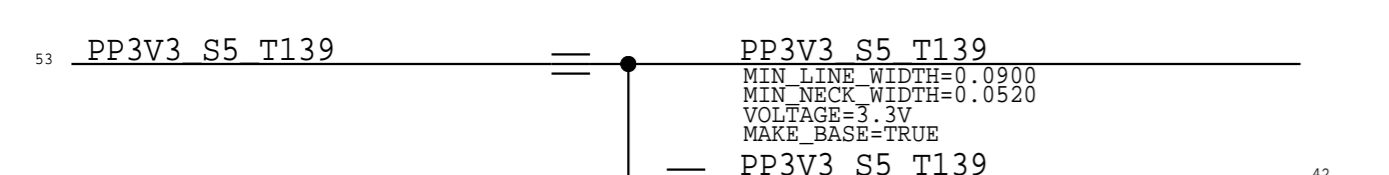
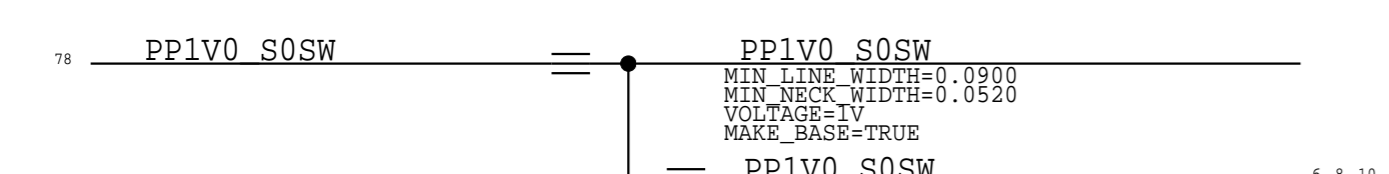
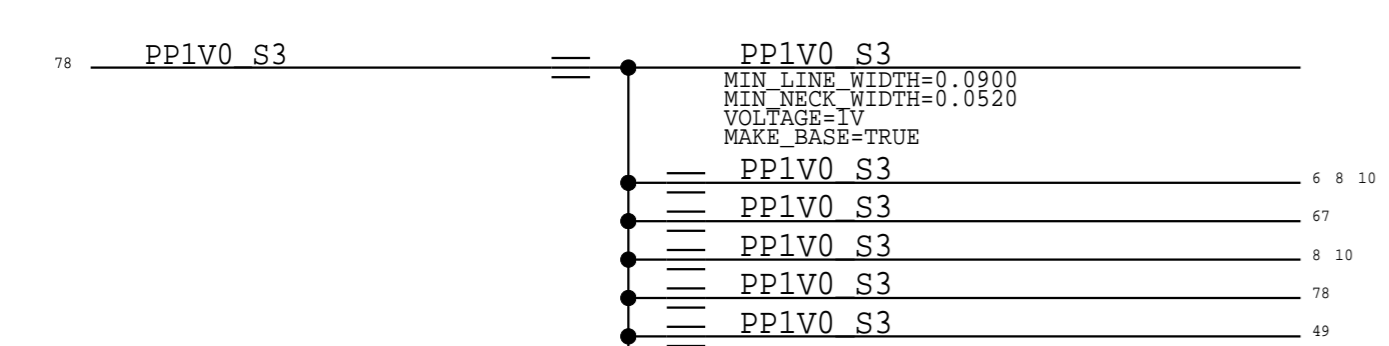
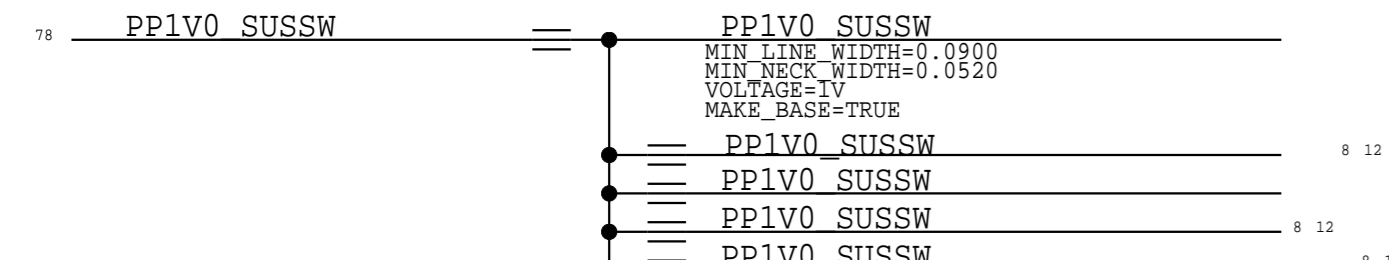
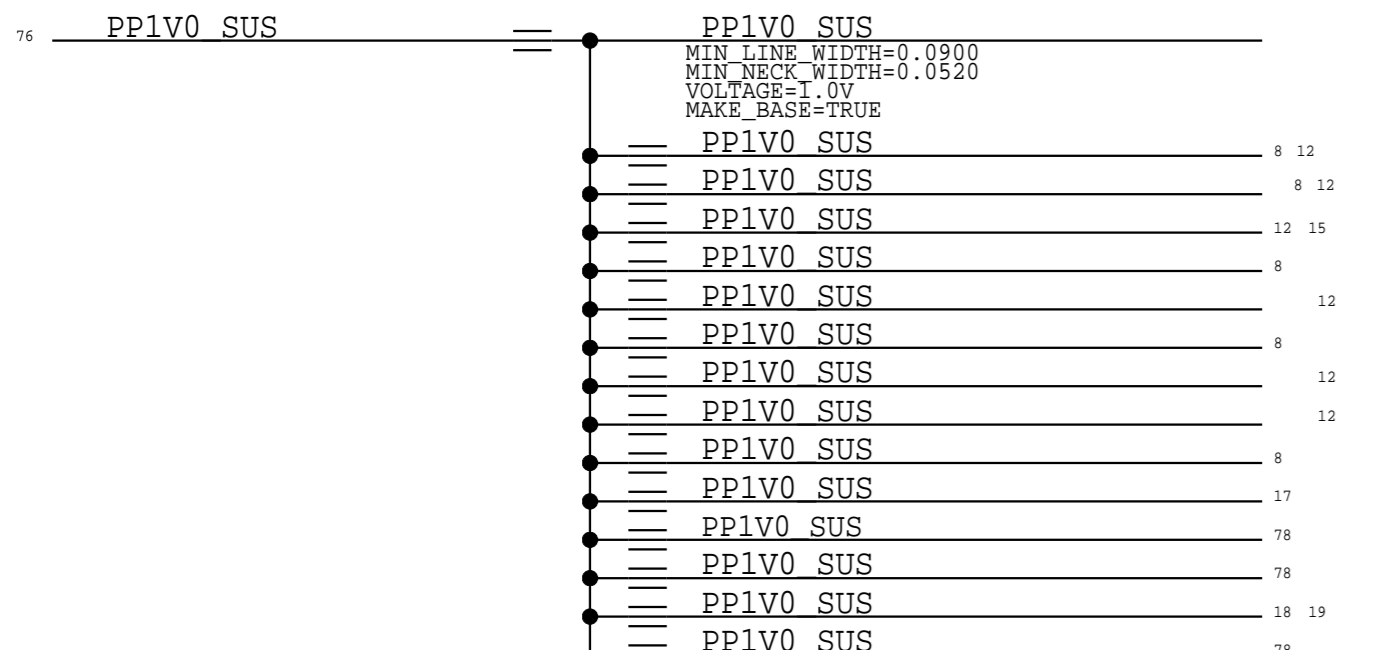
1V0 Rails

5V Rails

3V3 Rails

T208 Rails

Digital Ground



PAGE TITLE		Power Aliases - 2	
	DRAWING NUMBER	051-00515	STEP
	REVISION	9.0.0	D
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UNUSED TP ALIASES

UNUSED TP ALIASES

UNUSED SIGNAL ALIAS

83	NC S3X VSS S	==	NC S3X VSS S
82	NC S3X VDD S	==	NC S3X VDD S
81	NC S3X PMIC CTRL 2	==	NC S3X PMIC CTRL 2
81	NC S3X PCIE ATB1	==	NC S3X PCIE ATB1
81	NC S3X PCIE ATB0	==	NC S3X PCIE ATB0
81	NC S3X DT1	==	NC S3X DT1
81	NC S3X DT0	==	NC S3X DT0
81	NC S3X DDR ATO	==	NC S3X DDR ATO
74	NC PMIC PGG	==	NC PMIC PGG
74	NC PMIC PGF	==	NC PMIC PGF
74	NC PMIC PGE	==	NC PMIC PGE
74	NC PMIC PGD	==	NC PMIC PGD
74	NC PMIC PGC	==	NC PMIC PGC
88	NC PICCOLO 24M CLK REQ	==	NC PICCOLO 24M CLK REQ
14	NC PCH SLP A L	==	NC PCH SLP A L
14	NC PCH PME L	==	NC PCH PME L
14	NC PCH LANPHYC	==	NC PCH LANPHYC
14	NC PCH GPP F9	==	NC PCH GPP F9
14	NC PCH GPP F8	==	NC PCH GPP F8
14	NC PCH GPP F10	==	NC PCH GPP F10
16	NC PCH GPP D4	==	NC PCH GPP D4
16	NC PCH GPP D3	==	NC PCH GPP D3
16	NC PCH GPP D1	==	NC PCH GPP D1
14	NC PCH GPP D0	==	NC PCH GPP D0
14	NC PCH GPD7	==	NC PCH GPD7
99	NC P5VUSBC T PGOOD	==	NC P5VUSBC T PGOOD
34	NC DPMUX SAK 20	==	NC DPMUX SAK 20
34	NC DPMUX SAK 19	==	NC DPMUX SAK 19
34	NC DPMUX SAK 18	==	NC DPMUX SAK 18
34	NC DPMUX SAK 17	==	NC DPMUX SAK 17
34	NC DPMUX SAK 16	==	NC DPMUX SAK 16
34	NC DPMUX SAK 15	==	NC DPMUX SAK 15
34	NC DPMUX SAK 14	==	NC DPMUX SAK 14

6	NC CPU RSVD BB69	==	NC CPU RSVD BB69
6	NC CPU RSVD BB68	==	NC CPU RSVD BB68
6	NC CPU RSVD BA70	==	NC CPU RSVD BA70
6	NC CPU RSVD BA68	==	NC CPU RSVD BA68
6	NC CPU RSVD AW71	==	NC CPU RSVD AW71
6	NC CPU RSVD AW70	==	NC CPU RSVD AW70
6	NC CPU RSVD AK13	==	NC CPU RSVD AK13
6	NC CPU RSVD AK12	==	NC CPU RSVD AK12
9	NC CPU NCTFVSS C1	==	NC CPU NCTFVSS C1
9	NC CPU NCTFVSS BB70	==	NC CPU NCTFVSS BB70
9	NC CPU NCTFVSS BA71	==	NC CPU NCTFVSS BA71
9	NC CPU NCTFVSS BA1	==	NC CPU NCTFVSS BA1
9	NC CPU NCTFVSS B71	==	NC CPU NCTFVSS B71
9	NC CPU NCTFVSS AV1	==	NC CPU NCTFVSS AV1
9	NC CPU NCTFVSS A70	==	NC CPU NCTFVSS A70
9	NC CPU NCTFVSS A5	==	NC CPU NCTFVSS A5
6	NC CPU BB5	==	NC CPU BB5
6	NC CPU BB3	==	NC CPU BB3
6	NC CPU AY4	==	NC CPU AY4
6	NC CPU AU5	==	NC CPU AU5
6	NC CPU AT5	==	NC CPU AT5
13	NC CPU MSM L	==	NC CPU MSM L
28	NC USBC XA RESET L	==	NC USBC XA RESET L
34	NC USBC TB RESET L	==	NC USBC TB RESET L

UNUSED SIGNALS

14	NC PCH SLP WLAN L	==	TRUE	NC PCH SLP WLAN L	105
102	NC SPI CS1 L	==	TRUE	NC SPI CS1 L	102 105
102	NC SPI CS2 L	==	TRUE	NC SPI CS2 L	102 105
102	NC SPI CS1 L	==	TRUE	NC SPI CS1 L	102 105
102	NC SPI CS2 L	==	TRUE	NC SPI CS2 L	102 105
15	NC PCIE CAMERA D2R N	==	TRUE	NC PCIE CAMERA D2R N	105
15	NC PCIE CAMERA D2R P	==	TRUE	NC PCIE CAMERA D2R P	105
15	NC PCIE CAMERA R2D C N	==	TRUE	NC PCIE CAMERA R2D C N	105
15	NC PCIE CAMERA R2D C P	==	TRUE	NC PCIE CAMERA R2D C P	105
15	NC PCIE CLK100M CAMERA N	==	TRUE	NC PCIE CLK100M CAMERA N	105
15	NC PCIE CLK100M CAMERA P	==	TRUE	NC PCIE CLK100M CAMERA P	105
15	NC USB EXTA N	==	TRUE	NC USB EXTA N	TRUE
15	NC USB EXTA P	==	NO_TEST=1	NC USB EXTA P	TRUE
15	NC USB EXTB N	==	TRUE	NC USB EXTB N	TRUE
15	NC USB EXTB P	==	NO_TEST=1	NC USB EXTB P	TRUE
6	NC XDP BPM L<1>	==	TRUE	NC XDP BPM L<1>	TRUE
6	NC XDP BPM L<2>	==	NO_TEST=1	NC XDP BPM L<2>	TRUE
6	NC XDP BPM L<3>	==	NO_TEST=1	NC XDP BPM L<3>	TRUE
15	NC USB3 EXTB D2R N	==	TRUE	NC USB3 EXTB D2R N	TRUE
15	NC USB3 EXTB D2R P	==	NO_TEST=1	NC USB3 EXTB D2R P	TRUE
15	NC USB3 EXTB R2D C N	==	NO_TEST=1	NC USB3 EXTB R2D C N	TRUE
15	NC USB3 EXTB R2D C P	==	NO_TEST=1	NC USB3 EXTB R2D C P	TRUE

86	NC ANI0 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI0 NCE4
86	NC ANI0 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI0 NCE5
86	NC ANI0 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI0 NCE6
86	NC ANI0 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI0 NCE7
86	NC ANI1 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI1 NCE4
86	NC ANI1 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI1 NCE5
86	NC ANI1 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI1 NCE6
86	NC ANI1 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI1 NCE7
86	NC ANI2 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI2 NCE4
86	NC ANI2 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI2 NCE5
86	NC ANI2 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI2 NCE6
86	NC ANI2 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI2 NCE7
86	NC ANI3 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI3 NCE4
86	NC ANI3 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI3 NCE5
86	NC ANI3 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI3 NCE6
86	NC ANI3 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI3 NCE7
87	NC ANI4 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI4 NCE4
87	NC ANI4 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI4 NCE5
87	NC ANI4 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI4 NCE6
87	NC ANI4 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI4 NCE7
87	NC ANI5 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI5 NCE4
87	NC ANI5 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI5 NCE5
87	NC ANI5 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI5 NCE6
87	NC ANI5 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI5 NCE7
87	NC ANI6 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI6 NCE4
87	NC ANI6 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI6 NCE5
87	NC ANI6 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI6 NCE6
87	NC ANI6 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI6 NCE7
87	NC ANI7 NCE4	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI7 NCE4
87	NC ANI7 NCE5	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI7 NCE5
87	NC ANI7 NCE6	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI7 NCE6
87	NC ANI7 NCE7	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI7 NCE7
86	NC ANI1 RNB	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI1 RNB
86	NC ANI3 RNB	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI3 RNB
87	NC ANI5 RNB	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI5 RNB
87	NC ANI7 RNB	==	MAKE_BASE=TRUE	NO_TEST=1	NC ANI7 RNB

S3X Aliasing

19	SSD_CLKREQ L	==	SSD_CLKREQ_L	91	
14	SSD_SR_EN L	==	SSD_SR_EN L	91 104	
79	I2C_BKLT_SCL	==	TRUE	I2C_BKLT_SCL	80 104
79	I2C_BKLT_SDA	==	TRUE	I2C_BKLT_SDA	80 104

EPD PANEL

SYNC_MASTER=SHART_J44		SYNC_DATE=11/19/2012	
PAGE TITLE			
<h3>Signal Aliases</h3>			
		DRAWING NUMBER	051-00515
		REVISION	9.0.0
		BRANCH	dvt-fab09-0
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		SHEET	102 OF 119

Memory Bit & Byte Swizzle

```

MAKE_BASE=TRUE
MEM A DQ<0> == MEM A DQ<0> 21
MEM A DQ<1> == MEM A DQ<1> 21
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MEM A DQ<11> == MEM A DQ<11> 21
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MEM A DQS N<7> == MEM A DQS N<7> 22

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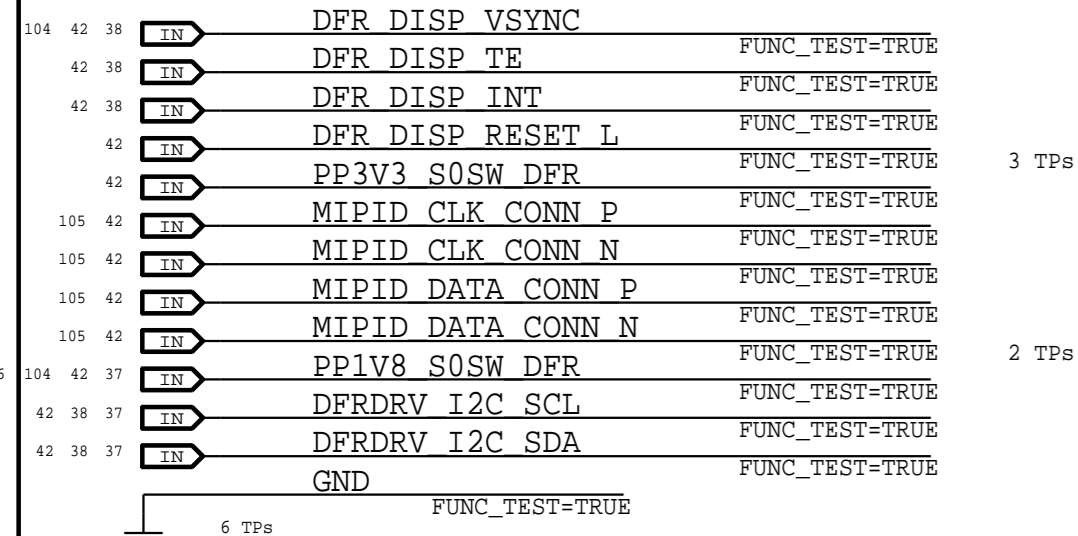
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MEM B DQS N<1> == MEM B DQS N<1> 23
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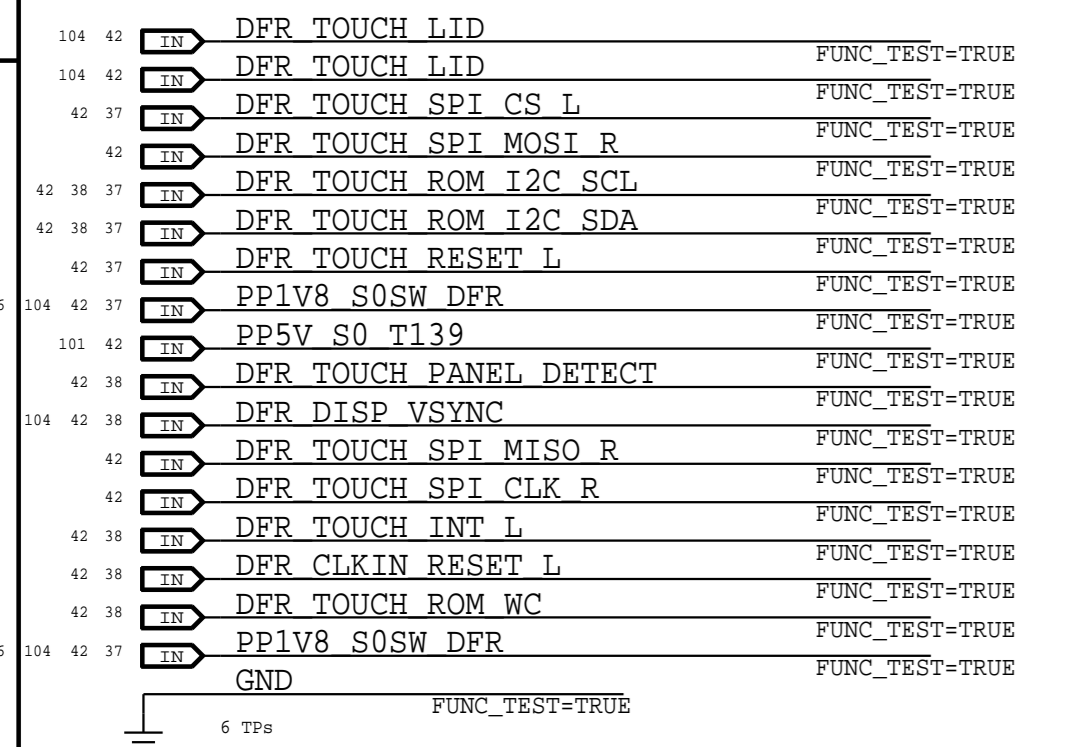
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IV ALL RIGHTS RESERVED			

Functional Test Points

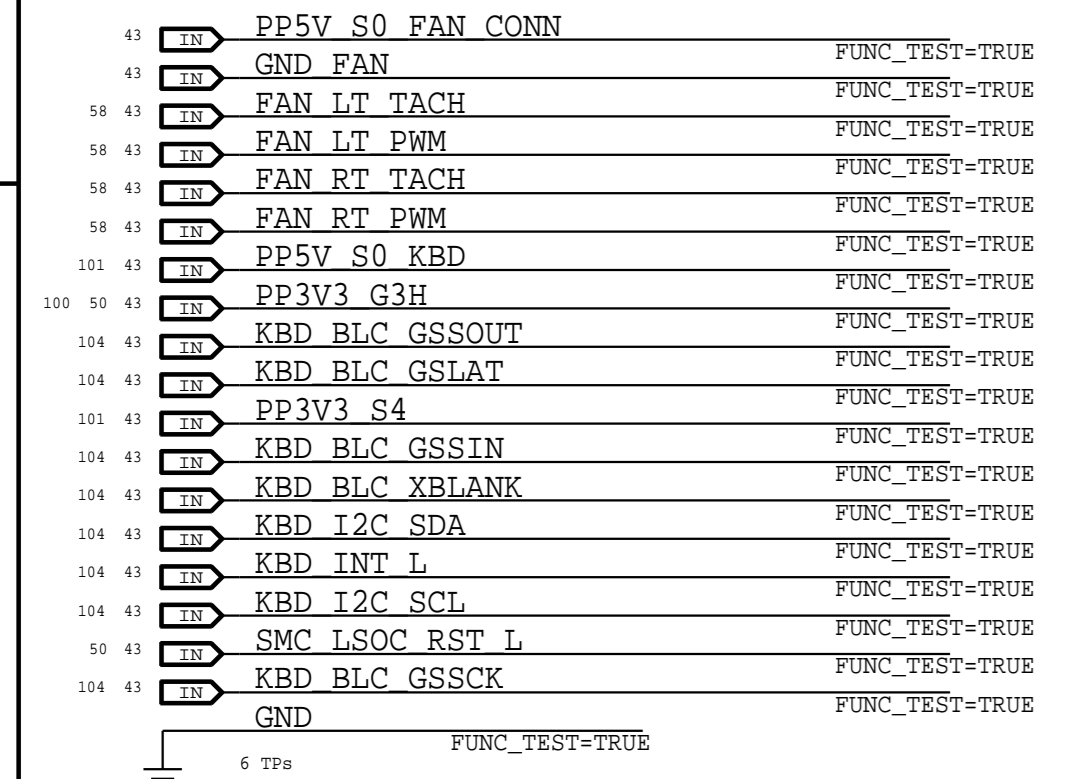
J4401 - DFR Display Connector



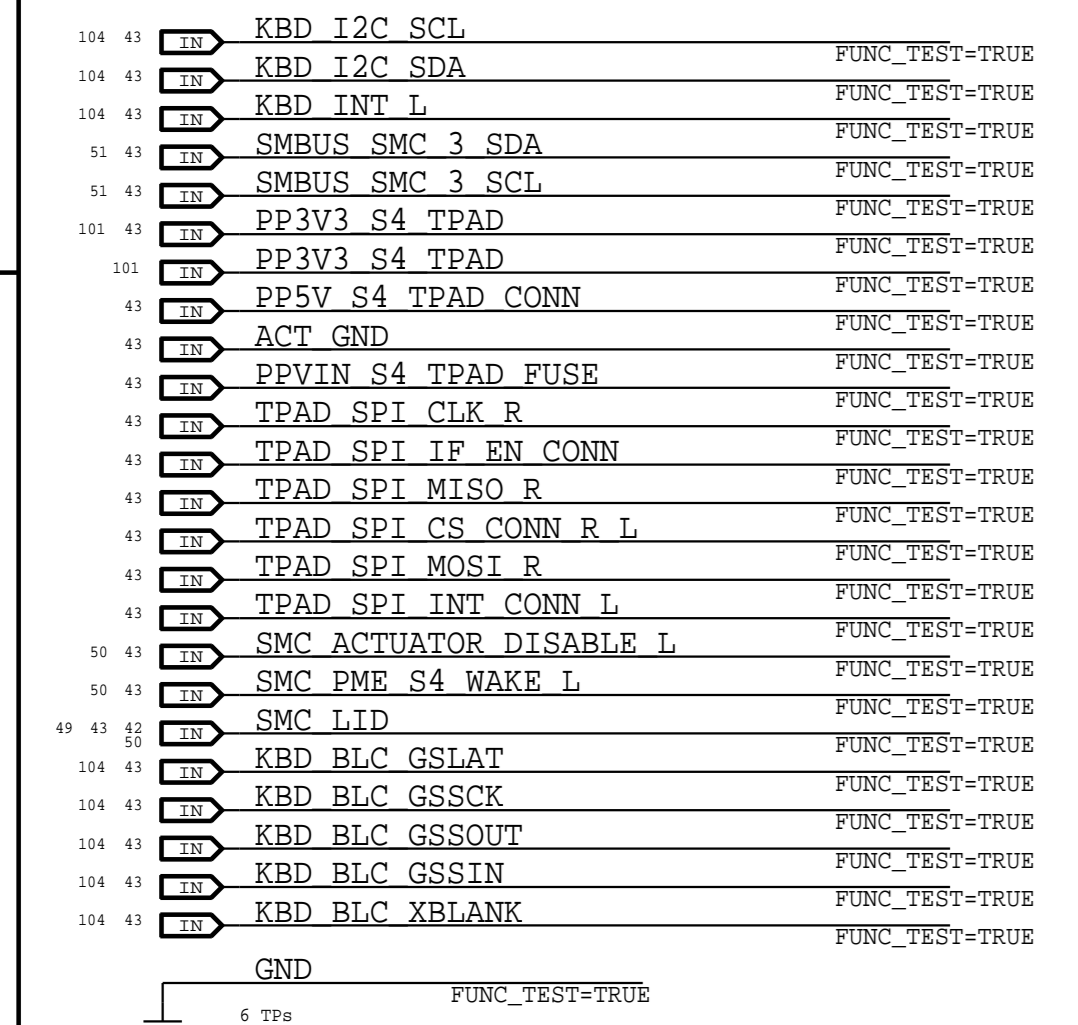
J4402 - DFR Touch Connector



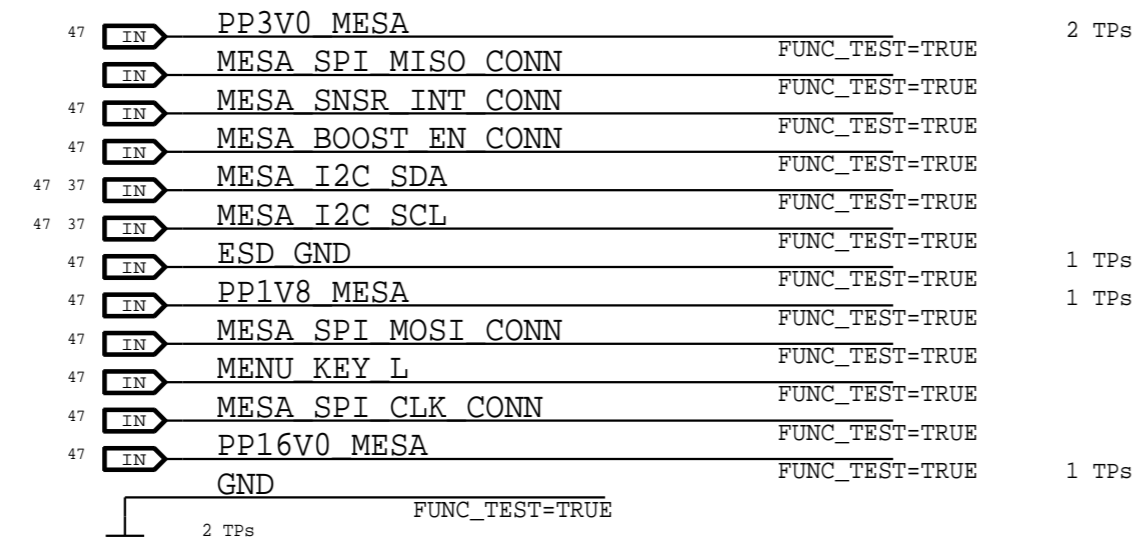
J4500 - Keyboard Connector



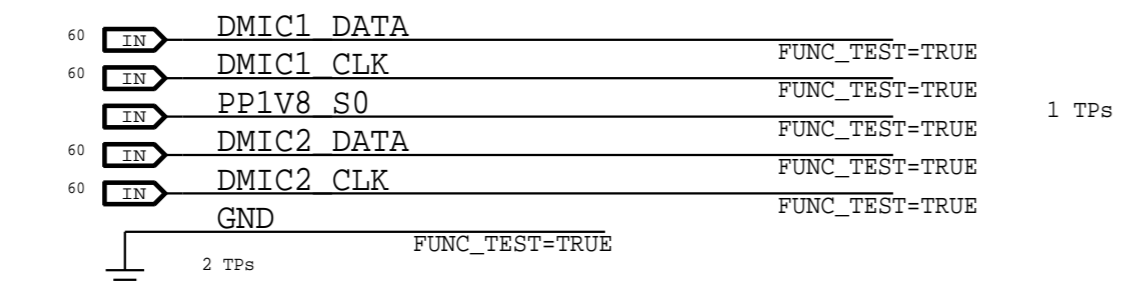
J4501 - Trackpad Connector



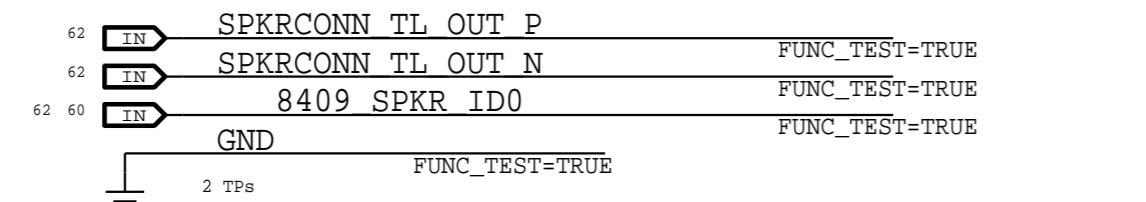
J4900 - Mesa Connector



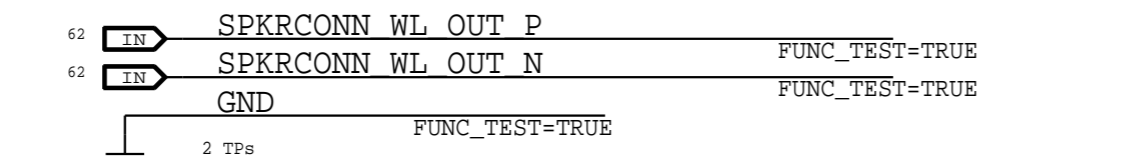
J6200 - MIC Connector



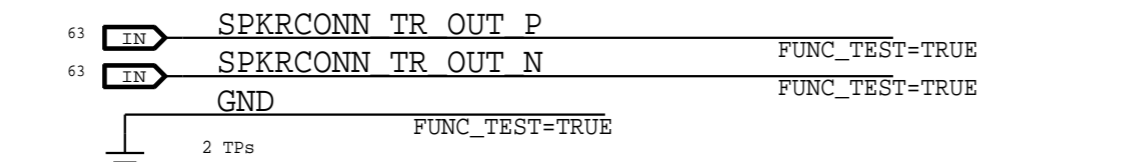
J6410 - Left Tweeter Connector



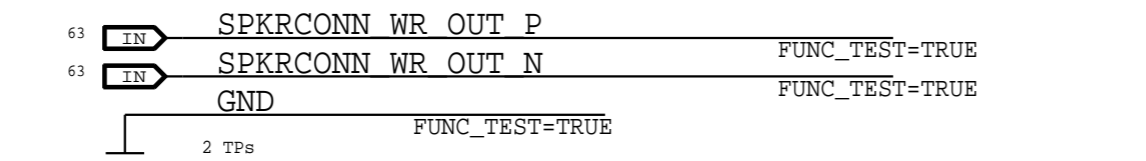
J6430 - Left Woofer Connector



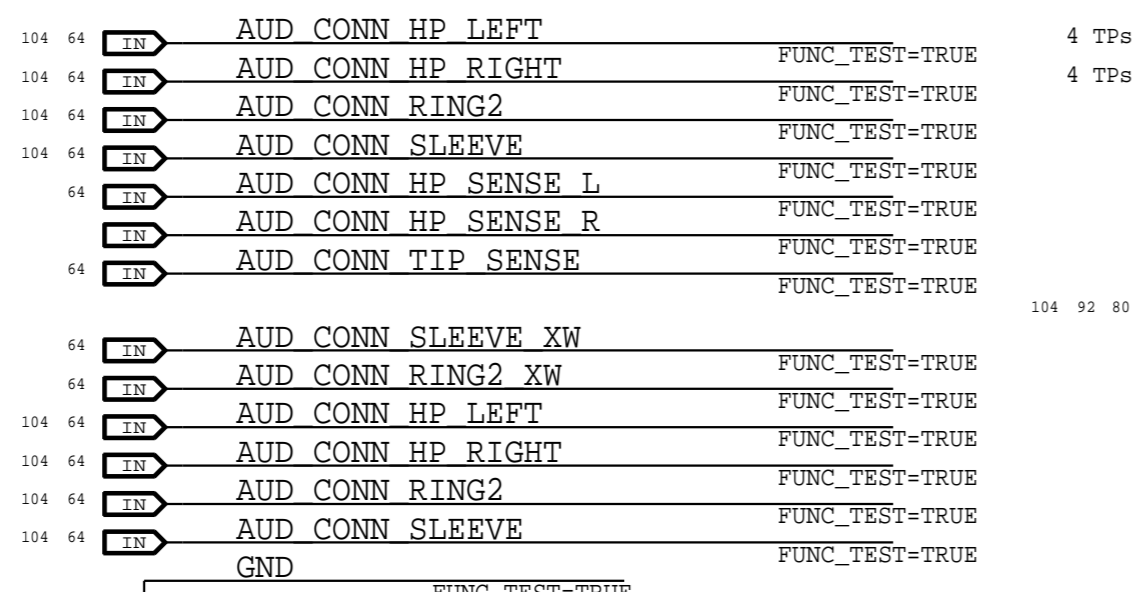
J6500 - Right Tweeter Connector



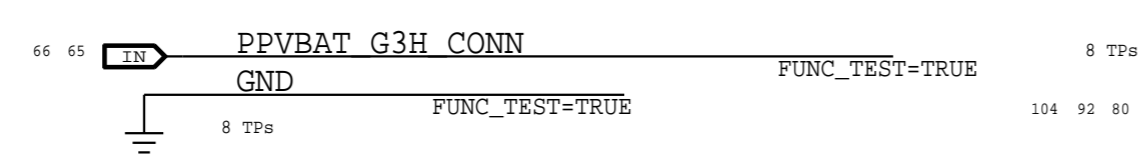
J6550 - Right Woofer Connector



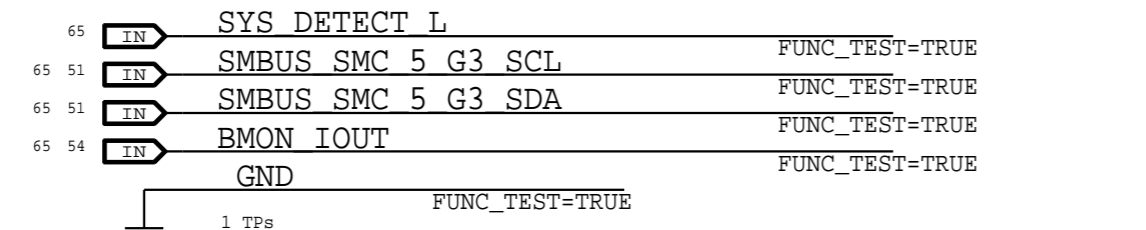
J6600 - Audio Jack Connector



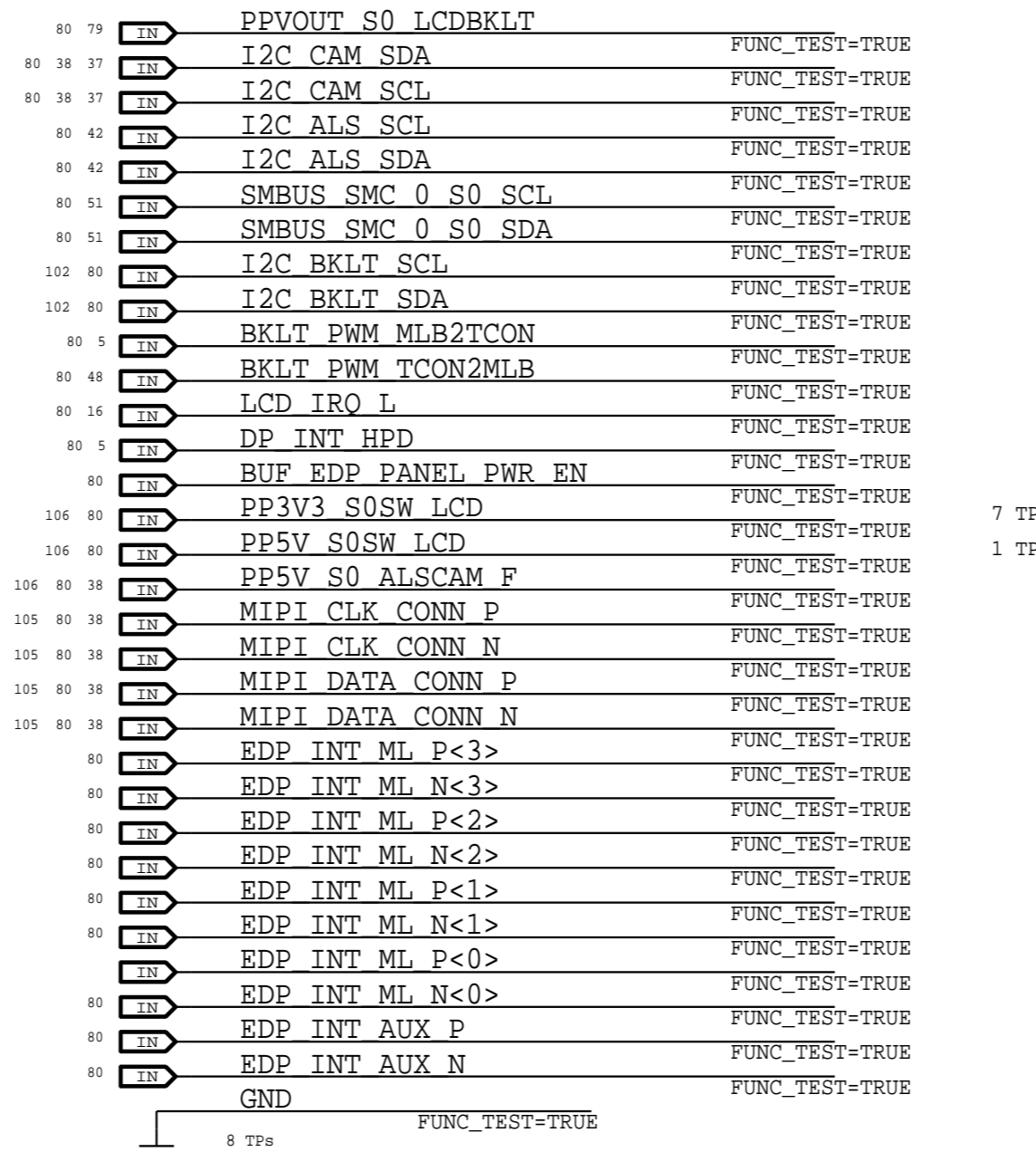
J6950 - Battery Connector



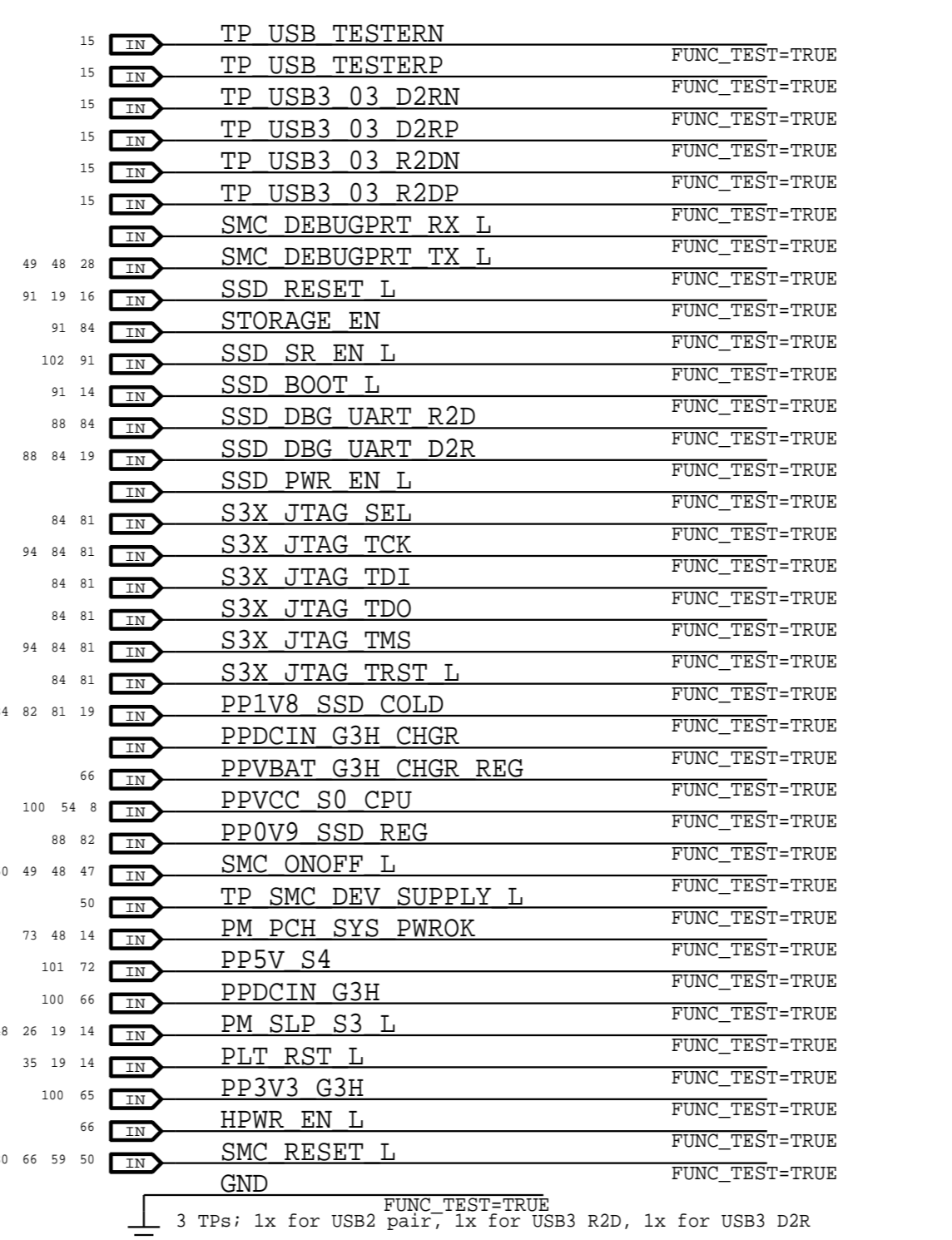
J6951 - Battery Sense Connector



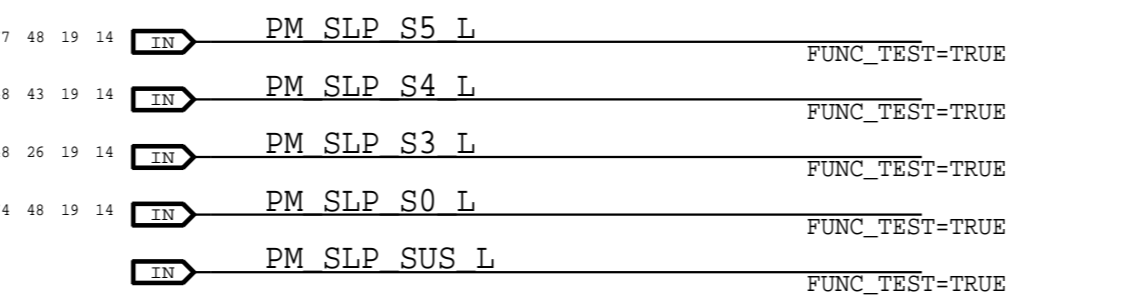
J8500 - eDP Connector



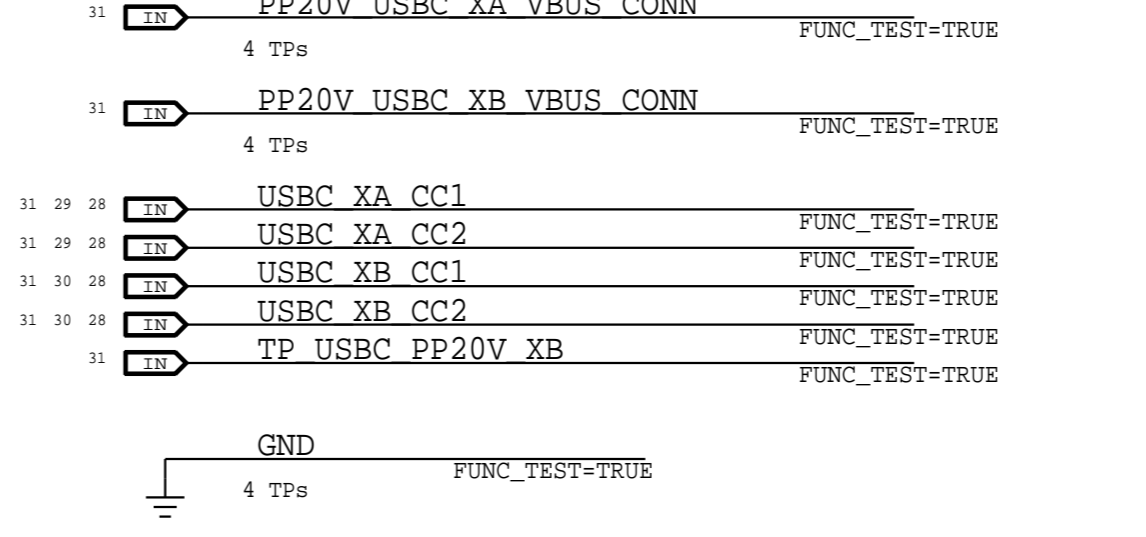
Probe Block Grid - WiPass and NAND Rack



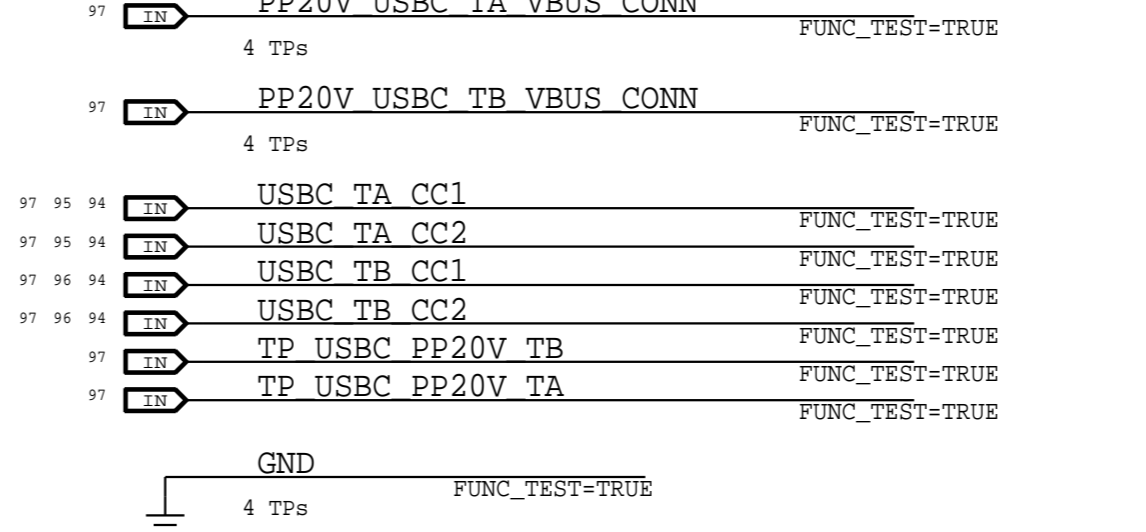
Debug LEDs



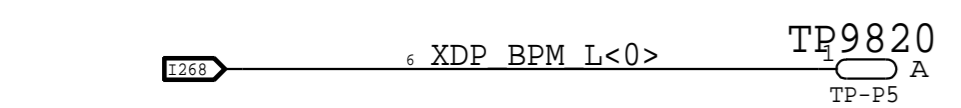
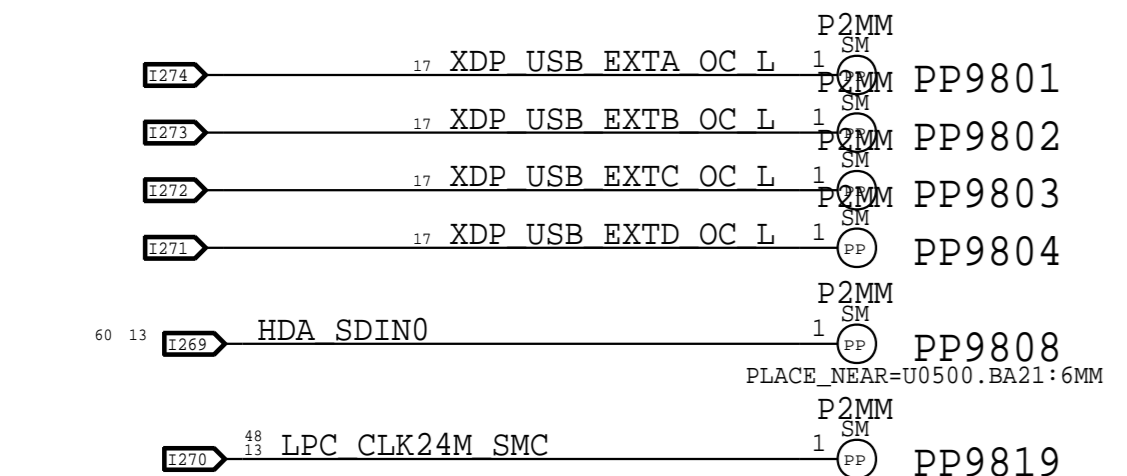
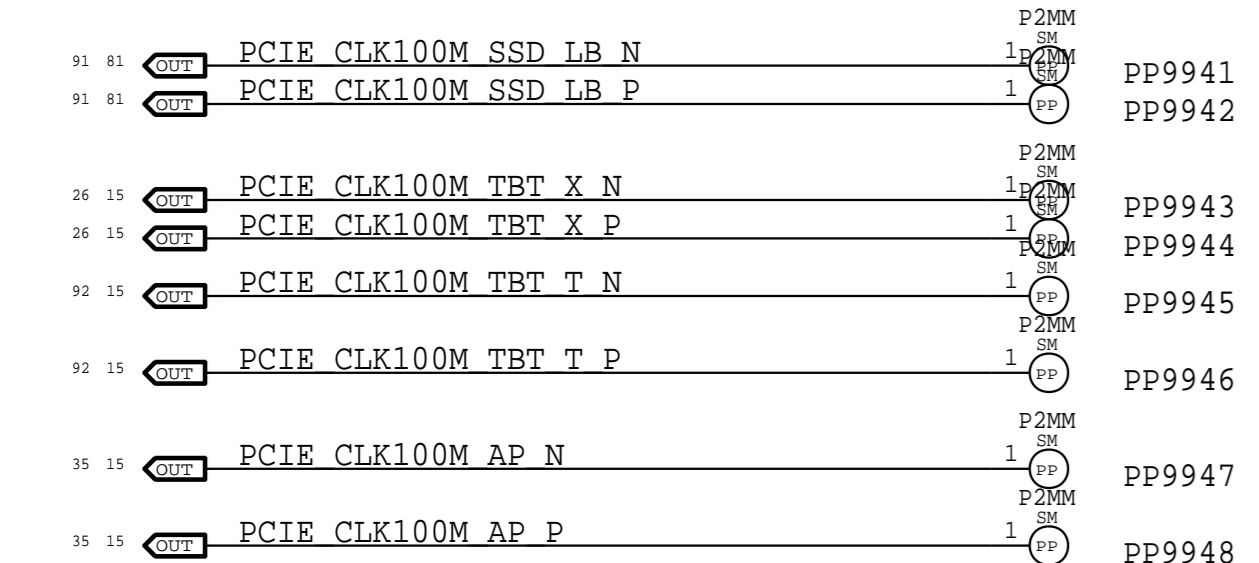
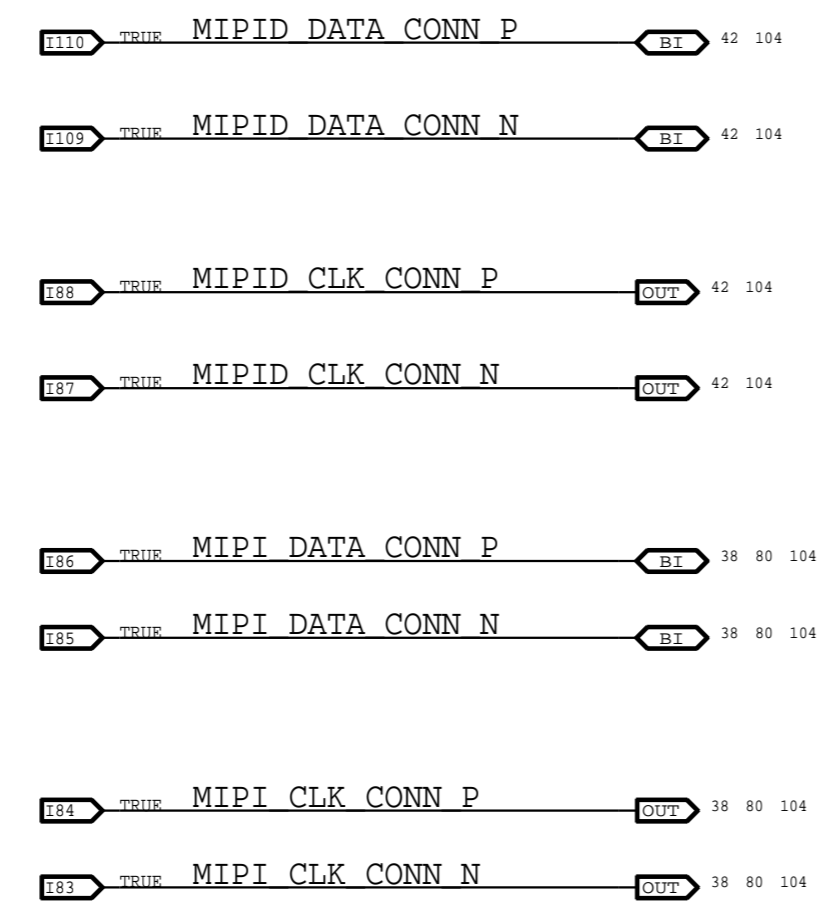
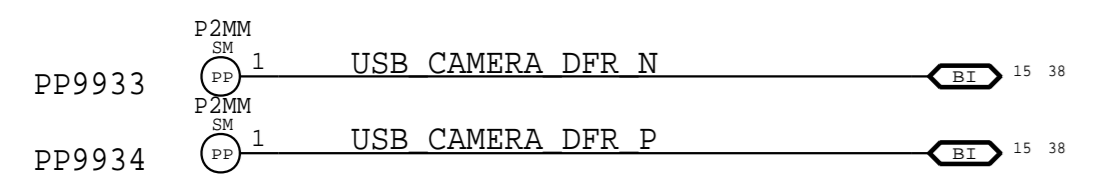
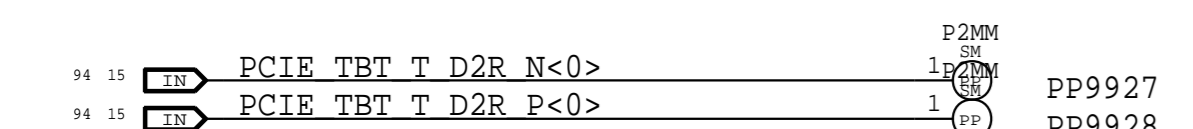
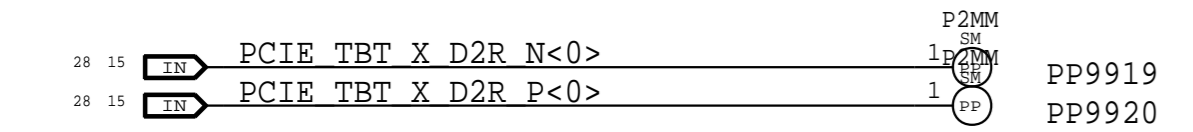
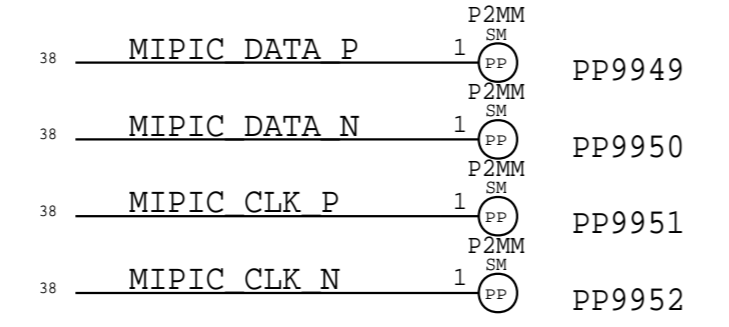
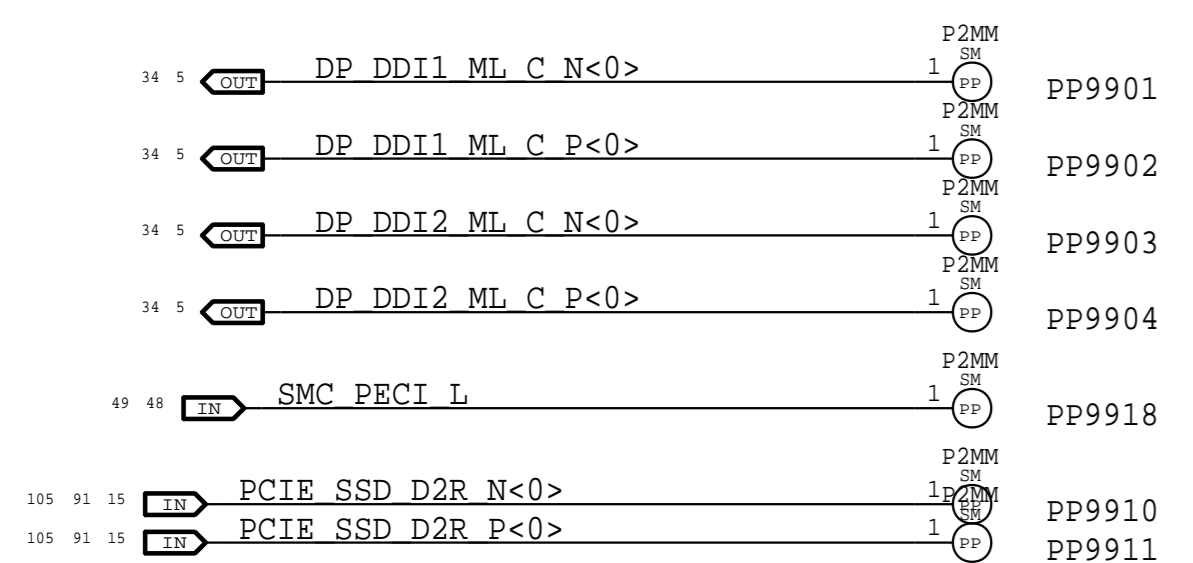
J3300 - Left USB-C Connector



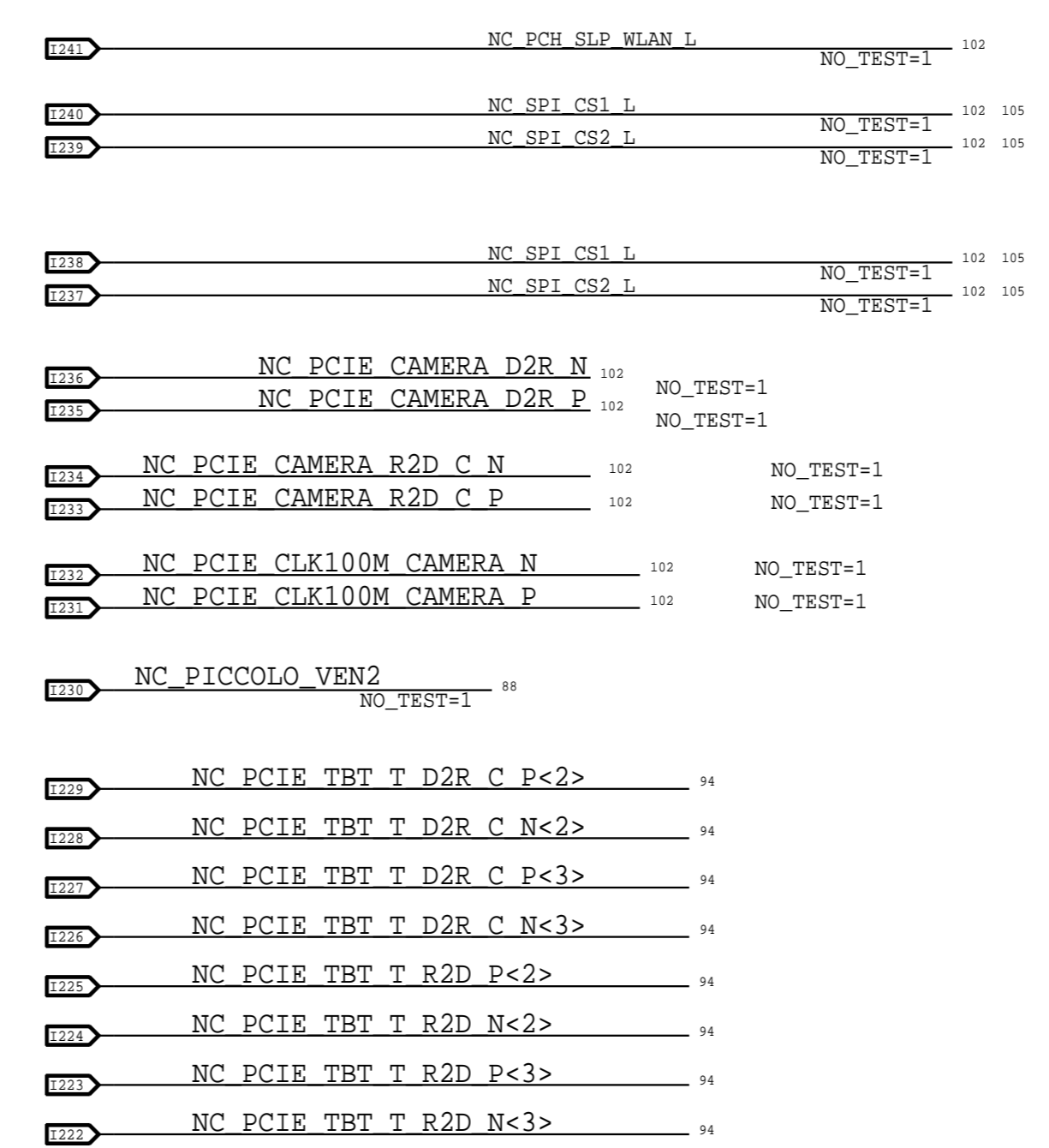
JB500 - Right USB-C Connector



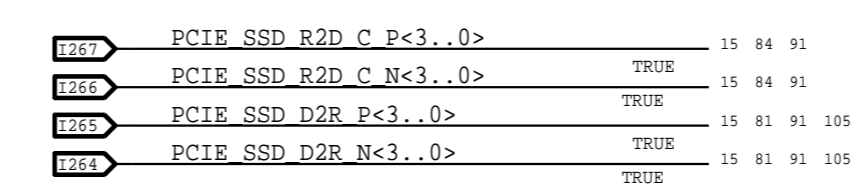
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NO_TESTS

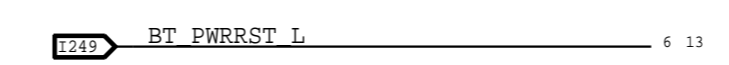


High Speed NO_TEST

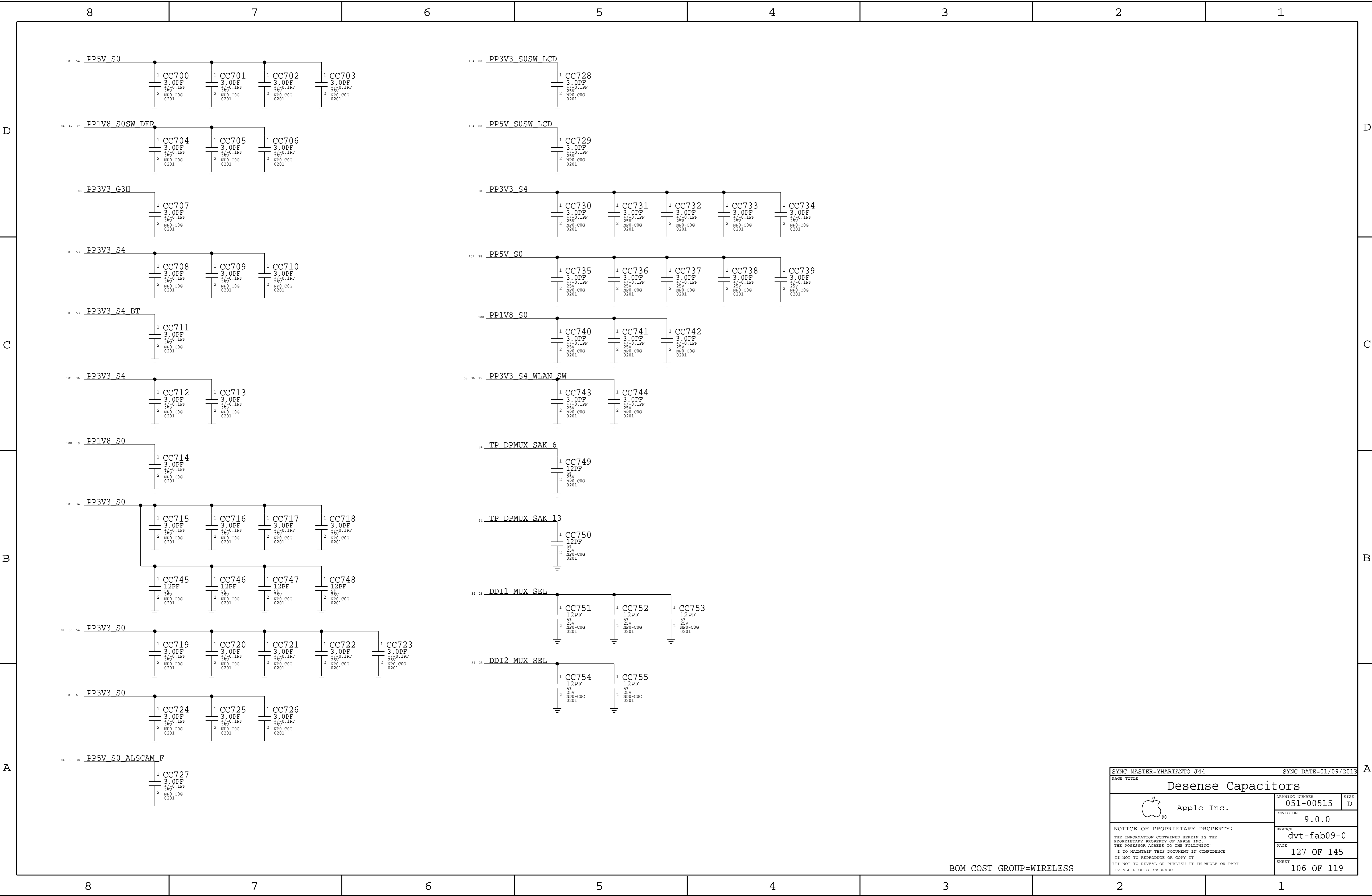


Unused nets with offpage

(Nets with offpages not used on this project)



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J79 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_75D	*	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=4x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=6x_DIELECTRIC	?
MEM_CMD2CMD	*	=6x_DIELECTRIC	?
MEM_CMD2CTL	*	=6x_DIELECTRIC	?
MEM_CTL2CTL	*	=6x_DIELECTRIC	?
MEM_CLK2CLK	*	=12x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=16x_DIELECTRIC	?
MEM_2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_2PWR	*	=4x_DIELECTRIC	?
MEM_2GND	*	=4x_DIELECTRIC	?
MEM_2OTHER	*	=12x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF_B	*	=1.5x_DIELECTRIC	?
MEM_DQS2OWNDATA_B	*	=1.5x_DIELECTRIC	?
MEM_CMD2CMD_B	*	=1.5x_DIELECTRIC	?
MEM_CMD2CTL_B	*	=1.5x_DIELECTRIC	?
MEM_CTL2CTL_B	*	=1.5x_DIELECTRIC	?
MEM_CLK2CLK_B	*	=1.5x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	BGA_MEM	MEM_80D
MEM_40S	BGA_MEM	MEM_45S

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Memory Constraints

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2X_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

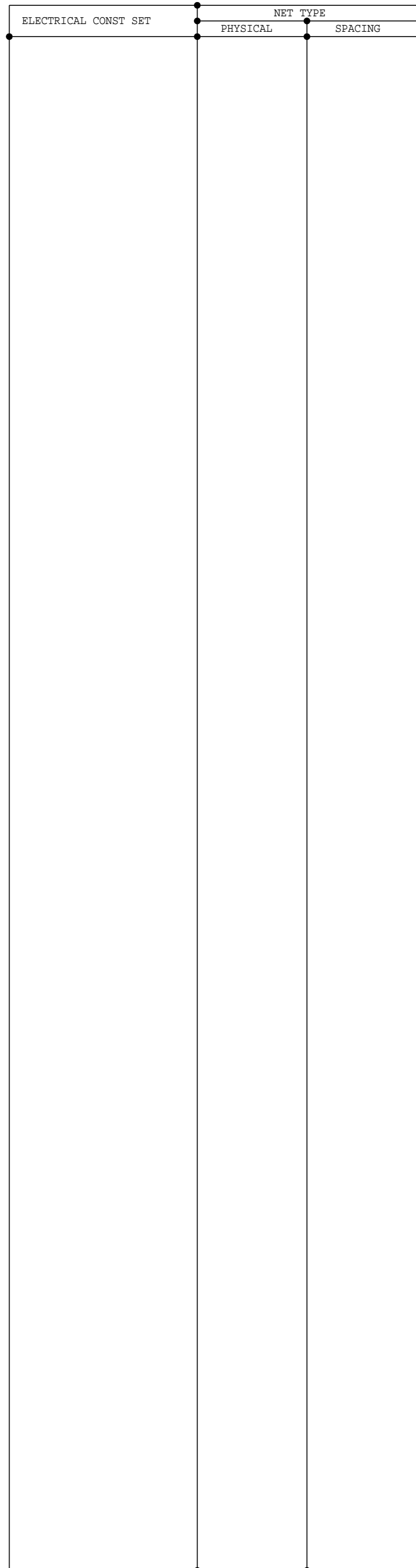
DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3X_DIELECTRIC	?
DP_2OTHER	*	=4X_DIELECTRIC	?
HDMICLK_2OTHER	*	=7X_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4X_DIELECTRIC	?
HDMIDATA_2SAME	*	=3X_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

Thunderbolt, DP, HDMI Net Properties



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Change List:

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Kismet:

AFP://KISMET.APPLE.COM/KISMET-PROJECTS/J79

Useful Wiki Links:

Schematic Conventions - <https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions>

Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

<rdar://component/XXXXXX> MobileMac HW | Task

<rdar://component/XXXXXX> MobileMac HW | Schematic

<rdar://component/XXXXXX> MobileMac HW | New Bugs


<rdar://component/XXXXXX> MobileMac HW | Layout

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<rdar://component/XXXXXX> MobileMac HW | Architecture

Other Info:

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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107800033	107800034		ALL	
13880738	13881101		ALL	Samsung alt to Murata
13880846	13880811		ALL	Samsung alt to Murata
152800359	152800253		ALL	Chilisin alt to Cyttec
37180704	371800077		ALL	NXP alt to Diodes
37681053	37680604		ALL	Diodes alt to Fairchild
37681106	37680678		ALL	Fairchild alt to Vishay
740800027	74080159		ALL	Bourns alt to Little Fuse
10780249	10780251		ALL	
107800015	107800011		ALL	
107800071	107800053		ALL	
12880364	12880264		ALL	Kemet w/ Panasonic
12880325	12880397		ALL	
128800009	128800007		ALL	
128800029	128800007		ALL	
128800070	128800007		ALL	
128800010	128800011		ALL	
128800031	128800011		ALL	
128800026	128800011		ALL	
132800064	13280409		ALL	
13880614	13880578		ALL	
13880703	13880648		ALL	
138800032	13880831		ALL	
138800049	13880831		ALL	
13880863	13880853		ALL	
13880775	13880860		ALL	
138800084	138800060		ALL	
152800369	152800268		ALL	Cyntec w/ NEC
155800188	155800275		ALL	Murata w/ Taiyo
15580694	15580387		ALL	
15580660	15580513		ALL	
155800018	15580664		ALL	Murata w/ Taiyo
155800007	15580667		ALL	

BLC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197800046	197800036		ALL	Epson w/ TXC
197800047	197800036		ALL	Kyocera w/ TXC
197800048	197800036		ALL	Murata w/ TXC
197800053	197800050		ALL	Kyocera w/ TXC
197800054	197800050		ALL	NDK w/ TXC
197800055	197800050		ALL	Murata w/ TXC
31180596	31180593		ALL	NXP w/ Diodes
10780276	10780020		ALL	Cyntec w/ TFT
107800021	10780284		ALL	TFT w/ Yageo
152800343	15281682		ALL	NXP w/ Diodes
107800087	107800029		ALL	TFT w/ Yageo
128800058	128800018		ALL	NEC w/ Rohm
13880706	13880739		ALL	NEC w/ Vishay
13880945	13880739		ALL	NEC w/ Rohm
152800358	152800208		ALL	Murata w/ Chillisin
152800400	152800361		ALL	Murata w/ Cyntec
15281872	152800361		ALL	Murata w/ Cyntec
155800034	15580706		ALL	Taiyo w/ Murata

353800711	35382073		ALL	On Semi w/ TI
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740800019	740800007		ALL	Bourns w/ Polytronics
155800189	15580342		ALL	Murata w/ Taiyo
13880714	13880713		ALL	Murata w/ Samsung
13880715	13880732		ALL	Murata w/ Samsung
107800086	107800056		ALL	TFT w/ Cyntec
13880875	13880678		ALL	Taiyo w/ Mur&SS
13880786	13880705		ALL	Murata w/ Samsung
15282052	15281954		ALL	Taiyo w/ Cyntec
15282015	15281958		ALL	Taiyo w/ Cyntec
13880789	13880941		ALL	Murata w/ SS
107800101	107800005		ALL	Cyntec w/ Yageo
107800102	107800017		ALL	Cyntec w/ Yageo
107800100	107800057		ALL	Cyntec w/ TFT
107800103	107800058		ALL	Cyntec w/ Yageo
107800104	107800061		ALL	Cyntec w/ Yageo
107800105	107800062		ALL	Cyntec w/ Yageo
152800403	152800322		ALL	Murata w/ Chillisin

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138800104	13880978		ALL	Murata w/ Taiyo
311800072	31180657		ALL	NXP w/ On Semi
311800090	311800028		ALL	On Semi w/ TI
353800854	35384342		ALL	TI w/ ST
377800077	37780183		ALL	Infineon w/ ST

13880700	13880641		ALL	Murata w/ SS&Taiyo
152800363	152800048		ALL	Cyntec w/ Vishay
15580659	15580382		ALL	Murata w/ TDK
376800146	37681061		ALL	NXP w/ Diodes

128800062	128800067		ALL	
128800069	128800067		ALL	
132800012	13280401		ALL	
13880660	13880684		ALL	
13881103	13880719		ALL	
138800097	13880750		ALL	
138800111	138800036		ALL	
155800203	15580894		ALL	
197800082	197800081		ALL	
311800060	31180273		ALL	
311800118	31180489		ALL	
31180271	311800008		ALL	
311800104	311800091		ALL	
31180437	311800112		ALL	
335800213	33580888		ALL	
343800136	343800135		ALL	
343800137	343800135		ALL	
343800138	343800135		ALL	
353800880	35383452		ALL	
353800878	353800599		ALL	
353800879	353800754		ALL	
353800750	353800877		ALL	
371800089	371800085		ALL	
37780178	377800031		ALL	

15580914	15580897		ALL	
155800190	15580897		ALL	
311800004	31180370		ALL	
311800013	31180508		ALL	NXP w/ Diodes
353800107	35383239		ALL	
353800525	35384471		ALL	
37280186	37280185		ALL	
376800014	37680761		ALL	
376800086	37680761		ALL	
37681080	37680820		ALL	
376800074	37680855		ALL	
37681089	37681128		ALL	
74080144	74080118		ALL	
740800028	74080118		ALL	
740800003	74080135		ALL	
998-04070	998-04071		ALL	Hynix alt to SS

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Apple Inc.		REVISION		9.0.0
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