1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
1	0006782329	ENGINEERING RELEASED	2016-08-10

DESIGN: X502/MLB_CATZ

LAST CHANGE: Tue Aug 9 17:02:57 2016

LAST_MODIFICATION=Tue Aug 9 17:03:06 2016

DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02265	1	SCHEM,MLB_CATZ,X502	SCH		
820-00875	1	PCBF,MLB_CATZ,X502	MLB	CRITICAL	
639-03266		PCBA,MLB_CATZ,XXXXX,X502			
685-00125	1	COMMON PARTS,MLB_CATZ,X502	CBOM		CMN_PARTS_BOM
985-00239	1	DEV PARTS,MLB_CATZ,X502	DEV1		DEVELOPMENT_LIST

BOM_COST_GROUP=NO COST ITEMS

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Apple Inc.

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Major ICs

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-00235	1	IC,CPU,SKL-ULT,2+3E,42X24MM,BGA1356	U0500	CRITICAL	CPU_SKL:BASE
998-04195	1	INTERPOSER,VTT ADAPTER,SKL-U,BGA1356	U0500	CRITICAL	CPU_SKL:VTT_INTERPOSER
337S00168	1	CPU,SKYU,QJ8N,D0,QS,2/2,2.3,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.3
337S00170	1	CPU,SKYU,QJ8K,D0,QS,2/2,2.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.6
337S00149	1	CPU,SKYU,QJ57,J0,ES0,2/3,1.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_GD
337S00150	1	CPU,SKYU,QJ58,J0,ES0,2/3,1.6,28W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_BT
337S00219	1	CPU,SKYU,QK2T,K1,SQS,1.8,15W,.95,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_1G8
337S00220	1	CPU,SKYU,QKBY,K1,SQS,2.2,15W,1.05,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G2
337S00222	1	CPU,SKYU,QK33,K1,SQS,2.0,15W,1.0,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G0
337S00233	1	CPU,SKYU,QK32,K1,SQS,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G4
337S00232	1	CPU,SKY,SR2JC,K1,PRQ,1.8,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_1G8
337S00239	1	CPU,SKY,SR2JM,K1,PRQ,2.0,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G0
337S00234	1	CPU,SKYU,SR2JL,K1,PRQ,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G4

ACE

353S00422	2	IC,CD3215,USB PWR SWITCH,A0,6X6MM,BGA96	U3100,U3200	CRITICAL	ACE:A0
353S00660	2	IC,CD3215,ACE,A1,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:A1
353S00807	2	IC,CD3215,ACE,B0,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:B0
353S00887	2	IC,CD3215,ACE,B0,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_B (BOOT CODE: 0002.08.07)
353S00888	2	IC,CD3215,ACE,B0,USB PWR SW,OTP=2,BGA96	U3100,U3200	CRITICAL	ACE:B0_2 (BOOT CODE: 0002.08.07)
353S00926	2	IC,CD3215,ACE,B03,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_3 (BOOT CODE: 0002.08.08)
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:C0

TBT ALPINE RIDGE

338S00160	1	IC,TBT,ALPINE RIDGE DP,QSJV,B1,6X6MM,BGA96	U2800	CRITICAL	TBT_AR:B1_QS
998-04160	1	IC,TBT,ALP-RIDGE DP,SLL44-TRAY,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ_TRAY
338S00176	1	IC,TBT,ALPN-RIDGE DP,SLL43-T&R,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ
338S00229	1	IC,TBT,ALPINE RIDGE,QSTY,QS,C0,CSP337	U2800	CRITICAL	TBT_AR:C0_QS
338S00249	1	IC,TBT,ALPINE RIDGE,QT5S,QS,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_QS
338S00254	1	IC,TBT,ALPINE RIDGE,SLLSM,PRQ,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_PRQ

WIRELESS MODULE

339S0250	1	MODULE,WIFI/BT,STELLA CIDRE,MUR,LGA80	U3700	CRITICAL	WIRELESS:MURATA
339S0251	1	MODULE,WIFI/BT,STELLA CIDRE,USI,LGA80	U3700	CRITICAL	WIRELESS:USI

Programmables (All Builds)

SMC

338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00334	1	IC,SMC-B1,EXT (V2.31A18) POC,X502	U5000	CRITICAL	SMC:POC
341S00429	1	IC,SMC-B1,EXT (V2.35A4) PROTO 1,X502	U5000	CRITICAL	SMC:PROTO1
341S00517	1	IC,SMC-B1,EXT (V2.35A51) PROTO 2,X502	U5000	CRITICAL	SMC:PROTO2
341S00562	1	IC,SMC-B1,EXT (V2.36A2) EVT,X502	U5000	CRITICAL	SMC:EVT
341S00611	1	IC,SMC-B1,EXT (V2.36A33) PRE-DVT,X502	U5000	CRITICAL	SMC:PREDVT
341S00633	1	IC,SMC-B1,EXT (V2.36A48) DVT,X502	U5000	CRITICAL	SMC:DVT
341S00662	1	IC,SMC-B1,EXT (V2.36F58) PVT,X502	U5000	CRITICAL	SMC:PVT

EFI ROM

335S0959	1	IC,SPI SERIAL FLASH,64M BITS,3V,CSP,QE=1	U6100	CRITICAL	BOOTROM:BLANK	MICRON
335S00006	335S0959	ALT_CMN	ALL		MACRONIX	
341S00389	1	IC,EFI (V0072) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO0	
341S00452	1	IC,EFI (V0093) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO1	
341S00513	1	IC,EFI (V0114) PROTO 2,X502	U6100	CRITICAL	BOOTROM:PROTO2	
341S00543	1	IC,EFI (V0130) PROTO 2.2,X502	U6100	CRITICAL	BOOTROM:PROTO2_2	
341S00573	1	IC,EFI (V0143) EVT,X502	U6100	CRITICAL	BOOTROM:EVT	
341S00673	1	IC,EFI (V0173) PVT,X502	U6100	CRITICAL	BOOTROM:PVT	

BT ROM

335S00024	1	IC,FLASH,USON8,512KBIT,75MHZ	U3770	CRITICAL	BT_ROM:BLANK
335S0837	335S00024	ALT_CMN	ALL	ALTERNATE	
341S00196	1	IC,BT ROM (V53) DVT,X261	U3770	CRITICAL	BT_ROM:X261
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PROTO0
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PVT

WIFI ROM

335S0956	1	IC,MEMORY,EEPROM,4K,1.7V-5.5V,UDFN8	U3780	CRITICAL	WIFI-ROM:BLANK
335S00145	335S0956	ALT_CMN	ALL	ALTERNATE	
341S00607	1	WIFI ROM (P175) PRE-DVT,WW1,X502	U3780	CRITICAL	WIFI-ROM:MURATA-FCC
341S00608	1	WIFI ROM (P175) PRE-DVT,WW2,X502	U3780	CRITICAL	WIFI-ROM:MURATA-ETSI
341S00609	1	WIFI ROM (P175) PRE-DVT,WW3,X502	U3780	CRITICAL	WIFI-ROM:MURATA-APAC
341S00610	1	WIFI ROM (P175) PRE-DVT,IND,X502	U3780	CRITICAL	WIFI-ROM:MURATA-IND
341S00636	1	WIFI ROM (P177) USI-WW1,X502	U3780	CRITICAL	WIFI-ROM:USI-FCC
341S00637	1	WIFI ROM (P177) USI-WW2,X502	U3780	CRITICAL	WIFI-ROM:USI-ETSI
341S00638	1	WIFI ROM (P177) USI-WW3,X502	U3780	CRITICAL	WIFI-ROM:USI-APAC
341S00639	1	WIFI ROM (P177) USI-IND,X502	U3780	CRITICAL	WIFI-ROM:USI-IND

TBT ROM

335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	AR_ROM:BLANK
341S00451	1	IC,NVM / AR (V0.8.15.E1) PROTO 1,X502	U2890	CRITICAL	AR_ROM:PROTO1
341S00512	1	IC,NVM (VB1-10.11-E2.6.3) PROTO 2,X502	U2890	CRITICAL	AR_ROM:PROTO2
341S00559	1	IC,NVM (V16.8) EVT,X502	U2890	CRITICAL	AR_ROM:EVT
341S00606	1	IC,NVM (V1.5) PRE-DVT,X502	U2890	CRITICAL	AR_ROM:PREDVT
341S00628	1	IC, NVM (V3.8), DVT, X502	U2890	CRITICAL	AR_ROM:DVT
341S00661	1	IC, NVM (VTBD), PVT, X502	U2890	CRITICAL	AR_ROM:PVT

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
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Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00101	4	IC,LPDDR3-1866,16GB,512MX32,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_8GB_1866
333S0784	4	IC,LPDDR3-1866,32GBIT,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_16GB_1866
333S00097	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_8GB_1866
333S00098	4	IC,LPDDR3-1866,32GB,1GX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_16GB_1866
333S00099	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_8GB_1866
333S00049	4	IC,SDRAM,LPDDR3-1866,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_16GB_1866

Main DRAM SPD Straps

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

	RAMCFG1	RAMCFG0
HYNIX	0 (STUFF R)	0 (STUFF R)
MICRON	0 (STUFF R)	1 (OPEN)
SAMSUNG	1 (OPEN)	0 (STUFF R)
-RESERVED-	1 (OPEN)	1 (OPEN)

	RAMCFG2
8GB	0 (STUFF R)
16GB	1 (OPEN)

	RAMCFG3
2133	0 (STUFF R)
1867	1 (OPEN)

	RAMCFG4
DIE A	0 (STUFF R)
DIE B	1 (OPEN)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0006	4	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1332,R1334		DRAM:HYNIX_8GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1334		DRAM:HYNIX_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1332,R1334		DRAM:MICRON_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1334		DRAM:MICRON_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1332,R1334		DRAM:SAMSUNG_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1334		DRAM:SAMSUNG_16GB_1866

MLB VERSION ID STRAPS

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE	INVERT TO VALUE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:POC	<11111>	<00000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:PROTO0	<11110>	<00001>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:PRE_PROTO1	<11101>	<00010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:PROTO1	<11100>	<00011>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:PROTO2	<11011>	<00100>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:PROTO2_2	<11010>	<00101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:EVT	<11001>	<00110>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:PREDVT	<11000>	<00111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:DVT	<10111>	<01000>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:DVT3	<10110>	<01001>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:PVT	<10101>	<01010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:PRQ1	<10100>	<01011>

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
107S00015	107S00011	ALT_CMN	ALL		TFT
107S00087	107S00029	ALT_CMN	ALL		YAGEO
107S00033	107S00034	ALT_CMN	ALL		TFT
107S00071	107S00053	ALT_CMN	ALL		YAGEO
107S00044	107S00076	ALT_CMN	ALL		CYNTEC
107S00070	107S0085	ALT_CMN	ALL		TDK
107S0248	107S0250	ALT_CMN	ALL		TFT
107S0249	107S0251	ALT_CMN	ALL		TFT
128S00009	128S00015	ALT_CMN	ALL		KEMET
128S00070	128S00015	ALT_CMN	ALL		PANASONIC
128S00010	128S00011	ALT_CMN	ALL		PANASONIC
128S00026	128S00011	ALT_CMN	ALL		NEC
128S00031	128S00011	ALT_CMN	ALL		ROHM
128S00058	128S00018	ALT_CMN	ALL		ROHM
128S00069	128S00067	ALT_CMN	ALL		ROHM
128S00062	128S00067	ALT_CMN	ALL		NEC
128S0364	128S0264	ALT_CMN	ALL		SANYO 2ND FACTORY
128S0311	128S0329	ALT_CMN	ALL		NEC ALT TO SANYO
128S0325	128S0397	ALT_CMN	ALL		PANASONIC
131S00134	131S00041	ALT_CMN	ALL		TAIYO YUDEN
132S00064	132S0409	ALT_CMN	ALL		MURATA
138S00077	138S00035	ALT_CMN	ALL		TAIYO YUDEN
138S00093	138S00035	ALT_CMN	ALL		KYOCERA
138S00084	138S00060	ALT_CMN	ALL		TAIYO YUDEN
138S0703	138S0648	ALT_CMN	ALL		MURATA
138S0700	138S0641	ALT_CMN	ALL		MURATA
138S0689	138S0701	ALT_CMN	ALL		MURATA
138S0864	138S0709	ALT_CMN	ALL		MULTIPLE
138S1103	138S0719	ALT_CMN	ALL		TAIYO YUDEN
138S0706	138S0739	ALT_CMN	ALL		MURATA
138S00106	138S0754	ALT_CMN	ALL		KYOCERA
138S00015	138S0777	ALT_CMN	ALL		MULTIPLE
138S0846	138S0811	ALT_CMN	ALL		SAMSUNG
138S00032	138S0831	ALT_CMN	ALL		TAIYO YUDEN
138S00049	138S0831	ALT_CMN	ALL		KYOCERA
138S0775	138S0860	ALT_CMN	ALL		SAMSUNG
138S00086	138S0884	ALT_CMN	ALL		TAIYO YUDEN
138S0738	138S1101	ALT_CMN	ALL		SAMSUNG
152S00381	152S1129	ALT_CMN	ALL		CHILISIN
152S00343	152S1682	ALT_CMN	ALL		MURATA
152S00363	152S00048	ALT_CMN	ALL		NEC
152S00358	152S00208	ALT_CMN	ALL		CHILISIN
152S00367	152S00266	ALT_CMN	ALL		NEC
152S00403	152S00322	ALT_CMN	ALL		CHILISIN
152S1872	152S00361	ALT_CMN	ALL		MURATA
155S0659	155S0382	ALT_CMN	ALL		MURATA
155S0694	155S0387	ALT_CMN	ALL		MURATA
155S00155	155S0441	ALT_CMN	ALL		TDK
155S0660	155S0513	ALT_CMN	ALL		MURATA
155S00007	155S0667	ALT_CMN	ALL		TAIYO YUDEN
155S00034	155S0706	ALT_CMN	ALL		MURATA
155S00203	155S0894	ALT_CMN	ALL		TAIYO YUDEN
155S00115	155S00114	ALT_CMN	ALL		MURATA

More Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
197S00046	197S00036	ALT_CMN	ALL		EPSON
197S00047	197S00036	ALT_CMN	ALL		KYOCERA
197S00048	197S00036	ALT_CMN	ALL		MURATA
197S00053	197S00050	ALT_CMN	ALL		KYOCERA
197S00054	197S00050	ALT_CMN	ALL		NDK
197S00055	197S00050	ALT_CMN	ALL		MURATA
311S00008	311S0271	ALT_CMN	ALL		DIODES INC
311S00060	311S0273	ALT_CMN	ALL		DIODES INC
311S00004	311S0370	ALT_CMN	ALL		ON SEMI
311S00013	311S0508	ALT_CMN	ALL		DIODES INC
311S00122	311S0543	ALT_CMN	ALL		DIODES INC
311S0596	311S0593	ALT_CMN	ALL		TI
311S00097	311S00036	ALT_CMN	ALL		DIODES INC
353S00711	353S2073	ALT_CMN	ALL		ON SEMI
353S00712	353S2216	ALT_CMN	ALL		ON SEMI
353S00107	353S3239	ALT_CMN	ALL		ON SEMI
353S00854	353S4342	ALT_CMN	ALL		ST MICRO
353S00769	353S4398	ALT_CMN	ALL		DIODES INC
353S00525	353S4471	ALT_CMN	ALL		VISHAY
371S0713	371S0558	ALT_CMN	ALL		DIODES INC
371S00074	371S0602	ALT_CMN	ALL		INFINEON
371S0704	371S00077	ALT_CMN	ALL		NXP
371S00089	371S00085	ALT_CMN	ALL		DIODES INC
372S0186	372S0185	ALT_CMN	ALL		NXP
372S00016	372S00015	ALT_CMN	ALL		DIODES INC
376S1053	376S0604	ALT_CMN	ALL		DIODES INC
376S1106	376S0678	ALT_CMN	ALL		FAIRCHILD
376S00014	376S0761	ALT_CMN	ALL		TOSHIBA
376S00086	376S0761	ALT_CMN	ALL		DIODES INC.
376S1080	376S0820	ALT_CMN	ALL		DIODES INC
376S00074	376S0855	ALT_CMN	ALL		TOSHIBA
376S00146	376S1061	ALT_CMN	ALL		ROHM
376S1089	376S1128	ALT_CMN	ALL		NXP
377S00031	377S0178	ALT_CMN	ALL		ON SEMI
377S00048	377S00017	ALT_CMN	ALL		ST MICRO
377S0155	377S00011	ALT_CMN	ALL		ON SEMI
740S0144	740S0118	ALT_CMN	ALL		LITTELFUSE
740S00028	740S0118	ALT_CMN	ALL		BUSSMANN
740S00003	740S0135	ALT_CMN	ALL		AEM, INC.
740S00027	740S0159	ALT_CMN	ALL		BOURNS
740S00033	740S00002	ALT_CMN	ALL		THINKING
740S00007	740S00019	ALT_CMN	ALL		BOURNS

BOM_COST_GROUP=NO COST ITEMS

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MOUNTING HOLES

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SH0400
4.0R3.6-NSP

SH0401
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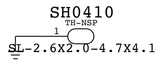
FAN MOUNTING HOLE

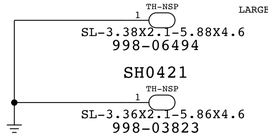
998-03850

SH0410
TH-NSP



PLATED HOLES

SH0420
TH-NSP
LARGER SLOT, NEAR ANTENNA



998-06494

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998-03823

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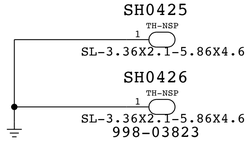

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SH0431
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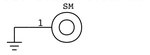

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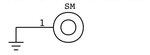

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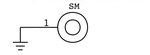

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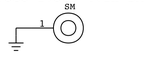

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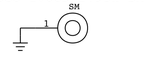

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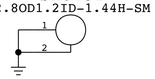

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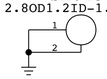

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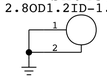

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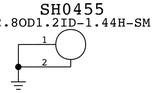

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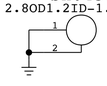

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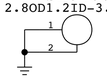

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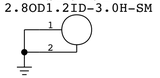

SHIELD CANS

MEMORY CAN - TOP

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07887	1	SHIELD CAN FENCE,DRAM,MN,X520	SHLD4	CRITICAL	SHIELD_CAN_MEMORY_TOP

MEMORY CAN - BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08894	1	SHIELD FENCE,BOT DRAM,SUS,PRE-MN,X520	SHLD1	CRITICAL	SHIELD_CAN_MEMORY_BOT

WIRELESS CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07884	1	SHIELD CAN,WIFI,BT,SYM,MN,TALL,X520	SHLD2	CRITICAL	SHIELD_CAN_WIFI

USB-C CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07885	1	SHIELD CAN,AR,USB-C,THRU,X520	SHLD3	CRITICAL	SHIELD_CAN_USBC

BOM_COST_GROUP=MECHANICALS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PD Parts

Apple Inc.

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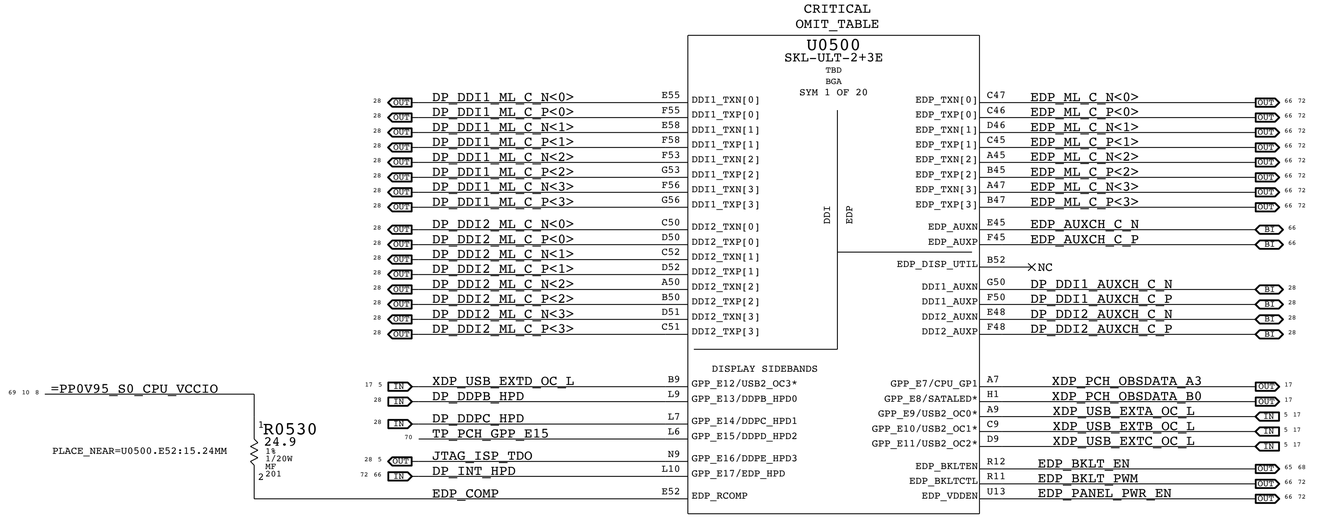

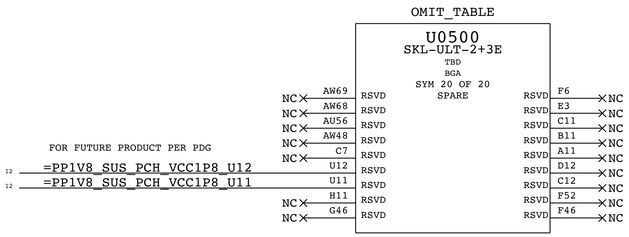

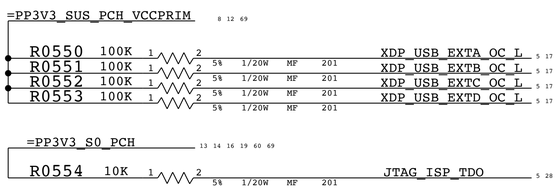

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
CPU GFX

Apple Inc.

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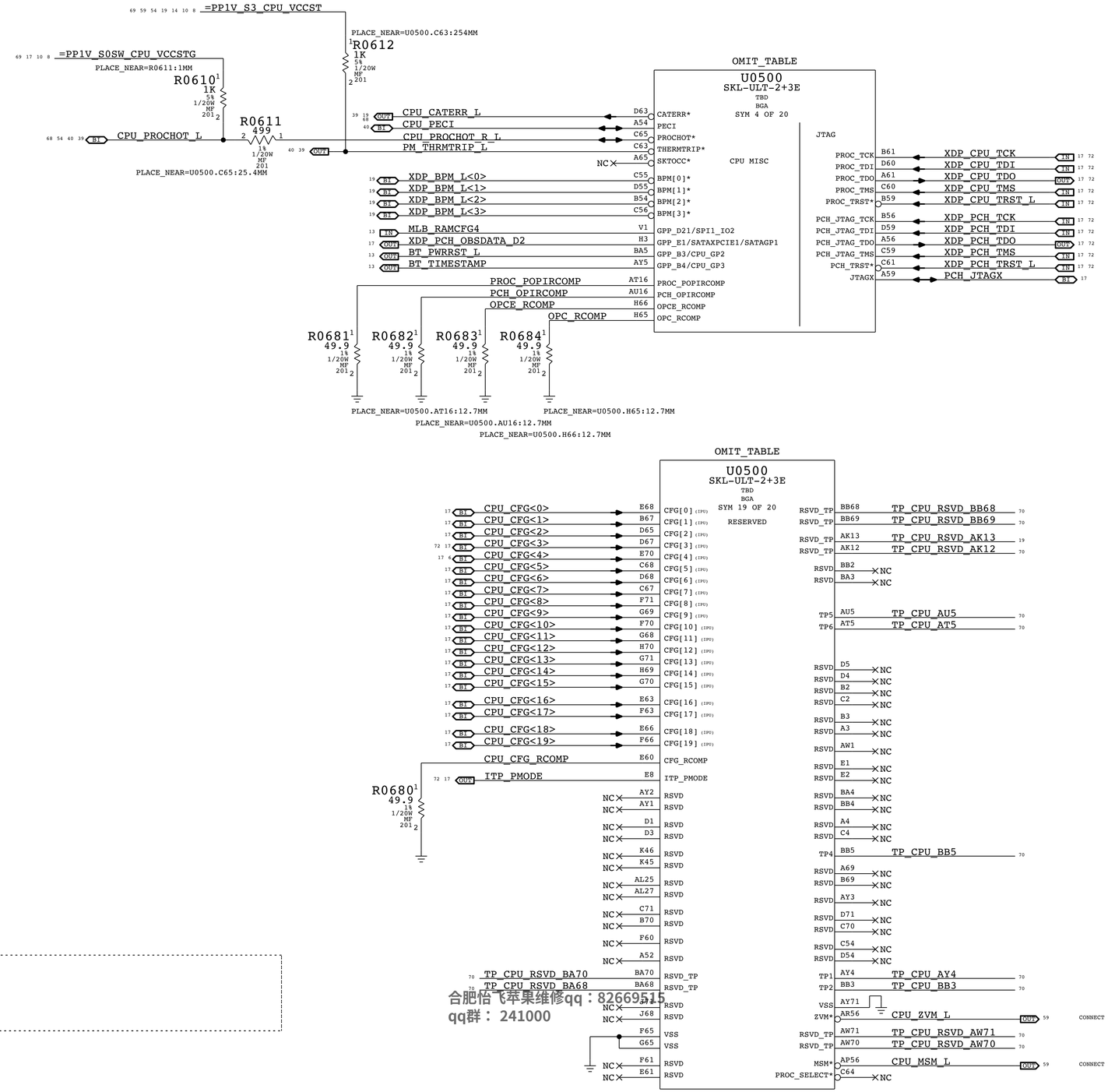

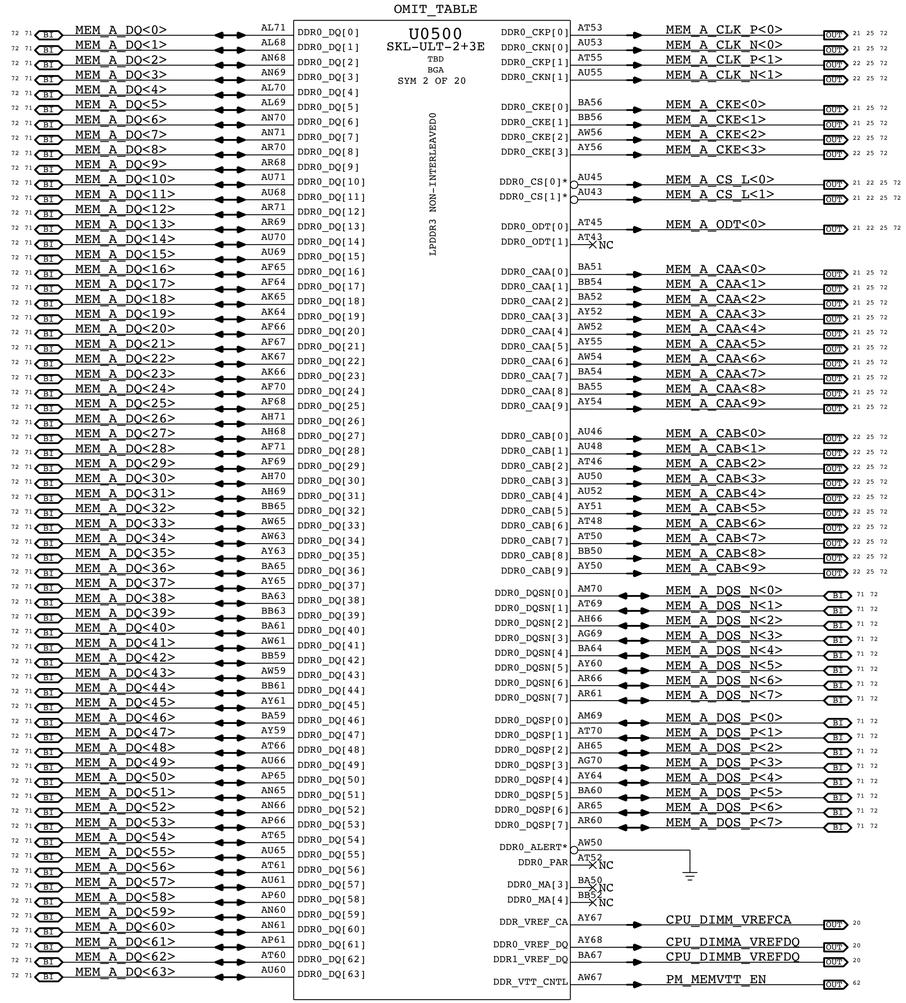

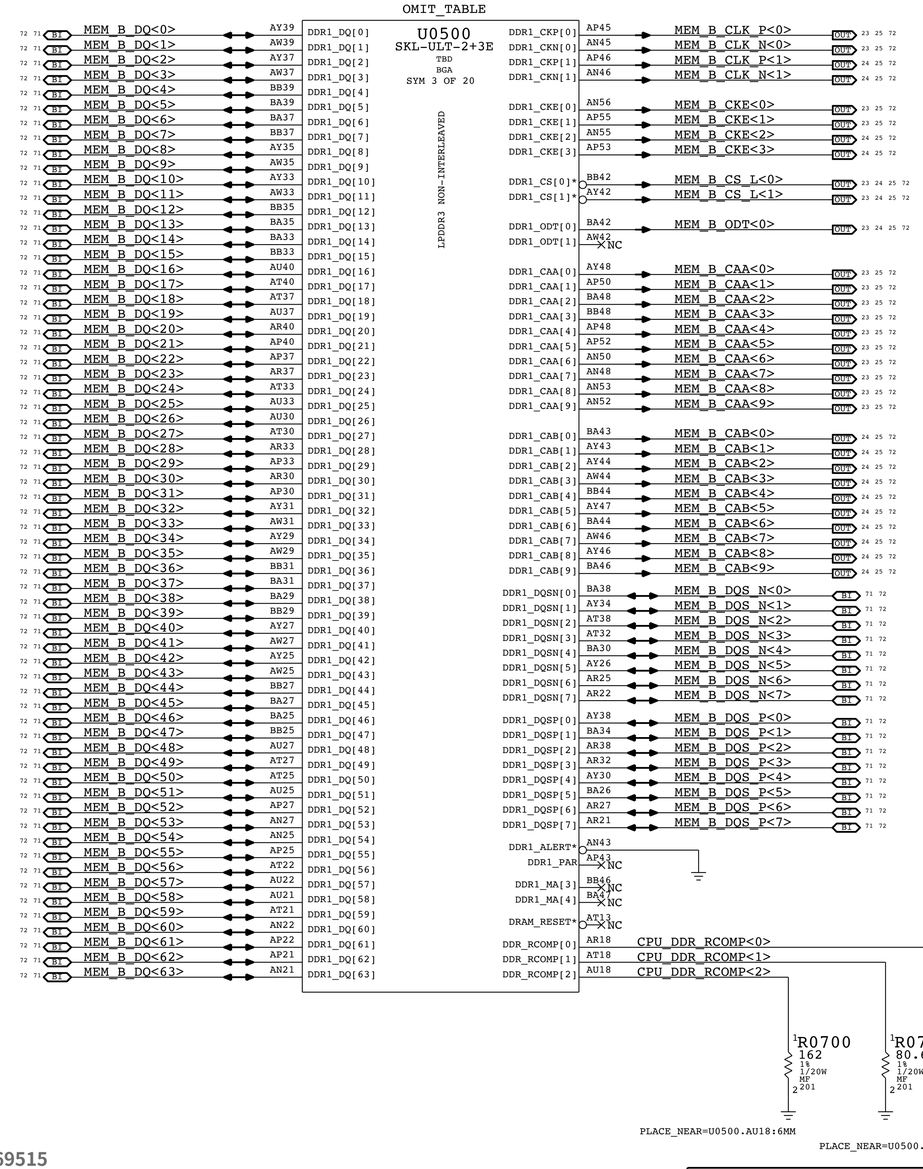

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SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

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CPU LPDDR3 Interface

Apple Inc.

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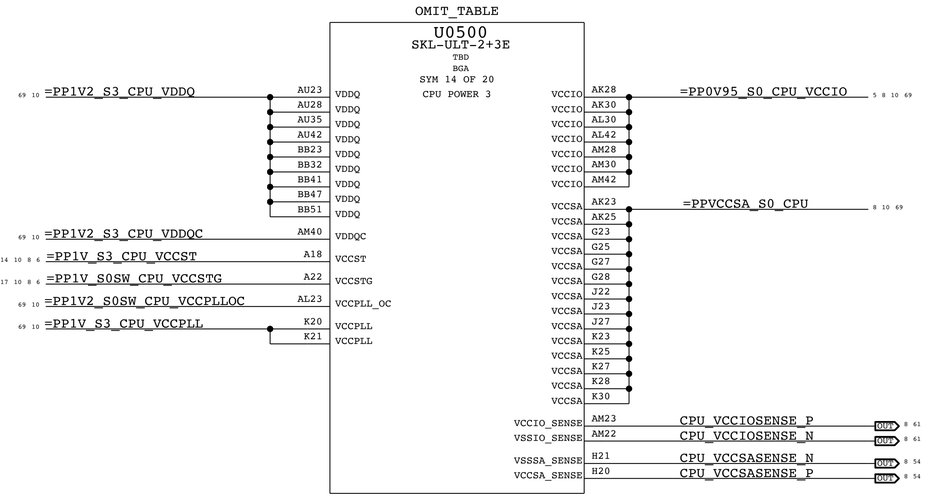

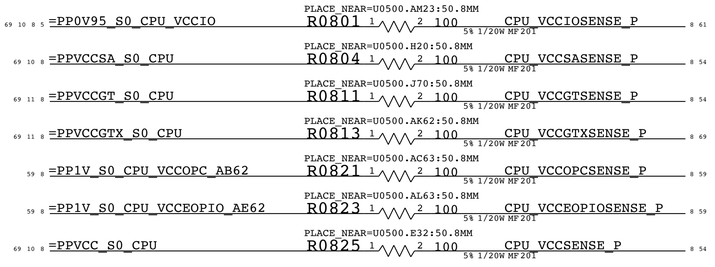

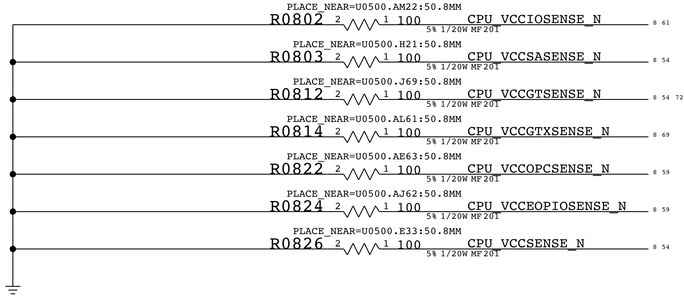

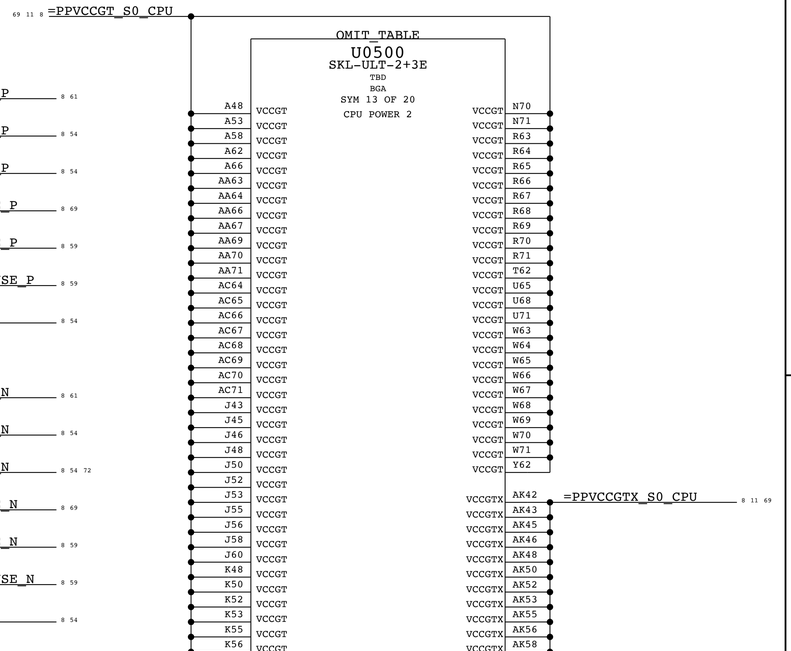

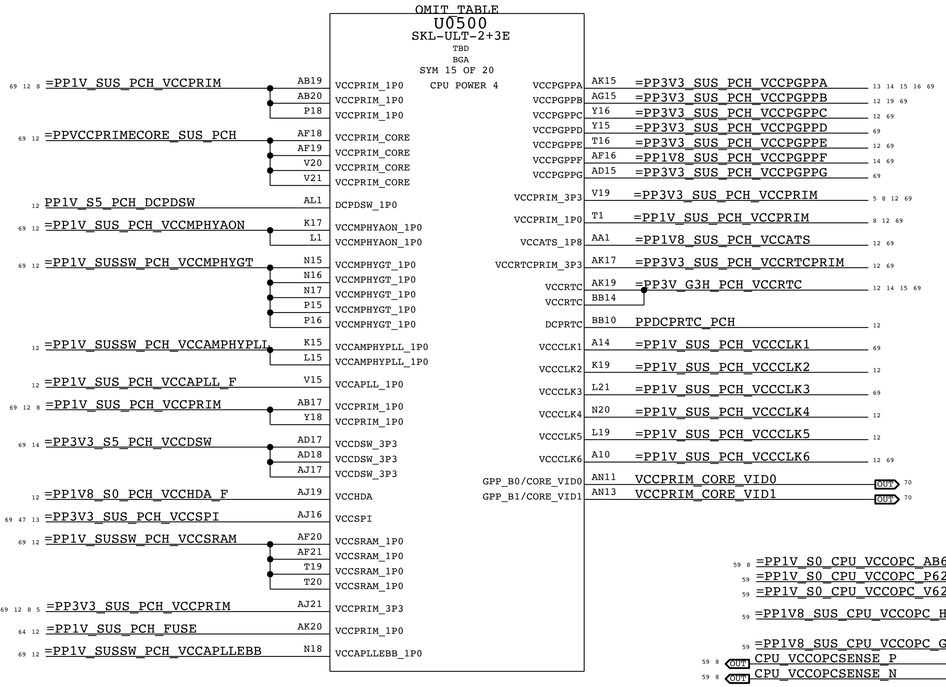

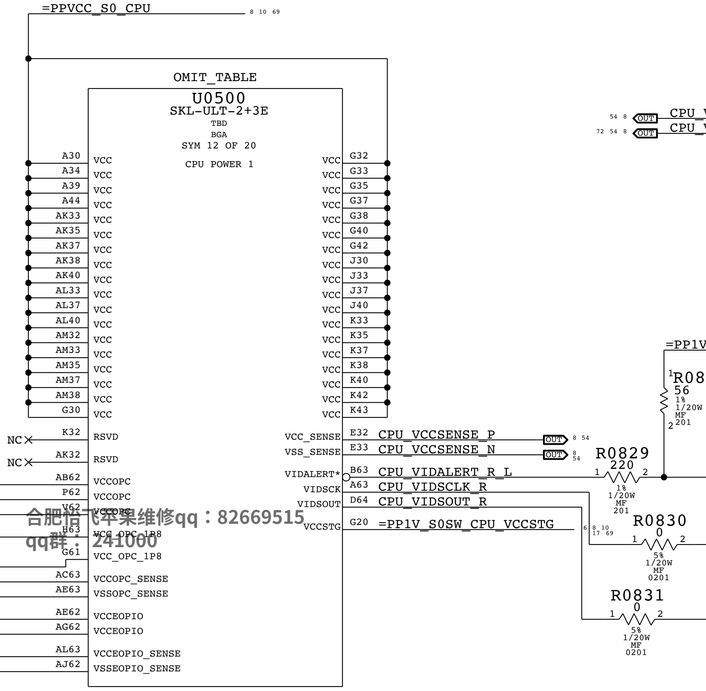

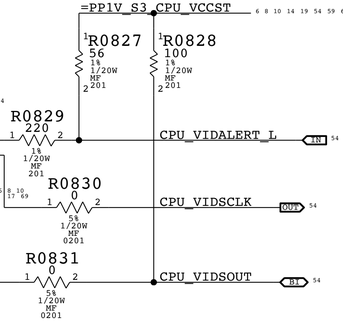

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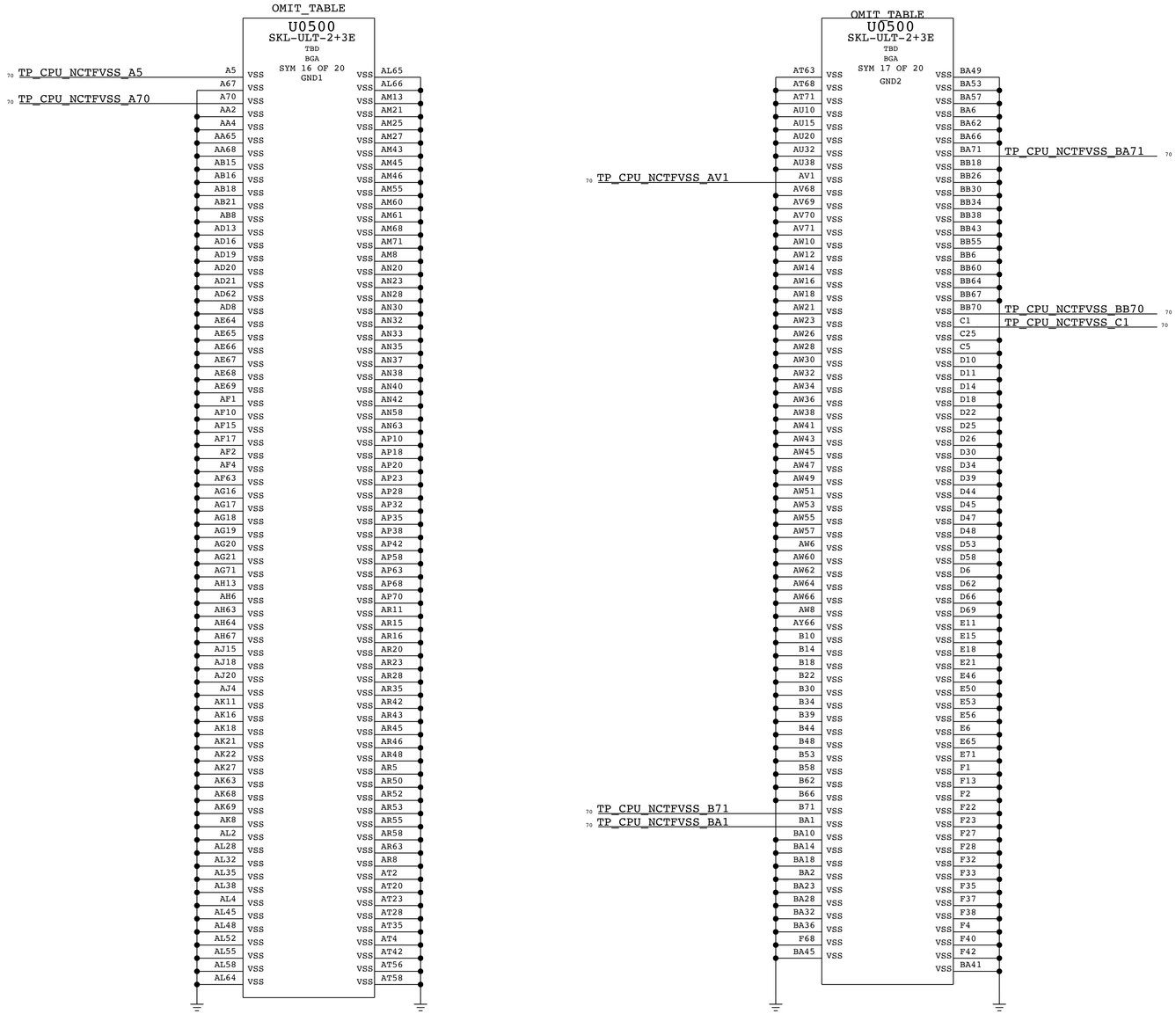

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CPU & PCH Grounds

Apple Inc.

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CRITICAL C10B1 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B2 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B3 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B4 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B5 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B6 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B7 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B8 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10B9 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10BA NOSTUFF 20UF 20% 2.5V X6S-CERM 0402

CRITICAL C10C0 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C1 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C2 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C3 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C4 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C5 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C6 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C7 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C8 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10C9 NOSTUFF 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C10CA NOSTUFF 20UF 20% 2.5V X6S-CERM 0402

CRITICAL C10H0 220UF 20% 2V ELEC SM-COMBO

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE
CPU Core Decoupling

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
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69 8 =PPVCCGT_S0_CPU

C1100 C1101 C1102 C1103 C1104 C1105 C1106 C1107 C1108 C1109 C110A C110B C110C C110D
1UF 20% 6.3V X6S-CERM 0201

C110E C110F C110G C110H C110I C110J C110K C110L C110M C110N C110O C110P C110Q C110R C110S C110T C110U C110V C110W C110X
1UF 20% 6.3V X6S-CERM 0201

C1110 C1111 C1112 C1113 C1114 C1115 C1116 C1117 C1118 C1119 C1130 C1131 C1132 C1133 C1134 C1135 C1136 C1137 C1138 C1139
NOSTUFF / CRITICAL 20UF 20% 2.5V X6S-CERM 0402

C1120 C1121 C1122 C1123 C1124 C1125 C1126 C1127 C1128 C1129 C1140 C1141 C1142 C1143 C1144 C1145 C1146 C1147 C1148 C1149
NOSTUFF / CRITICAL 20UF 20% 2.5V X6S-CERM 0402

C1160 C1161 C1162 C1163 C1164
CRITICAL / NOSTUFF 220UF 20% 2V ELEC SM-COMBO

69 8 =PPVCCGTX_S0_CPU

C1170 C1171 C1172 C1173 C1174 C1175 C1176 C1177 C1150 C1151 C1152 C1153 C1154 C1155 C1156 C1157
CRITICAL / NOSTUFF 20UF 20% 2.3V X6S-CERM 0402

C1180 C1181 C1182 C1183 C1184 C1185 C1186 C1187 C1194 C1195 C1196 C1197 C1198 C1199
CRITICAL / NOSTUFF 20UF 20% 2.3V X6S-CERM 0402

C1190 C1191
CRITICAL / NOSTUFF 220UF 20% 2V ELEC SM-COMBO

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU GT Decoupling

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D
REVISION: 1.0.0
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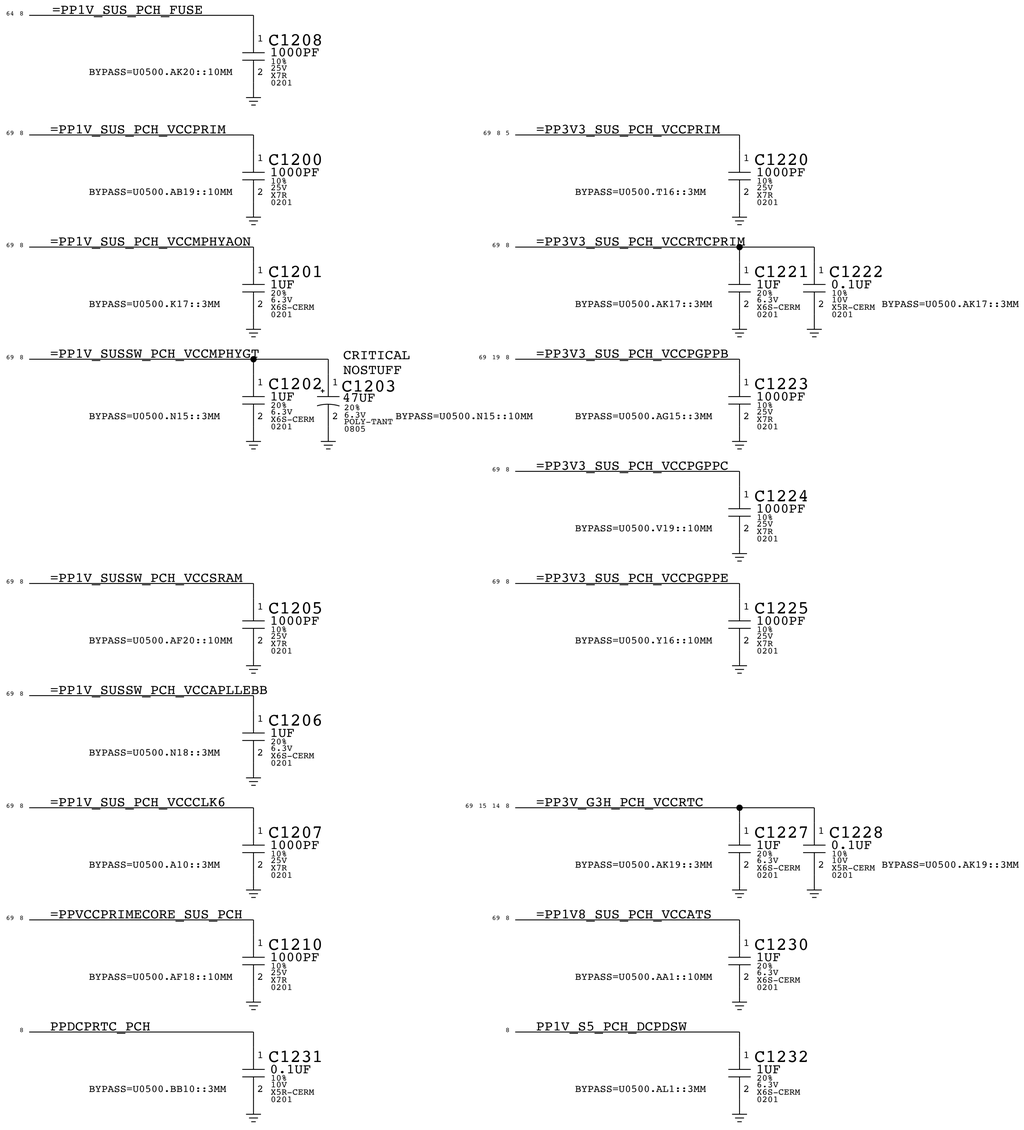
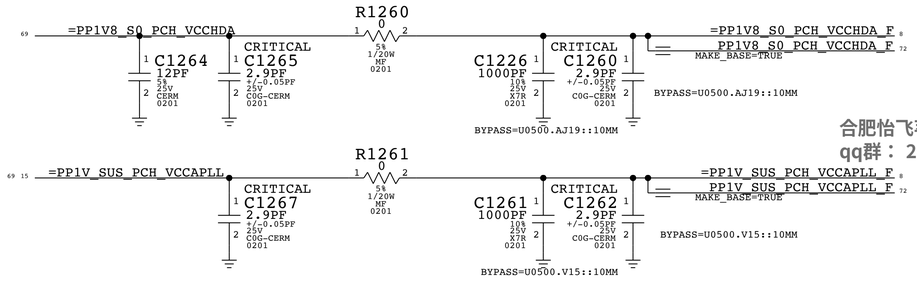
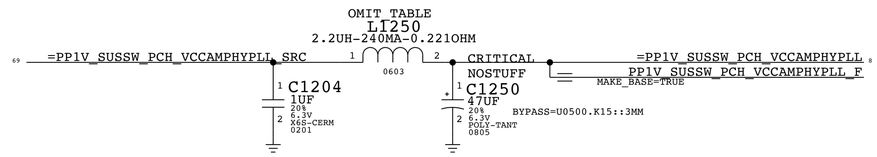


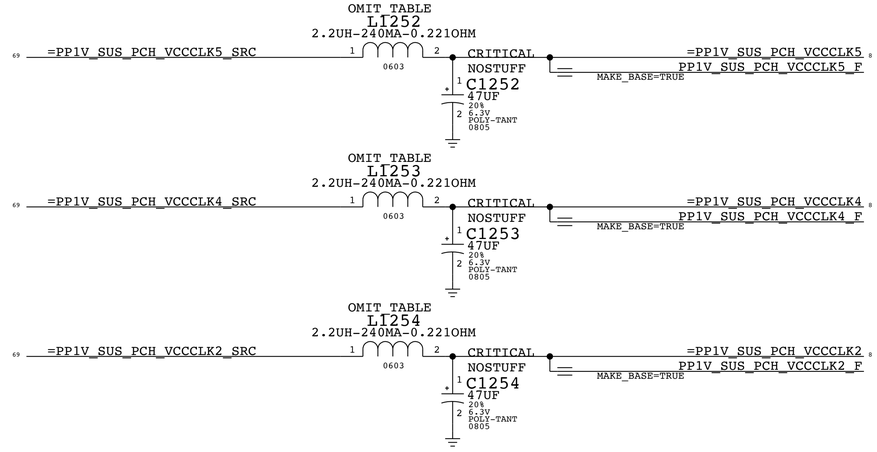
CPU CIRCUITS GENERATE NOISE AT WIFI BAND FREQUENCIES.
USE SPECIFIC 3PF CAPS FOR BEST FILTERING OF THOSE FREQUNCIES.



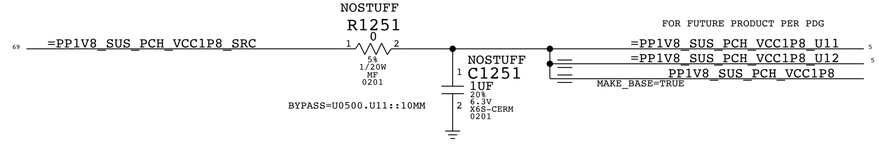
FILTER PLACEHOLDERS ONLY

RAIL SIDE PCH SIDE





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,0OHM,5%,0603	L1250,L1252,L1253,L1254		



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH Decoupling

Apple Inc.

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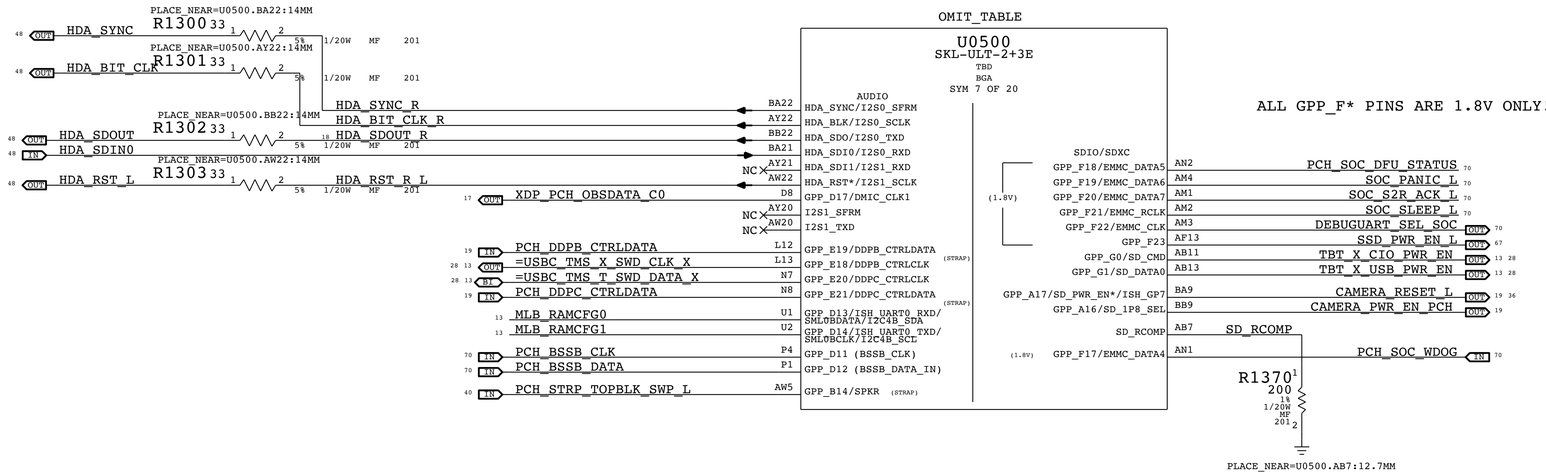
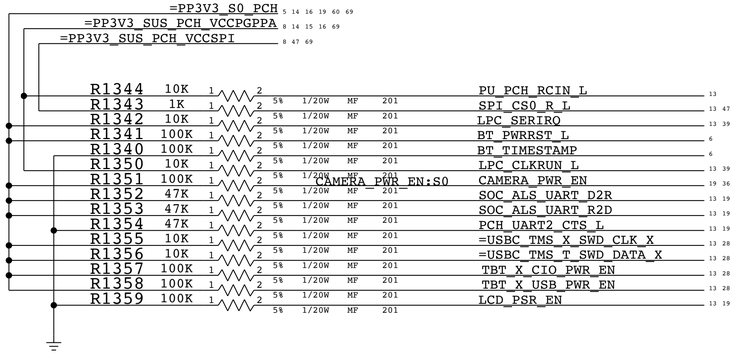
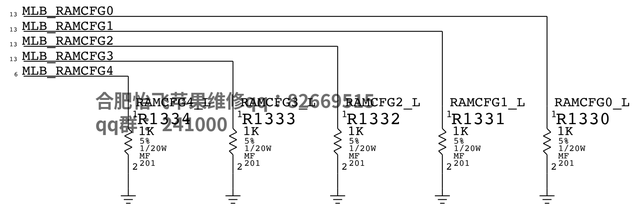




MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016
PAGE TITLE: PCH Audio/LPC/SPI/SMBus
Apple Inc.
DRAWING NUMBER: 051-02265
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PCH Reset Button

=PP3V3_SUS_PCH_VCCPGPPA
=PP3V3_S0_PCH
=PP1V_S3_CPU_VCCST

R1405 1K 5% 1/20W MF 201
NOSTUFF R1407 2.2K 5% 1/20W MF 201
R1408 2.2K 5% 1/20W MF 201

PM_SYSRST_L
CPU_VCCST_PWRGD
VCCST_PWRGD 1V TOLERANT
PM_DSW_PWRGD

R1406 60.4 1% 1/20W MF 201
PLACE_NEAR=U0500.B65:38mm

R1403 100K 5% 1/20W MF 201

NO STUFF R1400 0 5% 1/20W MF 0201

R1400 kept for debug purposes.

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 11 OF 20
SYSTEM POWER MANAGEMENT

PLT_RST_L	AN10	GPP_B13/PLTRST*	
	B5	SYS_RESET*	
PM_RSMRST_L	AY17	RSMRST*	
TP_CPU_PWRGD	A68	PROCPWRGD	
CPU_VCCST_PWRGD_R	B65	VCCST_PWRGD (1V ONLY)	
PM_PCH_SYS_PWROK	B6	SYS_PWROK	
PM_PCH_PWROK	BA20	PCH_PWROK	
	BB20	DSW_PWROK	
PCH_SUSWARN_L	AR13	GPP_A13/SUSWARN*/SUSPWRDNACK	
PCH_SUSACK_L	AP11	GPP_A15/SUSACK*	
PCIE_WAKE_L	BB15	WAKE*	
SMC_WAKE_SCI_L	AM15	GPD2/LAN_WAKE*	
TP_PCH_LANPHYPC	AW17	GPD11/LANPHYPC	
TP_PCH_GPD7	AT15	GPD7/RSVD	

PM_SLP_S0_L	AT11	GPP_B12/SLP_S0*	
PM_SLP_S3_L	AP15	GPD4/SLP_S3*	
PM_SLP_S4_L	BA16	GPD5/SLP_S4*	
PM_SLP_S5_L	AY16	GPD10/SLP_S5*	
PM_SLP_SUS_L	AN15	SLP_SUS*	
NC	AW15	SLP_LAN*	
TP_PCH_SLP_WLAN_L	BB17	GPD9/SLP_WLAN*	
TP_PCH_SLP_A_L	AN16	GPD6/SLP_A*	
PCH_PWRBTN_L	BA15	GPD3/PWRBTN*	
SSD_SR_EN_L	AY15	GPD1/ACPRESENT	
PM_BATLOW_L	AU13	GPD0/BATLOW*	
TP_PCH_PME_L	AU11	GPP_A11/PME*	
PCH_INTRUDER_L	AP16	INTRUDER*	
PCH_HSIO_PWR_EN	AM10	GPP_B11/EXT_PWR_GATE*	
BT_LOW_PWR_L	AM11	GPP_B2/VRALERT*	

=PP3V_G3H_PCH_VCCRTC
R1401 1M 5% 1/20W MF 201

=PP1V8_SUS_PCH_VCCPGPPF
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S4_PCH
=PP3V3_S0_PCH

R1446	100K		PCH_SWD_CLK
R1445	100K		PCH_SWD_IO
R1444	100K		PCH_SWD_MUX_SEL
NOSTUFF R1443	100K		SOC_S2R_L
R1442	100K		SSD_BOOT_L
R1441	10K		BT_LOW_PWR_L
R1440	100K		SSD_SR_EN_L
R1450	1K		PCH_PWRBTN_L
R1451	10K		PM_BATLOW_L
R1452	10K		PCIE_WAKE_L
R1453	100K		SMC_WAKE_SCI_L
R1454	100K		PM_SLP_S5_L
R1455	100K		PM_SLP_S4_L
R1456	100K		PM_SLP_S3_L
R1457	220K		PM_SLP_S0_L
R1458	100K		PM_SLP_SUS_L

NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 9 OF 20

CSI-2

NC	A36	CSI2_DN0	
NC	B36	CSI2_DP0	
NC	C38	CSI2_DN1	
NC	D38	CSI2_DP1	
NC	C36	CSI2_DN2	
NC	D36	CSI2_DP2	
NC	A38	CSI2_DN3	
NC	B38	CSI2_DP3	
NC	C31	CSI2_DN4	
NC	D31	CSI2_DP4	
NC	C33	CSI2_DN5	
NC	D33	CSI2_DP5	
NC	A31	CSI2_DN6	
NC	B31	CSI2_DP6	
NC	A33	CSI2_DN7	
NC	B33	CSI2_DP7	
NC	A29	CSI2_DN8	
NC	B29	CSI2_DP8	
NC	C28	CSI2_DN9	
NC	D28	CSI2_DP9	
NC	A27	CSI2_DN10	
NC	B27	CSI2_DP10	
NC	C27	CSI2_DN11	
NC	D27	CSI2_DP11	

NC	C37	CSI2_CLKN0	
NC	D37	CSI2_CLKP0	
NC	C32	CSI2_CLKN1	
NC	D32	CSI2_CLKP1	
NC	C29	CSI2_CLKN2	
NC	D29	CSI2_CLKP2	
NC	B26	CSI2_CLKN3	
NC	A26	CSI2_CLKP3	
CSI2_COMP	E13	CSI2_COMP	
TP_PCH_GPP_D0	M1	GPP_D0/SPI1_CS*	

R1480 100 1% 1/20W MF 201
PLACE_NEAR=U0500.E13:12.7MM

ALL GPP_F* PINS ARE 1.8V ONLY!

EMMC (1.8V)

SSD_BOOT_L	AH12	GPP_F7/I2C3_SCL
TP_PCH_GPP_F8	AF11	GPP_F8/I2C4_SDA
TP_PCH_GPP_F9	AF12	GPP_F9/I2C4_SCL
TP_PCH_GPP_F10	AD11	GPP_F10/I2C5_SDA/ISH_I2C2_SDA
PCH_BT_ROM_BOOT	AD12	GPP_F11/I2C5_SCL/ISH_I2C2_SCL
PCH_SWD_CLK	AP4	GPP_F12/EMMC_CMD
PCH_SWD_IO	AP2	GPP_F13/EMMC_DATA0
PCH_SWD_MUX_SEL	AP1	GPP_F14/EMMC_DATA1
SOC_S2R_L	AP3	GPP_F15/EMMC_DATA2
PCH_SOC_FORCE_DFU	AN3	GPP_F16/EMMC_DATA3
UPC_I2C_INT_L	AH11	GPP_F6/I2C3_SDA
EMMC_RCOMP	AT1	EMMC_RCOMP

R1481 200 1% 1/20W MF 201
PLACE_NEAR=U0500.AT1:12.7MM

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH Power Management

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
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PCIe Port Assignments:

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

SSD LANE 0
PCIE_SSD_D2R_N<0> H13 PCIE1_RXN/USB3_5_RXN
PCIE_SSD_D2R_P<0> G13 PCIE1_RXP/USB3_5_RXP
PCIE_SSD_R2D_C_N<0> B17 PCIE1_TXN/USB3_5_TXN
PCIE_SSD_R2D_C_P<0> A17 PCIE1_TXP/USB3_5_TXP

SSD LANE 1
PCIE_SSD_D2R_N<1> G11 PCIE2_RXN/USB3_6_RXN
PCIE_SSD_D2R_P<1> F11 PCIE2_RXP/USB3_6_RXP
PCIE_SSD_R2D_C_N<1> D16 PCIE2_TXN/USB3_6_TXN
PCIE_SSD_R2D_C_P<1> C16 PCIE2_TXP/USB3_6_TXP

SSD LANE 2
PCIE_SSD_D2R_N<2> H16 PCIE3_RXN
PCIE_SSD_D2R_P<2> G16 PCIE3_RXP
PCIE_SSD_R2D_C_N<2> D17 PCIE3_TXN
PCIE_SSD_R2D_C_P<2> C17 PCIE3_TXP

SSD LANE 3
PCIE_SSD_D2R_N<3> G15 PCIE4_RXN
PCIE_SSD_D2R_P<3> F15 PCIE4_RXP
PCIE_SSD_R2D_C_N<3> B19 PCIE4_TXN
PCIE_SSD_R2D_C_P<3> A19 PCIE4_TXP

Thunderbolt X lane 0
PCIE_TBT_X_D2R_N<0> F16 PCIE5_RXN
PCIE_TBT_X_D2R_P<0> E16 PCIE5_RXP
PCIE_TBT_X_R2D_C_N<0> C19 PCIE5_TXN
PCIE_TBT_X_R2D_C_P<0> D19 PCIE5_TXP

Thunderbolt X lane 1
PCIE_TBT_X_D2R_N<1> G18 PCIE6_RXN
PCIE_TBT_X_D2R_P<1> F18 PCIE6_RXP
PCIE_TBT_X_R2D_C_N<1> D20 PCIE6_TXN
PCIE_TBT_X_R2D_C_P<1> C20 PCIE6_TXP

Thunderbolt X lane 2
PCIE_TBT_X_D2R_N<2> F20 PCIE7_RXN/SATA0_RXN
PCIE_TBT_X_D2R_P<2> E20 PCIE7_RXP/SATA0_RXP
PCIE_TBT_X_R2D_C_N<2> B21 PCIE7_TXN/SATA0_TXN
PCIE_TBT_X_R2D_C_P<2> A21 PCIE7_TXP/SATA0_TXP

Thunderbolt X lane 3
PCIE_TBT_X_D2R_N<3> G21 PCIE8_RXN/SATA1A_RXN
PCIE_TBT_X_D2R_P<3> F21 PCIE8_RXP/SATA1A_RXP
PCIE_TBT_X_R2D_C_N<3> D21 PCIE8_TXN/SATA1A_TXN
PCIE_TBT_X_R2D_C_P<3> C21 PCIE8_TXP/SATA1A_TXP

AirPort
PCIE_AP_D2R_N E22 PCIE9_RXN
PCIE_AP_D2R_P E23 PCIE9_RXP
PCIE_AP_R2D_C_N B23 PCIE9_TXN
PCIE_AP_R2D_C_P A23 PCIE9_TXP

CAMERA
PCIE_CAMERA_D2R_N F25 PCIE10_RXN
PCIE_CAMERA_D2R_P E25 PCIE10_RXP
PCIE_CAMERA_R2D_C_N D23 PCIE10_TXN
PCIE_CAMERA_R2D_C_P C23 PCIE10_TXP

PLACE_NEAR=U0500.F5:12.7mm
R1504 1 100 1% 1/20W MF 201 2
PCH_PCIE_RCOMP_N F5 PCIE_RCOMPN
PCH_PCIE_RCOMP_P E5 PCIE_RCOMPP

XDP_CPU_PRDY_L D56 PROC_PRDY*
XDP_CPU_PREQ_L D61 PROC_PREQ*
SMC_RUNTIME_SCI_L BB11 GPP_A7/PIRQA*

Thunderbolt T lane 0
PCIE_TBT_T_D2R_N<0> E28 PCIE11_RXN/SATA1B_RXN
PCIE_TBT_T_D2R_P<0> E27 PCIE11_RXP/SATA1B_RXP
PCIE_TBT_T_R2D_C_N<0> D24 PCIE11_TXN/SATA1B_TXN
PCIE_TBT_T_R2D_C_P<0> C24 PCIE11_TXP/SATA1B_TXP

Thunderbolt T lane 1
PCIE_TBT_T_D2R_N<1> E30 PCIE12_RXN/SATA2_RXN
PCIE_TBT_T_D2R_P<1> F30 PCIE12_RXP/SATA2_RXP
PCIE_TBT_T_R2D_C_N<1> A25 PCIE12_TXN/SATA2_TXN
PCIE_TBT_T_R2D_C_P<1> B25 PCIE12_TXP/SATA2_TXP

PCIE/USB3/SATA

SSIC/USB3
USB3_1_RXN H8 USB3_EXTA_D2R_N
USB3_1_RXP G8 USB3_EXTA_D2R_P
USB3_1_TXN C13 USB3_EXTA_R2D_C_N
USB3_1_TXP D13 USB3_EXTA_R2D_C_P
EXT A (SS,DCI)

USB3_2_RXN/SSIC_RXN J6 USB3_EXTB_D2R_N
USB3_2_RXP/SSIC_RXP H6 USB3_EXTB_D2R_P
USB3_2_TXN/SSIC_TXN B13 USB3_EXTB_R2D_C_N
USB3_2_TXP/SSIC_TXP A13 USB3_EXTB_R2D_C_P
EXT B (SS)

USB3_3_RXN J10 TP_USB3_03_D2RN
USB3_3_RXP H10 TP_USB3_03_D2RP
USB3_3_TXN B15 TP_USB3_03_R2DN
USB3_3_TXP A15 TP_USB3_03_R2DP

USB3_4_RXN E10 TP_USB3_04_D2RN
USB3_4_RXP F10 TP_USB3_04_D2RP
USB3_4_TXN C15 TP_USB3_04_R2DN
USB3_4_TXP D15 TP_USB3_04_R2DP

USB2
USB2N_1 AB9 USB_EXTA_N
USB2P_1 AB10 USB_EXTA_P
EXT A (LS/FS/HS)

USB2N_2 AD6 USB_EXTB_N
USB2P_2 AD7 USB_EXTB_P
EXT B (LS/FS/HS)

USB2N_3 AH3 USB_CAMERA_DFR_N
USB2P_3 AJ3 USB_CAMERA_DFR_P
USB2N_4 AD9 TP_USB_TESTERN
USB2P_4 AD10 TP_USB_TESTERP
USB2N_5 AJ1 NC_USB2_05N
USB2P_5 AJ2 NC_USB2_05P
USB2N_6 AF6 NC_USB2_06N
USB2P_6 AF7 NC_USB2_06P
USB2N_7 AH1 NC_USB2_07N
USB2P_7 AH2 NC_USB2_07P
USB2N_8 AF8 NC_USB2_08N
USB2P_8 AF9 NC_USB2_08P
USB2N_9 AG1 NC_USB2_09N
USB2P_9 AG2 NC_USB2_09P
USB2N_10 AH7 NC_USB2_10N
USB2P_10 AH8 NC_USB2_10P

USB2_COMP AB6 PCH_USB2_COMP
USB2_ID AG3
USB2_VBUSSENSE AG4 PCH_USB2_VBUSSENSE
GROUNDED PER SKYLAKE MOW 2015WW10.
R1503 1K 5% 1/20W MF 201
R1501 113 1% 1/20W MF 201
PLACE_NEAR=U0500.AB6:12.7MM
PLACE_NEAR=U0500.AG4:12.7MM

GPP_E3/CPU_GP0 A6 XDP_PCH_OBSFN_C1
GPP_E4/DEVSLP0 J1 XDP_JTAG_ISP_TCK
GPP_E5/DEVSLP1 J2 XDP_JTAG_ISP_TDI
GPP_E6/DEVSLP2 J3 XDP_PCH_OBSDATA_A2
GPP_D22/SPI1_IO3 V2 SPKR_ID0
GPP_D23/I2S_MCLK J5 XDP_PCH_OBSDATA_D0
GPP_E0/SATAXPCIE0/SATAGP0 H2 XDP_PCH_OBSDATA_D1
GPP_D18/DMIC_DATA1 C8 XDP_PCH_OBSDATA_C1
GPP_D19/DMIC_CLK0 H5 XDP_PCH_OBSDATA_C2
GPP_D20/DMIC_DATA0 D7 XDP_PCH_OBSDATA_C3
GPP_E2/SATAXPCIE2/SATAGP2 G4 XDP_PCH_OBSDATA_D3

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20

CLOCK SIGNALS

PCIE_CLK100M_SSD_N D42 CLKOUT_PCIE_N0
PCIE_CLK100M_SSD_P C42 CLKOUT_PCIE_P0
=SSD_CLKREQ_L AR10 GPP_B5/SRCCLKREQ0*

PCIE_CLK100M_TBT_X_N B42 CLKOUT_PCIE_N1
PCIE_CLK100M_TBT_X_P A42 CLKOUT_PCIE_P1
=TBT_X_CLKREQ_L AT7 GPP_B6/SRCCLKREQ1*

PCIE_CLK100M_TBT_T_N D41 CLKOUT_PCIE_N2
PCIE_CLK100M_TBT_T_P C41 CLKOUT_PCIE_P2
=TBT_T_CLKREQ_L AT8 GPP_B7/SRCCLKREQ2*

PCIE_CLK100M_AP_N D40 CLKOUT_PCIE_N3
PCIE_CLK100M_AP_P C40 CLKOUT_PCIE_P3
=AP_CLKREQ_L AT10 GPP_B8/SRCCLKREQ3*

PCIE_CLK100M_CAMERA_N B40 CLKOUT_PCIE_N4
PCIE_CLK100M_CAMERA_P A40 CLKOUT_PCIE_P4
=CAMERA_CLKREQ_L AU8 GPP_B9/SRCCLKREQ4*

TP_PCIE_CLK100M5N E40 CLKOUT_PCIE_N5
TP_PCIE_CLK100M5P E38 CLKOUT_PCIE_P5
TP_PCH_CLKREQ5_L AU7 GPP_B10/SRCCLKREQ5*

CLKOUT_ITPXDP_N F43 TP_ITPXDP_CLK100MN
CLKOUT_ITPXDP_P E43 TP_ITPXDP_CLK100MP
GPD8/SUSCLK BA17 PM_CLK32K_SUSCLK_R
XTAL24_IN E37 PCH_CLK24M_XTALIN
XTAL24_OUT E35 PCH_CLK24M_XTALOUT
XCLK_BIASREF E42 PCH_DIFFCLK_BIASREF
RTCX1 AM18 PCH_CLK32K_RTCX1
RTCX2 AM20 PCH_CLK32K_RTCX2
SRTCRST* AN18 PCH_SRTCRST_L
RTCRST* AM16 RTC_RESET_L

=PP1V_SUS_PCH_VCCAPLL
PLACE_NEAR=U0500.E42:2.54mm
R1520 2.7K 1% 1/20W MF 201
=PP3V_G3H_PCH_VCCRTC
R1530 20K 1% 1/20W MF 201
R1531 20K 1% 1/20W MF 201
C1530 1UF 20% 6.3V X6S-CERM 0201
C1531 1UF 20% 6.3V X6S-CERM 0201

=PP3V3_SUS_PCH_VCCPGPPA
R1550 100K 5% 1/20W MF 201 SMC_RUNTIME_SCI_L

BOM_COST_GROUP=CPU & CHIPSET

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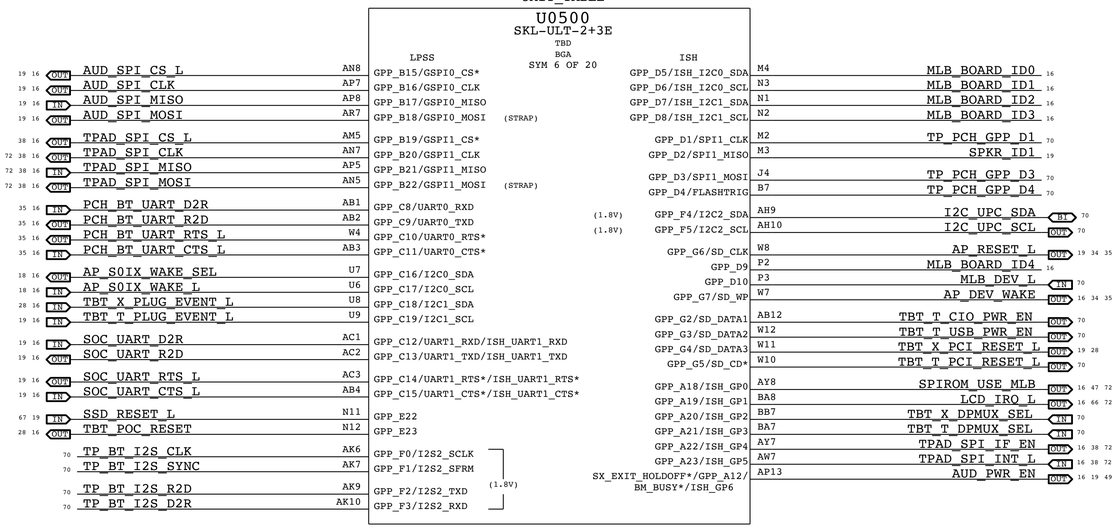
ALL GPP_F* PINS ARE 1.8V ONLY!

OMIT_TABLE



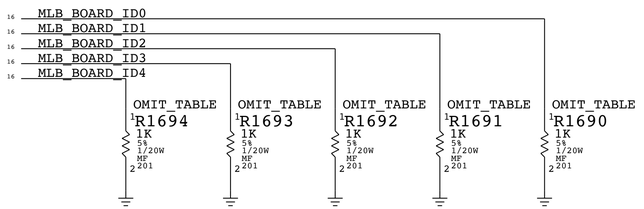
=PP3V3_S0_PCH 5 13 14 19 60 69

=PP3V3_SUS_PCH_VCCPGPPA 8 13 14 15 69

R1643	47K	1	2	5%	1/20W	MF	201	SOC_UART_D2R	16 19
R1642	47K	1	2	5%	1/20W	MF	201	SOC_UART_R2D	16 19
R1641	47K	1	2	5%	1/20W	MF	201	SOC_UART_RTS_L	16 19
R1640	47K	1	2	5%	1/20W	MF	201	SOC_UART_CTS_L	16 19
R1650	100K	1	2	5%	1/20W	MF	201	SPIROM_USE_MLB	16 47 72
R1652	100K	1	2	AUD_PWR_EN:S0				AUD_PWR_EN	16 19 49
R1653	47K	1	2	5%	1/20W	MF	201	AUD_SPI_CS_L	16 19
R1654	47K	1	2	5%	1/20W	MF	201	AUD_SPI_CLK	16 19
R1655	47K	1	2	5%	1/20W	MF	201	AUD_SPI_MISO	16 19
R1656	1K	1	2	5%	1/20W	MF	201	AUD_SPI_MOSI	16 19
R1657	47K	1	2	5%	1/20W	MF	201	TPAD_SPI_CS_L	16 38
R1658	47K	1	2	5%	1/20W	MF	201	TPAD_SPI_CLK	16 38 72
R1659	47K	1	2	5%	1/20W	MF	201	TPAD_SPI_MISO	16 38 72
R1660	150K	1	2	5%	1/20W	MF	201	TPAD_SPI_MOSI	16 38 72
R1674	100K	1	2	5%	1/20W	MF	201	TPAD_SPI_INT_L	16 38 72
R1673	100K	1	2	5%	1/20W	MF	201	TPAD_SPI_IF_EN	16 38 72
R1661	47K	1	2	5%	1/20W	MF	201	PCH_BT_UART_D2R	16 35
R1662	47K	1	2	5%	1/20W	MF	201	PCH_BT_UART_R2D	16 35
R1663	47K	1	2	5%	1/20W	MF	201	PCH_BT_UART_RTS_L	16 35
R1664	47K	1	2	5%	1/20W	MF	201	PCH_BT_UART_CTS_L	16 35
R1665	100K	1	2	5%	1/20W	MF	201	AP_S0IX_WAKE_SEL	16 18
R1666	100K	1	2	5%	1/20W	MF	201	AP_S0IX_WAKE_L	16 18
R1667	100K	1	2	5%	1/20W	MF	201	AP_DEV_WAKE	16 34 35
R1669	100K	1	2	5%	1/20W	MF	201	LCD_IRQ_L DRIVEN PUSH PULL FROM SWITCHED RAIL.	16 66 72
R1668	100K	1	2	5%	1/20W	MF	201	TBT_X_PLUG_EVENT_L	16 28
R1671	100K	1	2	5%	1/20W	MF	201	TBT_T_PLUG_EVENT_L	16 19
R1672	100K	1	2	5%	1/20W	MF	201	TBT_POC_RESET	16 28

MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>

BOM_COST_GROUP=CPU & CHIPSET

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Primary / Merged (CPU/PCH) Micro2-XDP

=PP1V_SUS_XDP

PLACE_NEAR=U0500.D67:2.54MM
XDP:YES
R1801 1K 5% 1/20W MF 201
PULL CFG<3> LOW
WHEN XDP PRESENT
NO_XNET_CONNECTION

XDP_CONN:YES
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_PRESENT_CPU	XDP_PIN_1				
XDP_CPU_PREQ_L	OBSFN_A0	CPU_CFG<17>	OBSFN_C0	CPU_CFG<16>	XDP_CPU_PRDY_L
CPU_CFG<0>	OBSDATA_A0	CPU_CFG<8>	OBSDATA_C0	CPU_CFG<9>	OBSDATA_C1
CPU_CFG<1>	OBSDATA_A1	CPU_CFG<10>	OBSDATA_C2	CPU_CFG<11>	OBSDATA_C3
CPU_CFG<2>	OBSDATA_A2	CPU_CFG<19>	OBSFN_D0	CPU_CFG<18>	OBSFN_D1
CPU_CFG<3>	OBSDATA_A3	CPU_CFG<12>	OBSDATA_D0	CPU_CFG<13>	OBSDATA_D1
NC	OBSFN_B0	CPU_CFG<14>	OBSDATA_D2	CPU_CFG<15>	OBSDATA_D3
NC	OBSFN_B1				
CPU_CFG<4>	OBSDATA_B0				
CPU_CFG<5>	OBSDATA_B1				
CPU_CFG<6>	OBSDATA_B2				
CPU_CFG<7>	OBSDATA_B3				
XDP_PM_RSMRST_L	HOOK0	ITPCLK/HOOK4 NC			
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 NC			
VCC_OBS_AB	HOOK2	VCC_OBS_CD			
NC	HOOK3	RESET#/HOOK6	ITP_PMODE		
NC	SDA	DBR#/HOOK7	XDP_DBRESET_L		
NC	SCL	TDO			
XDP_PCH_TCK	TCK1	TRSTn			
	TCK0	TDI			
		TMS			
		XDP_PRESENT#			

518S0847

XDP:YES C1804 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=J1800.42:28MM
XDP:YES C1800 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=J1800.44:28MM
XDP:YES C1801 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=J1800.43:28MM
XDP:YES C1806 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=J1800.47:28MM

=PP1V_S0SW_CPU_VCCSTG

XDP_PCH_TDO	R1890 51	PLACE_NEAR=U0500.A56:28MM
XDP_PCH_TDI	R1891 51	PLACE_NEAR=U0500.D59:28MM
XDP_PCH_TMS	R1892 51	PLACE_NEAR=U0500.C59:28MM
XDP_CPU_TDO	R1810 51	PLACE_NEAR=U0500.A61:28MM
XDP_CPU_TCK	R1813 51	PLACE_NEAR=U0500.B61:28MM
XDP_PCH_TCK	R1897 51	PLACE_NEAR=U0500.C61:28MM

All: XDP:YES, 5% 1/20W MF 201

R1830 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.E8:2.54MM

XDP:YES R1806 0 5% 1/20W MF 0201 PM_SYSRST_L

PM_RSMRST_L — XDP:YES R1800 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.AY17:19MM
PM_PWRBTN_L — R1802 10 5% 1/20W MF 201 PLACE_NEAR=U0500.BA15:2.54MM
XDP_CPU_TCK — XDP:YES R1835 0 5% 1/20W MF 0201 PCH_JTAGX PLACE_NEAR=J1800.58:28MM

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

R1821	XDP_CPU_TDO	PLACE_NEAR=J1800.51:2.54MM
R1822	XDP_CPU_TRST_L	PLACE_NEAR=J1800.53:2.54MM
R1823	XDP_CPU_TDI	PLACE_NEAR=J1800.55:2.54MM
R1824	XDP_CPU_TMS	PLACE_NEAR=J1800.57:2.54MM

All: XDP:YES, 0, 5% 1/20W MF 0201

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals		Non-XDP Signals
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE	JTAG_ISP_TCK
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE	JTAG_ISP_TDI
XDP_PCH_OBSDATA_A2	TP1870	
XDP_PCH_OBSDATA_A3	TP1871	
XDP_PCH_OBSDATA_B0	TP1872	
XDP_PCH_OBSDATA_C0	TP1873	
XDP_PCH_OBSDATA_C1	TP1874	
XDP_PCH_OBSDATA_C2	TP1875	
XDP_PCH_OBSDATA_C3	TP1876	
XDP_PCH_OBSDATA_D0	TP1877	
XDP_PCH_OBSDATA_D1	TP1878	
XDP_PCH_OBSDATA_D2	TP1879	
XDP_PCH_OBSDATA_D3	TP1880	
XDP_PCH_OBSFN_C1	TP1881	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE	USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE	USB_EXTD_OC_L

All TPs: TP-P6

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

=PP3V3_SUS_XDP

XDP_STRAP C1830 0.1UF 10% 10V X5R-CERM 0201

XDP_STRAP — U1830 74AUP1G07GF SOT891 (VCC, GND, OD)
NC — NC
SPI_IO2_STRAP_L — XDP_STRAP R1831 1.5K 5% 1/20W MF 201 — SPI_IO<2> (STRAP TO PCH)
PLACE_NEAR=U0500.AW2:10MM
NO_XNET_CONNECTION=1

=PP3V3_SUS_XDP — XDP:YES R1850 100K 5% 1/20W MF 201

PULL STRAP LOW WHEN XDP IS PLUGGED IN.
(UNDOCUMENTED STRAP FUNCTION)

XDP_PRESENT_L

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

BOM_COST_GROUP=DEBUG

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CPU/PCH Merged XDP

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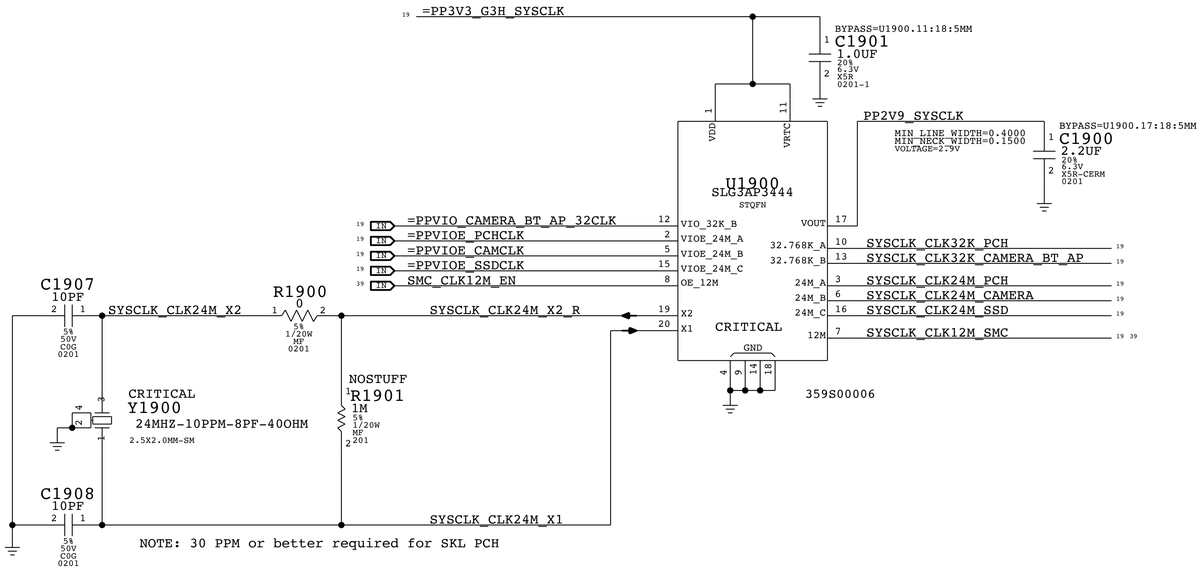
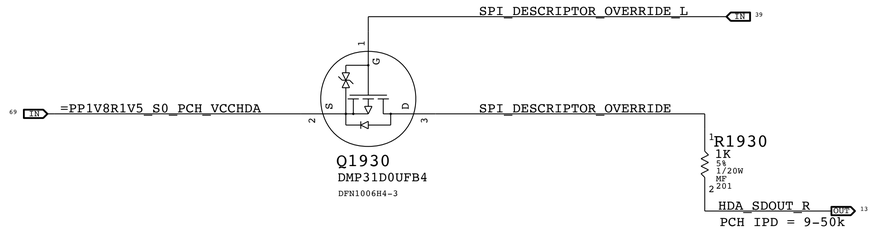
System 32kHz / 12MHz / 24MHz Clock Generator

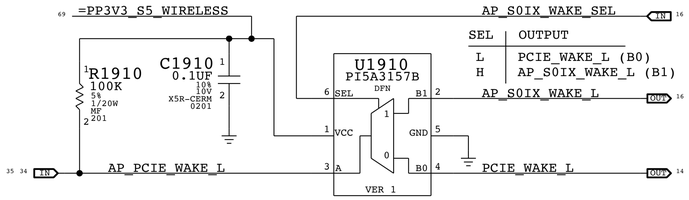


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=KSG SYNC_DATE=06/17/2015

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Chipset Support 1

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OPTION STRAPS

PROJECT DEPENDANT

=PP3V3_S0_PCH 5 13 14 16 19 60 69

STUFF PULL-UPS TO ENABLE INTERNAL GPU DP PORTS.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWNS TO DISABLE.

R2020 2.2K 5% 1/20W MF 201 (STRAP-OPTION) IG_DDI1_EN → PCH_DDPB_CTRLDATA 13
R2021 2.2K 5% 1/20W MF 201 (STRAP-OPTION) IG_DDI2_EN → PCH_DDPC_CTRLDATA 13

=PP3V3_SUS_PCH_VCCPGPPB 8 12 69

STUFF PULL-UP TO ENABLE BSSB (DCI) CLK/DI ON GPP_D11, _D12.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWN FOR BSSB ON USB-SS.

R2022 1K 5% 1/20W MF 201 (STRAP-OPTION) BSSB_ON_GPIOS → PCH_STRP_BSSB_SEL_GPIO 13

GREENCLK CLOCK CONNECTIONS.

10 =PP3V3_G3H_SYSCLK == PP3V3_G3H 28 41 42 47 51 52 53 60 68 69 72

BT_CLK32K:YES
R2030 0 5% 1/20W MF 0201

19 18 =PPVIO_CAMERA_BT_AP_32CLK == PPVIO_BT_AP_32CLK (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800) → =PP3V3_S4_WLAN 34 69

BT_CLK32K:NO
R2031 100K 5% 1/20W MF 0201

XW2000 SM
18 =PPVIOE_SSDCLK == PP_PPVIOE_SSDCLK (MAKE_BASE=TRUE)

XW2002 SM
19 18 =PPVIOE_CAMCLK == PPVIOE_CAMCLK (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800) → =PPVDDIO_S0_CAMCLK 36

PCH 24MHz VIOE Options

XW2065 SM
72 69 64 63 62 PP1V_S5G — PP1V_S5G_PCHCLK (VOLTAGE=1V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800)

PCH24M:SUS
R2065 0 5% 1/20W MF 0201
PP1V_S5G_PCHCLK → =PPVIOE_PCHCLK 18 19
PP1V_SUSRS0SW_PCHCLK (VOLTAGE=1V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800, MAKE_BASE=TRUE)

PCH24M:S0SW
R2066 0 5% 1/20W MF 0201
PP1V_S0SW_PCHCLK (VOLTAGE=1V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800)

SYM VER 3 DFN1006H4-3
DMN32D2LFB4 Q2065 CRITICAL
PM_SLP_S0S3_L → 60 68 72

19 18 =PPVIO_CAMERA_BT_AP_32CLK
=PPVIOE_PCHCLK 18 19
=PPVIOE_CAMCLK 18 19

BYPASS=U1900.12:18:5MM
BYPASS=U1900.02:18:5MM
BYPASS=U1900.05:18:5MM

C2004 0.1UF 10% 10V X5R-CERM 0201
C2005 0.1UF 10% 10V X5R-CERM 0201
C2006 0.1UF 10% 10V X5R-CERM 0201

18 IN SYSCLK_CLK32K_PCH (MAKE_BASE=TRUE) — (MAKE_BASE=TRUE) TP_PCH_CLK32K_RTCX2 — PCH_CLK32K_RTCX1 OUT 15; PCH_CLK32K_RTCX2 IN 15

BT_CLK32K:YES
R2032 0 5% 1/20W MF 0201
18 IN SYSCLK_CLK32K_CAMERA_BT_AP — SYSCLK_CLK32K_BT_AP_R (MAKE_BASE=TRUE) → SYSCLK_CLK32K_BT_AP OUT 34

18 IN SYSCLK_CLK24M_PCH (MAKE_BASE=TRUE) — (MAKE_BASE=TRUE) TP_PCH_CLK24M_XTALOUT — PCH_CLK24M_XTALIN OUT 15; PCH_CLK24M_XTALOUT IN 15

18 IN SYSCLK_CLK24M_SSD — TP_SYSCLK_CLK24M_SSD (MAKE_BASE=TRUE) 70

18 IN SYSCLK_CLK24M_CAMERA (MAKE_BASE=TRUE) — CLK25M_CAM_CLKP OUT 36

39 18 IN SYSCLK_CLK12M_SMC OUT

=PP3V3_S0_PCH 5 13 14 16 19 60 69

R2071 47K 5% 1/20W MF 201 SSD_CLKREQ_L 19 67
R2072 47K 5% 1/20W MF 201 TBT_X_CLKREQ_L 19 26
R2074 47K 5% 1/20W MF 201 AP_CLKREQ_L 19 34 35
R2075 47K 5% 1/20W MF 201 CAMERA_CLKREQ_L 19 36

SERIES R FOR VOLTAGE DIVIDER WHEN PCH IS DRIVING IN L1 SUB-STATE.

15 OUT =SSD_CLKREQ_L — SSD_CLKREQ_R_L (MAKE_BASE=TRUE)
R2001 1K 1/20W 5% 201 MF
SSD_CLKREQ_L IN 19 67

15 OUT =AP_CLKREQ_L — AP_CLKREQ_R_L (MAKE_BASE=TRUE)
R2002 1K 1/20W 5% 201 MF
AP_CLKREQ_L IN 19 34 35

15 OUT =CAMERA_CLKREQ_L — CAMERA_CLKREQ_R_L (MAKE_BASE=TRUE)
R2003 1K 1/20W 5% 201 MF
CAMERA_CLKREQ_L IN 19 36

15 OUT =TBT_X_CLKREQ_L — TBT_X_CLKREQ_R_L (MAKE_BASE=TRUE)
R2004 1K 1/20W 5% 201 MF
TBT_X_CLKREQ_L IN 19 26

UNUSED PCH XDP SIGNALS NEED TEST POINTS.

28 17 IN JTAG_ISP_TCK — TP2070 (TP-P6)
28 17 IN JTAG_ISP_TDI — TP2071 (TP-P6)
17 IN USB_EXTD_OC_L — TP2072 (TP-P6)
17 IN USB_EXTC_OC_L — TP2073 (TP-P6)

EXTRA BPM TESTPOINTS

6 IN XDP_BPM_L<1> — (MAKE_BASE=TRUE) TP_XDP_BPM_L<1> 70
6 IN XDP_BPM_L<2> — (MAKE_BASE=TRUE) TP_XDP_BPM_L<2> 70
6 IN XDP_BPM_L<3> — (MAKE_BASE=TRUE) TP_XDP_BPM_L<3> 70

IFDIM TRIGGERS USING R2055 & R2056 PADS
ASK DC/DC GROUP FOR DETAILS.

NOSTUFF R2055 100K 5% 1/16W MF-LF 402
6 IN XDP_BPM_L<0>

6 IN TP_CPU_RSVD_AK13 — (MAKE_BASE=TRUE) CPU_RSVD_AK13
NOSTUFF R2056 100K 5% 1/16W MF-LF 402

UNUSED GPIO SIGNALS

16 IN SOC_UART_D2R — (MAKE_BASE=TRUE) PU_SOC_UART_D2R
16 IN SOC_UART_R2D — (MAKE_BASE=TRUE) PU_SOC_UART_R2D
16 IN SOC_UART_RTS_L — (MAKE_BASE=TRUE) PU_SOC_UART_RTS_L
16 IN SOC_UART_CTS_L — (MAKE_BASE=TRUE) PD_SOC_UART_CTS_L
16 IN TBT_T_PLUG_EVENT_L — (MAKE_BASE=TRUE) PU_TBT_T_PLUG_EVENT_L
14 IN PCH_SWD_CLK — (MAKE_BASE=TRUE) PU_PCH_SWD_CLK
14 BI PCH_SWD_IO — (MAKE_BASE=TRUE) PU_PCH_SWD_IO
14 IN PCH_SWD_MUX_SEL — (MAKE_BASE=TRUE) PD_PCH_SWD_MUX_SEL
13 IN LCD_PSR_EN — (MAKE_BASE=TRUE) PD_LCD_PSR_EN
16 IN AUD_SPI_CS_L — (MAKE_BASE=TRUE) PU_AUD_SPI_CS_L
16 IN AUD_SPI_CLK — (MAKE_BASE=TRUE) PD_AUD_SPI_CLK
16 OUT AUD_SPI_MISO — (MAKE_BASE=TRUE) PD_AUD_SPI_MISO
16 IN AUD_SPI_MOSI — (MAKE_BASE=TRUE) PU_AUD_SPI_MOSI
15 OUT SPKR_ID0 — (MAKE_BASE=TRUE) TP_SPKR_ID0 70
16 OUT SPKR_ID1 — (MAKE_BASE=TRUE) TP_SPKR_ID1

13 IN CAMERA_PWR_EN_PCH — R2060 0 5% 1/20W MF 0201 — CAMERA_PWR_EN OUT 13 19 36

合肥怡飞维修qq：82669515
qq群： 241000

69 60 19 16 14 13 5 =PP3V3_S0_PCH
C2040 0.1UF 10% 10V X5R-CERM 0201

69 59 54 14 10 8 6 =PP1V_S3_CPU_VCCST
R2061 51 5% 1/20W MF 201
68 39 6 OUT CPU_CATERR_L

14 IN SOC_S2R_L — (MAKE_BASE=TRUE) SOC_WAKE_L

CRITICAL
U2040 74LVC1G08 SOT891
60 14 IN PM_PCH_PWROK
PM_PCH_PWROK_BUF 4
NC 2 5

R2040 100K 5% 1/20W MF 201
R2041 100K 5% 1/20W MF 201
AUD_PWR_EN 16 49
CAMERA_PWR_EN 13 19 36

BOM_COST_GROUP=CPU & CHIPSET

RESETS

68 35 14 IN PLT_RST_L
R2014 470K 5% 1/20W MF 201

R2010 100K 5% 1/20W MF 201 CAMERA_RESET_L OUT 13 36
R2011 100K 5% 1/20W MF 201 AP_RESET_L OUT 16 34 35
R2012 100K 5% 1/20W MF 201 SSD_RESET_L OUT 16 67
R2013 100K 5% 1/20W MF 201 TBT_X_PCI_RESET_L OUT 16 19 28
R2015 33 5% 1/20W MF 201 SMC_LRESET_L OUT 39

26 PM_PLT_RST_TBT_X_L — (MAKE_BASE=TRUE) TBT_X_PCI_RESET_L 16 19 28

S3X SSD CONTROL

PCH — S3X SSD DOWN

60 OUT SSD_PWR_REQ — (MAKE_BASE=TRUE) STORAGE_LATCH IN 67

UNUSED GPIO SIGNALS

13 IN SOC_ALS_UART_R2D — (MAKE_BASE=TRUE) PU_SSD_UART_R2D
13 OUT SOC_ALS_UART_D2R — (MAKE_BASE=TRUE) PU_SSD_UART_D2R
13 IN PCH_UART2_CTS_L — (MAKE_BASE=TRUE) PD_SSD_UART_CTS_L

PROBE POINTS

28 15 IN PCIE_TBT_X_R2D_C_P<0>
28 15 IN PCIE_TBT_X_R2D_C_N<0>
NO_XNET_CONNECTION=1
NOSTUFF PLACE_NEAR=C3040.1:1MM
C2090 0.22UF 20% 6.3V X5R 0201 — TBTXR2DP0 PLACE_NEAR=C2090.2:1MM
R2090 51 5% 1/20W MF 201 NOSTUFF
C2091 0.22UF 20% 6.3V X5R 0201 — TBTXR2DN0 PLACE_NEAR=C3040.1:1MM
R2091 51 5% 1/20W MF 201 NOSTUFF

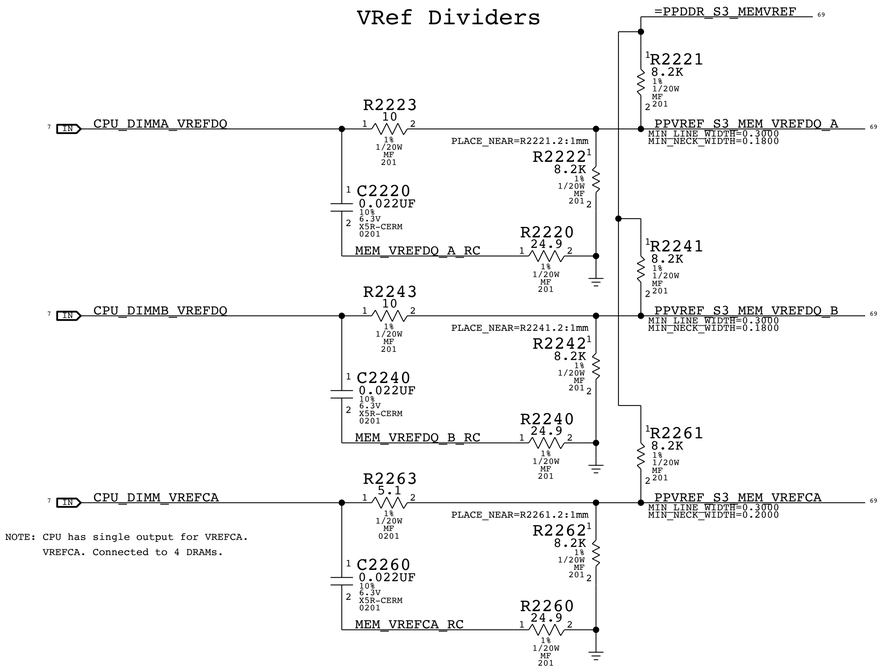
28 26 OUT DP_X_SNK1_ML_C_P<0>
28 26 IN DP_X_SNK1_ML_C_N<0>
NO_XNET_CONNECTION=1
NOSTUFF PLACE_NEAR=C3040.1:1MM
C2092 0.1UF 10% 16V X5R-CERM 0201 — DPX1P0 PLACE_NEAR=C2090.2:6MM
R2092 51 5% 1/20W MF 201 NOSTUFF
C2093 0.1UF 10% 16V X5R-CERM 0201 — DPX1N0 PLACE_NEAR=C2090.2:5MM
R2093 51 5% 1/20W MF 201 NOSTUFF

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016
PAGE TITLE
Chipset Support 2

Apple Inc.

DRAWING NUMBER 051-02265 | SIZE D
REVISION 1.0.0
BRANCH
PAGE 20 OF 500
SHEET 19 OF 73

CPU-Based Margining



NOTE: CPU has single output for VREFCA. VREFCA. Connected to 4 DRAMs.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE: LPDDR3 VREF Margining

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D

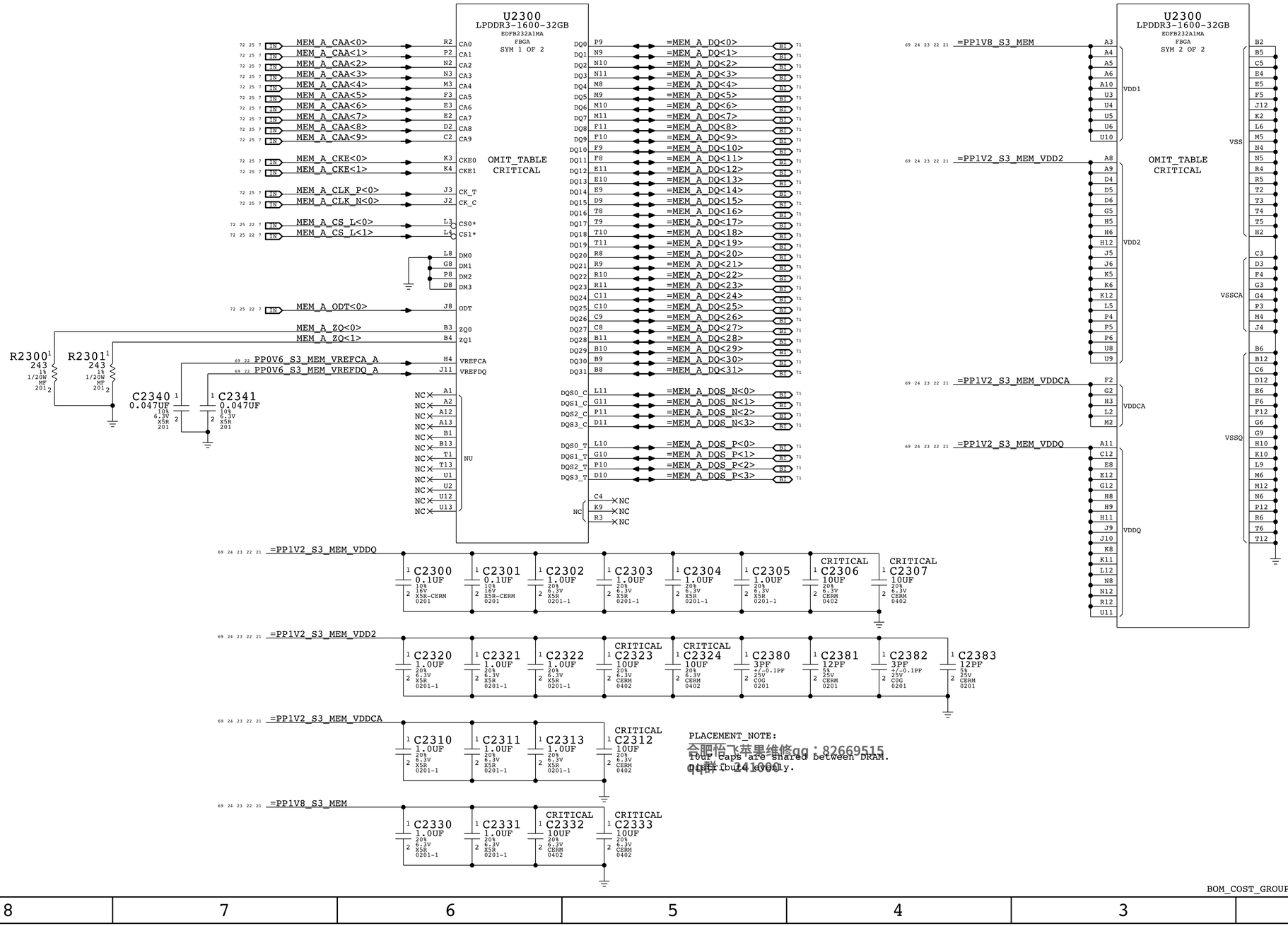
REVISION: 1.0.0

BRANCH:

PAGE: 22 OF 500

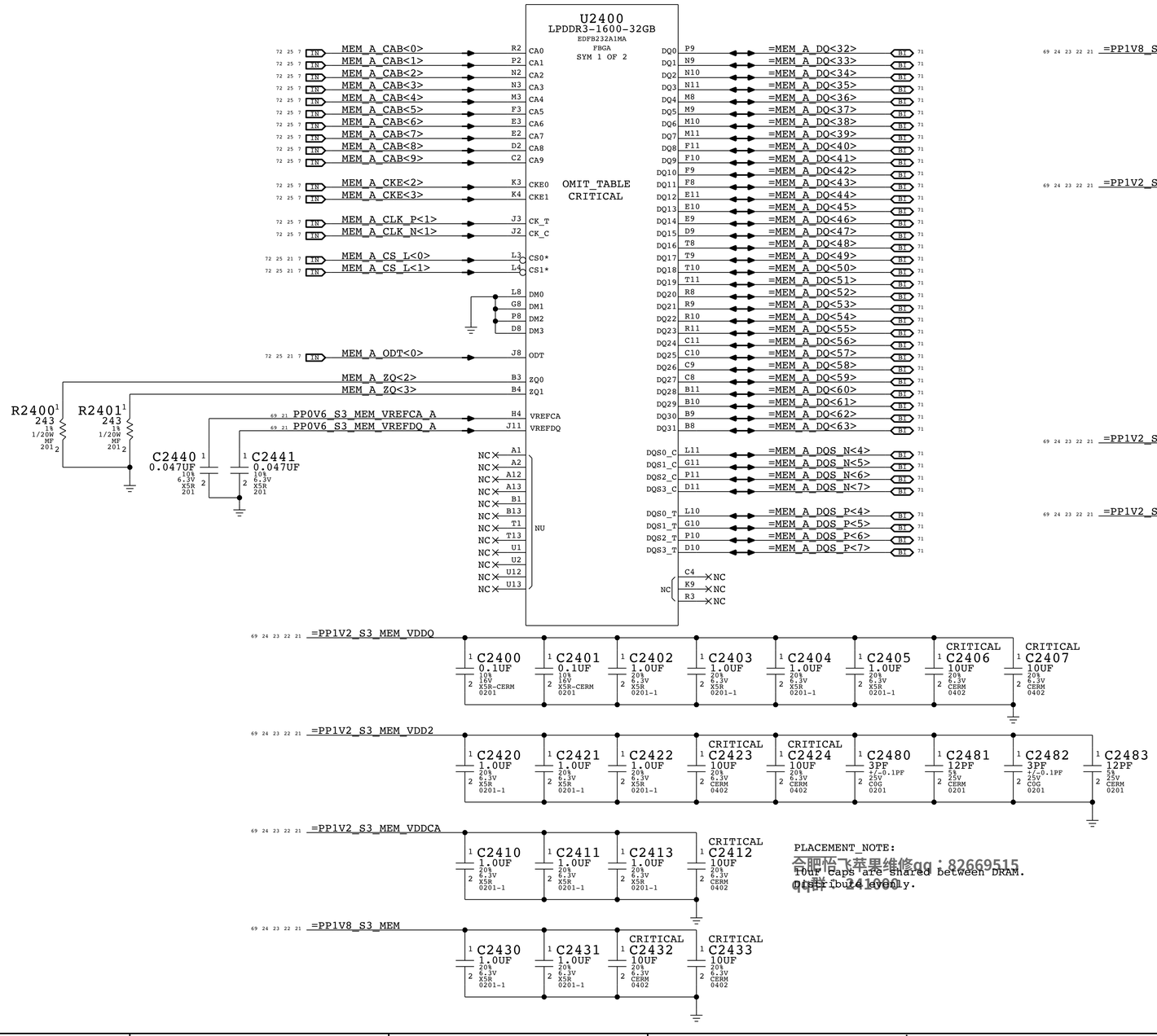
SHEET: 20 OF 73

LPDDR3 CHANNEL A (0-31)



SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel A (00-31)
Apple Inc.	DRAWING NUMBER 051-02265
	SIZE D
	REVISION 1.0.0
	BRANCH
	PAGE 23 OF 500
	SHEET 21 OF 73

LPDDR3 CHANNEL A (32-63)



BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

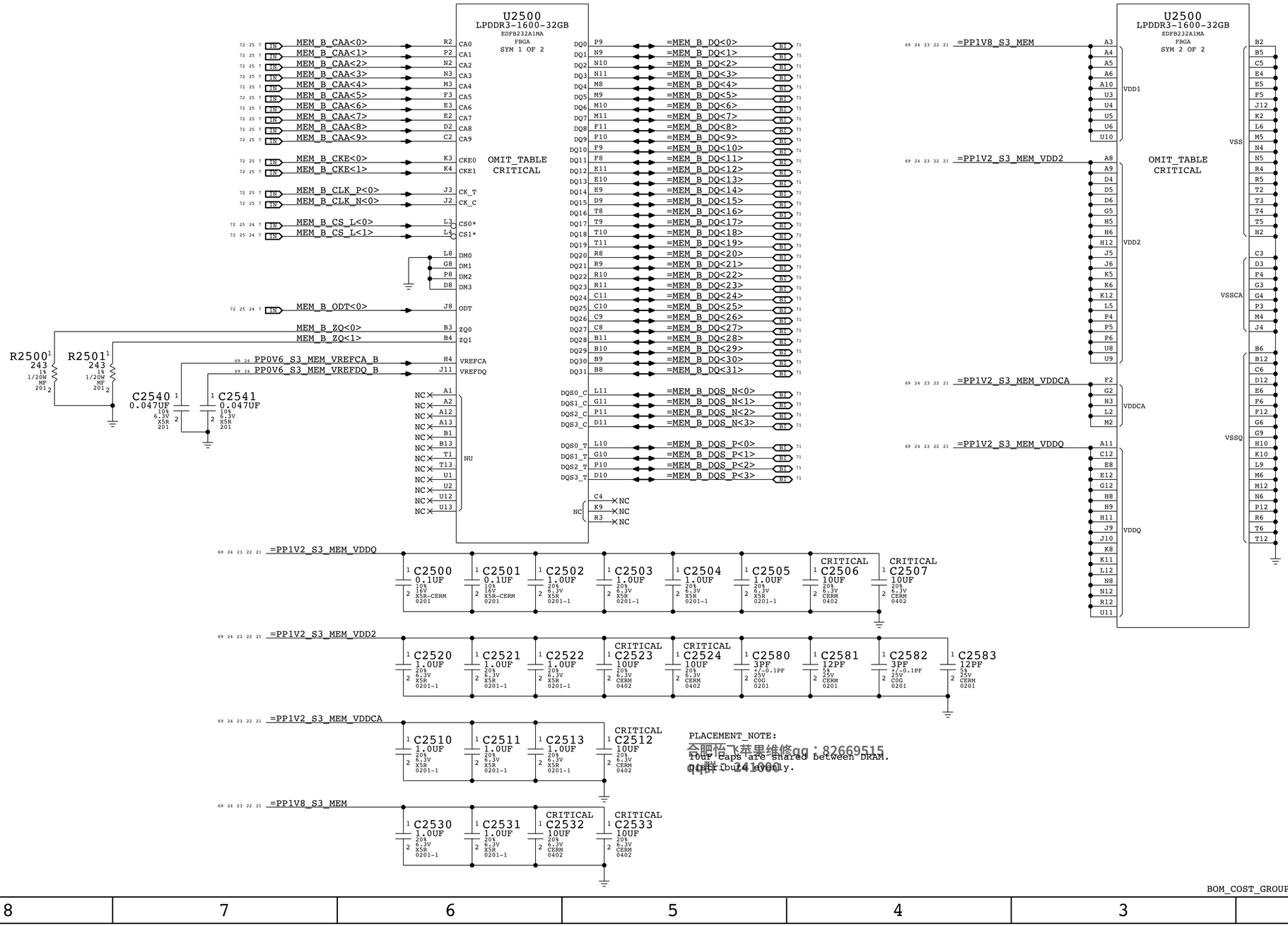
REVISION 1.0.0

BRANCH

PAGE 24 OF 500

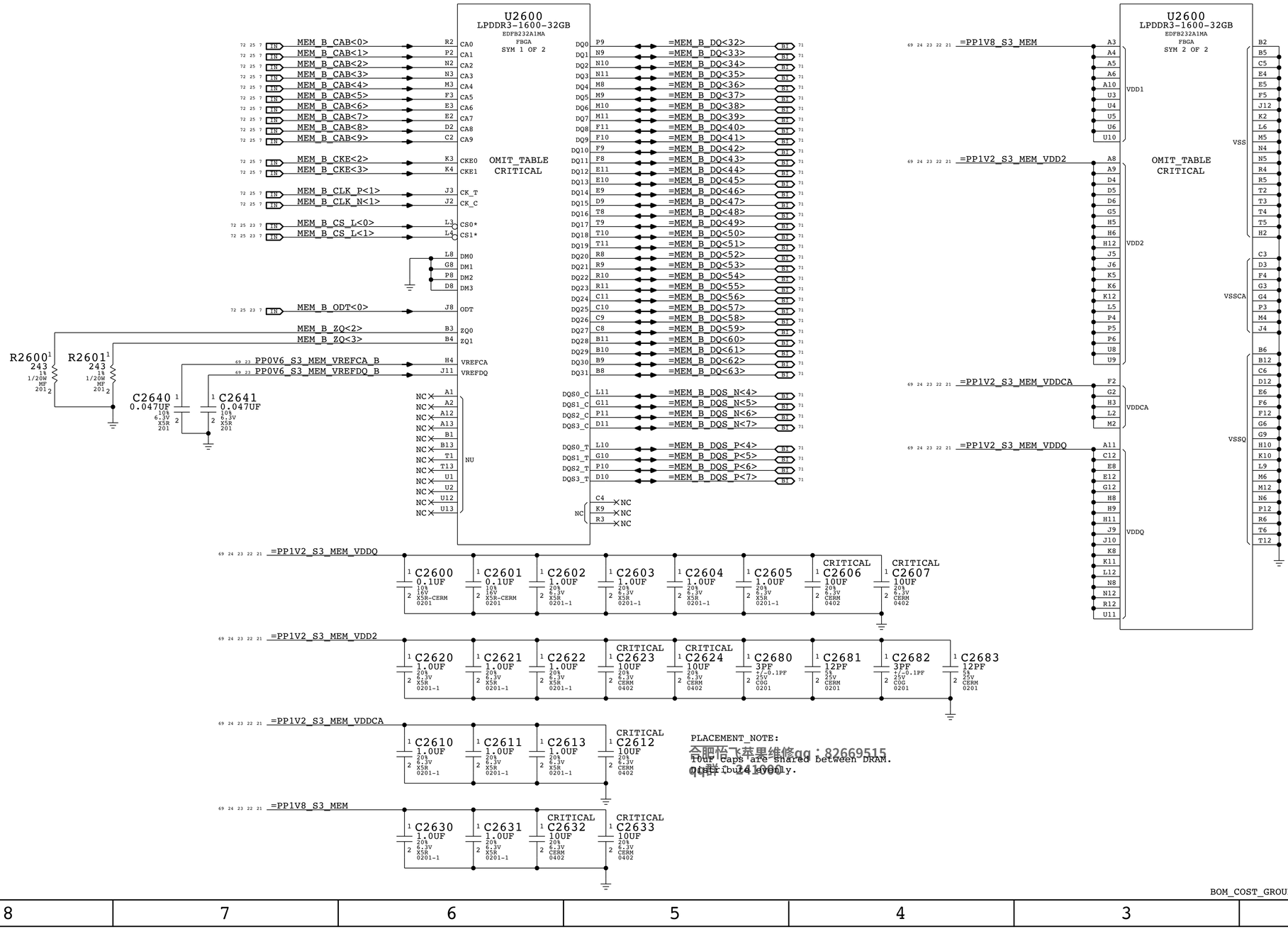
SHEET 22 OF 73

LPDDR3 CHANNEL B (0-31)



SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel B (00-31)
Apple Inc.	DRAWING NUMBER 051-02265 SIZE D
	REVISION 1.0.0
	BRANCH
	PAGE 25 OF 500
	SHEET 23 OF 73

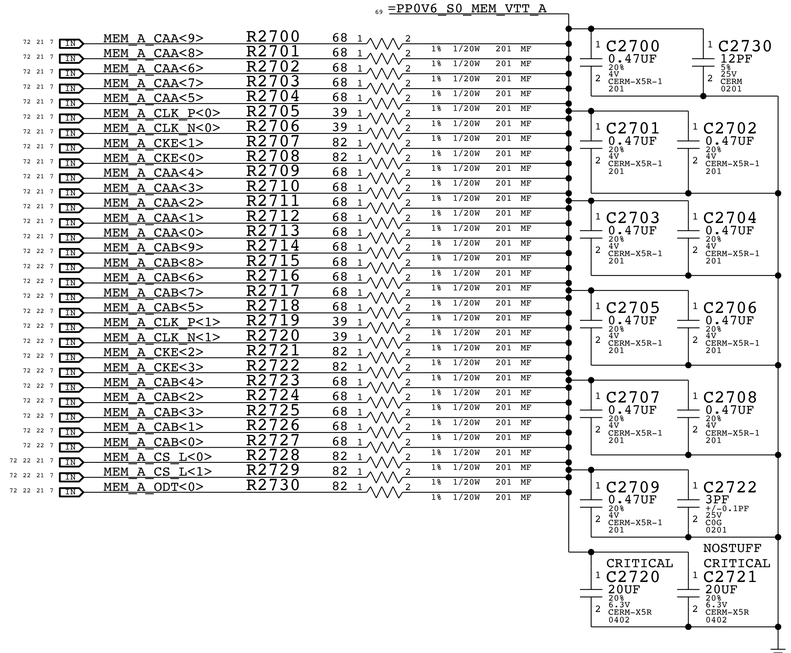
LPDDR3 CHANNEL B (32-63)

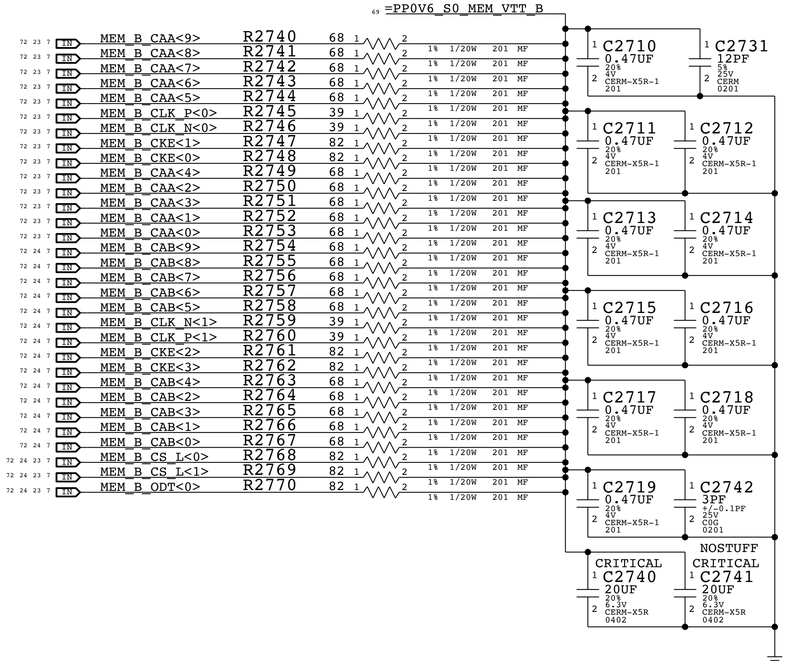


BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel B (32-63)
Apple Inc.	DRAWING NUMBER 051-02265 · SIZE D
	REVISION 1.0.0
	BRANCH
	PAGE 26 OF 500
	SHEET 24 OF 73

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
BRANCH
PAGE 27 OF 500
SHEET 25 OF 73

=PP3V3_TBT_X_FLASH

R2890 3.3K 5% 1/20W MF 201

R2891 3.3K 5% 1/20W MF 201

R2893 3.3K 5% 1/20W MF 201

R2892 3.3K 5% 1/20W MF 201

C2890 1UF 10% 10V X5R 402-1

U2890 8MBIT-3.0V W25Q80DVUXIE USON OMIT_TABLE CRITICAL

TBT_X_SPI_CLK	CLK	DI(IO0)	TBT_X_SPI_MOSI
TBT_X_SPI_CS_L	CS*	DO(IO1)	TBT_X_SPI_MISO
TBT_X_ROM_WP_L	WP*(IO2)		
TBT_X_ROM_HOLD_L	HOLD*(IO3)		
	GND EPAD		

SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820 0.1UF	DP_X_SNK0_ML_P<0>
DP_X_SNK0_ML_C_N<0>	C2821 0.1UF	DP_X_SNK0_ML_N<0>
DP_X_SNK0_ML_C_P<1>	C2822 0.1UF	DP_X_SNK0_ML_P<1>
DP_X_SNK0_ML_C_N<1>	C2823 0.1UF	DP_X_SNK0_ML_N<1>
DP_X_SNK0_ML_C_P<2>	C2824 0.1UF	DP_X_SNK0_ML_P<2>
DP_X_SNK0_ML_C_N<2>	C2825 0.1UF	DP_X_SNK0_ML_N<2>
DP_X_SNK0_ML_C_P<3>	C2826 0.1UF	DP_X_SNK0_ML_P<3>
DP_X_SNK0_ML_C_N<3>	C2827 0.1UF	DP_X_SNK0_ML_N<3>
DP_X_SNK0_AUXCH_C_P	C2828 0.1UF	DP_X_SNK0_AUXCH_P
DP_X_SNK0_AUXCH_C_N	C2829 0.1UF	DP_X_SNK0_AUXCH_N

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830 0.1UF	DP_X_SNK1_ML_P<0>
DP_X_SNK1_ML_C_N<0>	C2831 0.1UF	DP_X_SNK1_ML_N<0>
DP_X_SNK1_ML_C_P<1>	C2832 0.1UF	DP_X_SNK1_ML_P<1>
DP_X_SNK1_ML_C_N<1>	C2833 0.1UF	DP_X_SNK1_ML_N<1>
DP_X_SNK1_ML_C_P<2>	C2834 0.1UF	DP_X_SNK1_ML_P<2>
DP_X_SNK1_ML_C_N<2>	C2835 0.1UF	DP_X_SNK1_ML_N<2>
DP_X_SNK1_ML_C_P<3>	C2836 0.1UF	DP_X_SNK1_ML_P<3>
DP_X_SNK1_ML_C_N<3>	C2837 0.1UF	DP_X_SNK1_ML_N<3>
DP_X_SNK1_AUXCH_C_P	C2838 0.1UF	DP_X_SNK1_AUXCH_P
DP_X_SNK1_AUXCH_C_N	C2839 0.1UF	DP_X_SNK1_AUXCH_N

100K R2862	DP_XA_HPD
100K R2872	DP_XB_HPD
1M R2860	TBT_XA_LSTX
1M R2861	TBT_XA_LSRX
1M R2870	TBT_XB_LSTX
1M R2871	TBT_XB_LSRX

U2800 TBT-AR-4C-CNTRL SYM 1 OF 2 FCBGA OMIT_TABLE CRITICAL

PCIE GRP3

PCIE_TBT_X_R2D_P<0>	Y23	PCIE_RX0_P	
PCIE_TBT_X_R2D_N<0>	Y22	PCIE_RX0_N	
PCIE_TBT_X_R2D_P<1>	T23	PCIE_RX1_P	
PCIE_TBT_X_R2D_N<1>	T22	PCIE_RX1_N	
PCIE_TBT_X_R2D_P<2>	M23	PCIE_RX2_P	
PCIE_TBT_X_R2D_N<2>	M22	PCIE_RX2_N	
PCIE_TBT_X_R2D_P<3>	H23	PCIE_RX3_P	
PCIE_TBT_X_R2D_N<3>	H22	PCIE_RX3_N	
PCIE_CLK100M_TBT_X_P	V19	PCIE_REFCLK_100_IN_P	
PCIE_CLK100M_TBT_X_N	T19	PCIE_REFCLK_100_IN_N	
TBT_X_CLKREQ_L	AC5	PCIE_CLKREQ*	
		PCIE_TX0_P	V23 PCIE_TBT_X_D2R_C_P<0>
		PCIE_TX0_N	V22 PCIE_TBT_X_D2R_C_N<0>
		PCIE_TX1_P	P23 PCIE_TBT_X_D2R_C_P<1>
		PCIE_TX1_N	P22 PCIE_TBT_X_D2R_C_N<1>
		PCIE_TX2_P	K23 PCIE_TBT_X_D2R_C_P<2>
		PCIE_TX2_N	K22 PCIE_TBT_X_D2R_C_N<2>
		PCIE_TX3_P	F23 PCIE_TBT_X_D2R_C_P<3>
		PCIE_TX3_N	F22 PCIE_TBT_X_D2R_C_N<3>
		PERST*	L4 PM_PLT_RST_TBT_X_L
		PCIE_RBIAS	N16 TBT_X_PCIE_BIAS

10K PU ON CLOCKS PAGE

PLACE_NEAR=U2800.N16:2MM

R2851 3.01K 1% 1/20W MF 201

DP_X_SNK0_ML_P<0>	AB7	DPSNK0_ML0_P	
DP_X_SNK0_ML_N<0>	AC7	DPSNK0_ML0_N	
DP_X_SNK0_ML_P<1>	AB9	DPSNK0_ML1_P	
DP_X_SNK0_ML_N<1>	AC9	DPSNK0_ML1_N	
DP_X_SNK0_ML_P<2>	AB11	DPSNK0_ML2_P	
DP_X_SNK0_ML_N<2>	AC11	DPSNK0_ML2_N	
DP_X_SNK0_ML_P<3>	AB13	DPSNK0_ML3_P	
DP_X_SNK0_ML_N<3>	AC13	DPSNK0_ML3_N	
DP_X_SNK0_AUXCH_P	Y11	DPSNK0_AUX_P	
DP_X_SNK0_AUXCH_N	W11	DPSNK0_AUX_N	
DP_X_SNK0_HPD	AA2	DPSNK0_HPD	
=DP_X_SNK0_DDC_CLK	Y5	DPSNK0_DDC_CLK	
=DP_X_SNK0_DDC_DATA	R4	DPSNK0_DDC_DATA	
DP_X_SNK1_ML_P<0>	AB15	DPSNK1_ML0_P	
DP_X_SNK1_ML_N<0>	AC15	DPSNK1_ML0_N	
DP_X_SNK1_ML_P<1>	AB17	DPSNK1_ML1_P	
DP_X_SNK1_ML_N<1>	AC17	DPSNK1_ML1_N	
DP_X_SNK1_ML_P<2>	AB19	DPSNK1_ML2_P	
DP_X_SNK1_ML_N<2>	AC19	DPSNK1_ML2_N	
DP_X_SNK1_ML_P<3>	AB21	DPSNK1_ML3_P	
DP_X_SNK1_ML_N<3>	AC21	DPSNK1_ML3_N	
DP_X_SNK1_AUXCH_P	Y12	DPSNK1_AUX_P	
DP_X_SNK1_AUXCH_N	W12	DPSNK1_AUX_N	
DP_X_SNK1_HPD	Y6	DPSNK1_HPD	
=DP_X_SNK1_DDC_CLK	Y8	DPSNK1_DDC_CLK	
=DP_X_SNK1_DDC_DATA	N4	DPSNK1_DDC_DATA	
DP_X_SNK_RBIAS	Y18	DPSNK_RBIAS	

SINK PORT 0

SINK PORT 1

R2830 100K 5% 1/20W MF 201

R2831 100K 5% 1/20W MF 201

R2850 14K 1% 1/20W MF 201

PLACE_NEAR=U2800.Y18:2MM

JTAG_TBT_TDI	Y4	TDI	
JTAG_TBT_TMS	V4	TMS	
JTAG_TBT_TCK	T4	TCK	
JTAG_TBT_TDO	W4	TDO	
TBT_X_RBIAS	H6	RBIAS	
TBT_X_RSENSE	J6	RSENSE	

MISC

R2855 4.75K 0.5% 0201

PLACE_NEAR=U2800.H6:2MM
PLACE_NEAR=U2800.J6:2MM

		DPSRC_ML0_P	R2 =DP_X_SRC_ML_P<0>
		DPSRC_ML0_N	R1 =DP_X_SRC_ML_N<0>
		DPSRC_ML1_P	N2 =DP_X_SRC_ML_P<1>
		DPSRC_ML1_N	N1 =DP_X_SRC_ML_N<1>
		DPSRC_ML2_P	L2 =DP_X_SRC_ML_P<2>
		DPSRC_ML2_N	L1 =DP_X_SRC_ML_N<2>
		DPSRC_ML3_P	J2 =DP_X_SRC_ML_P<3>
		DPSRC_ML3_N	J1 =DP_X_SRC_ML_N<3>
		DPSRC_AUX_P	W19 =DP_X_SRC_AUX_P
		DPSRC_AUX_N	Y19 =DP_X_SRC_AUX_N
		DPSRC_HPD	G1 DP_X_SRC_HPD
		DPSRC_RBIAS	N6 DP_X_SRC_RBIAS

SOURCE PORT 0

PLACE_NEAR= U2800.N6:3.8MM

R2852 14K 1% 1/20W MF 201

=PP3V3_TBT_X_SX

R2834 2.2K 5% 1/20W MF 201

R2835 2.2K 5% 1/20W MF 201

		GPIO_0	U1 I2C_TBT_X_SDA
		GPIO_1	U2 I2C_TBT_X_SCL
		GPIO_2	V1 TBT_X_ROM_WP_L
		GPIO_3	V2 =TBT_X_TMU_CLK_OUT
		GPIO_4	W1 TBT_WAKE_L
		GPIO_5	W2 TBT_X_CIO_PLUG_EVENT_L
		GPIO_6	Y1 TBT_X_HDMI_DDC_DATA
		GPIO_7	Y2 TBT_X_HDMI_DDC_CLK
		GPIO_8	AA1 =TBT_X_GPIO_8

LC GPIO

=PP3V3_TBT_X_SX

R2836 2.2K 5% 1/20W MF 201

R2837 2.2K 5% 1/20W MF 201

		POC_GPIO_0	J4 I2C_TBT_XA_INT_L
		POC_GPIO_1	E2 I2C_TBT_XB_INT_L
		POC_GPIO_2	D4 TBT_X_RTD3_USB_PWR_EN
		POC_GPIO_3	H4 TBT_X_FORCE_PWR
		POC_GPIO_4	F2 =TBT_X_BATLOW_L
		POC_GPIO_5	D2 PM_SLP_S3_L
		POC_GPIO_6	F1 TBT_X_RTD3_CIO_PWR_EN

POC GPIO

PU at PCH

not used

R2827 100K 5% 1/20W MF 201

		TEST_EN	E1 TBT_X_TEST_EN
		TEST_PWR_GOOD	AB5 TBT_X_TEST_PWR_GOOD
		RESET*	F4 USBC_X_RESET_L
		XTAL_25_IN	D22 TBT_X_XTAL25M_IN
		XTAL_25_OUT	D23 TBT_X_XTAL25M_OUT
		EE_DI	AB3 =UPC_X_SPI_MOSI
		EE_DO	AC4 =UPC_X_SPI_MISO
		EE_CS*	AC3 =UPC_X_SPI_CS_L
		EE_CLK	AB4 =UPC_X_SPI_CLK

R2825 100 5% 1/20W MF 201

R2829 100 5% 1/20W MF 201

To SPI Flash

USBC_XA_D2R_P<2>	A15	PA_RX1_P	
USBC_XA_D2R_N<2>	B15	PA_RX1_N	
USBC_XA_R2D_C_P<2>	A17	PA_TX1_P	
USBC_XA_R2D_C_N<2>	B17	PA_TX1_N	
USBC_XA_R2D_C_P<1>	A19	PA_TX0_P	
USBC_XA_R2D_C_N<1>	B19	PA_TX0_N	
USBC_XA_D2R_P<1>	B21	PA_RX0_P	
USBC_XA_D2R_N<1>	A21	PA_RX0_N	
DP_XA_AUXCH_C_P	Y15	PA_DPSRC_AUX_P	
DP_XA_AUXCH_C_N	W15	PA_DPSRC_AUX_N	
USB_UPC_XA_P	E20	PA_USB2_D_P	
USB_UPC_XA_N	D20	PA_USB2_D_N	
TBT_XA_LSTX	A5	PA_LSTX	
TBT_XA_LSRX	A4	PA_LSRX	
DP_XA_HPD	M4	PA_DPSRC_HPD	
		PA_USB2_RBIAS	H19

PORT A

		PB_RX1_P	B7 USBC_XB_D2R_P<2>
		PB_RX1_N	A7 USBC_XB_D2R_N<2>
		PB_TX1_P	A9 USBC_XB_R2D_C_P<2>
		PB_TX1_N	B9 USBC_XB_R2D_C_N<2>
		PB_TX0_P	A11 USBC_XB_R2D_C_P<1>
		PB_TX0_N	B11 USBC_XB_R2D_C_N<1>
		PB_RX0_P	A13 USBC_XB_D2R_P<1>
		PB_RX0_N	B13 USBC_XB_D2R_N<1>
		PB_DPSRC_AUX_P	Y16 DP_XB_AUXCH_C_P
		PB_DPSRC_AUX_N	W16 DP_XB_AUXCH_C_N
		PB_USB2_D_P	E19 USB_UPC_XB_P
		PB_USB2_D_N	D19 USB_UPC_XB_N
		PB_LSTX	B4 TBT_XB_LSTX
		PB_LSRX	B5 TBT_XB_LSRX
		PB_DPSRC_HPD	G2 DP_XB_HPD
		PB_USB2_RBIAS	F19 TBT_XB_USB2_RBIAS

PORT B

TBT PORTS

GND_VOID=TRUE

C2810 0.1UF 16V 10% X5R-CERM

C2811 0.1UF 16V 10% X5R-CERM

GND_VOID=TRUE

C2812 0.1UF 16V 10% X5R-CERM

C2813 0.1UF 16V 10% X5R-CERM

GND_VOID=TRUE

PLACE_NEAR=U2800.H19:2MM

R2854 499 1% 1/20W MF 201

THERMDA	AC23		
THERMDA	AB23		
TBT_X_THERM_D_P			
TBT_X_THERM_D_N			
		MONDC_SVR	D6
		ATEST_P	A23 NC
		ATEST_N	B23 NC
PCIE_ATEST	V18	USB2_ATEST	E18 NC
TEST_EDM	AC1		
FUSE_VQPS_64	L15	MONDC_DPSNK_0	W13
FUSE_VQPS_128	N15	MONDC_DPSNK_1	W18
MONDC_CIO_0	C23	MONDC_DPSRC	AB2
MONDC_CIO_1	C22		

DEBUG

USE NEAREST GND BALL

(ACZ2) FOR THERM_D_N

PLACE_NEAR=U2800.F19:2MM

R2853 499 1% 1/20W MF 201

BOM_COST_GROUP=TBT

SYNC_MASTER=X362	SYNC_DATE=07/29/2015
PAGE TITLE	USB-C HIGH SPEED 1
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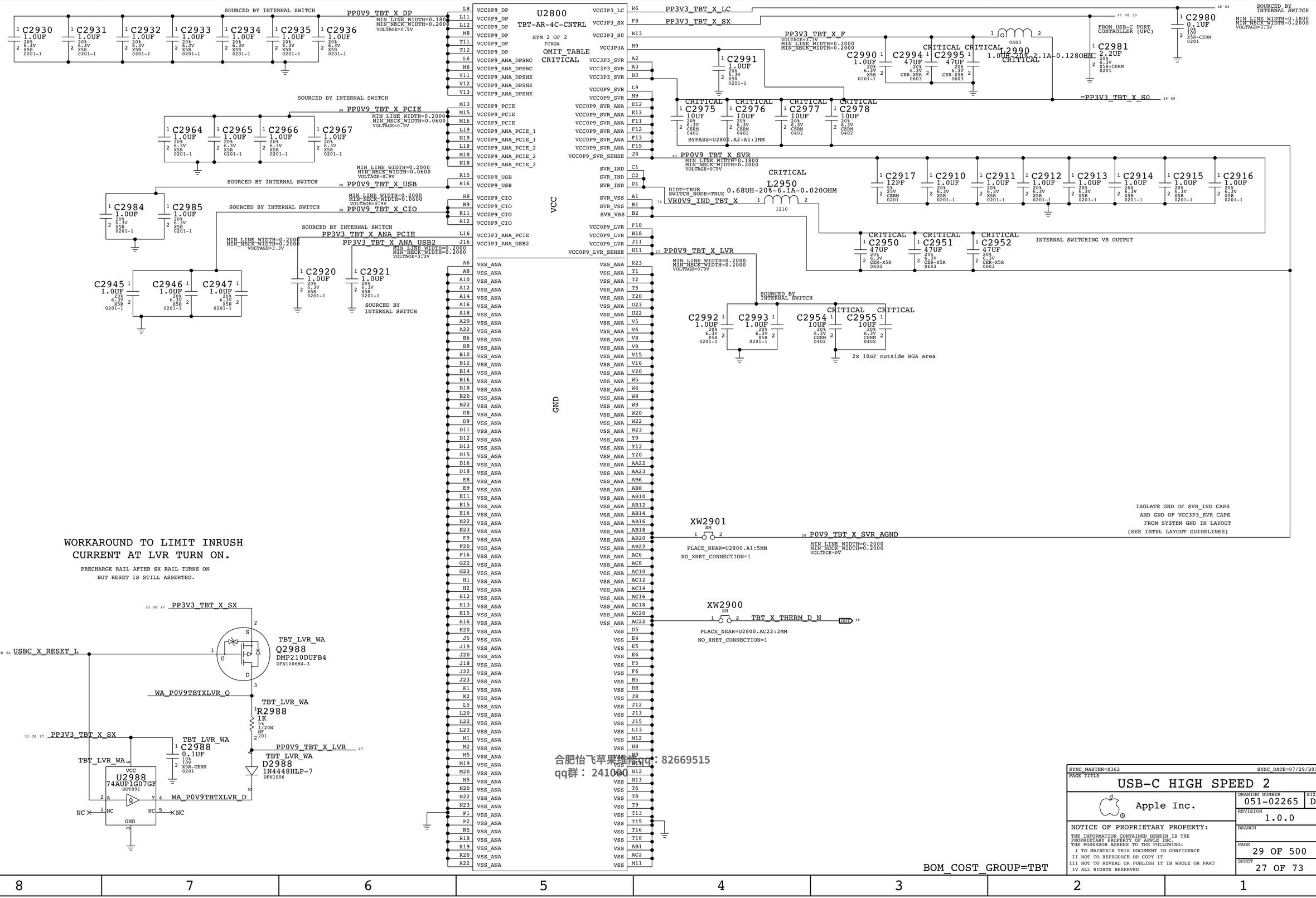

BOM_COST_GROUP=TBT

SYNC_MASTER=X362	SYNC_DATE=07/29/2015
PAGE TITLE	USB-C HIGH SPEED 2
Apple Inc.	DRAWING NUMBER 051-02265 SIZE D
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	BRANCH
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RIDGE AC COUPLING

R2D

19 15	IN	PCIE_TBT_X_R2D_C_P<0>	C3040 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_R2D_P<0>	OUT 26
19 15	IN	PCIE_TBT_X_R2D_C_N<0>	C3041 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_R2D_N<0>	OUT 26
15	IN	PCIE_TBT_X_R2D_C_P<1>	C3042 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_R2D_P<1>	OUT 26
15	IN	PCIE_TBT_X_R2D_C_N<1>	C3043 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_R2D_N<1>	OUT 26
15	IN	PCIE_TBT_X_R2D_C_P<2>	C3044 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_R2D_P<2>	OUT 26
15	IN	PCIE_TBT_X_R2D_C_N<2>	C3045 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_R2D_N<2>	OUT 26
15	IN	PCIE_TBT_X_R2D_C_P<3>	C3046 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_R2D_P<3>	OUT 26
15	IN	PCIE_TBT_X_R2D_C_N<3>	C3047 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_R2D_N<3>	OUT 26

D2R

26	IN	PCIE_TBT_X_D2R_C_P<0>	C3050 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_D2R_P<0>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_N<0>	C3051 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_D2R_N<0>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_P<1>	C3052 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_D2R_P<1>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_N<1>	C3053 0201 X5R	0.22UF 20% 6.3V	PCIE_TBT_X_D2R_N<1>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_P<2>	C3055 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_D2R_P<2>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_N<2>	C3056 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_D2R_N<2>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_P<3>	C3057 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_D2R_P<3>	OUT 15
26	IN	PCIE_TBT_X_D2R_C_N<3>	C3054 0201 X5R	0.22UF 20% 6.3V	TBT_PCIE_4LANES PCIE_TBT_X_D2R_N<3>	OUT 15

ACE RPD STRAPPING

CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE

29	USBC_XA_RPD_G1	R3026 0 5% 1/20W MF 0201		USBC_XA_CC1 29 31
29	USBC_XA_RPD_G2	R3022 0 5% 1/20W MF 0201		USBC_XA_CC2 29 31
30	USBC_XB_RPD_G1	R3011 0 5% 1/20W MF 0201		USBC_XB_CC1 30 32
30	USBC_XB_RPD_G2	R3024 0 5% 1/20W MF 0201		USBC_XB_CC2 30 32

ACE BUSPOWERZ STRAPPING

R3017 0 5% 1/20W MF 0201 — UPC_XA_BUSPOWERZ 29

R3019 0 5% 1/20W MF 0201 — UPC_XB_BUSPOWERZ 30

PU BUSPOWERZ TO LDO_3V3 TO NOT PASS VBUS TO SYS UNDER DB CASE

PU BUSPOWERZ TO 1V8D TO PASS VBUS TO SYS UNDER DB CASE USES INT POWER PATH

GND BUSPOWERZ TO PASS VBUS TO SYS UNDER DB CASE USES EXT POWER PATH

RIDGE DEBUG CONN

J3099 505070-1220 M-ST-SM UPC_DBG_HDR — 516S00115

28 26	OUT	TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L OUT 16 19
28 26	BI	DP_X_SNK0_HPD	3	4	USBC_X_RESET_L BI 26 27 33
28		ARKANOID_P5	5	6	PP3V3_TBT_X_SX 27 33
28		ARKANOID_P7	7	8	PP0V9_TBT_X_PCIE 27
28 16	BI	TBT_POC_RESET	9	10	PP0V9_TBT_X_USB 27
63 28 27	IN	PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO 27
			15	16	

ACE DEBUG CONN

J3098 505070-1220 M-ST-SM UPC_DBG_HDR — 516S00115

28 26	OUT	I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L OUT 26 28
42 29	BI	=I2C_UPC_XA_SCL2	3	4	I2C_TBT_X_SDA BI 26 28
42 29	BI	=I2C_UPC_XA_SDA2	5	6	I2C_TBT_X_SCL BI 26 28
42 39	BI	SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA OUT 29
28	BI	TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL 29
30 29	IN	UPC_XA_UART_TX	11	12	UPC_XA_UART_RX OUT 29 30
			15	16	

28 26	BI	DP_X_SNK1_HPD	ARKANOID:HPD R3080 0 5% 1/20W MF 0201	ARKANOID_P5 28
72 40 39 28	BI	SMC_DEBUGPRT_RX_L	ARKANOID:MOJO R3081 0 5% 1/20W MF 0201	
29 26	BI	DP_XA_HPD	ARKANOID:HPD R3082 0 5% 1/20W MF 0201	ARKANOID_P7 28
72 40 39 28	BI	SMC_DEBUGPRT_TX_L	ARKANOID:MOJO R3083 0 5% 1/20W MF 0201	

F3000 CRITICAL
6AMP-32V-0.0095OHM 0603
=PP20V_USBC_XA_VBUS 29 28 — PP20V_USBC_XA_VBUS_F 29

F3010 CRITICAL
6AMP-32V-0.0095OHM 0603
=PP20V_USBC_XB_VBUS 30 28 — PP20V_USBC_XB_VBUS_F 30

POWER ALIASES

29	=PP3V3_G3H_UPC_XA	PP3V3_G3H_UPC_XA	R3000 0 5% 1/20W MF 0201 PP3V3_G3H 19 28 41 42 47 51 52 53 60 68
30	=PP3V3_G3H_UPC_XB	PP3V3_G3H_UPC_XB	R3001 0 5% 1/20W MF 0201 PP3V3_G3H 19 28 41 42 47 51 52 53 60 68

MAKE_BASE=TRUE

29 28	=PP20V_USBC_XA_VBUS	MAKE_BASE=TRUE	PP20V_USBC_XA_VBUS 31 72
30 28	=PP20V_USBC_XB_VBUS	MAKE_BASE=TRUE	PP20V_USBC_XB_VBUS 32 72
29	=UPC_XA_I2C_STRAP	MAKE_BASE=TRUE	PP3V3_UPC_XA_LDO 29 69
29	=PP3V3R1V8_UPC_XA		
30	=UPC_XB_I2C_STRAP	MAKE_BASE=TRUE	PP3V3_UPC_XB_LDO 30 63 69
26	=PP3V3_TBT_X_FLASH	MAKE_BASE=TRUE	
30	=PP3V3R1V8_UPC_XB		
69 27	=PP3V3_TBT_X_S0	MAKE_BASE=TRUE	PP3V3_TBT_X_S0 63
30 29	=PPHV_INT_G3H		

MISC ALIASES

28 26	=UPC_X_SPI_CLK	UPC_X_SPI_CLK
28 26	=UPC_X_SPI_CS_L	UPC_X_SPI_CS_L
28 26	=UPC_X_SPI_MOSI	UPC_X_SPI_MOSI
28 26	=UPC_X_SPI_MISO	UPC_X_SPI_MISO
30 29	USBC_X_POC_RESET	TBT_POC_RESET 16 28
30 29 26	TBT_X_RTD3_CIO_PWR_EN	TBT_X_CIO_PWR_EN 13
30 29 26	TBT_X_RTD3_USB_PWR_EN	TBT_X_USB_PWR_EN 13
16	TBT_X_PLUG_EVENT_L	TBT_X_CIO_PLUG_EVENT_L 26 28
26	=TBT_X_BATLOW_L	PM_BATLOW_L 14 39
13	=USBC_TMS_X_SWD_CLK_X	JTAG_TBT_X_TMS 26 72
13	=USBC_TMS_T_SWD_DATA_X	PU_USBC_TMS_T_SWD_DATA_X
26	JTAG_TBT_TDO	JTAG_ISP_TDO 5
29	=USBC_XA_RESET_L	TP_USBC_XA_RESET_L
29	UPC_XA_SPI_CLK	
29	UPC_XA_SPI_CS_L	
29	UPC_XA_SPI_MISO	
29	UPC_XA_SPI_MOSI	
29	UPC_XA_RESET	
30	UPC_XB_RESET	

MAKE_BASE=TRUE

XW3001 SM
1 2 — P0V9_TBT_X_SVR_AGND 27
PLACE_NEAR=U2800.A1:5MM
NO_XNET_CONNECTION=1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

28 26	I2C_TBT_X_SDA	UPC XA - U3100	=I2C_UPC_XA_SDA1 29
28 26	I2C_TBT_X_SCL	(WRITE: 0X70 READ: 0X71)	=I2C_UPC_XA_SCL1 29
28 26	I2C_TBT_XA_INT_L		=I2C_UPC_XA_INT1_L 29
28 26	I2C_TBT_XB_INT_L		=I2C_UPC_XB_SDA1 30
	TBT - MASTER ALPINE RIDGE - U2800	UPC XB - U3200 (WRITE: 0X7E READ: 0X7F)	=I2C_UPC_XB_SCL1 30 =I2C_UPC_XB_INT1_L 30

MAKE_BASE=TRUE

26	TBT_X_SPI_CLK	R3098 100 5% 1/20W MF 201	TBT_X_SPI_CLK_DBG 28
26	TBT_X_SPI_CS_L	R3090 15 5% 1/20W MF 201	UPC_XB_SPI_CLK 30
26	TBT_X_SPI_MOSI	R3091 15 5% 1/20W MF 201	UPC_XB_SPI_CS_L 30
26	TBT_X_SPI_MISO	R3092 15 5% 1/20W MF 201	UPC_XB_SPI_MOSI 30
		R3093 15 5% 1/20W MF 201	UPC_XB_SPI_MISO 30
		R3094 15 5% 1/20W MF 201	=UPC_X_SPI_CLK 26 28
		R3095 15 5% 1/20W MF 201	=UPC_X_SPI_CS_L 26 28
		R3096 15 5% 1/20W MF 201	=UPC_X_SPI_MOSI 26 28
		R3097 15 5% 1/20W MF 201	=UPC_X_SPI_MISO 26 28

26	TBT_X_XTAL25M_OUT	C3002 20PF 5% C0G 25V 0201	
	NOSTUFF R3006 1M 5% 1/20W MF 201	CRITICAL Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM	
26	TBT_X_XTAL25M_IN	C3003 20PF 5% C0G 25V 0201	

15	BI	USB3_EXTA_R2D_C_P	C3020 0.1UF 0201 X5R-CERM 10% 16V	USB3_EXTA_R2D_P TP TP3091 SM-TPP3
15	BI	USB3_EXTA_R2D_C_N	C3021 0.1UF 0201 X5R-CERM 10% 16V	USB3_EXTA_R2D_N TP TP3092 SM-TPP3
15	OUT	USB3_EXTA_D2R_P		TP TP3093 SM-TPP3
15	OUT	USB3_EXTA_D2R_N		TP TP3094 SM-TPP3

72 29	BI	USBC_XA_USB_TOP_P	MAKE_BASE=TRUE	USBC_XA_USB_DBG_TOP_P BI 31
72 29	BI	USBC_XA_USB_TOP_N	MAKE_BASE=TRUE	USBC_XA_USB_DBG_TOP_N BI 31
72 29	BI	USBC_XA_USB_BOT_P	MAKE_BASE=TRUE	USBC_XA_USB_DBG_BOT_P BI 31
72 29	BI	USBC_XA_USB_BOT_N	MAKE_BASE=TRUE	USBC_XA_USB_DBG_BOT_N BI 31

CRITICAL
I3000
90-OHM-0.1A
EXCX4CE 2X1.6MM
PLACE_NEAR=U3100.L5:5MM
PLACE_NEAR=U3100.K5:5MM

28	=USB_UPC_XA_P	1 4	USB_UPC_XA_F_P MAKE_BASE=TRUE	=USB_UPC_XA_F_P OUT 29
28	=USB_UPC_XA_N	2 3	USB_UPC_XA_F_N MAKE_BASE=TRUE	=USB_UPC_XA_F_N OUT 29
30	TP_UPC_XB_SWD_CLK	TSP_UPC_XB_SWD_CLK MAKE_BASE=TRUE		TP TP3090 SM-TPP3

DP / USB SOURCE ALIASES

5 BI	DP_DDI1_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_P<3..0>	BI 19 26
5 BI	DP_DDI1_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_N<3..0>	BI 19 26
5 BI	DP_DDI1_AUXCH_C_P	MAKE_BASE=TRUE	DP_X_SNK1_AUXCH_C_P	BI 26
5 BI	DP_DDI1_AUXCH_C_N	MAKE_BASE=TRUE	DP_X_SNK1_AUXCH_C_N	BI 26
5 OUT	DP_DDPB_HPD	MAKE_BASE=TRUE	DP_X_SNK1_HPD	IN 26 28
5 BI	DP_DDI2_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_P<3..0>	BI 26
5 BI	DP_DDI2_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_N<3..0>	BI 26
5 BI	DP_DDI2_AUXCH_C_P	MAKE_BASE=TRUE	DP_X_SNK0_AUXCH_C_P	BI 26
5 BI	DP_DDI2_AUXCH_C_N	MAKE_BASE=TRUE	DP_X_SNK0_AUXCH_C_N	BI 26
5 OUT	DP_DDPC_HPD	MAKE_BASE=TRUE	DP_X_SNK0_HPD	IN 26 28

15 BI	USB_EXTB_P	MAKE_BASE=TRUE	USB_UPC_PCH_XA_P	=USB_UPC_XA_P BI 28
15 BI	USB_EXTB_N	MAKE_BASE=TRUE	USB_UPC_PCH_XA_N	=USB_UPC_XA_N BI 28
26 BI	USB_UPC_XA_P	R3012 0 5% 1/20W MF 0201		
26 BI	USB_UPC_XA_N	R3013 0 5% 1/20W MF 0201		
29 IN	UPC_XA_FAULT_L	R3008 0 5% 1/20W MF 0201	USB_EXTA_OC_L	OUT 17
15 BI	NC_USB2_08P	MAKE_BASE=TRUE	USB_UPC_PCH_XB_P	=USB_UPC_XB_P BI 30
15 BI	NC_USB2_08N	MAKE_BASE=TRUE	USB_UPC_PCH_XB_N	=USB_UPC_XB_N BI 30
26 BI	USB_UPC_XB_P	R3014 0 5% 1/20W MF 0201		
26 BI	USB_UPC_XB_N	R3015 0 5% 1/20W MF 0201		
30 IN	UPC_XB_FAULT_L	R3018 0 5% 1/20W MF 0201	USB_EXTB_OC_L	OUT 17

PP3V3_TBT_X_LC 27 28 63

1	100K	R3071 5% 1/20W MF 201	TBT_X_HDMI_DDC_CLK 26
1	100K	R3035 5% 1/20W MF 201	72 26 JTAG_TBT_TCK — R3033 0 5% 1/20W MF 0201 — JTAG_ISP_TCK 17 19
1	100K	R3036 5% 1/20W MF 201	72 26 JTAG_TBT_TDI — R3034 0 5% 1/20W MF 0201 — JTAG_ISP_TDI 17 19
1	100K	R3073 5% 1/20W MF 201	UPC_XA_DBG3 29
1	100K	R3074 5% 1/20W MF 201	UPC_XA_DBG4 29
1	100K	R3072 5% 1/20W MF 201	TBT_X_HDMI_DDC_DATA 26
1	100K	R3066 5% 1/20W MF 201	DP_X_SNK0_DDC_DATA — MAKE_BASE=TRUE — =DP_X_SNK0_DDC_DATA OUT 26
1	100K	R3067 5% 1/20W MF 201	DP_X_SNK0_DDC_CLK — MAKE_BASE=TRUE — =DP_X_SNK0_DDC_CLK OUT 26
1	100K	R3069 5% 1/20W MF 201	DP_X_SNK1_DDC_CLK — MAKE_BASE=TRUE — =DP_X_SNK1_DDC_CLK OUT 26
1	100K	R3070 5% 1/20W MF 201	DP_X_SNK1_DDC_DATA — MAKE_BASE=TRUE — =DP_X_SNK1_DDC_DATA OUT 26
1	100K	R3040 5% 1/20W MF 201	PD_UPC_XA_GPIO5 — MAKE_BASE=TRUE — UPC_XA_HPD_RX OUT 29
1	100K	R3041 5% 1/20W MF 201	PD_UPC_XB_GPIO5 — MAKE_BASE=TRUE — UPC_XB_HPD_RX OUT 30
1	100K	R3042 5% 1/20W MF 201	PD_UPC_XA_GPIO6 — MAKE_BASE=TRUE — UPC_XA_5V_EN OUT 29 PD WHEN NOT USED
1	100K	R3043 5% 1/20W MF 201	PD_UPC_XB_GPIO6 — MAKE_BASE=TRUE — UPC_XB_5V_EN OUT 30
1	100K	R3049 5% 1/20W MF 201	PD_TBT_X_TMU_CLK_OUT — MAKE_BASE=TRUE — =TBT_X_TMU_CLK_OUT OUT 26
1	100K	R3050 5% 1/20W MF 201	PD_TBT_X_GPIO_8 — MAKE_BASE=TRUE — =TBT_X_GPIO_8 OUT 26
1	1M	R3020 5% 1/20W MF 201	DP_X_SRC_HPD 26

LOCAL BULK CAP

=PP5V_USBC 69

CRITICAL
C3000 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

29	OUT	UPC_XA_DBG1	SMC_TCK OUT 39 40 47 72
29	IN	UPC_XA_DBG2	SMC_TMS IN 39 40 47 72
30	OUT	UPC_XB_DBG1	SSD_JTAG_TCK OUT 67
30	IN	UPC_XB_DBG2	SSD_JTAG_TMS IN 67
30	OUT	UPC_XB_DBG3	SMC_DEBUGPRT_TX_L OUT 28 39 40 72
30	IN	UPC_XB_DBG4	SMC_DEBUGPRT_RX_L IN 28 39 40 72

MAKE_BASE=TRUE

XPD JTAG ISOLATION

PD WHEN NOT USED

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE
USB-C SUPPORT

Apple Inc.

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PRIMARY ACE USB-C PORT CONTROLLER (UPC)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0304	2	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C3109,C3209		ACE_SS_CAP:A_B
132S0390	2	CAP,CER,X5R,0.47UF,10%,6.3V,0201	C3109,C3209		ACE_SS_CAP:C0

BOM_COST_GROUP=USB-C

SYNC_MASTER=X85-REF SYNC_DATE=06/17/2015

PAGE TITLE: USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D

REVISION: 1.0.0

BRANCH

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

PULL R3209 AND R3208 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

=UPC_XB_I2C_STRAP 28

1M R3209 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SCL 30
1M R3208 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SDA 30

1M R3205 5% 1/20W MF 201 — UPC_XA_UART_TX 28 29 30

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

CRITICAL
R3203 15K 0.1% 1/20W TF-LF 0201
NEED 0.1%

TO SMC
=I2C_UPC_XB_SDA2 42
=I2C_UPC_XB_SCL2 42
=I2C_UPC_XB_INT2_L 42

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

CRITICAL
L3200 90-OHM-0.1A EXCX4CE

=USB_UPC_XB_P 28 B1 — 1 — PLACE_NEAR=U3200.L5:5mm
=USB_UPC_XB_N 28 B1 — 2 — 3 — PLACE_NEAR=U3200.K5:5mm

=PP3V3_UPC_XB_AUX 69
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
R3210 100K 5% 1/20W MF 201
R3211 100K 5% 1/20W MF 201

FUSE
Add on support page
PP20V_USBC_XB_VBUS_F 28
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=20V

=PP20V_USBC_XB_VBUS 28

CRITICAL
Q3200
FDPC4044
PWR-CLIP-33

NOSTUFF C3220 4700PF 10% 25V CER-X5R 0201
NOSTUFF C3221 4700PF 10% 25V CER-X5R 0201
NCNC

C3201 1UF 10% 25V X5R 0402

=PPHV_EXT_G3H 29 69
MAX 100uF TOTAL ON RAIL

UPC_XB_GATE1
UPC_XB_GATE2

=PP3V3R1V8_UPC_XB 28
=PP3V3_G3H_UPC_XB 28
=PPHV_INT_G3H 29 28
=PP5V_XB_USBC 69
CAP FOR PP_5V0 ON VR PAGE

CRITICAL
C3200 10UF 20% 6.3V CERM 0402

PP3V3_UPC_XB_LDO 28 63 69
MIN_LINE_WIDTH=0.0180
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V
=PP3V3_UPC_XB_SX 33
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_XB_LDOA
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.3V
PP1V8_UPC_XB_LDOD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
PP1V1_UPC_XB_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.1V

C3205 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C3208 10UF 20% 6.3V CERM 0402
C3204 2.2UF 20% 6.3V X5R-CERM 0201
C3206 0.47UF 20% 4V CERM-X5R-1 201

CRITICAL
OMIT_TABLE
U3200
CD3215A10
BGA

29 28	USBC_X_POC_RESET	E11	MRESET
33	=USBC_XB_RESET_L	F11	RESET*
72	TP_UPC_XB_DBG_UART_TX	B2	GPIO0
72	TP_UPC_XB_DBG_UART_RX	C2	GPIO1
29 28 26 B1	TBT_X_RTD3_CIO_PWR_EN	D10	GPIO2
29 28 26 B1	TBT_X_RTD3_USB_PWR_EN	G11	GPIO3
26 OUT	DP_XB_HPD	C10	GPIO4
28	UPC_XB_HPD_RX	E10	GPIO5
28 OUT	UPC_XB_5V_EN	G10	GPIO6
41 29 OUT	=UPC_WAKE_L	D7	GPIO7
28 OUT	UPC_XB_FAULT_L	H6	GPIO8
28 IN	UPC_XB_BUSPOWERZ	F10	BUSPOWERZ
70	NC_UPC_XB_I2C_ADDR	F1	I2C_ADDR
	UPC_XB_R_OSC	G2	R_OSC
30	I2C_UPC_XB_DBG_CTL_SCL	E4	DEBUG_CTL1
30	I2C_UPC_XB_DBG_CTL_SDA	D5	DEBUG_CTL2
28 B1	=I2C_UPC_XB_SDA1	D1	I2C_SDA1
28 B1	=I2C_UPC_XB_SCL1	D2	I2C_SCL1
28 OUT	=I2C_UPC_XB_INT1_L	C1	I2C_IRQ1*
42 B1	=I2C_UPC_XB_SDA2	A5	I2C_SDA2
42 B1	=I2C_UPC_XB_SCL2	B5	I2C_SCL2
42 OUT	=I2C_UPC_XB_INT2_L	B6	I2C_IRQ2*
28 OUT	UPC_XB_SPI_CLK	A3	SPI_CLK
28 OUT	UPC_XB_SPI_MOSI	B4	SPI_MOSI
28 IN	UPC_XB_SPI_MISO	A4	SPI_MISO
28 OUT	UPC_XB_SPI_CS_L	B3	SPI_SSZ
70	TP_UPC_XB_SWD_DATA	F4	SWD_DATA
28	TP_UPC_XB_SWD_CLK	G4	SWD_CLK
30 29 28	UPC_XA_UART_TX	F2	UART_RX
29 28 OUT	UPC_XA_UART_RX	E2	UART_TX
26 IN	TBT_XB_LSTX	L4	LSX_R2P
26 OUT	TBT_XB_LSRX	K4	LSX_P2R
72	USB_UPC_XB_F_P	L5	USB_RP_P
72	USB_UPC_XB_F_N	K5	USB_RP_N
	DP_XB_AUXCH_P	J1	AUX_P
	DP_XB_AUXCH_N	J2	AUX_N
28 B1	UPC_XB_DBG1	L2	DEBUG1
28 B1	UPC_XB_DBG2	K2	DEBUG2
28 B1	UPC_XB_DBG3	L3	DEBUG3
28 B1	UPC_XB_DBG4	K3	DEBUG4

DIGITAL CORE I/O AND CONTROL
PORT MUX
HV FET/SENSE CONTROL
TYPE-C

VBUS	H11 J10 J11 K11	
VIN_3V3	H1	
VDDIO	B1	
LDO_3V3	G1	
VOUT_3V3	H2	
LDO_1V8A	K1	
LDO_1V8D	A2	
LDO_BMC	E1	
PP_5V0	A11 B11 C11 D11	
PP_HV	A6 A7 A8 B7	
PP_CABLE	H10	
SS	H7	UPC_XB_SS
SENSEP	B10	
SENSEN	A10	
HV_GATE1	B9	
HV_GATE2	A9	

OMIT_TABLE
C3209 0.22UF 20% 6.3V X5R 0201

C_CC1	L9	USBC_XB_CC1
C_CC2	L10	USBC_XB_CC2
RPD_G1	K9	USBC_XB_RPD_G1
RPD_G2	K10	USBC_XB_RPD_G2
C_USB_TP	K6	USBC_XB_USB_TOP_P
C_USB_TN	L6	USBC_XB_USB_TOP_N
C_USB_BP	K7	USBC_XB_USB_BOT_P
C_USB_BN	L7	USBC_XB_USB_BOT_N
C_SBU1	K8	USBC_XB_SBU1
C_SBU2	L8	USBC_XB_SBU2
GROUND		
NC	L11	

B1 28 32 / B1 28 32
B1 28 / B1 28
B1 32 72 / B1 32 72
B1 32 72 / B1 32 72
B1 32 / B1 32

C3214 220PF 2% 50V C0G 0201
C3213 220PF 2% 50V C0G 0201

MIN_LINE_WIDTH=0.3500
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.3500
MIN_NECK_WIDTH=0.2000

NC or GND to dissipate heat

GND: A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7

UPC_XB_RESET 28
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=E85-REF SYNC_DATE=06/17/2015
PAGE TITLE
USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
BRANCH
PAGE 32 OF 500
SHEET 30 OF 73

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S00017	4	TVS DIODE,1LINE,BIDIR,3.5HF,3.3V,0201	D3300,D3309,D3408,D3409	CRITICAL	

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
OMIT
L3300
SHORT
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.1500
PP20V_USBC_XA_VBUS
PP20V_USBC_XA_VBUS_CONN
PLACE VBUS CAP NEAR EACH VBUS PIN
CRITICAL D3300 NSR20F40NX_G
NOSTUFF C3304 1UF 10% 25V X5R 402
C3309 1UF 10% 25V X5R 402
C3300 0.01UF 10% 25V X5R-CERM 0201
C3301 0.01UF 10% 25V X5R-CERM 0201
C3302 0.01UF 10% 25V X5R-CERM 0201
C3303 0.01UF 10% 25V X5R-CERM 0201
C3306 0.01UF 10% 25V X5R-CERM 0201
C3307 0.01UF 10% 25V X5R-CERM 0201
C3308 0.01UF 10% 25V X5R-CERM 0201
C3305 0.01UF 10% 25V X5R-CERM 0201

TBT_RX0
USBC_XA_D2R_P<1>
USBC_XA_D2R_N<1>
R3374 0 5% 1/20W MF 0201
R3375 0 5% 1/20W MF 0201
GND_VOID=TRUE
USBC_XA_D2R_CONN_P<1>
USBC_XA_D2R_CONN_N<1>
D3302 ESD101-B1-02ELS 0201-THICKSTNCL
D3303 ESD101-B1-02ELS 0201-THICKSTNCL
D3310 ESD101-B1-02ELS 0201-THICKSTNCL
D3311 ESD101-B1-02ELS 0201-THICKSTNCL
C3370 0.22UF 10% 6.3V X5R-CERM 0201
C3371 0.22UF 10% 6.3V X5R-CERM 0201
USBC_XA_R2D_C_P<1>
USBC_XA_R2D_C_N<1>
TBT_TX0

J3300
RCPT-USBC-POR-J130
M-RT-TH
SYM 1 OF 2
PORT A
514-00062
(NO LANE REVERSALS ALLOWED.)

DP_HPD
SBU2 (RFU2)
USBC_XA_SBU2
USBC_XA_CC1_CONN
CC1
D+/D- BOTTOM CC2
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_CC2_CONN
D3304 ESD112-B1-02ELS 0201-THICKSTNCL
D3305 ESD112-B1-02ELS 0201-THICKSTNCL
D3301 5.5V-6.2PF 0201-THICKSTNCL
OMIT_TABLE
D3308 5.5V-6.2PF 0201-THICKSTNCL
D3309 5.5V-6.2PF 0201-THICKSTNCL
D3316 5.5V-6.2PF 0201-THICKSTNCL
D3312 ESD112-B1-02ELS 0201-THICKSTNCL
D3313 ESD112-B1-02ELS 0201-THICKSTNCL
USBC_XA_USB_DBG_TOP_P
USBC_XA_USB_DBG_TOP_N
USBC_XA_SBU1
D+/D- TOP
DP_AUX_P
SBU1 (RFU1)

TBT_TX1
USBC_XA_R2D_C_N<2>
USBC_XA_R2D_C_P<2>
C3372 0.22UF 10% 6.3V X5R-CERM 0201
C3373 0.22UF 10% 6.3V X5R-CERM 0201
GND_VOID=TRUE
USBC_XA_R2D_N<2>
USBC_XA_R2D_P<2>
D3306 ESD101-B1-02ELS 0201-THICKSTNCL
D3307 ESD101-B1-02ELS 0201-THICKSTNCL
GND
SHLD
USBC_XA_D2R_CONN_N<2>
USBC_XA_D2R_CONN_P<2>
R3376 0 5% 1/20W MF 0201
R3377 0 5% 1/20W MF 0201
USBC_XA_D2R_N<2>
USBC_XA_D2R_P<2>
D3314 ESD101-B1-02ELS 0201-THICKSTNCL
D3315 ESD101-B1-02ELS 0201-THICKSTNCL
TBT_RX1

R3350 100OHM-20%-24V-0.3A 0603
Q3350 DMT5015LFDF UDFN202-6
USBC_XA_CC1_CONN
USBC_XA_CC1
C3352 680PF 10% 25V X7R-CERM 0201
R3352 4.02K 1% 1/20W MF 201
SAVE_CC1A_Y
R3351 10K 5% 1/20W MF 201
=PPBUS_G3H
SAVE_CC1A_G
D3352 GDZ5V6LP3 5.6V DFN0201
SAVE_CC1A_B
Q3351 NSS60101DMT WDFN6
R3353 4.99K 1% 1/20W MF 201

R3360 100OHM-20%-24V-0.3A 0603
Q3360 DMT5015LFDF UDFN202-6
USBC_XA_CC2_CONN
USBC_XA_CC2
C3362 680PF 10% 25V X7R-CERM 0201
R3362 4.02K 1% 1/20W MF 201
SAVE_CC2A_Y
R3361 10K 5% 1/20W MF 201
=PPBUS_G3H
SAVE_CC2A_G
D3362 GDZ5V6LP3 5.6V DFN0201
SAVE_CC2A_B
Q3351 NSS60101DMT WDFN6
R3363 4.99K 1% 1/20W MF 201

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016
PAGE TITLE
USB-C CONNECTOR A
Apple Inc.
DRAWING NUMBER 051-02265
SIZE D
REVISION 1.0.0
BRANCH
PAGE 33 OF 500
SHEET 31 OF 73

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500

OMIT
L3400
SHORT
MAX RDCR = 12 MOHM
MANUFACTURER_PART_NUMBER NONE
MANUFACTURER NONE
PACKAGE 603

PP20V_USBC_XB_VBUS
PP20V_USBC_XB_VBUS_CONN

CRITICAL
D3400
DSN2
NSR20F40NX_G

NOSTUFF
C3404
1UF
10% 25V X5R 402

C3409
1UF
10% 25V X5R 402

PLACE VBUS CAP NEAR EACH VBUS PIN

BYPASS=J3300.A58::2MM
BYPASS=J3300.A59::2MM
BYPASS=J3300.A68::2MM
BYPASS=J3300.A67::2MM

CRITICAL
C3400 C3401 C3402 C3403 C3406 C3407 C3408 C3405
0.01UF
10% 25V X5R-CERM 0201

GND_VOID=TRUE

TBT_RX0
USBC_XB_D2R_P<1>
USBC_XB_D2R_N<1>
R3474 R3475
0 5% 1/20W MF 0201
USBC_XB_D2R_CONN_P<1>
USBC_XB_D2R_CONN_N<1>

CRITICAL
D3402 D3403
ESD101-B1-02ELS
0201-THICKSTNCL

USBC_XB_R2D_P<1>
USBC_XB_R2D_N<1>
C3470 C3471
0.22UF 10% 6.3V X5R-CERM 0201
USBC_XB_R2D_C_P<1>
USBC_XB_R2D_C_N<1>
TBT_TX0

CRITICAL
D3410 D3411
ESD101-B1-02ELS
0201-THICKSTNCL

DP_HPD
SBU2 (RFU2)
USBC_XB_SBU2
USBC_XB_CC1_CONN
CC1

J3300
RCPT-USBC-POR-J130
M-RT-TH
SYM 2 OF 2
PORT B
514-00062

CONN2_RX1+ 33
CONN2_RX1- 32
CONN2_VBUS0 30
CONN2_RFU2 48
CONN2_D2- 47
CONN2_D2+ 46
CONN2_CC2 45
CONN2_VBUS1 31
CONN2_TX2- 29
CONN2_TX2+ 28
CONN2_TX1+ 17
CONN2_TX1- 16
CONN2_VBUS2 34
CONN2_CC1 52
CONN2_D1+ 51
CONN2_D1- 50
CONN2_RFU1 49
CONN2_VBUS3 35
CONN2_RX2- 13
CONN2_RX2+ 12
GND 14 15 18 11 44 68 69 70 71 72 73 74 75 76 79 80 81 82 83 84

D+/D-
BOTTOM
CC2
USBC_XB_USB_BOT_N
USBC_XB_USB_BOT_P
USBC_XB_CC2_CONN

CRITICAL
D3404
ESD112-B1-02ELS
0201-THICKSTNCL

CRITICAL
D3405
ESD112-B1-02ELS
0201-THICKSTNCL

CRITICAL
D3401
5.5V-6.2PF
0201-THICKSTNCL

OMIT_TABLE
CRITICAL
D3408
5.5V-6.2PF
0201-THICKSTNCL

OMIT_TABLE
CRITICAL
D3409
5.5V-6.2PF
0201-THICKSTNCL

CRITICAL
D3416
5.5V-6.2PF
0201-THICKSTNCL

USBC_XB_USB_TOP_P
USBC_XB_USB_TOP_N
USBC_XB_SBU1
D+/D- TOP
DP_AUX_P
SBU1 (RFU1)

CRITICAL
D3412 D3413
ESD112-B1-02ELS
0201-THICKSTNCL

TBT_TX1
USBC_XB_R2D_C_N<2>
USBC_XB_R2D_C_P<2>
C3472 C3473
0.22UF 10% 6.3V X5R-CERM 0201
USBC_XB_R2D_N<2>
USBC_XB_R2D_P<2>

CRITICAL
D3406 D3407
ESD101-B1-02ELS
0201-THICKSTNCL

470K PD PROVIDES
DC PATH TO GND
(NEEDED EVEN IF
ESD DIODES PRESENT)

(NO LANE REVERSALS ALLOWED.)

USBC_XB_D2R_CONN_N<2>
USBC_XB_D2R_CONN_P<2>
R3476 R3477
0 5% 1/20W MF 0201
USBC_XB_D2R_N<2>
USBC_XB_D2R_P<2>
TBT_RX1

CRITICAL
D3414 D3415
ESD101-B1-02ELS
0201-THICKSTNCL

CRITICAL
R3450
100OHM-20%-24V-0.3A
0603

CRITICAL
Q3450
DMT5015LFDF
UDFN202-6

USBC_XB_CC1_CONN
USBC_XB_CC1
C3452
680PF
10% 25V X7R-CERM 0201
R3452
4.02K
1% 1/20W MF 201
R3451
10K
5% 1/20W MF 201
=PPBUS_G3H
SAVE_CC1B_Z
SAVE_CC1B_G
SAVE_CC1B_B
CRITICAL
D3452
GDZ5V6LP3
DFN0201
Q3451
NSS60101DMT
WDFN6
R3453
4.99K
1% 1/20W MF 201

CRITICAL
R3460
100OHM-20%-24V-0.3A
0603

CRITICAL
Q3460
DMT5015LFDF
UDFN202-6

USBC_XB_CC2_CONN
USBC_XB_CC2
C3462
680PF
10% 25V X7R-CERM 0201
R3462
4.02K
1% 1/20W MF 201
R3461
10K
5% 1/20W MF 201
=PPBUS_G3H
SAVE_CC2B_Z
SAVE_CC2B_G
SAVE_CC2B_B
CRITICAL
D3462
GDZ5V6LP3
DFN0201
Q3451
NSS60101DMT
WDFN6
R3463
4.99K
1% 1/20W MF 201

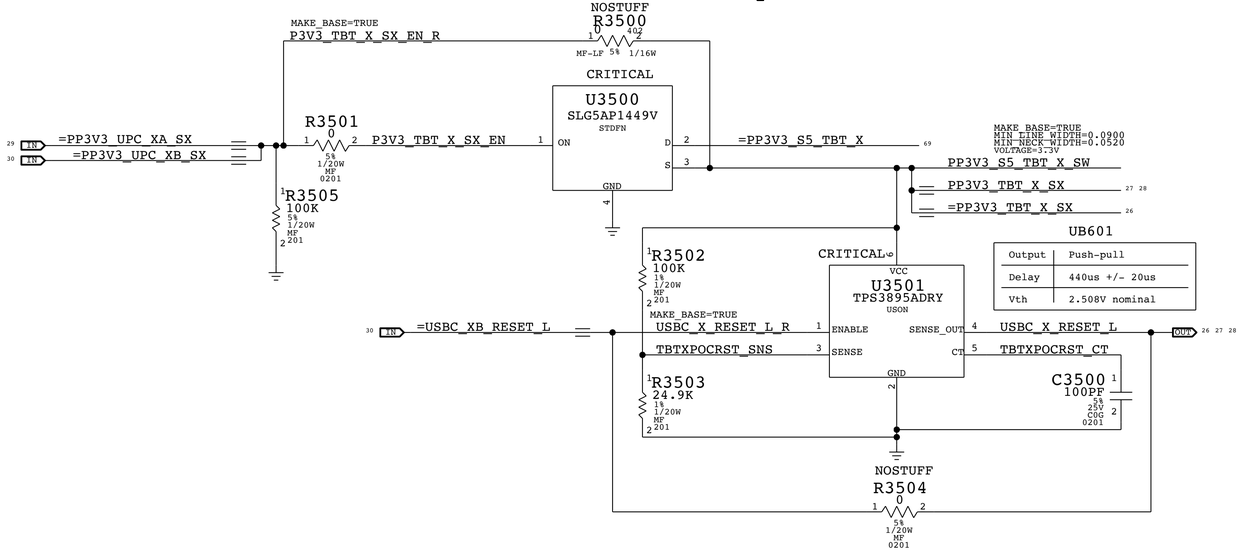
BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016
SYNC_MASTER=PAULH SYNC_DATE=04/15/2015
PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
BRANCH
PAGE 34 OF 500
SHEET 32 OF 73

TBT T "POC" Power-up Reset



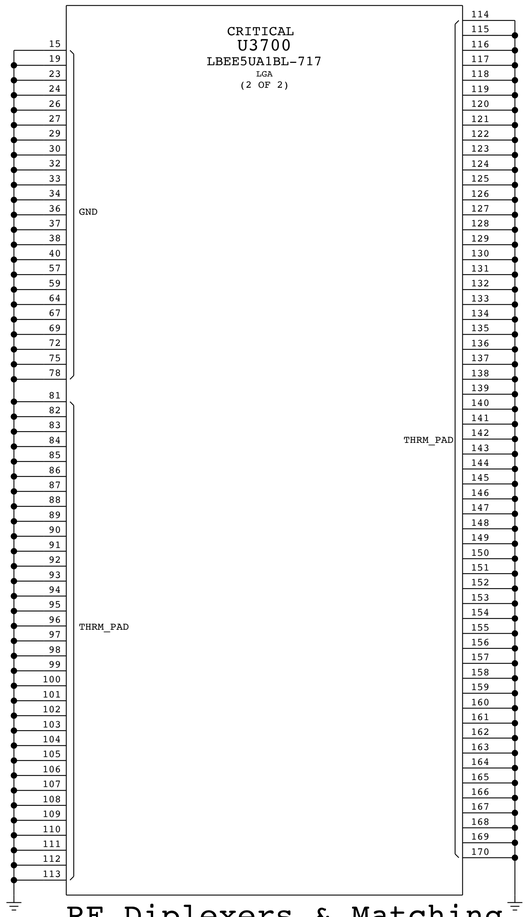
BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

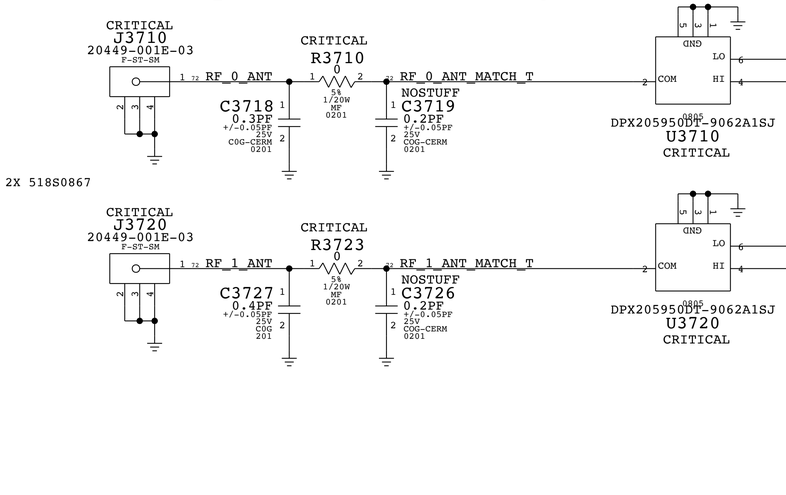
PAGE TITLE
USB-C SUPPORT 2

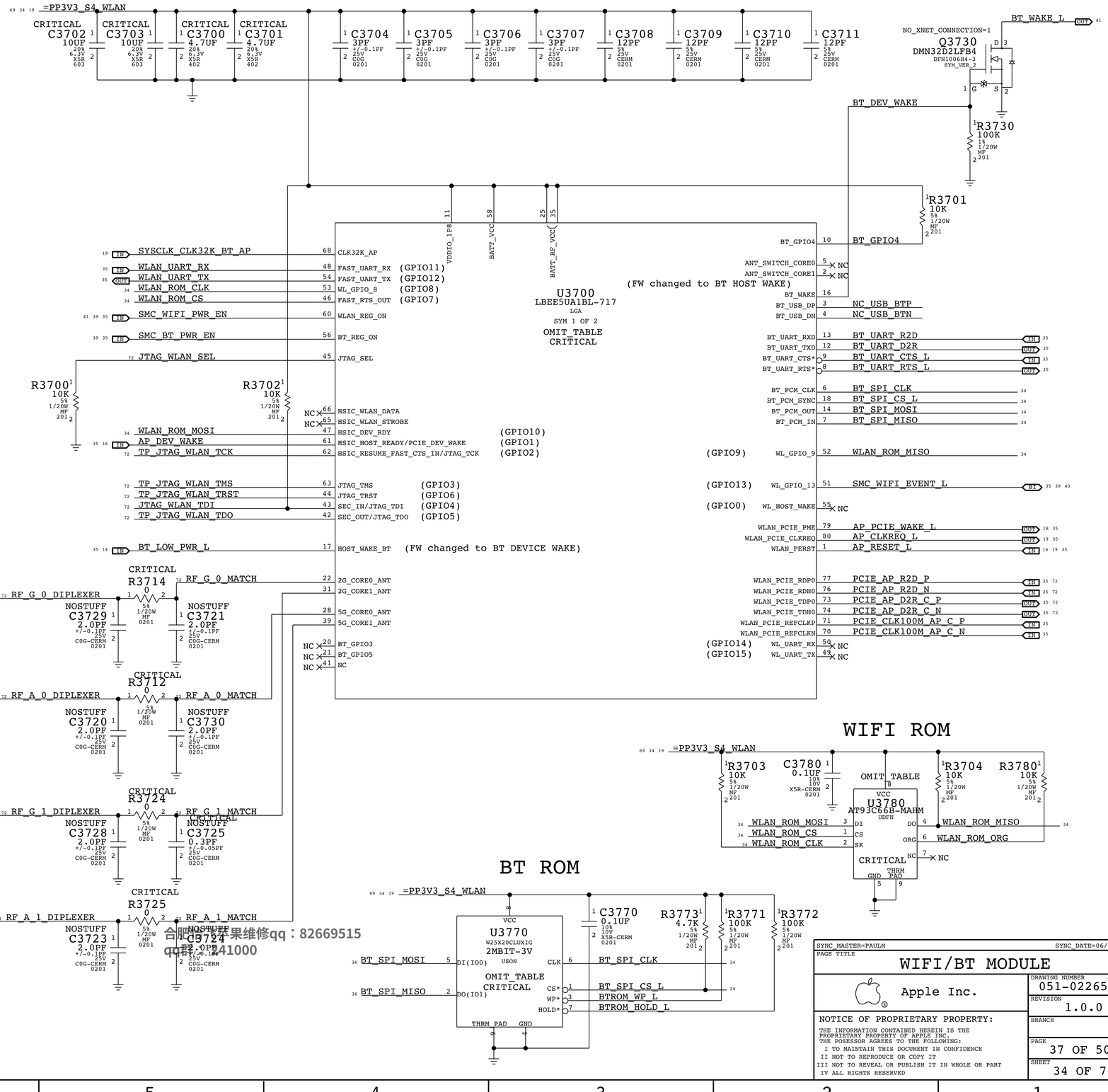
Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
BRANCH
PAGE 35 OF 500
SHEET 33 OF 73



RF Diplexers & Matching





WIFI ROM

BT ROM

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

WIFI/BT MODULE

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

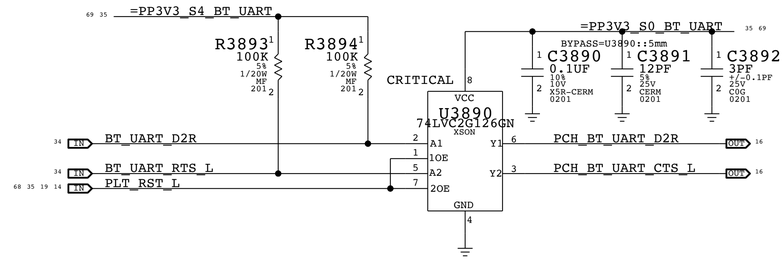
REVISION 1.0.0

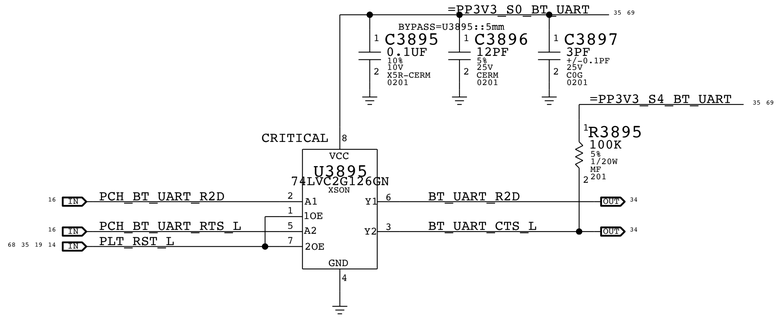
BRANCH

PAGE 37 OF 500

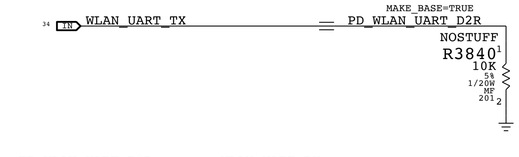
SHEET 34 OF 73

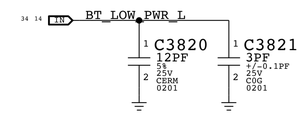
BT UART Isolation

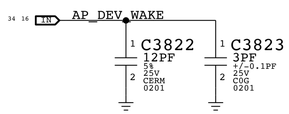


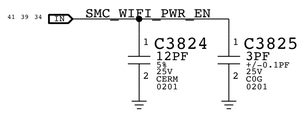


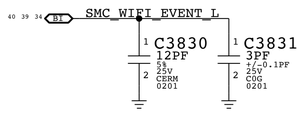
WIFI UART ISOLATION

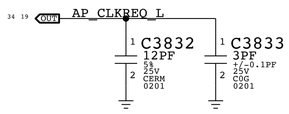


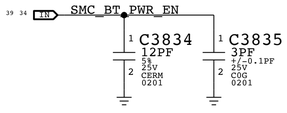


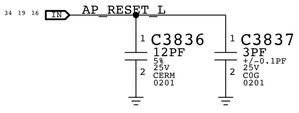


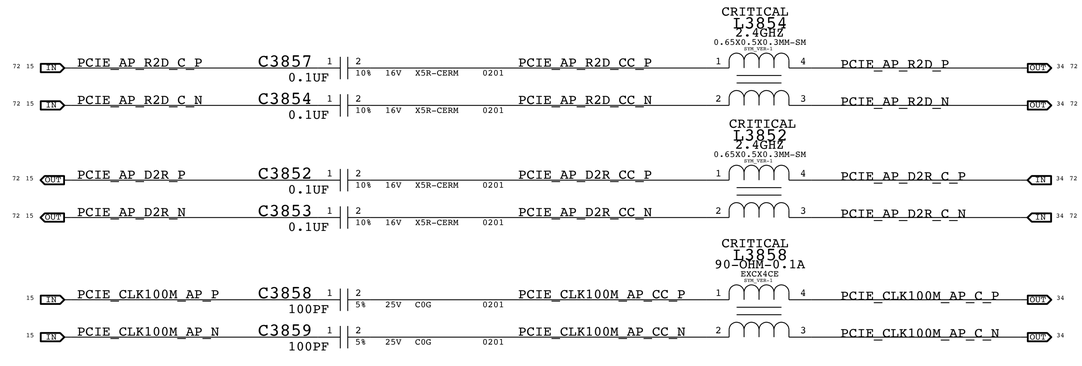












PAGE TITLE

WIFI/BT Module Support

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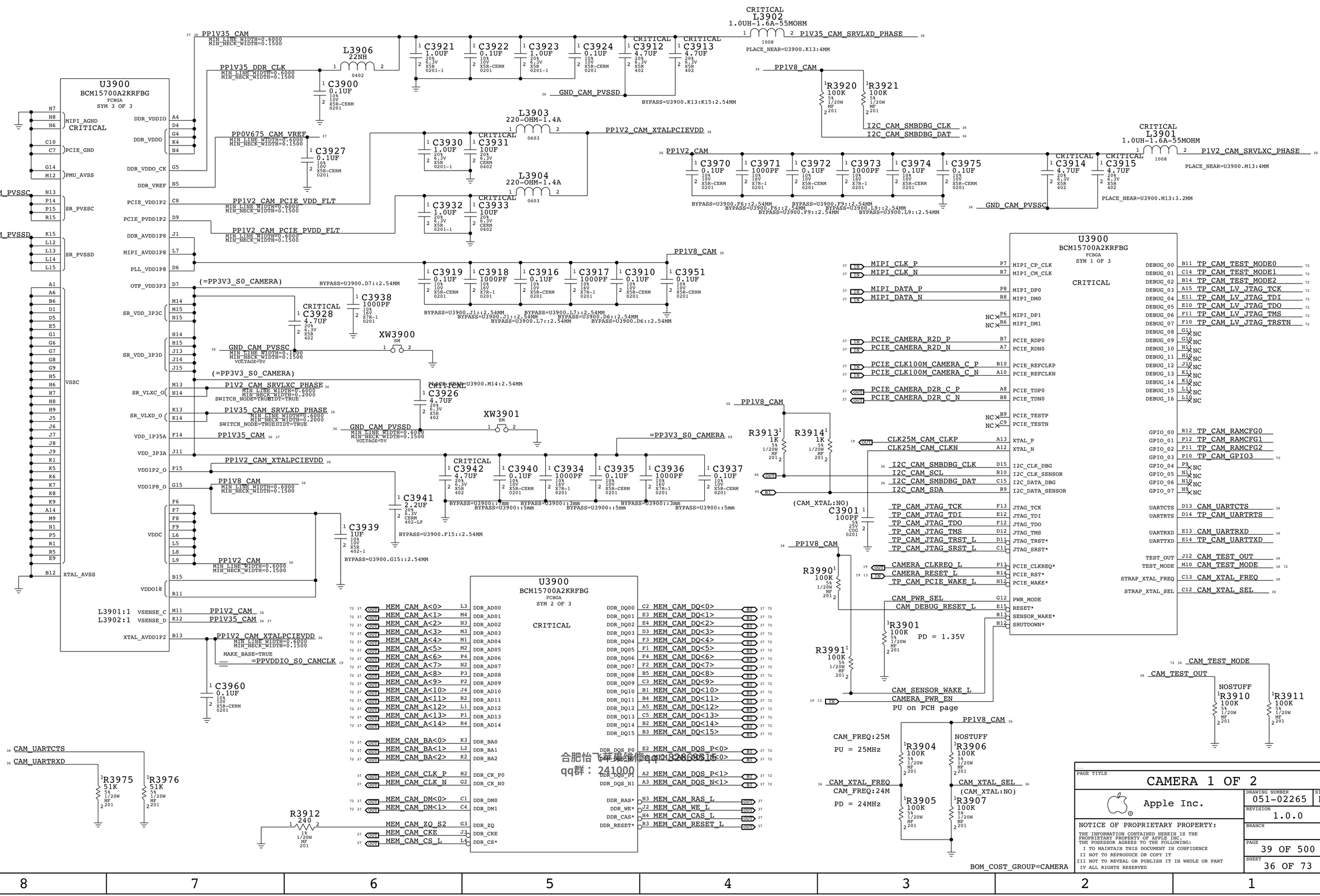
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U3900
BCM15760A2KRFBG
FCBGA
SYM 3 OF 3
CRITICAL
U3900
BCM15760A2KRFBG
FCBGA
SYM 1 OF 3
CRITICAL
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
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PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V2_CAM_XTALPCIEVDD
PP1V35_CAM_SRVLXD_PHASE
PP1V2_CAM_SRVLXC_PHASE
PP1V8_CAM
PP1V35_CAM
GND_CAM_PVSSD
GND_CAM_PVSSC
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
=PP3V3_S0_CAMERA
=PPVDDIO_S0_CAMCLK
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I2C_CAM_SMBDBG_DAT
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SCL
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
TP_CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAMERA_RESET_L
TP_CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
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MEM_CAM_CKE
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MEM_CAM_WE_L
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MEM_CAM_RESET_L
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CAM_TEST_OUT
TP_CAM_TEST_MODE0
TP_CAM_TEST_MODE1
TP_CAM_TEST_MODE2
TP_CAM_LV_JTAG_TCK
TP_CAM_LV_JTAG_TDI
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CAM_TEST_MODE
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CAM_FREQ:24M
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PAGE TITLE
CAMERA 1 OF 2
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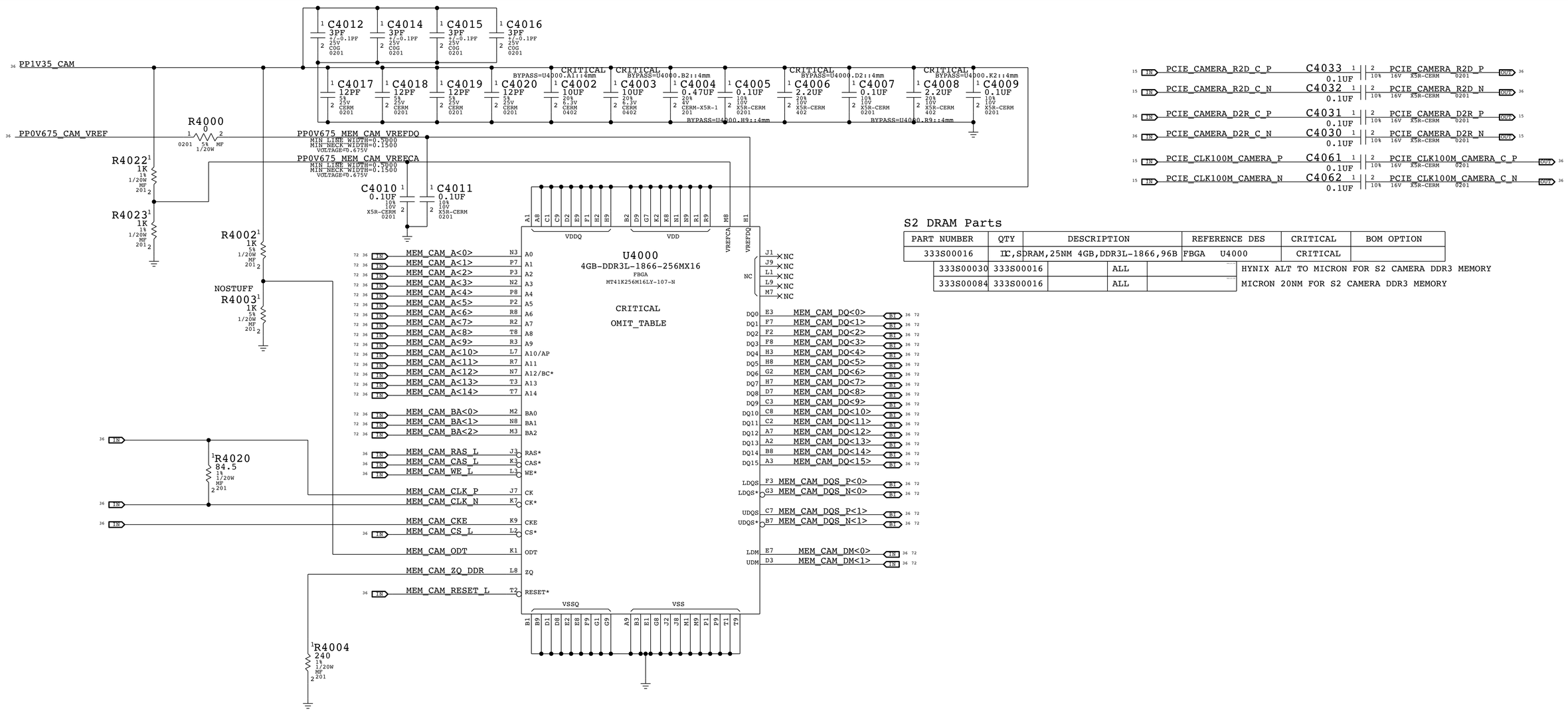

S2 DRAM Parts

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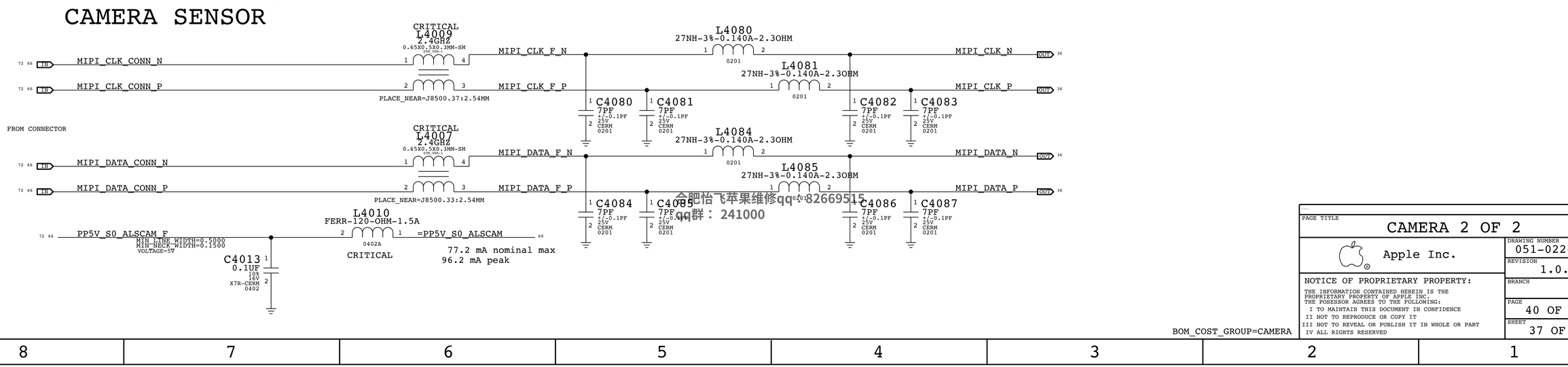
333S00030	333S00016	ALL			HYNIX ALT TO MICRON FOR S2 CAMERA DDR3 MEMORY
333S00084	333S00016	ALL			MICRON 20NM FOR S2 CAMERA DDR3 MEMORY



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PAGE TITLE: CAMERA 2 OF 2

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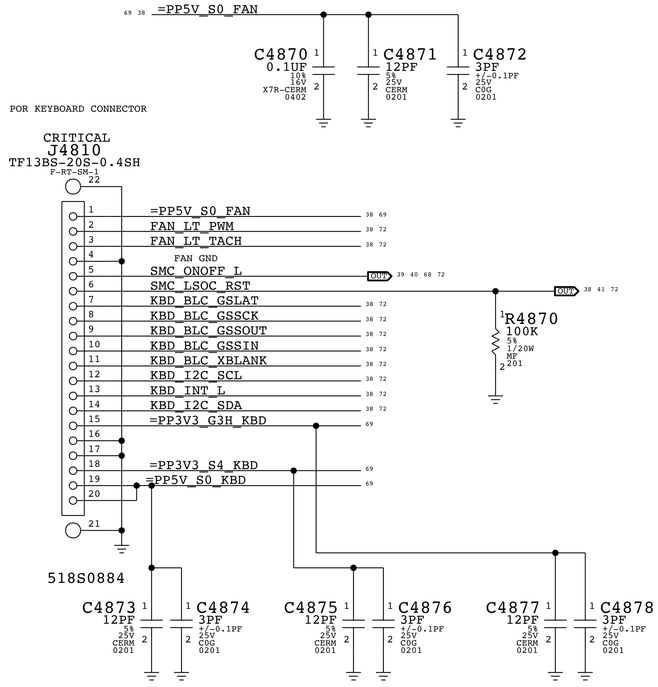
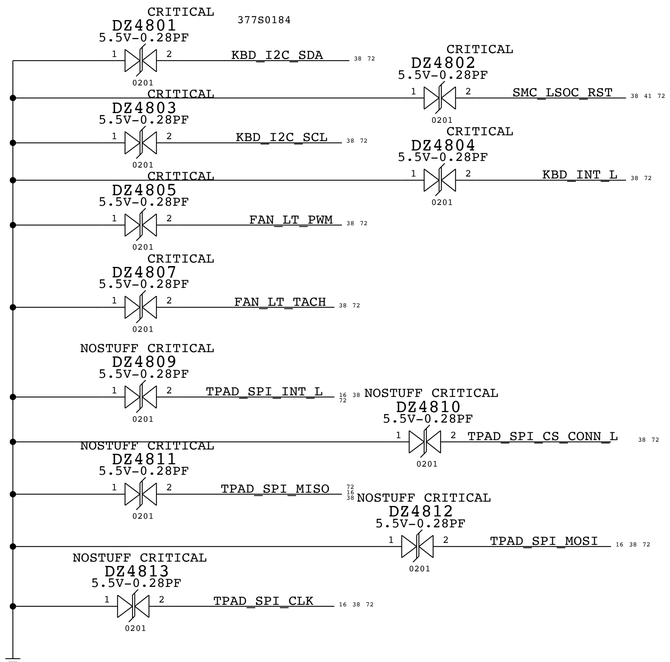
KEYBOARD CONNECTOR



ESD DIODES



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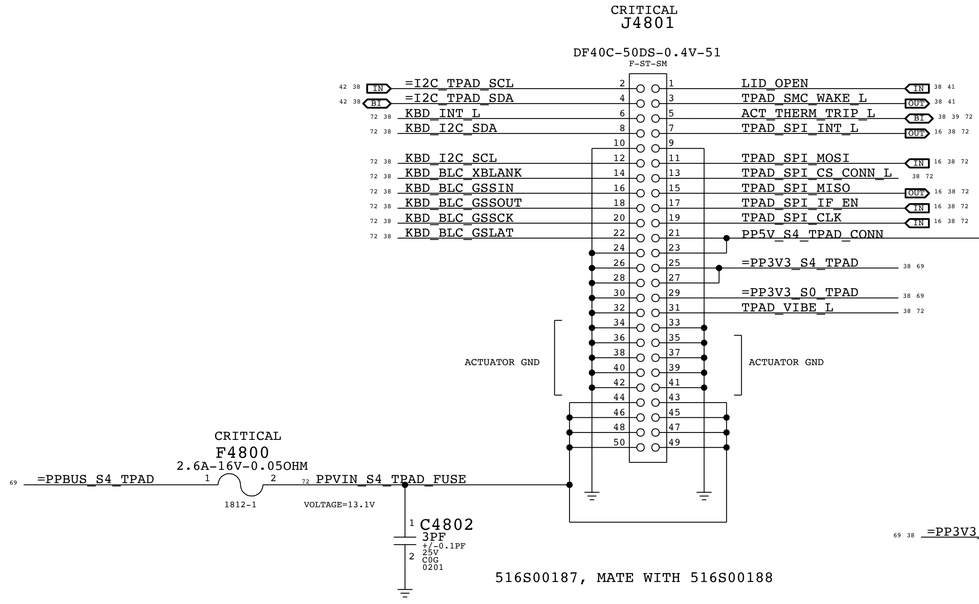


516S00187, MATE WITH 516S00188

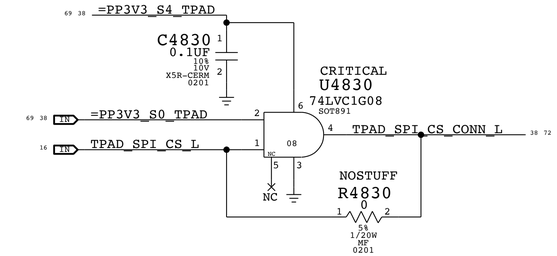
COWLING BOSES

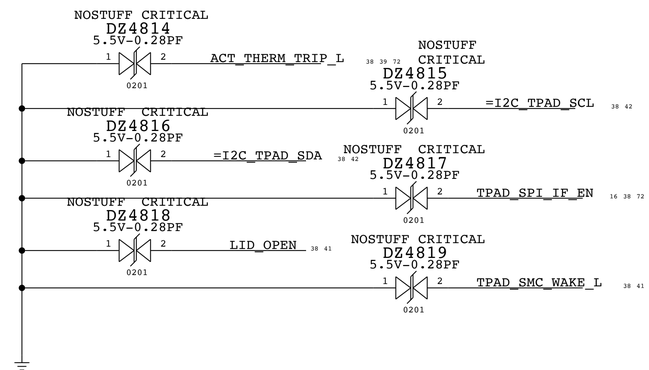
860-00381

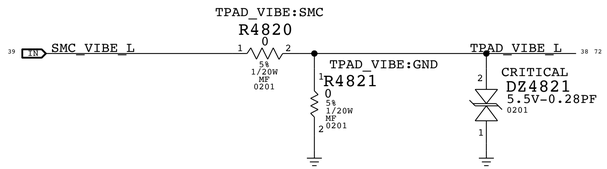
SH4801
3.5OD1.85ID-1.41H-SM

SH4802
3.5OD1.85ID-1.41H-SM

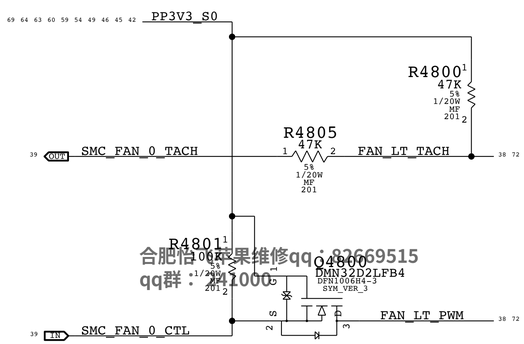
CS ISOLATION







FAN SUPPORT



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P1:KEYBOARD & TRACKPAD CONN

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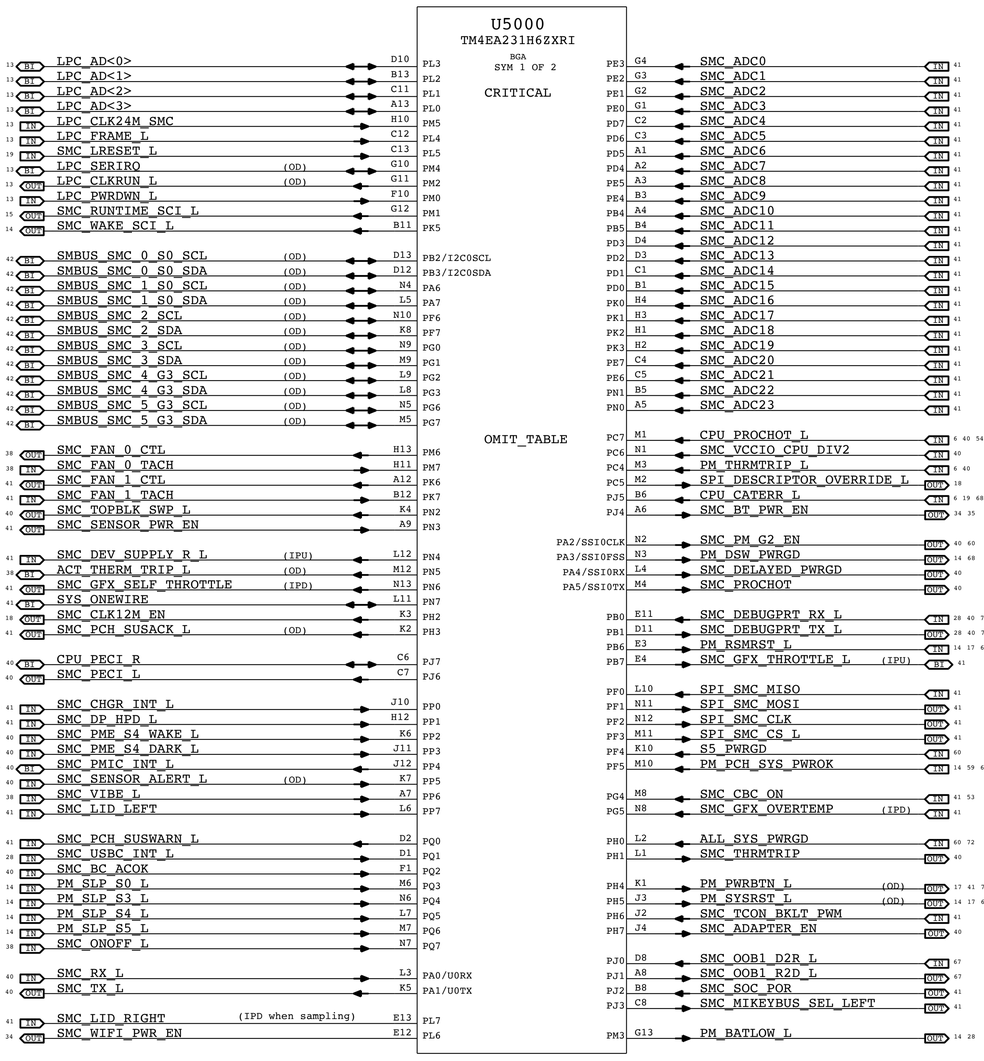

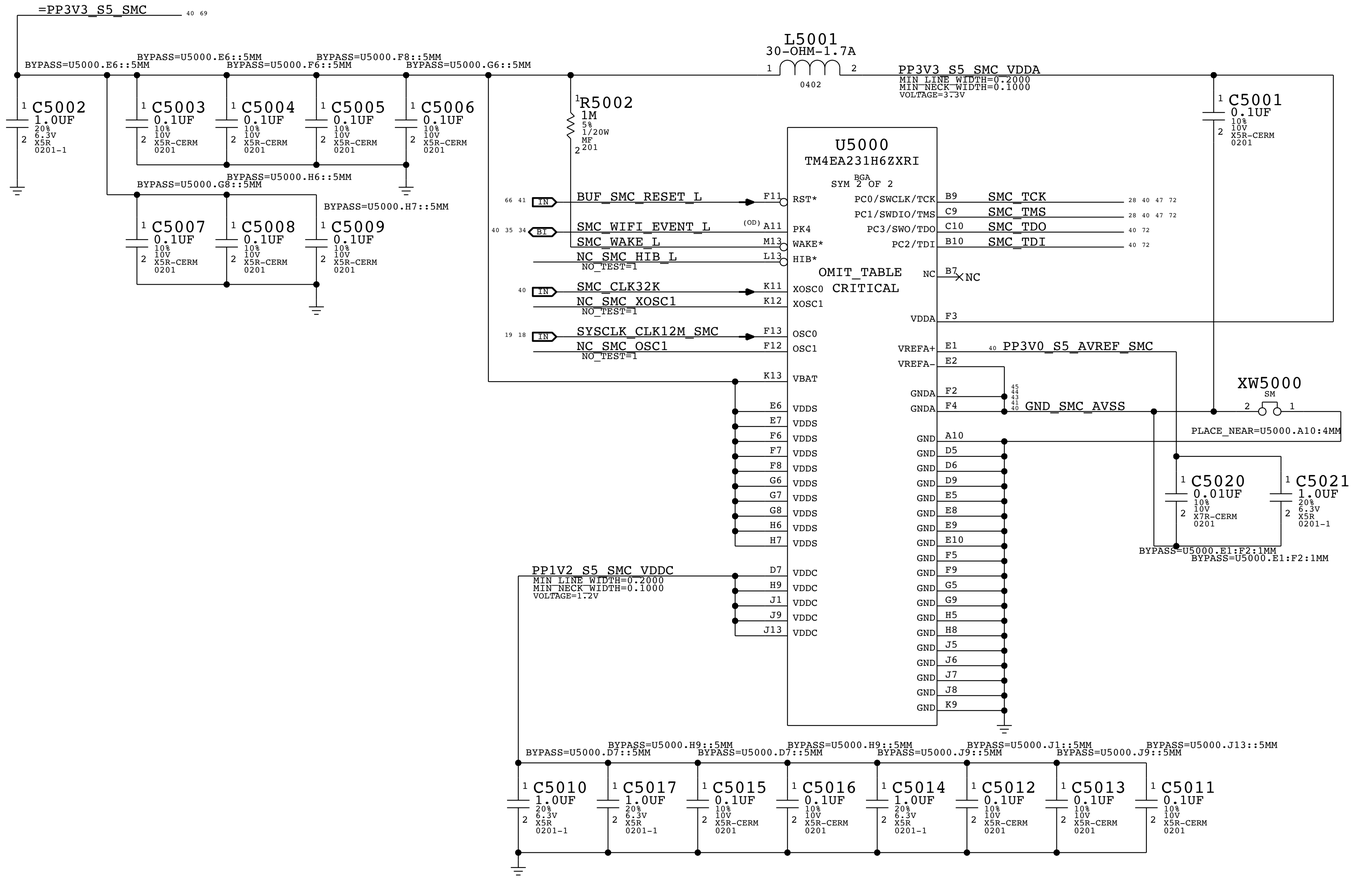

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

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SMC

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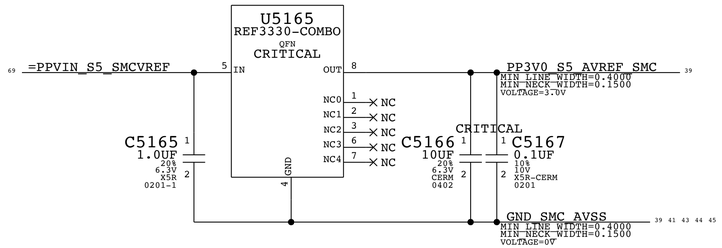
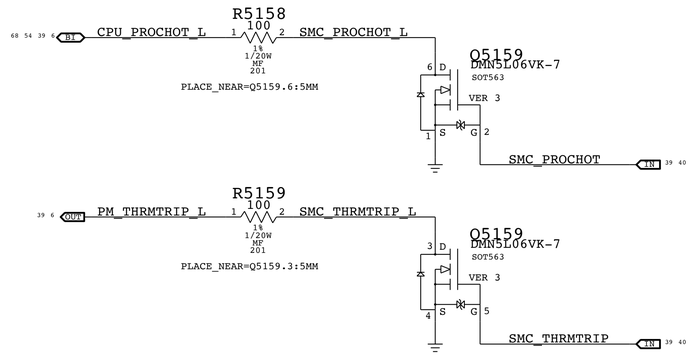
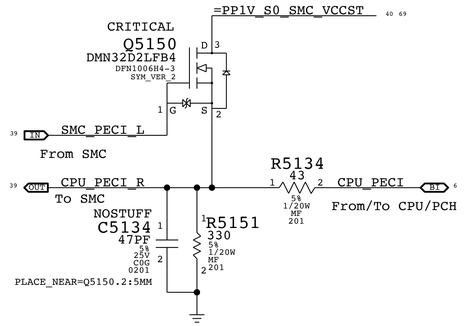
SMC AVREF Supply



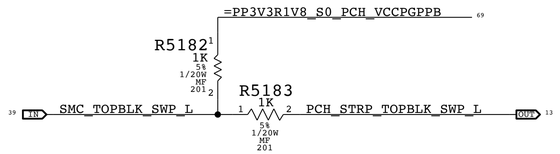
PROCHOT/THRMTRIP Support

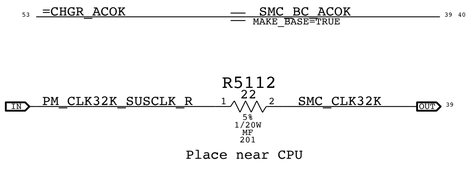


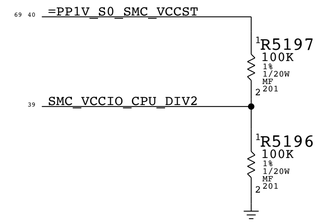
PECI Support

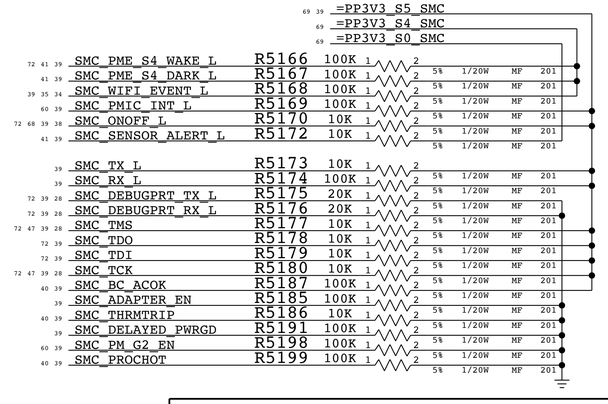


Top-Block Swap









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PAGE TITLE

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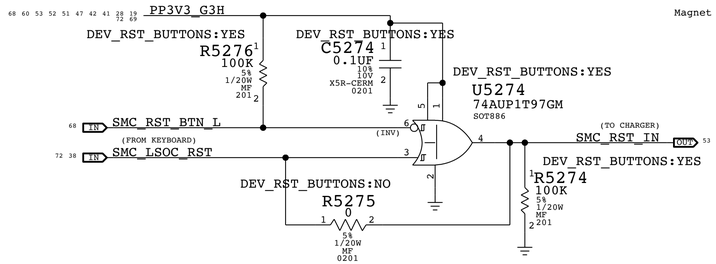
SMC ANALOG INPUTS

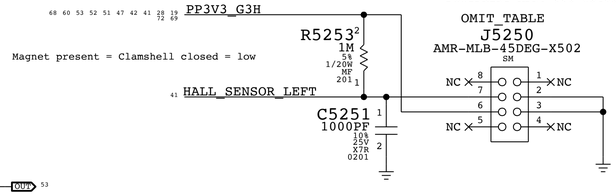
39	OUT	SMC_ADC0	MAKE_BASE=TRUE	SMC_DCIN_VSENSE	IN 43
39	OUT	SMC_ADC1	MAKE_BASE=TRUE	SMC_DCIN_ISENSE	IN 43
39	OUT	SMC_ADC2	MAKE_BASE=TRUE	SMC_PBUS_VSENSE	IN 43
39	OUT	SMC_ADC3	MAKE_BASE=TRUE	SMC_BMON_ISENSE	IN 43
39	OUT	SMC_ADC4	MAKE_BASE=TRUE	SMC_TPAD_ISENSE	IN 43
39	OUT	SMC_ADC5	MAKE_BASE=TRUE	SMC_CPU_HI_ISENSE	IN 43
39	OUT	SMC_ADC6	MAKE_BASE=TRUE	SMC_CPU_VSENSE	IN 45
39	OUT	SMC_ADC7	MAKE_BASE=TRUE	SMC_CPU_ISENSE	IN 45
39	OUT	SMC_ADC8	MAKE_BASE=TRUE	SMC_GT_VSENSE	IN 45
39	OUT	SMC_ADC9	MAKE_BASE=TRUE	SMC_GT_ISENSE	IN 45
39	OUT	SMC_ADC10	MAKE_BASE=TRUE	SMC_SA_ISENSE	IN 45
39	OUT	SMC_ADC11	MAKE_BASE=TRUE	SMC_1V5S_ISENSE	IN 44
39	OUT	SMC_ADC12	MAKE_BASE=TRUE	SMC_SSD_ISENSE	IN 43
39	OUT	SMC_ADC13	MAKE_BASE=TRUE	SMC_3V3SSD_ISENSE	IN 44
39	OUT	SMC_ADC14	MAKE_BASE=TRUE	SMC_1V2S3_ISENSE	IN 44
39	OUT	SMC_ADC15	MAKE_BASE=TRUE	SMC_CPU_IMON_ISENSE	IN 45
39	OUT	SMC_ADC16	MAKE_BASE=TRUE	SMC_GT_IMON_ISENSE	IN 45
39	OUT	SMC_ADC17	MAKE_BASE=TRUE	SMC_3V3LCD_ISENSE	IN 44
39	OUT	SMC_ADC18	MAKE_BASE=TRUE	SMC_3V3WLS_ISENSE	IN 44
39	OUT	SMC_ADC19	MAKE_BASE=TRUE	SMC_LCDBKLT_ISENSE	IN 43
39	OUT	SMC_ADC20	MAKE_BASE=TRUE	SMC_SA_IMON_ISENSE	IN 45
39	OUT	SMC_ADC21	MAKE_BASE=TRUE	SMC_5VS4_ISENSE	IN 44
39	OUT	SMC_ADC22	MAKE_BASE=TRUE	SMC_3V3S5_ISENSE	IN 44
39	OUT	SMC_ADC23	MAKE_BASE=TRUE	SMC_TBT_ISENSE	IN 45

39	IN	SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_THROTTLE_L
39	IN	SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_OVERTEMP
39	IN	SMC_FAN_1_CTL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_CTL
39	IN	SMC_FAN_1_TACH	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_TACH
39	IN	SMC_SOC_POR	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_SOC_POR
39	IN	SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_SELF_THROTTLE
39	IN	SPI_SMC_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CLK
39	IN	SPI_SMC_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CS_L
39	IN	SPI_SMC_MISO	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MISO
39	IN	SPI_SMC_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MOSI
39	IN	SMC_MIKEYBUS_SEL_LEFT	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_MIKEYBUS_SEL_LEFT
39	IN	SYS_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1	NC_SYS_ONEWIRE



AMR SENSOR PADS

FOOTPRINT APN: 998-05495



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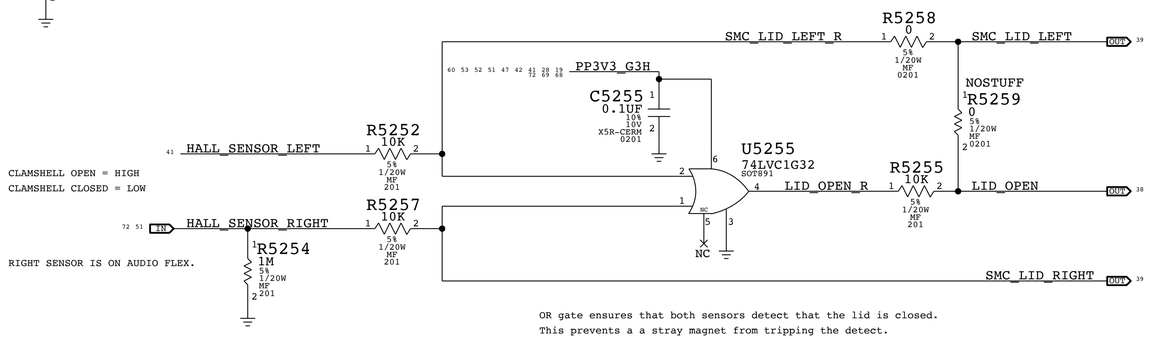
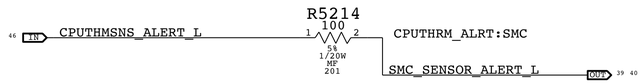
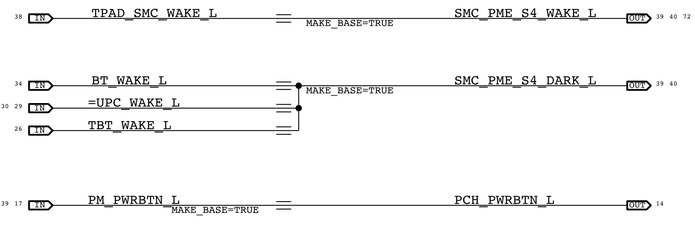


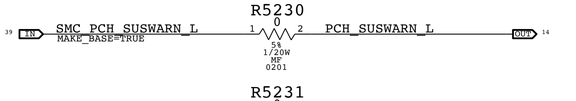
OR gate ensures that both sensors detect that the lid is closed.
This prevents a a stray magnet from tripping the detect.

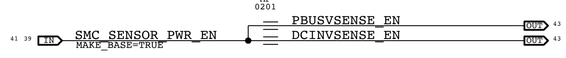
Thermal Alerts

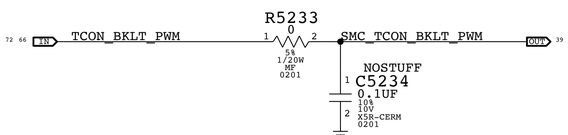


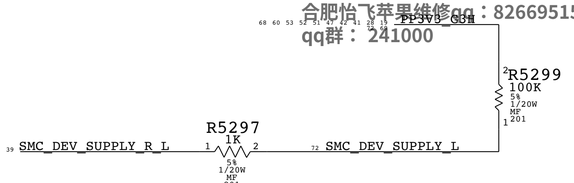
S4 SMC Wake Sources

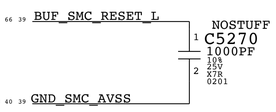


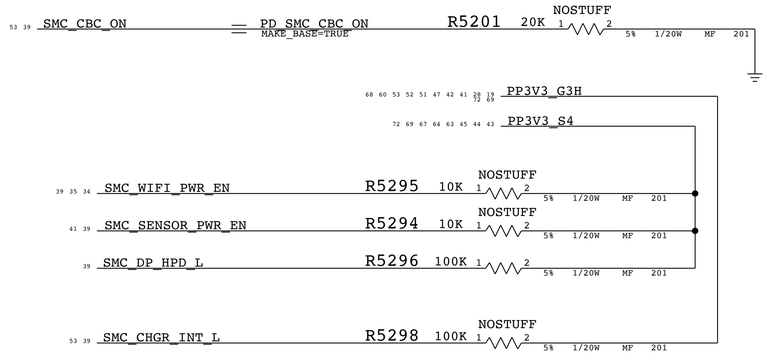












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DESIGN: X502/MLB CATZ
SYNC MASTER=PAULM

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SMC Project Support

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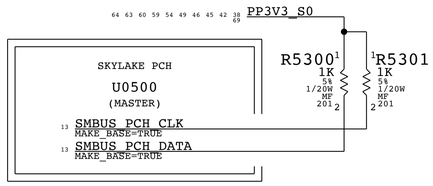
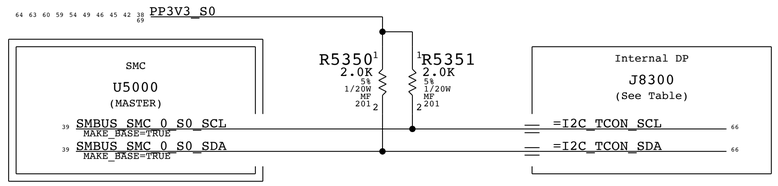
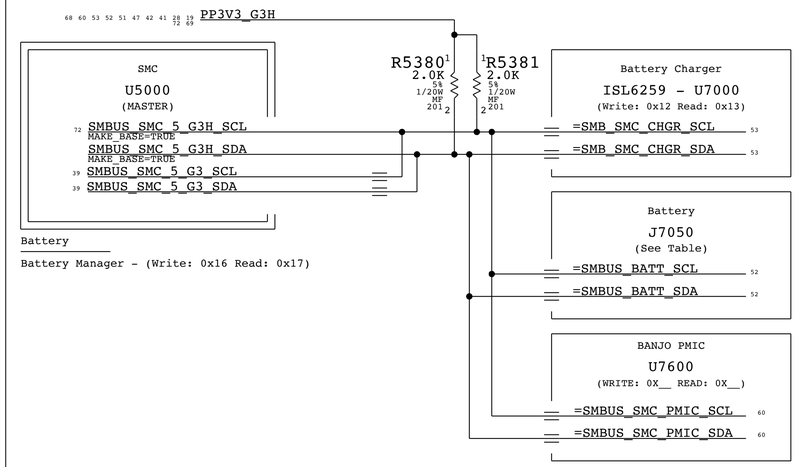
SKYLAKE PCH S0 "SMBUS 0" CONNECTIONS



SMC SMBus "0" S0 Connections



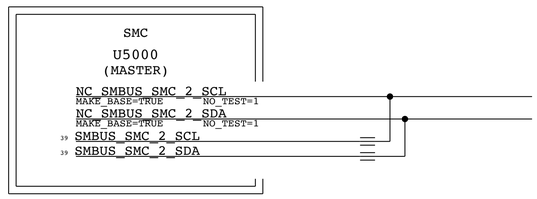
SMC SMBus "5" G3H Connections



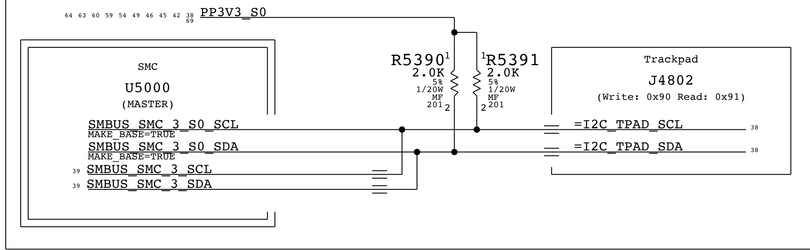
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

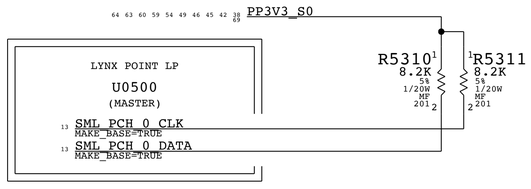
SMC SMBus "2" S3 Connections



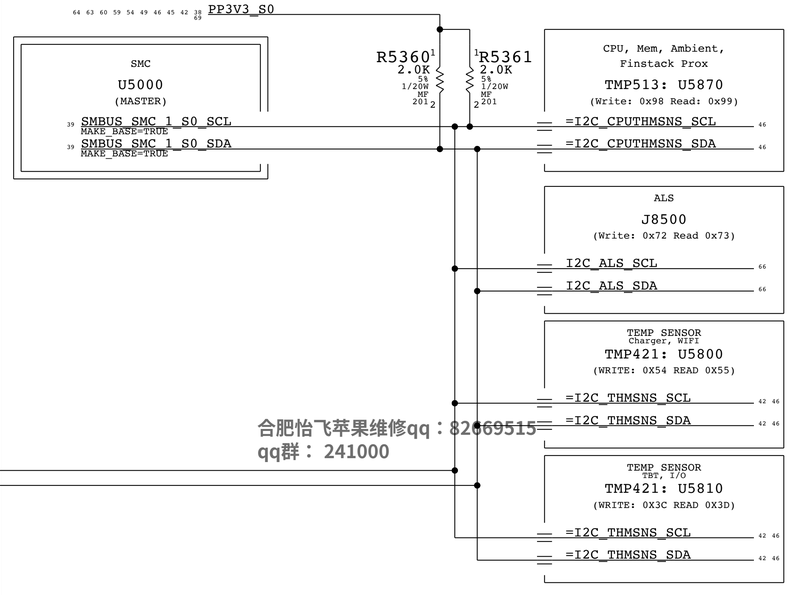
SMC SMBus "3" S0 Connections



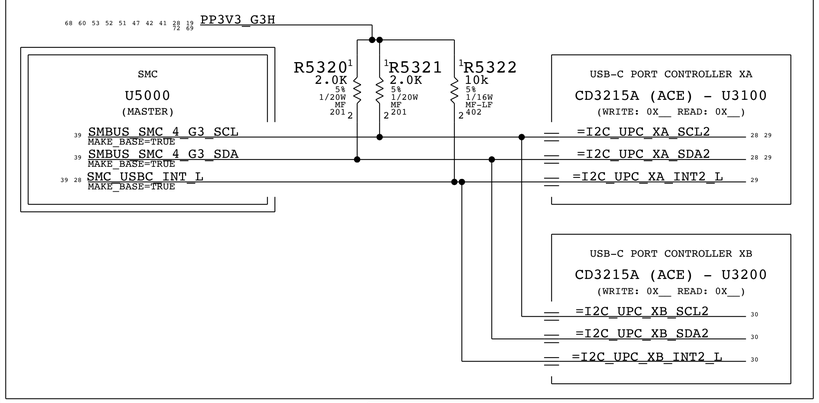
LYNX POINT LP S0 "SMLink 0" Connections



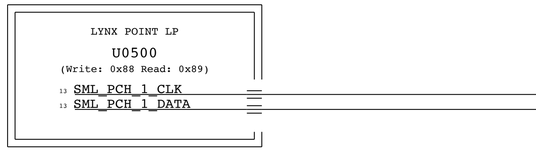
SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH.

BOM_COST_GROUP=SMC

DESIGN: X502/MLB CATZ

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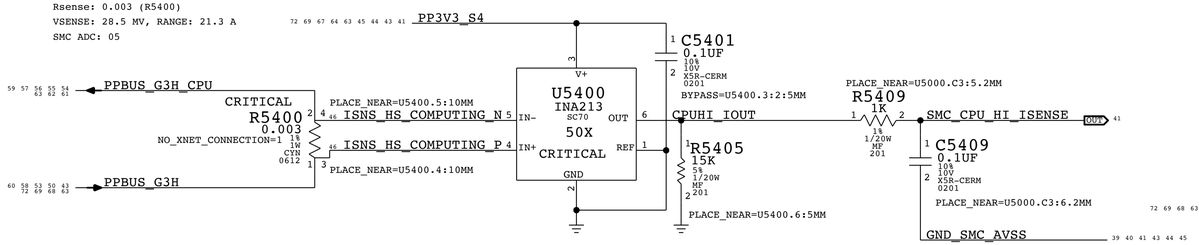
INA21X PARTS HAVE MINOR LEAKAGE PATH FROM INPUTS TO OUTPUT WHEN UNPOWERED.
PULL-DOWN RESISTERS ON INA OUTPUTS BLEED OFF THE LEAKAGE CURRENT TO PREVENT
SIGNAL PUMP-UP.

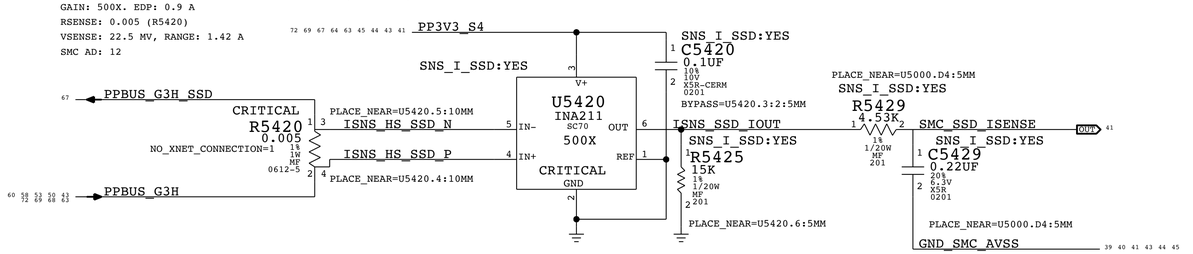
CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A
Rsense: 0.003 (R5400)
VSENSE: 28.5 MV, RANGE: 21.3 A
SMC ADC: 05



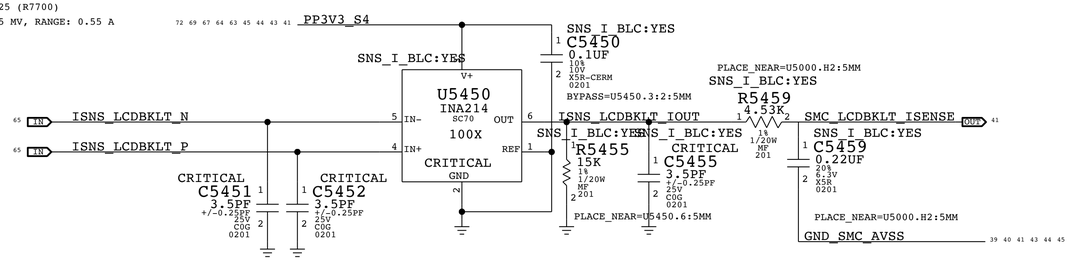
SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R5420)
VSENSE: 22.5 MV, RANGE: 1.42 A
SMC AD: 12



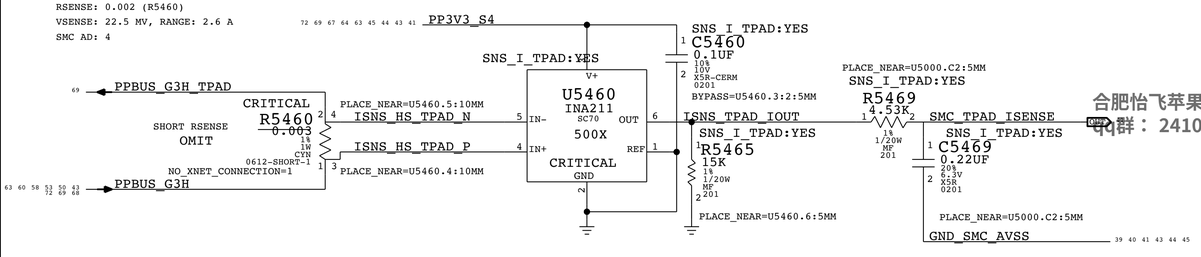
LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X. EDP: 0.9 A
Rsense: 0.025 (R7700)
VSENSE: 22.5 MV, RANGE: 0.55 A
SMC AD: 19



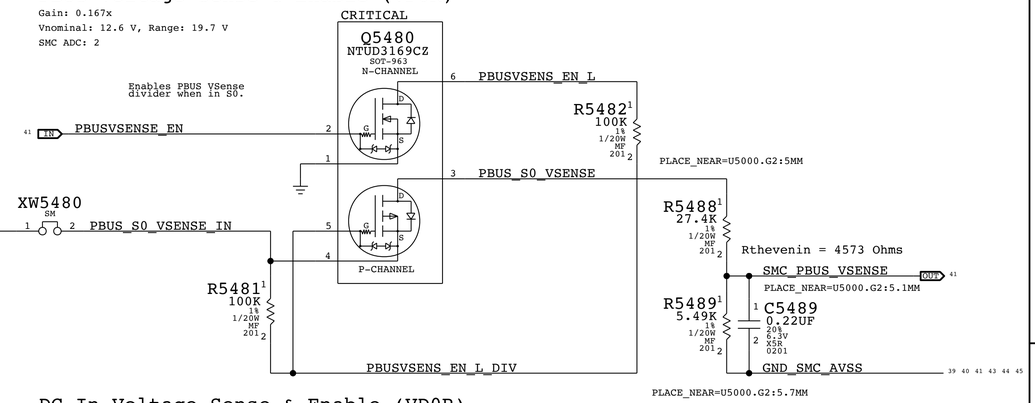
TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R5460)
VSENSE: 22.5 MV, RANGE: 2.6 A
SMC AD: 4



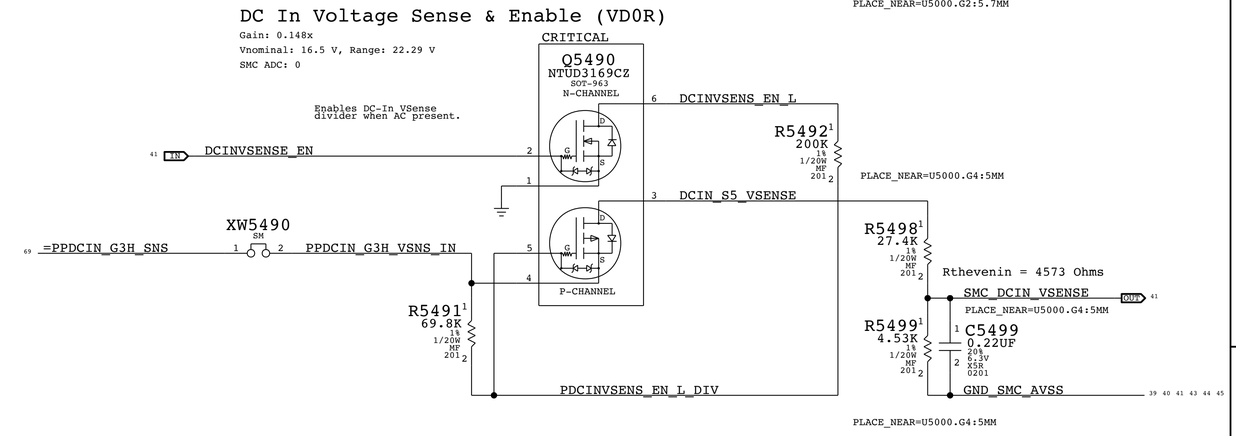
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 2



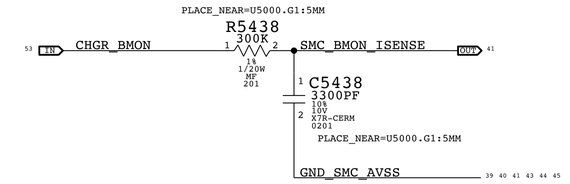
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 0



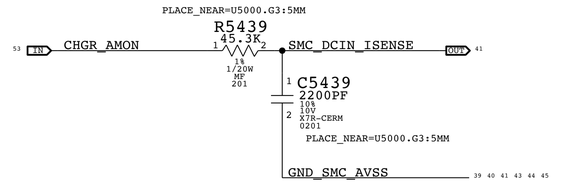
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
RSENSE: 0.005 (R7160)
SMC ADC: 03



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
RSENSE: 0.010 (R7120)
SMC ADC: 01



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5429		SNS_I_SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

BOM_COST_GROUP=SENSORS

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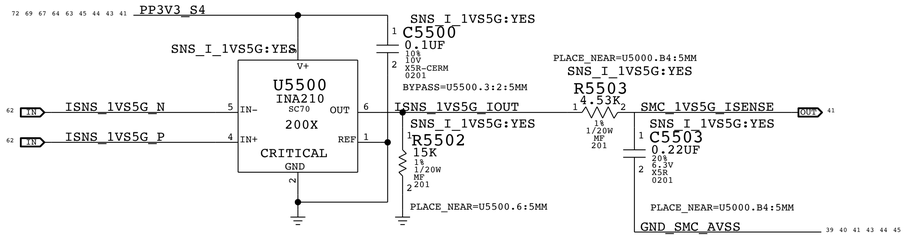
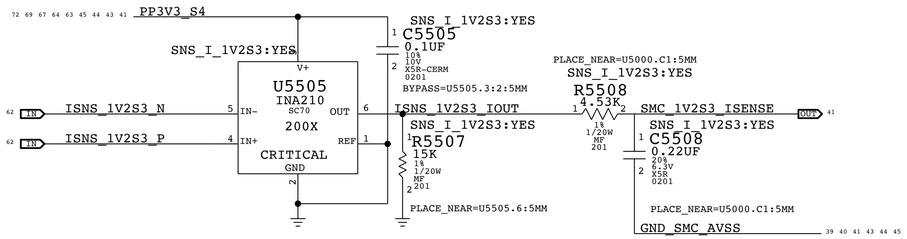
1V_S5G CURRENT SENSE (ISIC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7700)
VSENSE: 22.5 MV, RANGE: 3.0 A
SMC AD: 11



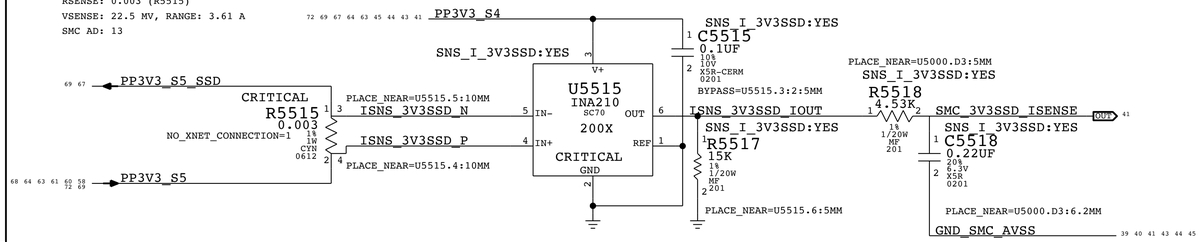
1V2_S3 CURRENT SENSE (IM0C)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 14



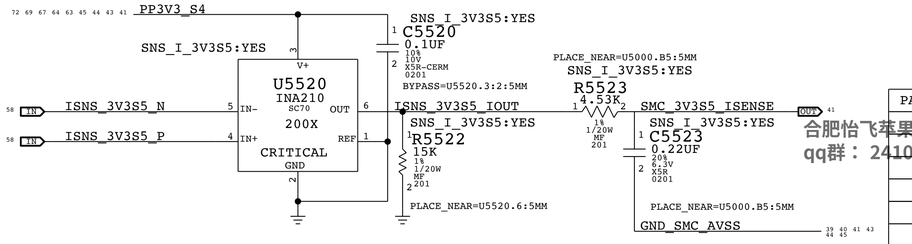
3V3_SSD CURRENT SENSE (IHCC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R5515)
VSENSE: 22.5 MV, RANGE: 3.61 A
SMC AD: 13



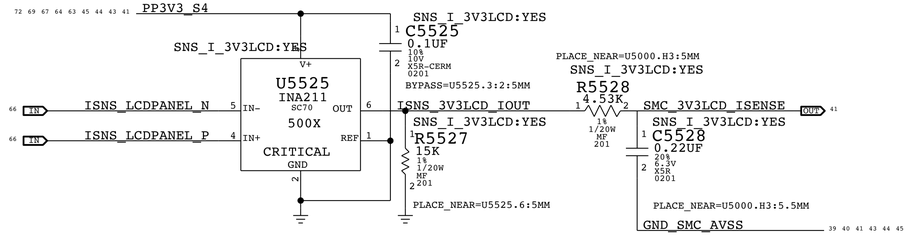
3V3_S5 CURRENT SENSE (IO3R) (HIGH-SIDE)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7710)
VSENSE: 22.5 MV ?, RANGE: 4 A
SMC AD: 22



3V3_S0 LCD CURRENT SENSE (ILDC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R5525)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

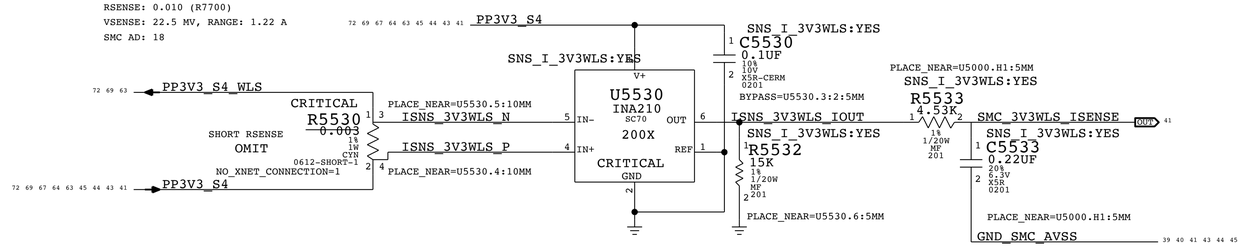


5V_S0 LCD CURRENT SENSE (I___)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R8520)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

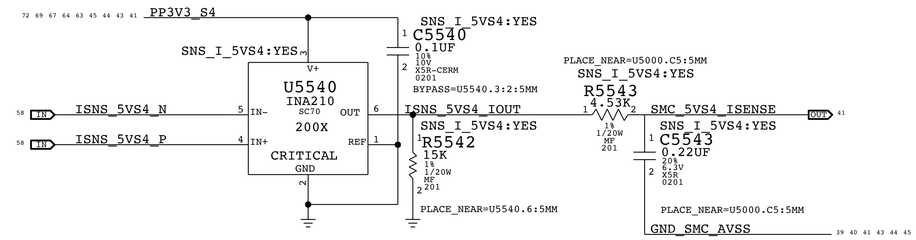
3V3_S4 WIRELESS CURRENT SENSE (IAPC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.010 (R7700)
VSENSE: 22.5 MV, RANGE: 1.22 A
SMC AD: 18



5V_S4 CURRENT SENSE (IO5R) (HIGH-SIDE)

GAIN: 200X. EDP: ?? A
RSENSE: 0.003 (R7900)
VSENSE: 22.5 MV ?, RANGE: 6.8 A
SMC AD: 21



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5508		SNS_I_1V2S3:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5518		SNS_I_3V3SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5523		SNS_I_3V3S5:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5528		SNS_I_3V3LCD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5533		SNS_I_3V3WLS:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5543		SNS_I_5VS4:NO

BOM_COST_GROUP=SENSORS

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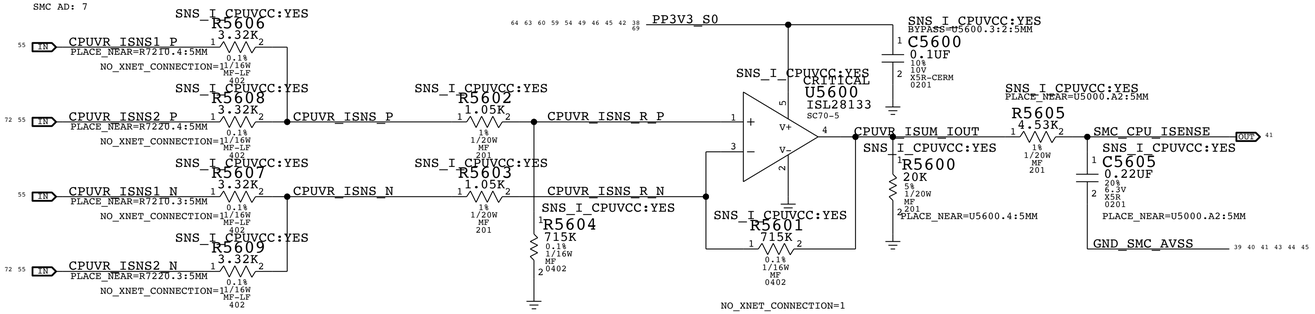
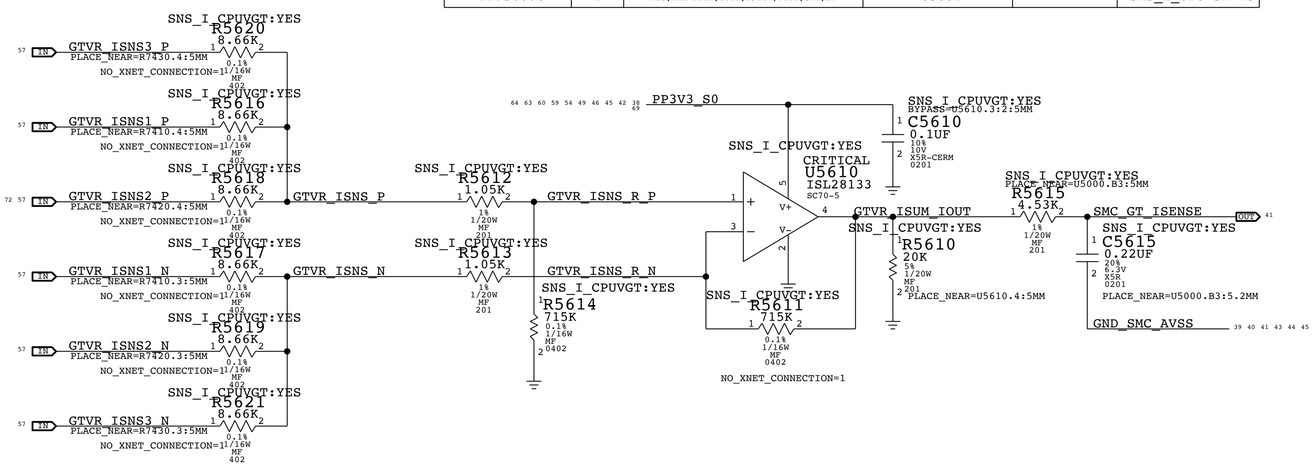
CPU VCC CURRENT SENSE (ICAC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 7



CPU GT CURRENT SENSE (ICGC)

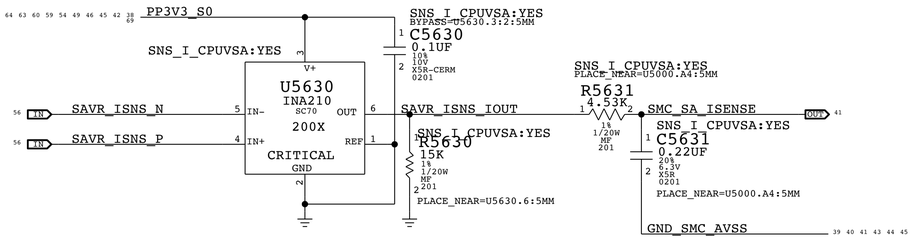
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 9



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO

CPU SA CURRENT SENSE (ICSC)

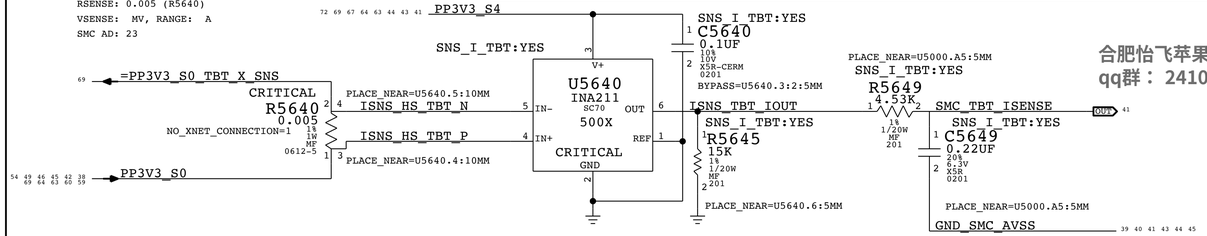
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 10



TBT CURRENT SENSE (IULC)

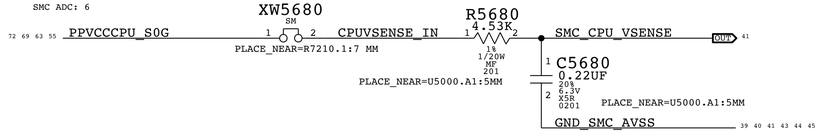
GAIN: 500X. EDP: A
RSENSE: 0.005 (R5640)
VSENSE: MV, RANGE: A
SMC AD: 23

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO



CPU CORE VOLTAGE SENSE (VCAC)

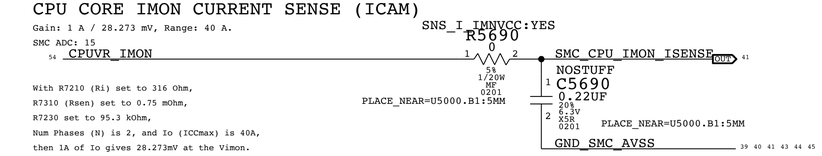
SMC ADC: 6



CPU CORE IMON CURRENT SENSE (ICAM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 15

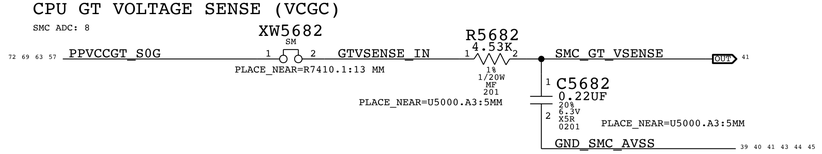
With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5690		SNS_I_IMNVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5692		SNS_I_IMNVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5691		SNS_I_IMNVSA:NO

CPU GT VOLTAGE SENSE (VCGC)

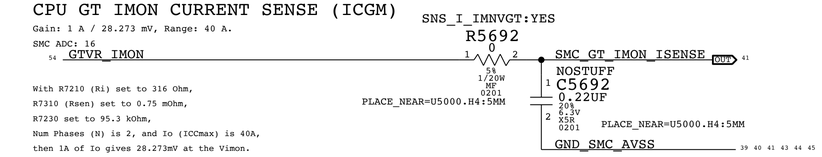
SMC ADC: 8



CPU GT IMON CURRENT SENSE (ICGM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 16

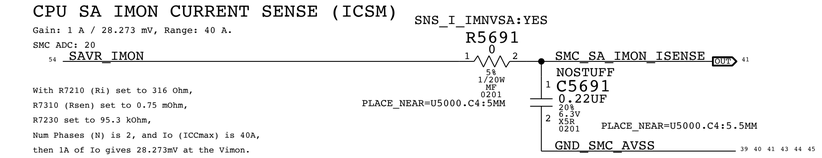
With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.



CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 20

With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.



BOM_COST_GROUP=SENSORS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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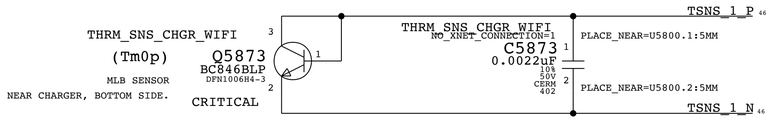
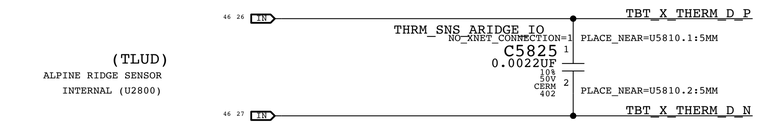
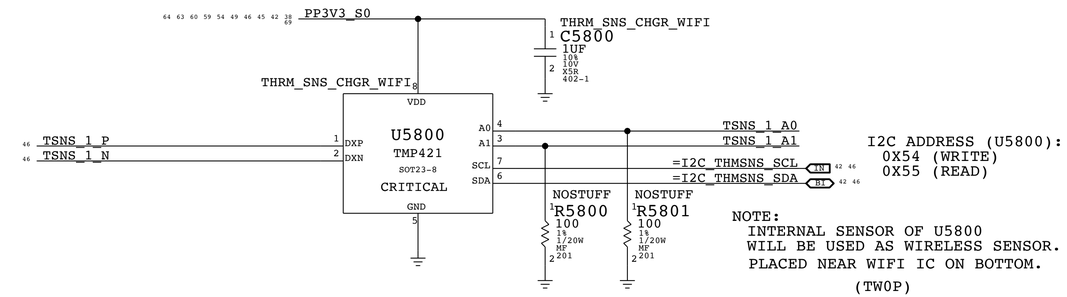
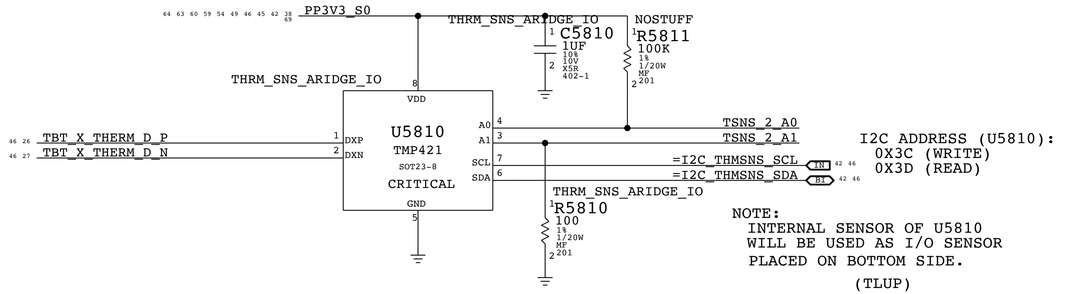


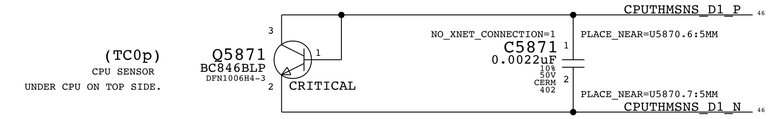


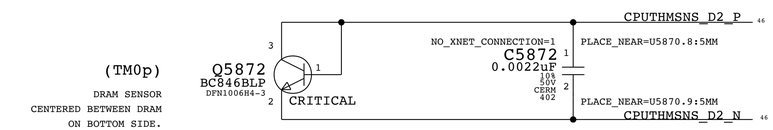


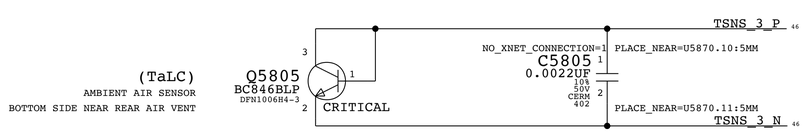


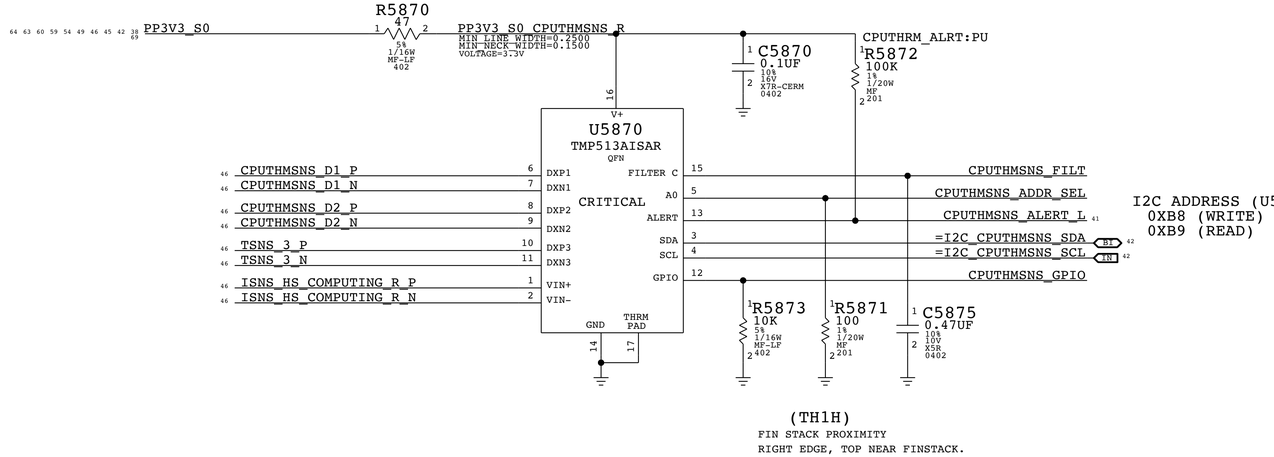
Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0x98, I2C Read: 0x99









BOM_COST_GROUP=SENSORS

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
Thermal Sensors

Apple Inc.

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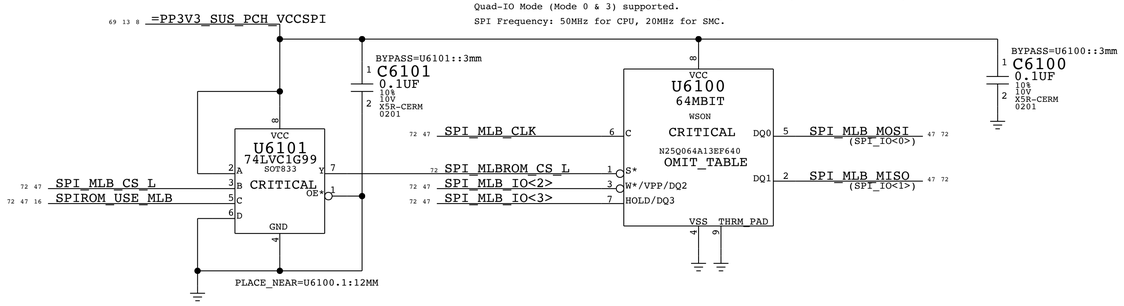
SPI ROM - Combo BGA Footprint (3 vendors)

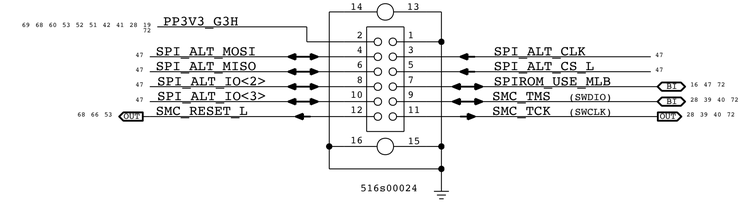
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



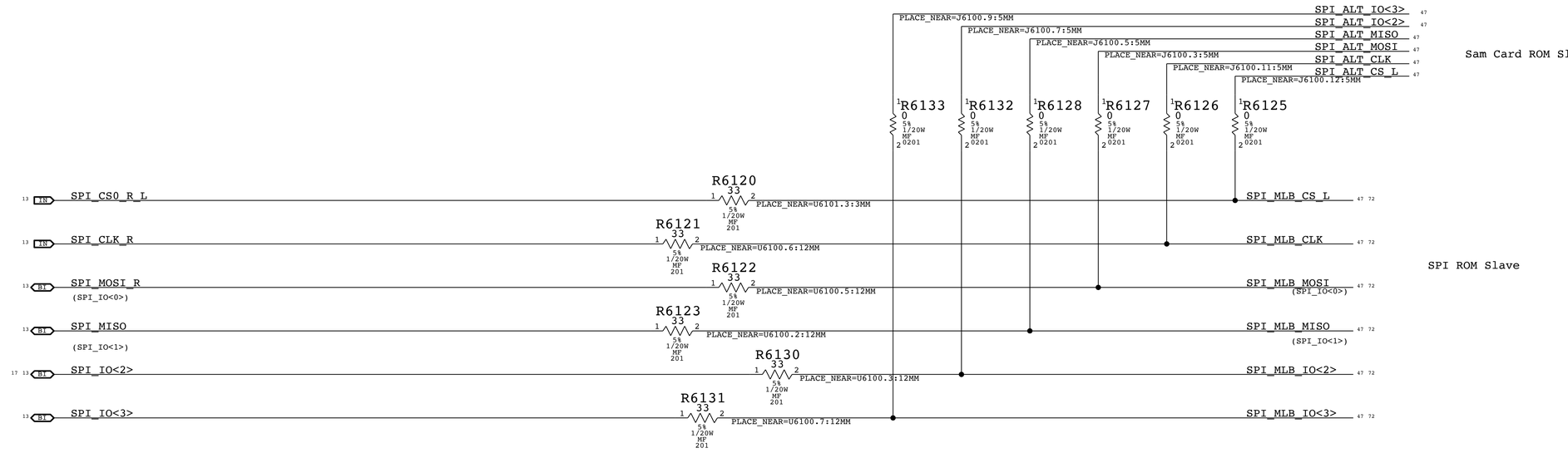
SPI+SWD SAM Connector

CRITICAL

J6100
DF40PC-12DP-0.4V-51
M-ST-SM



BootROM SPI Bus Series Termination



BOM_COST_GROUP=CPU SUPPORT

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
SPI ROM & SWD Debug

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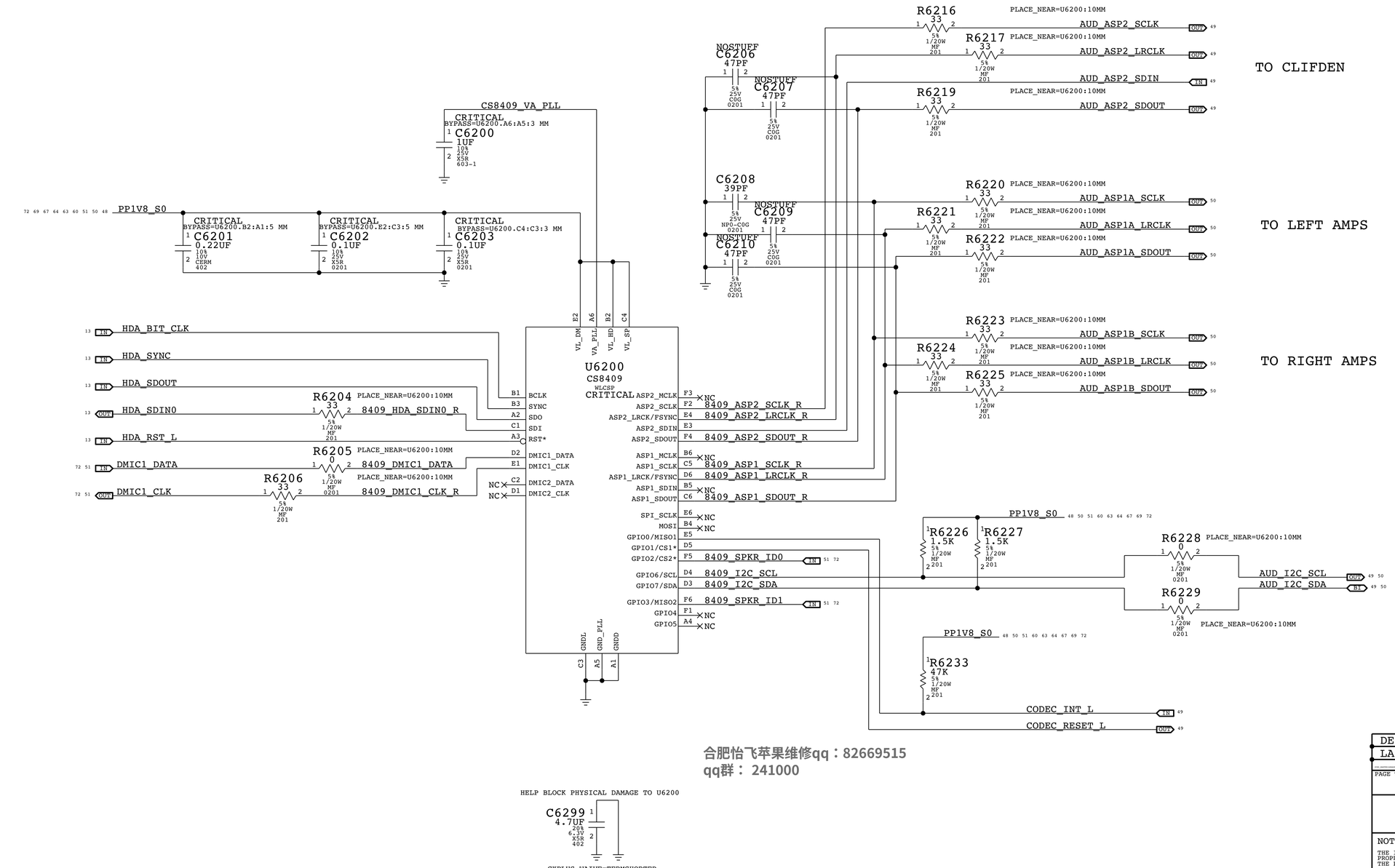

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
HDA BRIDGE

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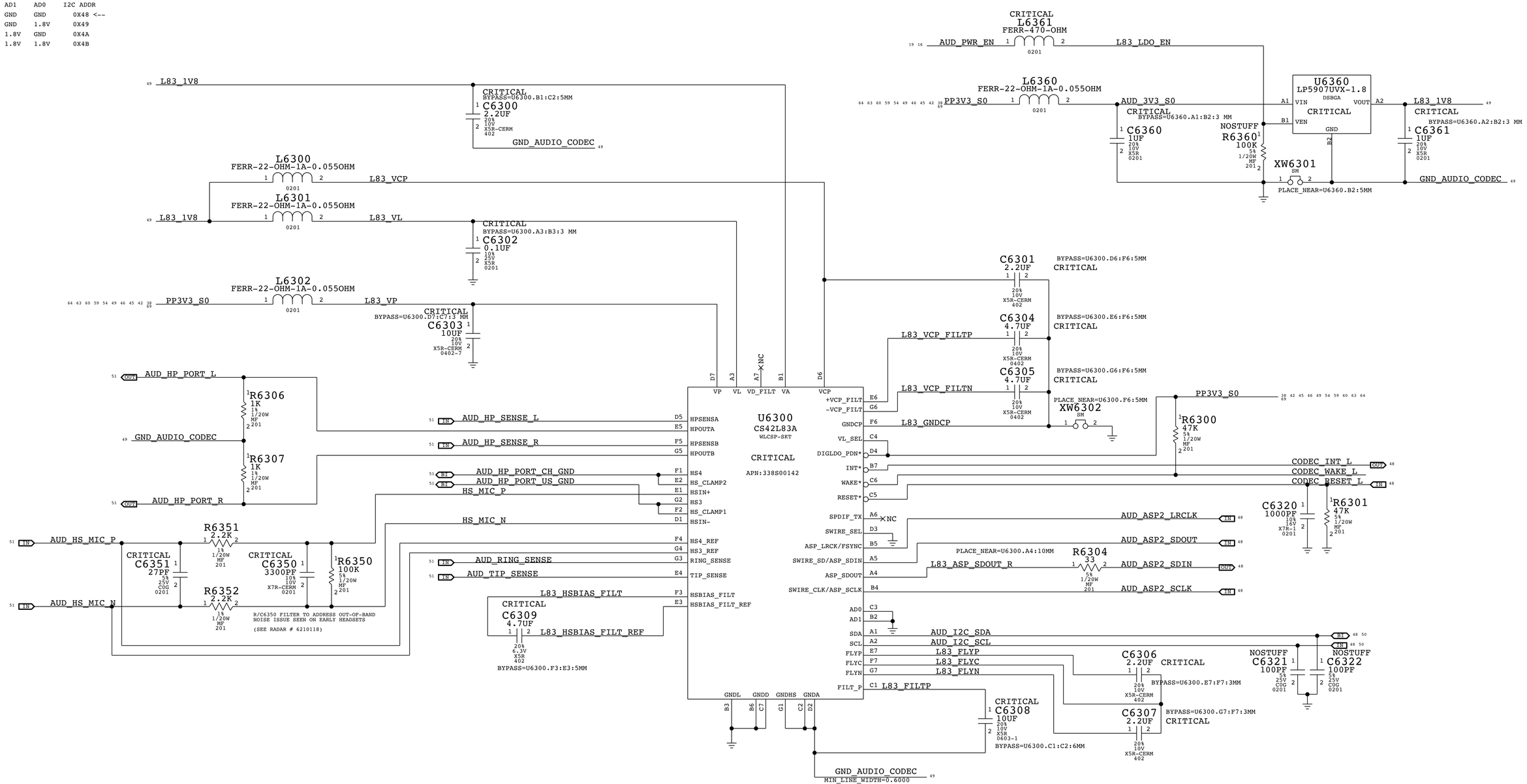
AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B



合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB CATZ	
LAST CHANGE: Mon Aug 8 12:54:34 2016	
PAGE TITLE: JACK CODEC	
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	REVISION: 1.0.0
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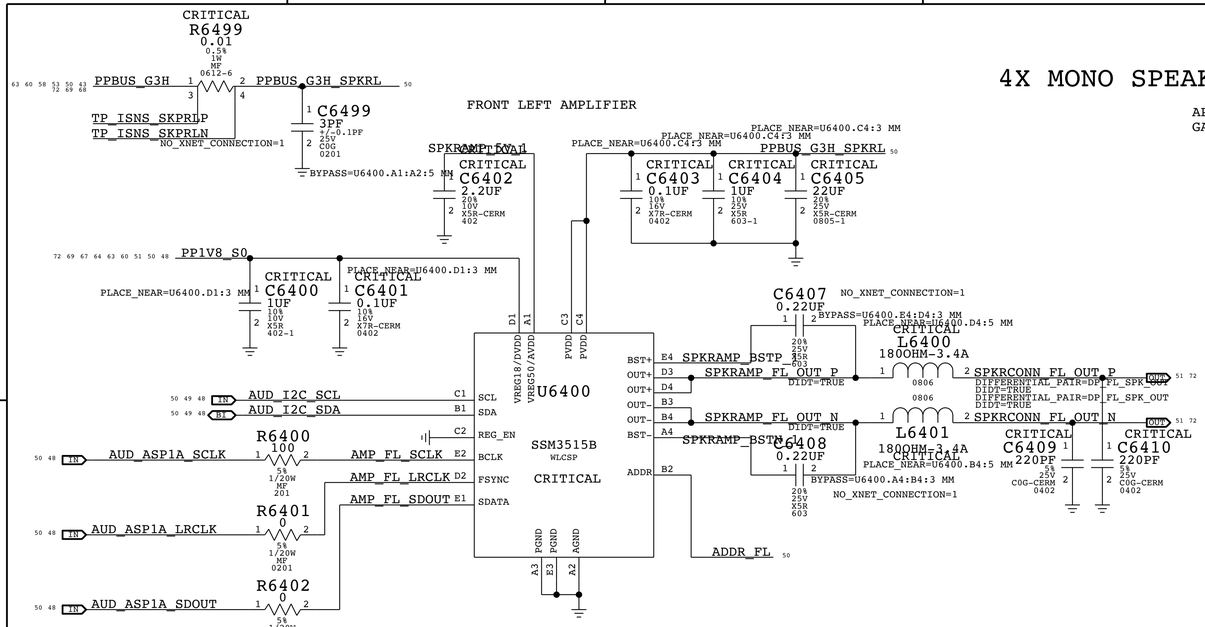
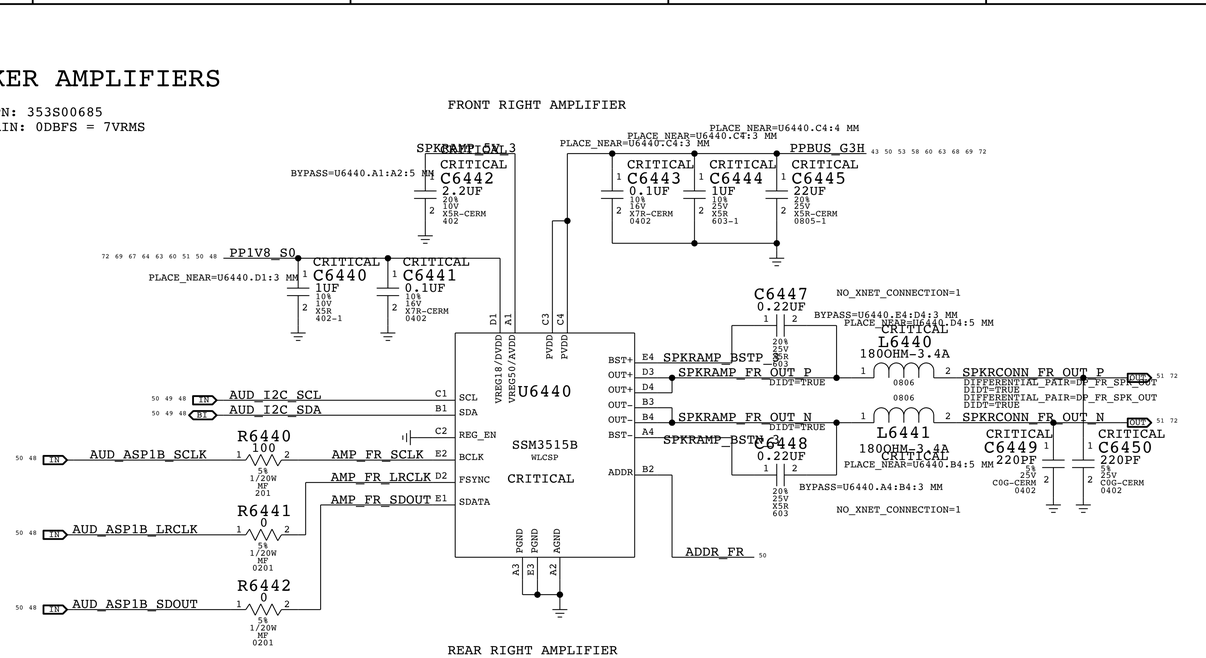
4X MONO SPEAKER AMPLIFIERS

APN: 353S00685
GAIN: 0DBFS = 7VRMS

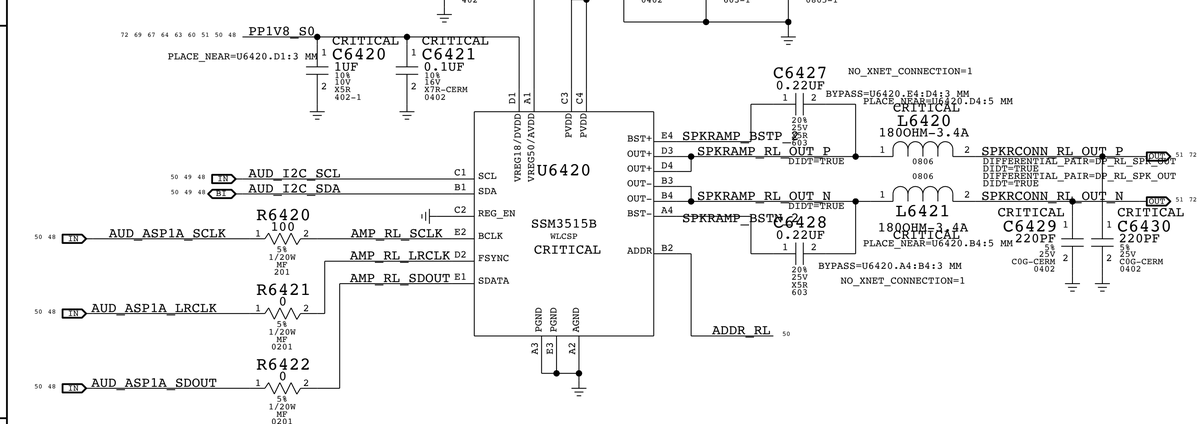
FRONT LEFT AMPLIFIER



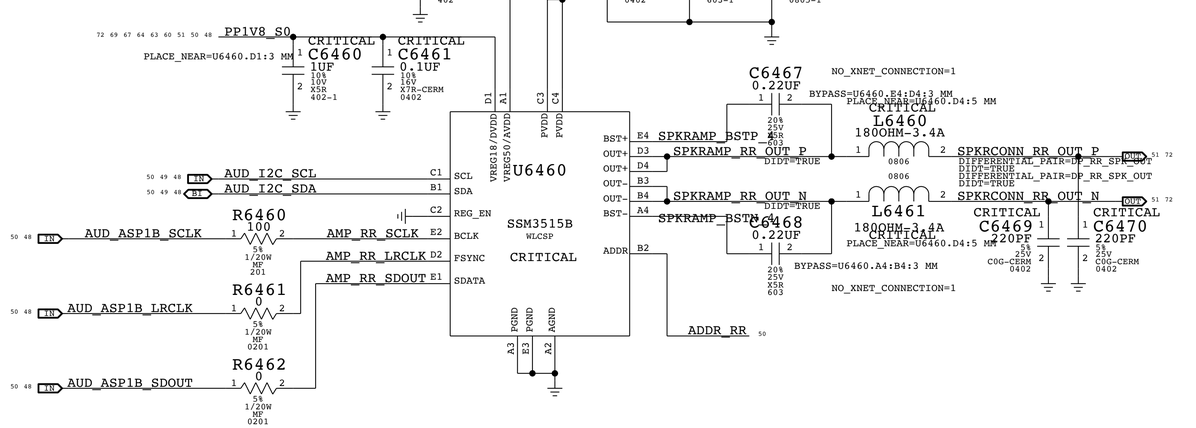
FRONT RIGHT AMPLIFIER



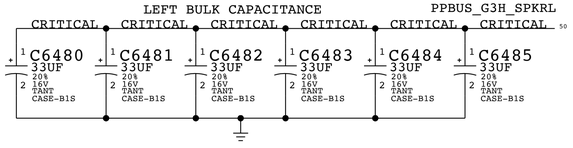
REAR LEFT AMPLIFIER



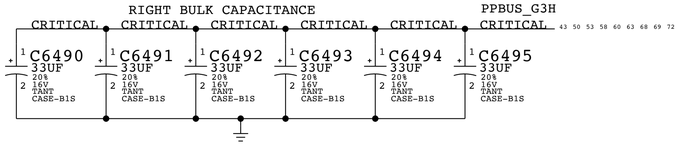
REAR RIGHT AMPLIFIER

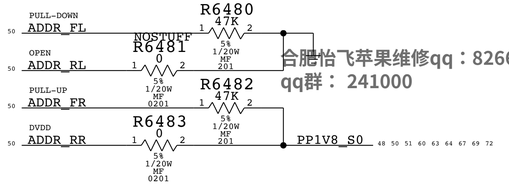


LEFT BULK CAPACITANCE



RIGHT BULK CAPACITANCE





	TDM SLOT	I2C ADDR
FRONT LEFT	1	0X28
REAR LEFT	2	0X2A
FRONT RIGHT	3	0X2C
REAR RIGHT	4	0X2E

BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB CATZ
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PAGE TITLE
SPEAKER AMP

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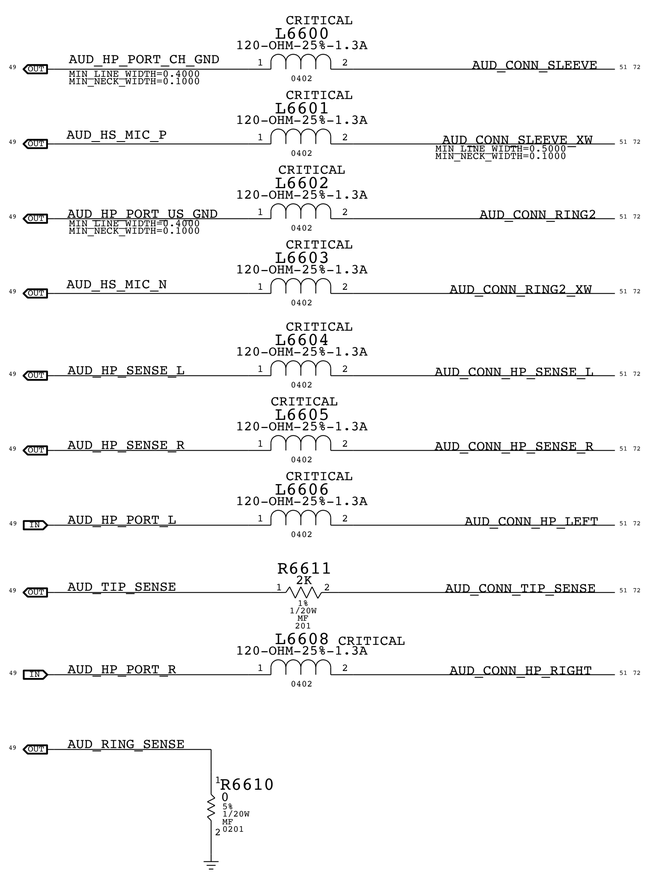
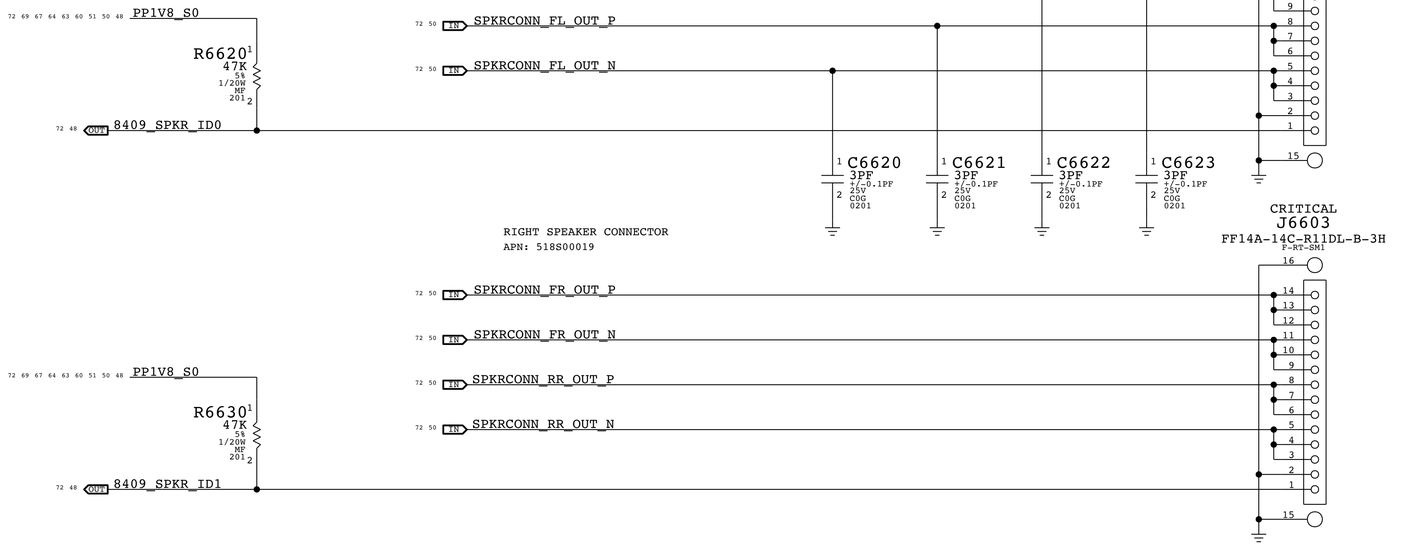
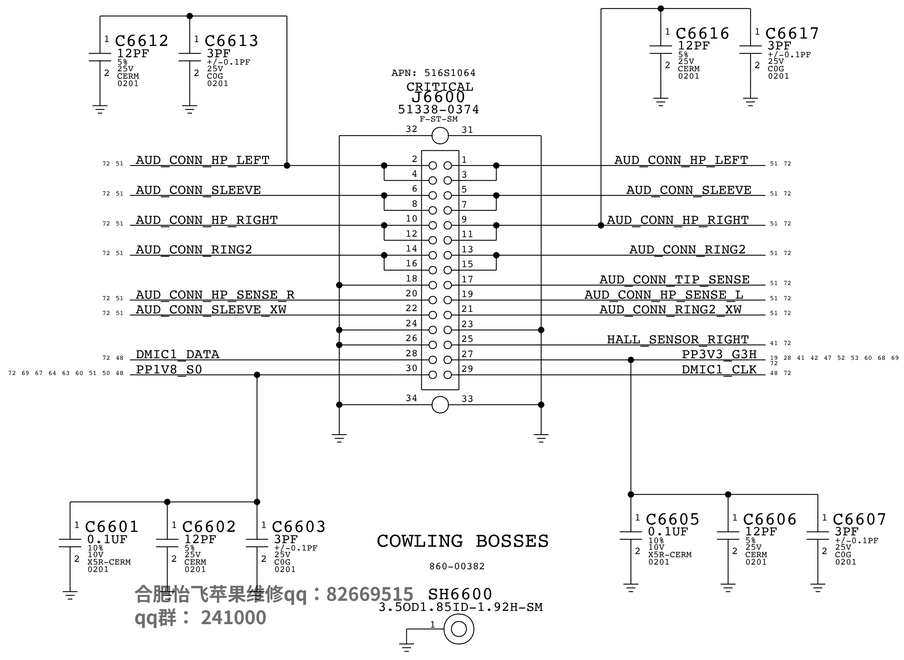




AUDIO FLEX CONNECTOR



COWLING BOSSES

860-00382

SH6600

3.5OD1.85ID-1.92H-SM

BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB CATZ

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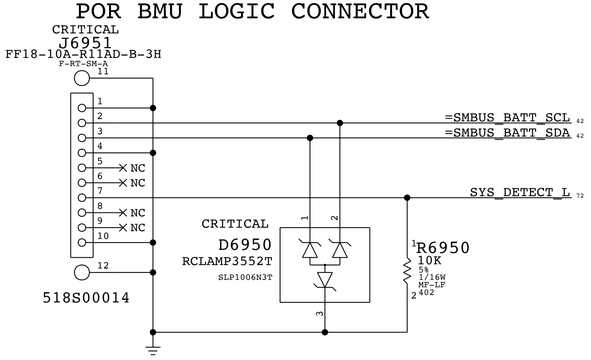
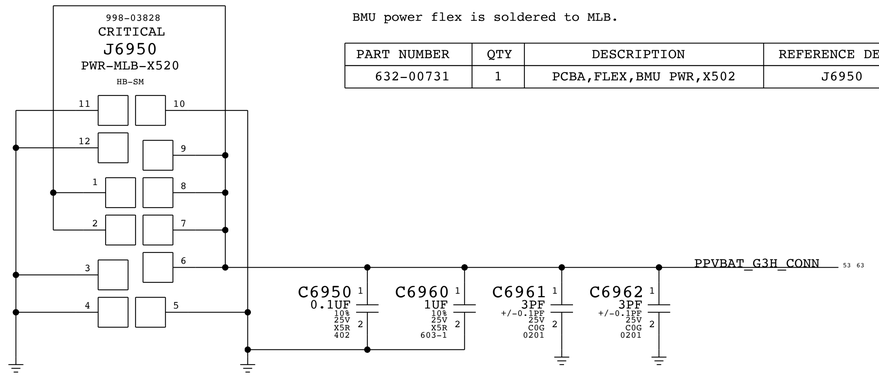
POR BMU LOGIC CONNECTOR



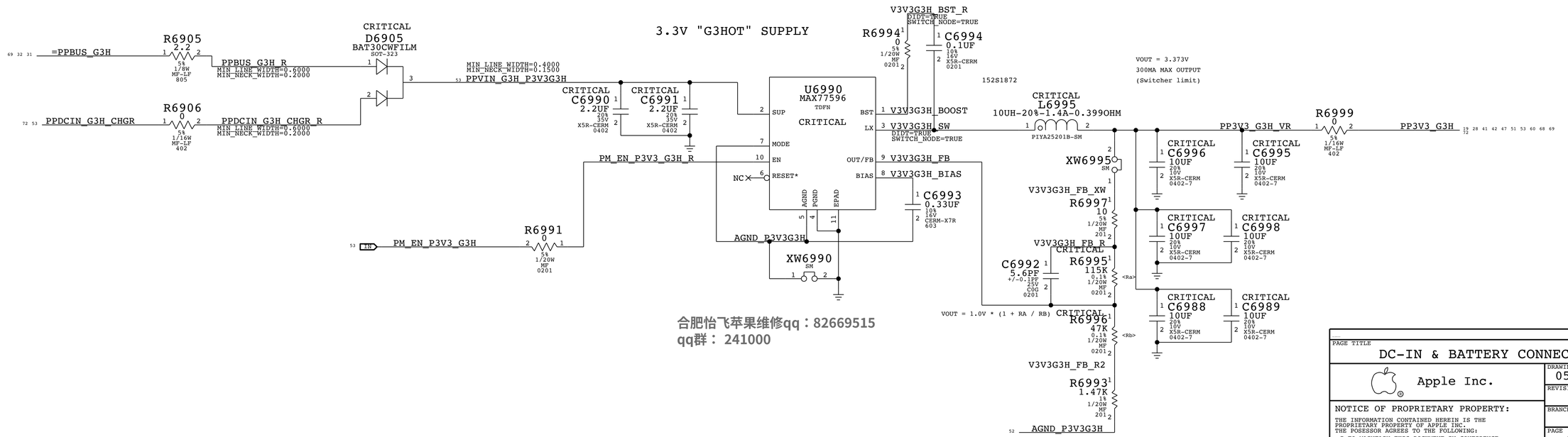
POR BATTERY (BMU) FLEX SOLDER PADS.



BMU power flex is soldered to MLB.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	

3.3V "G3HOT" SUPPLY



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PAGE TITLE
DC-IN & BATTERY CONNECTORS

Apple Inc.

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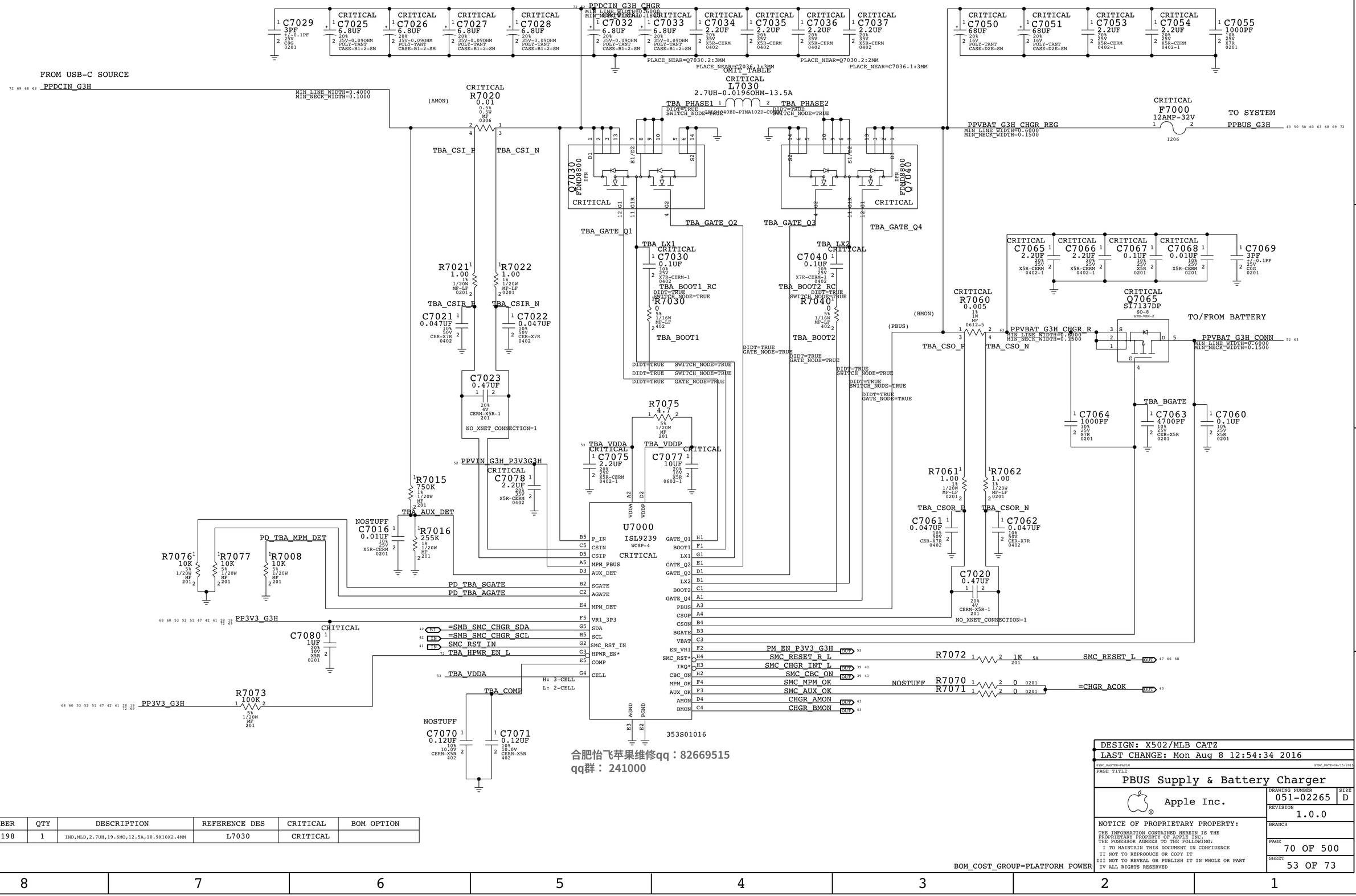

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016
SYNC_MASTER=FAUSH SYNC_DATE=04/15/2015
PAGE TITLE
PBUS Supply & Battery Charger

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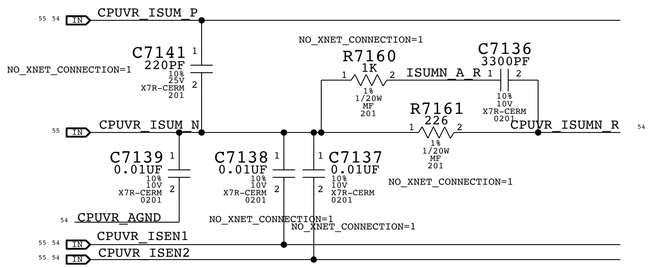

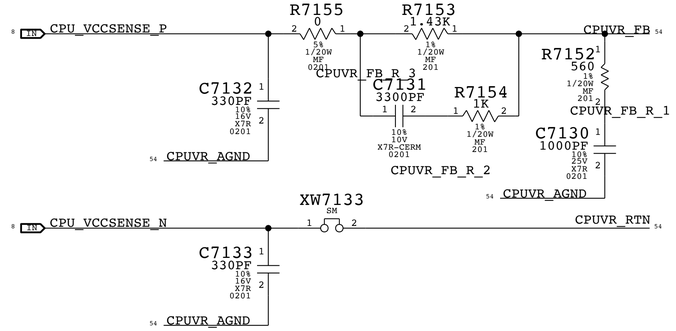

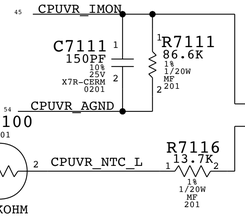

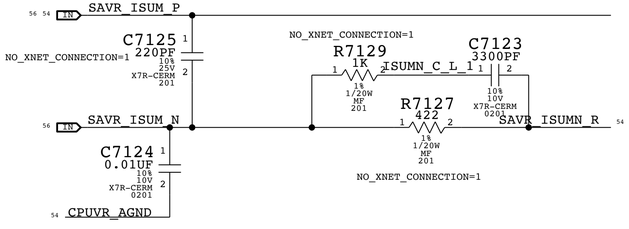

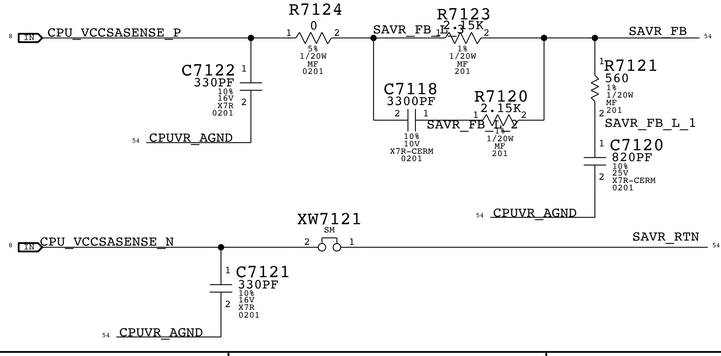

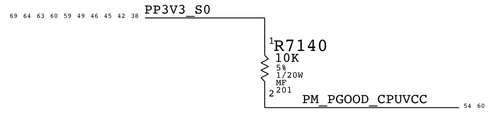

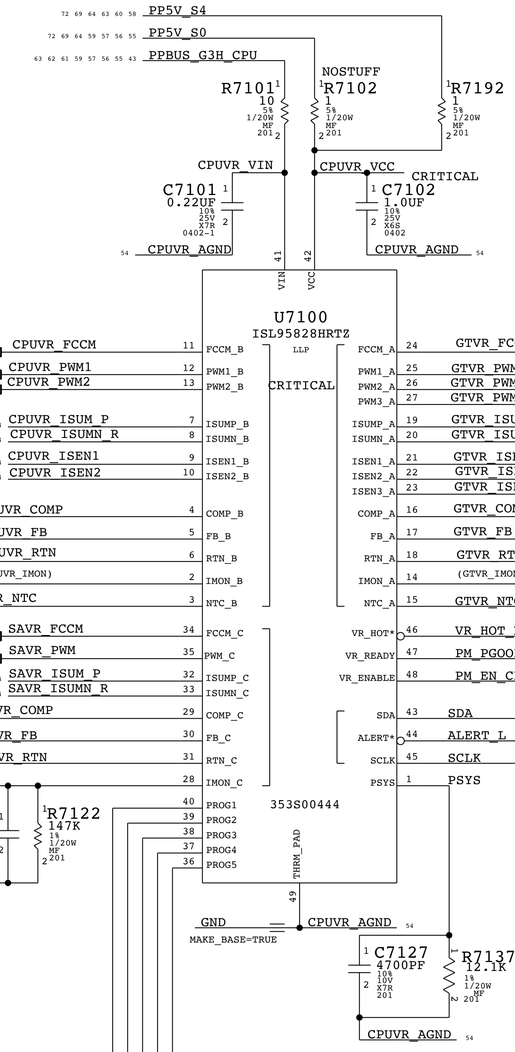

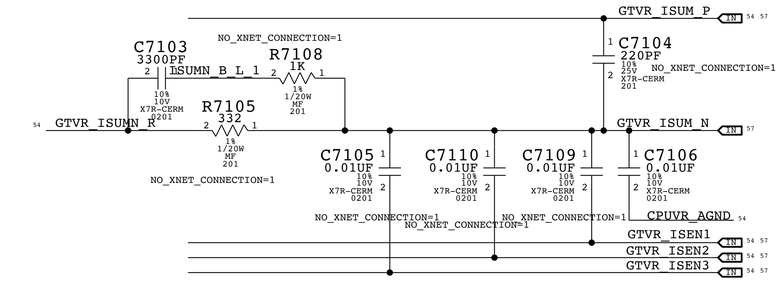

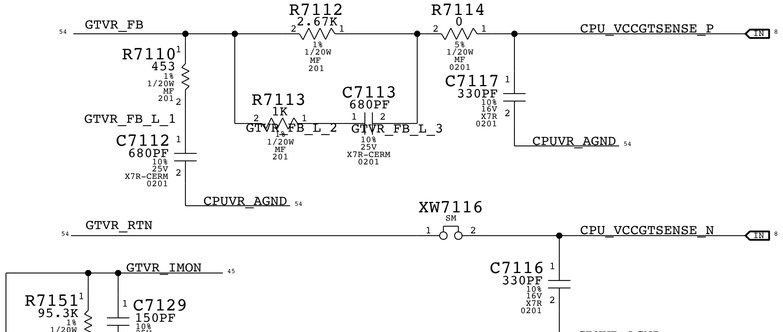

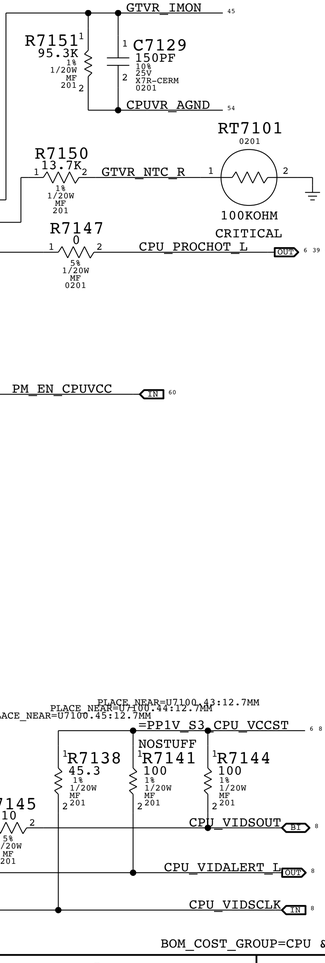

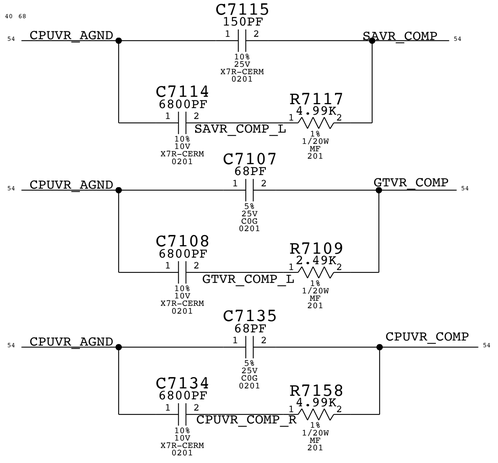

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
VReg CPU VCC Cntl

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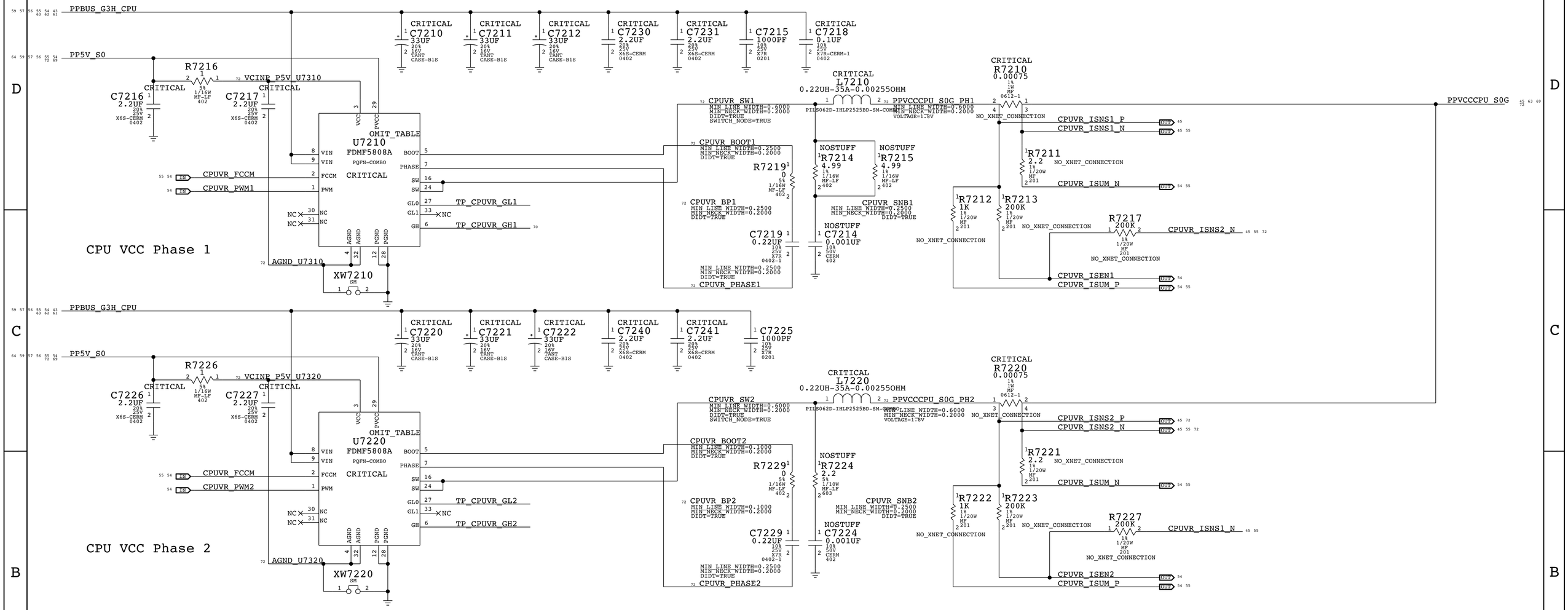

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	5	IC,SIC635,DR MOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7410,U7420,U7430	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
CPU IMVP VCC & VCCSA

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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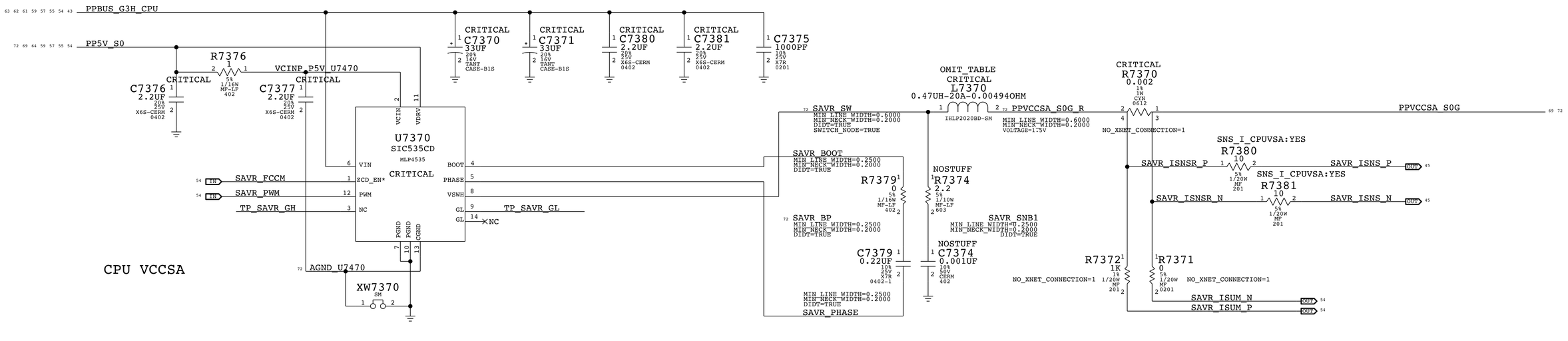

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
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PAGE TITLE
IMVP VCCSA

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CPU VCCGT Phase 1

PPBUS_G3H_CPU
PP5V_S0
R7416 1 5% 1/16W MF-LF 402
VCINP_P5V_U7510
C7416 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7417 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7410 33UF 20% 16V TANT CASE-B1S CRITICAL
C7411 33UF 20% 16V TANT CASE-B1S CRITICAL
C7412 33UF 20% 16V TANT CASE-B1S CRITICAL
C7450 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7451 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7415 1000PF 10% 25V X7R 0201
U7410 FDMF5808A PQFN-COMBO CRITICAL
OMIT_TABLE
VCC PVCC VIN VIN FCCM PWM NC NC NC NC BOOT PHASE SW SW GL0 GL1 GH AGND AGND PGND PGND
GTVR_FCCM
GTVR_PWM1
TP_GTVR_GL1
TP_GTVR_GH1
AGND_U7510
XW7410 SM
L7410 0.22UH-20%-44A-0.0019OHM PILA082D-SM CRITICAL
GTVR_SW1 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE
PPVCCGT_S0G_PH1 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1500
R7410 0.00075 1% 1W MF 0612-1 CRITICAL
PPVCCGT_S0G
GTVR_BOOT1 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
R7419 0 5% 1/16W MF-LF 402
R7414 2.2 5% 1/10W MF-LF 603 NOSTUFF
GTVR_BP1 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
GTVR_SNB1 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
C7419 0.22UF 10% 25V X7R 0402-1
C7414 0.001UF 10% 50V CERM 402 NOSTUFF
MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
GTVR_PHASE1
NO_XNET_CONNECTION
GTVR_ISNS1_P
GTVR_ISNS1_N
GTVR_ISUM_N
GTVR_ISEN1
GTVR_ISUM_P
R7411 2.2 1% 1/20W MF 201
R7412 1K 1% 1/20W MF 201
R7413 200K 1% 1/20W MF 201
R7417 200K 1% 1/20W MF 201
R7418 200K 1% 1/20W MF 201
GTVR_ISNS2_N
GTVR_ISNS3_N

CPU VCCGT Phase 2

PPBUS_G3H_CPU
PP5V_S0
R7426 1 5% 1/16W MF-LF 402
VCINP_P5V_U7520
C7426 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7427 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7420 33UF 20% 16V TANT CASE-B1S CRITICAL
C7421 33UF 20% 16V TANT CASE-B1S CRITICAL
C7422 33UF 20% 16V TANT CASE-B1S CRITICAL
C7460 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7461 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7425 1000PF 10% 25V X7R 0201
U7420 FDMF5808A PQFN-COMBO CRITICAL
OMIT_TABLE
VCC PVCC VIN VIN FCCM PWM NC NC NC NC BOOT PHASE SW SW GL0 GL1 GH AGND AGND PGND PGND
GTVR_FCCM
GTVR_PWM2
TP_GTVR_GL2
TP_GTVR_GH2
AGND_U7520
XW7420 SM
L7420 0.22UH-20%-44A-0.0019OHM PILA082D-SM CRITICAL
GTVR_SW2 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE
PPVCCGT_S0G_PH2 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.8V
R7420 0.00075 1% 1W MF 0612-1 CRITICAL
GTVR_BOOT2 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
R7429 0 5% 1/16W MF-LF 402
R7424 2.2 5% 1/10W MF-LF 603 NOSTUFF
GTVR_BP2 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
GTVR_SNB2 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
C7429 0.22UF 10% 25V X7R 0402-1
C7424 0.001UF 10% 50V CERM 402 NOSTUFF
MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
GTVR_PHASE2
NO_XNET_CONNECTION
GTVR_ISNS2_P
GTVR_ISNS2_N
GTVR_ISUM_N
GTVR_ISEN2
GTVR_ISUM_P
R7421 2.2 1% 1/20W MF 201
R7422 1K 1% 1/20W MF 201
R7423 200K 1% 1/20W MF 201
R7427 200K 1% 1/20W MF 201
R7428 200K 1% 1/20W MF 201
GTVR_ISNS1_N
GTVR_ISNS3_N

CPU VCCGT PHASE 3

PPBUS_G3H_CPU
PP5V_S0
R7436 1 5% 1/16W MF-LF 402
VCINP_P5V_U7530
C7436 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7437 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7430 33UF 20% 16V TANT CASE-B1S CRITICAL
C7431 33UF 20% 16V TANT CASE-B1S CRITICAL
C7470 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7471 2.2UF 20% 25V X6S-CERM 0402 CRITICAL
C7435 1000PF 10% 25V X7R 0201
U7430 FDMF5808A PQFN-COMBO CRITICAL
OMIT_TABLE
VCC PVCC VIN VIN FCCM PWM NC NC NC NC BOOT PHASE SW SW GL0 GL1 GH AGND AGND PGND PGND
GTVR_FCCM
GTVR_PWM3
TP_GTVR_GL3
TP_GTVR_GH3
AGND_U7530
XW7430 SM
L7430 0.22UH-20%-44A-0.0019OHM PILA082D-SM CRITICAL
GTVR_SW3 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE
PPVCCGT_S0G_PH3 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.8V
R7430 0.00075 1% 1W MF 0612-1 CRITICAL
GTVR_BOOT3 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
R7439 0 5% 1/16W MF-LF 402
R7434 2.2 5% 1/10W MF-LF 603 NOSTUFF
GTVR_BP3 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
GTVR_SNB3 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
C7439 0.22UF 10% 25V X7R 0402-1
C7434 0.001UF 10% 50V CERM 402 NOSTUFF
MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
GTVR_PHASE3
NO_XNET_CONNECTION
GTVR_ISNS3_P
GTVR_ISNS3_N
GTVR_ISUM_N
GTVR_ISEN3
GTVR_ISUM_P
R7431 2.2 1% 1/20W MF 201
R7432 1K 1% 1/20W MF 201
R7433 200K 1% 1/20W MF 201
R7437 200K 1% 1/20W MF 201
R7438 200K 1% 1/20W MF 201
GTVR_ISNS1_N
GTVR_ISNS2_N

BOM_COST_GROUP=CPU & CHIPSET

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5V S4

VOUT = 5.1V
6.67A MAX OUTPUT
F = 600 KHZ

PP5V_S4
CRITICAL C7671 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C7670 2.2UF 20% 25V X6S-CERM 0402
C7672 1000PF 10% 25V X7R 0201
CRITICAL C7675 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7676 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7677 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7601 150UF 20% 6.3V TANT-POLY CASE-B1S-1

PPBUS_G3H
CRITICAL R7610 0.003 1% 1W CYN 0612-SHORT-1
SHORT RSENSE
OMIT
PLACE_NEAR=U5540.5:10MM
ISNS_5VS4_P
NO_XNET_CONNECTION=1
ISNS_5VS4_N
PLACE_NEAR=U5540.4:10MM

PPBUS_G3H_P5VS4
CRITICAL C7665 33UF 20% 16V TANT CASE-B1S
CRITICAL C7666 33UF 20% 16V TANT CASE-B1S
CRITICAL C7667 33UF 20% 16V TANT CASE-B1S
C7662 1000PF 10% 25V X7R 0201
CRITICAL C7660 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C7661 2.2UF 20% 25V X6S-CERM 0402

CRITICAL Q7660 CSD58873Q3D Q3D
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
GATE_NODE=TRUE
DIDT=TRUE
VIN
TG
BG
PGND
P5VS4_DRVH
P5VS4_DRVL
376S1038

CRITICAL L7670 1.5UH-20%-12.5A-0.01OHM PIMA082D-COMBO 152M00329
PLACE_NEAR=C7675.1i5.3MM
PLACE_NEAR=L7670.1i3MM
PLACE_NEAR=L7670.2i3MM
P5VS4_VSW

R7666 0 5% 1/16W MF-LF 402
R7664 0 5% 1/16W MF-LF 402
NOSTUFF R7674 2.2 5% 1/10W MF-LF 603
P5VS4_SNUBR
MIN_LINE_WIDTH=0.1500
MIN_NECK_WIDTH=0.0600
DIDT=TRUE
SWITCH_NODE=TRUE
NOSTUFF C7674 0.001UF 10% 50V CERM 402

XW7675 SM P5VS4_VFB1_R
XW7671 SM NO_XNET_CONNECTION=1
XW7670 SM NO_XNET_CONNECTION=1
R7671 10 5% 1/20W MF 201 P5VS4_VFB1_R2
R7677 6.34K 1% 1/20W MF 201 P5VS4_VFB1_RR
CRITICAL R7678 34.8K 0.1% 1/20W MF 0201-1
CRITICAL R7679 10K 0.1% 1/20W MF 0201-1

DIDT=TRUE
P5VS4_CS1_L_P
P5VS4_CS1_L_N
R7672 4.02K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
C7673 0.1UF 10% 6.3V X7R 0201 NO_XNET_CONNECTION=1
R7673 2.67K 1% 1/20W MF 201 NO_XNET_CONNECTION=1

P5VS4_VBST_R
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE
CRITICAL C7669 0.1UF 10% 25V X7R-CERM-1 0402
CRITICAL R7665 2.2 5% 1/16W MF-LF 402
P5VS4_VBST
P5VS4_DRVH_R
P5VS4_SW
P5VS4_DRVL_R
P5VS4_CSP1
P5VS4_VFB1
P5VS4_COMP1
P5VS4_EN
PM_PGOOD_P5VS4
NOSTUFF R7676 10K 1% 1/20W MF 201
R7675 11.3K 1% 1/20W MF 201
P5VS4_COMP1_R
C7678 220PF 10% 25V X7R-CERM 201
C7679 4700PF 10% 10V X7R 201
(P5VP3V3_VREF2)

AUDIBLE SKIPPING
R7651 0 5% 1/20W MF 0201
INAUDIBLE SKIPPING
NOSTUFF R7650 0 5% 1/20W MF 0201
P5VP3V3_SKIPSEL
P5VP3V3_VREG3
P5VP3V3_VREF2
CRITICAL C7652 2.2UF 20% 25V CERM 402
CRITICAL C7653 2.2UF 20% 25V X6S-CERM 0402
CRITICAL U7650 TPS51980A QFN
V5SW VIN VREG5 VREG3 VREF2
SKIPSEL1 SKIPSEL2 OCSEL VBST1 DRVH1 SW1 DRVL1 CSP1 CSN1 MODE VFB1 COMP1 EN1 PGOOD1 GND THRM_PAD
EN VBST2 DRVH2 SW2 DRVL2 CSP2 CSN2 RF VFB2 COMP2 EN2 PGOOD2
P5VXX_EN
P3V3S5_VBST
P3V3S5_DRVH_R
P3V3S5_SW
P3V3S5_DRVL_R
P3V3S5_CSP2
353S3905
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_EN
PM_PGOOD_P3V3S5
NOSTUFF R7695 7.5K 1% 1/20W MF 201
R7696 10K 1% 1/20W MF 201
P3V3S5_COMP2_R
C7699 4700PF 10% 10V X7R 201
C7698 330PF 10% 16V X7R 0201
(P5VP3V3_VREF2)
PLACE_NEAR=U7650.28:1MM
XW76500 SM
GND_5V3V3_AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500
VOLTAGE=0V

PPBUS_G3H
CRITICAL R7620 0.003 1% 1W CYN 0612-SHORT-1
SHORT RSENSE
OMIT
PLACE_NEAR=U5520.5:10MM
ISNS_3V3S5_P
NO_XNET_CONNECTION=1
ISNS_3V3S5_N
PLACE_NEAR=U5520.4:10MM

PPBUS_G3H_P3V3S5
C7682 1000PF 10% 25V X7R 0201
CRITICAL C7685 33UF 20% 16V TANT CASE-B1S
CRITICAL C7686 33UF 20% 16V TANT CASE-B1S
CRITICAL C7687 33UF 20% 16V TANT CASE-B1S

VOUT = 5V
100MA MAX OUTPUT
=PP5V_S5_LDO
CRITICAL C7650 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C7651 10UF 20% 16V X6S-CERM 0603
CRITICAL C7680 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C7681 2.2UF 20% 25V X6S-CERM 0402

CRITICAL Q7680 CSD58873Q3D Q3D
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
GATE_NODE=TRUE
DIDT=TRUE
VIN
TG
BG
PGND
P3V3S5_DRVH
P3V3S5_DRVL
376S1038

P3V3S5_VBST_R
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE
R7685 2.2 5% 1/16W MF-LF 402
CRITICAL C7689 0.1UF 10% 25V X7R-CERM-1 0402
CRITICAL R7686 1 5% 1/16W MF-LF 402
R7684 0 5% 1/16W MF-LF 402
DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000

CRITICAL L7690 1UH-20%-16A-0.0067OHM PIMA082D-COMBO 152S00328
PLACE_NEAR=C7695.1i6.6MM
PLACE_NEAR=L7690.2i3MM
PLACE_NEAR=L7690.1i3MM
P3V3S5_VSW

NOSTUFF R7694 2.2 5% 1/10W MF-LF 603
NO_XNET_CONNECTION=1
XW7690 SM
XW7691 SM
XW7695 SM
P3V3S5_SNUBR
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
DIDT=TRUE
SWITCH_NODE=TRUE
NOSTUFF C7694 0.001UF 10% 50V CERM 402

P3V3S5_VFB2_R
R7691 10 5% 1/20W MF 201
P3V3S5_VFB2_R2
R7697 2.2K 1% 1/20W MF 201
P3V3S5_VFB2_RR
CRITICAL R7698 21K 0.1% 1/20W MF 0201
CRITICAL R7699 10K 0.1% 1/20W MF 0201-1

R7693 3.16K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7692 3.16K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
P3V3S5_CS2_L_P
P3V3S5_CS2_L_N
DIDT=TRUE

V6 (3.3V S5 (DSW))

VOUT = 3.3V
7.33A MAX OUTPUT
F = 600 KHZ

PP3V3_S5
CRITICAL C7690 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C7691 2.2UF 20% 25V X6S-CERM 0402
C7692 1000PF 10% 25V X7R 0201
CRITICAL C7695 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7696 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7613 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7611 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7697 150UF 20% 6.3V TANT-POLY CASE-B1S-1
CRITICAL C7612 150UF 20% 6.3V TANT-POLY CASE-B1S-1

R7660 0 5% 1/20W MF 0201
PM_EN_P5VS5
P5VXX_EN

R7661 0 5% 1/20W MF 0201
PM_EN_P5VS4
P5VS4_EN
NOSTUFF D7663 0201 RB521ES-30
P5VS4_EN_D
NOSTUFF R7663 33 5% 1/20W MF 201
NOSTUFF C7663 1UF 20% 6.3V X6S-CERM 0201

R7662 0 5% 1/20W MF 0201
PM_EN_P3V3S5
P3V3S5_EN
NOSTUFF D7668 0201 RB521ES-30
P3V3S5_EN_D
NOSTUFF R7668 33 5% 1/20W MF 201
NOSTUFF C7668 1UF 20% 6.3V X6S-CERM 0201

BOM_COST_GROUP=PLATFORM POWER

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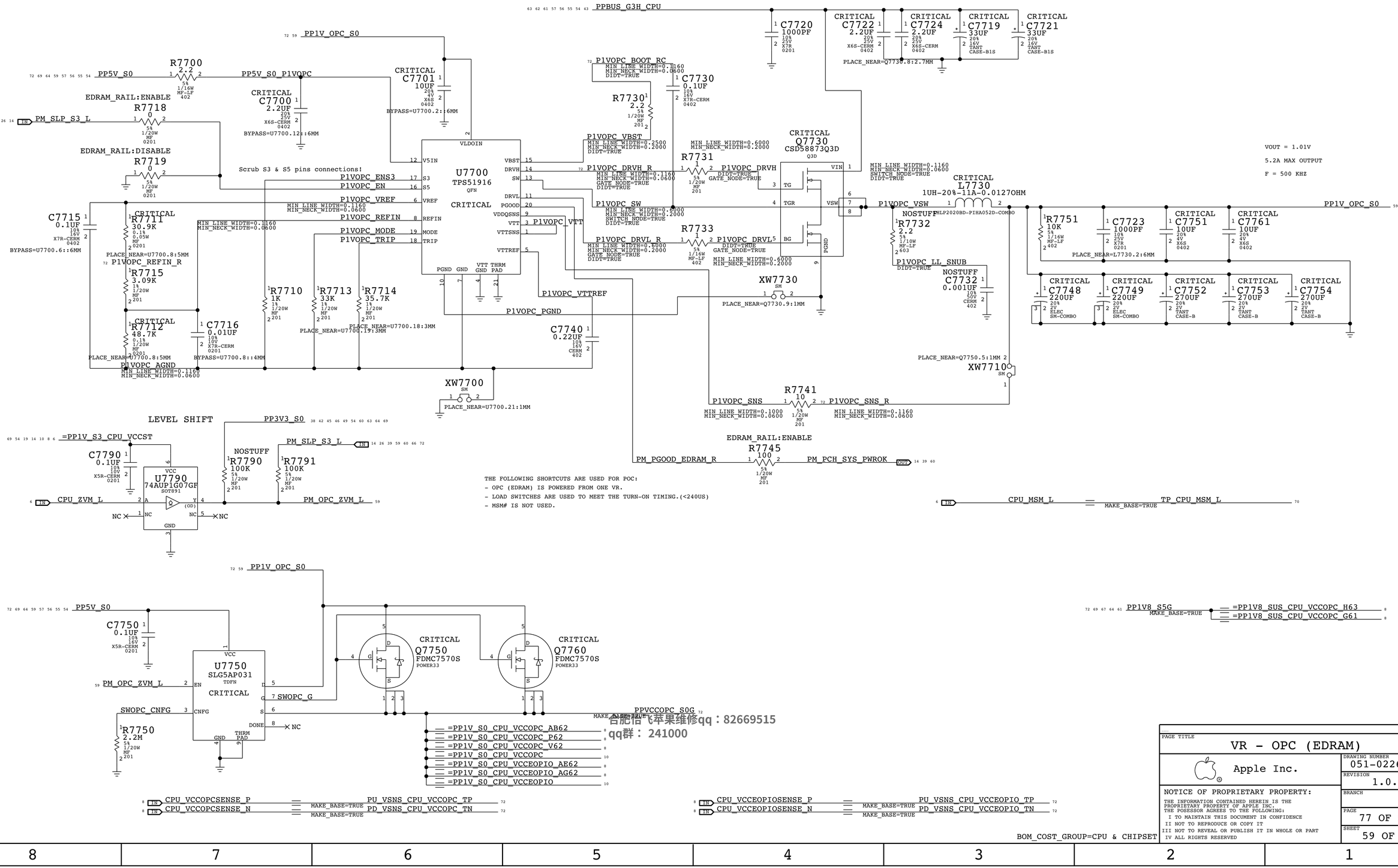
1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)



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OPTIONAL: DIVIDE 1.8V FOR 1.5V INPUT.

PP1V8_S0 — R7865 0 5% 1/20W MF 0201 — PMIC_VSF

NOSTUFF R7868 2.55K 0.1% 1/20W MF 0201

NOSTUFF R7869 174K 1% 1/20W MF 201

PP3V3_S5

PP3V3_LDO3V — CRITICAL C7805 2.2UF 20% 25V X6S-CERM 0402 — AGND_PMIC

U7800 SN650839ZAJ BGA (1 OF 10)

CRITICAL: VDDPG, VDDLV, L8

PP3V3_LDO3V — BANJO_SHUTDOWN:NO R7828 100K 201

BANJO_SHUTDOWN:SMC R7829 100K 201 — PMIC_SHUTDOWN_L

SMC_PM_G2_EN		C7	SHUTDOWN*
PM_SLP_S0_L		D9	STANDBY*
PP3V3_S5G	R7860 0 0201 PMIC_VSA	E7	VSA
PP1V8_S3	R7861 0 0201 PMIC_VSB	K9	VSB
PP3V3_LDO3V	R7862 0 0201 PMIC_VSC	K8	VSC
PM_PGOOD_P3V3S5	R7863 0 0201 PMIC_VSD	E6	VSD
PP3V3_S0	R7864 0 0201 PMIC_VSE	F4	VSE
	PMIC_VSF	E8	VSF
PM_PGOOD_P5VS4	R7866 0 0201 PMIC_VSG	J10	VSG
PM_SLP_S3_L		F5	VSH
(PGVR2) PM_PGOOD_P1V8	R7867 0 0201 PMIC_ENA	B12	ENA
PM_SLP_S4_L		C11	ENB
PM_SLP_S5_L		C12	ENC
SMC_PM_G2_EN		J13	END
PM_SLP_SUS_L		F10	ENE
PM_SLP_S3_L		J12	ENF
PM_SLP_S3_L		B10	ENG
PM_PGOOD_CPUVCC	R7874 0 0201 PMIC_ENH	L11	ENH
PM_SLP_S0_L	R7875 0 0201 PMIC_ENLVA	L6	ENLVA

PP3V3_S5 — R7820 100K 201 PM_PGOOD_P3V3S5; R7821 100K 201 PM_PGOOD_P5VS4; R7825 100K 201 PM_PGOOD_PVDDQ; R7827 100K 201 PM_EN_S0_SW

PM_PGOOD_PVCCPCH	(PGVR5)	(ENVR1)	PM_EN_P1V00
PM_SLP_SUS_L	MAKE_BASE=TRUE	(ENVR2)	PM_EN_P1V8
PM_SLP_S4_L	MAKE_BASE=TRUE	(ENVR4)	PM_EN_PVDDQ
PM_PGOOD_P3V3S5G	MAKE_BASE=TRUE	(ENVR5)	PM_EN_PVCCPCH
PCH_HSIO_PWR_EN	MAKE_BASE=TRUE		PM_EN_P1VS5GTD
PM_EN_S0_SW (BUFFERED PM_SLP_S3_L)	MAKE_BASE=TRUE		PM_EN_P5VS0
	MAKE_BASE=TRUE		

PM_SLP_S0S3_L — R7888 0 0201 — PM_EN_P1V2S0G

PM_PGOOD_P3V3S5		S5_PWRGD (TO SMC)
PM_PGOOD_PVCCIO	(PGVR3) MAKE_BASE=TRUE	TP_PGOOD_PVCCIO
PM_PGOOD_P1V00	(PGVR1) MAKE_BASE=TRUE	TP_PGOOD_P1V00

PP3V3_G3H — C7890 0.1UF 10% 10V X5R-CERM 0201

PMIC_EN_P3V3S5 — U7890 74LVC1G32 SOT891 — SSD_PWR_REQ

PM_EN_PVXS5 (MAKE_BASE=TRUE); PM_EN_P5VS5; PM_EN_P3V3S5

R7890 47K 5% 1/20W MF 201 — 2.4UA CURRENT SOURCE AT VR

=PP3V3_SUS_XDP — C7892 0.1UF 10% 10V X5R-CERM 0201

XDP_PRESENT_L; PM_SLP_S4_L; XDP_PWR:NO R7893 0 5% 1/20W MF 0201

XDP_PWR:YES U7892 74AUP1T97GM SOT886 (INV) — PM_EN_P1VS3; XDP_PWR:YES R7892 100K 5% 1/20W MF 201

KEEP THESE RAILS ON WHEN USING XDP

(S4# OR XDP)

=PP3V3_SUS_XDP — C7894 0.1UF 10% 10V X5R-CERM 0201

XDP_PRESENT_L; PM_SLP_S0S3_L; XDP_PWR:NO R7895 0 5% 1/20W MF 0201

XDP_PWR:YES U7894 74AUP1T97GM SOT886 (INV) (S3# AND S0# OR XDP) — PM_EN_P1VS0G; XDP_PWR:YES R7894 100K 5% 1/20W MF 201

PP3V3_S5 — C7850 0.1UF 10% 10V X5R-CERM 0201

PM_SLP_S3_L; PM_EN_P1V8S0; R7851 36.5K 1% 1/20W MF 201; C7851 0.1UF 10% 10V X5R-CERM 0201 DELAY > 5MS

U7850 74AUP1T97GM SOT886 — PM_EN_P3V3S0; R7850 100K 5% 1/20W MF 201

PP3V3_S5 — C7852 0.1UF 10% 10V X5R-CERM 0201

PM_SLP_S3_L; PM_EN_P3V3S0; R7853 59K 1% 1/20W MF 201; C7853 0.1UF 10% 10V X5R-CERM 0201 DELAY > 1.5MS

U7852 74AUP1T97GM SOT886 — PM_EN_P1V8S0; R7852 100K 5% 1/20W MF 201

PMIC_EN_P3V3S5 — R7886 6.04K 1% 1/20W MF 201

RC DELAY. TPAD REQUIRES 10US MINIMUM OFF TIME < 0.5V.

PGA	D6		PM_PGOOD_P3V3S5G
PGB	C5	PMIC_PGB 0201 0 R7881	PM_EN_P1V8S3
PGC	C6	PMIC_PGC (MAKE_BASE=TRUE)	TP_PMIC_PGC
PGD	H3	PMIC_PGD 0201 0 R7883	PMIC_EN_P3V3S5
PGE	C4	PMIC_PGE 0201 0 R7884	PM_EN_P3V3S5G
PGF	H4		PM_EN_P5VS4
PGG	F3		PM_EN_P3V3S4
PGH	M6	PMIC_PGH 0201 0 R7889	PM_EN_S0_SW
LVA	L12		
LVB	L10	PM_PCH_PWROK	

C7886 0.01UF 10% 10V X7R-CERM 0201

WIRE-ORED WITH PMIC PCHPWROK OUTPUT

PM_SLP_S3_L — R7882 100K 5% 1/20W MF 201

R7887 0 5% 1/20W MF 0201 — PM_SLP_S0_OD_L — PM_SLP_S0S3_L

SLP_S0# Isolation

SLP_S0# IS DRIVEN HIGH OUTSIDE OF S0.
SOME DEVICES CARE ABOUT THIS.
USE BANJO AS BUFFER AND PULL-UP TO SLP_S3# TO CREATE VERSION THAT IS HIGH ONLY IN S0.

=PP3V3_S0_PCH — C7896 0.1UF 10% 10V X5R-CERM 0201

CRITICAL U7896 74LVC1G08 SOT891 — (PGVR4) PM_PGOOD_PVDDQ; PM_SLP_S3_L; (ENVR3) PM_EN_PVCCIO; R7896 100K 5% 1/20W MF 201

AGND_PMIC — CKPLUS_WAIVE=PWRTERM — AGND — BLVCCIO

CRITICAL

U7800 SN650839ZAJ BGA (8 OF 10)

SMC_PM_G2_EN		D11	ACOK
PP3V3_LDO3V		H2	PWRBTNIN
PPBUS_PMIC		E5	VINPP
		F1	BAT1
		G1	BAT2
		E2	ACIN
PPBUS_G3H	PMIC_VDCSNS	G3	VDCSNS
		H9	NVDC*

NOSTUFF R7812 1M 1% 1/20W MF 201 — R7813 150K 1% 1/20W MF 201

0V = HIGH FSW (2 CELL)
3.3V = LOW FSW (3 CELL)

AGND_PMIC

DS3_VREN		K13	NC
1HZ		K11	NC
SYS_PWROK	PMIC_SYSPWROK 0201 0 R7804	H11	PM_PCH_SYS_PWROK
PCH_PWROK	PMIC_PCH_PWROK 0201 0 R7805	E11	PM_PCH_PWROK
ALL_SYS_PWRGD	PMIC_ALLSYSPGD 0201 0 R7806	G11	ALL_SYS_PWRGD (MAKE_BASE=TRUE)
RSMRST_L_PWRGD	PMIC_RSMRST_L 0201 0 R7807	J11	PM_RSMRST_L
PMIC_INT*	PMIC_INT_L 0201 0 R7808	D12	SMC_PMIC_INT_L (PULL-UP AT SMC)
EC_RST*		J3	
EC_ONOFF*		K4	
PCH_PWRBTN*		K2	
DPWROK		K12	(SMC DRIVES DPWROK TO PCH)
ACSWON*		J2	
BAT1SWON*		F2	
BAT2SWON*		G2	
VCCST_PWRGD		E4	

PM_EN_CPUVCC

PMIC_VCCST_PGD — R7803 0 5% 1/20W MF 0201 — CPU_VCCST_PWRGD (PU AT PCH)

AGND_PMIC

PP3V3_S5G — PP3V3_S0

PM_PCH_SYS_PWROK	R7841 100K 5% 201	
PM_PCH_PWROK	R7842 100K 5% 201	
ALL_SYS_PWRGD	R7846 10K 5% 201	
PM_RSMRST_L	R7847 4.7K 5% 201	

PP3V3_LDO3V — CRITICAL C7824 2.2UF 20% 25V X6S-CERM 0402 — AGND_PMIC

CAP AT D1

FOR REPROGRAMMING OTP CONTENTS.

R7830 0 1/20W MF 0201 — PP5VR7V_VPROGOTP — PP5V_LDO5V

CRITICAL

U7800 SN6508392AJ BGA (7 OF 10)

VDD10O0, VDD10I1, VDD5_VPROGOTP

I2C BUS ADDRESS
0V => 0X30/31
3.3V => 0X32/33
FLOAT => 0X34/35

PP3V3_LDO3V — NOSTUFF R7839 3.3K 5% 1/20W MF 201; NOSTUFF R7838 3.3K 5% 1/20W MF 201; NOSTUFF R7832 0 5% 1/20W MF 0201

=SMBUS_SMC_PMIC_SDA	R7836 0 0201 SMB_PMIC_SDA	H1	SDA
=SMBUS_SMC_PMIC_SCL	R7837 0 0201 SMB_PMIC_SCL	J1	SCLK
	PMIC_SLVADDR	L3	SLAVEADDR
AGND_PMIC	R7833 100K 201 PMIC_EN3V3SW	K3	EN3V3SW
PM_PGOOD_P5VS4	R7834 4.7K 201 PMIC_EN5VSW	M5	EN5VSW
	PP5V_S4	N5	VIN5VSW
PPBUS_PMIC		M8	VINLDO3
PPBUS_G3H	R7835 0 0201	N6	VIN

TEMP_ALERT* — AGND_PMIC

VOUT3V3SW; LDO3V — PP3V3_LDO3V

VREF1V25 — PP1V25_VREF

LDO5V — PP5V_LDO5V

CRITICAL C7843 2.2UF 20% 25V X6S-CERM 0402; CRITICAL C7844 2.2UF 20% 25V X6S-CERM 0402

CRITICAL C7837 2.2UF 20% 25V X6S-CERM 0402; CRITICAL C7838 0.47UF 10% 10V X7R 0402; CRITICAL C7839 2.2UF 20% 25V X6S-CERM 0402; CRITICAL C7840 2.2UF 20% 25V X6S-CERM 0402

AGND1, AGND2, AGND3, AGND4 — AGND_PMIC

C1, K1, L13, D13

GND (MAKE_BASE=TRUE)

BOM_COST_GROUP=PLATFORM POWER

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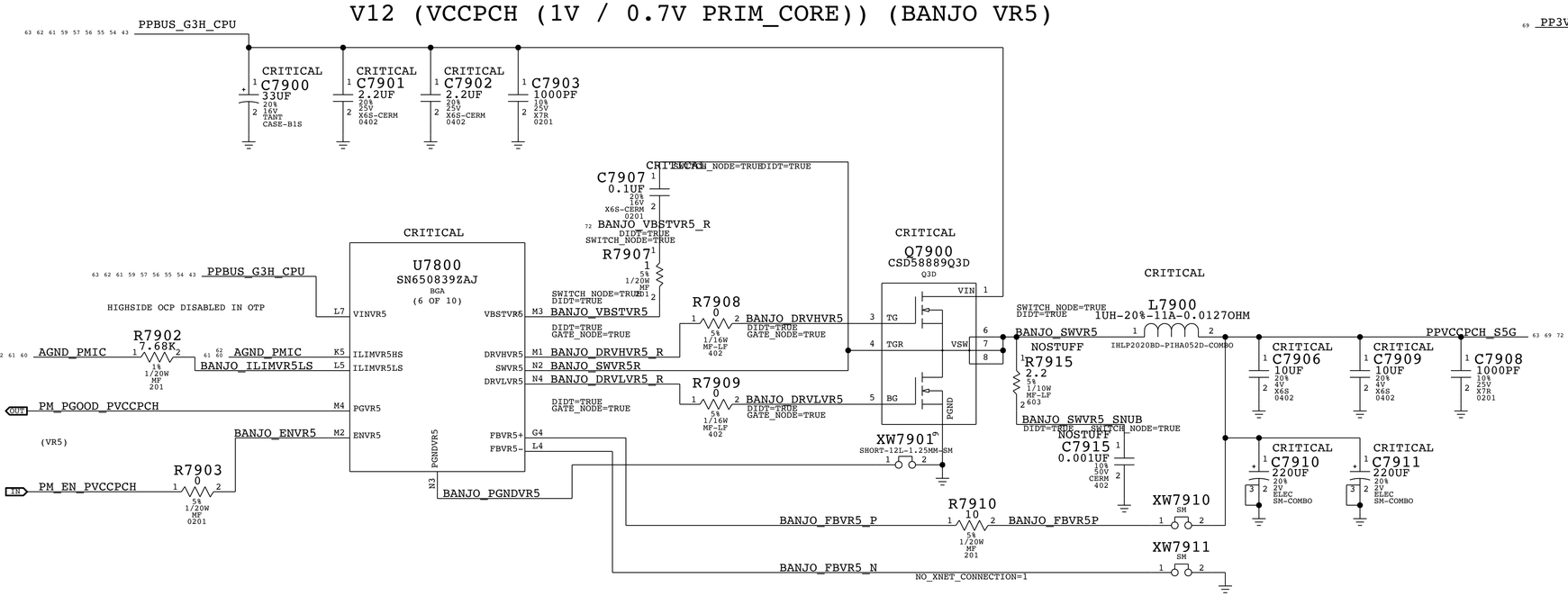
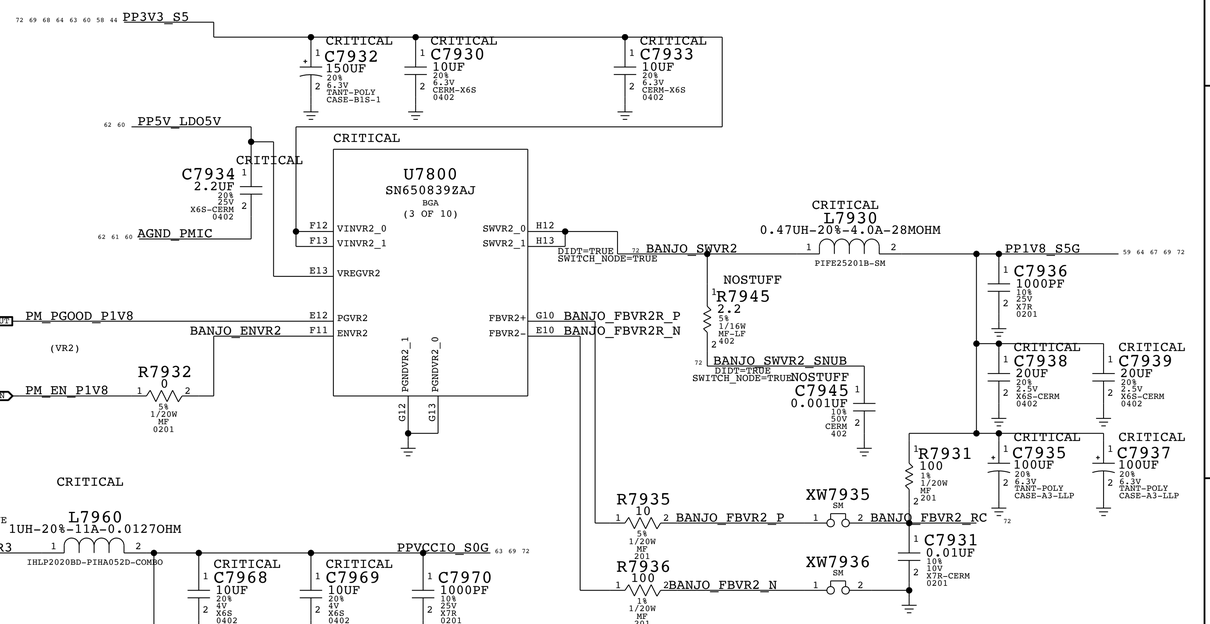
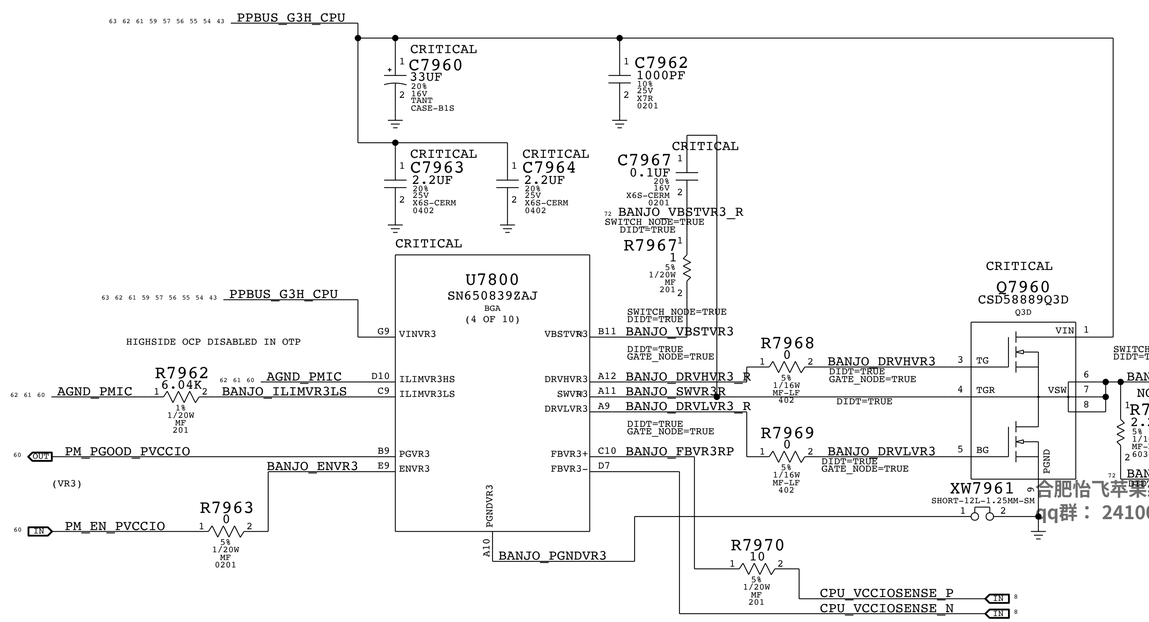
V12 (VCCPCH (1V / 0.7V PRIM_CORE)) (BANJO VR5)



V8 (1.8V) (Banjo VR2)



V4 (0.95V VCCIO) (BANJO VR3)



BOM_COST_GROUP=PLATFORM POWER

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V11 (1V) (Banjo VR1)

PPBUS_G3H_CPU
CRITICAL C8060 33UF 20% 16V TANT CASE-B1S
CRITICAL C8061 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C8062 2.2UF 20% 25V X6S-CERM 0402
C8063 1000PF 10% 25V X7R 0201

PP5V_LDO5V
CRITICAL C8065 2.2UF 20% 25V X6S-CERM 0402
AGND_PMIC

CRITICAL C8067 0.1UF 20% 25V X6S-CERM 0201
DIDT=TRUE SWITCH_NODE=TRUE
BANJO_VBSTVR1_R
R8067 1 5% 1/20W MF 201 2
DIDT=TRUE SWITCH_NODE=TRUE

U7800 SN650839ZAJ BGA (2 OF 10)
M10 VREGVR1
VBSTVR1 M11 BANJO_VBSTVR1
DIDT=TRUE GATE_NODE=TRUE
DRVHVR1 N12 BANJO_DRVHVR1_R
SWVR1 N11 BANJO_SWVR1R
DRVLVR1 N9 BANJO_DRVLVR1_R
DIDT=TRUE GATE_NODE=TRUE
L9 ILIMVR1
M9 PGVR1
M12 ENVR1
FBVR1+ K10
FBVR1- J9
N10 PGNDVR1

R8062 0 5% 1/16W MF-LF 402
BANJO_DRVHVR1 DIDT=TRUE GATE_NODE=TRUE
R8063 0 5% 1/16W MF-LF 402
BANJO_DRVLVR1 DIDT=TRUE GATE_NODE=TRUE

CRITICAL Q8060 CSD58889Q3D Q3D
VIN 1
TG 3
TGR 4
VSW 6 7 8
BG 5
PGND 9

XW8061 SHORT-12L-1.25MM-SM

R8066 6.04K 1% 1/20W MF 201
AGND_PMIC
BANJO_ILIMVR1

PM_PGOOD_P1V00 OUT
BANJO_ENVR1
(VR1)
R8068 0 5% 1/20W MF 0201
PM_EN_P1V00 IN

BANJO_PGNDVR1
BANJO_FBVR1_P
BANJO_FBVR1_N

SWITCH_NODE=TRUE DIDT=TRUE
BANJO_SWVR1
CRITICAL L8060 1UH-20%-11A-0.0127OHM IHLP2020BD-PIHA052D-COMBO
PP1V_S5G_REG
NOSTUFF R8069 2.2 5% 1/10W MF-LF 603
BANJO_SWVR1_SNUB DIDT=TRUE
NOSTUFF C8069 0.001UF 10% 50V CERM 402
R8070 10 5% 1/20W MF 201
BANJO_FBVR1P

SHORT RSENSE
OMIT CRITICAL R8060 0.005 1% 1W CYM 0612-SHORT-1
NO_XNET_CONNECTION=1
ISNS_1VS5G_P OUT 44
ISNS_1VS5G_N OUT 44

CRITICAL C8070 220UF 20% 2V ELEC SM-COMBO
CRITICAL C8071 220UF 20% 2V ELEC SM-COMBO
CRITICAL C8075 10UF 20% 4V X6S 0402
CRITICAL C8076 10UF 20% 4V X6S 0402
C8077 1000PF 10% 25V X7R 0201
PP1V_S5G

XW8070 SM
XW8071 SM
NO_XNET_CONNECTION=1

V13 (0.6V) (Banjo LDO1)

PP1V2_S3
CRITICAL C8090 10UF 20% 4V X6S 0402
CRITICAL C8091 10UF 20% 4V X6S 0402
XW8090 SHORT-12L-0.1MM-SM
BANJO_VINLDO1S

CRITICAL U7800 SN650839ZAJ BGA (9 OF 10)
A6 VINLDO1_0
B6 VINLDO1_1
F9 VINLDO1S
A8 VOUTLDO1_0
B8 VOUTLDO1_1
A7 PGNDLDO1_0
B7 PGNDLDO1_1
D8 FBLDO1

PPVTT_S0
CRITICAL C8095 15UF 20% 2V X6S 0402
CRITICAL C8096 15UF 20% 2V X6S 0402
CRITICAL C8094 15UF 20% 2V X6S 0402
CRITICAL C8097 15UF 20% 2V X6S 0402
CRITICAL C8098 15UF 20% 2V X6S 0402
CRITICAL C8099 15UF 20% 2V X6S 0402

R8095 10 5% 1/20W MF 201
BANJO_FBLDO1_R
XW8095 SM

V10 (1.2V VDDQ) (Banjo VR4)

PPBUS_G3H_CPU
CRITICAL C8030 33UF 20% 16V TANT CASE-B1S
CRITICAL C8031 33UF 20% 16V TANT CASE-B1S
C8036 1000PF 10% 25V X7R 0201
CRITICAL C8033 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C8034 2.2UF 20% 25V X6S-CERM 0402

PP5V_LDO5V
CRITICAL C8035 2.2UF 20% 25V X6S-CERM 0402
AGND_PMIC

CRITICAL C8037 0.1UF 20% 25V X6S-CERM 0201
DIDT=TRUE SWITCH_NODE=TRUE
BANJO_VBSTVR4_R
R8037 1 5% 1/20W MF 201 2
SWITCH_NODE=TRUE DIDT=TRUE

U7800 SN650839ZAJ BGA (5 OF 10)
B4 VREGVR4
VBSTVR4 B3 BANJO_VBSTVR4
DIDT=TRUE GATE_NODE=TRUE
DRVHVR4 A2 BANJO_DRVHVR4_R
SWVR4 A3 BANJO_SWVR4R
DRVLVR4 A5 BANJO_DRVLVR4_R
DIDT=TRUE GATE_NODE=TRUE
D2 ILIMVR4
D4 DDRID
E3 DDR_VTT_CTRL
B5 PGVR4
C2 ENVR4
FBVR4+ C3
FBVR4- D5
A4 PGNDVR4

R8036 0 5% 1/16W MF-LF 402
BANJO_DRVHVR4 DIDT=TRUE GATE_NODE=TRUE
R8039 0 5% 1/16W MF-LF 402
BANJO_DRVLVR4 DIDT=TRUE GATE_NODE=TRUE

CRITICAL Q8030 CSD58873Q3D Q3D
VIN 1
TG 3
TGR 4
VSW 6 7 8
BG 5
PGND 9

XW8031 SHORT-12L-1.25MM-SM

R8031 11K 1% 1/20W MF 201
AGND_PMIC
BANJO_ILIMVR4
0V = 1.2V LPDDR3
R8034 0 5% 1/20W MF 0201
PM_MEMVTT_EN IN
PMIC_VTT_CTRL
(1V INPUT, 3.3V TOLERANT)

PM_PGOOD_PVDDQ OUT
(VR4)
R8033 0 5% 1/20W MF 0201
PM_EN_PVDDQ IN
BANJO_ENVR4

R8032 100K 5% 1/20W MF 201
AGND_PMIC

BANJO_PGNDVR4
BANJO_FBVR4_P
BANJO_FBVR4_N

SWITCH_NODE=TRUE DIDT=TRUE
BANJO_SWVR4
CRITICAL L8030 0.56UH-20%-19A-0.0065OHM PILA062D-SM-COMBO
PP1V2_S3_REG
NOSTUFF R8038 2.2 5% 1/10W MF-LF 603
BANJO_SWVR4_SNUB DIDT=TRUE
NOSTUFF C8038 0.001UF 10% 50V CERM 402
R8040 10 5% 1/20W MF 201
BANJO_FBVR4P

SHORT RSENSE
OMIT CRITICAL R8030 0.003 1% 1W CYM 0612-SHORT-1
NO_XNET_CONNECTION=1
ISNS_1V2S3_P OUT 44
ISNS_1V2S3_N OUT 44

CRITICAL C8040 270UF 20% 2V TANT CASE-B
CRITICAL C8041 270UF 20% 2V TANT CASE-B
NOSTUFF C8042 270UF 20% 2V TANT CASE-B
C8047 1000PF 10% 25V X7R 0201
PP1V2_S3

CRITICAL C8043 220UF 20% 2V ELEC SM-COMBO
CRITICAL C8044 220UF 20% 2V ELEC SM-COMBO
CRITICAL C8045 10UF 20% 4V X6S 0402
CRITICAL C8046 10UF 20% 4V X6S 0402

XW8040 SM
XW8041 SM
NO_XNET_CONNECTION=1

BOM_COST_GROUP=PLATFORM POWER

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69 64 63 62	PP1V2_S3	C8100	12PF 5% 25V CERM 0201	CRITICAL	C8101	3PF +/-0.1PF 25V C0G 0201	CRITICAL	
69 64 63 62	PP1V2_S3	C8102	3PF +/-0.1PF 25V C0G 0201		C8103	3PF +/-0.1PF 25V C0G 0201		
69 64 63 62	PP1V2_S3	C8104	3PF +/-0.1PF 25V C0G 0201		C8105	3PF +/-0.1PF 25V C0G 0201		
69 64 63 60	PP1V8_S3	C8106	3PF +/-0.1PF 25V C0G 0201		C8107	3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8108	3PF +/-0.1PF 25V C0G 0201		C8109	3.5PF +/-0.25PF 25V C0G 0201		
72 69 68 64 63 61 60 58 44	PP3V3_S5	C8110	12PF 5% 25V CERM 0201		C8111	3PF +/-0.1PF 25V C0G 0201		
72 69 64 63 60 58 54	PP5V_S4	C8112	12PF 5% 25V CERM 0201		C8113	3.5PF +/-0.25PF 25V C0G 0201		
72 69 64 63 60 58 54	PP5V_S4	C8114	3.5PF +/-0.25PF 25V C0G 0201		C8115	3.5PF +/-0.25PF 25V C0G 0201		
72 69 64 63 60 58 54	PP5V_S4	C8116	12PF 5% 25V CERM 0201		C8117	3PF +/-0.1PF 25V C0G 0201		
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8118	3PF +/-0.1PF 25V C0G 0201		C8119	3PF +/-0.1PF 25V C0G 0201		
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8120	3PF +/-0.1PF 25V C0G 0201		C8121	3.5PF +/-0.25PF 25V C0G 0201		
72 69 68 53	PPDCIN_G3H	C8122	12PF 5% 25V CERM 0201		C8123	3PF +/-0.1PF 25V C0G 0201		
63 53	PPVBAT_G3H_CHGR_R	C8124	3PF +/-0.1PF 25V C0G 0201		C8125	3PF +/-0.1PF 25V C0G 0201		
63 53	PPVBAT_G3H_CHGR_R	C8126	3PF +/-0.1PF 25V C0G 0201		C8127	3PF +/-0.1PF 25V C0G 0201		
63 53 52	PPVBAT_G3H_CONN	C8128	12PF 5% 25V CERM 0201		C8129	3PF +/-0.1PF 25V C0G 0201		
63 53 52	PPVBAT_G3H_CONN	C8130	3PF +/-0.1PF 25V C0G 0201		C8131	3PF +/-0.1PF 25V C0G 0201		
72 69 55 45	PPVCCCPU_S0G	C8132	3PF +/-0.1PF 25V C0G 0201		C8133	3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 60 51 50 48	PP1V8_S0	C8134	12PF 5% 25V CERM 0201	FREQUENCY SPECIFIC CRITICAL	C8135	3.0PF +/-0.1PF 25V NP0-C0G 0201		
72 69 64 63 62 19	PP1V_S5G	C8137	3PF +/-0.1PF 25V C0G 0201					
72 69 64 63 62 19	PP1V_S5G	C8138	3PF +/-0.1PF 25V C0G 0201	NOSTUFF				
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8136	3PF +/-0.1PF 25V C0G 0201					
72 69 67 64 63 45 44 43 41 72 69	PP3V3_S4	C8139	3PF +/-0.1PF 25V C0G 0201	NOSTUFF				
69 64 63 62	PP1V2_S3	C8140	12PF 5% 25V CERM 0201	NOSTUFF	C8141	3PF +/-0.1PF 25V C0G 0201		
69 64 63 62	PP1V2_S3	C8142	12PF 5% 25V CERM 0201	NOSTUFF	C8143	3PF +/-0.1PF 25V C0G 0201		
69 64 63 62	PP1V2_S3	C8144	12PF 5% 25V CERM 0201	NOSTUFF	C8145	3PF +/-0.1PF 25V C0G 0201		
69 64 63 62	PP1V2_S3	C8146	12PF 5% 25V CERM 0201	NOSTUFF	C8147	3PF +/-0.1PF 25V C0G 0201		
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8148	12PF 5% 25V CERM 0201		C8149	3PF +/-0.1PF 25V C0G 0201		
69 64 63 60	PP1V8_S3	C8150	12PF 5% 25V CERM 0201	NOSTUFF	C8151	3PF +/-0.1PF 25V C0G 0201		
69 64 63 62	PP1V2_S3	C8152	3PF +/-0.1PF 25V C0G 0201		C8153	3PF +/-0.1PF 25V C0G 0201		
69 64 63 60	PP1V8_S3	C8155	3PF +/-0.1PF 25V C0G 0201					
67	PPBUS_SSD_FLT	C8157	3.5PF +/-0.25PF 25V C0G 0201					
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8158	3PF +/-0.1PF 25V C0G 0201		C8159	3PF +/-0.1PF 25V C0G 0201		
69 64 63	PP5V_S5	C8154	3PF +/-0.1PF 25V C0G 0201					
69 64 63	PP5V_S5	C8156	3PF +/-0.1PF 25V C0G 0201					
63 28 27	PP3V3_TBT_X_LC	C8160	12PF 5% 25V CERM 0201		C8161	3PF +/-0.1PF 25V C0G 0201		
63 28 27	PP3V3_TBT_X_LC	C8162	12PF 5% 25V CERM 0201		C8163	3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8164	3PF +/-0.1PF 25V C0G 0201		C8165	3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8166	12PF 5% 25V CERM 0201		C8167	3PF +/-0.1PF 25V C0G 0201		
28	PP3V3_TBT_X_S0	C8168	12PF 5% 25V CERM 0201		C8169	3PF +/-0.1PF 25V C0G 0201		
72 69 61	PPVCCPCH_S5G	C8170	3PF +/-0.1PF 25V C0G 0201		C8171	3PF +/-0.1PF 25V C0G 0201		
72 69 63 57 45	PPVCCGT_S0G	C8172	3PF +/-0.1PF 25V C0G 0201		C8173	3PF +/-0.1PF 25V C0G 0201		
72 69 61	PPVCCIO_S0G	C8175	3PF +/-0.1PF 25V C0G 0201					
69 30 28	PP3V3_UPC_XB_LDO	C8176	12PF 5% 25V CERM 0201		C8177	3PF +/-0.1PF 25V C0G 0201		
72 69 68 64 63 61 60 58 44	PP3V3_S5	C8178	12PF 5% 25V CERM 0201		C8179	3PF +/-0.1PF 25V C0G 0201		
69	PP3V3_S5_SSD_SNS	C8174	3.5PF +/-0.25PF 25V C0G 0201					
72 69 63 57 45	PPVCCGT_S0G	C8181	3PF +/-0.1PF 25V C0G 0201					
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8182	3PF +/-0.1PF 25V C0G 0201		C8183	3PF +/-0.1PF 25V C0G 0201		
69 64 63 62	PP1V2_S3	C8185	3PF +/-0.1PF 25V C0G 0201					
72 69 68 60 58 53 50 43	PPBUS_G3H	C8187	3PF +/-0.1PF 25V C0G 0201					
27	PP0V9_TBT_X_SVR	C8188	12PF 5% 25V CERM 0201		C8189	3PF +/-0.1PF 25V C0G 0201		
72 69 68 64 63 61 60 58 44	PP3V3_S5	C8180	3PF +/-0.1PF 25V C0G 0201					
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8191	3PF +/-0.1PF 25V C0G 0201					
72 69 64 63 60 58 54	PP5V_S4	C8192	12PF 5% 25V CERM 0201		C8193	3PF +/-0.1PF 25V C0G 0201		
72 69 64 63 60 58 54	PP5V_S4	C8194	12PF 5% 25V CERM 0201		C8195	3PF +/-0.1PF 25V C0G 0201		
72 69 64 63 60 58 54	PP5V_S4	C8197	3PF +/-0.1PF 25V C0G 0201					
69 64 63	PP5V_S5	C8199	3PF +/-0.1PF 25V C0G 0201					
72 69 64 63 60 58 54	PP5V_S4	C8196	12PF 5% 25V CERM 0201		C8198	3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 60 51 50 48	PP1V8_S0	C81A0	2.9PF +/-0.05PF 25V C0G-CERM 0201	CRITICAL	C81A1	2.9PF +/-0.05PF 25V C0G-CERM 0201	CRITICAL	
72 69 67 64 63 60 51 50 48	PP1V8_S0	C81A3	2.9PF +/-0.05PF 25V C0G-CERM 0201					
72 69 67 64 63 45 44 43 41	PP3V3_S4	C81A5	3.5PF +/-0.25PF 25V C0G 0201					
72 69 44	PP3V3_S4_WLS	C81A7	3PF +/-0.1PF 25V C0G 0201					
69 64 60 59 54 49 46 45 42 38	PP3V3_S0	C81A8	3PF +/-0.1PF 25V C0G 0201	NOSTUFF	C81A9	3PF +/-0.1PF 25V C0G 0201	NOSTUFF	

BOM_COST_GROUP=PLATFORM POWER

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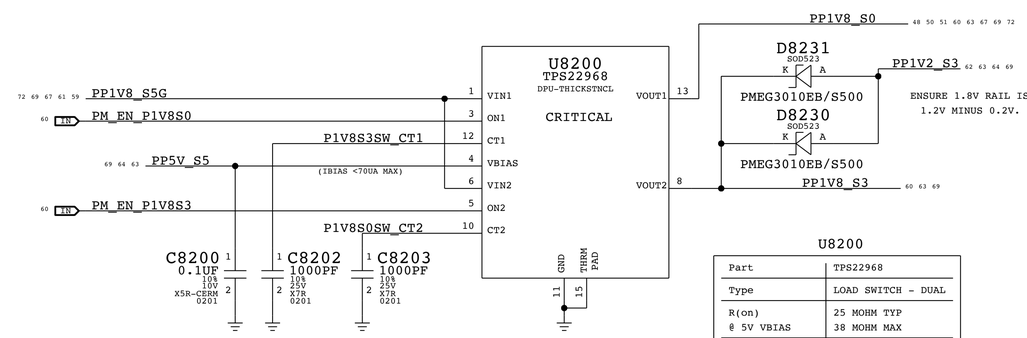
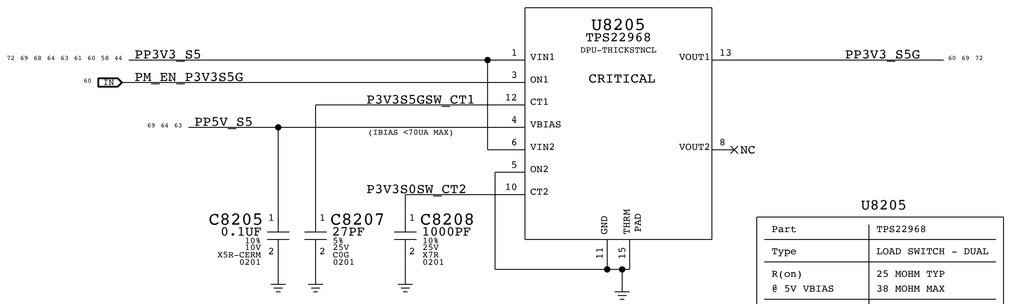


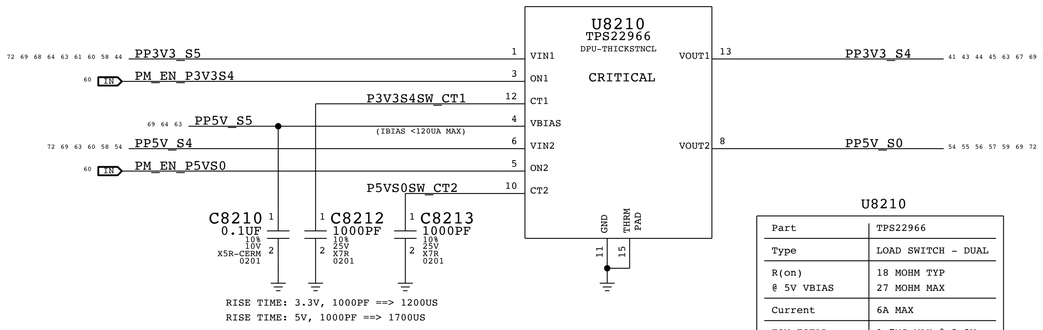
RISE TIME: 1.8V, 1000PF ==> 540US

U8200	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1MS MAX @ 1.8V



RISE TIME: 3.3V, 1000PF ==> 930US

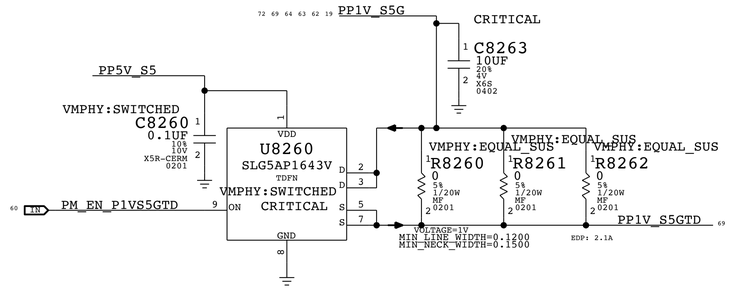
U8205	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1.4MS MAX @ 3.3V



RISE TIME: 3.3V, 1000PF ==> 1200US
RISE TIME: 5V, 1000PF ==> 1700US

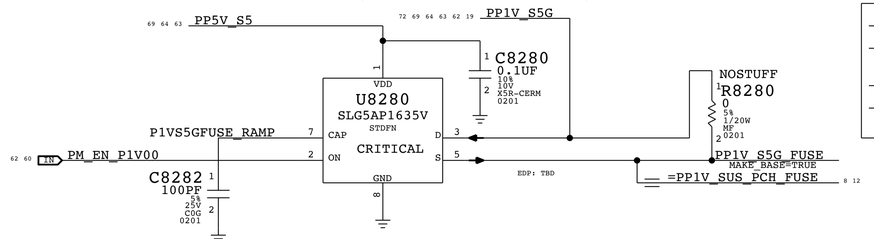
U8210	
Part	TPS22966
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	18 MOHM TYP 27 MOHM MAX
Current	6A MAX
TON-TOTAL	1.7MS MAX @ 3,3V 2.4MS MAX @ 5V

1V S5GTD SWITCH (VCCMPHYGT,VCCSRAM,VCCAPLLEBB)



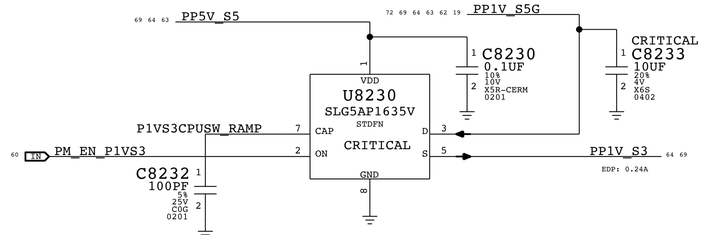
U8260	
Part	SLG5AP1643V
Type	Load Switch
R(on) @ 25C R(on) @ 70C	7.4 MOHM TYP 10.6 MOHM MAX
Current	6A MAX
TON-TOTAL	65US MAX @ 1V

1V S5G FUSE (FOR FAST TURN OFF)



U8230	
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

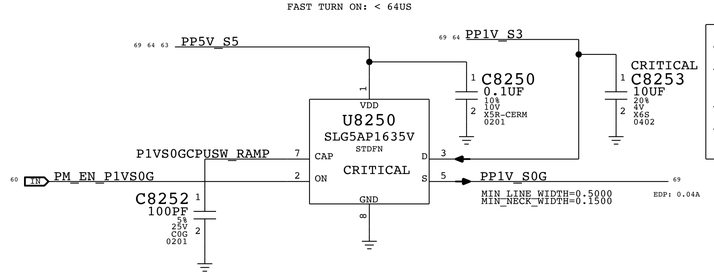
1V S3 SWITCH (VCCST, VCCPLL)



U8230	
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

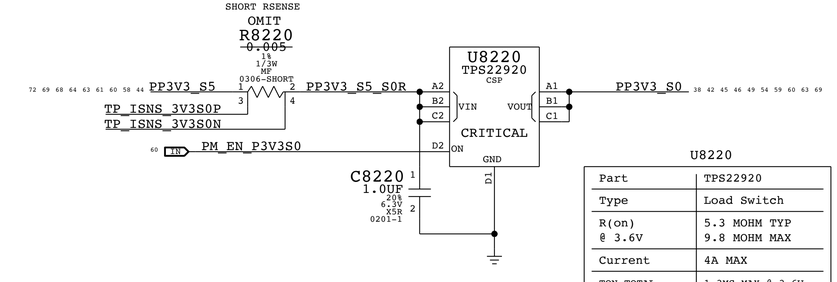
1V S0G CPU SWITCH (VCCSTG)

FAST TURN ON: < 64US

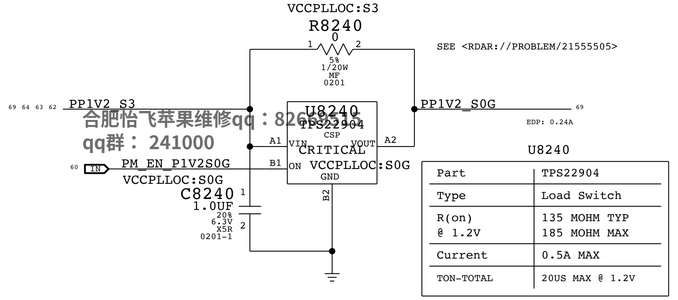


U8250	
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V2 S0G SWITCH (VCCPLL_OC)



U8220	
Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.3 MOHM TYP 9.8 MOHM MAX
Current	4A MAX
TON-TOTAL	1.3MS MAX @ 3.6V



U8240	
Part	TPS22904
Type	Load Switch
R(on) @ 1.2V	135 MOHM TYP 185 MOHM MAX
Current	0.5A MAX
TON-TOTAL	20US MAX @ 1.2V

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER 051-02265 | SIZE D
REVISION 1.0.0
BRANCH
PAGE 82 OF 500
SHEET 64 OF 73

Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)

=PPVIN_S0SW_LCDBKLTFET
740S0159
CRITICAL
F8400
3AMP-32V
0603
PPVIN_S0SW_LCDBKLT_F
R8400 0.025 1% 1W MF 0612-1
107S00034
PPVIN_S0SW_LCDBKLT_R
CRITICAL
Q8400
FDC638APZ_SBMS001
SSOT6-HF
C8400 1000PF 10% 16V X7R-1 0201
R8401 80.6K 1% 1/16W MF-LF 402
NOSTUFF C8401 0.001UF 10% 50V CERM 402
LCDBKLT_EN_L
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
R8402 63.4K 1% 1/16W MF-LF 402
=PP5V_S0_BKLT
R8444 0 5% 1/16W MF-LF 402
R8445 0 5% 1/16W MF-LF 402
PP5V_S0_BKLT_A
PP5V_S0_BKLT_D
C8440 1UF 10% 10V X5R 402-1
C8441 1UF 10% 10V X5R 402-1
PLACE_NEAR=U8400.5:5MM
PLACE_NEAR=U8400.18:5MM
GND_BKLT_SGND
R8440 1M 5% 1/20W MF 201
BKLT_SD
BKLT_SENSE_OUT
PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW
EDP_BKLT_EN
R8442 0 5% 1/20W MF 0201
BKLT_EN_R
NO STUFF C8442 33PF 5% 25V NP0-C0G 0201
GND_BKLT_SGND
BKLT_PWM_KEYB
R8447 10K 5% 1/20W MF 201
GND_BKLT_SGND
=PP5V_S0_BKLT
R8452 1.8K 5% 1/20W MF 201
R8453 1.8K 5% 1/20W MF 201
PLACE_NEAR=U8400.15:10MM
R8450 0 5% 1/20W MF 0201
=I2C_BKLT_SCL
BKLT_SCL
R8451 0 5% 1/20W MF 0201
=I2C_BKLT_SDA
BKLT_SDA
I2C ID DEDICATED.ONLY CONNECTS TO JERRY
PLACE_NEAR=U8400.16:10MM

U8400
LLP
LP8548B1SQ_-04
VDDD 5
VDDA 18
SD 11
VSENSE_N 9
VSENSE_P 10
SENSE_OUT 19
EN 17
PWM_KEYB 12
SCL (IPU) 15
SDA (IPU) 16
SW 2
SW 1
FB 21
GD 4
ISET_KEYB 20 NC
KEYB1 13 NC
KEYB2 14 NC
SW2 6 NC
FB2 8 NC
GND_SW 24
GND_SW 23
GND_SW2 7
GNDD 3
GNDA 22
THRM PAD 25
CRITICAL
353S4160
XW8400 SM
GND_BKLT_SGND
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V
MAKE_BASE=TRUE
C8413 12PF 5% 25V CERM 0201
C8414 3PF +/-0.1PF 25V C0G 0201
PLACE_NEAR=Q8401.5:3MM
CRITICAL
L8410
15UH-20%-1.9A-0.24OHM
PIME062D-SM
152S00253
CRITICAL C8410 4.7UF 10% 25V X6S-CERM 0603
CRITICAL C8411 4.7UF 10% 25V X6S-CERM 0603
C8412 0.1UF 10% 25V X5R 402
PLACE_NEAR=L8410.1:5MM
PLACE_NEAR=L8410.1:5MM
PLACEMENT_NOTE:
SANDWICH C8410 AND C8411
PLACE_NEAR=L8410.2:3MM
371S0704
CRITICAL
D8410
SOD123-COMBO
PMEG10020ELR-DFLS2100
PPVIN_SW_LCDBKLT_SW
R8410 10 5% 1/16W MF-LF 402
LCDBKLT_FET_DRV_R
GATE_NODE=TRUE
DIDT=TRUE
DIDT=TRUE
SWITCH_NODE=TRUE
VOLTAGE=55V
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=2.0000
CRITICAL
Q8401
SI7812DN
PWRPK-1212-8
PLACE_NEAR=U8400.1:3MM
LCDBKLT_SW
LCDBKLT_FB
LCDBKLT_FET_DRV
GATE_NODE=TRUE
DIDT=TRUE

PPVOUT_S0_LCDBKLT
CRITICAL C8460 2.2UF 10% 100V X5R 1206
CRITICAL C8461 2.2UF 10% 100V X5R 1206
CRITICAL C8462 2.2UF 10% 100V X5R 1206
CRITICAL C8463 2.2UF 10% 100V X5R 1206
CRITICAL C8464 2.2UF 10% 100V X5R 1206
CRITICAL C8465 2.2UF 10% 100V X5R 1206
CRITICAL C8466 2.2UF 10% 100V X5R 1206
CRITICAL C8467 2.2UF 10% 100V X5R 1206
CRITICAL C8468 2.2UF 10% 100V X5R 1206
CRITICAL C8469 2.2UF 10% 100V X5R 1206
CRITICAL C8470 2.2UF 10% 100V X5R 1206
CRITICAL C8471 2.2UF 10% 100V X5R 1206
CRITICAL C8472 2.2UF 10% 100V X5R 1206
CRITICAL C8473 2.2UF 10% 100V X5R 1206
C8474 12PF 5% 100V CERM 0402
C8475 12PF 5% 100V CERM 0402
C8476 3PF +/-0.1PF 100V C0G 0201
C8477 12PF 5% 100V C0G 0201
C8478 3PF +/-0.1PF 100V C0G 0201
C8479 12PF 5% 100V C0G 0201
XW8410 SM
LCDBKLT_TB_XWR
R8431 18.2K 1% 1/16W MF-LF 402
R8432 150K 1% 1/16W MF-LF 402
NOSTUFF C8432 100PF 5% 100V C0G-CERM 0603

Vout = 46V Typ, 55V Max
Iout = 0.12A Typ, 0.15A Max
Fs = 625kHz Typ (+/- 7%)

LINE WIDTHS
PP5V_S0_BKLT_A
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
PP5V_S0_BKLT_D
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

PBUS LINE WIDTHS
PPVIN_S0SW_LCDBKLT_F
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V
PPVIN_S0SW_LCDBKLT_R
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V
PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

LCD BKLT LINE WIDTHS
LCDBKLT_FET_DRV
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V
GATE_NODE=TRUE
DIDT=TRUE
PPVIN_SW_LCDBKLT_SW
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V
SWITCH_NODE=TRUE
DIDT=TRUE
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=K36J SYNC_DATE=06/15/2011
PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
BRANCH
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LCD PANEL INTERFACE (eDP) + Camera (MIPI)

LCD Panel HPD & AUX strapping

=PP3V3_S0_LCD
NO_XNET_CONNECTION=1
R8503 1M 5% 1/20W MF 201
DP_INT_HPD
R8501 1M 5% 1/20W MF 201
EDP_INT_AUX_P
NO_XNET_CONNECTION=1
R8502 1M 5% 1/20W MF 201
EDP_INT_AUX_N

=PP5V_S0_LCD
CRITICAL
U8500 SLG5AP1443V TDFN
R8517 330 1% 1/20W MF 201
PANEL_P5V_EN_D
D8517 SC2 DSF01S30SCAP
LCD_PWR_SLEW
PANEL_P5V_EN
R8515 150K 1% 1/20W MF 201
C8515 0.1UF 10% 10V X5R-CERM 0201
C8509 2200PF 10% 10V X7R-CERM 0201
C8511 0.1UF 10% 10V X5R-CERM 0201
CRITICAL C8512 10UF 10% 10V X5R-CERM 0402-7
VOLTAGE=5V
PP5V_S0SW_LCD
C8560 12PF 5% 25V CERM 0201
C8561 3PF +/-0.1PF 25V C0G 0201

PPVOUT_S0_LCDBKLT
C8504 3PF +/-0.1PF 100V C0G 0201
C8503 12PF 5% 100V C0G 0201

=PP3V3_S5_LCD
CRITICAL
U8501 SLG5AP1443V TDFN
LCD_PWR_SLEW_3V3
C8513 2200PF 10% 10V X7R-CERM 0201
C8510 1.0UF 20% 6.3V X5R 0201-1
VOLTAGE=3.3V
PP3V3_S0SW_LCD_R
R8554 0 5% 1/16W MF-LF 402
VOLTAGE=3.3V
PP3V3_S0SW_LCD_R1
SHORT RSENSE
OMIT
R8520 0.005 1% 1/3W MF 0306-SHORT
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.5000
VOLTAGE=3.3V
PP3V3_S0SW_LCD
C8562 12PF 5% 25V CERM 0201
C8563 3PF +/-0.1PF 25V C0G 0201

R8516 200K 1% 1/20W MF 201
PANEL_P3V3_EN
C8516 0.47UF 10% 6.3V CERM-X5R 0201
ISNS_LCDPANEL_P
ISNS_LCDPANEL_N

PPVOUT_S0_LCDBKLT
C8502 3PF +/-0.1PF 100V C0G 0201
C8501 12PF 5% 100V C0G 0201
C8500 1000PF 10% 100V X7R-CERM 0603
PLACE_NEAR=J8500:5MM

R8518 330 1% 1/20W MF 201
PANEL_P3V3_EN_D
D8518 SC2 DSF01S30SCAP

PANEL_P3V3_EN_DLY

CRITICAL
J8500 20759-042E-02 F-ST-SM

PPVOUT_S0_LCDBKLT 43 PWR 44 PP3V3_S0SW_LCD

	1	2	
EDP_INT_AUX_N	3	4	BUF_EDP_PANEL_PWR_EN
EDP_INT_AUX_P	5	6	DP_INT_HPD (OUTP)
EDP_INT_ML_N<0>	7	8	
EDP_INT_ML_P<0>	9	10	LCD_IRQ_L (OUTP)
	11	12	
EDP_INT_ML_N<1>	13	14	TCON_BKLT_PWM (OUTP)
EDP_INT_ML_P<1>	15	16	EDP_BKLT_PWM (IN)
	17	18	
EDP_INT_ML_N<2>	19	20	
EDP_INT_ML_P<2>	21	22	
	23	24	I2C_BKLT_SDA (BI)
EDP_INT_ML_N<3>	25	26	I2C_BKLT_SCL (BI)
EDP_INT_ML_P<3>	27	28	I2C_TCON_SDA_CONN
	29	30	I2C_TCON_SCL_CONN
MIPI_DATA_CONN_N (OUTP)	31	32	
MIPI_DATA_CONN_P (OUTP)	33	34	I2C_ALS_SDA_CONN
	35	36	I2C_ALS_SCL_CONN
MIPI_CLK_CONN_N (OUTP)	37	38	I2C_CAM_SCL_CONN
MIPI_CLK_CONN_P (OUTP)	39	40	I2C_CAM_SDA_CONN
	41	42	
	PWR		
PP5V_S0SW_LCD	45	46	PP5V_S0_ALSCAM_F
	GND		
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	

C8564 12PF 5% 25V CERM 0201

516S00228

COWLING BOSES
860-00469
SH8501 2.7X1.8R-1.4ID-0.91H-SM
SH8502 2.7X1.8R-1.4ID-0.91H-SM

U8510 BYPASS

PANEL_P3V3_EN
NOSTUFF R8590 0 5% 1/20W MF 0201
PANEL_P3V3_EN_DLY
NOSTUFF R8591 0 5% 1/20W MF 0201
BUF_EDP_PANEL_PWR_EN
NOSTUFF R8592 0 5% 1/20W MF 0201
SMC_RESET_L
BUF_SMC_RESET_L

=PP3V3_G3H_SMC
CRITICAL
U8510 SLG4AP4998 STQFN
EDP_PANEL_PWR_EN
PM_SLP_S3_L
SMC_RESET_L
EDP_PANEL_PWR_EN
PM_SLP_S3_L
SMC_RESET_INPUT_L
PANEL_FET_EN_DLY
PANEL_PWR_EN_CONN
SMC_RESET_OUTPUT_L
BUF_EDP_PANEL_PWR_EN
BUF_SMC_RESET_L
X604_DISP_PWR_EN
X604_DISP_SMC_RST_L
NC0
NC1
R8510 100K 5% 1/20W MF 201

I2C_ALS_SDA	R8556 33 5% 1/20W MF 201	PLACE_NEAR=J8500:5MM	I2C_ALS_SDA_CONN
I2C_ALS_SCL	R8558 33 5% 1/20W MF 201	PLACE_NEAR=J8500:5MM	I2C_ALS_SCL_CONN
I2C_CAM_SDA	R8560 33 5% 1/20W MF 201	PLACE_NEAR=J8500:5MM	I2C_CAM_SDA_CONN
I2C_CAM_SCL	R8562 33 5% 1/20W MF 201	PLACE_NEAR=J8500:5MM	I2C_CAM_SCL_CONN
=I2C_TCON_SDA	R8572 33 5% 1/20W MF 201	PLACE_NEAR=J8500:5MM	I2C_TCON_SDA_CONN
=I2C_TCON_SCL	R8568 33 5% 1/20W MF 201	PLACE_NEAR=J8500:5MM	I2C_TCON_SCL_CONN

C8550 12PF 5% 25V CERM 0201
C8551 12PF 5% 25V CERM 0201
C8552 12PF 5% 25V CERM 0201
C8553 12PF 5% 25V CERM 0201
C8554 12PF 5% 25V CERM 0201
C8555 12PF 5% 25V CERM 0201

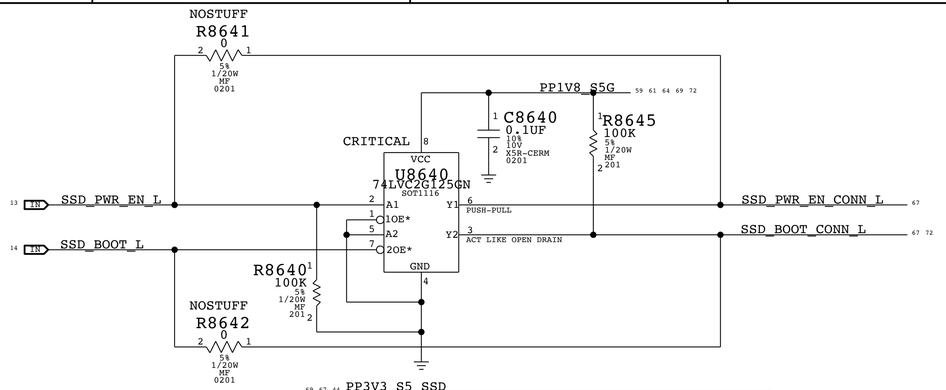
EDP_ML_C_P<0>	C8520 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_P<0>
EDP_ML_C_N<0>	C8521 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_N<0>
EDP_ML_C_P<1>	C8522 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_P<1>
EDP_ML_C_N<1>	C8523 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_N<1>
EDP_ML_C_P<2>	C8524 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_P<2>
EDP_ML_C_N<2>	C8525 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_N<2>
EDP_ML_C_P<3>	C8526 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_P<3>
EDP_ML_C_N<3>	C8527 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_ML_N<3>
EDP_AUXCH_C_P	C8528 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_AUX_P
EDP_AUXCH_C_N	C8529 0.1UF 10% 16V X5R-CERM 0201		EDP_INT_AUX_N

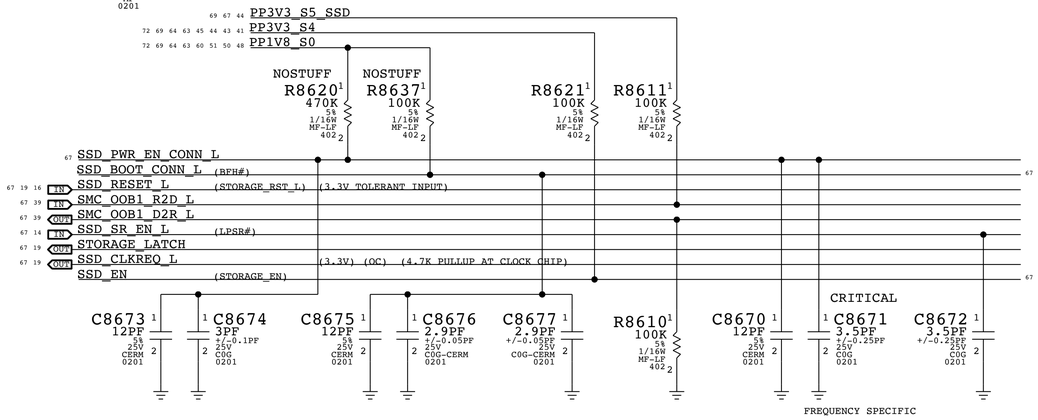
BUF_EDP_PANEL_PWR_EN
LCD_IRQ_L
TCON_BKLT_PWM
I2C_BKLT_SDA

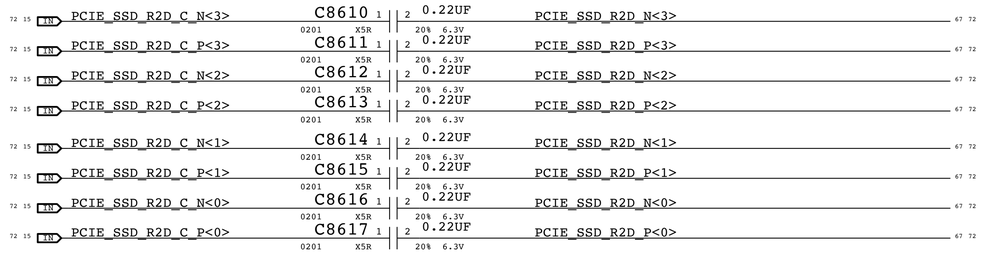
C8570 12PF 5% 25V CERM 0201
C8571 12PF 5% 25V CERM 0201
C8572 12PF 5% 25V CERM 0201
C8573 12PF 5% 25V CERM 0201

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=K362
SYNC_DATE=06/23/2015
PAGE TITLE: eDP Display Connector
Apple Inc.
DRAWING NUMBER: 051-02265
SIZE: D
REVISION: 1.0.0
BRANCH:
PAGE: 85 OF 500
SHEET: 66 OF 73

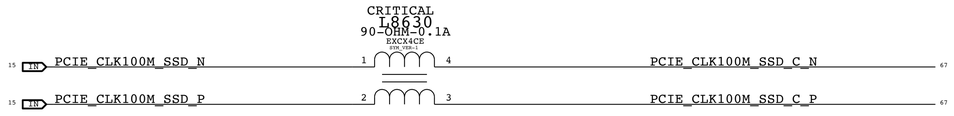






AC CAPS FOR PCIE GEN 3

Per PCIe spec, only TX side should have AC cap



NOTES:

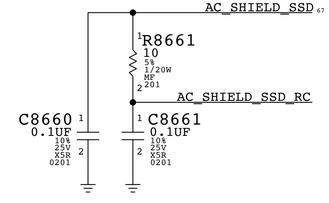
1. POWER-ON TO PERST_L DE-ASSERTION = 10MS MINIMUM
2. PP3V3_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF. (PIN 47, PP3V3_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
3. PCIE CLK100M ARE 2.5V SIGNALS.
4. OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.

SSD STANDOFFS

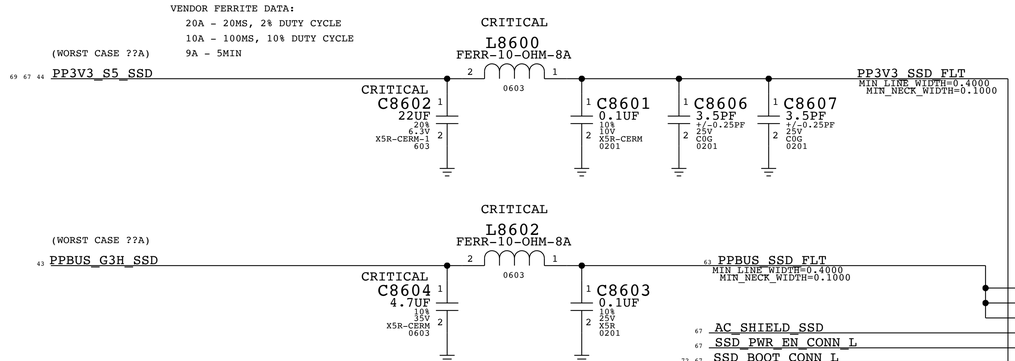
860-00380

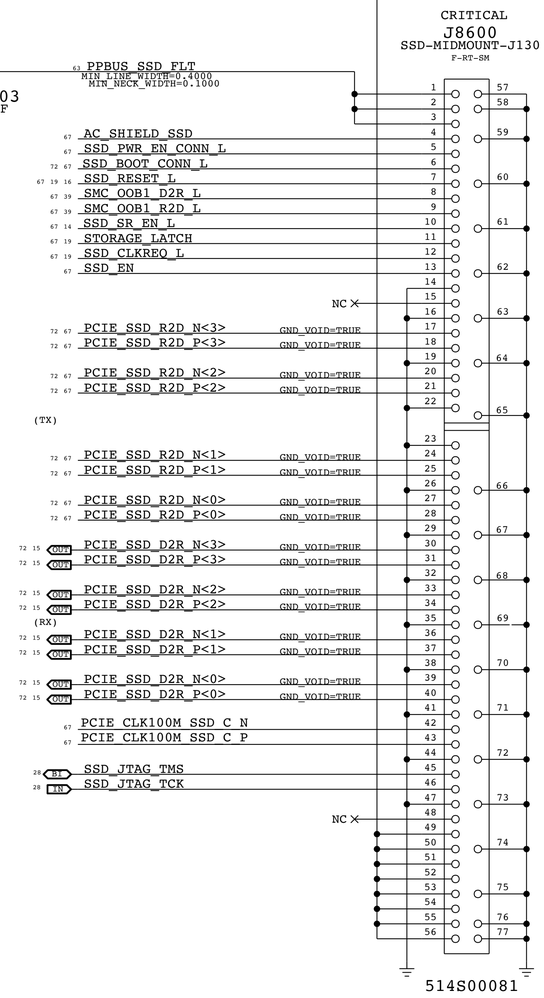
SH8600
4.0OD1.6ID-0.85H-TH

SH8601
4.0OD1.6ID-0.85H-TH



BOM_COST_GROUP=SSD





DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE

SSD MODULE

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
BRANCH
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ON-BOARD POWER BUTTON

DEV_POWER_BUTTON
SW9988
SOX-152HNT
SM

SILK_PART=PWR_BTN
PLACE_SIDE=TOP

SMC_ONOFF_R_L

DEV_POWER_BUTTON
R9988
0
5%
1/20W
MF
0201

SMC_ONOFF_L → OUT 38 39 40 72

NOSTUFF
C9988
1000PF
10%
25V
X7R
0201

DEV_POWER_BUTTON
SW9989
SOX-152HNT
SM

SILK_PART=PWR_BTN
PLACE_SIDE=BOTTOM

SMC_RESET BUTTON

DEV_RST_BUTTONS:YES
SW9998
SOX-152HNT
SM

SILK_PART=SMC_RST

SMC_RST_BTN_R_L

DEV_RST_BUTTONS:YES
R9998
0
5%
1/20W
MF
0201

SMC_RST_BTN_L → OUT 41

NOSTUFF
C9998
1000PF
10%
25V
X7R
0201

SYSTEM RESET BUTTON

DEV_RST_BUTTONS:YES
SW9999
SOX-152HNT
SM

SILK_PART=SMC_RST

SYSRST_R_L

DEV_RST_BUTTONS:YES
R9999
0
5%
1/20W
MF
0201

PM_SYSRST_L → OUT 14 17 39

NOSTUFF
C9999
1000PF
10%
25V
X7R
0201

DIAG LED BUTTON

PRESS TO ENABLE DIAG LEDS.

DEV_LEDS
SW9930
SOX-152HNT
SM

SILK_PART=DIAG_LED

PLACE ON SAME SIDE
AS DIAG LEDS.

DIAG_LED_EN_R_L

DEV_LEDS
R9933
20
5%
1/20W
MF
201

DIAG_LED_ENABLE_L

DEV_LEDS
C9933
1UF
20%
6.3V
X6S-CERM
0201

NOSTUFF
R9930
0
5%
1/20W
MF
0201

STUFF TO ALWAYS ENABLE LEDS.

(1V SIGNALS)

72 69 63 60 58 53 50 43 IN PPBUS_G3H

DEV_LEDS
DZ9927
GDZ-0201
GDZT2R8.2

DIV_PPBUS_G3H

DEV_LEDS
R9928
470K
5%
1/20W
MF
201

72 69 63 53 IN PPDCIN_G3H

DEV_LEDS
R9920
470K
5%
1/20W
MF
201

DIV_PPDCIN

DEV_LEDS
R9921
470K
5%
1/20W
MF
201

66 53 47 IN SMC_RESET_L

39 14 IN PM_DSW_PWRGD

60 39 17 14 IN PM_RSMRST_L

60 58 IN PM_PGOOD_P5VS4

62 60 IN PM_PGOOD_PVDDQ

72 68 60 19 IN PM_SLP_S0S3_L

35 19 14 IN PLT_RST_L

DEV_LEDS
R9922
10K
5%
1/20W
MF
201

PLTRST_LED_L

65 5 IN EDP_BKLT_EN

72 60 39 14 PM_SLP_S4_L

DEV_LEDS
R9923
470K
5%
1/20W
MF
201

CATERR_LED

39 19 6 IN CPU_CATERR_L

DEV_LEDS
R9925
100K
5%
1/20W
MF
201

CATERR_LED_L

DEV_LEDS
Q9922
DST3904DJ
SOT963

72 69 68 64 63 61 60 58 44 PP3V3_S5

DEV_LEDS
C9911
0.1UF
10%
10V
X5R-CERM
0201

DEV_LEDS
CRITICAL
U9911
74LVC1G08
SOT891

72 68 60 19 IN PM_SLP_S0S3_L

PM_SLP_S0S3_BUFFLED_L

DEV_LEDS
R9924
470K
5%
1/20W
MF
201

NC

PROCHOT_LED

54 40 39 6 IN CPU_PROCHOT_L

DEV_LEDS
R9926
100K
5%
1/20W
MF
201

PROCHOT_LED_L

DEV_LEDS
Q9922
DST3904DJ
SOT963

PROCHOT IS ONLY VALID IN FULL S0, NOT S0I OR LOWER.

VF = 2V
IF = 1MA

DEV_LEDS Q9900 DMN5L06VK-7 SOT563 VER 5 — LED_PBUS
DEV_LEDS Q9900 DMN5L06VK-7 SOT563 VER 5 — LED_DCIN
DEV_LEDS Q9902 DMN5L06VK-7 SOT563 VER 5 — LED_G3H
DEV_LEDS Q9902 DMN5L06VK-7 SOT563 VER 5 — LED_DS5
DEV_LEDS Q9904 DMN5L06VK-7 SOT563 VER 5 — LED_S5
DEV_LEDS Q9904 DMN5L06VK-7 SOT563 VER 5 — LED_S4
DEV_LEDS Q9906 DMN5L06VK-7 SOT563 VER 5 — LED_S3
DEV_LEDS Q9906 DMN5L06VK-7 SOT563 VER 5 — LED_S0I
DEV_LEDS Q9908 DMN5L06VK-7 SOT563 VER 5 — LED_PLTRST
DEV_LEDS Q9908 DMN5L06VK-7 SOT563 VER 5 — LED_BKLT
DEV_LEDS Q9910 DMN5L06VK-7 SOT563 VER 5 — LED_CATERR
DEV_LEDS Q9910 DMN5L06VK-7 SOT563 VER 5 — LED_PROCHOT

DEV_LEDS LED9900 YELLOW-586NM-7.6MCD-1MA SML-P11-SM — LED_PBUS_R
DEV_LEDS LED9901 YELLOW-586NM-7.6MCD-1MA SML-P11-SM — LED_DCIN_R
DEV_LEDS LED9902 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_G3H_R
DEV_LEDS LED9903 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_DS5_R
DEV_LEDS LED9904 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_S5_R
DEV_LEDS LED9905 YELLOW-586NM-7.6MCD-1MA SML-P11-SM — LED_S4_R
DEV_LEDS LED9906 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_S3_R
DEV_LEDS LED9907 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_S0I_R
DEV_LEDS LED9908 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_PLTRST_R
DEV_LEDS LED9909 GREEN-569NM-2.1MCD-1MA SML-P11-SM — LED_BKLT_R
DEV_LEDS LED9910 RED-621NM-2.5MCD-1MA SML-P11-SM — LED_CATERR_R
DEV_LEDS LED9911 RED-621NM-2.5MCD-1MA SML-P11-SM — LED_PROCHOT_R

DEV_LEDS R9900 1.3K 5% 1/20W MF 201
DEV_LEDS R9901 1.3K 5% 1/20W MF 201
DEV_LEDS R9902 1.3K 5% 1/20W MF 201
DEV_LEDS R9903 1.3K 5% 1/20W MF 201
DEV_LEDS R9904 1.3K 5% 1/20W MF 201
DEV_LEDS R9905 1.3K 5% 1/20W MF 201
DEV_LEDS R9906 1.3K 5% 1/20W MF 201
DEV_LEDS R9907 1.3K 5% 1/20W MF 201
DEV_LEDS R9908 1.3K 5% 1/20W MF 201
DEV_LEDS R9909 1.3K 5% 1/20W MF 201
DEV_LEDS R9910 1.3K 5% 1/20W MF 201
DEV_LEDS R9911 1.3K 5% 1/20W MF 201

PP3V3_G3H 10 28 41 42 47 51 52 53 60 69 72
PP3V3_S5 44 58 60 61 63 64 68 69 72

BOM_COST_GROUP=DEBUG

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015
PAGE TITLE: DEVELOPMENT ONLY

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CPU RAILS

=PPVCC_S0_CPU	MAKE_BASE=TRUE	PPVCCCPU_S0G	45 55 63 72
=PPVCCSA_S0_CPU	MAKE_BASE=TRUE	PPVCCSA_S0G	56 72
=PPVCCGT_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
=PPVCCGTX_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
=PP1V2_S3_CPU_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP1V2_S3_CPU_VDDQC	MAKE_BASE=TRUE	=PP1V2_S3_CPU_VDDQ	8 10 69
=PP0V95_S0_CPU_VCCIO		PPVCCIO_S0G	61 63 72
=PP1V_S3_CPU_VCCST	MAKE_BASE=TRUE	PP1V_S3	64 69
=PP1V_S0_SMC_VCCST	MAKE_BASE=TRUE		
=PP1V_S0SW_CPU_VCCSTG		PP1V_S0G	64
=PP1V_S3_CPU_VCCPLL	MAKE_BASE=TRUE	PP1V_S3	64 69
=PP1V2_S0SW_CPU_VCCPLLOC	MAKE_BASE=TRUE	PP1V2_S0G	64
	MAKE_BASE=TRUE		

PCH RAILS

=PP3V_G3H_PCH_VCCRTC	MAKE_BASE=TRUE	PP3V1_RTC	61
=PP3V3_S5_PCH_VCCDSW	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP3V3_SUS_PCH_VCCPGPPA	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPC	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPD	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPE	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPG	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCSPI	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCRTCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP1V_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCMPHYAON	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK1	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK2_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK3	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK4_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK5_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK6	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCAPLL	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V8_SUS_PCH_VCCPGPPF	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
=PP1V8_SUS_PCH_VCCATS	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
=PP1V8_SUS_PCH_VCC1P8_SRC	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
=PPVCCPRIMECORE_SUS_PCH	MAKE_BASE=TRUE	PPVCCPCH_S5G	61 63 72
=PP1V_SUSSW_PCH_VCCAMPHYPLL_SRC	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V_SUSSW_PCH_VCCMPHYGT	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V_SUSSW_PCH_VCCSRAM	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V_SUSSW_PCH_VCCAPLLEBB	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V8_S0_PCH_VCCHDA	MAKE_BASE=TRUE	PP1V8_S0	48 50 51 60 63 64 67 72
=PP1V8R1V5_S0_PCH_VCCHDA			
=PP3V3_S0_PCH	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S4_PCH	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP3V3R1V8_S0_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69

SSD RAILS

=PP3V3_S5_SSD	MAKE_BASE=TRUE	PP3V3_S5_SSD_SNS	63
=PP3V3_S0_TBT_X_SNS		=PP3V3_TBT_X_S0	27 28

=PPBUS_G3H	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
=PPDCIN_G3H_SNS	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72
=PP5V_S5_LDO	MAKE_BASE=TRUE	PP5V_S5	63 64
=PP3V3_G3H_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP3V3_S5_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP3V3_S4_SMC	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP3V3_S0_SMC	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PPVIN_S5_SMCVREF	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP1V8_S3_MEM	MAKE_BASE=TRUE	PP1V8_S3	60 63 64
=PP1V2_S3_MEM_VDD2	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP1V2_S3_MEM_VDDCA	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP1V2_S3_MEM_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PPDDR_S3_MEMVREF	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP0V6_S0_MEM_VTT_A	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
=PP0V6_S0_MEM_VTT_B	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
PPVREF_S3_MEM_VREFDQ_A		PP0V6_S3_MEM_VREFDQ_A	21 22
PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_A	21 22
PPVREF_S3_MEM_VREFDQ_B	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_B	23 24
PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_B	23 24
	MAKE_BASE=TRUE		

CPU_VCCGTXSENSE_P	MAKE_BASE=TRUE	PU_VSNS_CPU_VCCGTX_TP	
CPU_VCCGTXSENSE_N	MAKE_BASE=TRUE	PD_VSNS_CPU_VCCGTX_TN	
=PP3V3_S0_CAMERA	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP5V_S0_ALSCAM	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PP3V3_S0_LCD	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S5_LCD	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP5V_S0_LCD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PP3V3_S0_BT_UART	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S4_BT_UART	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP3V3_G3H_KBD	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP3V3_S4_KBD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP5V_S0_KBD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PP3V3_S4_WLAN	MAKE_BASE=TRUE	PP3V3_S4_WLS	44 63 72
=PP3V3_S5_WIRELESS	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP3V3_S0_TPAD	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S4_TPAD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP5V_S4_TPAD	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
=PPBUS_S4_TPAD	MAKE_BASE=TRUE	PPBUS_G3H_TPAD	43
=PP1V_SUS_XDP		=PP1V_SUS_PCH_VCCPRIM	8 12 69
=PP3V3_SUS_XDP	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP5V_S0_BKLT	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PPVIN_S0SW_LCDBKLTFET	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
=PP5V_S0_FAN	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.0850
MIN_LINE_WIDTH=0.3000

USB-C GLOBAL POWER ALIASES

=PP3V3_UPC_XA_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XA_LDO	28 29
=PP3V3_UPC_XB_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XB_LDO	28 30 63
=PP3V3_S5_TBT_X	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP5V_XA_USBC	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
=PP5V_XB_USBC			
=PP5V_USBC			
=PPHV_EXT_G3H	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 19:33:56 2016

PAGE TITLE
Power Aliases

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UNUSED GPIOS, HSIO

9	IN	VCCPRIM_CORE_VID0	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID0
9	IN	VCCPRIM_CORE_VID1	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID1
16	IN	MLB_DEV_L	MAKE_BASE=TRUE	NO_TEST=1	NC_MLB_DEV_L
16	IN	I2C_UPC_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SDA
16	IN	I2C_UPC_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SCL
13	IN	PCH_BSSB_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_CLK
13	IN	PCH_BSSB_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_DATA
16	IN	TBT_X_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_X_DPMUX_SEL
16	IN	TBT_T_CIO_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CIO_PWR_EN
16	IN	TBT_T_USB_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_USB_PWR_EN
16	IN	TBT_T_PCI_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_PCI_RESET_L
16	IN	TBT_T_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_DPMUX_SEL
15	OUT	=TBT_T_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CLKREQ_L
15	IN	PCIE_CLK100M_TBT_T_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TN
15	IN	PCIE_CLK100M_TBT_T_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TP
15	OUT	PCIE_TBT_T_D2R_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN0
15	OUT	PCIE_TBT_T_D2R_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP0
15	IN	PCIE_TBT_T_R2D_C_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN0
15	IN	PCIE_TBT_T_R2D_C_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP0
15	OUT	PCIE_TBT_T_D2R_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN1
15	OUT	PCIE_TBT_T_D2R_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP1
15	IN	PCIE_TBT_T_R2D_C_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN1
15	IN	PCIE_TBT_T_R2D_C_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP1
15	BI	USB_CAMERA_DFR_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03N
15	BI	USB_CAMERA_DFR_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03P
13	IN	DEBUGUART_SEL_SOC	MAKE_BASE=TRUE	NO_TEST=1	NC_DEBUGUART_SEL_SOC
15	BI	USB3_EXTB_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RN
15	BI	USB3_EXTB_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RP
15	BI	USB3_EXTB_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCN
15	BI	USB3_EXTB_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCP
26	BI	=DP_X_SRC_ML_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CP<3..0>
26	BI	=DP_X_SRC_ML_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CN<3..0>
26	BI	=DP_X_SRC_AUX_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHP
26	BI	=DP_X_SRC_AUX_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHN
15	BI	USB_EXTA_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01N
15	BI	USB_EXTA_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01P

15	BI	NC_USB2_05N	NO_TEST=1
15	BI	NC_USB2_05P	NO_TEST=1
15	BI	NC_USB2_06N	NO_TEST=1
15	BI	NC_USB2_06P	NO_TEST=1
15	BI	NC_USB2_07N	NO_TEST=1
15	BI	NC_USB2_07P	NO_TEST=1
15	BI	NC_USB2_09N	NO_TEST=1
15	BI	NC_USB2_09P	NO_TEST=1
15	BI	NC_USB2_10N	NO_TEST=1
15	BI	NC_USB2_10P	NO_TEST=1

30	BI	NC_UPC_XB_I2C_ADDR	NO_TEST=1

GND
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.0850
VOLTAGE=0V

Digital Ground

MAKE_BASE

65	BI	=I2C_BKLT_SCL	TRUE	I2C_BKLT_SCL	BI	66 72
65	BI	=I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	BI	66 72

16	IN	TP_BT_I2S_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_CLK
16	IN	TP_BT_I2S_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_D2R
16	IN	TP_BT_I2S_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_R2D
16	IN	TP_BT_I2S_SYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_SYNC
36	IN	TP_CAM_GPIO3	MAKE_BASE=TRUE	NO_TEST=1	NC_CAM_GPIO3
6	IN	TP_CPU_AT5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AT5
6	IN	TP_CPU_AU5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AU5
6	IN	TP_CPU_AY4	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AY4
6	IN	TP_CPU_BB3	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB3
6	IN	TP_CPU_BB5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB5
59	IN	TP_CPU_MSM_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_MSM_L
9	IN	TP_CPU_NCTFVSS_A5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A5
9	IN	TP_CPU_NCTFVSS_A70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A70
9	IN	TP_CPU_NCTFVSS_AV1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_AV1
9	IN	TP_CPU_NCTFVSS_B71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_B71
9	IN	TP_CPU_NCTFVSS_BA1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA1
9	IN	TP_CPU_NCTFVSS_BA71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA71
9	IN	TP_CPU_NCTFVSS_BB70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BB70
9	IN	TP_CPU_NCTFVSS_C1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_C1
13	IN	TP_PCH_CLKOUT_LPC1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKOUT_LPC1
14	IN	TP_PCH_GPD7	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPD7
14	IN	TP_PCH_GPP_D0	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D0
16	IN	TP_PCH_GPP_D1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D1
16	IN	TP_PCH_GPP_D3	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D3
16	IN	TP_PCH_GPP_D4	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D4
5	IN	TP_PCH_GPP_E15	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_E15
14	IN	TP_PCH_GPP_F8	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F8
14	IN	TP_PCH_GPP_F9	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F9
14	IN	TP_PCH_GPP_F10	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F10
14	IN	PCH_BT_ROM_BOOT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F11
13	IN	PCH_SOC_DFU_STATUS	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F18
13	IN	SOC_PANIC_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F19
13	IN	SOC_S2R_ACK_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F20
13	IN	SOC_SLEEP_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F21
14	IN	TP_PCH_LANPHYPC	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_LANPHYPC
14	IN	TP_PCH_PME_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_PME_L
14	IN	TP_PCH_SLP_WLAN_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SLP_WLAN_L
13	IN	TP_PCH_STRP_ESPI	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_ESPI
13	IN	TP_PCH_STRP_TLSCONF	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_TLSCONF
60	IN	TP_PMIC_PGC	MAKE_BASE=TRUE	NO_TEST=1	NC_PMIC_PGC
13	IN	TP_SPI_CS1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS1_L
13	IN	TP_SPI_CS2_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS2_L
19	IN	TP_SYSCLK_CLK24M_SSD	MAKE_BASE=TRUE	NO_TEST=1	NC_SYSCLK_CLK24M_SSD
15	IN	TP_USB3_03_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RN
15	IN	TP_USB3_03_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RP
15	IN	TP_USB3_03_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DN
15	IN	TP_USB3_03_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DP
15	IN	TP_USB3_04_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RN
15	IN	TP_USB3_04_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RP
15	IN	TP_USB3_04_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DN
15	IN	TP_USB3_04_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DP
14	IN	PCH_SOC_FORCE_DFU	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_FORCE_DFU
13	OUT	PCH_SOC_WDOG	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_WDOG
14	OUT	UPC_I2C_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_I2C_INT_L
30	IN	TP_UPC_XB_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XB_SWD_DATA
29	IN	TP_UPC_XA_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_DATA
29	IN	TP_UPC_XA_SWD_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_CLK
15	IN	TP_PCIE_CLK100M5P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5P
15	IN	TP_PCIE_CLK100M5N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5N
15	IN	TP_PCH_CLKREQ5_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKREQ5_L
15	IN	TP_ITPXDP_CLK100MP	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MP
15	IN	TP_ITPXDP_CLK100MN	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MN
55	IN	TP_CPUVR_GH1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPUVR_GH1
6	IN	TP_CPU_RSVD_BB69	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB69
6	IN	TP_CPU_RSVD_BB68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB68
6	IN	TP_CPU_RSVD_BA70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA70
6	IN	TP_CPU_RSVD_BA68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA68
6	IN	TP_CPU_RSVD_AW71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW71
6	IN	TP_CPU_RSVD_AW70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW70
6	IN	TP_CPU_RSVD_AK12	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AK12
19	IN	TP_SPKR_ID0	MAKE_BASE=TRUE	NO_TEST=1	NC_SPKR_ID0
60	IN	TP_PGOOD_PVCCIO	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_PVCCIO
60	IN	TP_PGOOD_P1V00	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_P1V00
19	IN	TP_PCH_CLK32K_RTCX2	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK32K_RTCX2
19	IN	TP_PCH_CLK24M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK24M_XTALOUT
19	IN	TP_XDP_BPM_L<3>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<3>
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BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
NC_ AND NO_TEST SIGNALS

Apple Inc.

DRAWING NUMBER 051-02265 | SIZE D
REVISION 1.0.0
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SHEET 70 OF 73

Memory Bit/Byte Swizzle

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BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
Memory Signal Swaps

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
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XDP

17 4	B1	CPU_CFG<3>
17 4	B1	ITP_PMODE
17 15	B1	XDP_CPU_PRDY_L
17 15	B1	XDP_CPU_PREQ_L
17	B1	XDP_CPU_PWRBTN_L
17 4	B1	XDP_CPU_TCK
17 4	B1	XDP_CPU_TDI
17 4	B1	XDP_CPU_TDO
17 4	B1	XDP_CPU_TMS
17 4	B1	XDP_CPU_TRST_L
17	B1	XDP_DBRESET_L
17 4	B1	XDP_PCH_TCK
17 4	B1	XDP_PCH_TDI
17 4	B1	XDP_PCH_TDO
17 4	B1	XDP_PCH_TMS
17 4	B1	XDP_PCH_TRST_L
17	B1	XDP_PM_RSMRST_L
17	B1	XDP_PRESENT_CPU
60 17	B1	XDP_PRESENT_L

All: FUNC_TEST=TRUE

69 64 63 62 19	B1	PP1V_S5G
		GND

All: FUNC_TEST=TRUE

AUDIO FLEX

51	B2	AUD_CONN_HP_LEFT
51	B2	AUD_CONN_HP_RIGHT
51	B2	AUD_CONN_HP_SENSE_L
51	B2	AUD_CONN_HP_SENSE_R
51	B2	AUD_CONN_RING2
51	B2	AUD_CONN_RING2_XW
51	B2	AUD_CONN_SLEEVE
51	B2	AUD_CONN_SLEEVE_XW
51	B2	AUD_CONN_TIP_SENSE
51 48	B2	DMIC1_CLK
51 48	B2	DMIC1_DATA
51 43	B2	HALL_SENSOR_RIGHT

All: FUNC_TEST=TRUE

69 67 64 63 60 51 50 48	B2	PP1V8_S0
53 52 51 47 42 41 28 19 72 69 68 66	B2	PP3V3_G3H
		GND

All: FUNC_TEST=TRUE

LEFT SPEAKERS

51 48	B2	8409_SPKR_ID0
51 50	B2	SPKRCONN_FL_OUT_N
51 50	B2	SPKRCONN_FL_OUT_P
51 50	B2	SPKRCONN_RL_OUT_N
51 50	B2	SPKRCONN_RL_OUT_P

All: FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

RIGHT SPEAKERS

51 48	B2	8409_SPKR_ID1
51 50	B2	SPKRCONN_FR_OUT_N
51 50	B2	SPKRCONN_FR_OUT_P
51 50	B2	SPKRCONN_RR_OUT_N
51 50	B2	SPKRCONN_RR_OUT_P

All: FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

BATTERY

52	B2	SYS_DETECT_L
72 42	B2	SMBUS_SMC_5_G3H_SCL
72 42	B2	SMBUS_SMC_5_G3H_SCL

All: FUNC_TEST=TRUE

SMC

47 40 39 28	B2	SMC_TCK
40 39	B2	SMC_TDI
40 39	B2	SMC_TDO
47 40 39 28	B2	SMC_TMS
41	B2	SMC_DEV_SUPPLY_L

All: FUNC_TEST=TRUE

BOOTROM

47 16	B2	SPIROM_USE_MLB
47	B2	SPI_MLBROM_CS_L
47	B2	SPI_MLB_CLK
47	B2	SPI_MLB_CS_L
47	B2	SPI_MLB_IO<2>
47	B2	SPI_MLB_IO<3>
47	B2	SPI_MLB_MISO
47	B2	SPI_MLB_MOSI

All: FUNC_TEST=TRUE

USB2 FIXTURE PORT

15	B2	TP_USB_TESTERN
15	B2	TP_USB_TESTERP

All: FUNC_TEST=TRUE

69 64 63 60 58 54	B2	PP5V_S4
		GND

All: FUNC_TEST=TRUE

USB_TESTER_N — MAKE_BASE=TRUE, FUNC_TEST=TRUE — TP-P6 — TPA410

USB_TESTER_P — MAKE_BASE=TRUE, FUNC_TEST=TRUE — TP-P6 — TPA411

CRITICAL

DA410 ESD112-B1-02ELS 0201-THICKSTNCL

DA411 ESD112-B1-02ELS 0201-THICKSTNCL

CAP POWER DISCHARGE

69 68 63 60 58 53 50 43	B2	PPBUS_G3H
69 68 63 53	B2	PPDCIN_G3H
53 52	B2	PPDCIN_G3H_CHGR
72 66 65	B2	PPVOUT_S0_LCDBKLT

All: FUNC_TEST=TRUE

SYSTEM STATE

68 60 19	B2	PM_SLP_S0S3_L
60 39 18	B2	PM_SLP_S0_L
66 60 59 39 26 18	B2	PM_SLP_S3_L
68 60 39 18	B2	PM_SLP_S4_L
60 39 18	B2	PM_SLP_S5_L
60 18	B2	PM_SLP_SUS_L
41 39 17	B2	PM_PWRBTN_L
60 39	B2	ALL_SYS_PWRGD

All: FUNC_TEST=TRUE

MOJO PORT

40 39 28	B2	SMC_DEBUGPRT_TX_L
40 39 28	B2	SMC_DEBUGPRT_RX_L

All: FUNC_TEST=TRUE

MISC

67	B2	SSD_BOOT_CONN_L
14	B2	TP_PCH_SLP_A_L

All: FUNC_TEST=TRUE

CAMERA

36	B2	CAM_TEST_MODE
36	B2	TP_CAM_LV_JTAG_TCK
36	B2	TP_CAM_LV_JTAG_TDI
36	B2	TP_CAM_LV_JTAG_TDO
36	B2	TP_CAM_LV_JTAG_TMS
36	B2	TP_CAM_LV_JTAG_TRSTN
36	B2	TP_CAM_TEST_MODE0
36	B2	TP_CAM_TEST_MODE1
36	B2	TP_CAM_TEST_MODE2

All: FUNC_TEST=TRUE

DISPLAY

66 5	B2	DP_INT_HPD
66 5	B2	EDP_BKLT_PWM
66	B2	EDP_INT_AUX_N
66	B2	EDP_INT_AUX_P

All: FUNC_TEST=TRUE

66 5	B2	EDP_PANEL_PWR_EN
66	B2	I2C_ALS_SCL_CONN
66	B2	I2C_ALS_SDA_CONN
70 66	B2	I2C_BKLT_SCL
70 66	B2	I2C_BKLT_SDA
66	B2	I2C_CAM_SCL_CONN
66	B2	I2C_CAM_SDA_CONN
66	B2	I2C_TCON_SCL_CONN
66	B2	I2C_TCON_SDA_CONN
66	B2	LCD_IRQ_L
66 16	B2	MIPI_CLK_CONN_N
66 37	B2	MIPI_CLK_CONN_P
66 37	B2	MIPI_DATA_CONN_N
66 37	B2	MIPI_DATA_CONN_P
66 37	B2	TCON_BKLT_PWM
66 41	B2	PP3V3_S0SW_LCD
66	B2	PP5V_S0SW_LCD
66 37	B2	PP5V_S0_ALSCAM_F
72 66 65	B2	PPVOUT_S0_LCDBKLT

All: FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

USBC/TBT

28 26	B2	JTAG_TBT_TCK
28 26	B2	JTAG_TBT_TDI
28 26	B2	JTAG_TBT_X_TMS
26	B2	TBT_X_TEST_EN
31 28	B2	PP20V_USBC_XA_VBUS
32 28	B2	PP20V_USBC_XB_VBUS

All: FUNC_TEST=TRUE

POWER

69 67 64 61 59	B2	PP1V8_S5G
59	B2	PP1V_OPC_S0
69 63 44	B2	PP3V3_S4_WLS
69 68 64 63 61 60 58 44	B2	PP3V3_S5
69 64 60	B2	PP3V3_S5G
69 63 55 45	B2	PPVCCCPU_S0G
69 63 57 45	B2	PPVCCGT_S0G
69 63 61	B2	PPVCCIO_S0G
59	B2	PPVCCOPC_S0G
69 63 61	B2	PPVCCPCH_S5G
69 56	B2	PPVCCSA_S0G
69 62	B2	PPVTT_S0

All: FUNC_TEST=TRUE

WIRELESS

34	B2	JTAG_WLAN_SEL
34	B2	TP_JTAG_WLAN_TCK
34	B2	JTAG_WLAN_TDI
34	B2	TP_JTAG_WLAN_TDO
34	B2	TP_JTAG_WLAN_TMS
34	B2	TP_JTAG_WLAN_TRST

All: FUNC_TEST=TRUE

TRACKPAD AND KEYBOARD

39 38	B2	ACT_THERM_TRIP_L
38	B2	FAN_LT_PWM
38	B2	FAN_LT_TACH
38	B2	KBD_BLC_GSLAT
38	B2	KBD_BLC_GSSCK
38	B2	KBD_BLC_GSSIN
38	B2	KBD_BLC_GSSOUT
38	B2	KBD_BLC_XBLANK
38	B2	KBD_I2C_SCL
38	B2	KBD_I2C_SDA
38	B2	KBD_INT_L

All: FUNC_TEST=TRUE

38 16	B2	TPAD_SPI_MOSI
38 16	B2	TPAD_SPI_INT_L
38	B2	TPAD_SPI_CS_CONN_L
38 16	B2	TPAD_SPI_MISO
38 16	B2	TPAD_SPI_IF_EN
38 16	B2	TPAD_SPI_CLK

All: FUNC_TEST=TRUE

38	B2	TPAD_VIBE_L
38	B2	SMC_ESOD_RST
38	B2	KBD_ONOFF_L
41 40 39	B2	SMC_PME_S4_WAKE_L
68 60 53 52 51 47 42 41 28 19 72	B2	PP3V3_G3H
69 67 64 63 45 44 43 41	B2	PP3V3_S4
69 64 59 57 56 55 54	B2	PP5V_S0
38	B2	PP5V_S4_TPAD_CONN
38	B2	PPVIN_S4_TPAD_FUSE

All: FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

66 5	B1	EDP_ML_C_N<0..3>
66 5	B1	EDP_ML_C_P<0..3>
66	B1	EDP_INT_ML_N<0..3>
66	B1	EDP_INT_ML_P<0..3>
35 34	B1	PCIE_AP_D2R_C_N
35 34	B1	PCIE_AP_D2R_C_P
35 15	B1	PCIE_AP_D2R_N
35 15	B1	PCIE_AP_D2R_P
35 15	B1	PCIE_AP_R2D_C_N
35 15	B1	PCIE_AP_R2D_C_P
35 34	B1	PCIE_AP_R2D_N
35 34	B1	PCIE_AP_R2D_P

All: NO_TEST=1

67 15	B1	PCIE_SSD_D2R_N<0..3>
67 15	B1	PCIE_SSD_D2R_P<0..3>
67 15	B1	PCIE_SSD_R2D_C_N<0..3>
67 15	B1	PCIE_SSD_R2D_C_P<0..3>
67	B1	PCIE_SSD_R2D_N<0..3>
67	B1	PCIE_SSD_R2D_P<0..3>

All: NO_TEST=1

30	B1	USB_UPC_XB_F_N
30	B1	USB_UPC_XB_F_P

All: NO_TEST=1

31 26	B1	USBC_XA_D2R_N<1..2>
31 26	B1	USBC_XA_D2R_P<1..2>
31 26	B1	USBC_XA_R2D_C_N<1..2>
31 26	B1	USBC_XA_R2D_C_P<1..2>
31	B1	USBC_XA_R2D_N<1..2>
31	B1	USBC_XA_R2D_P<1..2>
29 28	B1	USBC_XA_USB_BOT_N
29 28	B1	USBC_XA_USB_BOT_P
29 28	B1	USBC_XA_USB_TOP_N
29 28	B1	USBC_XA_USB_TOP_P
32 26	B1	USBC_XB_D2R_N<1..2>
32 26	B1	USBC_XB_D2R_P<1..2>
32 26	B1	USBC_XB_R2D_C_N<1..2>
32 26	B1	USBC_XB_R2D_C_P<1..2>
32	B1	USBC_XB_R2D_N<1..2>
32	B1	USBC_XB_R2D_P<1..2>
32 30	B1	USBC_XB_USB_BOT_N
32 30	B1	USBC_XB_USB_BOT_P
32 30	B1	USBC_XB_USB_TOP_N
32 30	B1	USBC_XB_USB_TOP_P

All: NO_TEST=1

55	B1	AGND_U7320
	B1	BANJO_VBSTVR1
	B1	BANJO_VBSTVR3
62	B1	BANJO_VBSTVR4
61	B1	BANJO_VBSTVR5
55	B1	CPUVR_BP2
55	B1	CPUVR_PHASE2
55	B1	CPUVR_SNB1
55	B1	CPUVR_SNB2
59	B1	PD_VSNS_CPU_VCCEOPIO_TN
59	B1	PD_VSNS_CPU_VCCOPC_TN
55	B1	PPVCCCPU_S0G_PH1
55	B1	PPVCCCPU_S0G_PH2
56	B1	PPVCCSA_S0G_R
59	B1	PU_VSNS_CPU_VCCEOPIO_TP
59	B1	PU_VSNS_CPU_VCCOPC_TP
27	B1	VR0V9_IND_TBT_X
12	B1	PP1V_SUS_PCH_VCCAPLL_F
12	B1	PP1V8_S0_PCH_VCCHDA_F

All: NO_TEST=1

FOR DC/DC

53	B1	TBA_HPWR_EN_L
53	B1	PD_TBA_MPM_DET

All: FUNC_TEST=TRUE

FOR DEBUG

29	B1	TP_UPC_XA_DBG_UART_TX
29	B1	TP_UPC_XA_DBG_UART_RX
30	B1	TP_UPC_XB_DBG_UART_TX
30	B1	TP_UPC_XB_DBG_UART_RX

All: FUNC_TEST=TRUE

25 21 7	B1	MEM_A_CAA<0..9>
25 22 7	B1	MEM_A_CAB<0..9>
25 22 21 7	B1	MEM_A_CKE<0..3>
25 22 21 7	B1	MEM_A_CLK_N<0..1>
25 22 21 7	B1	MEM_A_CLK_P<0..1>
25 22 21	B1	MEM_A_CS_L<0..1>
71 7	B1	MEM_A_DQ<0..63>
71 7	B1	MEM_A_DQS_N<0..7>
71 7	B1	MEM_A_DQS_P<0..7>
25 22 21 7	B1	MEM_A_ODT<0>

All: NO_TEST=1

25 23 7	B1	MEM_B_CAA<0..9>
25 24 7	B1	MEM_B_CAB<0..9>
25 24 23 7	B1	MEM_B_CKE<0..3>
25 24 23 7	B1	MEM_B_CLK_N<0..1>
25 24 23 7	B1	MEM_B_CLK_P<0..1>
25 24 23 7	B1	MEM_B_CS_L<0..1>
71 7	B1	MEM_B_DQ<0..63>
71 7	B1	MEM_B_DQS_N<0..7>
71 7	B1	MEM_B_DQS_P<0..7>
25 24 23 7	B1	MEM_B_ODT<0>

All: NO_TEST=1

37 36	B1	MEM_CAM_A<0..14>
37 36	B1	MEM_CAM_BA<0..2>
37 36	B1	MEM_CAM_DM<0..1>
37 36	B1	MEM_CAM_DQ<0..15>
37 36	B1	MEM_CAM_DQS_N<0..1>
37 36	B1	MEM_CAM_DQS_P<0..1>
34	B1	RF_0_ANT
34	B1	RF_0_ANT_MATCH_T
34	B1	RF_1_ANT
34	B1	RF_1_ANT_MATCH_T
34	B1	RF_A_0_DIPLEXER
34	B1	RF_A_0_MATCH
34	B1	RF_A_1_DIPLEXER
34	B1	RF_A_1_MATCH
34	B1	RF_G_0_DIPLEXER
34	B1	RF_G_0_MATCH
34	B1	RF_G_1_DIPLEXER
34	B1	RF_G_1_MATCH
55	B1	AGND_U7310

All: NO_TEST=1

61	B1	BANJO_FBVR2_N
61	B1	BANJO_FBVR2_RC
61	B1	BANJO_SWVR2
61	B1	BANJO_SWVR2_SNUB
61	B1	BANJO_SWVR3R
61	B1	BANJO_SWVR3_SNUB
62	B1	BANJO_VBSTVR1_R
61	B1	BANJO_VBSTVR3_R
62	B1	BANJO_VBSTVR4_R
61	B1	BANJO_VBSTVR5_R
55	B1	CPUVR_BOOT1
55	B1	CPUVR_BP1
55 45	B1	CPUVR_ISNS2_N
55 45	B1	CPUVR_ISNS2_P
55	B1	CPUVR_PHASE1
55	B1	CPUVR_SW1
6	B1	CPU_PROCHOT_R_L
54 6	B1	CPU_VCCGTSENSE_N
14	B1	CPU_VCCST_PWRGD_R
57	B1	GTVR_BP1
57 45	B1	GTVR_ISNS2_P
57	B1	GTVR_SNB1
57	B1	GTVR_SNB2
57	B1	GTVR_SNB3
57	B1	GTVR_SW1
57	B1	GTVR_SW2
59	B1	P1VOPC_BOOT_RC
59	B1	P1VOPC_DRVH_R
59	B1	P1VOPC_REFIN_R
59	B1	P1VOPC_SNS_R
59	B1	P3V3S5_DRVH_R
59	B1	P5VS4_DRVH_R
59	B1	SAVR_BP
59	B1	SAVR_SNB1
59	B1	SAVR_SW
72 55	B1	VCINP_P5V_U7310

All: NO_TEST=1

56	B1	AGND_U7470
72 55	B1	VCINP_P5V_U7310
55	B1	VCINP_P5V_U7320
53	B1	TBA_PHASE1
69	B1	PMIC_ENH

All: NO_TEST=1

BOM_COST_GROUP=NO COST ITEMS

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

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