

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X941 MLB SCHEMATIC

LAST_MODIFICATION=Wed Jan 10 14:52:52 2018


REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
4	0010936498	ENGINEERING RELEASED		2018-01-10

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02166	1	SCHEM,MLB,X941	SCH	CRITICAL	SCH
820-00850	1	PCBF,MLB,X941	PCB	CRITICAL	PCB

DRAWING TITLE		SCHEM,MLB,X941	
 Apple Inc.		DRAWING NUMBER	051-02166
		REVISION	4.0.0
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BOM GROUP	BOM OPTIONS
X941_COMMON	SCH,PCB,ALTERNATE,COMMON,X941_COMMON1,X941_COMMON2,X941_COMMON3,X941_PROGPARTS
X941_COMMON1	TBT_TR<C1,ACE:C0_NFBGA,SE:DEV_2017,PBUS:3S,SYSDET:FET,TBTTRM_SNS,BOARD_ID,BOARD_REV:100,RF_DOE
X941_COMMON2	EDP_ENABLE,XDP:YES,SKIP_SV3V3-AUDIBLE
X941_COMMON3	LOADRC:YES
X941_PROGPARTS	TBT_LT_ROM:EVT,TBT_RT_ROM:EVT,WIFI_ROM:P0,BT_ROM:EVT
X941_DEVEL:ENG	ALTERNATE,ESPI_DBG,DBGLED,SOC_DBG,USBC_DBG,XDP_CONN:YES,WIFI_DBG,SSD_DBG,DBG_FAN,DEBUG_BUTTON,LOADISMS,AP_TEMP:YES,SENSOR:DEV,BOOTCFG0
X941_DEVEL:DVT	ALTERNATE,SOC_DBG,USBC_DBG,XDP_CONN:YES,WIFI_DBG
X941_DEVEL:PVT	ALTERNATE

Variable BOM Groups
Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00187	1	COMMON PARTS,MLB,X941	BASE	CRITICAL	BASE_BOM
985-00366	1	DEV,MLB,X941	DEVEL	CRITICAL	DEVEL_BOM

NAND Configs

BOM GROUP	BOM OPTIONS
NANDCFG:SD_256G	NAND:SD_256G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:TO_256G	NAND:TO_256G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:SD_512G	NAND:SD_512G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:TO_512G	NAND:TO_512G,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:SD_1T	NAND:SD_1T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:SS_1T	NAND:SS_1T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:TO_1T	NAND:TO_1T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:SS_2T	NAND:SS_2T,SOC:B0_2G,NAND_VCC:2.5V
NANDCFG:SS_2T_DOE	NAND:SS_2T_DOE,SOC:B0_2G,NAND_VCC:2.7V
NANDCFG:SD_256G_DOE	NAND:SD_256G_DOE,SOC:B0_1G,NAND_VCC:2.5V
NANDCFG:TO_256G_DOE	NAND:TO_256G_DOE,SOC:B0_1G,NAND_VCC:2.5V

Main DRAM SPD Straps


BOM GROUP	BOM OPTIONS
DRAMCFG:HY_8G	DRAM:HY_8G,DRAMCFG4_L,DRAMCFG3_L,DRAMCFG2_L,DRAMCFG1_L,DRAMCFG0_L
DRAMCFG:MI_8G	DRAM:MI_8G,DRAMCFG4_L,DRAMCFG3_L,DRAMCFG2_L,DRAMCFG1_L
DRAMCFG:SS_8G	DRAM:SS_8G,DRAMCFG3_L,DRAMCFG2_L,DRAMCFG0_L
DRAMCFG:HY_16G	DRAM:HY_16G,DRAMCFG4_L,DRAMCFG3_L,DRAMCFG1_L,DRAMCFG0_L
DRAMCFG:MI_16G	DRAM:MI_16G,DRAMCFG4_L,DRAMCFG3_L,DRAMCFG1_L
DRAMCFG:SS_16G	DRAM:SS_16G,DRAMCFG3_L,DRAMCFG0_L

CPU DRAM CFG Chart

DIE REV	CFG 4	VENDOR	CFG 1	CFG 0
A	0	HYNIX	0	0
B	1	MICRON	0	1
		SAMSUNG	1	0
		N/A	1	1

SPEED	CFG 3
2133	0
1866	1

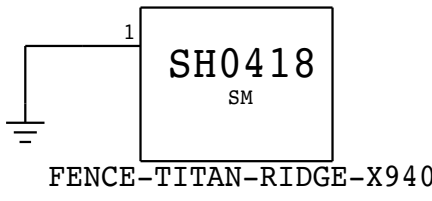
CAPACITY	CFG 2
8GB	0
16GB	1

PAGE TITLE		BOM Configuration	
 Apple Inc.	DRAWING NUMBER	051-02166	SIZE
	REVISION	4.0.0	D
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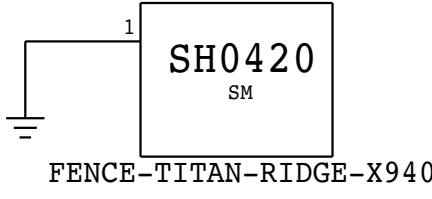
BOARD MECHANICALS

Shield Cans - BOTTOM SIDE

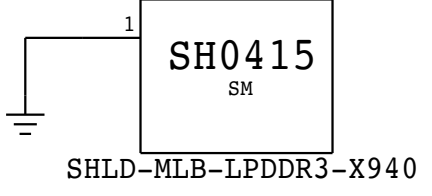
TITAN RIDGE - LEFT (U2800) - 806-12859



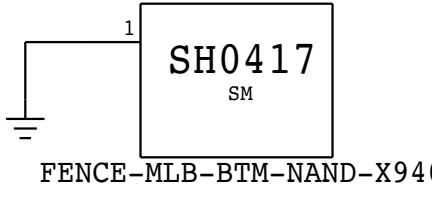
TITAN RIDGE - RIGHT (UB000) - 806-12859



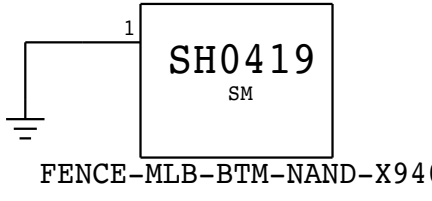
LPDDR3 (U2300 ~ U2600) - 806-15451



NAND - BOTTOM SOUTH (U8700) - 806-12858

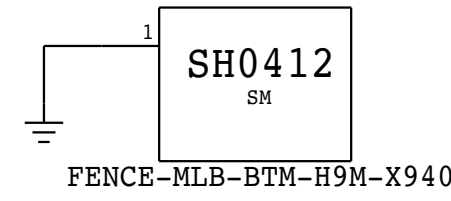


NAND - BOTTOM NORTH (U8900) - 806-12858

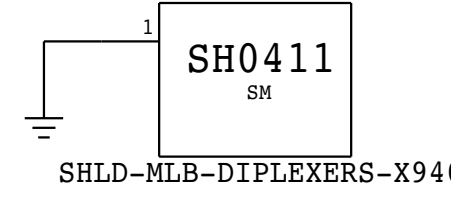


Shield Cans - TOP SIDE

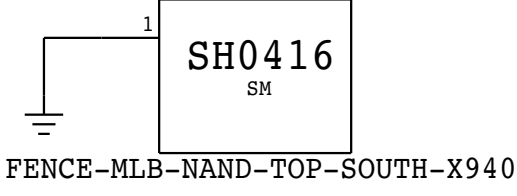
SOC (U3900) - 806-12855



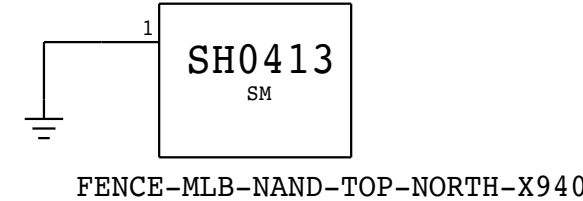
DIPLEXERS - 806-12854



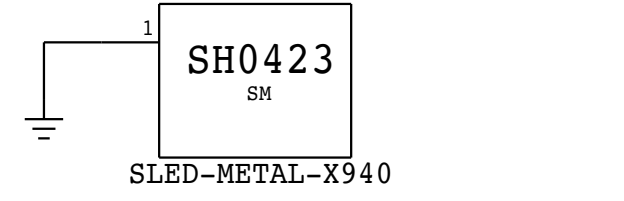
NAND - TOP SOUTH (U8600) - 806-12857



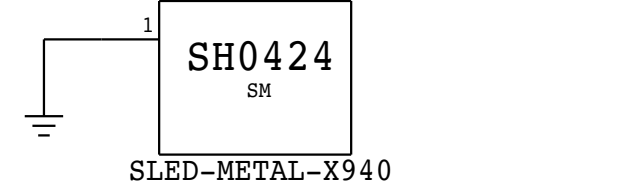
NAND - TOP NORTH (U8800) - 806-12856



CPU SLED (U0500) - 806-12626

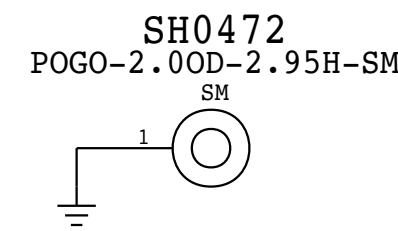
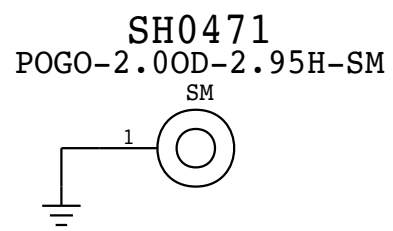


CPU SLED (U0500) - 806-12626

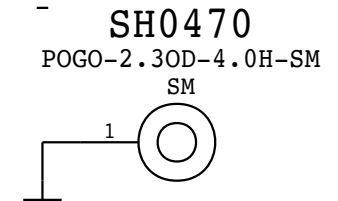
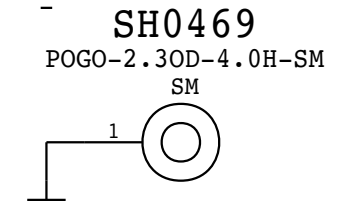
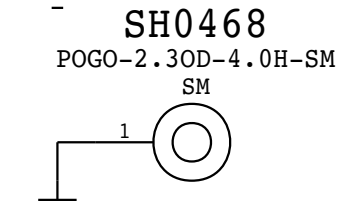
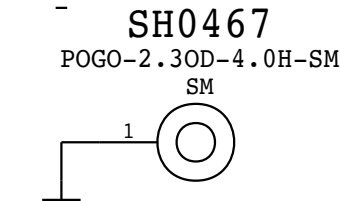
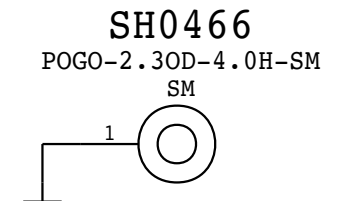
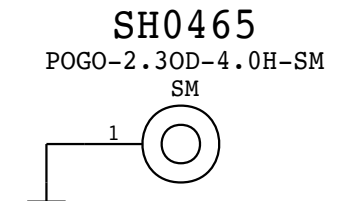
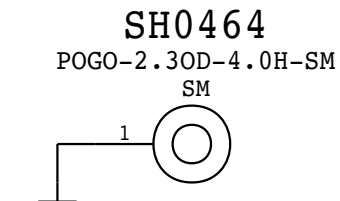
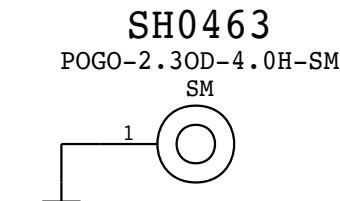


POGO PINS

LIO and RIO -2X (870-5071)

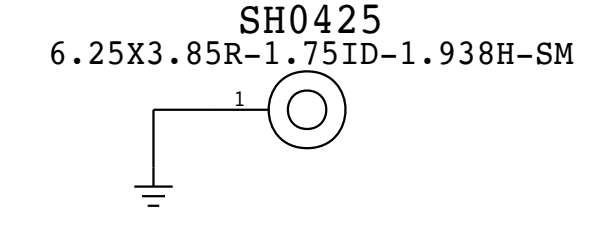


AROUND THE FAN AND CENTER - 8X (870-01518)

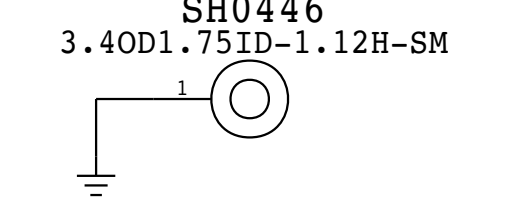
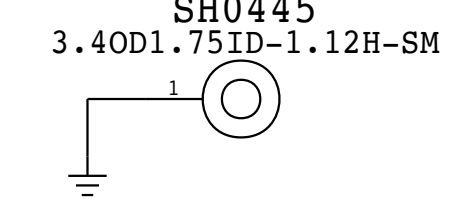


Cowling Bosses - BOTTOM SIDE

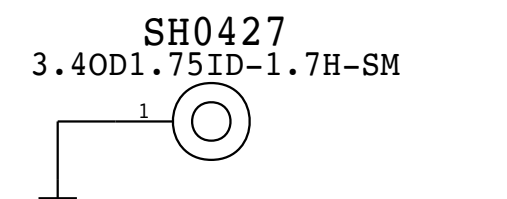
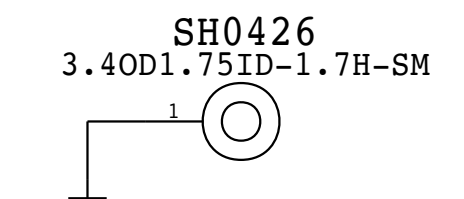
DFR TOUCH CONN (J4402) - 860-00414



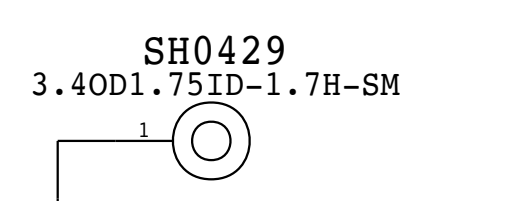
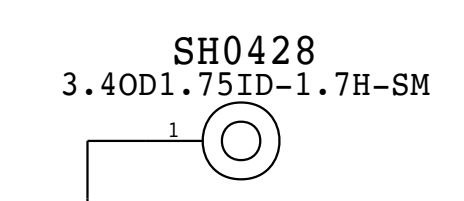
USB-C CONN - LIO (J3300) - 860-00392



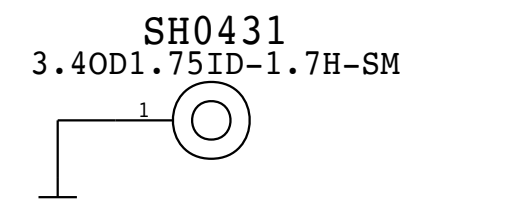
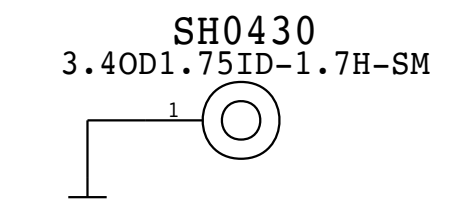
DFR DISPLAY CONN (J4401) - 860-00412



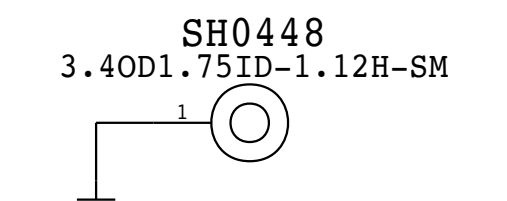
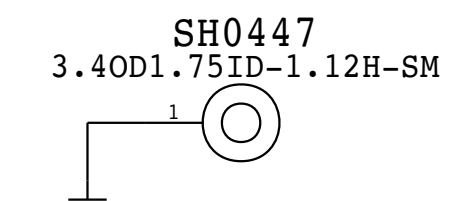
IPD CONN (J4501) - 860-00412



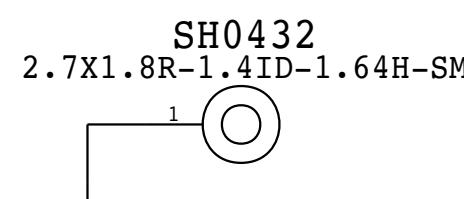
KBD CONN (J4500) - 860-00412



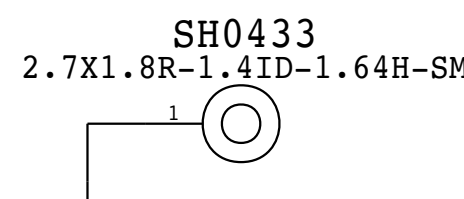
USB-C CONN - RIO (JB500) - 860-00392



AUDIO JACK CONN (J6600) - 860-00829

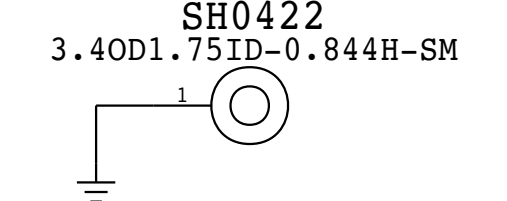
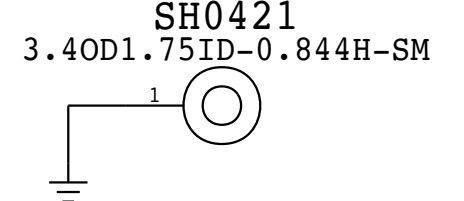


MESA CONN (J4900) - 860-00829



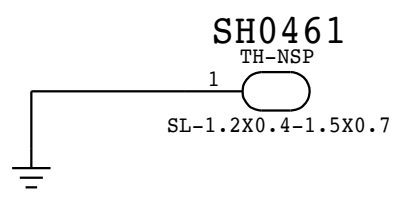
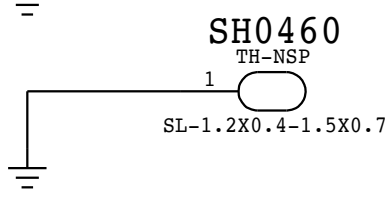
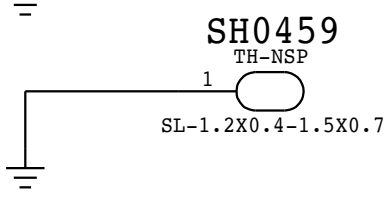
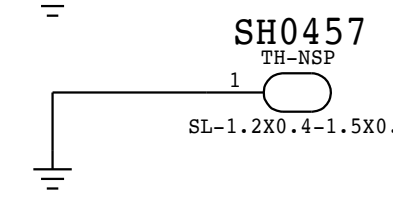
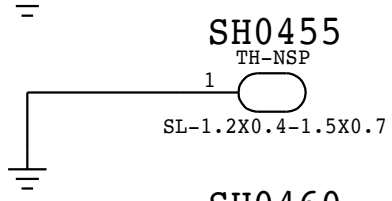
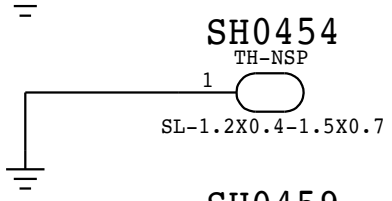
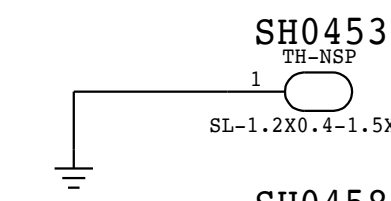
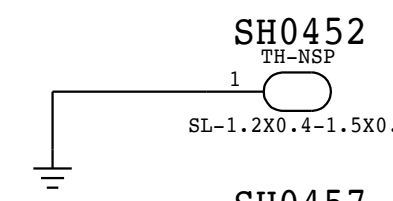
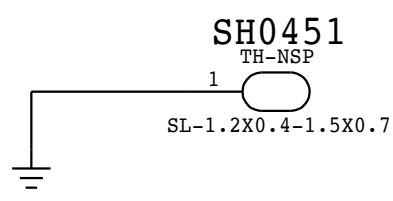
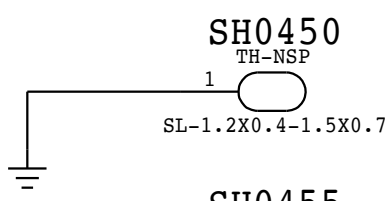
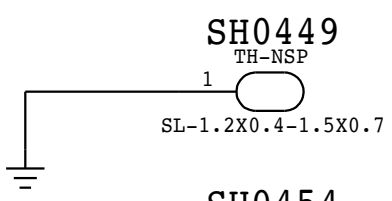
Cowling Bosses - TOP SIDE

eDP CONN (J8500) - 860-00415



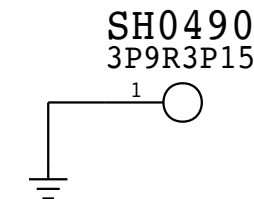
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Shield CAN Alignment Slots 14X - 998-04440 (1.2mm X 0.4mm)

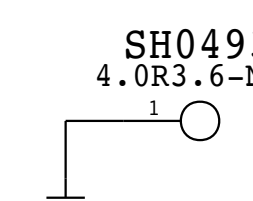
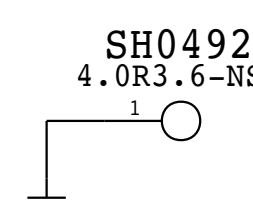
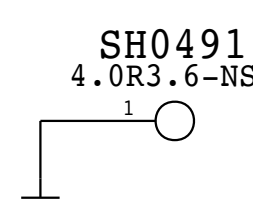


Thermal Stage Mounting Holes

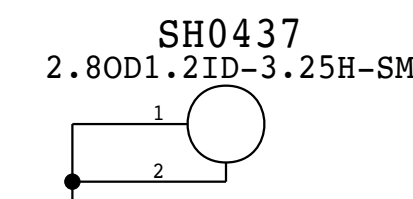
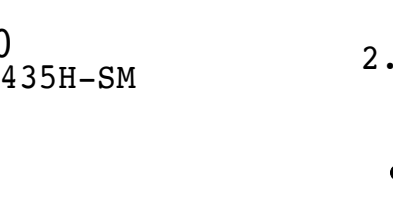
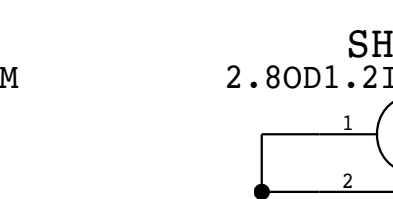
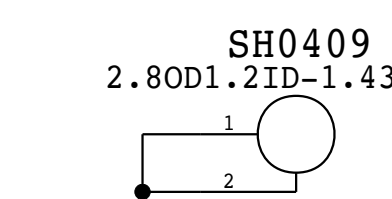
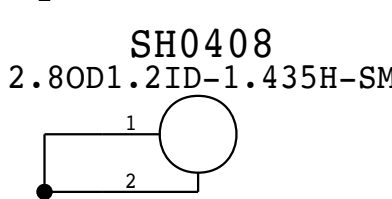
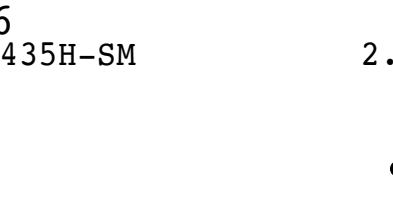
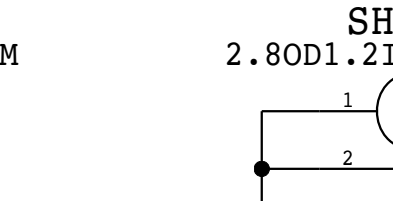
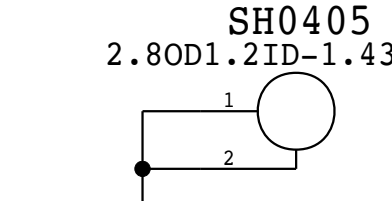
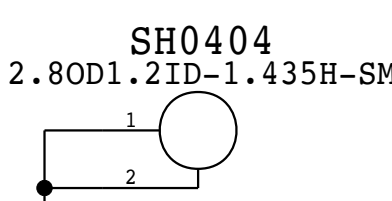
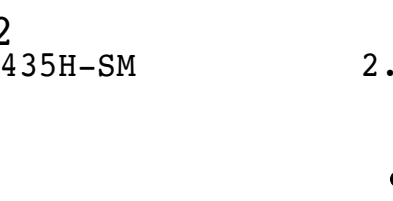
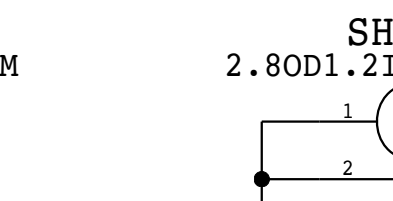
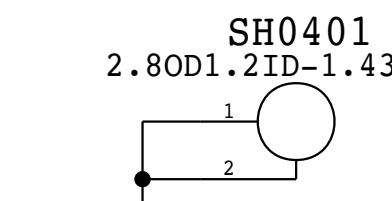
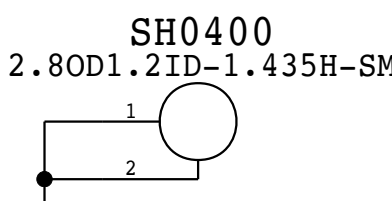
Plated Through Hole - 3.15mm - APN 998-0845



Plated Through Hole - 3.6mm - APN 998-03850



TOP Rubber Mount Standoffs - 12X - (860-00430)



Bottom Rubber Mount Standoffs - 1X - (860-00476)

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		PAGE	4 OF 150
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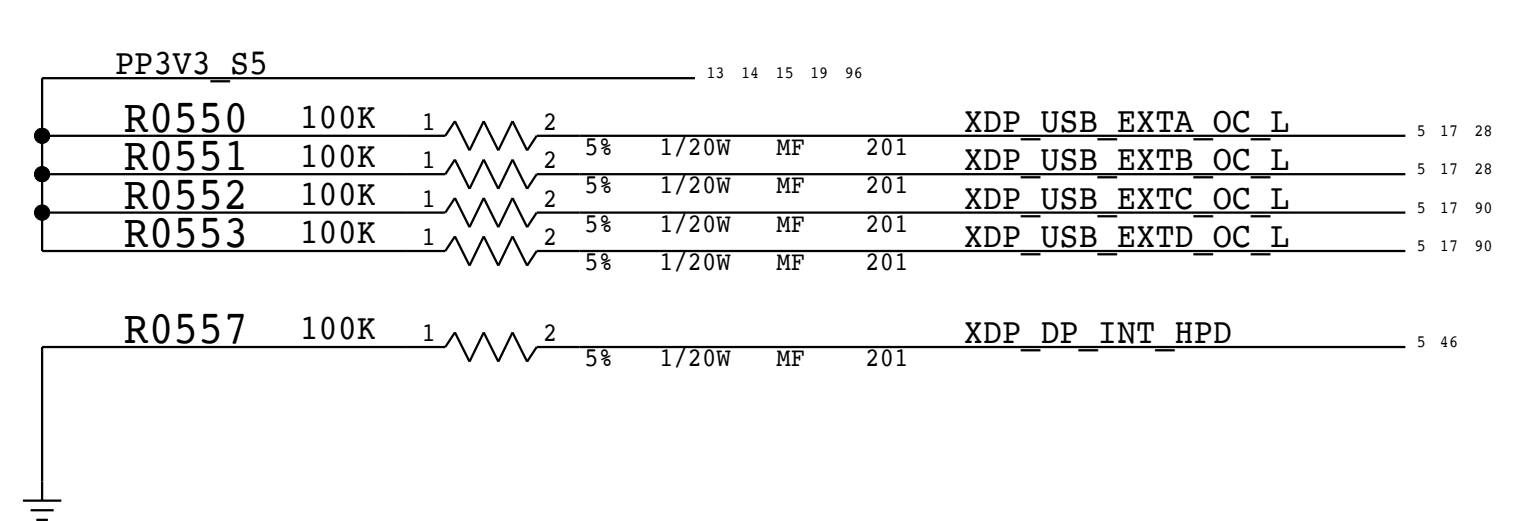
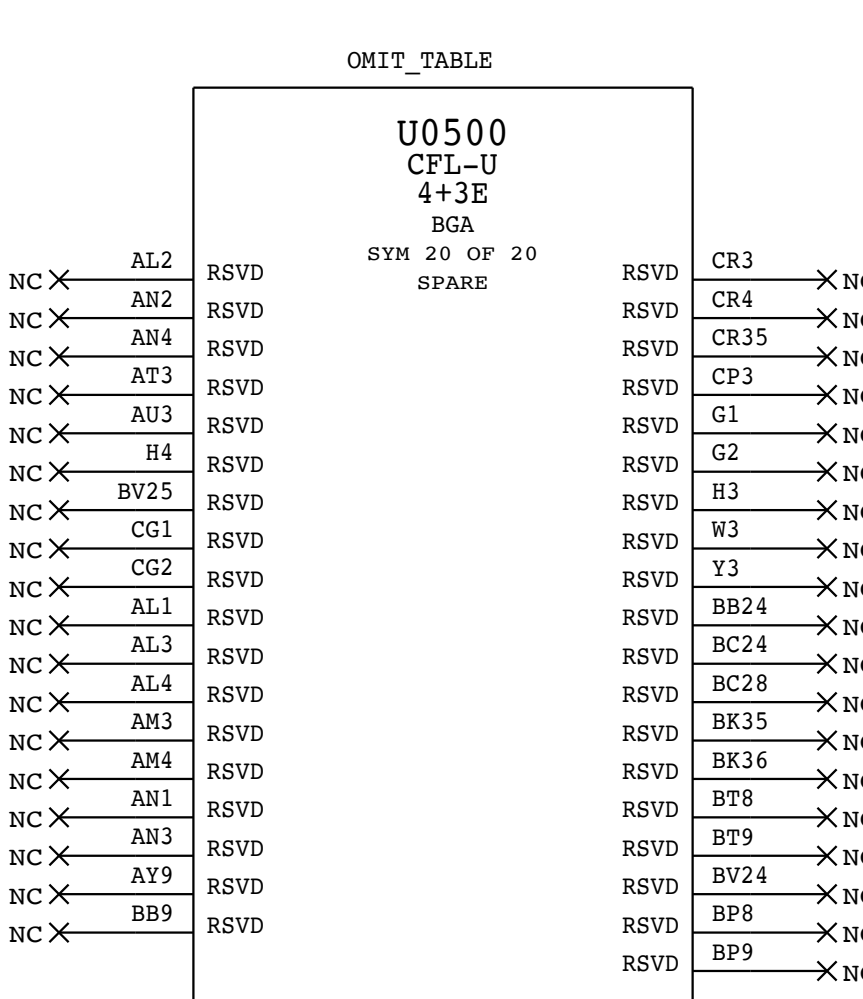
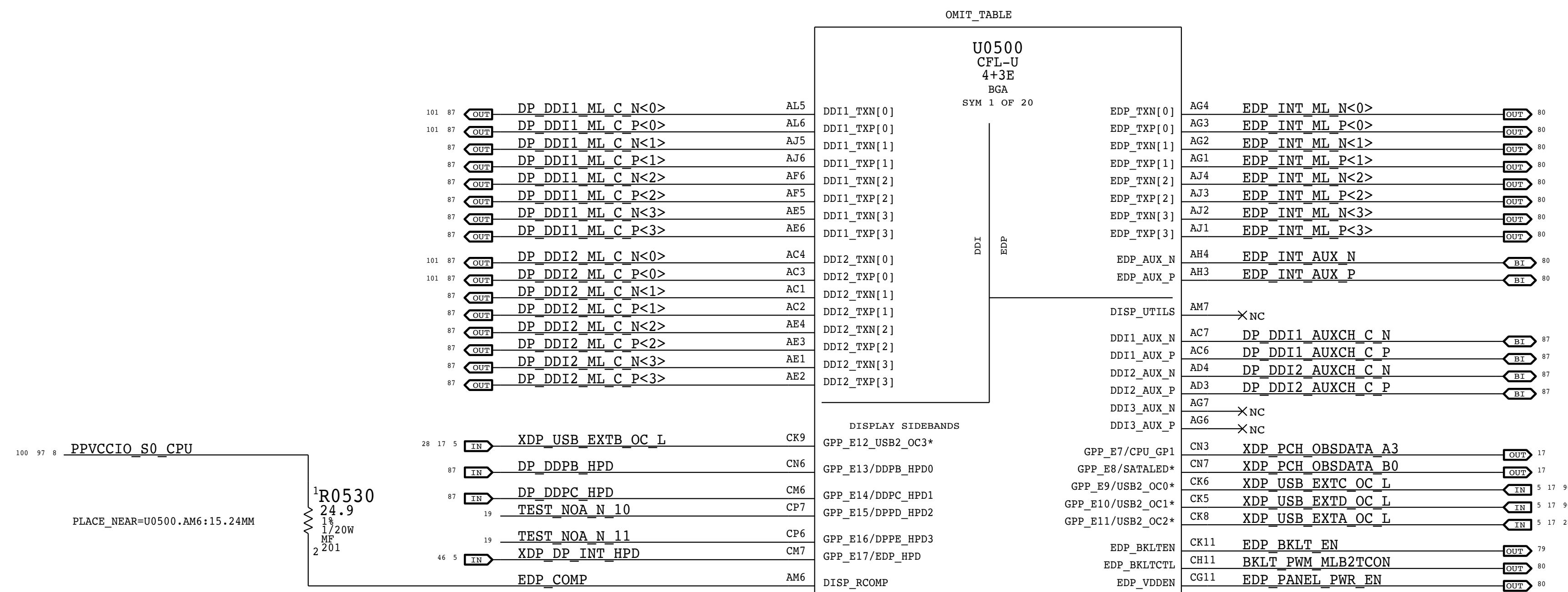
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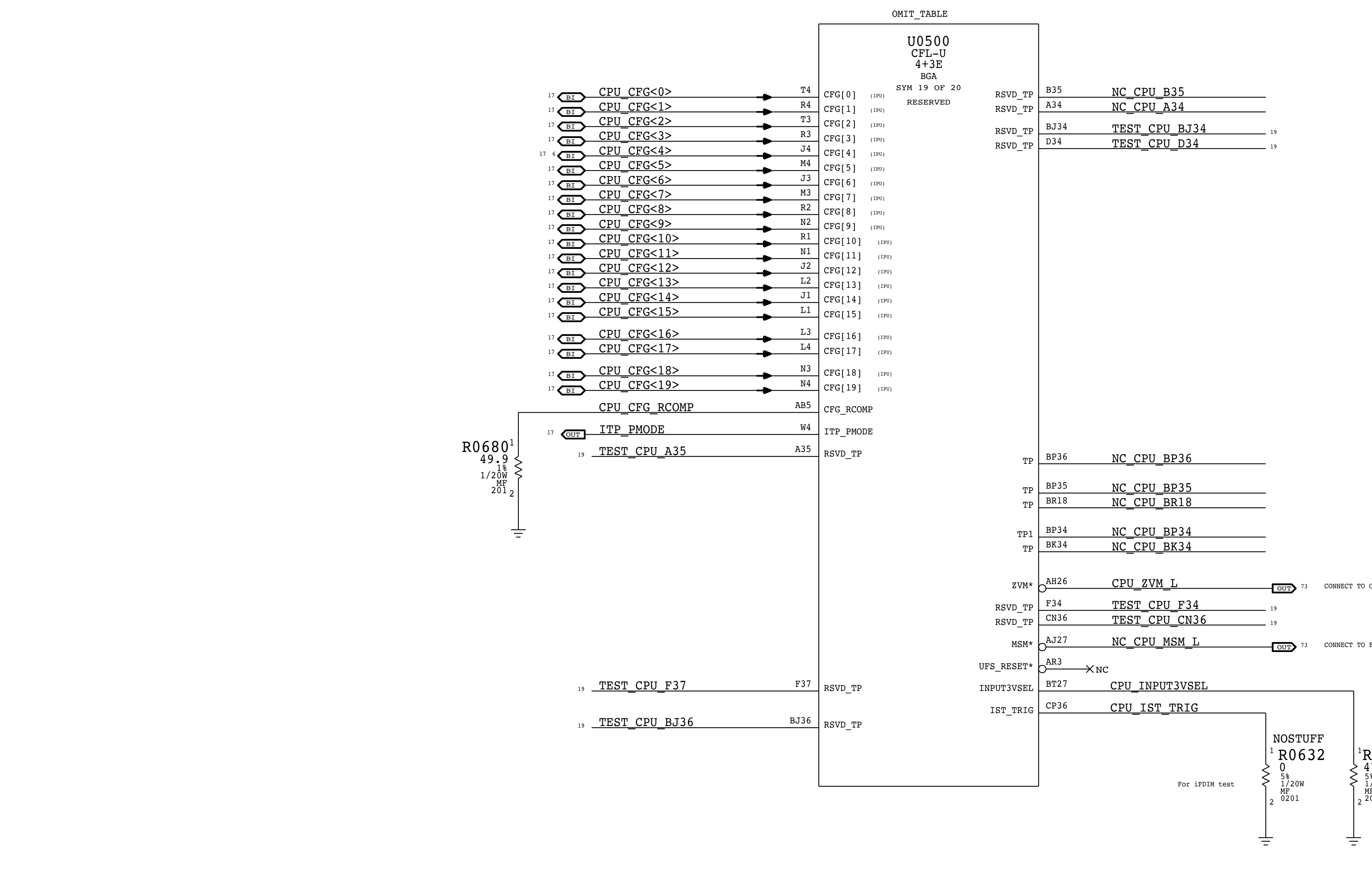
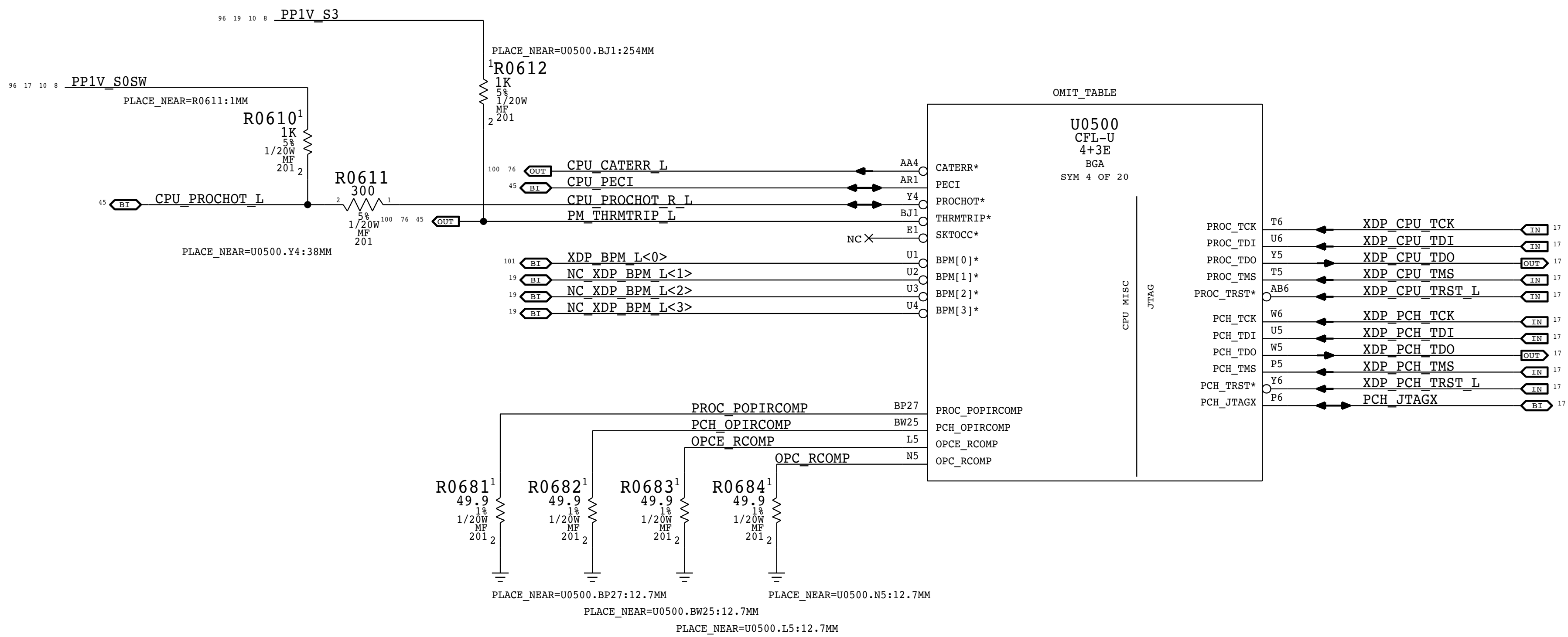
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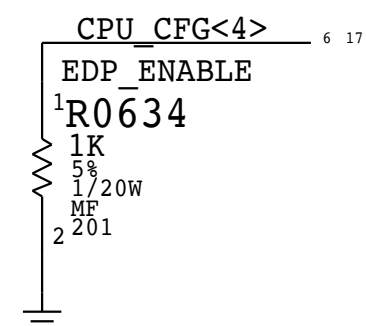


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	SHEET	5 OF 108



CFG<>: 1=EDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED



BOM_COST_GROUP=CPU & CHIPSET

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LAST CHANGE: Mon Apr 27 22:56:39 2015	
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DRAWING NUMBER 051-02166	SIZE D
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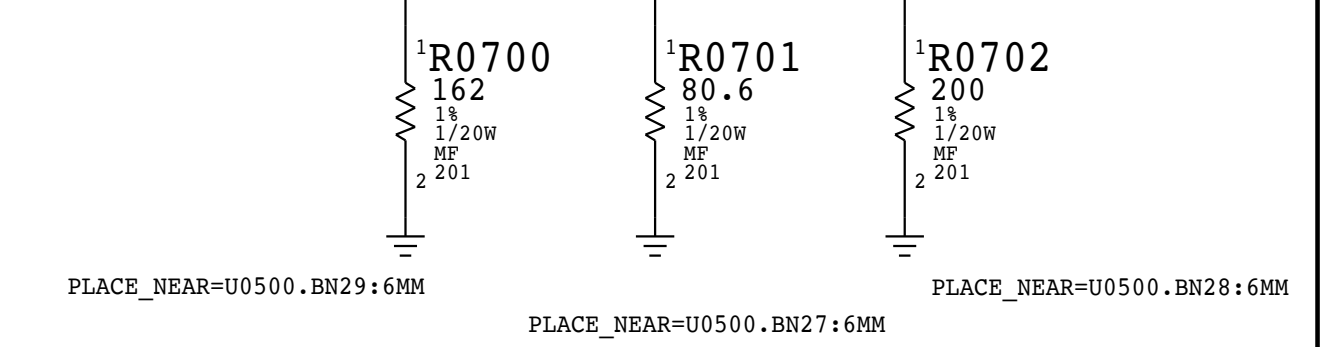
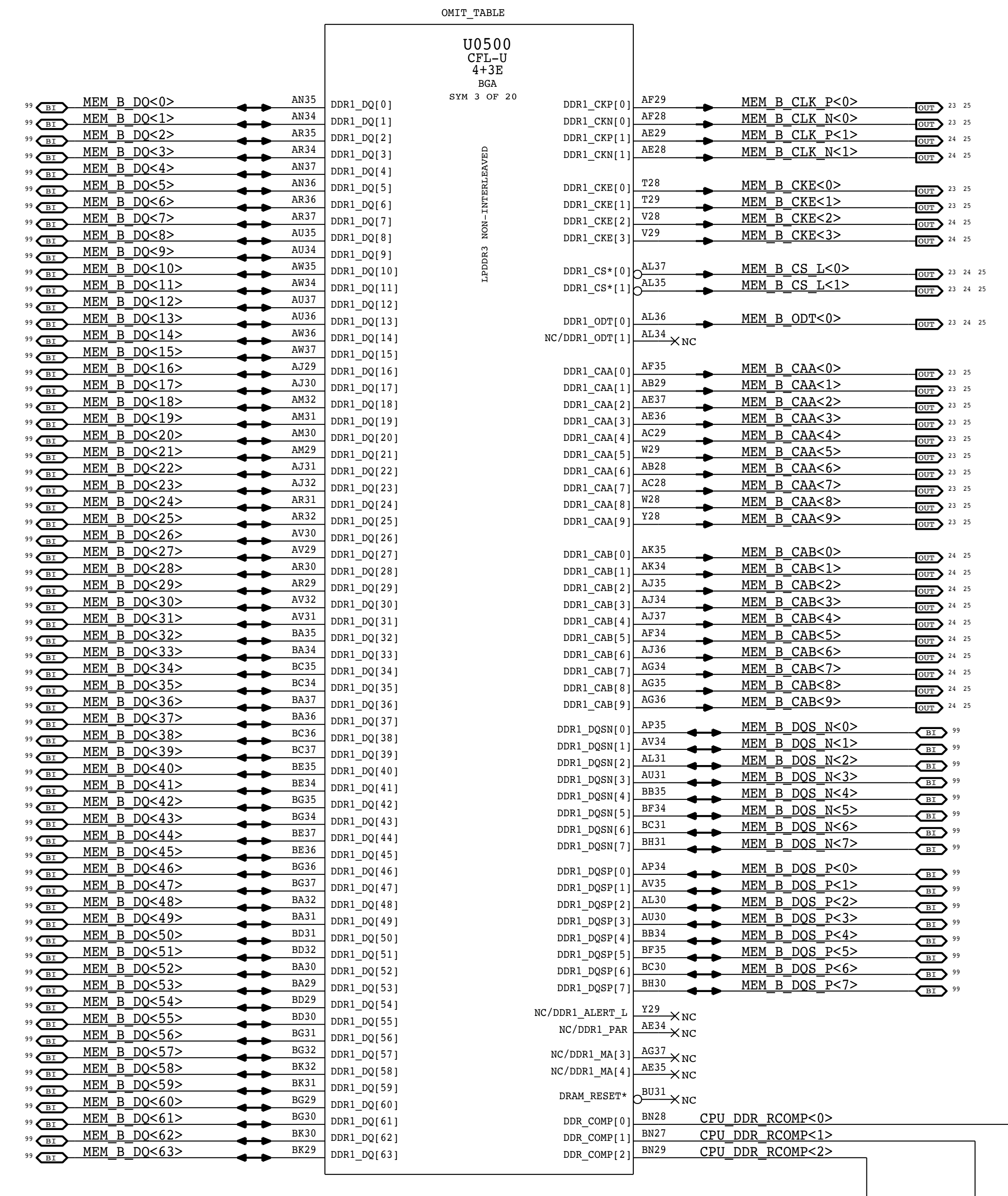
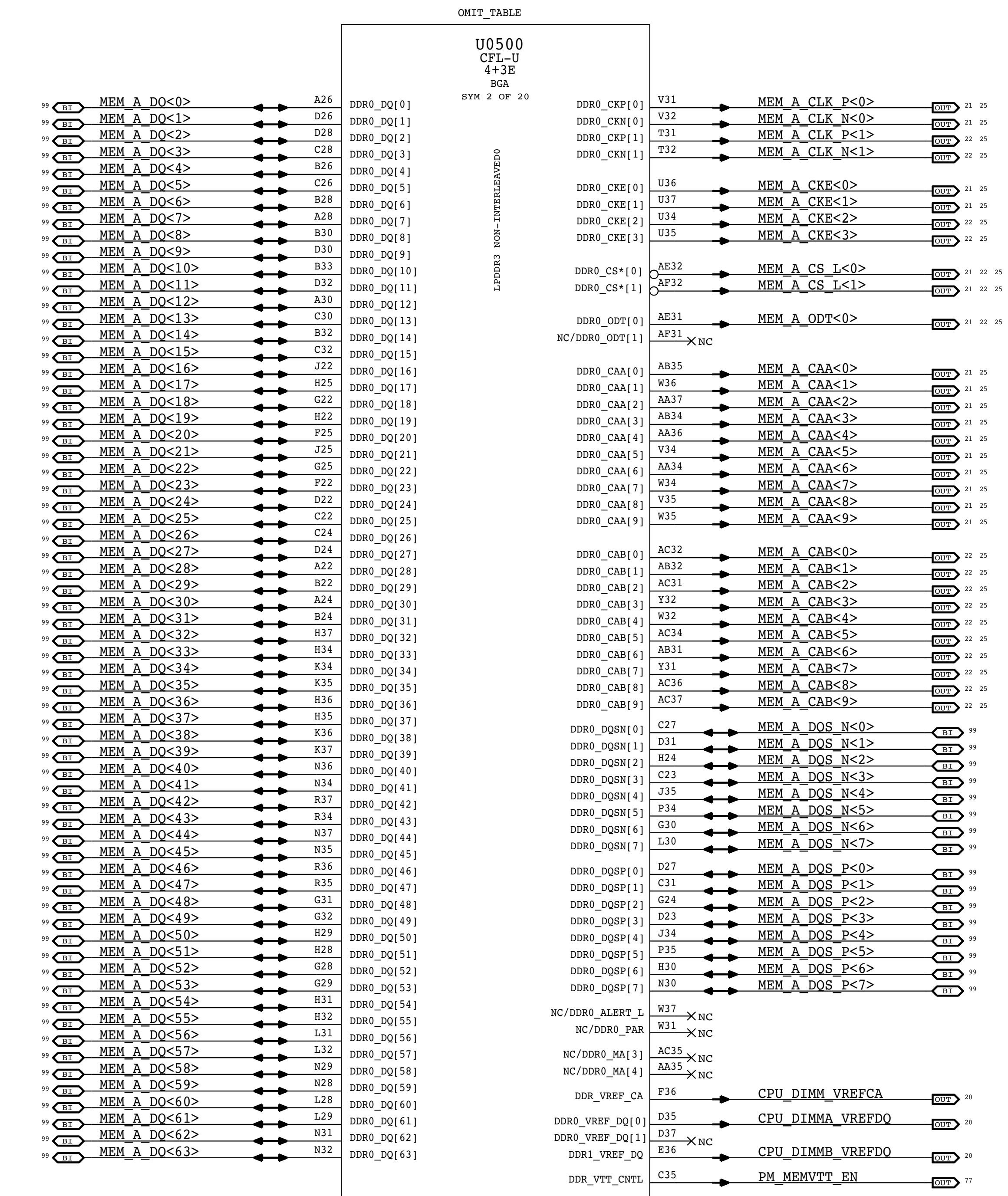
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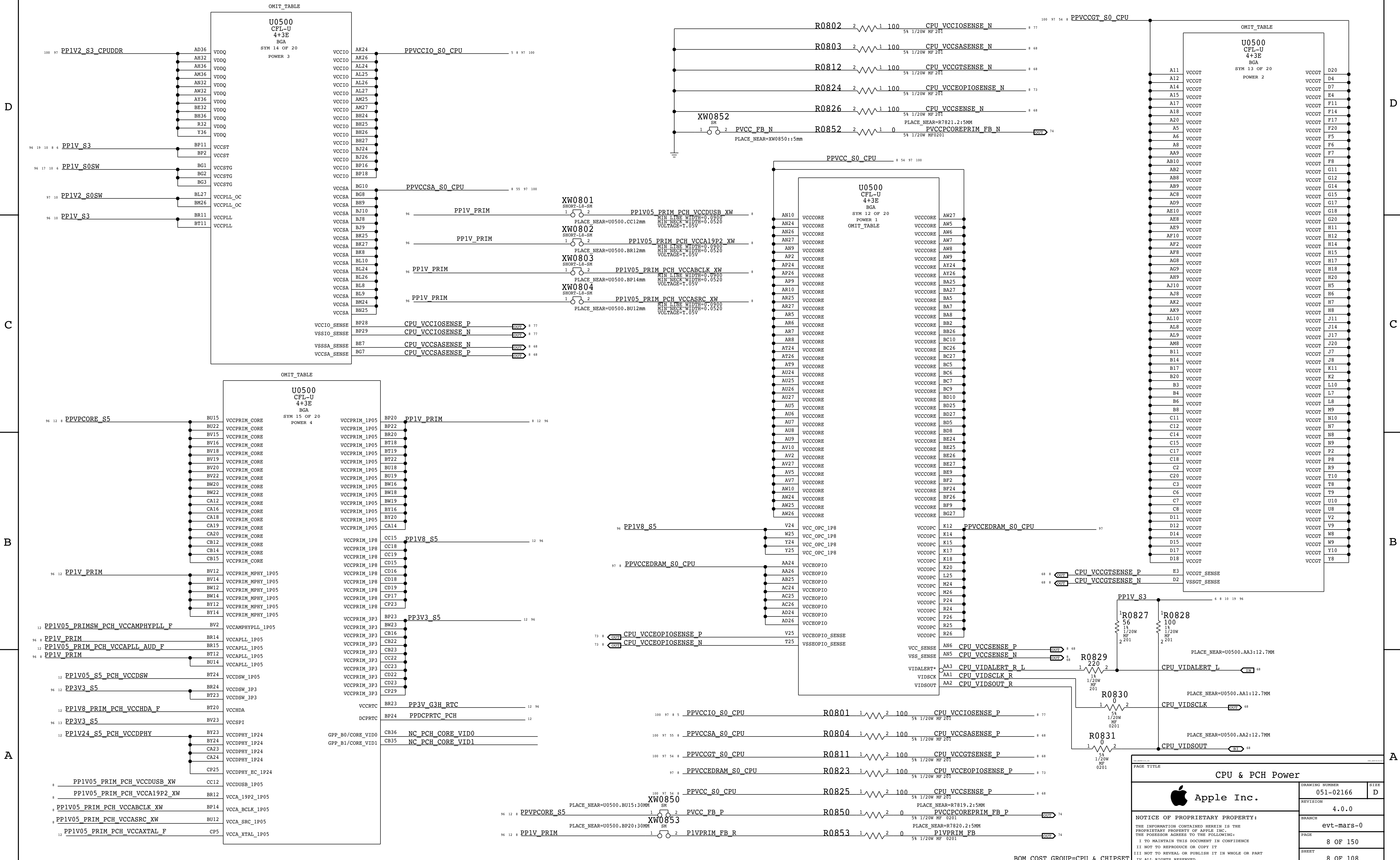
CPU LPDDR3 Interface

Apple Inc.

DRAMING NUMBER: 051-02166
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BOM_COST_GROUP=CPU & CHIPSET



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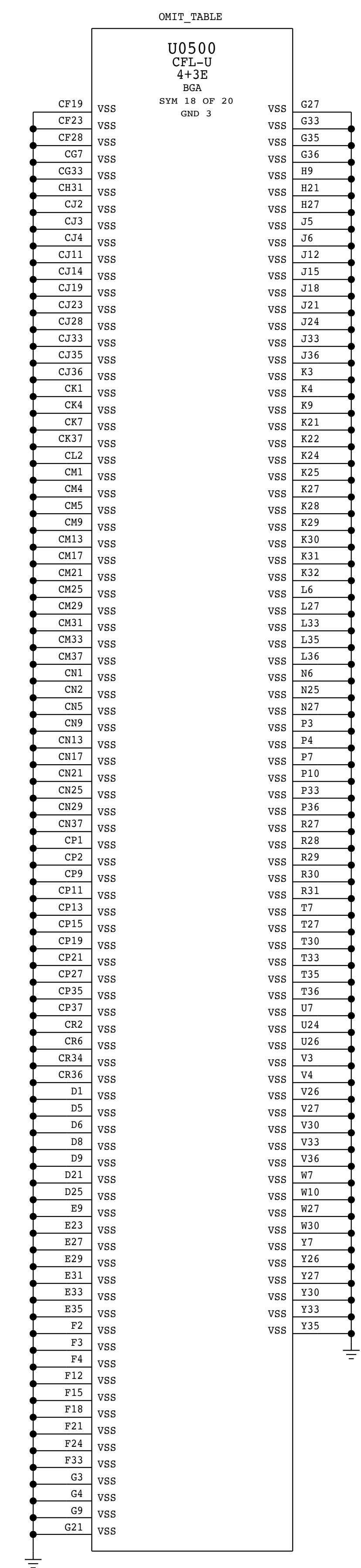
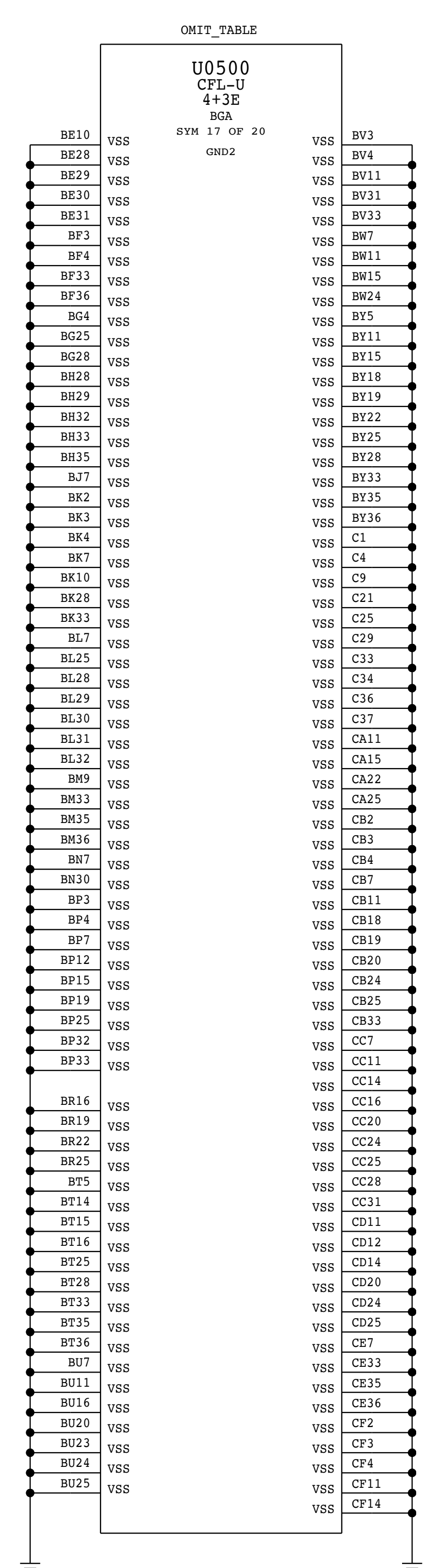
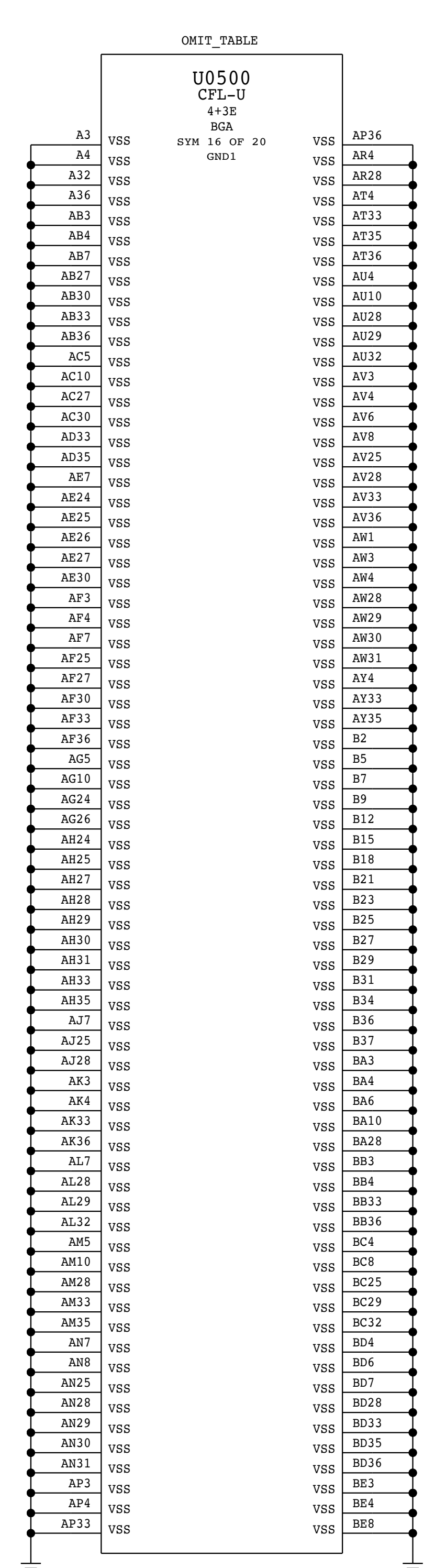
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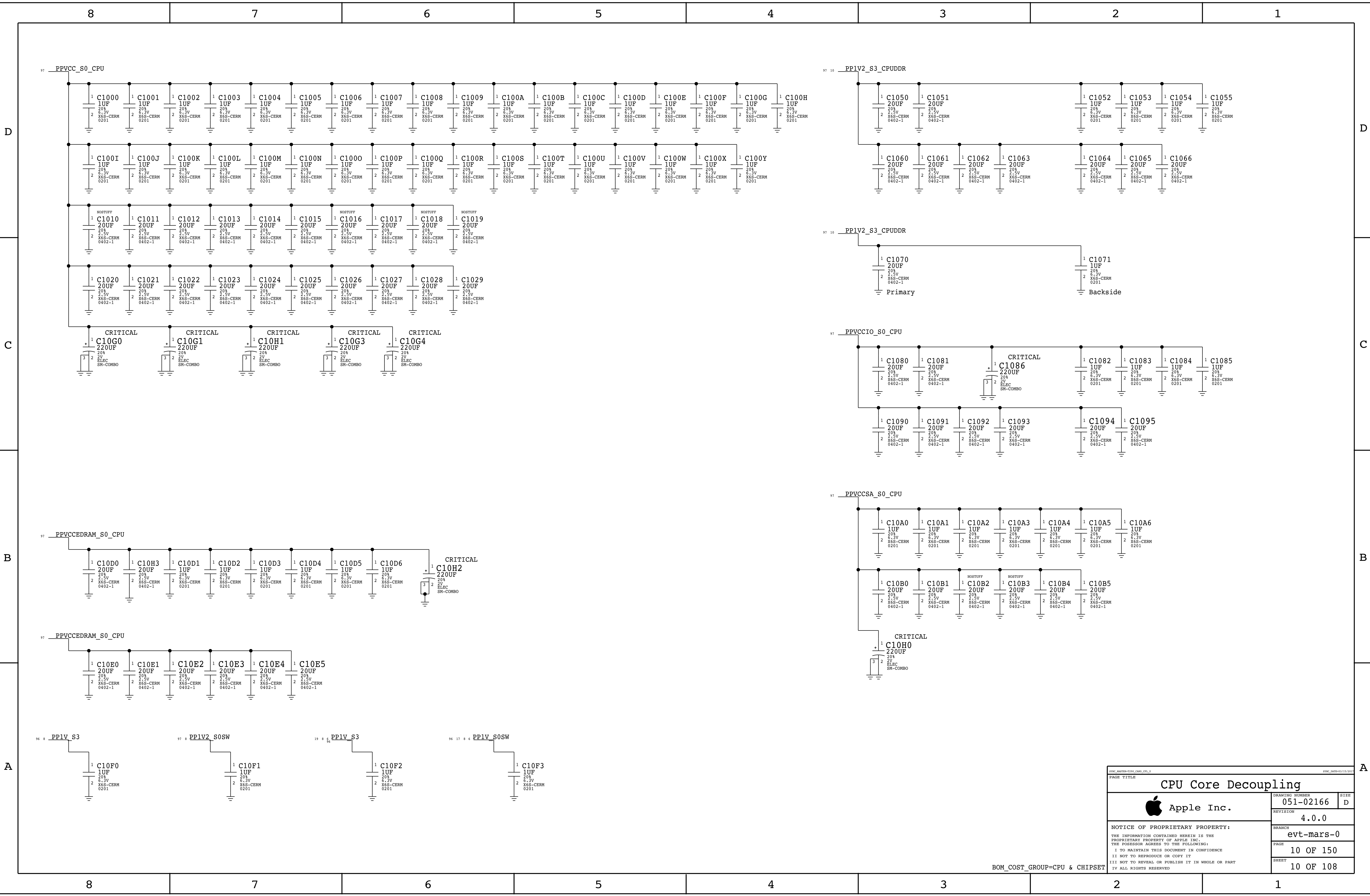
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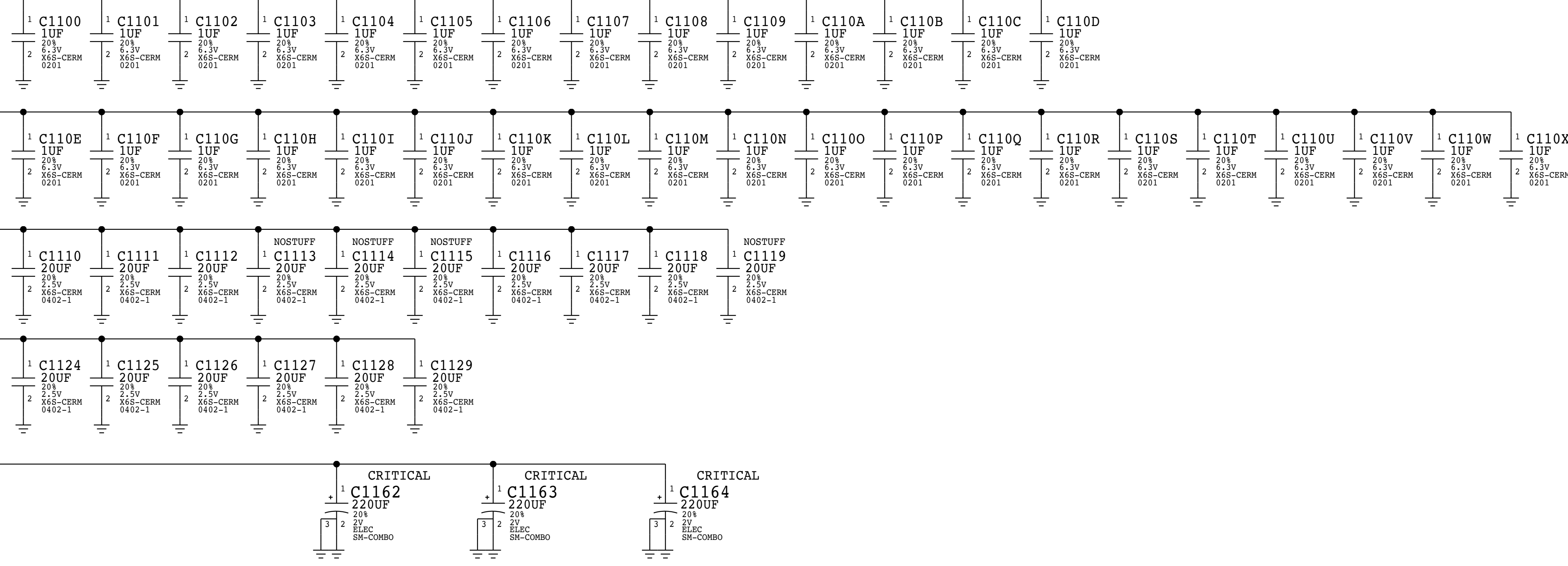
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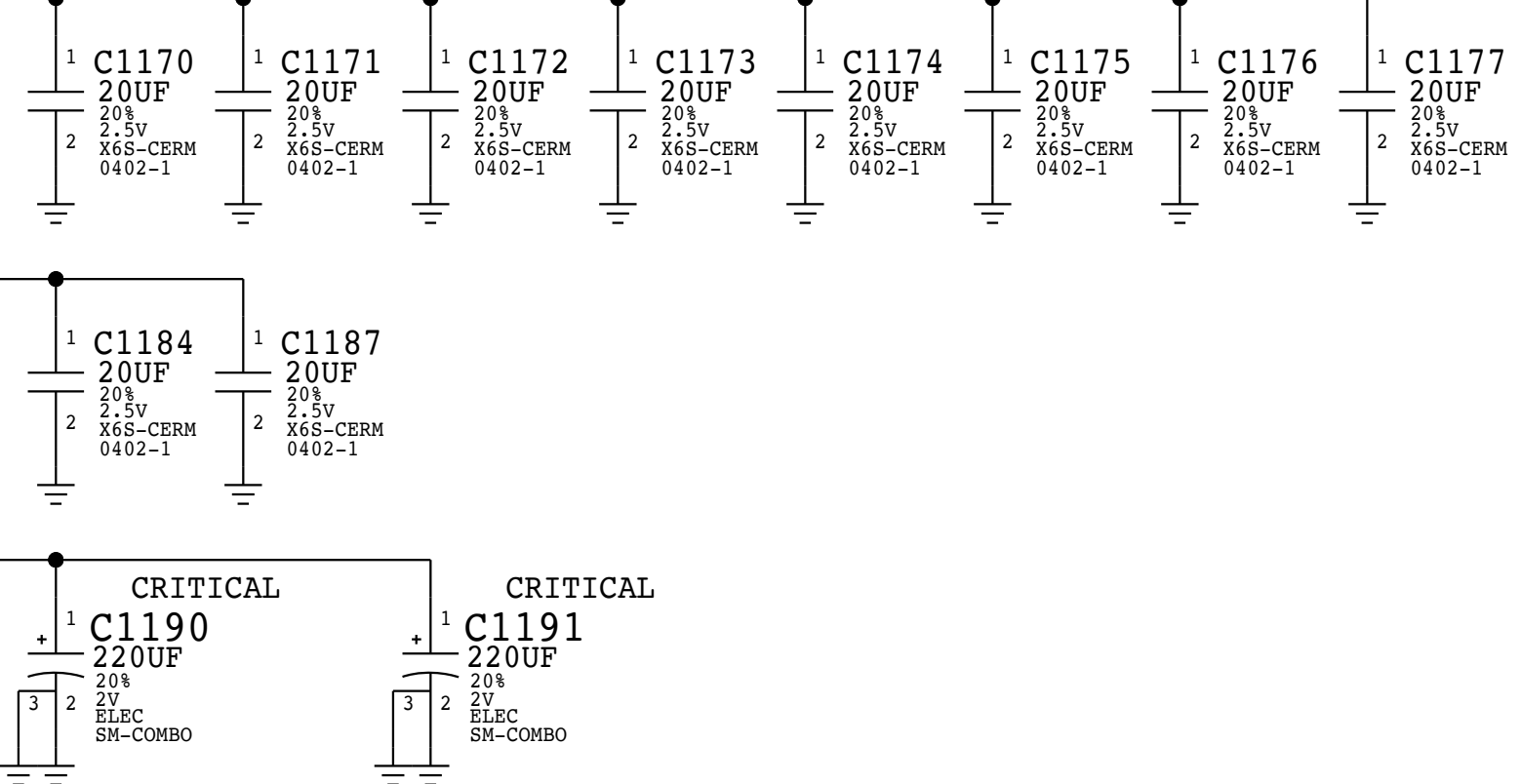
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CPU Core Decoupling		
Apple Inc.	DRAWING NUMBER 051-02166	SIZE D
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97 PPVCCGT_S0_CPU



97 PPVCCGT_S0_CPU



BOM_COST_GROUP=CPU & CHIPSET

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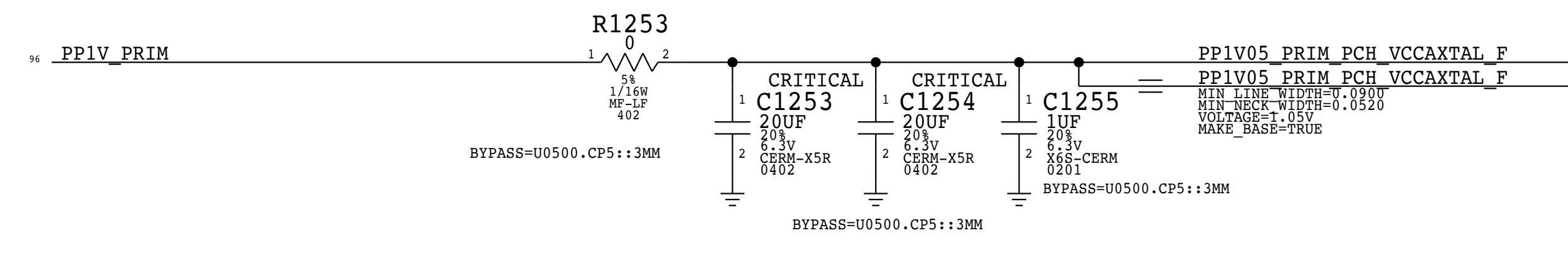
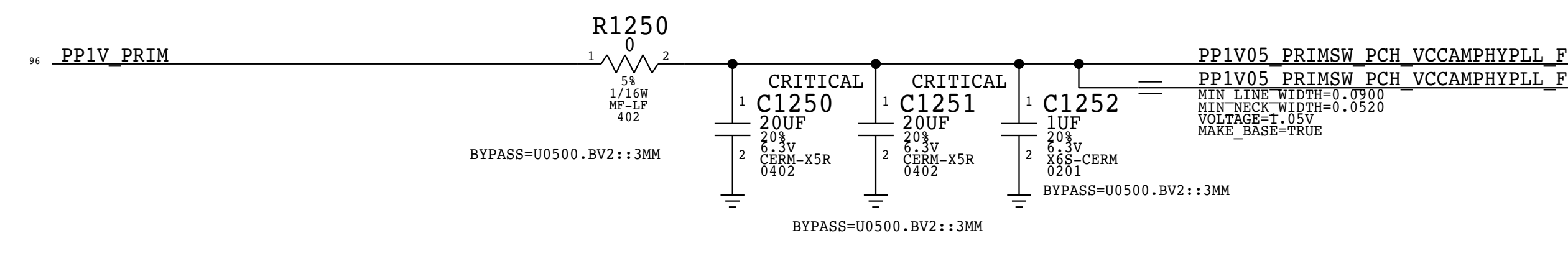
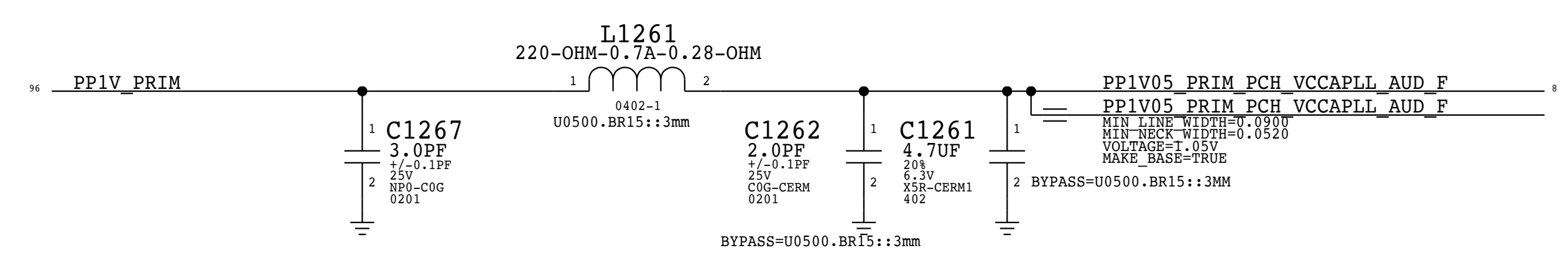
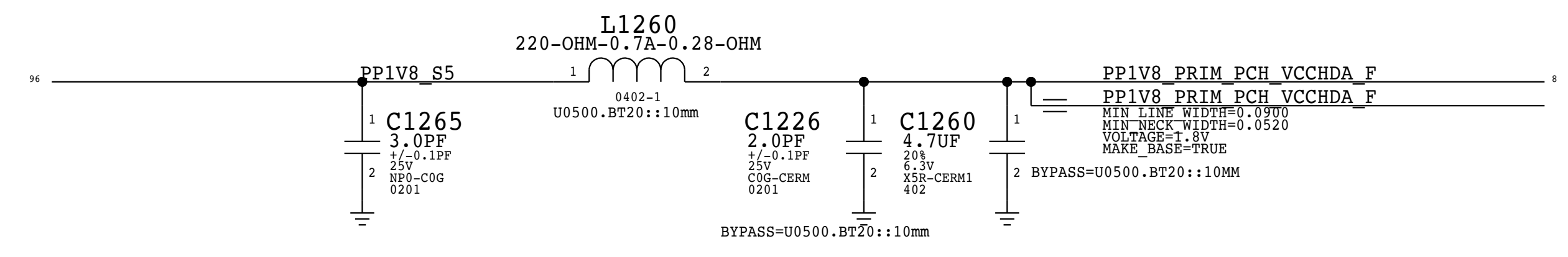
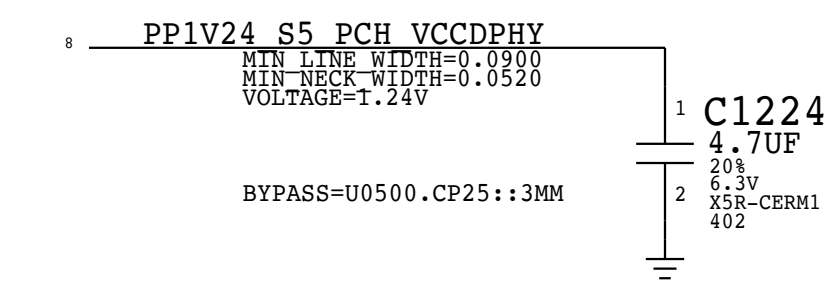
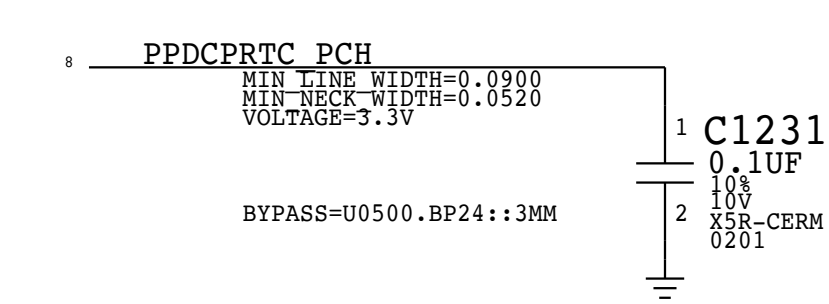
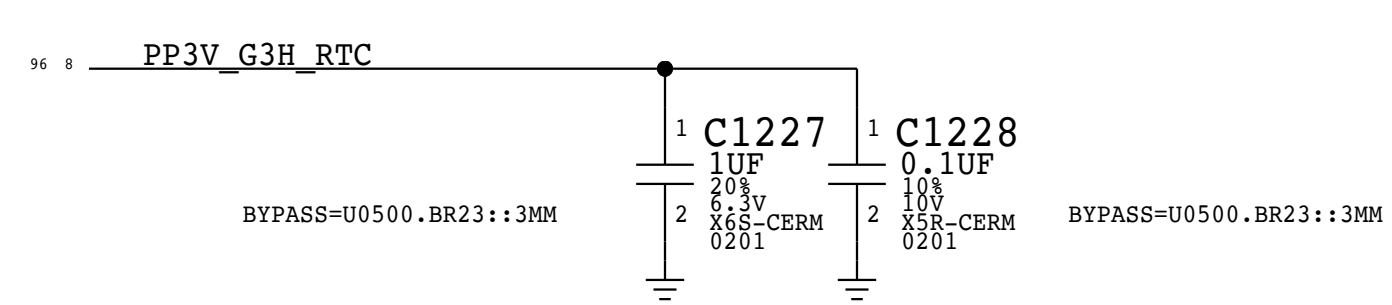
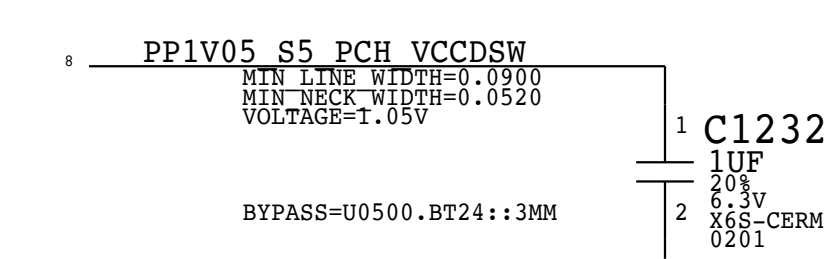
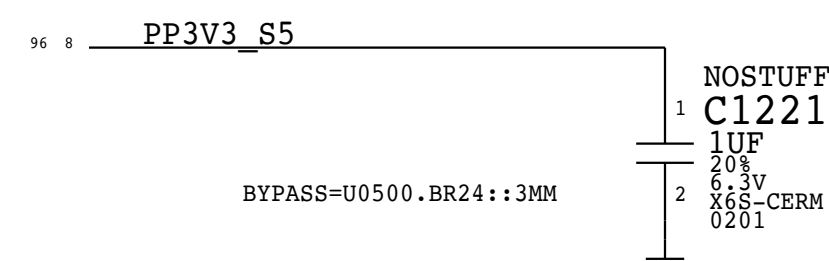
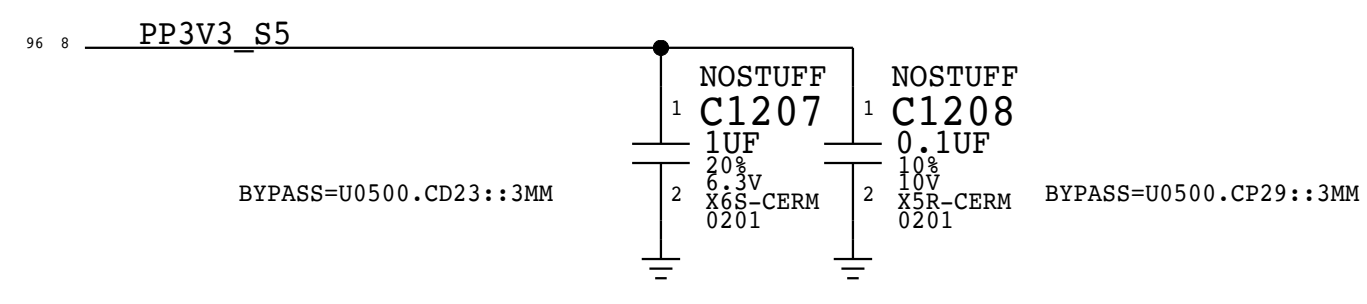
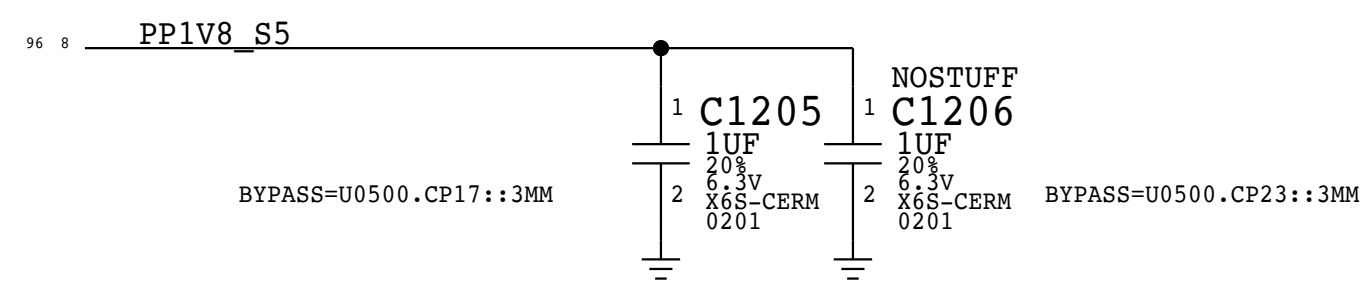
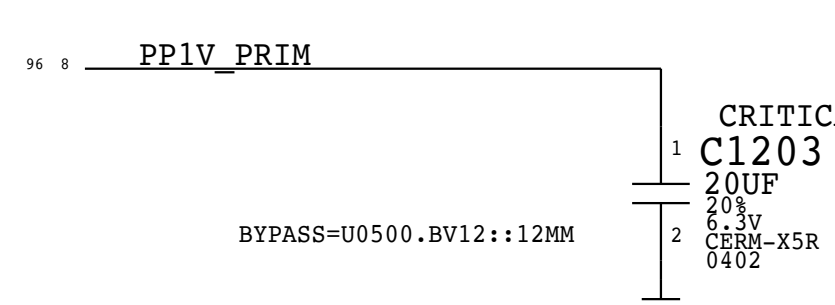
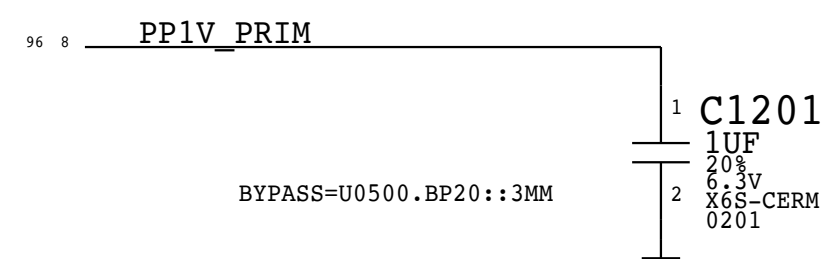
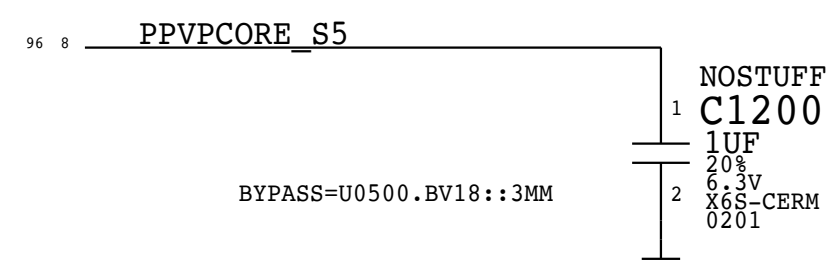
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FILTER PLACEHOLDERS ONLY

RAIL SIDE

PCH SIDE



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PCH Decoupling		
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BOM_COST_GROUP=CPU & CHIPSET

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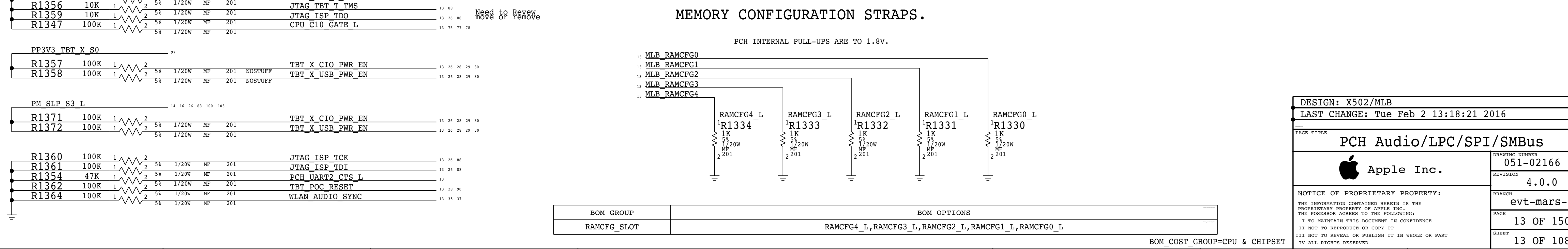
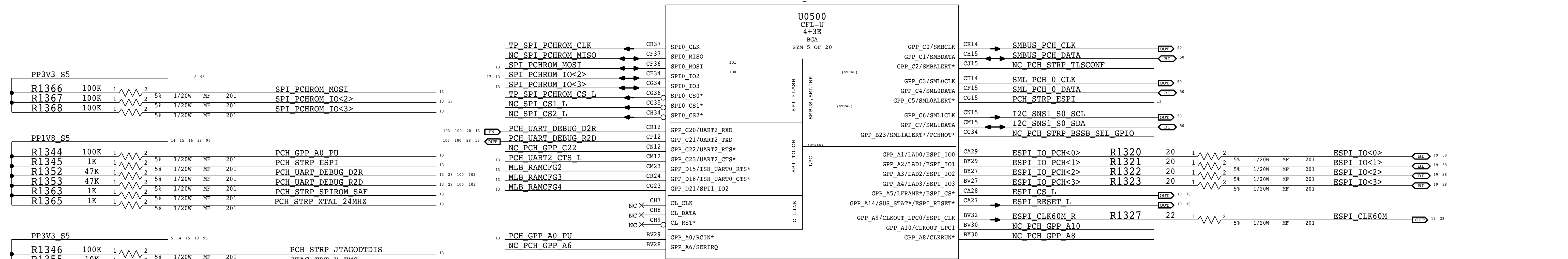
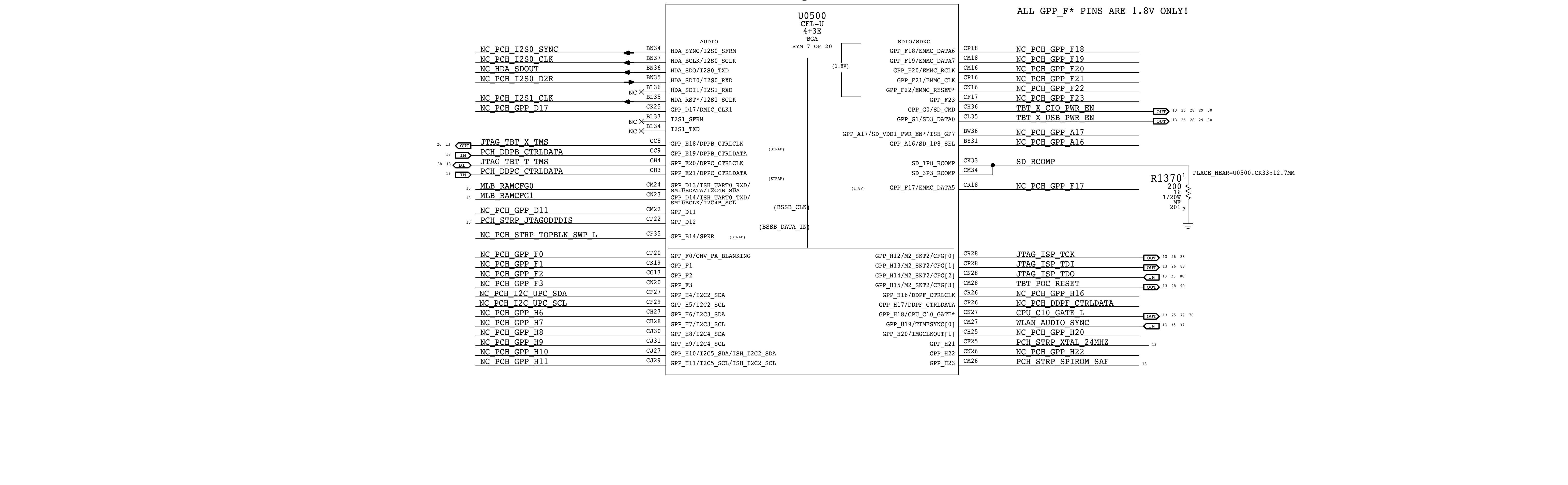
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L, RAMCFG3_L, RAMCFG2_L, RAMCFG1_L, RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue Feb 2 13:18:21 2016

PAGE TITLE
PCH Audio/LPC/SPI/SMBus

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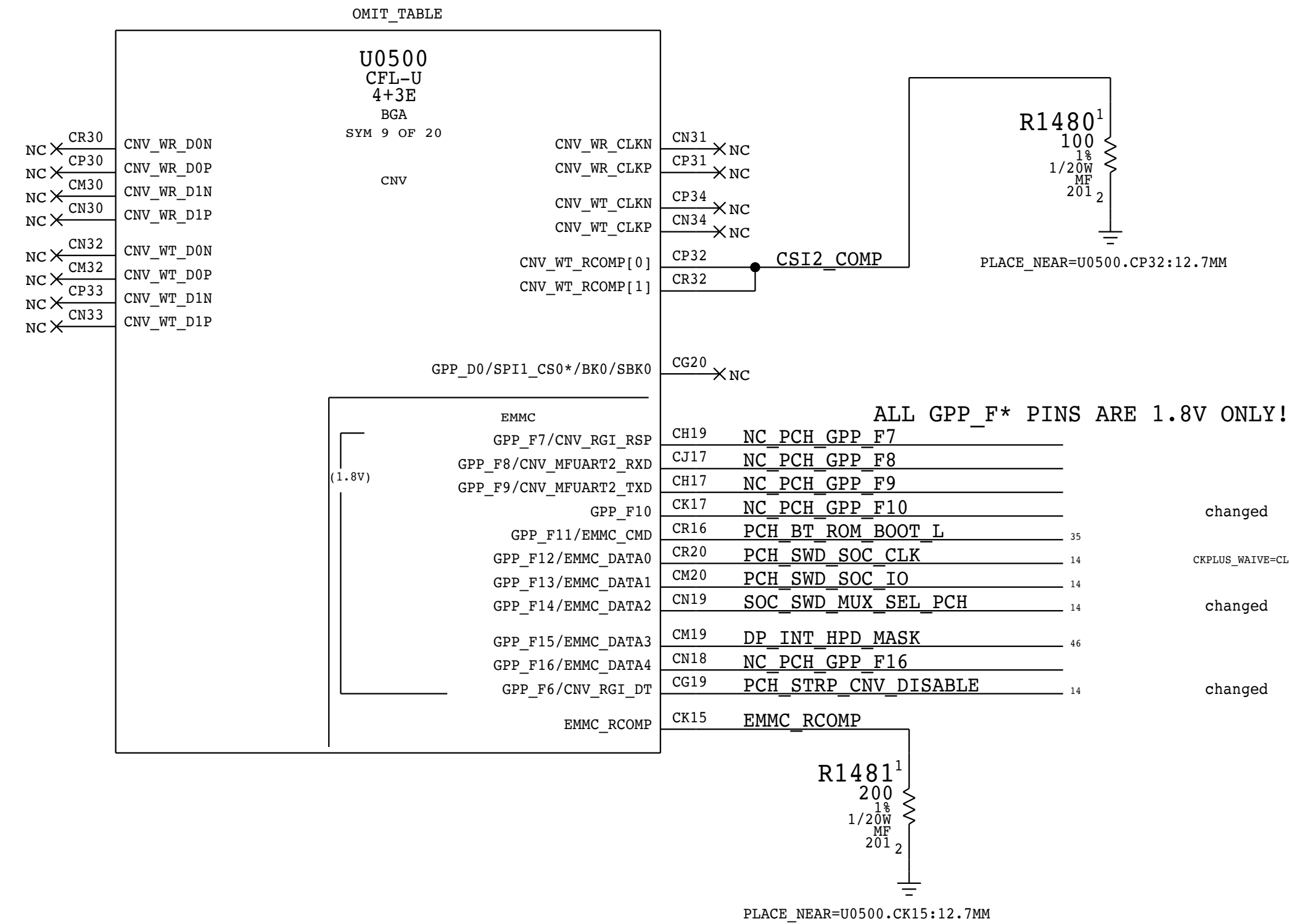
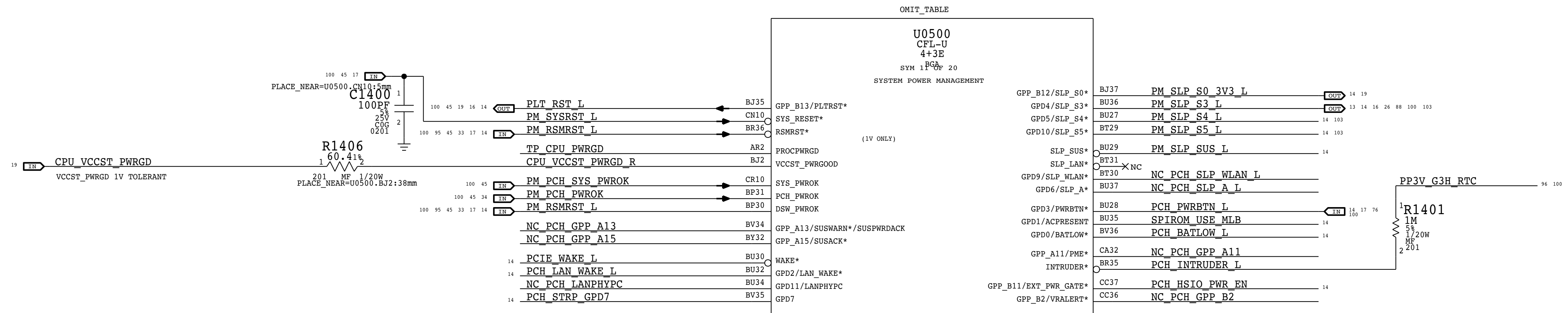
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Part	Value	Footprint	Package	Pin	Signal	Notes
R1461	1K	1	MF	2	PCH_STRP_CNV_DISABLE	
R1446	100K	1	MF	201	PCH_SWD_SOC_CLK	changed
R1445	100K	1	MF	201	PCH_SWD_SOC_IO	
PP3V3_S5						
R1440	100K	1	MF	201	SPIROM_USE_MLB	
R1441	100K	1	MF	201	PCH_STRP_GPD7	
R1451	100K	1	MF	201	PCH_BATLOW_L	
R1452	10K	1	MF	201	PCIE_WAKE_L	
R1453	100K	1	MF	201	PCH_LAN_WAKE_L	
R1459	100K	1	MF	201	PCH_HSI0_PWR_EN	
R1463	1K	1	MF	201	PCH_PWRBTN_L	
PP1V8_S5						
R1460	100K	1	MF	201	PLT_RST_L	
R1444	100K	1	MF	201	SOC_SWD_MUX_SEL_PCH	
R1454	100K	1	MF	201	PM_SLP_S5_L	
R1455	100K	1	MF	201	PM_SLP_S4_L	
R1456	100K	1	MF	201	PM_SLP_S3_L	
R1457	100K	1	MF	201	PM_SLP_S0_3V3_L	
R1458	100K	1	MF	201	PM_SLP_SUS_L	

NOTE: =PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
 THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
 THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.

ALL GPP_F* PINS ARE 1.8V ONLY!

DESIGN: X502/MLB	
LAST CHANGE: Tue Apr 5 13:08:54 2016	
PAGE TITLE	
PCH Power Management	
DRAWING NUMBER	051-02166
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BOM_COST_GROUP=CPU & CHIPSET

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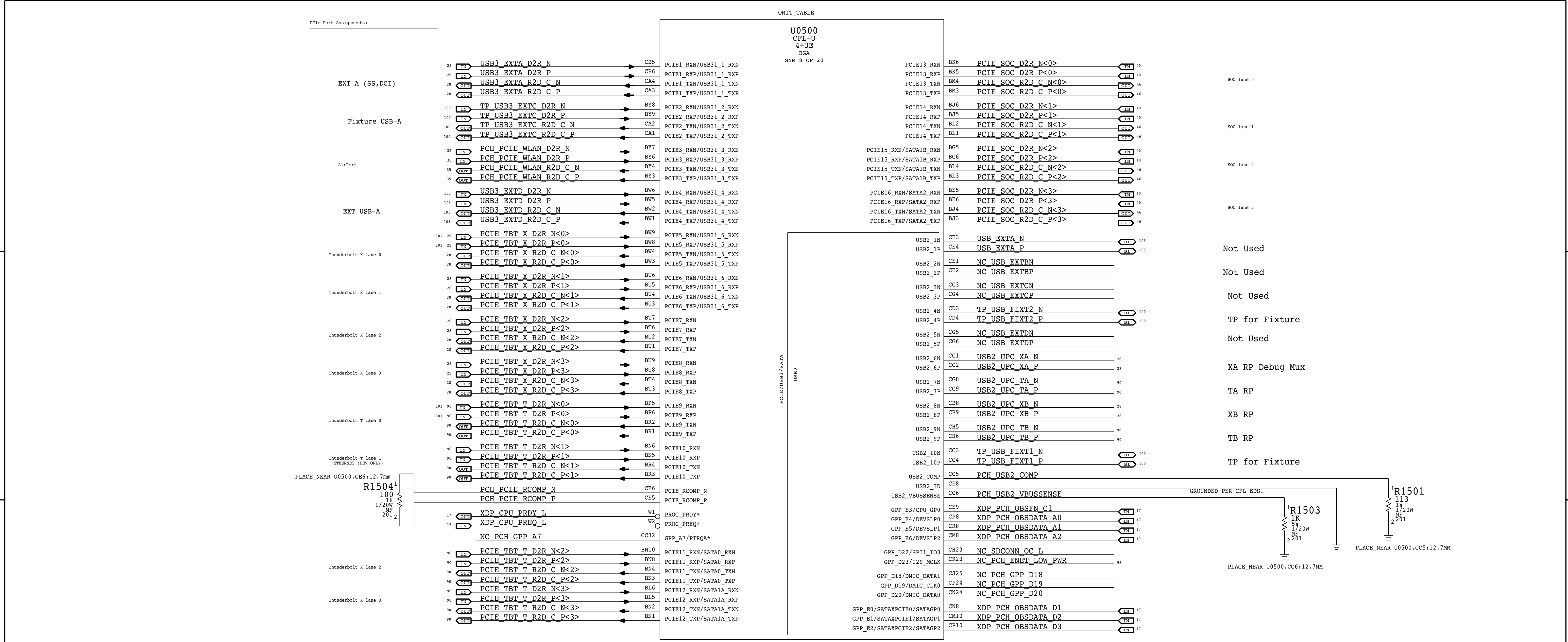
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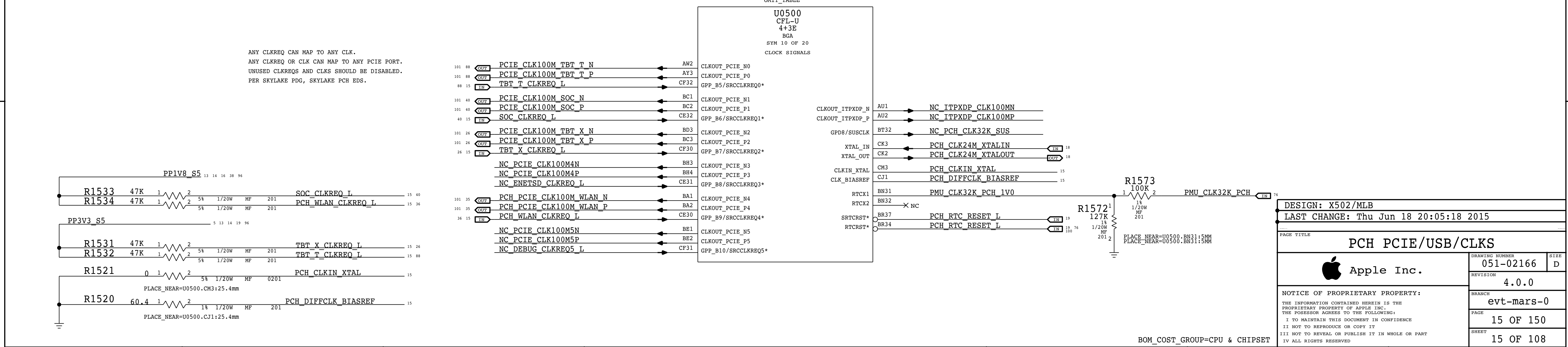
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DESIGN: X502/MLB
 LAST CHANGE: Thu Jun 18 20:05:18 2015

PAGE TITLE
PCH PCIE/USB/CLKS

Apple Inc.

DRAWING NUMBER	051-02166	SIZE	D
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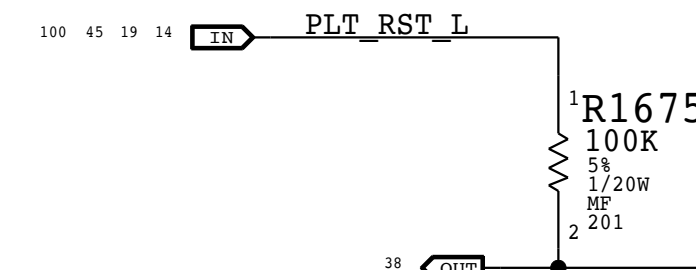
BOM_COST_GROUP=CPU & CHIPSET

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ALL GPP_F* PINS ARE 1.8V ONLY!

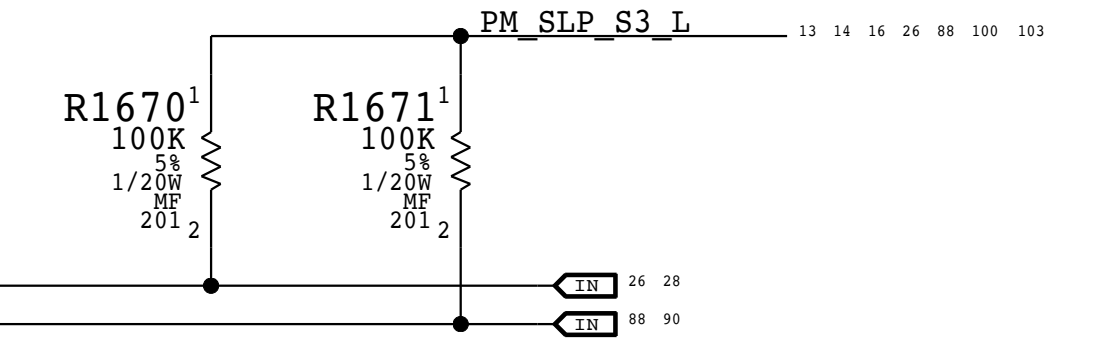
OMIT TABLE



37 16	PCH_SOC_SYNC	CC27
	SOC_PERST_L	CE28
	NC_PCH_ENETSD_RESET_L	CE27
16	PCH_STRP_NO_REBOOT	CE29
	NC_PCH_GPP_B19	CA31
	NC_PCH_GPP_B20	CC29
	NC_PCH_GPP_B21	CC30
	NC_PCH_STRP_BOOT_SPI_L	CA30
34 16	PCH_UART_BT_D2R	CR14
34 16	PCH_UART_BT_R2D	CP14
34 16	PCH_UART_BT_RTS_L	CN14
34 16	PCH_UART_BT_CTS_L	CM14
	NC_PCH_GPP_C16	CM11
	NC_PCH_GPP_C17	CN11
	NC_PCH_GPP_C18	CK12
	NC_PCH_GPP_C19	CJ12
	NC_PCH_GPP_C12	CG12
	NC_PCH_GPP_C13	CH12
	NC_PCH_GPP_C14	CF12
	NC_PCH_GPP_C15	CG14
	NC_MEM_OK	CP4
	NC_PCH_DDPD_CTRLDATA	CN4
	NC_PCH_I2S_BT_CLK	CH32
	NC_PCH_I2S_BT_SYNC	CJ32
	NC_PCH_I2S_BT_R2D	CH29
	NC_PCH_I2S_BT_D2R	CH30
36 35 19	PCH_WLAN_PERST_L	CB34
36 35	PCH_WLAN_DEV_WAKE	CC35

U0500	
CFI-U	
4+3E	
BGA	
SYM 6 OF 20	
LPSS	
GPP_B15/GSPI0_CS0*	
GPP_B16/GSPI0_CLK	
GPP_B17/GSPI0_MISO	
GPP_B18/GSPI0_MOSI	(STRAP)
GPP_B19/GSPI1_CS0*	
GPP_B20/GSPI1_CLK	
GPP_B21/GSPI1_MISO	
GPP_B22/GSPI1_MOSI	(STRAP)
GPP_C8/UART0_RXD	
GPP_C9/UART0_TXD	(1.8V)
GPP_C10/UART0_RTS*	(1.8V)
GPP_C11/UART0_CTS*	
GPP_C16/I2C0_SDA	
GPP_C17/I2C0_SCL	
GPP_C18/I2C1_SDA	
GPP_C19/I2C1_SCL	
GPP_C12/UART1_RXD/ISH_UART1_RXD	
GPP_C13/UART1_TXD/ISH_UART1_TXD	
GPP_C14/UART1_RTS*/ISH_UART1_RTS*	
GPP_C15/UART1_CTS*/ISH_UART1_CTS*	
GPP_E22/DPPD_CTRLCLK	
GPP_E23/DPPD_CTRLDATA	
GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK	
GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK	
GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI	(1.8V)
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO	
GPP_B3/CPU_GP2	
GPP_B4/CPU_GP3	

ISH	
GPP_D5/ISH_I2C0_SDA	CK22
GPP_D6/ISH_I2C0_SCL	CH20
GPP_D7/ISH_I2C1_SDA	CH22
GPP_D8/ISH_I2C1_SCL	CJ22
GPP_D1/SPI1_CLK	CF20
GPP_D2/SPI1_MISO_I01	CG22
GPP_D3/SPI1_MOSI_I00	CF22
GPP_D4/IMGCLKROUT0	CG25
GPP_F4/CNV_BRI_DT	CJ20
GPP_F5/CNV_BRI_RSP	CK20
GPP_G6/SD_CLK	CK36
GPP_D9	CN22
GPP_D10	CR22
GPP_G7/SD_WF	CK34
GPP_G2/SD3_DATA1	CL36
GPP_G3/SD3_DATA2	CM35
GPP_G4/SD_DATA3	CN35
GPP_G5/SD_CD*	CH35
GPP_A18/ISH_GP0	BW35
GPP_A19/ISH_GP1	BW34
GPP_A20/ISH_GP2	CA37
GPP_A21/ISH_GP3	CA36
GPP_A22/ISH_GP4	CA35
GPP_A23/ISH_GP5	CA34
GPP_A12/ISH_GP6/BM_BUSY*/SX_EXIT_HOLDOFF*	BW37

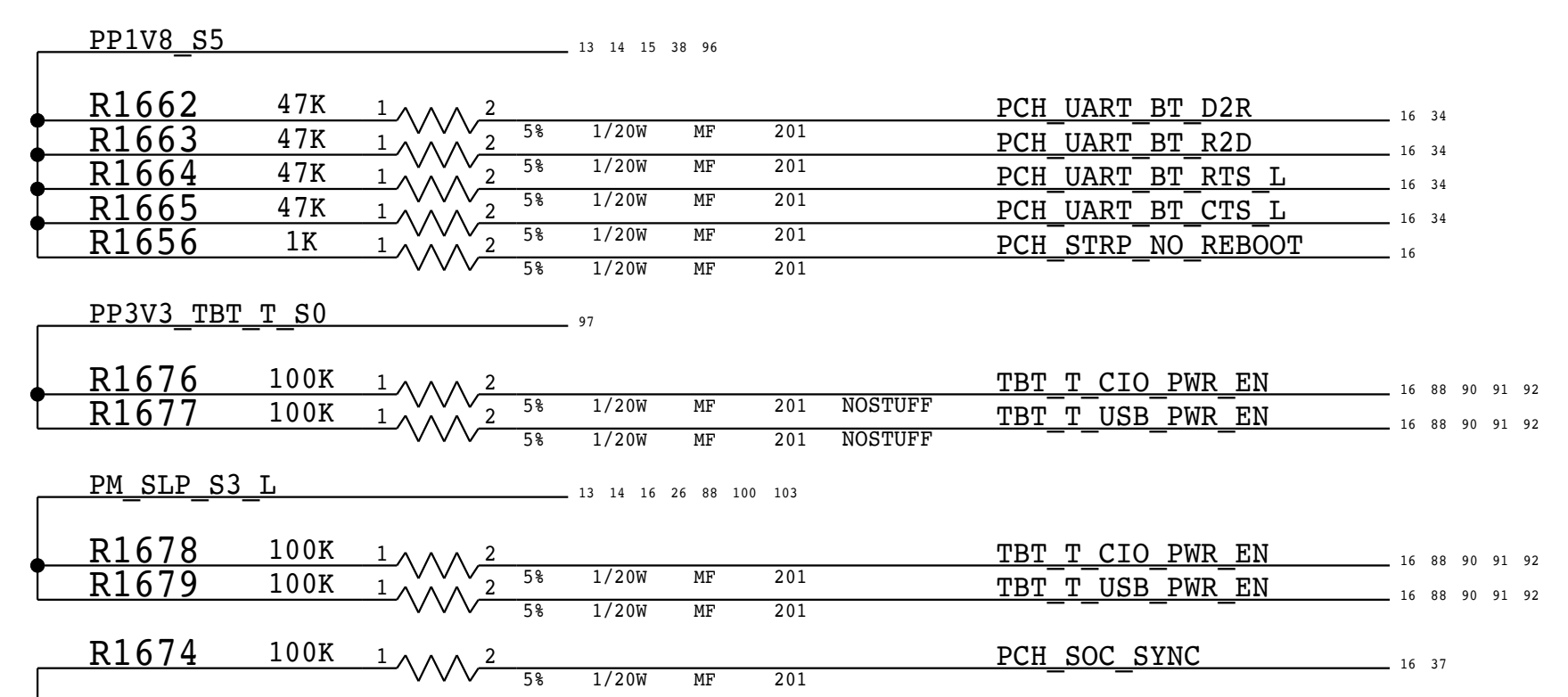


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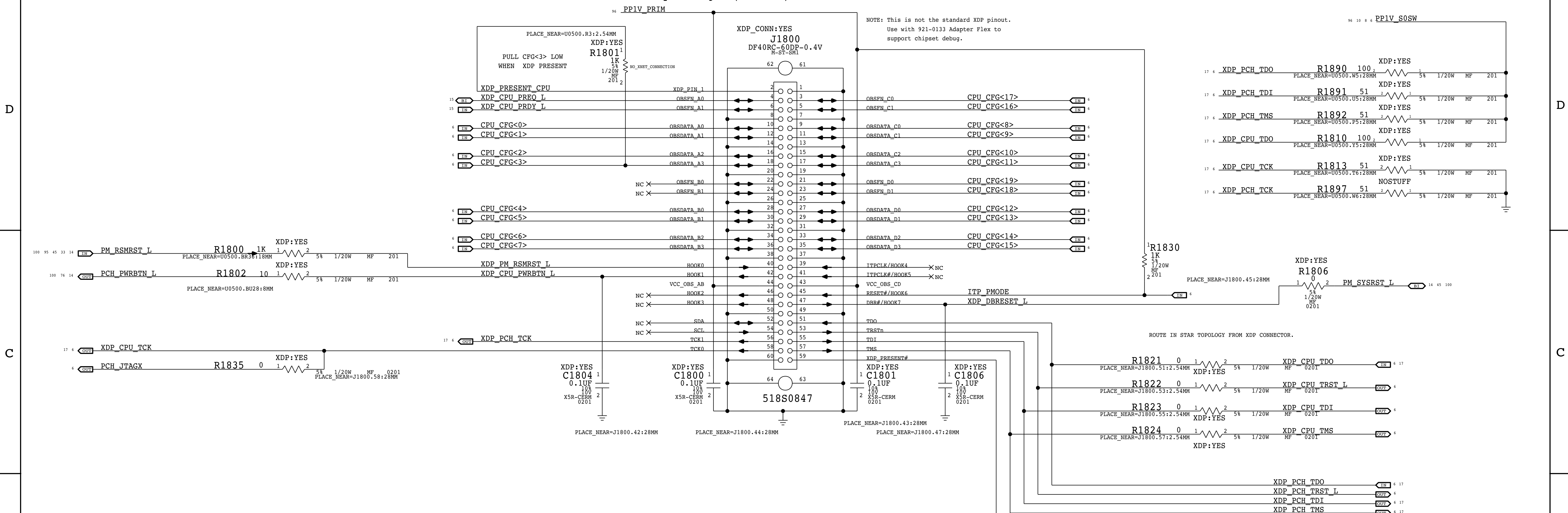
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DESIGN: X502/MLB	
LAST CHANGE: Wed Oct 28 12:50:22 2015	
PAGE TITLE	
PCH SPI/UART/GPIO	
Apple Inc.	
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BOM_COST_GROUP=CPU & CHIPSET

Primary / Merged (CPU/PCH) Micro2-XDP



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture. The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation. They are listed here to show their secondary XDP functions and to provide test points that are not used elsewhere.

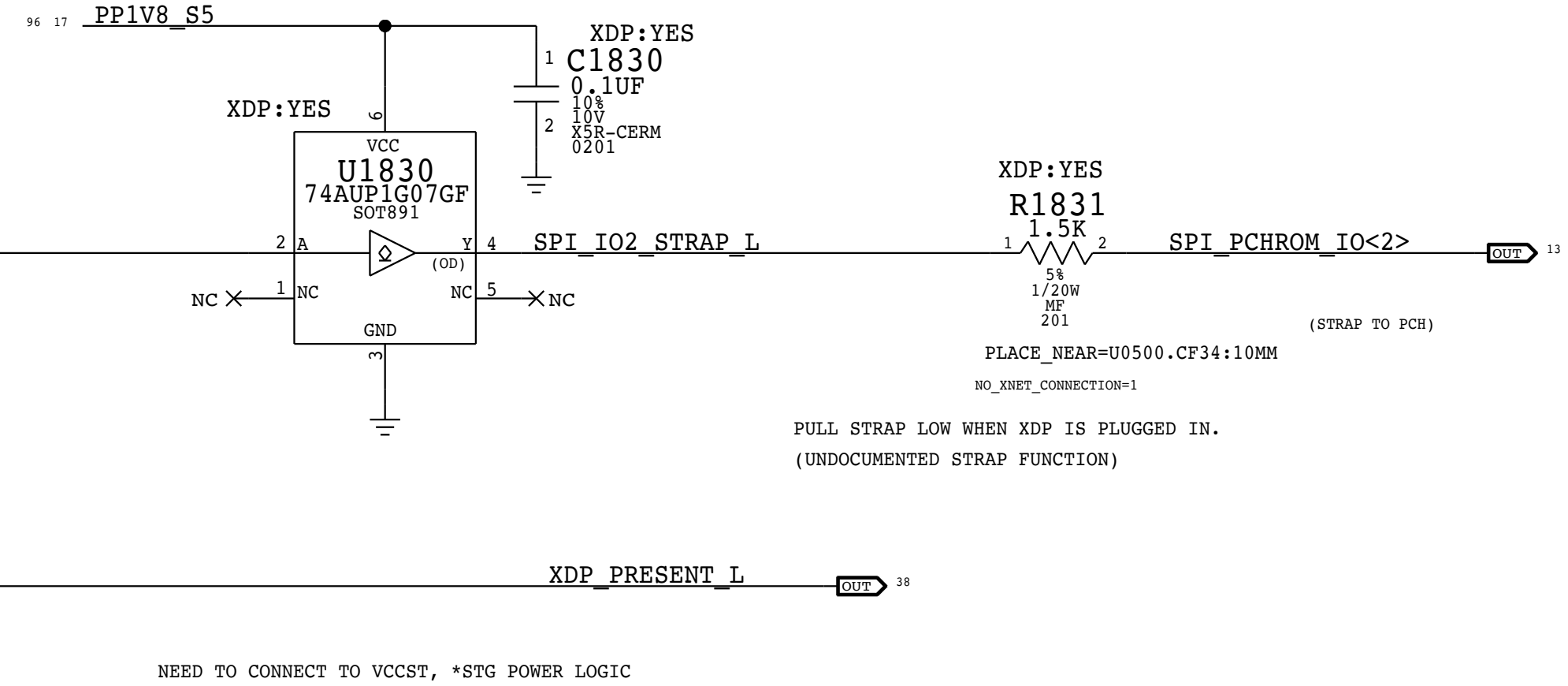
PCH/XDP Signals

XDP_PCH_OBSDATA_A0	TP1868
XDP_PCH_OBSDATA_A1	TP1869
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C1	TP1881
XDP_USB_EXT*_OC*_L	MAKE_BASE=TRUE
XDP_USB_EXT*_OC*_L	MAKE_BASE=TRUE
XDP_USB_EXT*_OC*_L	MAKE_BASE=TRUE
XDP_USB_EXT*_OC*_L	MAKE_BASE=TRUE

Non-XDP Signals

XDP_USB_EXT*_OC*_L	101
XDP_USB_EXT*_OC*_L	101
XDP_USB_EXT*_OC*_L	101
XDP_USB_EXT*_OC*_L	101

Unused GPIOs have TPs.
 USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
 JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.



PAGE TITLE		
CPU/PCH Merged XDP		
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BOM_COST_GROUP=DEBUG

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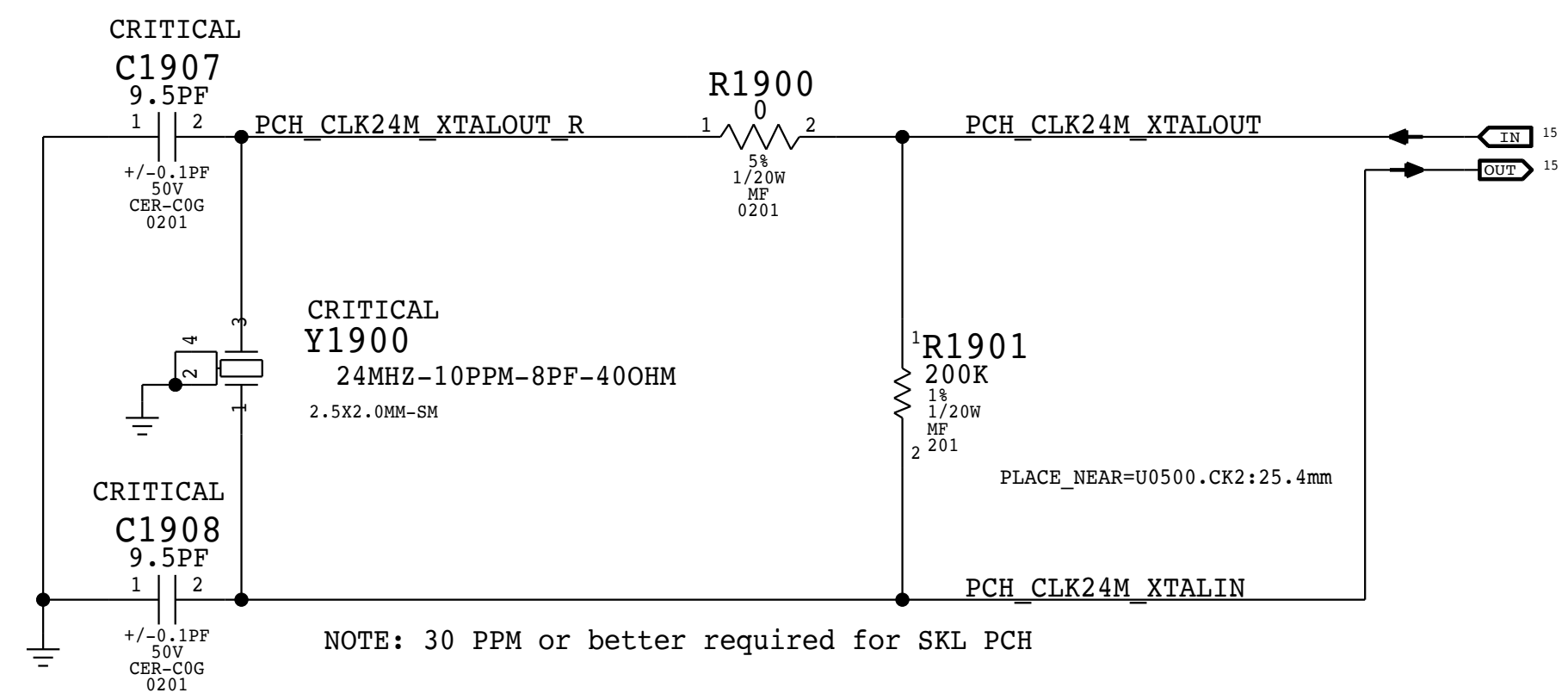
4

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24MHz CLOCK



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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE		SYNC MASTER=J132 JIN		SYNC DATE=06/05/2017		
Chipset Support 1						
	DRAWING NUMBER		051-02166		SIZE	
	REVISION		4.0.0		D	
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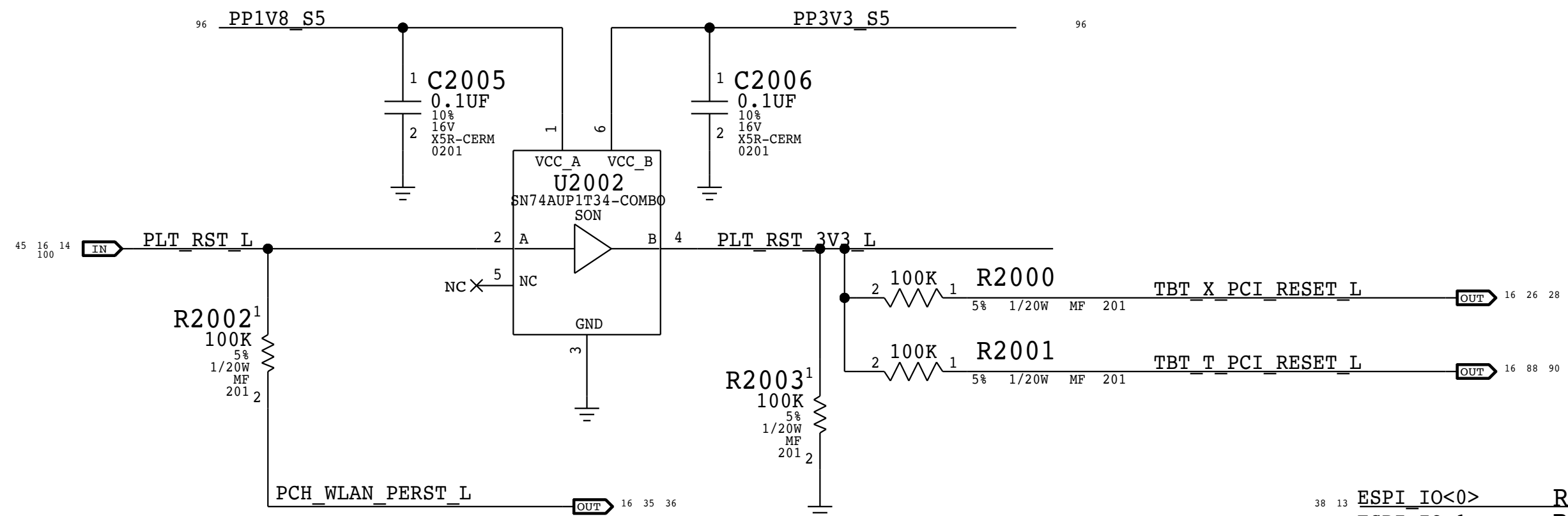
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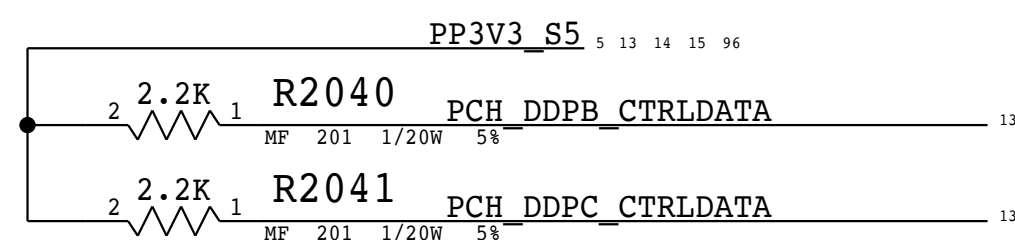
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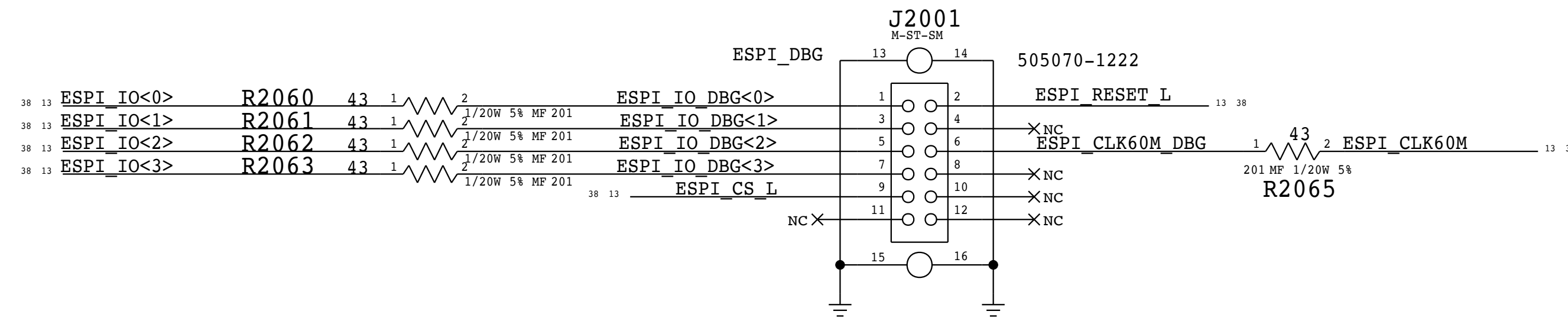
Platform Reset Connections



ENABLE DDPB DDPC INTERFACES



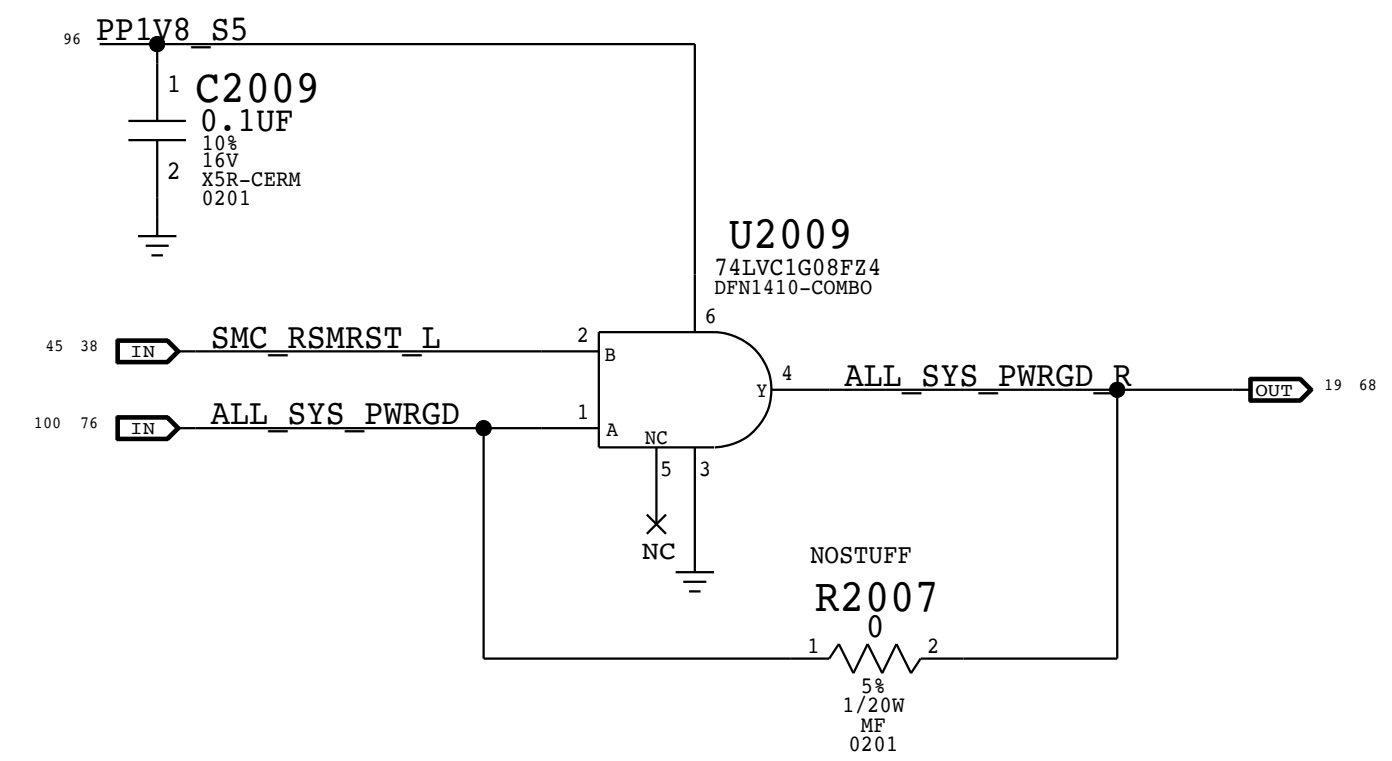
eSPI Analyzer Placement study first



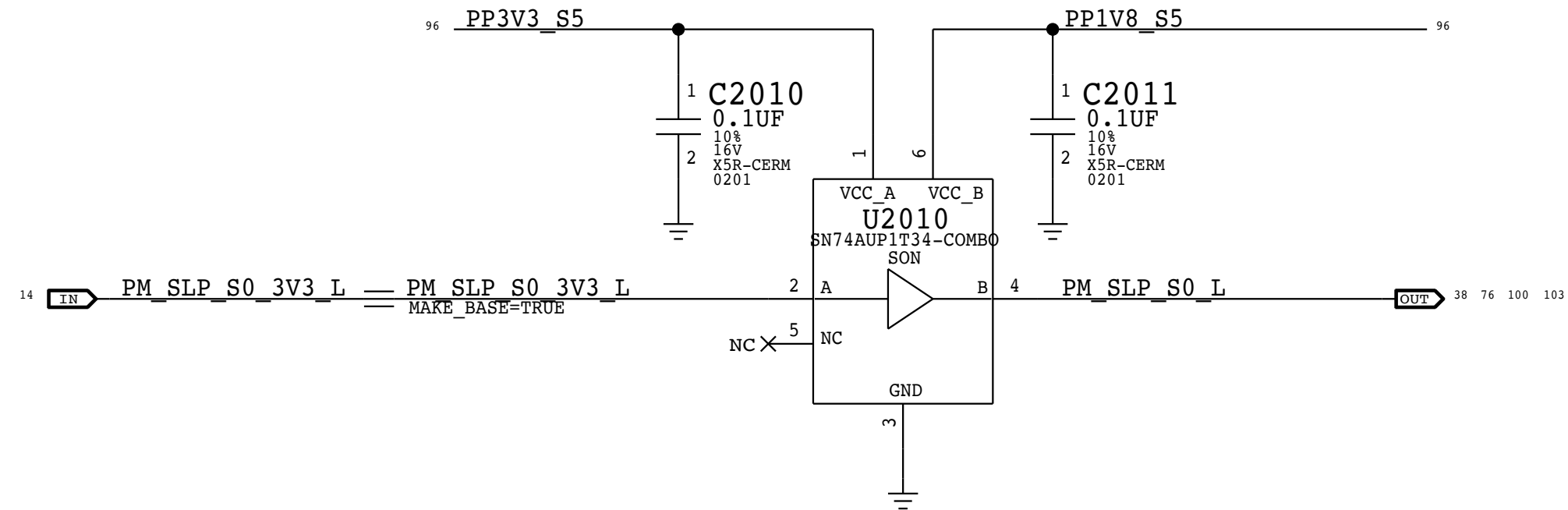
SIGNAL ALIASES

15	PCH_RTC_RESET_L	==	MAKE_BASE=TRUE	PCH_RTC_RESET_L	15	76
		==	MAKE_BASE=TRUE	PCH_RTC_RESET_L		
5	TEST_NOA_N_10	==	MAKE_BASE=TRUE	TEST_NOA_N_10	19	
		==	MAKE_BASE=TRUE	TEST_NOA_N_10		
5	TEST_NOA_N_11	==	MAKE_BASE=TRUE	TEST_NOA_N_11	19	
		==	MAKE_BASE=TRUE	TEST_NOA_N_11		
		==	NO_TEST=1	TEST_NOA_N_11		
6	XDP_BPM_L<3..1>	==	MAKE_BASE=TRUE	NC_XDP_BPM_L<3..1>		
		==	NO_TEST=1	NC_XDP_BPM_L<3..1>		

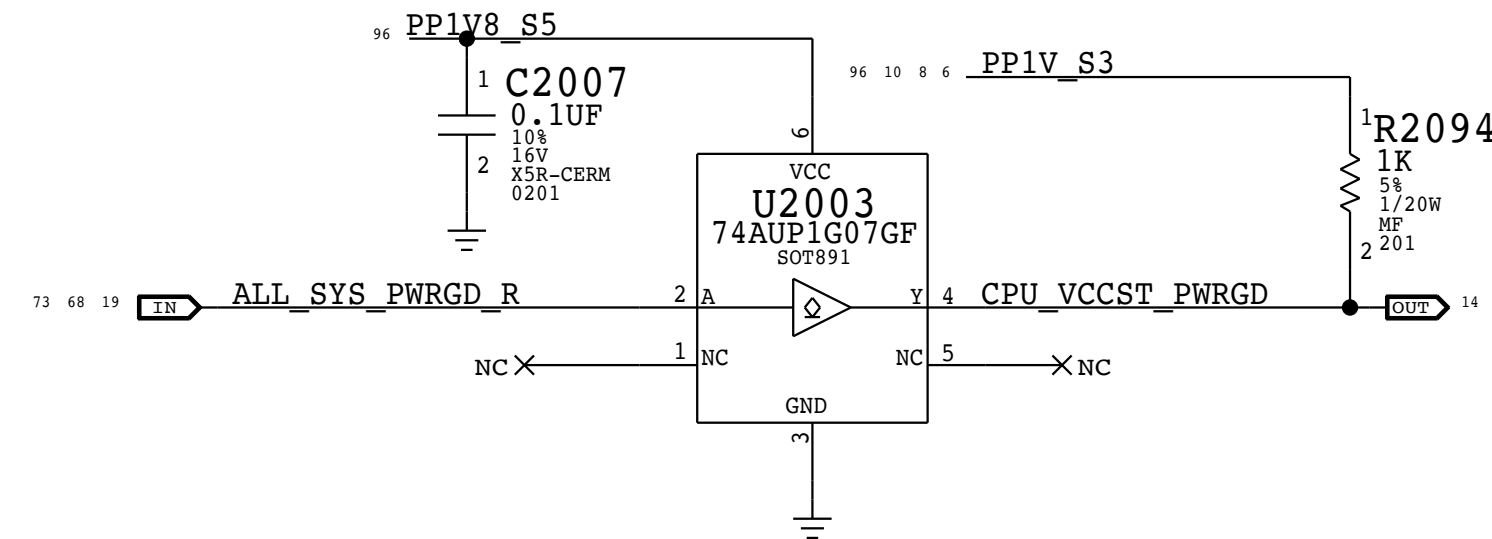
ALL_SYS_PWRGD QUALIFIER



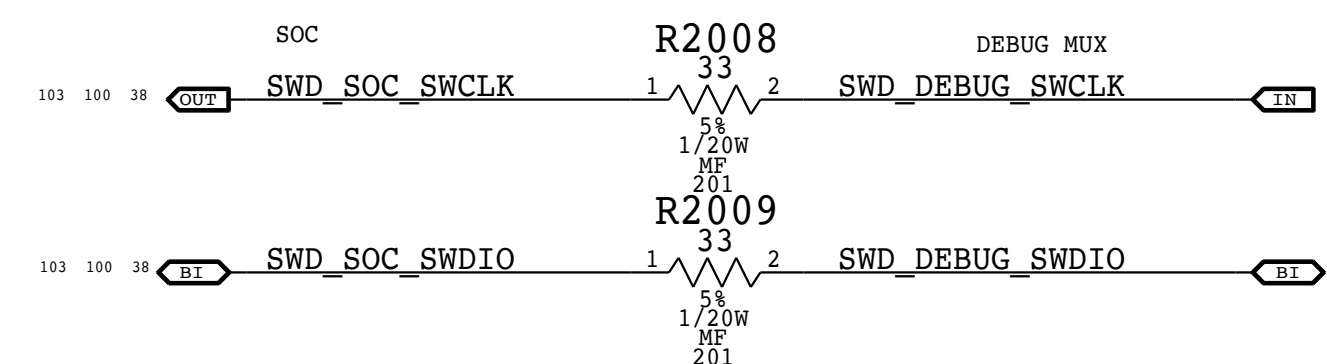
SLP_S0# LEVEL SHIFTER



VCCST_PWRGD LEVEL SHIFTER



SOC SWD <=> DEBUG MUX PATH



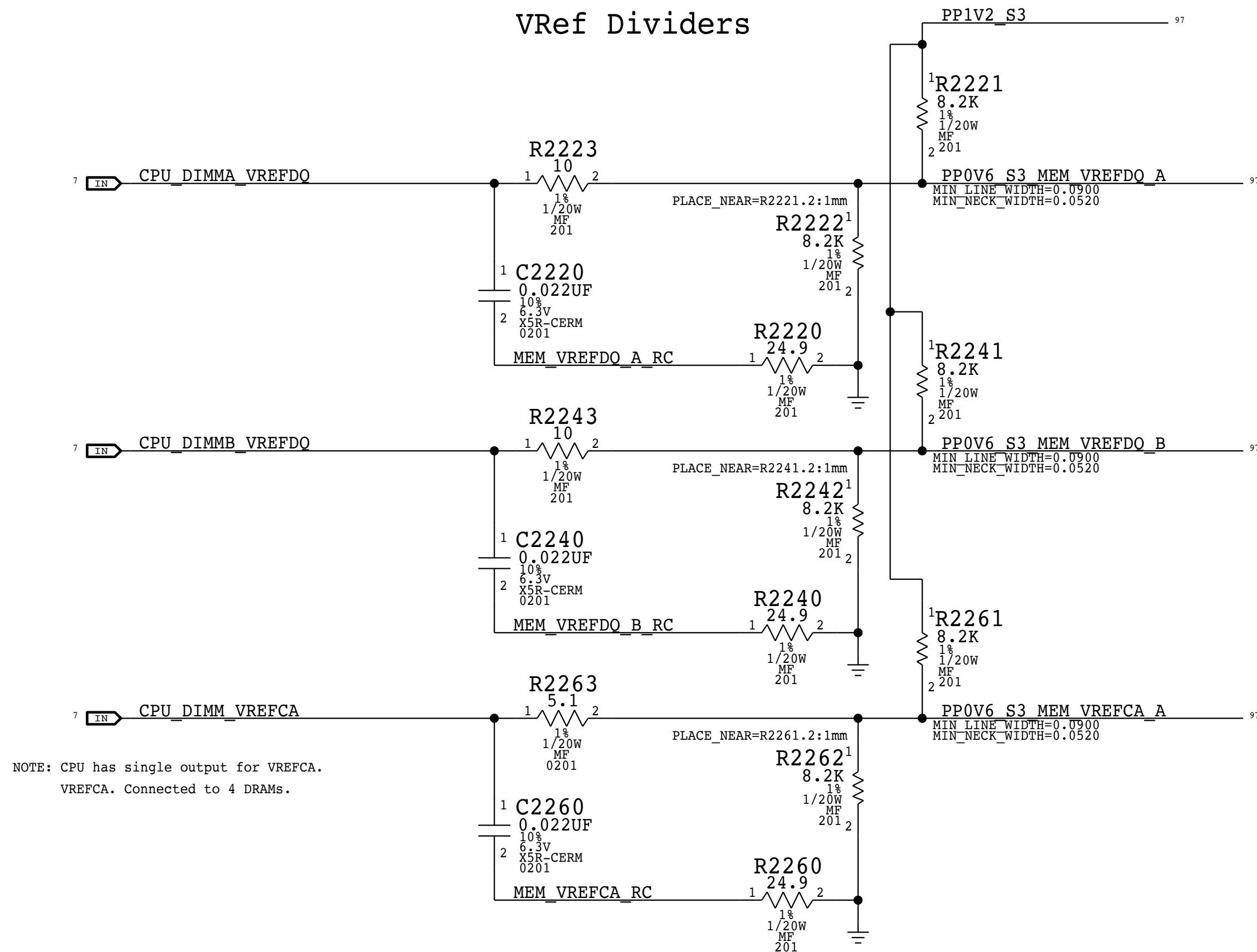
TPs for Chipset Debug Pins

6	TEST_CPU_D34	P2MM	1	PP2001
6	TEST_CPU_BJ34	P2MM	1	PP2002
6	TEST_CPU_A35	P2MM	1	PP2003
6	TEST_CPU_F37	P2MM	1	PP2004
6	TEST_CPU_BJ36	P2MM	1	PP2005
6	TEST_CPU_F34	P2MM	1	PP2006
6	TEST_CPU_CN36	P2MM	1	PP2007
19	TEST_NOA_N_10	P2MM	1	PP2008
19	TEST_NOA_N_11	P2MM	1	PP2009

Chipset Support 2	
Apple Inc.	DRAWING NUMBER 051-02166
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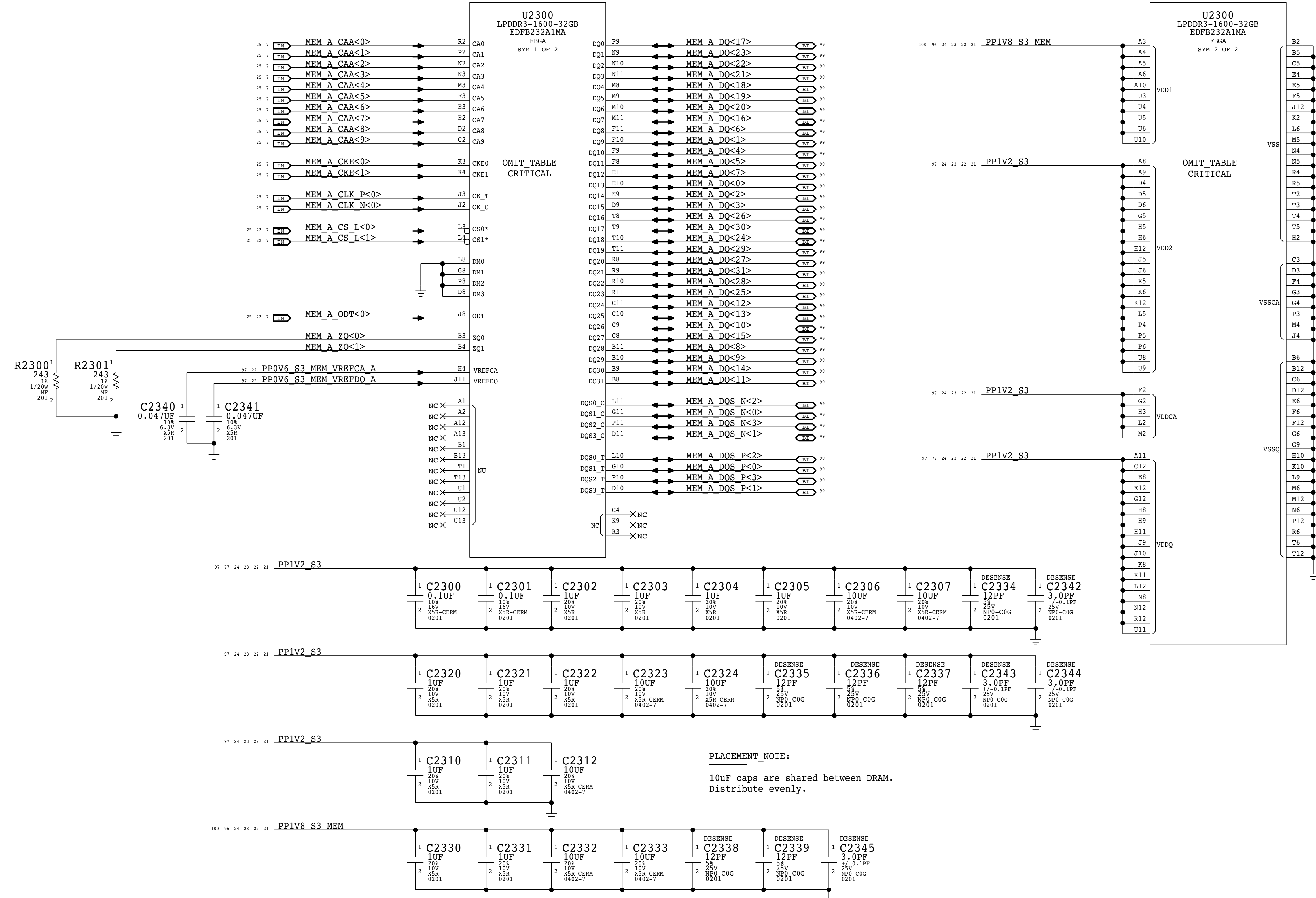
CPU-Based Margining

VRef Dividers



PAGE TITLE		DRAWING NUMBER		SIZE
LPDDR3 VREF Margining		051-02166	D	
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LPDDR3 CHANNEL A (0-31)



PLACEMENT NOTE:
10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC MASTER=J79A MLB		SYNC DATE=01/31/2017	
PAGE TITLE			
LPDDR3 DRAM Channel A (00-31)			
Apple Inc.	DRAWING NUMBER	051-02166	SIZE
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LPDDR3 CHANNEL A (32-63)

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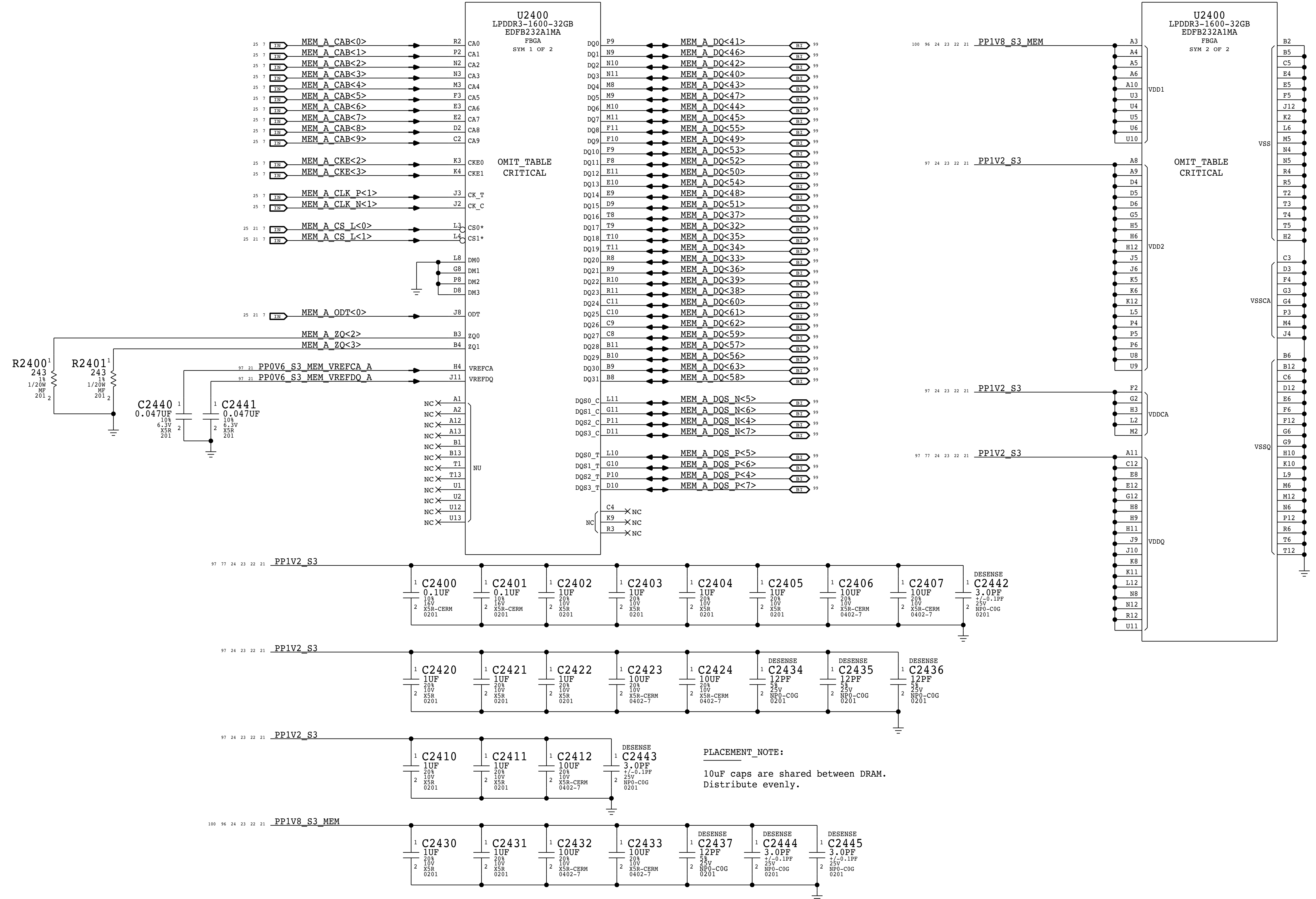
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SYNC MASTER=J79A MLB		SYNC DATE=01/31/2017	
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		PAGE	24 OF 150
		SHEET	22 OF 108

BOM_COST_GROUP=DRAM

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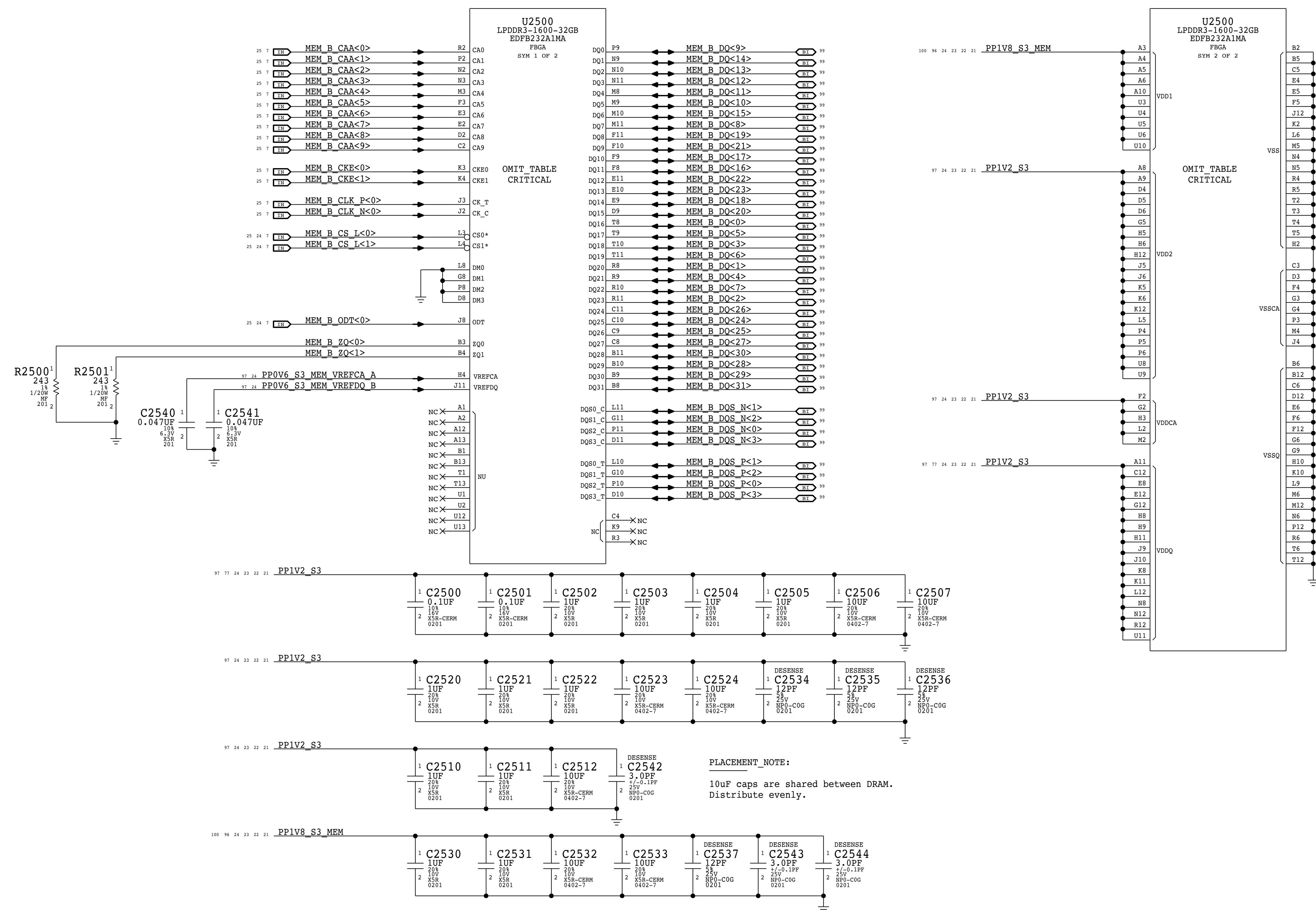
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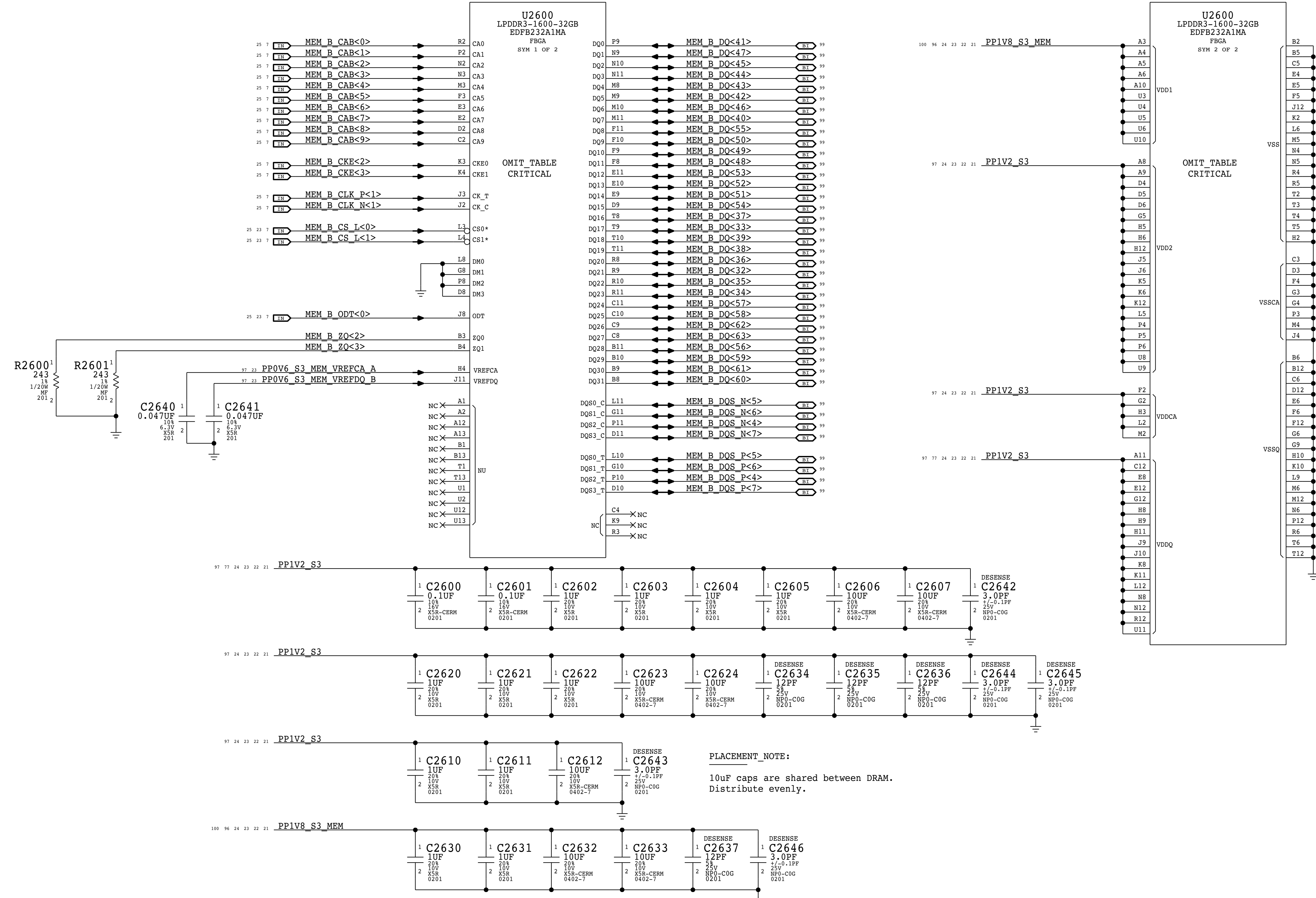
LPDDR3 CHANNEL B (0-31)



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LPDDR3 DRAM Channel B (00-31)					
		DRAWING NUMBER	051-02166	SIZE	D
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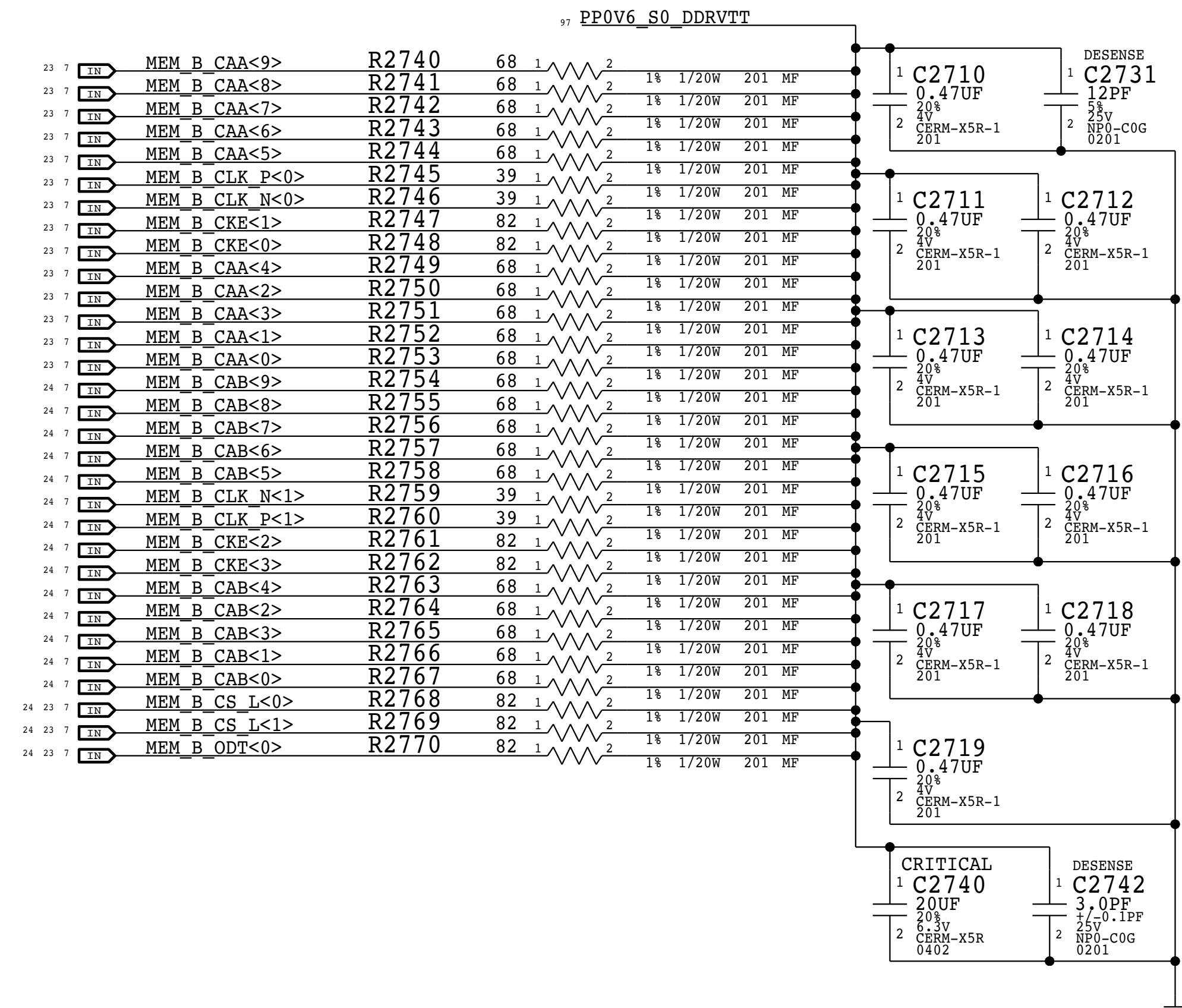
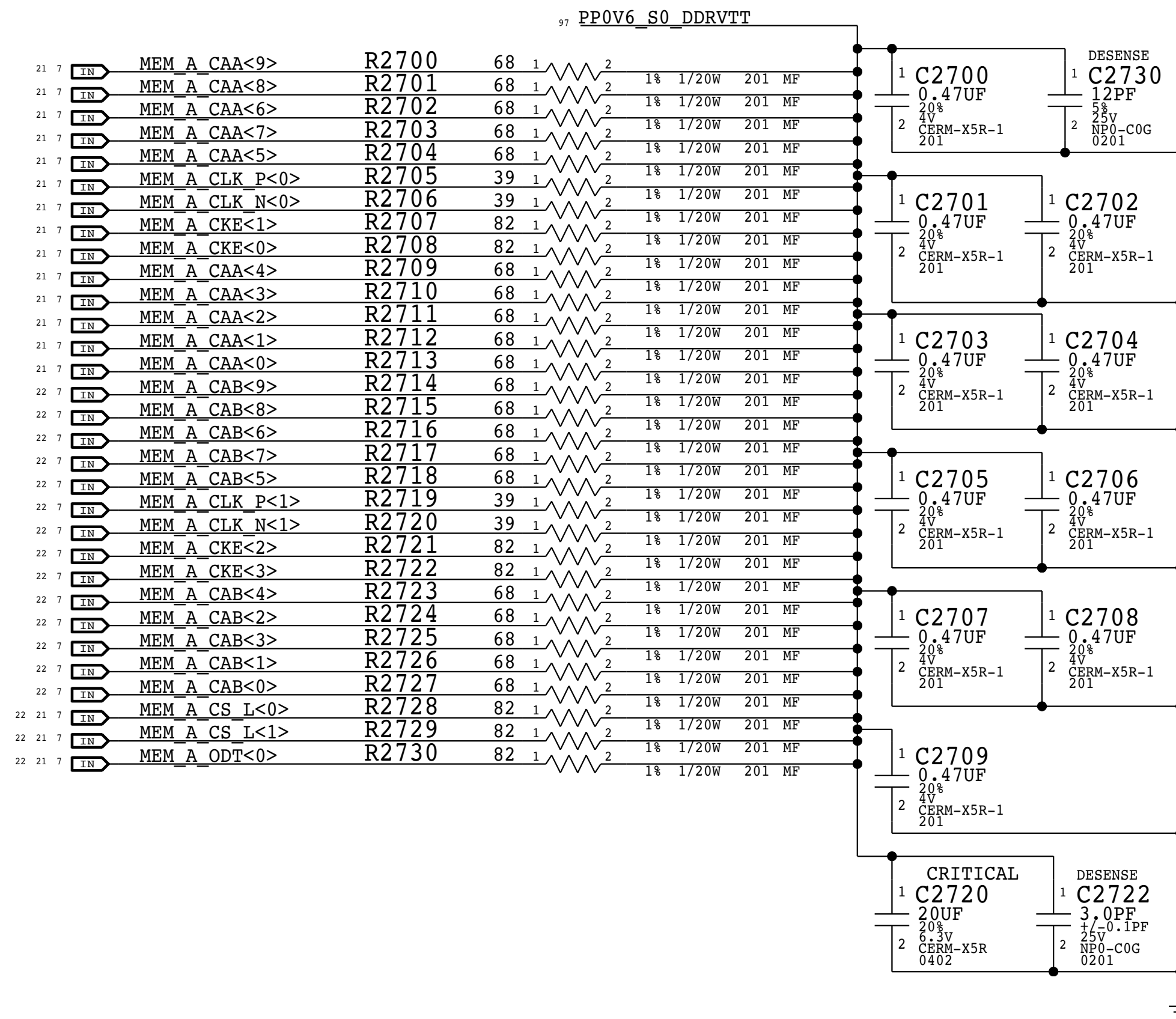
LPDDR3 CHANNEL B (32-63)



SYNC MASTER=J79A MLB		SYNC DATE=01/31/2017	
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LPDDR3 DRAM Channel B (32-63)			
Apple Inc.	DRAWING NUMBER	051-02166	SIZE
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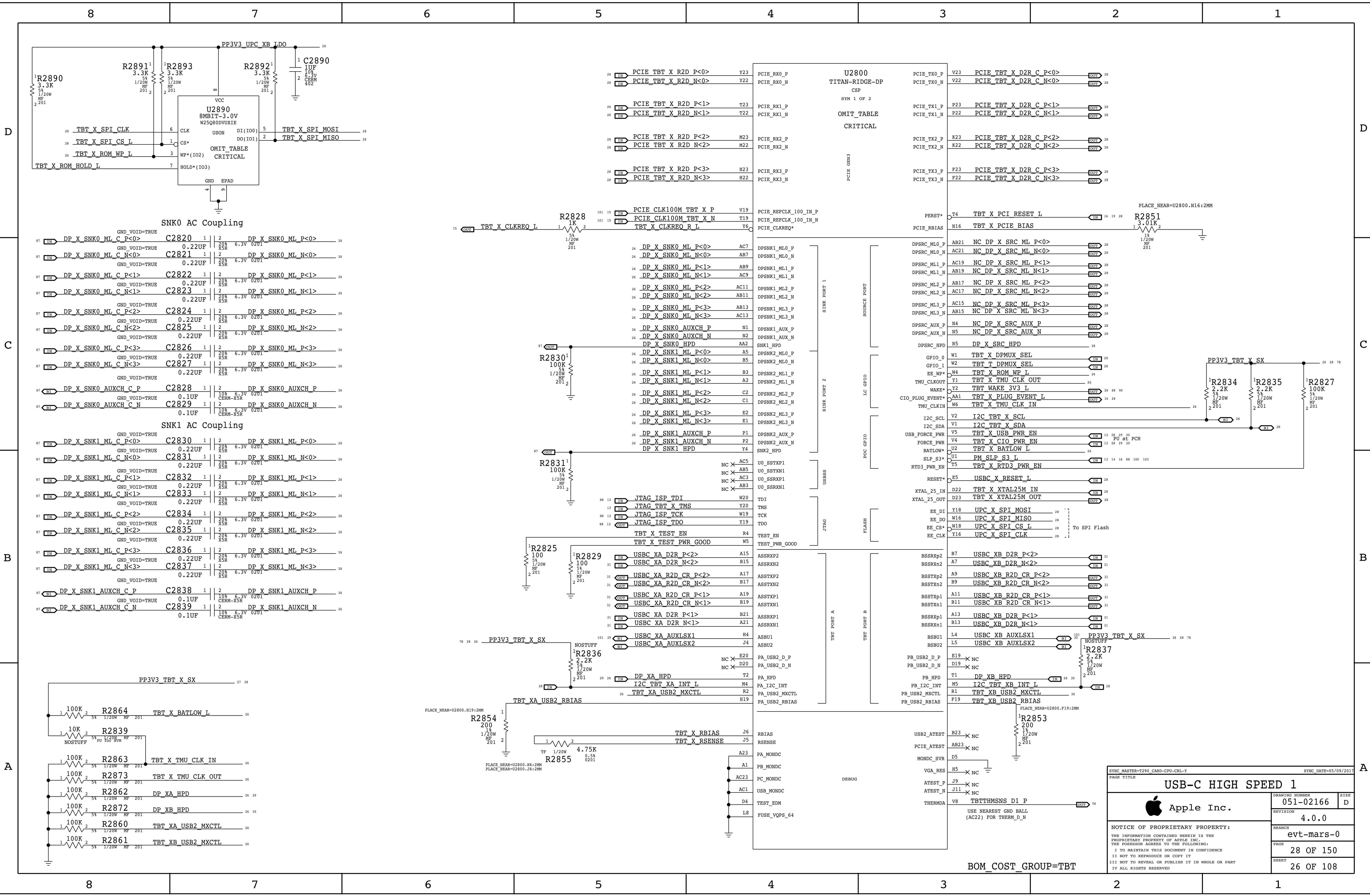
BOM_COST_GROUP=DRAM

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK



SYNC MASTER=J79A MLB		SYNC DATE=01/31/2017	
PAGE TITLE LPDDR3 DRAM Termination			
	DRAWING NUMBER	051-02166	
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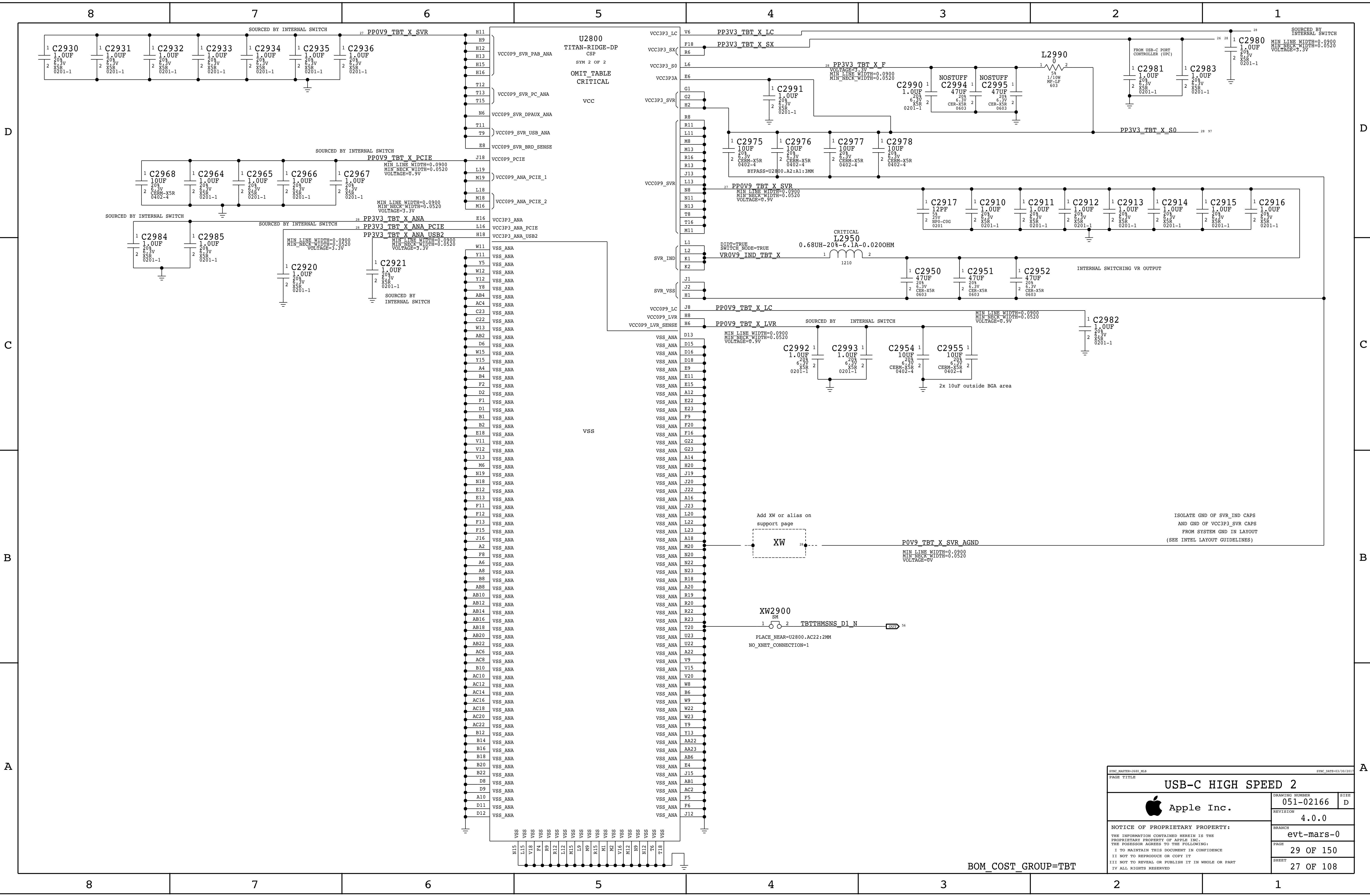


SNK0 AC Coupling

SNK1 AC Coupling

BOM_COST_GROUP=TBT

		DRAWING NUMBER 051-02166	SIZE D
REVISION 4.0.0		BRANCH evt-mars-0	
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PAGE TITLE			
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BOM_COST_GROUP=TBT

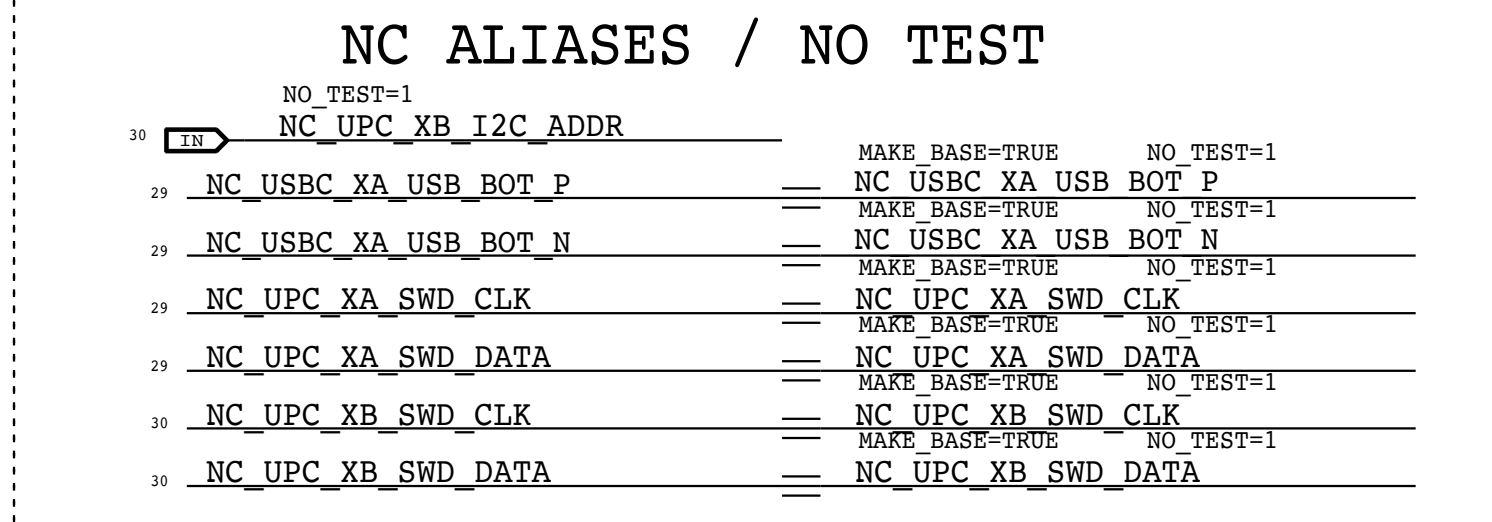
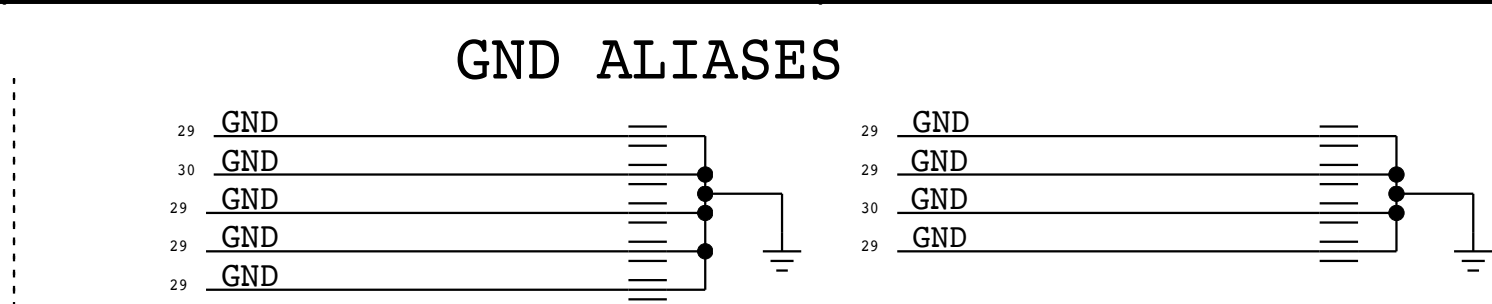
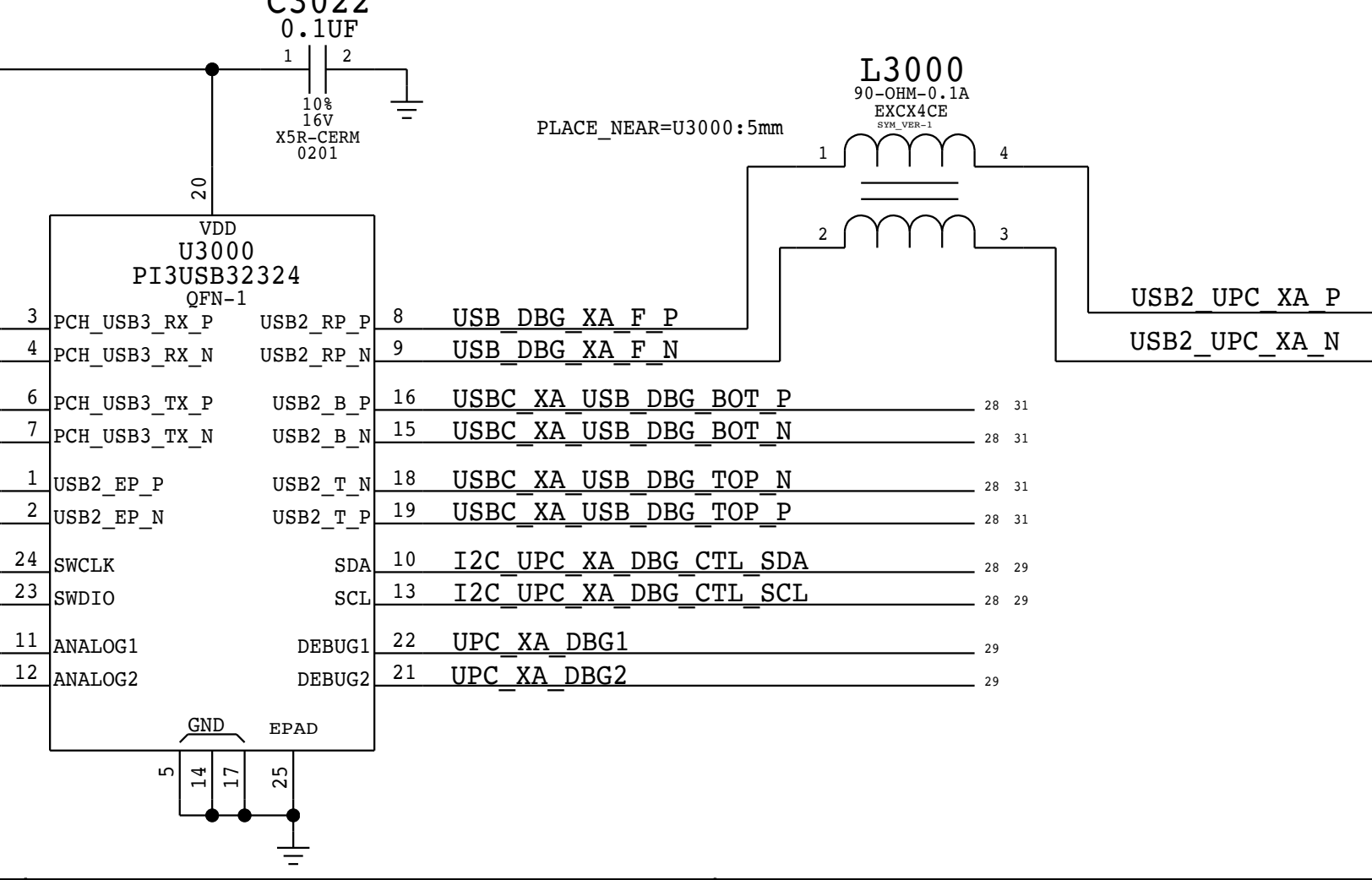
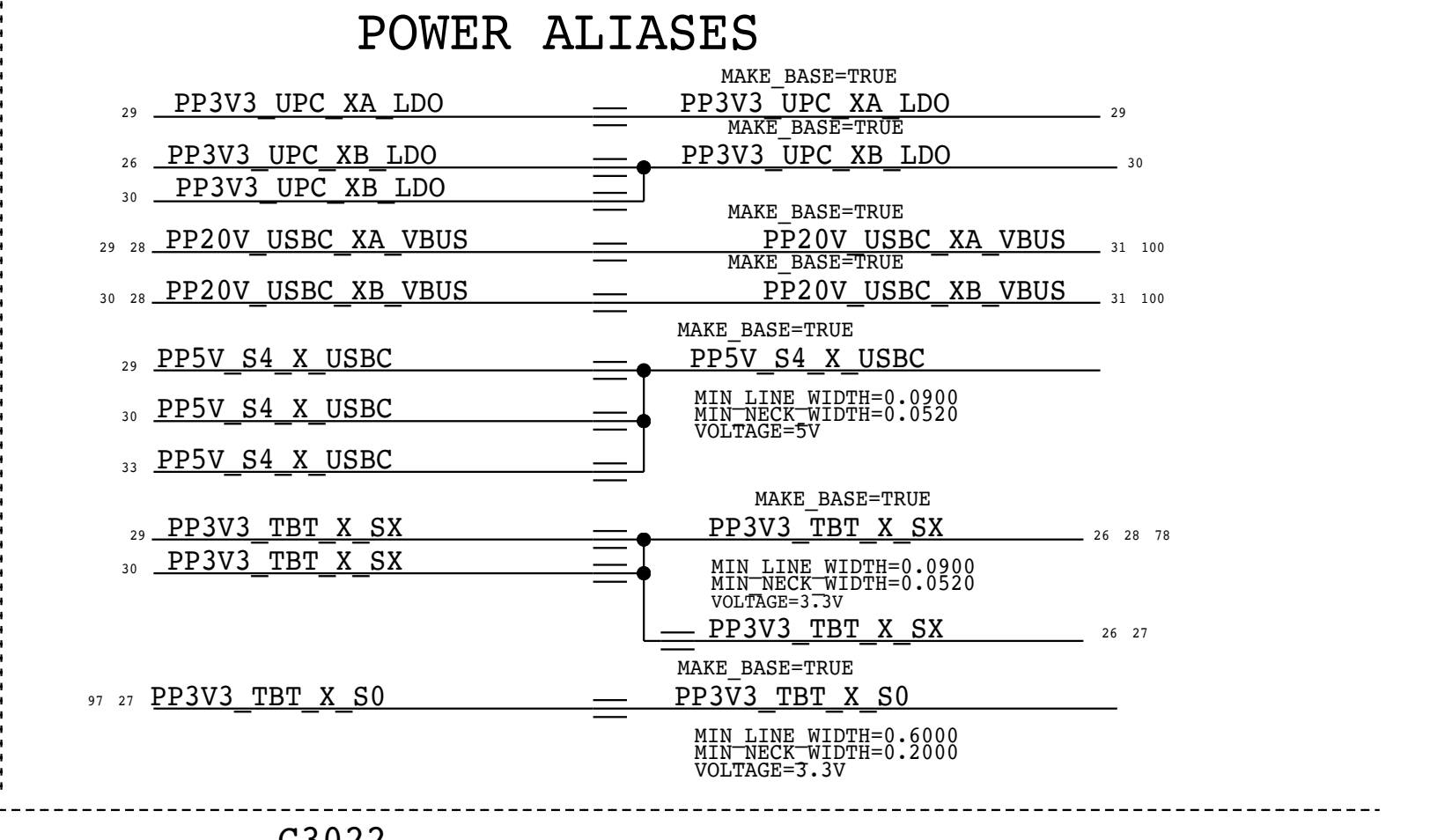
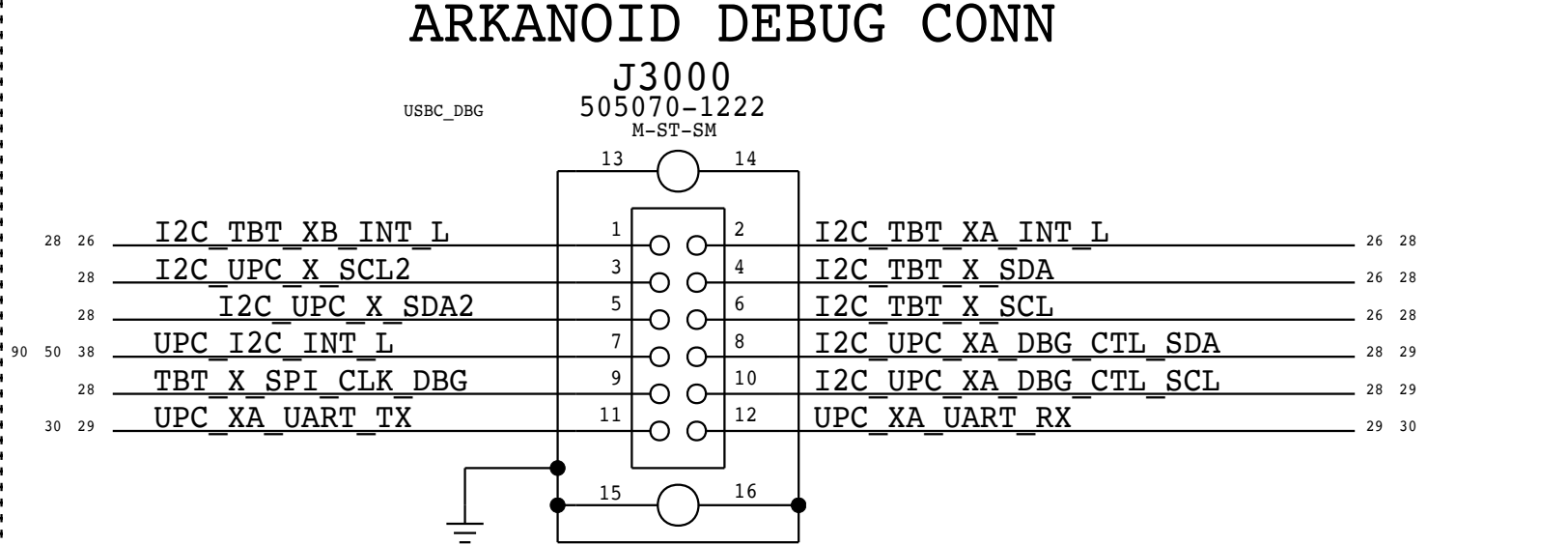
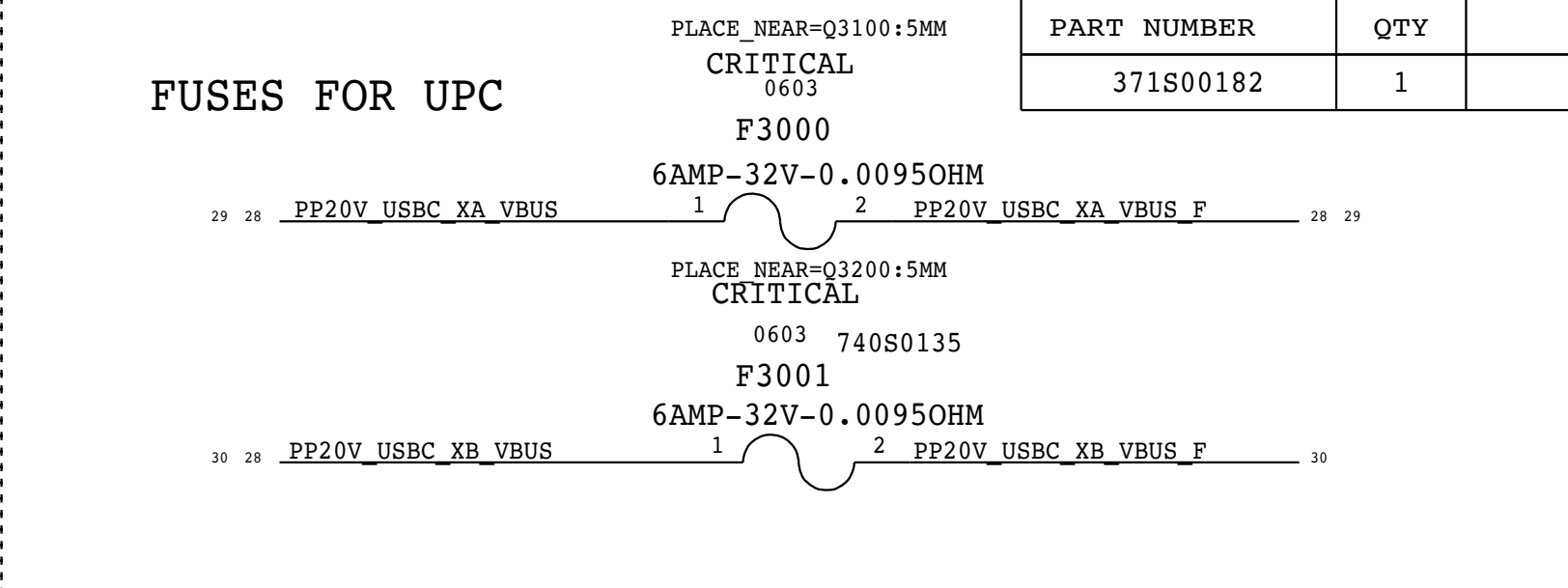
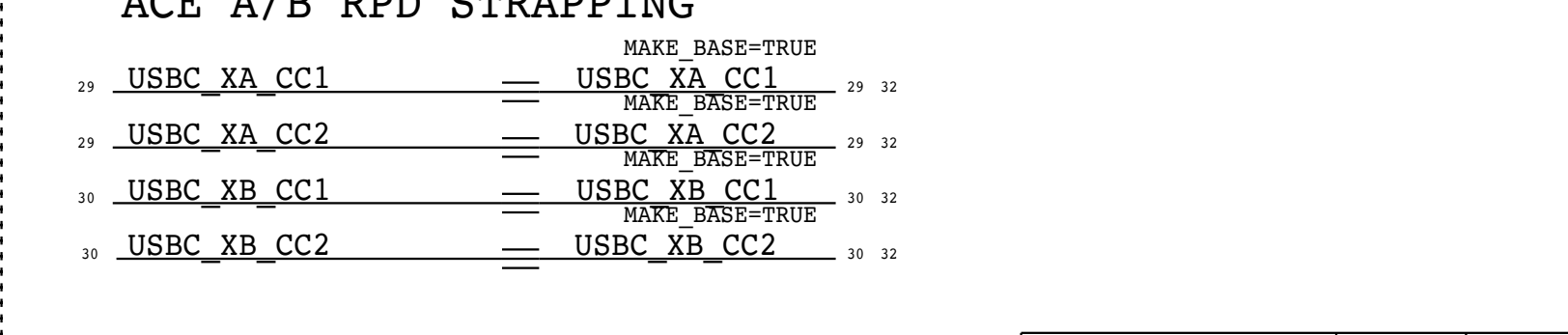
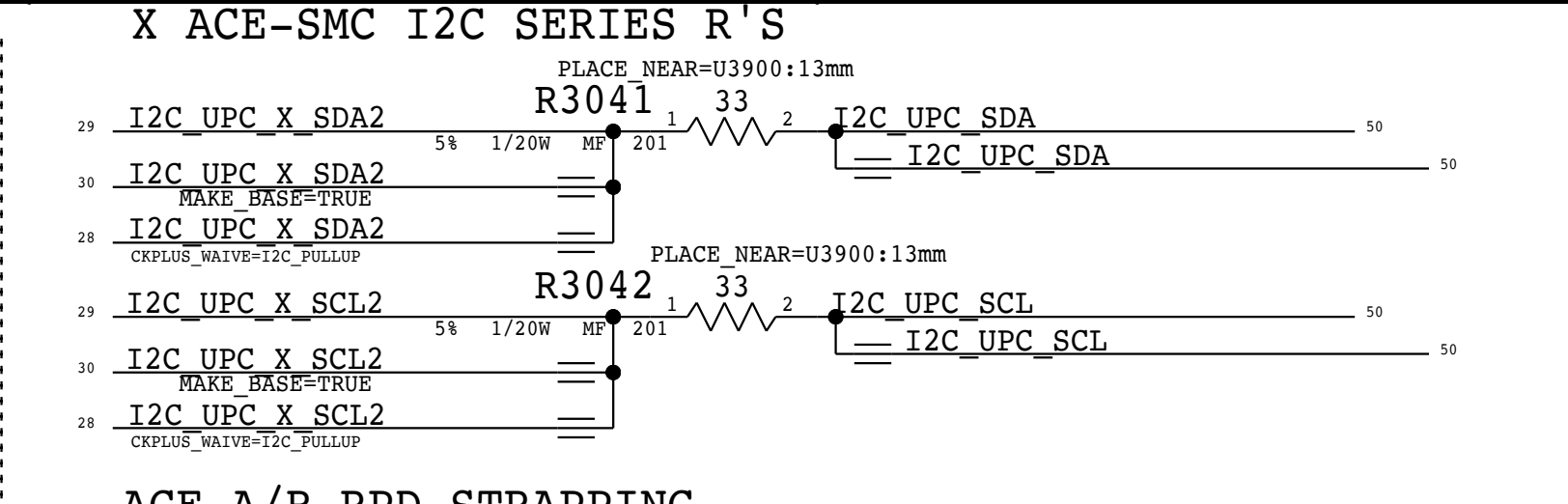
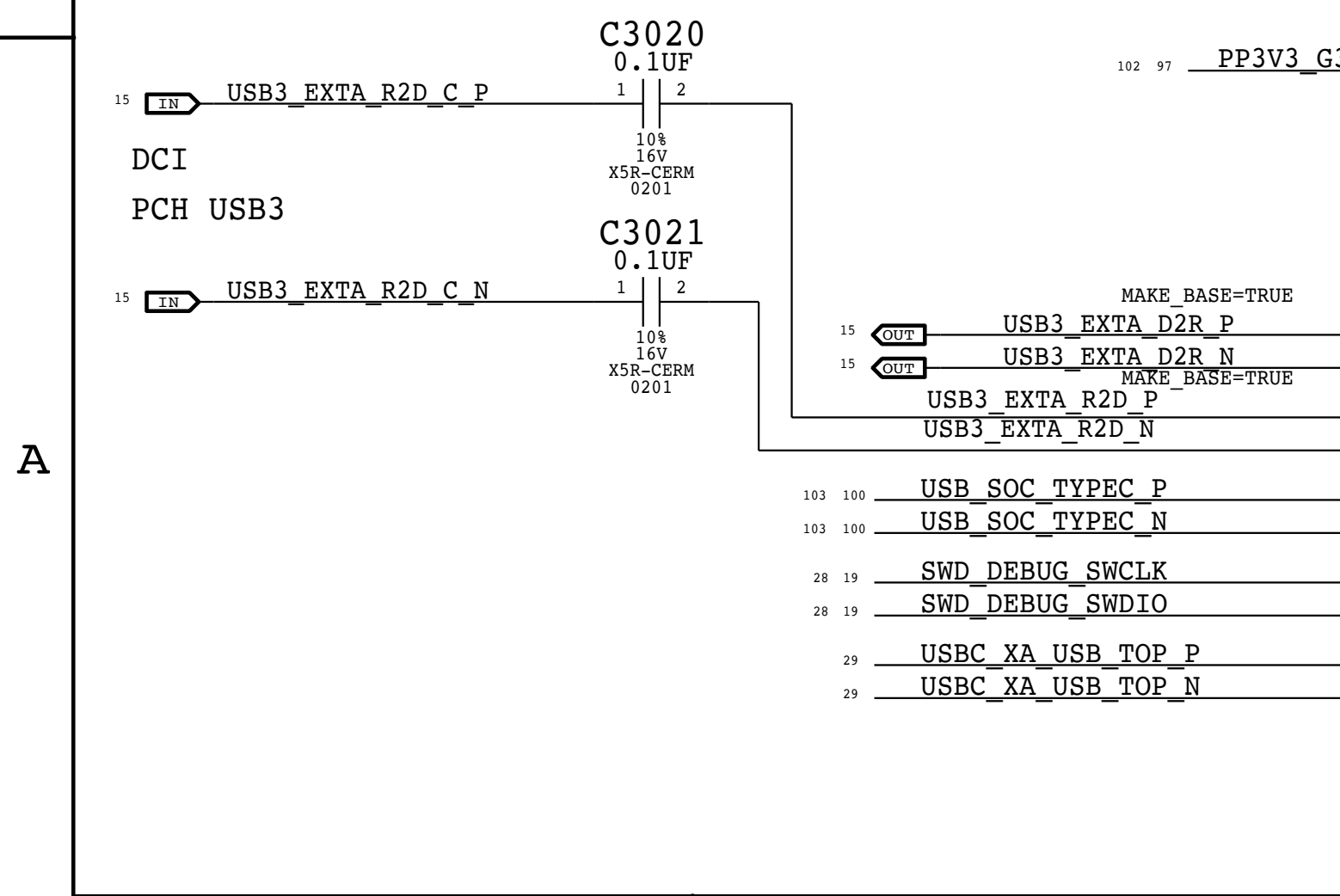
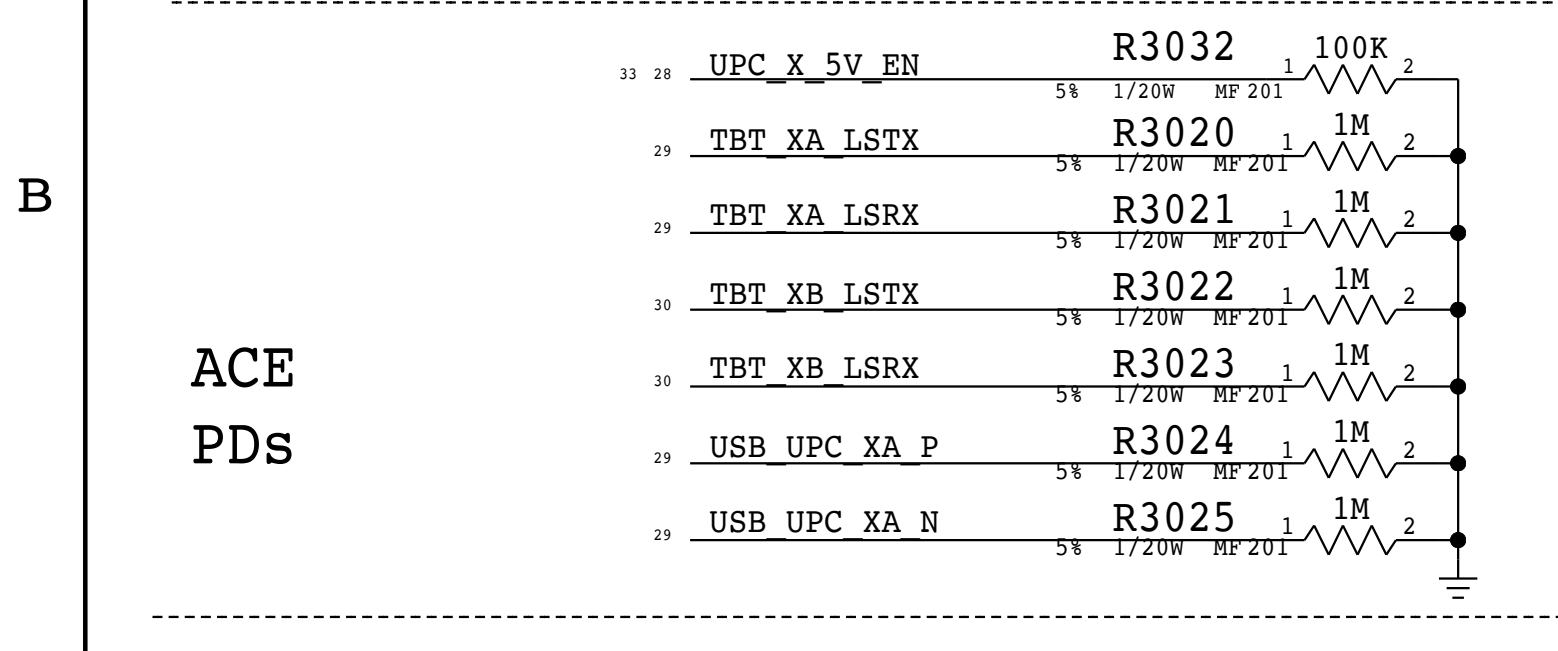
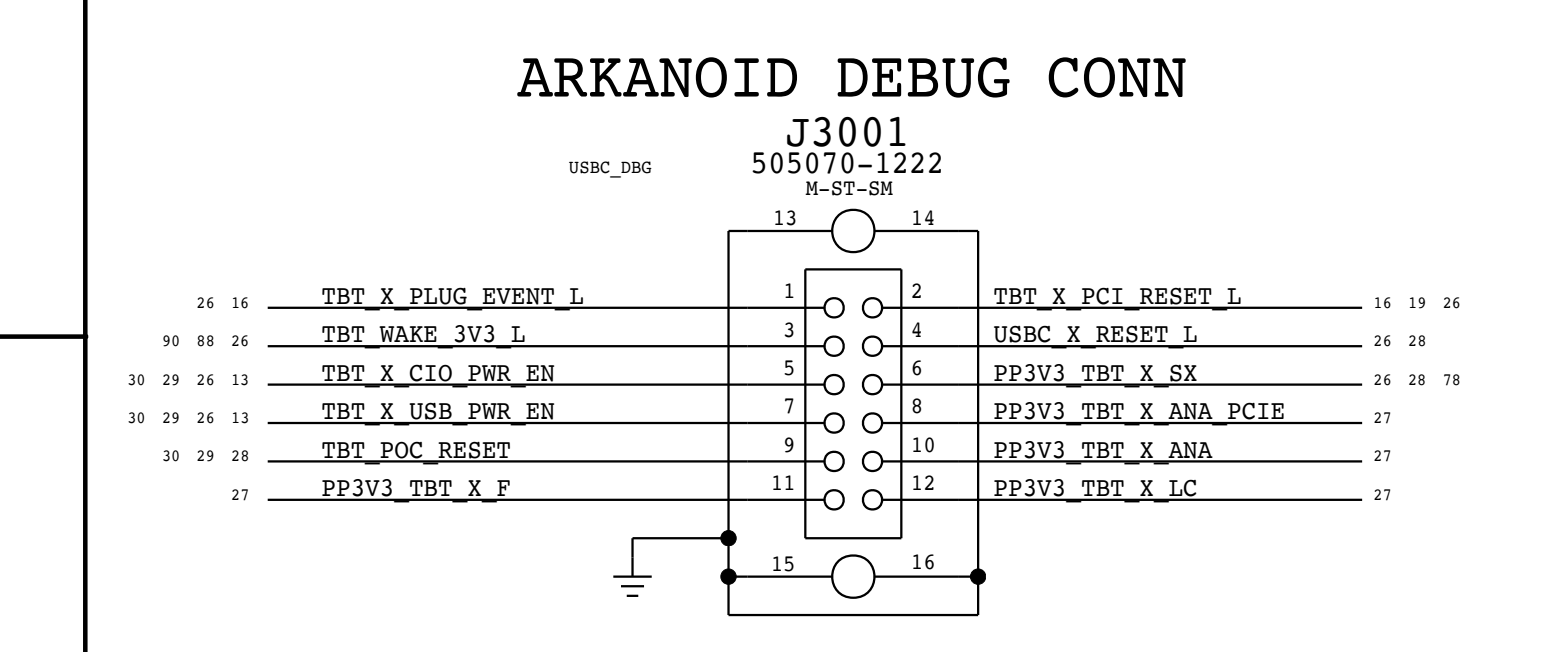
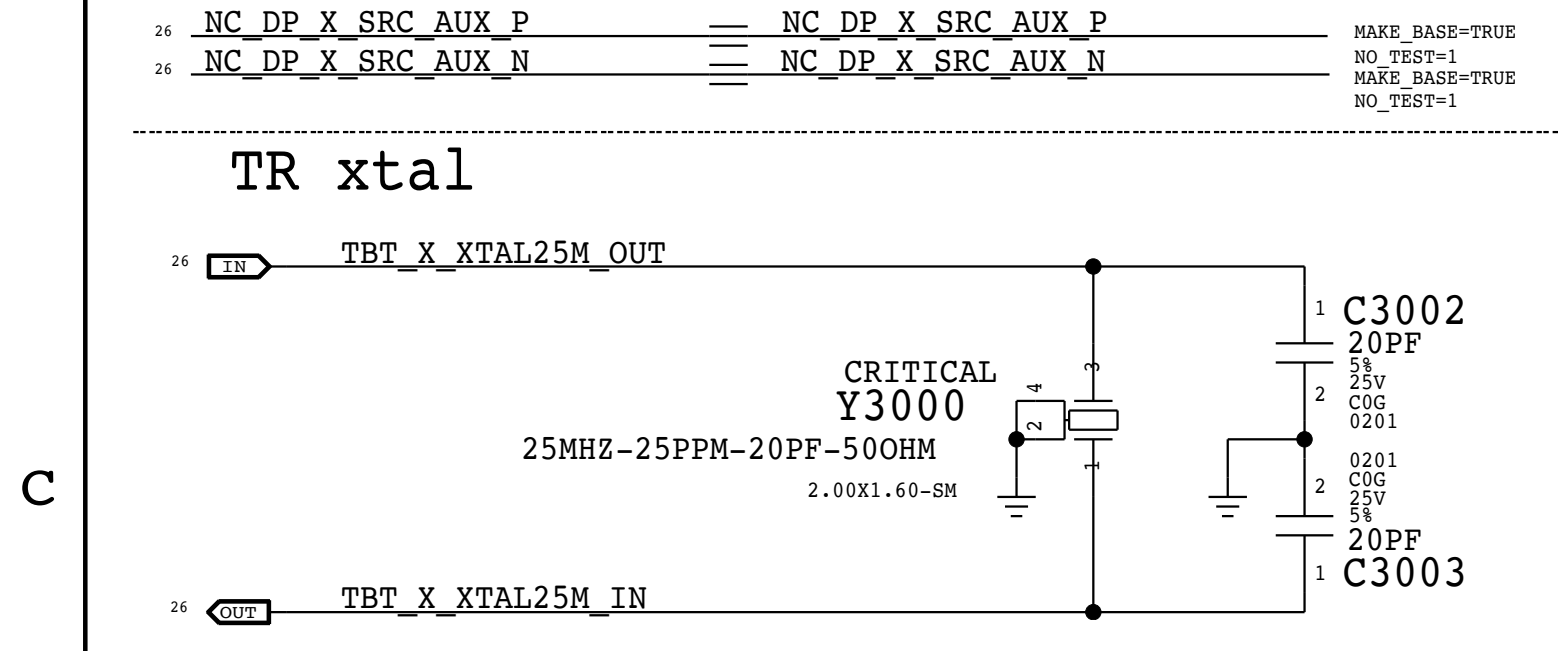
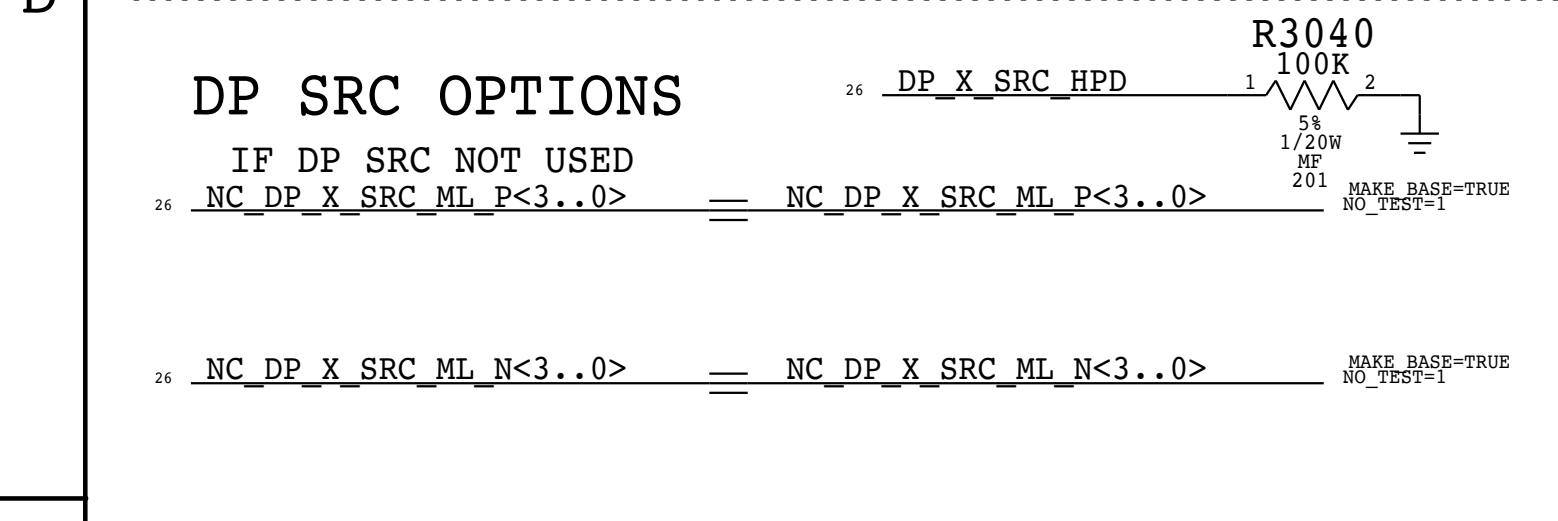
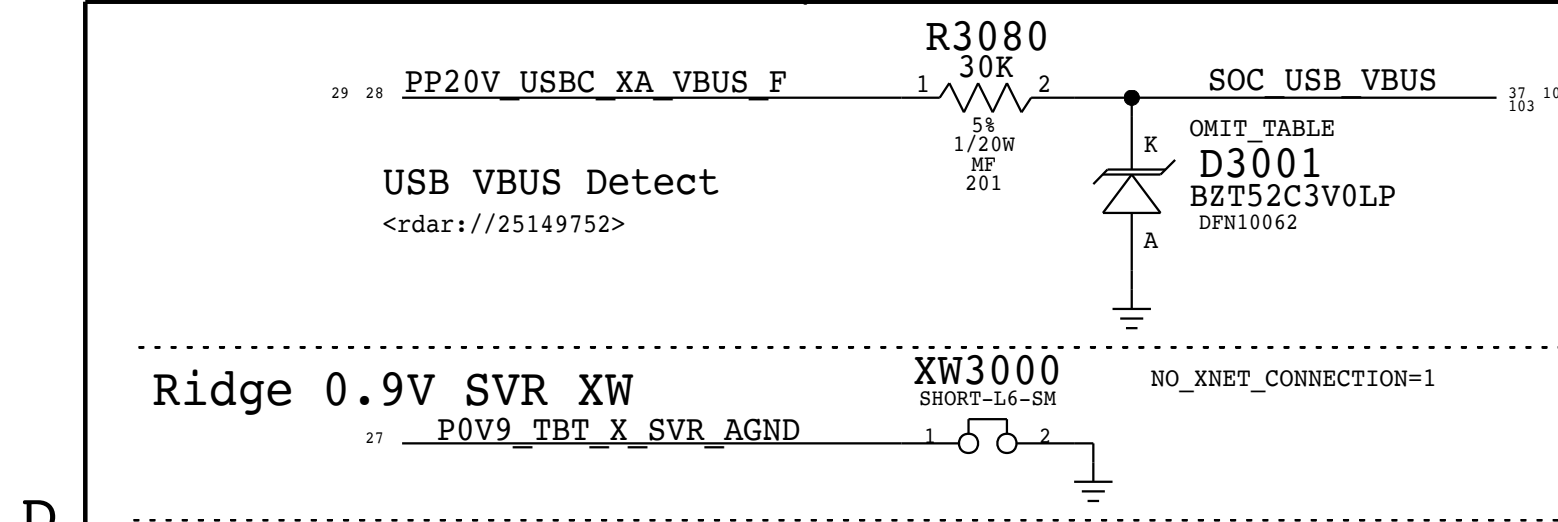
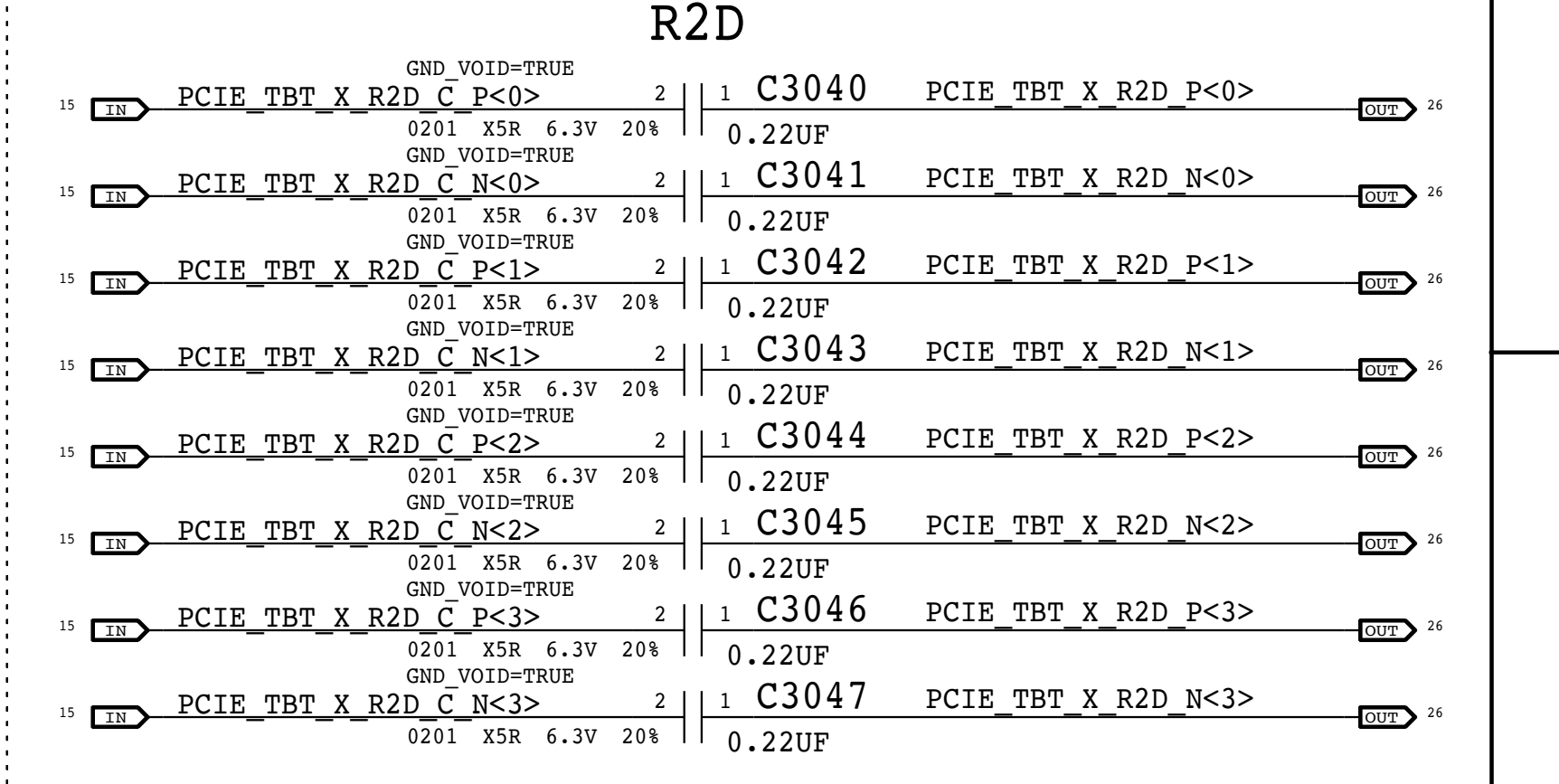
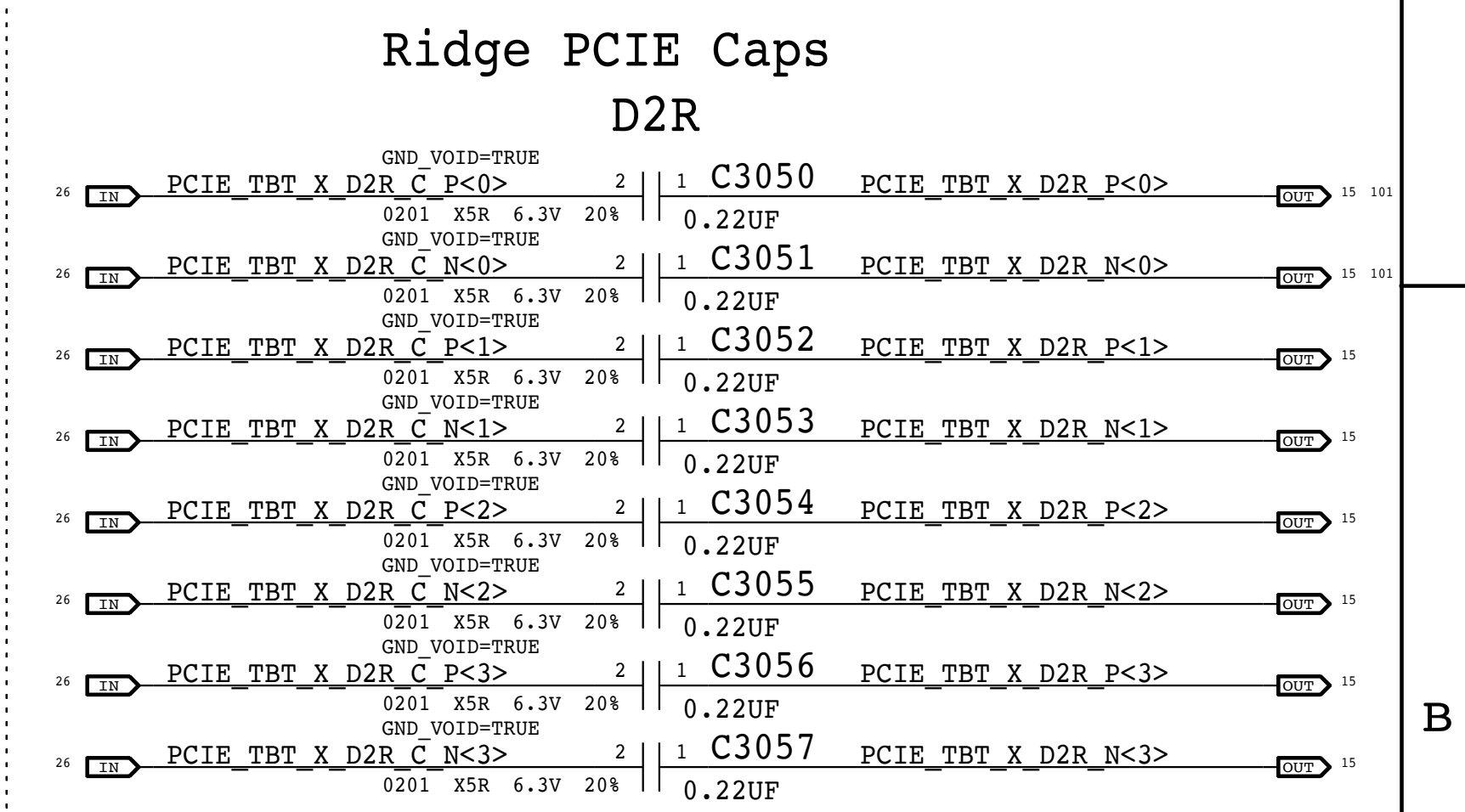
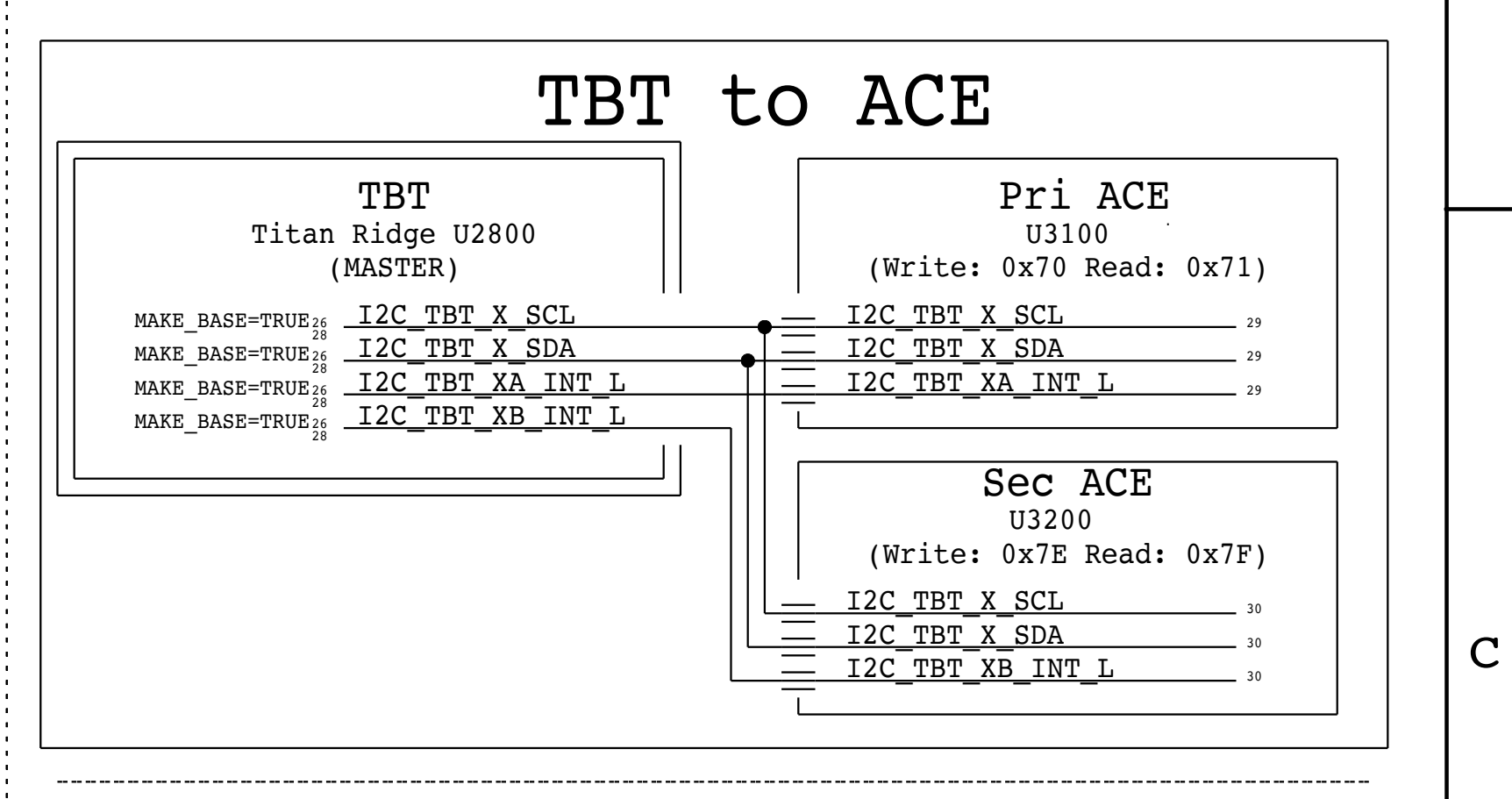
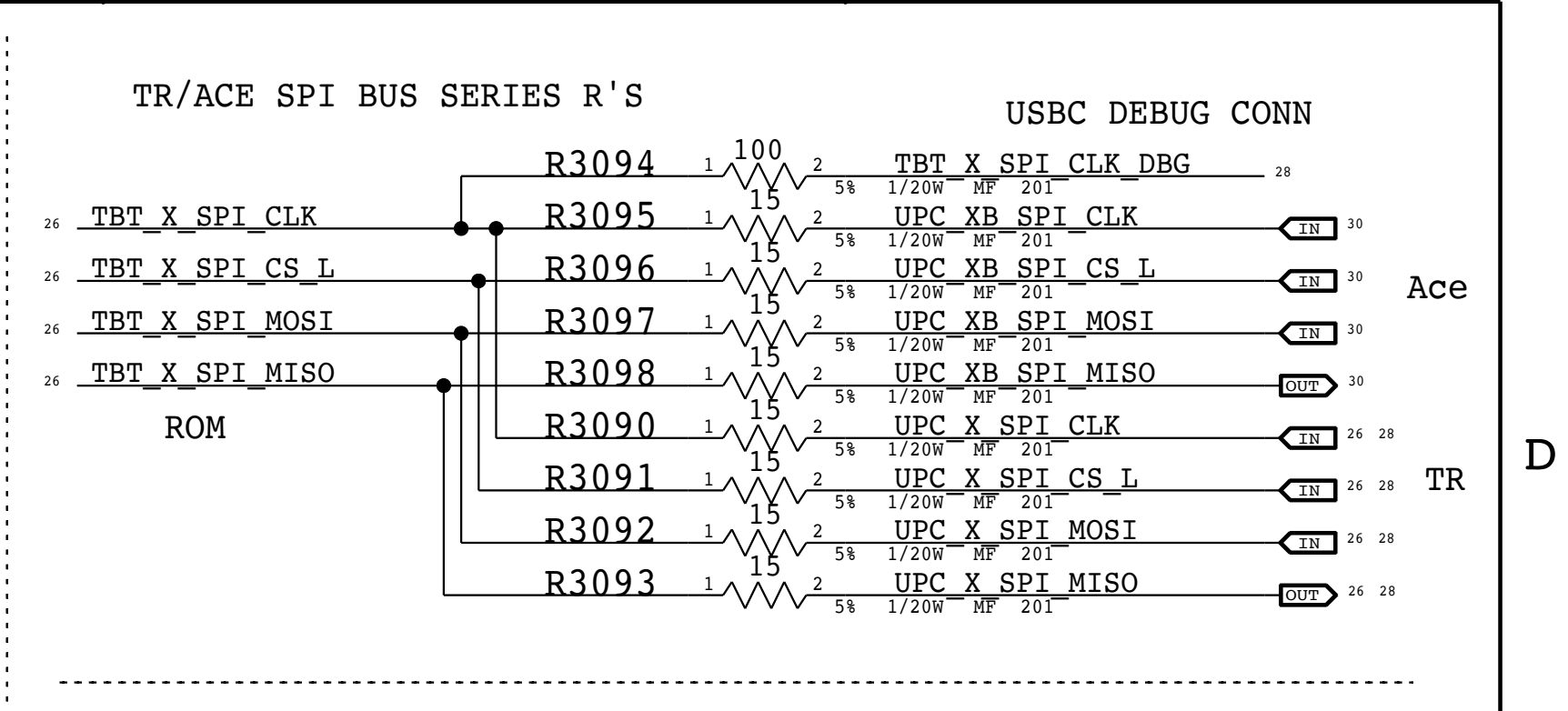
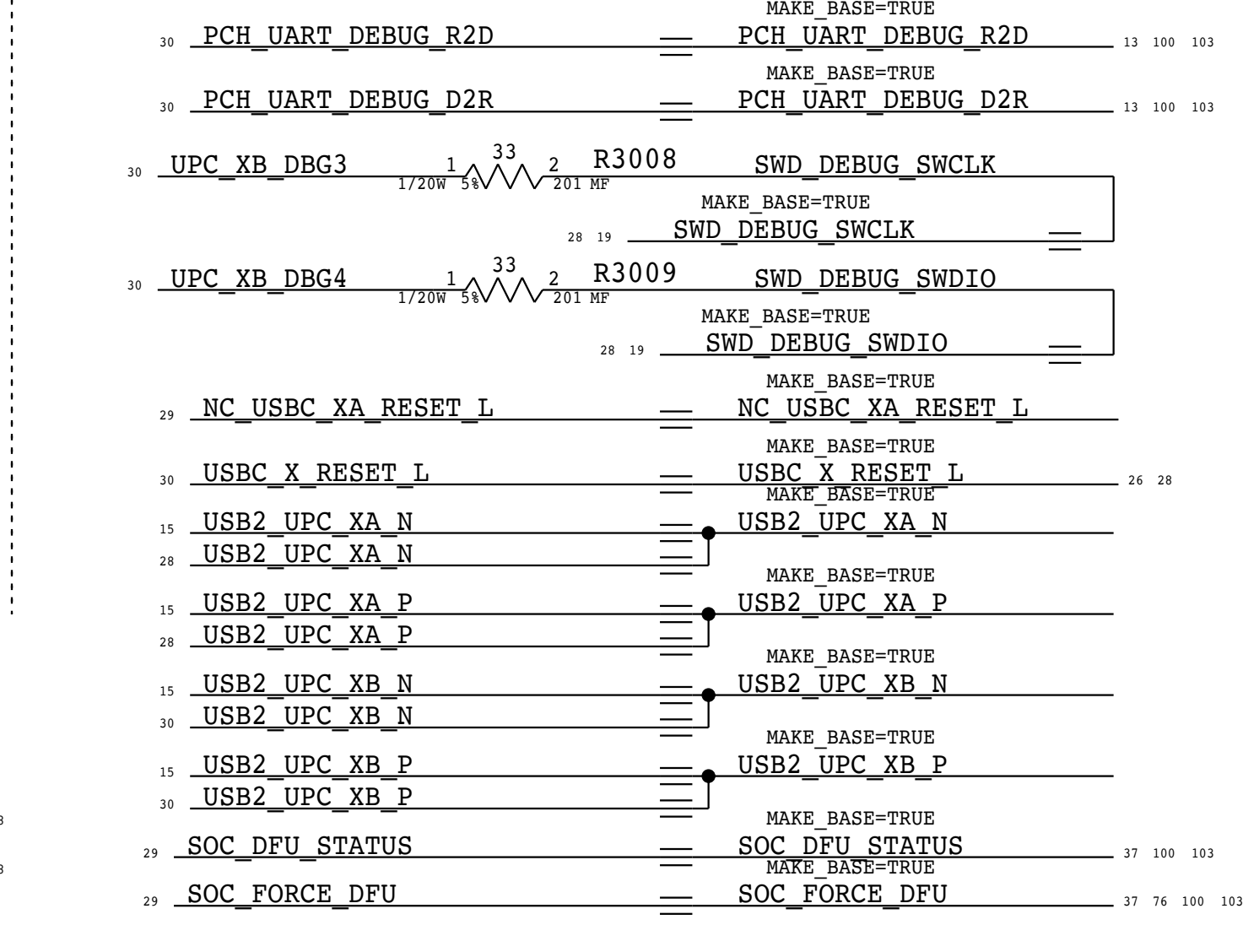
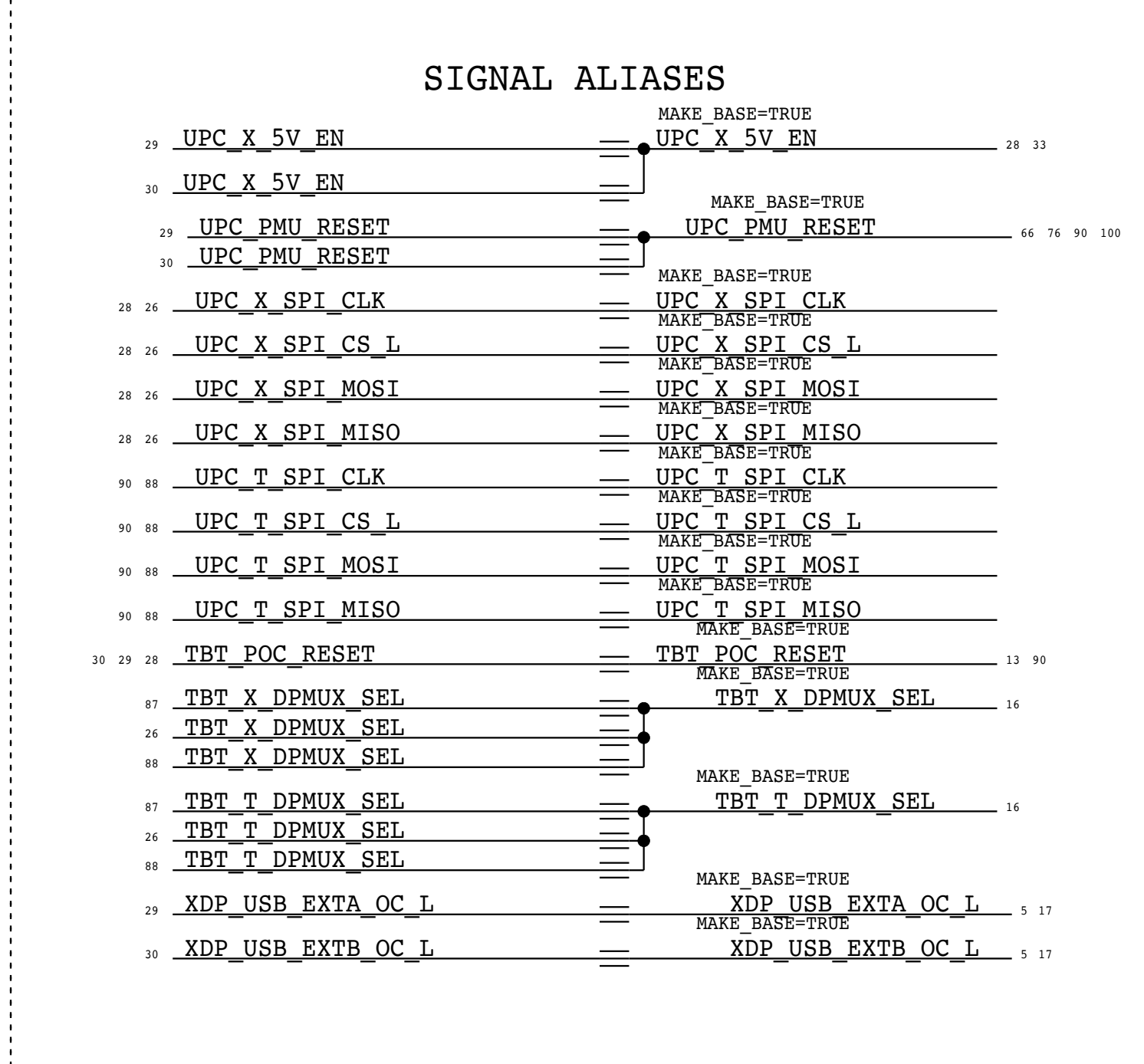
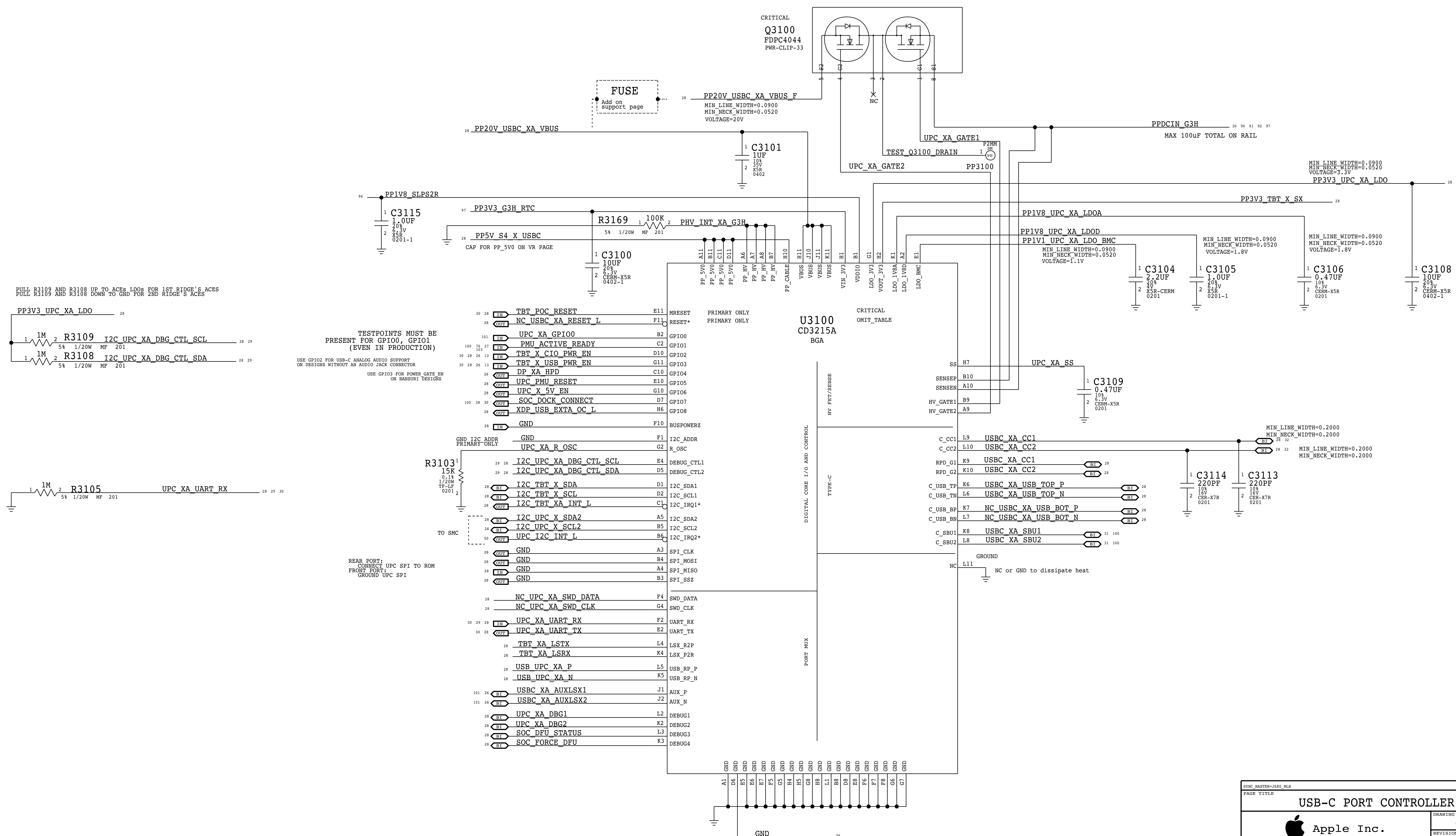


Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Row 1: 371S00182, 1, D3001, D3001, NO, NO.



USB-C Support header with Apple logo, drawing number 051-02166, revision 4.0.0, and page 30 of 150.

PRIMARY ACE USB-C PORT CONTROLLER (UPC)



PULL R3109 AND R3108 UP TO ACES LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XA_LDO

1M R3109 I2C_UPC_XA_DBG_CTL_SCL
5% 1/20W MF 201

1M R3108 I2C_UPC_XA_DBG_CTL_SDA
5% 1/20W MF 201

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANBUKI DESIGNS

UPC_XA_UART_RX

1M R3105
5% 1/20W MF 201

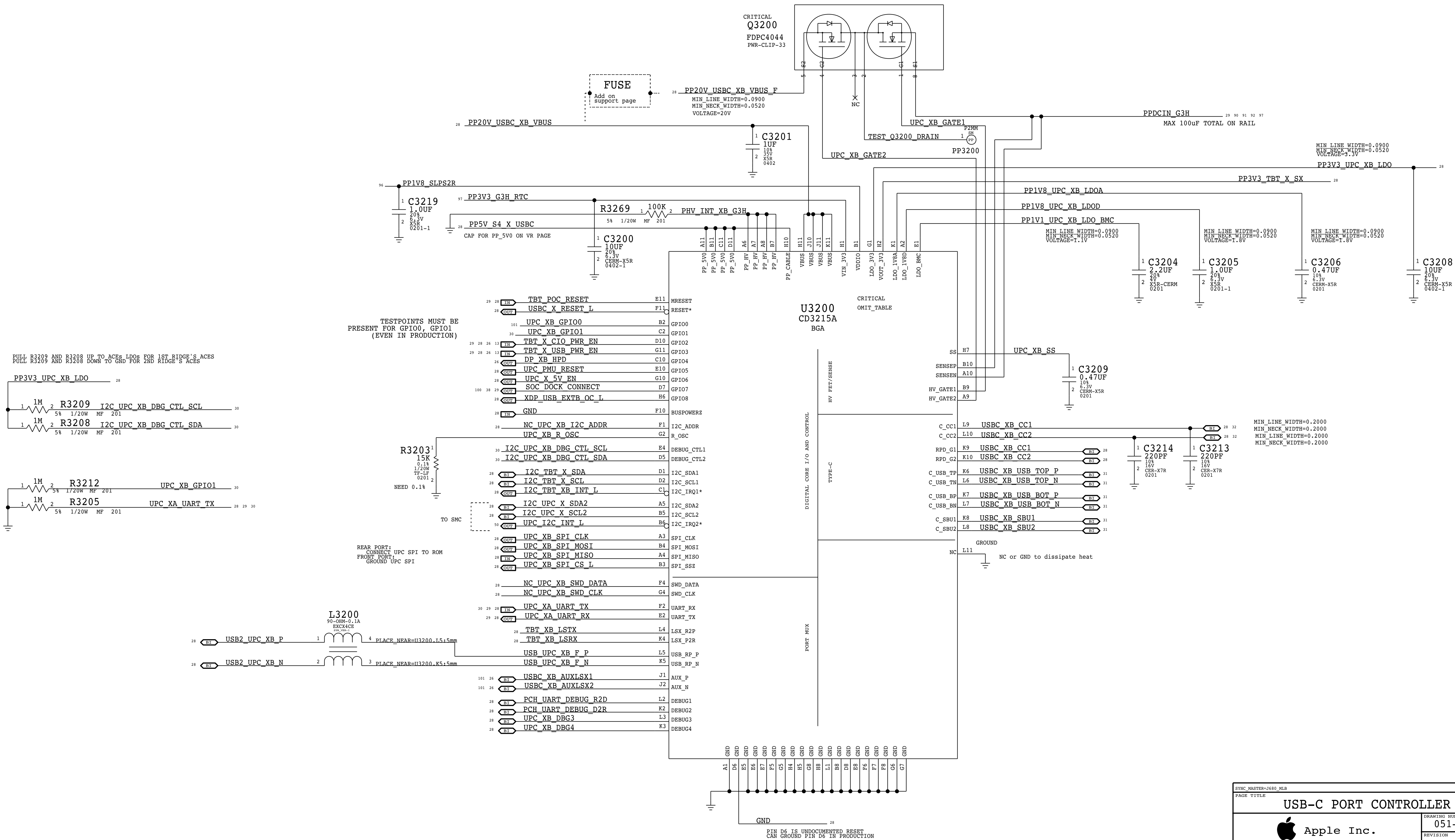
REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE		USB-C PORT CONTROLLER A	
DRAWING NUMBER		051-02166	
REVISION		4.0.0	
BRANCH		evt-mars-0	
PAGE		31 OF 150	
SHEET		29 OF 108	

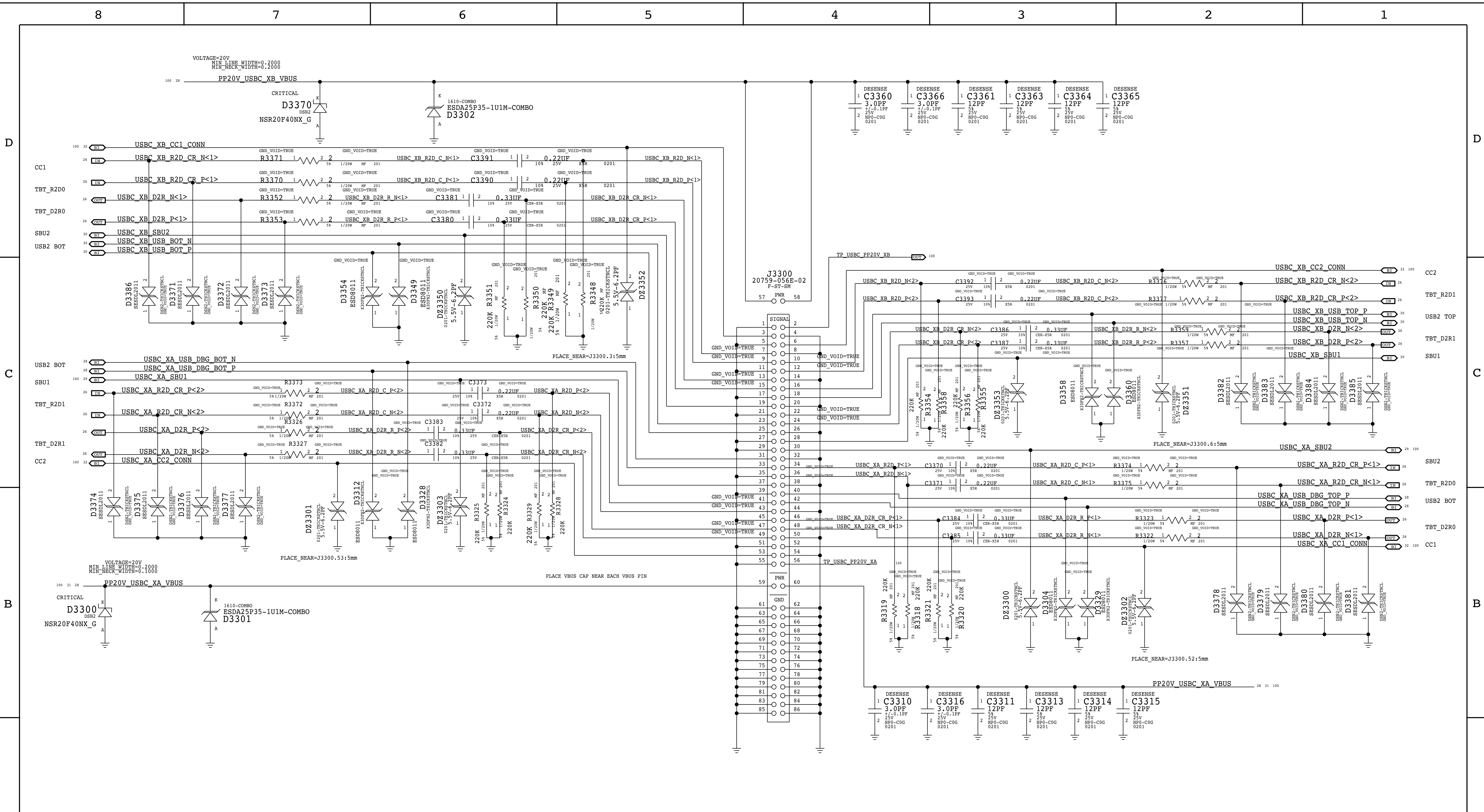
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM COST GROUP=USB-C

PAGE TITLE		DRAWING NUMBER	
USB-C PORT CONTROLLER B		051-02166	
REVISON		SIZE	
4.0.0		D	
BRANCH		PAGE	
evt-mars-0		32 OF 150	
SHEET		30 OF 108	
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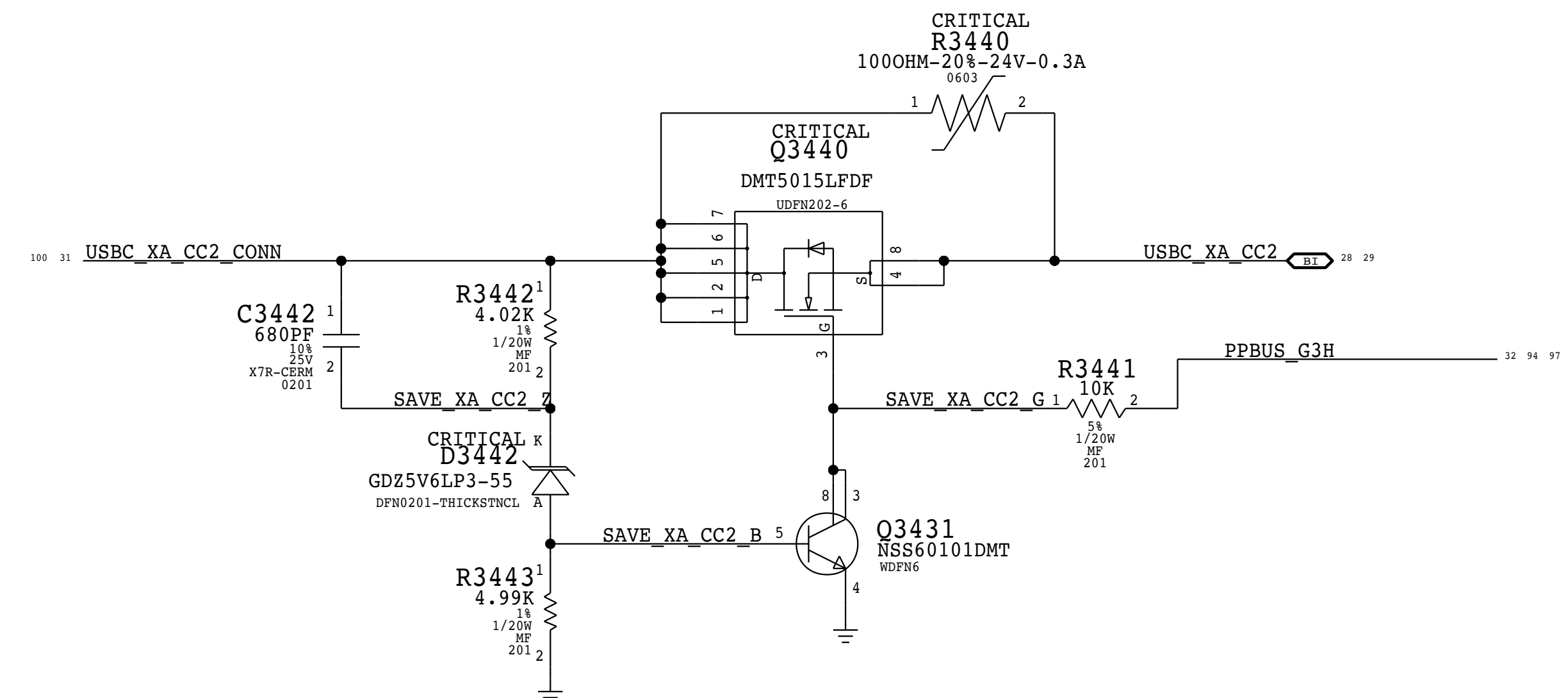
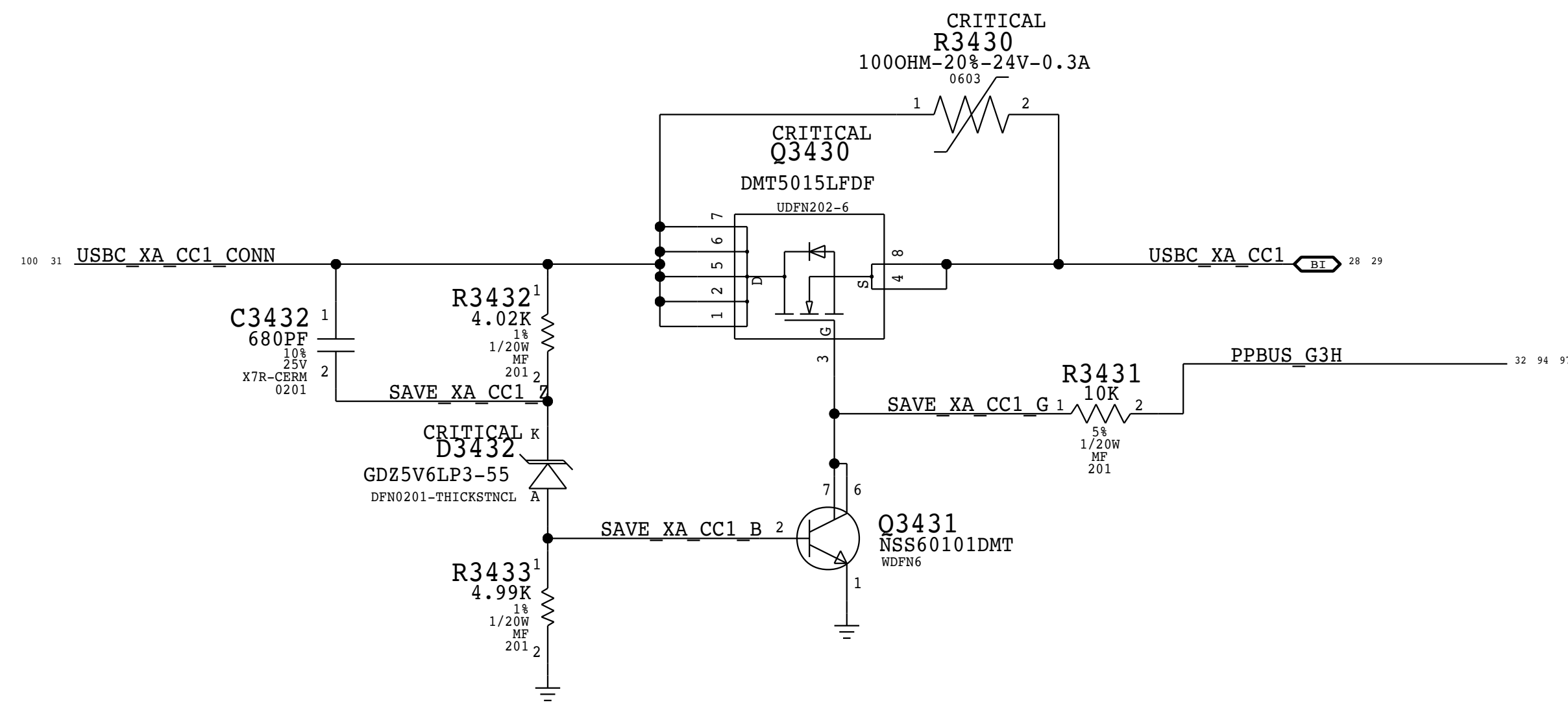
PIN D6 IS UNDOCUMENTED RESET CAN GROUND PIN D6 IN PRODUCTION



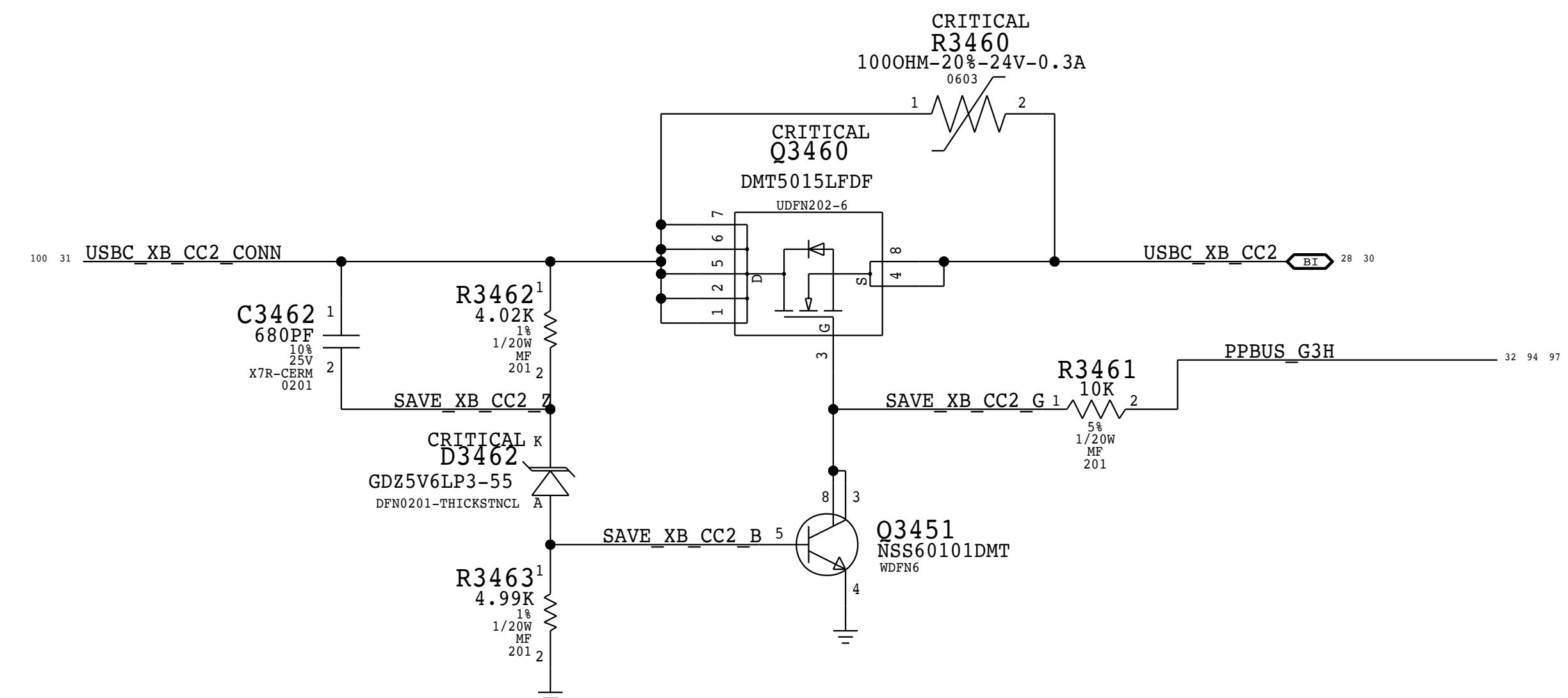
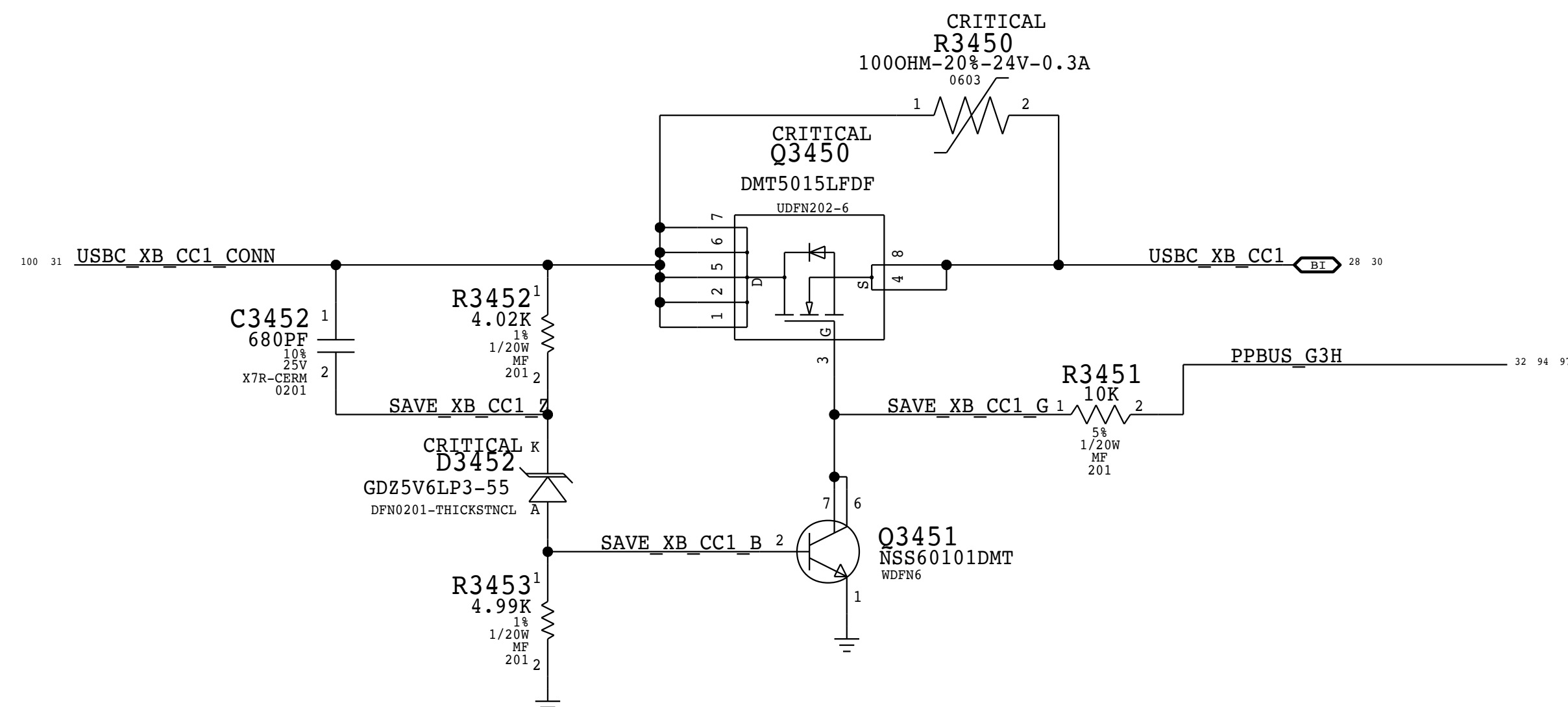
LAST CHANGE: Wed Apr 1 22:57:37 2015		
PAGE TITLE		
USB-C CONNECTOR A		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	33 OF 150
	SHEET	31 OF 108

BOM_COST_GROUP=USB-C

XA CC Protection

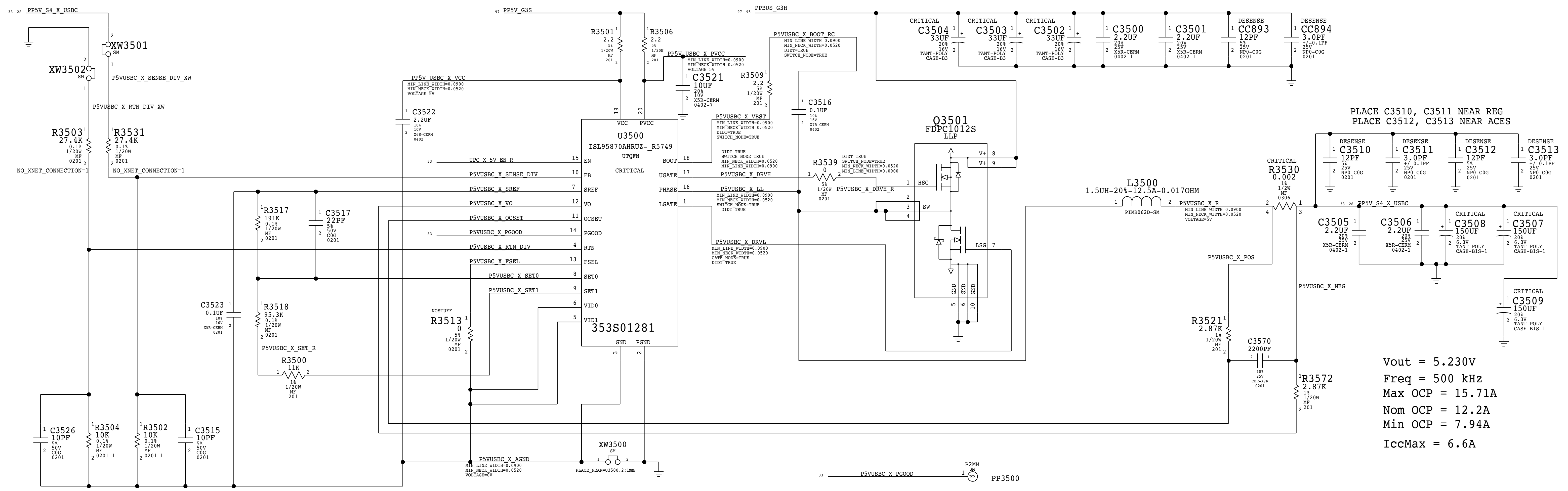


XB CC Protection



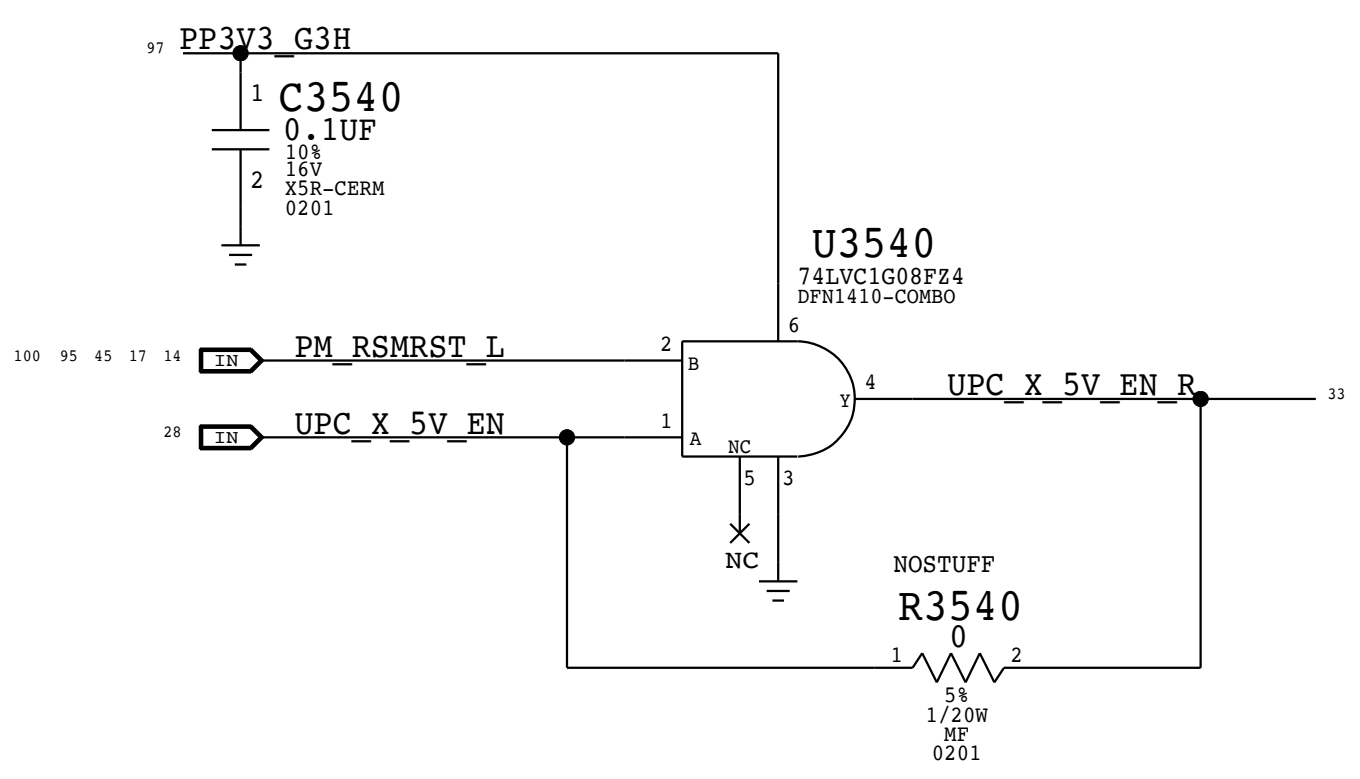
DESIGN: X1032/MLB P4BP		
LAST CHANGE: Fri Jan 6 16:01:21 2017		
PAGE TITLE		
USBC X Connector Support		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	34 OF 150
	SHEET	32 OF 108

BOM_COST_GROUP=USB-C



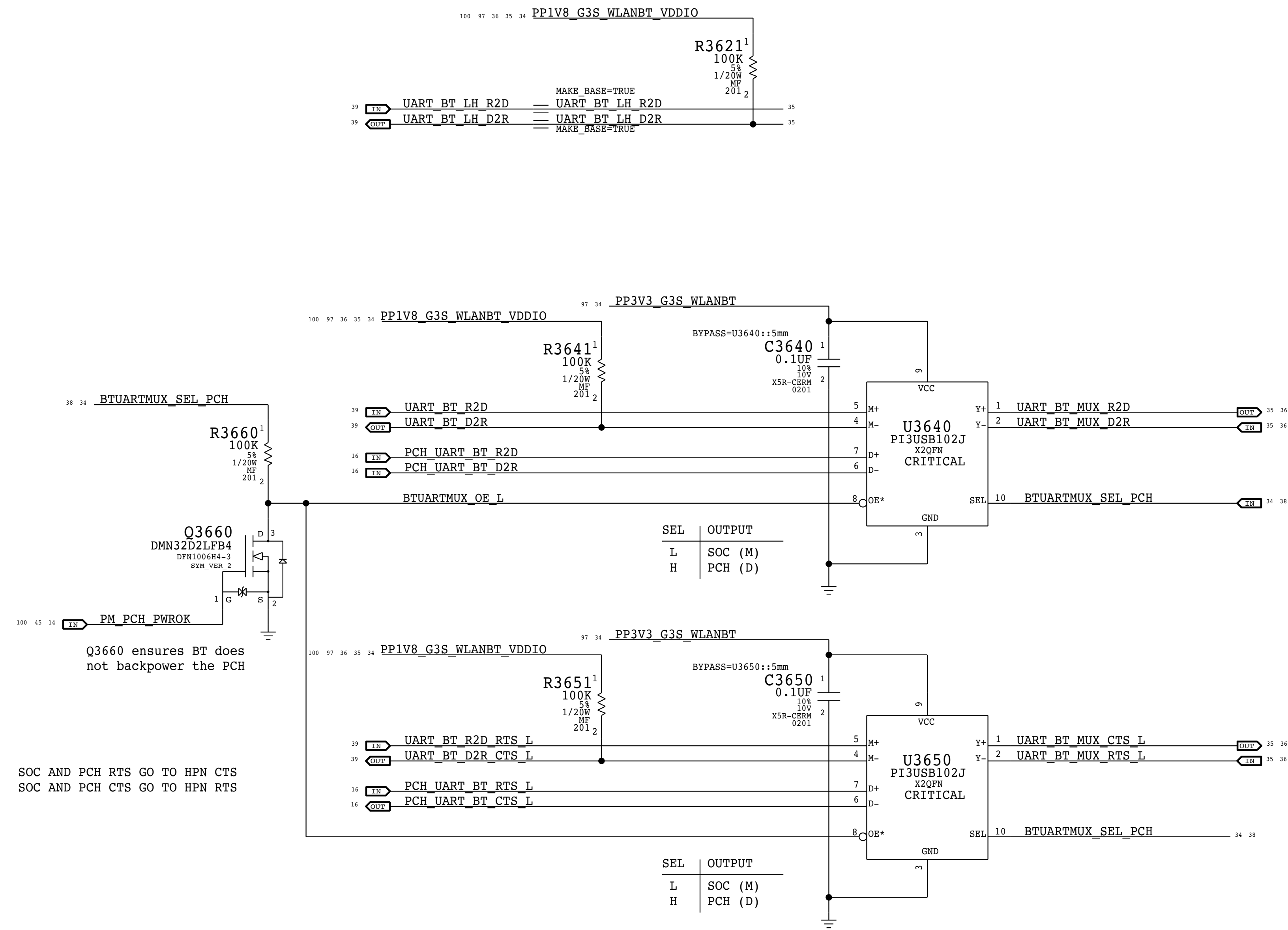
Vout = 5.230V
 Freq = 500 kHz
 Max OCP = 15.71A
 Nom OCP = 12.2A
 Min OCP = 7.94A
 IccMax = 6.6A

UPC X 5V EN QUALIFIER



PAGE TITLE		
TBT 5V REGULATOR		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	35 OF 150
	SHEET	33 OF 108

Software	I2S_SEL	UART_SEL	I2S I/F	UART I/F
Gen1 (macOS)	0	1	UART (PCH)	UART (PCH)
Gen1 (Bootcamp)	1	1	I2S (PCH)	UART (PCH)
Gen2	X	0	X	UART (SOC)



PAGE TITLE		SYNC_MASTER=J132_JACK		SYNC_DATE=05/30/2017	
WIFI/BT: Support					
		DRAWING NUMBER	051-02166	SIZE	D
		REVISION	4.0.0		
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		PAGE	36 OF 150		
		SHEET	34 OF 108		

BOM_COST_GROUP=WIRELESS

D

C

B

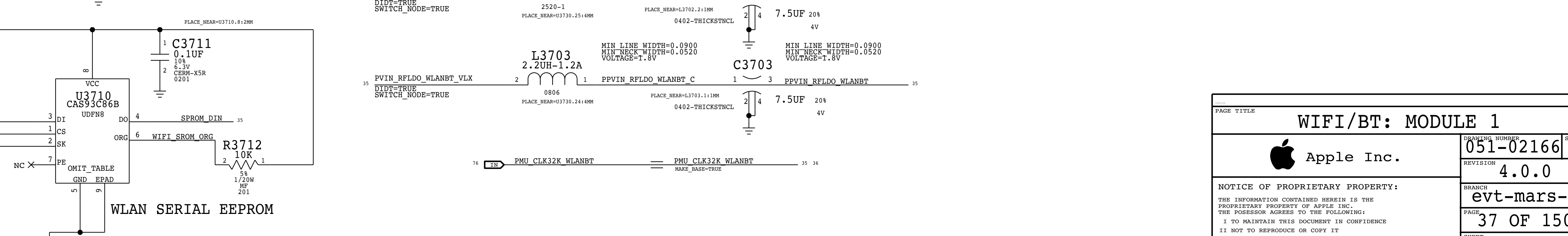
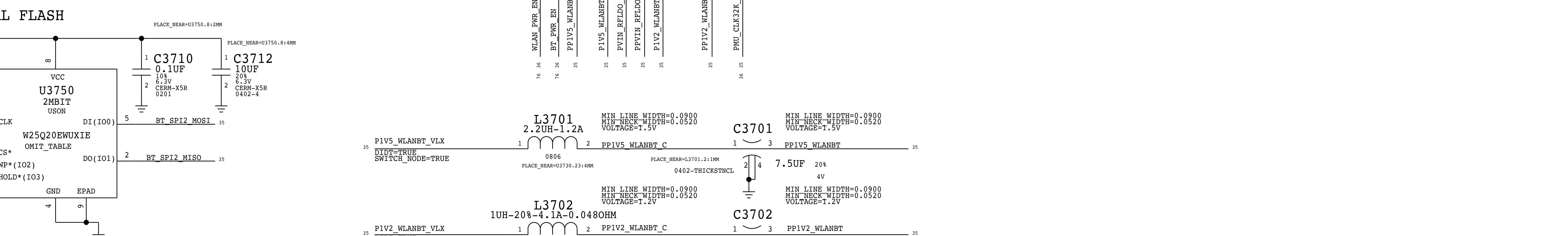
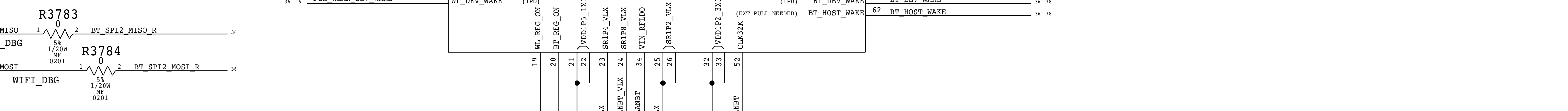
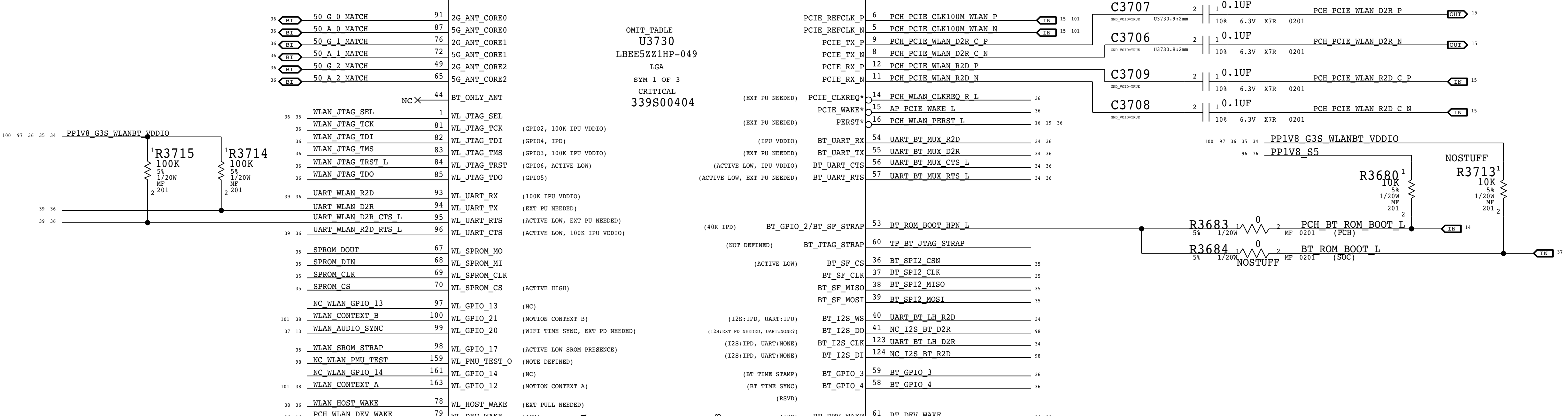
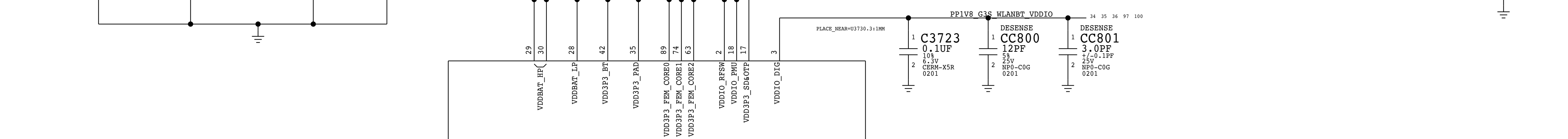
A

D

C

B

A



WLAN SROM STRAP: LOW: SROM Enabled HIGH: SROM Disabled

WLAN_JTAG_SEL: LOW: Some JTAG are GPIOs HIGH: JTAG Enabled

WLAN SERIAL EEPROM

BOM_COST_GROUP=WIRELESS

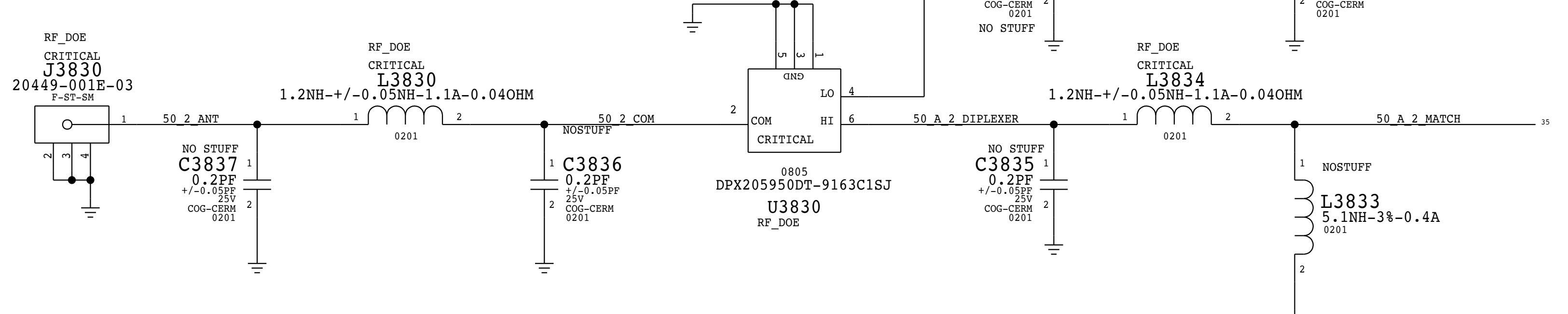
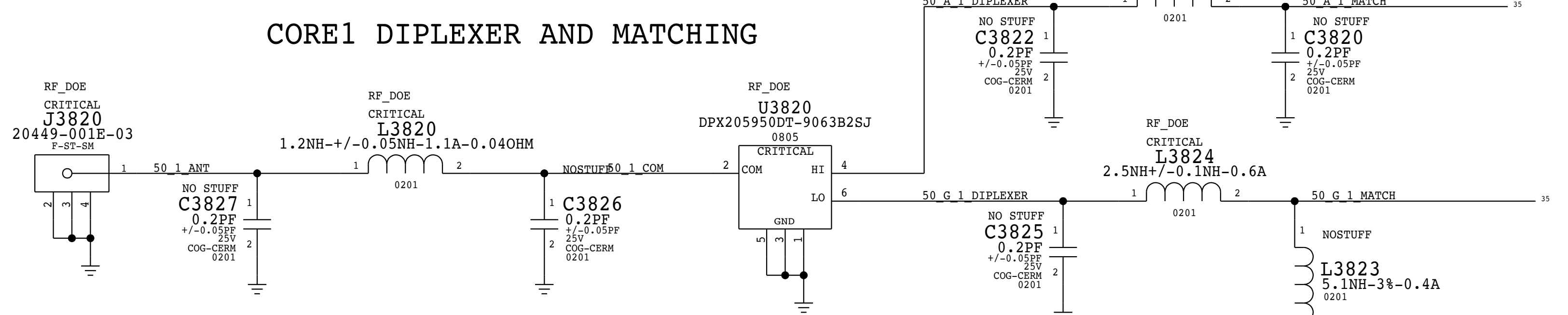
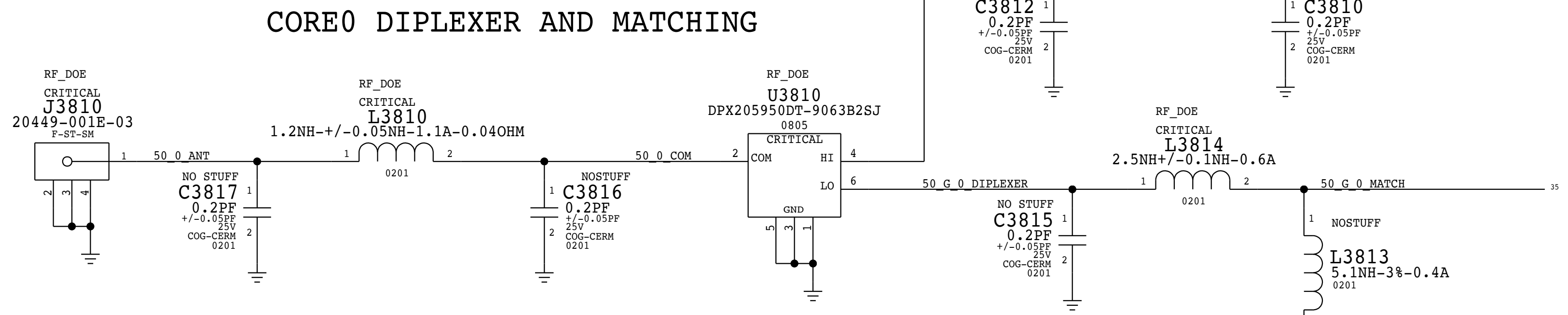
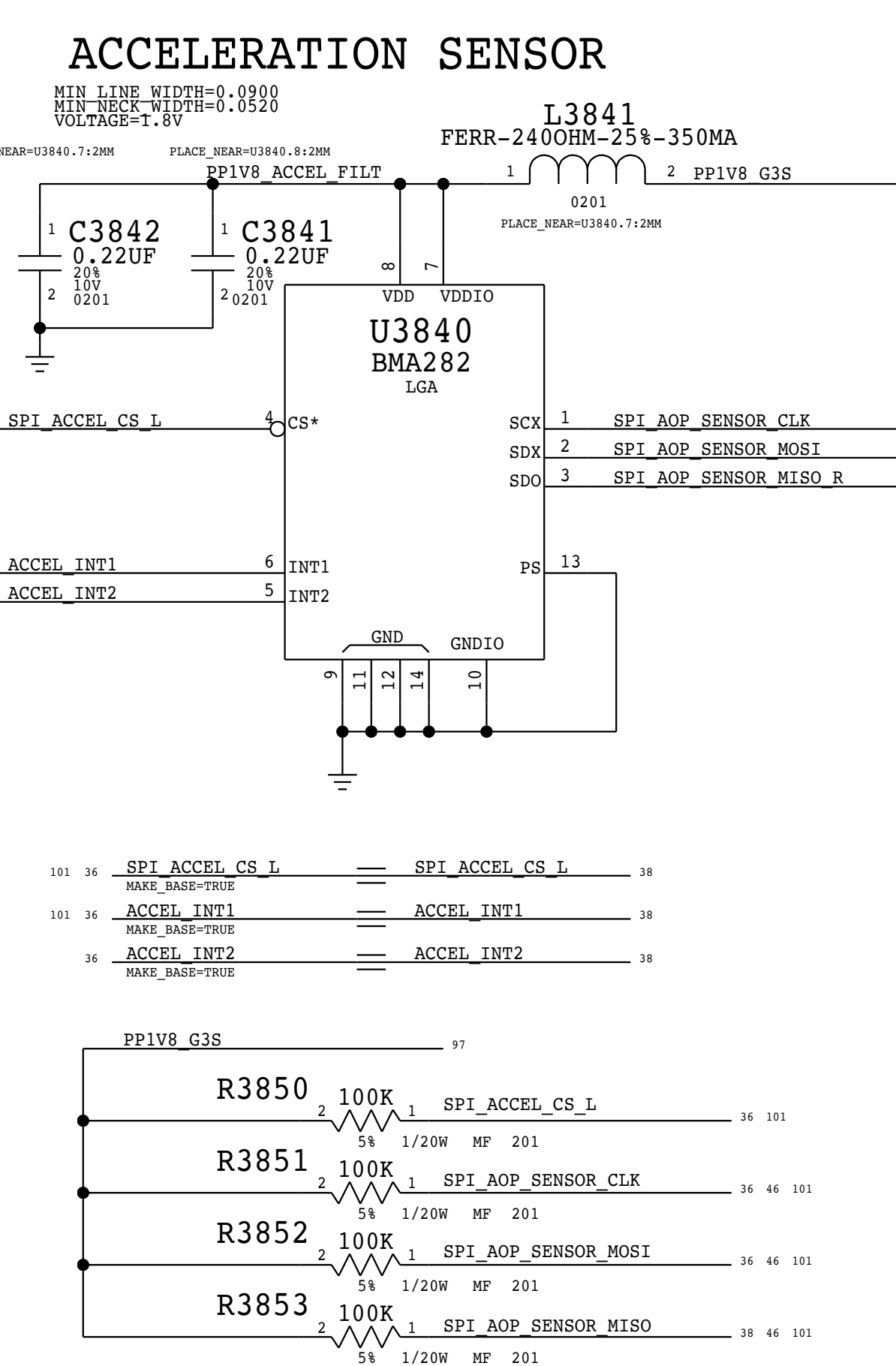
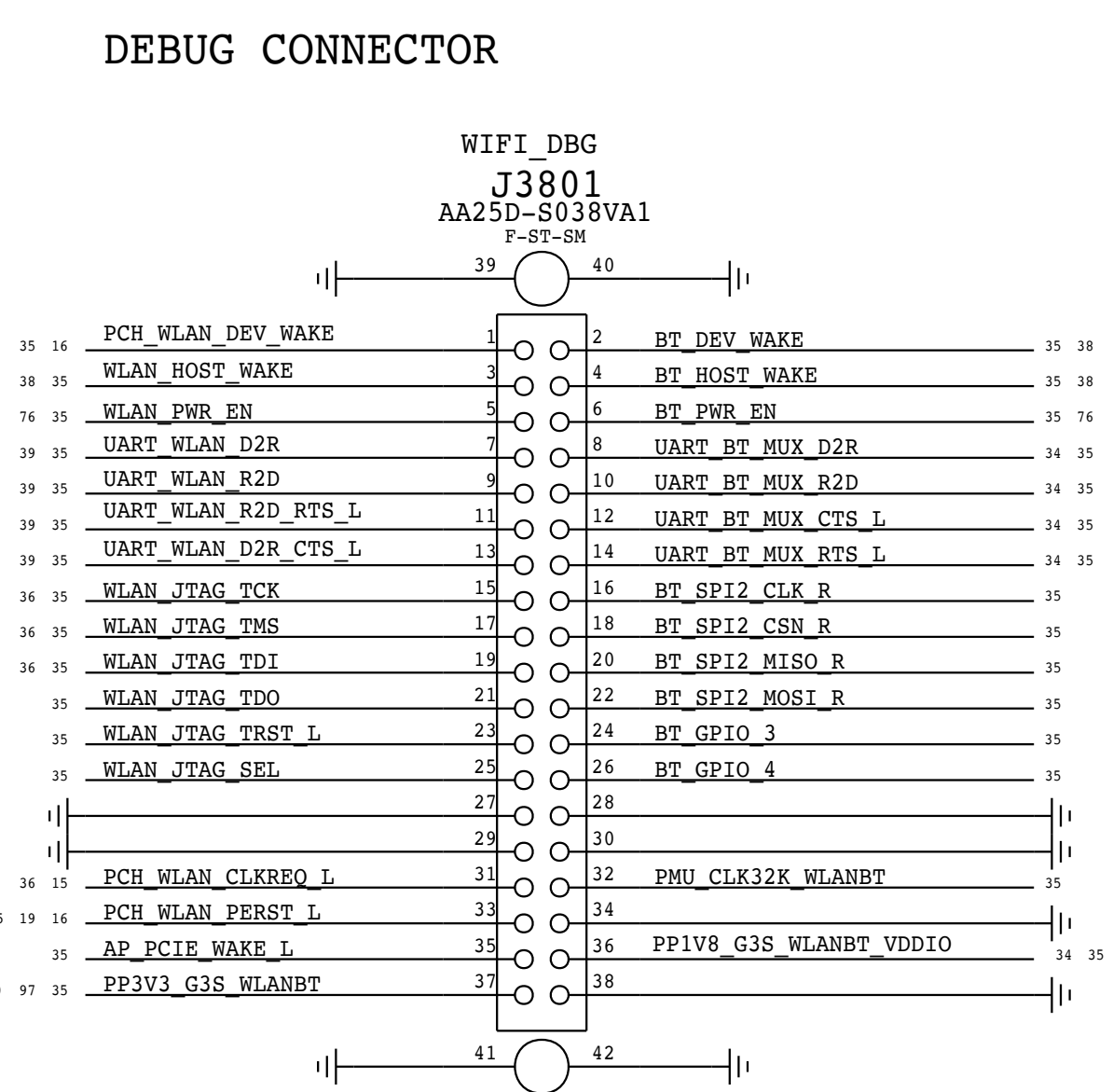
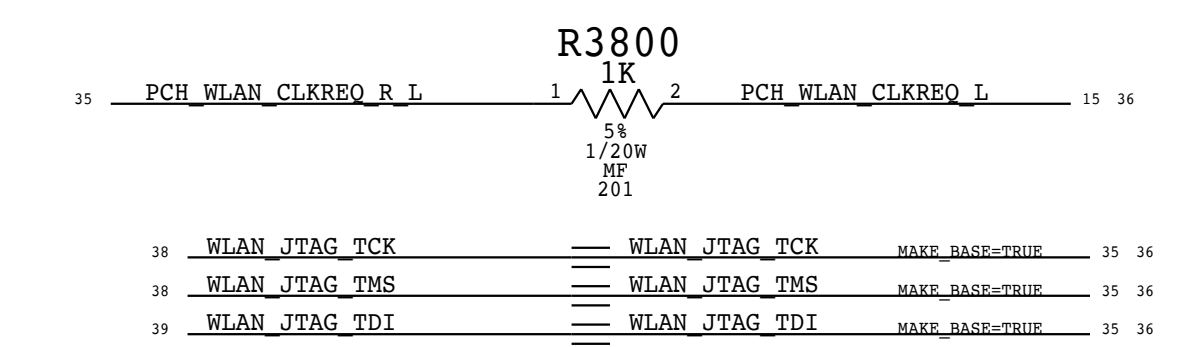
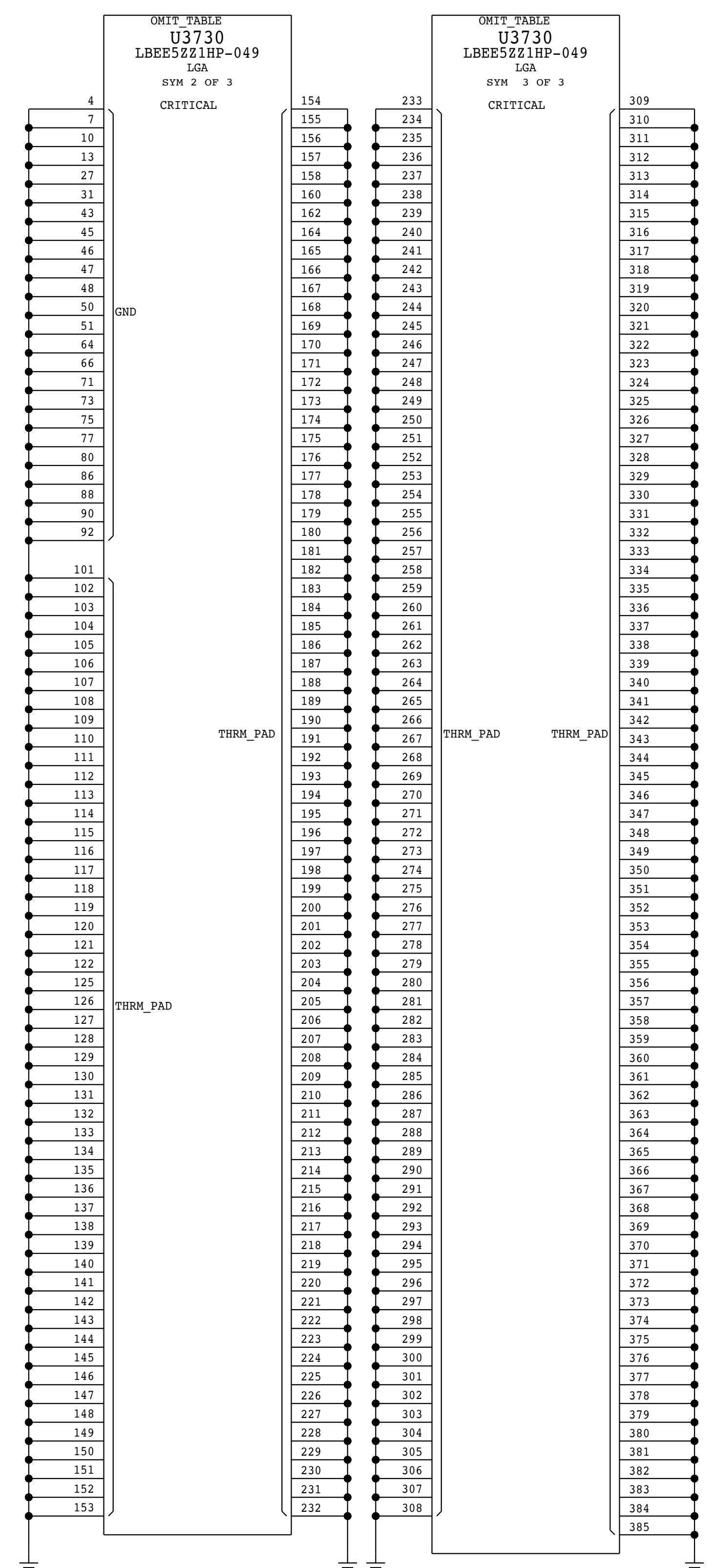
PAGE TITLE		WIFI/BT: MODULE 1	
DRAWING NUMBER		051-02166	SIZE D
REVISION		4.0.0	
BRANCH		evt-mars-0	
PAGE		37 OF 150	
SHEET		35 OF 108	
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D

C

B

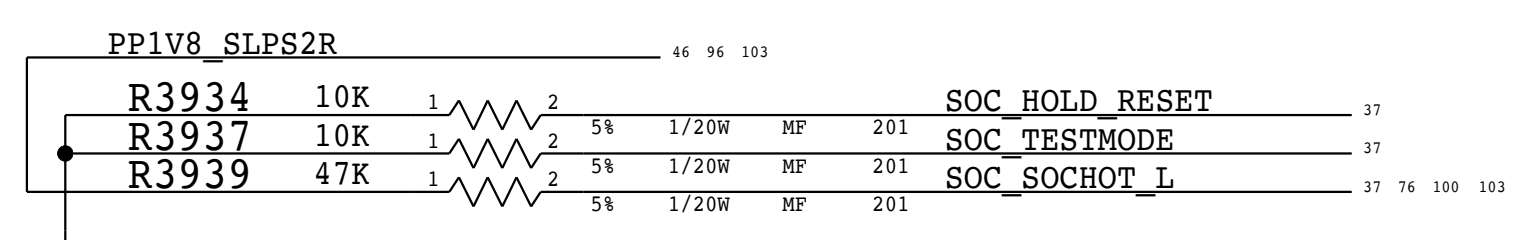
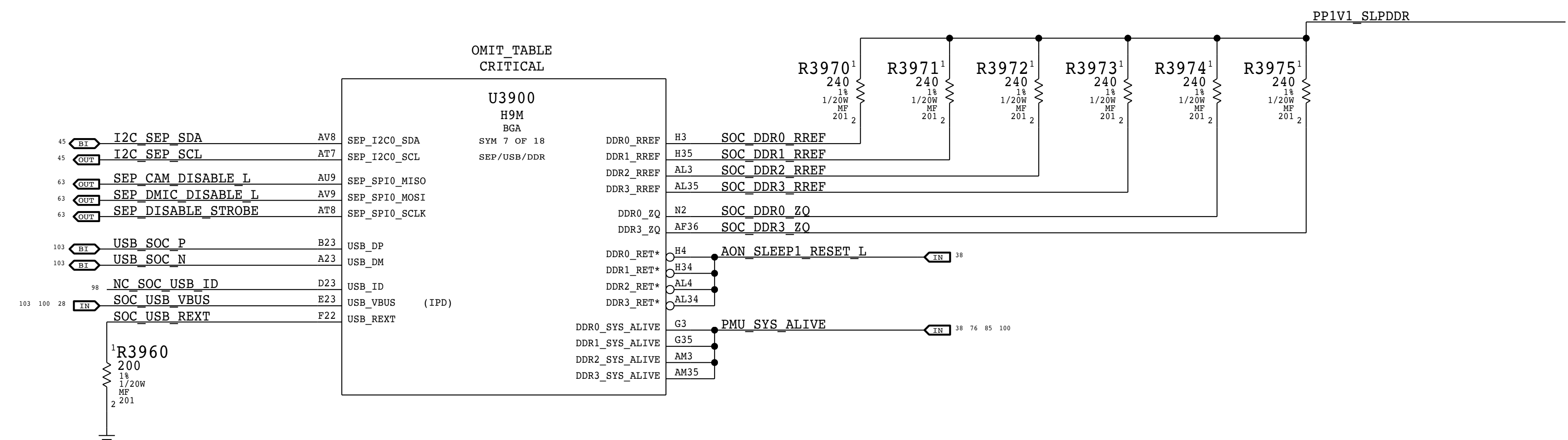
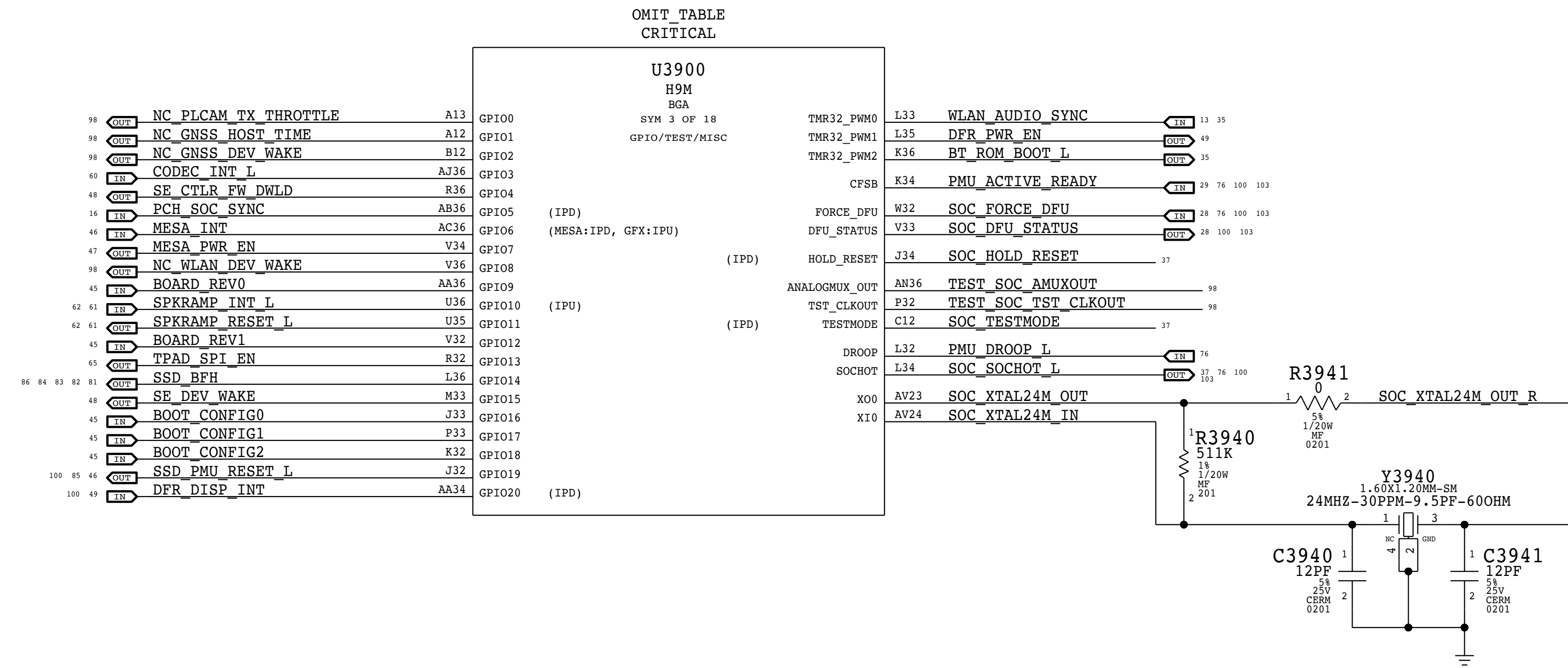
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BOM_COST_GROUP=WIRELESS

PAGE TITLE		WIFI/BT: MODULE 2	
		DRAWING NUMBER	051-02166
		REVISION	4.0.0
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		PAGE	38 OF 150
		SHEET	36 OF 108

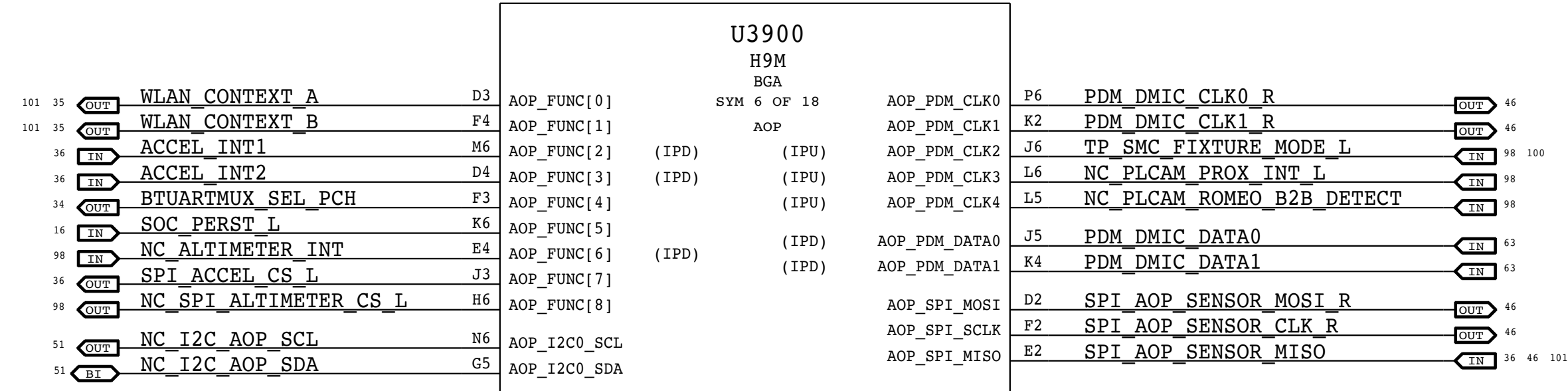
Note 1) IPU represents SW configured state, not HW default



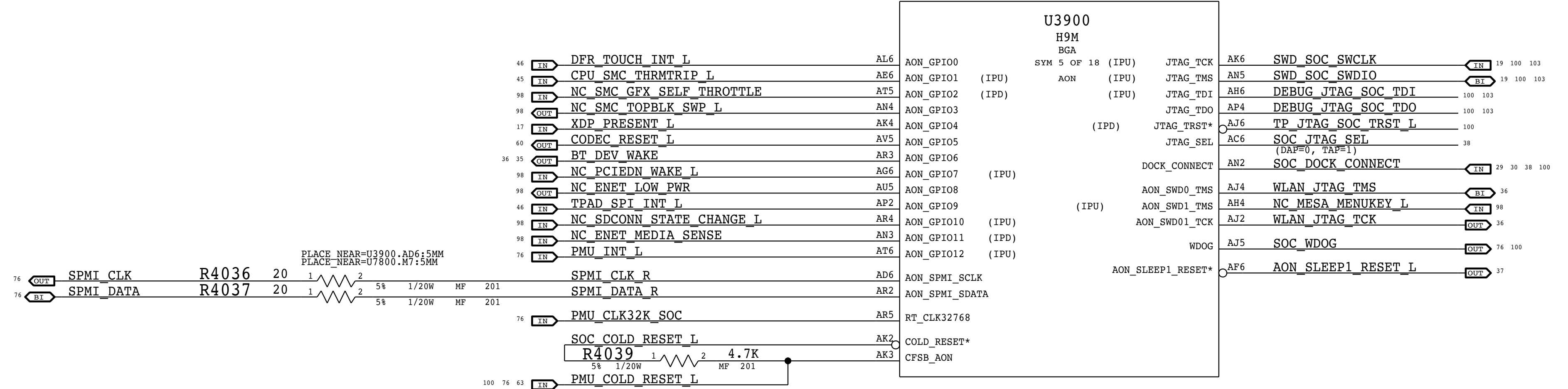
SYNC MASTER=T290 BIGSUR		SYNC DATE=06/14/2017	
PAGE TITLE Soc GPIO/SEP/USB/DDR/Test			
		DRAWING NUMBER	051-02166
		REVISION	4.0.0
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		PAGE	39 OF 150
		SHEET	37 OF 108

BOM_COST_GROUP=SOC

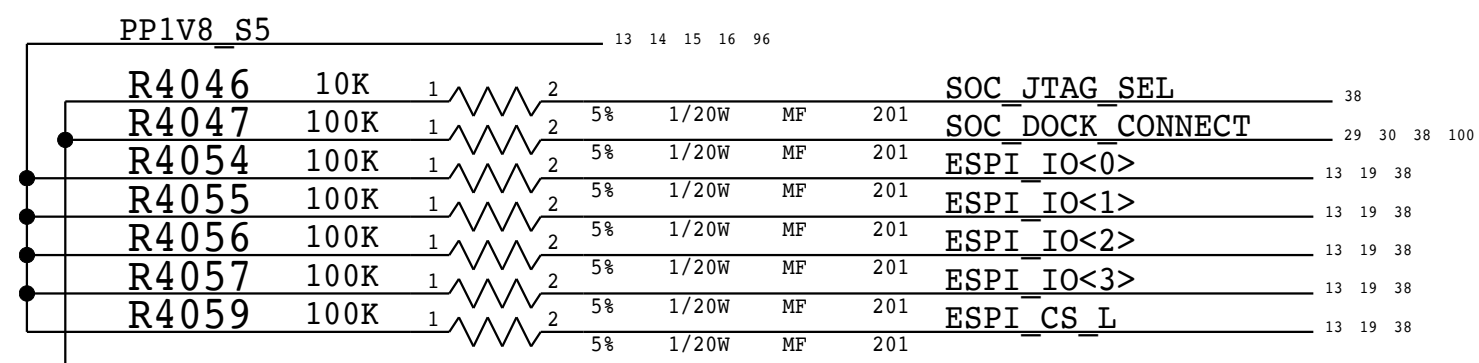
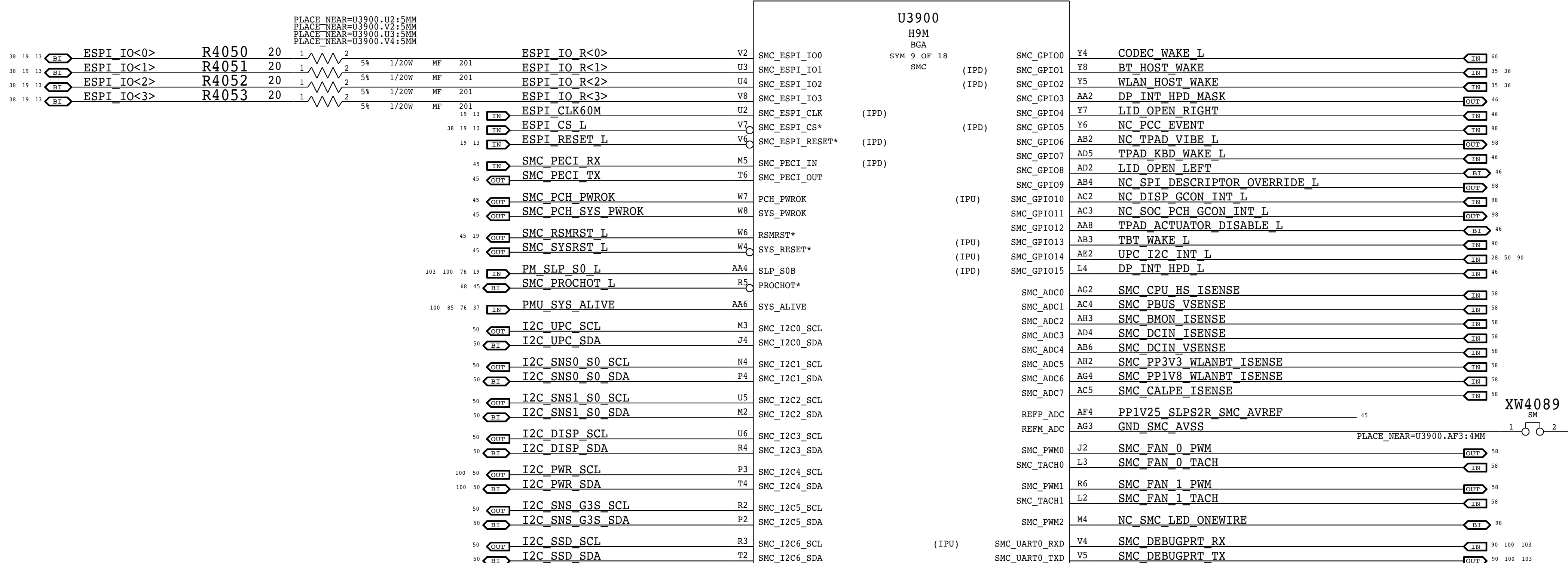
OMIT TABLE
CRITICAL



OMIT TABLE
CRITICAL



OMIT TABLE
CRITICAL

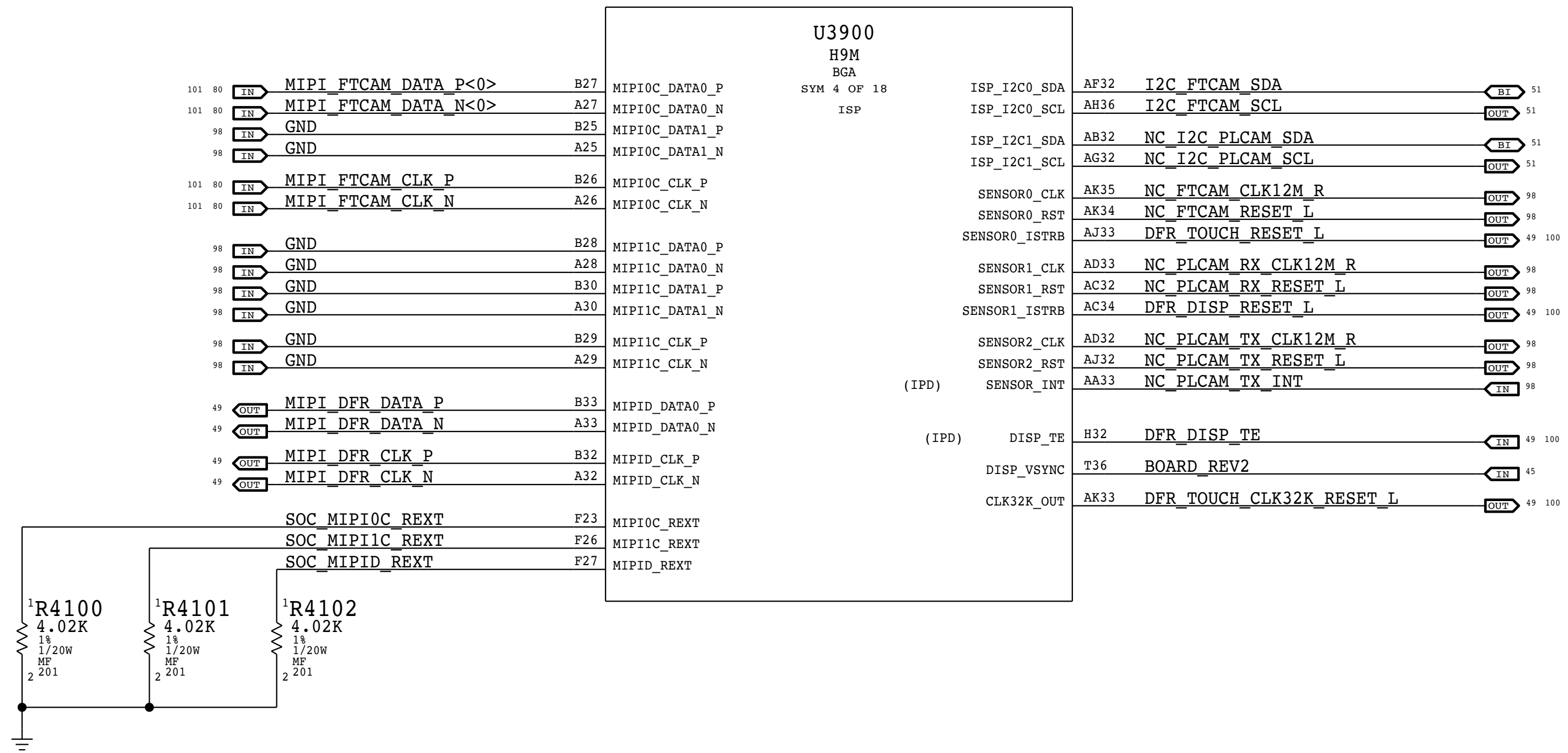


BOM_COST_GROUP=SOC

SYNC MASTER=T290 BIGSUR		SYNC DATE=06/14/2017	
PAGE TITLE			
SoC AOP/AON/SMC		DRAWING NUMBER	051-02166
		REVISION	4.0.0
		BRANCH	evt-mars-0
		PAGE	40 OF 150
		SHEET	38 OF 108
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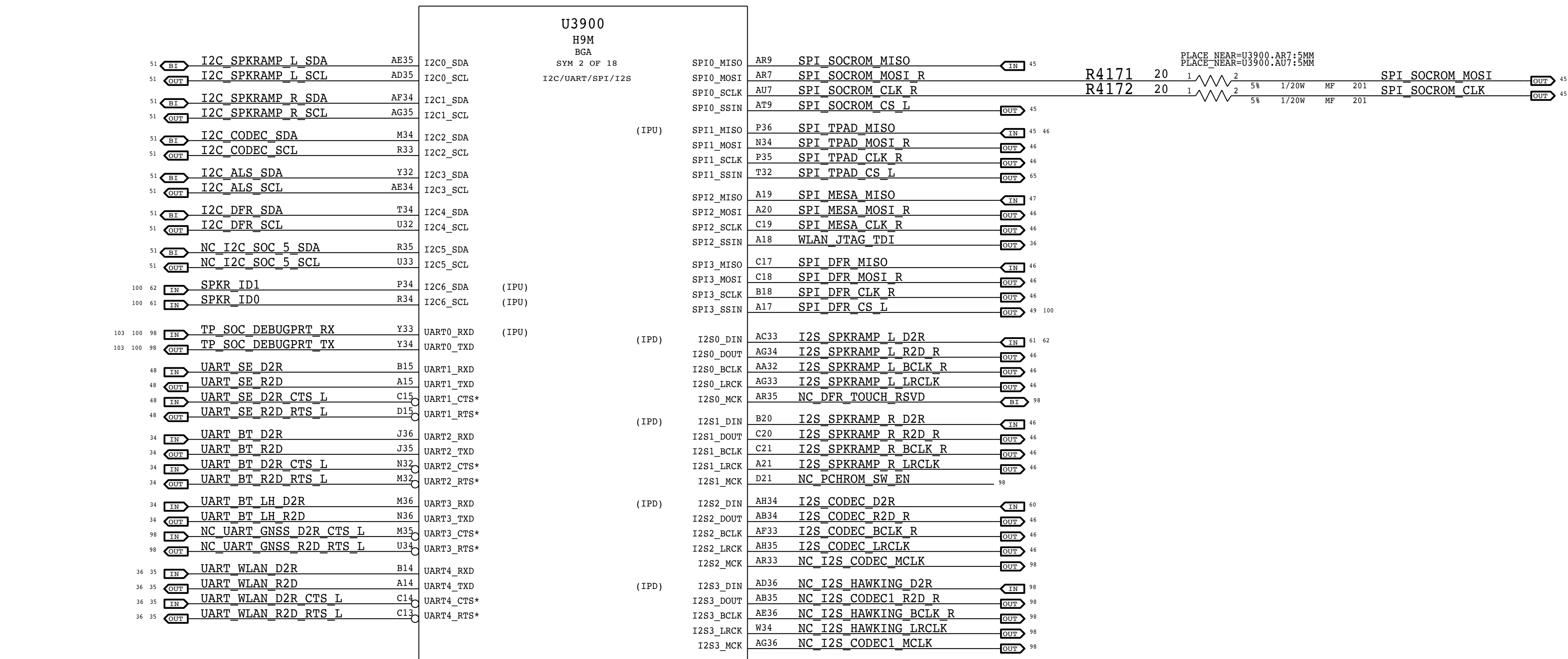
OMIT TABLE

CRITICAL



OMIT TABLE

CRITICAL



BOM_COST_GROUP=SOC

SYNC MASTER=T290 BIGSUR SYNC DATE=05/26/2017

PAGE TITLE: SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRIVING NUMBER: 051-02166

REVISION: 4.0.0

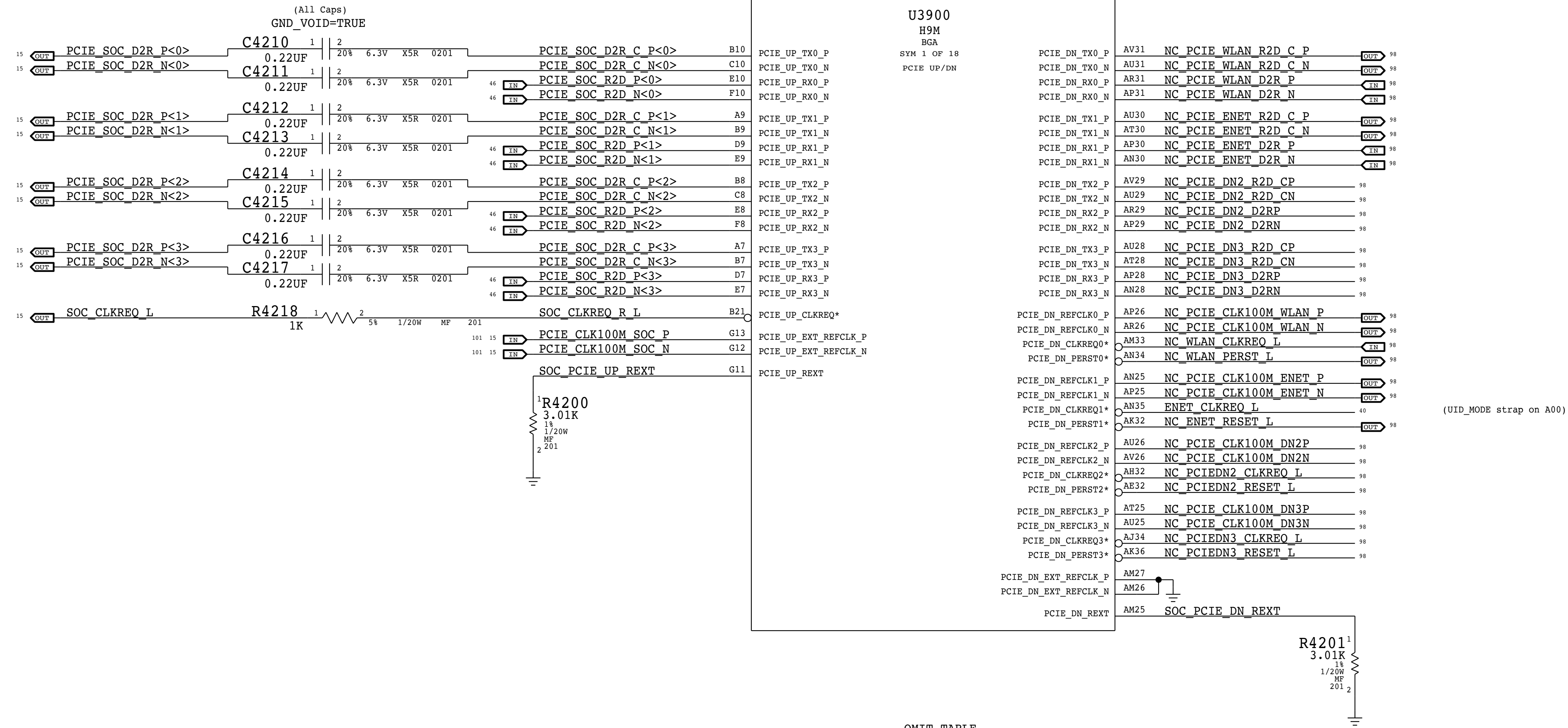
BRANCH: evt-mars-0

PAGE: 41 OF 150

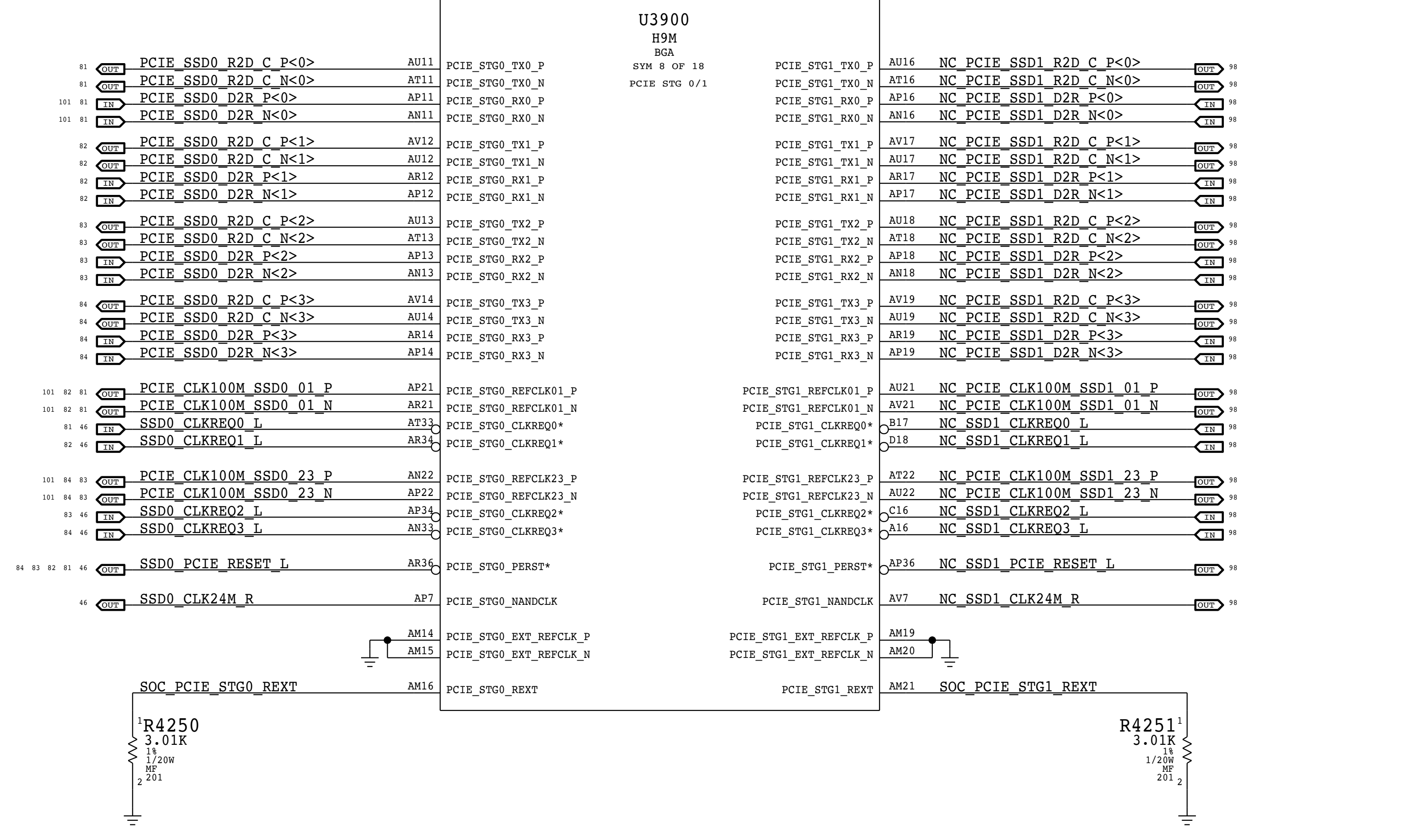
SHEET: 39 OF 108

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OMIT TABLE
CRITICAL



OMIT TABLE
CRITICAL

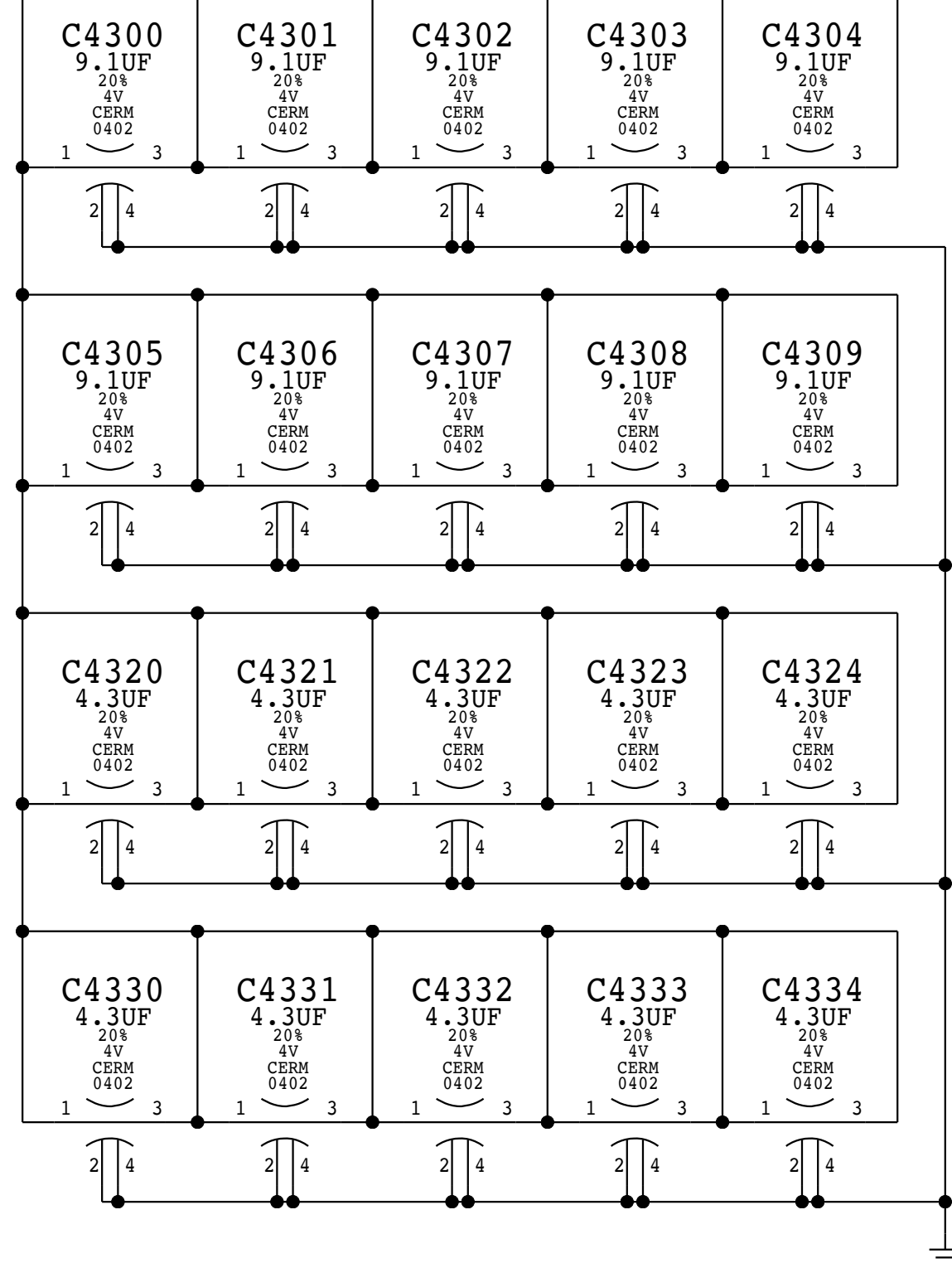


SYNC MASTER=T290 BIGSUR		SYNC DATE=03/15/2017	
PAGE TITLE			
SoC PCIe		DRAWING NUMBER	051-02166
		REVISION	4.0.0
		BRANCH	evt-mars-0
		PAGE	42 OF 150
		SHEET	40 OF 108

BOM_COST_GROUP=SOC

Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

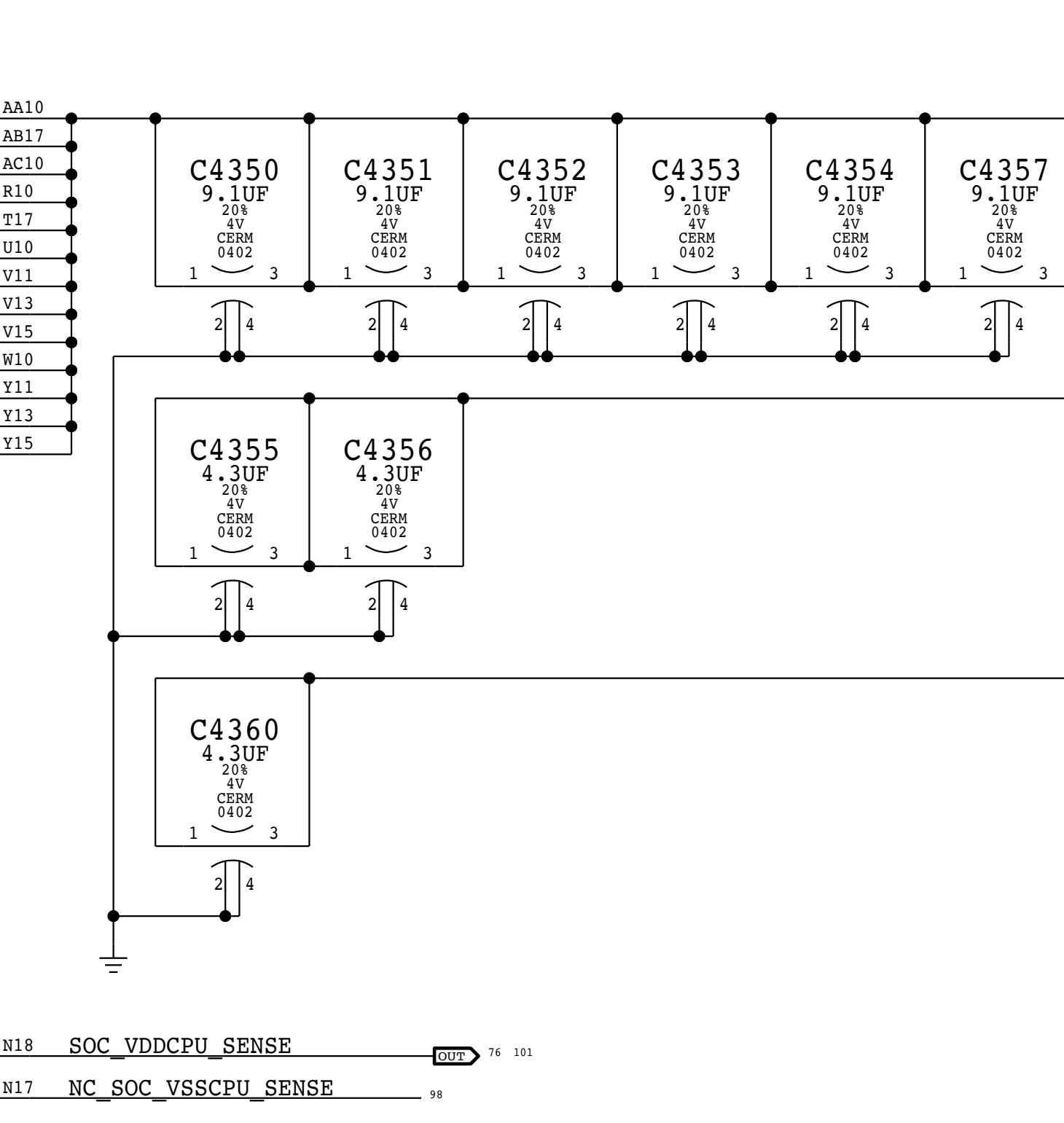
PPVDDCPU_AWAKE
0.625V - 1.06V
11.6A Max



OMIT TABLE
CRITICAL

U3900
H9M
BGA
SYM 10 OF 18

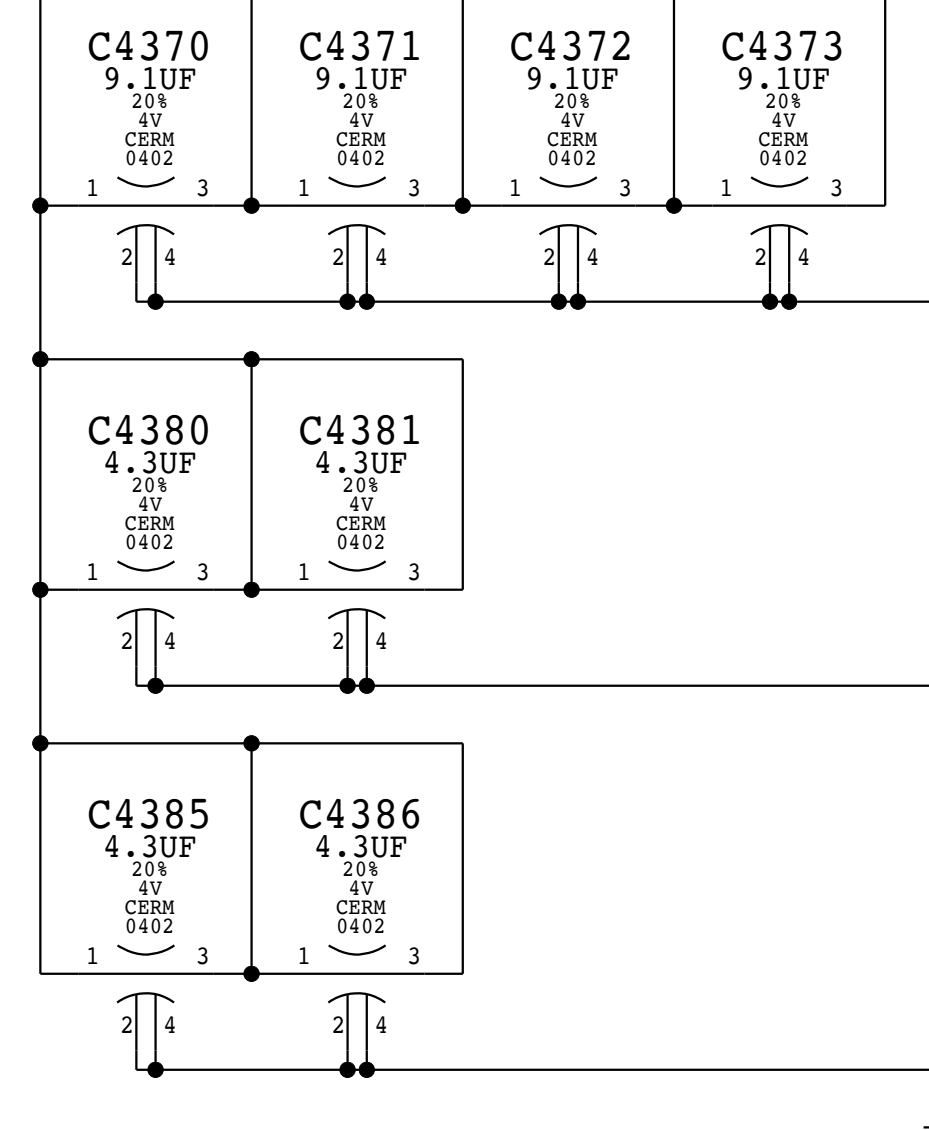
AA12	VDD_CPU
AA14	VDD_CPU
AA16	VDD_CPU
AB11	VDD_CPU
AB13	VDD_CPU
AB15	VDD_CPU
AC12	VDD_CPU
AC14	VDD_CPU
AC16	VDD_CPU
AD11	VDD_CPU
AD13	VDD_CPU
AD15	VDD_CPU
AD17	VDD_CPU
AE10	VDD_CPU
AE12	VDD_CPU
AE14	VDD_CPU
AE16	VDD_CPU
AE18	VDD_CPU
P11	VDD_CPU
P13	VDD_CPU
P15	VDD_CPU
P17	VDD_CPU
R12	VDD_CPU
R14	VDD_CPU
R16	VDD_CPU
T11	VDD_CPU
T13	VDD_CPU
T15	VDD_CPU
U12	VDD_CPU
U14	VDD_CPU
U16	VDD_CPU
U17	VDD_CPU
W12	VDD_CPU
W14	VDD_CPU
W16	VDD_CPU
Y17	VDD_CPU



PPVDDCPUSRAM_AWAKE
0.8V - 1.06V
0.9A Max

VDD_CPU_SENSE N18 SOC_VDDCPU_SENSE
VSS_CPU_SENSE N17 NC_SOC_VSSCPU_SENSE

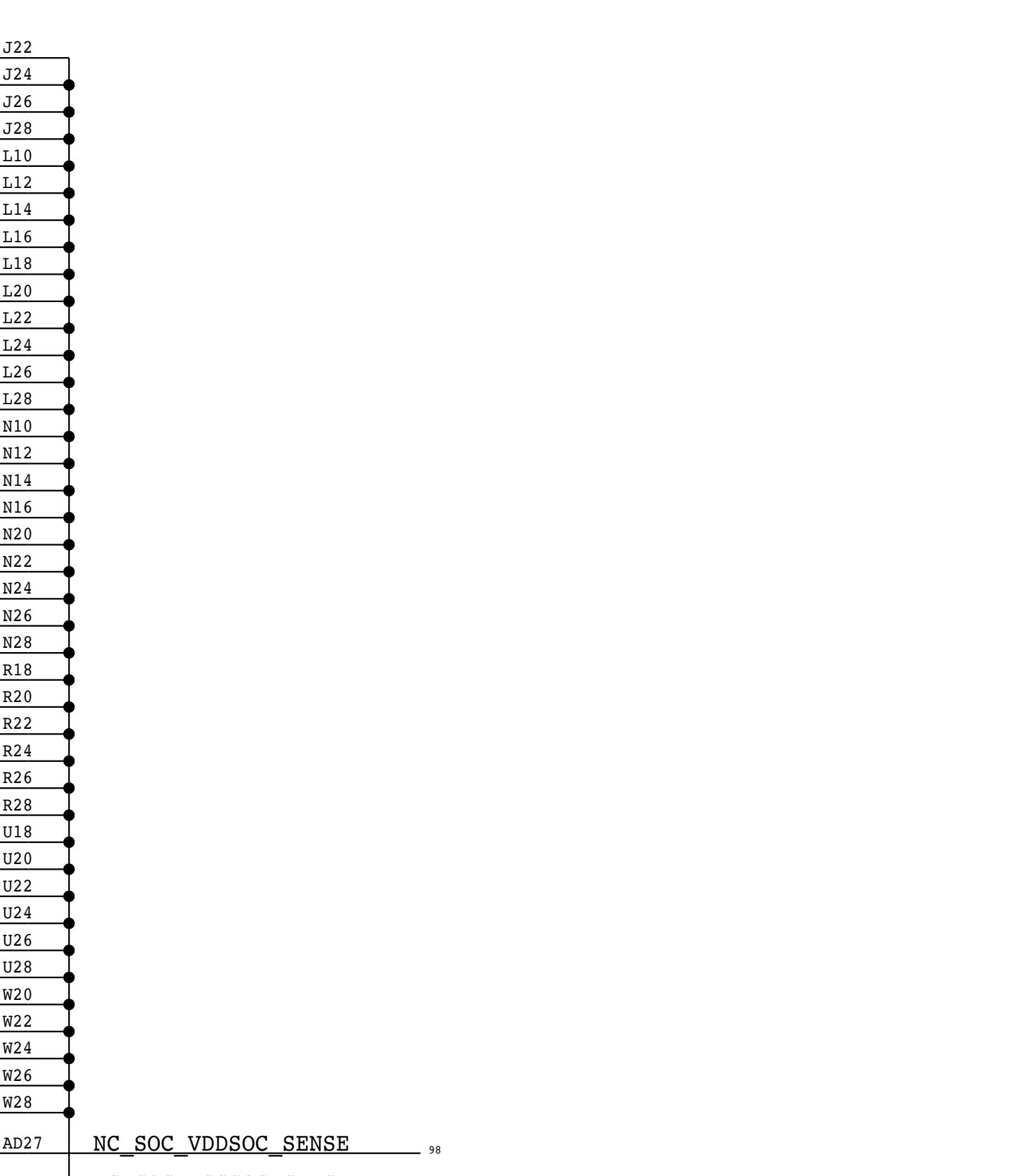
PPOV82_SLPDDR
5.6A Max



OMIT TABLE
CRITICAL

U3900
H9M
BGA
SYM 11 OF 18

AA20	VDD_SOC
AA22	VDD_SOC
AA24	VDD_SOC
AA26	VDD_SOC
AA28	VDD_SOC
AC18	VDD_SOC
AC20	VDD_SOC
AC22	VDD_SOC
AC24	VDD_SOC
AC26	VDD_SOC
AC28	VDD_SOC
AE20	VDD_SOC
AE22	VDD_SOC
AE24	VDD_SOC
AE26	VDD_SOC
AE28	VDD_SOC
AG10	VDD_SOC
AG12	VDD_SOC
AG14	VDD_SOC
AG16	VDD_SOC
AG18	VDD_SOC
AG20	VDD_SOC
AG22	VDD_SOC
AG24	VDD_SOC
AG26	VDD_SOC
AG28	VDD_SOC
AJ10	VDD_SOC
AJ12	VDD_SOC
AJ14	VDD_SOC
AJ16	VDD_SOC
AJ18	VDD_SOC
AJ20	VDD_SOC
AJ22	VDD_SOC
AJ24	VDD_SOC
AJ26	VDD_SOC
AJ28	VDD_SOC
J10	VDD_SOC
J12	VDD_SOC
J14	VDD_SOC
J16	VDD_SOC
J18	VDD_SOC
J20	VDD_SOC



VDD_SOC_SENSE AD27 NC_SOC_VDDSOC_SENSE
VSS_SENSE AD28 NC_SOC_VSSSOC_SENSE

BOM_COST_GROUP=SOC

SYNC MASTER=T290 BIGSUR SYNC DATE=03/29/2017

SoC Power 1

Apple Inc.

DRAWING NUMBER	051-02166	SIZE	D
REVISION	4.0.0		
BRANCH	evt-mars-0		
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Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

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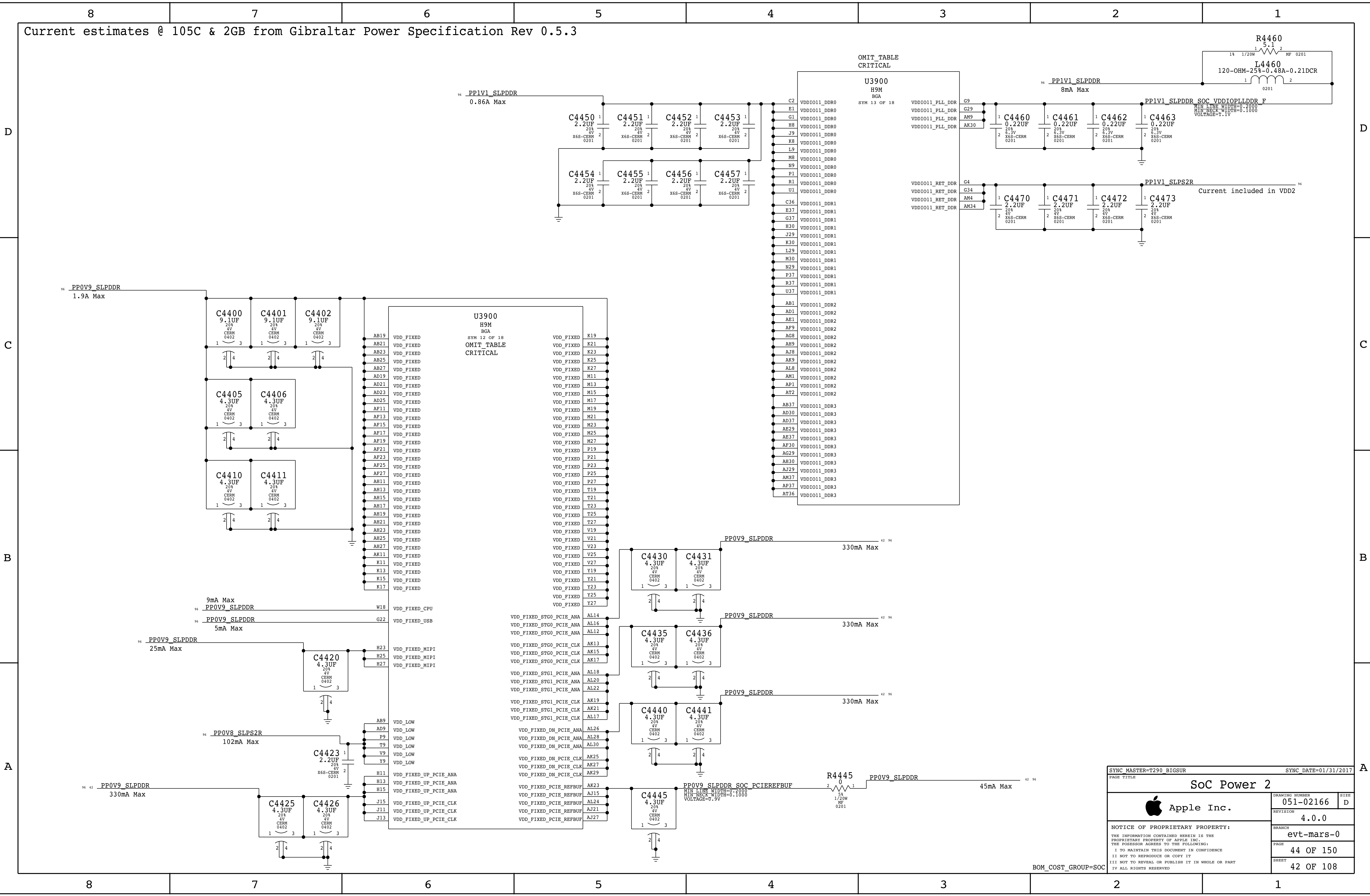
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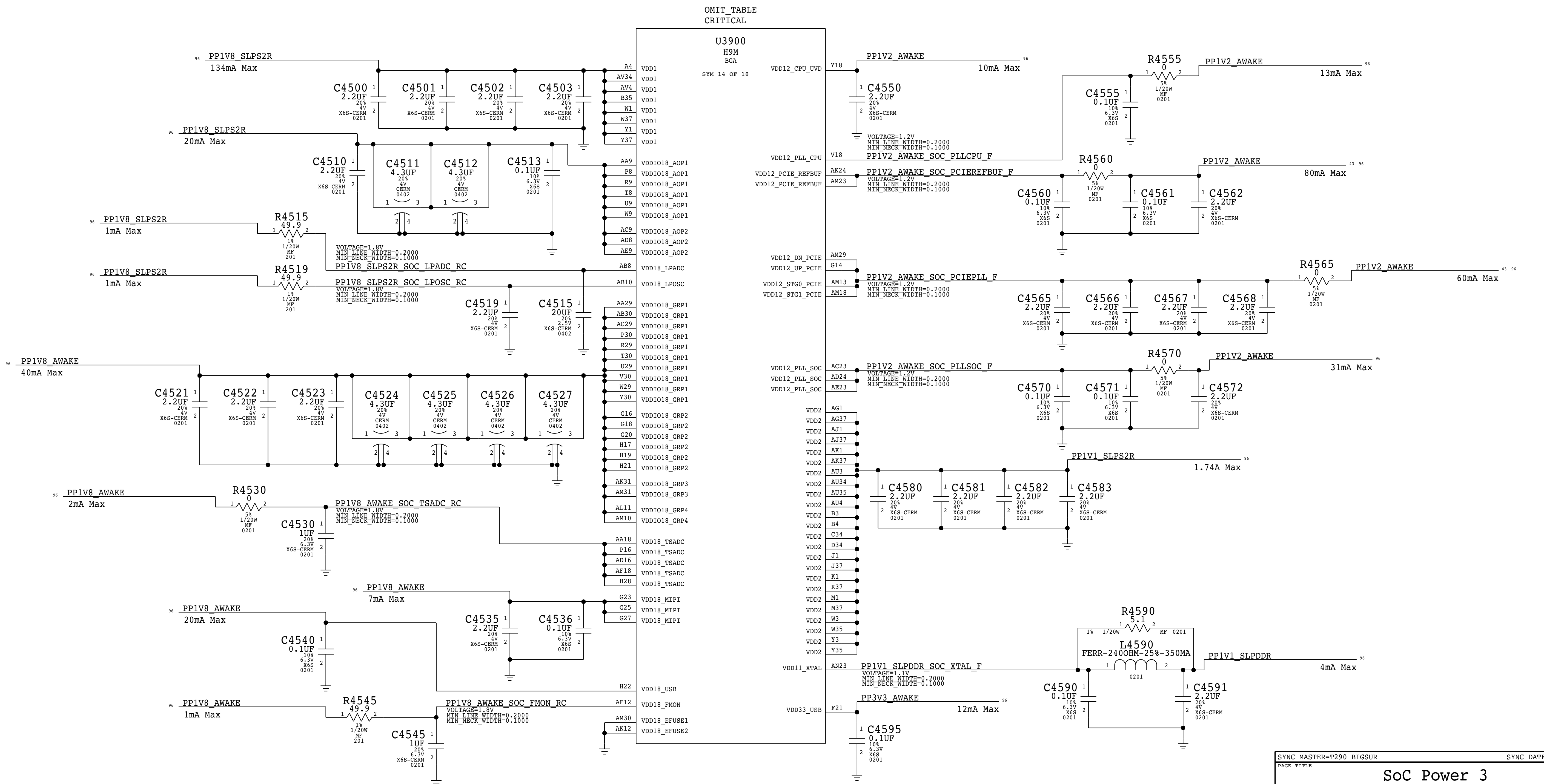
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		BRANCH	evt-mars-0
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BOM_COST_GROUP=SOC



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BOM_COST_GROUP=SOC

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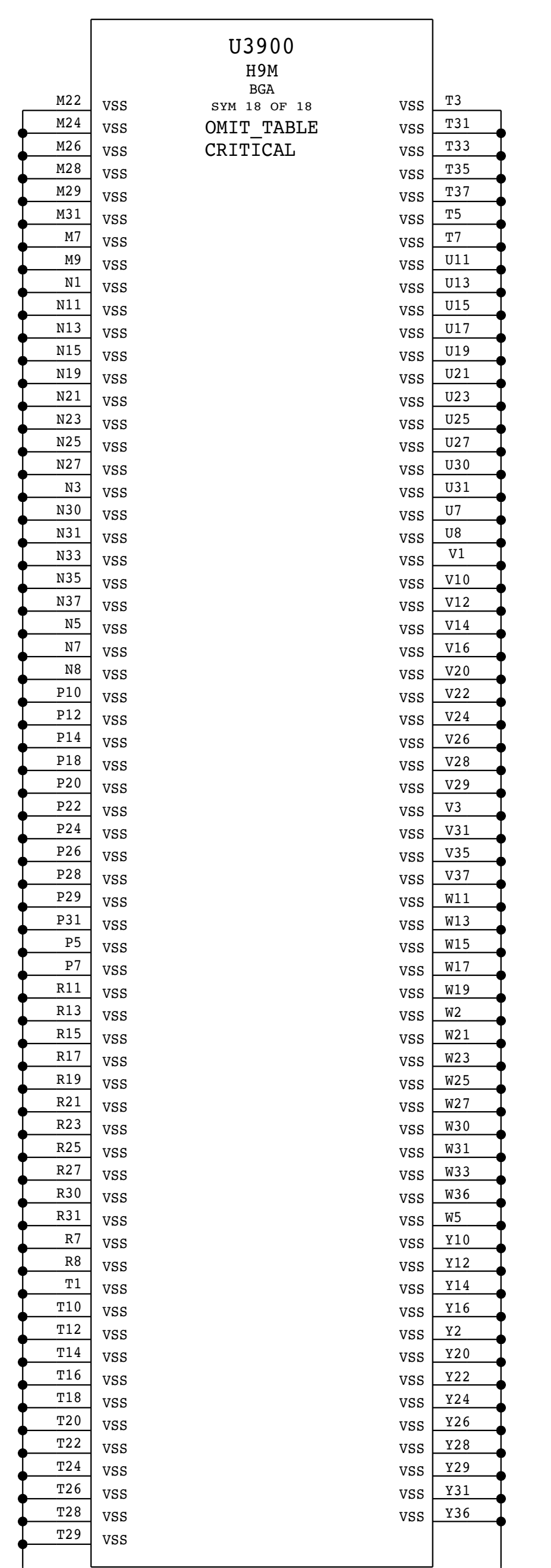
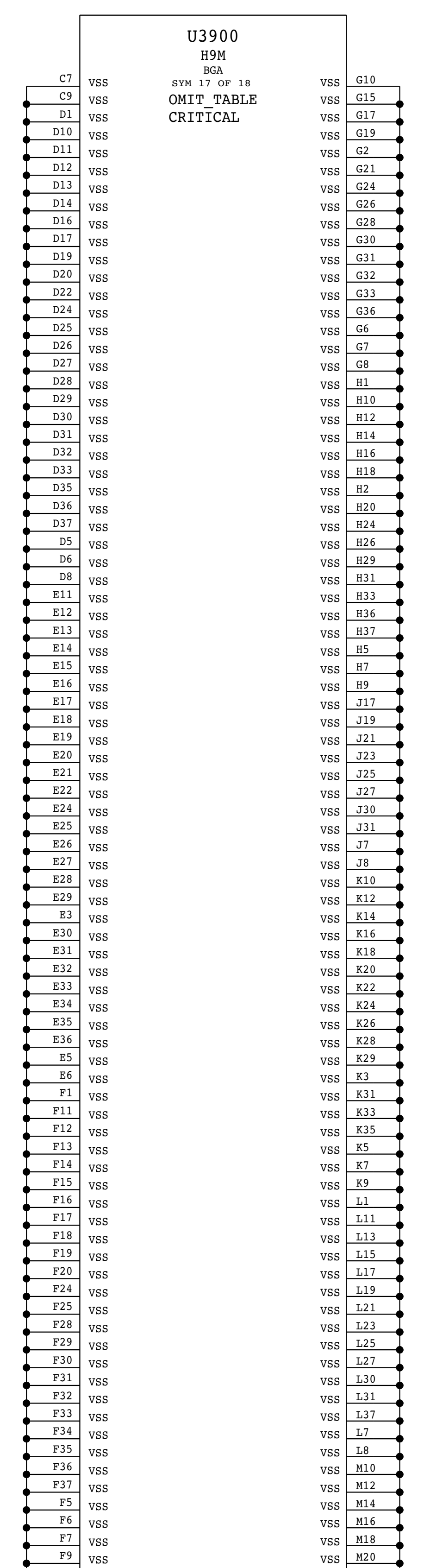
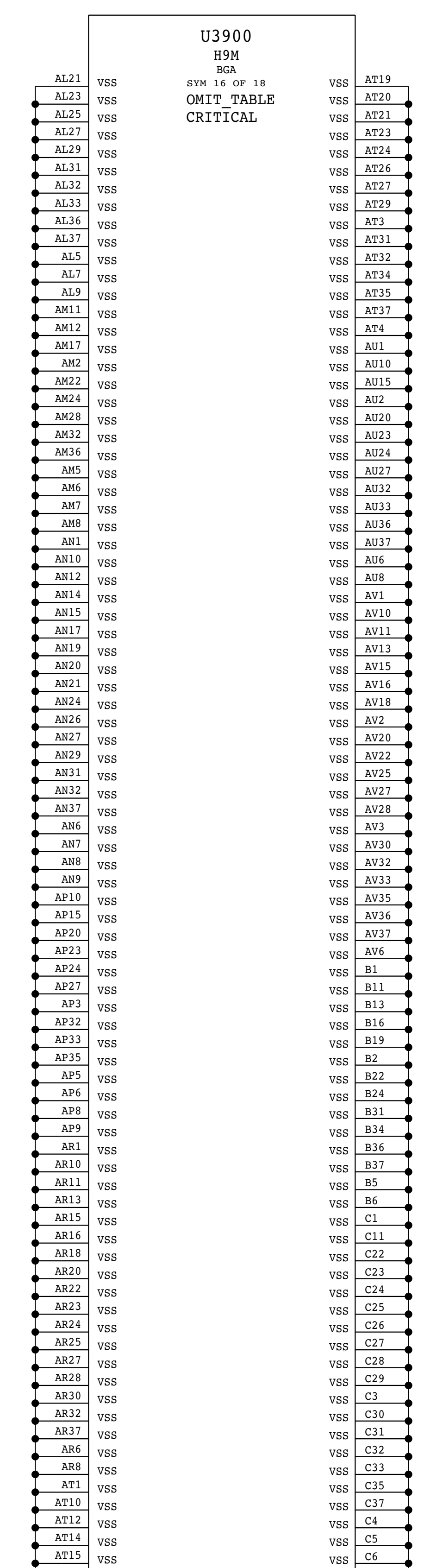
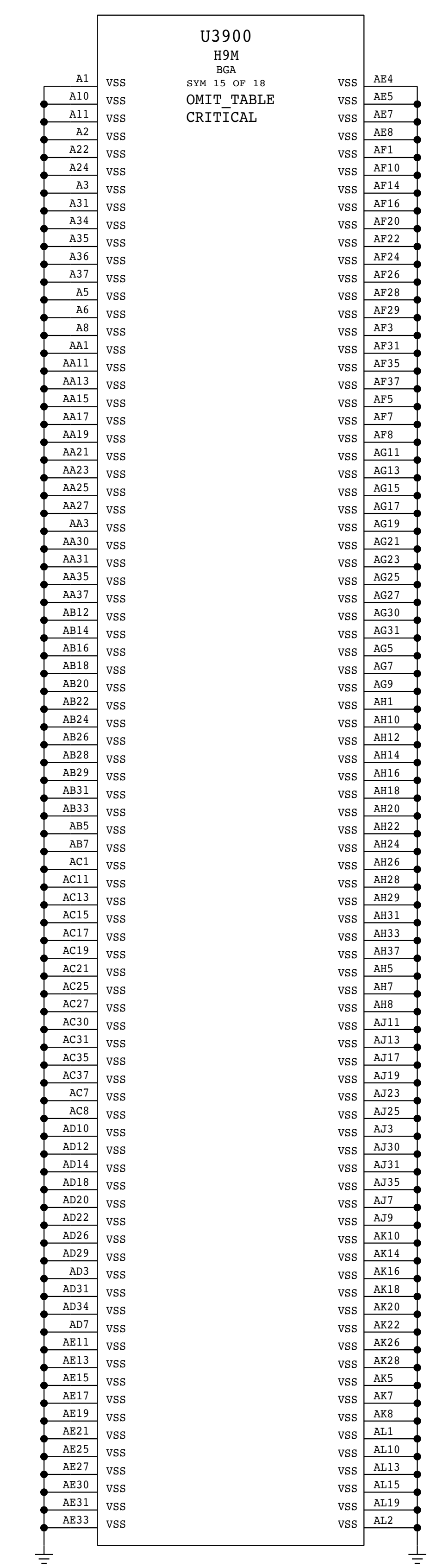
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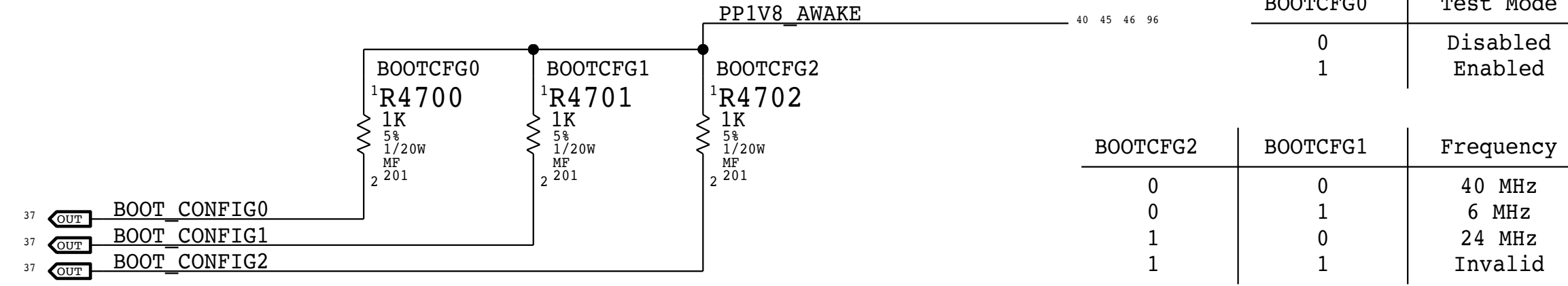
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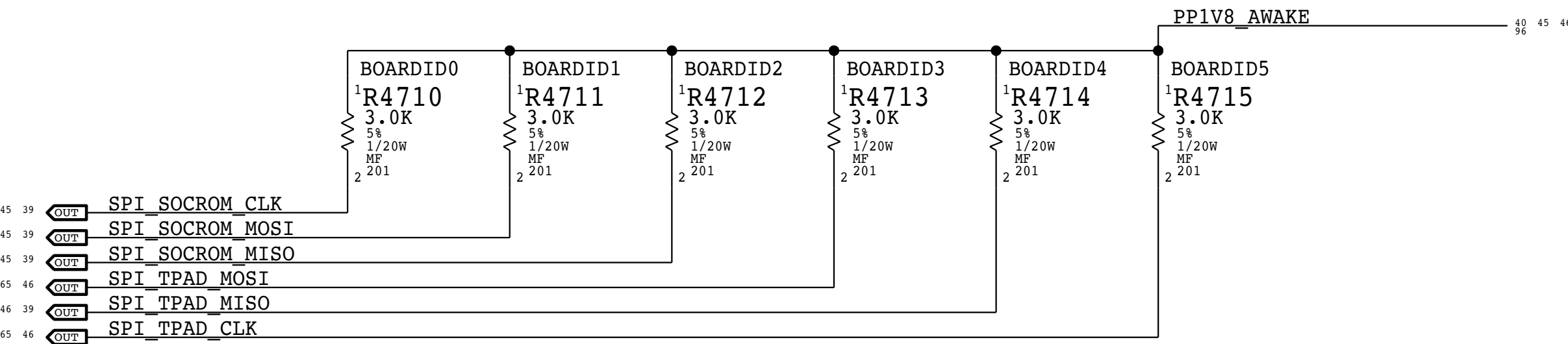
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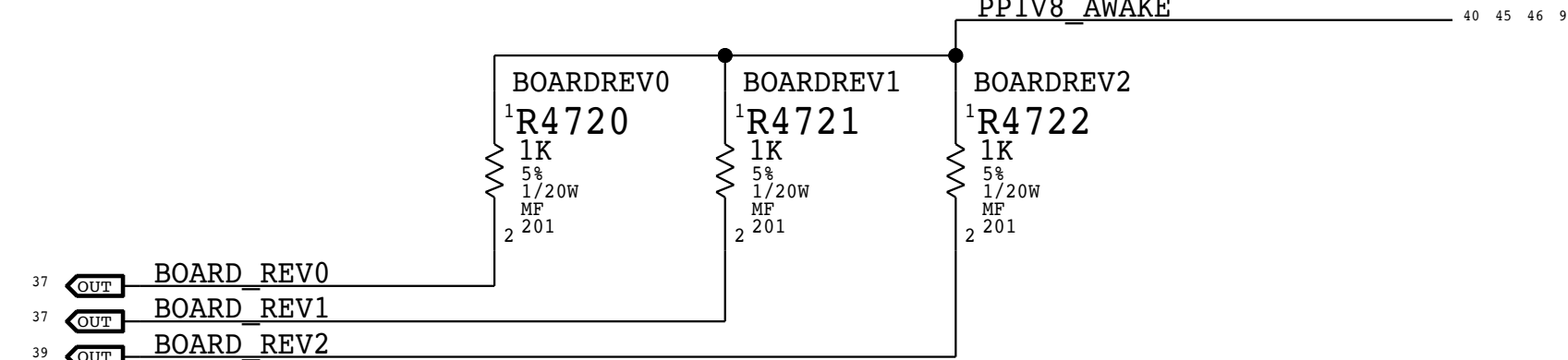
Boot Config



Board ID

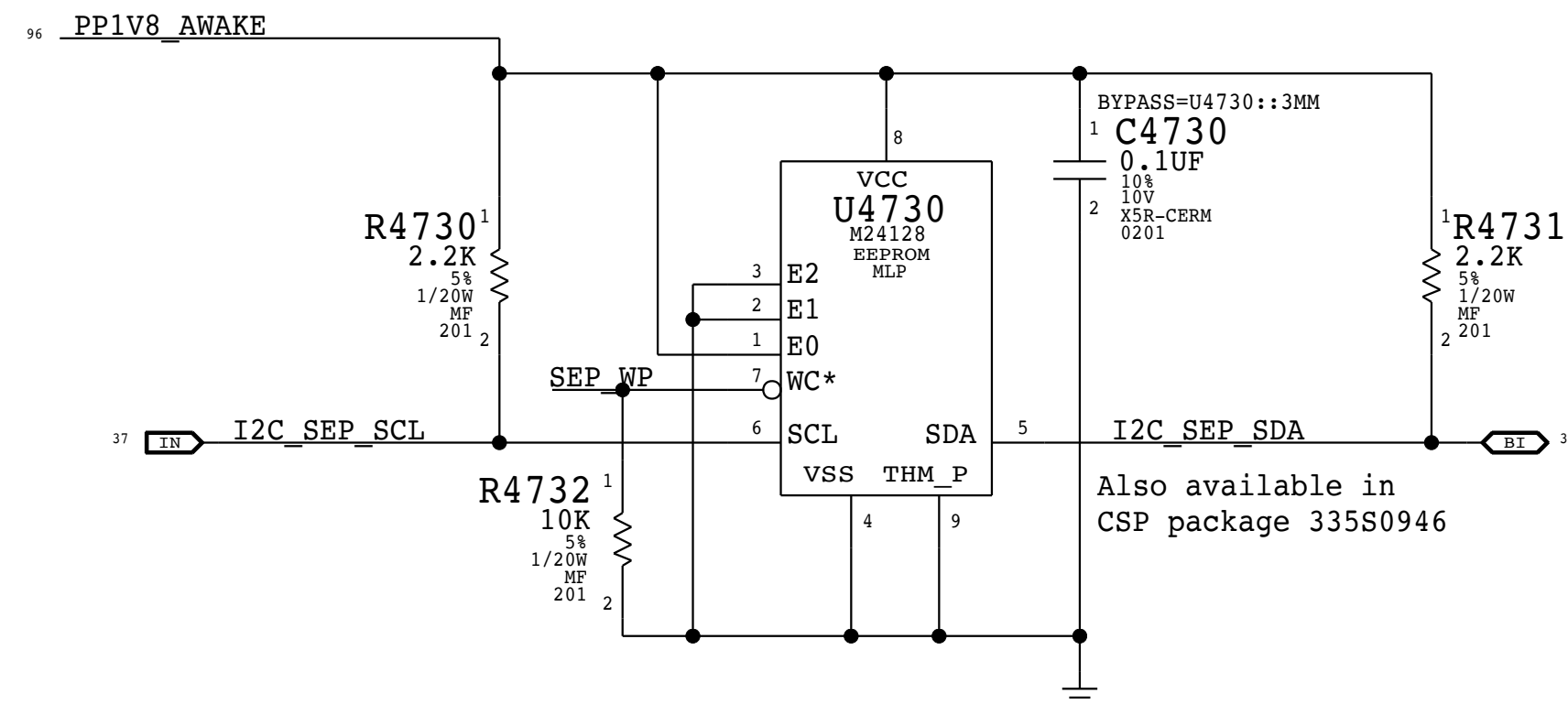


Board Revision

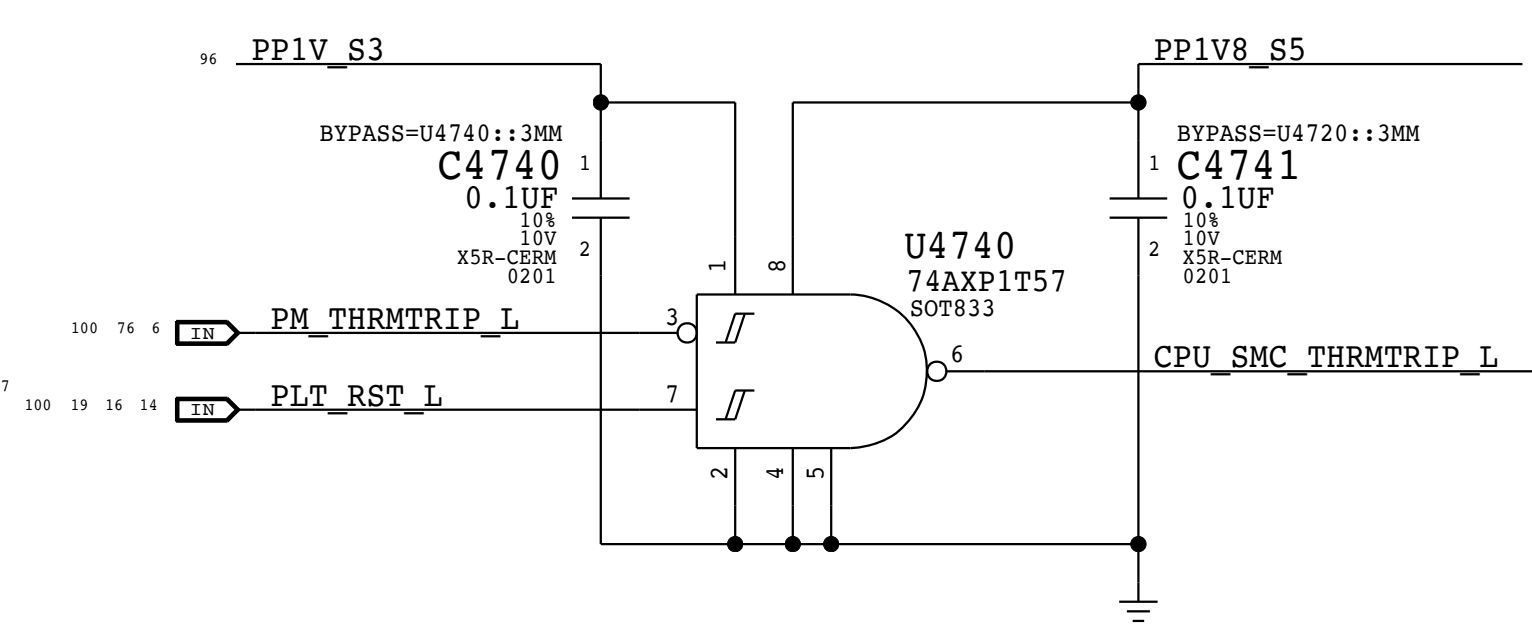


SEP EEPROM

(Write: 0xA2, Read 0xA3)

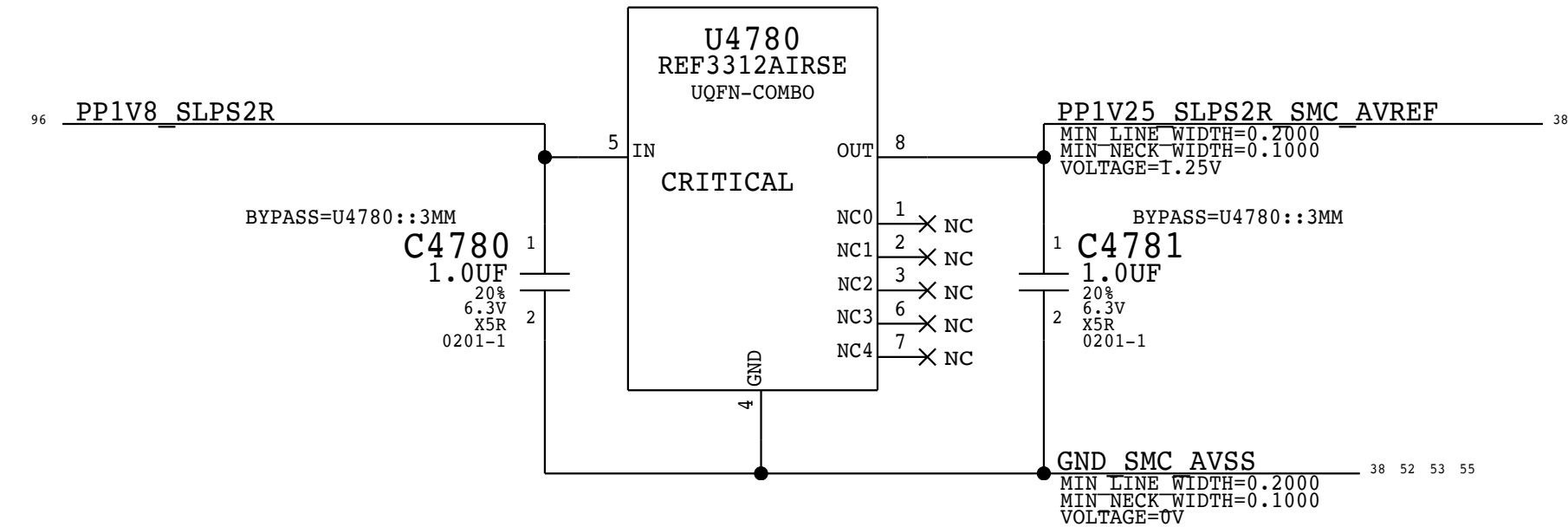


THRMTRIP# Isolation



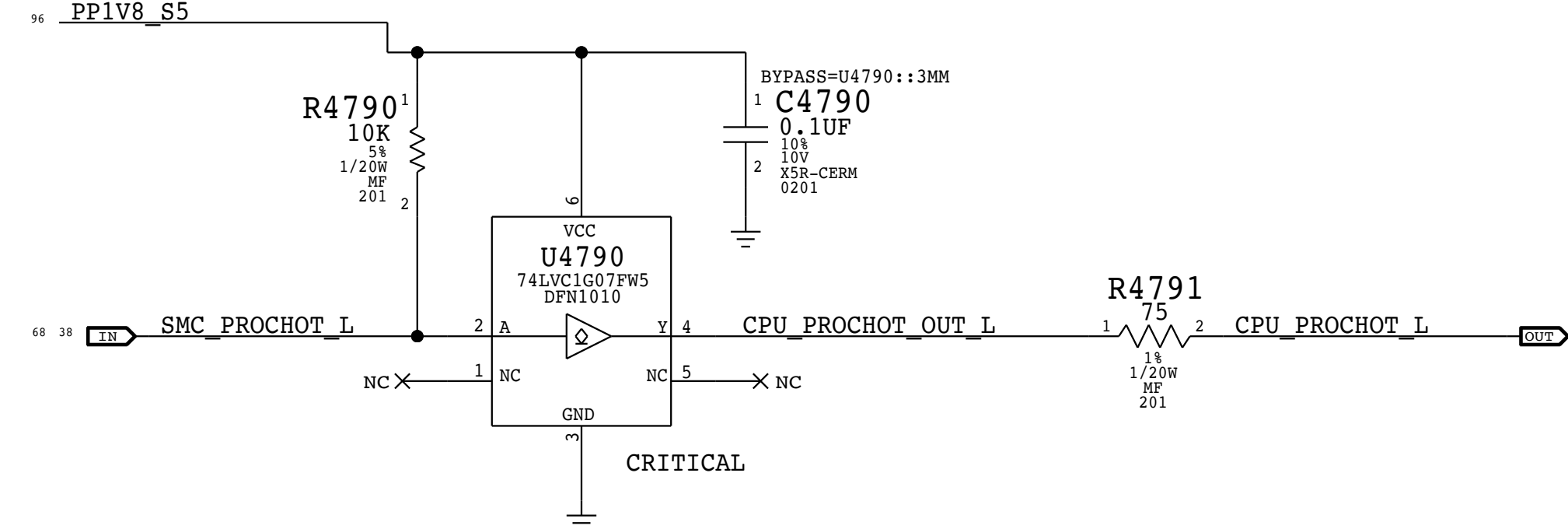
SMC AVREF Supply

Footprint supports 353S01042 alternate

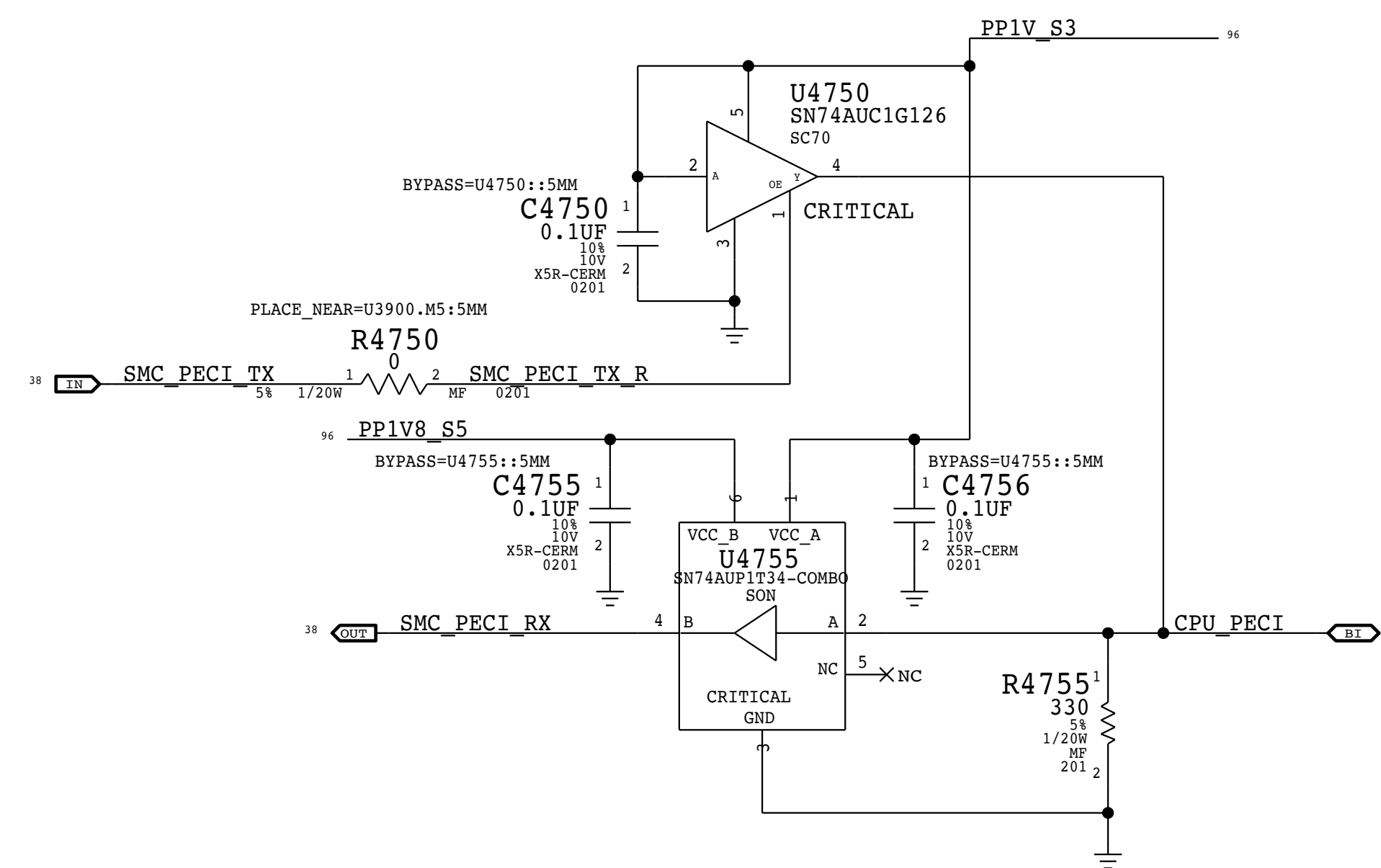


PROCHOT# Level Shifting

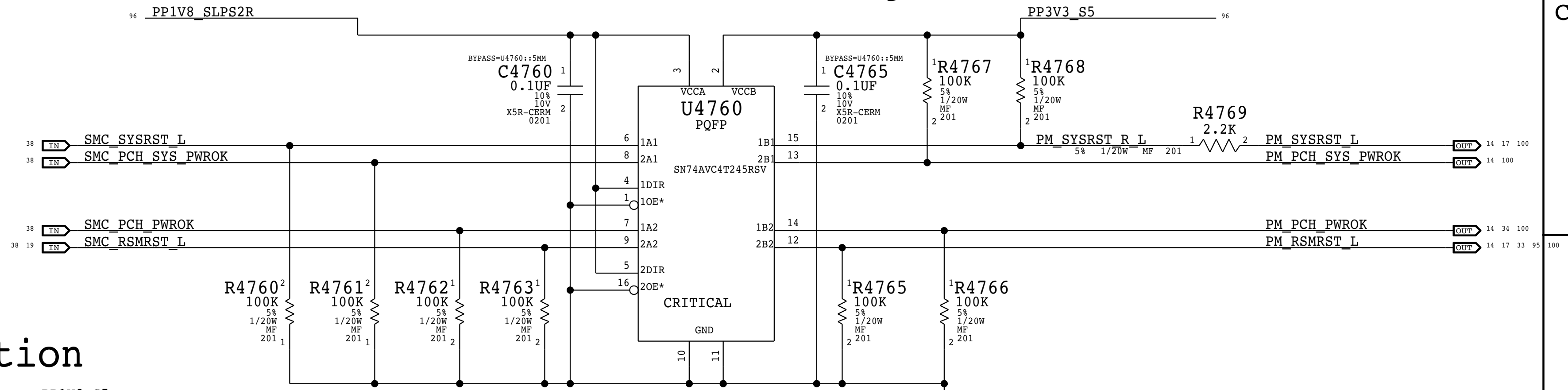
rdar://problem/34583713



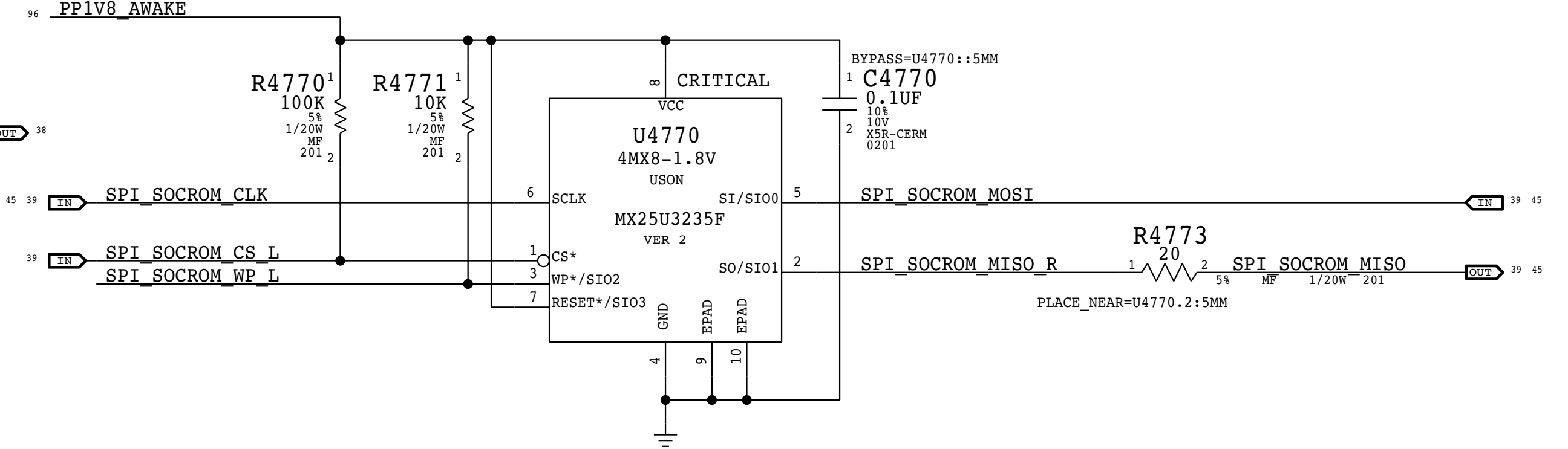
PECI Level Shifting



PCH PM Level Shifting

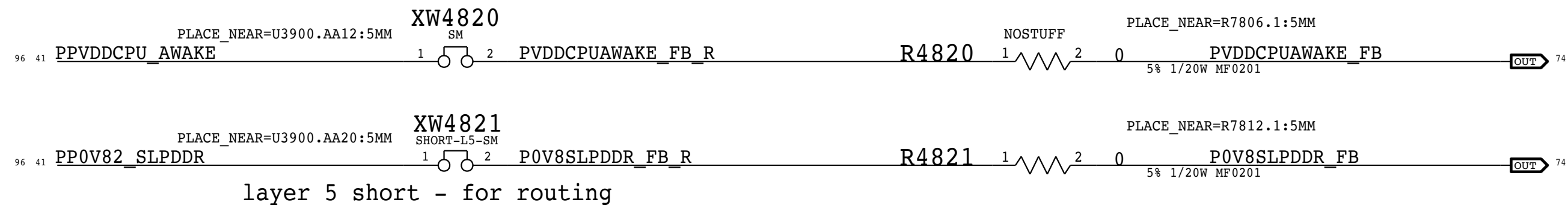


SoC ROM



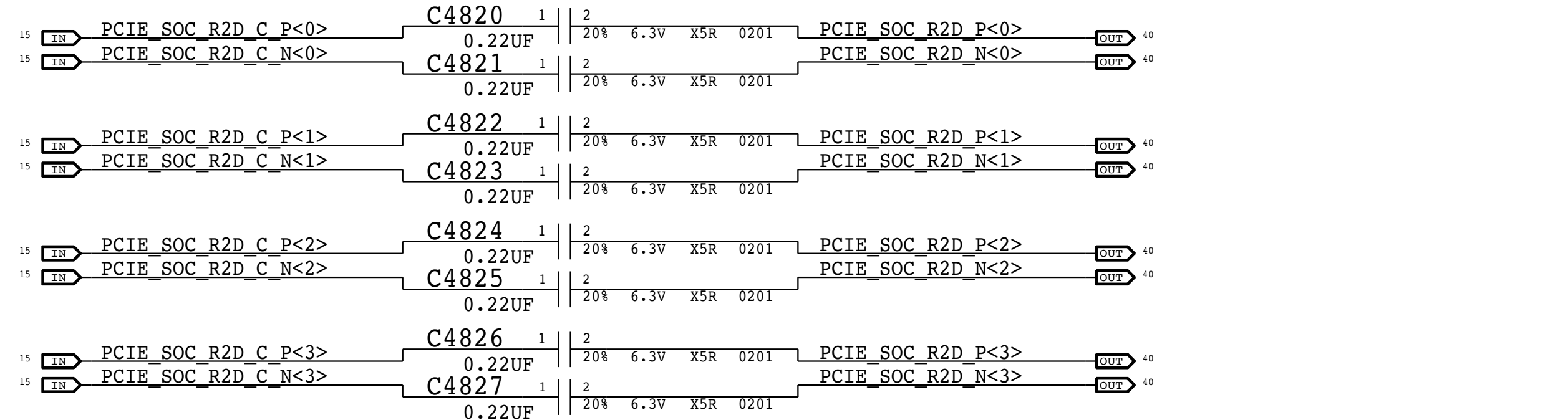
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Alternate Feedback Sense

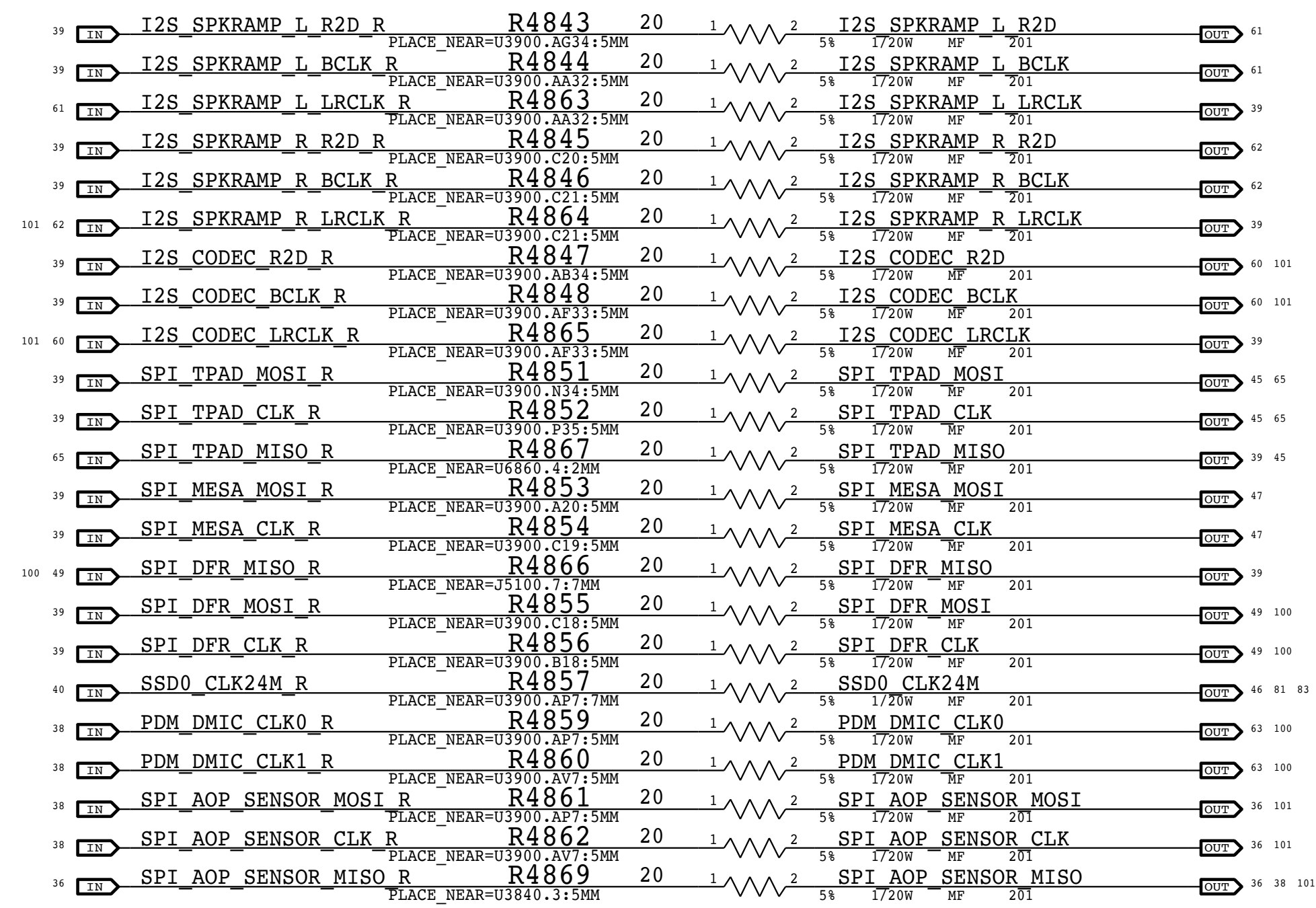


PCIe Up R2D AC Caps

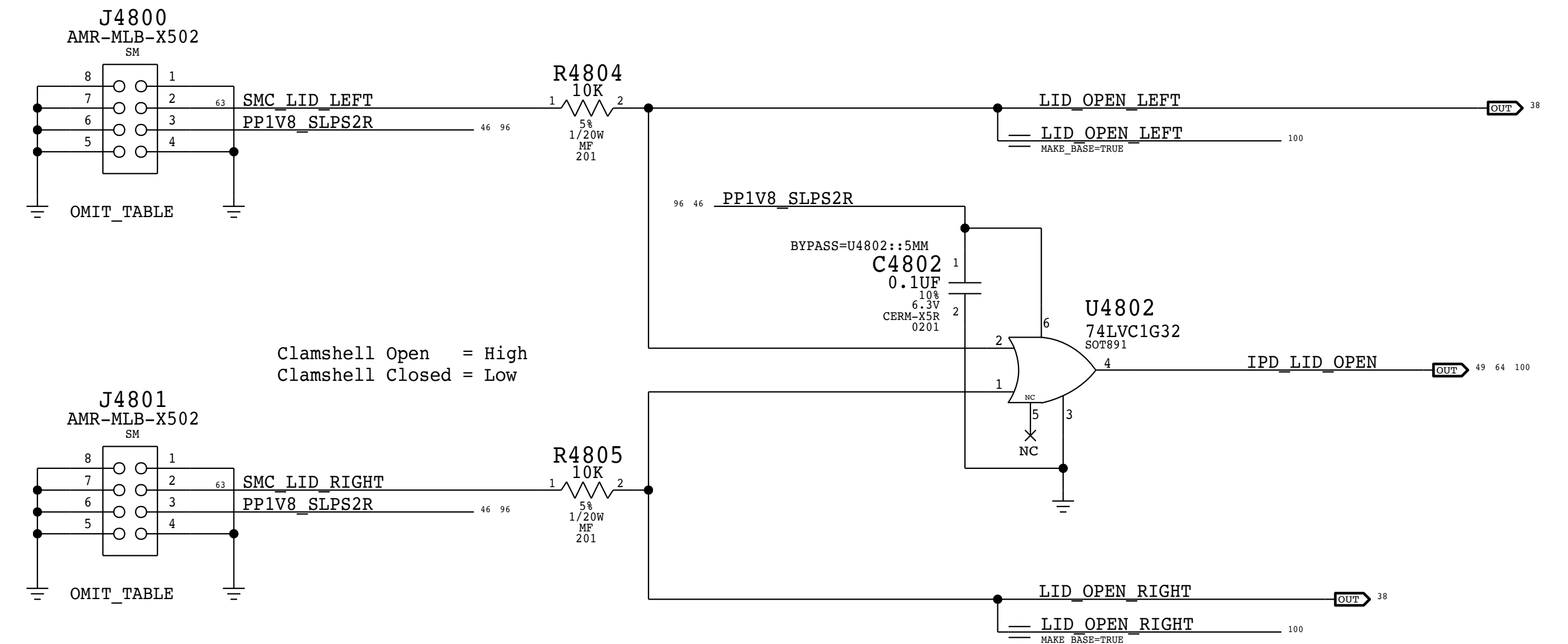
(All Caps Except C4822, C4823)
GND_VOID=TRUE



GPIO Source Termination

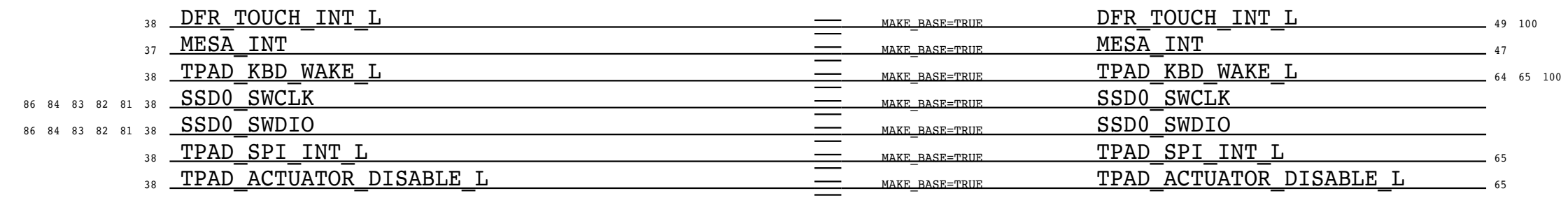


Lid Detect Sensors

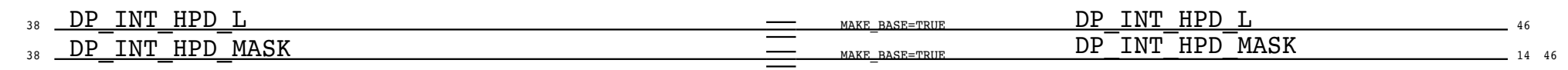


Clamshell Open = High
Clamshell Closed = Low

SOC Overloaded GPIOs

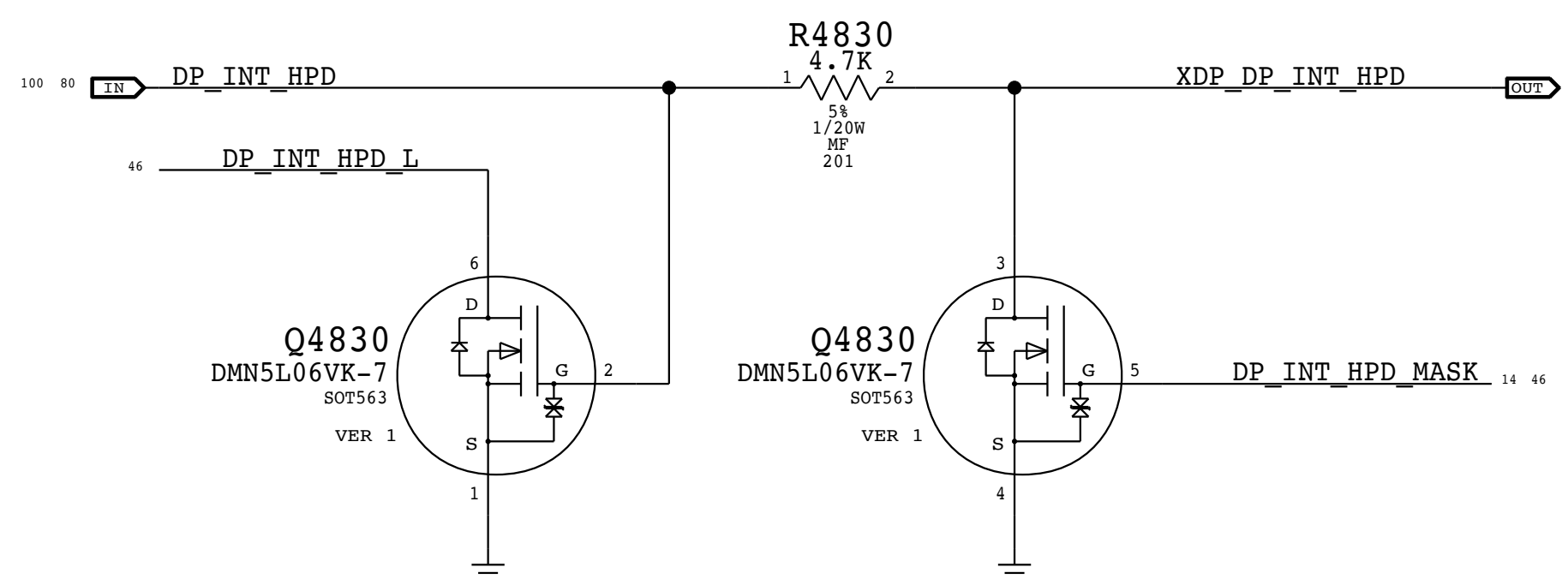


Platform-Specific GPIOs

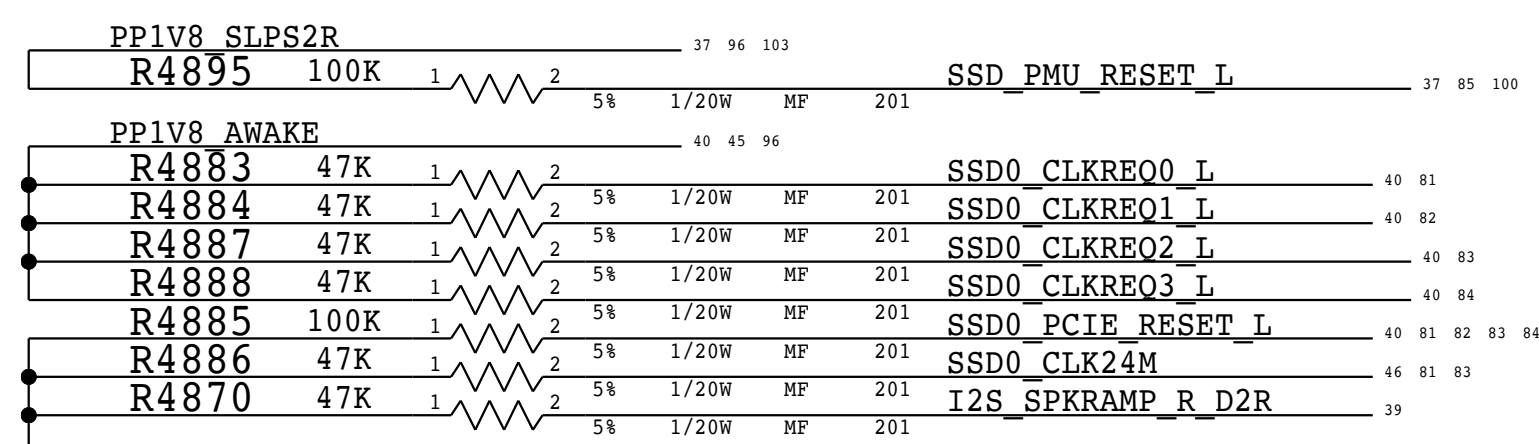


HPD KSF Comp Circuit

R4830 needs to be characterized and adjusted if necessary



Project Specific Pull-Ups



BOM GROUP	BOM OPTIONS
BOARD_REV:111	BOARDREV2, BOARDREV1, BOARDREV0
BOARD_REV:110	BOARDREV2, BOARDREV1
BOARD_REV:101	BOARDREV2, BOARDREV0
BOARD_REV:100	BOARDREV2
BOARD_REV:011	BOARDREV1, BOARDREV0

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARDID2, BOARDID3

BOM_COST_GROUP=SOC

SoC Project Support

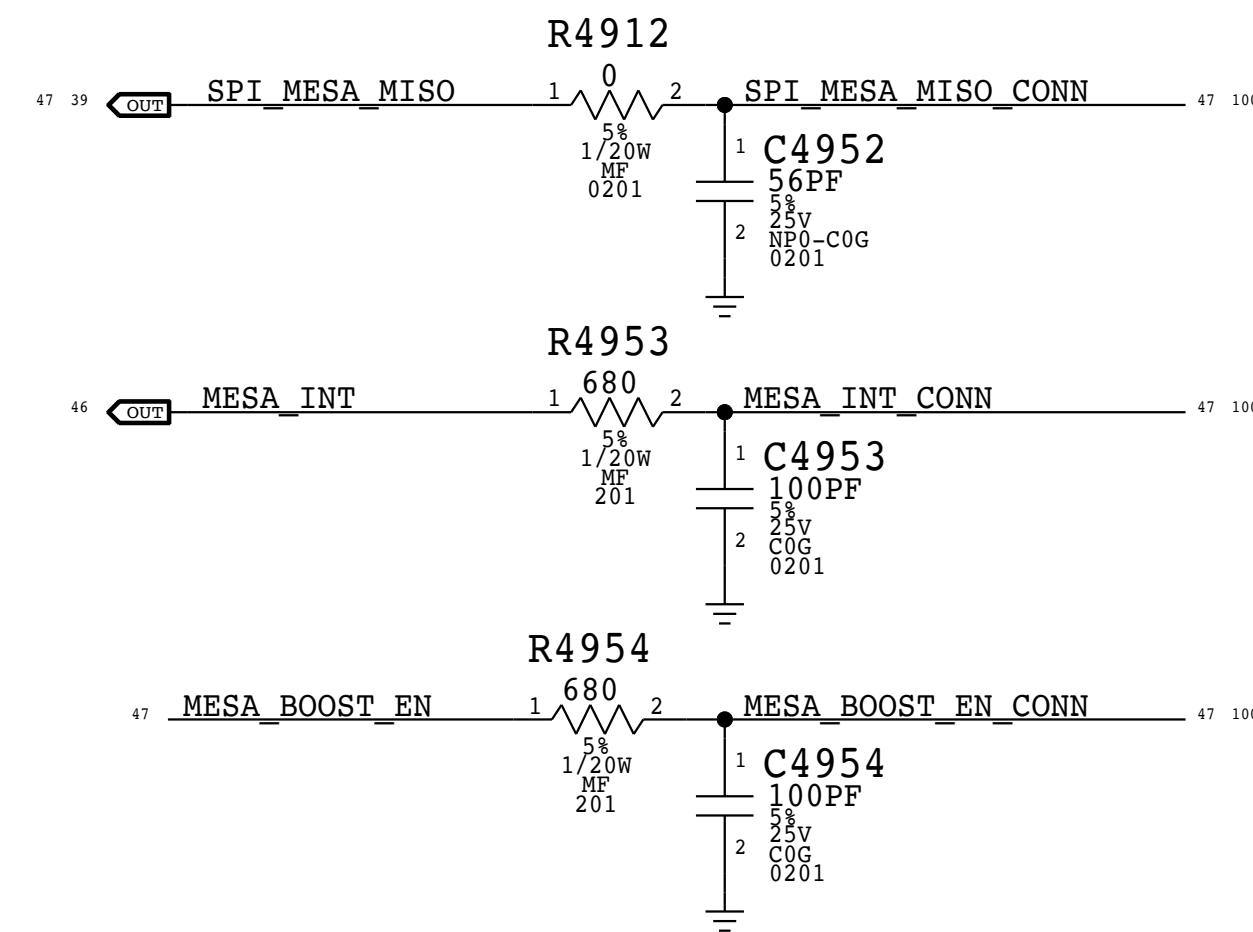
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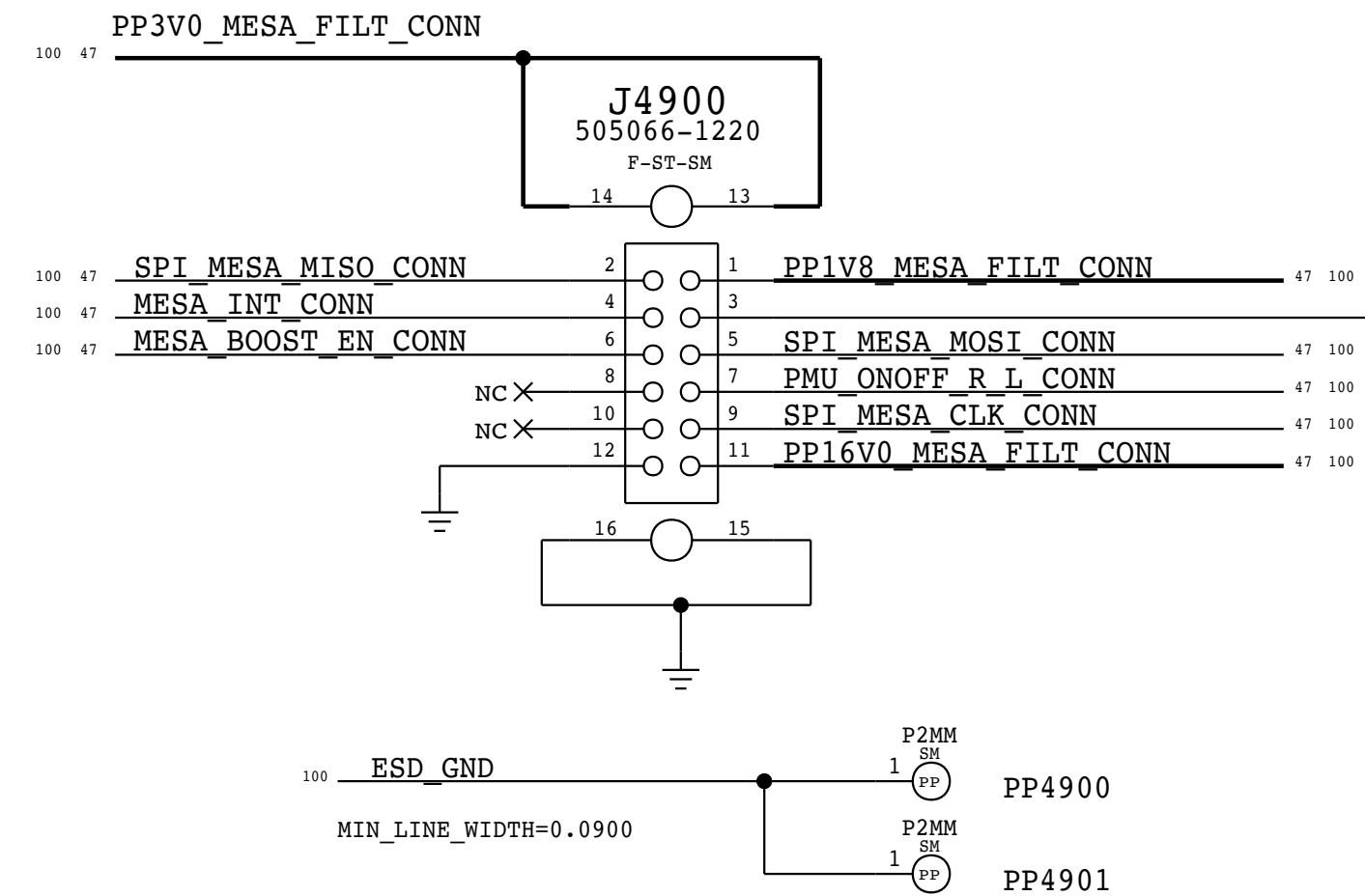
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

ESD Filters



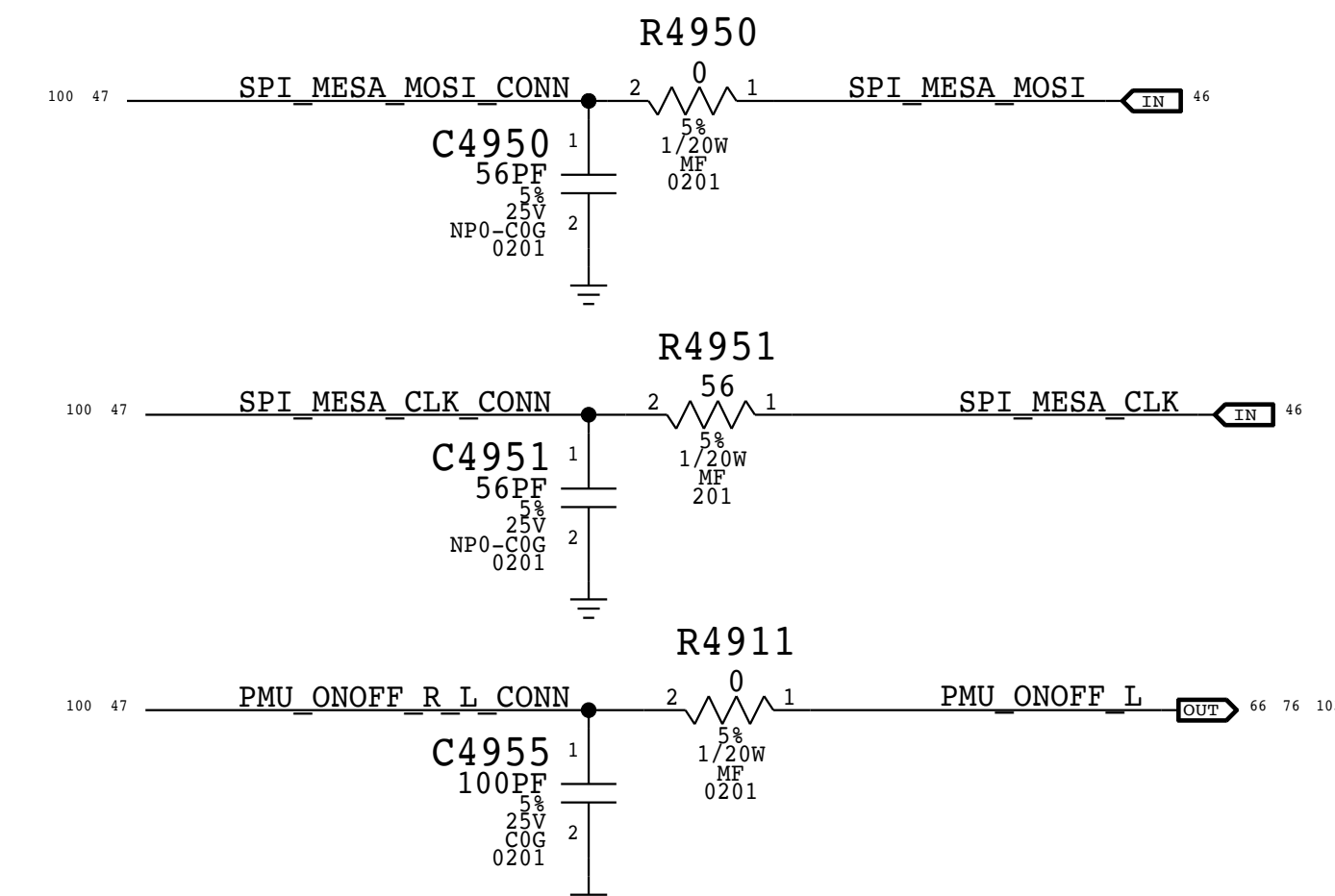
T151 FLEX CONNECTOR

PLUG (516S00115) - X434/ X435 Jumper
RECEPTACLE (516S00203) - MLB



ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

ESD Filters

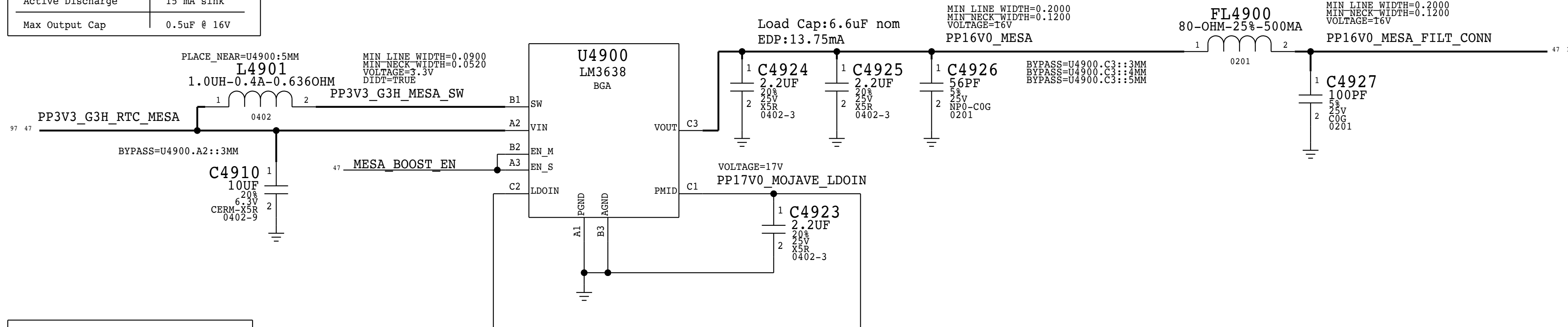


Output Voltage	16.0V +/- 2%
Iout (max avg)	6mA
OCP (min)	13 mA
Active Discharge	15 mA sink
Max Output Cap	0.5uF @ 16V

Mesa Power Sequencing Requirements

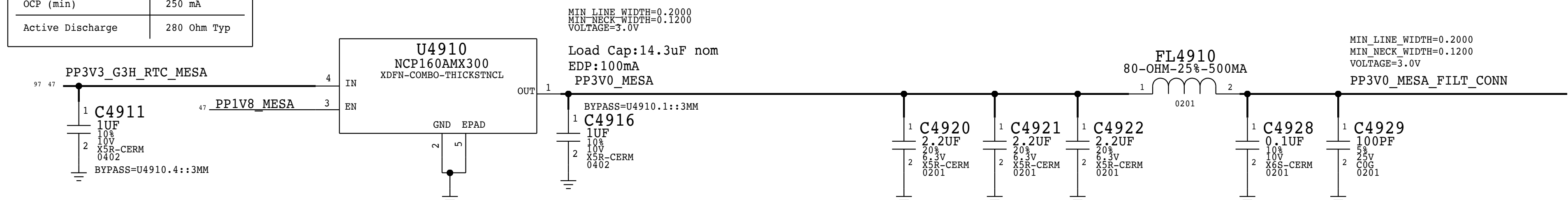
Power On: 1V8 -> 3V3 -> 16V0

MOJAVE 16V BOOST



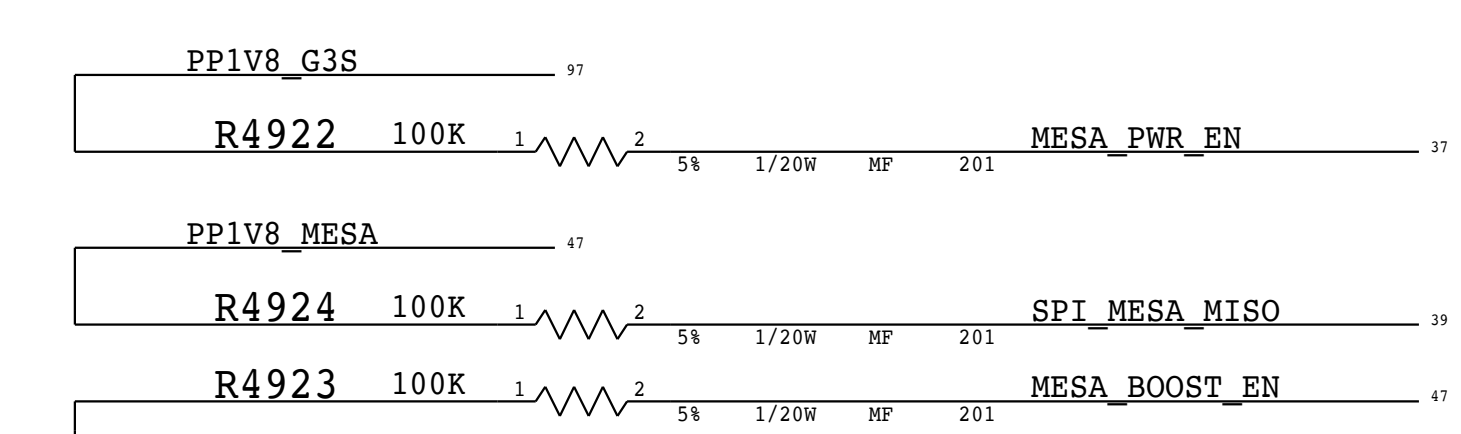
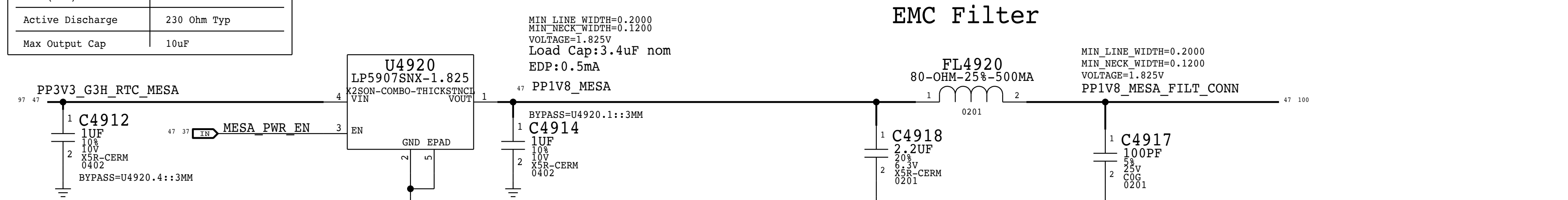
Output Voltage	3.0V +/- 2%
Iout (max avg)	250mA
Dropout Voltage	155mV
OCP (min)	250 mA
Active Discharge	280 Ohm Typ

3.0V MESA



Output Voltage	1.825V +/- 2%
Iout (max avg)	250mA
Dropout Voltage	50mV Typ @ 100mA
OCP (min)	250 mA
Active Discharge	230 Ohm Typ
Max Output Cap	10uF

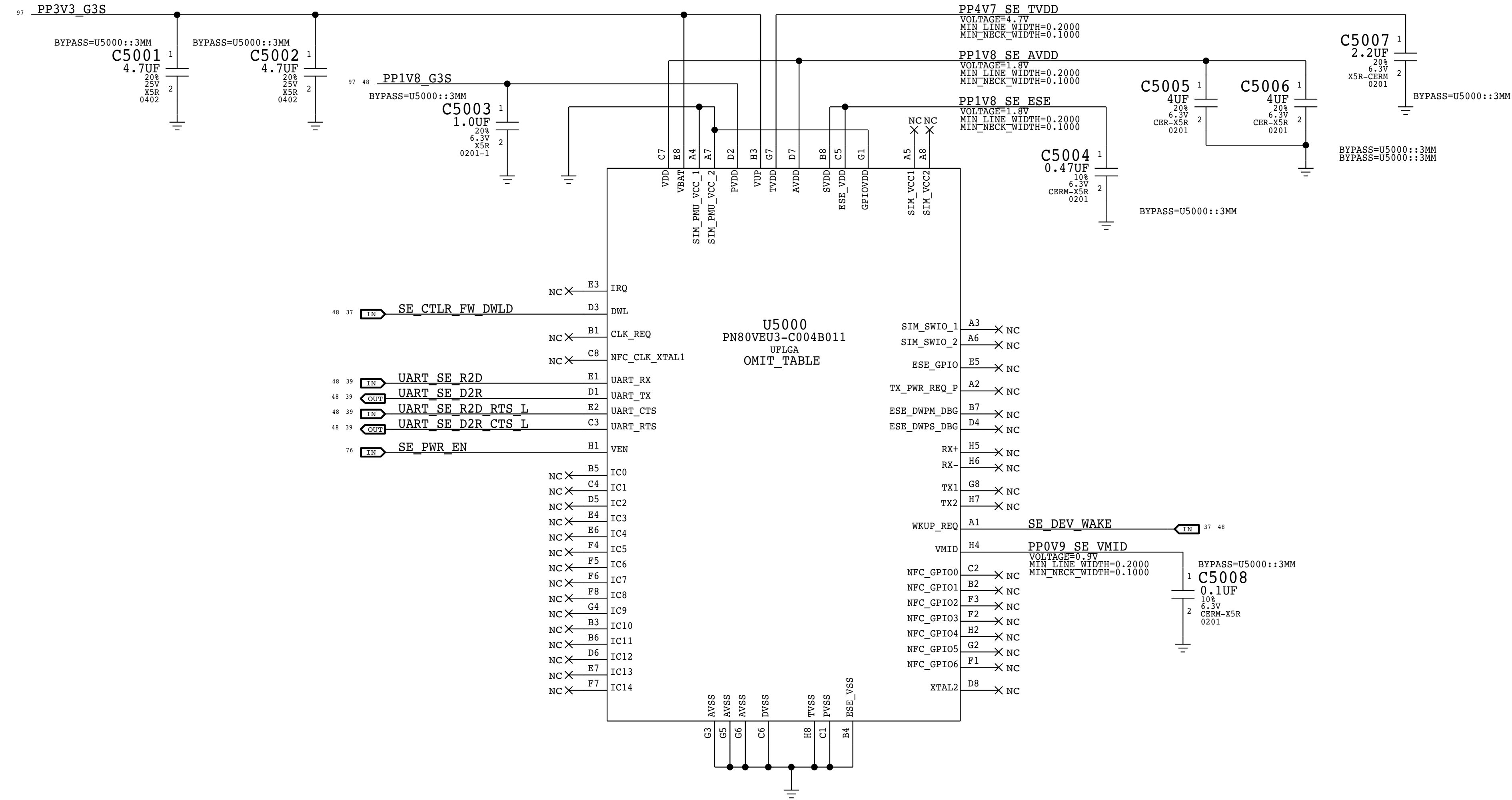
1.8V MESA



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T151		
Apple Inc.		DRAWING NUMBER 051-02166
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REVISION 4.0.0		BRANCH evt-mars-0
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BOM_COST_GROUP=T151

STOCKHOLM

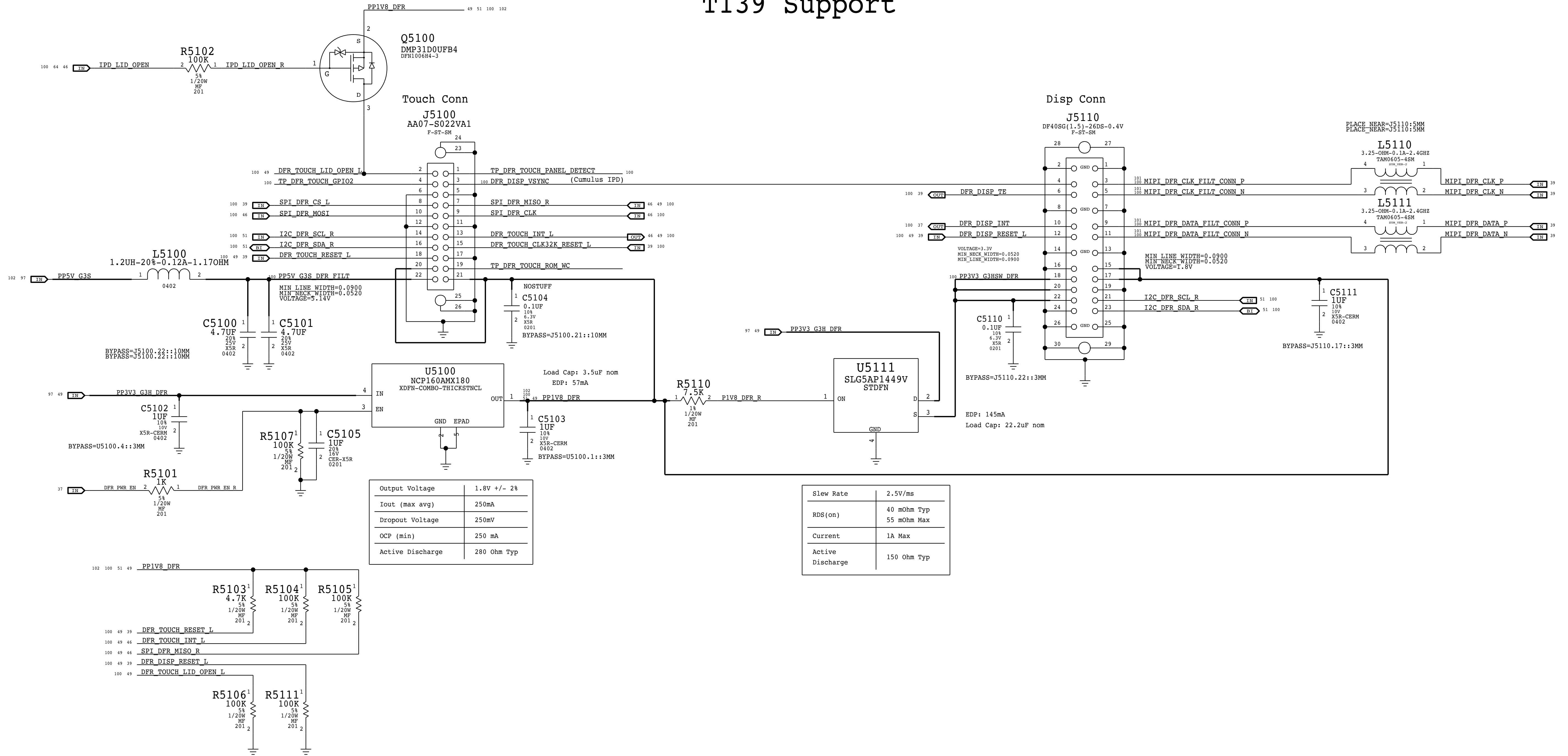


Part	Value	Footprint	Package	Quantity	Ref	Target
R5001	100K	1	MF	201	39	UART_SE_R2D
R5002	100K	1	MF	201	39	UART_SE_D2R
R5003	100K	1	MF	201	39	UART_SE_R2D_RTS_L
R5004	100K	1	MF	201	39	UART_SE_D2R_CTS_L
R5000	100K	1	MF	201	37	SE_CTLR_FW_DWLD
R5005	100K	1	MF	201	37	SE_DEV_WAKE

BOM_COST_GROUP=SOC

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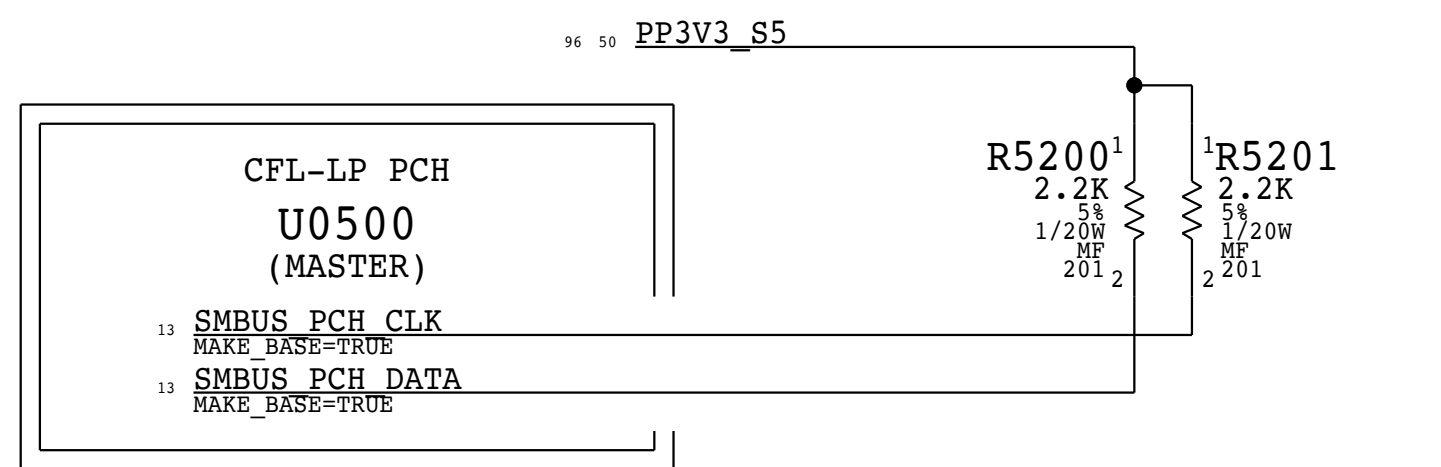
T139 Support



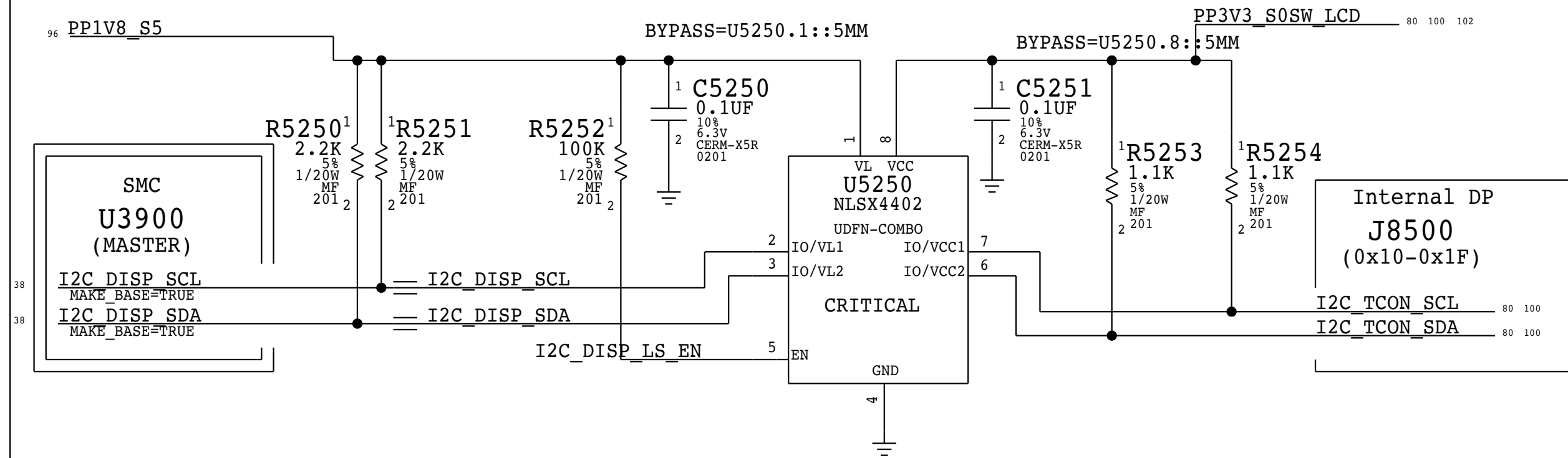
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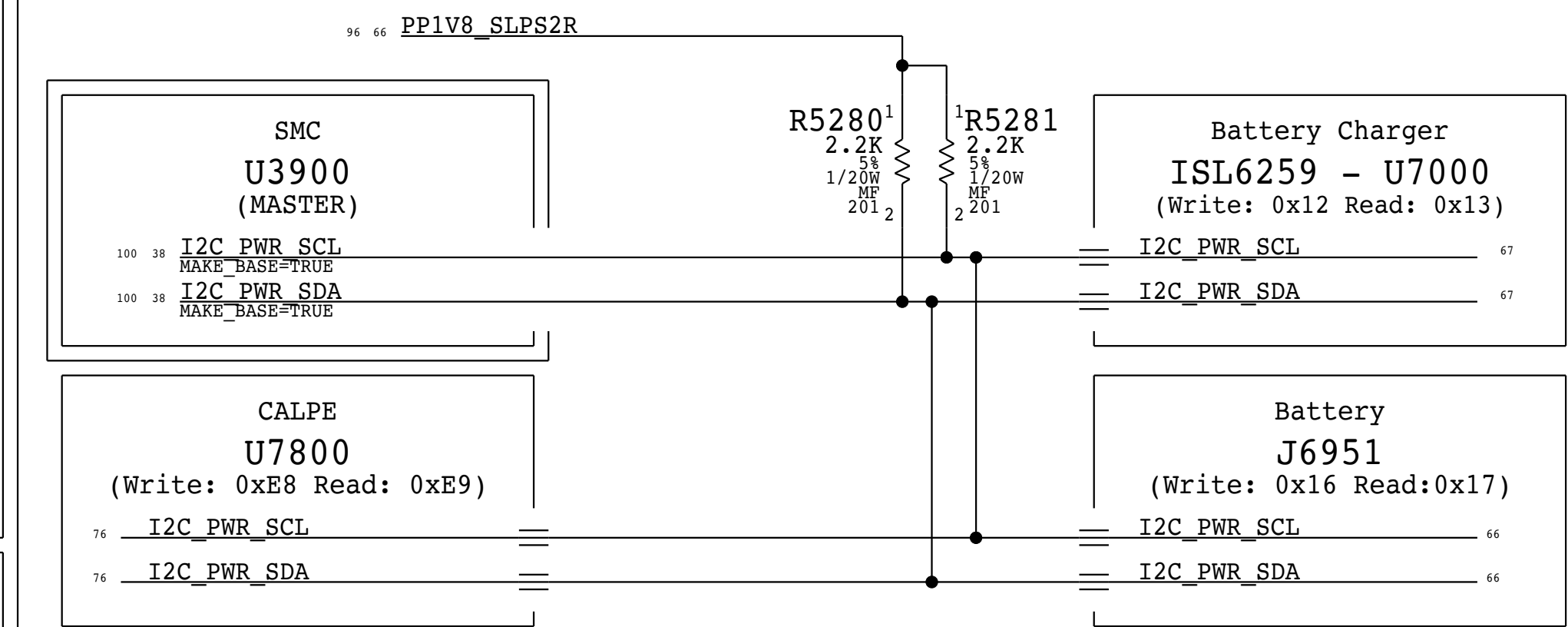
CNL-LP PCH S0 "SMBus 0" Connections



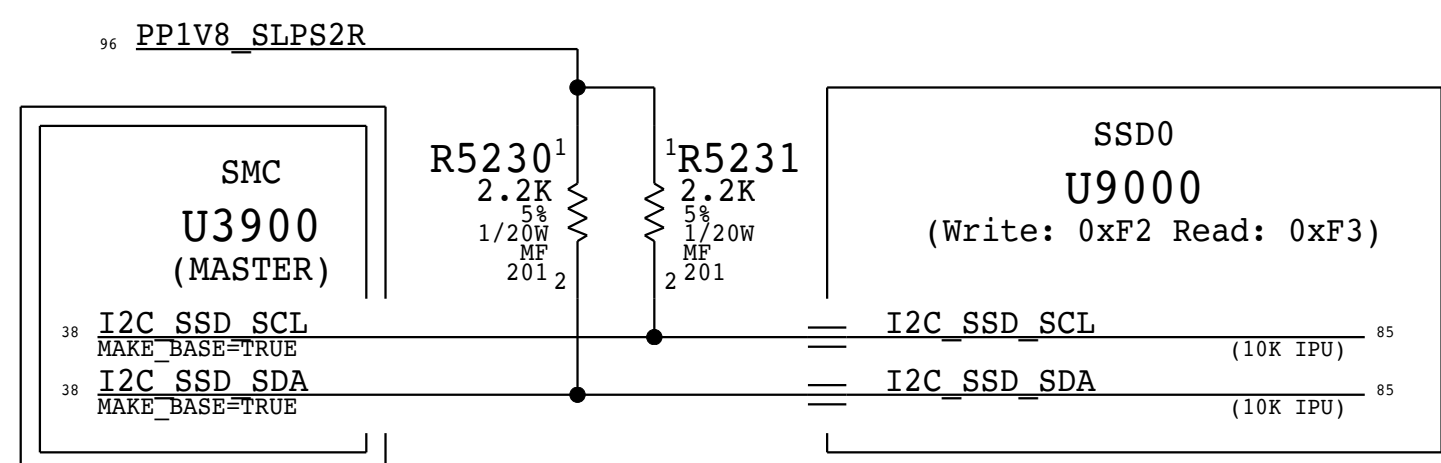
SMC I2C "3" S0 Connections



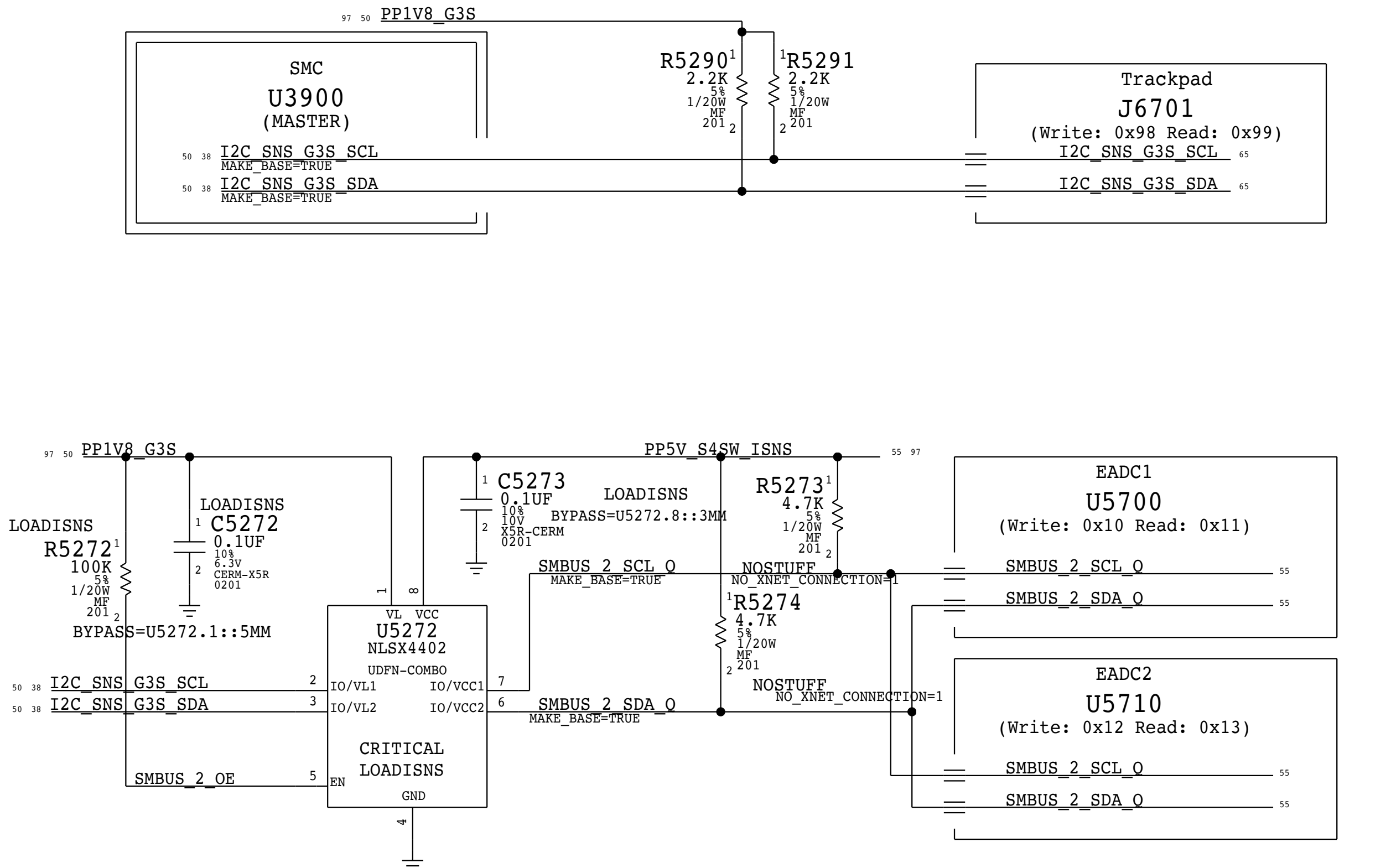
SMC I2C "4" G3H Connections



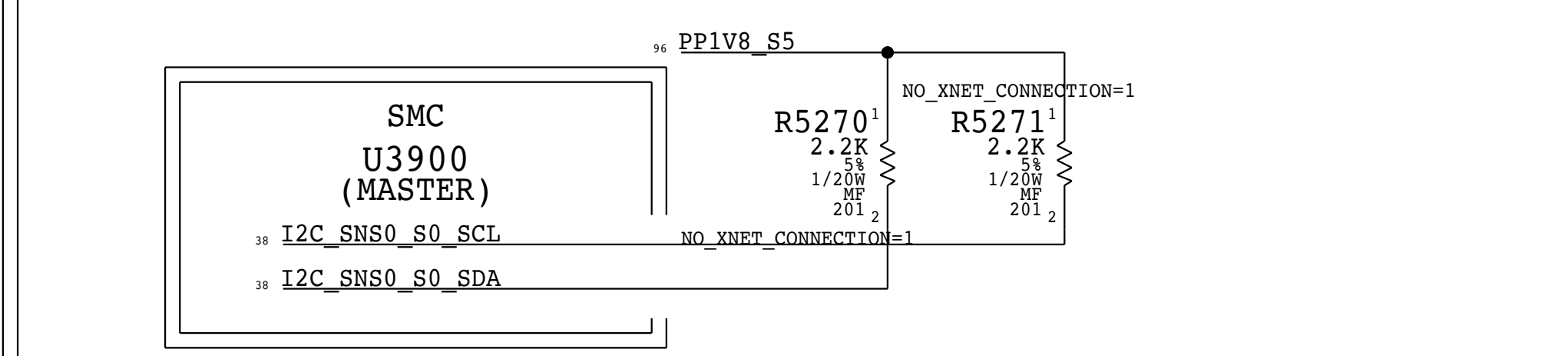
SMC I2C "6" G3H Connections



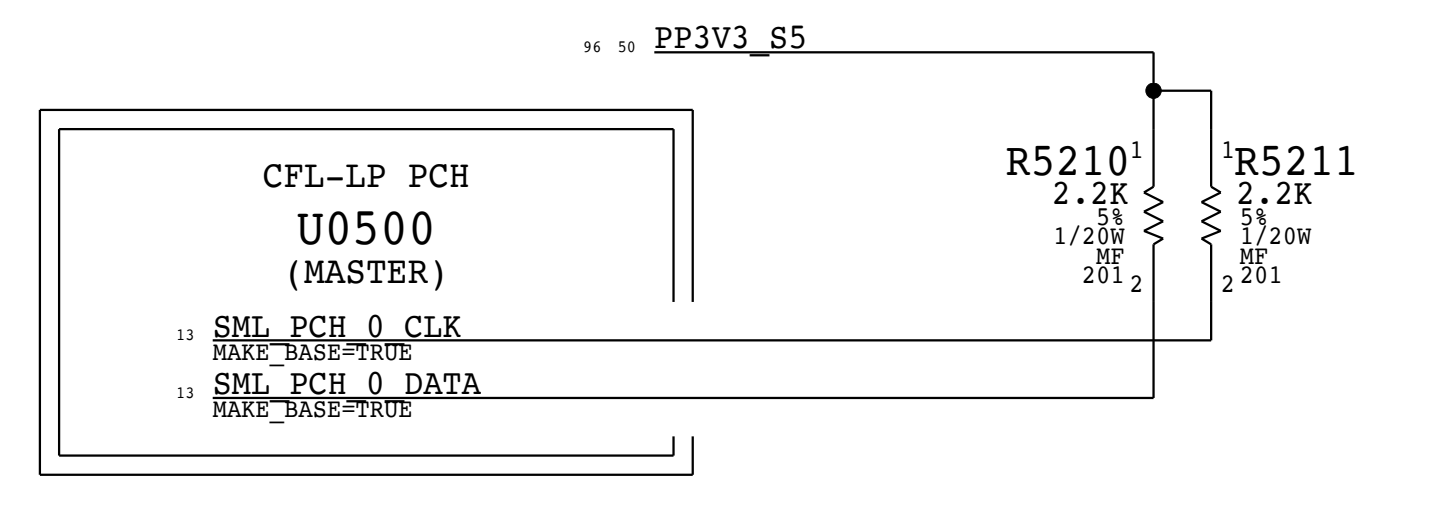
SMC I2C "5" G3S Connections



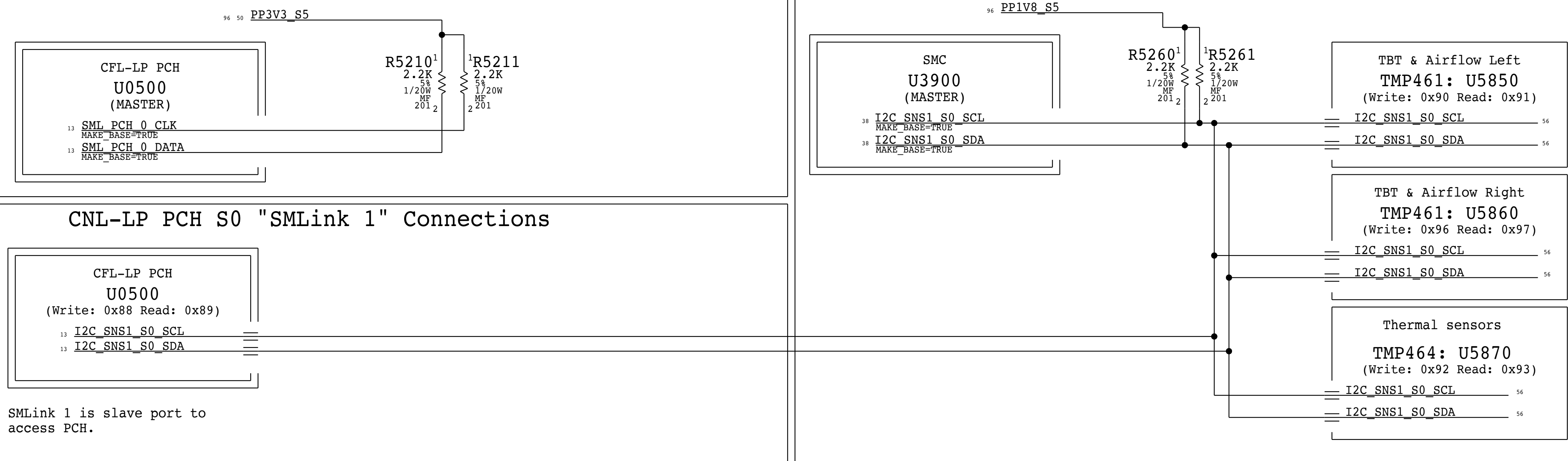
SMC I2C "1" S0 Connections



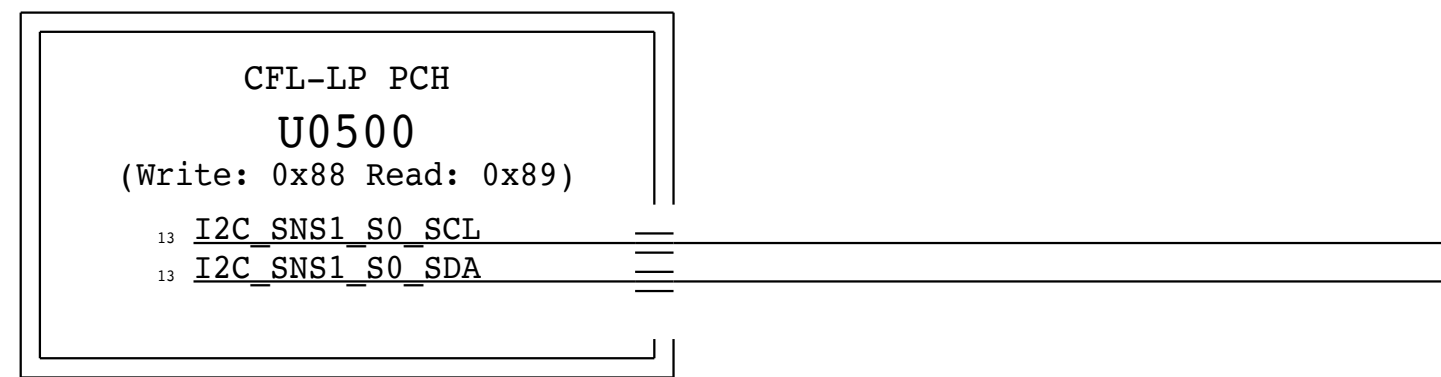
CNL-LP PCH S0 "SMLink 0" Connections



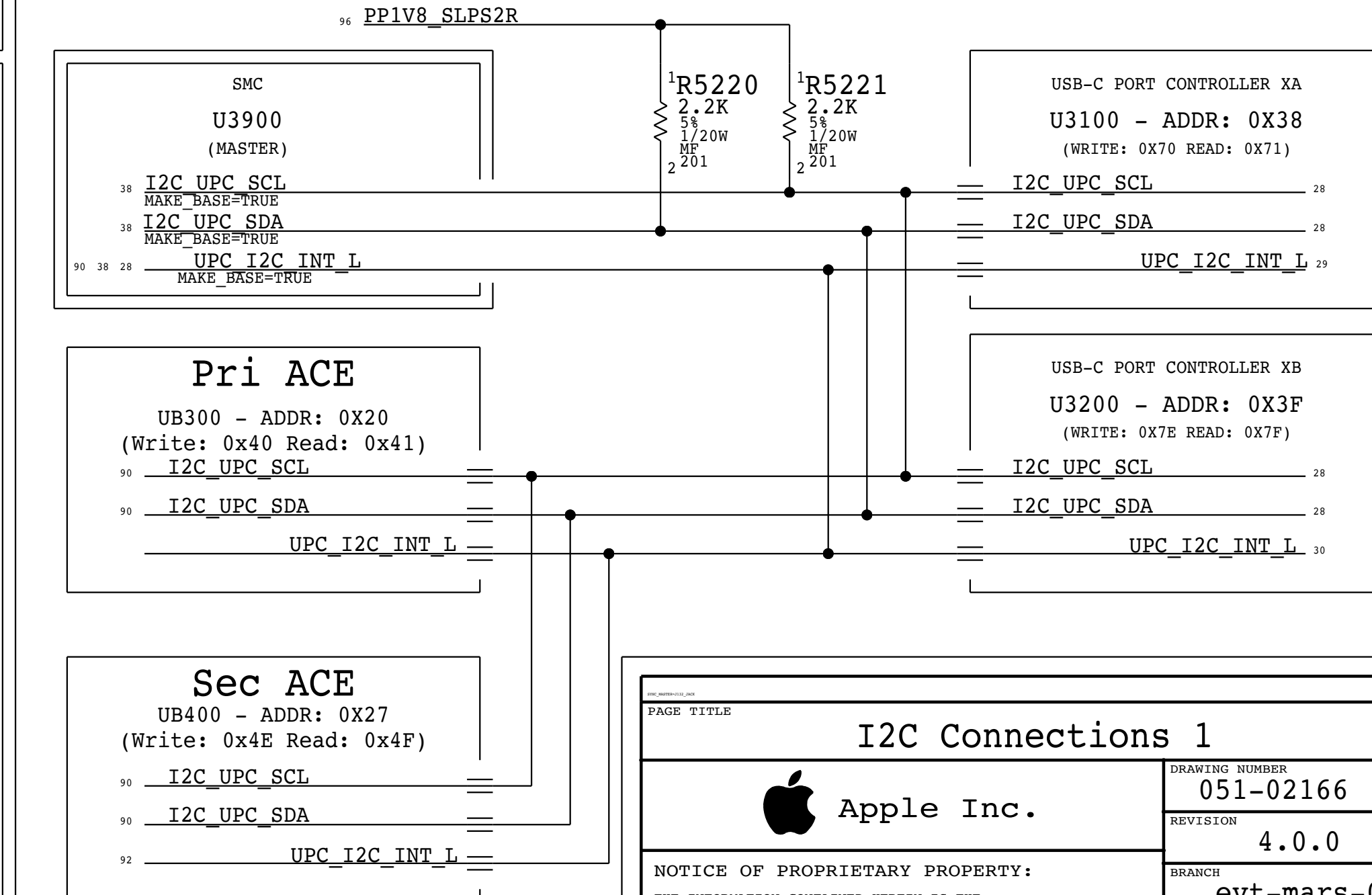
SMC I2C "2" S0 Connections



CNL-LP PCH S0 "SMLink 1" Connections



SMC I2C "0" G3H CONNECTIONS

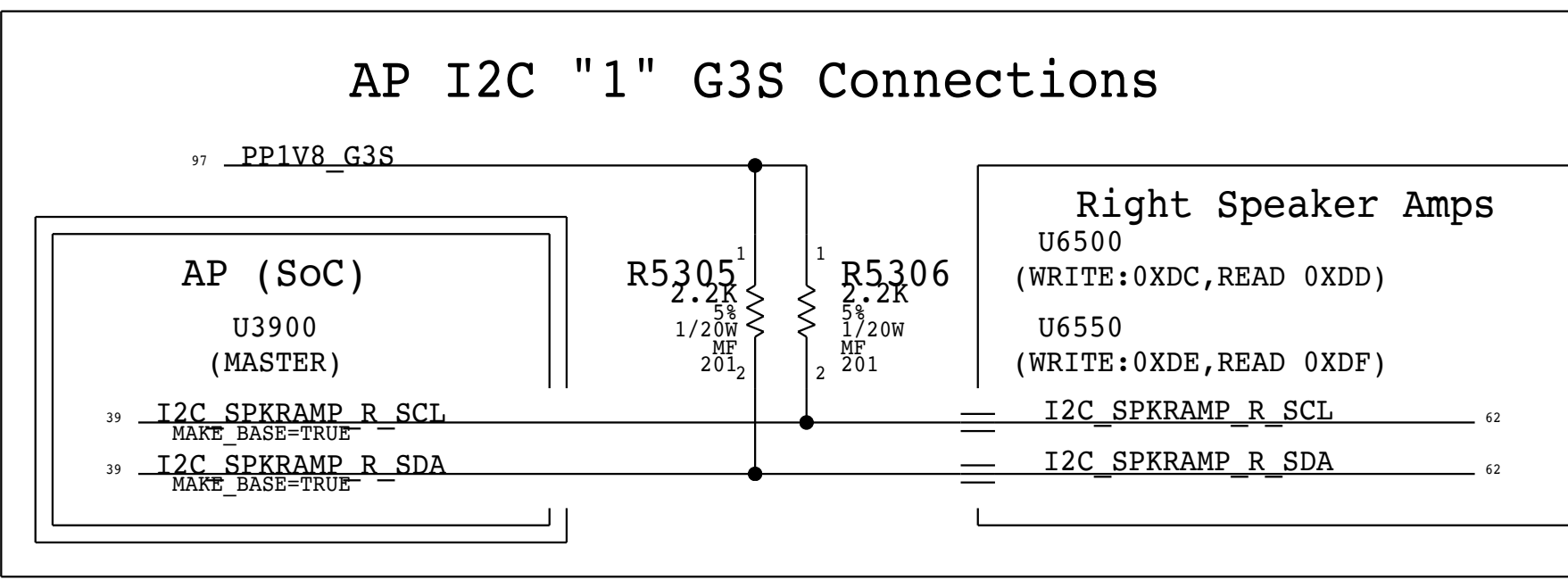
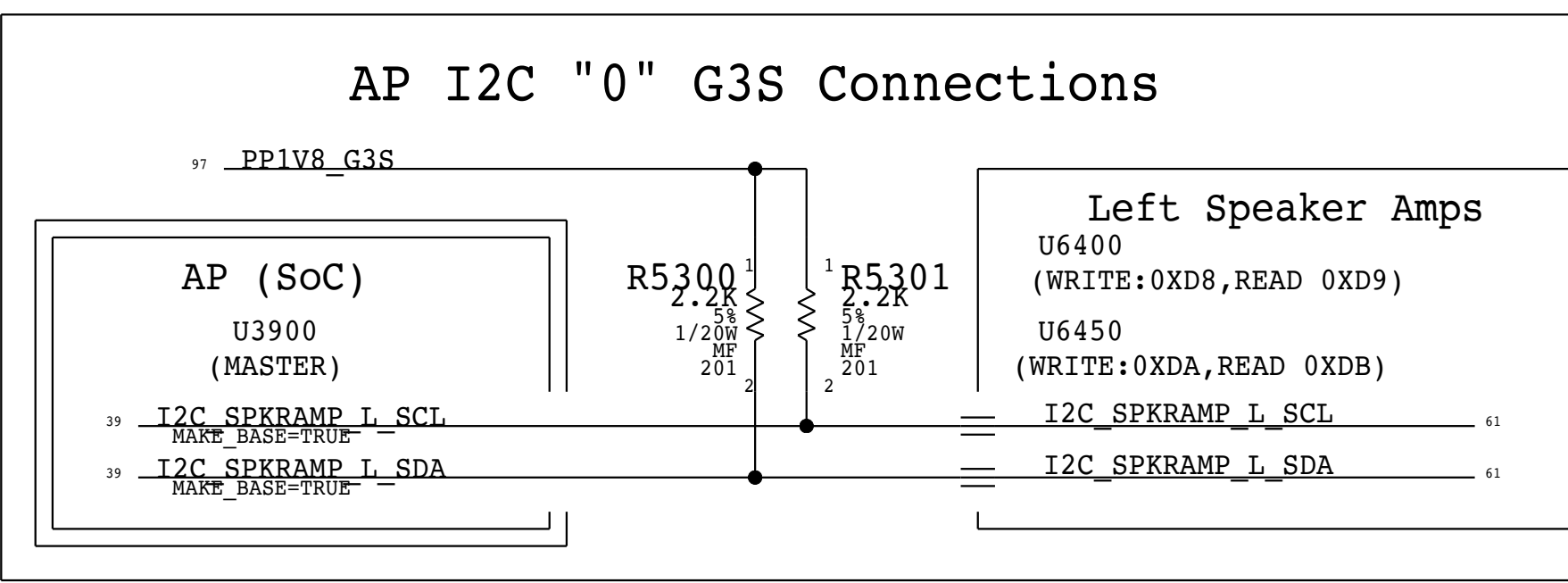


SMLink 1 is slave port to access PCH.

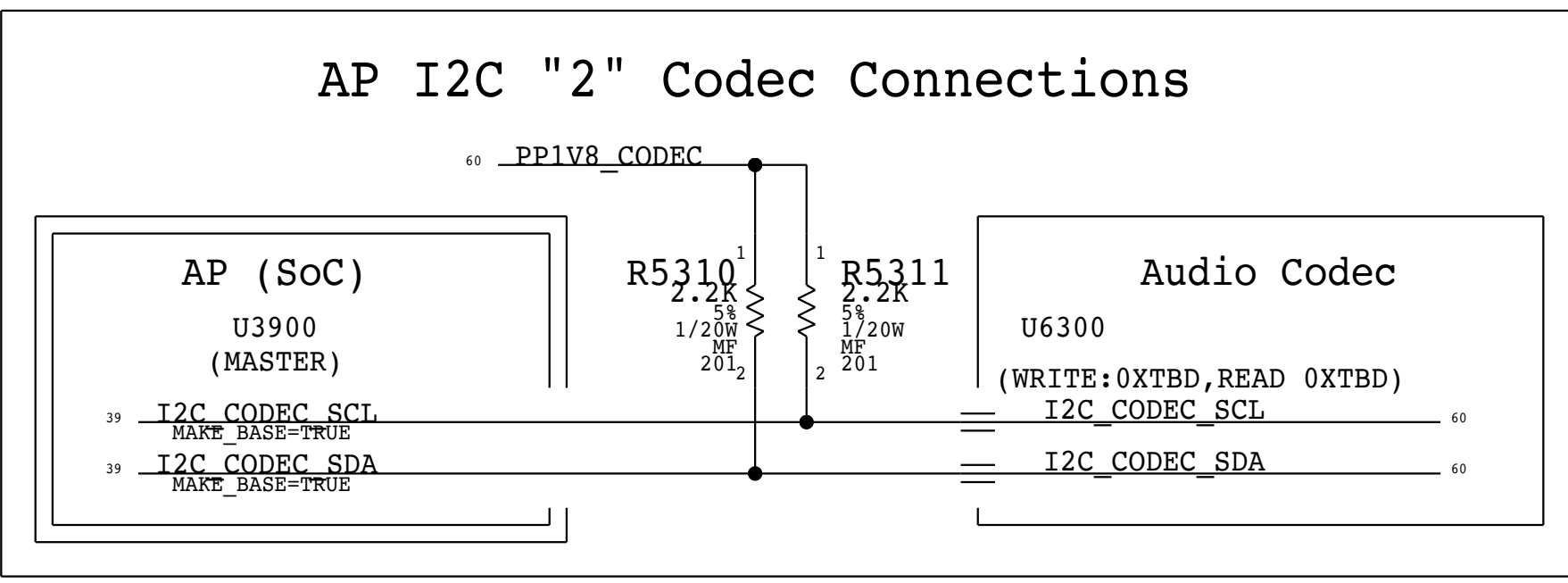
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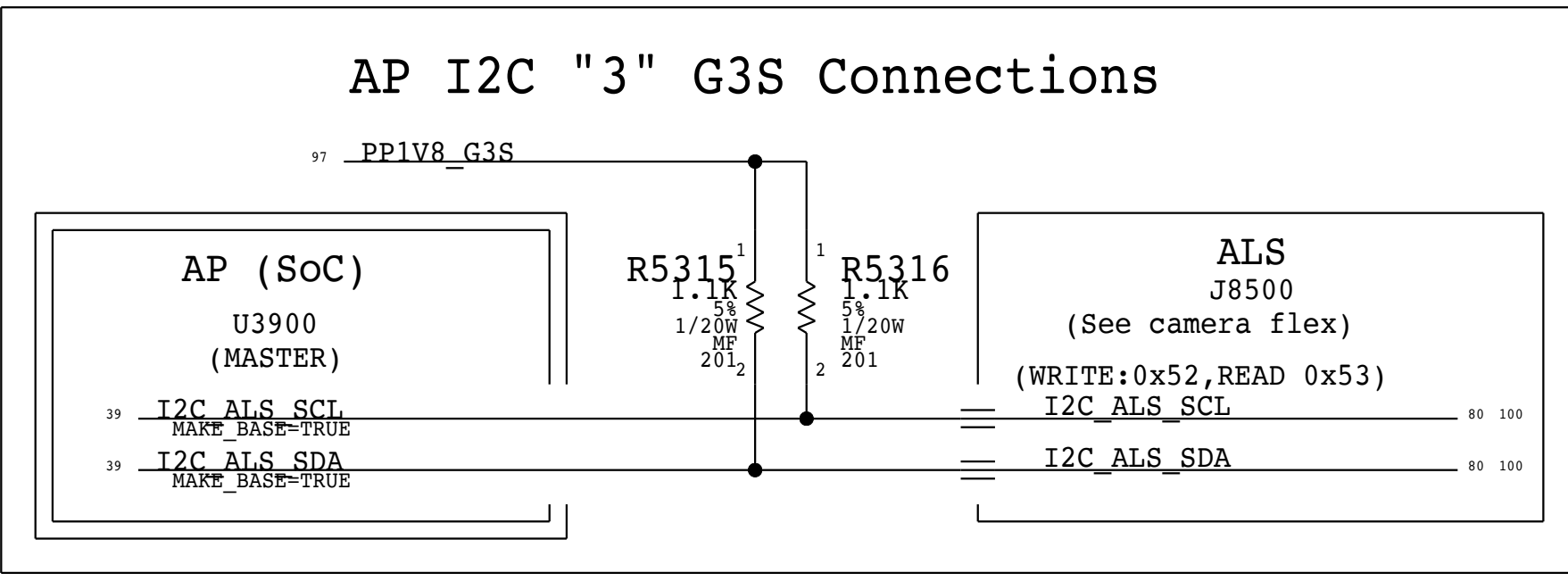
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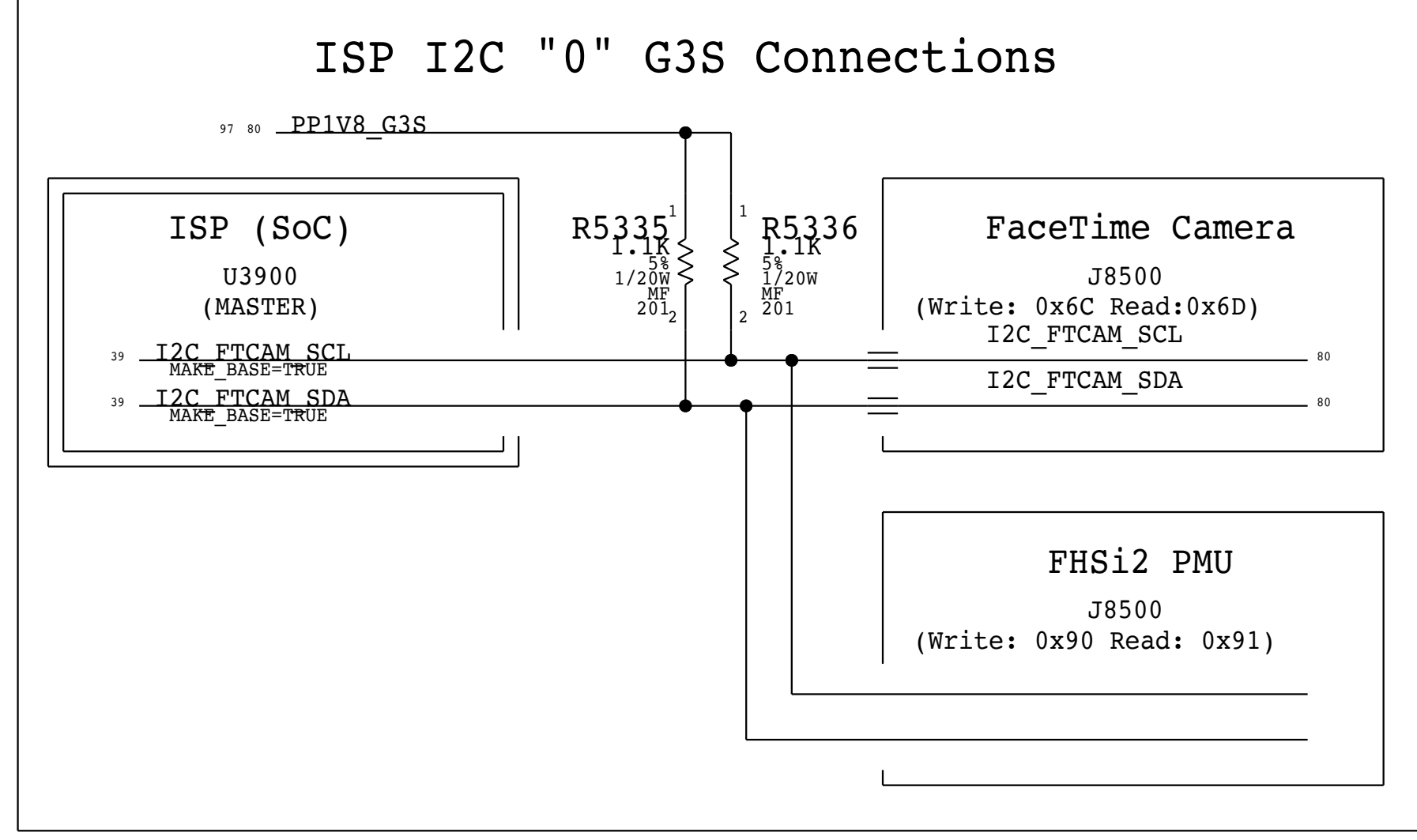
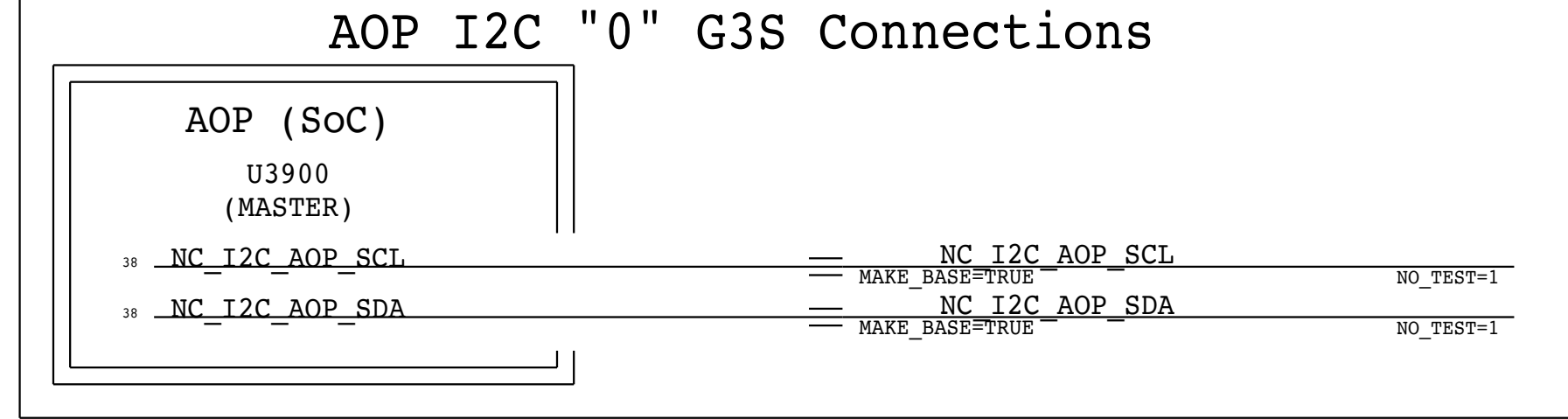
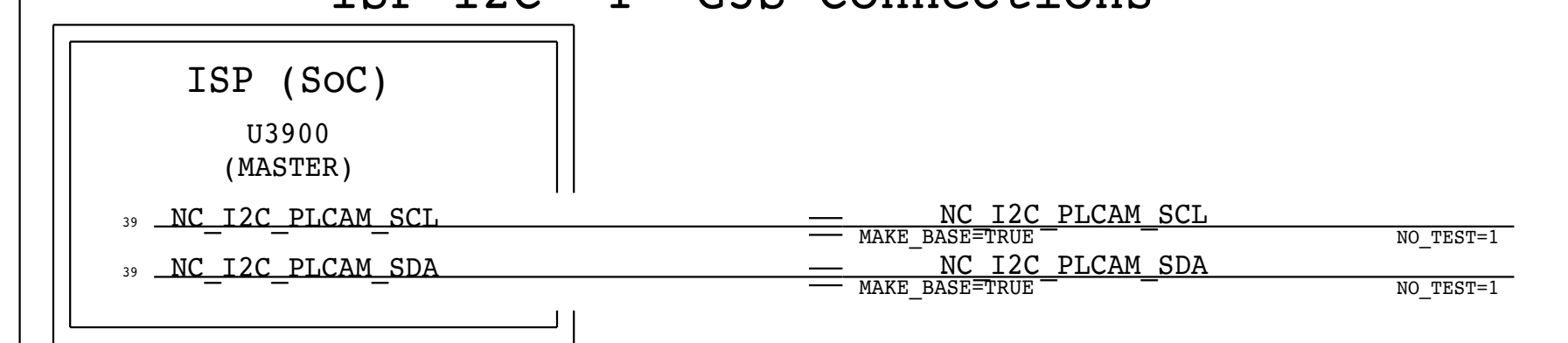
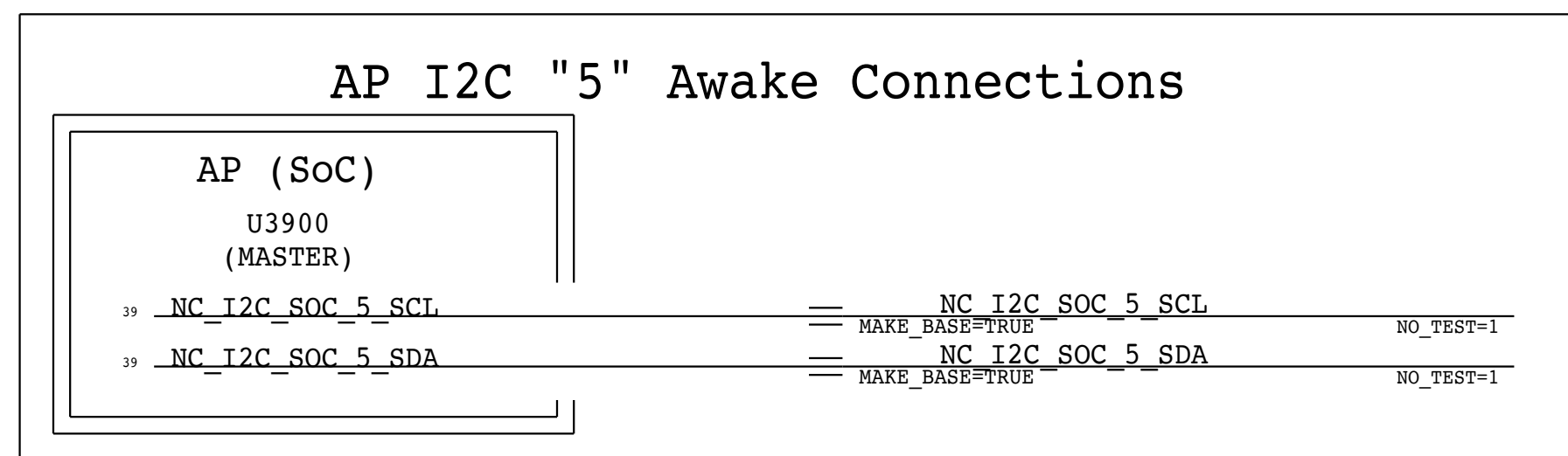
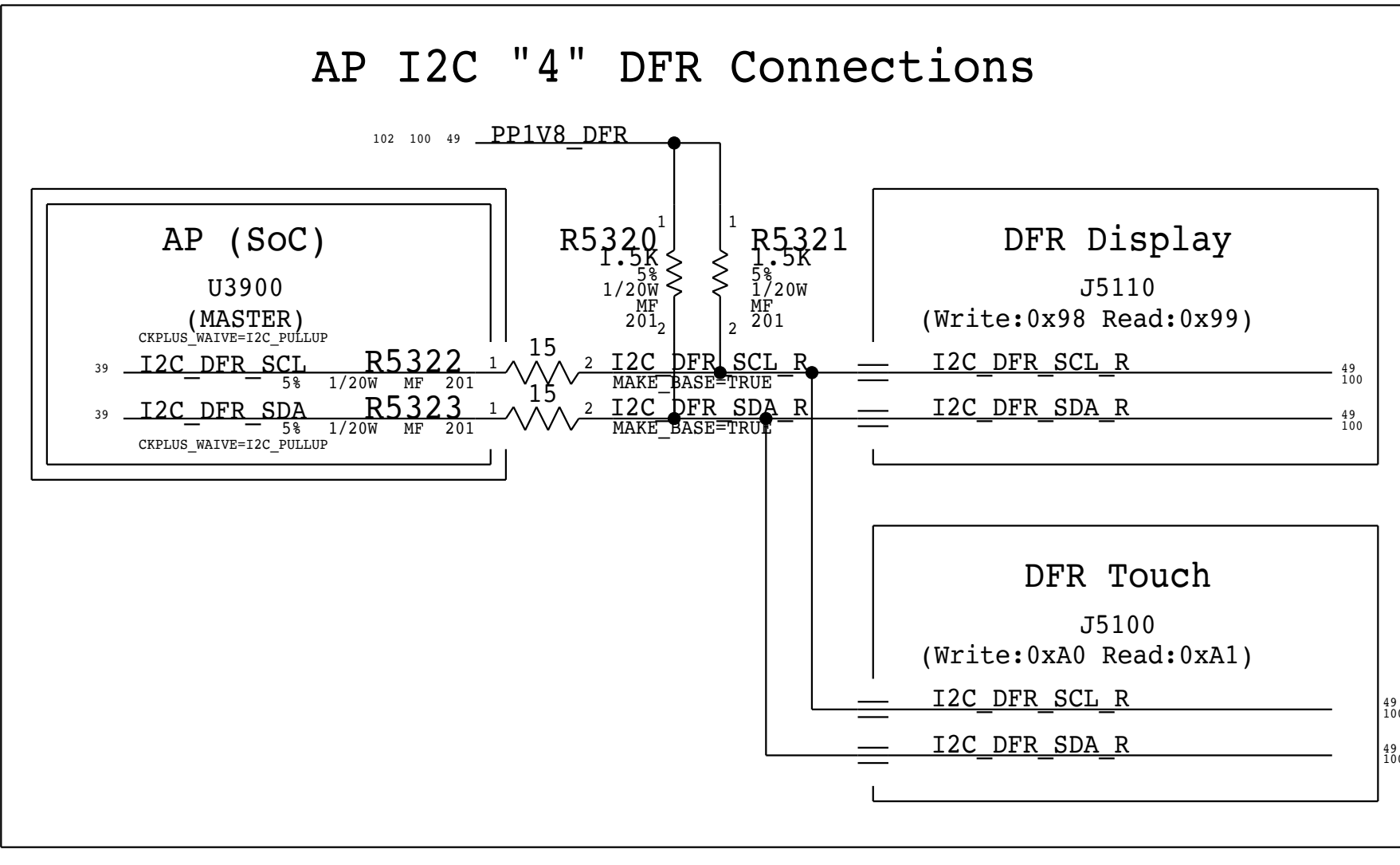
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Device	SMC IF	ADDR. (8b)
ACE XA	I2C0	0X70/1
ACE XB	I2C0	0X7E/F
ACE TA	I2C0	0X40/1
ACE TB	I2C0	0X4E/F
NC.	I2C1	
Temp. Sensor Left	I2C2	0X90/1
Temp. Sensor Right	I2C2	0X96/7
Platform Thermal Sensor	I2C2	0X92/3
PCH	I2C2	0X88/9
TCON	I2C3	0X10-1F
Charger	I2C4	0X12/3
Battery	I2C4	0X16/7
Calpe	I2C4	0XE8/9
Trackpad	I2C5	0X98/9
EADC1	I2C5	0X10/1
EADC2	I2C5	0X12/3
SSD	I2C6	0XF2/3
SoC IF		
Left Spkr Amp.(U6400)	I2C0	0XD8/9
Left Spkr Amp.(U6450)	I2C0	0XDA/B
Right Spkr Amp.(U6500)	I2C1	0XDC/D
Right Spkr Amp.(U6550)	I2C1	0XDE/F
Audio Codec	I2C2	0X90/1
ALS	I2C3	0X52/3
DFR Display	I2C4	0X98/9
DFR Touch	I2C4	0XA0/1
NC.	I2C5	
Spkr ID1	I2C6	
Spkr ID0	I2C6	
SIP IF		
FT Camera	I2C0	0X6C/D
FHSi2	I2C0	0X90/1
NC.	I2C1	
AOP IF		
NC.	I2C0	

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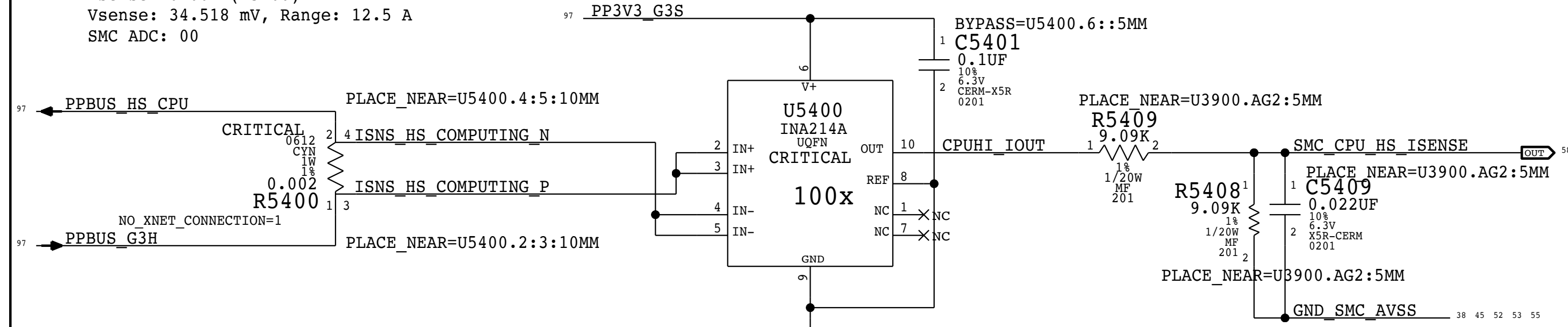
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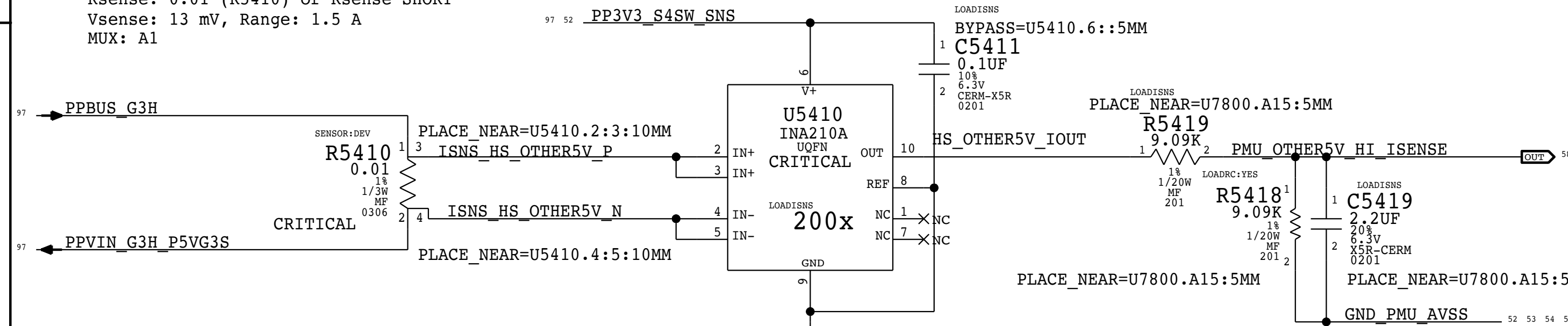
CPU High Side Current Sense (ICOR)

Gain: 100x, EDP: 17.259 A
 Rsense: 0.002 (R5400)
 Vsense: 34.518 mV, Range: 12.5 A
 SMC ADC: 00



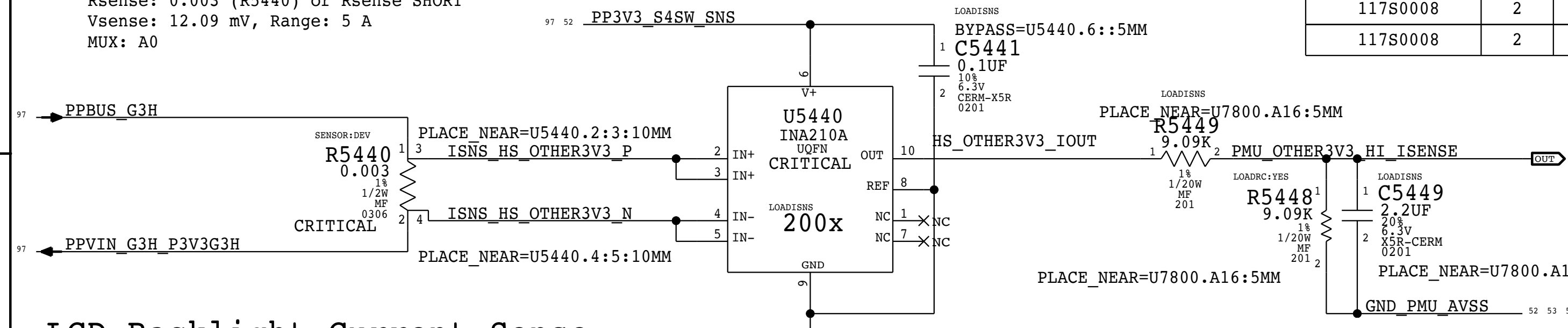
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.3 A
 Rsense: 0.01 (R5410) or Rsense SHORT
 Vsense: 12.09 mV, Range: 1.5 A
 MUX: A1



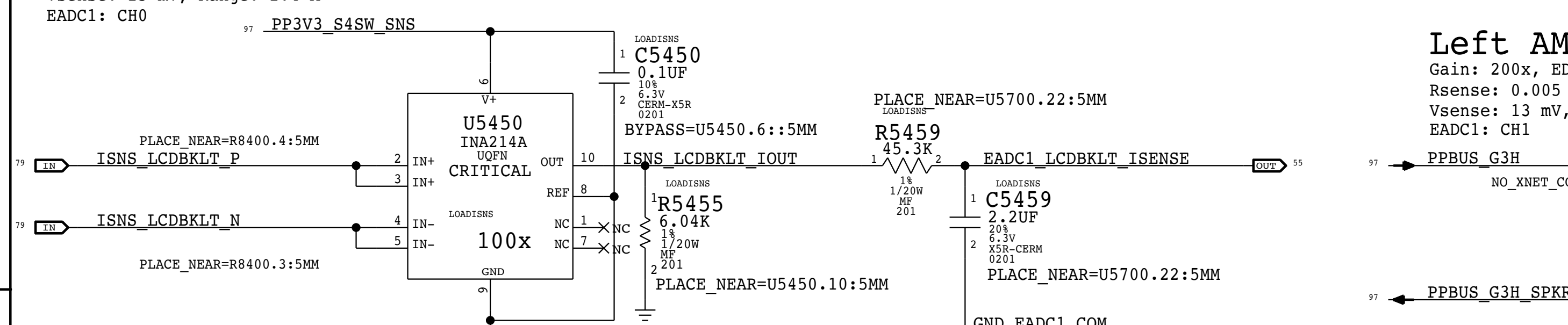
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.03 A
 Rsense: 0.003 (R5440) or Rsense SHORT
 Vsense: 12.09 mV, Range: 5 A
 MUX: A0



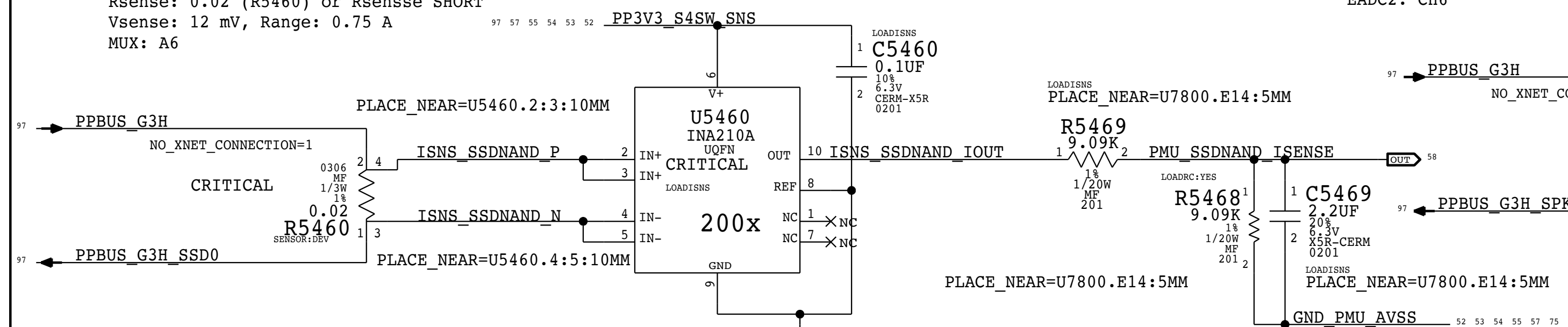
LCD Backlight Current Sense (IBLR)

Gain: 100x, EDP: 1 A
 Rsense: 0.025 (R8400)
 Vsense: 25 mV, Range: 2.4 A
 EADC1: CH0



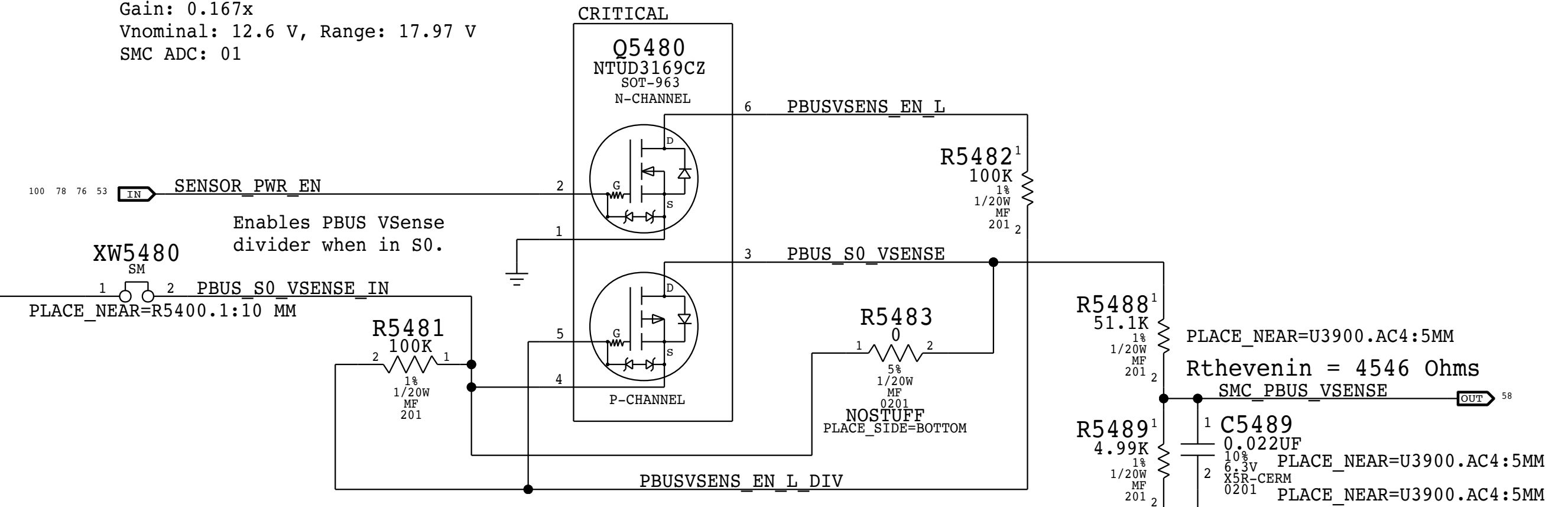
NAND Current Sense (IHNR)

Gain: 200x, EDP: 0.6 A
 Rsense: 0.02 (R5460) or Rsense SHORT
 Vsense: 12 mV, Range: 0.75 A
 MUX: A6



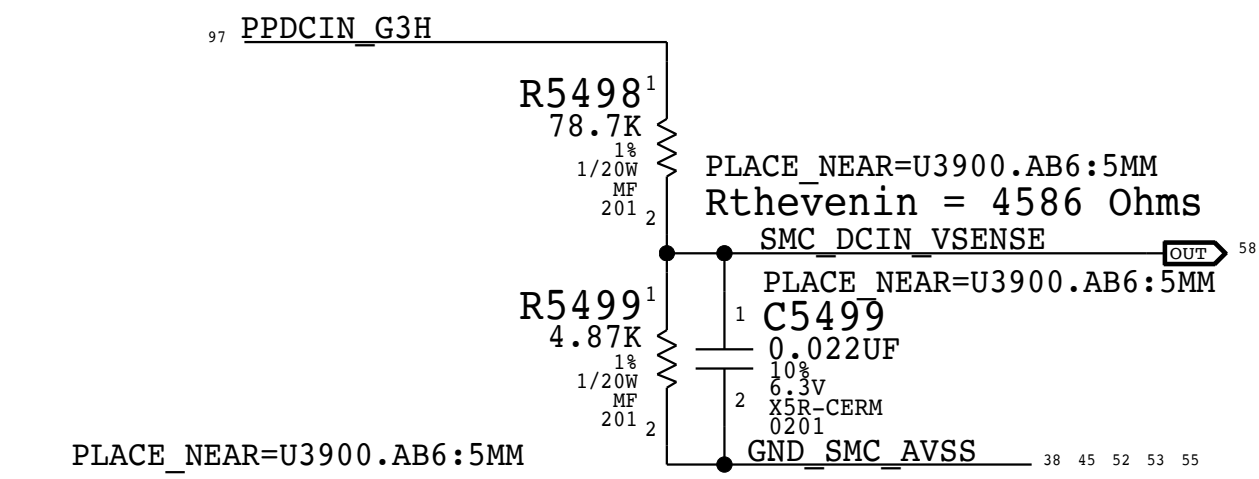
PBUS Voltage Sense & Enable (VPOR)

Gain: 0.167x
 Vnominal: 12.6 V, Range: 17.97 V
 SMC ADC: 01



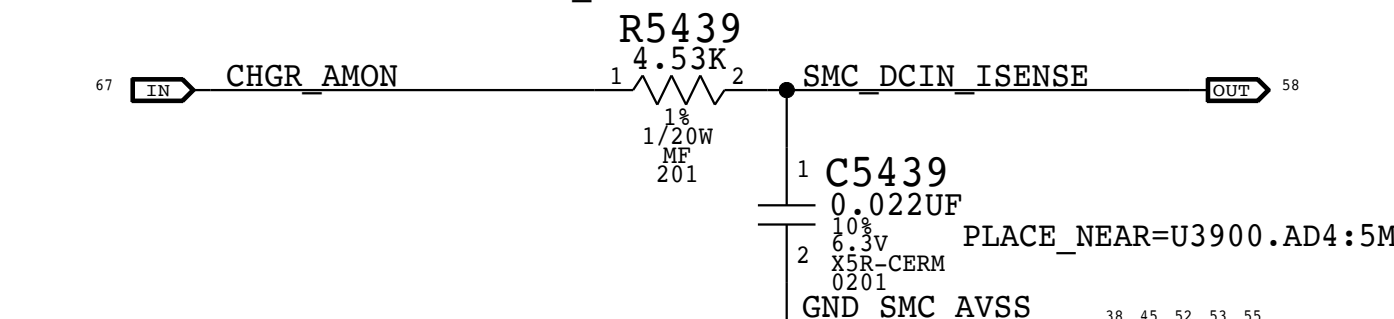
DC In Voltage Sense & Enable (VDOR)

Gain: 0.13x
 Vnominal: 16.5 V, Range: 22.96 V
 SMC ADC: 04



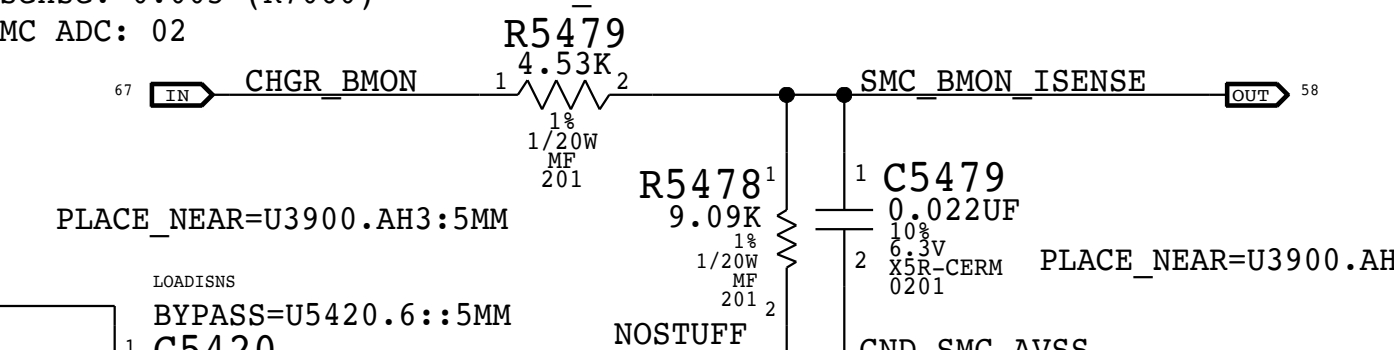
DC-IN (AMON) Current Sense (IDOR)

Charger Gain: 20x, EDP: 4.6 A
 Rsense: 0.010 (R7020)
 SMC ADC: 03



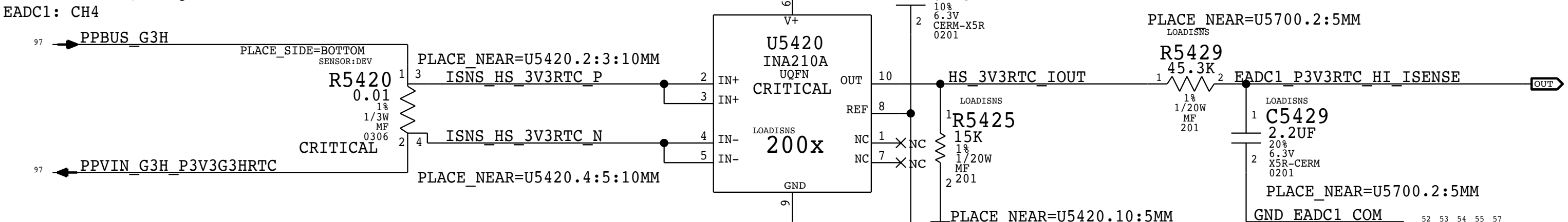
Charger (BMON) Current Sense (IPBR)

Charger Gain: 12x, EDP: 20.83 A
 Rsense: 0.005 (R7060)
 SMC ADC: 02



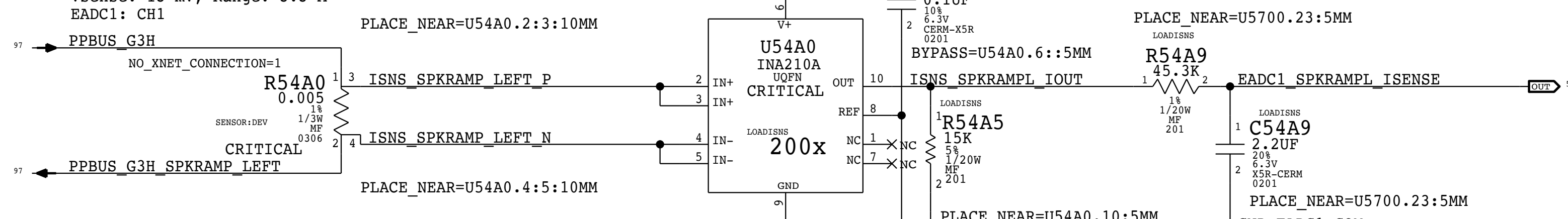
3.3V RTC High Side Current Sense (IR3R)

Gain: 200x, EDP: 1.8 A
 Rsense: 0.01 (R5420) or Rsense SHORT
 Vsense: 18 mV, Range: 1.65 A
 EADC1: CH4



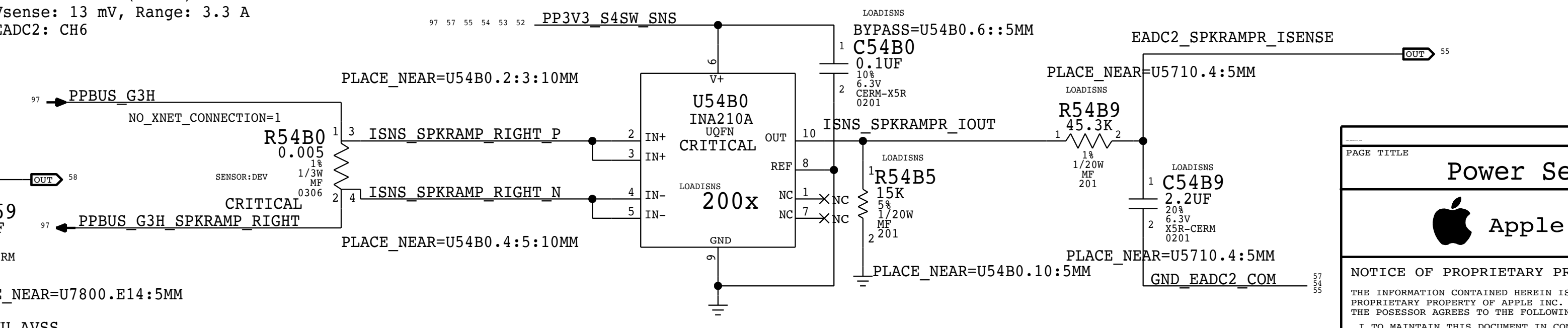
Left AMP Current Sense (IALR)

Gain: 200x, EDP: 2.6 A
 Rsense: 0.005 (R54A0) or Rsense SHORT
 Vsense: 13 mV, Range: 3.3 A
 EADC1: CH1



Right AMP Current Sense (IARR)

Gain: 200x, EDP: 2.6 A
 Rsense: 0.005 (R54B0) or Rsense SHORT
 Vsense: 13 mV, Range: 3.3 A
 EADC2: CH6



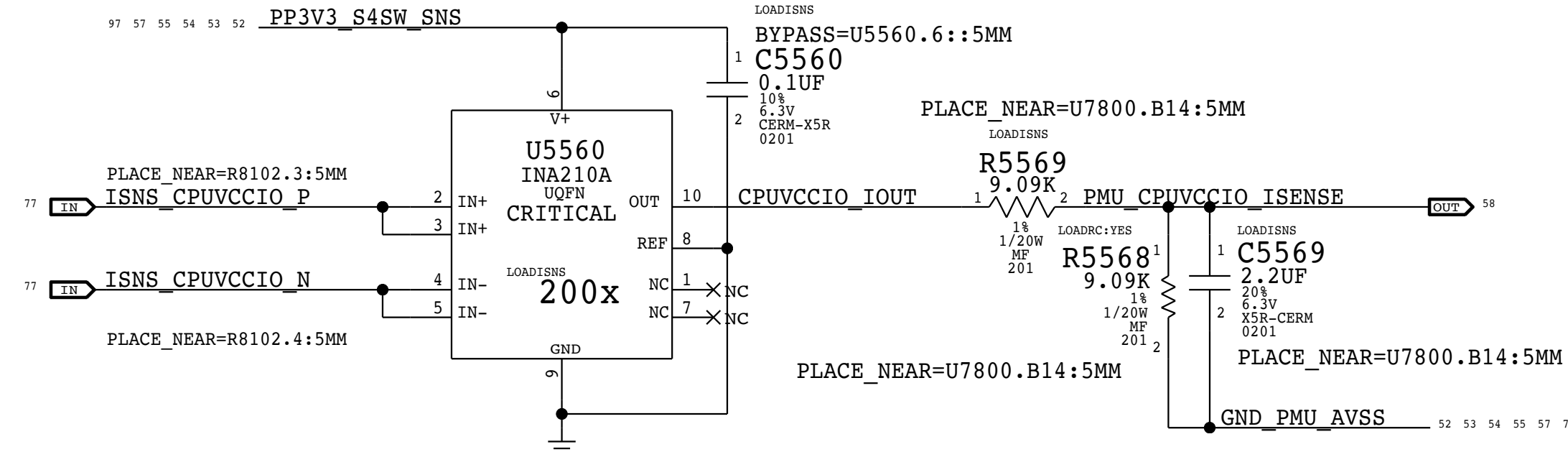
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117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5418,R5448		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5468,R5478		LOADRC:NO

PAGE TITLE		Power Sensors: High Side	
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BOM_COST_GROUP=SENSORS

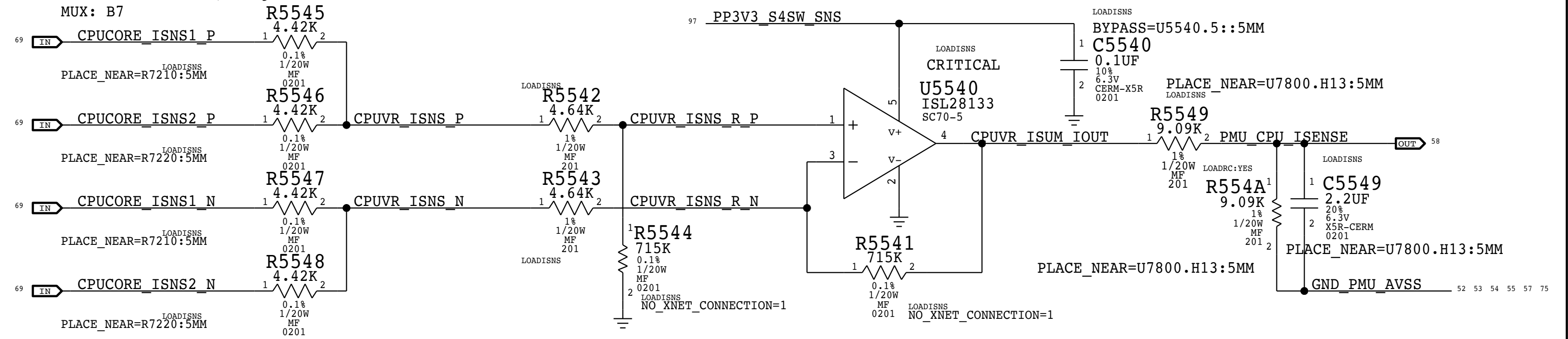
CPU VCCIO Current Sense (IC1C)

Gain: 200x, EDP: 3.6 A
 Rsense: 0.003 (R8102) or Rsense SHORT
 Vsense: 10.8 mV, Range: 5 A
 MUX: A3



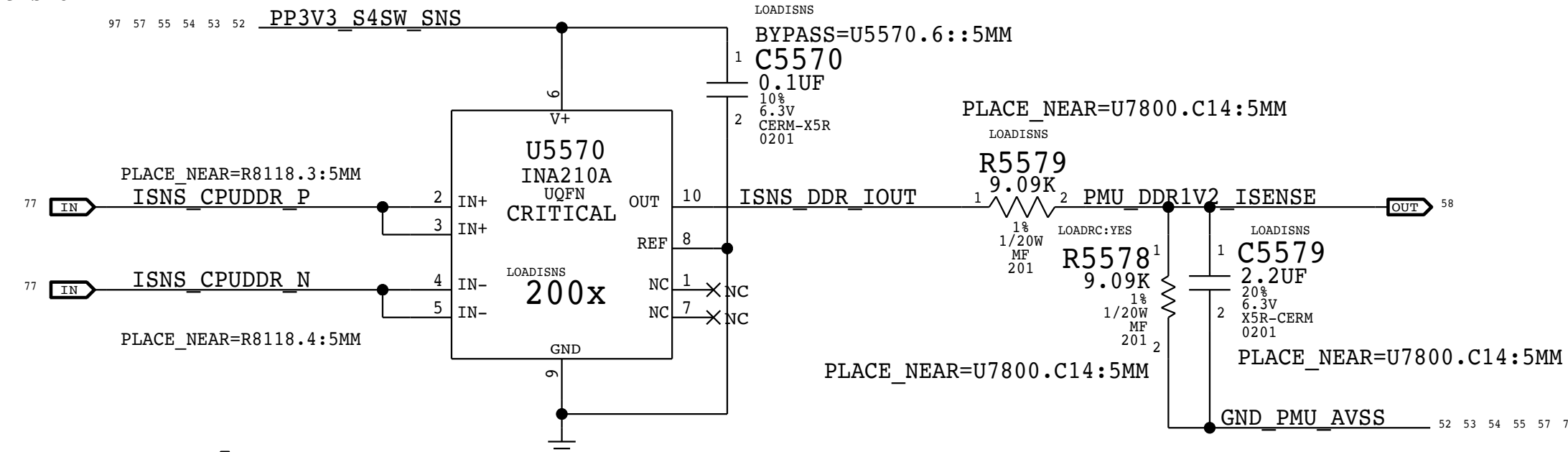
CPU Fixed Current Sense (ICAC)

Gain: 275.74x, EDP: 29 A
 Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
 Vsense: 10.875 mV, Range: 29.01 A
 MUX: B7



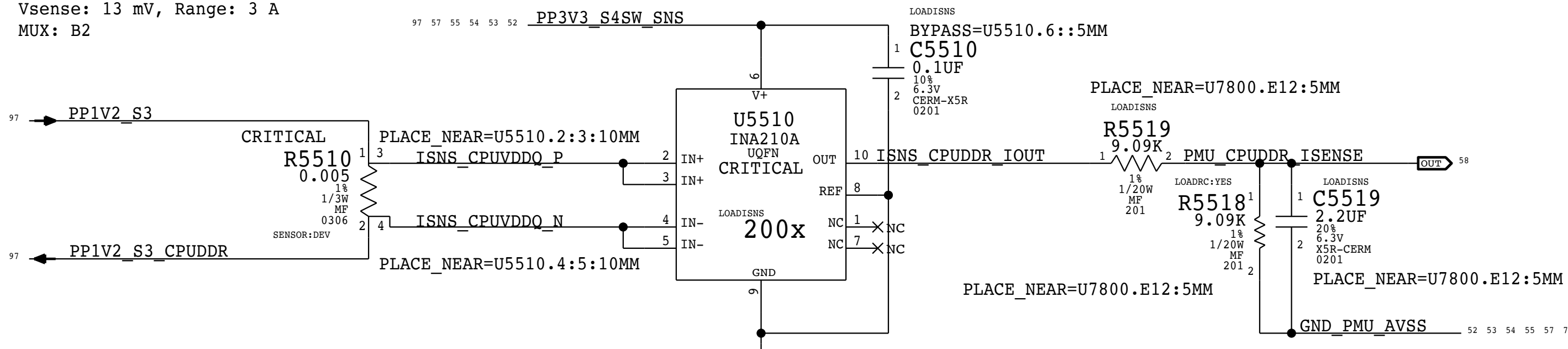
DDR 1.2V S3 (CPU & Memory) Current Sense (IMOC)

Gain: 200x, EDP: 6.9 A
 Rsense: 0.002 (R8118) or Rsense SHORT
 Vsense: 13.8 mV, Range: 7.5 A
 MUX: A4



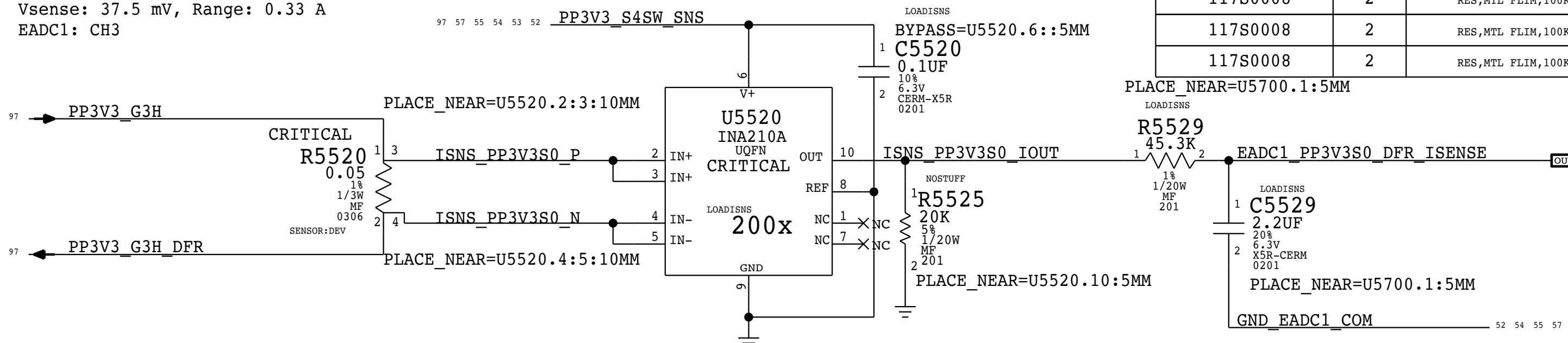
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2.6 A
 Rsense: 0.005 (R5510) or Rsense SHORT
 Vsense: 13 mV, Range: 3 A
 MUX: B2



DFR Current Sense (IF3C)

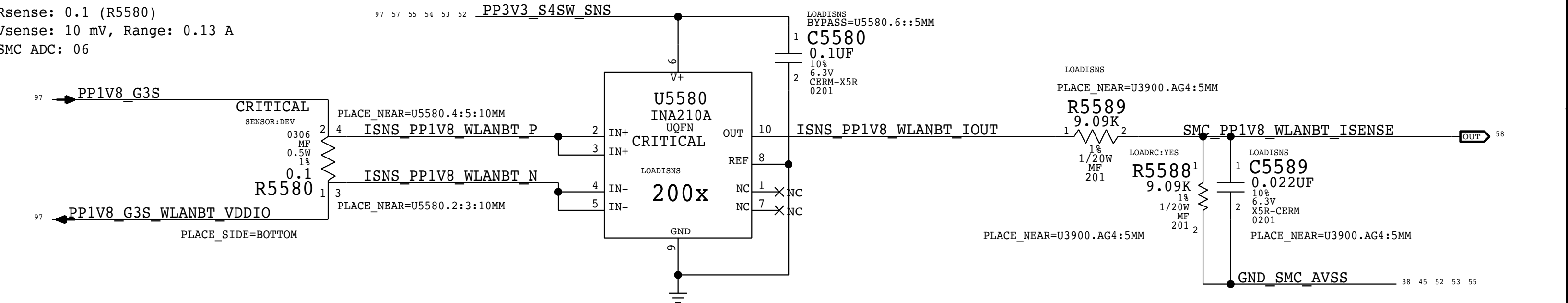
Gain: 200x, EDP: 0.75 A
 Rsense: 0.05 (R5520) or Rsense SHORT
 Vsense: 37.5 mV, Range: 0.33 A
 EADC1: CH3



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5568,R5518		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R554A,R5578		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5539,R5588		LOADRC:NO

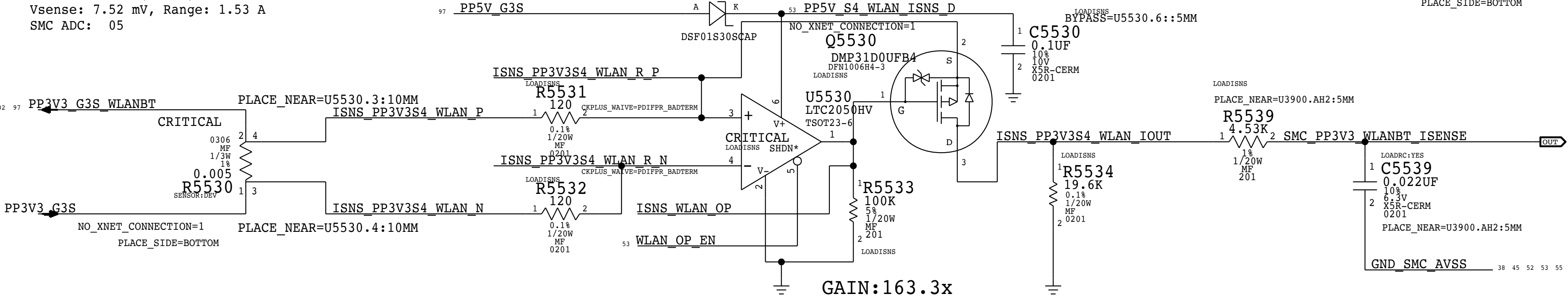
WLANBT 1.8V Current Sense (IW2C)

Gain: 200x, EDP: 0.1 A
 Rsense: 0.1 (R5580)
 Vsense: 10 mV, Range: 0.13 A
 SMC ADC: 06



WLANBT 3.3V Current Sense (IW3C)

Gain: 163.3x, EDP: 1.504 A
 Rsense: 0.005 (R5530) or Rsense SHORT
 Vsense: 7.52 mV, Range: 1.53 A
 SMC ADC: 05

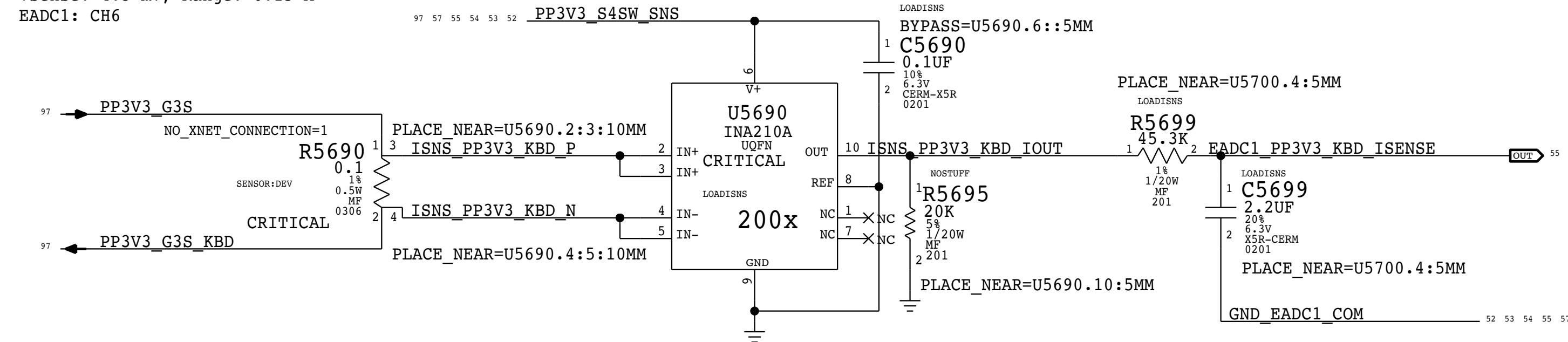


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BOM_COST_GROUP=SENSORS

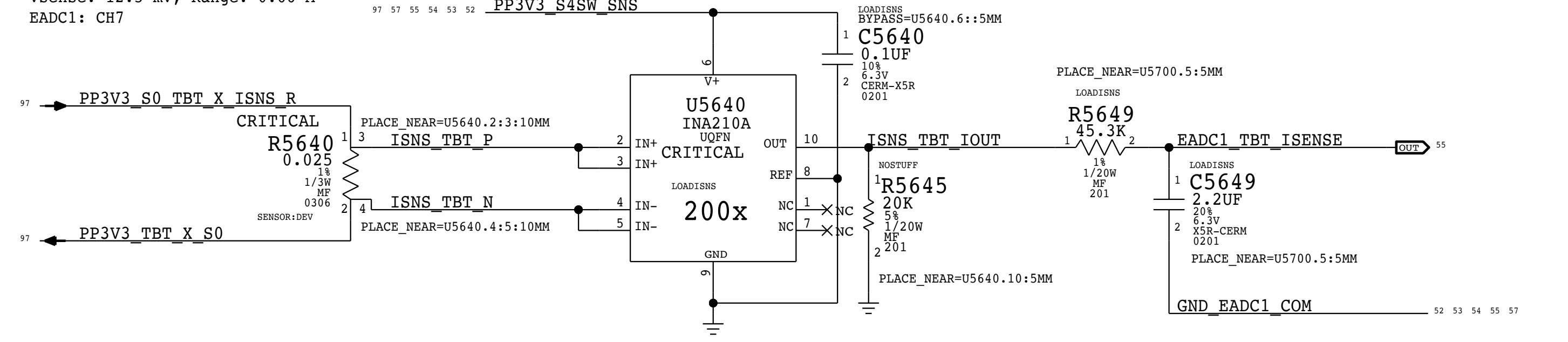
Keyboard 3V Current Sense (IK3C)

Gain: 200x, EDP: 0.043 A
 Rsense: 0.1 (R5690) or Rsense SHORT
 Vsense: 4.3 mV, Range: 0.15 A
 EADC1: CH6



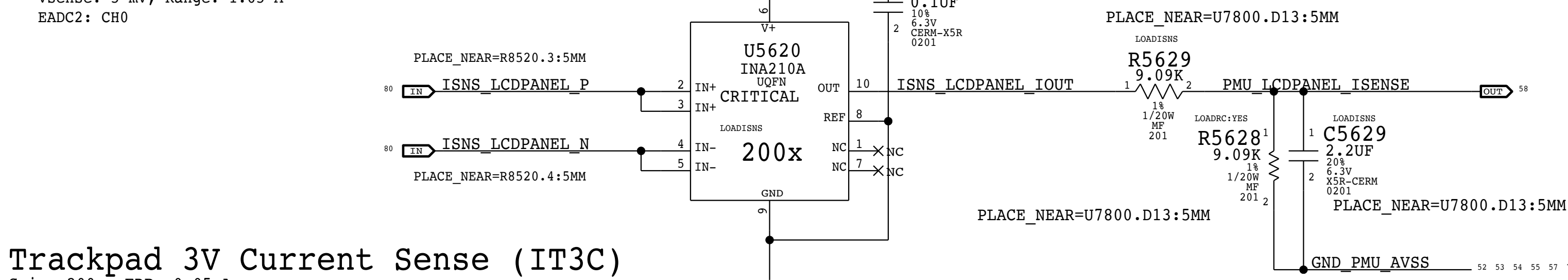
Thunderbolt TBT Current Left (IULC)

Gain: 200x, EDP: 0.8 A
 Rsense: 0.025 (R5640) or Rsense SHORT
 Vsense: 12.5 mV, Range: 0.66 A
 EADC1: CH7



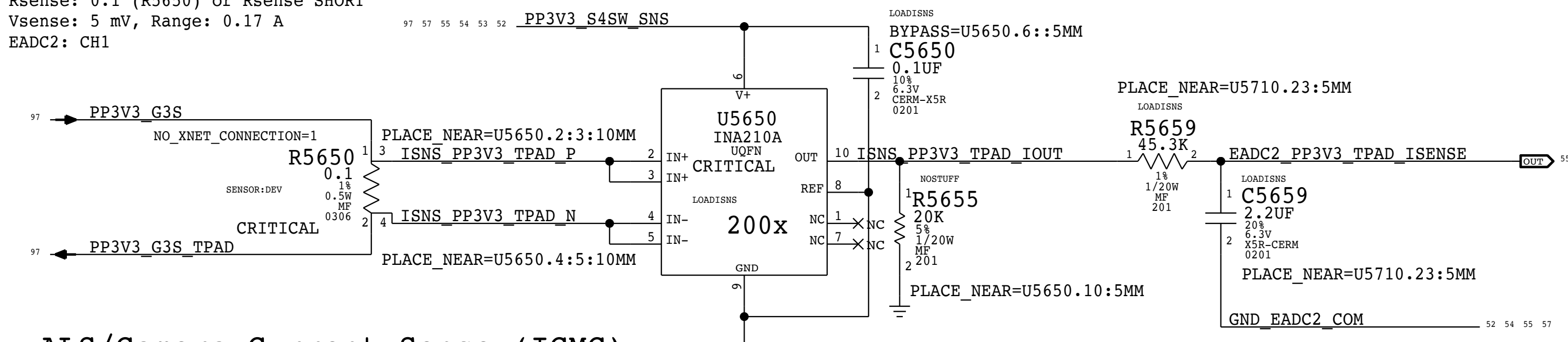
LCD Panel 3V Current Sense (ILDC)

Gain: 200x, EDP: 1 A
 RSENSE: 0.01 (R8520) or Rsense SHORT
 Vsense: 5 mV, Range: 1.65 A
 EADC2: CH0



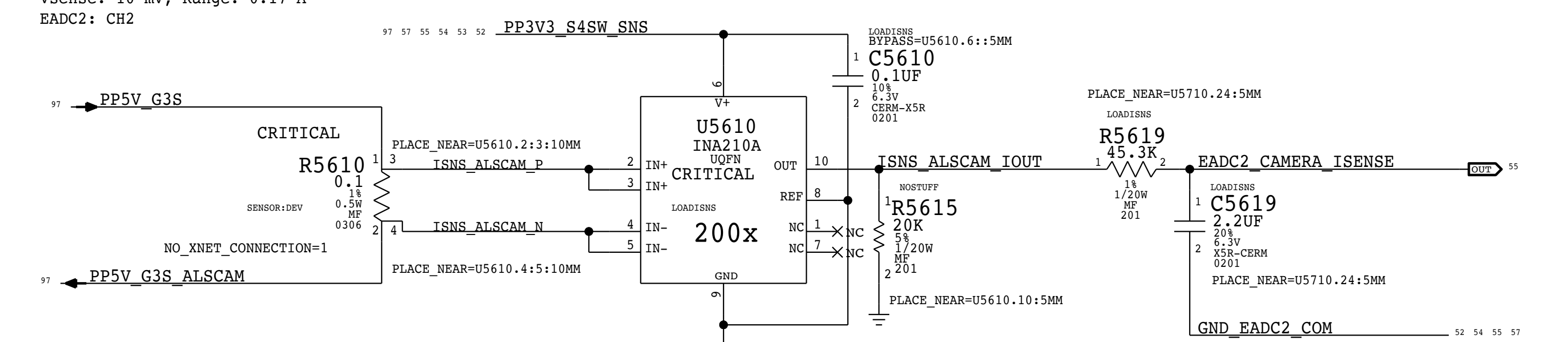
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.05 A
 Rsense: 0.1 (R5650) or Rsense SHORT
 Vsense: 5 mV, Range: 0.17 A
 EADC2: CH1



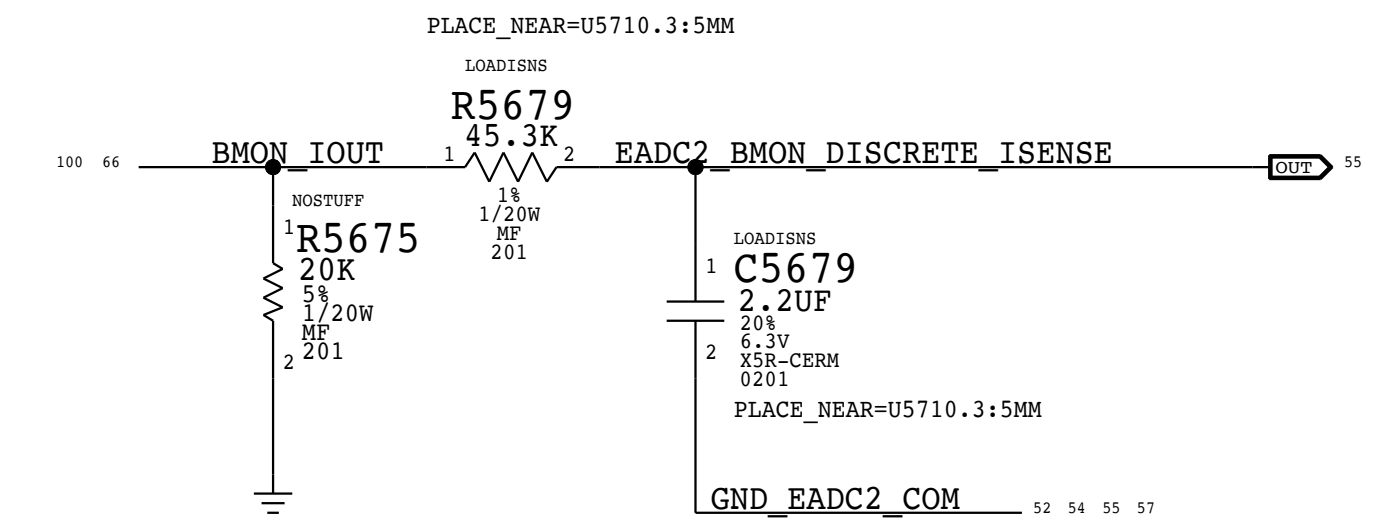
ALS/Camera Current Sense (ICMC)

Gain: 200x, EDP: 0.1 A
 Rsense: 0.1 (R5610) or Rsense SHORT
 Vsense: 10 mV, Range: 0.17 A
 EADC2: CH2



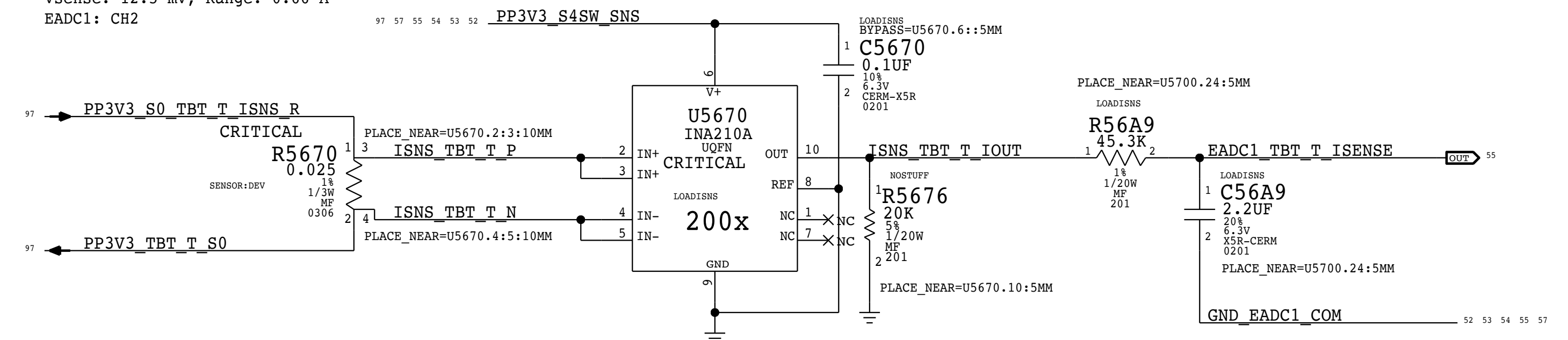
Battery Discrete Current Sense (IBOL)

Gain: 2940x, EDP: 8 A
 Rsense: 0.003 (R501//R502)
 Vsense: 24 mV, Range: 0.28 A
 EADC2: CH5



Thunderbolt TBT Current Right (IURC)

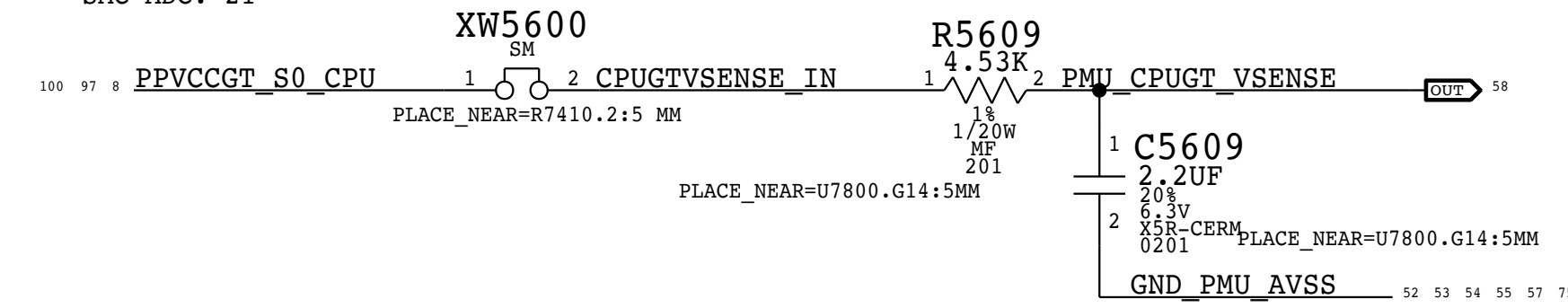
Gain: 200x, EDP: 0.8 A
 Rsense: 0.025 (R5670) or Rsense SHORT
 Vsense: 12.5 mV, Range: 0.66 A
 EADC1: CH2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MFL,FLM,100K,1/16W,0201,SMD,LF	R5698,R5628		LOADRC:NO

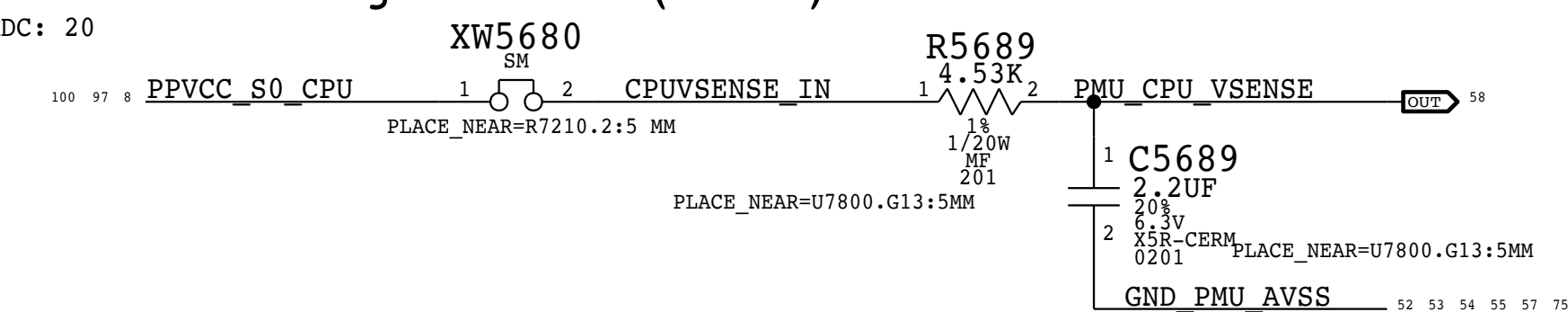
CPU GT Voltage Sense (VCGC)

SMC ADC: 21



CPU Core Voltage Sense (VCAC)

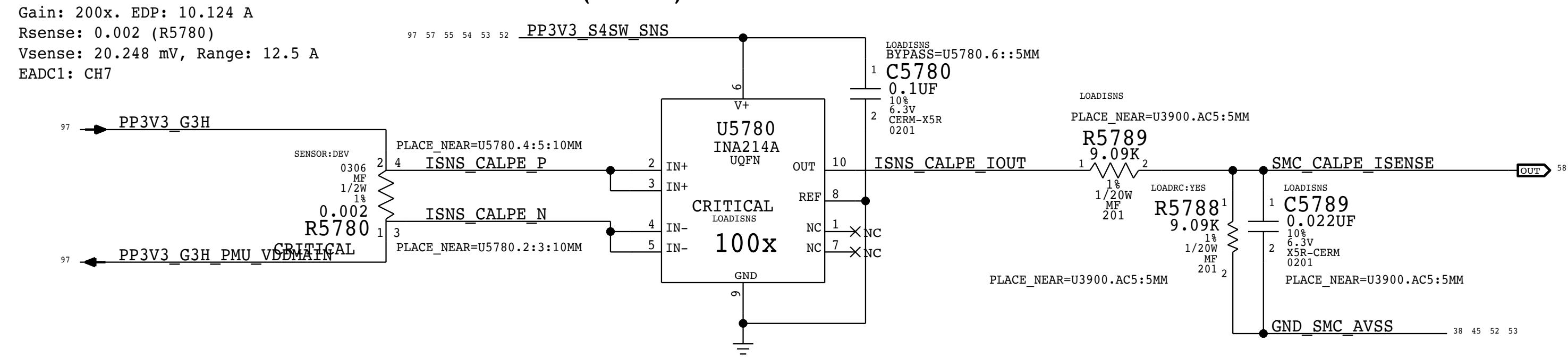
SMC ADC: 20



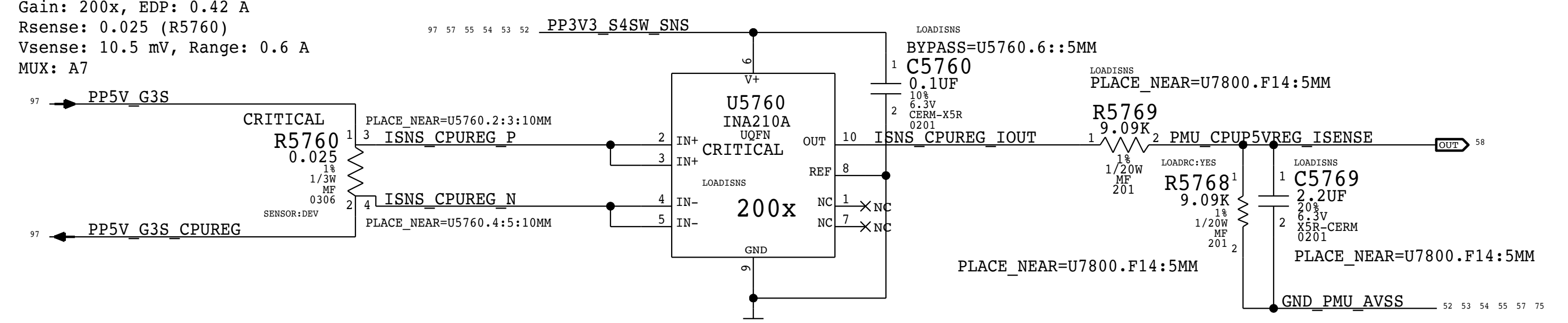
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BOM_COST_GROUP=SENSORS

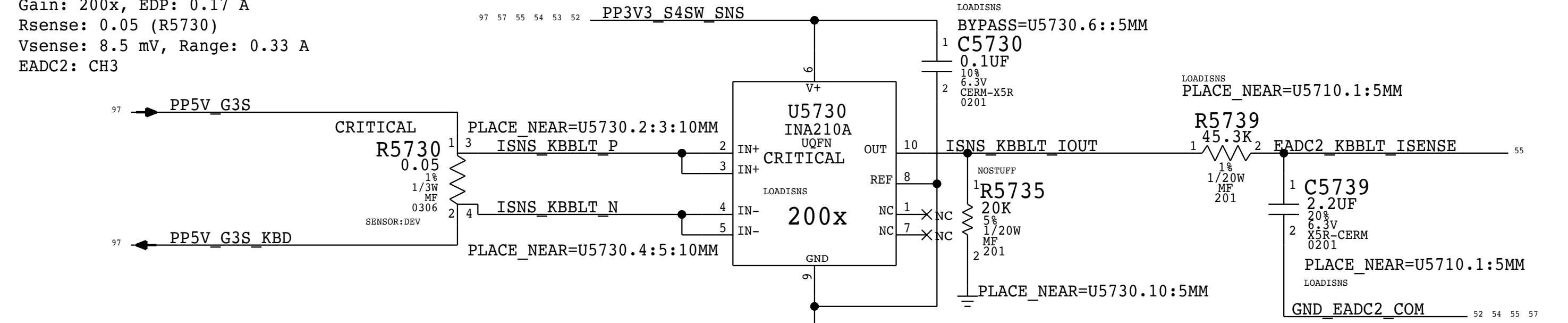
CALPE 3.3V INPUT Current Left (IP3C)



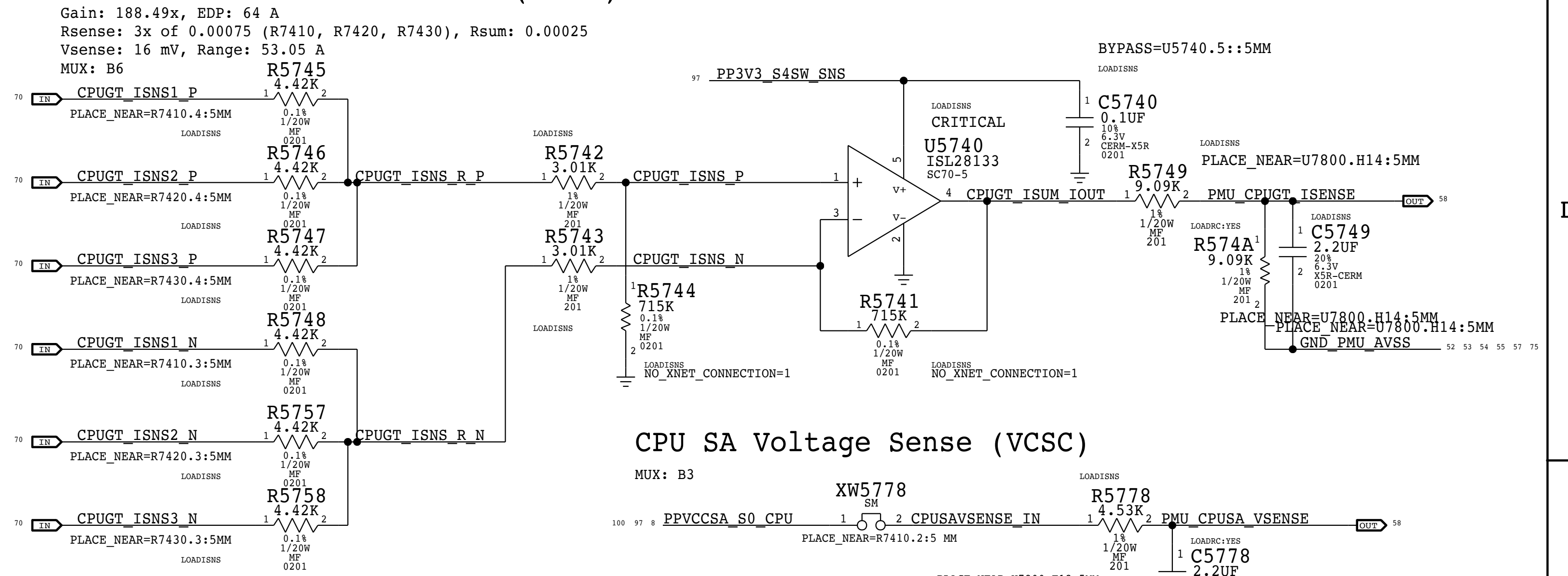
CPU REG.5V Current Sense (IC5C)



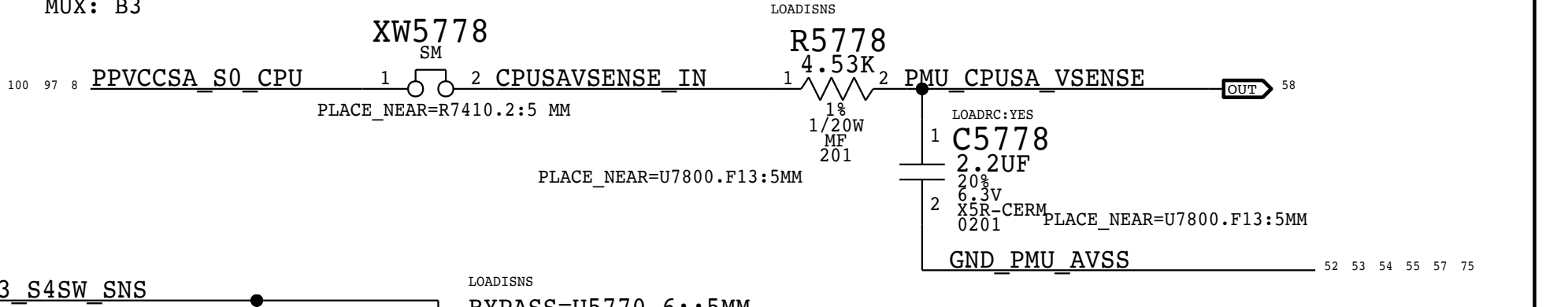
KB backlite Current Sense (IKBC)



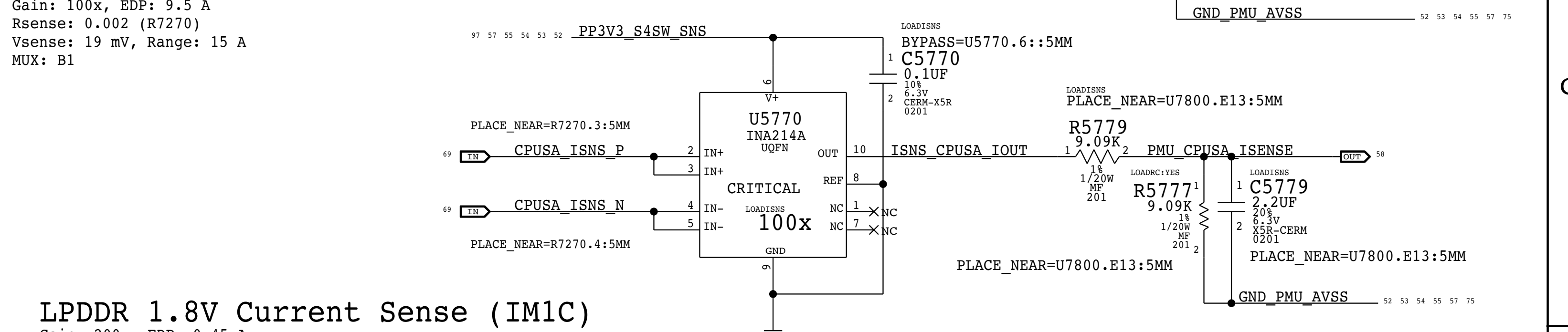
CPU GT+GTX Current Sense (ICGC)



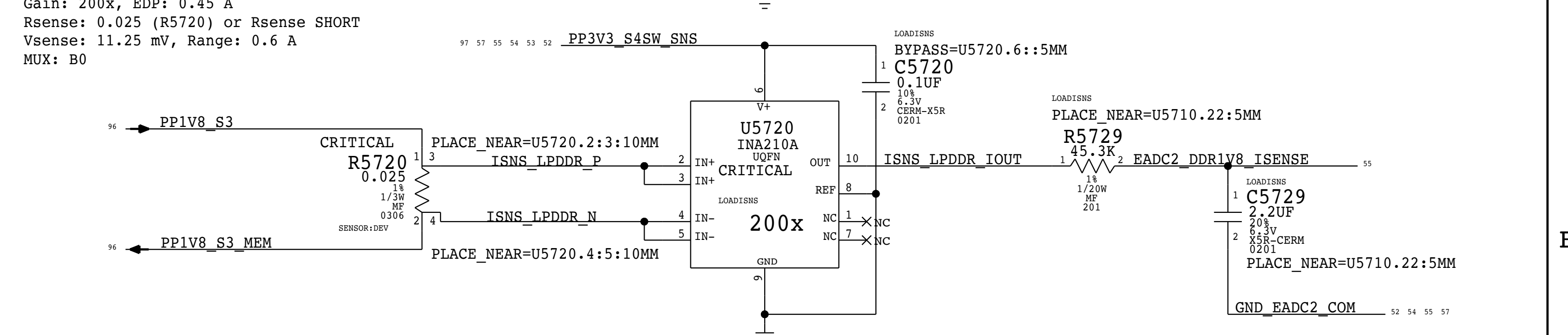
CPU SA Voltage Sense (VCSC)



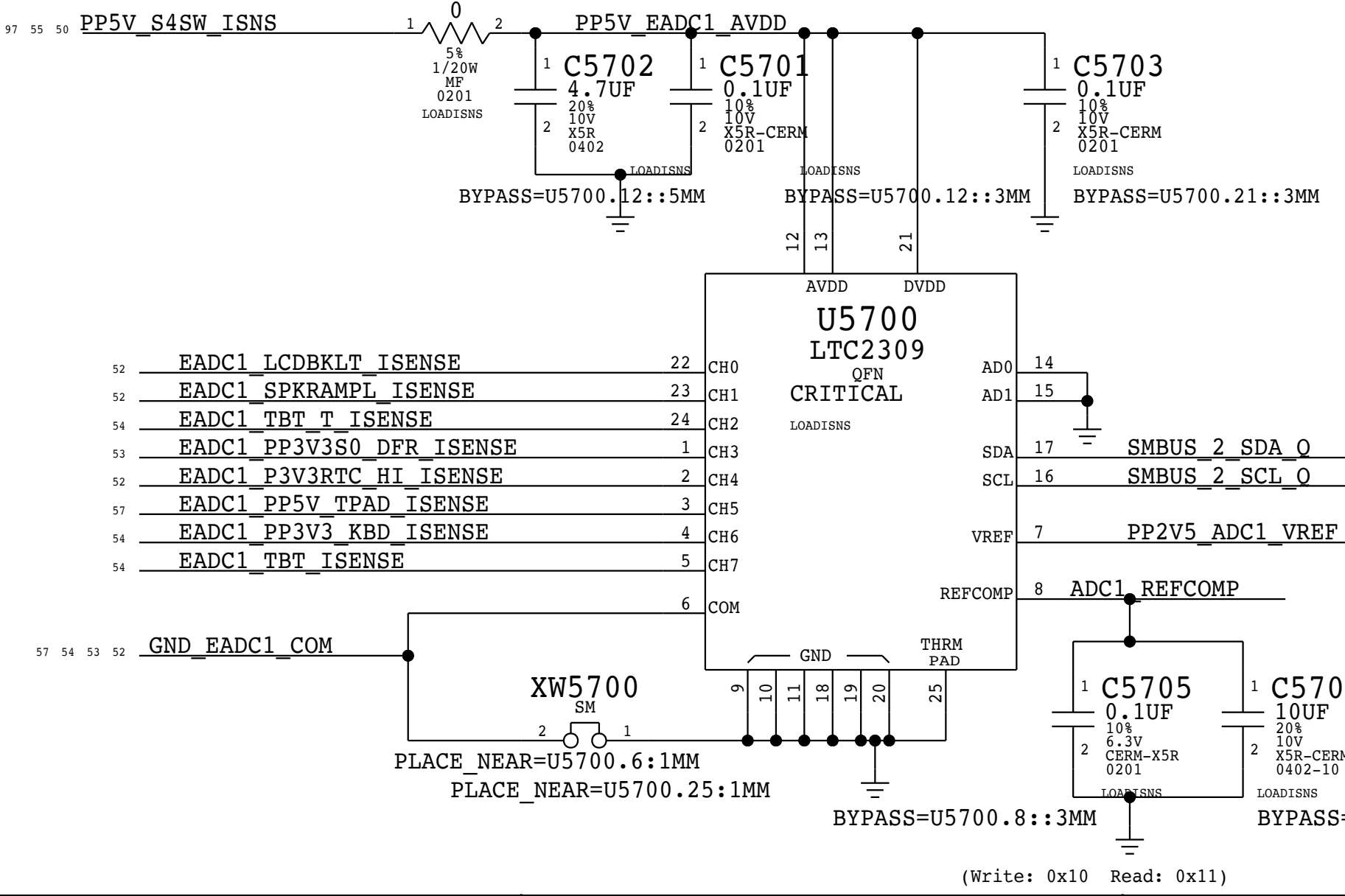
CPU SA Current Sense (ICSC)



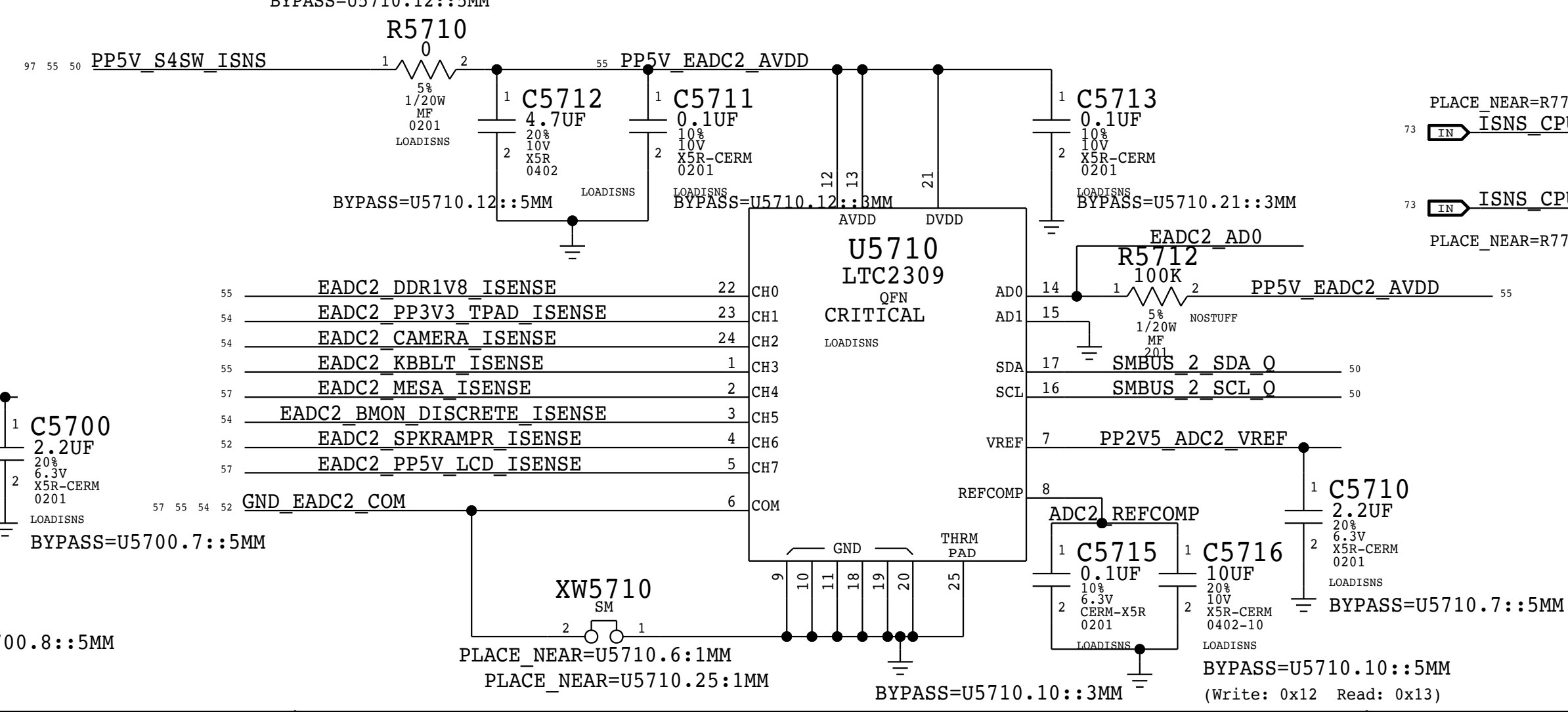
LPDDR 1.8V Current Sense (IM1C)



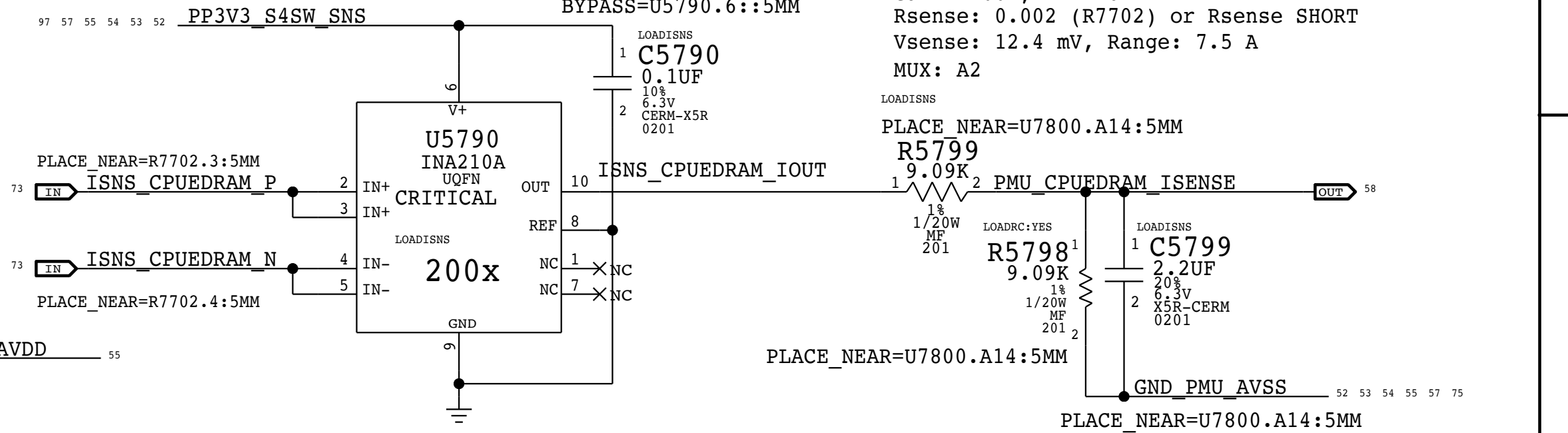
EADC1



EADC2



CPU EDRAM Current Sense (ICEC)



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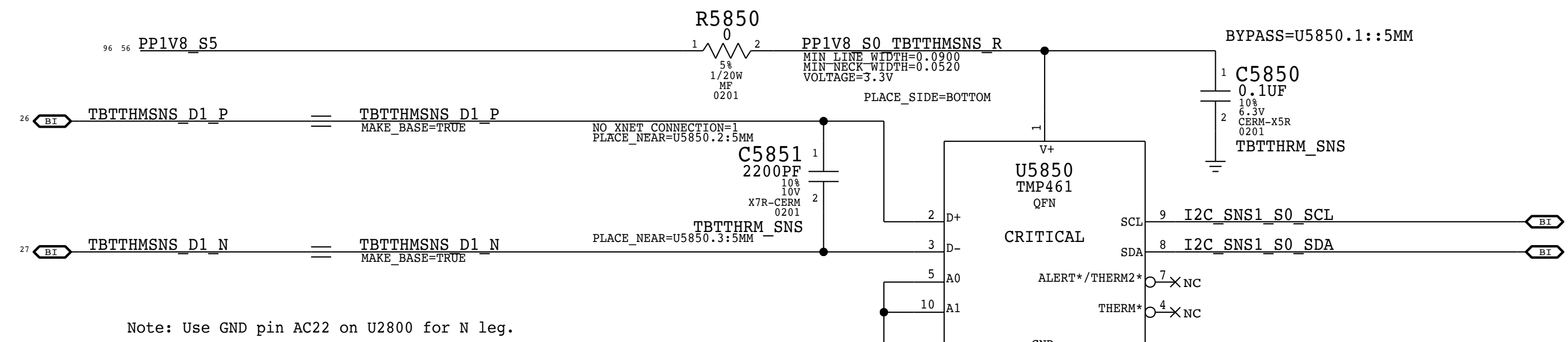
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117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5768,R5777		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R574A,R5788		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5798		LOADRC:NO

**Thermal Sensor A:
Thunderbolt Die, Airflow Left**

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



U5850 I2C Address: TMP461 is 0x90/0x91.

Thermal Sensor: Airflow Left (TaLC)

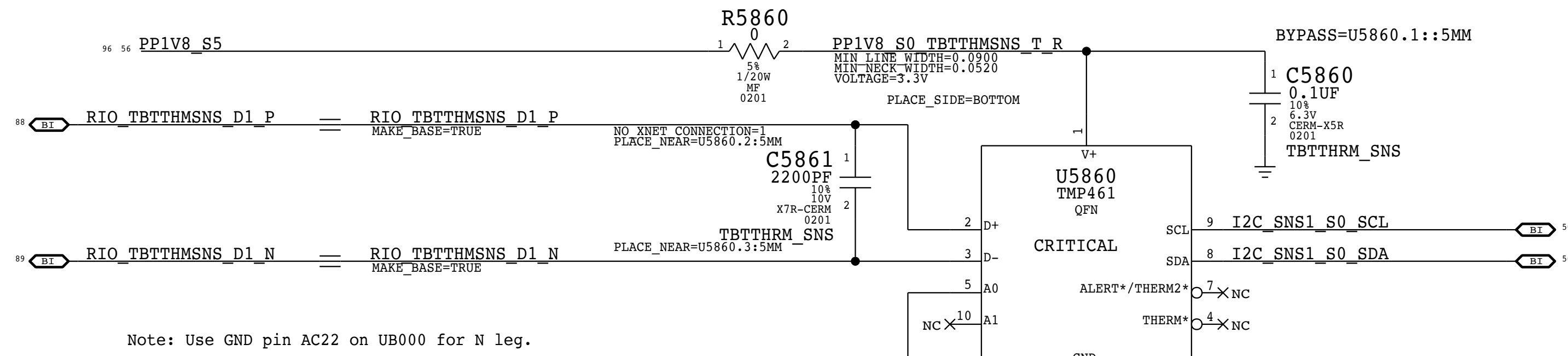
Placement Note:
Place U5860 on the BOTTOM side, at the lower corner near left fan.

**Thermal Sensor C:
Thunderbolt Die, Air Flow Right**

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: TBT Die (TRD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



U5860 I2C Address: TMP461 is 0x96/0x97.

Thermal Sensor: Airflow Right (TaRC)

Placement Note:
Place U5860 on the BOTTOM side, at the lower corner near right fan.

**Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right**

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.

Thermal Diode: CPU Proximity (TCOP)

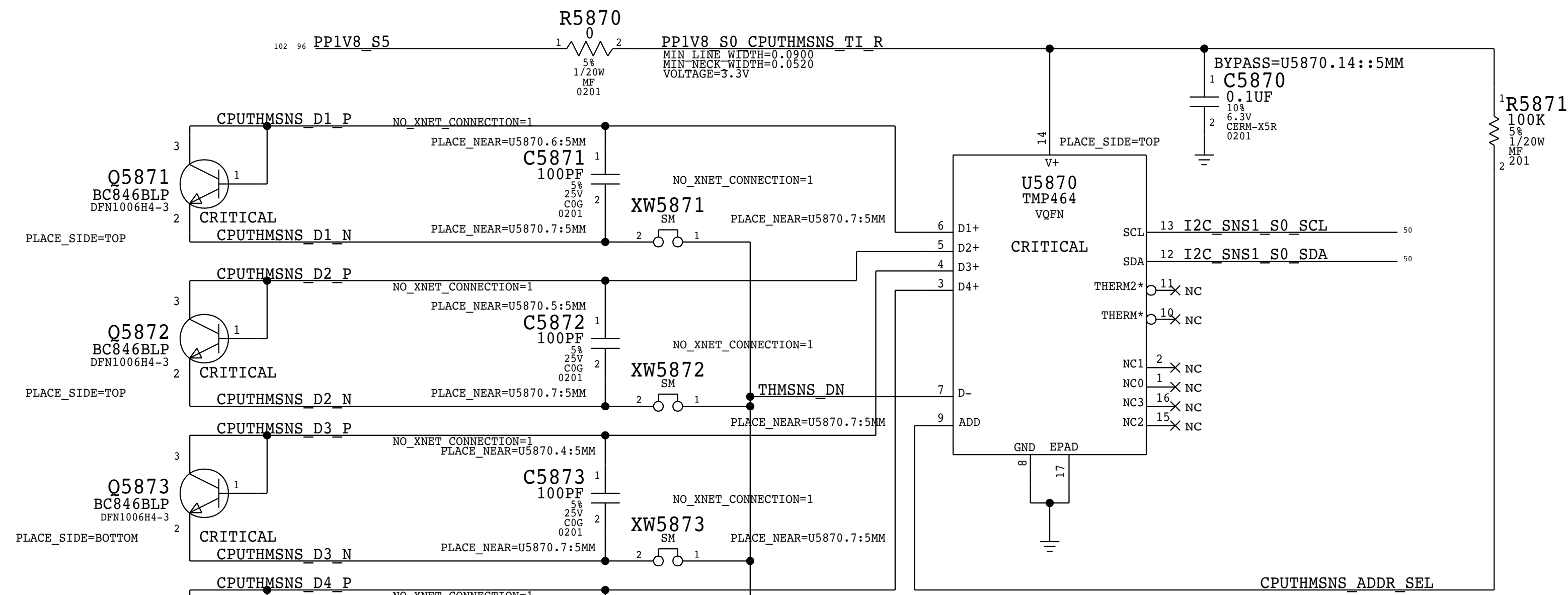
Placement Note:
Place Q5872 under the CPU, on the TOP side.

Thermal Diode: Memory Proximity (TMOP)

Placement Note:
Place Q5873 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

HARPOON PROXIMITY (TWOP)

Placement note:
PLACE Q5874 ON BOTTOM NEAR HARPOON



U5870 I2C Address: TMP464 is 0x92/0x93.

Thermal Sensor: Fin Stack Right (Th1H)

Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

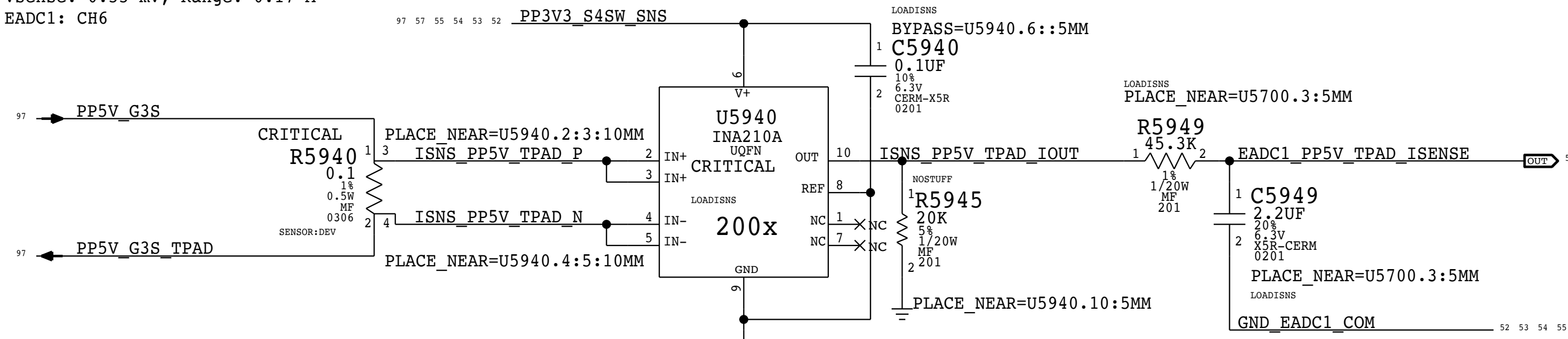
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,WTL,FLIM,0ohm,1/20W,0201,SMD,LF	C5874		AP_TEMP:NO

BOM_COST_GROUP=SENSORS

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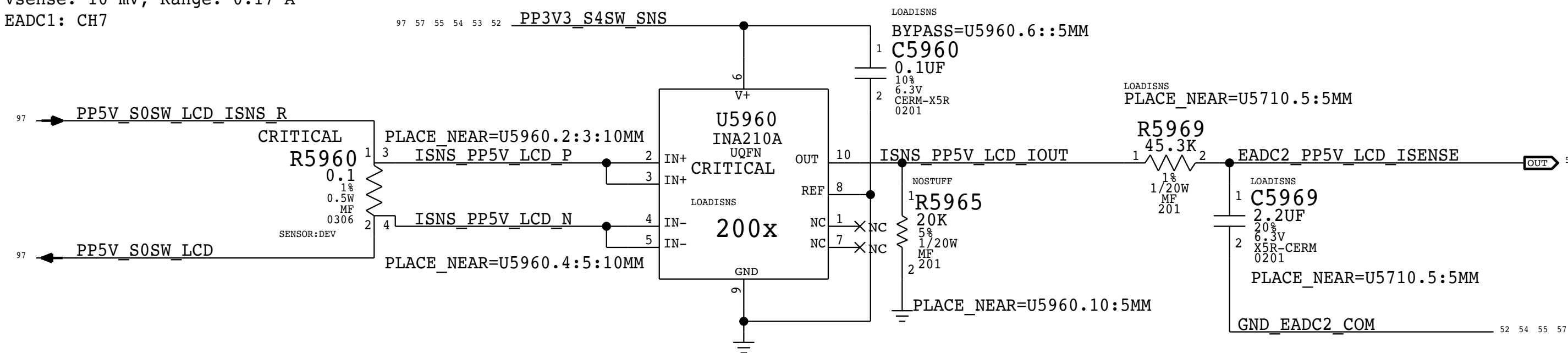
Trackpad 5V Current Sense (IT5C)

Gain: 200x, EDP: 0.0055 A
 Rsense: 0.1 (R5940) or Rsense SHORT
 Vsense: 0.55 mV, Range: 0.17 A
 EADC1: CH6



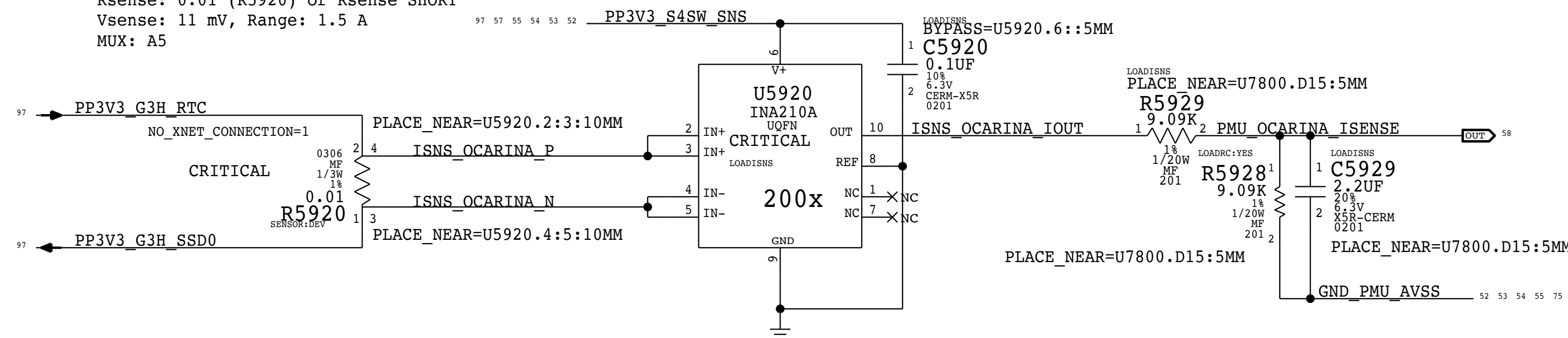
LCD Panel 5V Current Sense (IL5C)

Gain: 200x, EDP: 0.1 A
 Rsense: 0.1 (R5960) or Rsense SHORT
 Vsense: 10 mV, Range: 0.17 A
 EADC1: CH7



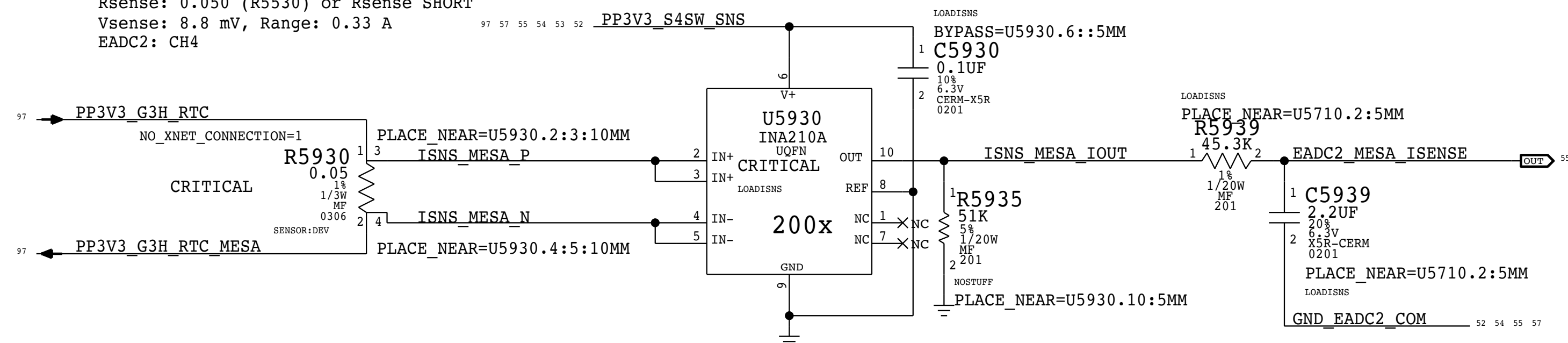
Ocarina Current Sense (IHCC)

Gain: 200x, EDP: 1.1 A
 Rsense: 0.01 (R5920) or Rsense SHORT
 Vsense: 11 mV, Range: 1.5 A
 MUX: A5



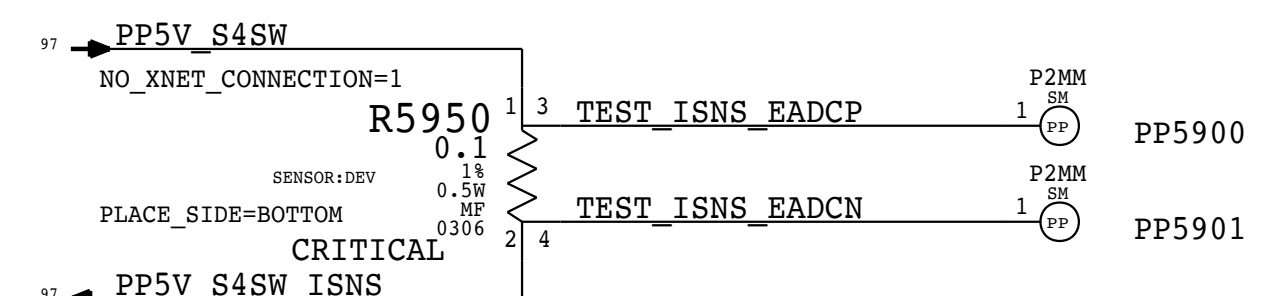
MESA Current Sense (IIDC)

Gain: 200x, EDP: 0.176 A
 Rsense: 0.050 (R5930) or Rsense SHORT
 Vsense: 8.8 mV, Range: 0.33 A
 EADC2: CH4



EADC Current Sense

EDP: 6m A
 Rsense: 0.1 (R5950) or Rsense SHORT
 Vsense: 0.6 mV

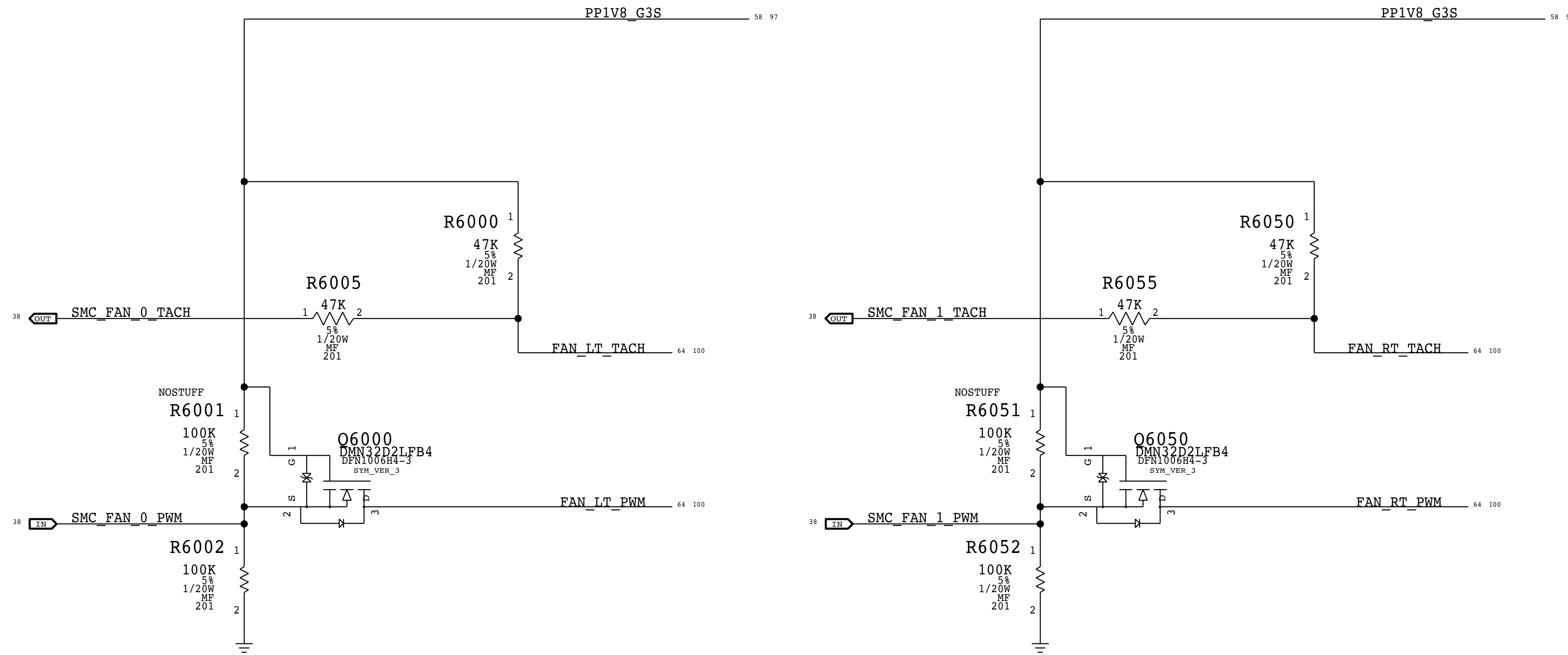


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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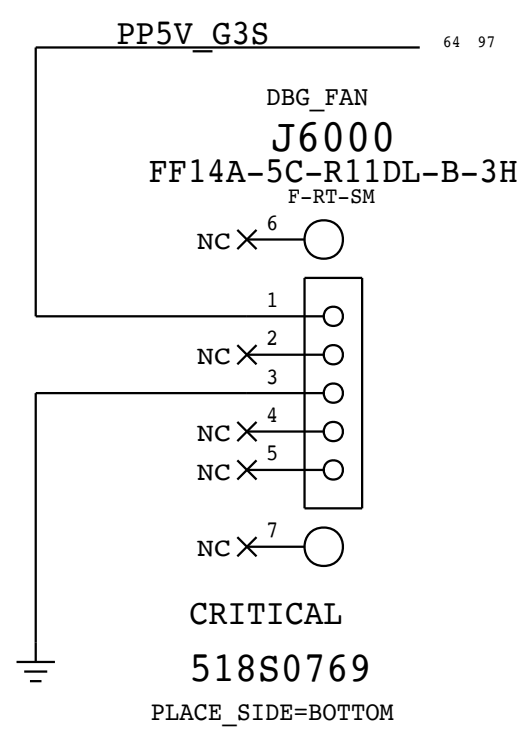
PAGE TITLE Power Sensors:Extended 3		
	DRAWING NUMBER 051-02166	SIZE D
	REVISION 4.0.0	
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BRANCH evt-mars-0	PAGE 59 OF 150	SHEET 57 OF 108

BOM_COST_GROUP=SENSORS

FAN CONTROL



FOR DEBUG FAN POWER



SMC ADC Assignments

52	IN	SMC_CPU_HS_ISENSE	==	SMC_CPU_HS_ISENSE	OUT	38
52	IN	SMC_PBUS_VSENSE	==	SMC_PBUS_VSENSE	OUT	38
52	IN	SMC_BMON_ISENSE	==	SMC_BMON_ISENSE	OUT	38
52	IN	SMC_DCIN_ISENSE	==	SMC_DCIN_ISENSE	OUT	38
52	IN	SMC_DCIN_VSENSE	==	SMC_DCIN_VSENSE	OUT	38
53	IN	SMC_PP3V3_WLANBT_ISENSE	==	SMC_PP3V3_WLANBT_ISENSE	OUT	38
53	IN	SMC_PP1V8_WLANBT_ISENSE	==	SMC_PP1V8_WLANBT_ISENSE	OUT	38
55	IN	SMC_CALPE_ISENSE	==	SMC_CALPE_ISENSE	OUT	38

KBL-U NB Assignments
 CPUGT ISNS | ADC5
 IACORE ISNS | ADC6

Desktop Assignments
 GPU_AUX | ADC0
 GPU_CORE | ADC1
 12V_VSNS | ADC2
 12V_ISNS | ADC3
 Same | ADC4-7

PMU ADC Assignments

52	IN	PMU_OTHER3V3_HI_ISENSE	==	PMU_OTHER3V3_HI_ISENSE	OUT	76
52	IN	PMU_OTHER5V_HI_ISENSE	==	PMU_OTHER5V_HI_ISENSE	OUT	76
55	IN	PMU_CPUEDRAM_ISENSE	==	PMU_CPUEDRAM_ISENSE	OUT	76
53	IN	PMU_CPUVCCIO_ISENSE	==	PMU_CPUVCCIO_ISENSE	OUT	76
53	IN	PMU_DDR1V2_ISENSE	==	PMU_DDR1V2_ISENSE	OUT	76
57	IN	PMU_OCARINA_ISENSE	==	PMU_OCARINA_ISENSE	OUT	76
57	IN	PMU_SSDNAND_ISENSE	==	PMU_SSDNAND_ISENSE	OUT	76
55	IN	PMU_CPUP5VREG_ISENSE	==	PMU_CPUP5VREG_ISENSE	OUT	76
		NC_PMU_AMUX_AY	==	NC_PMU_AMUX_AY	OUT	76
54	IN	PMU_LCDPANEL_ISENSE	==	PMU_LCDPANEL_ISENSE	OUT	76
55	IN	PMU_CPUSA_ISENSE	==	PMU_CPUSA_ISENSE	OUT	76
53	IN	PMU_CPUDDR_ISENSE	==	PMU_CPUDDR_ISENSE	OUT	76
53	IN	PMU_CPUSA_VSENSE	==	PMU_CPUSA_VSENSE	OUT	76
54	IN	PMU_CPU_VSENSE	==	PMU_CPU_VSENSE	OUT	76
54	IN	PMU_CPUGT_VSENSE	==	PMU_CPUGT_VSENSE	OUT	76
55	IN	PMU_CPUGT_ISENSE	==	PMU_CPUGT_ISENSE	OUT	76
53	IN	PMU_CPU_ISENSE	==	PMU_CPU_ISENSE	OUT	76
		NC_PMU_AMUX_BY	==	NC_PMU_AMUX_BY	OUT	76

PAGE TITLE		
Fans/SMC/AMUX Support		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	60 OF 150
	SHEET	58 OF 108

BOM_COST_GROUP=FAN

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DESIGN: X502/DEV MLB U	
LAST CHANGE: Wed Feb 18 17:12:24 2015	
PAGE TITLE	
Audio Placeholder	
 Apple Inc.	DRAWING NUMBER 051-02166
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	BRANCH evt-mars-0
	PAGE 62 OF 150
	SHEET 59 OF 108

BOM_COST_GROUP=AUDIO

8

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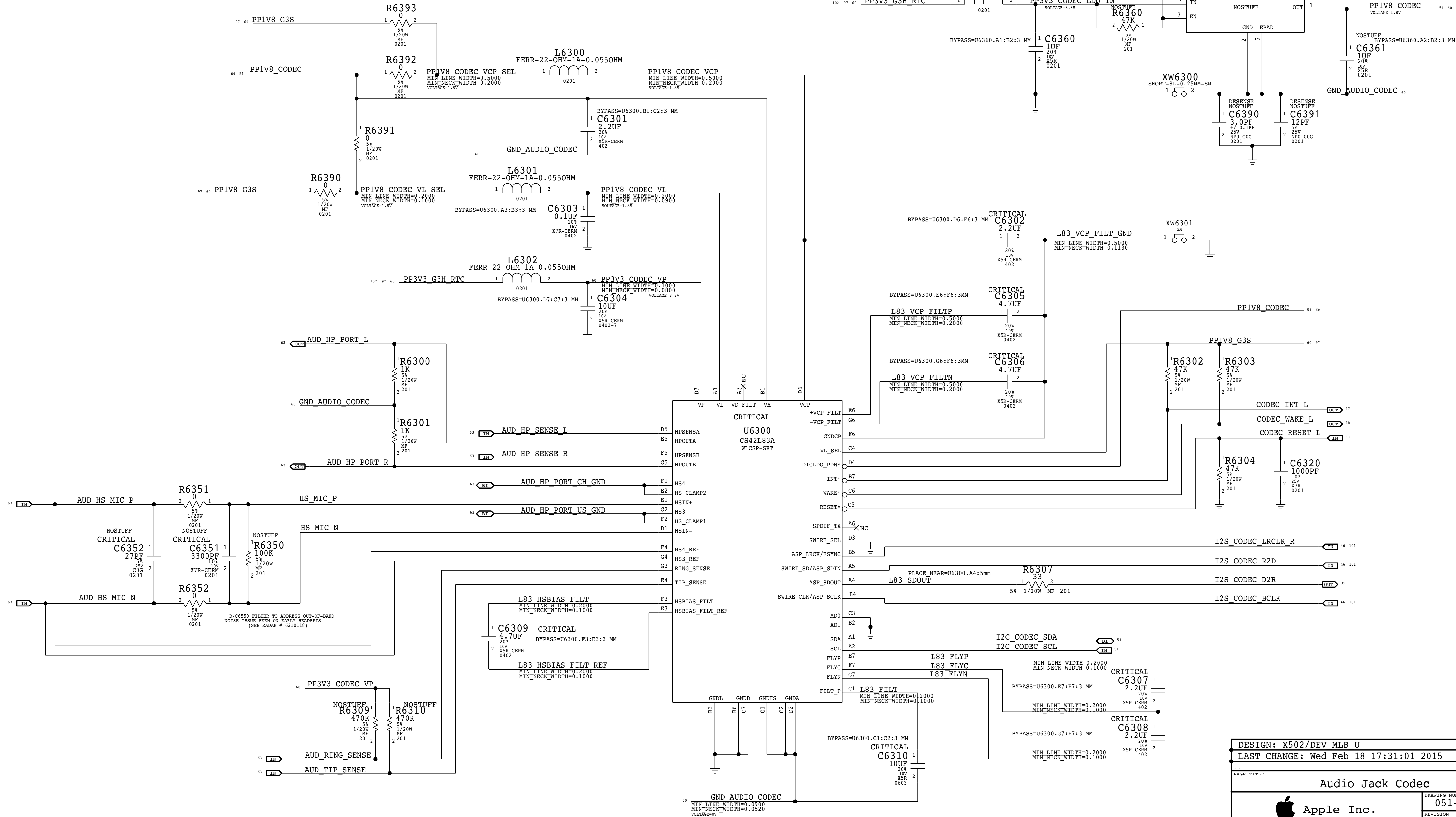
4

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2

1

AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B

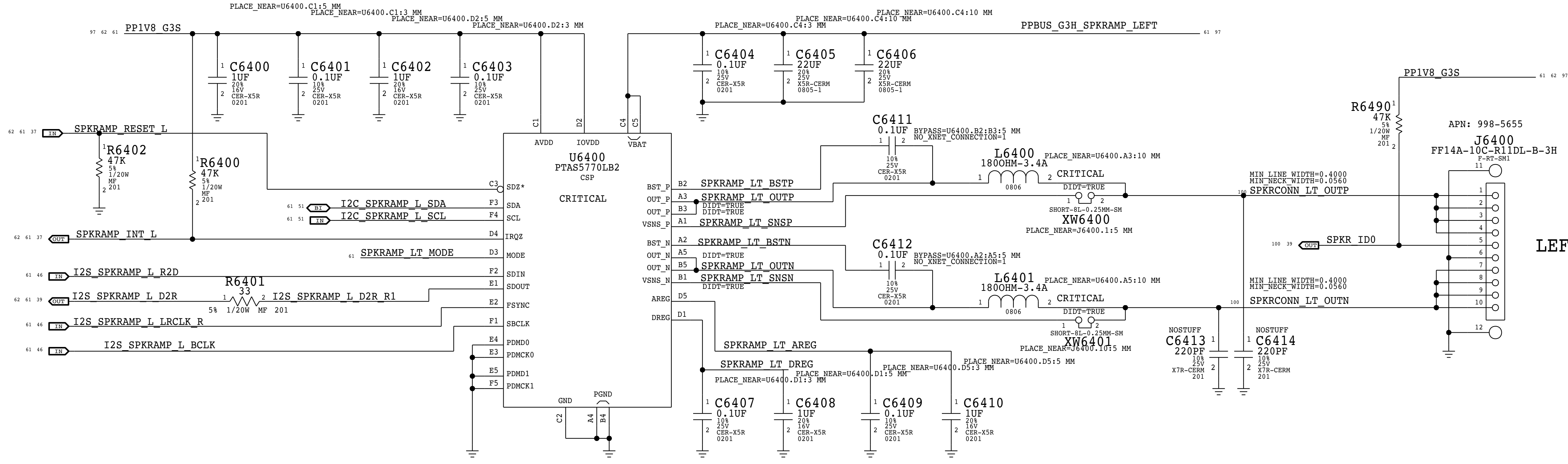


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LAST CHANGE: Wed Feb 18 17:31:01 2015	
PAGE TITLE Audio Jack Codec	
	DRAWING NUMBER 051-02166
	REVISION 4.0.0
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BRANCH evt-mars-0	PAGE 63 OF 150
	SHEET 60 OF 108

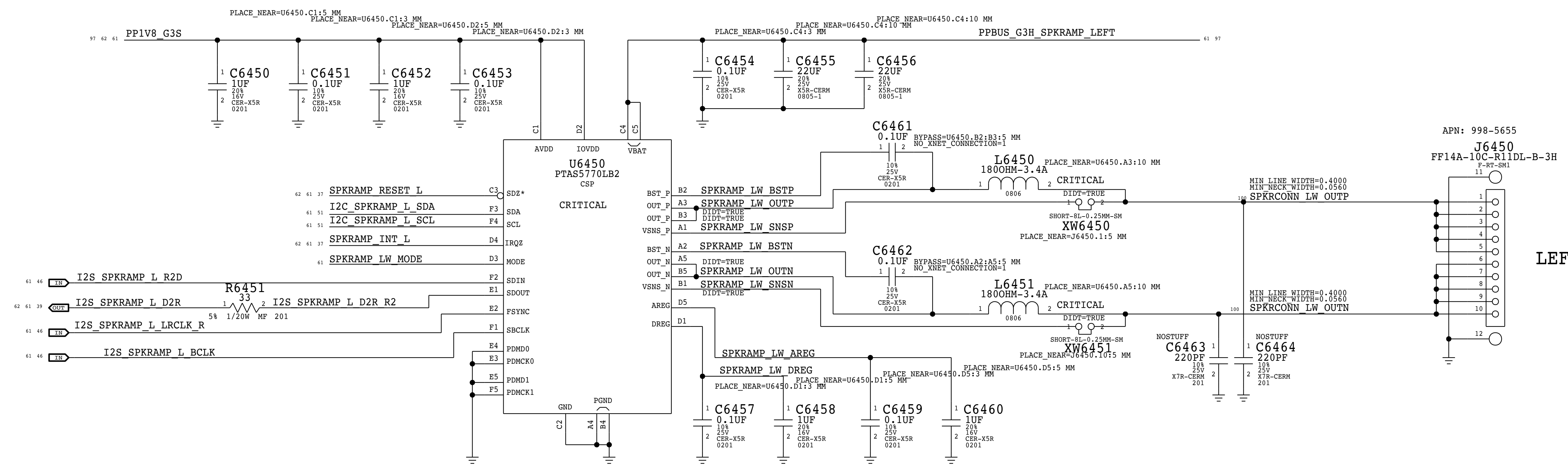
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2X MONO SPEAKER LEFT AMPLIFIERS

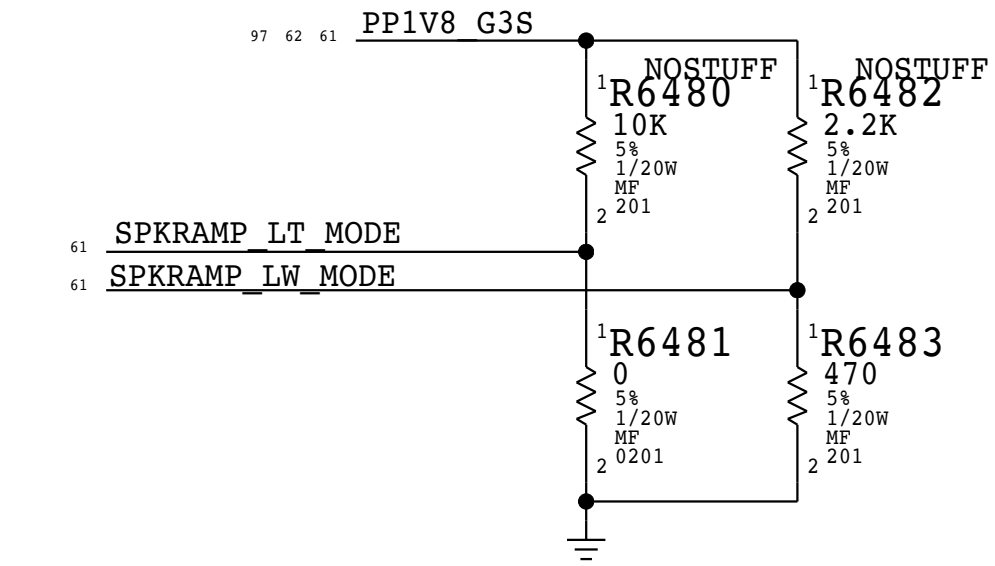
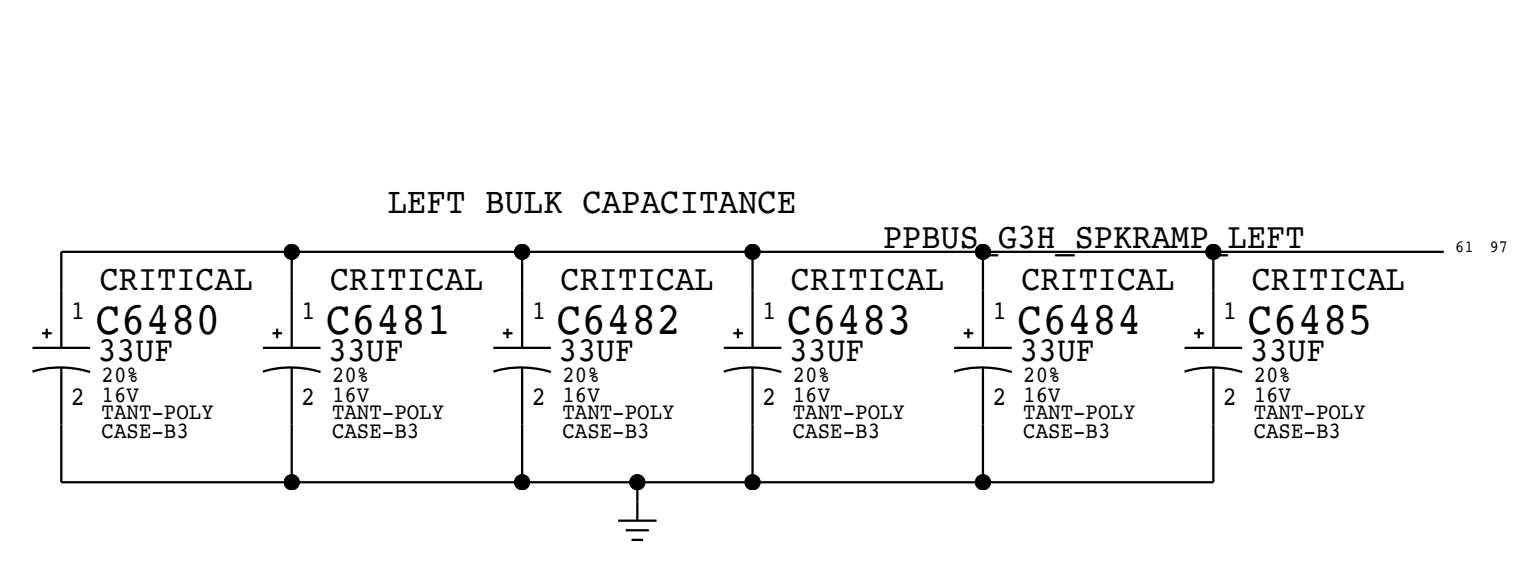
APN: 353S01252
GAIN: 0DBFS = xxVRMS



LEFT TWEETER



LEFT WOOFER



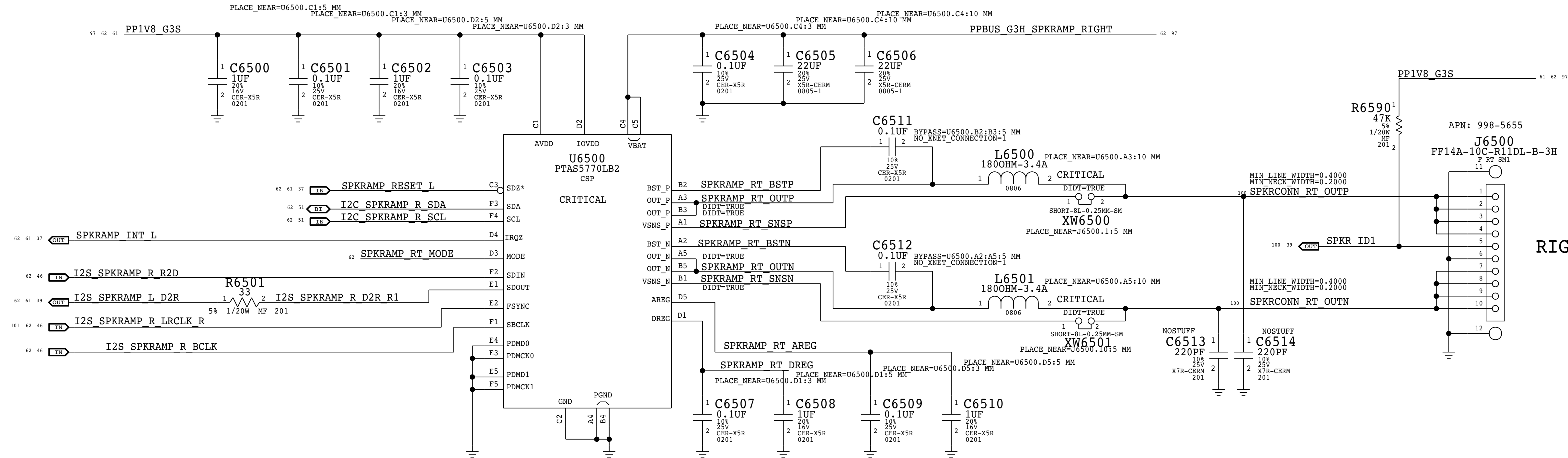
MODE PIN	I2C ADDR	CHANNEL
GND	0x31	L TW
470 to GND	0x32	L WF
470 to IOVDD	0x33	R TW
2K2 to GND	0x34	R WF
2K2 to IOVDD	0x35	
10K to GND	0x36	
10K to IOVDD	0x37	
47K to IOVDD	0x38	

BOM_COST_GROUP=AUDIO

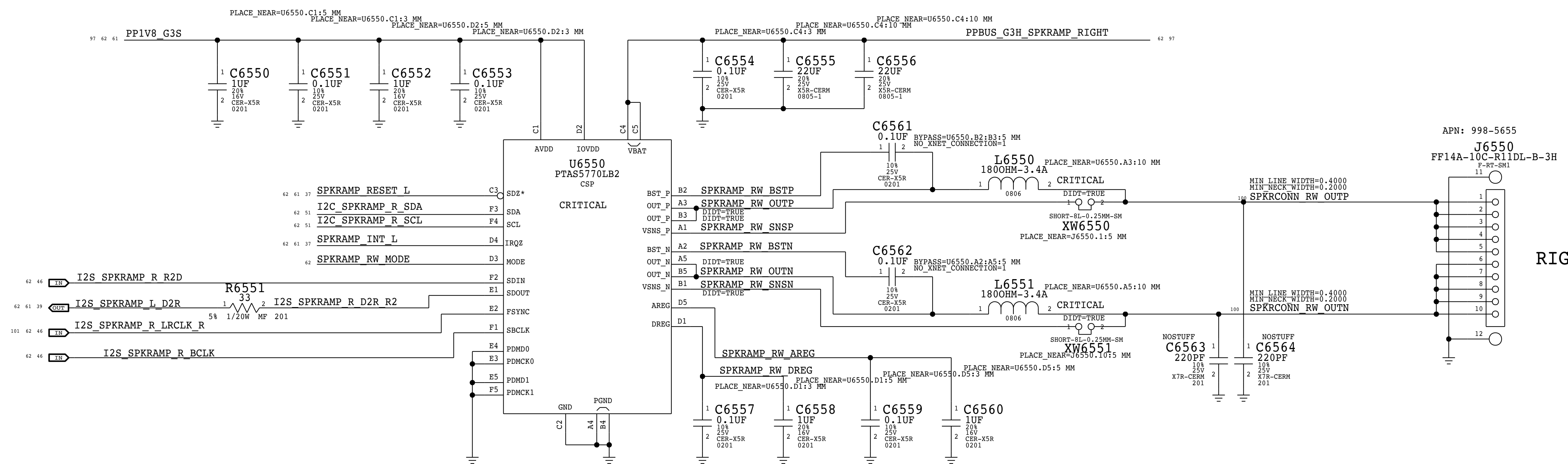
PAGE TITLE		
Audio Left Amplifiers		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	64 OF 150
	SHEET	61 OF 108

2X MONO SPEAKER RIGHT AMPLIFIERS

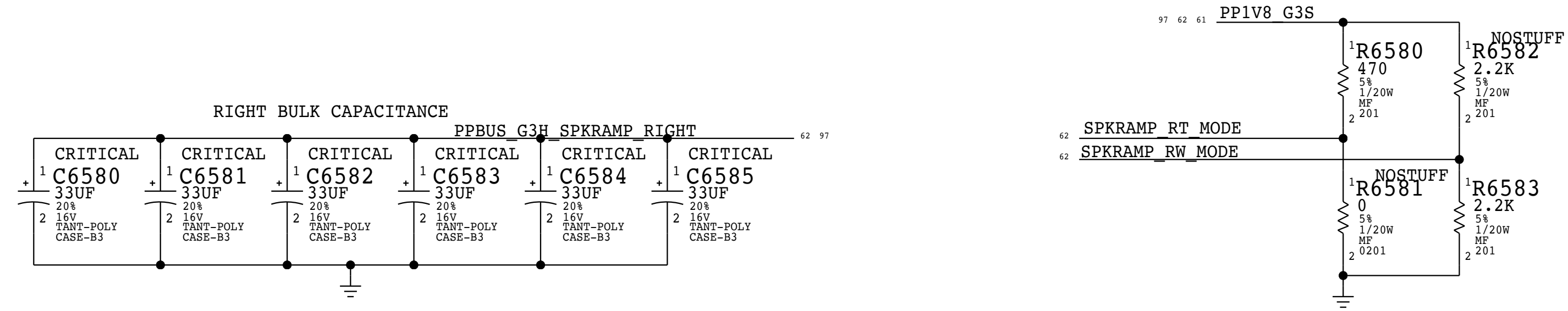
APN: 353S01252
GAIN: 0DBFS = xxVRMS



RIGHT TWEETER



RIGHT WOOFER

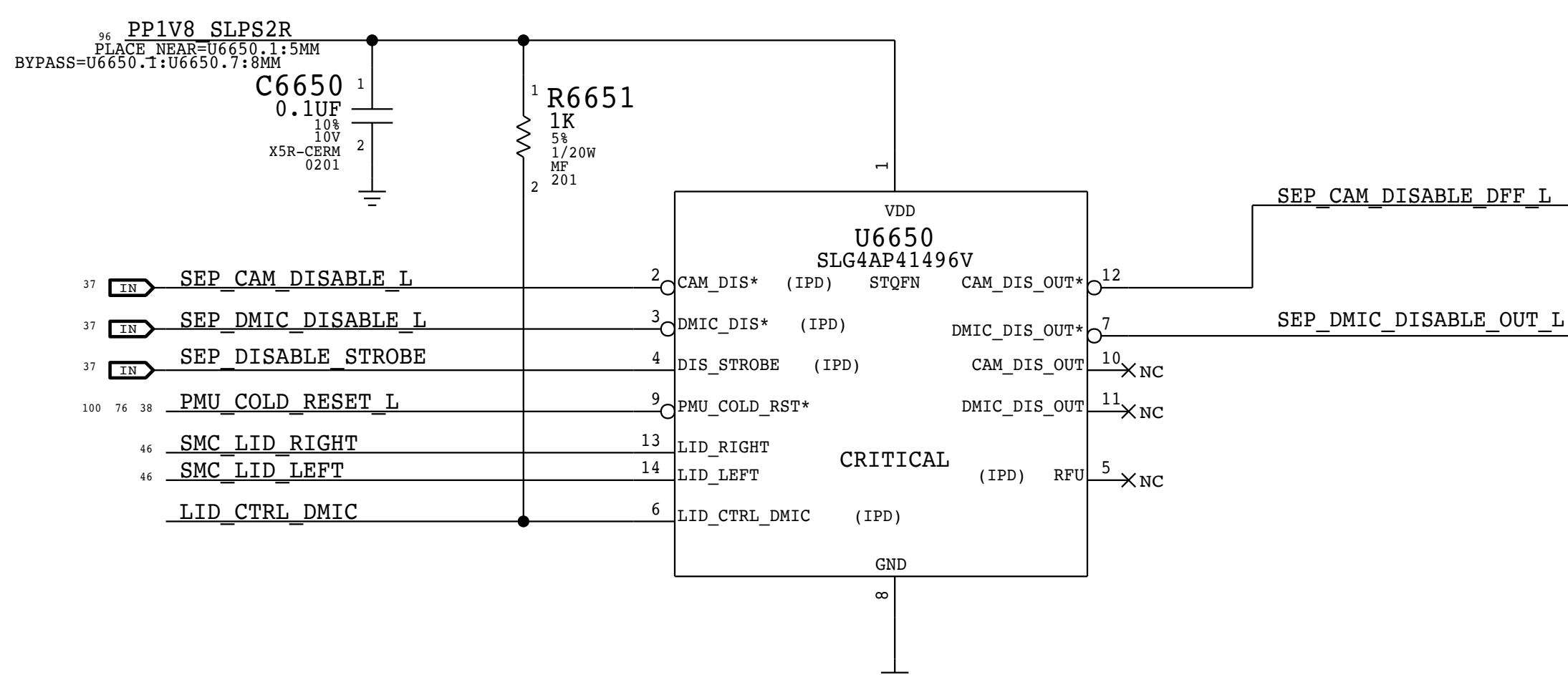


MODE	PIN	I2C ADDR	CHANNEL
GND	0x31		L TW
470 to GND	0x32		L WF
470 to IOVDD	0x33		R TW
2K2 to GND	0x34		R WF
2K2 to IOVDD	0x35		
10K to GND	0x36		
10K to IOVDD	0x37		
47K to IOVDD	0x38		

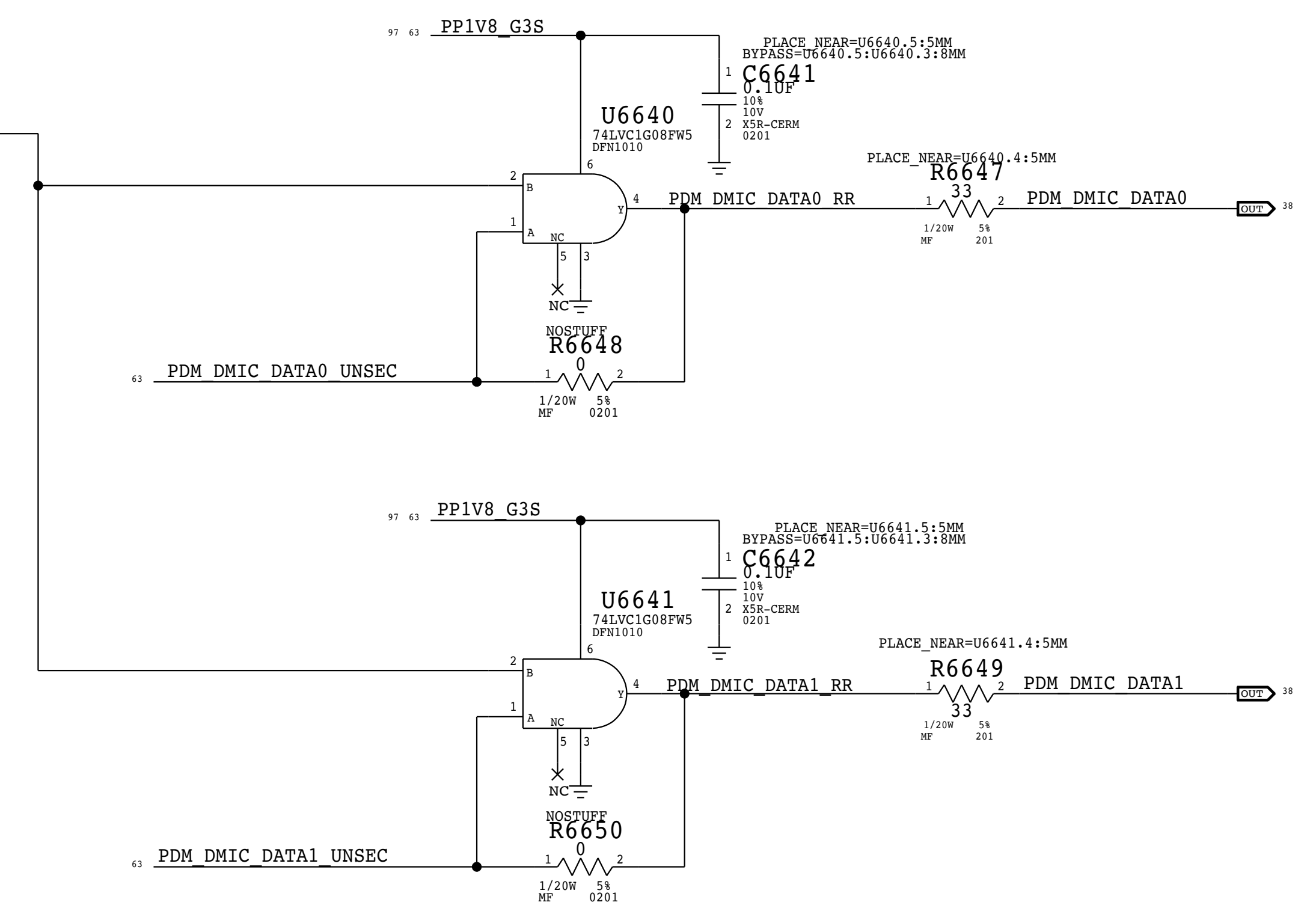
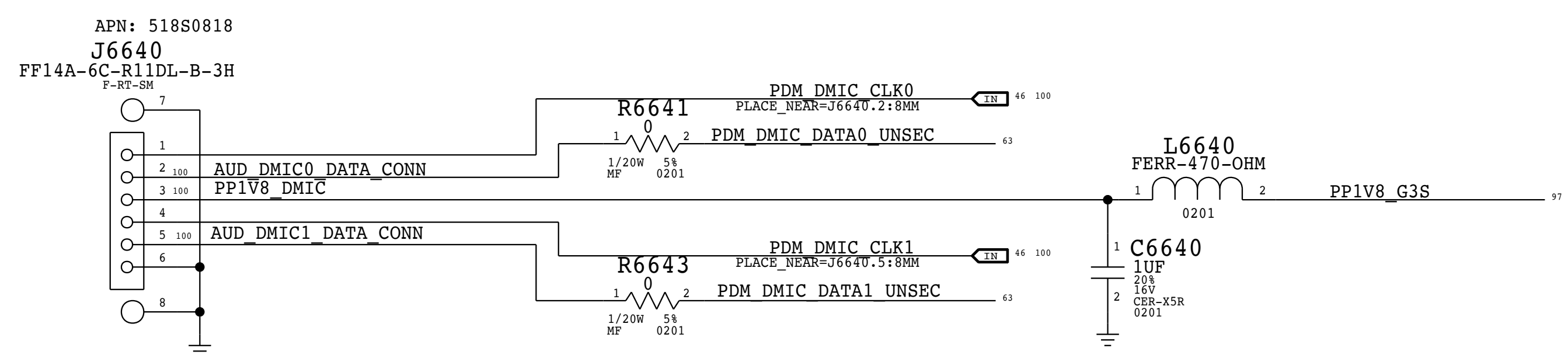
PAGE TITLE		
Audio Right Amplifiers		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	65 OF 150
	SHEET	62 OF 108

BOM_COST_GROUP=AUDIO

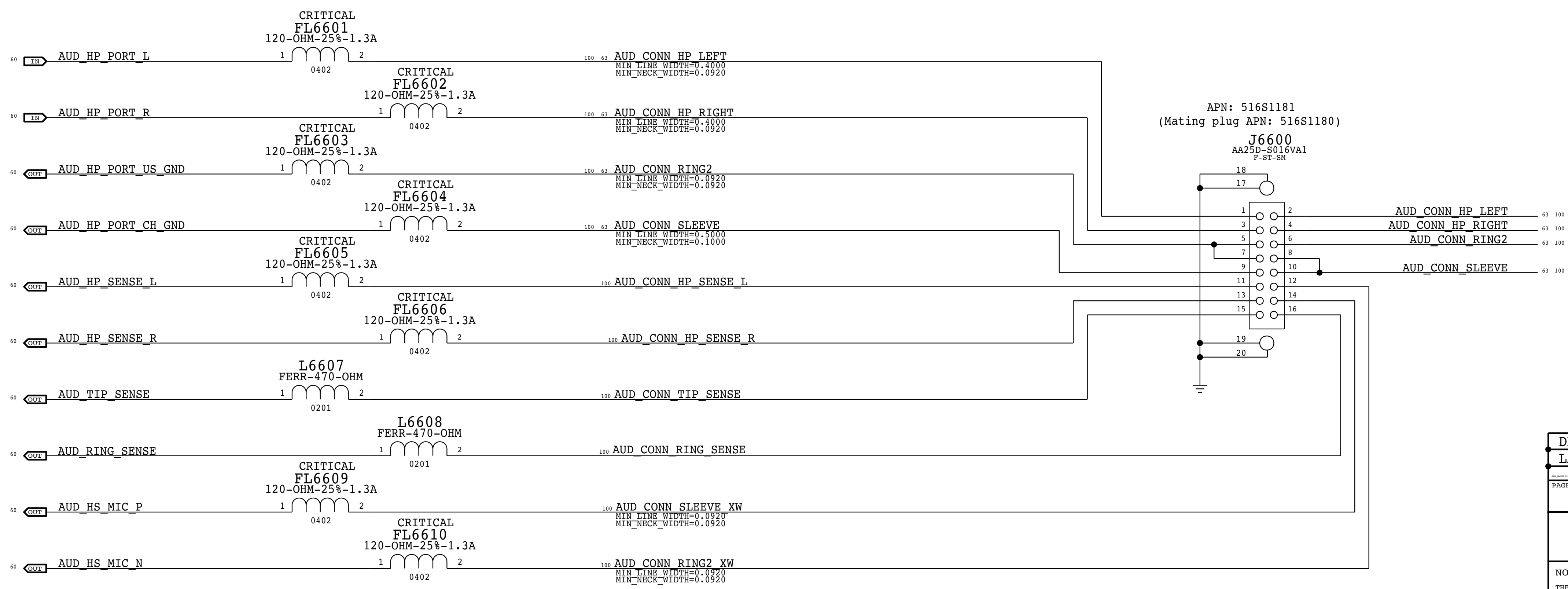
DMIC Secure Disable



Digital Mic Flex Connector



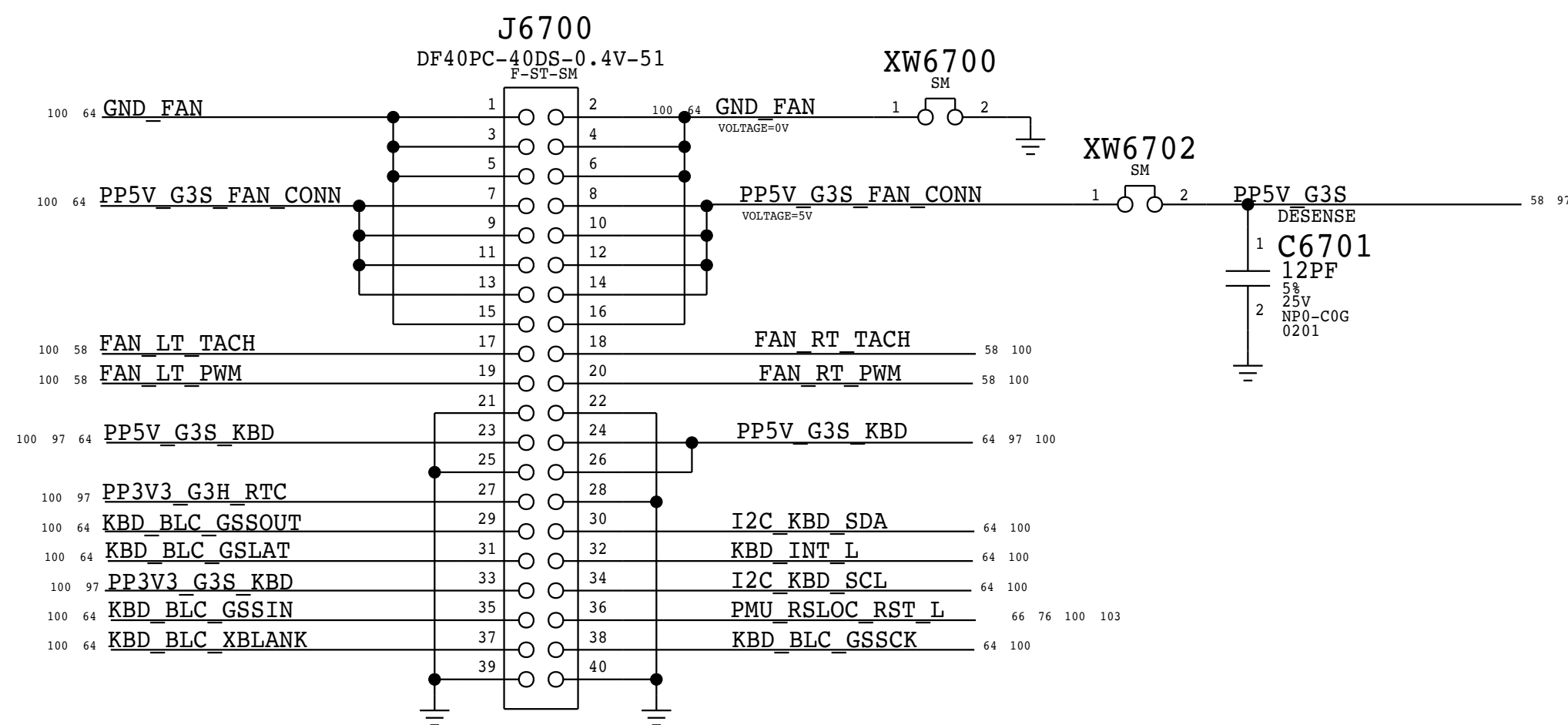
Audio Jack Flex Connector



DESIGN: X502/DEV MLB U		
LAST CHANGE: Wed Feb 18 17:12:24 2015		
PAGE TITLE		
Audio Flex Connectors		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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II NOT TO REPRODUCE OR COPY IT		66 OF 150
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET
IV ALL RIGHTS RESERVED		63 OF 108

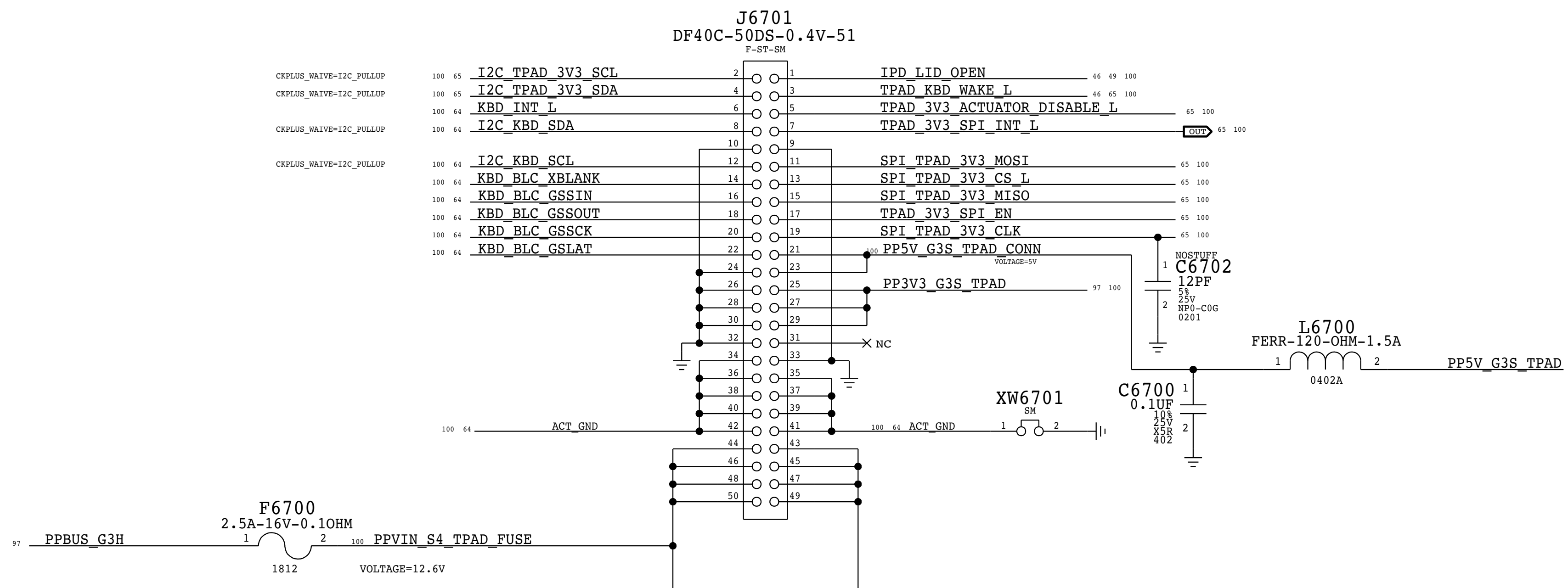
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KBD CONNECTOR



516S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

TPAD CONNECTOR

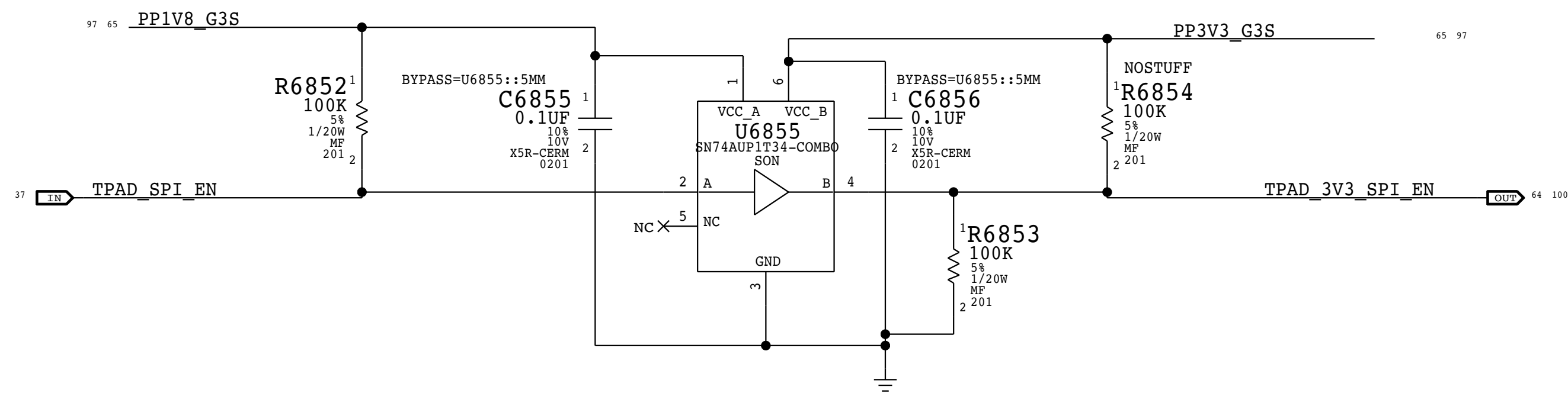
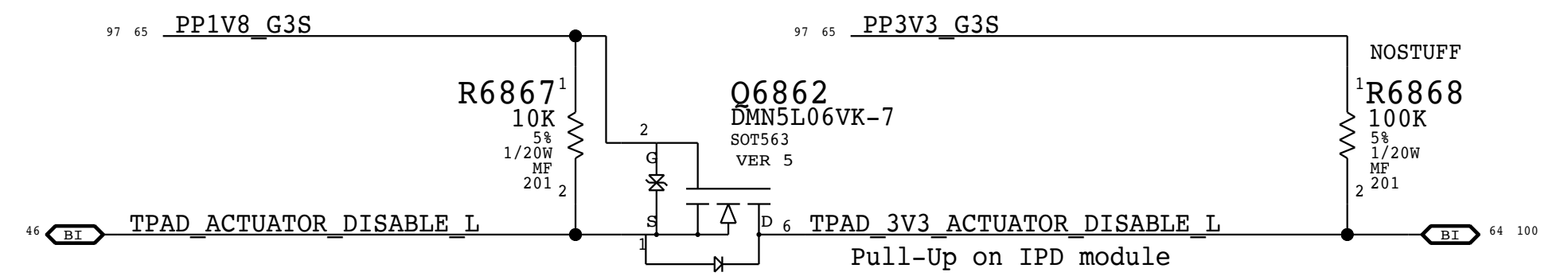
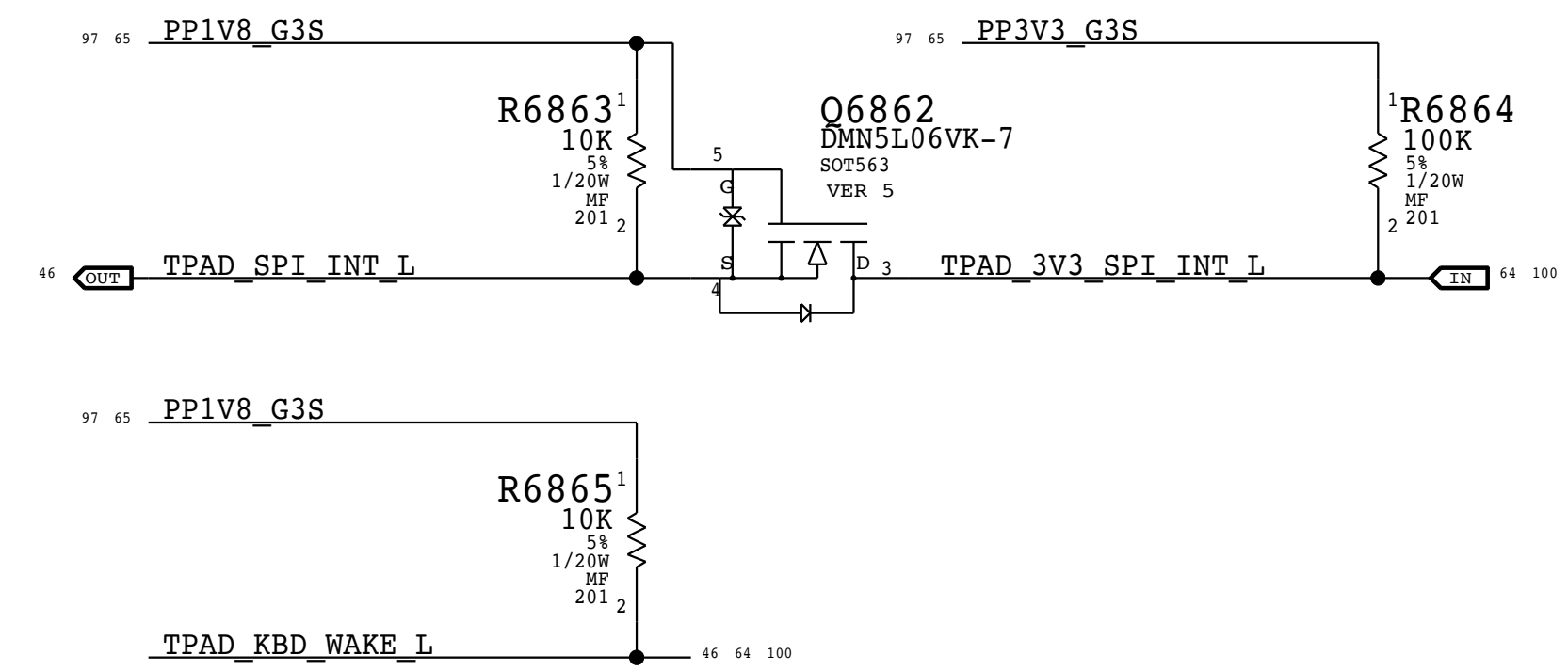
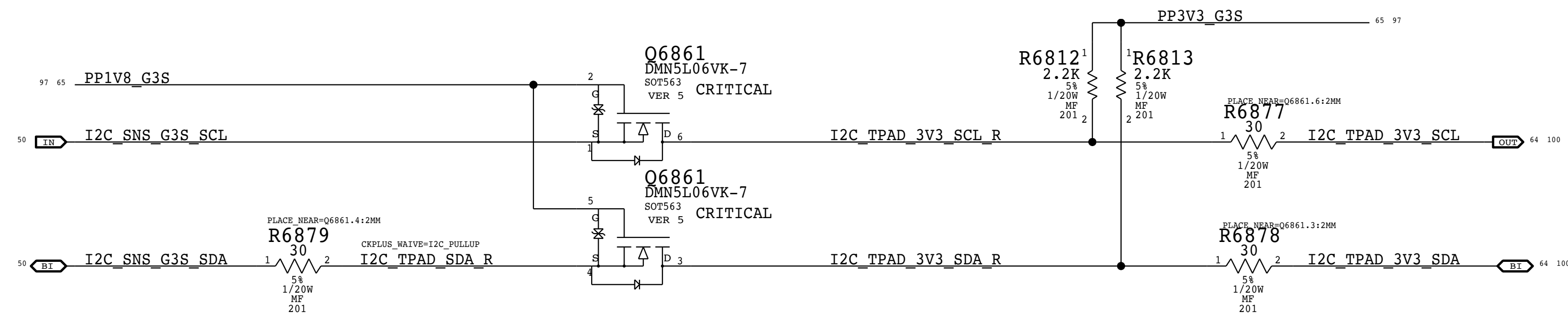
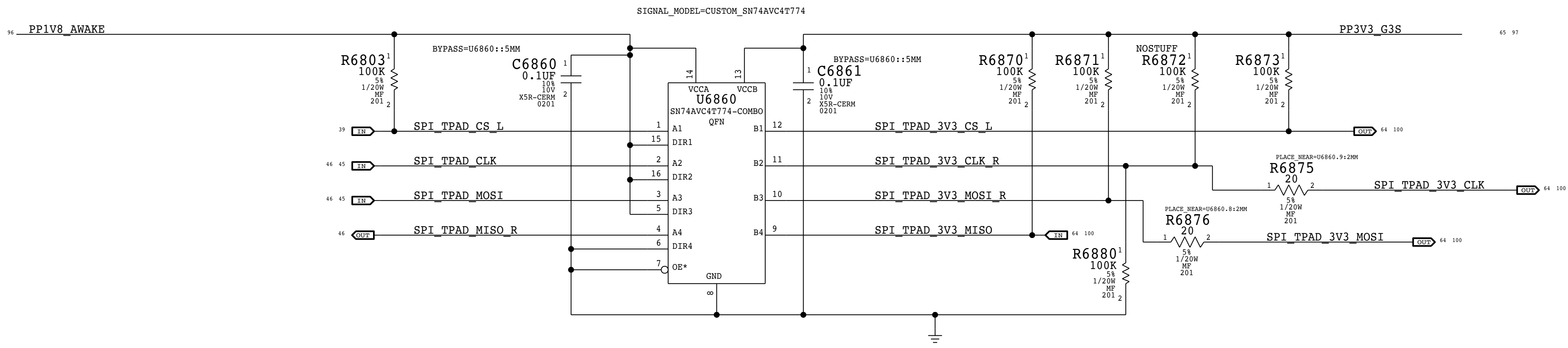


516S00187, MATE WITH 516S00188

PAGE TITLE		Keyboard & Trackpad 1	
Apple Inc.	DRAWING NUMBER	051-02166	SIZE
	REVISION	4.0.0	D
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		PAGE	67 OF 150
		SHEET	64 OF 108

BOM_COST_GROUP=KEYBOARD

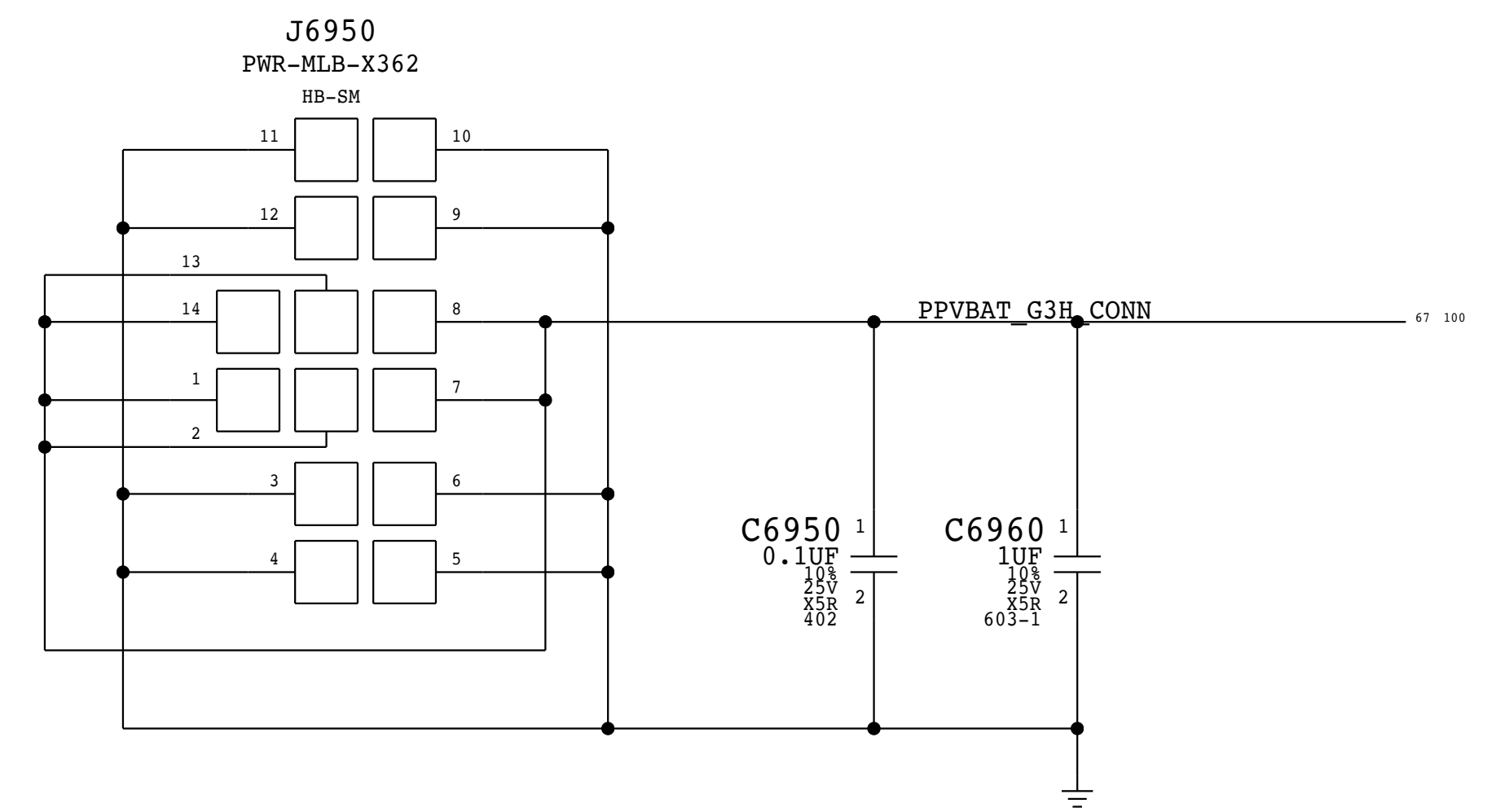
Trackpad Level Shifting



PAGE TITLE		KEYBOARD & TRACKPAD 2	
DRAWING NUMBER		051-02166	SIZE D
REVISION		4.0.0	
BRANCH		evt-mars-0	
PAGE		68 OF 150	
SHEET		65 OF 108	

BOM_COST_GROUP=TRACKPAD

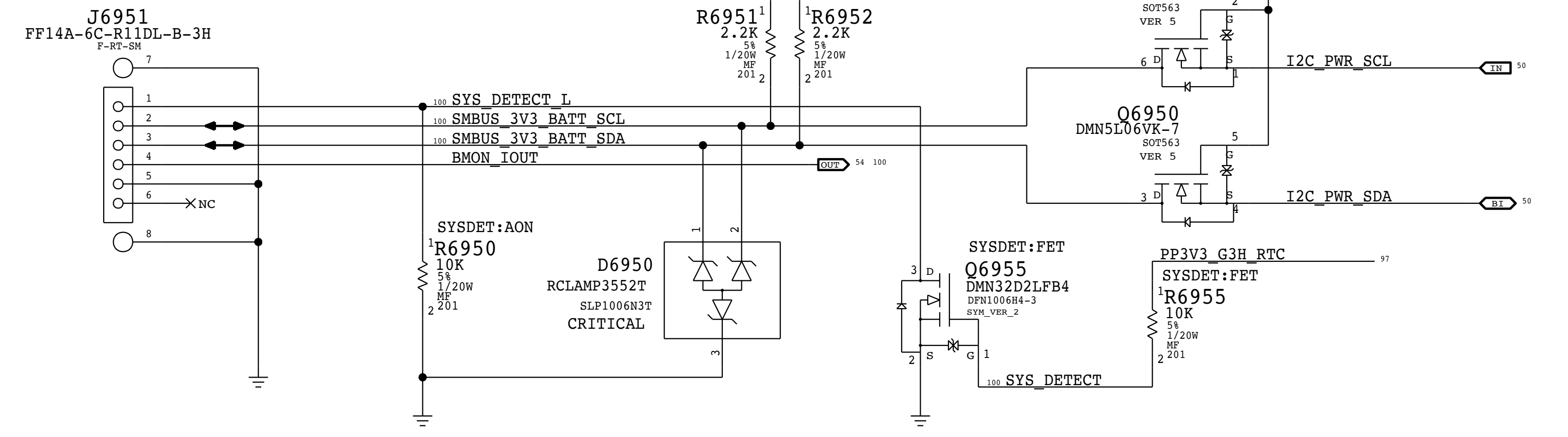
J79 Battery Hotbar Flex Pads



BMU POWER FLEX HOTBAR'd TO THE MLB:

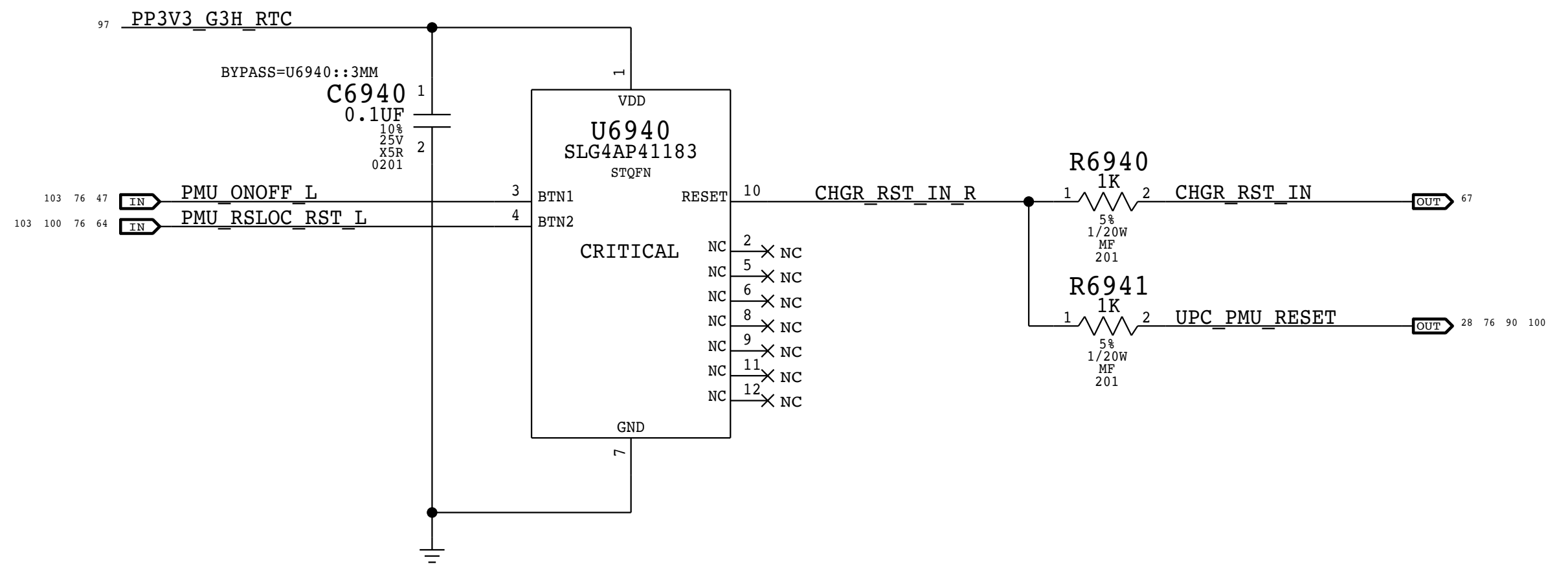
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00566	1	PCBA, FLEX, BMU PWR, X362	J6950	CRITICAL	

APN: 518S0818

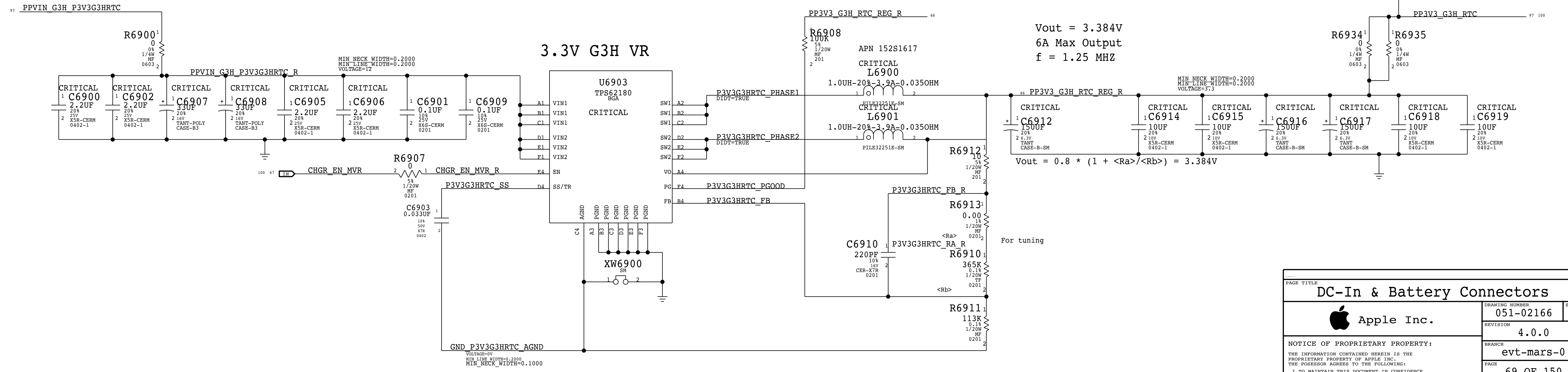


SMC Reset Circuit

Right Shift & Left Option Control followed by ON OFF button press.

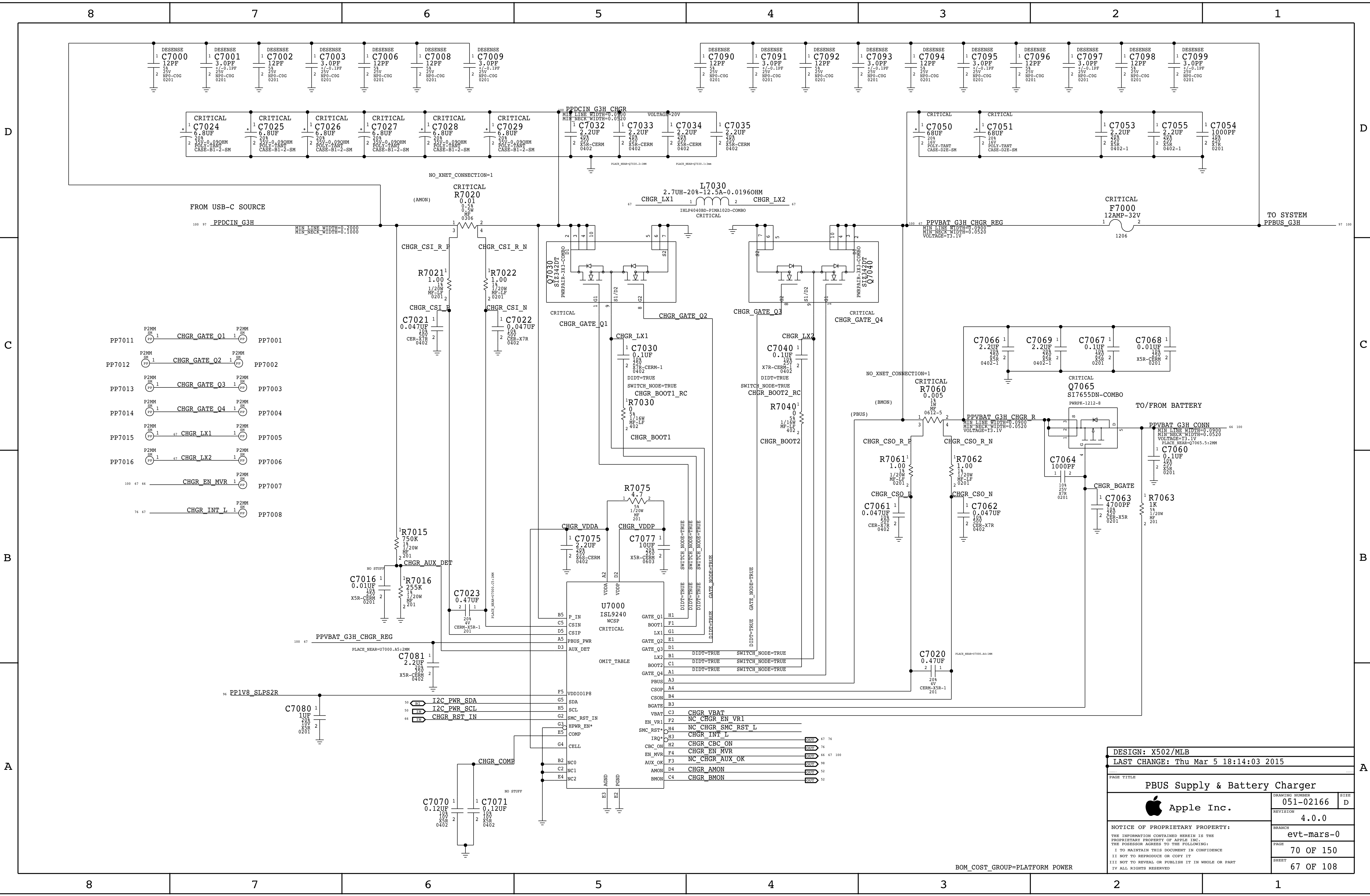



3.3V G3H VR



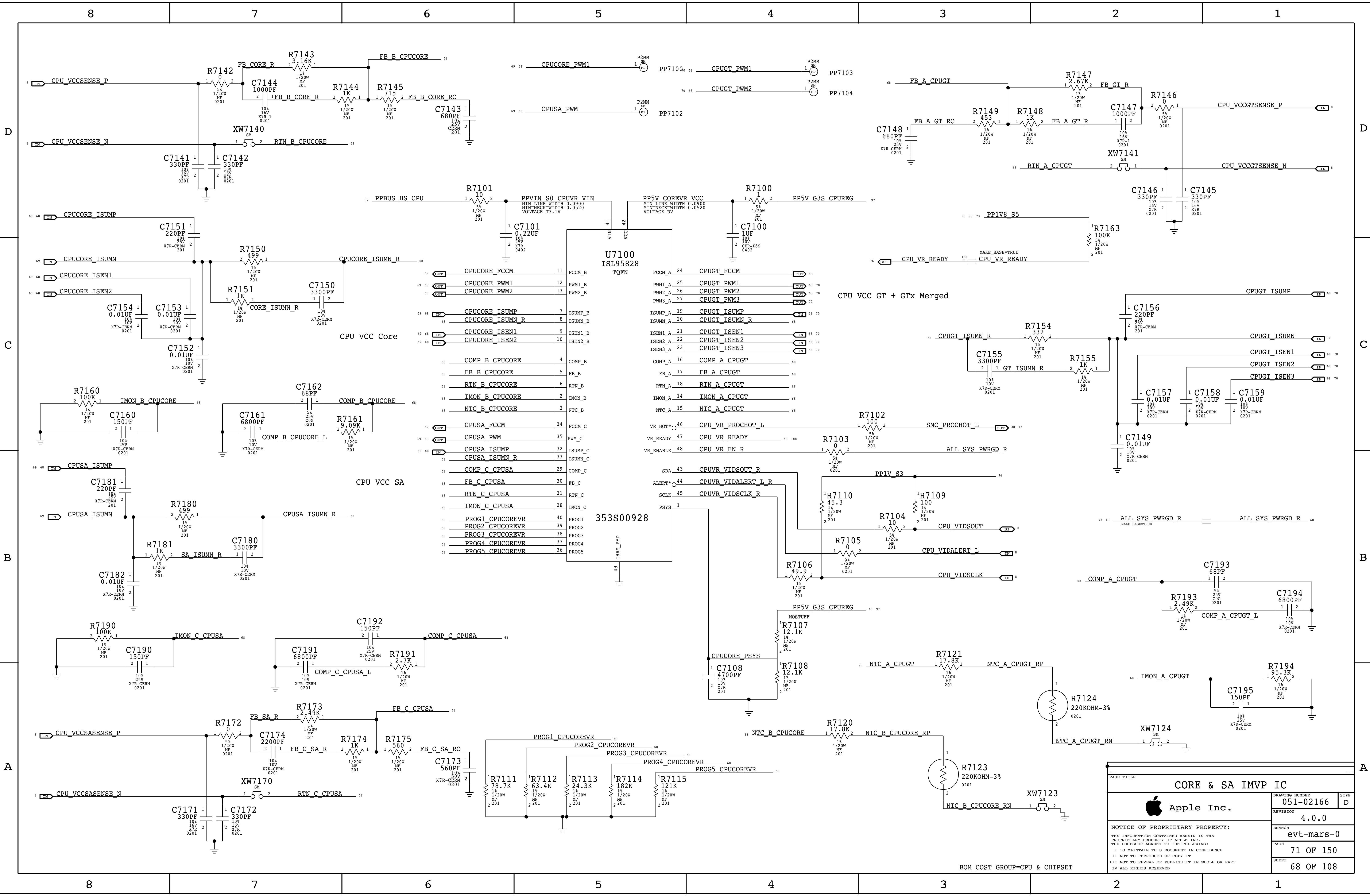
PAGE TITLE		
DC-In & Battery Connectors		
	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	69 OF 150
	SHEET	66 OF 108

BOM_COST_GROUP=PLATFORM POWER



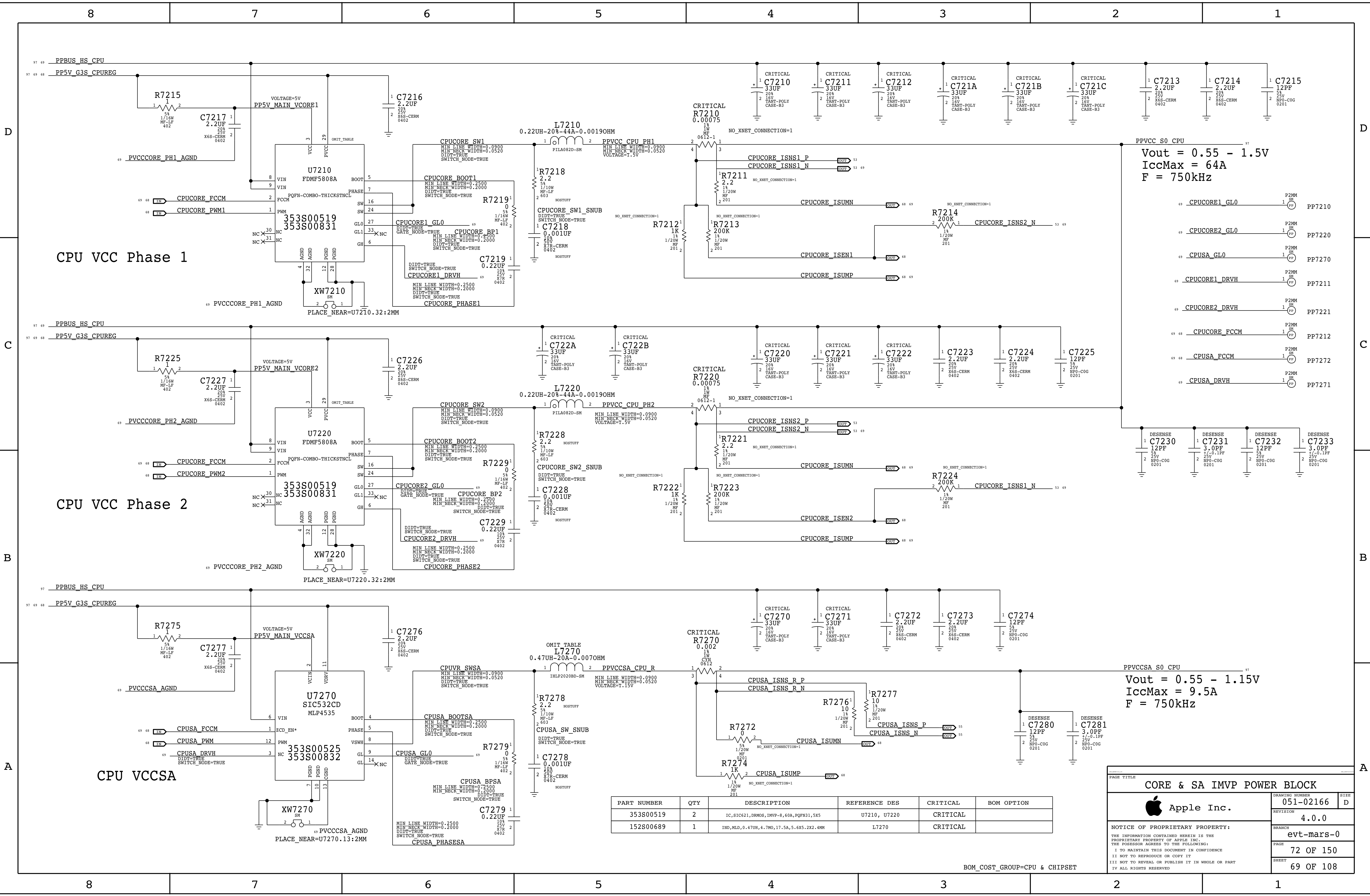
DESIGN: X502/MLB	
LAST CHANGE: Thu Mar 5 18:14:03 2015	
PAGE TITLE	
PBUS Supply & Battery Charger	
 Apple Inc.	DRAWING NUMBER 051-02166
REVISION	
4.0.0	
BRANCH	
evt-mars-0	
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SHEET	
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BOM_COST_GROUP=PLATFORM POWER



PAGE TITLE		
CORE & SA IMVP IC		
		DRAWING NUMBER 051-02166
		SIZE D
		REVISION 4.0.0
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		PAGE 71 OF 150
		SHEET 68 OF 108

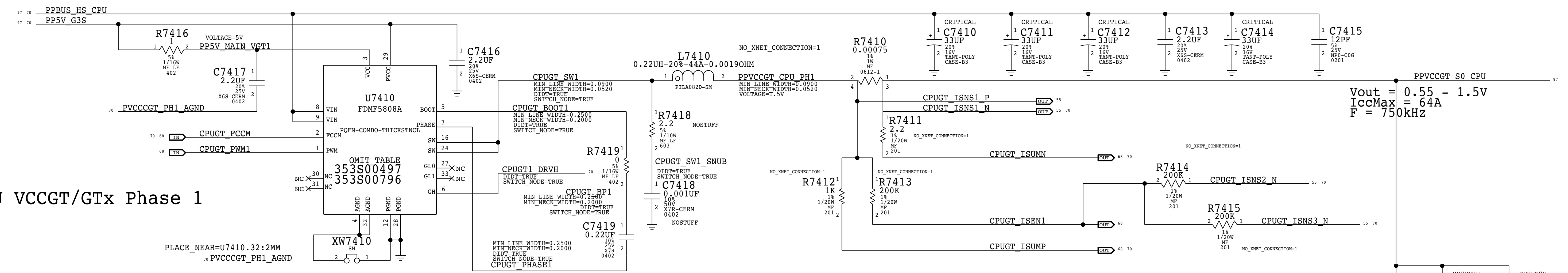
BOM_COST_GROUP=CPU & CHIPSET



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00519	2	IC, SiC621, DRMOS, IMVP-8, 60A, PQFN31, 5x5	U7210, U7220	CRITICAL	
152S00689	1	IND, MLD, 0.47UH, 4.7mH, 17.5A, 5.6x5.2x2.4mm	L7270	CRITICAL	

PAGE TITLE		
CORE & SA IMVP POWER BLOCK		
		DRAWING NUMBER 051-02166
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BOM_COST_GROUP=CPU & CHIPSET		BRANCH evt-mars-0
SHEET 72 OF 150		PAGE 69 OF 108

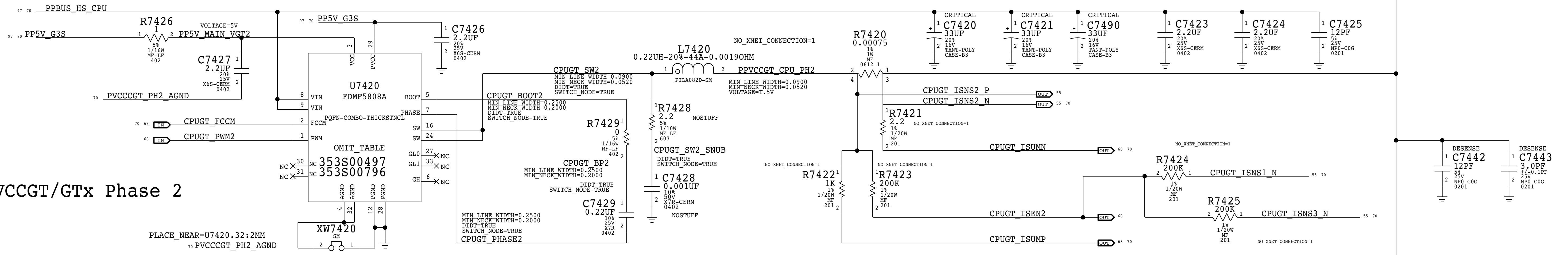
CPU VCCGT/GTx Phase 1



PLACE_NEAR=U7410.32:2MM
70 PVCCCGT_PH1_AGND

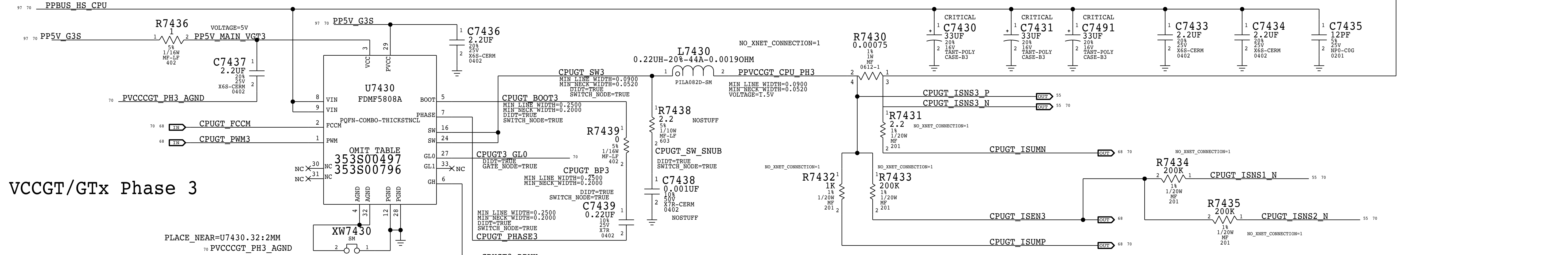
Vout = 0.55 - 1.5V
IccMax = 64A
F = 750kHz

CPU VCCGT/GTx Phase 2



PLACE_NEAR=U7420.32:2MM
70 PVCCCGT_PH2_AGND

CPU VCCGT/GTx Phase 3



PLACE_NEAR=U7430.32:2MM
70 PVCCCGT_PH3_AGND

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,FDMF808A,DEMOS,IMVP8,50A,POFN31,5X5	U7410, U7420, U7430	CRITICAL	

PAGE TITLE		
GT & GTX IMVP POWER BLOCK		
		DRAWING NUMBER 051-02166
		SIZE D
		REVISION 4.0.0
		BRANCH evt-mars-0
		PAGE 74 OF 150
		SHEET 70 OF 108
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BOM_COST_GROUP=CPU & CHIPSET

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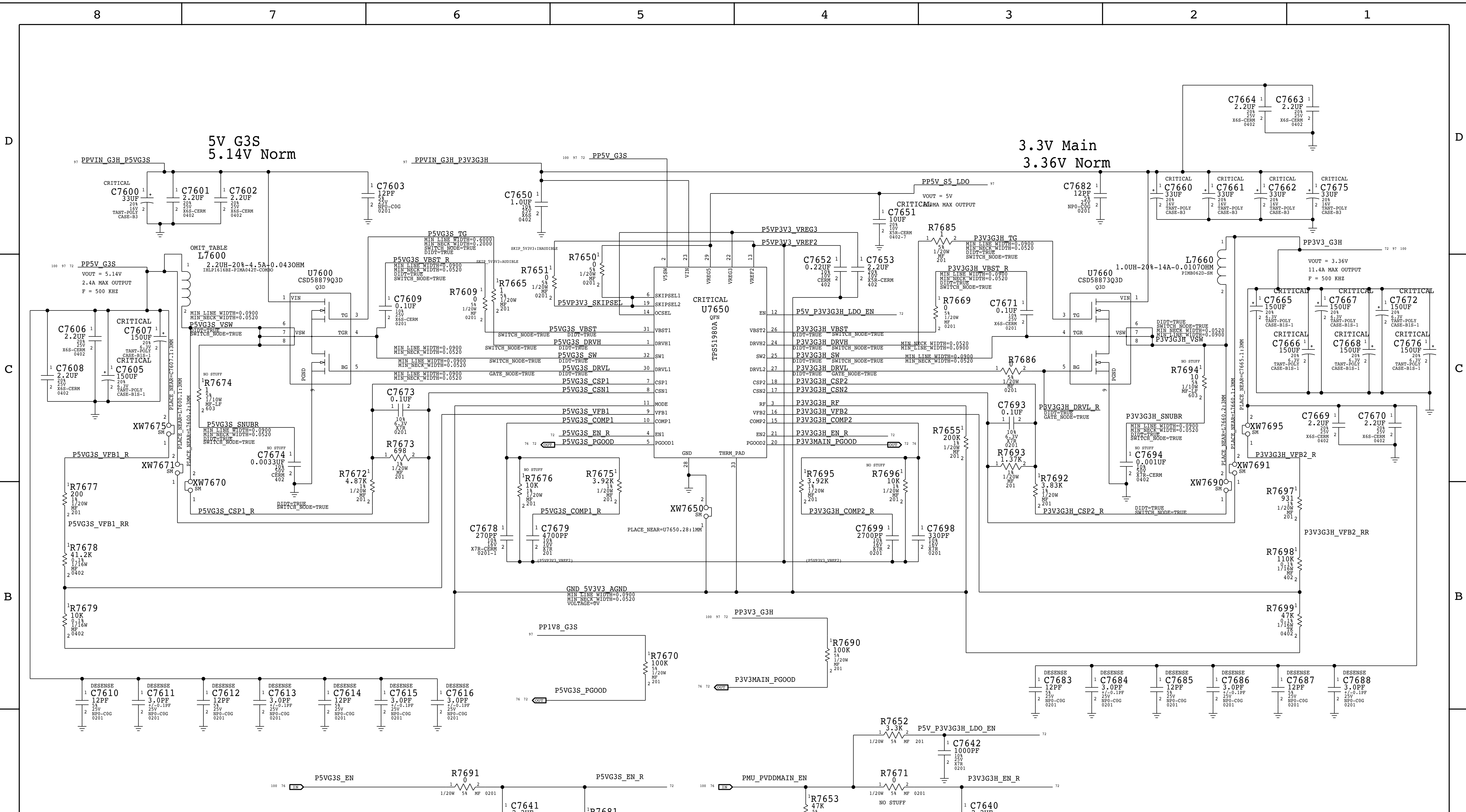
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SYNC MASTER=J132 MAO		SYNC DATE=02/09/2017	
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	REVISION	4.0.0	
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	PAGE	75 OF 150	
	SHEET	71 OF 108	

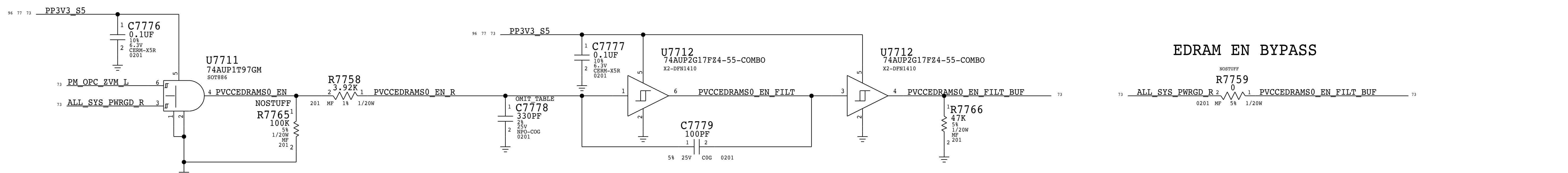
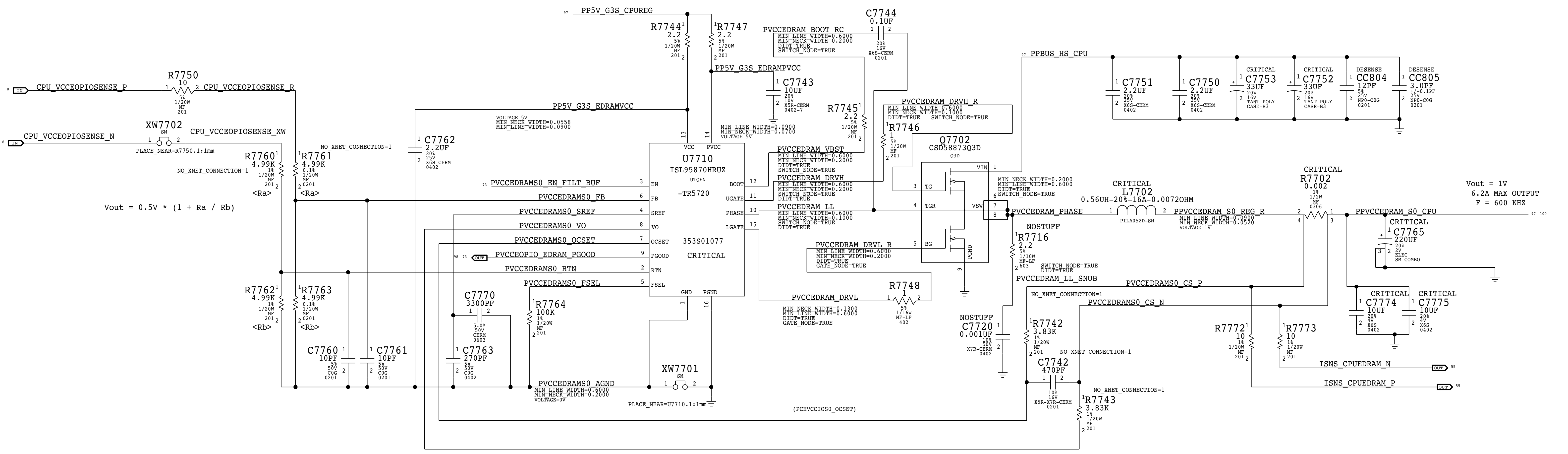


PAGE TITLE		
Power - 5V 3.3V Supply		
		DRAWING NUMBER 051-02166
Apple Inc.		SIZE D
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BRANCH evt-mars-0		PAGE 76 OF 150
SHEET 72 OF 108		

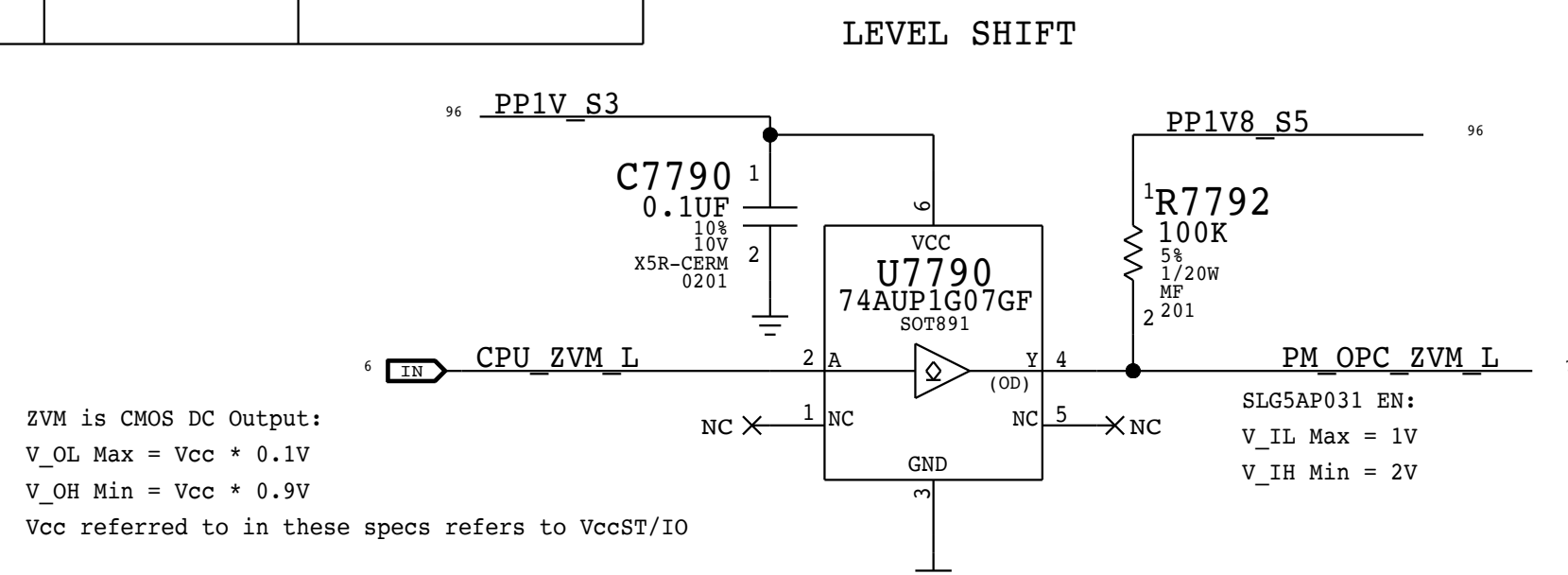
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00182	1	IND,PWR,2.2UH,20%,4.5A,43MOHM,4X4MM	L7600	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

1V EDRAM & EOPIO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00294	1	CAP,COG,330PF,5%,25V,0201	C7778		



ZVM is CMOS DC Output:
 V_OL Max = Vcc * 0.1V
 V_OH Min = Vcc * 0.9V
 Vcc referred to in these specs refers to VccST/IO

PAGE TITLE Power - EOPIO EDRAM Supply		
	DRAWING NUMBER 051-02166	SIZE D
	REVISION 4.0.0	BRANCH evt-mars-0
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BOM_COST_GROUP=CPU & CHIPSET

Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
 System Block Diagram - T290 Power System Architecture . v9
 Optimize components for individual projects based on EDP(A)

CRITICAL OMIT_TABLE

D

D

C

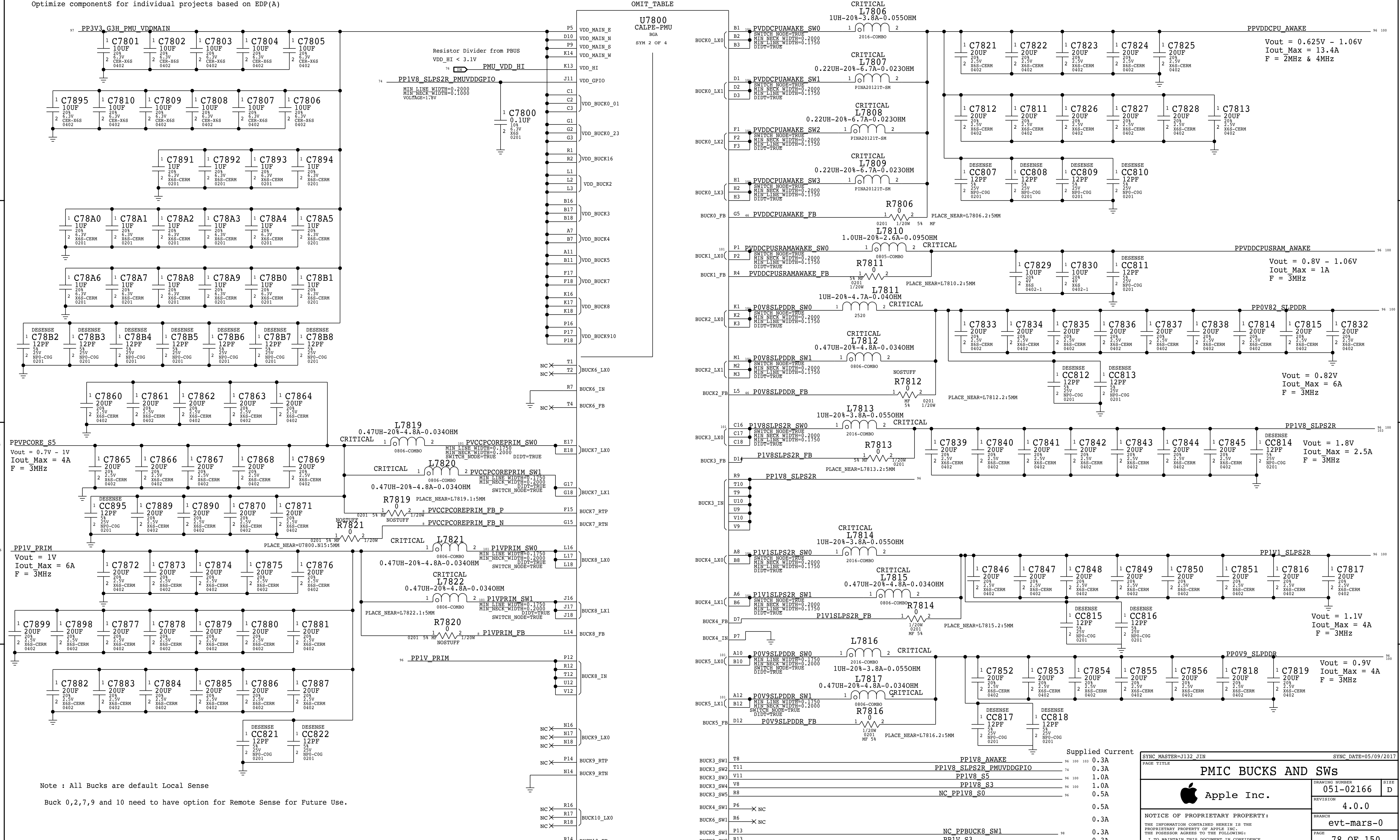
C

B

B

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A



Note : All Bucks are default Local Sense
 Buck 0,2,7,9 and 10 need to have option for Remote Sense for Future Use.

Supplied Current

BUCK3_SW1	T8	PP1V8_AWAKE	96	0.3A
BUCK3_SW2	T11	PP1V8_SLPS2R_PMUVDGGPIO	94	0.3A
BUCK3_SW3	V11	PP1V8_S5	96	1.0A
BUCK3_SW4	V8	PP1V8_S3	96	1.0A
BUCK3_SW5	R8	NC_PP1V8_S0	96	0.5A
BUCK4_SW1	P6	NC		0.5A
BUCK6_SW1	R6	NC		0.3A
BUCK8_SW1	P13	NC_PPBUCK8_SW1	98	0.3A
BUCK8_SW2	R13	PP1V_S3	96	0.3A

BOM_COST_GROUP=PLATFORM POWER

SYNC MASTER=J132 JIN SYNC DATE=05/09/2017

PAGE TITLE

PMIC BUCKS AND SWs

Apple Inc.

DRAWING NUMBER	051-02166	SIZE	D
REVISION	4.0.0	BRANCH	evt-mars-0
PAGE	78 OF 150	SHEET	74 OF 108

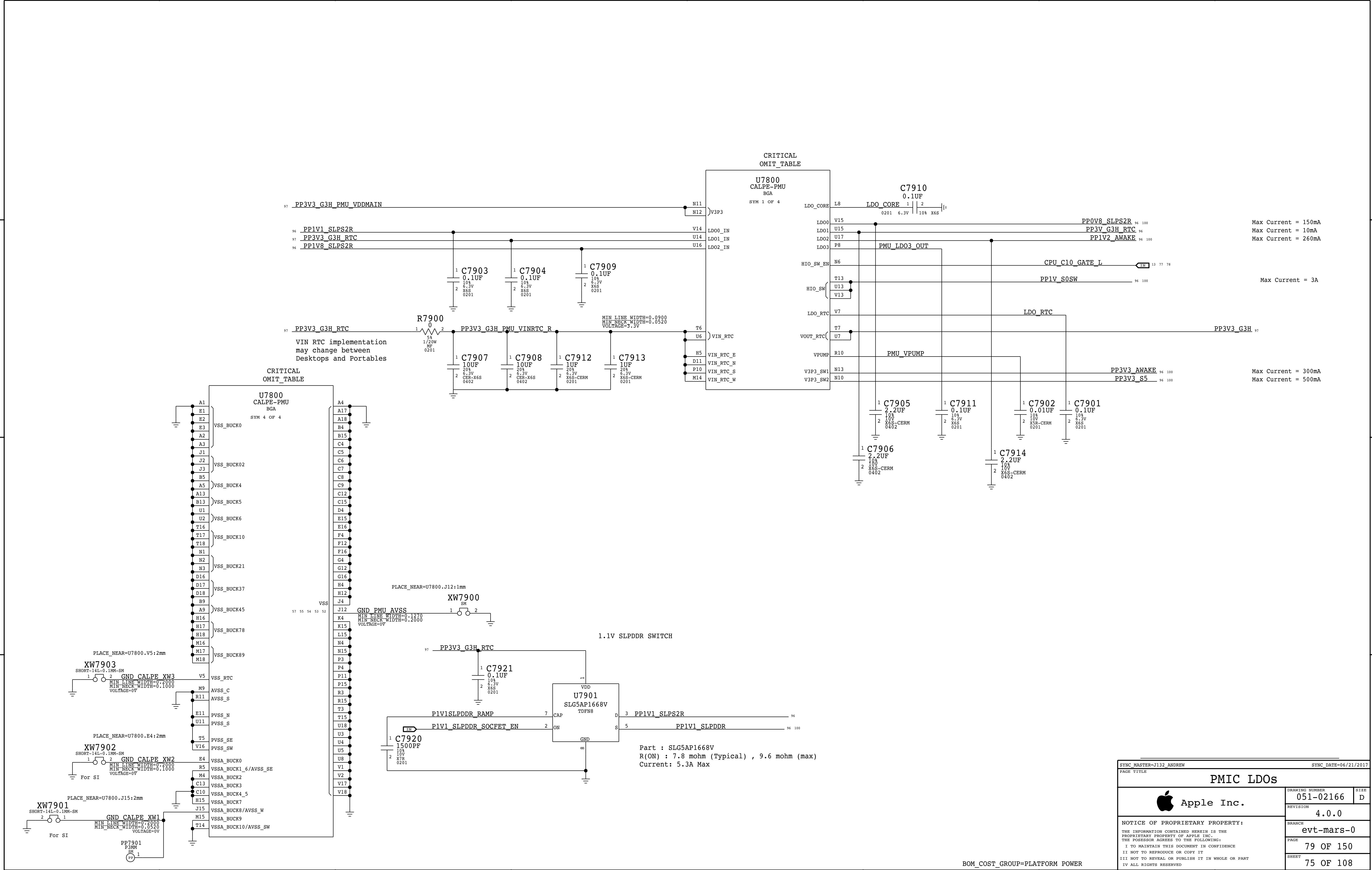
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Max Current = 150mA
Max Current = 10mA
Max Current = 260mA

Max Current = 3A

Max Current = 300mA
Max Current = 500mA

VIN RTC implementation may change between Desktops and Portables

CRITICAL OMIT_TABLE

CRITICAL OMIT_TABLE

C7910

C7907 C7908 C7912 C7913

C7905 C7911 C7902 C7901

C7906 C7914

1.1V SLPDDR SWITCH

Part : SLG5AP1668V
R(ON) : 7.8 mohm (Typical) , 9.6 mohm (max)
Current: 5.3A Max

SYNC_MASTER=J132 ANDREW		SYNC_DATE=06/21/2017	
PAGE TITLE			
		DRAWING NUMBER	
		051-02166	
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		4.0.0	
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		evt-mars-0	
		PAGE	
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		SHEET	
		75 OF 108	

D

C

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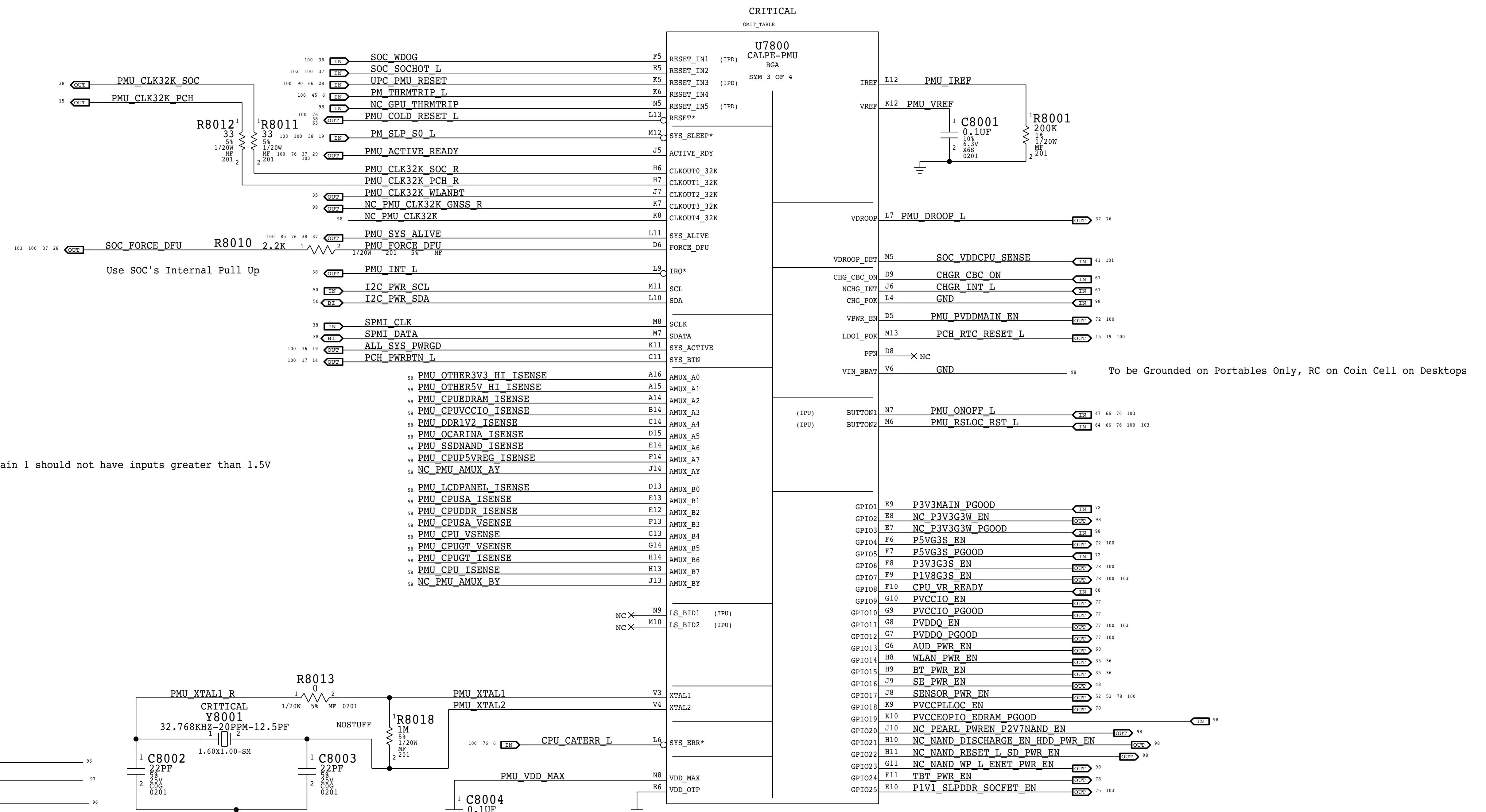
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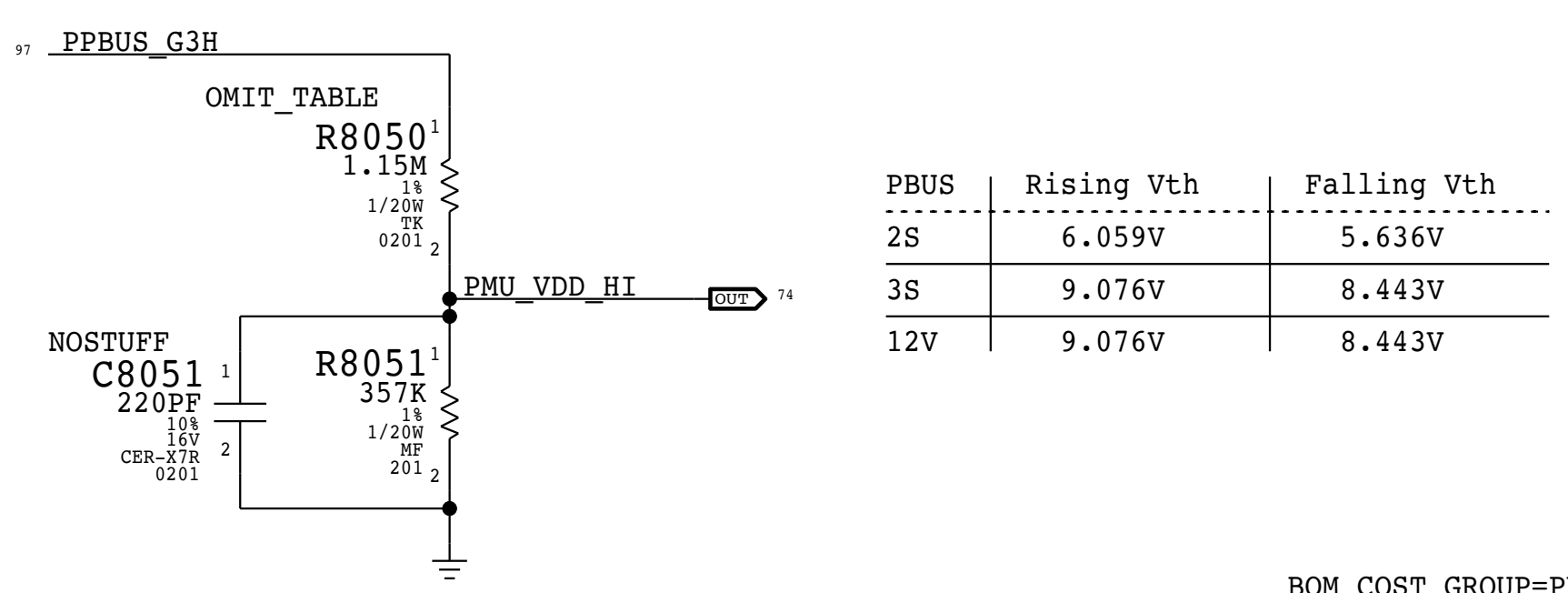
A



Caution : AMUX programmed with Gain 1 should not have inputs greater than 1.5V

VDD_HI Threshold Select

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0481	1	RES, MF, 649K, 1%, 1/20W, 0201	R8050		PBUS:2S
118S00077	1	RES, MF, 1.15M, 1%, 1/16W, 0201	R8050		PBUS:3S
118S00077	1	RES, MF, 1.15M, 1%, 1/16W, 0201	R8050		PBUS:12V



BOM_COST_GROUP=PLATFORM POWER

Apple Inc. logo and title: **PMIC GPIOs & Control**

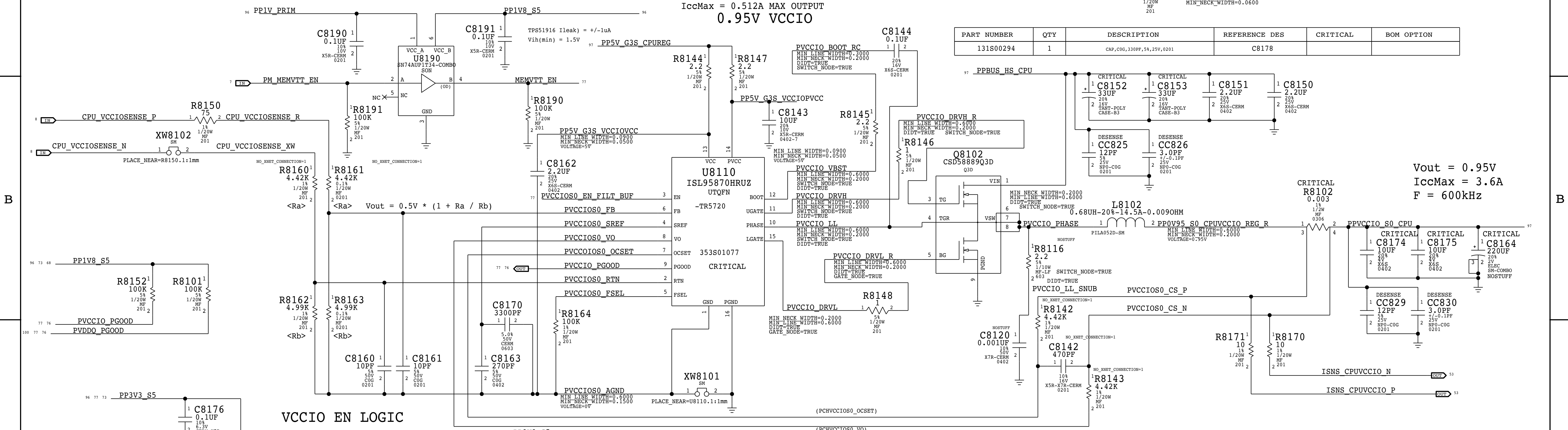
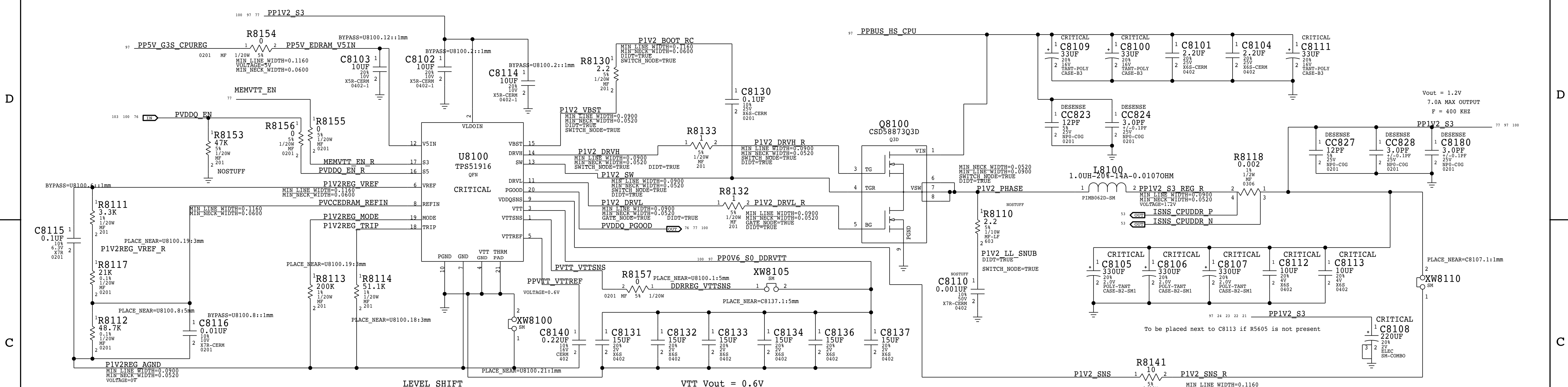
Apple Inc. logo

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 REVISION: 4.0.0
 evt-mars-0

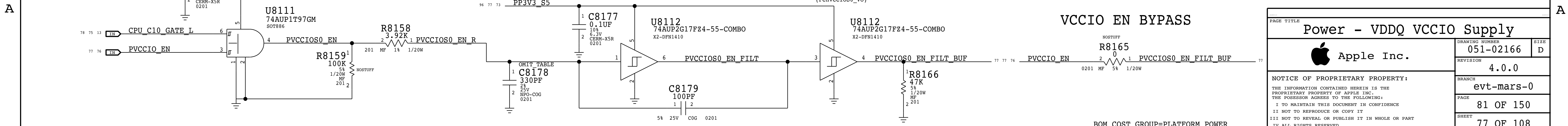
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PAGE: 80 OF 150
 SHEET: 76 OF 108

1.2V VDDQ & 0.6V VTT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00294	1	CAP, COG, 330PF, 5V, 25V, 0201	C8178		



Power - VDDQ VCCIO Supply

Apple Inc.

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REVISION	4.0.0	BRANCH	evt-mars-0
PAGE	81 OF 150	SHEET	77 OF 108

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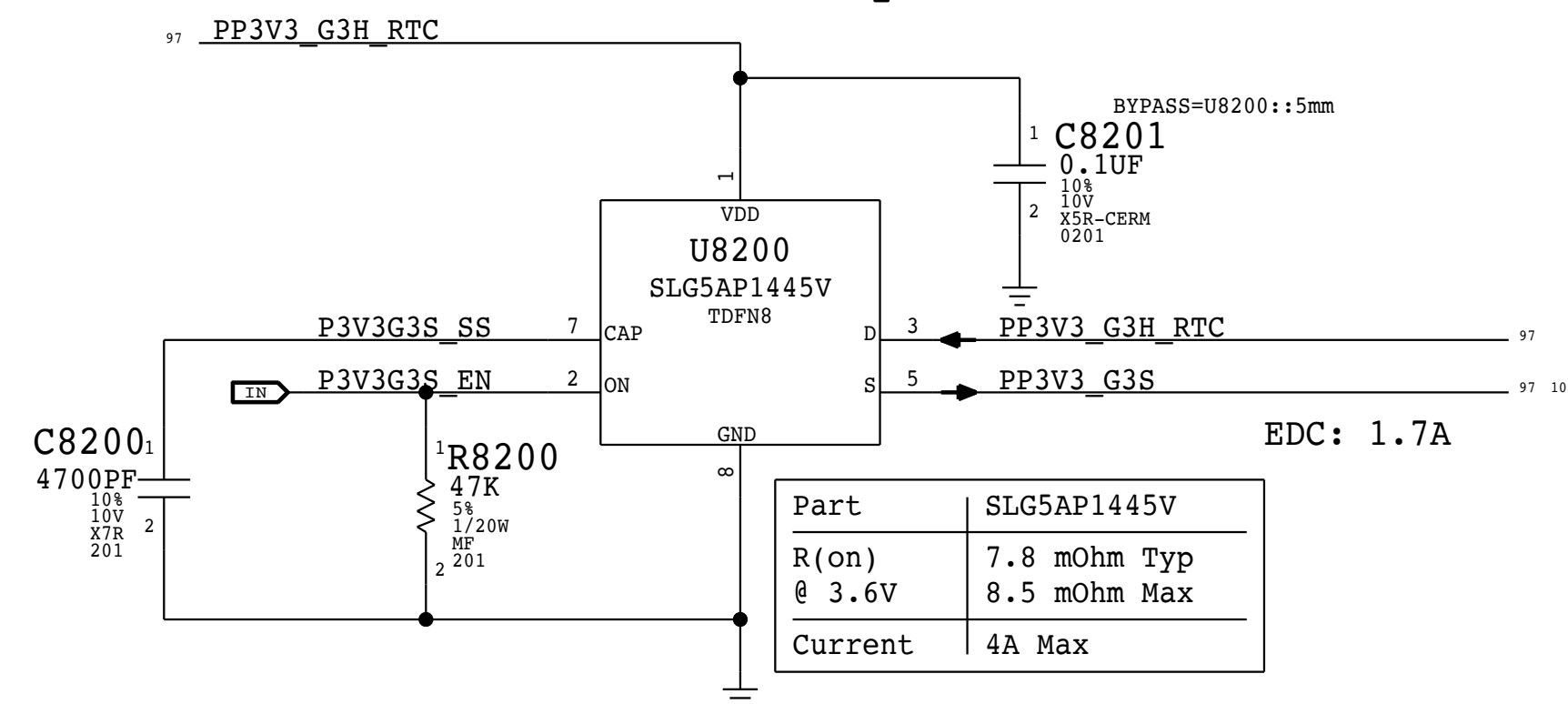
Note: Load switches may be larger than necessary

System Power States

System State:	Shutdown (G3H)		Standby (G3S)		Standby (S4)		Sleep (S0i/S3)		Run (S0)
	CPU/PCH State:		CPU/PCH State:		CPU/PCH State:		CPU/PCH State:		CPU/PCH State:
Rails	SoC State:	S2R	Awake	S2R	Awake	S2R	Awake	S2R	Awake
PP*_S2R (0.8,1.1,1.8V)	Off	Off	On	On	On	On	On	On	On
PP*_DDR (0.8,0.9,1.1V)	Off	Off	On	On	Off	On	Off	On	On
PP*_AWAKE (CPU,SRAM,1.2,1.8,3.3V)	Off	Off	On	On	Off	On	Off	On	On
PP3V3_G3H (VR1)	On	On	On	On	On	On	On	On	On
PP*_G3S (1.8,3.3,5V)	Off	On	On	On	On	On	On	On	On
PP*_S5 (1.8,3.3V)	Off	Off	Off	Off	On	On	On	On	On
CPU/PCH VRS	Off	Off	Off	Off	Off/On	Off/On	Off/On	Off/On	On

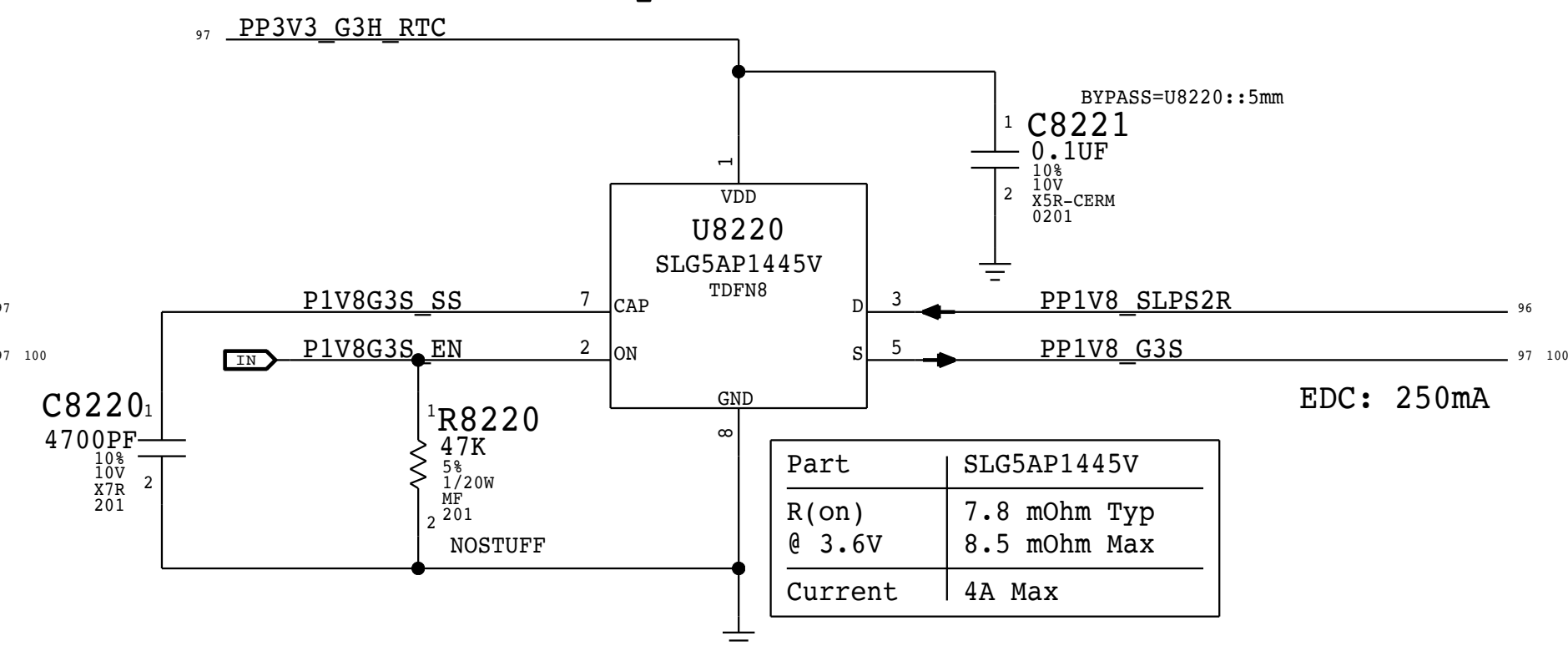
* System: Shutdown Awake is a transition state only.
 * SoC: SLP_DDR is a transition state only.
 * CPU/PCH: S4 is only used by desktops for USB wakes.
 * CPU/PCH: S5 is a transition state. May also be used for RTC wakes.

3.3V G3 Standby Switch



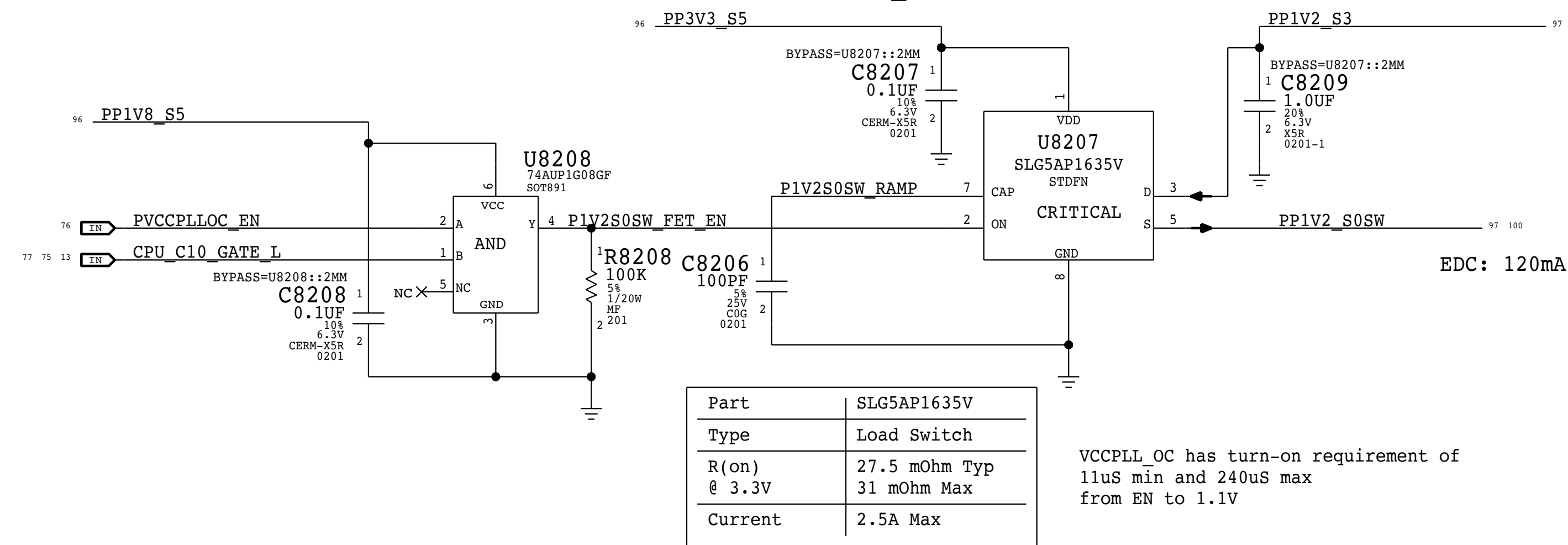
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

1.8V G3 Standby Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

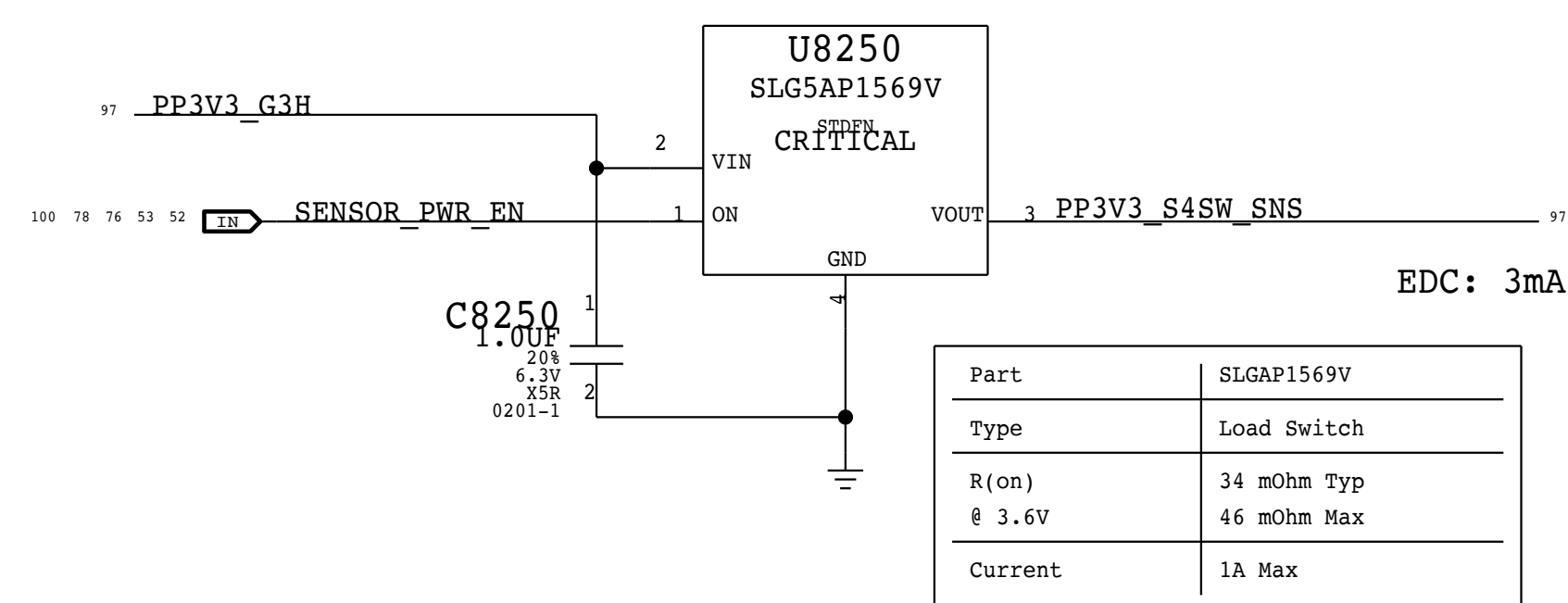
1.2V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.3V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

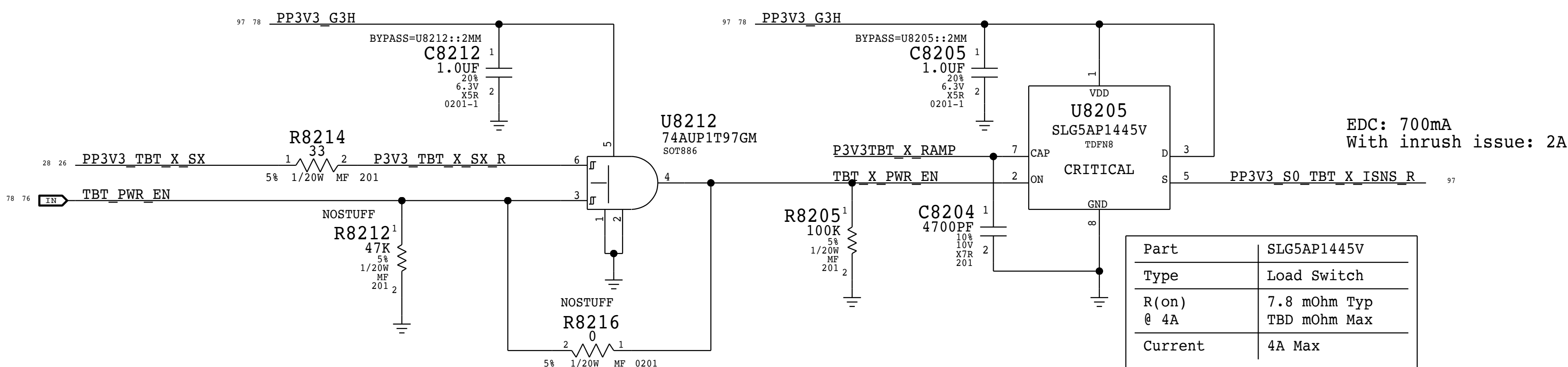
VCCPLL_OC has turn-on requirement of 11uS min and 240uS max from EN to 1.1V

3.3V Sensor Switch



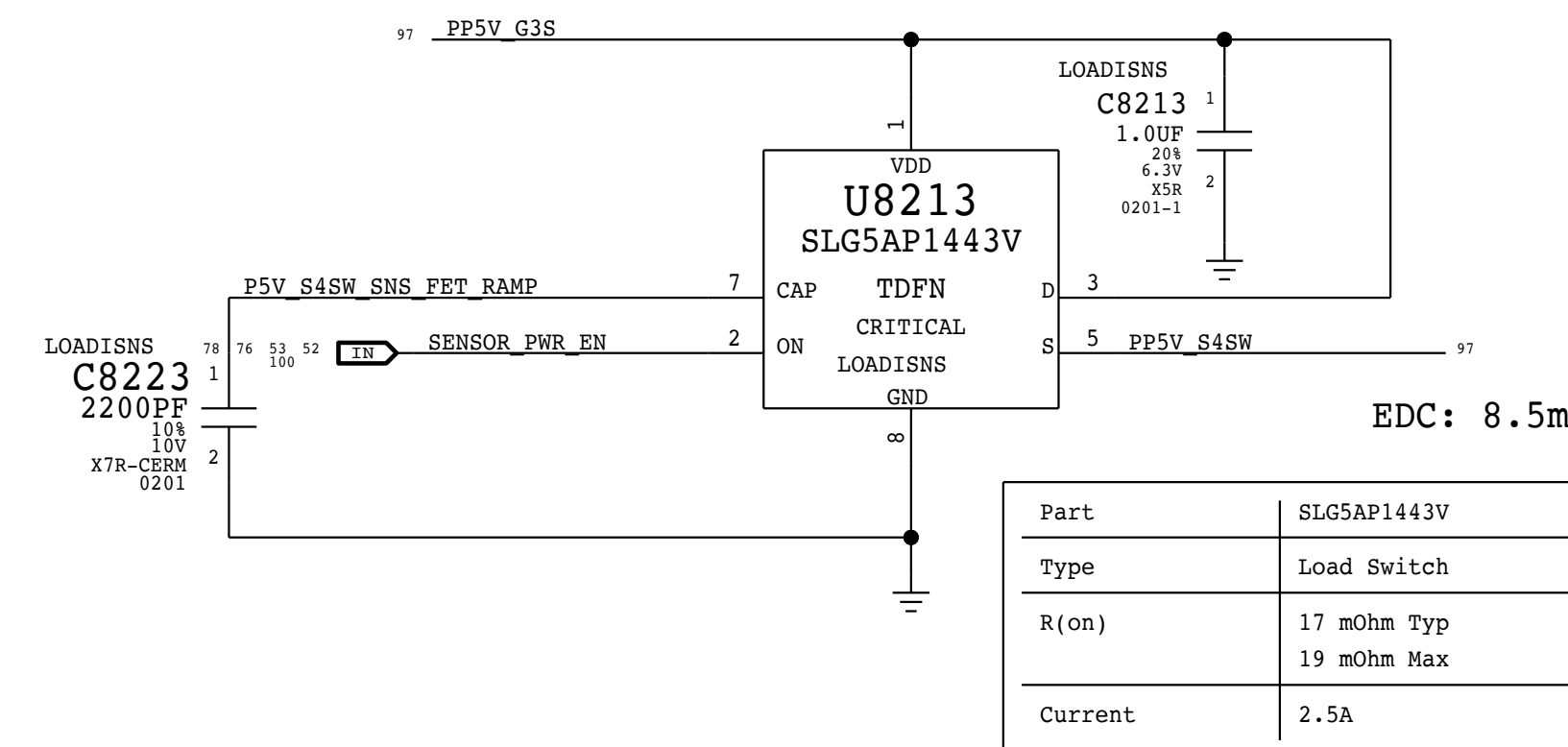
Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

3.3V S0SW TBT X Switch



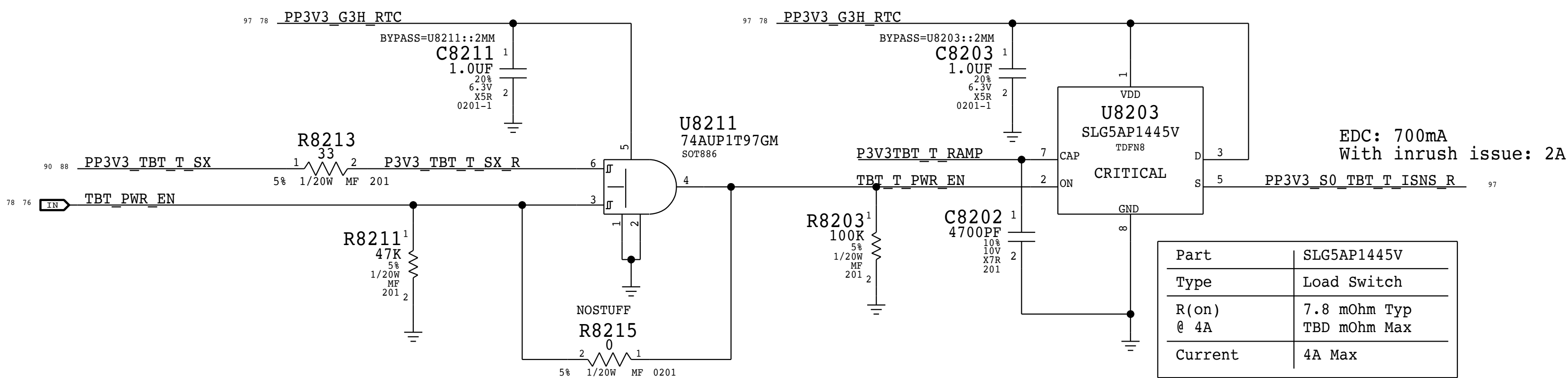
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

5V Sensor Switch



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 4A	17 mOhm Typ 19 mOhm Max
Current	2.5A

3.3V S0SW TBT T Switch



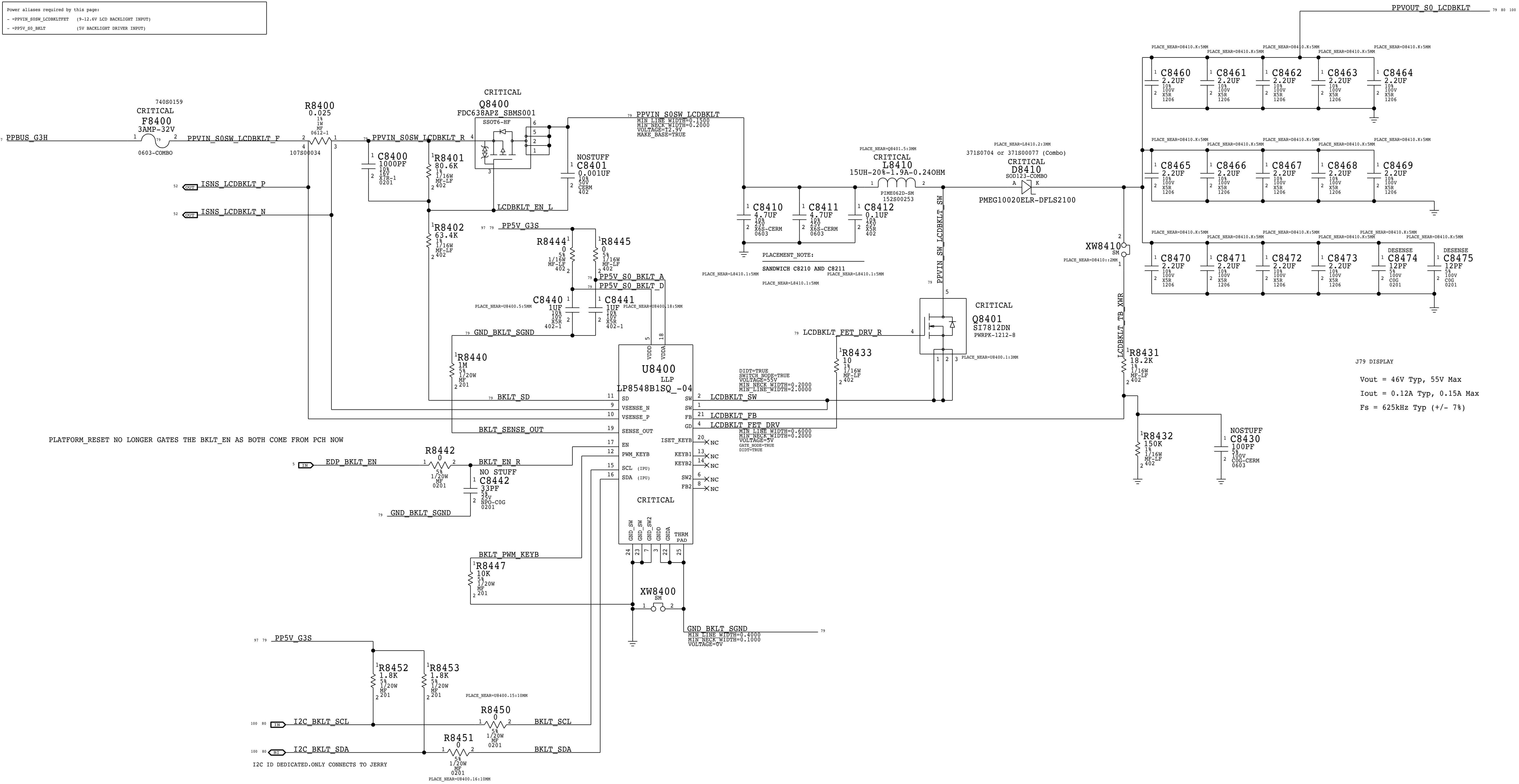
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE		DRAWING NUMBER		SIZE
Power FETs		051-02166		D
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Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

J79 DISPLAY
Vout = 46V Typ, 55V Max
Iout = 0.12A Typ, 0.15A Max
Fs = 625kHz Typ (+/- 7%)

LINE WIDTHS

- PP5V_S0_BKLT_A: MIN LINE WIDTH=2.0000, MIN NECK WIDTH=0.2000, VOLTAGE=5V
- PP5V_S0_BKLT_D: MIN LINE WIDTH=2.0000, MIN NECK WIDTH=0.2000, VOLTAGE=5V
- BKLT_SD: MIN LINE WIDTH=0.2500, MIN NECK WIDTH=0.2000

PBUS LINE WIDTHS

- PPVIN_S0SW_LCDBKLT_F: MIN LINE WIDTH=2.0000, MIN NECK WIDTH=0.2000, VOLTAGE=12.5V
- PPVIN_S0SW_LCDBKLT_R: MIN LINE WIDTH=2.0000, MIN NECK WIDTH=0.2000, VOLTAGE=12.5V
- PPVIN_S0SW_LCDBKLT: MIN LINE WIDTH=0.1500, MIN NECK WIDTH=0.2000, VOLTAGE=12.5V

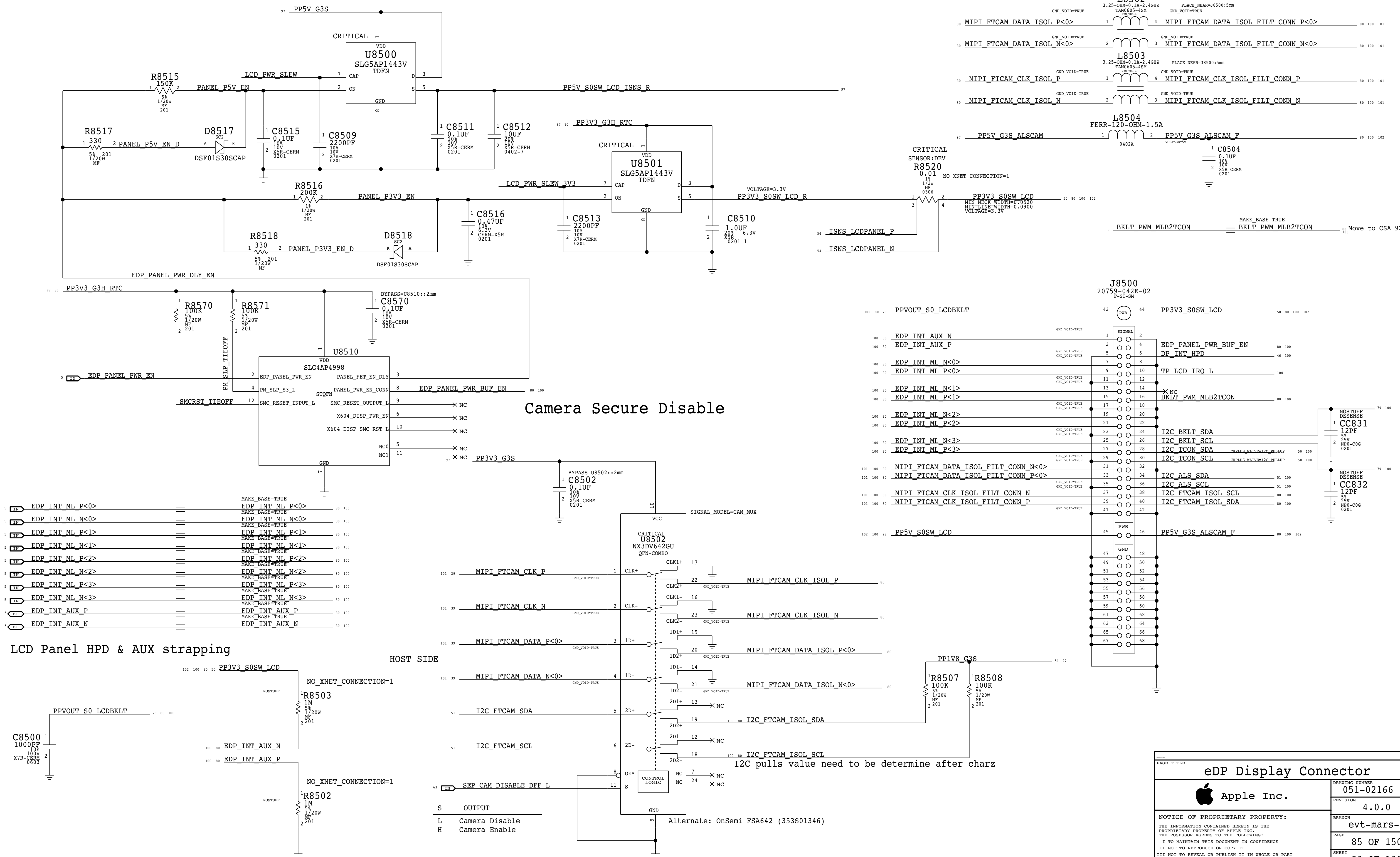
LCD BKLT LINE WIDTHS

- LCDBKLT_FET_DRV_R: MIN LINE WIDTH=0.6000, MIN NECK WIDTH=0.2000, VOLTAGE=5V
- PPVIN_SW_LCDBKLT_SW: MIN LINE WIDTH=2.0000, MIN NECK WIDTH=0.2000, VOLTAGE=5V
- PPVOUT_S0_LCDBKLT: MIN LINE WIDTH=0.5000, MIN NECK WIDTH=0.1500, VOLTAGE=55V

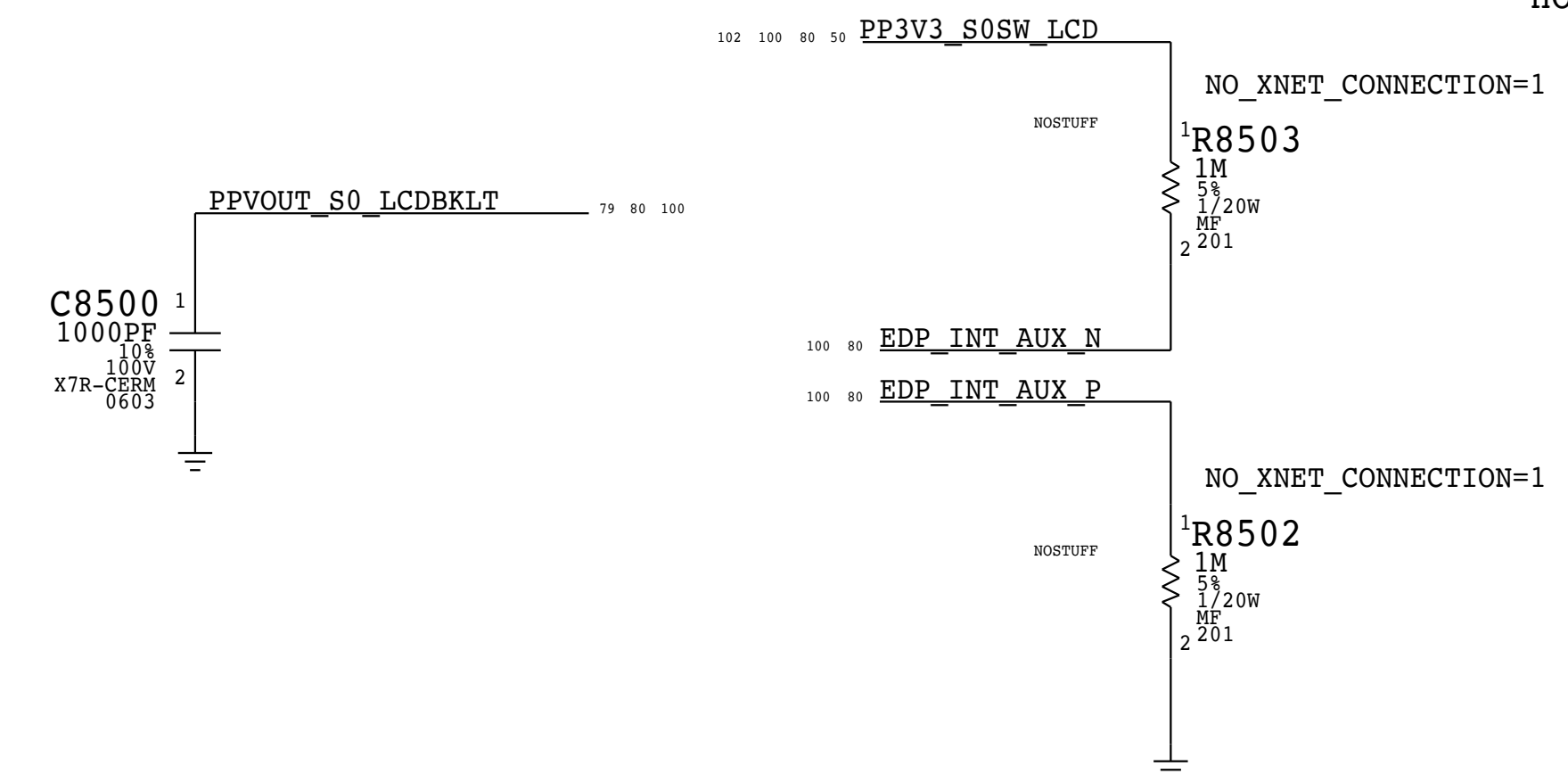
BOM_COST_GROUP=DISPLAY

PAGE TITLE LCD Backlight Driver		
DRAWING NUMBER 051-02166		SIZE D
REVISION 4.0.0		
BRANCH evt-mars-0		PAGE 84 OF 150
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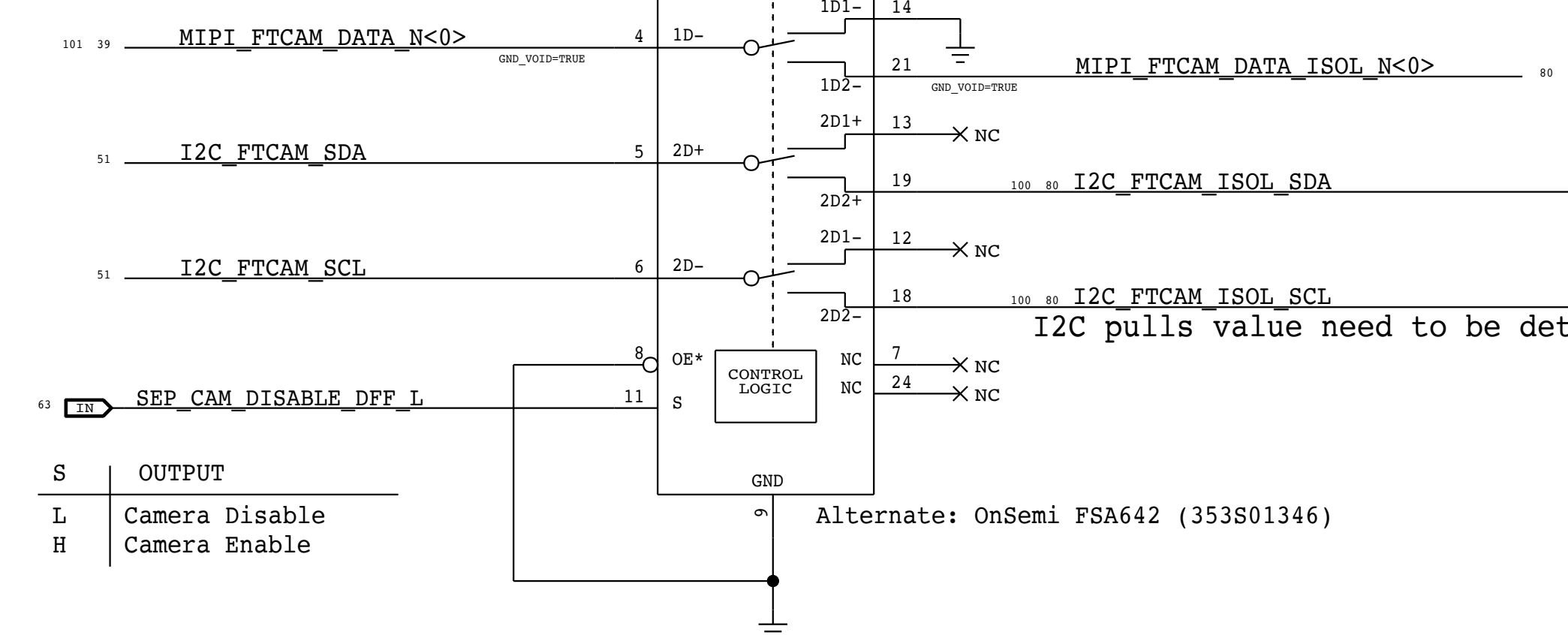
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



LCD Panel HPD & AUX strapping



HOST SIDE



S	OUTPUT
L	Camera Disable
H	Camera Enable

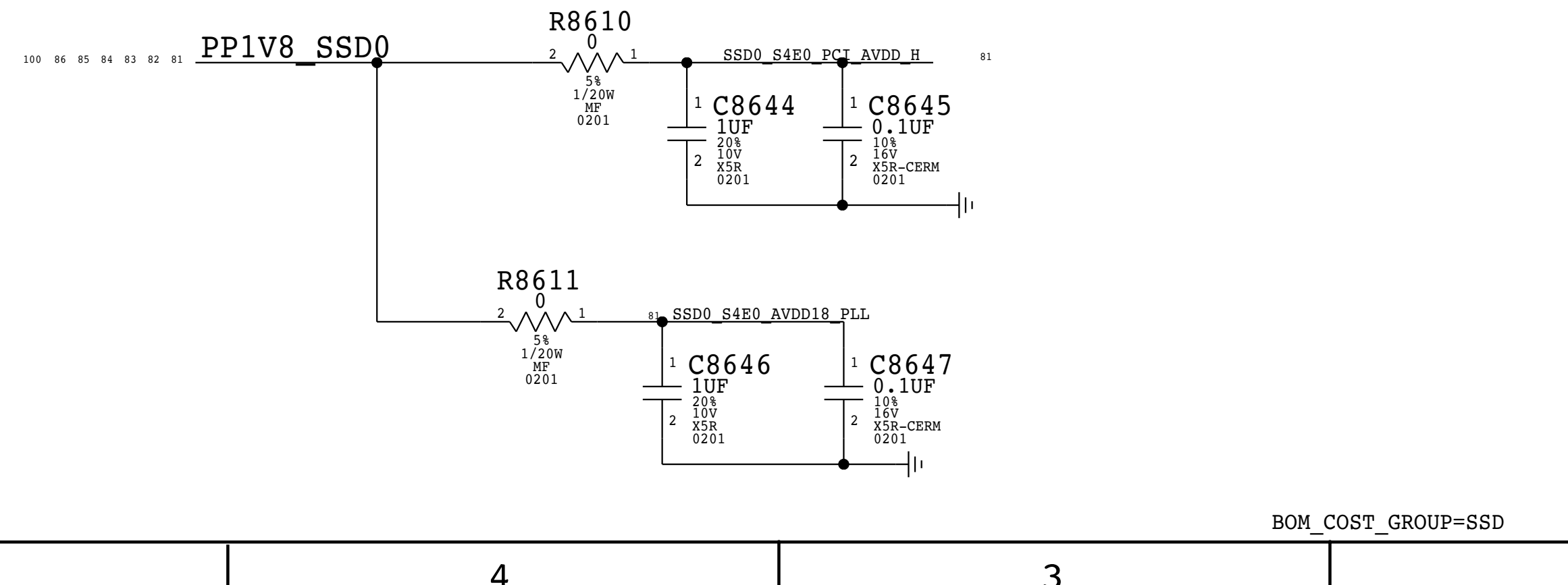
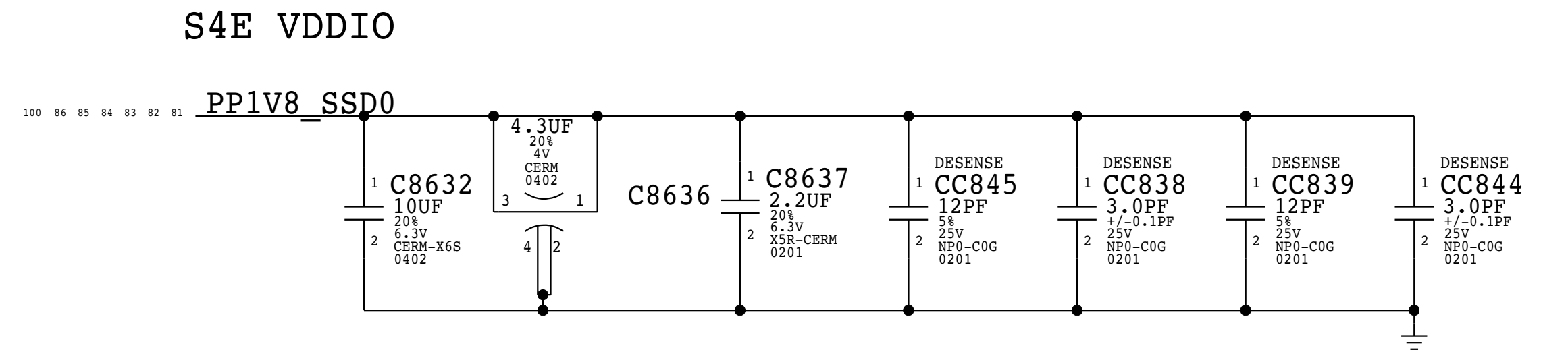
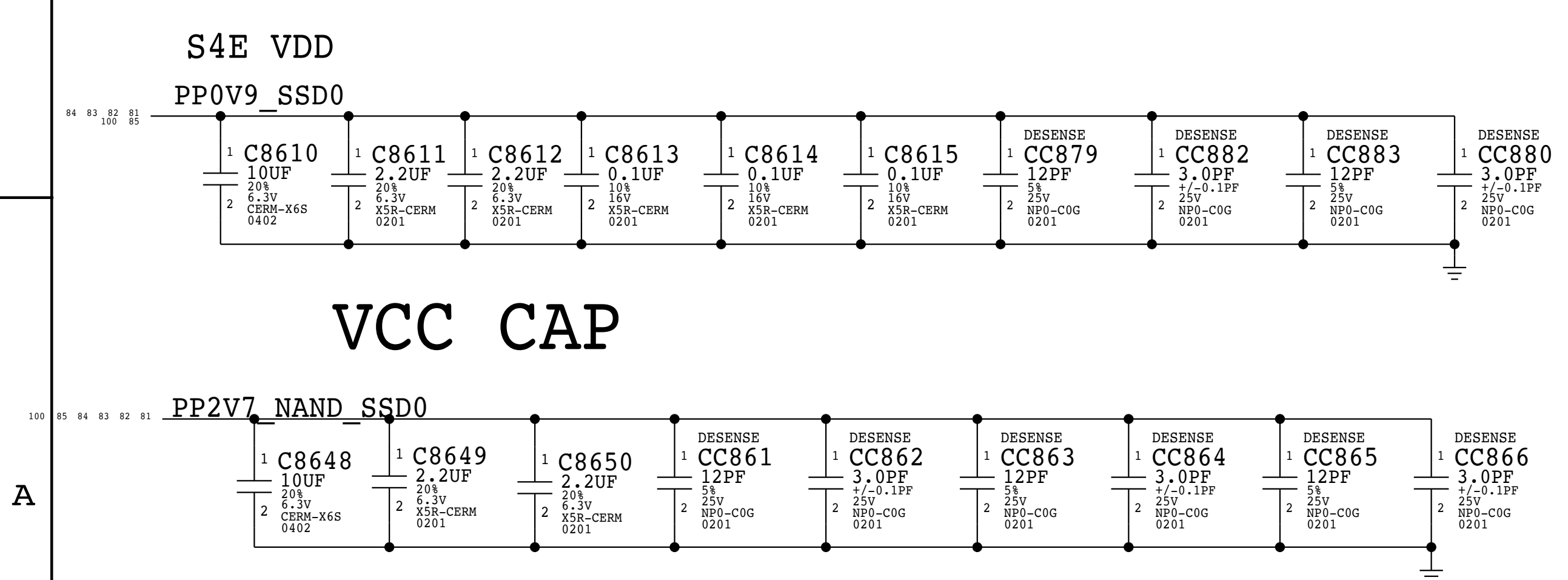
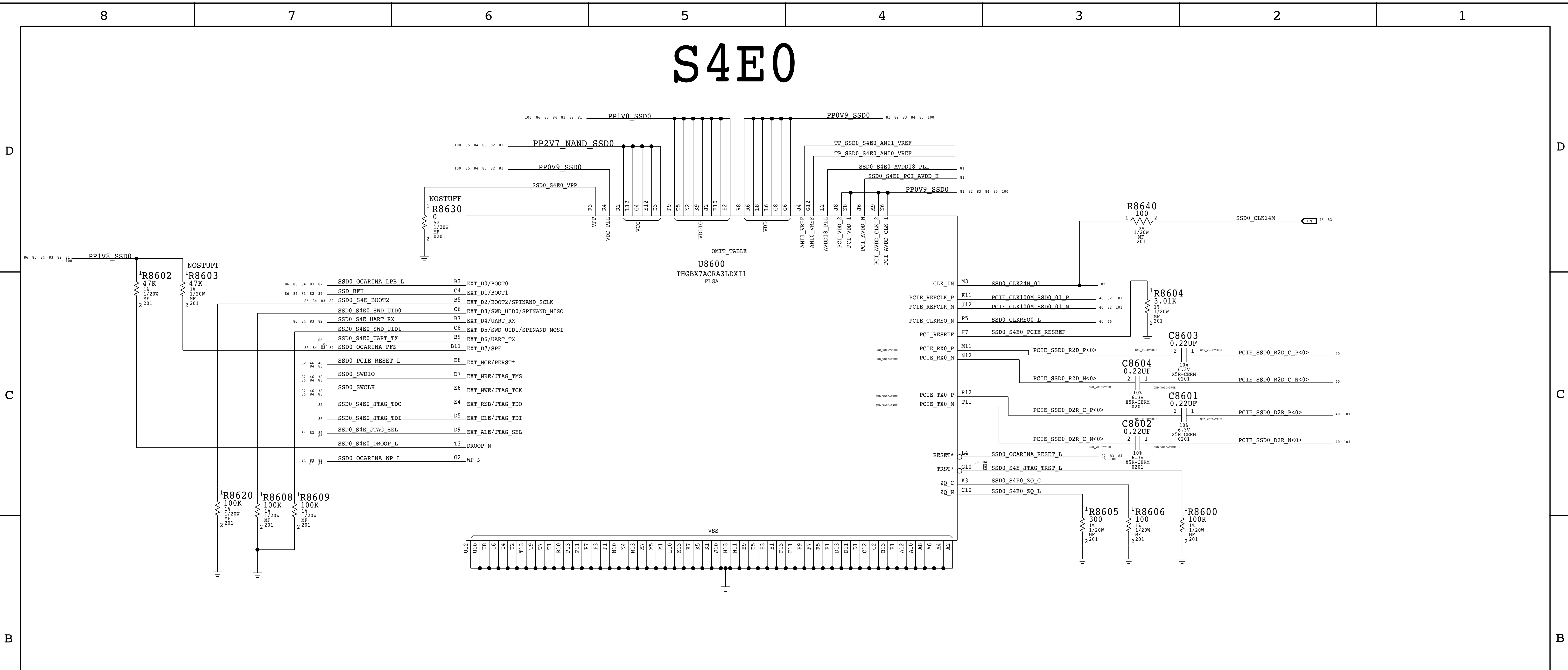
Alternate: OnSemi FSA642 (353S01346)

I2C pulls value need to be determine after charz

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eDP Display Connector		
		DRAWING NUMBER 051-02166
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		BRANCH evt-mars-0
		PAGE 85 OF 150
		SHEET 80 OF 108

BOM_COST_GROUP=DISPLAY

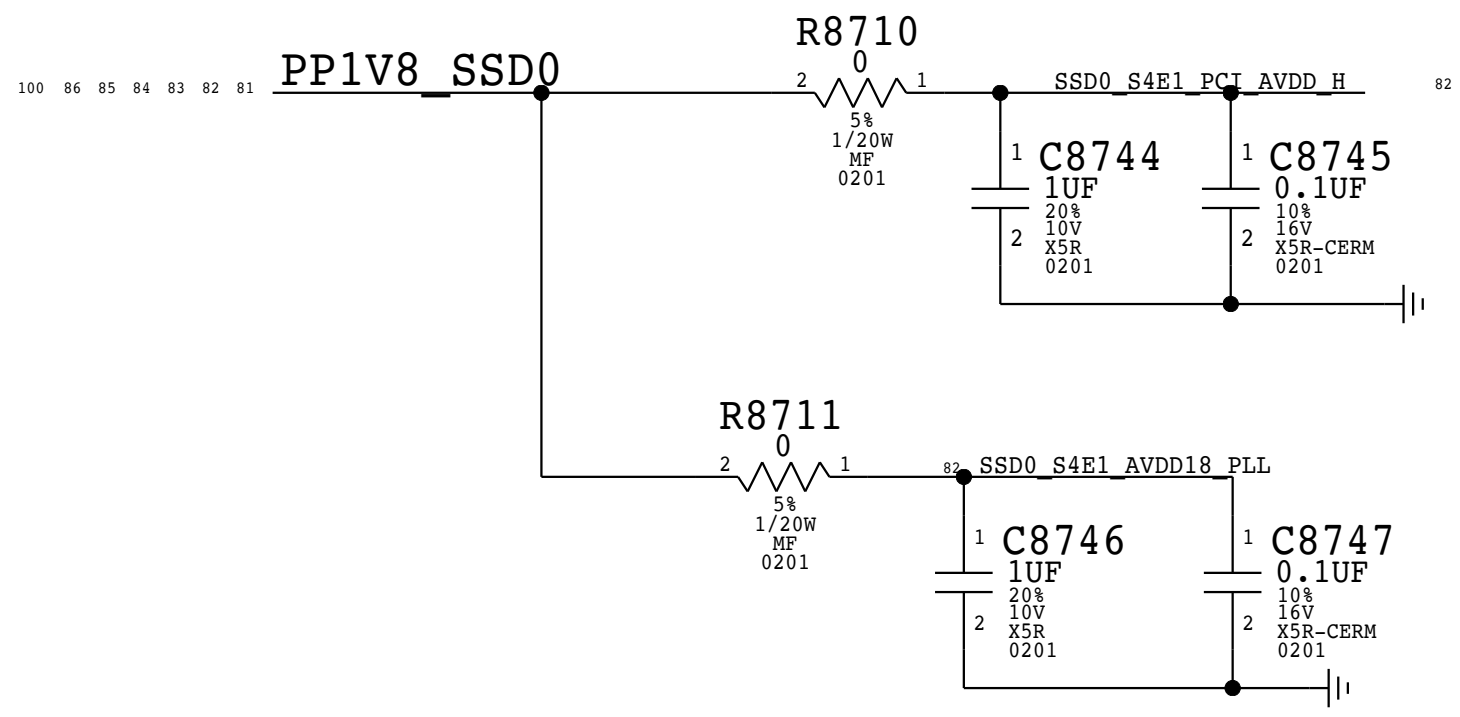
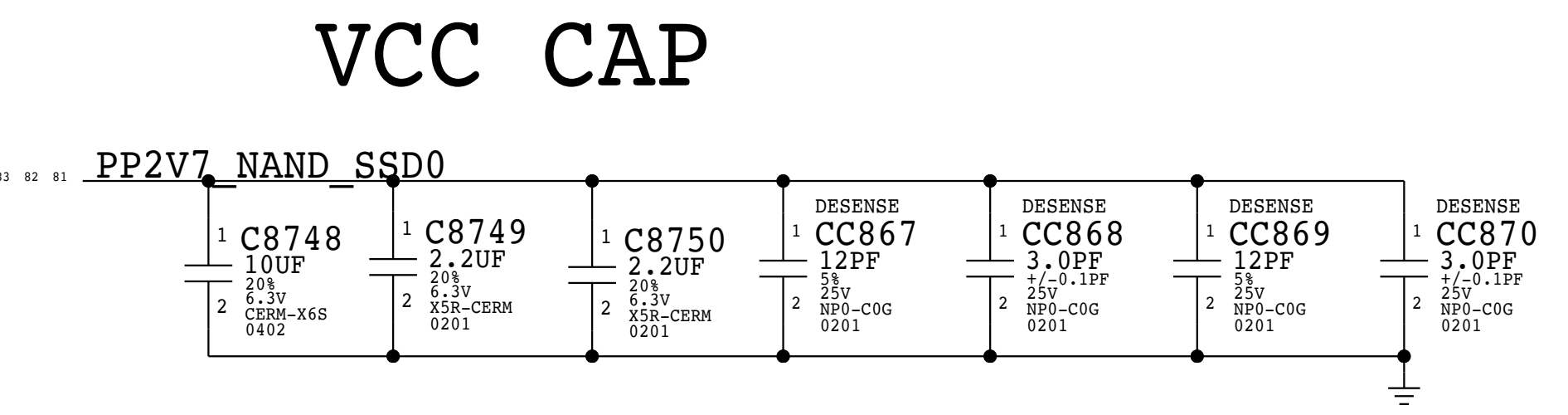
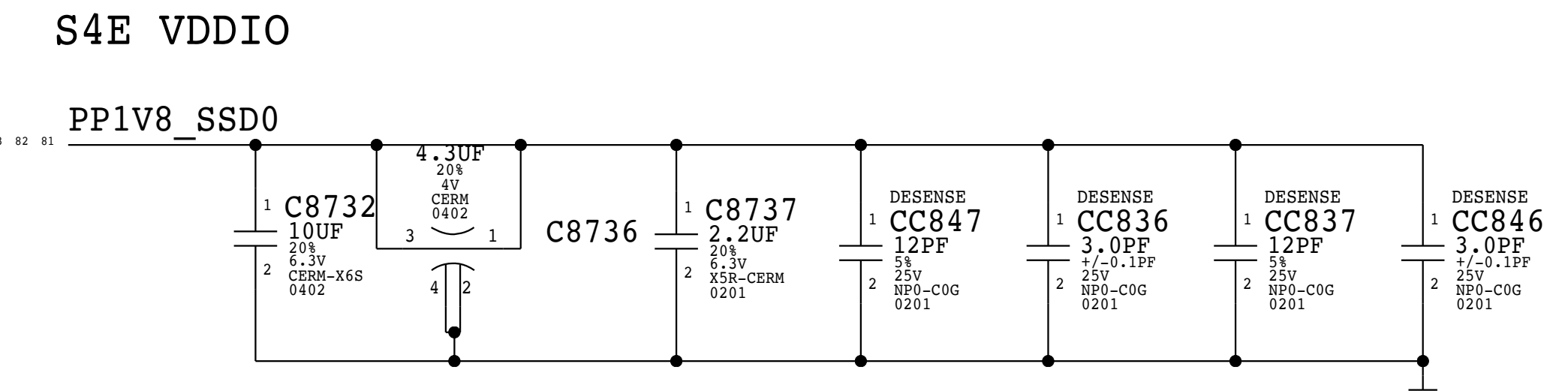
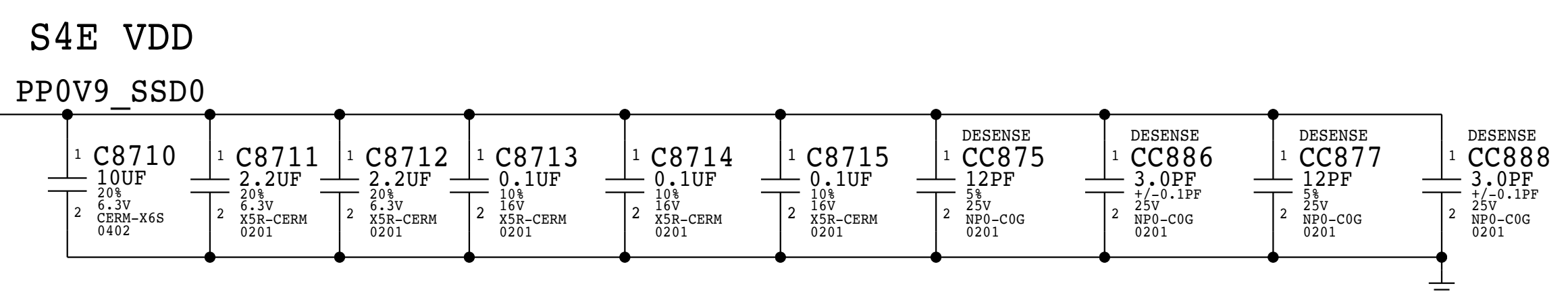
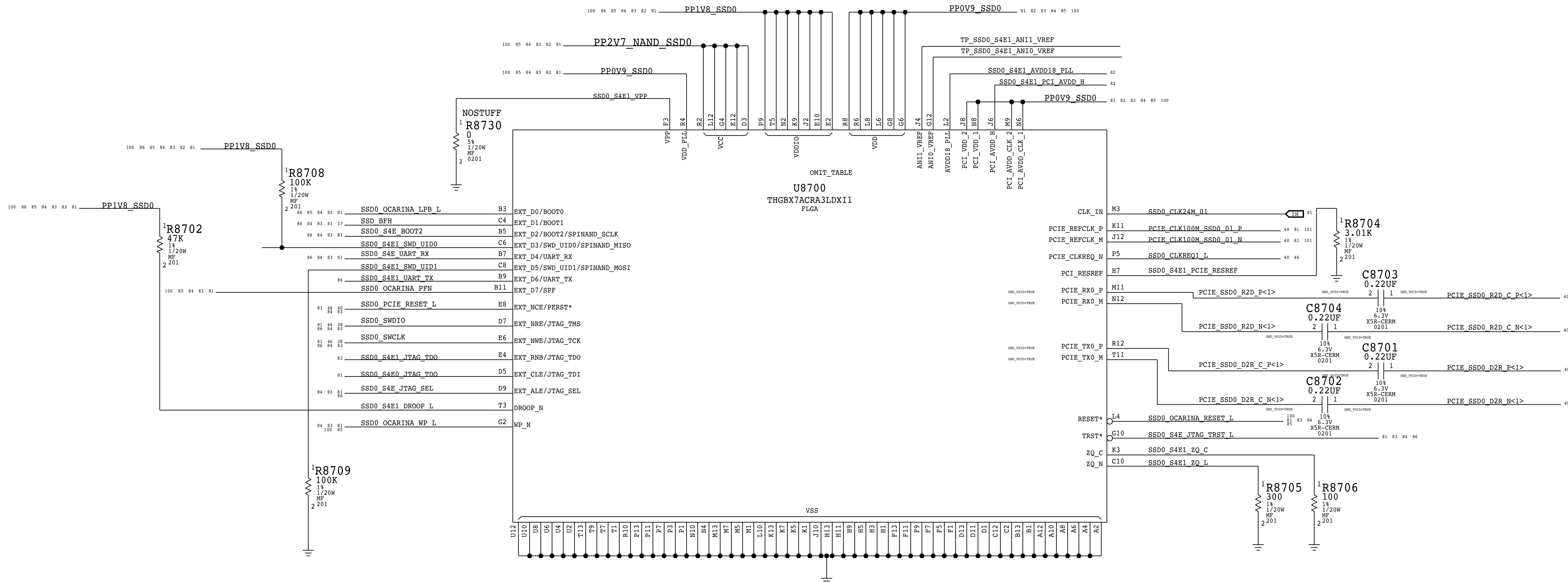
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		PAGE	86 OF 150
		SHEET	81 OF 108

BOM_COST_GROUP=SSD

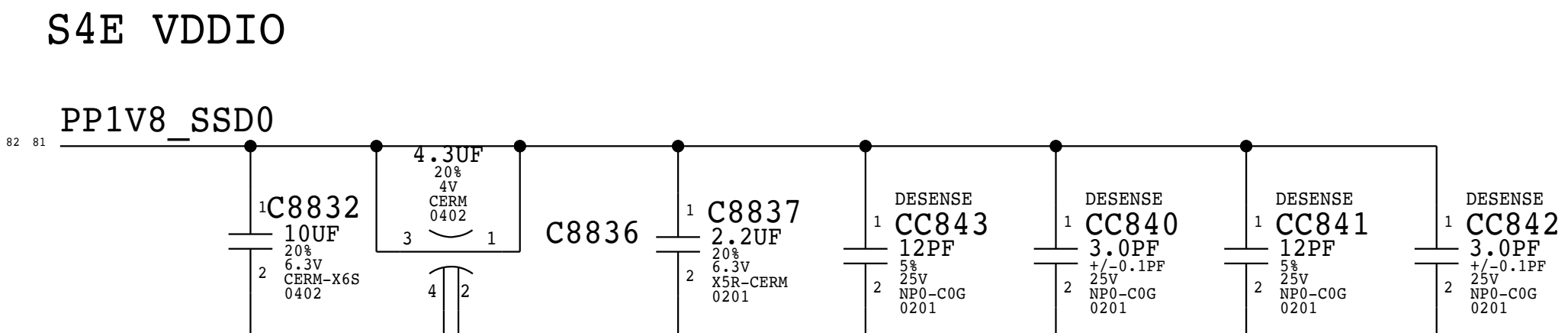
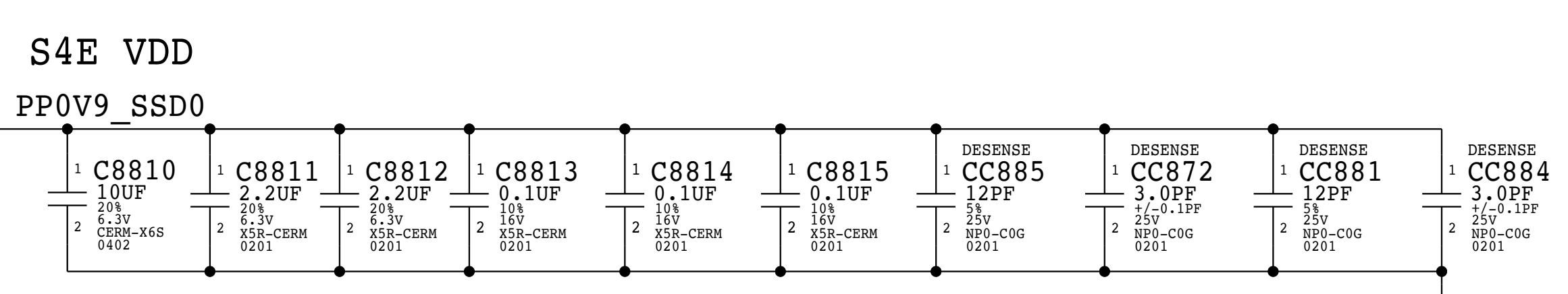
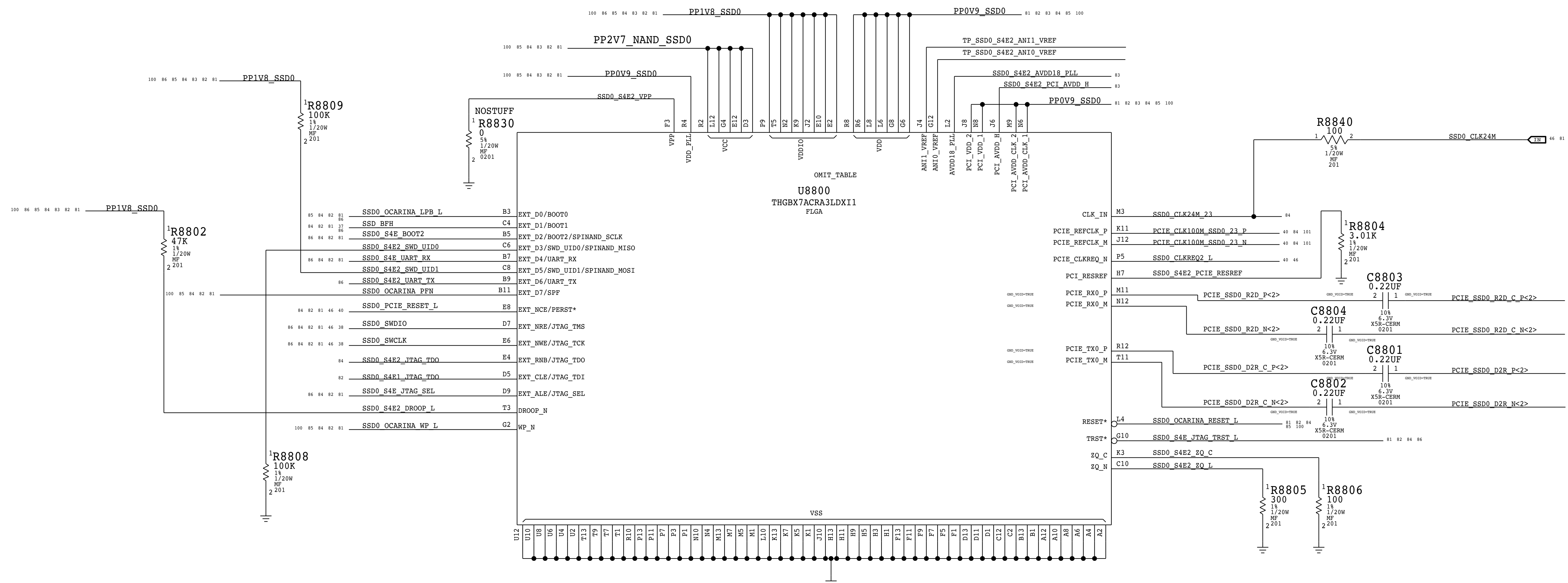
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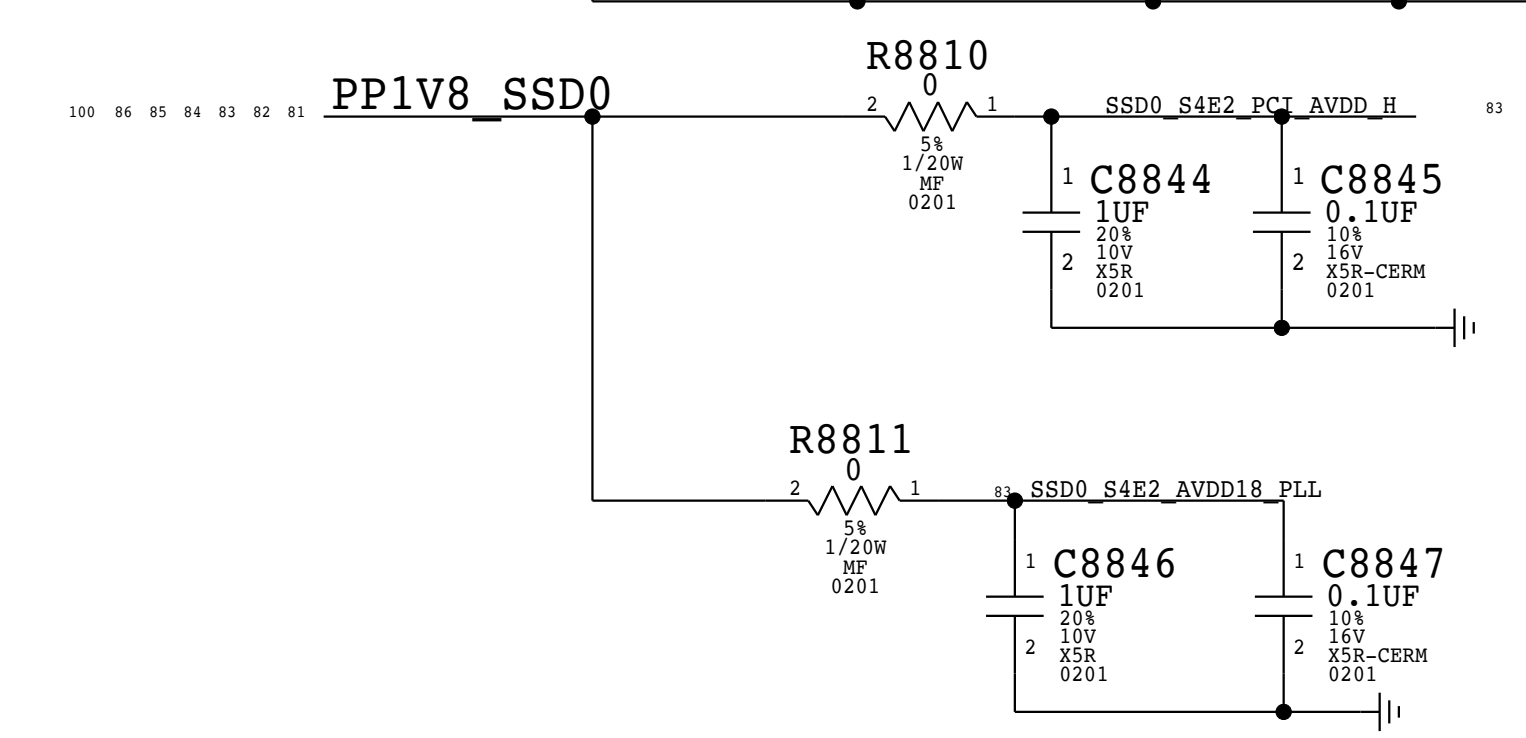
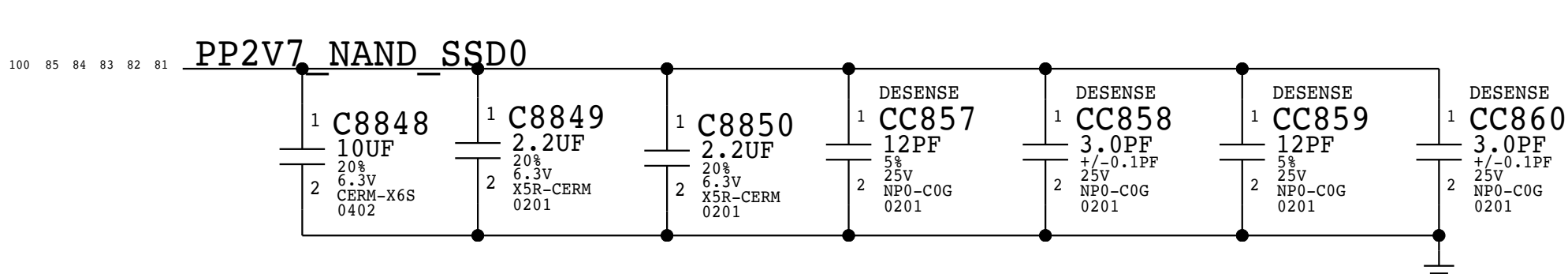
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	PAGE	87 OF 150	
	SHEET	82 OF 108	

BOM_COST_GROUP=SSD

S4E2



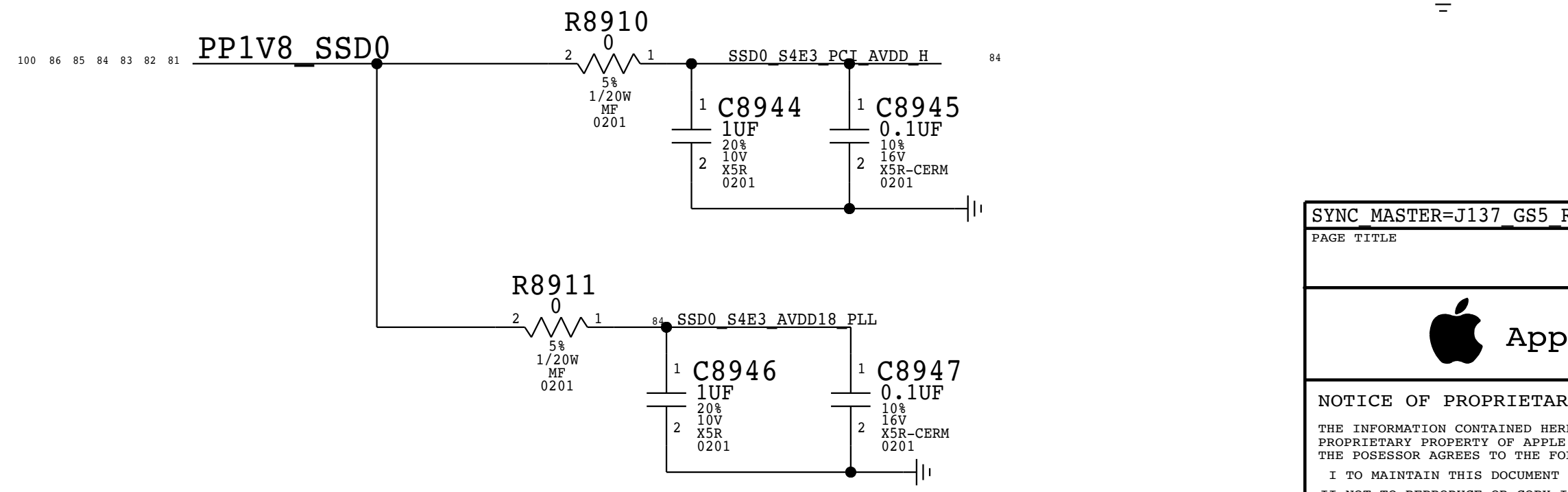
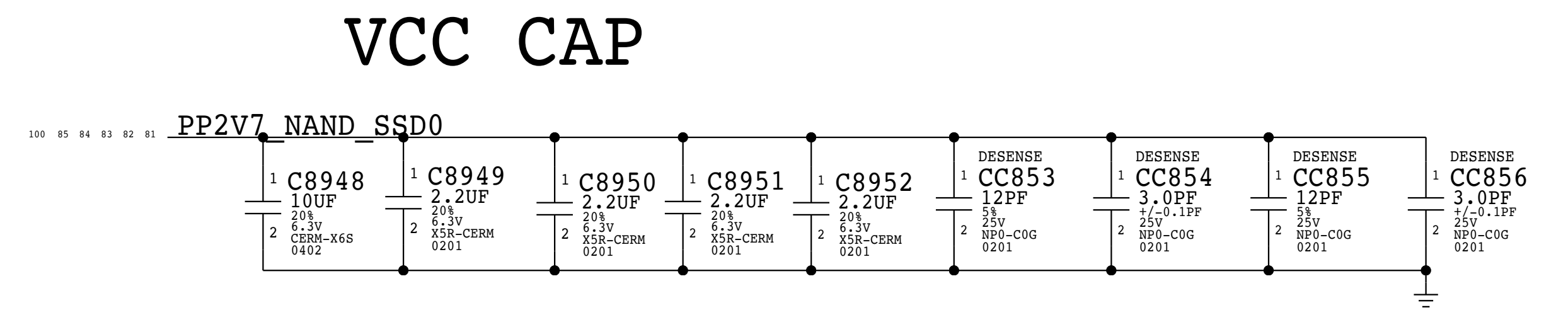
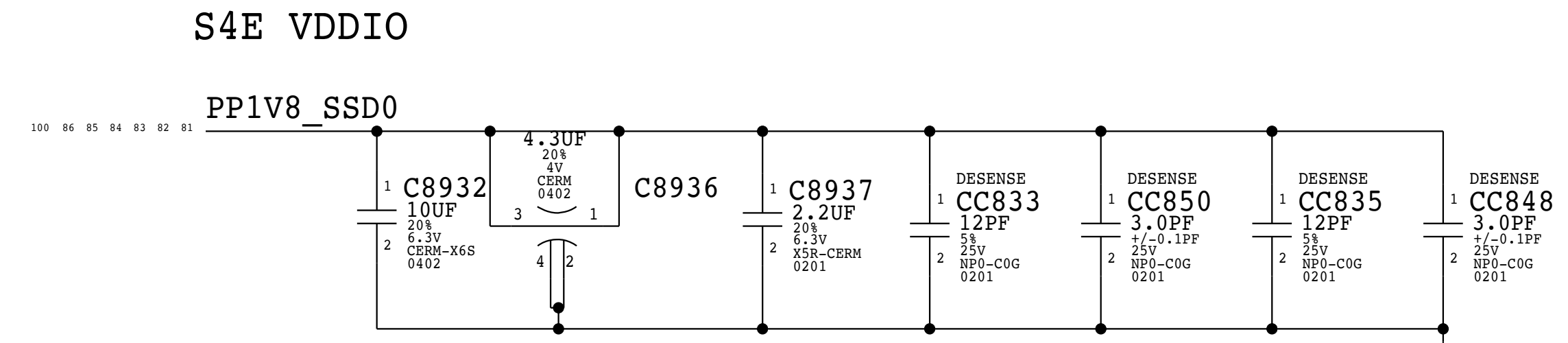
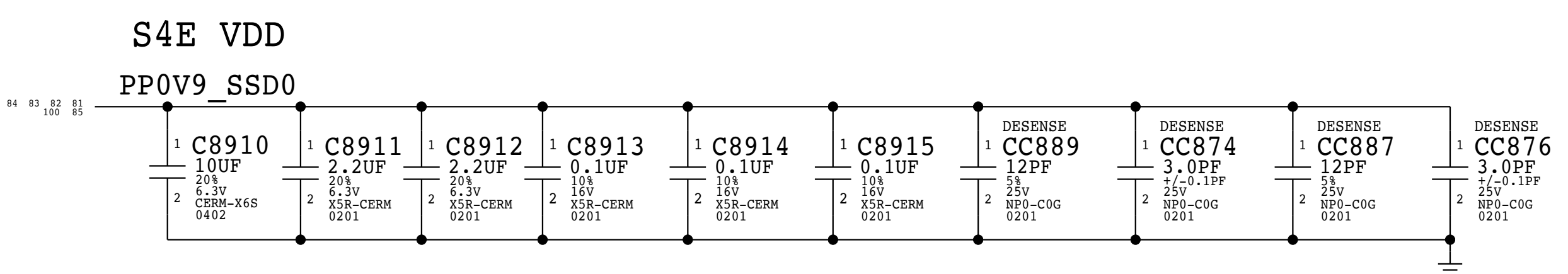
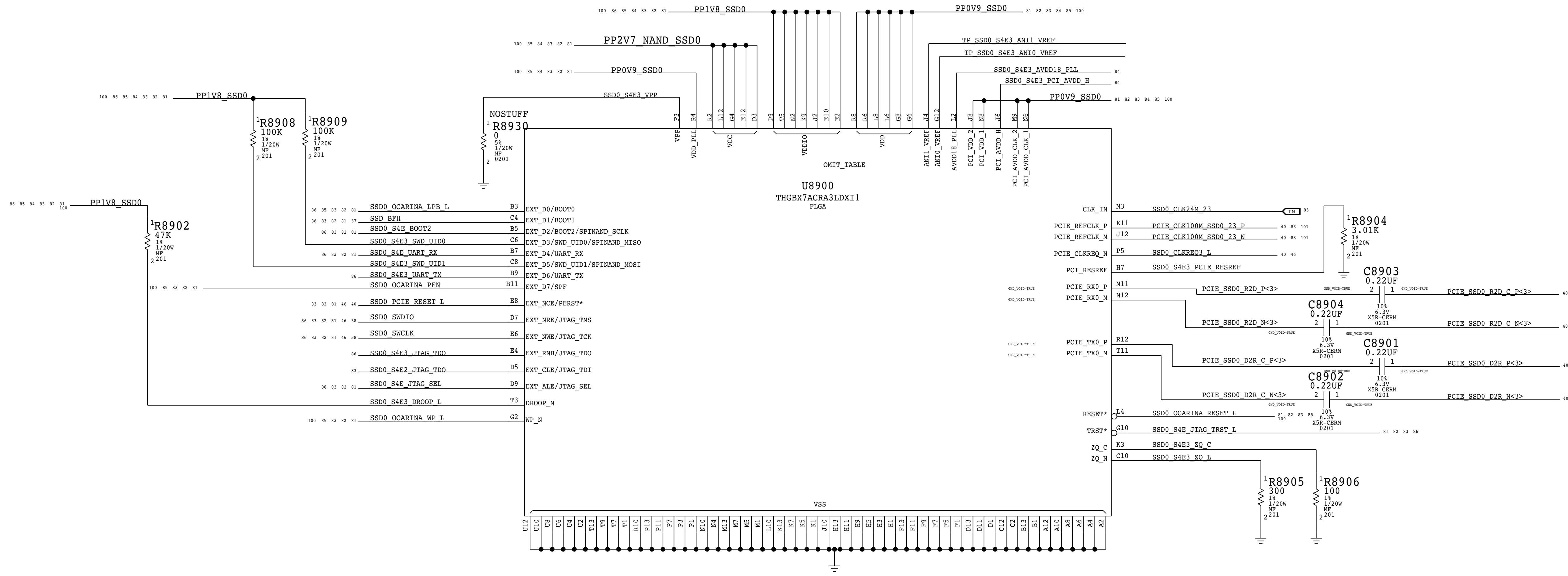
VCC CAP



SYNC MASTER=J137 GS5 REDHEAD		SYNC DATE=02/17/2017	
PAGE TITLE			
S4E<2>			
		DRAWING NUMBER	051-02166
		REVISION	4.0.0
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		PAGE	88 OF 150
		SHEET	83 OF 108

BOM_COST_GROUP=SSD

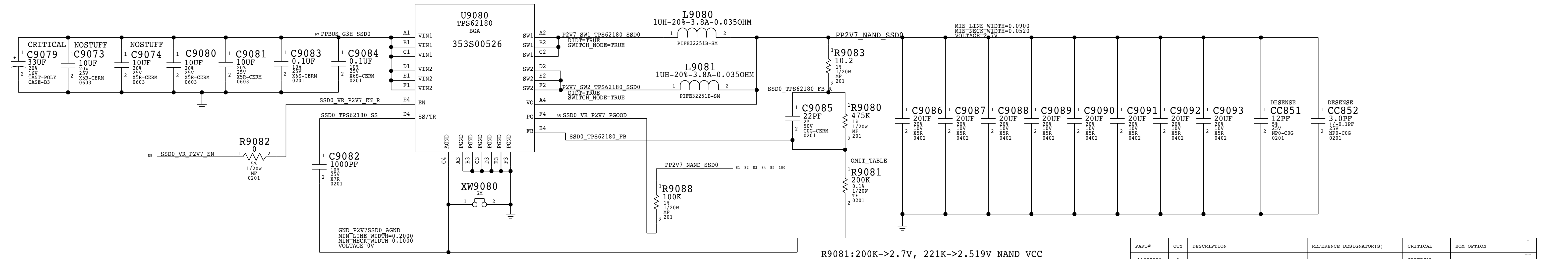
S4E3



SYNC MASTER=J137 GS5 REDHEAD		SYNC DATE=02/17/2017	
PAGE TITLE			
S4E<3>		DRAWING NUMBER	SIZE
		051-02166	D
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		BRANCH	evt-mars-0
		PAGE	89 OF 150
		SHEET	84 OF 108

BOM_COST_GROUP=SSD

D

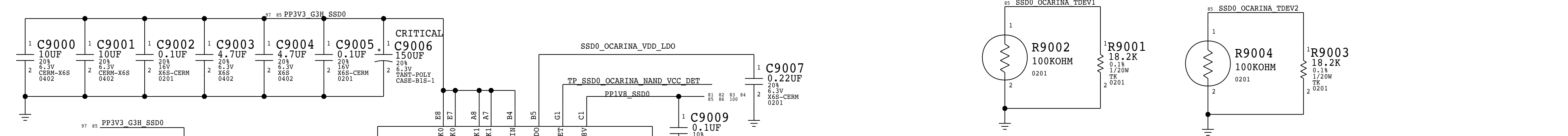


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0738	1	RES,CHIPFILM,2000HM,0.1%,1/20W,0201	R9081	CRITICAL	NAND_VCC=2.7V
103S00049	1	RES,CHIPFILM,221KOHM,0.1%,1/20W,0201	R9081	CRITICAL	NAND_VCC=2.5V

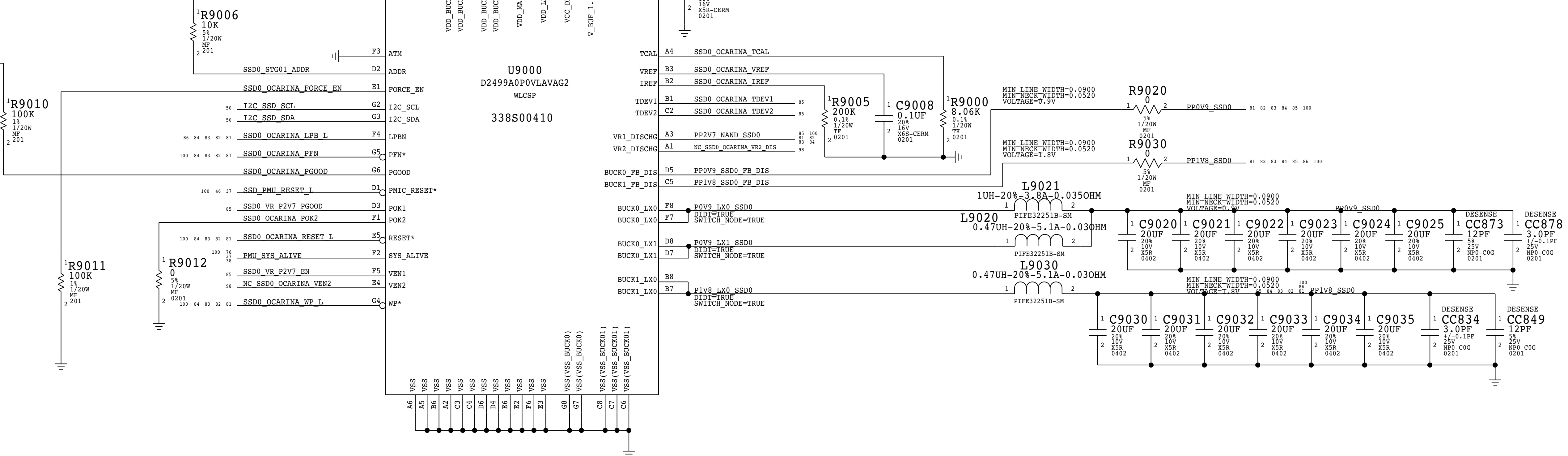
OCARINA I2C BASE ADDRESS
STG0: F2
STG1: F0

PLACE C9000-C9002 NEAR OCARINA PINS E7/E8
PLACE C9003-C9005 NEAR OCARINA PINS A7/A8
PLACE C9006 NEAR OCARINA PIN B4

C



B



A

SYNC MASTER=J137 GS5 REDHEAD SYNC DATE=02/17/2017

PAGE TITLE: OCARINA PMIC & NAND VCC VR

Apple Inc.

DRAMING NUMBER: 051-02166 SIZE: D

REVISION: 4.0.0

BRANCH: evt-mars-0

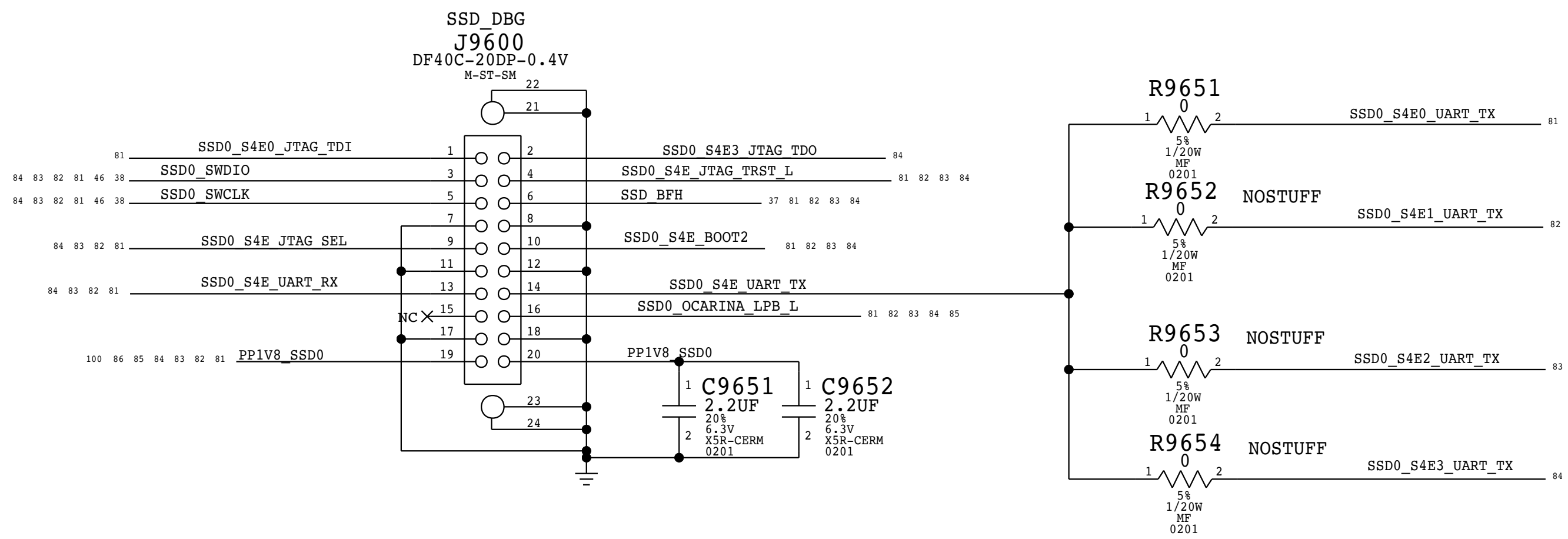
PAGE: 90 OF 150

SHEET: 85 OF 108

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BOM_COST_GROUP=SSD

SSD0



D

D

C

C

B

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A

A

SYNC MASTER=J680 MLB		SYNC DATE=03/20/2017	
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		PAGE	96 OF 150
		SHEET	86 OF 108

BOM_COST_GROUP=SSD

D

C

B

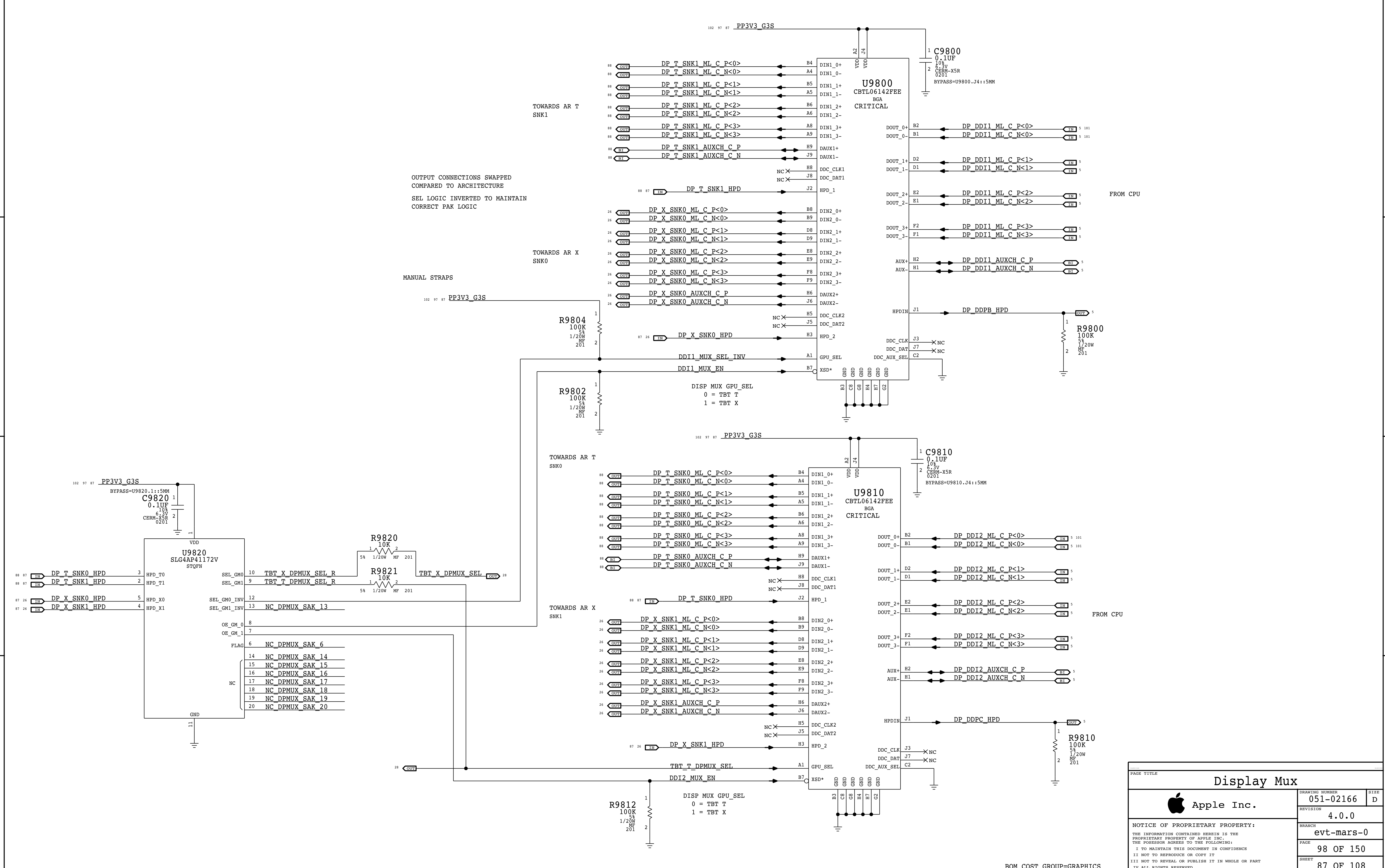
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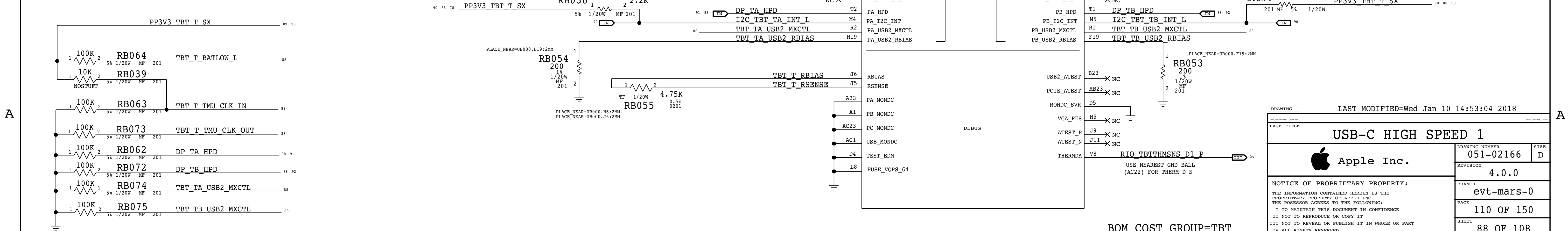
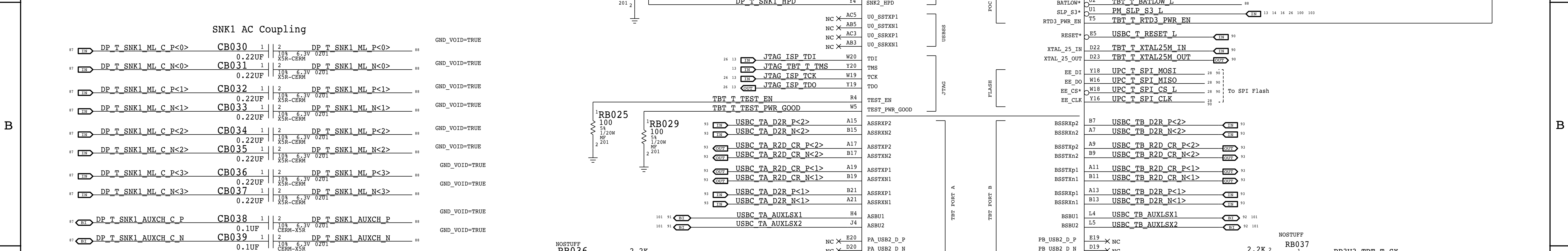
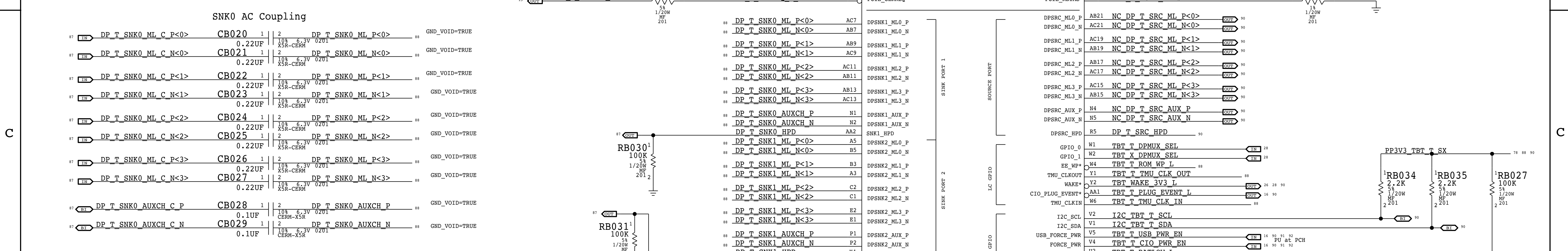
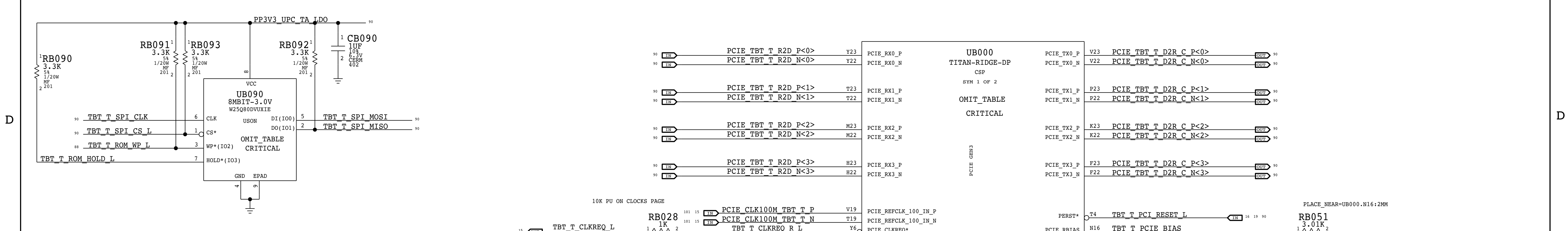
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BOM_COST_GROUP=GRAPHICS

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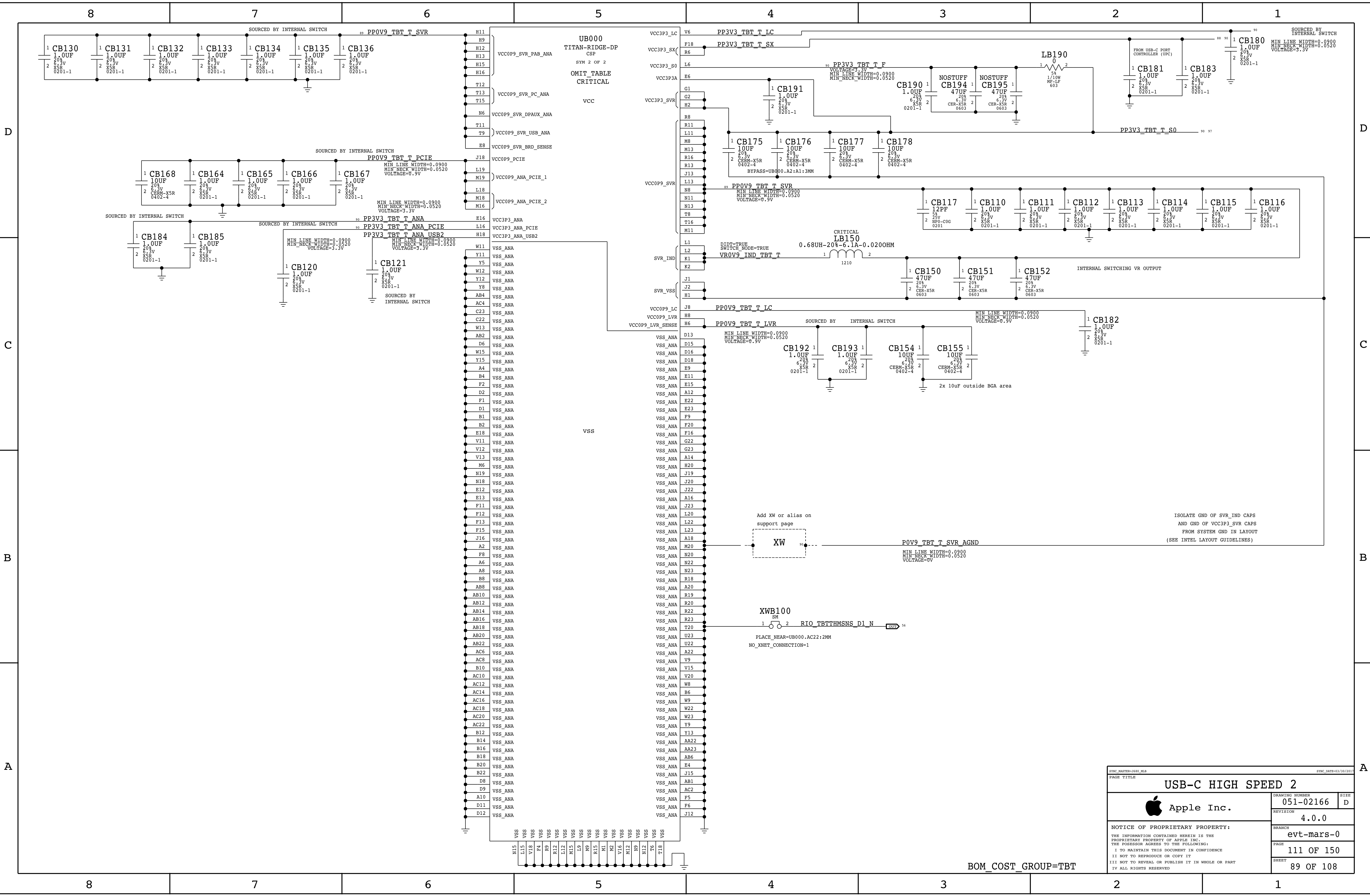
PAGE TITLE **USB-C HIGH SPEED 1**

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REVISION	4.0.0	BRANCH	evt-mars-0
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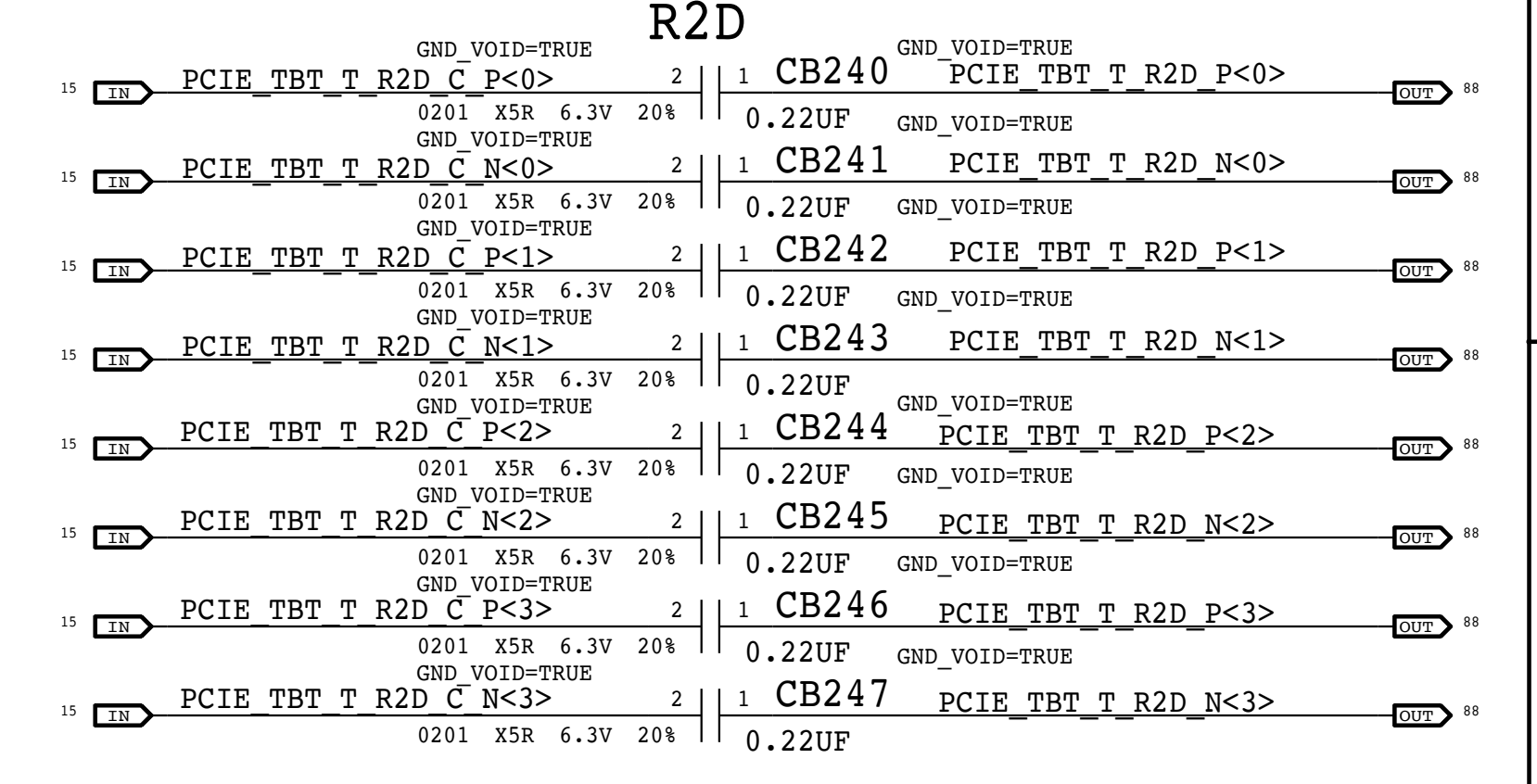
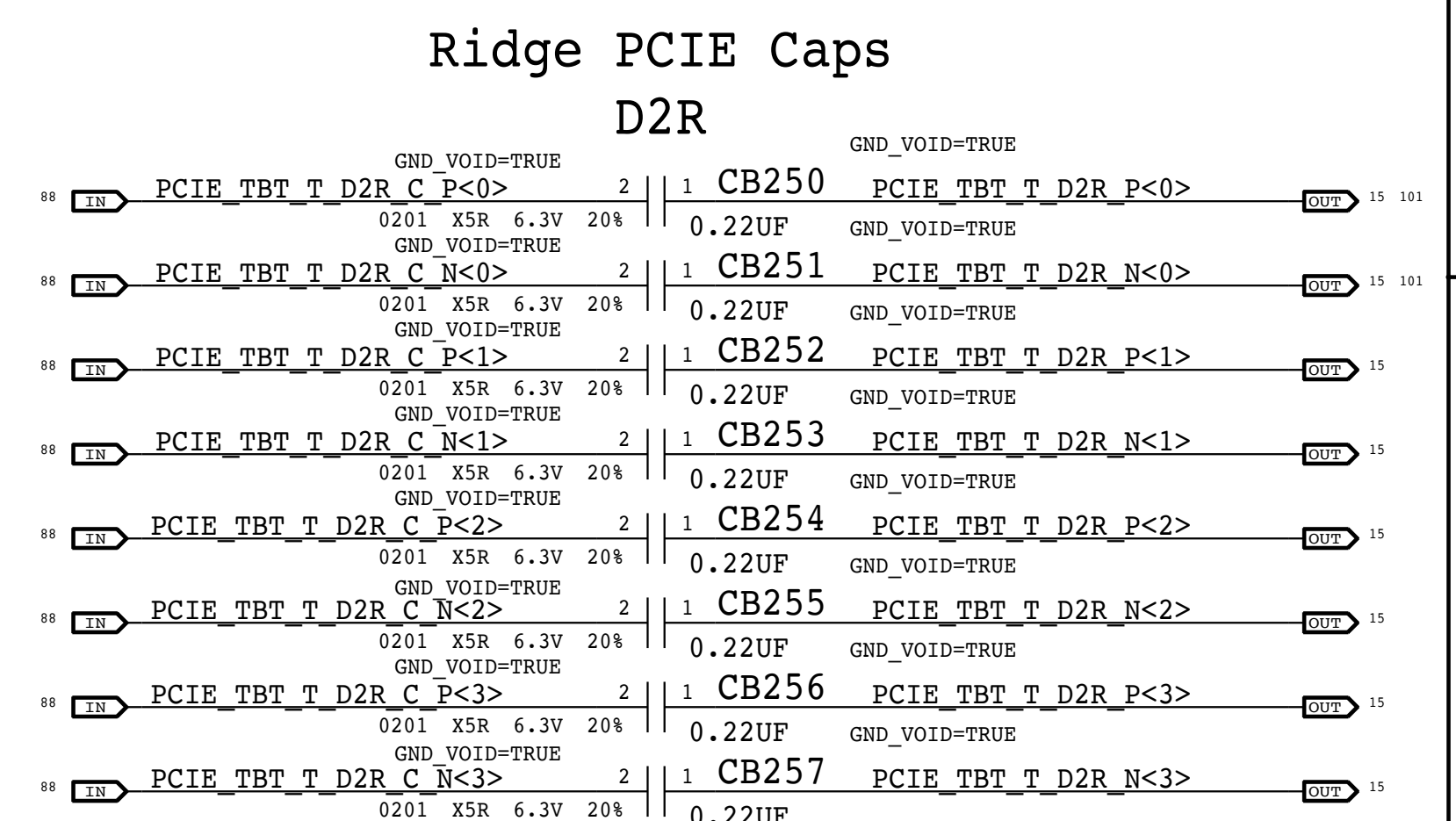
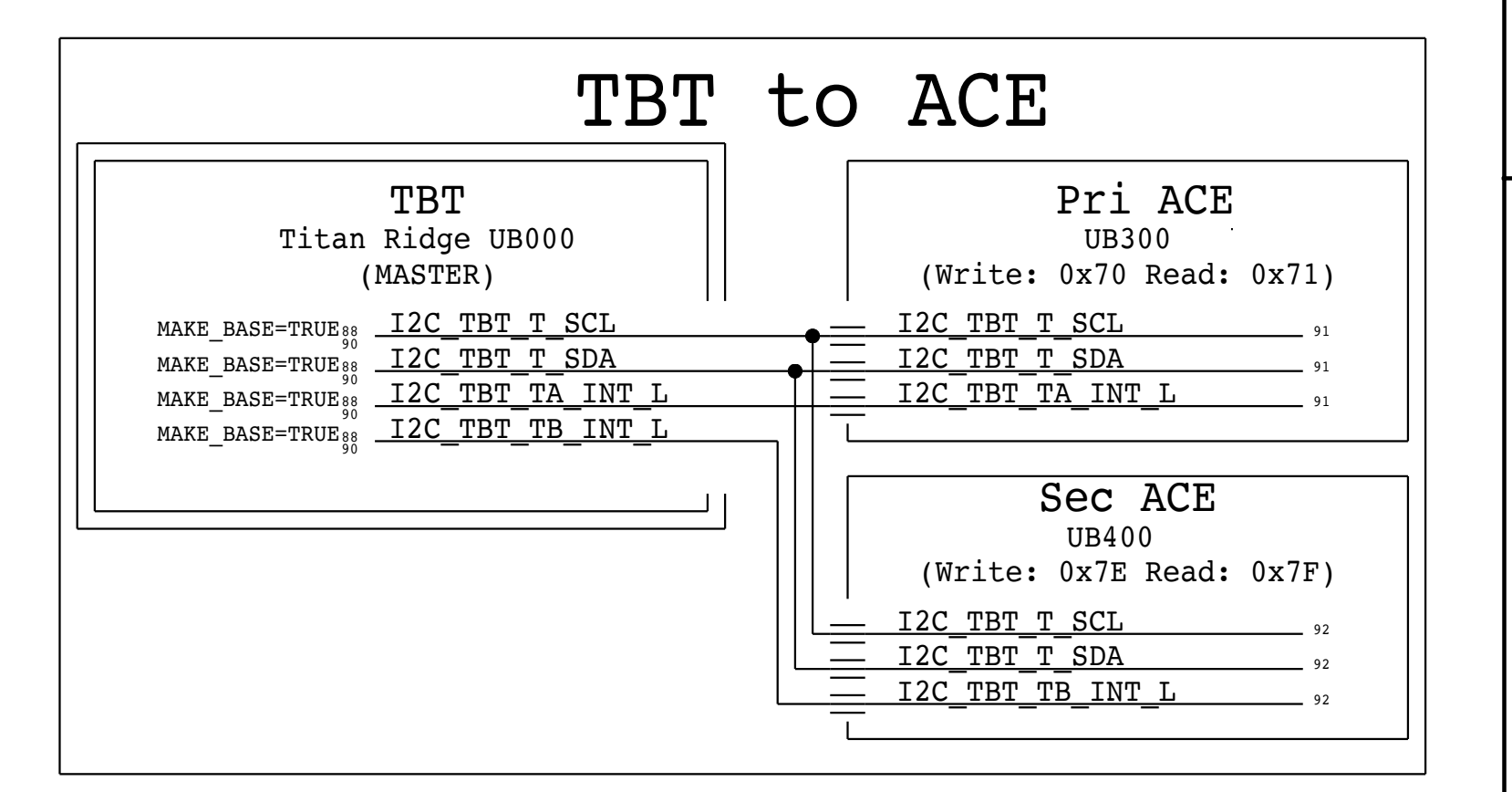
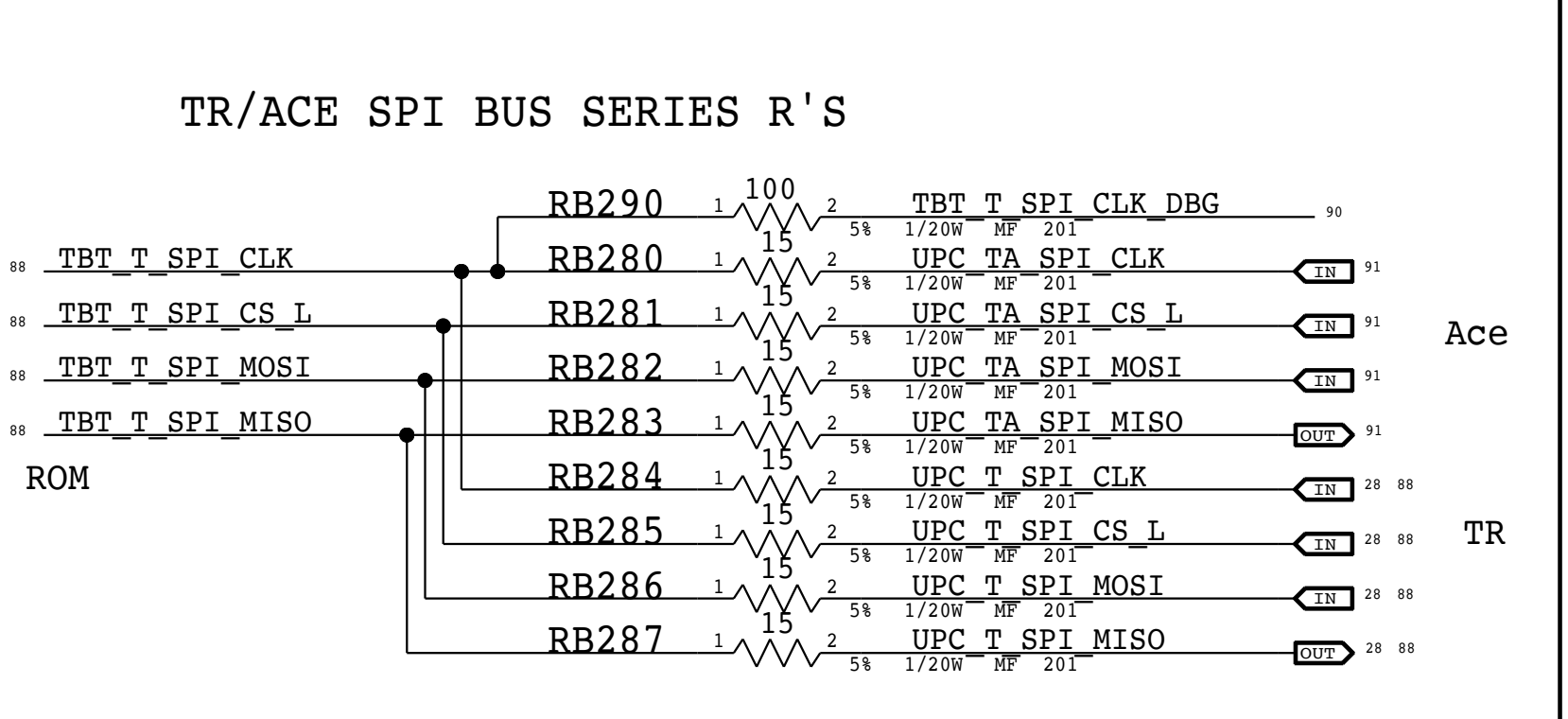
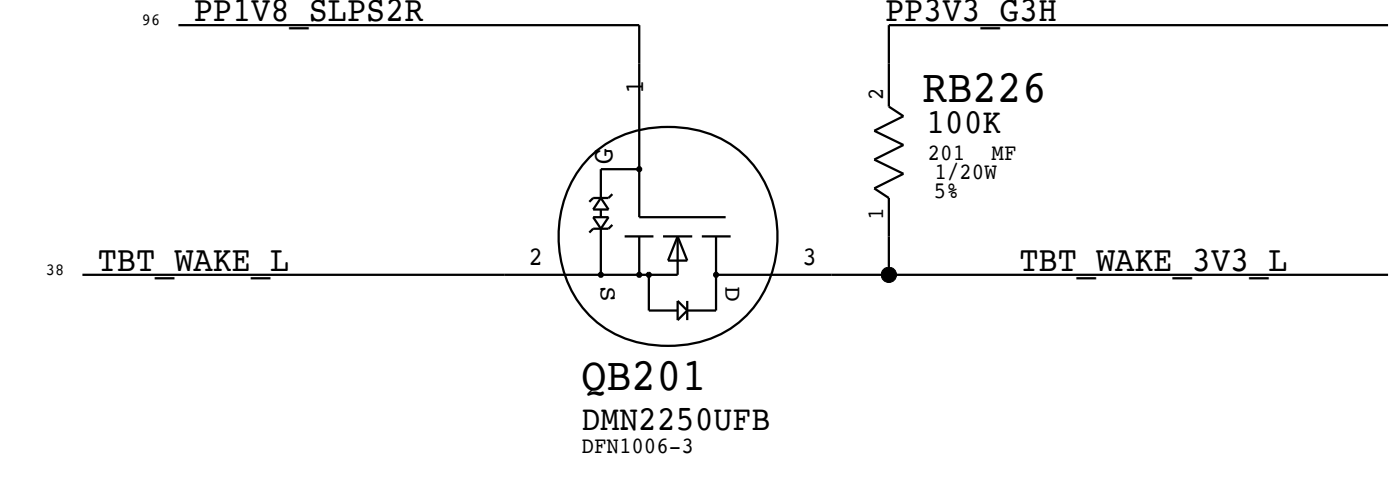
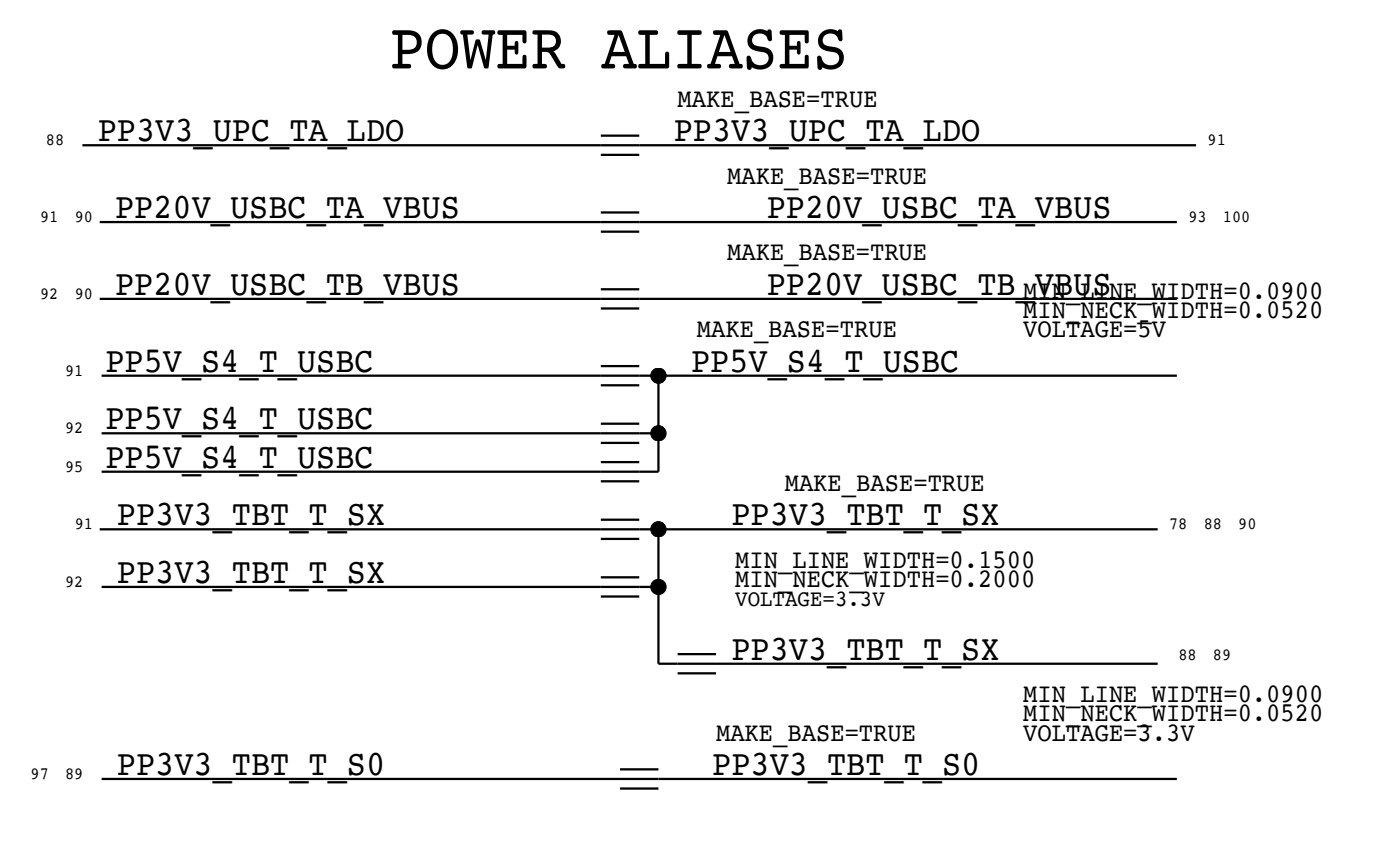
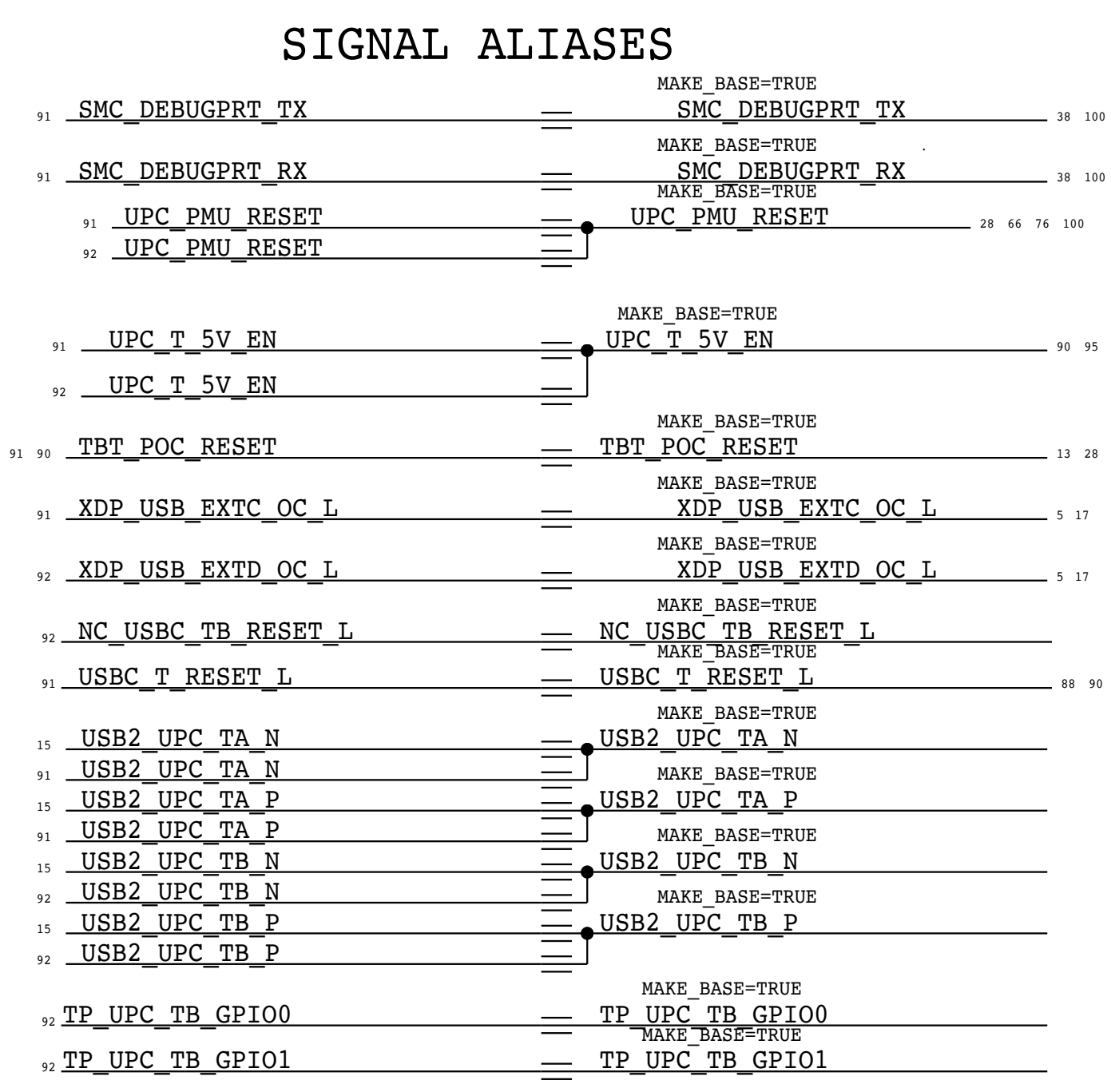
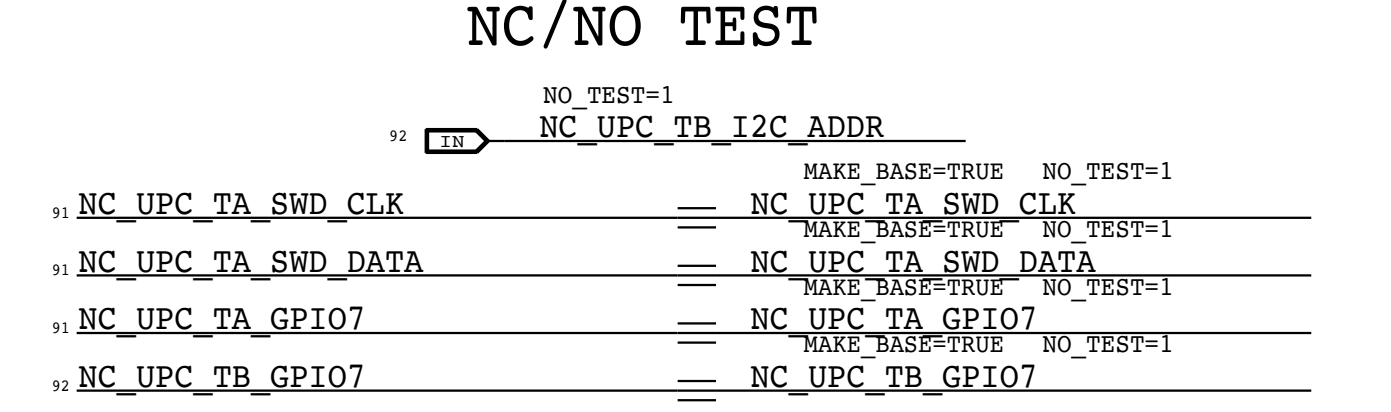
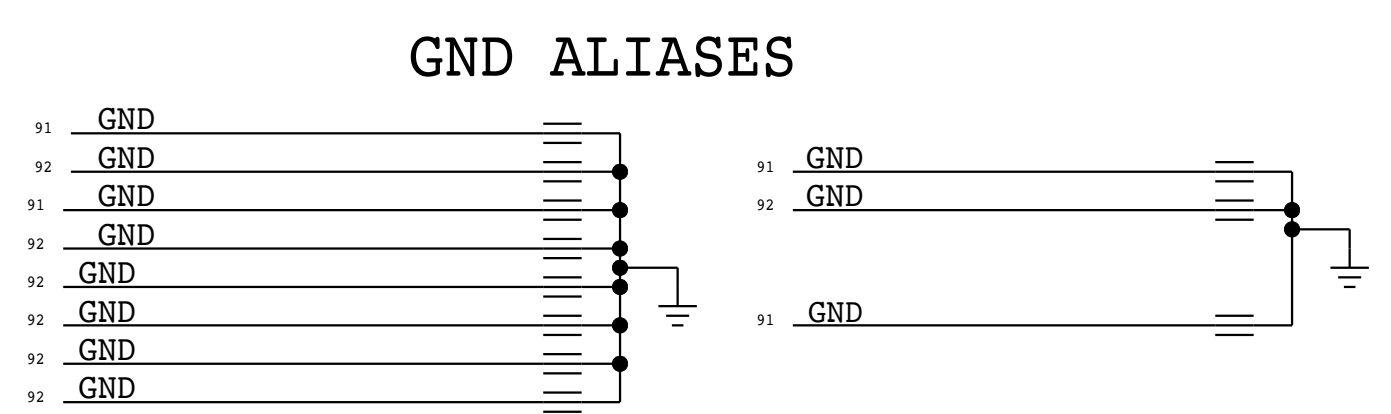
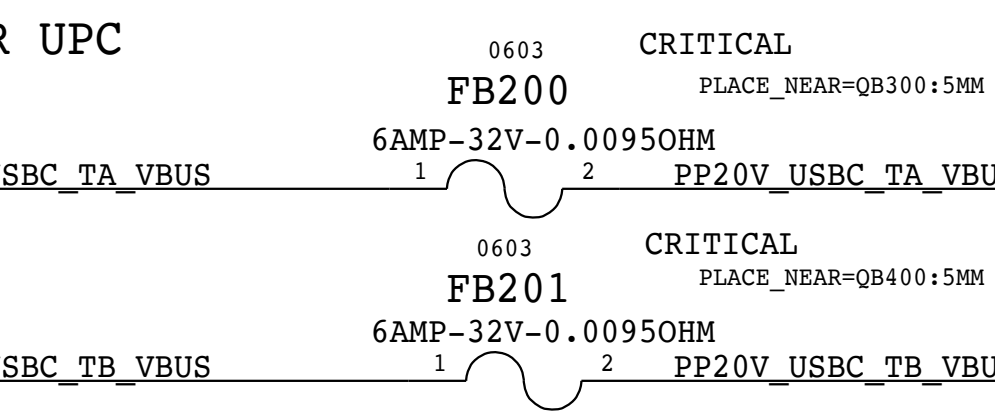
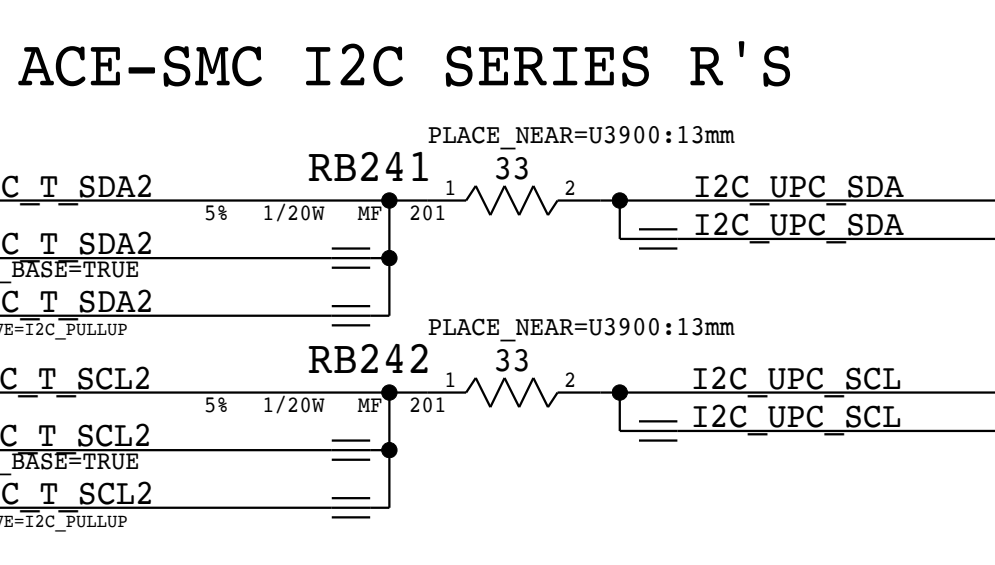
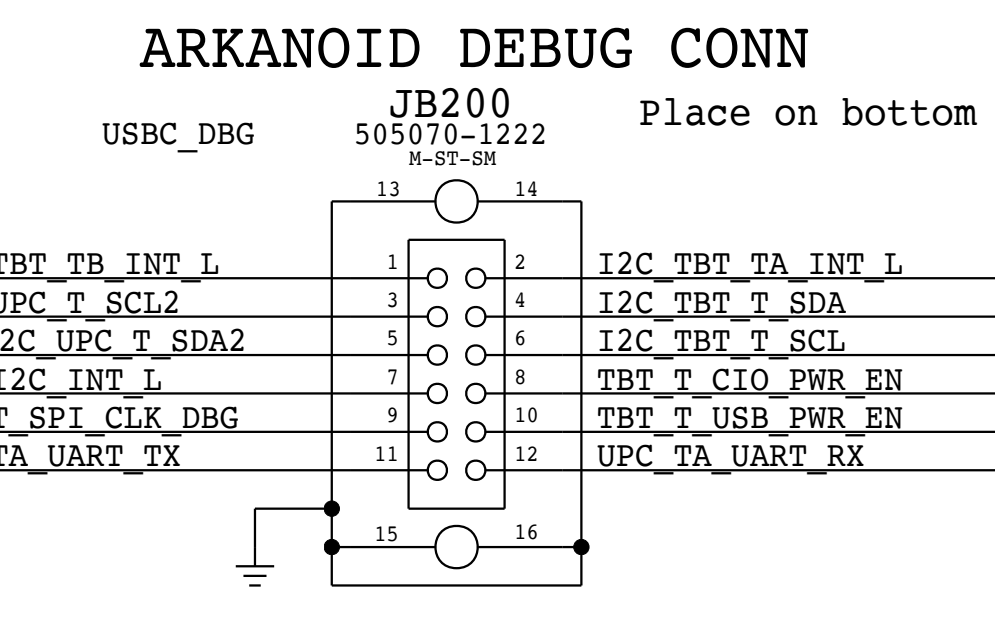
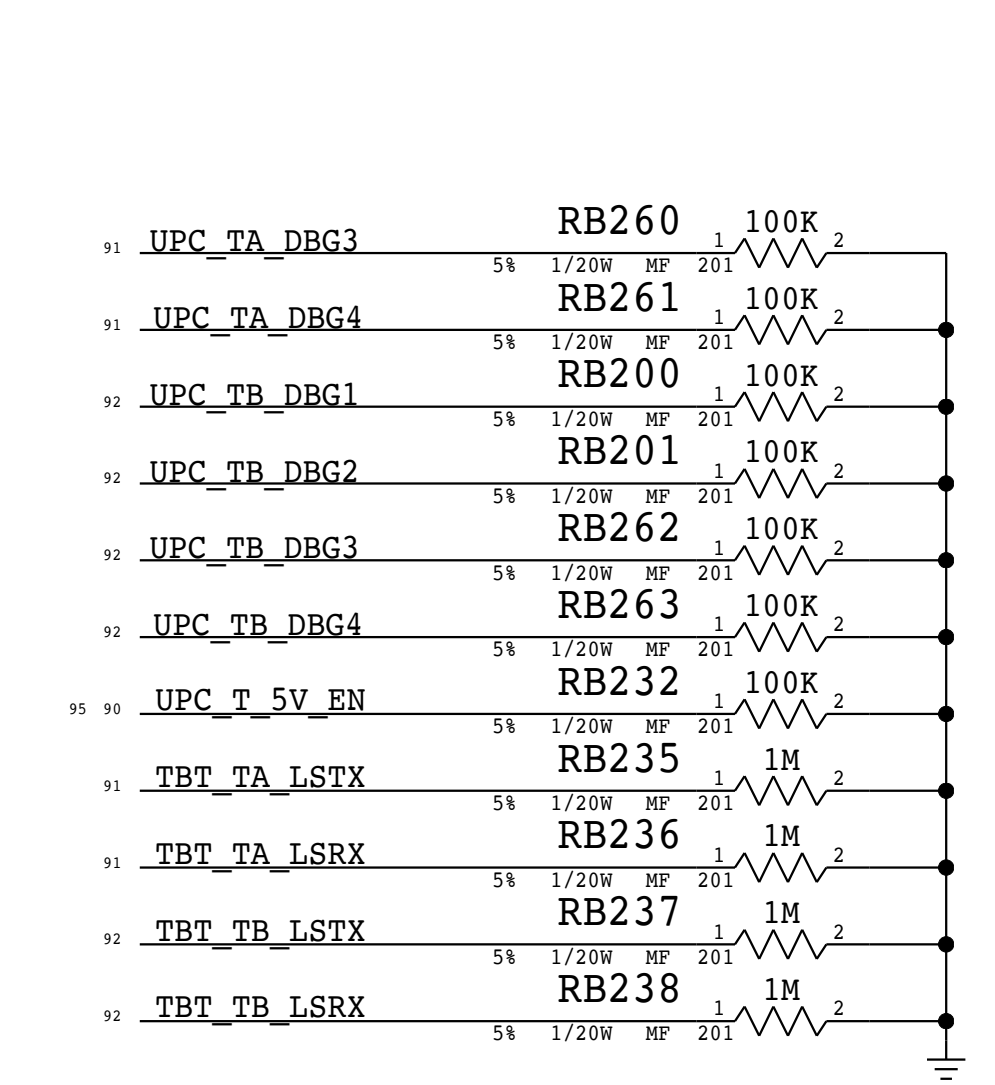
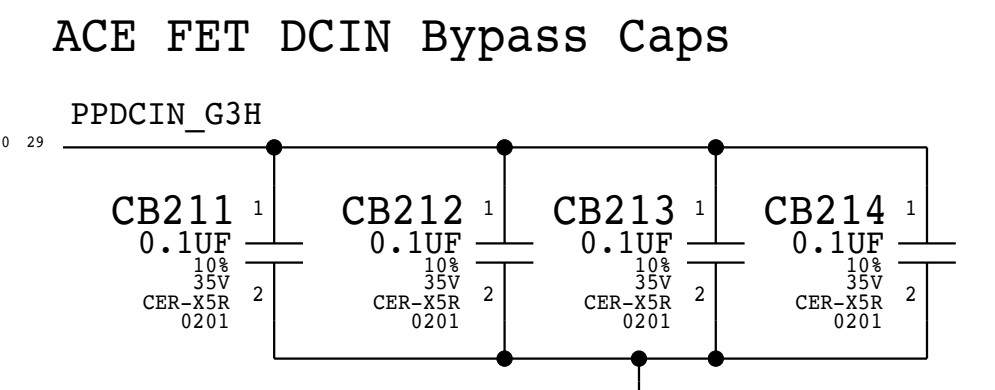
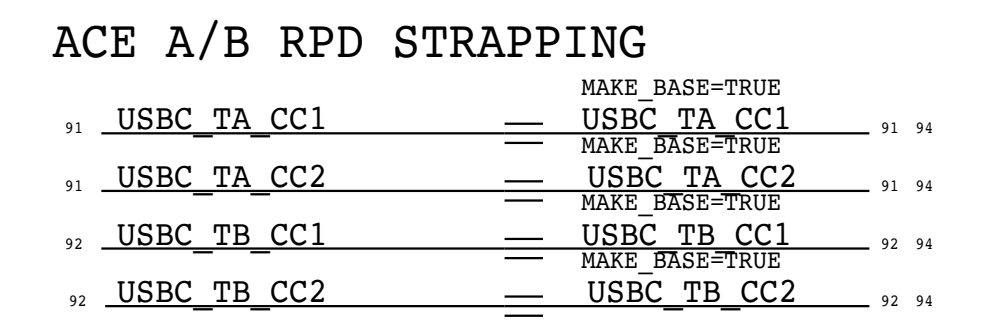
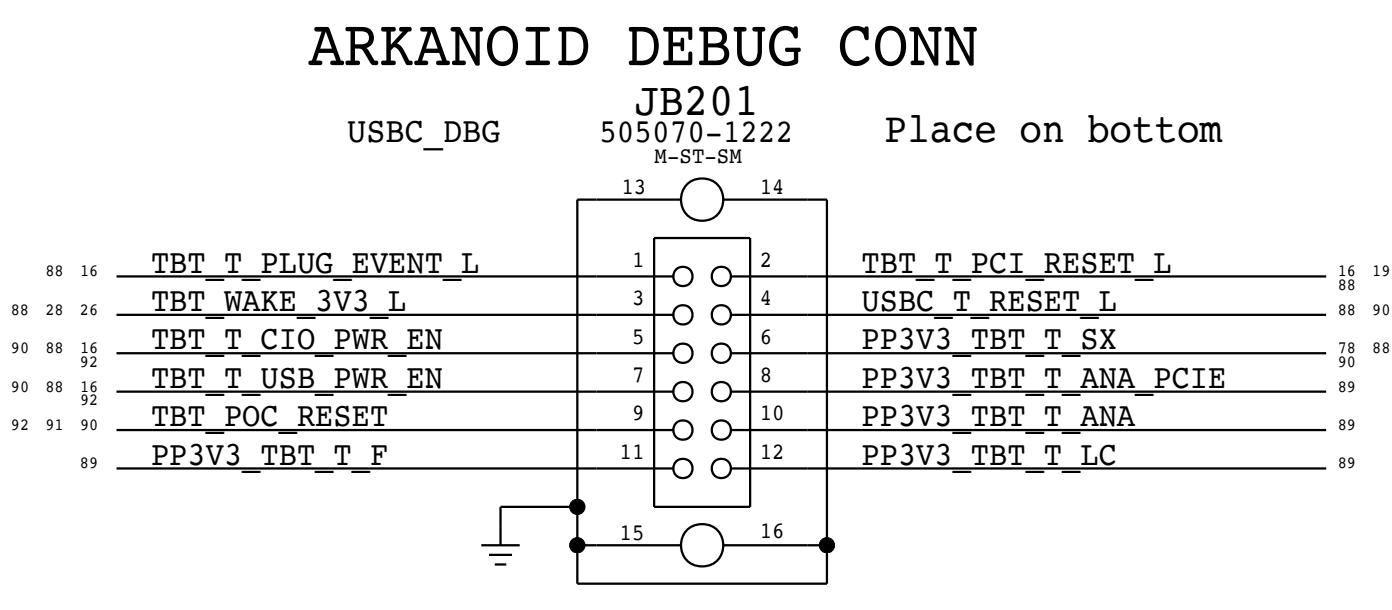
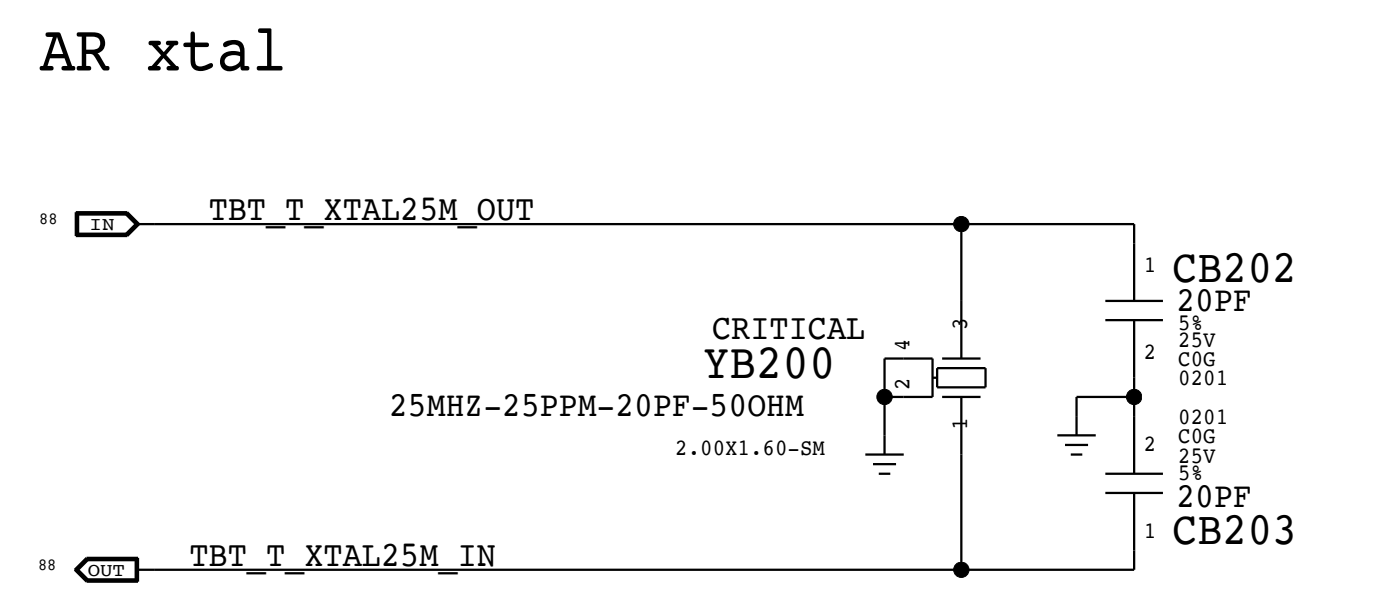
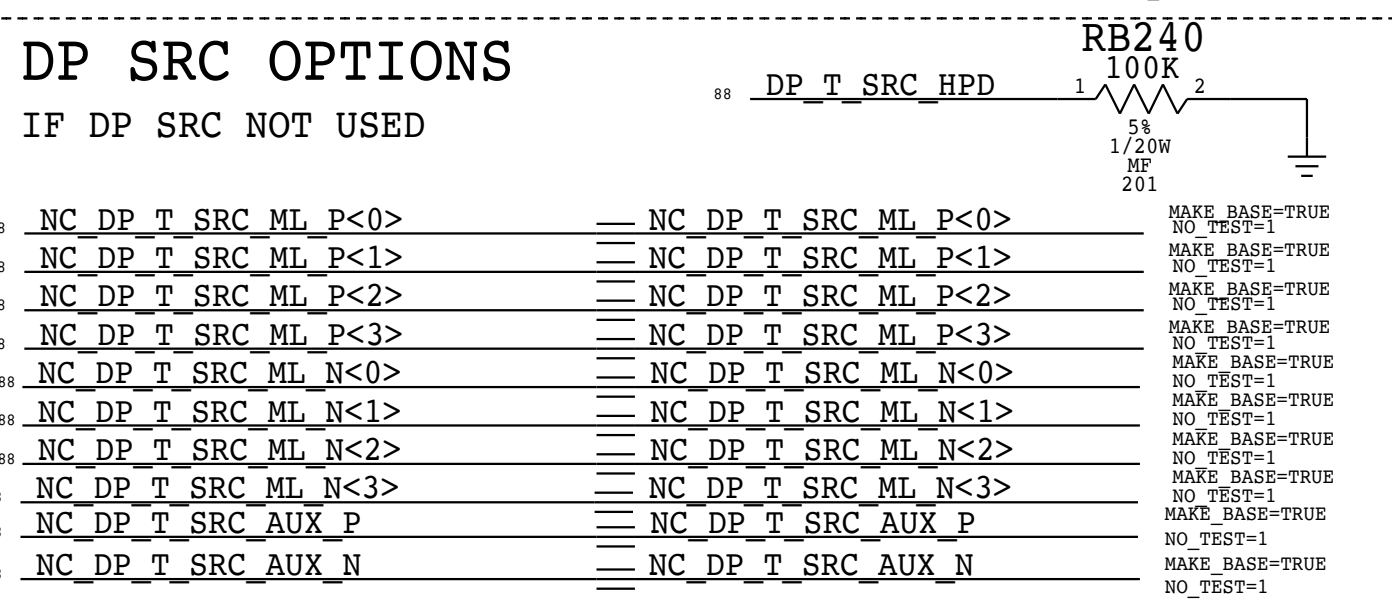
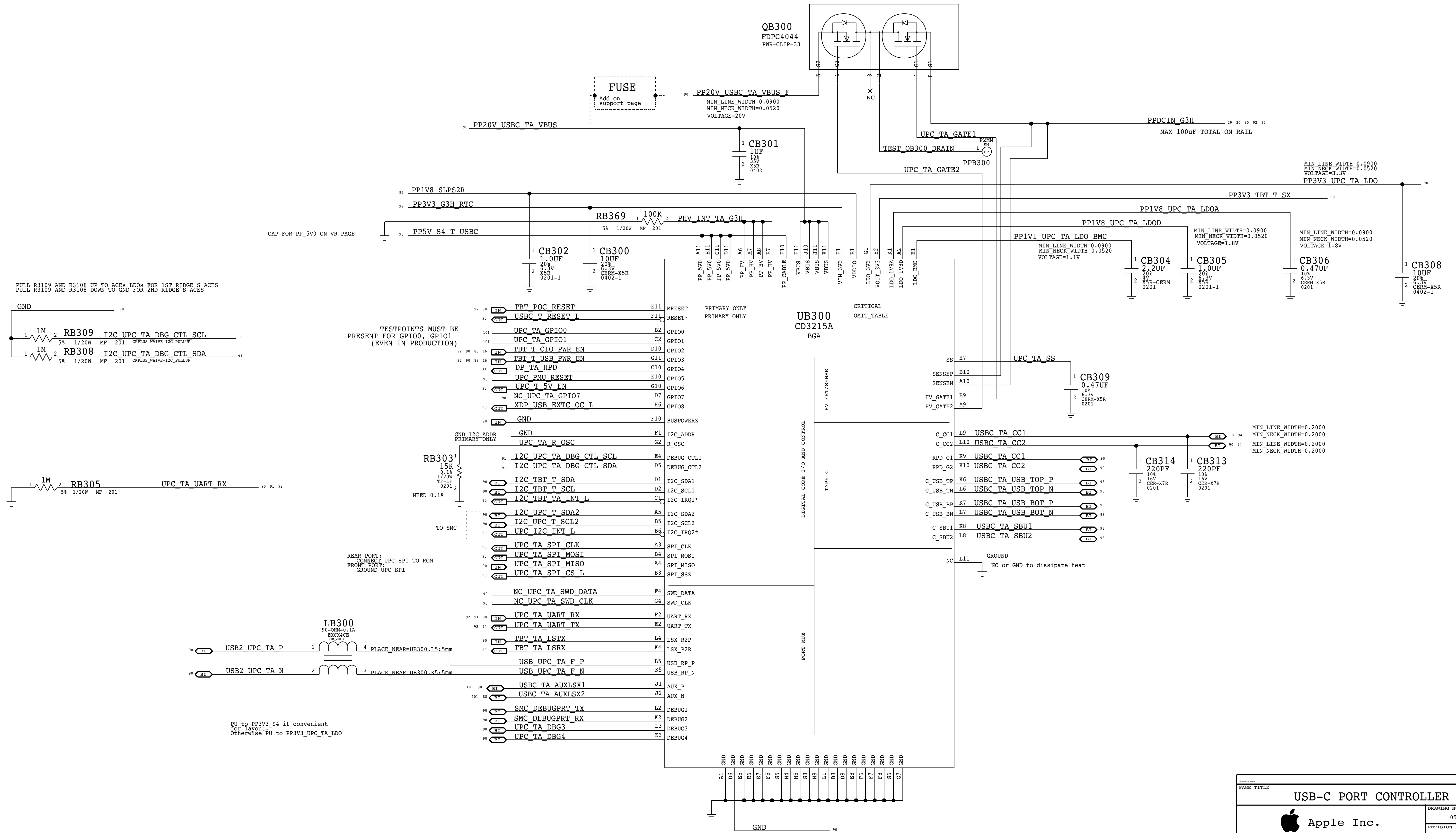


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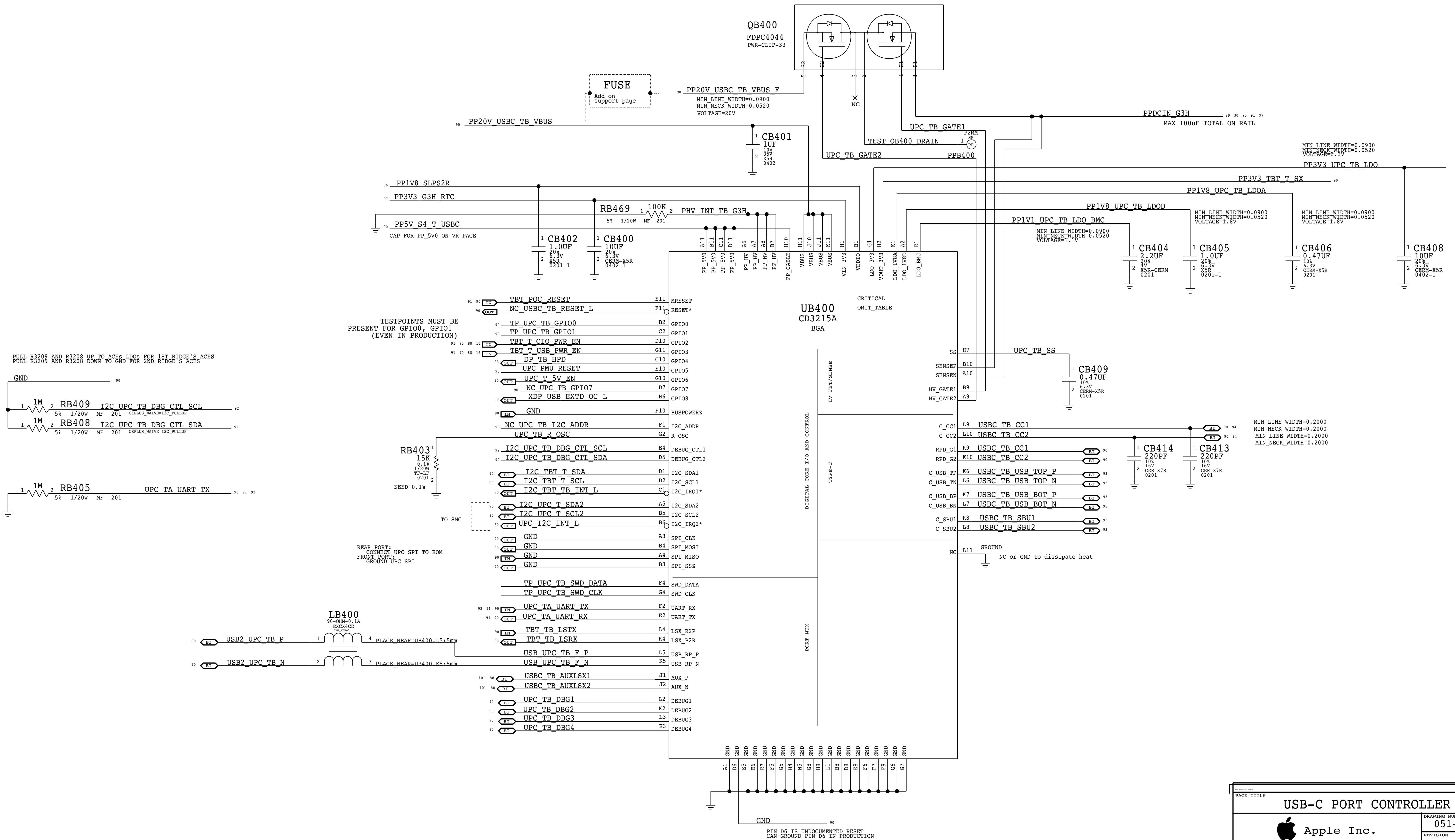
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



PAGE TITLE		
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	DRAWING NUMBER	051-02166
	REVISION	4.0.0
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	PAGE	113 OF 150
	SHEET	91 OF 108
	SIZE	D

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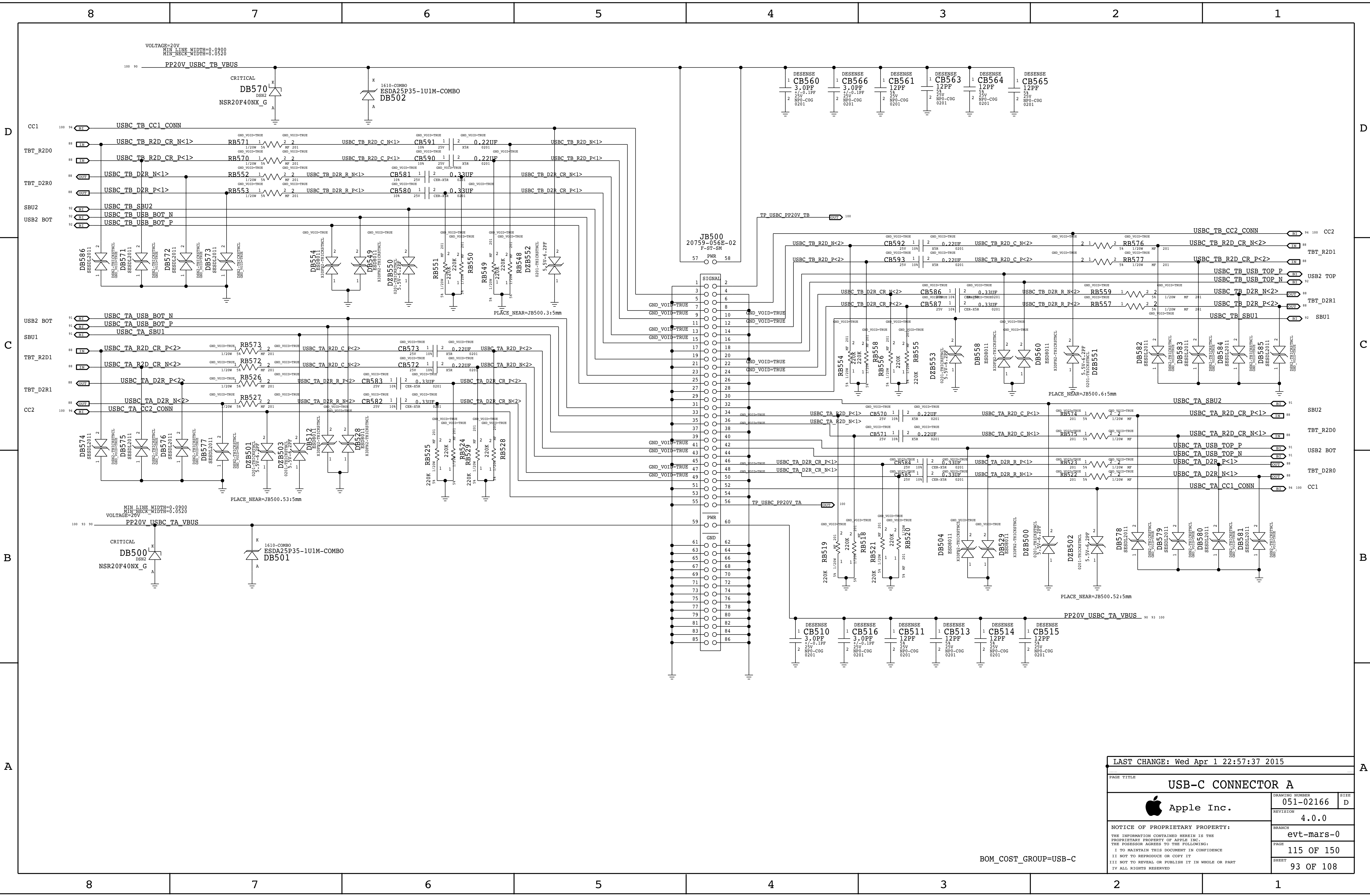
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



PAGE TITLE		
USB-C PORT CONTROLLER B		
Apple Inc.		
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REVISION	4.0.0	D
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BRANCH	evt-mars-0	
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BOM COST GROUP=USB-C

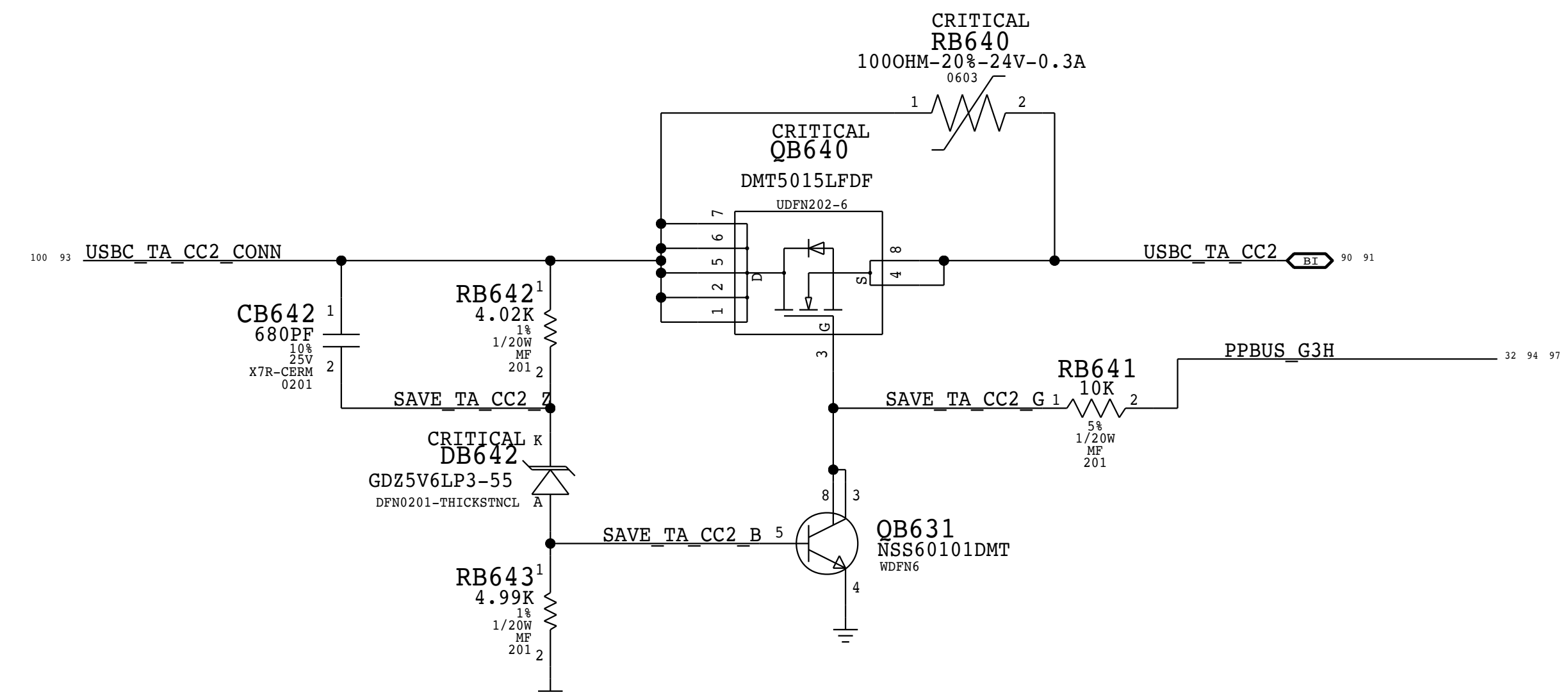
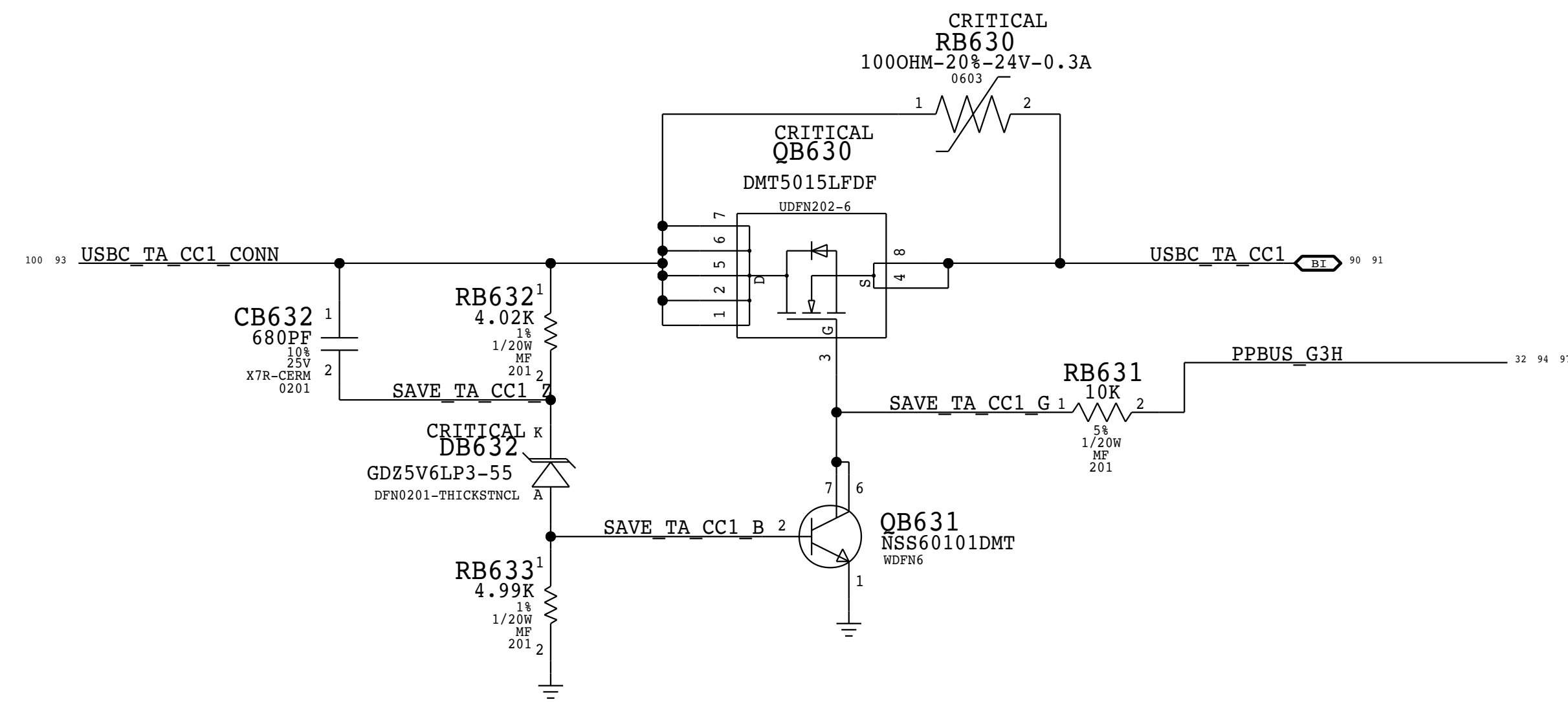
PIN D6 IS UNDOCUMENTED RESET CAN GROUND PIN D6 IN PRODUCTION



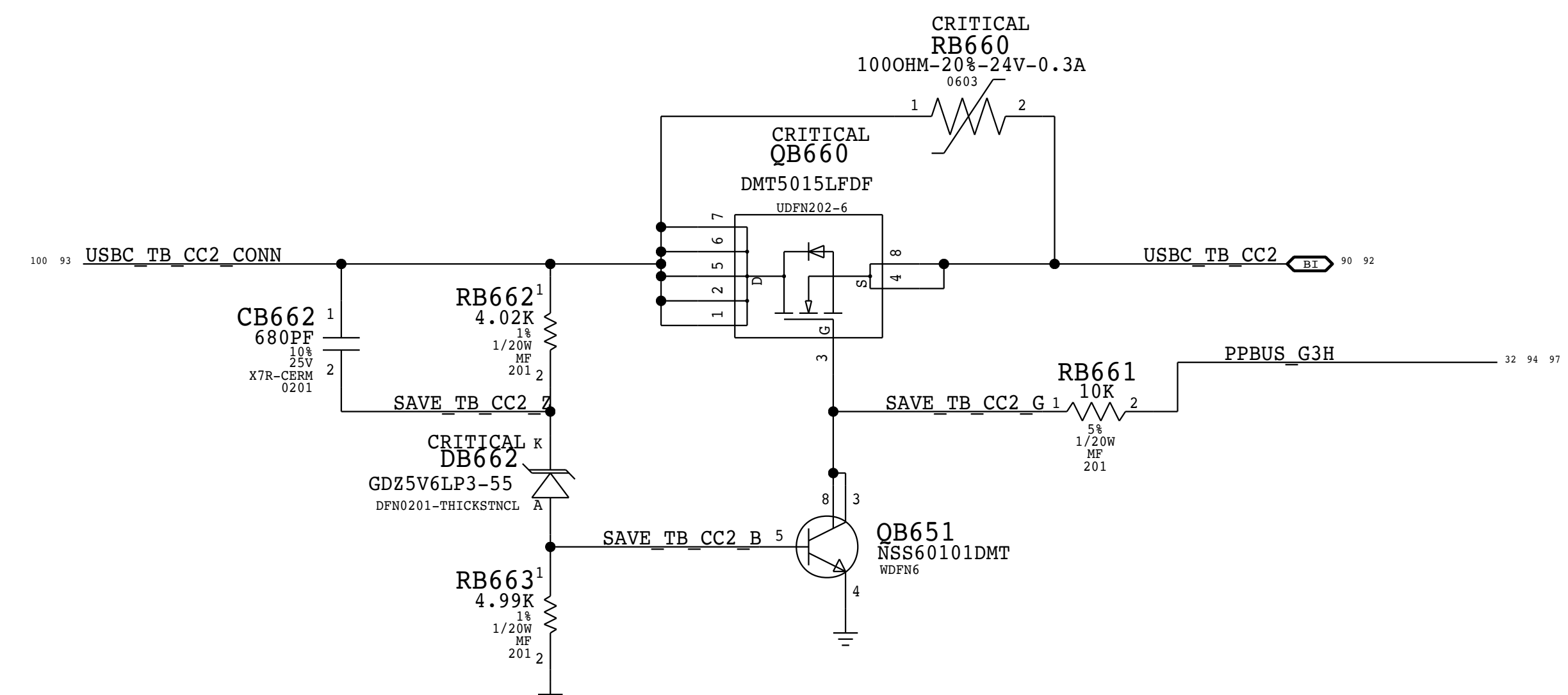
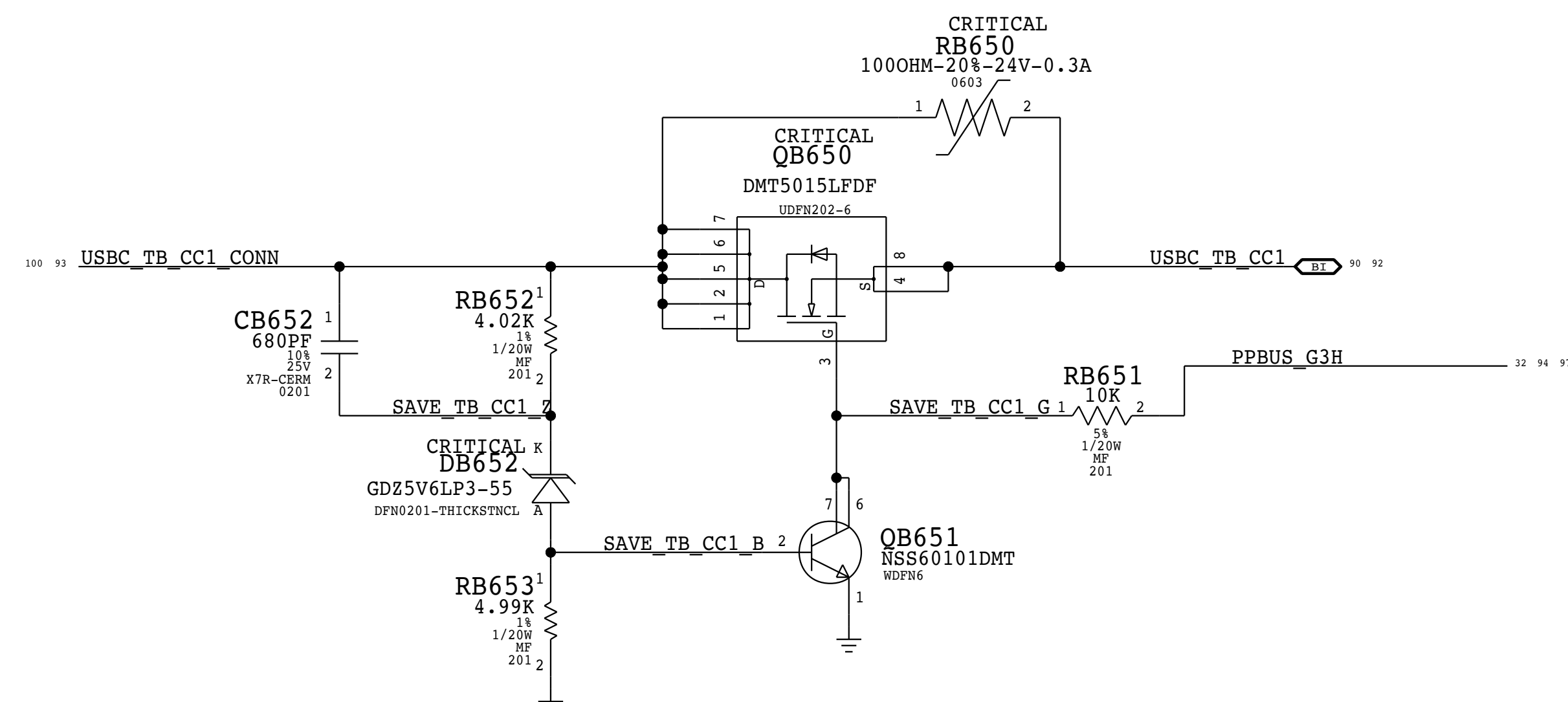
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BOM_COST_GROUP=USB-C

TA CC Protection

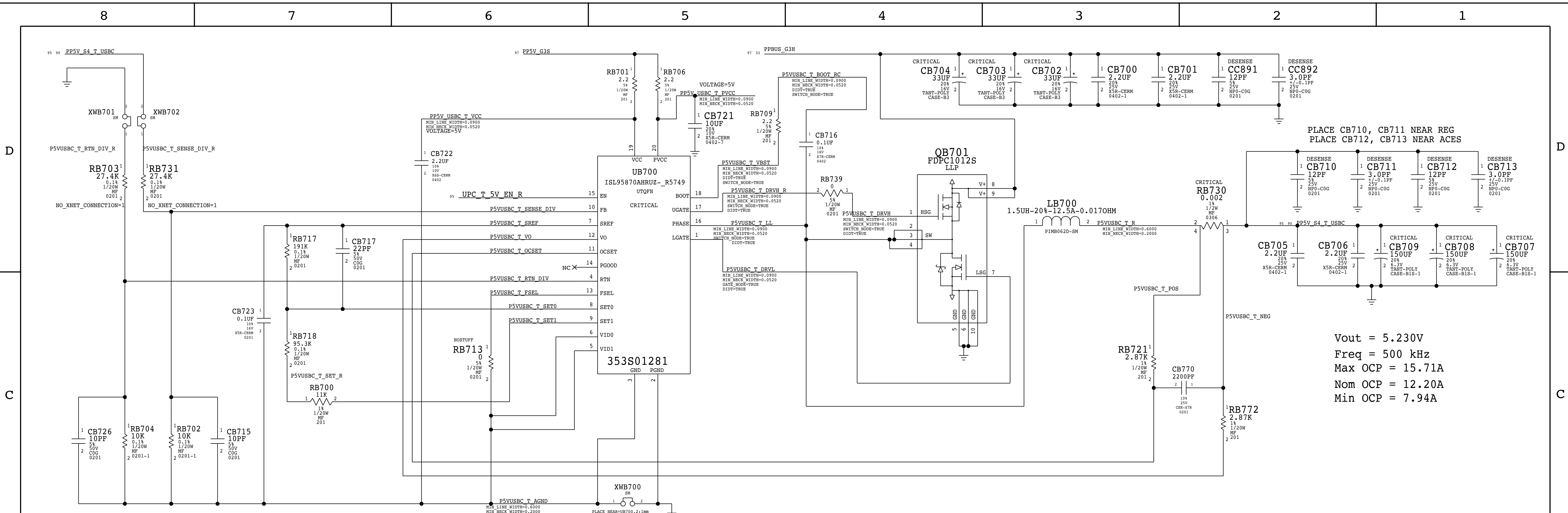


TB CC Protection



DESIGN: X1032/MLB P4BP		
LAST CHANGE: Fri Jan 6 16:01:21 2017		
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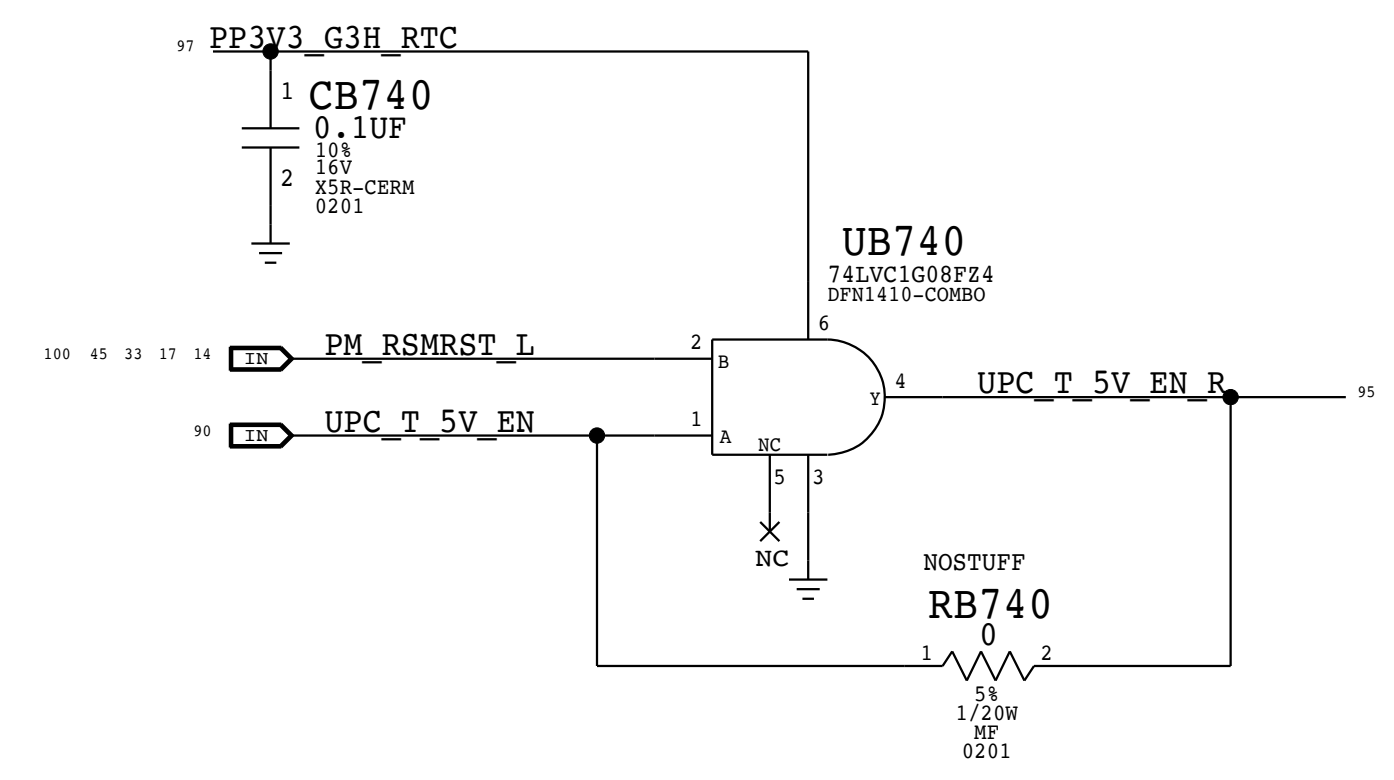
BOM_COST_GROUP=USB-C



PLACE CB710, CB711 NEAR REG
PLACE CB712, CB713 NEAR ACES

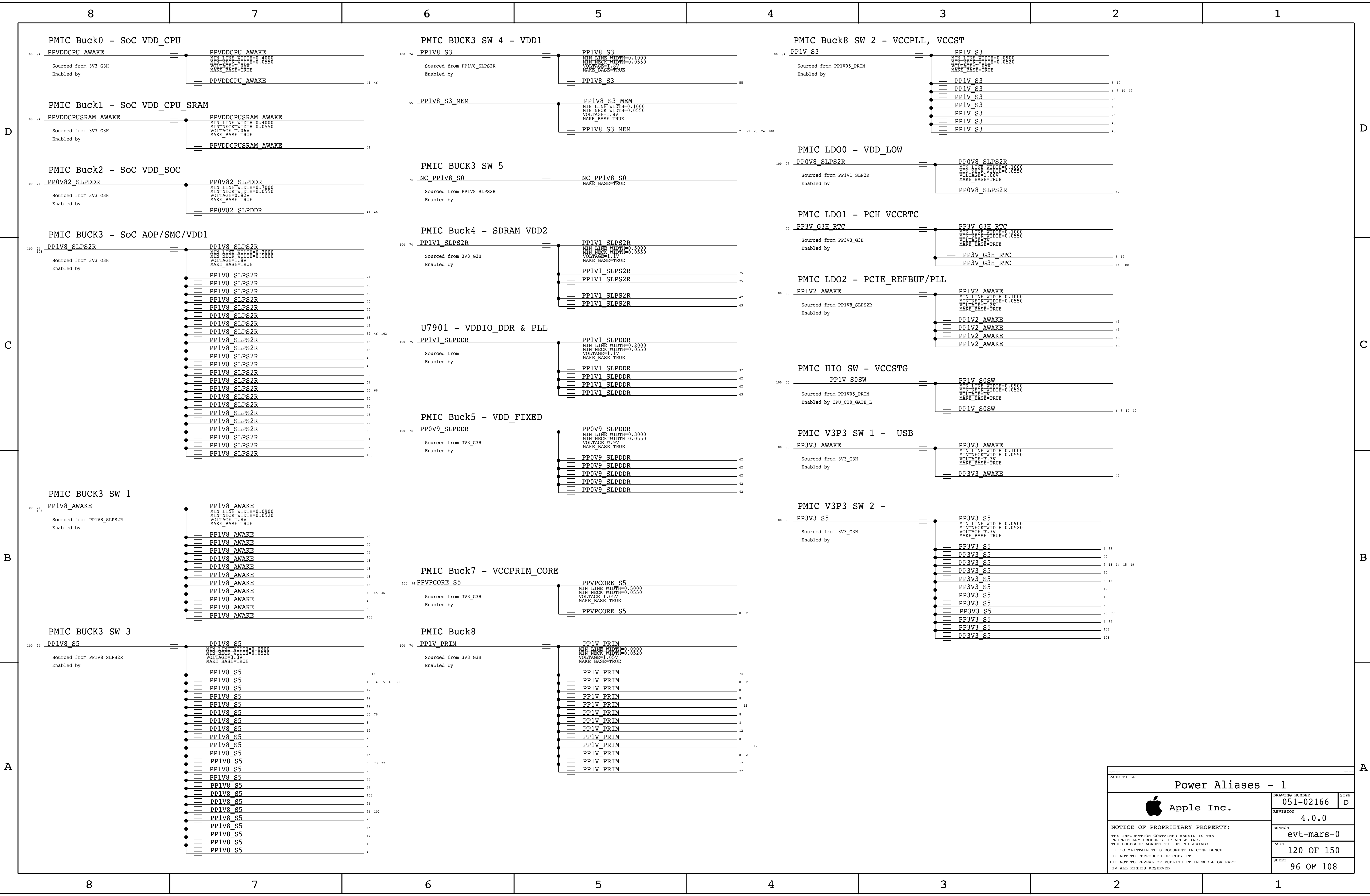
Vout = 5.230V
Freq = 500 kHz
Max OCP = 15.71A
Nom OCP = 12.20A
Min OCP = 7.94A

UPC T 5V EN QUALIFIER

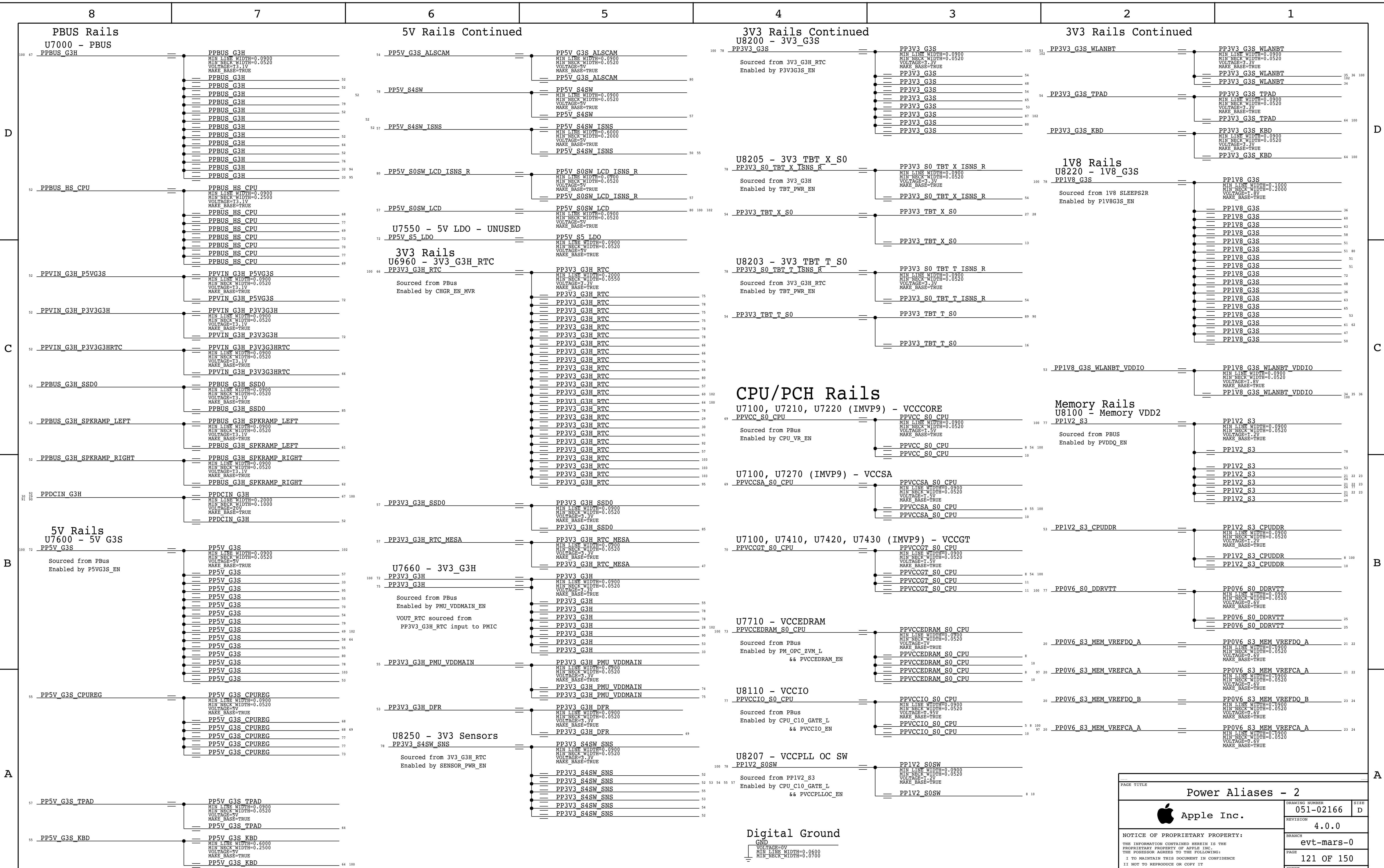


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	PAGE	117 OF 150
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	SIZE	D

BOM_COST_GROUP=USB-C



PAGE TITLE		
Power Aliases - 1		
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PAGE TITLE		
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Unused SoC Signals

TP SoC Signals

SoC Aliases

Unused PMIC Signals

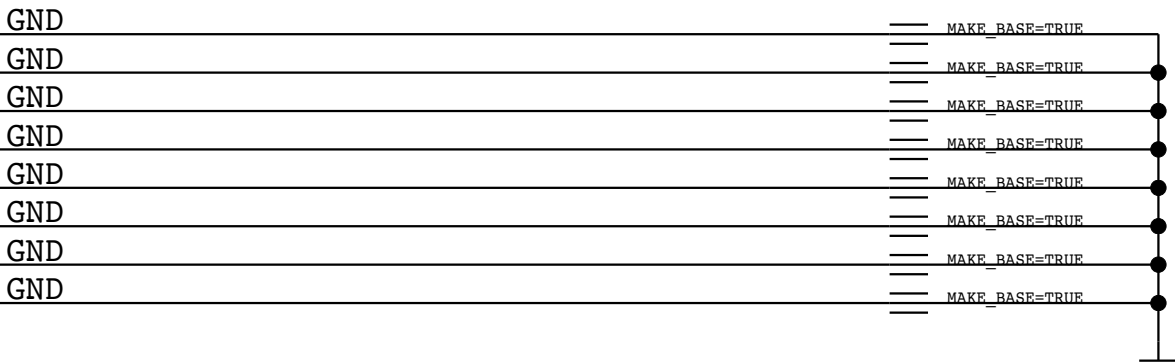
PMIC Aliases

Unused WIRELESS Signals

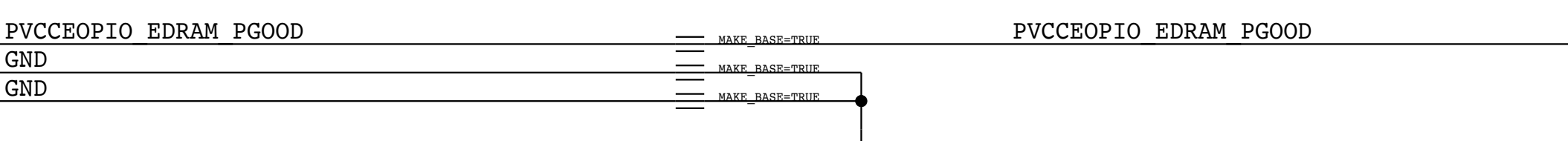
Unused SSD Signals

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38	NC DISP GCON INT L	---	MAKE_BASE+THRU	NO_TEST=1	NC DISP GCON INT L
38	NC DFR TOUCH RSV	---	MAKE_BASE+THRU	NO_TEST=1	NC DFR TOUCH RSV
38	NC ENET_LOW_PWR	---	MAKE_BASE+THRU	NO_TEST=1	NC ENET_LOW_PWR
38	NC ENET_MEDIA_SENSE	---	MAKE_BASE+THRU	NO_TEST=1	NC ENET_MEDIA_SENSE
38	NC ENET_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC ENET_RESET_L
38	NC FTCAM_CLK12M_R	---	MAKE_BASE+THRU	NO_TEST=1	NC FTCAM_CLK12M_R
38	NC FTCAM_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC FTCAM_RESET_L
38	NC GNSS_DEV_WAKE	---	MAKE_BASE+THRU	NO_TEST=1	NC GNSS_DEV_WAKE
38	NC GNSS_HOST_TIME	---	MAKE_BASE+THRU	NO_TEST=1	NC GNSS_HOST_TIME
38	NC I2S_CODEC_MCLK	---	MAKE_BASE+THRU	NO_TEST=1	NC I2S_CODEC_MCLK
38	NC I2S_CODEC1_MCLK	---	MAKE_BASE+THRU	NO_TEST=1	NC I2S_CODEC1_MCLK
38	NC I2S_CODEC1_R2D_R	---	MAKE_BASE+THRU	NO_TEST=1	NC I2S_CODEC1_R2D_R
38	NC I2S_HAWKING_BCLK_R	---	MAKE_BASE+THRU	NO_TEST=1	NC I2S_HAWKING_BCLK_R
38	NC I2S_HAWKING_D2R	---	MAKE_BASE+THRU	NO_TEST=1	NC I2S_HAWKING_D2R
38	NC I2S_HAWKING_LRCLK	---	MAKE_BASE+THRU	NO_TEST=1	NC I2S_HAWKING_LRCLK
38	NC MESA_MENUKEY_L	---	MAKE_BASE+THRU	NO_TEST=1	NC MESA_MENUKEY_L
38	NC PCC_EVENT	---	MAKE_BASE+THRU	NO_TEST=1	NC PCC_EVENT
38	NC PCH_ENET_LOW_PWR	---	MAKE_BASE+THRU	NO_TEST=1	NC PCH_ENET_LOW_PWR
38	NC SOC_PCH_GCON_INT_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SOC_PCH_GCON_INT_L
38	NC PCIE_CLK100M_ENET_N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_ENET_N
38	NC PCIE_CLK100M_ENET_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_ENET_P
38	NC PCIE_CLK100M_SSD1_01_N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_SSD1_01_N
38	NC PCIE_CLK100M_SSD1_01_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_SSD1_01_P
38	NC PCIE_CLK100M_SSD1_23_N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_SSD1_23_N
38	NC PCIE_CLK100M_SSD1_23_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_SSD1_23_P
38	NC PCIE_CLK100M_WLAN_N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_WLAN_N
38	NC PCIE_CLK100M_WLAN_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_WLAN_P
38	NC PCIE_ENET_D2R_N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_ENET_D2R_N
38	NC PCIE_ENET_D2R_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_ENET_D2R_P
38	NC PCIE_ENET_R2D_C_N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_ENET_R2D_C_N
38	NC PCIE_ENET_R2D_C_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_ENET_R2D_C_P
38	NC PCIE_SSD1_D2R_N<3..0>	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_SSD1_D2R_N<3..0>
38	NC PCIE_SSD1_D2R_P<3..0>	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_SSD1_D2R_P<3..0>
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38	NC PCIE_WLAN_R2D_C_P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_WLAN_R2D_C_P
38	NC PCIEDN_WAKE_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIEDN_WAKE_L
38	NC PLICAM_PROX_INT_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_PROX_INT_L
38	NC PLICAM_ROMEO_B2B_DETECT	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_ROMEO_B2B_DETECT
38	NC PLICAM_RX_CLK12M_R	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_RX_CLK12M_R
38	NC PLICAM_RX_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_RX_RESET_L
38	NC PLICAM_TX_CLK12M_R	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_TX_CLK12M_R
38	NC PLICAM_TX_INT	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_TX_INT
38	NC PLICAM_TX_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_TX_RESET_L
38	NC PLICAM_TX_THROTTLE	---	MAKE_BASE+THRU	NO_TEST=1	NC PLICAM_TX_THROTTLE
38	NC SDCONN_STATE_CHANGE_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SDCONN_STATE_CHANGE_L
38	NC SMC_GFX_SELF_THROTTLE	---	MAKE_BASE+THRU	NO_TEST=1	NC SMC_GFX_SELF_THROTTLE
38	NC SMC_LED_ONEWIRE	---	MAKE_BASE+THRU	NO_TEST=1	NC SMC_LED_ONEWIRE
38	NC SMC_TOPBLK_SWP_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SMC_TOPBLK_SWP_L
38	NC SPI_ALTIMETER_CS_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SPI_ALTIMETER_CS_L
38	NC SPI_DESCRIPTOR_OVERRIDE_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SPI_DESCRIPTOR_OVERRIDE_L
38	NC SSD1_CLK24M_R	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_CLK24M_R
38	NC SSD1_CLKREQ0_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_CLKREQ0_L
38	NC SSD1_CLKREQ1_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_CLKREQ1_L
38	NC SSD1_CLKREQ2_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_CLKREQ2_L
38	NC SSD1_CLKREQ3_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_CLKREQ3_L
38	NC SSD1_PCIE_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_PCIE_RESET_L
38	NC SSD1_SWCLK_UART_R2D	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_SWCLK_UART_R2D
38	NC SSD1_SWDIO_UART_D2R	---	MAKE_BASE+THRU	NO_TEST=1	NC SSD1_SWDIO_UART_D2R
38	NC PCHROM_SW_EN	---	MAKE_BASE+THRU	NO_TEST=1	NC PCHROM_SW_EN
38	NC PCIE_DN2_R2D_CP	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN2_R2D_CP
38	NC PCIE_DN2_R2D_CN	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN2_R2D_CN
38	NC PCIE_DN2_D2RP	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN2_D2RP
38	NC PCIE_DN2_D2RN	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN2_D2RN
38	NC PCIE_DN3_R2D_CP	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN3_R2D_CP
38	NC PCIE_DN3_R2D_CN	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN3_R2D_CN
38	NC PCIE_DN3_D2RP	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN3_D2RP
38	NC PCIE_DN3_D2RN	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_DN3_D2RN
38	NC PCIE_CLK100M_DN2P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_DN2P
38	NC PCIE_CLK100M_DN2N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_DN2N
38	NC PCIEDN2_CLKREQ_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIEDN2_CLKREQ_L
38	NC PCIEDN2_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIEDN2_RESET_L
38	NC PCIE_CLK100M_DN3P	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_DN3P
38	NC PCIE_CLK100M_DN3N	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIE_CLK100M_DN3N
38	NC PCIEDN3_CLKREQ_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIEDN3_CLKREQ_L
38	NC PCIEDN3_RESET_L	---	MAKE_BASE+THRU	NO_TEST=1	NC PCIEDN3_RESET_L
38	NC SOC_USB_ID	---	MAKE_BASE+THRU	NO_TEST=1	NC SOC_USB_ID
38	NC SOC_VDDSOC_SENSE	---	MAKE_BASE+THRU	NO_TEST=1	NC SOC_VDDSOC_SENSE
38	NC SOC_VSSCPU_SENSE	---	MAKE_BASE+THRU	NO_TEST=1	NC SOC_VSSCPU_SENSE
38	NC SOC_VSSSOC_SENSE	---	MAKE_BASE+THRU	NO_TEST=1	NC SOC_VSSSOC_SENSE
38	NC TPAD_VIBE_L	---	MAKE_BASE+THRU	NO_TEST=1	NC TPAD_VIBE_L
38	NC UART_GNSS_D2R_CTS_L	---	MAKE_BASE+THRU	NO_TEST=1	NC UART_GNSS_D2R_CTS_L
38	NC UART_GNSS_R2D_RTS_L	---	MAKE_BASE+THRU	NO_TEST=1	NC UART_GNSS_R2D_RTS_L
38	NC WLAN_CLKREQ_L	---	MAKE_BASE+THRU	NO_TEST=1	NC WLAN_CLKREQ_L
38	NC WLAN_DEV_WAKE	---	MAKE_BASE+THRU	NO_TEST=1	NC WLAN_DEV_WAKE
38	NC WLAN_PERST_L	---	MAKE_BASE+THRU	NO_TEST=1	NC WLAN_PERST_L

100	TP_SMC_FIXTURE_MODE_L	---	MAKE_BASE+THRU		TP_SMC_FIXTURE_MODE_L
100	TP_SOC_DEBUGPRT_RX	---	MAKE_BASE+THRU		TP_SOC_DEBUGPRT_RX
100	TP_SOC_DEBUGPRT_TX	---	MAKE_BASE+THRU		TP_SOC_DEBUGPRT_TX
101	TEST_SOC_AMUXOUT	---	MAKE_BASE+THRU		TEST_SOC_AMUXOUT
101	TEST_SOC_TST_CLKOUT	---	MAKE_BASE+THRU		TEST_SOC_TST_CLKOUT



67	NC_CHGR_AUX_OK	---	MAKE_BASE+THRU	NO_TEST=1	NC_CHGR_AUX_OK
67	NC_GPU_THRMTRIP	---	MAKE_BASE+THRU	NO_TEST=1	NC_GPU_THRMTRIP
76	NC_NAND_DISCHARGE_EN_HDD_PWR_EN	---	MAKE_BASE+THRU	NO_TEST=1	NC_NAND_DISCHARGE_EN_HDD_PWR_EN
76	NC_NAND_RESET_L_SD_PWR_EN	---	MAKE_BASE+THRU	NO_TEST=1	NC_NAND_RESET_L_SD_PWR_EN
76	NC_NAND_WP_L_ENET_PWR_EN	---	MAKE_BASE+THRU	NO_TEST=1	NC_NAND_WP_L_ENET_PWR_EN
76	NC_PEARL_PWREN_P2V7NAND_EN	---	MAKE_BASE+THRU	NO_TEST=1	NC_PEARL_PWREN_P2V7NAND_EN
76	NC_PMU_CLK32K_GNSS_R	---	MAKE_BASE+THRU	NO_TEST=1	NC_PMU_CLK32K_GNSS_R
76	NC_P3V3G3W_EN	---	MAKE_BASE+THRU	NO_TEST=1	NC_P3V3G3W_EN
76	NC_P3V3G3W_PGOOD	---	MAKE_BASE+THRU	NO_TEST=1	NC_P3V3G3W_PGOOD
76	NC_PMU_CLK32K	---	MAKE_BASE+THRU	NO_TEST=1	NC_PMU_CLK32K
74	NC_PPBUCK8_SW1	---	MAKE_BASE+THRU	NO_TEST=1	NC_PPBUCK8_SW1



35	NC_I2S_BT_D2R	---	MAKE_BASE+THRU	NO_TEST=1	NC_I2S_BT_D2R
35	NC_I2S_BT_R2D	---	MAKE_BASE+THRU	NO_TEST=1	NC_I2S_BT_R2D
35	NC_WLAN_PMU_TEST	---	MAKE_BASE+THRU	NO_TEST=1	NC_WLAN_PMU_TEST

85	NC_SSD0_OCARINA_VEN2	---	MAKE_BASE+THRU	NO_TEST=1	NC_SSD0_OCARINA_VEN2
85	NC_SSD0_OCARINA_VR2_DIS	---	MAKE_BASE+THRU	NO_TEST=1	NC_SSD0_OCARINA_VR2_DIS

SYNC MASTER=J132 GAREN SYNC DATE=04/12/2017

PAGE TITLE

Signal Aliases

DRAWING NUMBER	051-02166	SIZE	D
REVISION	4.0.0		
BRANCH	evt-mars-0		
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Memory Bit & Byte Swizzle

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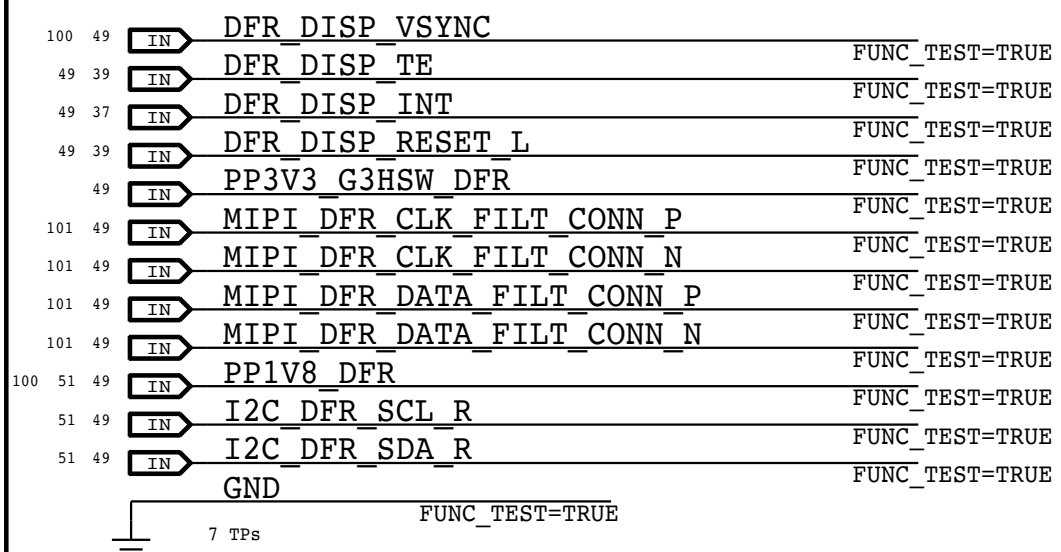
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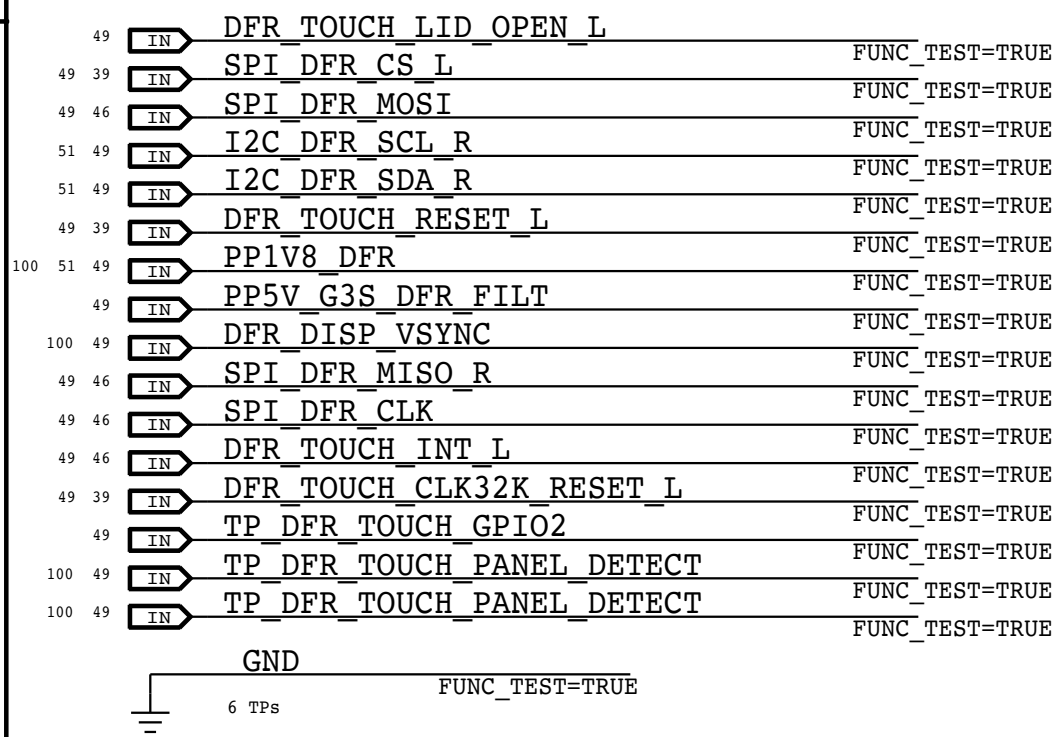
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Functional Test Points

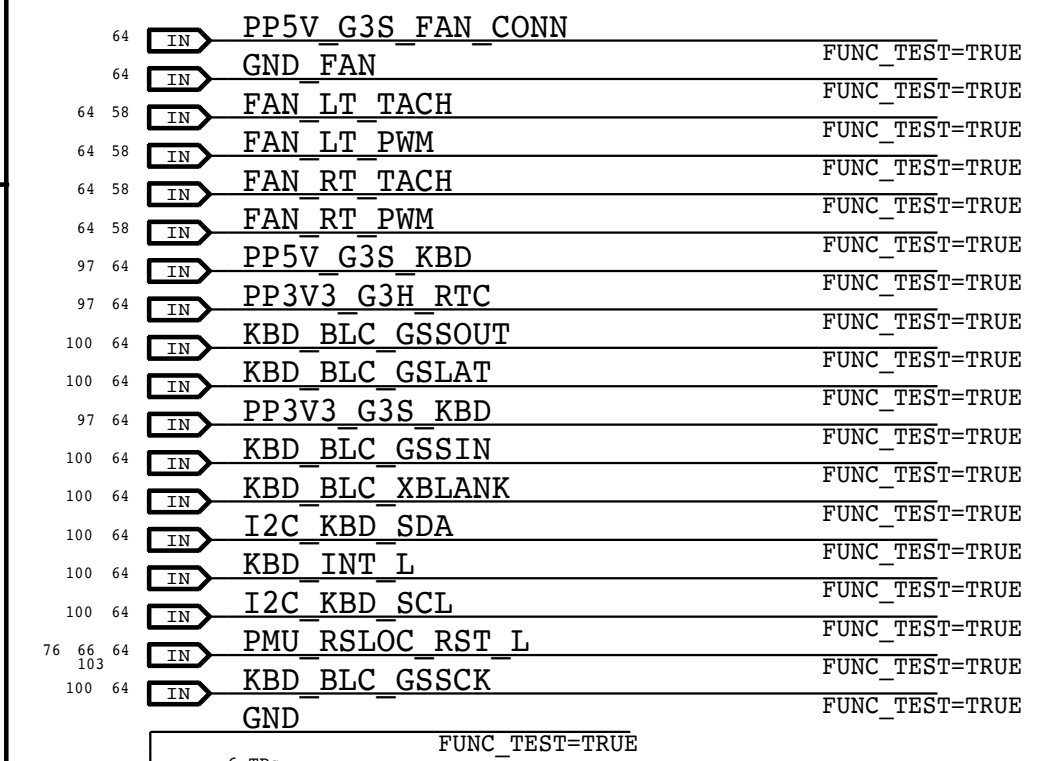
J5110 - DFR Display Connector



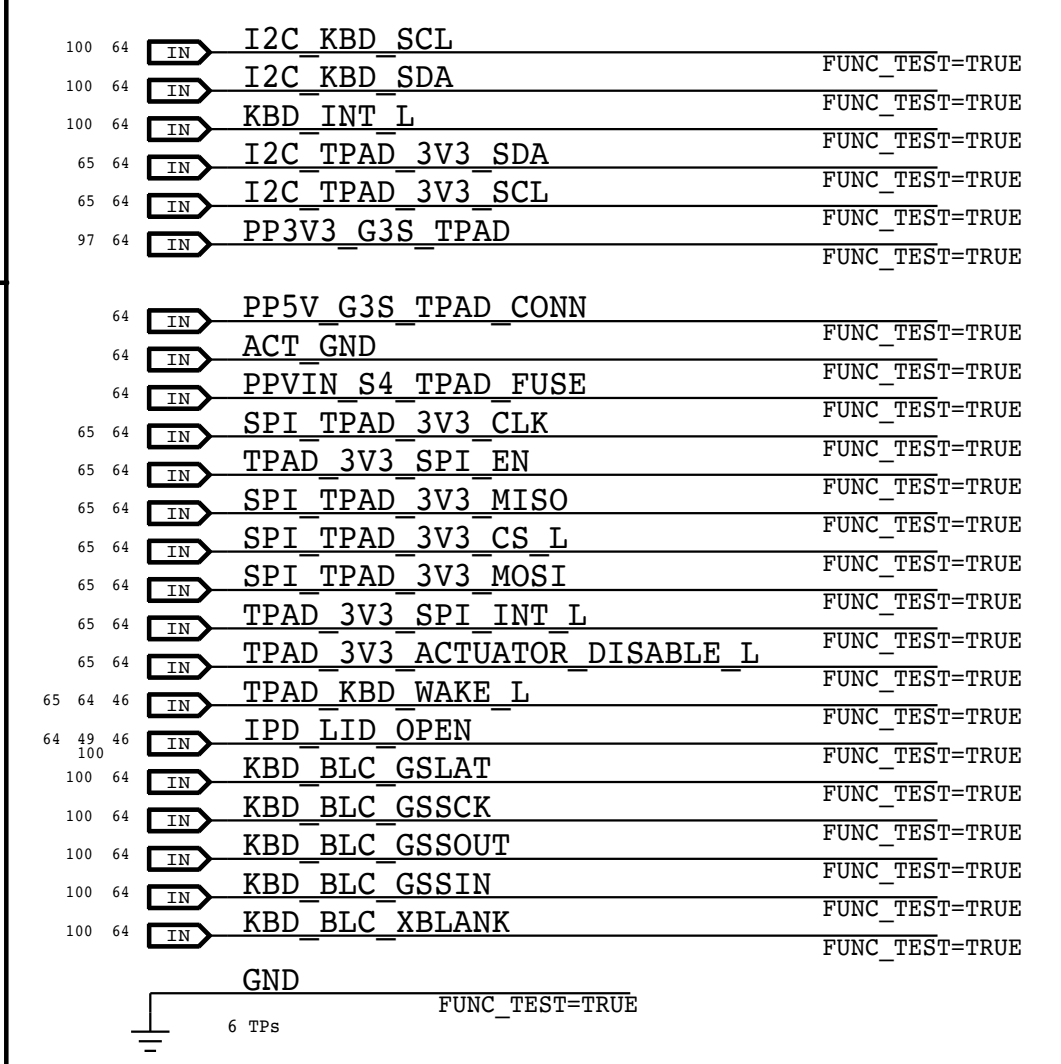
J5100 - DFR Touch Connector



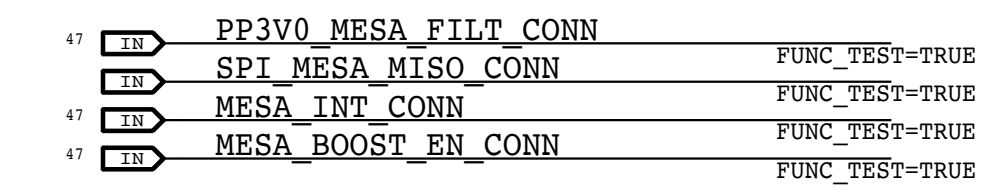
J6700 - Keyboard Connector



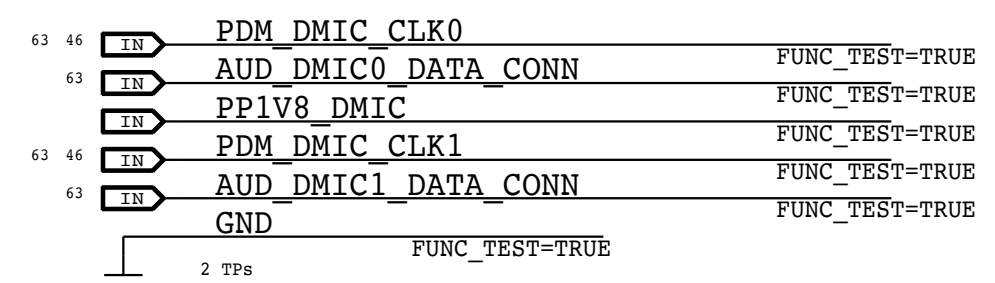
J6701 - Trackpad Connector



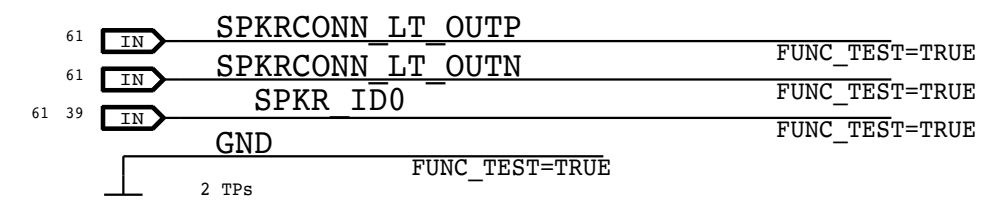
J4900 - Mesa Connector



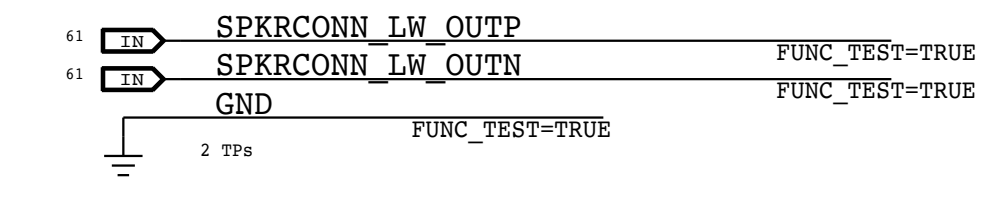
J6640 - MIC Connector



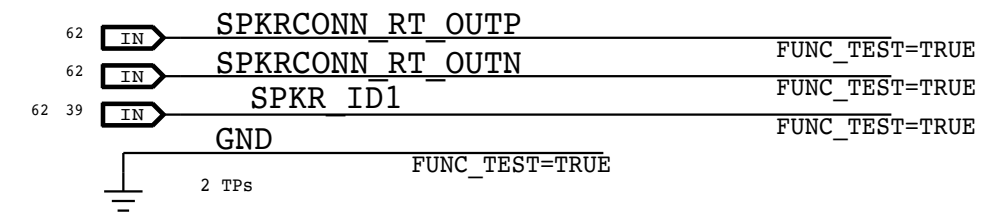
J6400 - Left Tweeter Connector



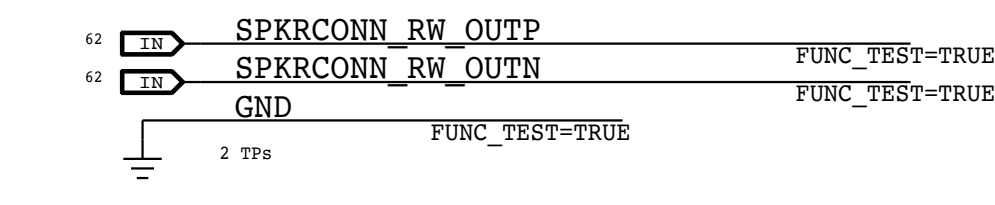
J6450 - Left Woofer Connector



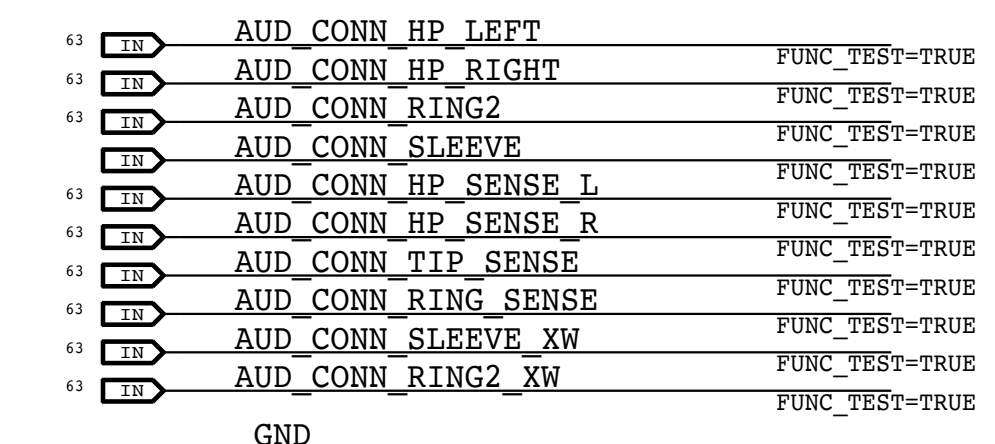
J6500 - Right Tweeter Connector



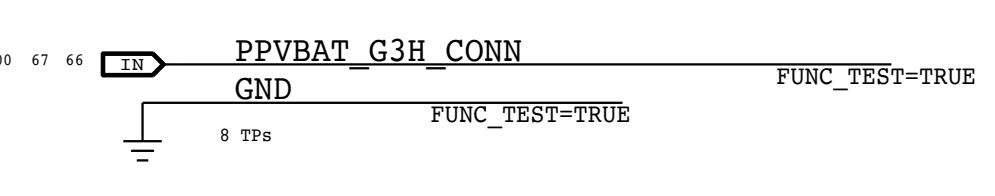
J6550 - Right Woofer Connector



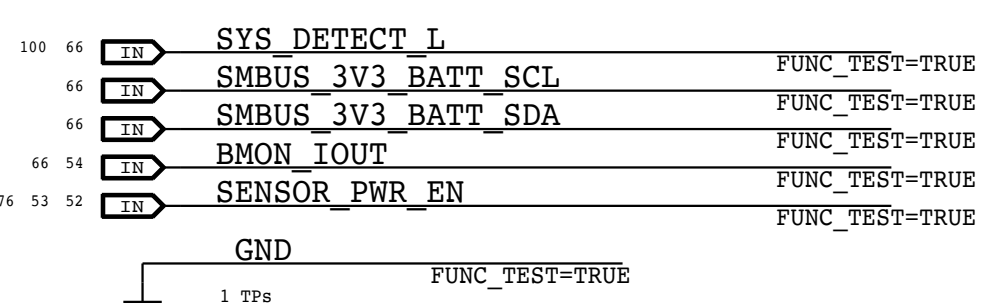
J6600 - Audio Jack Connector



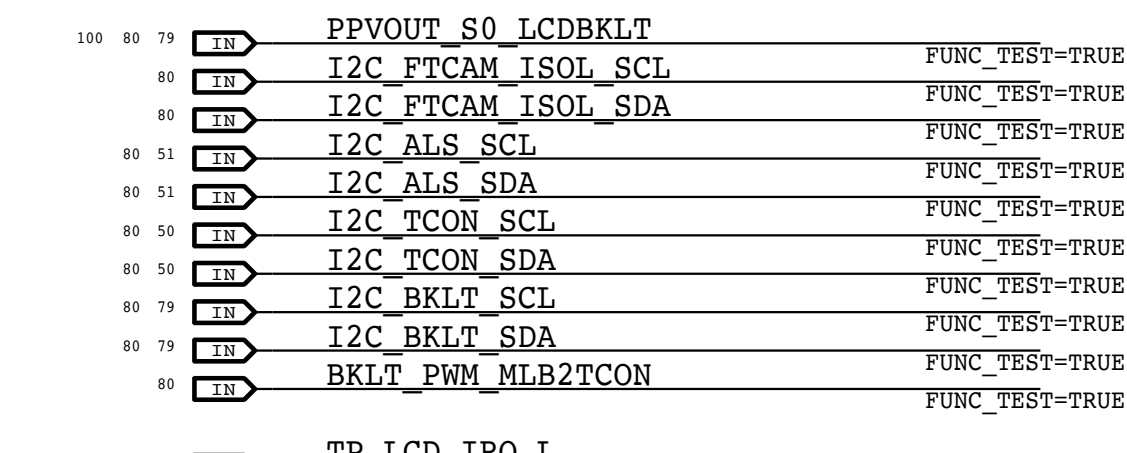
J6950 - Battery Connector



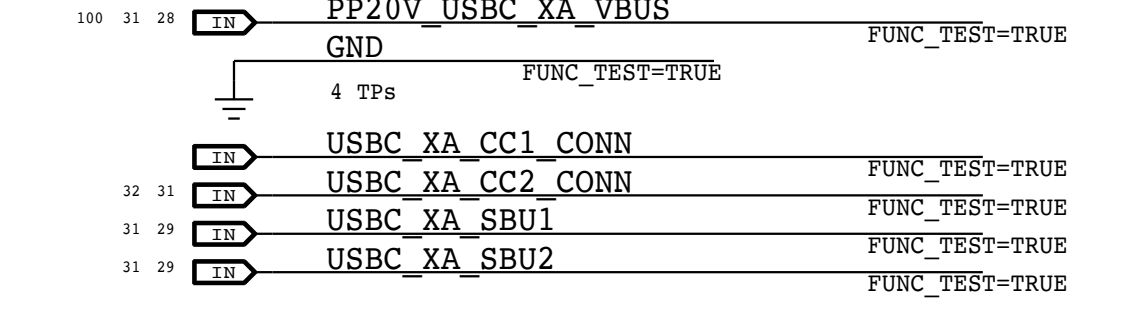
J6951 - Battery Sense Connector



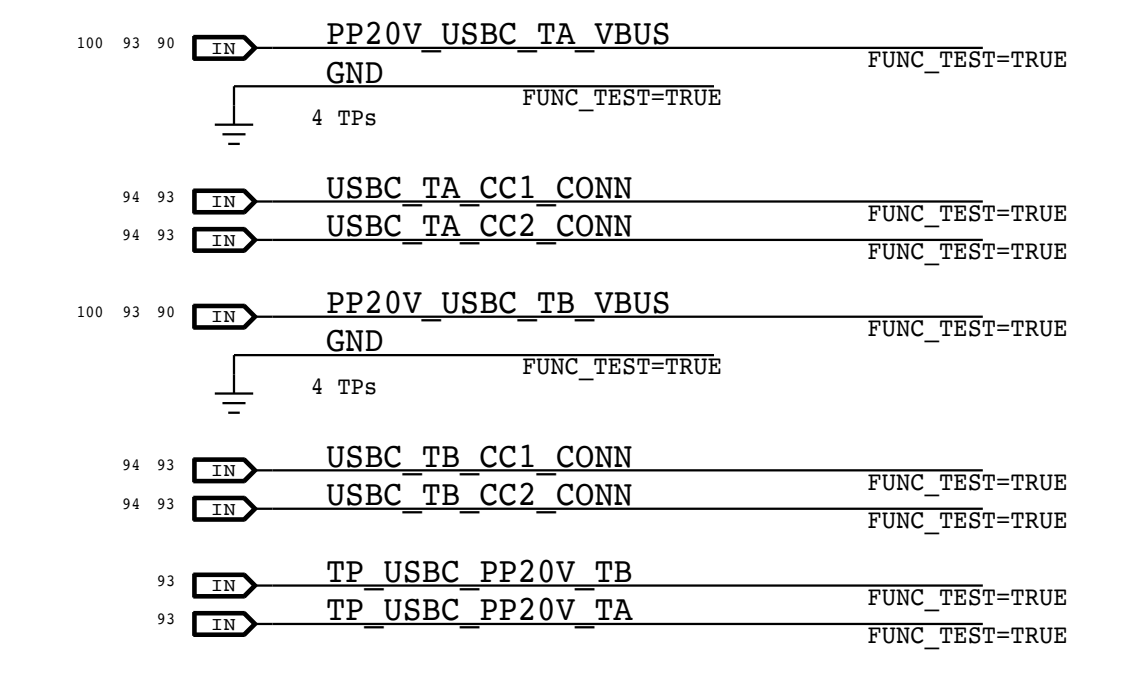
J8500 - eDP Connector



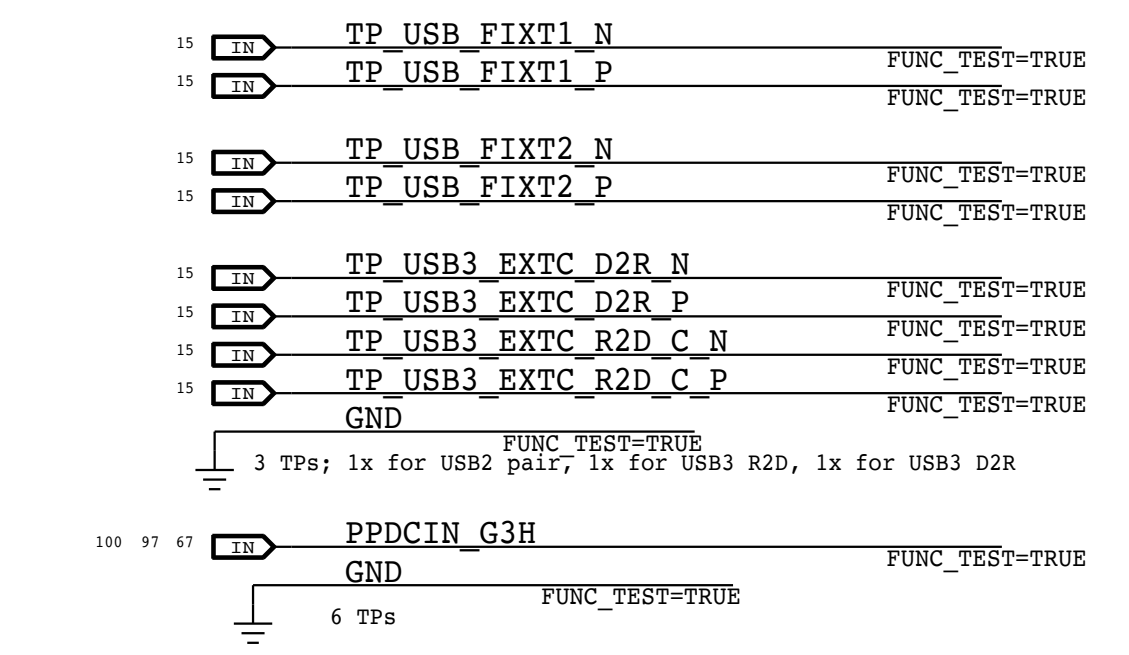
J3300 - Left USB-C Connector



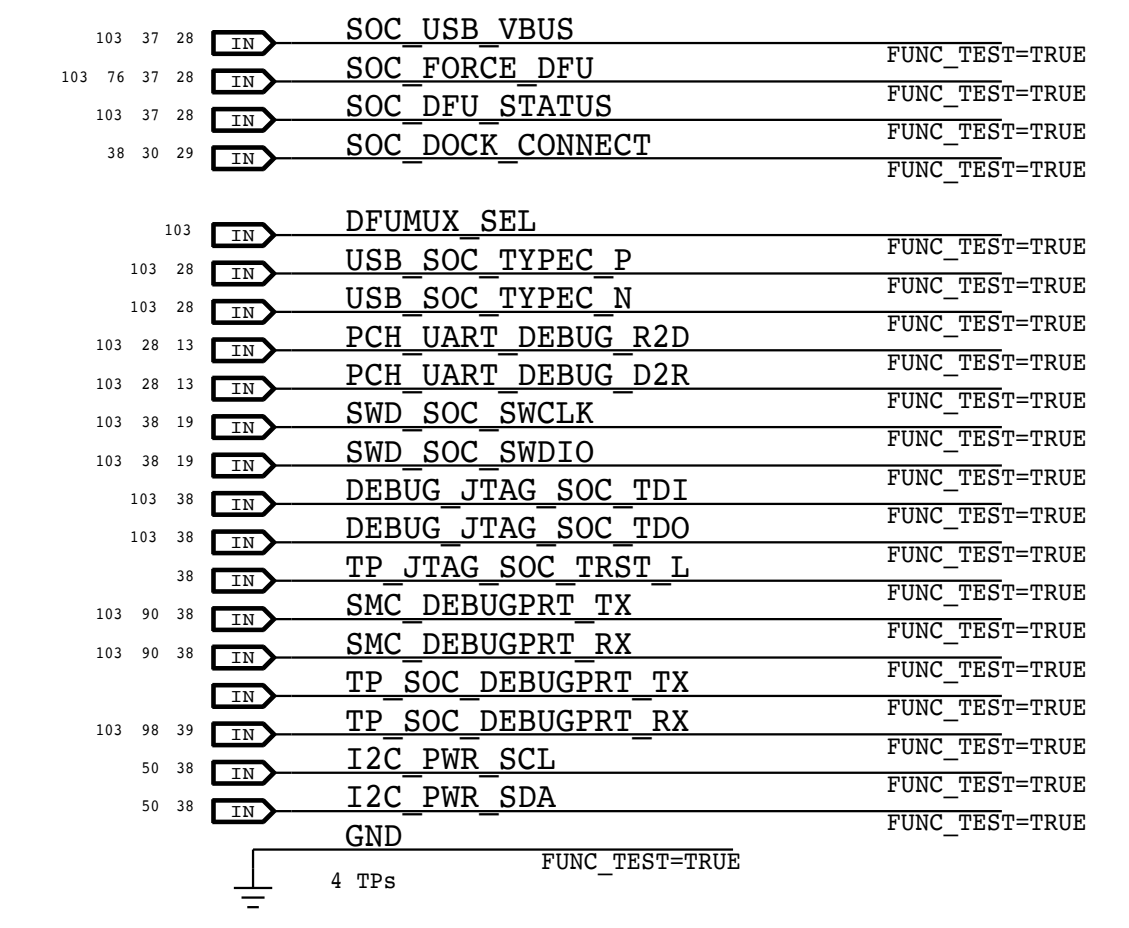
JB500 - Right USB-C Connector



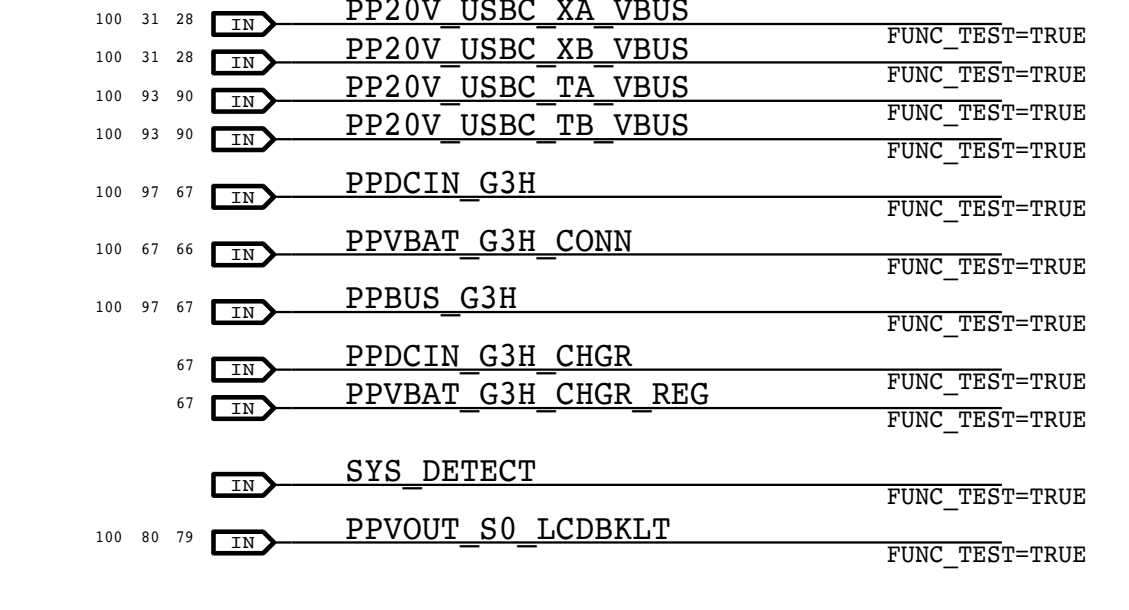
Probe Block Grid - DFU/SOC



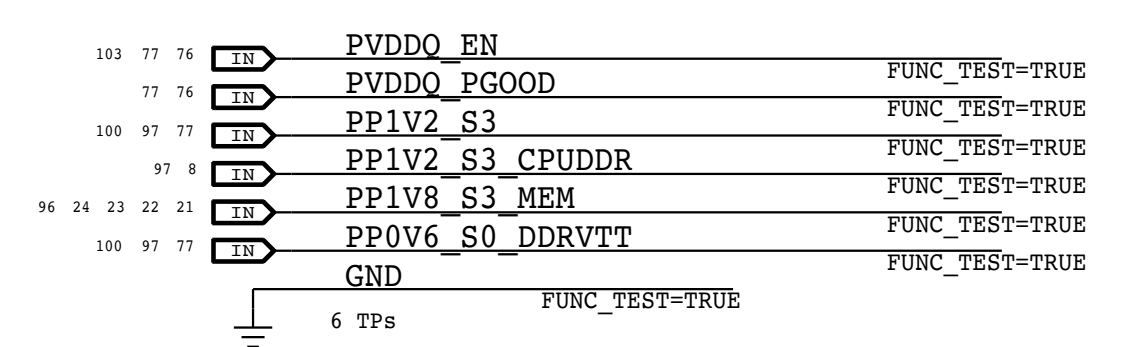
DFU/SOC/FCT DEBUG



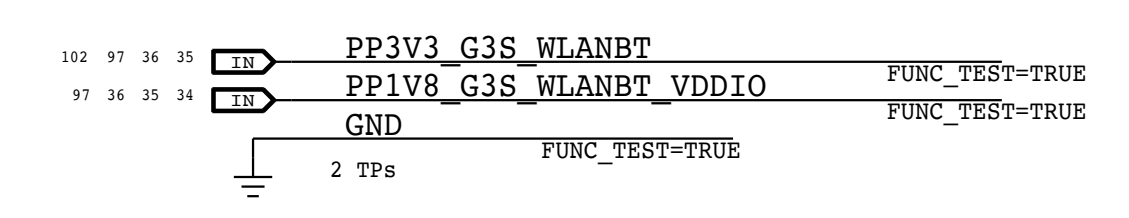
DFU/SOC/FCT DISCHARGE



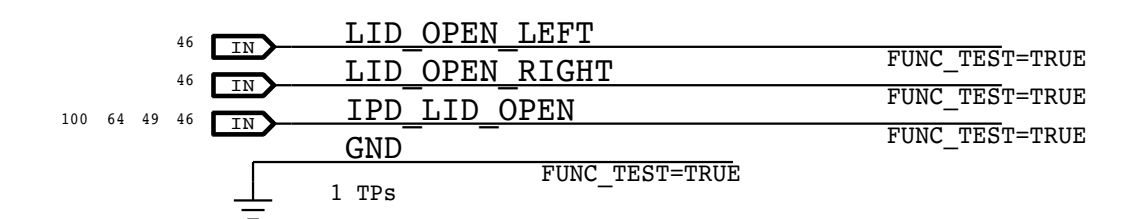
Memory Power



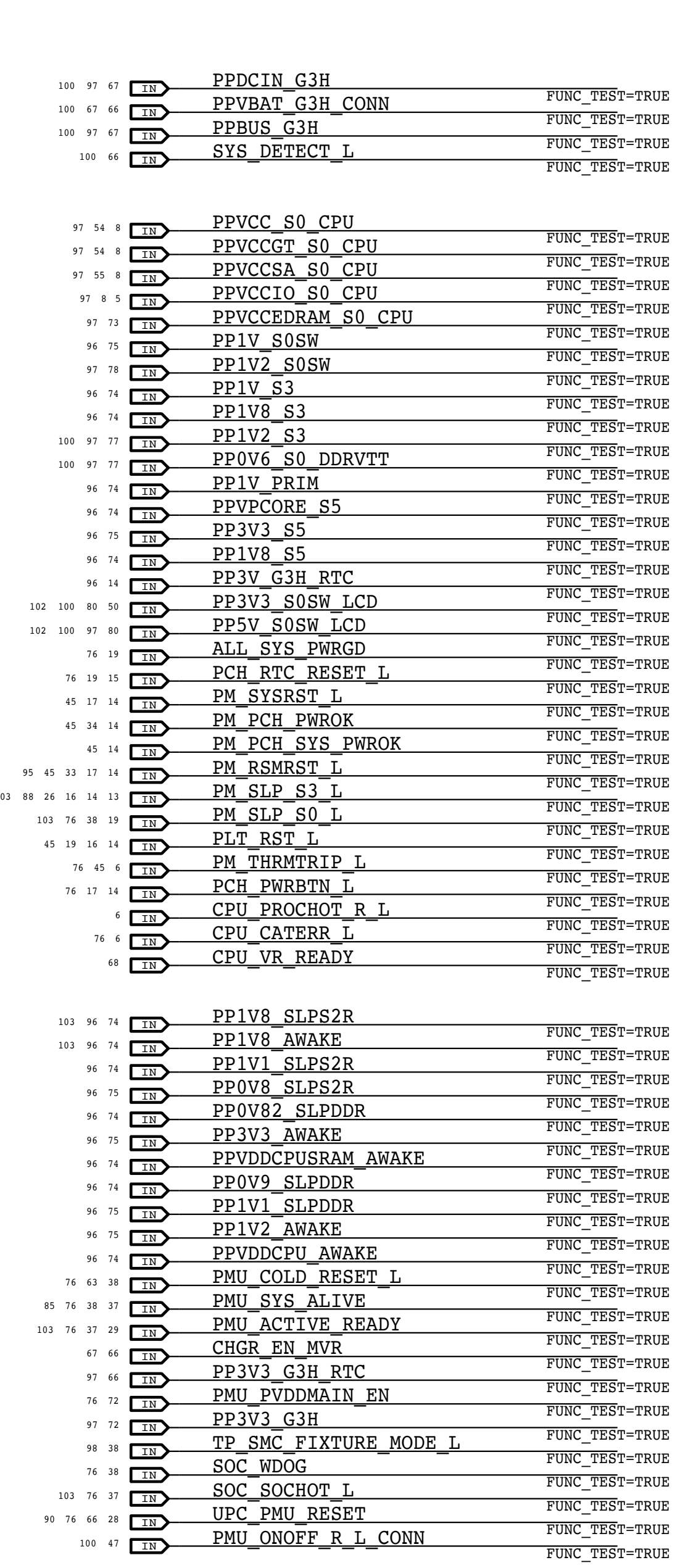
Wireless/BT Power



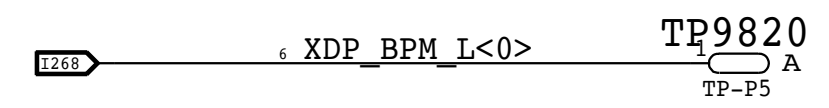
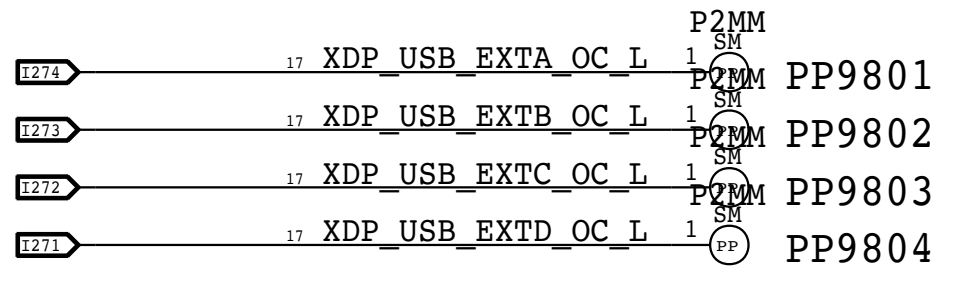
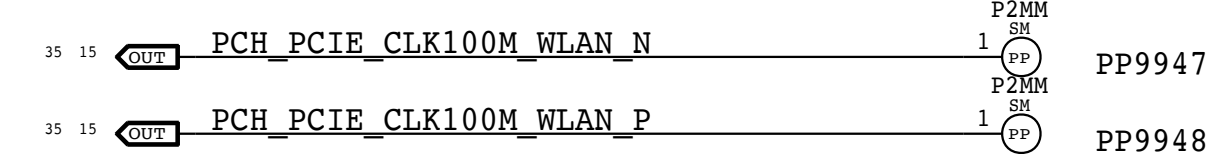
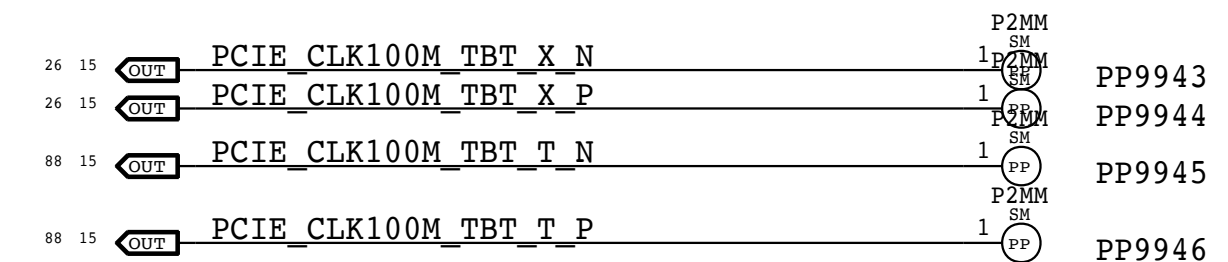
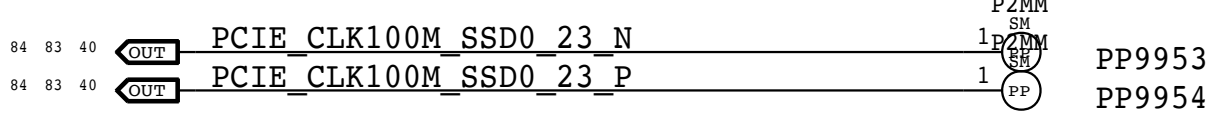
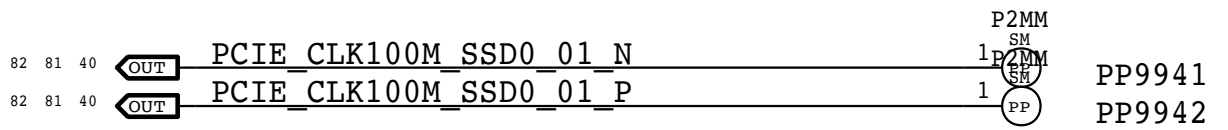
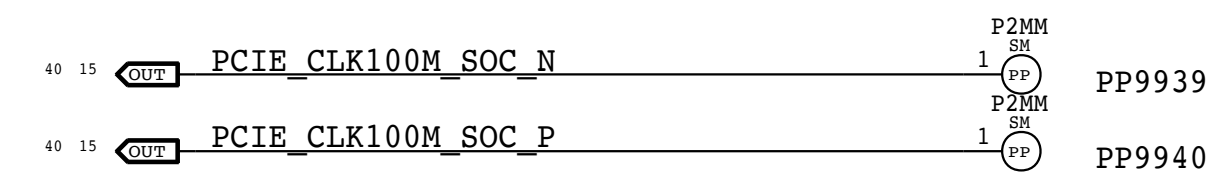
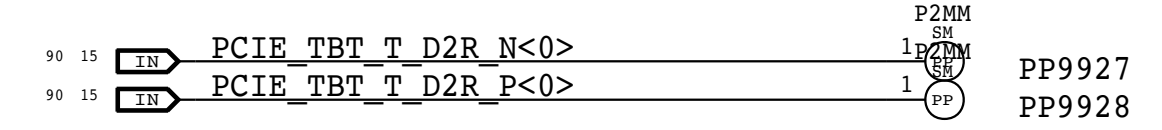
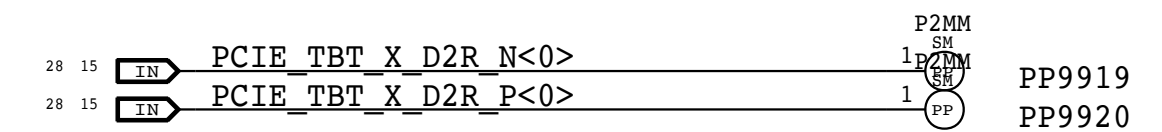
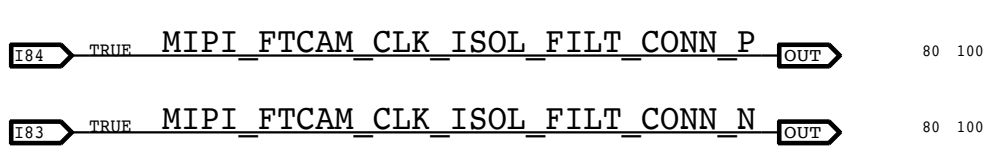
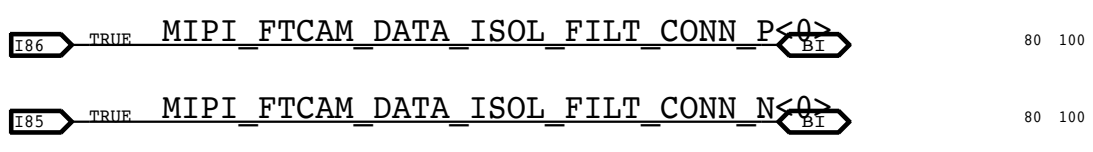
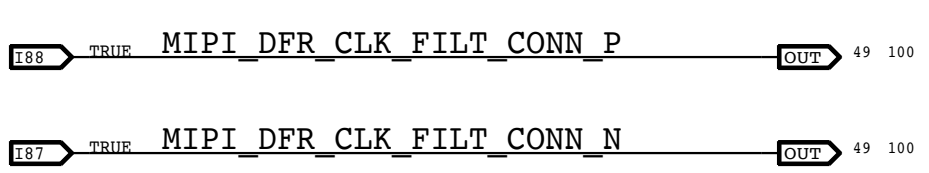
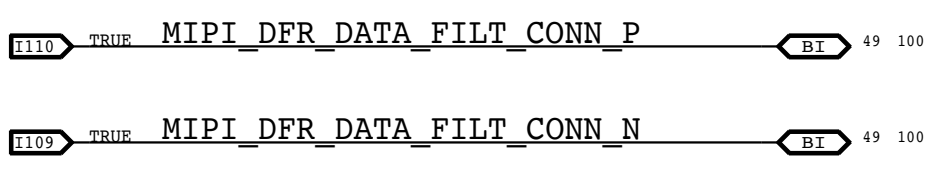
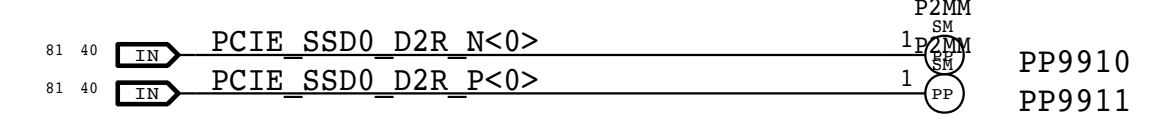
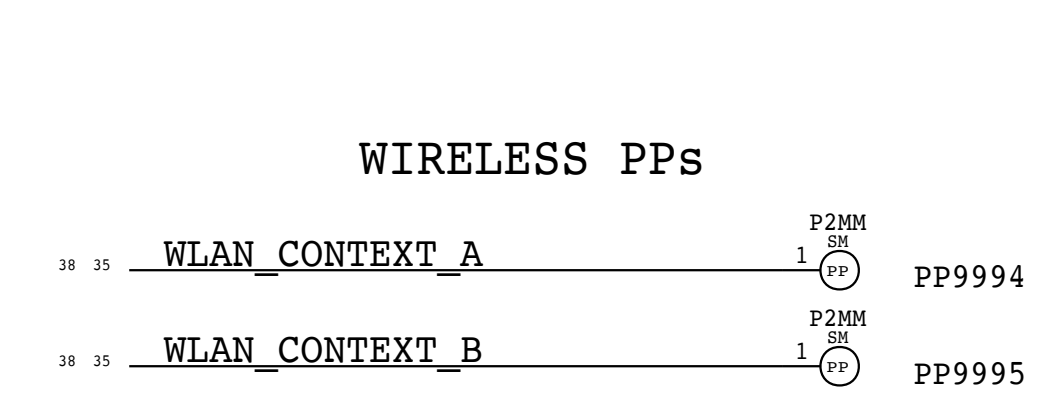
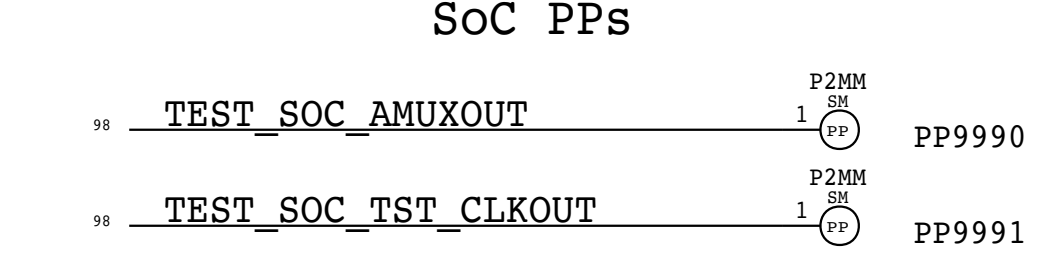
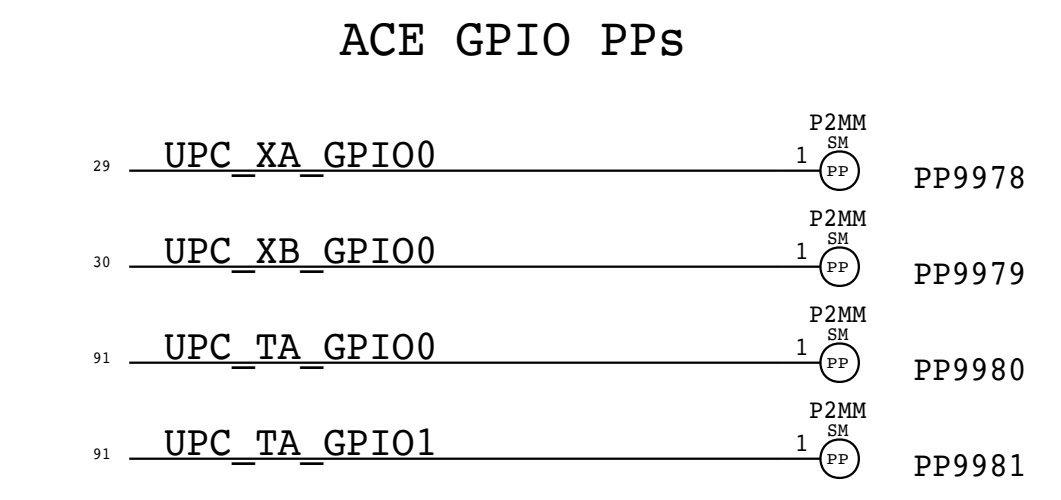
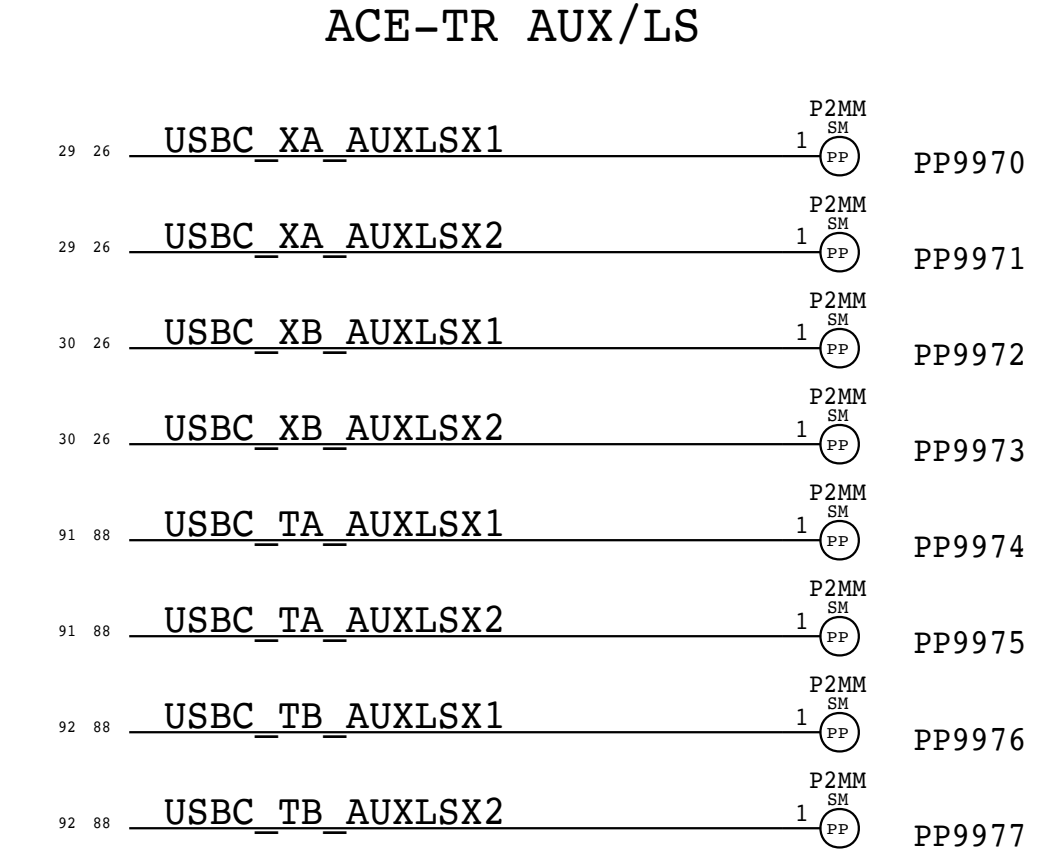
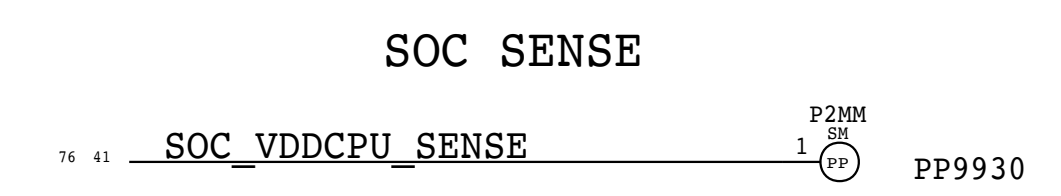
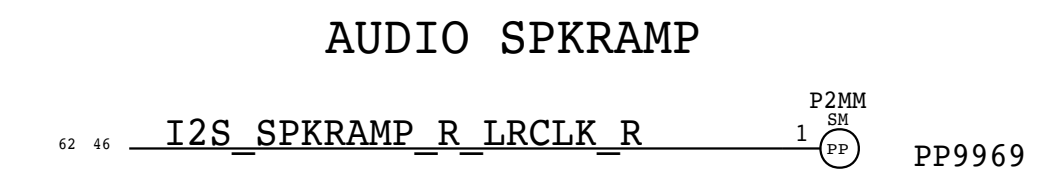
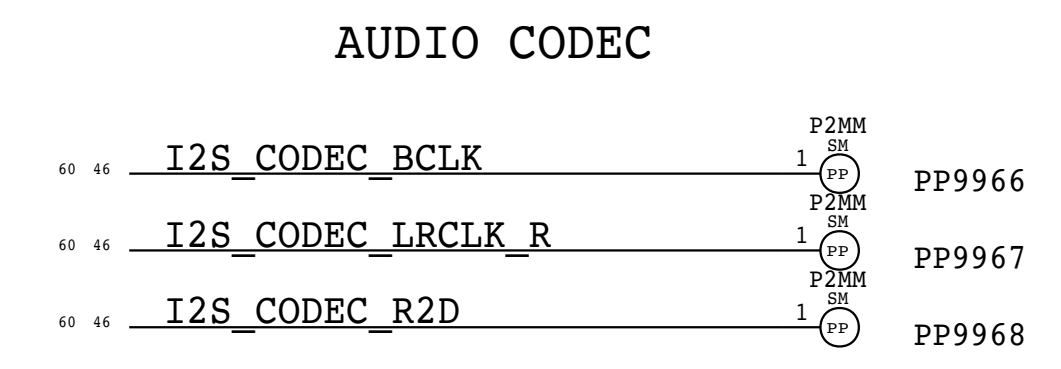
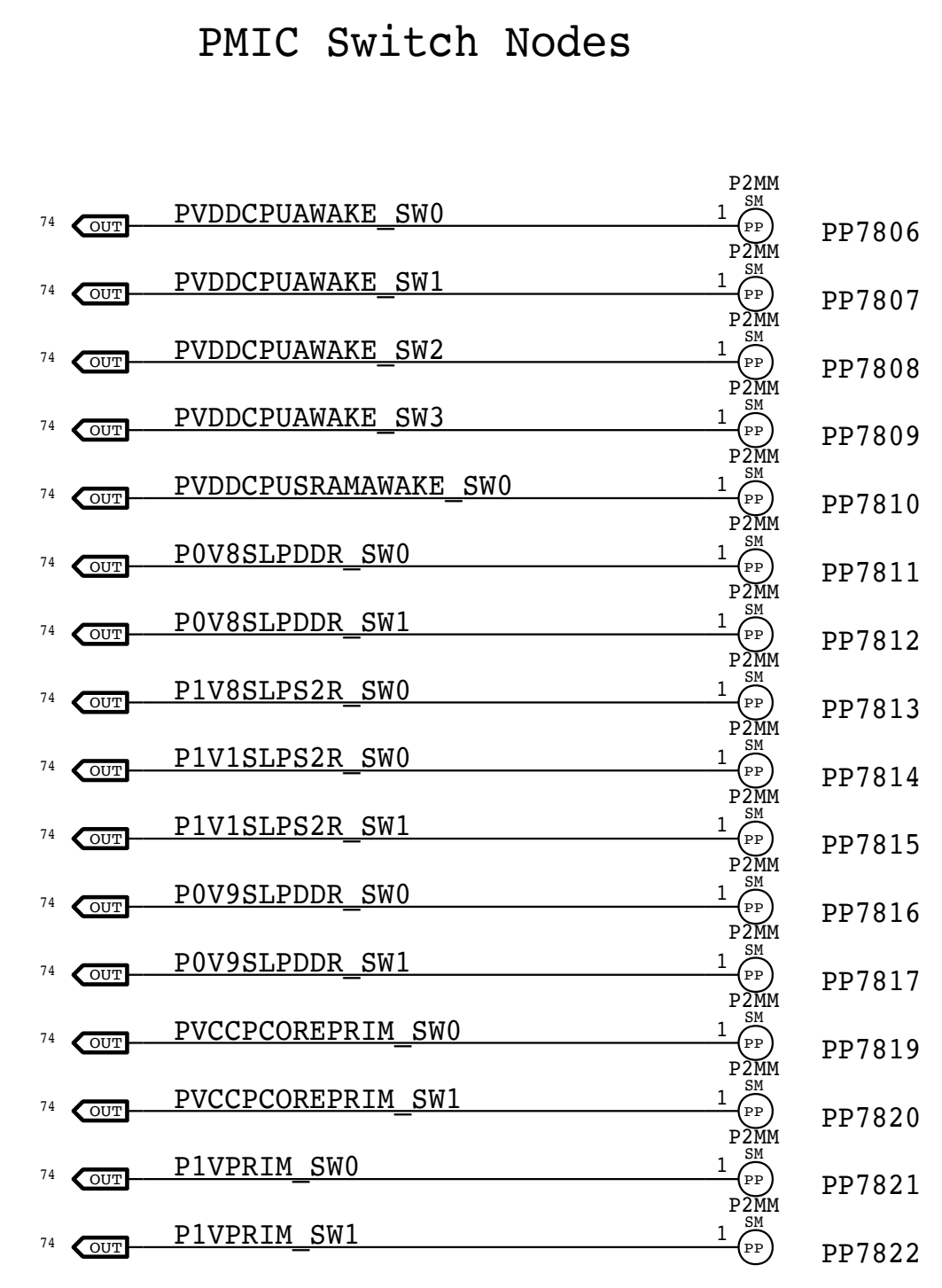
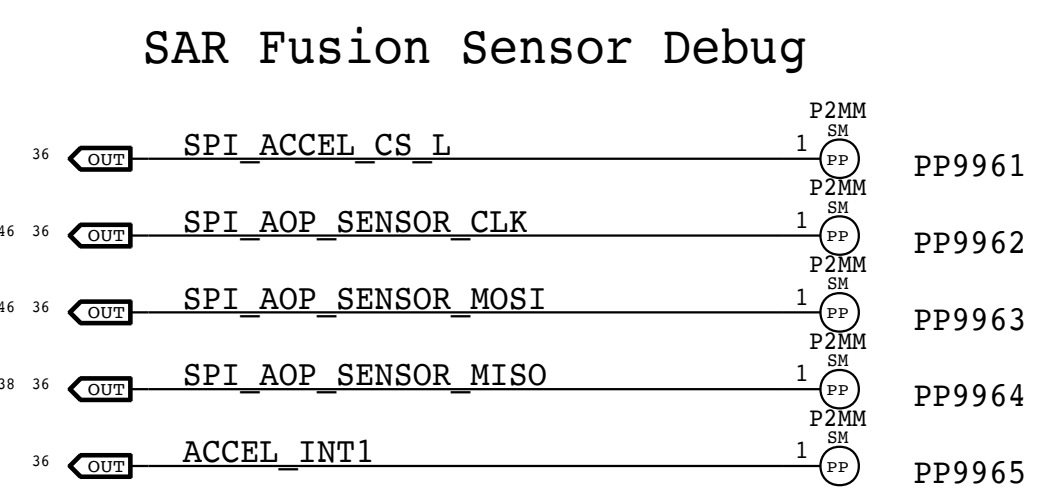
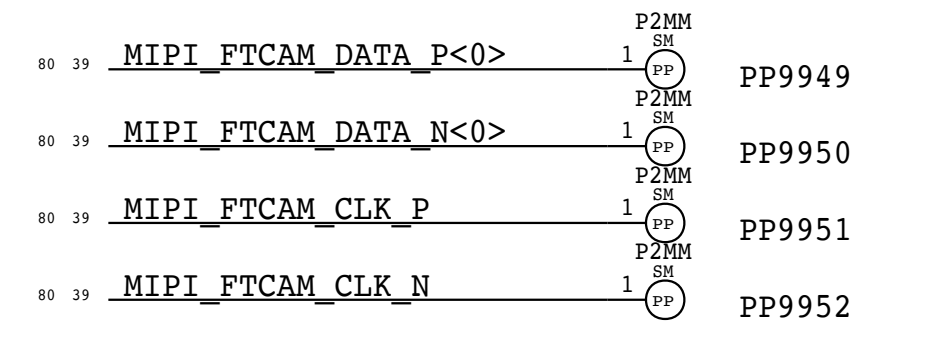
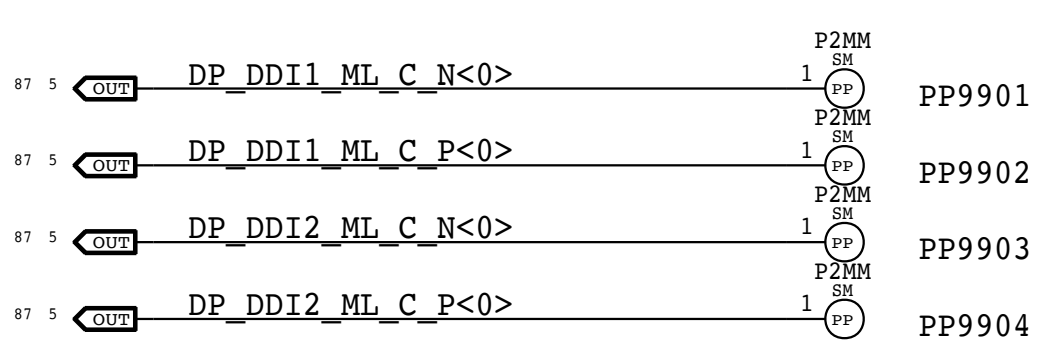
Hall Effect



DFU/SOC/FCT DMM/Power Sequence



ICT FCT 1
Apple Inc.
DRAWING NUMBER: 051-02166
REVISION: 4.0.0
BRANCH: evt-mars-0
PAGE: 124 OF 150
SHEET: 100 OF 108
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C

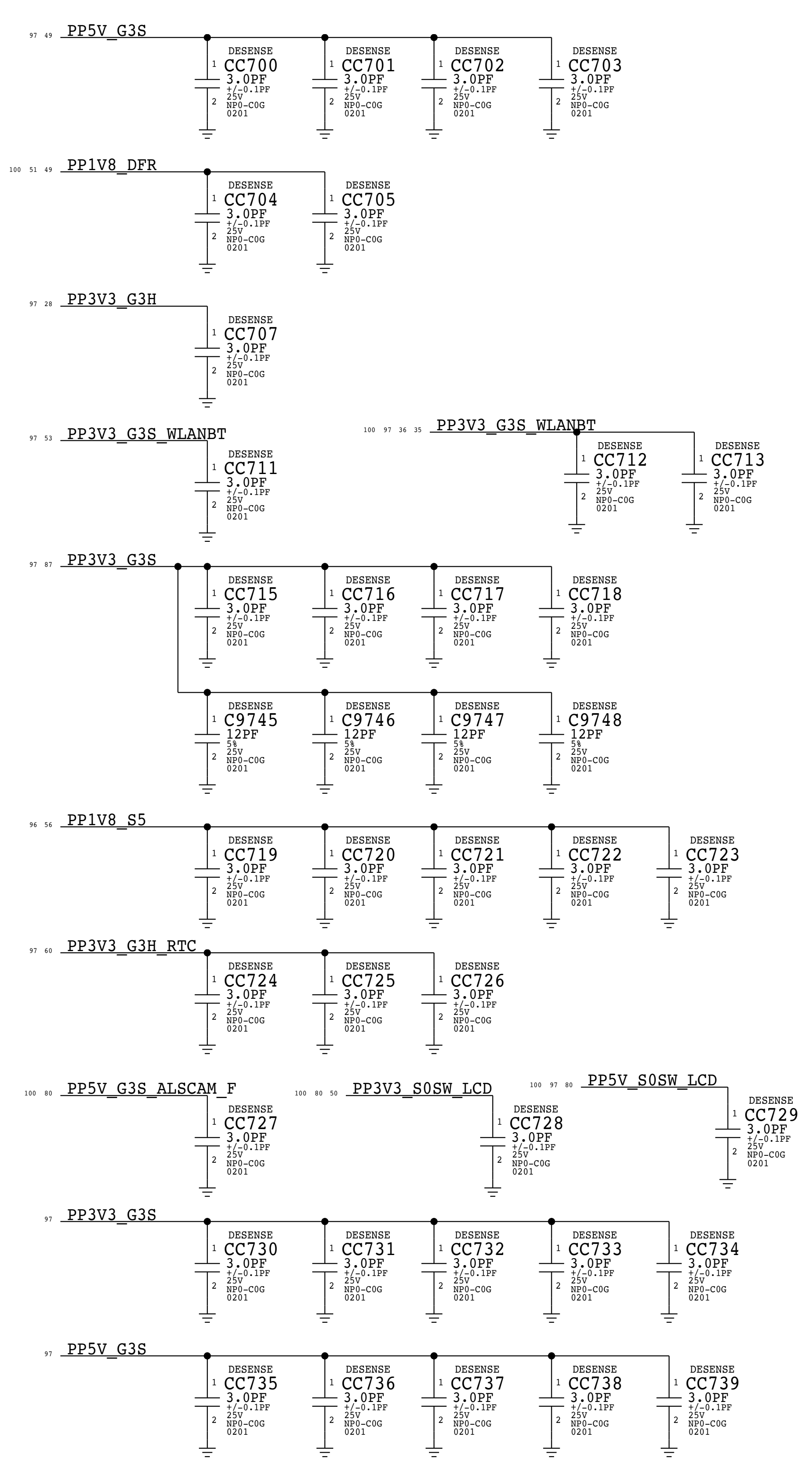
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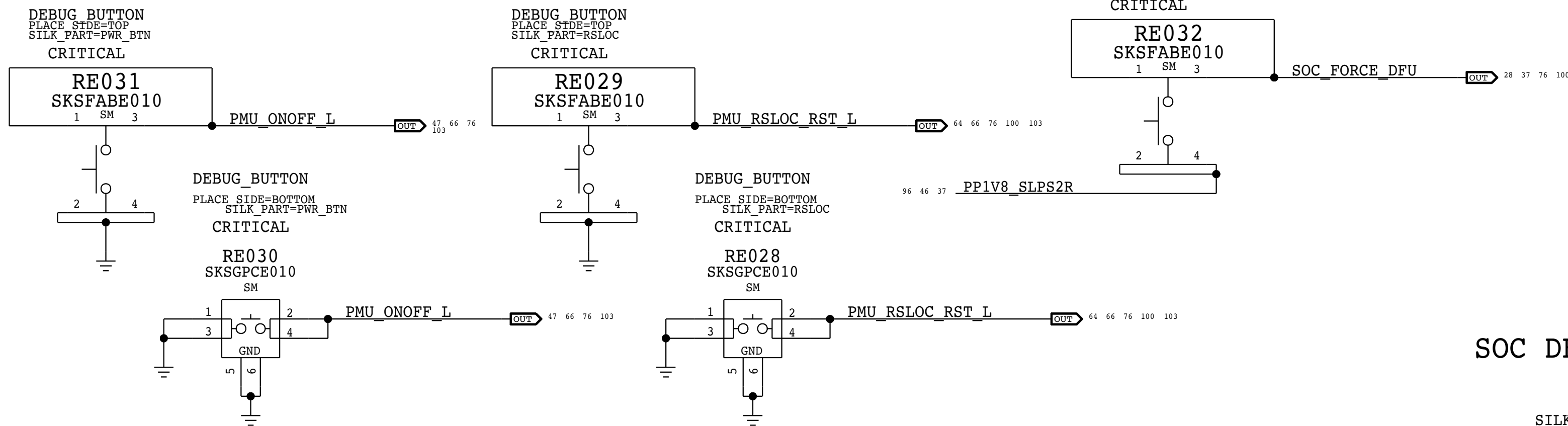
A



BOM_COST_GROUP=WIRELESS

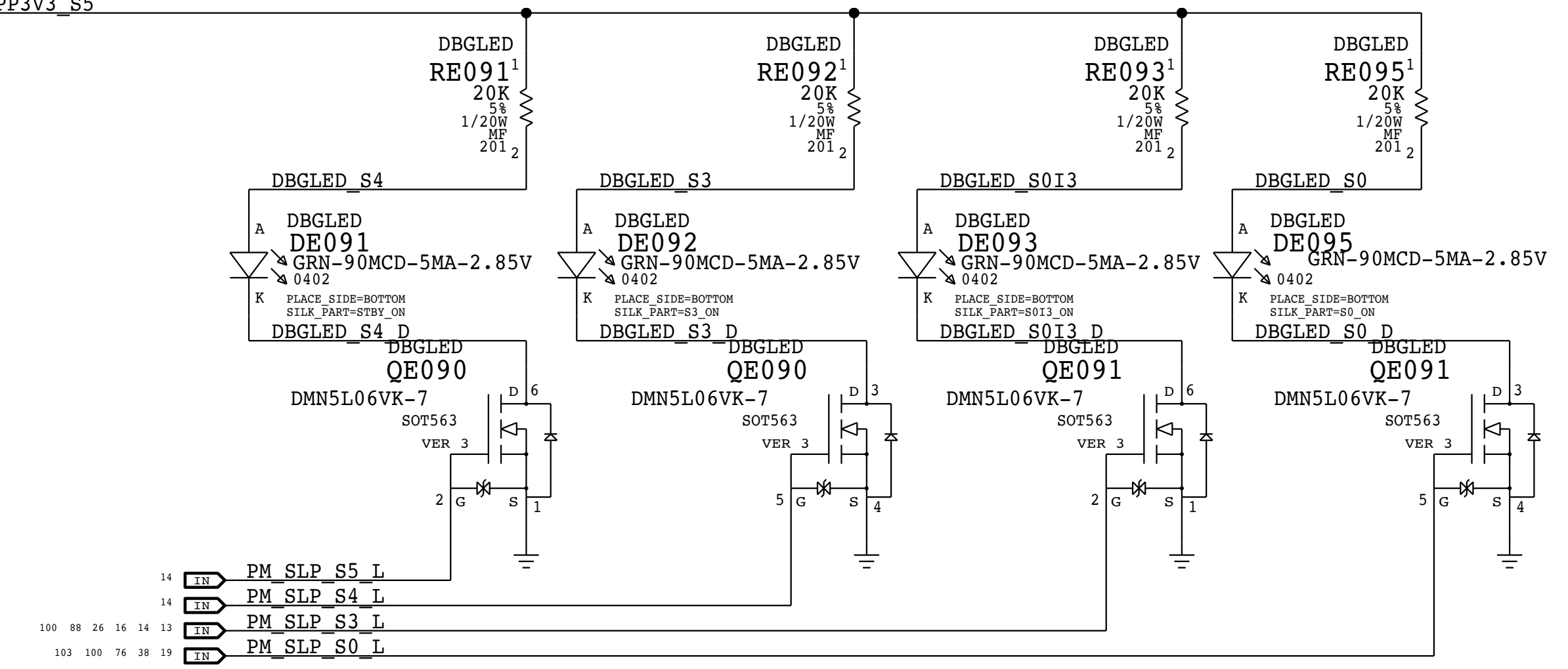
SYNC MASTER=YHARTANTO_J44		SYNC DATE=01/09/2013	
PAGE TITLE Desense Capacitors 1			
	DRAWING NUMBER 051-02166	SIZE D	
	REVISION 4.0.0		
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Debug Power "Buttons"

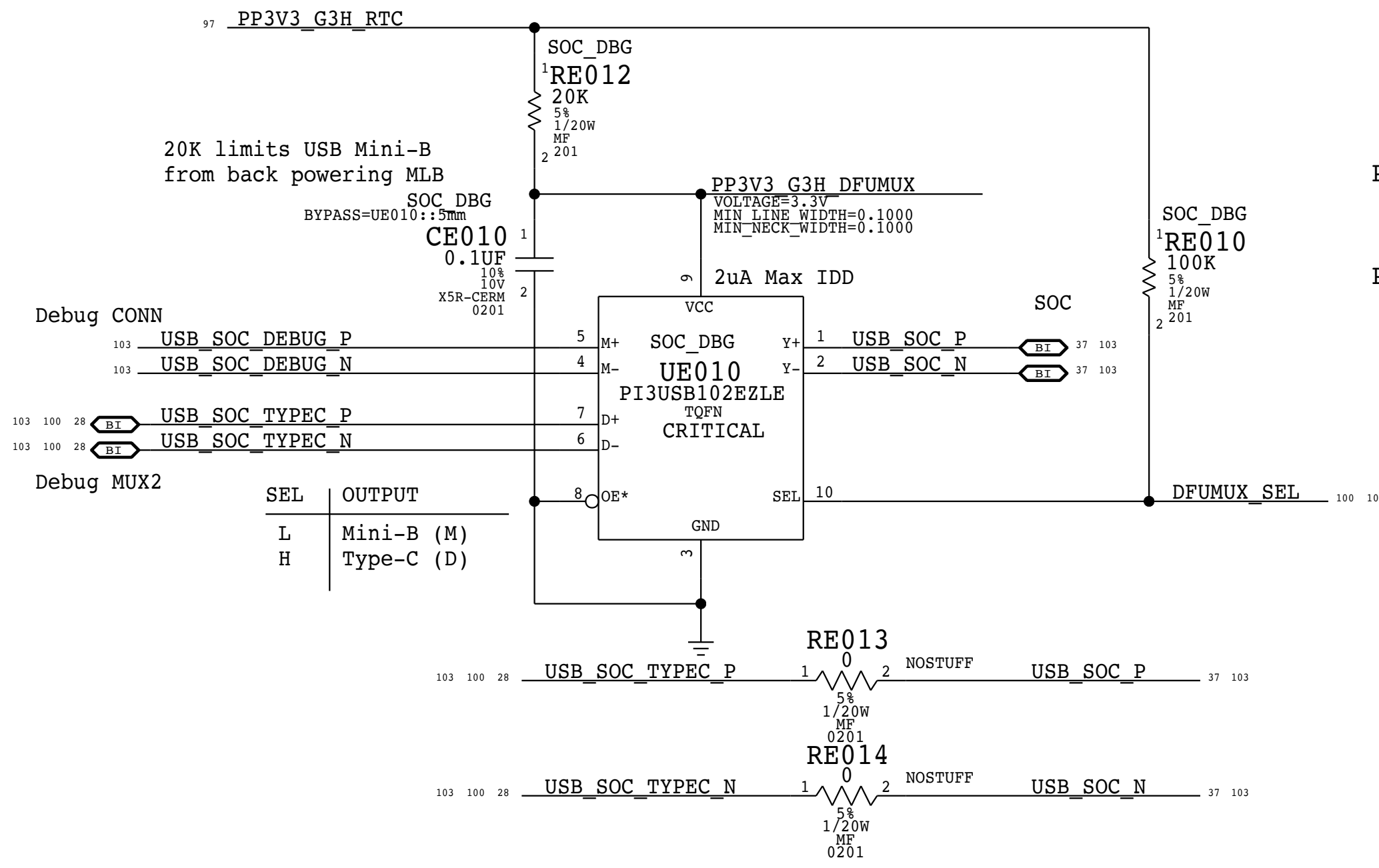


Power State Debug LEDs

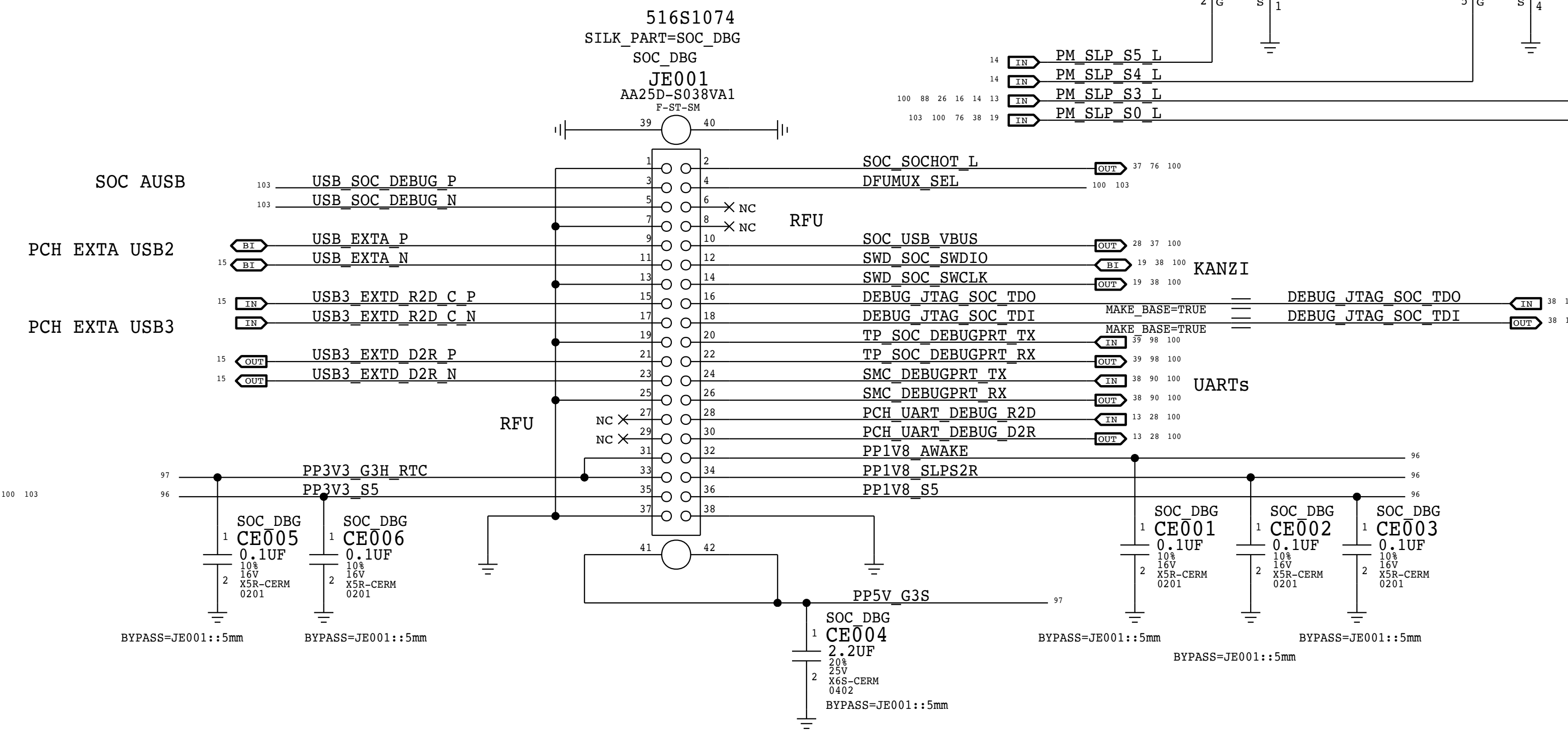
(For development only)



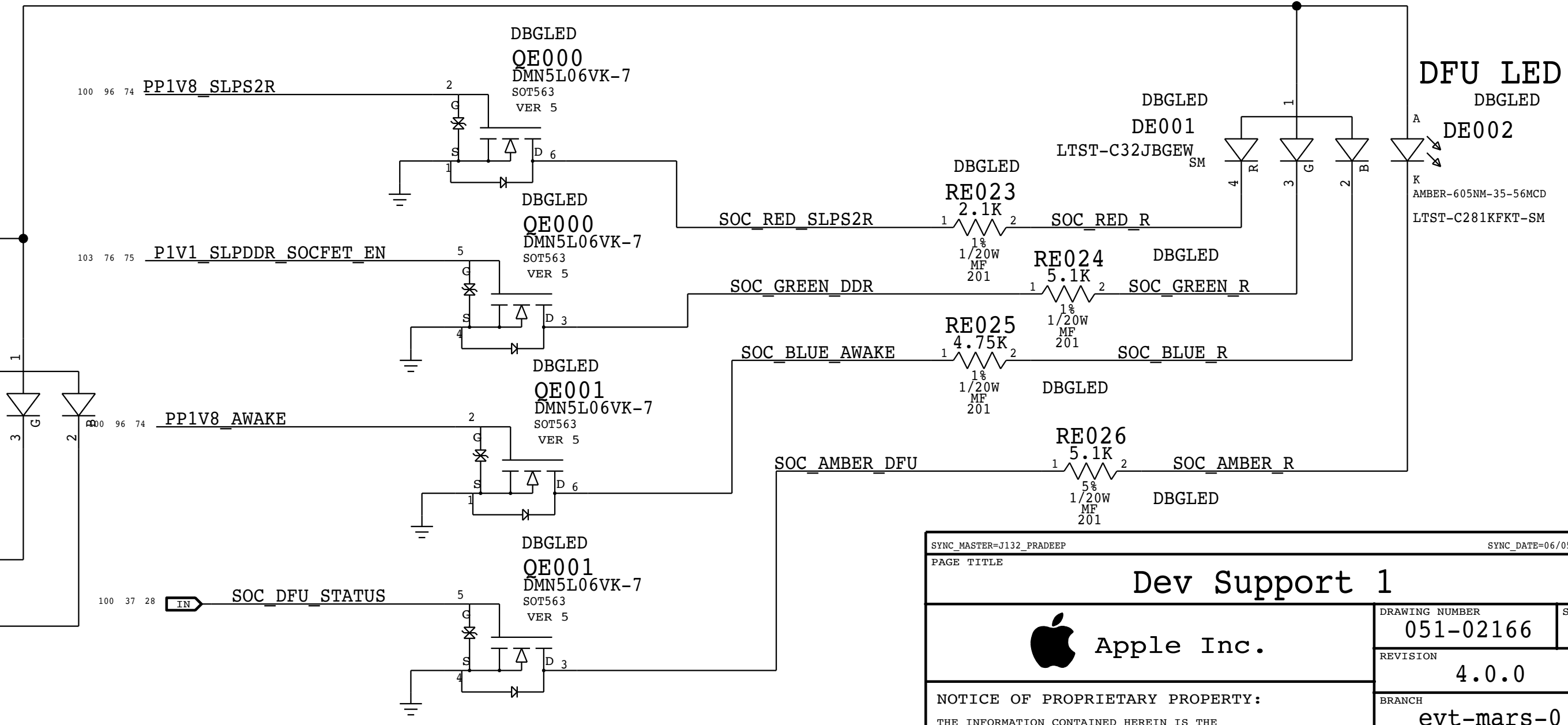
SoC USB DFU Mux



SOC DEBUG Connector

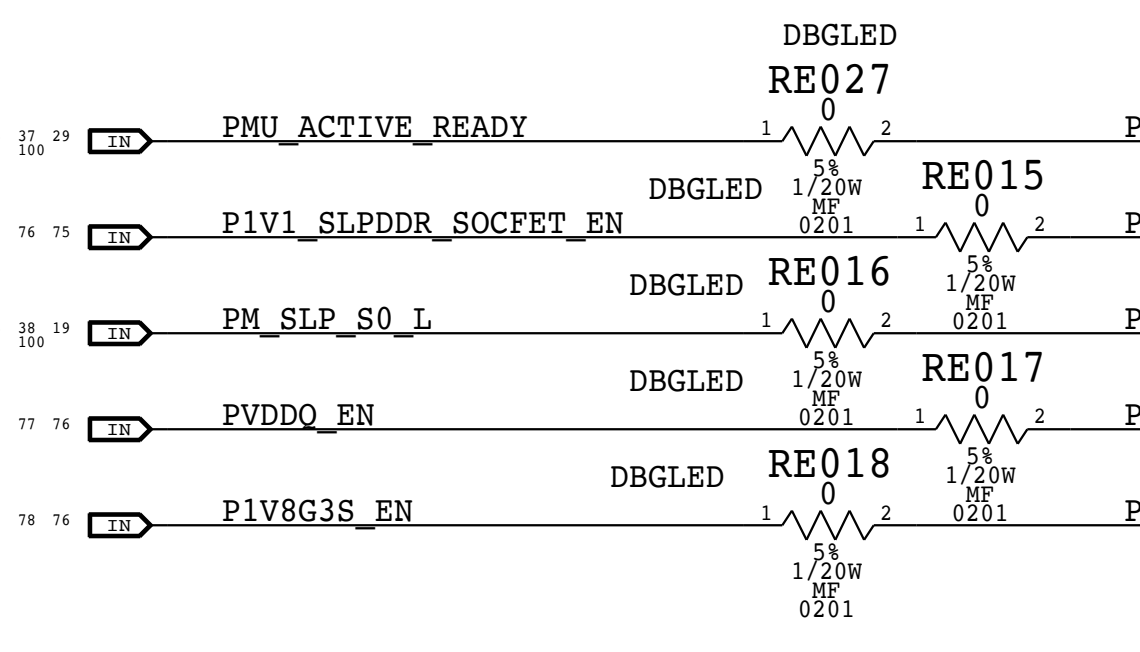
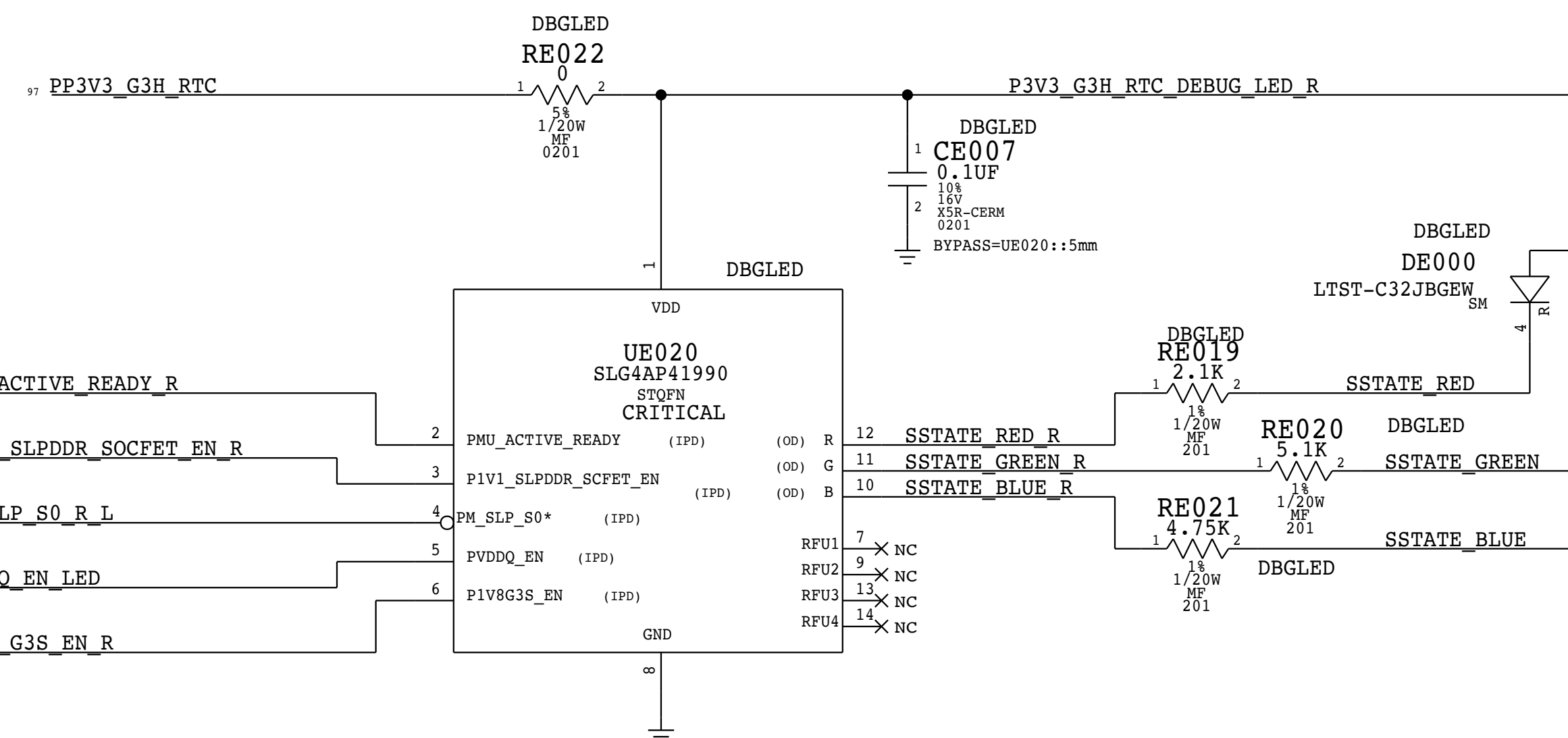


SOC State LEDs



System State LEDs

See color table on next page



		DRAWING NUMBER 051-02166	SIZE D
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PAGE TITLE <h3>Dev Support 1</h3>		PAGE 140 OF 150	SHEET 103 OF 108

BOM_COST_GROUP=DEBUG

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UE020 SAK Truth Table:

PMU_ACT_RDY	INPUTS				OUTPUTS (OD)			COLOR
	SLP_SCFET_EN	SLP_S0_L	VDDQ_EN	1V8G3S_EN	R	G	B	
0	0	0	0	0	BLINK	1	1	Blinking Red
0	0	0	0	1	0	1	1	Red
0	0	0	1	0	0	1	0	Magenta
0	0	0	1	1	0	0	0	White
0	0	1	0	0	0	1	0	Magenta
0	0	1	0	1	0	1	0	Magenta
0	0	1	1	0	0	1	0	Magenta
0	0	1	1	1	0	1	0	Magenta
0	1	0	0	0	0	1	0	Magenta
0	1	0	0	1	0	1	0	Magenta
0	1	0	1	0	0	1	0	Magenta
0	1	0	1	1	0	1	0	Magenta
0	1	1	0	0	0	1	0	Magenta
0	1	1	0	1	0	1	0	Magenta
0	1	1	1	0	0	1	0	Magenta
0	1	1	1	1	0	1	0	Magenta
0	1	1	1	1	0	1	0	Magenta
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1	0	0	0	1	0	1	0	Magenta
1	0	0	1	0	0	1	0	Magenta
1	0	0	1	1	0	1	0	Magenta
1	0	1	0	0	0	1	0	Magenta
1	0	1	0	1	0	1	0	Magenta
1	0	1	1	0	0	1	0	Magenta
1	0	1	1	1	0	1	0	Magenta
1	1	0	0	0	BLINK	0	1	Blinking Green & Yellow
1	1	0	0	1	0	0	1	Yellow
1	1	0	1	0	0	1	0	Magenta
1	1	0	1	1	1	1	0	Blue
1	1	1	0	0	0	1	0	Magenta
1	1	1	0	1	0	1	0	Magenta
1	1	1	1	0	0	1	0	Magenta
1	1	1	1	1	1	1	1	Green

SYNC MASTER=J79 RIO SYNC DATE=06/18/2015

PAGE TITLE		Dev Support 2	
 Apple Inc.	DRAWING NUMBER	051-02166	SIZE D
	REVISION	4.0.0	
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	PAGE	141 OF 150	
	SHEET	104 OF 108	

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BOM Variants

Table with 3 columns: BOM NUMBER, BOM NAME, BOM OPTIONS. Rows include variants like 685-00187 COMMON PARTS,MLB,X941 and 939-05022 PCBA,MLB,NO CPU,SS-8G,SD-256G,X941.


Table with 3 columns: BOM NUMBER, BOM NAME, BOM OPTIONS. Rows include variants like 639-05125 PCBA,MLB,2.3G,HY-8G,SD-256G,X941 and 639-05126 PCBA,MLB,2.3G,HY-8G,TO-256G,X941.

Table with 3 columns: BOM NUMBER, BOM NAME, BOM OPTIONS. Rows include variants like 639-05528 PCBA,MLB,2.5G,HY-8G,SD-256G,X941 and 639-05529 PCBA,MLB,2.5G,HY-8G,TO-256G,X941.

Apple Inc. BOM Variants 1 051-02166 4.0.0 evt-mars-0 142 OF 150 105 OF 108

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-05576	PCBA,MLB,2.6G,HY-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SD_256G
639-05577	PCBA,MLB,2.6G,HY-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:TO_256G
639-05578	PCBA,MLB,2.6G,MI-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SD_256G
639-05579	PCBA,MLB,2.6G,MI-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:TO_256G
639-05580	PCBA,MLB,2.6G,SS-8G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SD_256G
639-05581	PCBA,MLB,2.6G,SS-8G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:TO_256G
639-05582	PCBA,MLB,2.6G,HY-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SD_256G
639-05583	PCBA,MLB,2.6G,HY-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:TO_256G
639-05584	PCBA,MLB,2.6G,MI-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SD_256G
639-05585	PCBA,MLB,2.6G,MI-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:TO_256G
639-05586	PCBA,MLB,2.6G,SS-16G,SD-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SD_256G
639-05587	PCBA,MLB,2.6G,SS-16G,TO-256G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:TO_256G
639-05588	PCBA,MLB,2.6G,HY-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SD_512G
639-05589	PCBA,MLB,2.6G,HY-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:TO_512G
639-05590	PCBA,MLB,2.6G,MI-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SD_512G
639-05591	PCBA,MLB,2.6G,MI-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:TO_512G
639-05592	PCBA,MLB,2.6G,SS-8G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SD_512G
639-05593	PCBA,MLB,2.6G,SS-8G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:TO_512G
639-05594	PCBA,MLB,2.6G,HY-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SD_512G
639-05595	PCBA,MLB,2.6G,HY-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:TO_512G
639-05596	PCBA,MLB,2.6G,MI-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SD_512G
639-05597	PCBA,MLB,2.6G,MI-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:TO_512G
639-05598	PCBA,MLB,2.6G,SS-16G,SD-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SD_512G
639-05599	PCBA,MLB,2.6G,SS-16G,TO-512G,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:TO_512G
639-05600	PCBA,MLB,2.6G,HY-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SD_1T
639-05601	PCBA,MLB,2.6G,HY-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SS_1T
639-05602	PCBA,MLB,2.6G,HY-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:TO_1T
639-05603	PCBA,MLB,2.6G,MI-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SD_1T
639-05604	PCBA,MLB,2.6G,MI-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SS_1T
639-05605	PCBA,MLB,2.6G,MI-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:TO_1T
639-05606	PCBA,MLB,2.6G,SS-8G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SD_1T
639-05607	PCBA,MLB,2.6G,SS-8G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SS_1T
639-05608	PCBA,MLB,2.6G,SS-8G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:TO_1T
639-05609	PCBA,MLB,2.6G,HY-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SD_1T
639-05610	PCBA,MLB,2.6G,HY-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SS_1T
639-05611	PCBA,MLB,2.6G,HY-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:TO_1T
639-05612	PCBA,MLB,2.6G,MI-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SD_1T
639-05613	PCBA,MLB,2.6G,MI-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SS_1T
639-05614	PCBA,MLB,2.6G,MI-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:TO_1T
639-05615	PCBA,MLB,2.6G,SS-16G,SD-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SD_1T
639-05616	PCBA,MLB,2.6G,SS-16G,SS-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SS_1T
639-05617	PCBA,MLB,2.6G,SS-16G,TO-1T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:TO_1T
639-05618	PCBA,MLB,2.6G,HY-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_8G,NANDCFG:SS_2T
639-05619	PCBA,MLB,2.6G,MI-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_8G,NANDCFG:SS_2T
639-05620	PCBA,MLB,2.6G,SS-8G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_8G,NANDCFG:SS_2T
639-05621	PCBA,MLB,2.6G,HY-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:HY_16G,NANDCFG:SS_2T
639-05622	PCBA,MLB,2.6G,MI-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:MI_16G,NANDCFG:SS_2T
639-05623	PCBA,MLB,2.6G,SS-16G,SS-2T,X941	BASE_BOM,DEVEL_BOM,ALTERNATE,CPU:2.6G,DRAMCFG:SS_16G,NANDCFG:SS_2T

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Alternate Parts
System EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
10380221	10380276		ALL	
103800248	103800247		ALL	8.06K 0.1% RESISTOR
103800250	103800249		ALL	18.2K 0.1% RESISTOR
10780284	107800021	SENSOR:DEV	ALL	TFT w/ Yageo
107800101	107800005	SENSOR:DEV	ALL	Cyntec w/ Yageo
107800102	107800017	SENSOR:DEV	ALL	Cyntec w/ Yageo
10780276	107800020	SENSOR:DEV	ALL	Cyntec w/ TFT
107800086	107800056	ANY	ALL	TFT w/ Cyntec
107800100	107800057		ALL	Cyntec w/ TFT
107800103	107800058	SENSOR:DEV	ALL	Cyntec w/ Yageo
107800070	10780085		ALL	100K THERMISTOR
132800202	132800175		ALL	
138800084	138800060		ALL	
138800117	138800071		ALL	
13880714	13880713		ALL	Murata w/ Samsung
13880715	13880732		ALL	Murata w/ Samsung
13880706	13880739		ALL	NEC w/ Vishay
13880945	13880739		ALL	NEC w/ Rohm
138800049	13880831	ANY	ALL	
138800006	13880835		ALL	
138800086	13880884		ALL	
138800104	13880978		ALL	Murata w/ Taiyo
138800056	13881100		ALL	
152800369	152800268		ALL	Cyntec w/ NEC
152800403	152800322		ALL	Murata w/ Chillisin
152800864	152800851		ALL	
152800434	15281829		ALL	
15580665	155800232		ALL	
155800166	15580391		ALL	
155800018	15580664		ALL	Murata w/ Taiyo
155800007	15580667		ALL	
15580914	15580897		ALL	
155800190	15580897		ALL	
197800046	197800036		ALL	Epson w/ TXC
197800047	197800036		ALL	Kyocera w/ TXC
197800048	197800036		ALL	Murata w/ TXC
197800053	197800050		ALL	Kyocera w/ TXC
197800054	197800050		ALL	NDK w/ TXC
197800055	197800050		ALL	Murata w/ TXC
197800120	197800118		ALL	
31180426	311800007		ALL	
311800104	311800091	ANY	ALL	
311800156	311800129		ALL	
311800196	311800195		ALL	
311800060	31180273		ALL	
311800121	31180398		ALL	
311800138	31180436		ALL	
311800013	31180508		ALL	NXP w/ Diodes
335800270	335800203		ALL	
335800213	33580888		ALL	
353800878	353800599		ALL	
353800879	353800754		ALL	
353800750	353800877		ALL	
353801041	353801042		ALL	
353801346	353801320		ALL	
353801506	353801404	ANY	ALL	
353800107	35383239	ANY	ALL	Onsemi alt to Intersil
353800636	35384037	ANY	ALL	
353800772	35384068		ALL	
371800089	371800085		ALL	

System EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371800170	371800125		ALL	
371800127	371800182		ALL	
372800016	372800015		ALL	
37280186	37280185		ALL	
376800219	376800079		ALL	
376800292	376800294		ALL	
37681080	37680820		ALL	
376800074	37680855		ALL	
376800146	37681061		ALL	NXP w/ Diodes
376800282	37681128		ALL	
377800079	377800077		ALL	
377800077	37780183		ALL	Infineon w/ ST
740800033	740800002		ALL	
740800019	740800007		ALL	Bourns w/ Polytronics
740800003	74080135		ALL	

Audio

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
13880700	13880641		ALL	Murata w/ SS&Taiyo
13880660	13880684		ALL	
13880689	13880701		ALL	
13881103	13880719		ALL	
15580694	15580387		ALL	
15580660	15580513		ALL	
155800034	15580706		ALL	Taiyo w/ Murata
155800203	15580894		ALL	
31180271	311800008		ALL	

BLC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107800033	107800034		ALL	
13880738	13881101		ALL	Samsung alt to Murata
13880846	13880811		ALL	Samsung alt to Murata
152800359	152800253		ALL	Chillisin alt to Cyntec
353801615	35384160		ALL	Aizu alt to Maine
371800180	371800077		ALL	NXP alt to Diodes
37681053	37680604		ALL	Diodes alt to Fairchild
37681106	37680678		ALL	Fairchild alt to Vishay
740800041	74080159		ALL	

WIRELESS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138800024	13880986		ALL	
152800769	152800659		ALL	
152800770	15280857		ALL	
155800067	155800401		ALL	
339800428	339800458		ALL	

DC-DC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107800015	107800011		ALL	
107800087	107800029		ALL	TFT w/ Yageo
107800071	107800053		ALL	
107800139	10780178		ALL	
10780249	10780251		ALL	
128800009	128800007		ALL	
128800070	128800007		ALL	
128800026	128800011		ALL	
128800031	128800011		ALL	
128800087	128800011		ALL	
12880302	128800038		ALL	
128800039	128800038		ALL	
128800062	128800067		ALL	
128800065	128800067		ALL	
128800069	128800067		ALL	
12880364	12880264		ALL	Kemet w/ Panasonic
12880578	12880351		ALL	
128800050	12880351		ALL	
132800012	13280401		ALL	
132800064	13280409		ALL	
138800077	138800035		ALL	
138800093	138800035		ALL	
138800111	138800036		ALL	
138800047	138800073		ALL	
138800229	138800107		ALL	
13880786	13880705		ALL	Murata w/ Samsung
138800097	13880750		ALL	
13880863	13880853		ALL	
13880775	13880860		ALL	
13880789	13880941		ALL	Murata w/ SS
152800363	152800048		ALL	Cyntec w/ Vishay
152800388	152800182		ALL	
152800703	152800182		ALL	
152800383	152800198		ALL	
152800680	152800198		ALL	
152800398	152800204		ALL	
152800841	152800238		ALL	
152800765	152800239		ALL	
152800368	152800269		ALL	
152800724	152800311		ALL	
152800786	152800344		ALL	
152800725	152800590		ALL	
152800726	152800592		ALL	
152800707	152800689		ALL	
31180596	31180593		ALL	NXP w/ Diodes
311800192	311800191		ALL	
311800193	311800191		ALL	
353800831	353800519		ALL	
353800796	353800497		ALL	
353800832	353800525		ALL	
376800303	376800012		ALL	
376800204	376800203		ALL	
376800226	376800203		ALL	
376800227	376800203		ALL	
376800302	37681038		ALL	
376800281	37681147		ALL	
376800007	37681179		ALL	
376800228	37681179		ALL	
376800304	37681187		ALL	
74080144	74080118		ALL	
740800028	74080118		ALL	

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Confluence:

<https://confluence.apple.com/confluence/display/J79EE/Mac+HW+EE+Home>

Kismet:

<AFP://KISMET.APPLE.COM/KISMET-PROJECTS/J79>

Useful Wiki Links:

Schematic Conventions - <https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions>

Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

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- <rdar://component/XXXXXX> J132 HW EE BOM | Proto 0
- <rdar://component/XXXXXX> J132 HW EE Characterization | Proto 0
- <rdar://component/XXXXXX> J132 HW EE Layout | Proto 0
- <rdar://component/XXXXXX> J132 HW EE Schematic | Proto 0
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