1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X1757/MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0023281362	ENGINEERING RELEASED	2020-05-05

LAST_MODIFICATION=Tue May 5 21:26:43 2020

LAST_MODIFICATION=Tue May 5 21:26:43 2020

SYNC_MASTER=eli SYNC_DATE=08/27/2019

DRAWING TITLE
SCHEM,MLB,X1757

Apple Inc.

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A Module Parts

TBT Burnside Bridge

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00561	2	IC,TBT,BBR,SLMN7,PRQ,A1,BGA105	UF000,UF100	CRITICAL	TBT_BB:PRQA1

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02158	2	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500	CRITICAL	ACE2:B2_BGA

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-20641	2	IC,PARROT,CD2E224,B0,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_OTP6
338S00628	2	IC,PARROT,CD2E226B,B0 LSB1,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_LSB1_OTP6

Secure Element

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-19915	1	IC,SN210V,B1,CERES,DEV KY,SWrV7,WLCSP81	U5000	CRITICAL	SE:DEV_SW_V7
998-21255	1	IC,SN210V,B1,CERES,DEV,SWrH3,WLCSP81	U5000	CRITICAL	SE:DEV_SW_H3
338S00630	1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU

B Programmable Parts

TBT ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	TBT_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00232	335S00133	TBT_ROM:BLANK	UF260	rdar://problem/50598337

341S01617	1	ROM,TBT/ACE (V31.5) PROTO-1,X1757	UF260	CRITICAL	TBT_ROM:PP0
341S01676	1	ROM,TBT/ACE (V2.45.0.7) PROTO-1,X1757	UF260	CRITICAL	TBT_ROM:PP1

SOC ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-20613	1	IC,SPI SERIAL FLASH,64MBIT,1.8V,XSON8	U1970	CRITICAL	SOC_ROM:BLANK_ORIG
335S00494	1	IC,SPI SERIAL FLASH,64MBIT,1.8V,4X3,SON8	U1970	CRITICAL	SOC_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00500	335S00494	SOC_ROM:BLANK	U1970	rdar://problem/59964804

SYNC_DATE=06/06/2019

PAGE TITLE

BOM Configuration

Apple Inc.

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A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,ALTERNATE,COMMON,CMN_IC,MLB_PROGPARTS,MLB_USBC,MLB_POWER,MLB_WIRELESS,MLB_MECH,MLB_MISC,MLB_BLC,EVT,SECDIS_EXT_CLK,DMIC_CLK_10OHM
MLB_USBC	TBT_BB:PRQA1,ACE2:B2_BGA,UPC_ATCRTMR_INT,UPC_EUSBLS_INT,EUSB_LS:B0_LSB1_OTP6
MLB_PROGPARTS	WFBT_ROM:BLANK,SOC_ROM:BLANK,TBT_ROM:PP1,SE:PROD_SW_MU
MLB_POWER	PBUS_3S,MPMU_IC:B0,SPMU_IC:A1,P3V8AON_IC:A1_R0B0
MLB_WIRELESS	WLBT:ES6_3_M
MLB_MECH	SHLD_CAN_BSB:EVT,SHLD_CAN_ICE:EVT
MLB_MISC	BOARD_ID,SYSDET:FET,BOOT_CONFIG2,LOADISNS
MLB_DEV	DEVELOPMENT,WLBT_DBG,USBC_DBG
MLB_BLC	BLC_BEN_IC:V7,BLC_LEDS_PER_STRING:16,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM,BLC_KBD_BOOST_USED:YES

B Build Specific Groups

BOM GROUP	BOM OPTIONS	
BOARD_ID	BOARDID1,BOARDID2	Pull-ups: 0x0000110
PROTO0	BOARD_REV3,BOARD_REV2,BOARD_REV1,BOARD_REV0	Pull-downs: 0x0000
PROTO1	BOARD_REV3,BOARD_REV2,BOARD_REV1	Pull-downs: 0x0001
EVT	BOARD_REV3,BOARD_REV2,BOARD_REV0	Pull-downs: 0x0002

C DC/DC BOM Groups

BOM GROUP	BOM OPTIONS
DCDC_COMMON	SCHEM,PCBF,COMMON,DCDC_USBC,MLB_POWER,MLB_MECH,MLB_MISC,MLB_BLC,EVT
DCDC_USBC	UPC_ATCRTMR_INT,UPC_EUSBLS_INT

D Reference Design Pack Options

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_DEBUG_UPC0
USBC01_VR5V_LOCAL_NO
USBC_LAPTOP
NO_DFR
FTCAM
HAS_LID

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS-D12
3V3_S2_PBUS-D2
3V8_AON_PBUS-B12
3V8_AON_I2C-DEV
NO_AMR_INTERPOSER_LEFT
NO_AMR_INTERPOSER_RIGHT
PKGS:SMALL_PITCH
ACE2_SS_CAP

PACK_OPTIONS TO INCLUDE IN NETLIST
PROD_SECDIS
JTAG_SECDIS:NO
PROTO_PULLDOWN_SECDIS
80UM_STEN
INTERNAL_DISPLAY
CHGR_40W

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_DBG_CONN
SPKRAMP_A
PORTABLE
SMALL_NOR
SPKRAMP_LVL_SON

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_TP
CHGR_TP_BOT
3V8_EXT_DIODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
685-00339	1	COMMON PARTS,MLB,X1757	CBOM	CRITICAL	CMN_PARTS_BOM
685-00377	1	PARTS,SSDNAND1,MLB,X1757	P1BOM	CRITICAL	PARTS_SSDNAND1
985-01176	1	DEV PARTS,MLB,X1757	DEV1	CRITICAL	DEV_PARTS_BOM
051-05392	1	SCHEM,MLB,X1757	SCHEM	CRITICAL	SCHEM
820-02016	1	PCBF,MLB,X1757	PCBF	CRITICAL	PCBF

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BOM Configuration

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A Mounting Holes

998-19374
SH0400
TH-NSP
1
SL-3.41X2.0-5.91X4.5

998-19374
SH0401
TH-NSP
1
SL-3.41X2.0-5.91X4.5

998-11113
SH0402
4.6R1.7-NSP
1

998-11114
SH0403
4.6X5.2R1.7X2.3-NSP
1

B Heatsink Mounting Holes

998-6473
SH0410
4P0R3P15-NSP
1

998-22161
SH0411
TH-NSP
1
SL-3.65X3.15-4.45X4.0

998-21888
SH0412
4.45R3.6-NSP
1

998-21888
SH0413
4.45R3.6-NSP
1

C Antenna Cowling Bosses

860-01273
SH0420
5.25X2.8R-1.4ID-1.81H-SM
1

D Burnside Bridge Shield Can

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-19070	1	SHIELD CAN,BURNSIDE BRIDGE,X1419	SHLD1	CRITICAL	SHLD_CAN_BSB
806-26240	1	SHIELD CAN,BURNSIDE BRIDGE,X1739	SHLD1	CRITICAL	SHLD_CAN_BSB:EVT

Plated slots for shield can

SH0430
TH-NSP
1
SL-0.5X1.28-1.25X2.03

SH0431
TH-NSP
1
SL-0.5X1.28-1.25X2.03

E Sled, Thermal Module

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-25230	2	SLED,SOLDER,X1757	SLD1,SLD2	CRITICAL	

F Inductor Shield Fence

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-27192	1	SHIELD FENCE,ICEMAN,INDUCTORS,X1739	SHLD2	CRITICAL	SHLD_CAN_ICE
806-27475	1	SHIELD,FENCE,INDUCTORS,X1739	SHLD2	CRITICAL	SHLD_CAN_ICE:EVT

Plated slots for shield can

998-1681
SH0440
TH
1
SL-0.4X1.20

998-1681
SH0441
TH
1
SL-0.4X1.20

BOM_COST_GROUP=MECHANICALS

SYNC_DATE=06/06/2019

PAGE TITLE
PD Parts

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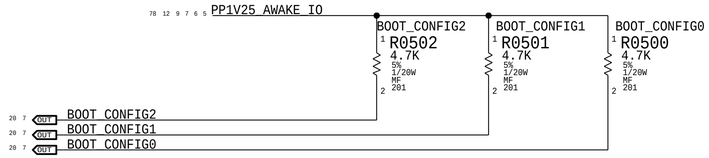
OK2INTEGRATE

BOOT CONFIG ID

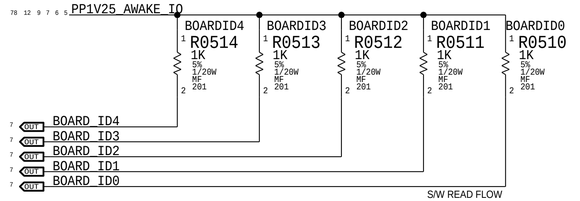


BOOT_CFG[2:0]	MODE
000	SPI1 NOR (12 MHZ)
001	SPI1 NOR (12 MHZ) TESTMODE
010	SPI0 NAND
011	SPI0 NAND TESTMODE
POR ---> 100	SPI1 NOR (40 MHZ)
101	SPI1 NOR (40 MHZ) TESTMODE
110	SPI1 NOR (6 MHZ)
111	SPI1 NOR (6MHZ) TESTMODE

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

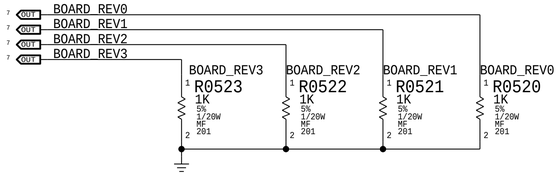


S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

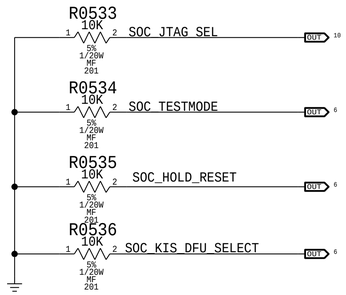
NOTE: STUFFING RESISTOR MEANS 0



board rev should start at 0b0000 and increment each rev.

S/W READ FLOW

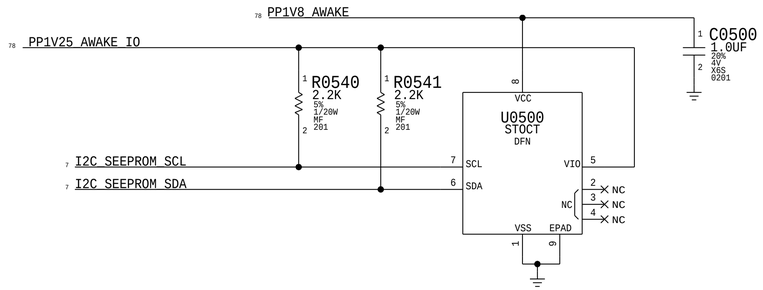
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ



SEP EEPROM (128-Kbit)

(Write: 0xA2, Read 0xA3)

APN:335S00455



OCELOT I2C pulls

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
U0600	TGA_PINDELAY_2020_03_26.csv

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: Support

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

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OK2INTEGRATE

SOC: CIO, USB, DRAM, RESETS, CLOCKS, SWD, FPWM

OMIT_TABLE

U0600
TMLR68A0-B09
BGA
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82 72 34 10	IN	PMU_RESET_L	R2	LP4_IN_RESET_N	
82 54 34 6	IN	SOC_FORCE_DFU	AA49	FORCE_DFU	
6		SOC_REQUEST_DFU1	AK55	REQUEST_DFU1	
6		SOC_REQUEST_DFU2	AJ54	REQUEST_DFU2	
5	IN	SOC_TESTMODE	AD2	TESTMODE	IPD
82 53 34	IN	PMU_ACTIVE_READY	AL54	CFSB	
5	IN	SOC_HOLD_RESET	AC1	HOLD_RESET	IPD
5		SOC_KIS_DFU_SELECT	AB49	KIS_DFU_SELECT	
20	BI	EUSB_ATC0_P	BB54	ATC0_USB_EDP	
20	BI	EUSB_ATC0_N	BB55	ATC0_USB_EDM	
58	IN	CIO_ATC0_LSRX_1V2	BE18	USB_C0_LSRX	
58	OUT	CIO_ATC0_LSTX_1V2	BE13	USB_C0_LSTX	
6		SOC_ATC0_USB_RESREF	BB53	ATC0_USB_RESREF	
20		TPT_TMU_CLK_OUT0	V48	USB_C0_HPD/TMU_CLK_OUT0	
20	BI	EUSB_ATC1_P	BC54	ATC1_USB_EDP	
20	BI	EUSB_ATC1_N	BC55	ATC1_USB_EDM	
58	IN	CIO_ATC1_LSRX_1V2	BD3	USB_C1_LSRX	
58	OUT	CIO_ATC1_LSTX_1V2	BE10	USB_C1_LSTX	
6		SOC_ATC1_USB_RESREF	BC53	ATC1_USB_RESREF	
20		TPT_TMU_CLK_OUT1	R48	USB_C1_HPD/TMU_CLK_OUT1	
6		USB_VBUS_DETECT	AG1	EUSB_VBUS_DETECT	
51	BI	USBC_ATC0_D2R_P<1>	BE50	ATCPHY0_RX0_P	GND_VOID=TRUE
51	BI	USBC_ATC0_D2R_N<1>	BF50	ATCPHY0_RX0_N	GND_VOID=TRUE
51	OUT	USBC_ATC0_R2D_C_P<1>	BC49	ATCPHY0_TX0_P	GND_VOID=TRUE
51	OUT	USBC_ATC0_R2D_C_N<1>	BD49	ATCPHY0_TX0_N	GND_VOID=TRUE
51	BI	USBC_ATC0_D2R_P<2>	BE48	ATCPHY0_RX1_P	GND_VOID=TRUE
51	BI	USBC_ATC0_D2R_N<2>	BF48	ATCPHY0_RX1_N	GND_VOID=TRUE
51	OUT	USBC_ATC0_R2D_C_P<2>	BC47	ATCPHY0_TX1_P	GND_VOID=TRUE
51	OUT	USBC_ATC0_R2D_C_N<2>	BD47	ATCPHY0_TX1_N	GND_VOID=TRUE
51	BI	USBC_ATC0_AUX_P	AY51	ATCPHY0_AUX_P	
51	BI	USBC_ATC0_AUX_N	AY52	ATCPHY0_AUX_N	
6		SOC_ATCPHY0_RCAL_POS	BE52	ATCPHY0_RCAL_P	
6		SOC_ATCPHY0_RCAL_NEG	BF52	ATCPHY0_RCAL_N	
52	BI	USBC_ATC1_D2R_P<1>	BF44	ATCPHY1_RX0_P	GND_VOID=TRUE
52	BI	USBC_ATC1_D2R_N<1>	BE44	ATCPHY1_RX0_N	GND_VOID=TRUE
52	OUT	USBC_ATC1_R2D_C_P<1>	BD43	ATCPHY1_TX0_P	GND_VOID=TRUE
52	OUT	USBC_ATC1_R2D_C_N<1>	BC43	ATCPHY1_TX0_N	GND_VOID=TRUE
52	BI	USBC_ATC1_D2R_P<2>	BF46	ATCPHY1_RX1_P	GND_VOID=TRUE
52	BI	USBC_ATC1_D2R_N<2>	BE46	ATCPHY1_RX1_N	GND_VOID=TRUE
52	OUT	USBC_ATC1_R2D_C_P<2>	BD45	ATCPHY1_TX1_P	GND_VOID=TRUE
52	OUT	USBC_ATC1_R2D_C_N<2>	BC45	ATCPHY1_TX1_N	GND_VOID=TRUE
52	BI	USBC_ATC1_AUX_P	BA52	ATCPHY1_AUX_P	
52	BI	USBC_ATC1_AUX_N	BA51	ATCPHY1_AUX_N	
6		SOC_ATCPHY1_RCAL_POS	BF42	ATCPHY1_RCAL_P	
6		SOC_ATCPHY1_RCAL_NEG	BE42	ATCPHY1_RCAL_N	

ATC

RESET

DFU_STATUS	V51	SOC_DFU_STATUS	OUT	20 54 82

AMUX_OUT can go to TP or to AMUX_IN on PMU

CLOCKS

XI0	BE36	SOC_XTAL24M_IN		
XO0	BF36	SOC_XTAL24M_OUT		
TST_CLKOUT	P54	TPT_TST_CLKOUT		20
ANALOGMUX_OUT	AL48	SOC_AMUX_OUT	OUT	20

SWD

SWD_TCK_OUT1	AJ1	SWD_NAND0_SWCLK	OUT	20
SWD_TMS2	U54	SWD_NAND0_SWDIO	BI	20
SWD_TMS3	V54	NC_SWD_TMS3		81
SWD_TMS4	AH3	NC_SWD_TMS4		81

FPW

IPD

FPWM0/MASTER_SYNC_GEN_0	V50	WLAN_TIME_SYNC	IN	60
FPWM1	Y49	KBD_BKLT_PWM	OUT	70
FPWM2	U50	NC_FPWM2		81

R0651 499 1% 1/20W MF 201
CRITICAL Y0600 1.00X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
SOC_24M_O_R
CRITICAL C0650 15PF 5% 50V C0G 0201
CRITICAL C0651 15PF 5% 50V C0G 0201

6 SOC_ATCPHY0_RCAL_POS — R0600 200 1% 1/20W MF 201 — C0600 10PF 5% 25V C0G 0201 — 6 SOC_ATCPHY0_RCAL_NEG

6 SOC_ATCPHY1_RCAL_POS — R0601 200 1% 1/20W MF 201 — C0601 10PF 5% 25V C0G 0201 — 6 SOC_ATCPHY1_RCAL_NEG

78 12 9 7 6 5 PP1V25_AWAKE_IO — R0630 10K 5% 1/20W MF 201 — 6 SOC_REQUEST_DFU1

78 12 9 7 6 5 PP1V25_AWAKE_IO — R0631 10K 5% 1/20W MF 201 — 6 SOC_REQUEST_DFU2

82 54 34 6 SOC_FORCE_DFU — R0632 47K 5% 1/20W MF 201

6 SOC_ATC0_USB_RESREF — R0641 200 1% 1/20W MF 201

6 SOC_ATC1_USB_RESREF — R0640 200 1% 1/20W MF 201

78 12 9 7 6 5 PP1V25_AWAKE_IO — R0639 0 5% 1/20W MF 0201 — 6 USB_VBUS_DETECT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON,24MHZ.XTAL
197S0588	197S0591		Y0600	TXC,24MHZ,XTAL

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE
SOC: CIO, USB, RESETS, CLOCKS, SWD

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OK2INTEGRATE

all signals are 1.2 unless otherwise specified.
all signals on this page reference PP1V2_AWAKE_GRP if they are 1.2V
if they are 1.8V they reference PP1V8_AWAKE_GRP

SOC: I/Os

U0600 TMLR68A0-B09 BGA SYM 3 OF 23

TDM_SPKRAMP_L_BCLK_R	AK4	I2S0_BCLK		SPI0_MISO	AL4	BOOT_CONFIG2	IN
TDM_SPKRAMP_L_D2R	AJ3	I2S0_DIN	IPD	SPI0_MOSI	AK2	BOOT_CONFIG1	OUT
TDM_SPKRAMP_L_R2D_R	AJ5	I2S0_DOUT		SPI0_SCLK	AK1	BOOT_CONFIG0	OUT
TDM_SPKRAMP_L_FSYNC_R	AJ4	I2S0_LRCK					
NC_SOC_I2S0_MCK	AK3	I2S0_MCK		SPI1_MISO	AD4	SPI_SOCROM_MISO	IN
TDM_SPKRAMP_R_BCLK_R	AG3	I2S1_BCLK	IPD	SPI1_MOSI	AE4	SPI_SOCROM_MOSI_R	OUT
TDM_SPKRAMP_R_D2R	AF3	I2S1_DIN		SPI1_SCLK	AF4	SPI_SOCROM_CLK_R	OUT
TDM_SPKRAMP_R_R2D_R	AG4	I2S1_DOUT		SPI1_SSIN	AE3	SPI_SOCROM_CS_L	OUT
TDM_SPKRAMP_R_FSYNC_R	AF2	I2S1_LRCK	I2S				
NC_SOC_I2S1_MCK	AG2	I2S1_MCK		SPI2_MISO	AF53	SPI_1V8_TOUCHID_MISO	IN
TDM_CODEC_BCLK_R	AK5	I2S2_BCLK		SPI2_MOSI	AF54	SPI_1V8_TOUCHID_MOSI_R	OUT
TDM_CODEC_D2R	AL6	I2S2_DIN	IPD	SPI2_SCLK	AF55	SPI_1V8_TOUCHID_CLK_R	OUT
TDM_CODEC_R2D_R	AJ7	I2S2_DOUT		SPI2_SSIN	AF52	NC_SOC_SPI2_SSIN	
TDM_CODEC_FSYNC_R	AM4	I2S2_LRCK					
NC_SOC_I2S2_MCK	AK6	I2S2_MCK		SPI3_MISO	Y1	SPI_IPD_MISO	IN
NC_I2S3_BCLK	AH6	I2S3_BCLK		SPI3_MOSI	W1	SPI_IPD_MOSI_R	OUT
NC_I2S3_D2R	AH4	I2S3_DIN		SPI3_SCLK	AB1	SPI_IPD_CLK_R	OUT
NC_I2S3_R2D	AG5	I2S3_DOUT		SPI3_SSIN	AA1	SPI_IPD_CS_L	OUT
NC_I2S3_LRCLK	AJ6	I2S3_LRCK					
NC_I2S3_MCLK	AF5	I2S3_MCK		SPI4_MISO	AC4	SPI_TCON_MISO	IN
				SPI4_MOSI	AB4	SPI_TCON_MOSI_R	OUT
I2C_UPC_SCL	W52	I2C0_SCL		SPI4_SCLK	AA4	SPI_TCON_CLK_R	OUT
I2C_UPC_SDA	V52	I2C0_SDA		SPI4_SSIN	AB3	SPI_TCON_CS_L	OUT
I2C_SPKRAMP_L_SCL	AA48	I2C1_SCL					
I2C_SPKRAMP_L_SDA	Y48	I2C1_SDA	SEP	SGPIO0	AC3	DBL_CLICK_DET	IN
				SGPIO1	AC2	DISABLE_STROBE	OUT
NC_I2C_CODEC_SCL	AB50	I2C2_SCL		SI2C0_SCL	Y5	I2C_SEEPROM_SCL	OUT
NC_I2C_CODEC_SDA	Y50	I2C2_SDA		SI2C0_SDA	Y4	I2C_SEEPROM_SDA	BI
I2C_SPKRAMP_R_CODEC_SCL	AF6	I2C3_SCL					
I2C_SPKRAMP_R_CODEC_SDA	AE6	I2C3_SDA	I2C	SSPI0_MISO	AC5	FTCAM_DISABLE_L	OUT
				SSPI0_MOSI	AD5	NC_SSPI0_MOSI	
NC_I2C_DFR_SCL	AF50	I2C4_SCL		SSPI0_SCLK	AD6	DMIC_DISABLE_L	OUT
NC_I2C_DFR_SDA	AG49	I2C4_SDA					
			THROTTLE	SOCHOT1	AK52	SOC_SOCHOT_L	OUT
NC_SPMI2_CLK	AK7	AP_SPMI2_SCLK	SPMI	THROTTLE_TRIGGER0/MTR_ADC_DOUT	AK53	BUCK1_THERMAL_THROTTLE_L	IN
NC_SPMI2_DATA	AL7	AP_SPMI2_SDATA		THROTTLE_TRIGGER1/MTR_ADC_CLKOUT	AL53	BUCK0_THERMAL_THROTTLE_L	IN
				THROTTLE_TRIGGER2/PLL_DIGOBS_0	AJ55	NC_SOC_TRIGGER2	IN
				THROTTLE_TRIGGER3/PLL_DIGOBS_1	AJ53	PMU_VDDHI_UVWARN_L	IN
				THROTTLE_TRIGGER4	AJ49	PMU_VDDMAIN_UVWARN_L	IN

1.8V IO

1.8V IO

IPU FOR ALL THROTTLE_TRIGGER

PORTABLES SHOULD NC TRIGGER2

PORTABLES SHOULD NC TRIGGER2

R0790 47K 5% 1/20W MF 201

PP1V25_AWAKE_IO

SOC_SOCHOT_L

U0600 TMLR68A0-B09 BGA SYM 2 OF 23

UPC_I2C_INT_L	AJ51	GPIO[0]	IPU	UART0_RXD	AB53	UART_DEBUGPRT_D2R	IN
NC_SOC_GPIO01	AA50	GPIO[1]		UART0_TXD	AC53	UART_DEBUGPRT_R2D	OUT
SPKR_ID0	V53	GPIO[2]	IPU				
SPKR_ID1	U53	GPIO[3]	IPU	UART1_CTSN	AC54	NC_DFR_1V8_TOUCH_RESET_L	OUT
SPKRAMP_RESET_L	T53	GPIO[4]		UART1_RTSN	AA53	NC_DFR_1V8_DISP_RESET_L	OUT
SPKRAMP_INT_L	W53	GPIO[5]	IPU	UART1_RXD	AA54	NC_DFR_1V8_DISP_INT	IN
CODEC_INT_L	W50	GPIO[6]	IPU	UART1_TXD	AC55	BT_TIME_SYNC_1V8	IN
SWD_UPC_SWCLK	U52	GPIO[7]					
GPU_CFG_L	AC48	GPIO[8]	IPU	UART2_CTSN	W55	UART_WLAN_D2R_CTS_L	IN
NC_SOC_GPIO09	R53	GPIO[9]		UART2_RTSN	Y54	UART_WLAN_R2D_RTS_L	OUT
NC_SOC_GPIO10	R52	GPIO[10]	IPU	UART2_RXD	Y53	UART_WLAN_D2R	IN
BOARD_REV0	N55	GPIO[11]		UART2_TXD	Y55	UART_WLAN_R2D	OUT
BOARD_REV1	AH54	GPIO[12]					
BOARD_REV2	Y52	GPIO[13]		UART3_CTSN	AC51	NC_UART3_D2R_CTS_L	
BOARD_REV3	AA51	GPIO[14]		UART3_RTSN	AC52	NC_UART3_R2D_RTS_L	
NC_SOC_GPIO15	R54	GPIO[15]	GPIO	UART3_RXD	AF48	NC_UART3_D2R	
NC_SOC_GPIO16	AC50	GPIO[16]		UART3_TXD	AB52	NC_UART3_R2D	
SWD_UPC_SWDIO0	U51	GPIO[17]					
NC_SWD_UPC_SWDIO1	AK50	GPIO[18]		UART4_CTSN	AJ48	NC_UART4_D2R_CTS_L	
NC_DFR_TOUCH_INT_L	T52	GPIO[19]		UART4_RTSN	AK48	NC_UART4_R2D_RTS_L	
IPD_SPI_EN	V49	GPIO[20]		UART4_RXD	AL52	NC_UART4_D2R	
TOUCHID_INT	AJ52	GPIO[21]	IPU	UART4_TXD	AL50	NC_UART4_R2D	
TOUCHID_PWR_EN	AJ50	GPIO[22]					
UPC_FORCE_PWR	AC49	GPIO[23]		UART6_RXD	AF51	UART_TCON_D2R	IN
NC_DFR_PWR_EN	R51	GPIO[24]		UART6_TXD	AG50	NC_UART_TCON_R2D	OUT
NC_SPI_DFR_CS_L	AL49	GPIO[25]					
NC_ENET_SYNC_1588	AF49	GPIO[26]		UART7_RXD	AM2	NC_UART7_RXD	
				UART7_TXD	AJ2	NC_UART7_TXD	
BOARD_ID0	W49	BOARD_ID0/SOC_DEBUG1	BOARD ID	NAND_SYS_CLK0	AG52	NAND0_CLK24M_0_R	OUT
BOARD_ID1	R55	BOARD_ID1/SOC_DEBUG2		NAND_SYS_CLK1	AH53	NAND0_CLK24M_1_R	OUT
BOARD_ID2	T55	BOARD_ID2/SOC_DEBUG3					
BOARD_ID3	V55	BOARD_ID3/SPI0_SSIN		SSD_BFH	AH51	NAND_BFH	OUT
BOARD_ID4	U55	BOARD_ID4		SSD_RESETN	AG53	NAND0_RESET_L	OUT

UPC_FORCE_PWR will likely be removed in the future

TOUCHID_PWR_EN gets pulled up to S2 on TOUCHID page
This is OK because the GPIO is failsafe

PD needed on DFR PAGE

1.8V IO

Use UART2 if your wireless module is 1.2V IO

1.8V IO

R2D is for desktop only

NOSTUFF R0791 47K 5% 1/20W MF 201

NAND0_RESET_L

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

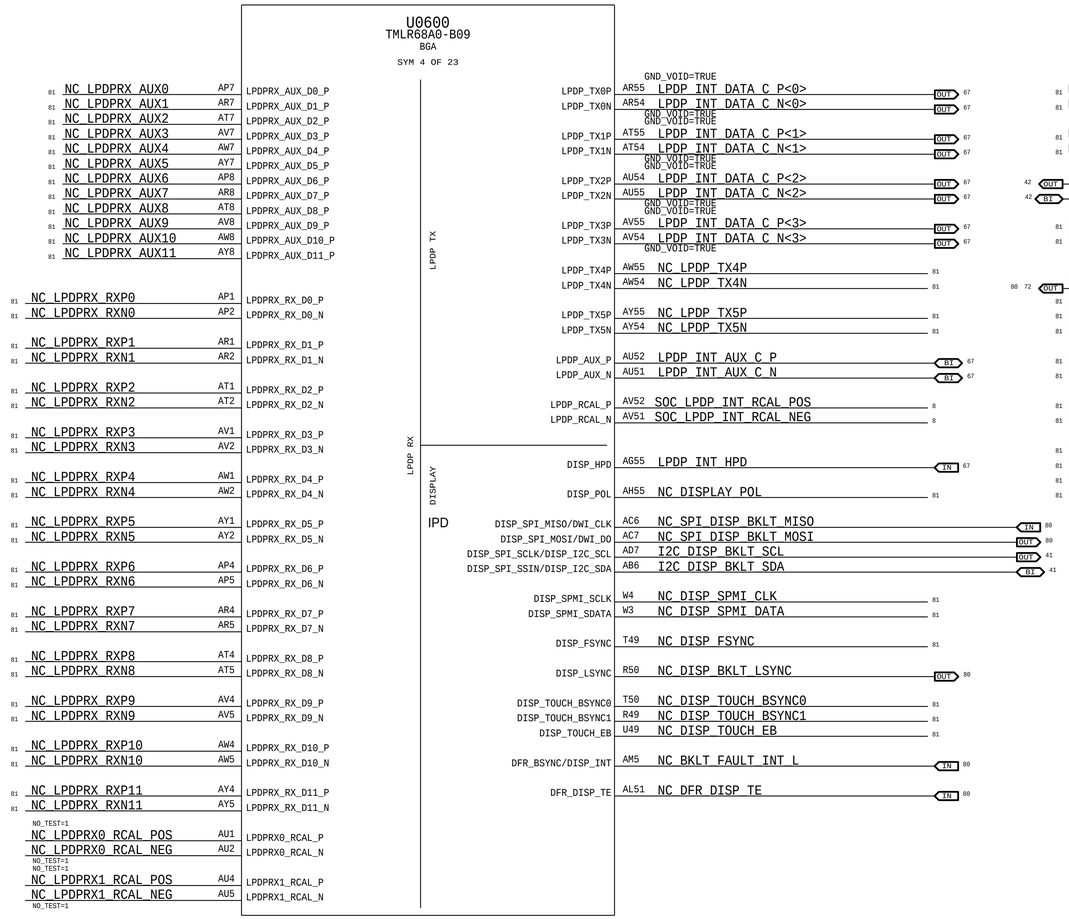
PAGE TITLE: SOC: AP I/Os

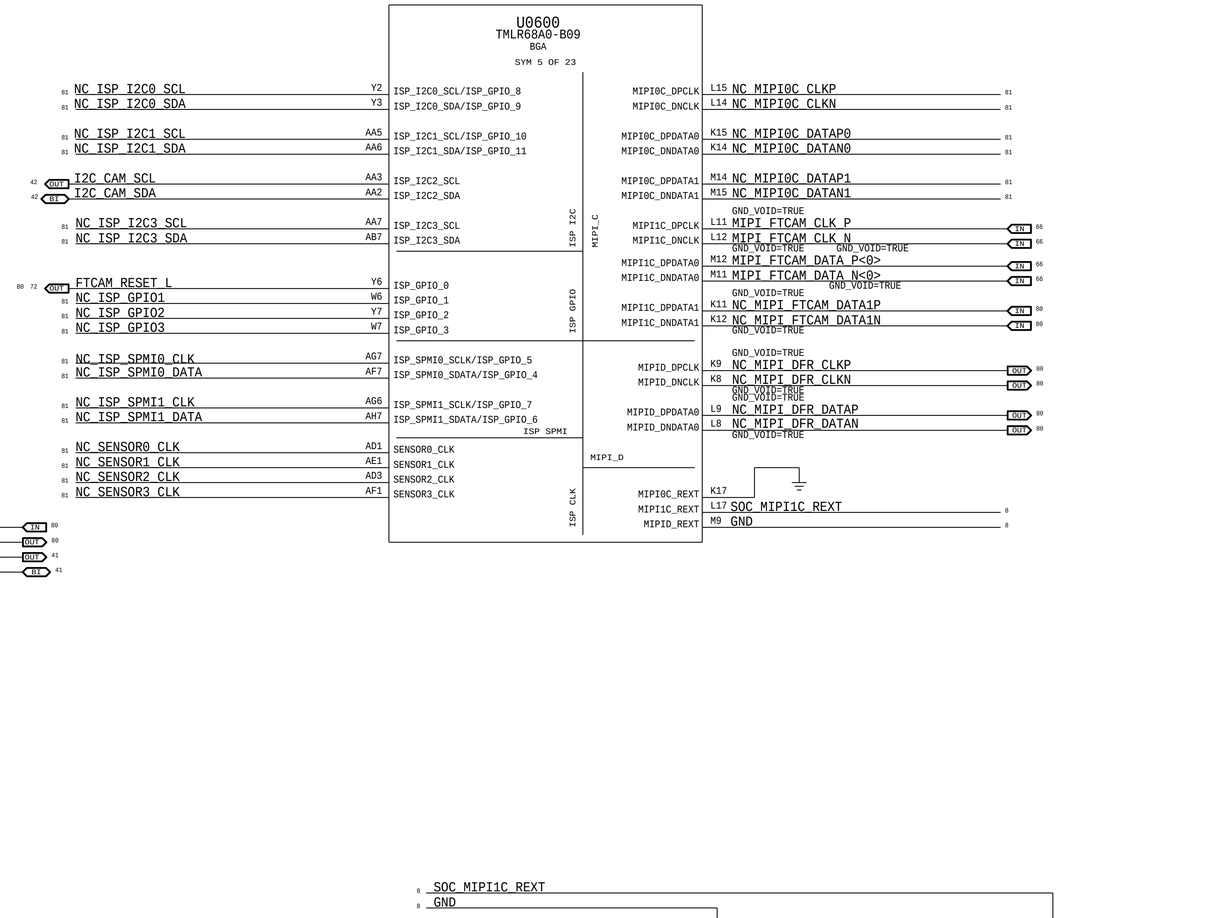
Apple Inc.

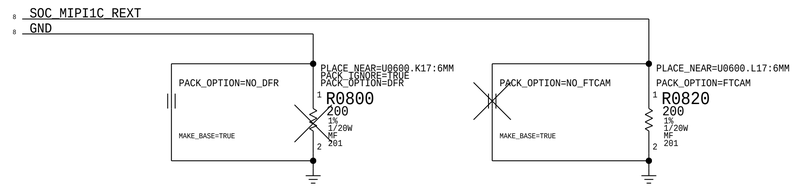
DRAWING NUMBER: 051-05392 SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
PAGE: 7 OF 801
SHEET: 7 OF 92

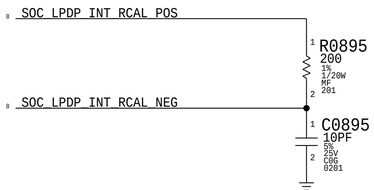
OK2INTEGRATE

SOC: LPDP & MIPI









BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: LPDP & MIPI

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
REVISION 4.0.0
BRANCH evt-1
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OK2INTEGRATE

SOC: PCIE

PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
75 NF AND 265 NF FOR GEN1/2 AND BETWEEN
176 NF AND 265 NF FOR GEN 3/4

R0970 IS NEEDED DUE TO RDAR://53793006

78 12 7 6 5 PP1V25_AWAKE_IO

- R0930 47K 5% 1/20W MF 201
- R0940 47K 5% 1/20W MF 201
- R0950 47K 5% 1/20W MF 201
- R0960 47K 5% 1/20W MF 201 ?PACK_IGNORE=TRUE PACK_OPTION=ENET
- R0970 47K 5% 1/20W MF 201

65 9 NAND0_CLKREQ1_L
61 60 9 WLBT_CLKREQ_L
65 9 NAND0_CLKREQ0_L
80 9 NC_ENET_CLKREQ_L
9 USBHC_CLKREQ_L

TO BE CHECKED WITH SEG- DO NOT MATCH WITH SILVAL
IS THE PULL-UP VOLTAGE CORRECT?

9 SOC_ST_PCIE_RCAL_POS
- R0990 200 1% 1/20W MF 201
9 SOC_ST_PCIE_RCAL_NEG
- C0990 10PF 5% 25V C0G 0201

9 SOC_GP_PCIE_RCAL_POS
- R0991 200 1% 1/20W MF 201
9 SOC_GP_PCIE_RCAL_NEG
- C0991 10PF 5% 25V C0G 0201

80 9 NC_USBHC_RESET_L
80 9 NC_ENET_RESET_L
63 62 9 NAND0_PCIE_RESET_L
61 60 9 WLBT_RESET_L

- R0941 47K 5% 1/20W MF 201
- R0951 47K 5% 1/20W MF 201
- R0961 47K 5% 1/20W MF 201 ?PACK_IGNORE=TRUE PACK_OPTION=ENET
- R0971 47K 5% 1/20W MF 201 ?PACK_IGNORE=TRUE PACK_OPTION=USBHC

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NAND

62 IN	PCIE_NAND0_D2R_P<0>	BE26	ST_PCIE_RX0_P	PCIE ST0	PCIE GP0	GP_PCIE_RX0_P	BE30	PCIE_WLBT_D2R_P	IN 60
62 IN	PCIE_NAND0_D2R_N<0>	BF26	ST_PCIE_RX0_N			GP_PCIE_RX0_N	BF30	PCIE_WLBT_D2R_N	IN 60
62 OUT	PCIE_NAND0_R2D_C_P<0>	BC27	ST_PCIE_TX0_P			GP_PCIE_TX0_P	BC31	PCIE_WLBT_R2D_C_P	OUT 60
62 OUT	PCIE_NAND0_R2D_C_N<0>	BD27	ST_PCIE_TX0_N			GP_PCIE_TX0_N	BD31	PCIE_WLBT_R2D_C_N	OUT 60
62 OUT	PCIE_CLK100M_NAND0_0_P	BB37	ST_PCIE_REF_CLK0_P			GP_PCIE_REF_CLK0_P	BE40	PCIE_CLK100M_WLBT_P	OUT 60
62 OUT	PCIE_CLK100M_NAND0_0_N	BC37	ST_PCIE_REF_CLK0_N			GP_PCIE_REF_CLK0_N	BF40	PCIE_CLK100M_WLBT_N	OUT 60
65 9 B3	NAND0_CLKREQ0_L	AH50	ST_PCIE_CLKREQ0_N			GP_PCIE_CLKREQ0_N	AB55	WLBT_CLKREQ_L	B3 9 60 61
63 62 9 OUT	NAND0_PCIE_RESET_L	AH52	ST_PCIE_PERST0_N			GP_PCIE_PERST0_N	AA52	WLBT_RESET_L	OUT 9 60 61
63 IN	PCIE_NAND0_D2R_P<1>	BE28	ST_PCIE_RX1_P	PCIE ST1	PCIE GP1	GP_PCIE_RX1_P	BE32	NC_PCIE_USBHC_D2RP	IN 80
63 IN	PCIE_NAND0_D2R_N<1>	BF28	ST_PCIE_RX1_N			GP_PCIE_RX1_N	BF32	NC_PCIE_USBHC_D2RN	IN 80
63 OUT	PCIE_NAND0_R2D_C_P<1>	BC29	ST_PCIE_TX1_P			GP_PCIE_TX1_P	BC33	NC_PCIE_USBHC_R2DCP	OUT 80
63 OUT	PCIE_NAND0_R2D_C_N<1>	BD29	ST_PCIE_TX1_N			GP_PCIE_TX1_N	BD33	NC_PCIE_USBHC_R2DCN	OUT 80
63 OUT	PCIE_CLK100M_NAND0_1_P	BB38	ST_PCIE_REF_CLK1_P			GP_PCIE_REF_CLK1_P	BE38	NC_PCIE_CLK100M_USBHCP	OUT 80
63 OUT	PCIE_CLK100M_NAND0_1_N	BC38	ST_PCIE_REF_CLK1_N			GP_PCIE_REF_CLK1_N	BF38	NC_PCIE_CLK100M_USBHCN	OUT 80
65 9 B3	NAND0_CLKREQ1_L	AH49	ST_PCIE_CLKREQ1_N			GP_PCIE_CLKREQ1_N	AA55	USBHC_CLKREQ_L	B3 9
81	NC_NAND0_PCIE_RESET1_L	AH48	ST_PCIE_PERST1_N			GP_PCIE_PERST1_N	P55	NC_USBHC_RESET_L	OUT 9 80
					PCIE GP2	GP_PCIE_RX2_P	BE34	NC_PCIE_ENET_D2RP	IN 80
						GP_PCIE_RX2_N	BF34	NC_PCIE_ENET_D2RN	IN 80
						GP_PCIE_TX2_P	BC35	NC_PCIE_ENET_R2DCP	OUT 80
						GP_PCIE_TX2_N	BD35	NC_PCIE_ENET_R2DCN	OUT 80
						GP_PCIE_REF_CLK2_P	BE39	NC_PCIE_CLK100M_ENETP	OUT 80
						GP_PCIE_REF_CLK2_N	BF39	NC_PCIE_CLK100M_ENETN	OUT 80
						GP_PCIE_CLKREQ2_N	AH1	NC_ENET_CLKREQ_L	B3 9 80
						GP_PCIE_PERST2_N	AE7	NC_ENET_RESET_L	OUT 9 80
9	SOC_ST_PCIE_RCAL_POS	BC24	ST_PCIE_RCAL_P			GP_PCIE_RCAL_P	BC25	SOC_GP_PCIE_RCAL_POS	9
9	SOC_ST_PCIE_RCAL_NEG	BB24	ST_PCIE_RCAL_N			GP_PCIE_RCAL_N	BB25	SOC_GP_PCIE_RCAL_NEG	9
81	NC_PAD_MTR_ANALOG_TEST_POS	AM3	PAD_MTR_ANALOG_TEST_P	MTR					
81	NC_PAD_MTR_ANALOG_TEST_NEG	AL3	PAD_MTR_ANALOG_TEST_N						
81	NC_PAD_MTR_VREF_POS	AL1	PAD_MTR_VREF_P						
81	NC_PAD_MTR_VREF_NEG	AM1	PAD_MTR_VREF_N						

GND_VOID=TRUE

WLAN/BT

USB3 CTLR

ENET/SD

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: PCIE

Apple Inc.

DRAWING NUMBER 051-05392 | SIZE D
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OK2INTEGRATE

AOP, NUB, and SMC GPIO's are referenced to PP1V25_S2_AOP

SOC: AOP

U0600
TMLR68A0-B09
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output if gyro, input for radar

I2C0 is ALS for portables

DOC_ATTENTION should be a TP for non dev programs,

SOC_SW_DBG SHOULD GO TO A LED IF POSSIBLE. NEEDS A TEST POINT AT MINIMUM

FIXTURE_MODE_L should be aliased to a TP for non dev programs, The TP is required

	NC_AOP_FUNC0	BB18	AOP_FUNC[0]	AOP GPIO	NUB_CLK_OUT0	BA17	NC_DFR_TOUCH_CLK32K_RESET_L	
	NC_AOP_FUNC1	BC16	AOP_FUNC[1]		NUB_DOCK_ATTENTION/CTM_TRIGGER	BC15	TPT_SOC_DOCK_ATTENTION	
	NC_AOP_FUNC2	BC12	AOP_FUNC[2]		NUB_DOCK_CONNECT	BC17	SOC_DOCK_CONNECT	
	NC_AOP_FUNC3	BC13	AOP_FUNC[3]					
	NC_SPI_R1_CS_L	BA16	AOP_FUNC[4]		NUB_GPIO_0/AOP_FUNC15/NUB_CLK_OUT1	BD14	NC_BKLT_PWR_ON	
	NC_AOP_FUNC5	BA13	AOP_FUNC[5]		NUB_GPIO_1/AOP_PDM_IN_CLK0	BD15	CODEC_RESET_L	
OUT	SPI_GYRO_CS_L	BA15	AOP_FUNC[6]		NUB_GPIO_2/AOP_PDM_IN_DATA0	BD21	SOC_SW_DBG	
IN	GYRO_INT	BD13	AOP_FUNC[7]		NUB_GPIO_3/AOP_LEAP_MADI_IN	BD17	IPD_SPI_INT_L	
IN	GYRO_MOTION_INT	BD16	AOP_FUNC[8]	IPU	NUB_GPIO_4/AOP_LEAP_MADI_OUT	BB13	SMC_FIXTURE_MODE_L	
IN	LID_OPEN (MAKE_BASE=TRUE)	BA14	AOP_FUNC[9]	IPD	NUB_GPIO_5/AOP_PDM_OUT_CLK0	BD19	CHGR_INT_L	
PACK_OPTION=HAS_LID	NC_AOP_FUNC10	BB12	AOP_FUNC[10]		NUB_GPIO_6/AOP_PDM_OUT_DATA0/AOP_FUNC16	BD22	NC_CCG_SMC_I2C_INT_L	
OUT	WLAN_CONTEXT_A	BD20	AOP_FUNC[11]		NUB_GPIO_7/AOP_FUNC17	BB10	NC_ACDC_ID	
OUT	WLAN_CONTEXT_B	BA11	AOP_FUNC[12]		NUB_GPIO_8/AOP_FUNC18	BD12	NC_ACDC_BURST_EN_L	
IN	NC_ALS_INT_L	BD18	AOP_FUNC[13]	NUB GPIO	NUB_GPIO_9/AOP_FUNC19	BD11	NC_SPI_DP2HDMI_HOLD_L	
	NC_AOP_FUNC14	BA10	AOP_FUNC[14]		NUB_GPIO_10/AOP_FUNC20	BC10	NC_HDMI_CEC_AOP_TX	
					NUB_GPIO_11/KIS_GPIO0/AOP_FUNC21	BB7	NC_HDMI_CEC_AOP_RX	
					NUB_GPIO_12/KIS_GPIO1/AOP_FUNC22	BD10	NC_HDMI_HPD_AOP	
OUT	I2C_AOP_ALS_SCL	BC20	AOP_I2CM0_SCL	AOP I2C				
BI	I2C_AOP_ALS_SDA	BB19	AOP_I2CM0_SDA		NUB_SPMI0_SCLK	BB15	SPMI_NUB_MPMU_CLK_R	
OUT	NC_I2C_AOP_ENET_SCL	BB16	AOP_I2CM1_SCL		NUB_SPMI0_SDATA	BC14	SPMI_NUB_MPMU_DATA_R	
BI	NC_I2C_AOP_ENET_SDA	BE15	AOP_I2CM1_SDA	NUB SPMI	NUB_SPMI1_SCLK	BA12	SPMI_NUB_SPMU_CLK_R	
	NC_PDM_CLK1	BB9	AOP_PDM_IN_CLK1/AOP_I2S1_BCLK		NUB_SPMI1_SDATA	BC11	SPMI_NUB_SPMU_DATA_R	
	NC_PDM_CLK2	BC9	AOP_PDM_IN_CLK2/AOP_I2S0_MCK					
OUT	PDM_DMIC_CLK3	BC6	AOP_PDM_IN_CLK3/AOP_I2S0_LRCK		NUB_SWD_TCK_OUT0	BC18	SWD_NUB_SWCLK	
OUT	PDM_DMIC_CLK4	BD9	AOP_PDM_IN_CLK4/AOP_I2S0_DOUT		NUB_SWD_TMS0	BC19	SWD_NUB_PMU_SWDIO	
	NC_PDM_CLK5	BC8	AOP_PDM_IN_CLK5/AOP_I2S0_DIN	NUB SWD	NUB_SWD_TMS1	BC21	NC_NUB_SWD_TMS1	
	NC_PDM_CLK6	BD8	AOP_PDM_IN_CLK6/AOP_I2S0_BCLK	AOP PDM				
	NC_PDM_DATA1	BE21	AOP_PDM_IN_DATA1/AOP_I2S1_MCK		JTAG_SEL	BE4	SOC_JTAG_SEL	
	NC_PDM_DATA2	BE16	AOP_PDM_IN_DATA2/AOP_I2S1_LRCK		IPU JTAG_TCK	BF5	SWD_SOC_SWCLK	
IPD IN	PDM_DMIC_DATA3 (CKPLUS_WAIVE=CLK_DATA_CON)	BE19	AOP_PDM_IN_DATA3/AOP_I2S1_DOUT/AOP_PDM_IN_CLK7		IPU JTAG_TDI	BF16	TPT_JTAG_SOC_TDI	
IPD IN	PDM_DMIC_DATA4 (CKPLUS_WAIVE=CLK_DATA_CON)	BD5	AOP_PDM_IN_DATA4/AOP_I2S1_DIN/AOP_PDM_IN_CLK8	JTAG	JTAG_TDO	BC1	TPT_JTAG_SOC_TDO	
IN	SPI_AOP_GYRO_MISO	BF15	AOP_SPI0_MISO		IPU JTAG_TMS	BB1	SWD_SOC_SWDIO	
OUT	SPI_AOP_GYRO_MOSI_R	BF14	AOP_SPI0_MOSI	AOP SPI	IPD JTAG_TRSTN	BF7	TPT_JTAG_SOC_TRST_L	
OUT	SPI_AOP_GYRO_CLK_R	BF17	AOP_SPI0_SCLK					
	NC_AOP_SPMI0_SCLK	BF18	AOP_SPMI0_SCLK/AOP_UART0_TXD		SMC_I2CM0_SCL	BC3	I2C_SMC_PWR_SCL	
	NC_AOP_SPMI0_SDATA	BF19	AOP_SPMI0_SDATA/AOP_UART0_RXD		SMC_I2CM0_SDA	BC2	I2C_SMC_PWR_SDA	
OUT	SPMI_SE_CLK_R	BF20	AOP_SPMI1_SCLK/AOP_UART1_TXD	AOP SPMI	SMC_I2CM1_SCL/SMC_UART1_TXD	BD4	I2C_SMC_UPC_SCL	
BI	SPMI_SE_DATA_R	BF21	AOP_SPMI1_SDATA/AOP_UART1_RXD		SMC_I2CM1_SDA/SMC_UART1_RXD	BB2	I2C_SMC_UPC_SDA	
	NC_AOP_UART2_D2R	BB3	AOP_UART2_RXD		SMC_I2CM2_SCL	BD6	NC_I2C_SMC_SNS1_SCL	
	NC_AOP_UART2_R2D	BB4	AOP_UART2_TXD	AOP UART	SMC_I2CM2_SDA	BC5	NC_I2C_SMC_SNS1_SDA	
					SMC_I2CM3_SCL	BC7	I2C_SMC_IPD_SCL	
					SMC_I2CM3_SDA	BD7	I2C_SMC_IPD_SDA	
IN	PMU_CLK32K_SOC	BE6	RT_CLK32768		SMC_I2CM4_SCL	BE7	NC_I2C_SMC_SNS0_SCL	
				AOP RESET	SMC_I2CM4_SDA	BF9	NC_I2C_SMC_SNS0_SDA	
		BF10	CFSB_AON					
IN	PMU_RESET_L	BB5	COLD_RESETN		IPU SMC_UART0_RXD	BF4	UART_SMC_DEBUGPRT_D2R	
	NC_AON_SLEEP1_RESET_L	BB21	AON_SLEEP1_RESETN		SMC_UART0_TXD	BF8	UART_SMC_DEBUGPRT_R2D	
OUT	SOC_WDOG	BF12	WDOG		IPU SMC_GPIO0	BF11	UPC_SMC_I2C_INT_L	
					SMC_GPIO1	BF13	NC_SMC_GPIO1	
	SOC_DBG_PROBE_VALID	BF6	DBG_PROBE_VALID		SMC_FPWM0	BE12	NC_SMC_FAN_PWM_SMC_SIL_LED_PWM	
BI	EUSB_DBG_P	BF24	DBG_USB_EDP	AOP DEBUG	SMC_FPWM1	BE9	NC_SMC_FAN_TACH	
BI	EUSB_DBG_N	BE24	DBG_USB_EDM					
	SOC_USBDBG_RESREF	BE23	DBG_USB_RESREF					

R1083 10K 5% 1/20W MF 201

XW1022 SHORT-14L-0.1MM-SM

R1042 200 1% 1/20W MF 201

R1066 47K 5% 1/20W MF 201

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g	SYNC_DATE=05/04/2020
PAGE TITLE	SOC: AOP
Apple Inc.	DRAWING NUMBER 051-05392 · SIZE D
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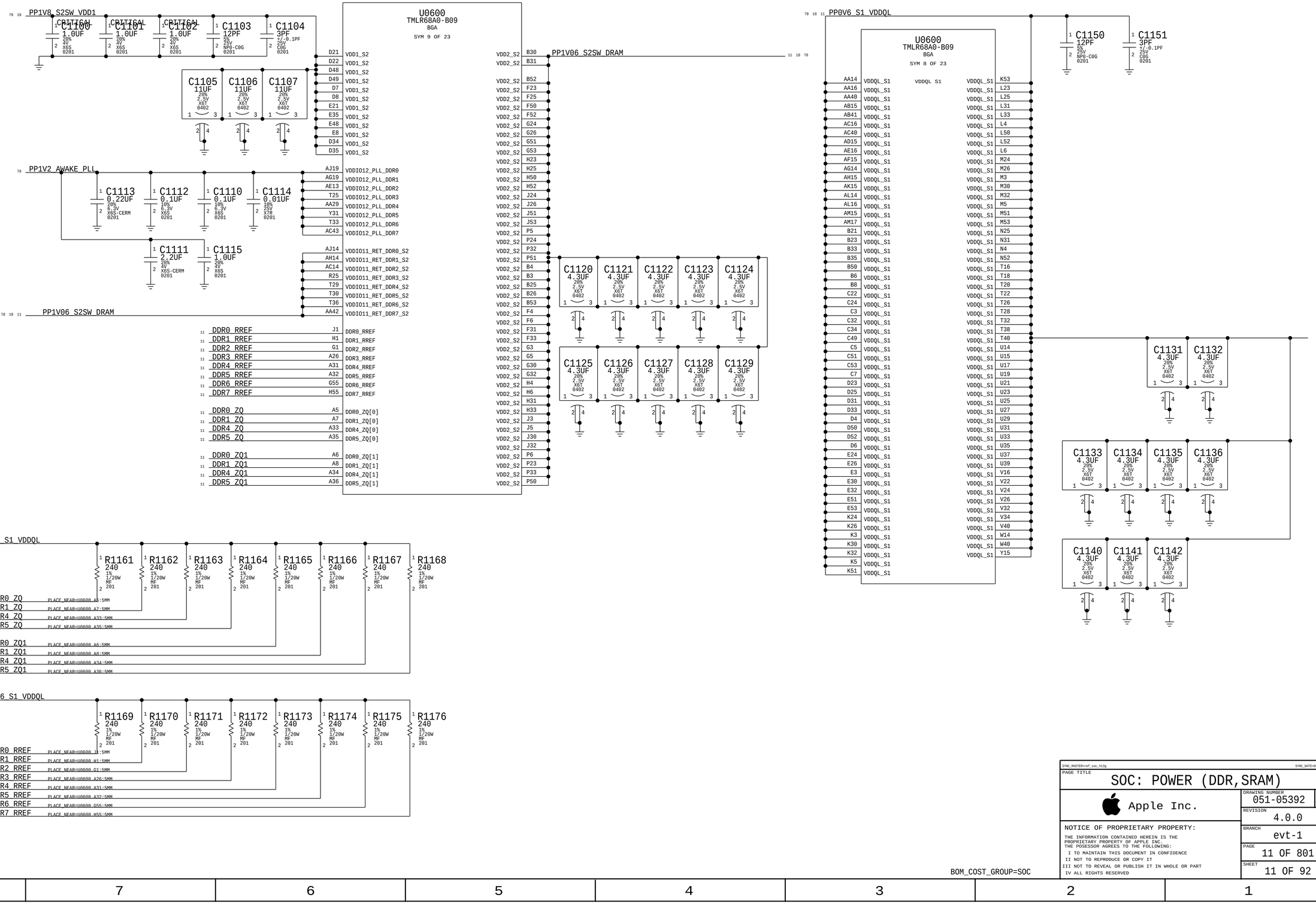
OK2INTEGRATE

SOC: POWER (DDR,SRAM)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00139	138S00138		ALL	4.7UF 20% 4V 0201
138S00164	138S00138		ALL	4.7UF 20% 4V 0201



BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: POWER (DDR,SRAM)

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

REVISION: 4.0.0

BRANCH: evt-1

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OK2INTEGRATE

SOC: POWER (IO)

Internally generated rail

PP0V6_S2_GRP1 — VOLTAGE=0.6V
- C1200 4UF 20% 2.5V X6S 0201
- C1201 4UF 20% 2.5V X6S 0201

PP0V6_S2_GRP2 — VOLTAGE=0.6V

78 10 PP1V25_S2
- C1213 2.2UF 20% 4V X6S-CERM 0201
- C1210 2.2UF 20% 4V X6S-CERM 0201
- C1211 0.1UF 10% 6.3V X6S 0201

78 PP1V25_S2
- C1234 2.2UF 20% 4V X6S-CERM 0201
- C1241 12PF 5% 25V NP0-C0G 0201
- C1242 3PF +/-0.1PF 25V C0G 0201

desense recomends an additional 3 pF cap on PP1v25_awake_grp3
J313 can't fit it so it should go on a project specific page

78 9 7 6 5 PP1V25_AWAKE_TO
- C1233 10UF 20% 6.3V CER-X6S 0402
- XW1230 SM — VOLTAGE=1.25V — PP1V25_AWAKE_GRP3
  - C1230 2.2UF 20% 4V X6S-CERM 0201
  - C1235 12PF 5% 25V NP0-C0G 0201
- XW1231 SM — VOLTAGE=1.25V — PP1V25_AWAKE_GRP4
  - C1231 2.2UF 20% 4V X6S-CERM 0201
  - C1236 12PF 5% 25V NP0-C0G 0201
  - C1237 3PF +/-0.1PF 25V C0G 0201
- XW1232 SM — PP1V25_AWAKE_GRP5 — VOLTAGE=1.25V
  - C1232 2.2UF 20% 4V X6S-CERM 0201
  - C1238 12PF 5% 25V NP0-C0G 0201
  - C1239 3PF +/-0.1PF 25V C0G 0201

78 PP1V8_AWAKE
- C1243 12PF 5% 25V NP0-C0G 0201
- C1244 3PF +/-0.1PF 25V C0G 0201
- C1240 2.2UF 20% 4V X6S-CERM 0201

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AR40	VDD06_GRP1_S2
AP40	VDD06_GRP2_S2
BB22	VDDDIO_HIB_S4
AY23	VDDIO12_AOP_S2
AY25	VDDIO12_AOP_S2
AY27	VDDIO12_AOP_S2
BA24	VDDIO12_AOP_S2
BA26	VDDIO12_AOP_S2
AP39	VDDIO12_GRP1_S2
AF41	VDDIO12_GRP3
AG42	VDDIO12_GRP3
AH40	VDDIO12_GRP3
AL40	VDDIO12_GRP3
AN40	VDDIO12_GRP3
AT40	VDDIO12_GRP4
AV40	VDDIO12_GRP4
AP16	VDDIO12_GRP5
AR17	VDDIO12_GRP5
AT16	VDDIO12_GRP5
AU17	VDDIO12_GRP5
AV16	VDDIO12_GRP5
AW17	VDDIO12_GRP5
AP41	VDDIO18_GRP1
AR41	VDDIO18_GRP1

VDD2_S2_SENSE1	B10	VSNS_VDD2_1 47
VDD2_S2_SENSE2	B37	VSNS_VDD2_2 47
VDD_PCPU_SENSE	AD36	VSNS_VDD_PCPU 47
VDD_ECPU_SENSE	AN23	VSNS_VDD_ECPU 47
VDD_GPU_SENSE	AC23	VSNS_VDD_GPU 47
VDD_SOC_S1_SENSE	AH22	VSNS_VDD_SOC 47
VDD_DISP_S1_SENSE	Y17	VSNS_VDD_DISP 47
VDD_DCS_SENSE	AN17	VSNS_VDD_DCS 47
VDDQL_SENSE	AN15	VSNS_VDDQL 47
VSS_PCPU_SENSE	AD37	VSNS_VSS_PCPU 47
VSS_DDR_SENSE	AN16	VSNS_VSS_DDR 47
VSS_SENSE1	B9	VSNS_VSS_1 47
VSS_SENSE2	B36	VSNS_VSS_2 47

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g — SYNC_DATE=05/04/2020

PAGE TITLE: SOC: POWER (IO)

Apple Inc.

DRAWING NUMBER: 051-05392 — SIZE: D
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OK2INTEGRATE

SOC: POWER (CPU, GPU)

0.575V @ 4400MA

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78 18 13 PPVDD_PCPU_AWAKE

78 18 13 PPVDD_GPU_AWAKE

PPVDD_PCPU_AWAKE 13 18 78

PPVDD_GPU_AWAKE 13 18 78

PPVDD_ECPU_AWAKE 18 78

PPVDD_SOC_S1 78

PPVDD_DISP_S1 18 78

C1300 3PF +/-0.1PF 25V C0G 0201
C1301 12PF 5% 25V NP0-C0G 0201
C1340 12PF 5% 25V NP0-C0G 0201
C1341 3PF +/-0.1PF 25V C0G 0201
C1370 12PF 5% 25V NP0-C0G 0201

C1310 C1311 C1312 C1313 C1314 C1315 C1316 C1317 C1318 C1319 11UF 20% 2.5V X6T 0402

C1320 C1321 C1322 C1323 C1324 C1325 11UF 20% 2.5V X6T 0402

C1330 C1331 C1332 C1333 C1334 C1335 C1336 C1337 11UF 20% 2.5V X6T 0402

C1350 C1351 C1352 11UF 20% 2.5V X6T 0402

C1353 C1354 C1355 C1356 C1357 11UF 20% 2.5V X6T 0402

C1361 C1362 C1363 C1364 11UF 20% 2.5V X6T 0402

C1365 C1366 11UF 20% 2.5V X6T 0402

AE33	VDD_PCPU	VDD_PCPU	AP45
AE35	VDD_PCPU	VDD_PCPU	AP46
AE36	VDD_PCPU	VDD_PCPU	AP47
AE37	VDD_PCPU	VDD_PCPU	AP48
AF33	VDD_PCPU	VDD_PCPU	AP49
AF36	VDD_PCPU	VDD_PCPU	AP50
AF39	VDD_PCPU	VDD_PCPU	AP51
AG34	VDD_PCPU	VDD_PCPU	AP52
AG38	VDD_PCPU	VDD_PCPU	AR30
AH34	VDD_PCPU	VDD_PCPU	AR32
AH39	VDD_PCPU	VDD_PCPU	AR33
AJ33	VDD_PCPU	VDD_PCPU	AR35
AJ34	VDD_PCPU	VDD_PCPU	AR36
AK29	VDD_PCPU	VDD_PCPU	AR37
AK33	VDD_PCPU	VDD_PCPU	AR39
AK35	VDD_PCPU		
AK36	VDD_PCPU	VDD_ECPU	AK25
AK38	VDD_PCPU	VDD_ECPU	AL26
AK40	VDD_PCPU	VDD_ECPU	AL28
AK41	VDD_PCPU	VDD_ECPU	AL29
AK42	VDD_PCPU	VDD_ECPU	AN24
AK43	VDD_PCPU	VDD_ECPU	AN29
AK44	VDD_PCPU	VDD_ECPU	AP25
AK45	VDD_PCPU	VDD_ECPU	AR26
AK46	VDD_PCPU	VDD_ECPU	AR28
AL30	VDD_PCPU		
AL32	VDD_PCPU	VDD_SOC_S1	AB23
AL37	VDD_PCPU	VDD_SOC_S1	AC33
AL41	VDD_PCPU	VDD_SOC_S1	AC38
AL42	VDD_PCPU	VDD_SOC_S1	AE23
AL43	VDD_PCPU	VDD_SOC_S1	AE32
AL44	VDD_PCPU	VDD_SOC_S1	AE38
AL45	VDD_PCPU	VDD_SOC_S1	AF28
AL46	VDD_PCPU	VDD_SOC_S1	AG23
AM29	VDD_PCPU	VDD_SOC_S1	AG39
AM34	VDD_PCPU	VDD_SOC_S1	AJ20
AM38	VDD_PCPU	VDD_SOC_S1	AJ22
AM41	VDD_PCPU	VDD_SOC_S1	AJ24
AM42	VDD_PCPU	VDD_SOC_S1	AJ26
AM43	VDD_PCPU	VDD_SOC_S1	AJ28
AM44	VDD_PCPU	VDD_SOC_S1	AJ30
AM45	VDD_PCPU	VDD_SOC_S1	AJ32
AM46	VDD_PCPU	VDD_SOC_S1	AL20
AM47	VDD_PCPU	VDD_SOC_S1	AL22
AM48	VDD_PCPU	VDD_SOC_S1	AL24
AM49	VDD_PCPU	VDD_SOC_S1	AM39
AM50	VDD_PCPU	VDD_SOC_S1	AN18
AM51	VDD_PCPU	VDD_SOC_S1	AN20
AM52	VDD_PCPU	VDD_SOC_S1	AN22
AM53	VDD_PCPU	VDD_SOC_S1	AR18
AM54	VDD_PCPU	VDD_SOC_S1	AR22
AM55	VDD_PCPU	VDD_SOC_S1	AR24
AN33	VDD_PCPU	VDD_SOC_S1	AT33
AN34	VDD_PCPU	VDD_SOC_S1	AT35
AN38	VDD_PCPU	VDD_SOC_S1	AT37
AN42	VDD_PCPU	VDD_SOC_S1	AU18
AN43	VDD_PCPU	VDD_SOC_S1	AU20
AN44	VDD_PCPU	VDD_SOC_S1	AU22
AN45	VDD_PCPU	VDD_SOC_S1	AU24
AN46	VDD_PCPU	VDD_SOC_S1	AU26
AN47	VDD_PCPU	VDD_SOC_S1	AU28
AN48	VDD_PCPU	VDD_SOC_S1	AU30
AN49	VDD_PCPU	VDD_SOC_S1	AU38
AN50	VDD_PCPU	VDD_SOC_S1	Y21
AN51	VDD_PCPU	VDD_SOC_S1	Y26
AN52	VDD_PCPU	VDD_SOC_S1	Y36
AN53	VDD_PCPU		
AN54	VDD_PCPU		
AN55	VDD_PCPU		
AP29	VDD_PCPU		
AP33	VDD_PCPU		
AP38	VDD_PCPU		
AP43	VDD_PCPU		
AP44	VDD_PCPU		

AA24	VDD_GPU	VDD_GPU	AE26
AA26	VDD_GPU	VDD_GPU	AE27
AA28	VDD_GPU	VDD_GPU	AE29
AA31	VDD_GPU	VDD_GPU	AE30
AA33	VDD_GPU	VDD_GPU	AE31
AA35	VDD_GPU	VDD_GPU	AE42
AA37	VDD_GPU	VDD_GPU	AE43
AB25	VDD_GPU	VDD_GPU	AE44
AB27	VDD_GPU	VDD_GPU	AE45
AB28	VDD_GPU	VDD_GPU	AE46
AB30	VDD_GPU	VDD_GPU	AE47
AB32	VDD_GPU	VDD_GPU	AE48
AB34	VDD_GPU	VDD_GPU	AE49
AB36	VDD_GPU	VDD_GPU	AE50
AC24	VDD_GPU	VDD_GPU	AE51
AC26	VDD_GPU	VDD_GPU	AE52
AC31	VDD_GPU	VDD_GPU	AE53
AC35	VDD_GPU	VDD_GPU	AE54
AC37	VDD_GPU	VDD_GPU	AE55
AD25	VDD_GPU	VDD_GPU	AF24
AD27	VDD_GPU	VDD_GPU	AF32
AD32	VDD_GPU	VDD_GPU	AG25
AD34	VDD_GPU	VDD_GPU	AG27
AD41	VDD_GPU	VDD_GPU	AG31
AD42	VDD_GPU	VDD_GPU	AG33
AD43	VDD_GPU		
AD44	VDD_GPU	VDD_DISP_S1	AA19
AD45	VDD_GPU	VDD_DISP_S1	AA21
AD46	VDD_GPU	VDD_DISP_S1	AA23
AD47	VDD_GPU	VDD_DISP_S1	AB22
AD48	VDD_GPU	VDD_DISP_S1	AC19
AD49	VDD_GPU	VDD_DISP_S1	AD22
AD50	VDD_GPU	VDD_DISP_S1	AE19
AD51	VDD_GPU	VDD_DISP_S1	AE21
AD52	VDD_GPU	VDD_DISP_S1	AG21
AD53	VDD_GPU		
AD54	VDD_GPU		
AD55	VDD_GPU		
AE24	VDD_GPU		

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE
SOC: POWER (SOC, CPU, GPU)

Apple Inc.

DRAWING NUMBER 051-05392
SIZE D
REVISION 4.0.0
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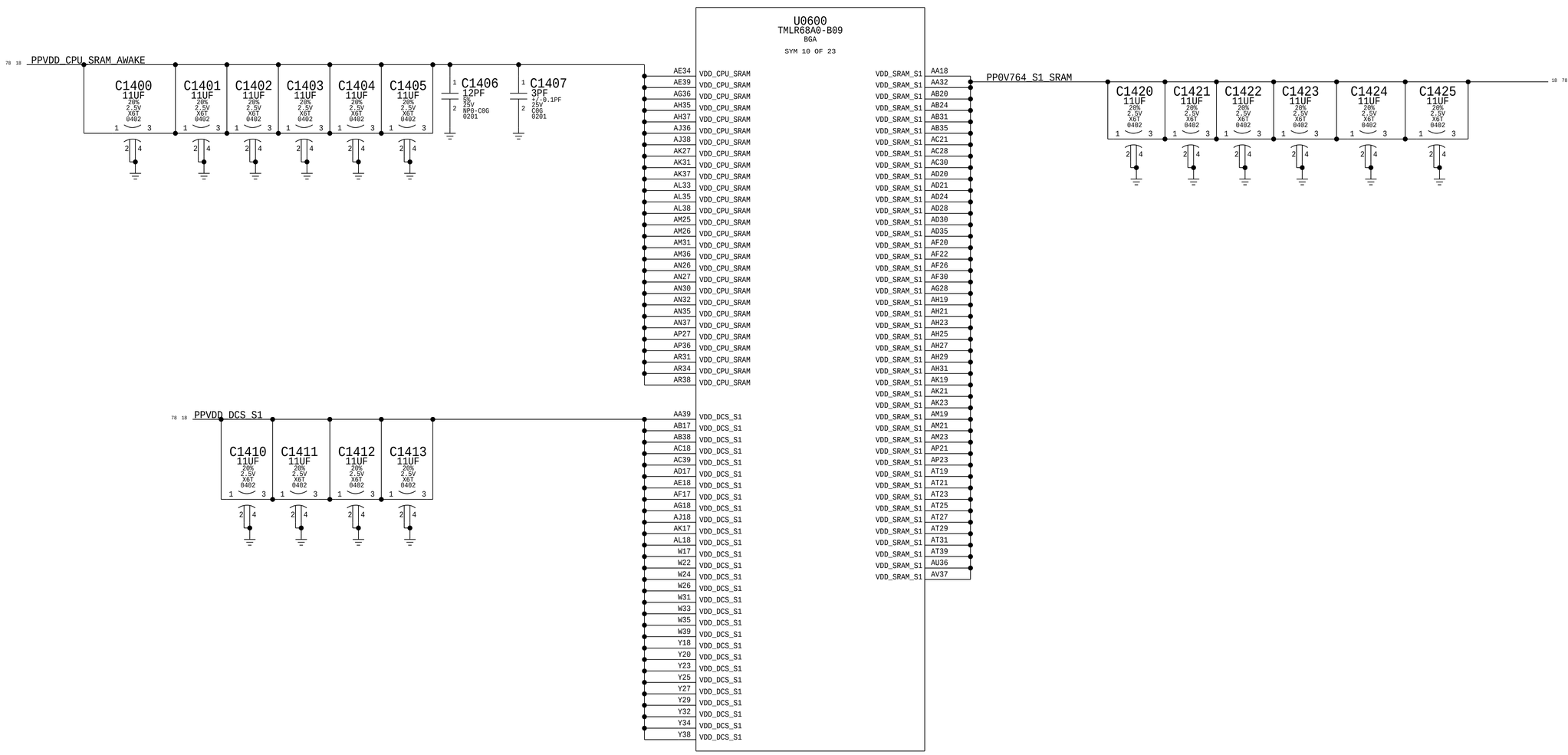
OK2INTEGRATE

SOC: POWER (SRAM, SOC)



BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: POWER (SRAM)

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

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OK2INTEGRATE

LPDP_RX Power may be grounded,

Wait until Dev Bringup is complete before grounding it.
Until then connect it to PP1V2_AWAKE

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PP0V805_S1_VDD_FIXED
PP0V72_S2_VDD_LOW
PP0V855_S2SW_CIO
PP1V2_S2_CIO
PP1V25_S2
PP1V25_AWAKE_IO
PP1V2_AWAKE_PLL
PP0V805_S1_SOC_VDDFIXEDPCIE_R
PP0V805_S1_SOC_VDDFIXEDPLL_F
PP0V805_S1_SOC_VDDFIXEDXTAL_R
PP0V72_S2_VDD_LOWFLPLL_R
PP0V72_S2_VDD_LOWULPLL_R
PP1V2_AWAKE_PLL_PCIE_R
PP1V25_AWAKE_XTAL_F
PP1V25_AWAKE_FMON_R

FL1510 120OHM-25%-0.25A-0.5OHM
FL1580 240-OHM-0.2A-0.9-OHM

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE
SOC: POWER (Fixed, PLL's, Filtered)

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
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OK2INTEGRATE

SOC: GND (1)

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A10	VSS	VSS	AB42
A11	VSS	VSS	AB44
A12	VSS	VSS	AB45
A13	VSS	VSS	AB46
A14	VSS	VSS	AB47
A15	VSS	VSS	AB48
A16	VSS	VSS	AB5
A17	VSS	VSS	AB51
A18	VSS	VSS	AB54
A19	VSS	VSS	AB8
A2	VSS	VSS	AB9
A20	VSS	VSS	AC10
A21	VSS	VSS	AC11
A22	VSS	VSS	AC12
A23	VSS	VSS	AC15
A24	VSS	VSS	AC17
A25	VSS	VSS	AC20
A27	VSS	VSS	AC22
A28	VSS	VSS	AC25
A29	VSS	VSS	AC27
A3	VSS	VSS	AC29
A30	VSS	VSS	AC32
A37	VSS	VSS	AC34
A38	VSS	VSS	AC36
A39	VSS	VSS	AC41
A4	VSS	VSS	AC44
A40	VSS	VSS	AC45
A41	VSS	VSS	AC46
A42	VSS	VSS	AC47
A43	VSS	VSS	AC8
A44	VSS	VSS	AC9
A45	VSS	VSS	AD10
A46	VSS	VSS	AD11
A47	VSS	VSS	AD12
A48	VSS	VSS	AD13
A49	VSS	VSS	AD14
A50	VSS	VSS	AD16
A51	VSS	VSS	AD18
A52	VSS	VSS	AD19
A53	VSS	VSS	AD23
A54	VSS	VSS	AD26
A9	VSS	VSS	AD29
AA10	VSS	VSS	AD31
AA11	VSS	VSS	AD33
AA12	VSS	VSS	AD38
AA13	VSS	VSS	AD39
AA15	VSS	VSS	AD8
AA17	VSS	VSS	AD9
AA20	VSS	VSS	AE10
AA22	VSS	VSS	AE11
AA25	VSS	VSS	AE12
AA27	VSS	VSS	AE14
AA30	VSS	VSS	AE15
AA34	VSS	VSS	AE17
AA36	VSS	VSS	AE2
AA38	VSS	VSS	AE20
AA41	VSS	VSS	AE22
AA43	VSS	VSS	AE25
AA44	VSS	VSS	AE28
AA45	VSS	VSS	AE41
AA46	VSS	VSS	AE5
AA47	VSS	VSS	AE8
AA8	VSS	VSS	AE9
AA9	VSS	VSS	AF10
AB10	VSS	VSS	AF11
AB11	VSS	VSS	AF12
AB12	VSS	VSS	AF13
AB13	VSS	VSS	AF14
AB14	VSS	VSS	AF16
AB16	VSS	VSS	AF18
AB18	VSS	VSS	AF19
AB19	VSS	VSS	AF21
AB2	VSS	VSS	AF23
AB21	VSS	VSS	AF25
AB26	VSS	VSS	AF27
AB29	VSS	VSS	AF31
AB33	VSS	VSS	AF34
AB37	VSS	VSS	AF35
AB39	VSS	VSS	AF37
AB40	VSS	VSS	AF38

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AF40	VSS	VSS	AK12
AF42	VSS	VSS	AK13
AF43	VSS	VSS	AK14
AF44	VSS	VSS	AK16
AF45	VSS	VSS	AK18
AF46	VSS	VSS	AK20
AF47	VSS	VSS	AK22
AF8	VSS	VSS	AK24
AF9	VSS	VSS	AK26
AG10	VSS	VSS	AK28
AG11	VSS	VSS	AK30
AG12	VSS	VSS	AK39
AG15	VSS	VSS	AK47
AG20	VSS	VSS	AK49
AG22	VSS	VSS	AK51
AG24	VSS	VSS	AK54
AG26	VSS	VSS	AK8
AG30	VSS	VSS	AK9
AG32	VSS	VSS	AL10
AG35	VSS	VSS	AL11
AG37	VSS	VSS	AL12
AG41	VSS	VSS	AL13
AG43	VSS	VSS	AL15
AG44	VSS	VSS	AL17
AG45	VSS	VSS	AL19
AG46	VSS	VSS	AL2
AG47	VSS	VSS	AL21
AG48	VSS	VSS	AL23
AG51	VSS	VSS	AL25
AG54	VSS	VSS	AL27
AG8	VSS	VSS	AL31
AG9	VSS	VSS	AL36
AH10	VSS	VSS	AL39
AH11	VSS	VSS	AL47
AH12	VSS	VSS	AL5
AH18	VSS	VSS	AL55
AH2	VSS	VSS	AL8
AH20	VSS	VSS	AL9
AH24	VSS	VSS	AM10
AH26	VSS	VSS	AM11
AH28	VSS	VSS	AM12
AH30	VSS	VSS	AM13
AH33	VSS	VSS	AM14
AH36	VSS	VSS	AM16
AH38	VSS	VSS	AM18
AH41	VSS	VSS	AM20
AH42	VSS	VSS	AM22
AH43	VSS	VSS	AM24
AH44	VSS	VSS	AM27
AH45	VSS	VSS	AM30
AH46	VSS	VSS	AM32
AH47	VSS	VSS	AM33
AH5	VSS	VSS	AM35
AH8	VSS	VSS	AM37
AH9	VSS	VSS	AM40
AJ10	VSS	VSS	AM6
AJ11	VSS	VSS	AM7
AJ12	VSS	VSS	AM8
AJ13	VSS	VSS	AM9
AJ15	VSS	VSS	AN1
AJ21	VSS	VSS	AN10
AJ23	VSS	VSS	AN11
AJ25	VSS	VSS	AN12
AJ27	VSS	VSS	AN13
AJ29	VSS	VSS	AN14
AJ31	VSS	VSS	AN19
AJ35	VSS	VSS	AN2
AJ37	VSS	VSS	AN21
AJ40	VSS	VSS	AN25
AJ41	VSS	VSS	AN28
AJ42	VSS	VSS	AN3
AJ43	VSS	VSS	AN31
AJ44	VSS	VSS	AN36
AJ45	VSS	VSS	AN39
AJ46	VSS	VSS	AN4
AJ47	VSS	VSS	AN41
AJ8	VSS	VSS	AN5
AJ9	VSS	VSS	AN6
AK10	VSS	VSS	AN7
AK11	VSS	VSS	AN8

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AN9	VSS	VSS	AT52
AP10	VSS	VSS	AT53
AP11	VSS	VSS	AT6
AP12	VSS	VSS	AT9
AP13	VSS	VSS	AU10
AP14	VSS	VSS	AU11
AP15	VSS	VSS	AU12
AP18	VSS	VSS	AU13
AP20	VSS	VSS	AU14
AP22	VSS	VSS	AU15
AP24	VSS	VSS	AU16
AP26	VSS	VSS	AU21
AP28	VSS	VSS	AU23
AP3	VSS	VSS	AU25
AP30	VSS	VSS	AU27
AP32	VSS	VSS	AU29
AP34	VSS	VSS	AU3
AP35	VSS	VSS	AU31
AP37	VSS	VSS	AU33
AP42	VSS	VSS	AU37
AP53	VSS	VSS	AU39
AP54	VSS	VSS	AU41
AP55	VSS	VSS	AU44
AP6	VSS	VSS	AU45
AP9	VSS	VSS	AU46
AR10	VSS	VSS	AU47
AR11	VSS	VSS	AU48
AR12	VSS	VSS	AU49
AR13	VSS	VSS	AU50
AR14	VSS	VSS	AU53
AR15	VSS	VSS	AU6
AR16	VSS	VSS	AU7
AR19	VSS	VSS	AU8
AR21	VSS	VSS	AU9
AR23	VSS	VSS	AV10
AR25	VSS	VSS	AV12
AR27	VSS	VSS	AV13
AR29	VSS	VSS	AV14
AR3	VSS	VSS	AV15
AR42	VSS	VSS	AV17
AR43	VSS	VSS	AV18
AR44	VSS	VSS	AV19
AR45	VSS	VSS	AV21
AR46	VSS	VSS	AV22
AR47	VSS	VSS	AV24
AR48	VSS	VSS	AV26
AR49	VSS	VSS	AV28
AR50	VSS	VSS	AV3
AR51	VSS	VSS	AV35
AR52	VSS	VSS	AV38
AR53	VSS	VSS	AV41
AR6	VSS	VSS	AV44
AR9	VSS	VSS	AV45
AT10	VSS	VSS	AV46
AT11	VSS	VSS	AV47
AT12	VSS	VSS	AV48
AT13	VSS	VSS	AV49
AT14	VSS	VSS	AV50
AT15	VSS	VSS	AV53
AT17	VSS	VSS	AV6
AT18	VSS	VSS	AV9
AT22	VSS	VSS	AW10
AT24	VSS	VSS	AW12
AT26	VSS	VSS	AW14
AT28	VSS	VSS	AW15
AT3	VSS	VSS	AW16
AT30	VSS	VSS	AW25
AT34	VSS	VSS	AW27
AT36	VSS	VSS	AW29
AT38	VSS	VSS	AW3
AT41	VSS	VSS	AW30
AT43	VSS	VSS	AW31
AT44	VSS	VSS	AW32
AT45	VSS	VSS	AW34
AT46	VSS	VSS	AW36
AT47	VSS	VSS	AW40
AT48	VSS	VSS	AW41
AT49	VSS	VSS	AW42
AT50	VSS	VSS	AW43
AT51	VSS	VSS	AW44

U0600 TMLR68A0-B09 BGA SYM 18 OF 23

AW45	VSS	VSS	BA28
AW46	VSS	VSS	BA29
AW47	VSS	VSS	BA3
AW48	VSS	VSS	BA30
AW49	VSS	VSS	BA31
AW50	VSS	VSS	BA34
AW51	VSS	VSS	BA36
AW52	VSS	VSS	BA4
AW53	VSS	VSS	BA40
AW6	VSS	VSS	BA41
AW9	VSS	VSS	BA44
AY10	VSS	VSS	BA45
AY11	VSS	VSS	BA46
AY12	VSS	VSS	BA47
AY14	VSS	VSS	BA48
AY17	VSS	VSS	BA49
AY22	VSS	VSS	BA5
AY24	VSS	VSS	BA50
AY3	VSS	VSS	BA53
AY33	VSS	VSS	BA54
AY35	VSS	VSS	BA55
AY37	VSS	VSS	BA6
AY38	VSS	VSS	BA7
AY39	VSS	VSS	BA8
AY40	VSS	VSS	BA9
AY41	VSS	VSS	BB11
AY42	VSS	VSS	BB14
AY44	VSS	VSS	BB17
AY45	VSS	VSS	BB20
AY46	VSS	VSS	BB23
AY47	VSS	VSS	BB26
AY48	VSS	VSS	BB27
AY49	VSS	VSS	BB28
AY50	VSS	VSS	BB29
AY53	VSS	VSS	BB30
AY6	VSS	VSS	BB31
AY9	VSS	VSS	BB32
B1	VSS	VSS	BB33
B11	VSS	VSS	BB34
B12	VSS	VSS	BB35
B13	VSS	VSS	BB36
B14	VSS	VSS	BB39
B15	VSS	VSS	BB40
B16	VSS	VSS	BB41
B17	VSS	VSS	BB42
B18	VSS	VSS	BB43
B19	VSS	VSS	BB44
B2	VSS	VSS	BB45
B20	VSS	VSS	BB46
B22	VSS	VSS	BB47
B24	VSS	VSS	BB48
B27	VSS	VSS	BB49
B28	VSS	VSS	BB50
B29	VSS	VSS	BB51
B32	VSS	VSS	BB52
B34	VSS	VSS	BB6
B38	VSS	VSS	BB8
B39	VSS	VSS	BC22
B40	VSS	VSS	BC23
B41	VSS	VSS	BC26
B42	VSS	VSS	BC28
B43	VSS	VSS	BC30
B44	VSS	VSS	BC32
B45	VSS	VSS	BC34
B46	VSS	VSS	BC36
B47	VSS	VSS	BC39
B49	VSS	VSS	BC4
B5	VSS	VSS	BC40
B51	VSS	VSS	BC41
B54	VSS	VSS	BC42
B55	VSS	VSS	BC44
B7	VSS	VSS	BC46
BA1	VSS	VSS	BC48
BA18	VSS	VSS	BC50
BA19	VSS	VSS	BC51
BA2	VSS	VSS	BC52
BA20	VSS	VSS	BD1
BA21	VSS	VSS	BD2
BA25	VSS	VSS	BD23
BA27	VSS	VSS	BD24

U0600 TMLR68A0-B09 BGA SYM 19 OF 23

BD25	VSS	VSS	C21
BD26	VSS	VSS	C23
BD28	VSS	VSS	C25
BD30	VSS	VSS	C26
BD32	VSS	VSS	C27
BD34	VSS	VSS	C28
BD36	VSS	VSS	C29
BD37	VSS	VSS	C30
BD38	VSS	VSS	C31
BD39	VSS	VSS	C33
BD40	VSS	VSS	C35
BD41	VSS	VSS	C36
BD42	VSS	VSS	C37
BD44	VSS	VSS	C38
BD46	VSS	VSS	C39
BD48	VSS	VSS	C4
BD50	VSS	VSS	C40
BD51	VSS	VSS	C41
BD52	VSS	VSS	C42
BD53	VSS	VSS	C43
BD54	VSS	VSS	C44
BD55	VSS	VSS	C45
BE1	VSS	VSS	C46
BE11	VSS	VSS	C47
BE14	VSS	VSS	C48
BE17	VSS	VSS	C50
BE2	VSS	VSS	C52
BE20	VSS	VSS	C54
BE22	VSS	VSS	C55
BE25	VSS	VSS	C6
BE27	VSS	VSS	C8
BE29	VSS	VSS	C9
BE3	VSS	VSS	D1
BE31	VSS	VSS	D10
BE33	VSS	VSS	D11
BE35	VSS	VSS	D12
BE37	VSS	VSS	D13
BE41	VSS	VSS	D14
BE43	VSS	VSS	D15
BE45	VSS	VSS	D16
BE47	VSS	VSS	D17
BE49	VSS	VSS	D18
BE5	VSS	VSS	D19
BE51	VSS	VSS	D2
BE53	VSS	VSS	D20
BE54	VSS	VSS	D24
BE55	VSS	VSS	D26
BE8	VSS	VSS	D27
BF2	VSS	VSS	D28
BF22	VSS	VSS	D29
BF23	VSS	VSS	D3
BF25	VSS	VSS	D30
BF27	VSS	VSS	D32
BF29	VSS	VSS	D36
BF3	VSS	VSS	D37
BF31	VSS	VSS	D38
BF33	VSS	VSS	D39
BF35	VSS	VSS	D40
BF37	VSS	VSS	D41
BF41	VSS	VSS	D42
BF43	VSS	VSS	D43
BF45	VSS	VSS	D44
BF47	VSS	VSS	D45
BF49	VSS	VSS	D46
BF51	VSS	VSS	D47
BF53	VSS	VSS	D5
BF54	VSS	VSS	D51
C1	VSS	VSS	D53
C10	VSS	VSS	D54
C11	VSS	VSS	D55
C12	VSS	VSS	D9
C13	VSS	VSS	E1
C14	VSS	VSS	E10
C15	VSS	VSS	E11
C16	VSS	VSS	E12
C17	VSS	VSS	E13
C18	VSS	VSS	E14
C19	VSS	VSS	E15
C2	VSS	VSS	E16
C20	VSS	VSS	E17

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: GND

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

REVISION: 4.0.0

BRANCH: evt-1

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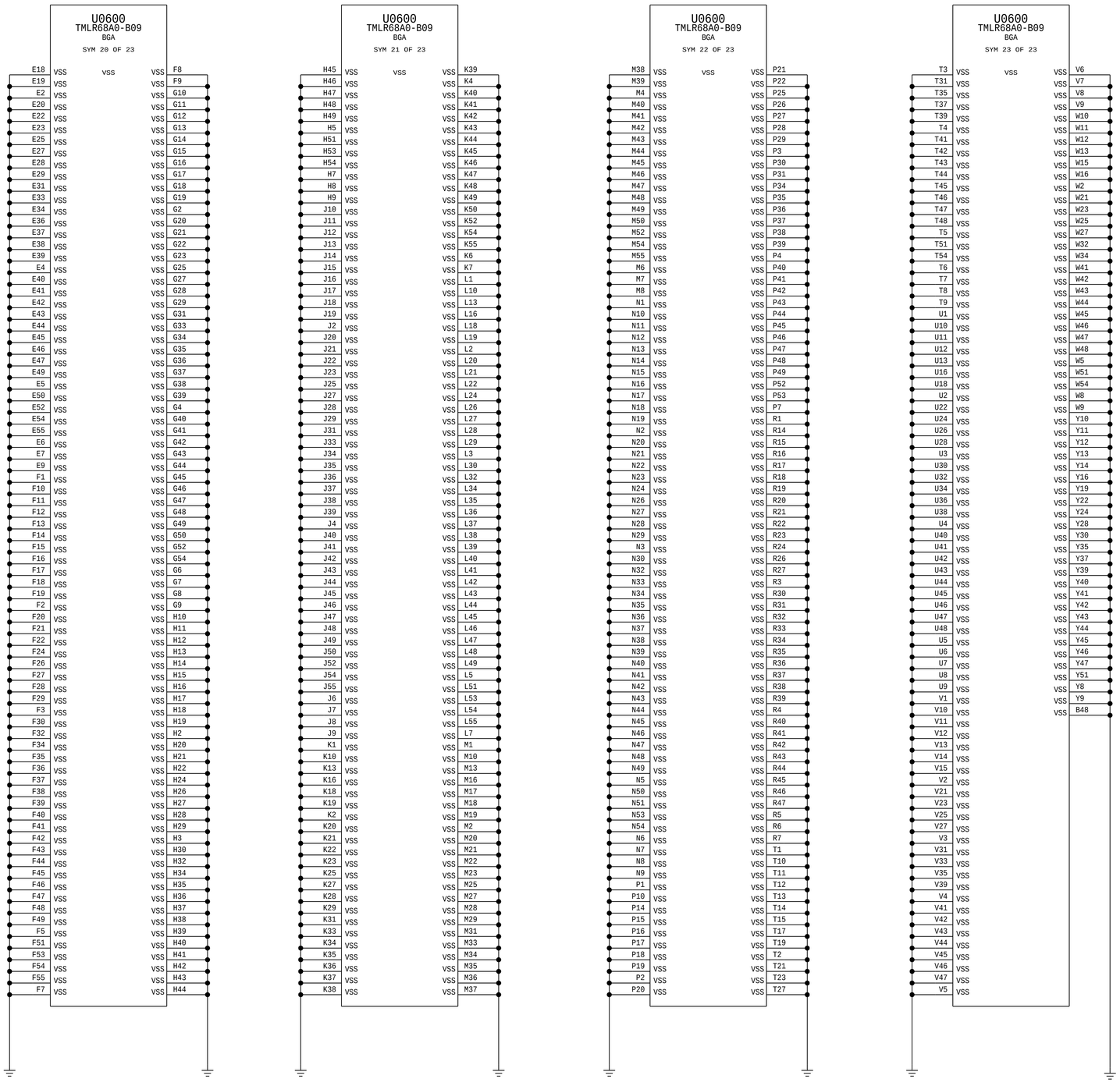
OK2INTEGRATE

SOC: GND (2)



BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE

SOC: GND-2

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D

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PP1V8_S2SW_VDD1

C1800 12PF 5% 25V NP0-C0G 0201	C1801 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1802 12PF 5% 25V NP0-C0G 0201	C1803 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1804 12PF 5% 25V NP0-C0G 0201	C1805 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V06_S2SW_DRAM

C1810 12PF 5% 25V NP0-C0G 0201	C1811 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1812 12PF 5% 25V NP0-C0G 0201	C1813 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1814 12PF 5% 25V NP0-C0G 0201	C1815 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V6_S1_VDDQL

C1820 12PF 5% 25V NP0-C0G 0201	C1821 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1822 12PF 5% 25V NP0-C0G 0201	C1823 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1824 12PF 5% 25V NP0-C0G 0201	C1825 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_PCPU_AWAKE

C1830 12PF 5% 25V NP0-C0G 0201	C1831 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1832 12PF 5% 25V NP0-C0G 0201	C1833 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1834 12PF 5% 25V NP0-C0G 0201	C1835 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_GPU_AWAKE

C1840 12PF 5% 25V NP0-C0G 0201	C1841 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1842 12PF 5% 25V NP0-C0G 0201	C1843 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1844 12PF 5% 25V NP0-C0G 0201	C1845 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_CPU_SRAM_AWAKE

C1850 12PF 5% 25V NP0-C0G 0201	C1851 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1852 12PF 5% 25V NP0-C0G 0201	C1853 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_DCS_S1

C1854 12PF 5% 25V NP0-C0G 0201	C1855 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1856 12PF 5% 25V NP0-C0G 0201	C1857 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V764_S1_SRAM

C1860 12PF 5% 25V NP0-C0G 0201	C1861 3.0PF +/-0.1PF 25V NP0-C0G 0201	C1862 12PF 5% 25V NP0-C0G 0201	C1863 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V805_S1_VDD_FIXED

C1864 12PF 5% 25V NP0-C0G 0201	C1865 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V805_S1_VDD_FIXED

C1866 12PF 5% 25V NP0-C0G 0201	C1867 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V72_S2_VDD_LOW

C1870 12PF 5% 25V NP0-C0G 0201	C1871 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_ECPU_AWAKE

C1872 12PF 5% 25V NP0-C0G 0201	C1873 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_DISP_S1

C1874 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DESENSE

SYNC_MASTER=ref_soc_h13g SYNC_DATE=10/08/2019

PAGE TITLE

SOC: DESENSE CAPS

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D

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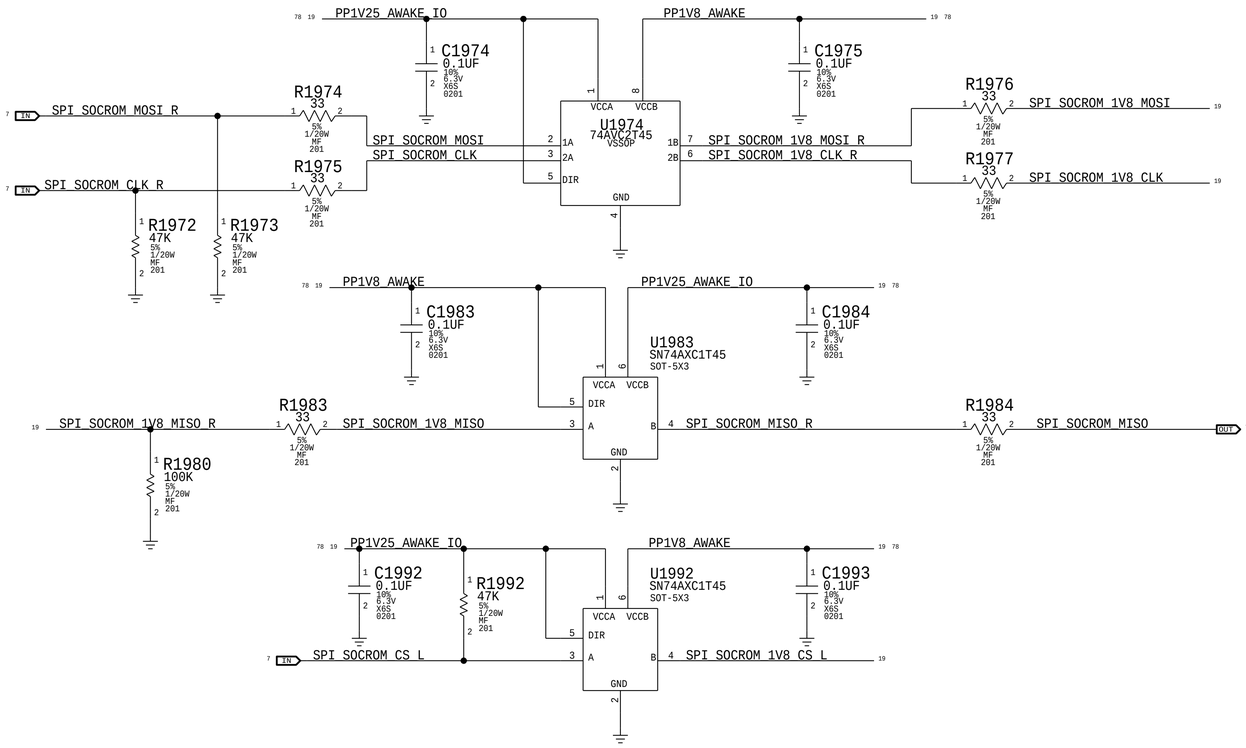
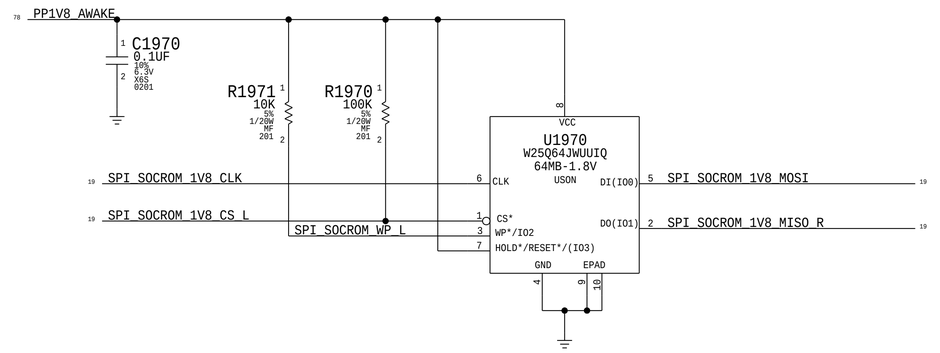
OK2INTEGRATE

SPI NOR (1.8V 64 M-BIT)





BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SPI NOR

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

REVISION: 4.0.0

BRANCH: evt-1

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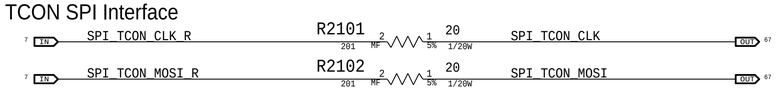
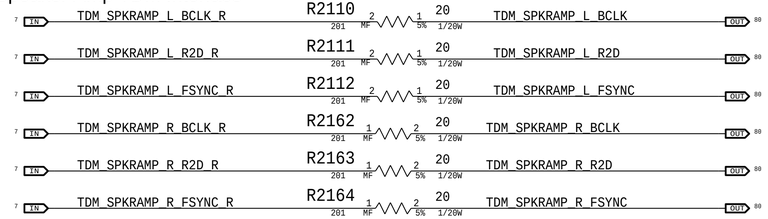
A Series Terminations

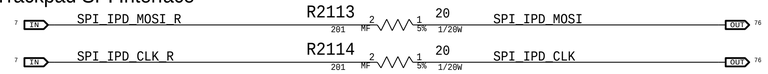
TCON SPI Interface



Speaker Amp TDM Interface

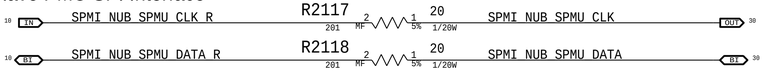


Trackpad SPI Interface

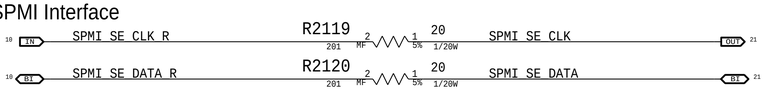


Master PMU SPI Interface

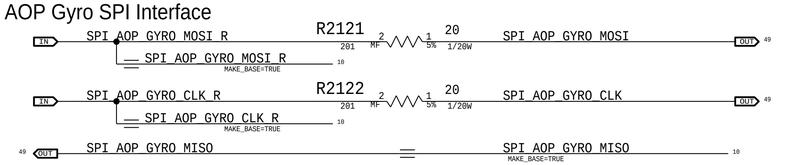
Slave PMU SPI Interface



SPMI Interface

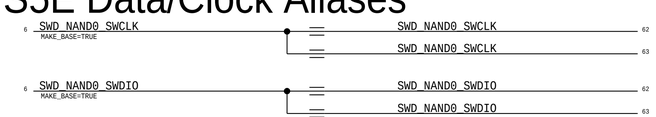


AOP Gyro SPI Interface

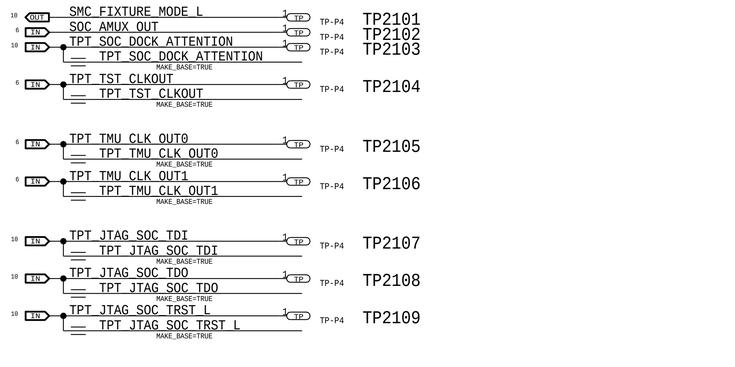


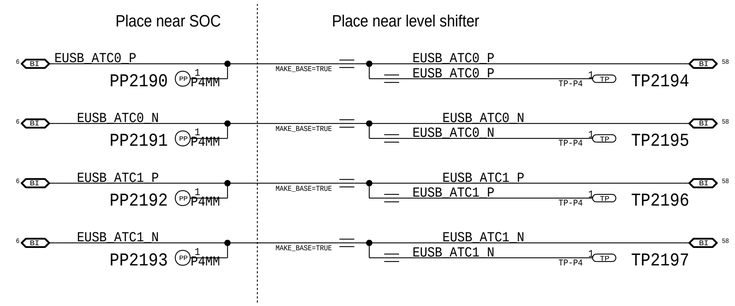
B BOOT Config Aliases

C SSD S5E Data/Clock Aliases

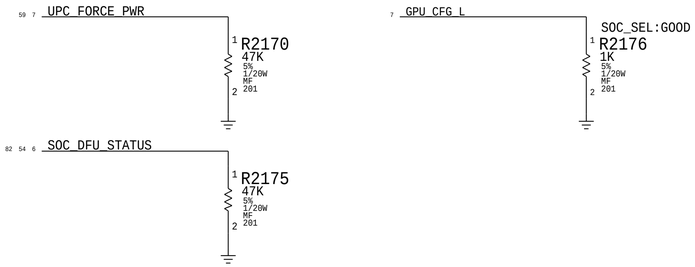


D Test Points





E Pull Down Resistors



BOM_COST_GROUP=SOC

PAGE TITLE: SOC: Project Support

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

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Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***

Per TGA Power Block Diagram v0.3

78 PP1V8_S2
IccMax SE only: 125mA

U5000.F9:3mm C5014 1.0UF 20% 6.3V X5R 0201-1

U5000.F8:3mm C5002 0.22UF 20% 6.3V X5R 0201

U5000.E7:3mm C5003 0.22UF 20% 6.3V X5R 0201

78 PP1V25_S2
IccMax SE only: 10mA

Based on SPMI only use case

VDDBOOST_SE — R5030 0 1/20W MF 0201 5% — VUP_SE

VDDPLL_SE
VDDNV_SE
VDDC_SE

U5000.B5:3mm C5008 0.22UF 20% 6.3V X5R 0201

U5000.E8:3mm C5009 0.22UF 20% 6.3V X5R 0201

U5000.E8:3mm C5010 0.22UF 20% 6.3V X5R 0201

21 79 PP3V8_AON_VDDMAIN — C5051 2.2UF 20% 10V X5R 0201

IccMax: 100mA

As per NXP preliminary estimate, final pending

U5000
SN210VUK/B101V7
WLCSP
OMIT_TABLE

H9	PMUVCC1		
J9	PMUVCC2		
G8	SIMVCC1		
H8	SIMVCC2		
A8	VDDBOOST		
A9	VDDBOOST		
B4	VDDA		
E9	VDDC		
F9	VDDCIN		
F8	VDDIO		
E7	VDDIO_I2C		
J1	VDDIO_SE		
A5	VDDMIX		
E8	VDDNV		
B2	VDDPA		
B5	VDDPLL		
A2	VUP		
A7	VBAT		
D9	VBATPWR		
D4	NFC_CLK_32K		
H6	NFC_CLK_REQ		
A6	NFC_CLK_XTAL1		
G4	NFC_DWL_REQ	21 SE_CTLR_FW_DWLD	
F6	NFC_GPIO0	81 NC_SE_GPIO0	
J7	NFC_GPIO1		50K internal pull-down
J5	NFC_GPIO2_AO		
H4	NFC_GPIO3_AO		
E6	NFC_HSU_CTS	R5042 47K 1/20W MF 201 5% — UART_SE_R2D_RTS_L	
F5	NFC_HSU_RTS	NC_UART_SE_D2R_CTS_L (NO_TEST)	
G5	NFC_HSU_RX	R5041 47K 1/20W MF 201 5% — UART_SE_R2D	
E5	NFC_HSU_TX	NC_UART_SE_D2R (NO_TEST)	
E4	NFC_I2C_SCL		
F4	NFC_I2C_SDA		
J6	NFC_IRQ		
G9	NFC_SIM_SWIO1		
J8	NFC_SIM_SWIO2		
H7	NFC_SPMI_SCLK	20 IN SPMI_SE_CLK	
G7	NFC_SPMI_SDATA	20 BI SPMI_SE_DATA	
H5	NFC_WKUP_REQ	21 SE_DEV_WAKE	
B6	NFC_XTAL2		
G6	TM		
A3	RXP		
A4	RXN		
F7	VSS_DIG		
J3	VSS_DIG		
E1	VSS_DIG_2		
J4	VSS_DIG_LN		
C3	VSS_NFC		
B1	VSS_PA		
C4	VSS_PLL		
D6	VSS_PMU		
C8	VSS_PWR		
C9	VSS_PWR		
C6	VSS_REF		
D8	VSS_SUB		
E3	VSS_SUB		
H3	SE_GPIO0	NC	
F3	SE_GPIO1	NC	
G1	SE_I2C_SCL	NC I2C_SE_SCL (IN 80)	
H1	SE_I2C_SDA	NC I2C_SE_SDA (BI 80)	
F2	SE_ISO_CLK	NC	
F1	SE_ISO_IO	NC	
G3	SE_ISO_RST	NC	
G2	SE_SPI_CLK	NC	
J2	SE_SPI_CS	NC	
H2	SE_SPI_MISO	NC	
E2	SE_SPI_MOSI	NC	
D2	TXVCASCP	NC	
D1	TXVCASCN	NC	
B3	RXVCM	NC	
C2	TXVCM	NC	
A1	TX1	NC	
C1	TX2	NC	
D7	VCASCHI	NC	
C7	VCASCLO	NC	
B8	BOOST_LX	21 79 PP3V8_AON_VDDMAIN	
B9	BOOST_LX		
B7	VHV	VHV_SE	
D3	VTUNE	NC	
D5	VEN	SE_PWR_EN (IN 34)	
C5	VREF	VREF_SE	

Pulls to be added in system, can be NC'd if unused

R5050 1M 5% 1/20W MF 201
R5051 1M 5% 1/20W MF 201

C5004 0.1UF 10% 6.3V CERM-X5R 0201

C5017 0.22UF 20% 6.3V X5R 0201

R5000 47K 5% 1/20W MF 201 — SE_CTLR_FW_DWLD (21)
R5006 47K 5% 1/20W MF 201 — SE_DEV_WAKE (21)

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

SYNC_MASTER=ref_se_ceres
SYNC_DATE=03/29/2020

PAGE TITLE: Secure Element

Apple Inc.

DRAWING NUMBER: 051-05392
SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
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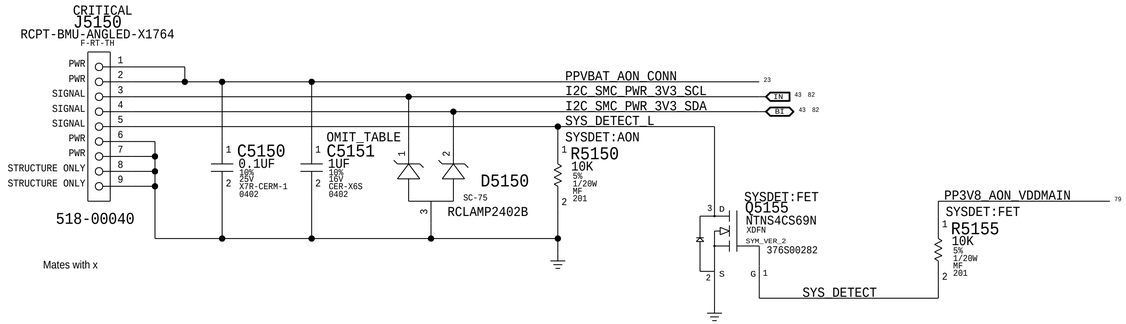

BMU output is enabled after power is
supplied by other means, such as USBC connector.
MLB is thus unpowered during system assembly.

BOM_COST_GROUP=BATTERY

SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE

BMU Connector, Btn Logic

Apple Inc.

DRAWING NUMBER 051-05392

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*** OK2INTEGRATE ***

PPDCIN_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

CRITICAL C5201 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5202 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5203 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C520A 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C520B 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C520C 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C520D 2.2UF 20% 35V X5R-CERM 0402

CRITICAL C5204 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5205 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5206 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5205 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5206 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5207 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
PACK_IGNORE=TRUE PACK_OPTION=CHGR_60W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_60W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_75W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_75W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_75W

CKPLUS_WAIVE=CAPDERATE CKPLUS_WAIVE=CAPDERATE CKPLUS_WAIVE=CAPDERATE

CRITICAL C5250 68UF 20% 16V POLY-TANT CASE-D2E-SM CAPMAT=POLY-TANT
CRITICAL C5251 68UF 20% 16V POLY-TANT CASE-D2E-SM CAPMAT=POLY-TANT
CRITICAL C5252 68UF 20% 16V POLY-TANT CASE-D2E-SM CAPMAT=POLY-TANT
CRITICAL C5253 68UF 20% 16V POLY-TANT CASE-D2E-SM CAPMAT=POLY-TANT
PACK_IGNORE=TRUE PACK_OPTION=CHGR_60W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_60W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_75W
PACK_IGNORE=TRUE PACK_OPTION=CHGR_75W

CRITICAL C5254 33UF 20% 25V TANT CASED12-SM CAPMAT=POLY-TANT
CRITICAL C5255 33UF 20% 25V TANT CASED12-SM CAPMAT=POLY-TANT
CRITICAL C5256 2.2UF 20% 25V X5R 0402-1
CRITICAL C5257 2.2UF 20% 25V X5R 0402-1
C5258 1000PF 10% 25V X7R 0201
PACK_OPTION=CHGR_40W
PACK_OPTION=CHGR_40W

FROM USB-C SOURCE
PPDCIN_AONSW

CRITICAL R5220 0.01 0.5% 0.5W MF 0306 NO_XNET_CONNECTION=1 (AMON) 2-CELL: 0.02 OHM 3-CELL: 0.01 OHM 107S00053

CRITICAL L5230 2.7UH-20%-12.5A-0.01960HM IHLP4040BD-PIMA102D-COMBO 152S00198

CHGR_PHASE1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_PHASE2 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL Q5230 SIZ342DT PWRPAIR-3X3-COMBO ALLOW_APPLE_PREFIX=Q
CRITICAL Q5240 SIZ342DT PWRPAIR-3X3-COMBO ALLOW_APPLE_PREFIX=Q

CHGR_GATE_Q1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_GATE_Q2 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q3 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4 DIDT=TRUE SWITCH_NODE=TRUE

PPVBAT_AON_CHGR_REG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V

CRITICAL F5200 12A-32V-0.00450HM 1206
TO SYSTEM
PPBUS_AON

PPVBAT_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=13.05V

CRITICAL C5265 2.2UF 20% 25V X5R 0402-1
CRITICAL C5266 2.2UF 20% 25V X5R 0402-1
CRITICAL C5267 0.1UF 10% 25V X5R 0201
CRITICAL C5268 0.01UF 10% 25V X5R-CERM 0201

PP5201 P2MM SM CHGR_GATE_Q1 PLACE_SIDE=TOP PACK_IGNORE=TRUE PACK_OPTION=CHGR_TP_TOP
PP5211 P2MM SM PLACE_SIDE=BOTTOM PACK_OPTION=CHGR_TP_BOT
PP5202 P2MM SM CHGR_GATE_Q2 PLACE_SIDE=TOP PACK_IGNORE=TRUE PACK_OPTION=CHGR_TP_TOP
PP5212 P2MM SM PLACE_SIDE=BOTTOM PACK_OPTION=CHGR_TP_BOT
PP5203 P2MM SM CHGR_GATE_Q3 PLACE_SIDE=TOP PACK_IGNORE=TRUE PACK_OPTION=CHGR_TP_TOP
PP5213 P2MM SM PLACE_SIDE=BOTTOM PACK_OPTION=CHGR_TP_BOT
PP5204 P2MM SM CHGR_GATE_Q4 PLACE_SIDE=TOP PACK_IGNORE=TRUE PACK_OPTION=CHGR_TP_TOP
PP5214 P2MM SM PLACE_SIDE=BOTTOM PACK_OPTION=CHGR_TP_BOT
PP5205 P2MM SM CHGR_PHASE1 PLACE_SIDE=TOP PACK_IGNORE=TRUE PACK_OPTION=CHGR_TP_TOP
PP5215 P2MM SM PLACE_SIDE=BOTTOM PACK_OPTION=CHGR_TP_BOT
PP5206 P2MM SM CHGR_PHASE2 PLACE_SIDE=TOP PACK_IGNORE=TRUE PACK_OPTION=CHGR_TP_TOP
PP5216 P2MM SM PLACE_SIDE=BOTTOM PACK_OPTION=CHGR_TP_BOT
PP5207 P2MM SM CHGR_EN_MVR PACK_OPTION=CHGR_TP
PP5208 P2MM SM CHGR_INT_1V8_L PACK_OPTION=CHGR_TP

CHGR_CSI_P PLACE_NEAR=U5200.D5:2MM
R5221 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_N PLACE_NEAR=U5200.C5:2MM
R5222 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_FILT_P
CRITICAL C5221 0.047UF 10% 50V CER-X7R 0402
CHGR_CSI_FILT_N
CRITICAL C5222 0.047UF 10% 50V CER-X7R 0402

CRITICAL C5220 0.47UF 20% 4V CERM-X5R-1 201 NO_XNET_CONNECTION=1

CHGR_LX1 DIDT=TRUE SWITCH_NODE=TRUE
XW5230 SM
CRITICAL C5230 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT1_RC DIDT=TRUE SWITCH_NODE=TRUE
R5230 0 5% 1/16W MF-LF 402
CHGR_BOOT1 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_LX2 DIDT=TRUE SWITCH_NODE=TRUE
XW5240 SM
CRITICAL C5240 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT2_RC DIDT=TRUE SWITCH_NODE=TRUE
R5240 0 5% 1/16W MF-LF 402
CHGR_BOOT2 DIDT=TRUE SWITCH_NODE=TRUE

R5275 4.7 5% 1/20W MF 201
VOLTAGE=5V PPCHGR_VDDA
CRITICAL C5275 2.2UF 20% 25V X5R-CERM 0402-1
VOLTAGE=5V PPCHGR_VDDP
CRITICAL C5277 10UF 20% 10V X5R 0603-1

XW5260 SM PLACE_NEAR=Q5240.3:2MM

NO_XNET_CONNECTION=1
CRITICAL R5260 0.005 (PMON) 1% 1W MF 0612-8 2-CELL: 0.010 OHM 3-CELL: 0.005 OHM 107S00087

CRITICAL Q5265 SI7655DN-COMBO PWRPK-1212-8 SYM-VER-2
C5264 1000PF 10% 25V X7R 0201
C5269 0.1UF 10% 25V X5R 0201
C5263 4700PF 10% 25V CER-X5R 0201
TO/FROM BATTERY
PPVBAT_AON_CONN
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=13.05V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

CHGR_CSO_P PLACE_NEAR=U5200.A4:2MM
R5261 1.00 1% 1/20W MF-LF 0201
CHGR_CSO_N PLACE_NEAR=U5200.B4:2MM
R5262 1.00 1% 1/20W MF-LF 0201
CHGR_CSO_FILT_P
CRITICAL C5261 0.047UF 10% 50V CER-X7R 0402
CHGR_CSO_FILT_N
CRITICAL C5262 0.047UF 10% 50V CER-X7R 0402

CRITICAL C5260 0.47UF 20% 4V CERM-XSR-1 201 NO_XNET_CONNECTION=1

CRITICAL Q5270 NTNS4CS69N XDFN SYM_VER_1 <rdar://37259372&39763505>
SAVE_BAT_S
SAVE_BAT_G
PPDCIN_AONSW
R5271 200K 1% 1/20W MF 201
R5263 1K 5% 1/20W MF 201
R5270 24K 5% 1/20W MF 201
CRITICAL D5270 DFN0201 ALLOW_APPLE_PREFIX=D GDZ5V6LP3-55

PPDCIN_AONSW
R5215 750K 1% 1/20W MF 201
CHGR_AUX_DET
NOSTUFF C5216 0.01UF 10% 16V X5R-CERM 0201
R5216 255K 1% 1/20W MF 201

PP1V8_S2
C5280 1.0UF 20% 6.3V X5R 0201-1

U5200 ISL9240HI WCSP
CRITICAL
SCH SYMBOL 353S01525

B5	P_IN	GATE_Q1	H1
C5	CSIN	BOOT1	F1
D5	CSIP	LX1	G1
A5	PBUS_PWR	GATE_Q2	E1
D3	AUX_DET	GATE_Q3	D1
		LX2	B1
		BOOT2	C1
		GATE_Q4	A1
	PBUS	A3	CHGR_PBUS_SNS (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000)
	CSOP	A4	
	CSON	B4	
	BGATE	B3	CHGR_BGATE
	VBAT	C3	CHGR_VBAT
F5	VDDIO1P8	EN_VR1	F2 NC_CHGR_EN_VR1
G5	SDA	SMC_RST*	H4 NC_CHGR_SMC_RST_L
H5	SCL	IRQ*	H3 CHGR_INT_1V8_L
G2	SMC_RST_IN	CBC_ON	H2 NC_CHGR_CBC_ON
G3	HPWR_EN*	(5V) EN_MVR	F4 CHGR_EN_MVR
E5	COMP	(OD) AUX_OK	F3 CHGR_AUX_OK
G4	CELL	AMON	D4 CHGR_AMON
B2	NC0	BMON	C4 CHGR_BMON
C2	NC1		
E4	NC2		
A2	VDDA		
D2	VDDP		
E3	AGND		
E2	PGND		

I2C_SMC_PWR_1V8_SDA
I2C_SMC_PWR_1V8_SCL
CHGR_RST_IN
CHGR_COMP
H:3-CELL L:2-CELL

CRITICAL C5270 0.12UF 10% 10V X5R 0402
NOSTUFF CRITICAL C5271 0.12UF 10% 10V X5R 0402

PPVBAT_AON_CHGR_REG
CRITICAL C5278 2.2UF 20% 25V X5R-CERM 0402

BOM_COST_GROUP=BATTERY

SYNC_MASTER=ref_charger_suona SYNC_DATE=05/02/2020
PAGE TITLE: PBUS SUPPLY & BATTERY CHARGER
Apple Inc.
DRAWING NUMBER: 051-05392 SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
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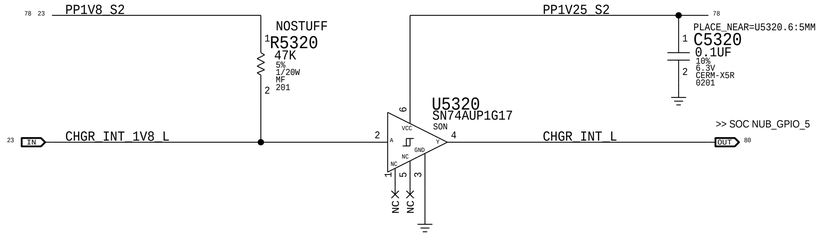
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

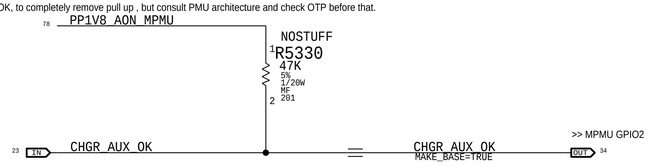
Stuff R5320 in case, glitch during power sequencing is a concern.



CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.

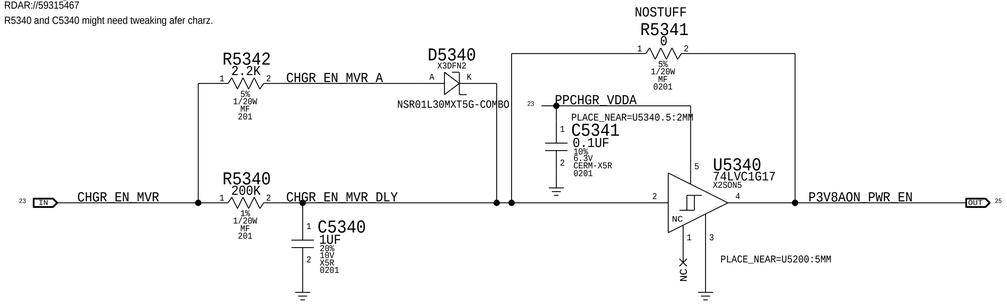
OK, to completely remove pull up , but consult PMU architecture and check OTP before that.



Delay for 3.8V VR Enable

RDAR://59315467

R5340 and C5340 might need tweaking afer charz.



BOM_COST_GROUP=BATTERY

SYNC_MASTER=ref_charger_suona SYNC_DATE=05/02/2020

PAGE TITLE

BATTERY CHARGER SUPPORT

Apple Inc.

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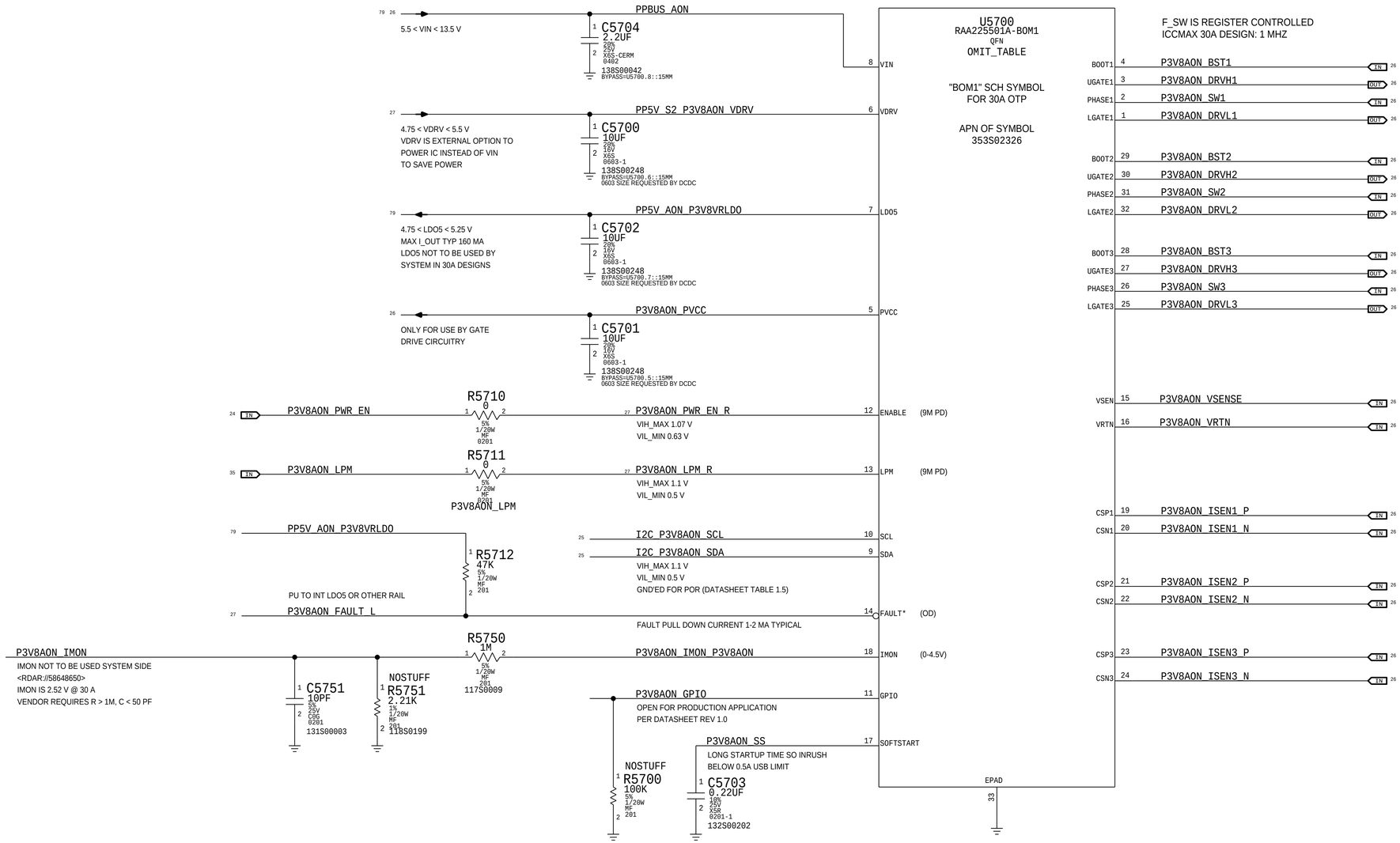
*** OK2RELEASE ***

3V8 AON CONTROLLER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_vr_iceman SYNC_DATE=04/20/2020

PAGE TITLE

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*** OK2RELEASE ***

PPBUS_AON

P3V8AON_DRVH1 — R5804 2.2 5% 1/20W MF 201 117S0056 <RDAR:/59524111> — P3V8AON_DRVH1_R

P3V8AON_BST1 — R5803 0 5% 1/20W MF 0201 117S0201 — P3V8AON_BST1_RC — C5811 0.1UF 10% 25V X7R-CERM-1 0402 132S0438 — P3V8AON_SW1

NOSTUFF D5800 SBR1A30T5 S0D523 371S00245 3V8_EXT_DIODE — P3V8AON_PVCC

P3V8AON_DRVL1 — R5805 1 5% 1/10W MF-LF 402 116S0006 — P3V8AON_DRVL1_R

P3V8AON_ISEN1_P

P3V8AON_ISEN1_N

CRITICAL Q5800 CSD58889Q3D Q3D 376S00012 — TG, TGR, BG, VIN, VSW, PGND

CRITICAL C5800 33UF 20% 16V TANT CASE-T 128S00009 3V8_AON_PBUS-B12

CRITICAL C5801 33UF 20% 16V TANT CASE-T 128S00009 3V8_AON_PBUS-B12

CRITICAL C5800 33UF 20% 16V TANT CASED12-SM 128S0436 PACK_IGNORE=TRUE 3V8_AON_PBUS-D12

CRITICAL C5801 33UF 20% 16V TANT CASED12-SM 128S0436 PACK_IGNORE=TRUE 3V8_AON_PBUS-D12

CRITICAL C5800 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 PACK_IGNORE=TRUE 3V8_AON_PBUS-02

CRITICAL C5801 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 PACK_IGNORE=TRUE 3V8_AON_PBUS-02

C5804 2.2UF 20% 25V X6S-CERM 0402 138S00042

MIRROR_WITH=C5804 C5805 2.2UF 20% 25V X6S-CERM 0402 138S00042

P3V8AON_VSW1

116S0007 R5809 1.5 5% 1/10W MF-LF 402 — P3V8AON_SNUB1

131S0514 C5809 150PF 5% 50V C0G-CERM 0402 <RDAR:/59524111>

CRITICAL L5800 1UH-20%-11A-0.0127OHM PIHA052D-SM 152S00265

PP3V8AON_PH1

107S00373 R5800 0.004 1% 1/3W LF 0306 NO_XNET_CONNECTION=1

ICCMAX = 30 A

PP3V8_AON_VDDMAIN

CRITICAL C5890 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

CRITICAL C5891 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

CRITICAL C5892 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

CRITICAL C5893 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

CRITICAL C5894 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

CRITICAL C5895 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

MIRROR_WITH=C5887 C5886 2.2UF 20% 25V X6S-CERM 0402 138S00042

C5887 2.2UF 20% 25V X6S-CERM 0402 138S00042

MIRROR_WITH=C5889 C5888 2.2UF 20% 25V X6S-CERM 0402 138S00042

C5889 2.2UF 20% 25V X6S-CERM 0402 138S00042

NOSTUFF C5814 220PF 5% 50V C0G 0201-1

C5810 5600PF 10% 10V CERM-X7R 0201 132S0370

R5801 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS1_P

NOSTUFF C5815 220PF 5% 50V C0G 0201-1

R5802 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS1_N

PPBUS_AON

P3V8AON_DRVH2 — R5824 1.5 5% 1/8W TK 0402 107S00371 — P3V8AON_DRVH2_R

P3V8AON_BST2 — R5823 0 5% 1/16W MTL-FILM 0402 116S00006 — P3V8AON_BST2_RC — C5831 0.22UF 10% 25V X7R 0402 132S0401 — P3V8AON_SW2

NOSTUFF D5820 SBR1A30T5 S0D523 371S00245 3V8_EXT_DIODE — P3V8AON_PVCC

P3V8AON_DRVL2 — R5825 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL2_R — R5826 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL2_RR

P3V8AON_ISEN2_P

P3V8AON_ISEN2_N

ALLOW_APPLE_PREFIX=Q CRITICAL Q5820 AONE36196 DFN 376S00281 — G1, D2/S1, G2, S2, VER-1

CRITICAL C5820 33UF 20% 16V TANT CASE-T 128S00009 3V8_AON_PBUS-B12

CRITICAL C5821 33UF 20% 16V TANT CASE-T 128S00009 3V8_AON_PBUS-B12

CRITICAL C5820 33UF 20% 16V TANT CASED12-SM 128S0436 PACK_IGNORE=TRUE 3V8_AON_PBUS-D12

CRITICAL C5820 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 PACK_IGNORE=TRUE 3V8_AON_PBUS-02

C5824 2.2UF 20% 25V X6S-CERM 0402 138S00042

MIRROR_WITH=C5824 C5825 2.2UF 20% 25V X6S-CERM 0402 138S00042

SAME SW NET ON BOTH SIDES — P3V8AON_SW2

R5829 NOSTUFF 2.2 5% 1/16W MF-LF 402 DIDT=TRUE SWITCH_NODE=TRUE — P3V8AON_SNUB2

C5829 NOSTUFF 100PF 5% 50V C0G 0402

CRITICAL L5820 0.56UH-20%-22.0A-0.0067OHM PILA062D-SM-COMBO 152S01248

PP3V8AON_PH2

107S00090 R5820 0.001 1% 1/3W MF 0306 NO_XNET_CONNECTION=1

NOSTUFF C5834 220PF 5% 50V C0G 0201-1

C5830 5600PF 10% 10V CERM-X7R 0201 132S0370

R5821 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS2_P

NOSTUFF C5835 220PF 5% 50V C0G 0201-1

R5822 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS2_N

PPBUS_AON

P3V8AON_DRVH3 — R5844 1.5 5% 1/8W TK 0402 107S00371 — P3V8AON_DRVH3_R

P3V8AON_BST3 — R5843 0 5% 1/16W MTL-FILM 0402 116S00006 — P3V8AON_BST3_RC — C5851 0.22UF 10% 25V X7R 0402 132S0401 — P3V8AON_SW3

NOSTUFF D5840 SBR1A30T5 S0D523 371S00245 3V8_EXT_DIODE — P3V8AON_PVCC

P3V8AON_DRVL3 — R5845 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL3_R — R5846 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL3_RR

P3V8AON_ISEN3_P

P3V8AON_ISEN3_N

ALLOW_APPLE_PREFIX=Q CRITICAL Q5840 AONE36196 DFN 376S00281 — G1, D2/S1, G2, S2, VER-1

CRITICAL C5840 33UF 20% 16V TANT CASE-T 128S00009 3V8_AON_PBUS-B12

CRITICAL C5841 33UF 20% 16V TANT CASE-T 128S00009 3V8_AON_PBUS-B12

CRITICAL C5840 33UF 20% 16V TANT CASED12-SM 128S0436 PACK_IGNORE=TRUE 3V8_AON_PBUS-D12

CRITICAL C5840 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 PACK_IGNORE=TRUE 3V8_AON_PBUS-02

C5844 2.2UF 20% 25V X6S-CERM 0402 138S00042

MIRROR_WITH=C5844 C5845 2.2UF 20% 25V X6S-CERM 0402 138S00042

SAME SW NET ON BOTH SIDES — P3V8AON_SW3

R5849 NOSTUFF 2.2 5% 1/16W MF-LF 402 DIDT=TRUE SWITCH_NODE=TRUE — P3V8AON_SNUB3

C5849 NOSTUFF 100PF 5% 50V C0G 0402

CRITICAL L5840 0.56UH-20%-22.0A-0.0067OHM PILA062D-SM-COMBO 152S01248

PP3V8AON_PH3

107S00090 R5840 0.001 1% 1/3W MF 0306 NO_XNET_CONNECTION=1

NOSTUFF C5854 220PF 5% 50V C0G 0201-1

C5850 5600PF 10% 10V CERM-X7R 0201 132S0370

R5841 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS3_P

NOSTUFF C5855 220PF 5% 50V C0G 0201-1

R5842 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS3_N

NO_XNET_CONNECTION=1 XW5870 SM — P3V8AON_VSNS_XW_P

NO_XNET_CONNECTION=1 XW5871 SM — P3V8AON_VSNS_XW_N

NO_XNET_CONNECTION=1 R5870 0 5% 1/20W MF 0201 117S0201 — P3V8AON_VSENSE

NO_XNET_CONNECTION=1 R5871 0 5% 1/20W MF 0201 117S0201 — P3V8AON_VRTN

NOSTUFF C5870 1UF 20% 10V X6S-CERM 0201 138S00044 NO_XNET_CONNECTION=1

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_vr_iceman SYNC_DATE=04/20/2020

PAGE TITLE: POWER: 3V8 AON (2/2)

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

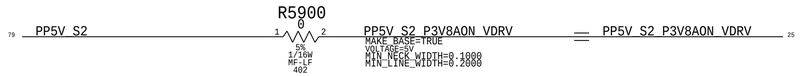
REVISION: 4.0.0

BRANCH: evt-1

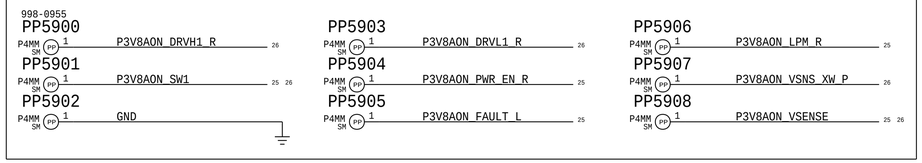
PAGE: 58 OF 801

SHEET: 26 OF 92

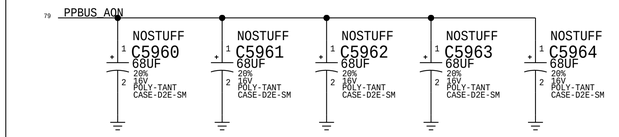
A PP5V_S2 to PP3V8_AON VDRV Connection



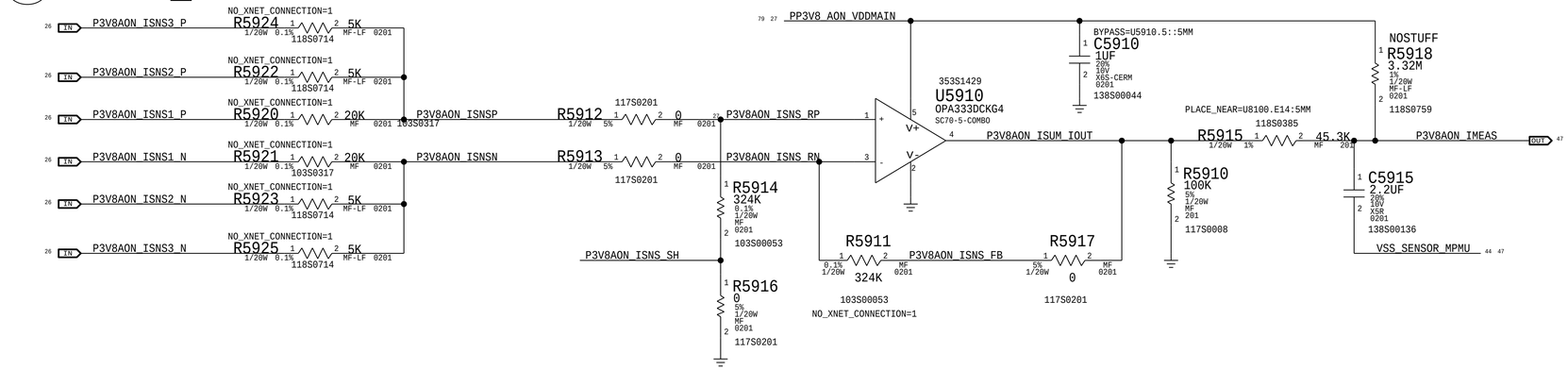
B PP3V8_AON Probe Points



C PPBUS_AON Bulk Capacitance

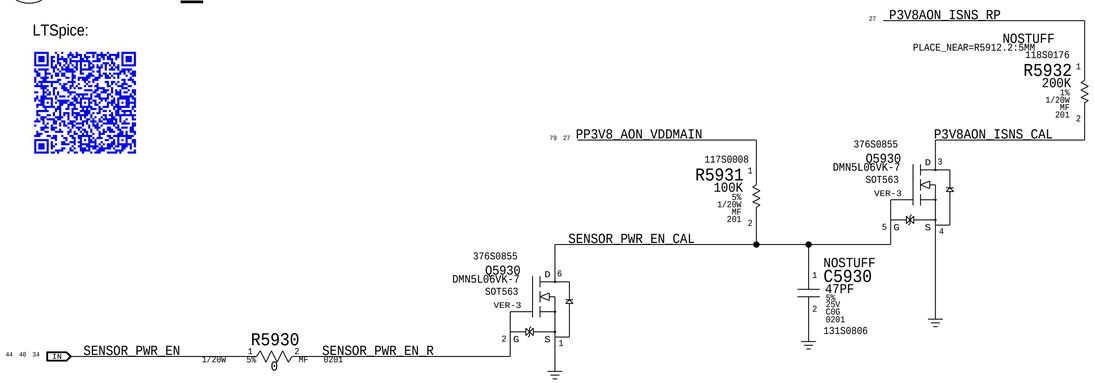


D PP3V8_AON Current Sense



E PP3V8_AON Current Sense Cal Control Circuit

LTSpice:



$X1757GHUB/mlb/sim/ltspice/pp3v8_aon_vddmain/pp3v8_aon_vddmain_current_sense.asc

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=T585_REF_VR_ICEMAN_0.36.0 SYNC_DATE=10/11/2019

PAGE TITLE: POWER: 3V8 AON SUPPORT

Apple Inc.

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SLAVE PMU BUCKS

U7700 SIM BGA SYM 1 OF 4 OMIT_TABLE

BUCK INPUTS

MAIN INPUTS

BUCK OUTPUTS

PP3V8_AON_VDDMAIN (29 28 79)

C7700 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7701 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7702 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7703 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7704 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7705 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7706 1UF 20% 10V X6S-CERM 0201
C7707 1UF 20% 10V X6S-CERM 0201
C7708 1UF 20% 10V X6S-CERM 0201
C7709 1UF 20% 10V X6S-CERM 0201

C770A 1UF 20% 10V X6S-CERM 0201
C770B 1UF 20% 10V X6S-CERM 0201
C770C 1UF 20% 10V X6S-CERM 0201
C770D 1UF 20% 10V X6S-CERM 0201
C770E 1UF 20% 10V X6S-CERM 0201
C770F 1UF 20% 10V X6S-CERM 0201
C770G 1UF 20% 10V X6S-CERM 0201
C770H 1UF 20% 10V X6S-CERM 0201
C770I 1UF 20% 10V X6S-CERM 0201
C770J 1UF 20% 10V X6S-CERM 0201

C770K 1UF 20% 10V X6S-CERM 0201 (PLACE_NEAR=U7700.L1:5MM)
C770L 1UF 20% 10V X6S-CERM 0201
C770M 12PF 5% 25V NP0-C0G 0201 (PLACE_NEAR=U7700.C13:5MM)
C770N 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=U7700.G13:5MM)
C771M 12PF 5% 25V NP0-C0G 0201
C771N 3PF +/-0.1PF 25V C0G 0201
C772M 12PF 5% 25V NP0-C0G 0201
C772N 3PF +/-0.1PF 25V C0G 0201

C773M 12PF 5% 25V NP0-C0G 0201 (PLACE_NEAR=U7700.M2:5MM)
C773N 3PF +/-0.1PF 25V C0G 0201
C774M 12PF 5% 25V NP0-C0G 0201 (PLACE_NEAR=U7700.N6:5MM)
C774N 3PF +/-0.1PF 25V C0G 0201
C775M 12PF 5% 25V NP0-C0G 0201 (PLACE_NEAR=U7700.L13:5MM)
C775N 3PF +/-0.1PF 25V C0G 0201
C776M 12PF 5% 25V NP0-C0G 0201 (PLACE_NEAR=U7700.D9:5MM)
C776N 3PF +/-0.1PF 25V C0G 0201

PP1V5_VLDOINT_SPMU (29)

PP3V8_AON_VDDMAIN (79 29 28)

PP5V_BSTLQ_SPMU (29) VOLTAGE=5V

C7717 0.1UF 10% 10V X6S-CERM 0201 CRITICAL (PLACE_NEAR=U7700.D4:5MM, PLACE_NEAR=U7700.L7:5MM)
C7714 0.1UF 10% 10V X6S-CERM 0201 CRITICAL (PLACE_NEAR=U7700.C9:5MM)
C7715 0.1UF 10% 10V X6S-CERM 0201 CRITICAL

FED BY SPMU BUCK13 (1.2V)POWER ALIAS=>

FED BY MPMU BUCK3 (1.8V)POWER ALIAS=>

PP1V25_S2 (78)

PP1V8_S2 (78)

C7716 0.1UF 10% 10V X6S-CERM 0201 CRITICAL (PLACE_NEAR=U7700.G10:5MM)
C771A 0.1UF 10% 10V X6S-CERM 0201 CRITICAL (PLACE_NEAR=U7700.H10:5MM)

VSS_ANA_SPMU (31 30 28)

U7700 pin map:
C12 VDD_ANA
D3 VDD_ANA
E7 VDD_ANA
G12 VDD_ANA
K3 VDD_ANA
L8 VDD_ANA
L12 VDD_ANA
M6 VDD_ANA
D5 VDD_DIG
D10 VDD_DIG
J3 VDD_DIG
J10 VDD_DIG
D9 VDD_BOOST
B2 VDD_BOOST_LDO
C2 VDD_BOOST_LDO
E9 VDD_BOOST_SNS
D4 VDD_HI_INT1
L4 VDD_HI_INT2
L7 VDD_HI_INT3
M10 VDD_HI_INT4
J11 VDD_HI_INT5
A11 VDD_HI_INT6
C9 VDD_HI_INT7
G10 VDDIO_1V2
H10 VDDIO_BUCK3
K6 VPP
C13 VDD_BUCK5_4_10
C14 VDD_BUCK5_4_10
G13 VDD_BUCK5_4_10
G14 VDD_BUCK5_4_10
M2 VDD_BUCK6
N2 VDD_BUCK6
P2 VDD_BUCK6
N6 VDD_BUCK12
P6 VDD_BUCK12
L13 VDD_BUCK13
L14 VDD_BUCK13
L1 VDD_MAIN_BUCK6
L9 VDD_MAIN_SOUTH
E8 VDD_MAIN
D2 VDD_MAIN_LDO
E2 VDD_MAIN_LDO
D8 VDD_MAIN_SNS
E10 VDD_SNS_SPARE

BUCK4_LX0 F14 — BUCK4_LX0 (31) DIDT=TRUE SWITCH_NODE=TRUE — L7740 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO CRITICAL
BUCK4_LX1 D13 D14 — BUCK4_LX1 (31) DIDT=TRUE SWITCH_NODE=TRUE — L7741 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM CRITICAL
BUCK4_FB F11 — BUCK4_FB — R770A 0 5% 1/20W MF 0201 — BUCK4_FB_R — XW7700 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1 (PLACE_NEAR=U7700.F11:5MM)
BUCK4_VSS_FB F12 — VSS_ANA_SPMU (28 30 31)

BUCK5_LX_0 H13 BUCK5_LX_1 H14 — BUCK5_LX0 (31) DIDT=TRUE SWITCH_NODE=TRUE — L7750 0.47UH-20%-4A-0.027OHM 2012 CRITICAL
BUCK5_FB H11 — BUCK5_FB — R770B 0 5% 1/20W MF 0201 — BUCK5_FB_R — XW7701 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1 (PLACE_NEAR=U7700.H12:5MM)
BUCK5_VSS_FB H12 — VSS_ANA_SPMU (28 30 31)

BUCK6_LX_0 M3 BUCK6_LX_1 N3 BUCK6_LX_2 P3 — BUCK6_LX0 (31) DIDT=TRUE SWITCH_NODE=TRUE — L7760 0.47UH-20%-6.9A-0.022OHM PIUA2520IB-SM CRITICAL
BUCK6_FB L3 — BUCK6_FB — R770C 0 5% 1/20W MF 0201 — BUCK6_FB_R — XW7760 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1 (PLACE_NEAR=U7700.L3:5MM)
BUCK6_VSS_FB K2 — VSS_ANA_SPMU (28 30 31)
BUCK6_VOUT_0 M1 BUCK6_VOUT_1 N1 BUCK6_VOUT_2 P1 — PP2V5_AWAKE_NAND (28 78)

BUCK10_LX_0 B13 BUCK10_LX_1 B14 — BUCK10_LX0 (31) DIDT=TRUE SWITCH_NODE=TRUE — L77A0 0.47UH-20%-4A-0.027OHM 2012 CRITICAL
BUCK10_FB B11 — BUCK10_FB — R770D 0 5% 1/20W MF 0201 — BUCK10_FB_R — XW77A0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1 (PLACE_NEAR=U7700.B11:5MM)
BUCK10_VSS_FB B12 — VSS_ANA_SPMU (28 30 31)

BUCK12_LX_0 N5 BUCK12_LX_1 P5 — BUCK12_LX0 (31) DIDT=TRUE SWITCH_NODE=TRUE — L77C0 0.47UH-20%-4A-0.027OHM 2012 CRITICAL
BUCK12_FB L5 — BUCK12_FB — R770E 0 5% 1/20W MF 0201 — BUCK12_FB_R — XW77C0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1 (PLACE_NEAR=U7700.L5:5MM)
BUCK12_VSS_FB M5 — VSS_ANA_SPMU (28 30 31)

BUCK13_LX_0 K13 BUCK13_LX_1 K14 — BUCK13_LX0 (31) DIDT=TRUE SWITCH_NODE=TRUE — L77D0 0.47UH-20%-4A-0.027OHM 2012 CRITICAL
BUCK13_FB K11 — BUCK13_FB — R770F 0 5% 1/20W MF 0201 — BUCK13_FB_R — XW77D0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1 (PLACE_NEAR=U7700.K11:5MM)
BUCK13_VSS_FB K12 — VSS_ANA_SPMU (28 30 31)

PP1V06_S2SW_DRAM (78)
C7740 15UF 20% 2V X6S 0402 CRITICAL
C7741 15UF 20% 2V X6S 0402 CRITICAL
C7742 15UF 20% 2V X6S 0402 CRITICAL
C7743 15UF 20% 2V X6S 0402 CRITICAL
C7744 15UF 20% 2V X6S 0402 CRITICAL (PLACE_NEAR=L7740.2:5MM)
C7745 15UF 20% 2V X6S 0402 CRITICAL
C7746 15UF 20% 2V X6S 0402 CRITICAL
C7747 15UF 20% 2V X6S 0402 CRITICAL
C7713 15UF 20% 2V X6S 0402 CRITICAL
C7712 15UF 20% 2V X6S 0402 CRITICAL
C7711 15UF 20% 2V X6S 0402 CRITICAL
C7710 15UF 20% 2V X6S 0402 CRITICAL
C777M 12PF 5% 25V NP0-C0G 0201
C777N 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=L7741.2:5MM)

PP0V764_S1_SRAM (78)
C7750 15UF 20% 2V X6S 0402 CRITICAL
C7751 15UF 20% 2V X6S 0402 CRITICAL
C7752 15UF 20% 2V X6S 0402 CRITICAL
C7753 15UF 20% 2V X6S 0402 CRITICAL
C7754 15UF 20% 2V X6S 0402 CRITICAL
C7755 15UF 20% 2V X6S 0402 CRITICAL
C7756 15UF 20% 2V X6S 0402 CRITICAL
C7757 15UF 20% 2V X6S 0402 CRITICAL
C778M 12PF 5% 25V NP0-C0G 0201
C778N 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=L7750.2:5MM)

PP2V5_AWAKE_NAND (28 78)
C7760 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7761 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7762 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7763 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7764 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7765 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C776C 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C776D 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7766 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7767 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7768 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C7769 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C776A 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C776B 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C776E 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C776F 10UF 20% 6.3V CER-X6S 0402 CRITICAL
C779M 12PF 5% 25V NP0-C0G 0201 (PLACE_NEAR=L7760.2:5MM)
C779N 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=L7760.2:5MM)

PP0V6_S1_VDDQL (78)
C77A0 15UF 20% 2V X6S 0402 CRITICAL
C77A1 15UF 20% 2V X6S 0402 CRITICAL
C77A2 15UF 20% 2V X6S 0402 CRITICAL
C77A3 15UF 20% 2V X6S 0402 CRITICAL
C7723 15UF 20% 2V X6S 0402 CRITICAL
C7722 15UF 20% 2V X6S 0402 CRITICAL
C7790 12PF 5% 25V NP0-C0G 0201
C7791 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=L77A0.2:5MM)

PP0V88_S1 (78)
C77C0 15UF 20% 2V X6S 0402 CRITICAL
C77C1 15UF 20% 2V X6S 0402 NOSTUFF
C77C2 15UF 20% 2V X6S 0402 CRITICAL
C77C3 15UF 20% 2V X6S 0402 NOSTUFF
C7719 15UF 20% 2V X6S 0402 CRITICAL
C7718 15UF 20% 2V X6S 0402 CRITICAL
C7721 15UF 20% 2V X6S 0402 CRITICAL
C7720 15UF 20% 2V X6S 0402 CRITICAL
C7792 12PF 5% 25V NP0-C0G 0201
C7793 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=L77C0.2:5MM)

PP1V25_S2 (78)
C77D6 15UF 20% 2V X6S 0402 CRITICAL
C77D3 15UF 20% 2V X6S 0402 CRITICAL
C77D4 15UF 20% 2V X6S 0402 CRITICAL
C77D5 15UF 20% 2V X6S 0402 CRITICAL
C77D7 15UF 20% 2V X6S 0402 CRITICAL
C77D8 15UF 20% 2V X6S 0402 CRITICAL
C7794 12PF 5% 25V NP0-C0G 0201
C7795 3PF +/-0.1PF 25V C0G 0201 (PLACE_NEAR=L77D0.2:5MM)

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_pmu_sera_simetra SYNC_DATE=04/28/2020

PAGE TITLE: PMU: SLAVE INPUT PWR & BUCKS

Apple Inc.

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SLAVE PMU LDO

LDO INPUTS

LDO OUTPUTS

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LDO INPUTS

FROM BUCK13 POWER ALIAS => OR OPTION BUCK14	78 PP1V25_S2	M7	VDD_LDO4
FROM BUCK13 POWER ALIAS => OR OPTION BUCK14	35 29 PPVDD_PMU_LDO_PREREG	C4	VDD_LDO8
FROM BUCK4 POWER ALIAS =>	78 PP1V06_S2SW_DRAM	N7	VDD_LDO11
FROM BUCK12 POWER ALIAS =>	78 29 PP0V88_S1	P7	VDD_LDO12
	79 29 28 PP3V8_AON_VDDMAIN	A1	VDD_LDO15
		A2	VDD_LDO15
FROM BUCK13 POWER ALIAS => OR OPTION BUCK14	35 29 PPVDD_PMU_LDO_PREREG	B4	VDD_LDO20
FROM BUCK3 POWER ALIAS =>	78 PP1V8_S2	M11	VDD_SW4
FROM BUCK13 POWER ALIAS =>	78 30 PP1V25_S2	M13	VDD_SW5
		N13	VDD_SW5
		P13	VDD_SW5
		N11	VDD_SW6
		P11	VDD_SW6
		N9	VDD_SW7
FROM BUCK12 POWER ALIAS =>	78 29 PP0V88_S1	P9	VDD_SW7
	79 29 26 PP3V8_AON_VDDMAIN	J2	VDD_MAIN_BSTLQ
THIS IS AN OUTPUT(1.5V) =>		E1	VLDOINT

SWITCHED RAILS

LDO OUTPUTS

VLDO4	M8	PP0V72_S2_VDD_LOW	29 78
VLDO6	D1	NC_SPMU_VLDO6	31
VLDO8	C3	PP1V2_AWAKE_PLL	29 78
VLDO9	E3	CAP_PPSPMU_VLDO9	29 31
VLDO11	N8	PP0V855_S2SW_CIO	29 78
VLDO12	P8	PP0V805_S1_VDD_FIXED	29 78
VLDO15	A3	NC_SPMU_VLDO15	31
VLDO17	B1	NC_SPMU_VLDO17	31
VLDO18	C1	NC_SPMU_VLDO18	31
VLDO20	B3	PP1V2_S2_CIO	29 78
		PP1V8_AWAKE_SPMU_GPIO	
BUCK_SW4	M12	VOLTAGE=1.8V	
BUCK_SW5	M14	PP1V25_AWAKE_NAND	29 78
BUCK_SW5	N14		
BUCK_SW5	P14		
BUCK_SW6	N12	PP0V88_AWAKE_NAND	29 78
BUCK_SW6	P12		
BUCK_SW7	N10		
BUCK_SW7	P10		
BSTLQ_LX	G1 31	SPMU_BSTLQ_LX	
BSTLQ_FB	J1 28	PP5V_BSTLQ_SPMU	
BSTLQ_VOUT	H1	VOLTAGE=5V	
VCP_OUT_SPARE	M9	NO_TEST=1 NC_SPMU_VCP_OUT_SPARE	
VMBX_SPARE	F10	NC_SPMU_VMBX_SPARE NO_TEST=1	

<<==BUCK4_SW USED FOR SPMU GPIO, INTERNALLY CONNECTED

PLACE_NEAR=U7700.M12:5MM
C7822 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U7700.M12:5MM
C7898 12PF 5% 25V NP0-C0G 0201
C7899 3PF +/-0.1PF 25V C0G 0201

L7800
0.47UH-20%-1.7A-0.175OHM
PIJT1005FE-SM-COMBO
PP3V8_AON_VDDMAIN

SWITCH_NODE=TRUE DIDT=TRUE
XW78D0 SM
PP5V_BSTLQ_VOUT_SPMU VOLTAGE=5V

PLACE_NEAR=U7700.H1:5MM
C7892 12PF 5% 25V NP0-C0G 0201
PLACE_NEAR=U7700.H1:5MM
C7893 3PF +/-0.1PF 25V C0G 0201
CRITICAL C7800 20UF 20% 6.3V X5R 0402
CRITICAL C7801 20UF 20% 6.3V X5R 0402
CRITICAL C7831 0.1UF 10% 10V X6S-CERM 0201
PLACE_NEAR=U7700.H1:5MM
GND

PLACE_NEAR=U7700.J1:5MM
CRITICAL C7825 0.1UF 10% 10V X6S-CERM 0201

CRITICAL C7810 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7811 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7812 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : VDD_LDO8
PPVDD_PMU_LDO_PREREG 29 35
PLACE_NEAR=U7700.C4:5MM
CRITICAL C7813 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : VDD_LDO20
PPVDD_PMU_LDO_PREREG 29 35
PLACE_NEAR=U7700.B4:5MM
CRITICAL C7814 10UF 20% 6.3V CER-X6S 0402

28 PP1V5_VLDOINT_SPMU VOLTAGE=1.5V
C7807 220PF 10% 10V CER-X7R 0201
C7808 220PF 10% 10V CER-X7R 0201
CRITICAL C7823 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7834 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : BSTLQ
PP3V8_AON_VDDMAIN 28 29 79
PLACE_NEAR=L7800.2:5MM
C7890 12PF 5% 25V NP0-C0G 0201
PLACE_NEAR=L7800.2:5MM
C7891 3PF +/-0.1PF 25V C0G 0201
CRITICAL C7815 1UF 20% 10V X6S-CERM 0201
CRITICAL C7816 1UF 20% 10V X6S-CERM 0201
PLACE_NEAR=U7700.J2:5MM
PLACE_NEAR=U7700.J2:5MM

DECOUPLING : LDO20
PLACE_NEAR=U7700.B3:5MM
PP1V2_S2_CIO 29 78
NOSTUFF CRITICAL C7804 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.B3:5MM
CRITICAL C7804A 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : LDO8
PLACE_NEAR=U7700.C3:5MM
PP1V2_AWAKE_PLL 29 78
CRITICAL C7805 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.C3:5MM
CRITICAL C7806 10UF 20% 6.3V CER-X6S 0402

DECOUPLING : LDO12
PLACE_NEAR=U7700.P8:5MM
PP0V805_S1_VDD_FIXED 29 78
CRITICAL C7821 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.N8:5MM
CRITICAL C7806B 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.P8:5MM

DECOUPLING : LDO11
PP0V855_S2SW_CIO 29 78
CRITICAL C7809 10UF 20% 6.3V CER-X6S 0402
NOSTUFF C780C 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.N8:5MM

DECOUPLING : SW6/7
PLACE_NEAR=U7700.N12:5MM
CRITICAL C7830 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7829 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.N12:5MM
CRITICAL C7828 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.N12:5MM
C7894 12PF 5% 25V NP0-C0G 0201
PP0V88_AWAKE_NAND 29 78
C7895 3PF +/-0.1PF 25V C0G 0201
PLACE_NEAR=U7700.N12:5MM
PLACE_NEAR=U7700.N12:5MM

DECOUPLING : LDO9
PLACE_NEAR=U7700.E3:5MM
CAP_PPSPMU_VLDO9 29 31
CRITICAL C7824 1UF 20% 10V X6S-CERM 0201
CRITICAL C7835 1UF 20% 10V X6S-CERM 0201
PLACE_NEAR=U7700.E3:5MM

DECOUPLING : LDO4
PP0V72_S2_VDD_LOW 29 78
CRITICAL C7820 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.M8:5MM
CRITICAL C780D 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.M8:5MM

DECOUPLING : SW5
PLACE_NEAR=U7700.M14:5MM
PP1V25_AWAKE_NAND 29 78
CRITICAL C7802 10UF 20% 6.3V CER-X6S 0402
CRITICAL C7803 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=U7700.M14:5MM
C7896 12PF 5% 25V NP0-C0G 0201
C7897 3PF +/-0.1PF 25V C0G 0201
PLACE_NEAR=U7700.M14:5MM
PLACE_NEAR=U7700.M14:5MM

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=rf_pbu_sara_simctrs
SYNC_DATE=04/29/2020

PAGE TITLE
PMU: SLAVE LDO

Apple Inc.

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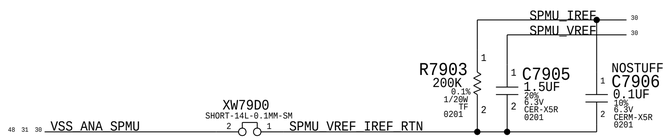
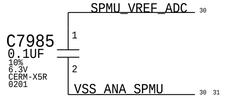
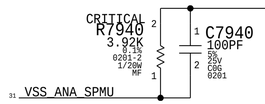
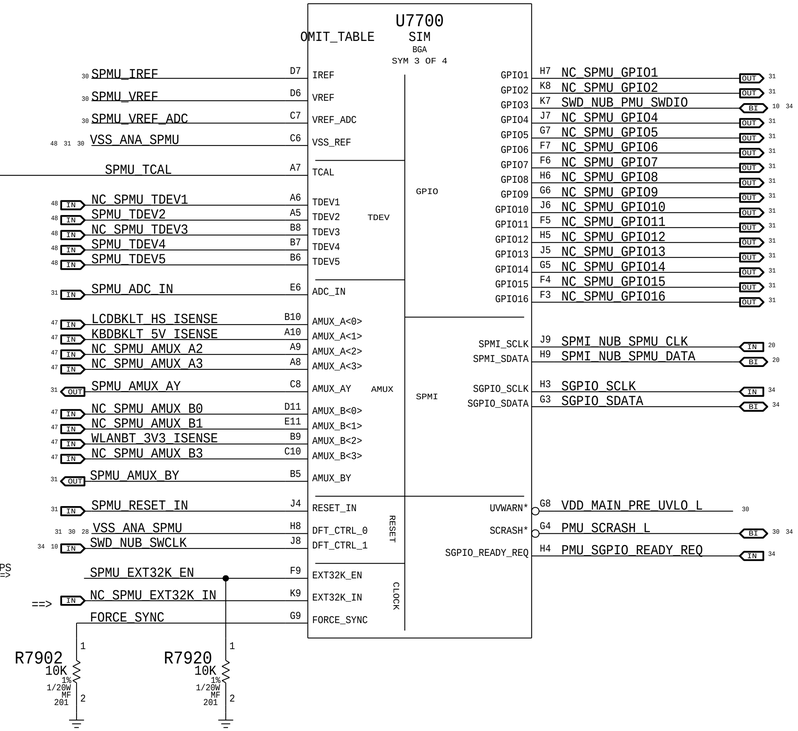
SLAVE PMU GND,ADC,& GPIO



PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN BACK FROM THE VREF / IREF PASSIVES





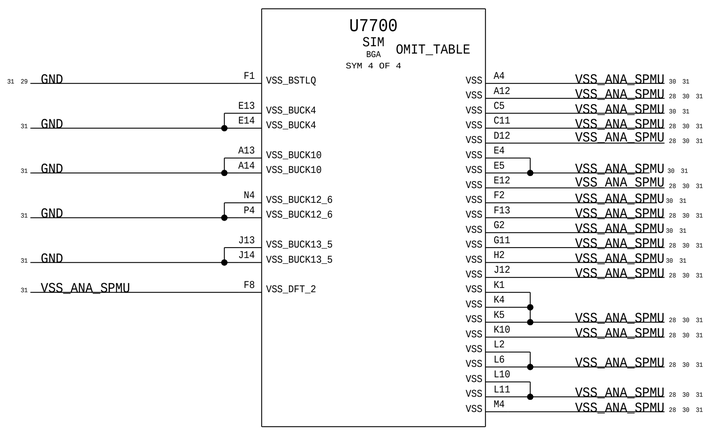


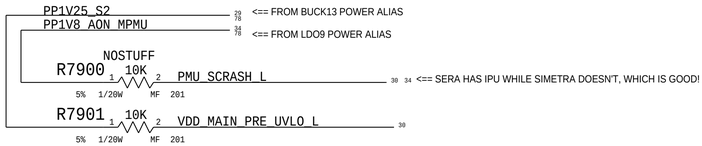
RECOMMENDED TO HAVE PD ON UNUSED RESET_IN PIN

DFT_CTRL0=0 ==> DFT_CTRL1=SWDCLK

CAN DIRECTLY SHORT TO GND BUT PD HELPS IF NEED TO OVERRIDE BY NOSTUFFING IT ==>

CAN LEAVE IT FLOATING AS OTP DISABLES IT AND HAS IPD, PAD KEEPS PD ON DEV TO BE ABLE TO OVERRIDE IT





BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=svf_pmu_sera_simetra SYNC_DATE=04/29/2020

PAGE TITLE

PMU: SLAVE GPIO & GND

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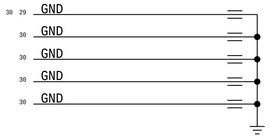

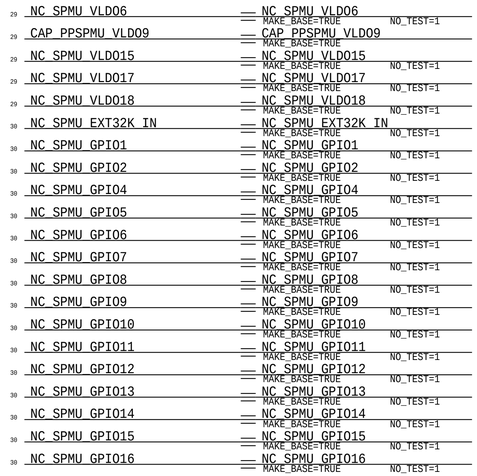

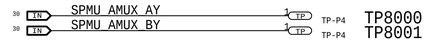

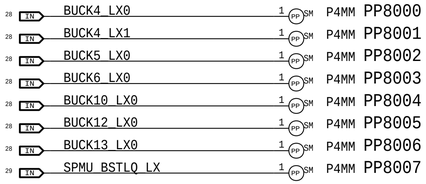

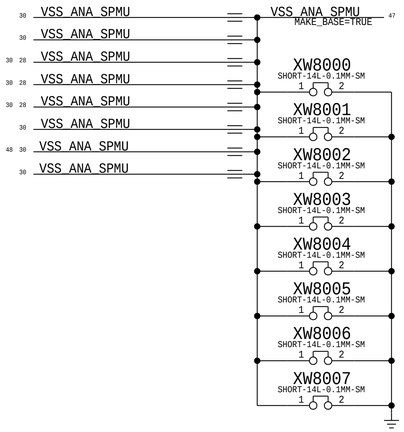

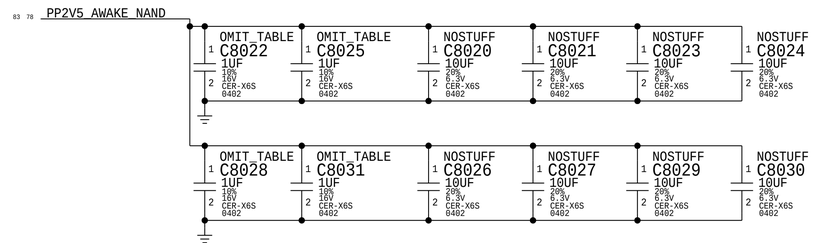

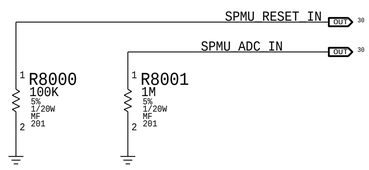

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138s00336	5	CAP,CER,1UF,10%,16V,X6S,MUR,0402	C5151,C8022,C8025,C8028,C8031		

BOM_COST_GROUP=PLATFORM POWER

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PMU: Slave extra

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MASTER PMU BUCKS

PP3V8_AON_VDDMAIN

FROM BUCK13 POWER ALIAS =>
OPTION BUCK14

FED BY SPMU BUCK13 (1.2V)POWER ALIAS=>
FED BY MPMU BUCK3 (1.8V)POWER ALIAS=>

COINCELL BATTERY =>

OMIT_TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_3S	<== FOR 3S BATTERY
103S00480	1	RES,MF,453KOHM,0.1,1/20W,0201	R8101	CRITICAL	PBUS_3S	
103S00481	1	RES,MF,910KOHM,0.1,1/20W,0201	R8100	CRITICAL	PBUS_12VDCIN	<== FOR 12V DCIN
103S00043	1	RES,MF,280KOHM,0.1,1/20W,0201	R8101	CRITICAL	PBUS_12VDCIN	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_15P8VDCIN	<== FOR 15.8V DCIN
103S00086	1	RES,MF,205KOHM,0.1%,1/20W,0201	R8101	CRITICAL	PBUS_15P8VDCIN	

NO_XNET_CONNECTION=1

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	PMU: MASTER INPUT PWR & BUCKS
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MASTER PMU BUCKS & GND

U8100
SER
BGA
SYM 6 OF 6
OMIT_TABLE

U8100
SER
BGA
SYM 2 OF 6
OMIT_TABLE

UNUSED ADC_IN PIN NEED 1M PD

MPMU_ADC_IN — K9 ADC_IN
PP1V5_VLDOINT_MPMU — C7 VDD_ANA
PLACE_NEAR=U8100.C15:5MM
C8206 0.1UF 10% 10V X6S-CERM 0201

C11 C15 F5 F18 J15 K5 K8 L5 P18 R5 V7 V11 V15 V19 VDD_ANA

D9 E16 J7 M18 P9 R17 VDD_DIG

MPMU_VREF — K12 VREF
MPMU_VBAT — J10 VBAT
MPMU_IBAT — J9 IBAT
MPMU_IREF — J8 IREF

UNUSED VBAT/IBAT PINS NEED 1M PD

VSS_BUCK0: N1 N2 N3 N4 U1 U2 U3 U4 W5 Y1 Y2 Y3 Y4 Y5 — GND
VSS_BUCK1: A1 A2 A3 A4 A5 B5 D1 D2 D3 D4 H1 H2 H3 H4 — GND
VSS_BUCK2: W17 W21 W22 Y17 Y21 Y22 — GND
VSS_BUCK3: A17 B17 — GND
VSS_BUCK7: W13 Y13 — GND
VSS_BUCK8: A9 B9 — GND
VSS_BUCK9_14: A13 B13 — GND
VSS_BUCK11: W9 Y9 — GND
VSS_BSTLQ: V22 — GND
VSS_WLED_LP: A21 A22 B21 B22
VSS_WLED_HP1: A20 B20 C20
VSS_WLED_HP2: D21 D22
VSS_REF: J11 — VSS_ANA_MPMU
VSS_DFT_2: K7 — VSS_ANA_MPMU

VSS_ANA_MPMU: A18 B8 B18 C5 C6 C9 C10 C13 C17 D5 D7 D10 D11 D15 D18 D19 D20 E5 E7 E15 E17 E20 F6 F16 F17 F21 F22 G5 G6 G15 G18 H5 H6 H15 H18 J5 J6 J13 J17 J18 K15 K18 L6 L7 L8 L9 L10 L11 L12 L15 M5 N5 N18 N22 P5 P7 R18 T5 T18 U5 U19 V5 V6 V9 V10 V13 V14 V16 V18 V21 W8 W12 W20

BUCK OUTPUTS

BUCK3_LX — A16 BUCK3_LX0 — DIDT=TRUE, SWITCH_NODE=TRUE
BUCK3_LX — B16
CRITICAL L8230 0.47UH-20%-4A-0.027OHM 2012
PP1V8_S2 — C8230 C8231 C8232 C8233 C8234 C8235 C82D0 12PF C82D1 3PF
C8230–C8235: 10UF 20% 6.3V CER-X6S 0402
PLACE_NEAR=L8230.1:5MM
C8236 C8237 C8238 C8239 C823A C823B: 10UF 20% 6.3V CER-X6S 0402

BUCK3_FB — D16 BUCK3_FB
R820A 0 5% 1/20W MF 0201
PLACE_NEAR=U8100.D16:5MM
BUCK3_FB_R — XW8230 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK3_VSS_FB — C16 VSS_ANA_MPMU

BUCK7_LX0 — Y12 BUCK7_LX0 — DIDT=TRUE, SWITCH_NODE=TRUE
BUCK7_LX1 — W14 BUCK7_LX1 — DIDT=TRUE, SWITCH_NODE=TRUE
BUCK7_LX1 — Y14
L8270 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
L8271 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
CRITICAL
PPVDD_CPU_SRAM_AWAKE — C8270 C8271 C8272 C8273 C8274 C8275 C8276 C8277
C8270–C8277: 15UF 20% 2V X6S 0402 (C8270, C8271 NOSTUFF)
PLACE_NEAR=L8270.1:5MM
PLACE_NEAR=L8271.1:5MM
C82D2 12PF 5% 25V NP0-C0G 0201
C82D3 3PF +/-0.1PF 25V C0G 0201

BUCK7_FB — U12 BUCK7_FB
R820B 0 5% 1/20W MF 0201
PLACE_NEAR=U8100.U12:5MM
BUCK7_FB_R — XW8270 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK7_VSS_FB — V12 VSS_ANA_MPMU

BUCK8_LX0 — A8 BUCK8_LX0 — DIDT=TRUE, SWITCH_NODE=TRUE
L8280 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
BUCK8_LX1 — A10 BUCK8_LX1 — DIDT=TRUE, SWITCH_NODE=TRUE
BUCK8_LX1 — B10
L8281 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
PPVDD_DISP_S1 — C8280 C8281 C8282 C8283 C8284 C8285 C82D4 12PF C82D5 3PF
C8280–C8285: 15UF 20% 2V X6S 0402
PLACE_NEAR=L8280.1:5MM
PLACE_NEAR=L8281.1:5MM

BUCK8_FB — D8
R820C 0 5% 1/20W MF 0201
PLACE_NEAR=U8100.D8:5MM
BUCK8_FB_R — XW8280 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK8_VSS_FB — C8 VSS_ANA_MPMU

BUCK9_LX — A12 BUCK9_LX0 — DIDT=TRUE, SWITCH_NODE=TRUE
BUCK9_LX — B12
L8290 CRITICAL 0.47UH-20%-4A-0.027OHM 2012
PPVDD_DCS_S1 — C8290 C8291 C8292 C8293 C8294 C82D6 12PF C82D7 3PF
C8290–C8294: 15UF 20% 2V X6S 0402
PLACE_NEAR=L8290.1:5MM
PLACE_NEAR=L8290.1:5MM

BUCK9_FB — D12
R820D 0 5% 1/20W MF 0201
PLACE_NEAR=U8100.D12:5MM
BUCK9_FB_R — XW8290 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK9_VSS_FB — C12 VSS_ANA_MPMU

BUCK11_LX0 — Y8 BUCK11_LX0 — DIDT=TRUE, SWITCH_NODE=TRUE
L82B0 CRITICAL 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO
BUCK11_LX1 — W10 BUCK11_LX1 — DIDT=TRUE, SWITCH_NODE=TRUE
BUCK11_LX1 — Y10
L82B1 CRITICAL 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM
PPVDD_ECPU_AWAKE — C82B6 C82B7 C82B8 C82B9 C82B1 C82B2 C82B3 C82B4
C82B6–C82B9: 15UF 20% 2V X6S 0402
C82B1–C82B4: 15UF 20% 2V X6S 0402 (NOSTUFF)
PLACE_NEAR=L82B0.1:5MM
PLACE_NEAR=L82B1.1:5MM
C82D8 12PF 5% 25V NP0-C0G 0201
C82D9 3PF +/-0.1PF 25V C0G 0201

BUCK11_FB — U8 BUCK11_FB
R820E 0 5% 1/20W MF 0201
PLACE_NEAR=U8100.U8:5MM
BUCK11_FB_R — XW82B0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1
BUCK11_VSS_FB — V8 VSS_ANA_MPMU

BUCK14_LX — A14 BUCK14_LX0
BUCK14_LX — B14
VIN FROM BUCK13 IS POR FOR LDO4,20,8. IF PDN (VMIN VIOLATION, WHEN LDO8 IN DROPOUT MODE) IS AN ISSUE THEN BUCK14 WILL BE THE BACKUP OPTION. THIS WOULD THEN REQUIRE ADDING BEAD AND CAPS

BUCK14_FB — D14 BUCK14_FB
BUCK14_VSS_FB — C14 VSS_ANA_MPMU

SWITCHED RAILS

PP1V8_S2 — FROM BUCVK3 POWER ALIAS => — R21 T20 R19 R20 VDD_SW1 VDD_SW1 VDD_SW2 VDD_SW3 VDD_SW3
PP1V25_S2 — FROM BUCK13 POWER ALIAS =>

BUCK_SW1 — P21 PP1V8_AWAKE
BUCK_SW1 — P22
BUCK_SW2 — T19 NC_MPMU_BUCK_SW2 — NO_TEST=1
BUCK_SW3 — P19
BUCK_SW3 — P20 PP1V25_AWAKE_IO

DECOUPLING : VDD_SW3
PP1V25_S2 — PLACE_NEAR=U8100.R19:5MM
CRITICAL C8201 10UF 20% 6.3V CER-X6S 0402

MPMU_VREF
MPMU_IREF
C8204 1.5UF 20% 6.3V CER-X5R 0201
R8201 200K 0.1% 1/20W TF 0201
NOSTUFF C8205 0.1UF 10% 6.3V CERM-X5R 0201
XW82B2 SHORT-14L-0.1MM-SM
VSS_ANA_MPMU — MPMU_VREF_IREF_RTN

CRITICAL C8240 15UF 20% 2V X6S 0402
CRITICAL C8241 15UF 20% 2V X6S 0402
PP1V25_AWAKE_IO

CRITICAL C8202 10UF 20% 6.3V CER-X6S 0402
CRITICAL C8203 10UF 20% 6.3V CER-X6S 0402
PP1V8_AWAKE

PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN BACK FROM THE VREF / IREF PASSIVES

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PMU: MASTER BUCKS & GND

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
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MASTER PMU LDO,ADC, & GPIO

U8100 SER BGA SYM 5 OF 6 (OMIT_TABLE)

NO_TEST=1	NC_MPMU_IDAC_OUT<0>	G17	IDAC_OUT<0>
NO_TEST=1	NC_MPMU_IDAC_OUT<1>	G16	IDAC_OUT<1>
NO_TEST=1	NC_MPMU_IDAC_OUT<2>	G14	IDAC_OUT<2>
NO_TEST=1	NC_MPMU_IDAC_OUT<3>	G13	IDAC_OUT<3>
NO_TEST=1	NC_MPMU_IDAC_OUT<4>	H17	IDAC_OUT<4>
NO_TEST=1	NC_MPMU_IDAC_OUT<5>	H16	IDAC_OUT<5>
NO_TEST=1	NC_MPMU_IDAC_OUT<6>	H14	IDAC_OUT<6>
NO_TEST=1	NC_MPMU_IDAC_OUT<7>	H13	IDAC_OUT<7>
NO_TEST=1	NC_MPMU_IDAC_OUT<8>	J16	IDAC_OUT<8>
NO_TEST=1	NC_MPMU_IDAC_OUT<9>	J14	IDAC_OUT<9>
NO_TEST=1	NC_MPMU_IDAC_OUT<10>	K17	IDAC_OUT<10>
NO_TEST=1	NC_MPMU_IDAC_OUT<11>	K16	IDAC_OUT<11>
NO_TEST=1	NC_MPMU_IDAC_OUT<12>	K14	IDAC_OUT<12>
NO_TEST=1	NC_MPMU_IDAC_OUT<13>	K13	IDAC_OUT<13>
NO_TEST=1	NC_MPMU_IDAC_OUT<14>	L17	IDAC_OUT<14>
NO_TEST=1	NC_MPMU_IDAC_OUT<15>	L16	IDAC_OUT<15>
NO_TEST=1	NC_MPMU_IDAC_OUT<16>	L14	IDAC_OUT<16>
NO_TEST=1	NC_MPMU_IDAC_OUT<17>	L13	IDAC_OUT<17>

WLED_LP_LX	NC_MPMU_WLED_LP_LX_0	C21	NO_TEST=1
WLED_LP_LX	NC_MPMU_WLED_LP_LX_1	C22	NO_TEST=1
WLED_HP1_LX	NC_MPMU_WLED_HP1_LX_0	A19	NO_TEST=1
WLED_HP1_LX	NC_MPMU_WLED_HP1_LX_1	B19	NO_TEST=1
WLED_HP1_LX	NC_MPMU_WLED_HP1_LX_2	C19	NO_TEST=1
WLED_HP2_LX	NC_MPMU_WLED_HP2_LX_0	E21	NO_TEST=1
WLED_HP2_LX	NC_MPMU_WLED_HP2_LX_1	E22	NO_TEST=1
WLED_VOUT_FB	NC_MPMU_WLED_VOUT_FB	E18	NO_TEST=1
VCP_OUT_SPARE	NC_MPMU_VCP_OUT_SPARE	U21	NO_TEST=1
VMBX_SPARE	NC_MPMU_VMBX_SPARE	J12	NO_TEST=1

CRITICAL
L8300
0.47UH-20%-1.7A-0.175OHM
PIJT1005FE-SM-COMBO

PP3V8_AON_VDDMAIN — PLACE_NEAR=L8300.1:5MM
MPMU_BSTLQ_LX — SWITCH_NODE=TRUE — DIDT=TRUE — U22
BSTLQ_LX
BSTLQ_VOUT — T22
VOLTAGE=5V — PP5V_BSTLQ_VOUT_MPMU
VDD_BOOST — H9
VDD_SNS_SPARE — H10
PP3V8_AON_VDDMAIN — XW83D0 SM
PP5V_BSTLQ_MPMU
VDD_HI_INT1 — T21
VDD_HI_INT2 — H11
VDD_HI_INT3 — D13
VDD_HI_INT4 — D17
VDD_HI_INT5 — H12
VDD_HI_INT6 — L18

C83A0 12PF 5% 25V NP0-C0G 0201
C83A1 3PF +/-0.1PF 25V C0G 0201
C83A2 12PF 5% 25V NP0-C0G 0201
C83A3 3PF +/-0.1PF 25V C0G 0201
C8300 20UF 20% 6.3V X5R 0402
C8301 20UF 20% 6.3V X5R 0402
C8302 0.1UF 10% 10V X6S-CERM 0201
C8310 0.1UF 10% 10V X6S-CERM 0201
C8311 0.1UF 10% 10V X6S-CERM 0201
C8316 0.1UF 10% 10V X6S-CERM 0201
C8317 0.1UF 10% 10V X6S-CERM 0201

PLACE_NEAR=L8300.1:5MM
PLACE_NEAR=U8100.T21:5MM
PLACE_NEAR=U8100.L18:5MM
PLACE_NEAR=U8100.T22:5MM
PLACE_NEAR=U8100.D17:5MM
PLACE_NEAR=U8100.H12:5MM
GND

U8100 SER BGA SYM 3 OF 6 (OMIT_TABLE)

VDD_BOOST_LDO		G19	VLDO1
VDD_BOOST_LDO		G21	VLDO2
VDD_BOOST_LDO		H19	VLDO3
VDD_BOOST_LDO		H21	VLDO5
VDD_BOOST_LDO		J21	VLDO7
VDD_MAIN_LDO		M20	VLDO9
	NC_MPMU_VLDO1	J22	VLDO1
	NC_MPMU_VLDO2	K20	VLDO2
NO_TEST=1			
	PP1V2_S2	L21	VLDO3
	NC_MPMU_VLDO5	K22	VLDO5
	PP3V3_S2_UPC	H22	VLDO7
	PP1V8_AON_MPMU	M19	VLDO9
	NC_MPMU_VLDO10	G20	VLDO10
	NC_MPMU_VLDO13	H20	VLDO13
	NC_MPMU_VLDO14	L19	VLDO14
	NC_MPMU_VLDO16	G22	VLDO16
NO_TEST=1	NC_MPMU_VLDO19	J20	VLDO19
	MPMU_VREF_ADC	H7	VREF_ADC

LDO OUTPUTS

PP3V8_AON_VDDMAIN
C8314 10UF 20% 6.3V CER-X6S 0402
C8315 10UF 20% 6.3V CER-X6S 0402
C8321 0.1UF 10% 6.3V CERM-X5R 0201
VSS_ANA_MPMU

LDO1 NOT USED ==> INT PD ENABLED
NC_MPMU_LDO1_EN — LDO1_EN — N17
THIS IS AN OUTPUT ==> PP1V5_VLDOINT_MPMU — VOLTAGE=1.5V — VLDOINT — M21
THIS IS AN OUTPUT ==> PP1V5_VLDOINT_MPMU — VLDORTC — N21
PACK_OPTION=PORTABLE
MAKE_BASE=TRUE

C8326 1.0UF 20% 6.3V X5R 0201-1
C8327 1.0UF 20% 6.3V X5R 0201-1
C8328 1.0UF 20% 6.3V X5R 0201-1
C8329 1.0UF 20% 6.3V X5R 0201-1
PACK_IGNORE=TRUE PACK_OPTION=DESKTOP
PACK_IGNORE=TRUE PACK_OPTION=DESKTOP
PACK_IGNORE=TRUE PACK_OPTION=DESKTOP
PACK_IGNORE=TRUE PACK_OPTION=DESKTOP

PORTABLE= NO CAPS NEEDED
DESKTOP =4X1UF

PP1V2_S2
C8307 10UF 20% 6.3V CER-X6S 0402
C830A 10UF 20% 6.3V CER-X6S 0402
C8309 10UF 20% 6.3V CER-X6S 0402

PP1V5_VLDOINT_MPMU — PLACE_NEAR=U8100.M21:5MM
C8322 10UF 20% 6.3V CER-X6S 0402
C830D 10UF 20% 6.3V CER-X6S 0402
C830G 220PF 10% 16V CER-X7R 0201
C830H 220PF 10% 16V CER-X7R 0201
PLACE_NEAR=U8100.M21:5MM
PLACE_NEAR=U8100.M21:5MM

PP1V8_AON_MPMU
C8304 1UF 20% 10V X6S-CERM 0201
C830C 1UF 20% 10V X6S-CERM 0201

PP3V3_S2_UPC
C8303 10UF 20% 6.3V CER-X6S 0402
C830E 10UF 20% 6.3V CER-X6S 0402

INTEGRATOR ALIAS TO:
1V8 OCARINA=Y
1V2 OCARINA=N

PP1V25_S2
R8343 10K 5% 1/20W MF 201
PMU_SYS_ALIVE
NOSTUFF

PP1V8_AON_MPMU <== LDO9 POWER ALIAS
R8324 10K 5% 1/20W MF 201 — PMU_ONOFF_L
R8325 100K 5% 1/20W MF 201 — PMU_RSLOC_RST_L
R8338 100K 5% 1/20W MF 201 — NOSTUFF — MPMU_FAULT_OUT_L
R8339 10K 5% 1/20W MF 201 — NOSTUFF — PMU_CRASH_L
OTP HAS IPU

U8100 SER BGA SYM 4 OF 6 (OMIT_TABLE)

NC_MPMU_TDEV1	TDEV1	E8	
NC_MPMU_TDEV2	TDEV2	F9	
MPMU_TDEV3	TDEV3	F8	
MPMU_TDEV4	TDEV4	F7	
MPMU_TDEV5	TDEV5	G9	
NC_MPMU_TDEV6	TDEV6	G10	
MPMU_TDEV7	TDEV7	G8	
MPMU_TDEV8	TDEV8	G7	
MPMU_TCAL	TCAL	F10	

CRITICAL R8320 3.92K 0.1% 0201-2 1/20W MF
C8320 100PF 5% 25V C0G 0201
VSS_ANA_MPMU

PMU_ONOFF_L	BUTTON1	P10	
PMU_RSLOC_RST_L	BUTTON2	M6	
NC_MPMU_BUTTON3	BUTTON3	N8	
NC_MPMU_BUTTON4	BUTTON4	P11	
SOC_WDOG	RESET_IN1	N11	
PMU_RESET_1V8	RESET_IN2	M10	
SOC_SOCHOT_L	RESET_IN3	M9	
MPMU_VBUS_DET	VBUS_DET	R7	
VSS_ANA_MPMU	BRICK_ID1	E9	
	BRICK_ID2	E10	
PMU_SHDN	SHDN	M8	

XW83D1 SHORT-14L-0.1MM-SM
PP1V8_AON_MPMU
R8322 10K 1% 1/20W MF 201 — NOSTUFF

NXTAL_MEMS=0 ==> XTAL

VSS_ANA_MPMU	NXTAL_MEMS	N19	
MPMU_XIN	XIN	L22	
MPMU_XOUT	XOUT	M22	
DCIN_VSENSE	AMUX_A<0>	E13	
DCIN_ISENSE	AMUX_A<1>	F11	
PBUS_VSENSE	AMUX_A<2>	E12	
BMON_ISENSE	AMUX_A<3>	E11	
MPMU_AMUX_AY	AMUX_AY	G12	
P3V8AON_IMEAS	AMUX_B<0>	E14	
P3V3S2_HS_ISENSE	AMUX_B<1>	F14	
P5VS2_HS_ISENSE	AMUX_B<2>	F12	
NC_MPMU_AMUX_B3	AMUX_B<3>	F13	
MPMU_AMUX_BY	AMUX_BY	G11	

NOSTUFF
R8326 100K 5% 1/20W MF 201 — WLBT_PWR_EN
R8327 100K 5% 1/20W MF 201 — NOSTUFF — SE_PWR_EN
R8328 100K 5% 1/20W MF 201 — NOSTUFF — LCD_PWR_EN
R8329 100K 5% 1/20W MF 201 — P3V3S2_PWR_EN_MPMU
R8335 100K 5% 1/20W MF 201 — SENSOR_PWR_EN
R8336 100K 5% 1/20W MF 201 — NOSTUFF — IPD_WAKE_L
117S0008

R8341 20 5% 1/20W MF 201 — SGPIO_SCLK_R — SGPIO_SCLK
R8342 20 5% 1/20W MF 201 — SGPIO_SDATA_R — SGPIO_SDATA
PLACE_NEAR=U8100.N15:5MM
PLACE_NEAR=U8100.P15:5MM

BOM_COST_GROUP=PLATFORM POWER

U8100 SER BGA SYM 4 OF 6 (OMIT_TABLE)

	GPIO01	P16	IPD_LID_OPEN_1V8
	GPIO02	T9	CHGR_AUX_OK
	GPIO03	T7	SWD_NUB_PMU_SWDIO
IPU	GPIO04	R11	CODEC_WAKE_L
	GPIO05	T8	WLBT_WAKE
	GPIO06	U7	IPD_PWR_EN
	GPIO07	T11	NC_HDMI_CEC_IRQ
	GPIO08	U10	NC_USB3_WAKE
	GPIO09	R12	NC_HDMI_RESET_L
	GPIO10	U9	LCD_PWR_EN
	GPIO11	T12	P3V3S2_PWR_EN_MPMU
TDEV	GPIO12	U11	PVDD1_PWR_EN
	GPIO13	T13	WLBT_PWR_EN
	GPIO14	U13	IPD_WAKE_L
	GPIO15	M13	SE_PWR_EN
	GPIO16	M14	SENSOR_PWR_EN
	GPIO17	N14	NAND0_LPB_L
	GPIO18	R13	BL_PWR_EN
	GPIO19	U14	P3V8AON_LPM
	GPIO20	U15	P5VS2_PWR_EN
	GPIO21	T14	NC_MPMU_NAND0_RESET_L
	GPIO22	U16	IPD_OCP_FLT
	GPIO23	U17	NC_USB3_PWR_EN
	GPIO24	R14	NC_MPMU_GPIO24
	GPIO25	N10	P2V5_NAND0_DISCHARGE_EN
	GPIO26	P8	NC_FAN_PWR_EN
	GPIO27	P17	NC_MPMU_GPIO27

	BUTTONO1	N7	NC_MPMU_BUTTONO1
BUTTONS	BUTTONO2	N9	NC_MPMU_BUTTONO2
	BUTTONO3	M7	NC_MPMU_BUTTONO3
	DBLCLICK_DET	N6	DBL_CLICK_DET
RESET	RESET*	N13	PMU_RESET_L
	FORCE_DFU	T10	SOC_FORCE_DFU
	FAULT_OUT*	M12	MPMU_FAULT_OUT_L
	SCRASH*	N12	PMU_SCRASH_L
	SGPIO_READY_REQ	M15	PMU_SGPIO_READY_REQ
SPMI	SGPIO_SCLK	N15	SGPIO_SCLK_R
	SGPIO_SDATA	P15	SGPIO_SDATA_R
	SPMI_SCLK	R15	SPMI_NUB_MPMU_CLK
	SPMI_SDATA	T15	SPMI_NUB_MPMU_DATA
CLOCKS	SLEEP_32K	U18	PMU_CLK32K_SOC_R
	OUT_32K	T16	PMU_CLK32K_WLBT_R
THROTTLE	CRASH*	P12	CRASH_L
	DFT_CTRL0	M16	VSS_ANA_MPMU
	DFT_CTRL1	M17	SWD_NUB_SWCLK
	SYS_ALIVE	M11	PMU_SYS_ALIVE
	ACTIVE_READY	P13	PMU_ACTIVE_READY
	REQUEST_DFU	R6	MPMU_REQUEST_DFU
	CPU_TRIGGER0*	P6	BUCK0_THERMAL_THROTTLE_L
	CPU_TRIGGER1*	R9	PMU_VDDHI_UVWARN_L
	GPU_TRIGGER0*	R8	BUCK1_THERMAL_THROTTLE_L
	GPU_TRIGGER1*	R10	NC_GPU_TRIGGER1_L
	UVWARN*	P14	PMU_VDDMAIN_UVWARN_L
	VDD_BOOST_UVLO*	T17	TPT_MPMU_BOOST_UVLO_L

MPMU_BOOST_UVLO IS OD. IF NEED TO PROBE OR USE IT , ADD A PU INTERNAL PULL CAN BE ENABLED AS WELL!

R8313 0 1/20W 5% MF 0201
MPMU_XTAL1_R — MPMU_XOUT
CRITICAL Y8301 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM — NOSTUFF — R8318 1M 5% 1/20W MF 201 — MPMU_XIN
C8312 18PF 5% 25V C0G-CERM 0201
C8313 18PF 5% 25V C0G-CERM 0201
VSS_ANA_MPMU
INTERNAL XTAL DRIVER CIRCUIT IS CONNECTED TO CLOSEST VSS PIN N22

PAGE TITLE	PMU: MASTER LDO & GPIO
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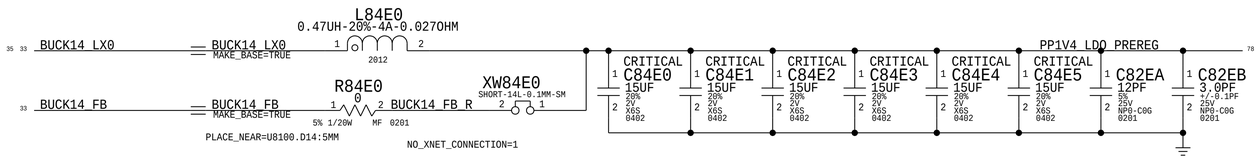
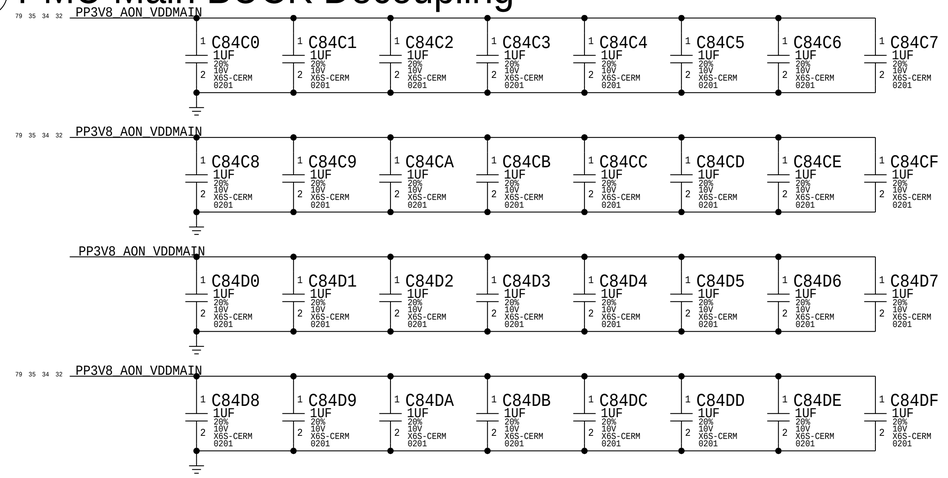
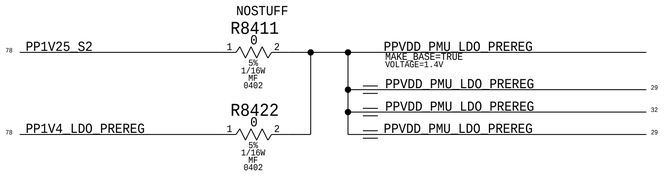
A BUCK 14 Filter



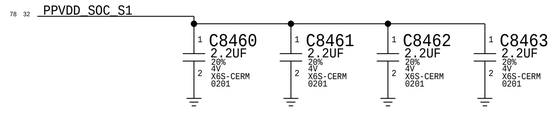
B PMU Main BUCK Decoupling



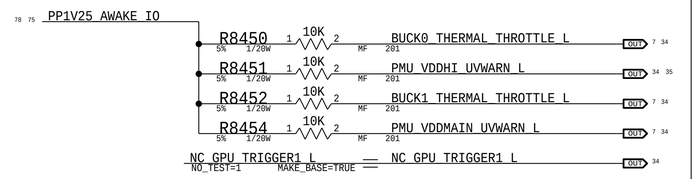
C PPVDD_PMU_LDO_PREREG Aliases



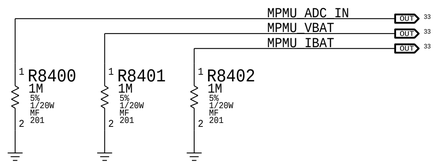
D PPVDD_SOC_S1 Decoupling



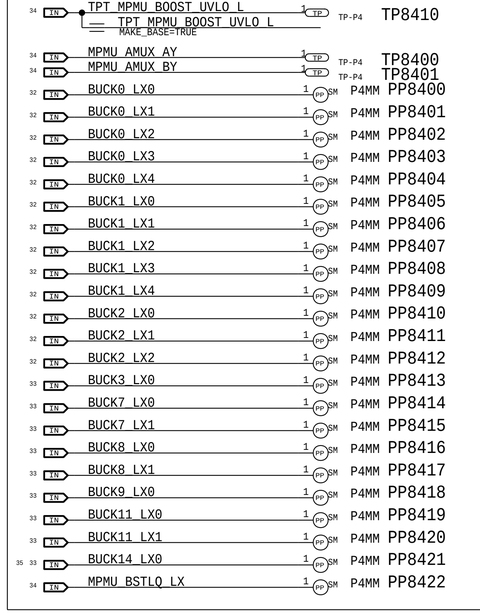
E PMU Control Flag Pull-Ups



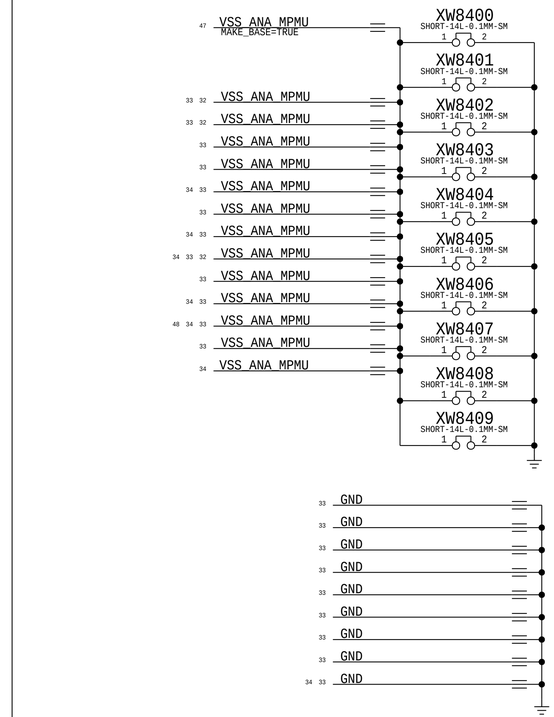
F PMU Input Protection



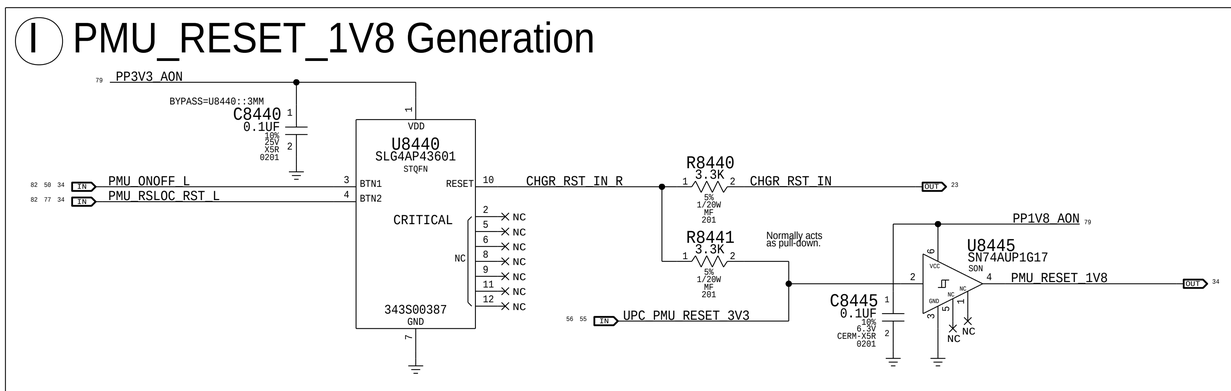
G PMU Test Points



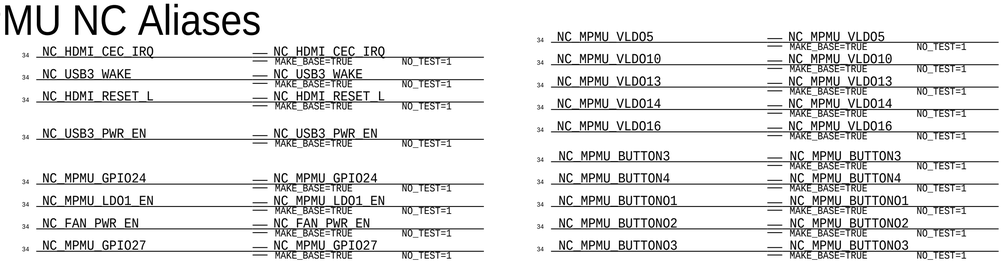
H PMU GND Aliases



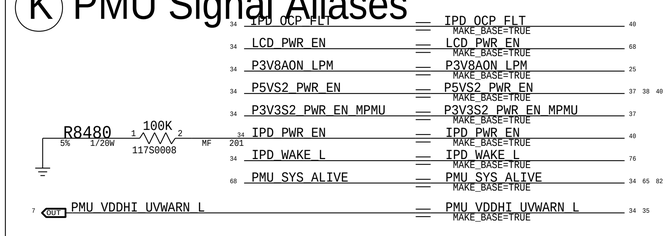
I PMU_RESET_1V8 Generation



J PMU NC Aliases



K PMU Signal Aliases



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMU: Master extra

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
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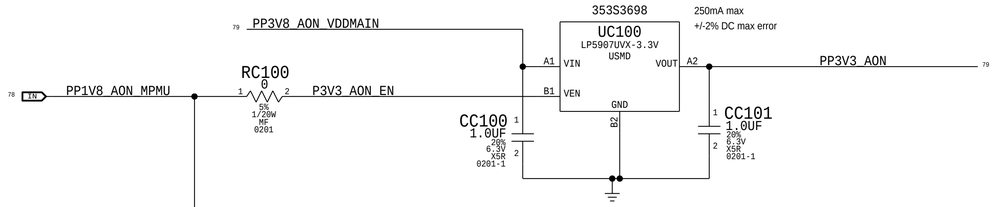
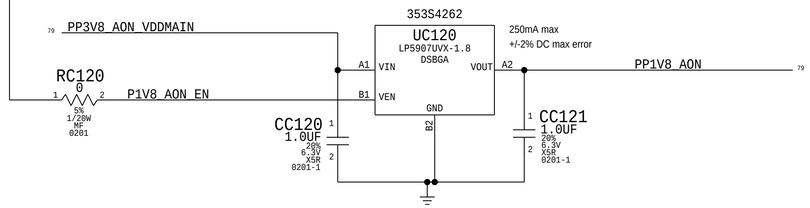
3.3V AON LDO



1.8V AON LDO



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE

Power: LDOs

Apple Inc.

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REVISION 4.0.0

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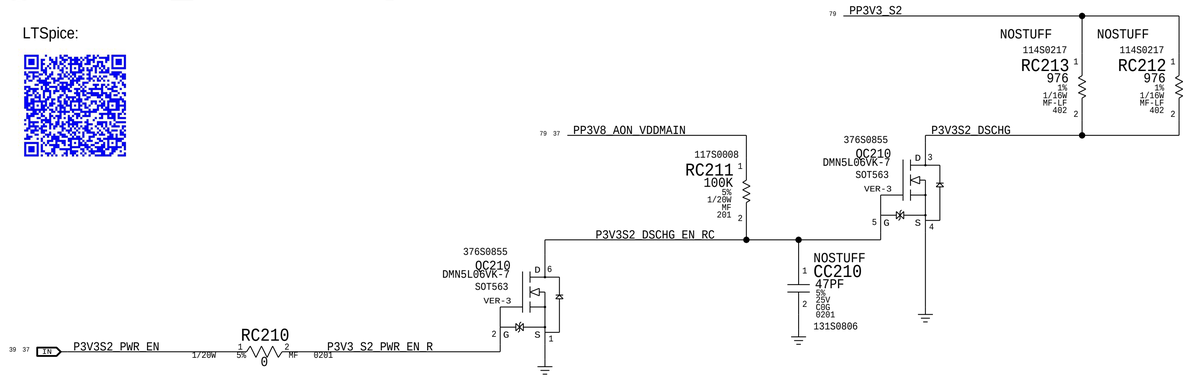
A PP3V3_S2 Discharge Circuit

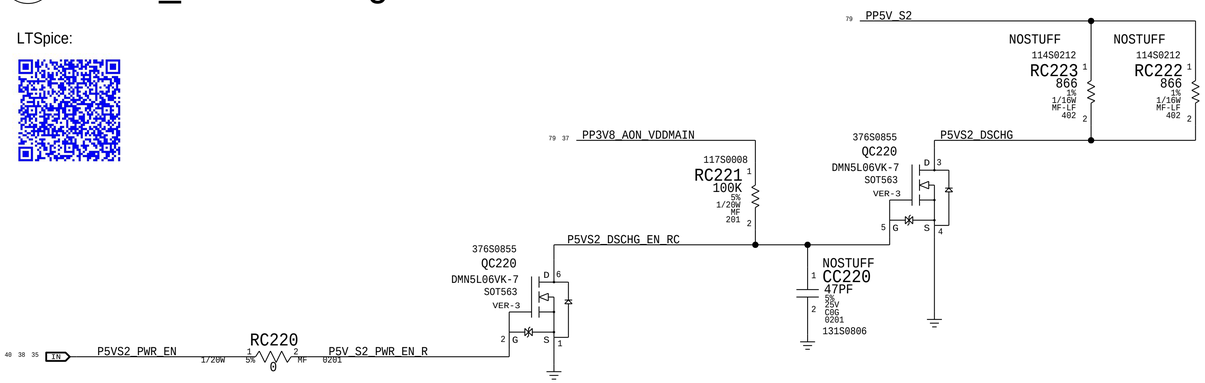
LTSpice:



$X1757GHUB/mlb/sim/ltspice/pp3v3_s2_discharge/pp3v3_s2_discharge_diodes_inc.asc

B PP5V_S2 Discharge Circuit

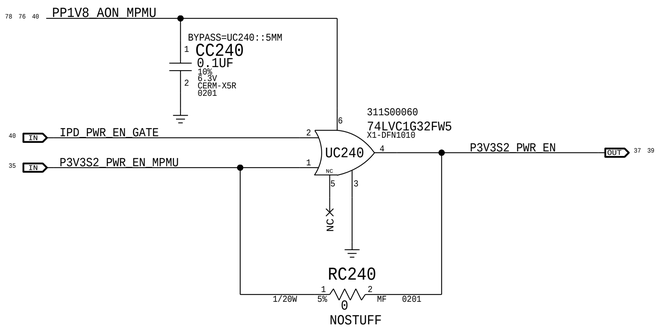
LTSpice:



$X1757GHUB/mlb/sim/ltspice/pp5v_s2_discharge/pp5v_s2_discharge_diodes_inc.asc

C P3V3S2_PWR_EN Gating Logic

Radar:



NOTE:
Per Sera PMU OTP, GPIO11 is OFF when the System is OFF.
A side-effect is that during the SIP_SMC->AWAKE transition the rail goes from ON->OFF->ON, which means we lose trackpad power during the OFF transition.

IPD_PWR_EN and PP5V_S2_EN were moved to GPIOs that Sera PMU can "hold" off.

D PP3V3_S2 Probe Points

PPC200 P4MM SM PP 1 — P3V3S2_EN — 39
PPC201 P4MM SM PP 1 — P3V3S2_PGOOD — 39
PPC202 P4MM SM PP 1 — P3V3S2_FB_LPF — 39
PPC203 P4MM SM PP 1 — P3V3S2_VOS — 39
PPC204 P4MM SM PP 1 — P3V3S2_SW — 39

E PP5V_S2 Probe Points

PPC210 P4MM SM PP 1 — P5VS2_EN — 38
PPC211 P4MM SM PP 1 — P5VS2_PGOOD — 38
PPC212 P4MM SM PP 1 — P5VS2_FB_XW — 38
PPC213 P4MM SM PP 1 — P5VS2_FB_RC — 38
PPC214 P4MM SM PP 1 — P5VS2_SW — 38 83
PPC215 P4MM SM PP 1 — GND

PAGE TITLE: POWER: 5V, 3V3 Support

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* OK2INTEGRATE *

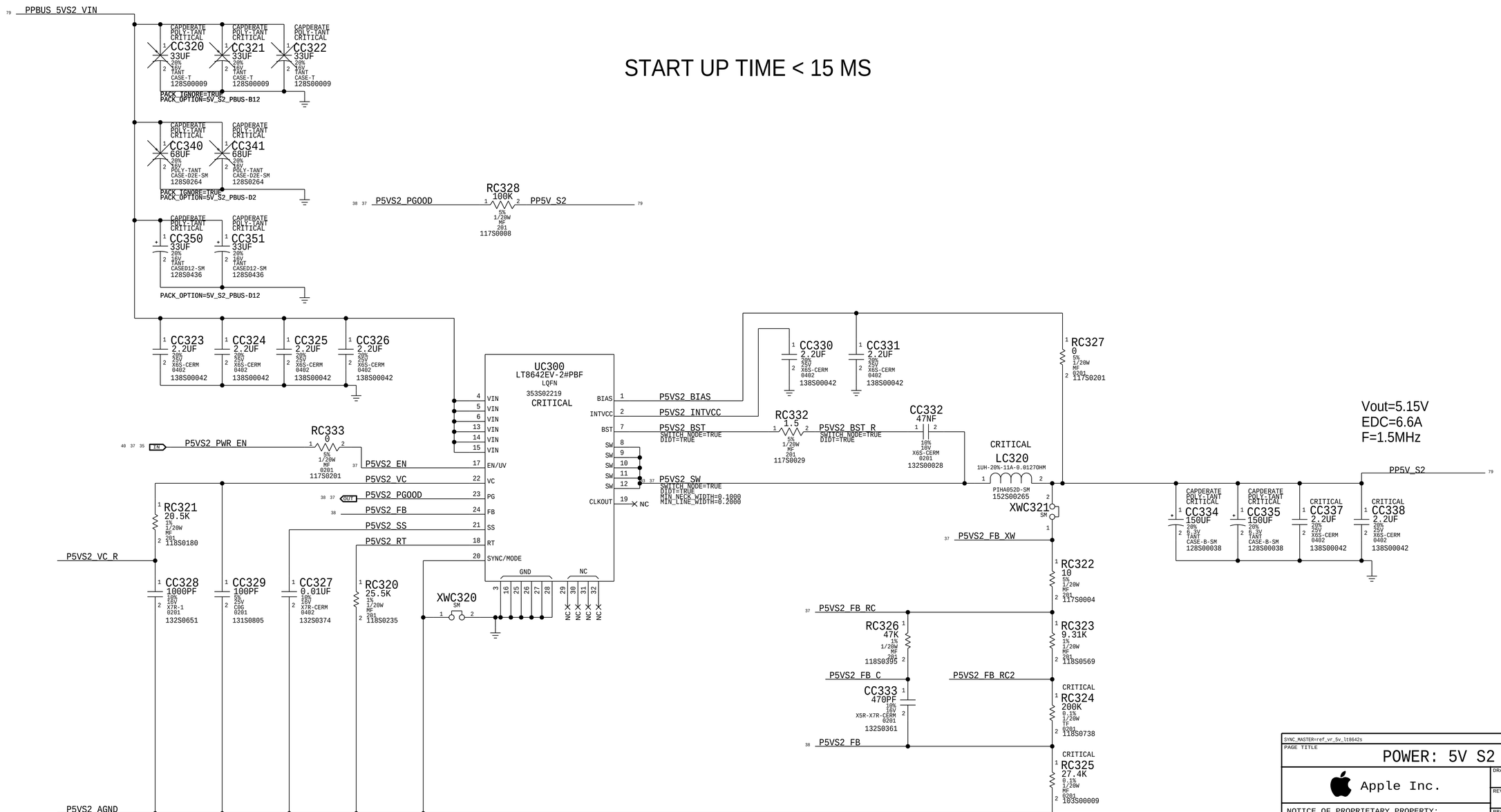
5V_S2 Voltage Regulator

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12

START UP TIME < 15 MS

Vout=5.15V
EDC=6.6A
F=1.5MHz



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_vr_5v_lt8642s
SYNC_DATE=04/20/2020

PAGE TITLE

POWER: 5V S2

Apple Inc.

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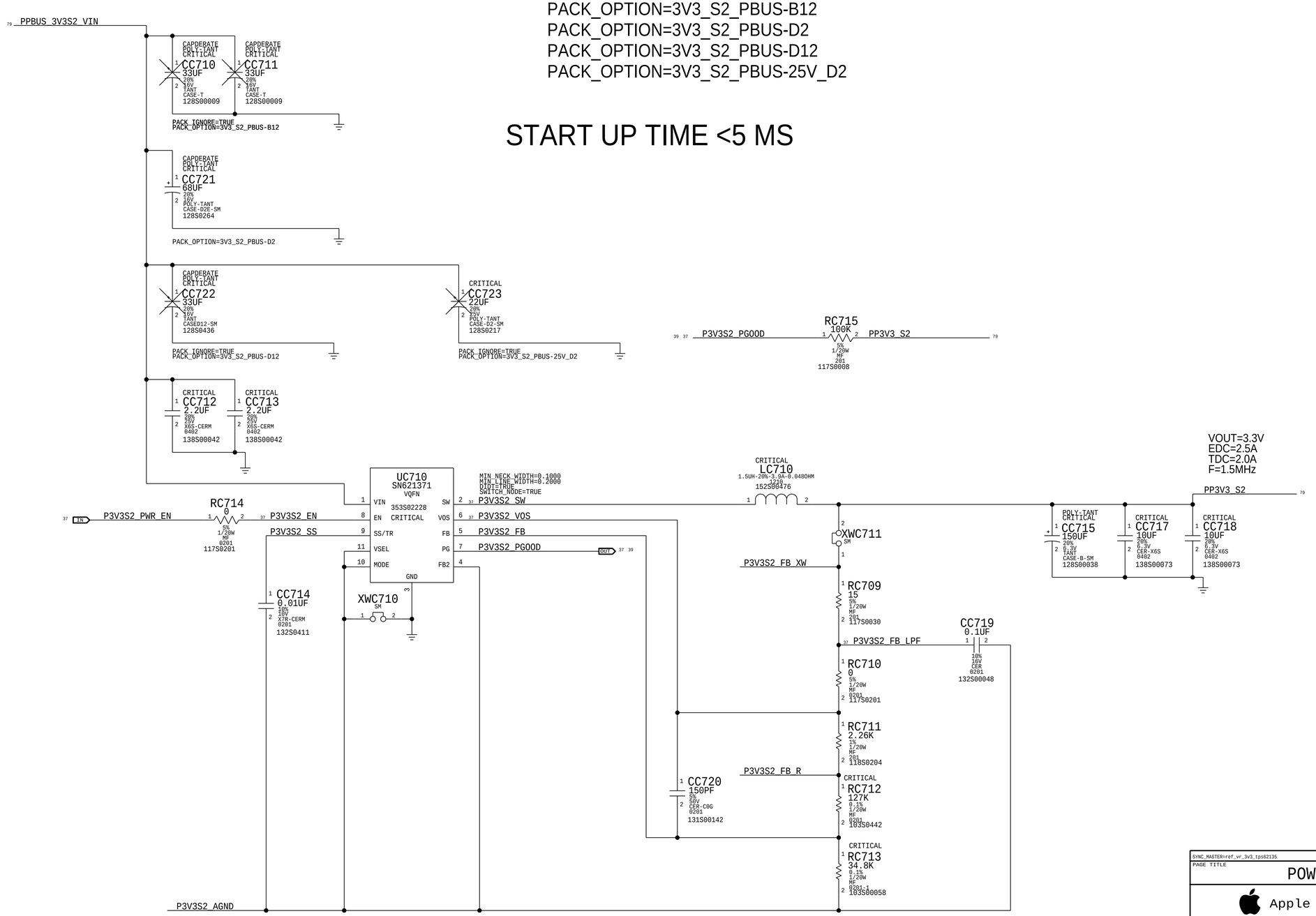
* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=3V3_S2_PBUS-B12
PACK_OPTION=3V3_S2_PBUS-D2
PACK_OPTION=3V3_S2_PBUS-D12
PACK_OPTION=3V3_S2_PBUS-25V_D2

START UP TIME <5 MS



SYNC_MASTER=ref_vr_3v3_tps62135 SYNC_DATE=01/02/2020

PAGE TITLE

POWER: 3V3 S2

Apple Inc.

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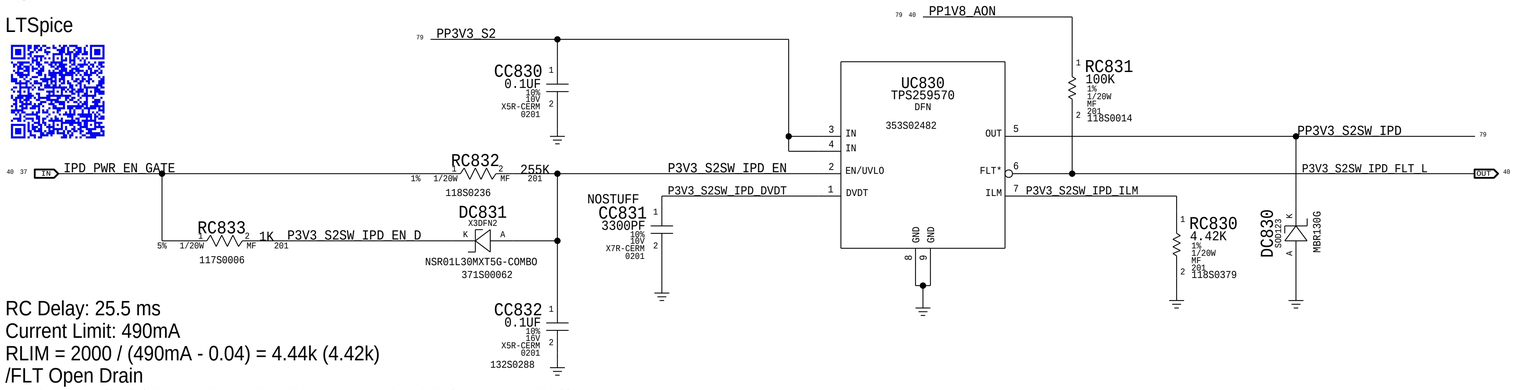
A PP3V3_S2SW_IPD Load Switch & e-Fuse

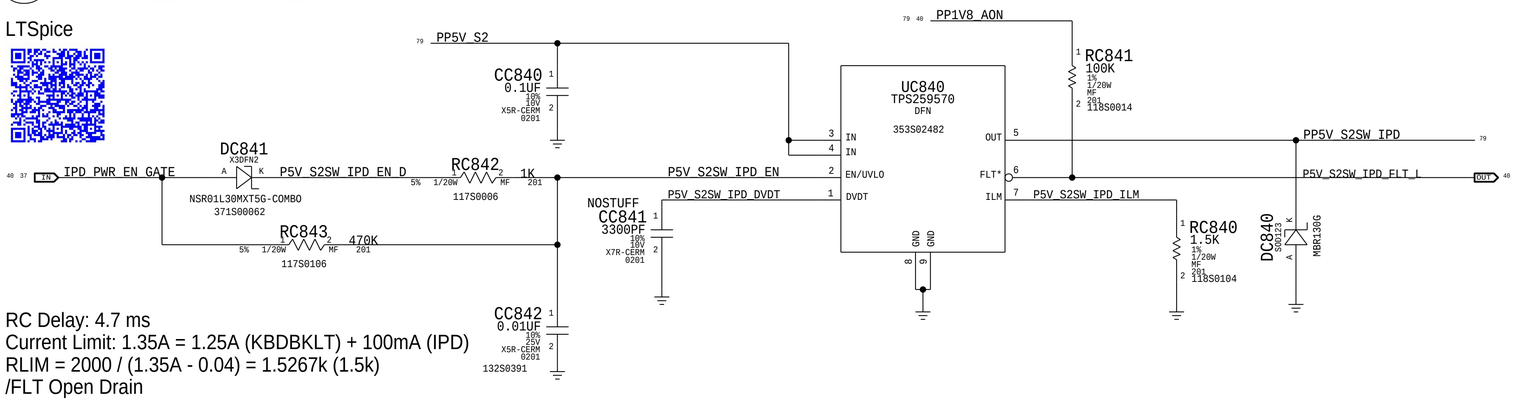
LTSpice



RC Delay: 25.5 ms
Current Limit: 490mA
RLIM = 2000 / (490mA - 0.04) = 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X1757GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

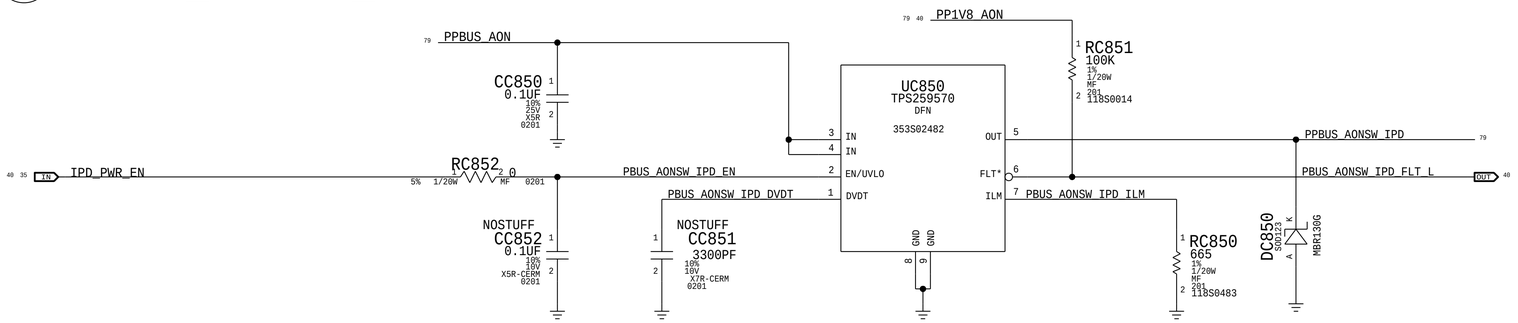
B PP5V_S2SW_IPD Load Switch & e-Fuse

LTSpice



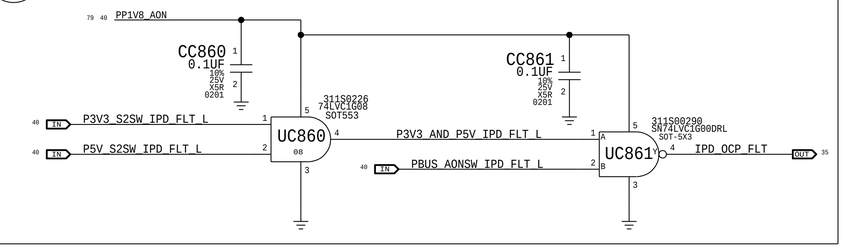
RC Delay: 4.7 ms
Current Limit: 1.35A = 1.25A (KBDBKLT) + 100mA (IPD)
RLIM = 2000 / (1.35A - 0.04) = 1.5267k (1.5k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X1757GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

C PPBUS_AONSW_IPD Load Switch & e-Fuse

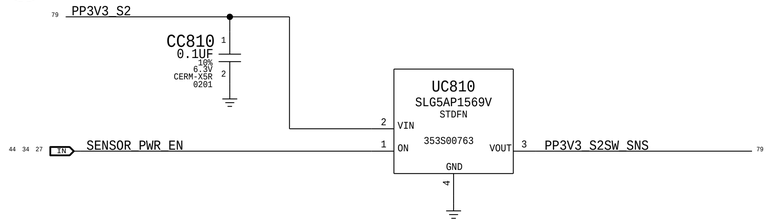


Current Limit: 3A
RLIM = 2000 / (3A - 0.04) = 676 (665)
/FLT Open Drain
Self-Controlled (EN = 3.13V to 5.93V)

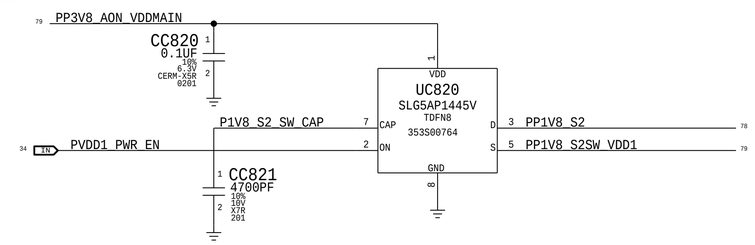
D IPD OCP Fault



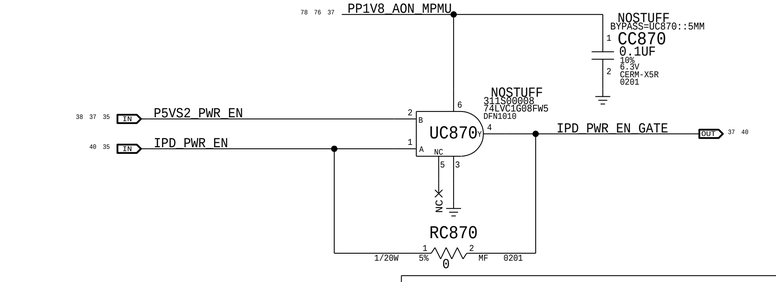
E PP3V3_S2SW_SNS Load Switch



F PP1V8_S2SW_VDD1 Load Switch



G IPD_PWR_EN Gating Logic



Radar:

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE: Power: Load Switches

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
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BRANCH: evt-1
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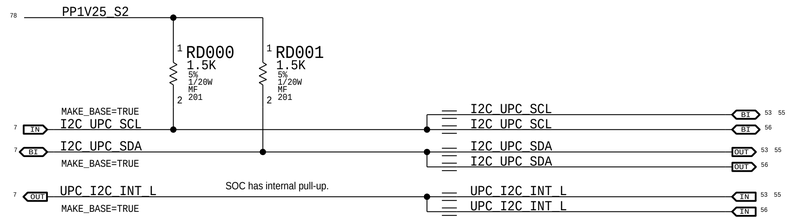
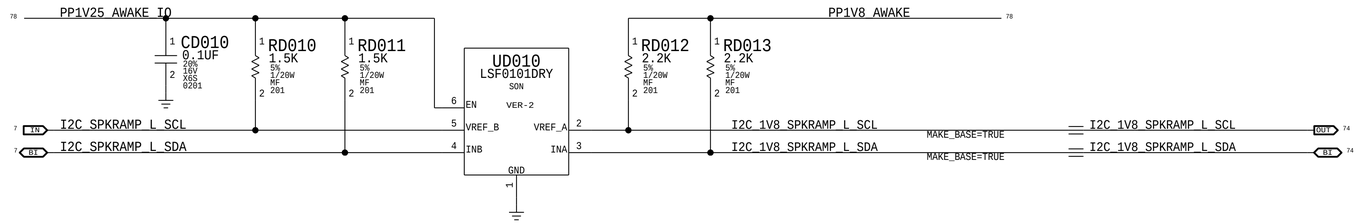
SIO I2C0

DEVICE	DEV	WR	RD
ACE 0	0x38	0x70	0x71
ACE 1	0x3F	0x7E	0x7F



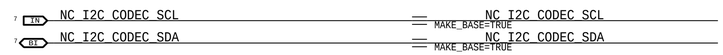
SIO I2C1

DEVICE	DEV	WR	RD
SPKR AMP L	0x31	0x62	0x63



SIO I2C2

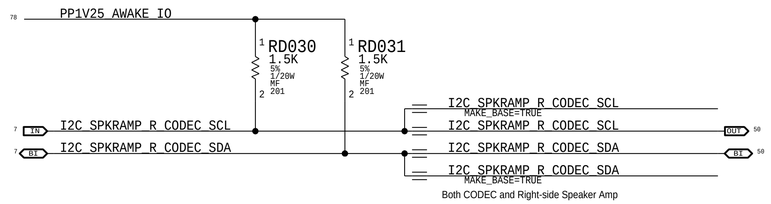
DEVICE	DEV	WR	RD



UNUSED

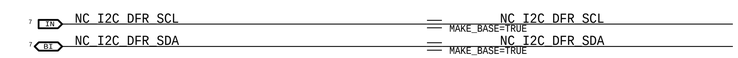
SIO I2C3

DEVICE	DEV	WR	RD
SPKR AMP R	0x34	0x68	0x69
CODEC	0x48	0x90	0x91



SIO I2C4

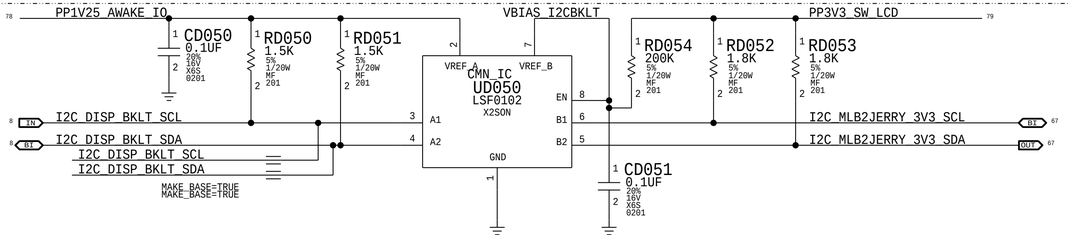
DEVICE	DEV	WR	RD



UNUSED

DISP I2C

DEVICE	DEV	WR	RD
LP8549	0x2C	0x58	0x59



BOM_COST_GROUP=SMC

SYNC_MASTER=T668 | SYNC_DATE=08/01/2019

PAGE TITLE

I2C: SIO, DISP

Apple Inc.

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ISP I2C0

DEVICE | DEV | WR | RD

UNUSED

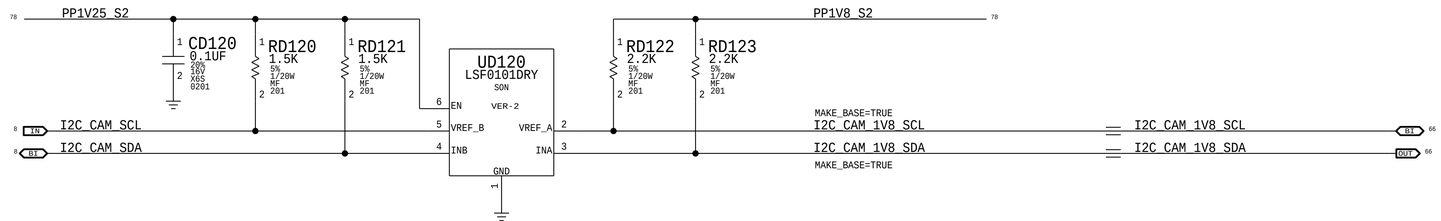
ISP I2C1

DEVICE | DEV | WR | RD

UNUSED

ISP I2C2

DEVICE	DEV	WR	RD
CAMERA	0x10	0x20	0x21
IMAGE SENSOR	0x36	0x6C	0x6D



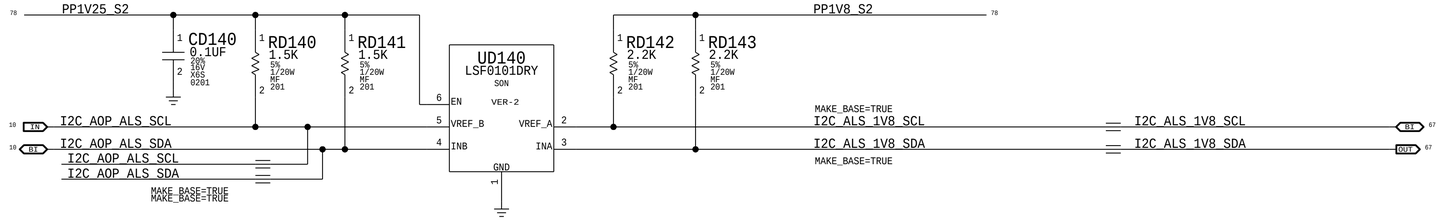
ISP I2C3

DEVICE | DEV | WR | RD

UNUSED

AOP I2C0

DEVICE	DEV	WR	RD
ALS	0x29	0x52	0x53



AOP I2C1

DEVICE | DEV | WR | RD

UNUSED

BOM_COST_GROUP=SMC

SYNC_MASTER=T668 SYNC_DATE=08/01/2019

PAGE TITLE

I2C: ISP, AOP

Apple Inc.

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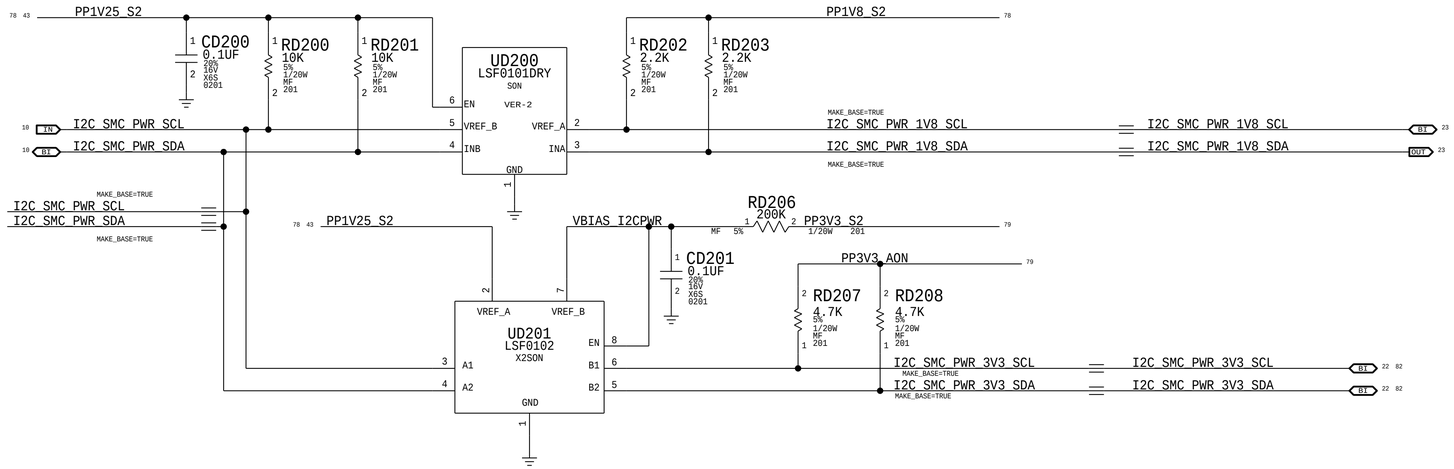
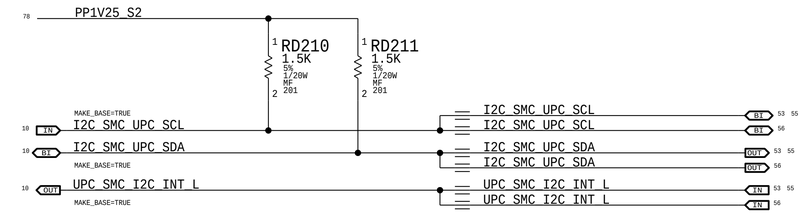
SMC I2C0

DEVICE	DEV	WR	RD
CHARGER	0x09	0x12	0x13
BMU	0x0B	0x16	0x17



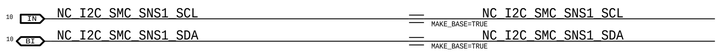
SMC I2C1

DEVICE	DEV	WR	RD
ACE 0	0x38	0x70	0x71
ACE 1	0x3F	0x7E	0x7F



SMC I2C2

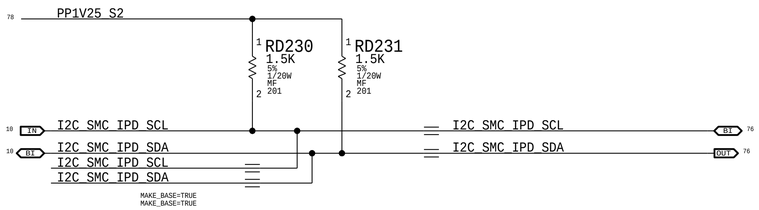
DEVICE	DEV	WR	RD
TBD	0x--	0x--	0x--



UNUSED

SMC I2C3

DEVICE	DEV	WR	RD
PALM TEMP	0x4C	0x98	0x99



SMC I2C4

DEVICE	DEV	WR	RD
TBD	0x--	0x--	0x--

UNUSED

BOM_COST_GROUP=SMC

SYNC_MASTER=T668 SYNC_DATE=08/01/2019

PAGE TITLE: I2C: SMC

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

REVISION: 4.0.0

BRANCH: evt-1

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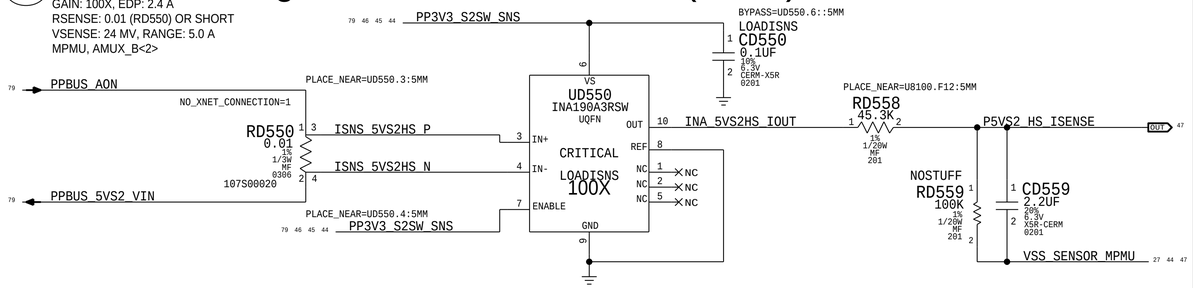
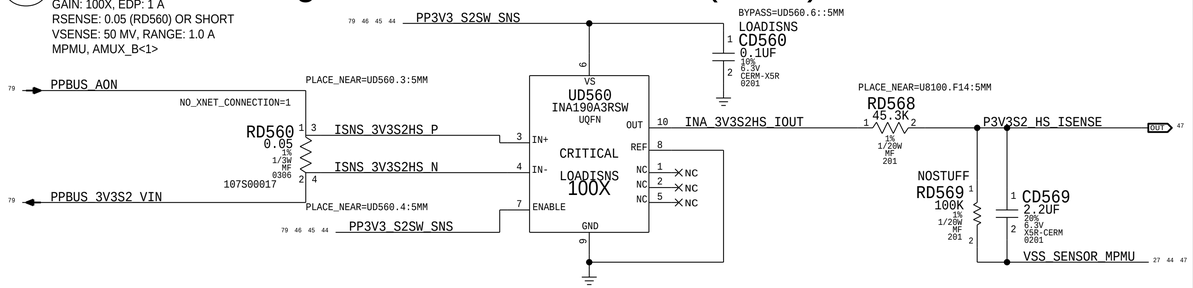
A 5V S2 VR High Side Current Sensor (IO5R)

GAIN: 100X, EDP: 2.4 A
RSENSE: 0.01 (RD550) OR SHORT
VSENSE: 24 MV, RANGE: 5.0 A
MPMU, AMUX_B<2>



B 3V3 S2 VR High Side Current Sensor (IO3R)

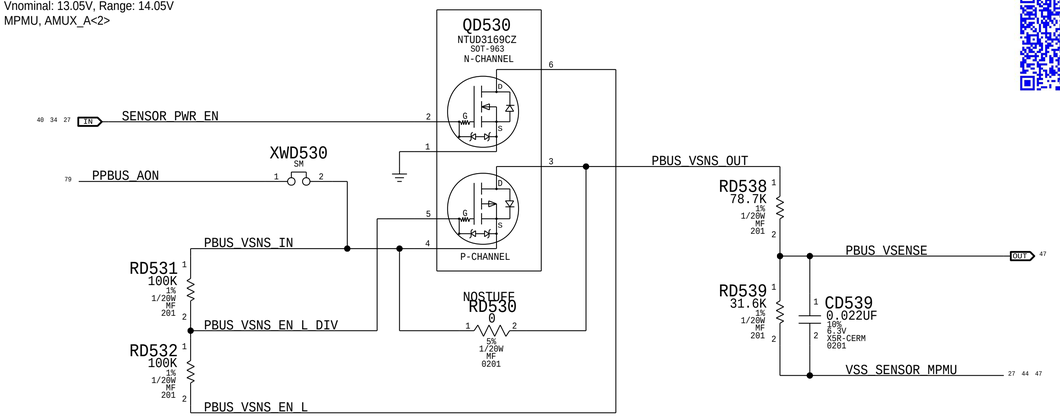
GAIN: 100X, EDP: 1 A
RSENSE: 0.05 (RD560) OR SHORT
VSENSE: 50 MV, RANGE: 1.0 A
MPMU, AMUX_B<1>



C PPBUS Voltage Sensor (VP0R)

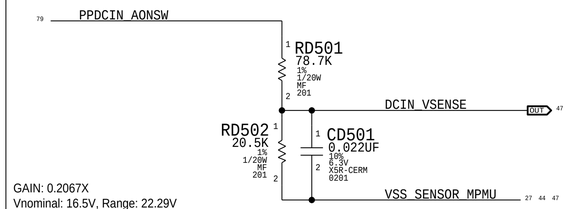
GAIN: 0.2865X
Vnominal: 13.05V, Range: 14.05V
MPMU, AMUX_A<2>

LTSpice:



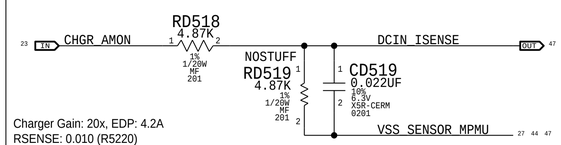
$X1757GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_diodesinc.asc
$X1757GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_onsemi.asc

D DCIN Voltage Sensor (VD0R)



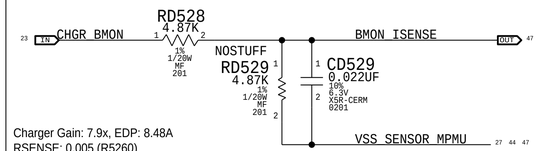
GAIN: 0.2067X
Vnominal: 16.5V, Range: 22.29V
MPMU, AMUX_A<0>

E DCIN Current Sensor (ID0R)



Charger Gain: 20x, EDP: 4.2A
RSENSE: 0.010 (R5220)
MPMU, AMUX_A<1>

F BMON Current Sensor (IPBR)



Charger Gain: 7.9x, EDP: 8.48A
RSENSE: 0.005 (R5260)
MPMU, AMUX_A<3>

BOM_COST_GROUP=SENSORS

SYNC_MASTER=1668

PAGE TITLE
SENSORS: POWER HIGH SIDE (1/2)

Apple Inc.

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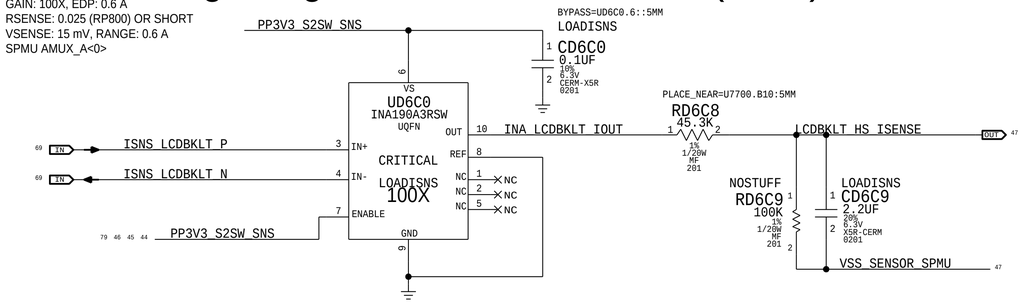
A LCD Backlight High Side Current Sensor (IBLR)

GAIN: 100X, EDP: 0.6 A
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 15 mV, RANGE: 0.6 A
SPMU AMUX_A<0>



BOM_COST_GROUP=SENSORS

SYNC_MASTER=1608

PAGE TITLE
SENSORS: POWER HIGH SIDE (2/2)

Apple Inc.

DRAWING NUMBER 051-05392
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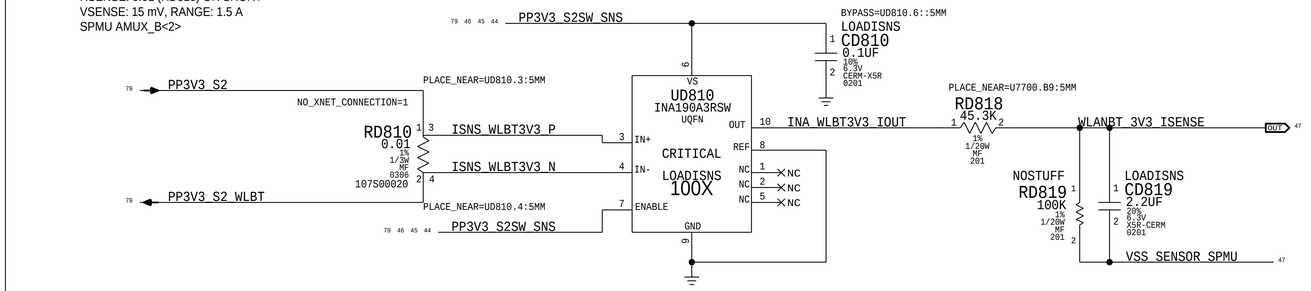
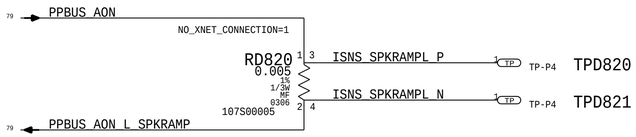
A WLAN BT 3V3 S2 Current Sensor (IW3C)

GAIN: 100X, EDP: 1.5 A
RSENSE: 0.01 (RD810) OR SHORT
VSENSE: 15 mV, RANGE: 1.5 A
SPMU AMUX_B<2>



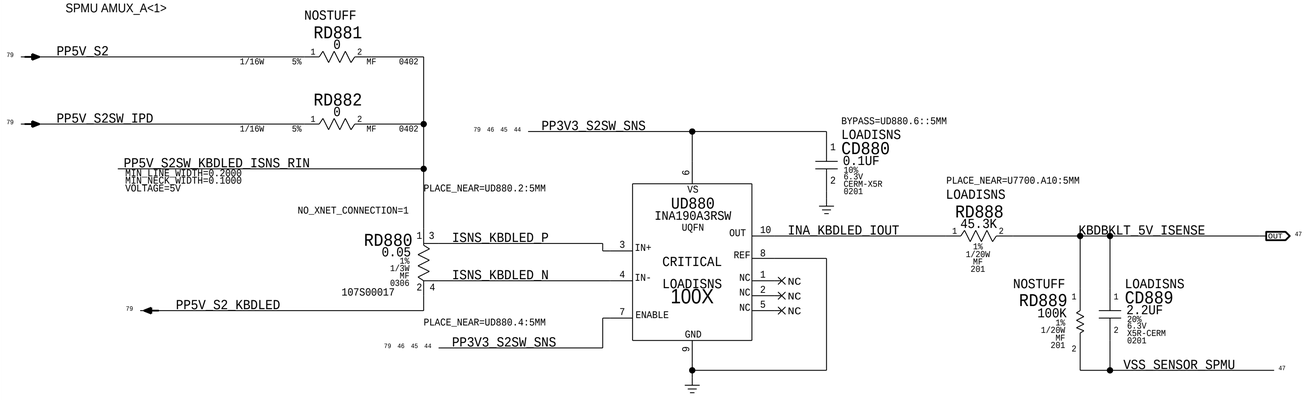
B Left Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



C Keyboard LED 5V Current Sensor (IKBC)

GAIN: 100X, EDP: 0.24 A
RSENSE: 0.05 (RD880) OR SHORT
VSENSE: 12 mV, RANGE: 0.33 A
SPMU AMUX_A<1>



BOM_COST_GROUP=SENSORS

SYNC_MASTER=t668
PAGE TITLE
SENSORS: POWER LOW SIDE (1/2)

Apple Inc.

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SIZE D
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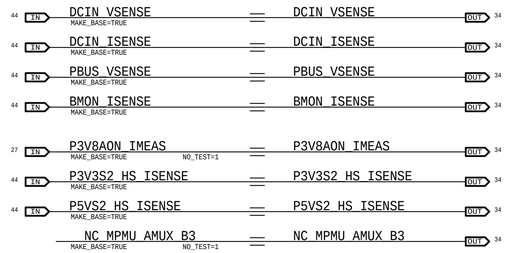
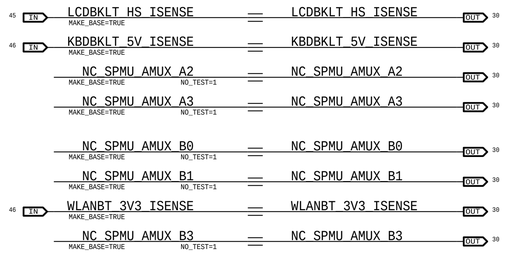
A ADC Input Aliases

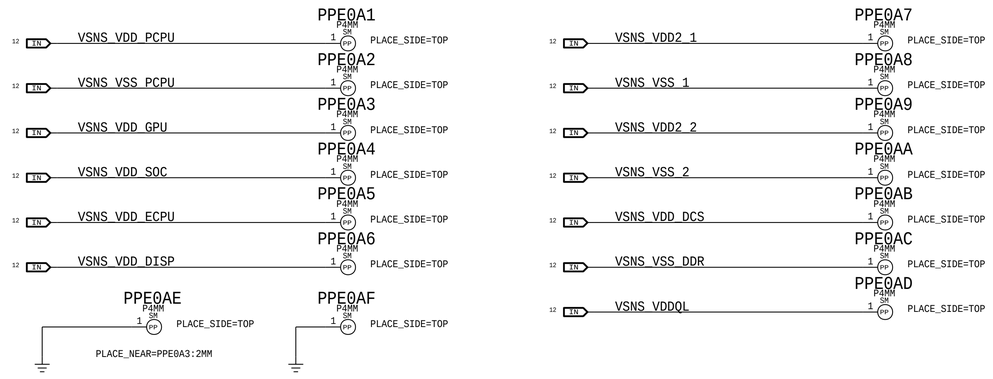
MASTER PMU AMUX ALIAS



SLAVE PMU AMUX ALIAS

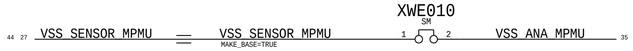


B SOC Sense Lines



C I/V Sensor Ground Reference Aliases

Master PMU ADC Ground Alias



Slave PMU ADC Ground Alias

BOM_COST_GROUP=SENSORS

PAGE TITLE	SENSORS: POWER SUPPORT
Apple Inc.	DRAWING NUMBER 051-05392 SIZE D
	REVISION 4.0.0
	BRANCH evt-1
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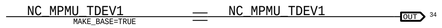
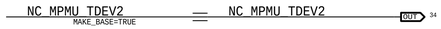
A Master PMU TDEV1 (Txxx)

Location: 3.8V AON VR



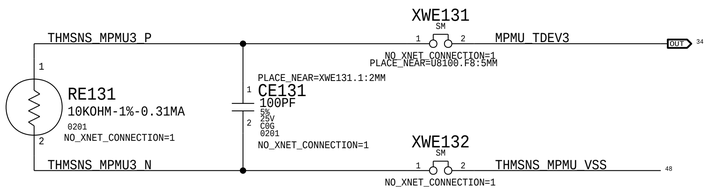
B Master PMU TDEV2 (Txxx)

Location: SoC back side ?



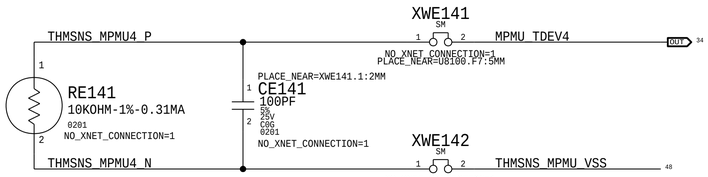
C Master PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

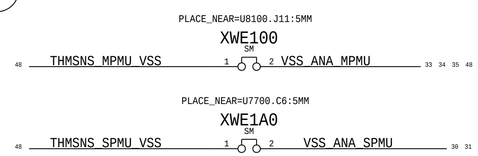


D Master PMU TDEV4 (TWOP)

Location: Wireless Proximity

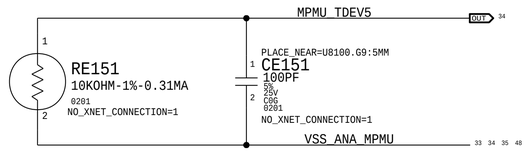


E Master/Slave PMU VSS Connection



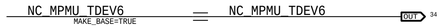
F Master PMU TDEV5 (TPMP)

Location: Master PMU Proximity



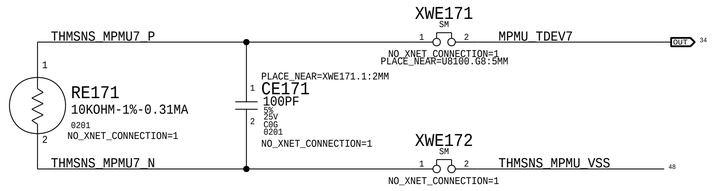
G Master PMU TDEV6 (Txxx)

Location: NAND, TBD



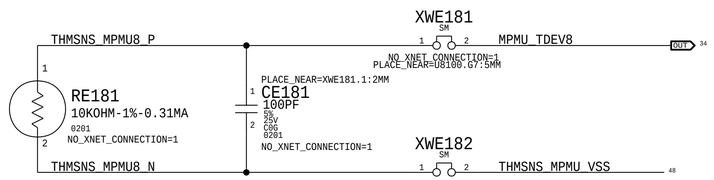
H Master PMU TDEV7 (TCHP)

Location: Charger Proximity



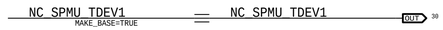
I Master PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)



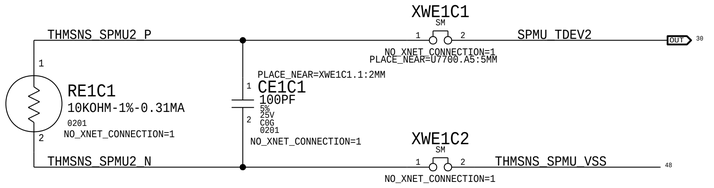
J Slave PMU TDEV1 (Txxx)

Location: TBD



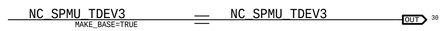
K Slave PMU TDEV2 (TH0T)

Location: NAND Proximity



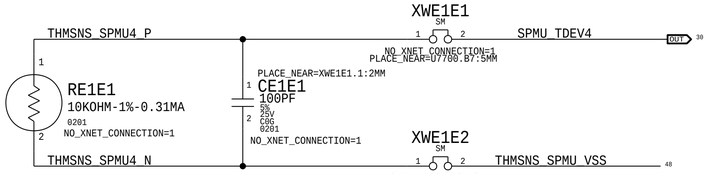
L Slave PMU TDEV3 (Txxx)

Location: TBD



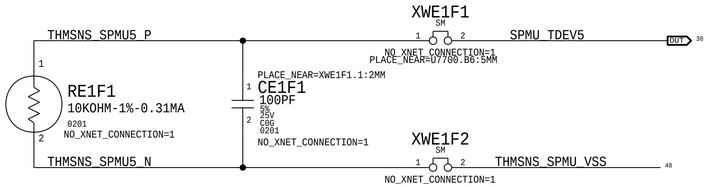
M Slave PMU TDEV4 (TSCD)

Location: SOC Proximity



N Slave PMU TDEV5 (TPSP)

Location: Slave PMU Proximity



BOM_COST_GROUP=SENSORS

PAGE TITLE: Sensors: Thermal

Apple Inc.

DRAWING NUMBER	051-05392
SIZE	D
REVISION	4.0.0
BRANCH	evt-1
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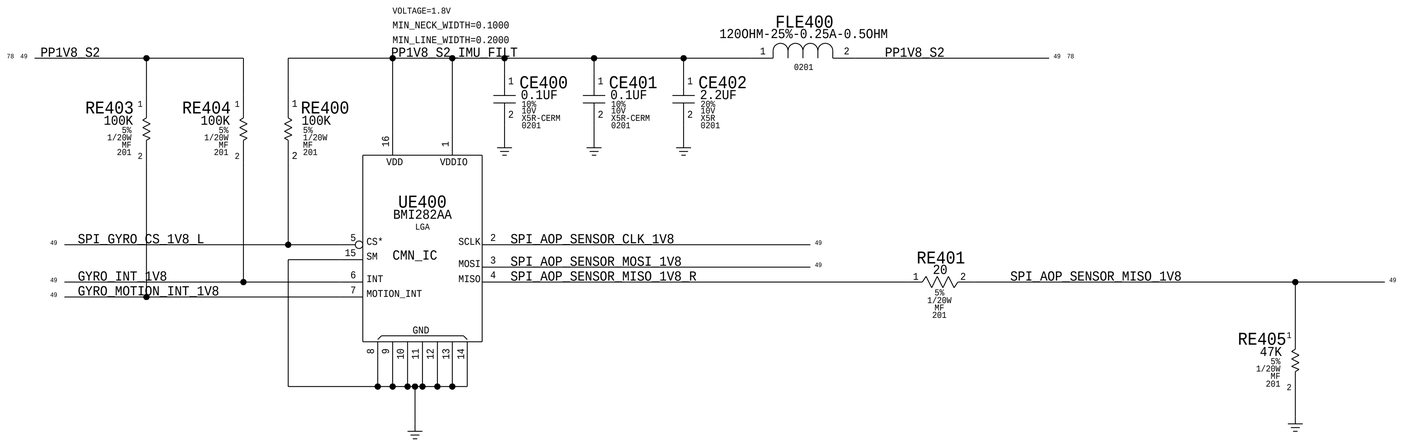
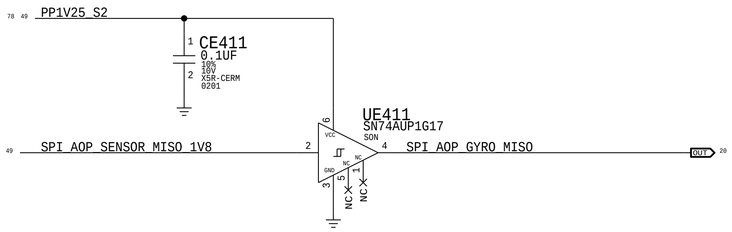
OPEN ITEMS:

FERRITE IS PLACEHOLDER ONLY
J417 USES 1555S0686 (01005)
MUST FIND PROPER PART, IF ONE IS NEEDED AT ALL

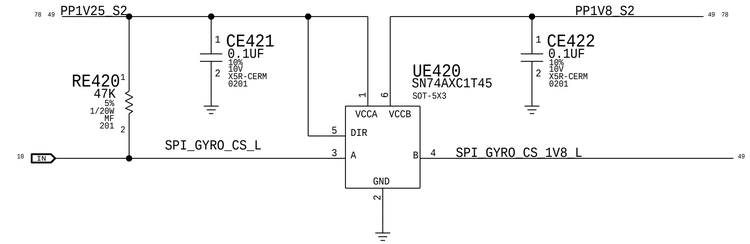
WHAT DOES SM SCAN MODE PIN DO AND WHY IS IT GROUNDED ON J417?

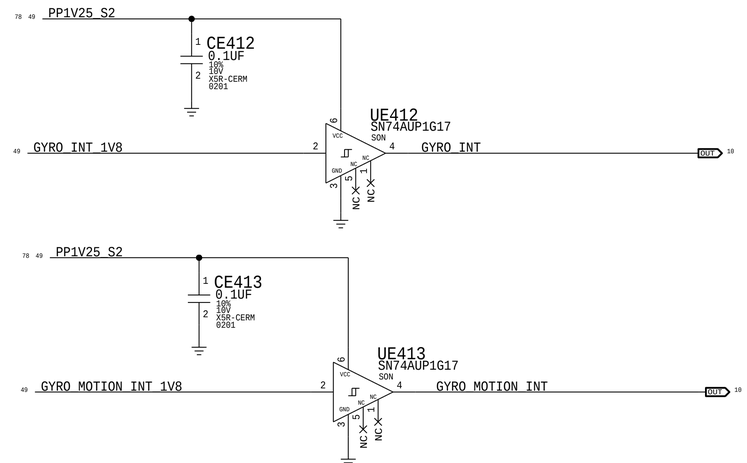
KOBOL: ACCEL & GYRO

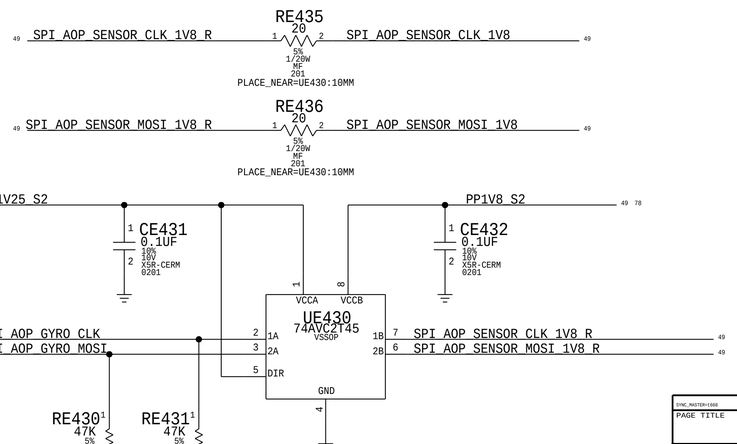




SPI LEVEL TRANSLATION







BOM_COST_GROUP=SENSORS

SYNC_MASTER=1668

PAGE TITLE

SENSORS: MOTION

Apple Inc.

DRAWING NUMBER	051-05392
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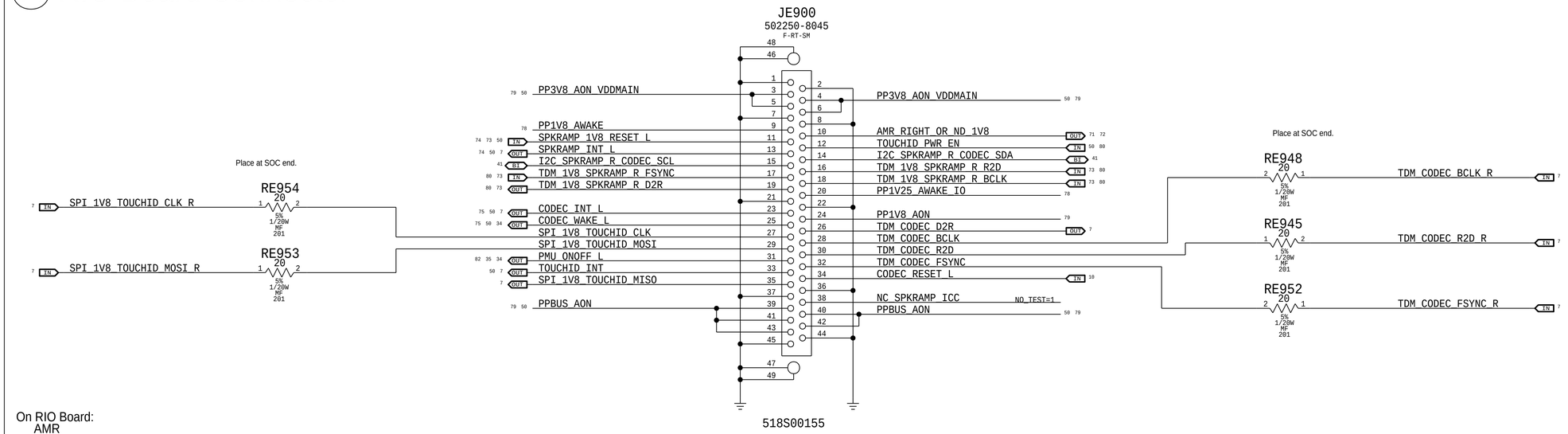
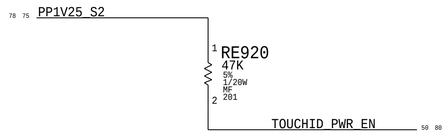
A RIO Board Connector



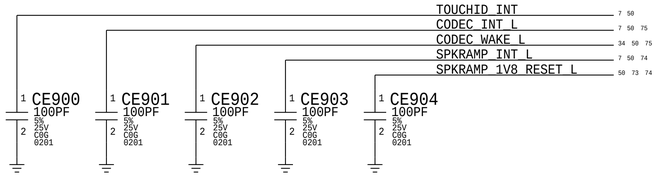
On RIO Board:
- AMR
- CODEC
- MESA
- SPKR AMP

Mates with 998-11285 or 998-11687
on RIO Flex J0200

B TOUCHID Power Enable Pull-Up



C RIO Control Capacitors



BOM_COST_GROUP=SYSTEM

SYNC_MASTER=ga_140 SYNC_DATE=05/31/2019

PAGE TITLE: RIO Connector

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
PAGE: 149 OF 801
SHEET: 50 OF 92

** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING

USBC_ATC0_R2D_C_P<1>	CF020	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_R2D_P<1>	GND_VOID=TRUE
USBC_ATC0_R2D_C_N<1>	CF021	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_R2D_N<1>	GND_VOID=TRUE
USBC_ATC0_R2D_C_P<2>	CF024	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_R2D_P<2>	GND_VOID=TRUE
USBC_ATC0_R2D_C_N<2>	CF025	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_R2D_N<2>	GND_VOID=TRUE
USBC_ATC0_D2R_P<1>	CF022	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_D2R_C_P<1>	GND_VOID=TRUE
USBC_ATC0_D2R_N<1>	CF023	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_D2R_C_N<1>	GND_VOID=TRUE
USBC_ATC0_D2R_P<2>	CF026	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_D2R_C_P<2>	GND_VOID=TRUE
USBC_ATC0_D2R_N<2>	CF027	0.22UF	20% X5R 6.3V 0201	USBC_ATC0_D2R_C_N<2>	GND_VOID=TRUE
USBC_ATC0_AUX_P	CF028	0.1UF	10% CERM-X5R 6.3V 0201	USBC_ATC0_AUX_C_P	
USBC_ATC0_AUX_N	CF029	0.1UF	10% CERM-X5R 6.3V 0201	USBC_ATC0_AUX_C_N	

RF028 33K 5% 1/20W MF 201 (NOSTUFF)
RF029 33K 5% 1/20W MF 201 (NOSTUFF)

CIO_ATC0_LSTX_3V3 → RF008 100K 5% 1/20W MF 201 → CIO_ATC0_LSTX
CIO_ATC0_LSRX_3V3 → RF009 100K 5% 1/20W MF 201 → CIO_ATC0_LSRX

UF000 9999HH BGA SYM 1 OF 2 (338S00561)

CRITICAL OMIT_TABLE

ASSRXP1	J1	USBC_ATC0_R2D_P<1>
ASSRXN1	J2	USBC_ATC0_R2D_N<1>
ASSRXP2	C1	USBC_ATC0_R2D_P<2>
ASSRXN2	C2	USBC_ATC0_R2D_N<2>
ASSTXP1	G1	USBC_ATC0_D2R_C_P<1>
ASSTXN1	G2	USBC_ATC0_D2R_C_N<1>
ASSTXP2	E1	USBC_ATC0_D2R_C_P<2>
ASSTXN2	E2	USBC_ATC0_D2R_C_N<2>
PA_AUX_P	L8	USBC_ATC0_AUX_C_P
PA_AUX_N	M8	USBC_ATC0_AUX_C_N
PA_LSTX_SBU1	M7	CIO_ATC0_LSTX_3V3
PA_LSRX_SBU2	L7	CIO_ATC0_LSRX_3V3
I2C_INT	A10	INT_I2C_ATCRTMR0_L
I2C_SCL	C9	I2C_UPC0_ATCRTMR0_SCL
I2C_SDA	E7	I2C_UPC0_ATCRTMR0_SDA
POC_GPIO_5	B9	ATCRTMR0_GPIO_5
POC_GPIO_6	A8	ATCRTMR0_GPIO_6
POC_GPIO_10 (IPU-65K)	A4	ATCRTMR0_FLASH_SHARE_EN
POC_GPIO_11 (IPU-65K)	A5	ATCRTMR01_FLASH_MSTR
POC_GPIO_12 (IPU-65K)	A6	ATCRTMR0_GPIO_12
THERMDA	M11	ATCRTMR0_THERM_DP
XTAL_25_IN	L9	ATCRTMR0_XTAL25M_IN
XTAL_25_OUT	M9	ATCRTMR0_XTAL25M_OUT
MONDC_SVR	L12	
MONDC	A11	
TEST_EDM	M12	
NC_A12	A12	NC
NC_J6	J6	NC
NC_L3	L3	NC
NC_J5	J5	NC

BSSRXP1	J12	USBC0_D2R_P<1>
BSSRXN1	J11	USBC0_D2R_N<1>
BSSRXP2	C12	USBC0_D2R_P<2>
BSSRXN2	C11	USBC0_D2R_N<2>
BSSTXP1	G12	USBC0_R2D_CR_P<1>
BSSTXN1	G11	USBC0_R2D_CR_N<1>
BSSTXP2	E12	USBC0_R2D_CR_P<2>
BSSTXN2	E11	USBC0_R2D_CR_N<2>
BSBU1	M10	USBC0_AUXLSX_P
BSBU2	L10	USBC0_AUXLSX_N
PERST*	B8	ATCRTMR01_ACTIVE_READY_3V3
RESET*	L11	ATCRTMR0_RESET_L
TDI	A3	JTAG_ATCRTMR01_TDI
TMS	C3	JTAG_ATCRTMR0_TMS
TCK	B5	JTAG_ATCRTMR01_TCK
TDO	C5	JTAG_ATCRTMR01_TDO
EE_DI	C6	SPI_ATCRTMR0_R_MOSI
EE_DO	B4	SPI_ATCRTMR0_R_MISO
EE_CS*	B6	SPI_ATCRTMR0_R_CS_L
EE_CLK	C7	SPI_ATCRTMR0_R_CLK
TEST_EN	B11	
TEST_PWR_GOOD	B3	ATCRTMR0_TEST_PWR_GOOD
RBIAS	L4	ATCRTMR0_RBIAS
RSENSE	L5	ATCRTMR0_RSENSE
ATEST_P	A1	NC
ATEST_N	A2	NC
FORCE_PWR	B10	ATCRTMR0_FORCE_PWR
FLASH_BUSY*	A9	FLASH_BUSY_USBC01_L
FUSE_VQPS_64	B2	
SMBUS_SCL	A7	NC_SMBUS_ATCRTMR0_SCL
SMBUS_SDA	B7	NC_SMBUS_ATCRTMR0_SDA

To SPI Flash

RF006 100 5% 1/20W MF 201
RF007 4.75K 0.5% 1/20W TF 0201 PLACE_NEAR=UF000.L5:2MM PLACE_NEAR=UF000.L4:2MM

PP3V3_S2SW_USBC0 pull-ups

PP3V3_S2SW_USBC0 → RF050 100K → ATCRTMR0_GPIO_5
NOSTUFF RF041 100K → ATCRTMR0_GPIO_6
ATCRTMR01_ACTIVE_READY_3V3 → RF040 0 → (ATCRTMR01_ACTIVE_READY_3V3)
NOSTUFF RF051 100K
NOSTUFF RF043 100K → ATCRTMR0_FLASH_SHARE_EN
NOSTUFF RF045 100K → ATCRTMR0_GPIO_12

Crystal

ATCRTMR0_XTAL25M_OUT_R → RF002 0 → ATCRTMR0_XTAL25M_OUT
CF002 20PF 5% 25V C0G 0201
CRITICAL YF000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CF003 20PF 5% 25V C0G 0201
ATCRTMR0_XTAL25M_IN_R → RF003 0 → ATCRTMR0_XTAL25M_IN

UF000 9999HH BGA SYM 2 OF 2 (338S00561)

CRITICIAL OMIT_TABLE

VCC0P9_SVR_ANA	F6 G6	
VCC0P9_SVR_PB_ANA	E9 G9	
VCC0P9_LVR	L6	PP0V9_ATCRTMR0_LVR (VOLTAGE=0.9V)
VCC0P9_LVR_SENSE	M6	
VCC3P3_LC	E5	
VCC3P3_ANA	L2	PP3V3_ATCRTMR0_ANA (VOLTAGE=3.3V)
VCC0P9_LC	J3	PP0V9_ATCRTMR0_LC (VOLTAGE=0.9V)
VSS	F3 F5 G5	
VSS_ANA	B1 B12 D1 D11 D12 D2 F1 F11 F12 F2	
VCC3P3_SX	E6	
VCC3P3A	J7	
VCC3P3_SVR	M4 M5	
VCC0P9_SVR	E3 G3	
SVR_IND	L1 M1	
SVR_VSS	M2 M3	
VSS_ANA	F7 F9 G7 H1 H11 H12 H2 J9 K1 K11 K12 K2	

MIN_LINE_WIDTH=0.1400
MIN_NECK_WIDTH=0.0750

CF054 10UF 20% 6.3V CERM 0402
CF055 2.2UF 20% 6.3V X5R-CERM 0201
CF056 2.2UF 20% 6.3V X5R-CERM 0201 (PP3V3_ATCRTMR0_LC, VOLTAGE=3.3V)
CF057 2.2UF 20% 6.3V X5R-CERM 0201
CF058 2.2UF 20% 6.3V X5R-CERM 0201

PP0V9_ATCRTMR0_SVR

CRITICAL CF065 20UF 20% 2.5V X6S-CERM 0402
CRITICAL CF064 20UF 20% 2.5V X6S-CERM 0402
CRITICAL CF063 20UF 20% 2.5V X6S-CERM 0402
CRITICAL CF062 20UF 20% 2.5V X6S-CERM 0402
CRITICAL CF061 4UF 20% 6.3V CER-X5R 0201
CRITICAL CF060 4UF 20% 6.3V CER-X5R 0201
CF050 4UF 20% 6.3V CER-X5R 0201
CF051 4UF 20% 6.3V CER-X5R 0201
CF052 4UF 20% 6.3V CER-X5R 0201
CF053 4UF 20% 6.3V CER-X5R 0201

PP3V3_ATCRTMR0_VCCA (VOLTAGE=3.3V)

CF043 12PF 5% 25V NP0-C0G 0201
CF030 2.2UF 20% 6.3V X5R-CERM 0201
CF031 10UF 20% 6.3V CERM 0402
RF000 0 5% 1/16W MF-LF 402
RF001 0 5% 1/16W MF-LF 402
CF036 2.2UF 20% 6.3V X5R-CERM 0201
CF037 2.2UF 20% 6.3V X5R-CERM 0201
NOSTUFF CF042 47UF 20% 6.3V CER-X5R 0603
FROM USB-C PORT CONTROLLER (UPC) PP3V3_S2SW_USBC0

PP3V3_ATCRTMR0_SVR (VOLTAGE=3.3V)

CF032 10UF 20% 6.3V CERM 0402 (BYPASS=UF000.M4:M3:3MM)
CF033 10UF 20% 6.3V CERM 0402
CF034 10UF 20% 6.3V CERM 0402
CF035 10UF 20% 6.3V CERM 0402
XWF001 SM NO_XNET_CONNECTION=1 → PP3V3_S2SW_USBC0
XWF000 SM P0V9_ATCRTMR0_SVR_PGND (VOLTAGE=0V) PLACE_NEAR=CF032.2:2MM NO_XNET_CONNECTION=1 → PP0V9_ATCRTMR0_SVR (VOLTAGE=0.9V)

CF038 12PF 5% 25V NP0-C0G 0201
CF039 4UF 20% 6.3V CER-X5R 0201
CF041 4UF 20% 6.3V CER-X5R 0201
CF040 47UF 20% 6.3V CER-X5R 0603

CRITICAL LF000 0.68UH-20%-4.3A-0.043OHM 0805
PP0V9_ATCRTMR0_SVR_IND (VOLTAGE=0.9V, DIDT=TRUE)

XWF030 SM ATCRTMR0_THERM_DN
PLACE_NEAR=UF000.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN CLOSEST TO THERMDA PIN

3.3V LDO

PACK_OPTION=PKGS:SMALL_PITCH
ALLOW_APPLE_PREFIX=U

UF015 TLV75533 X2SON-COMBO 353S02112
PP3V8_AON_VDDMAIN → IN
USBC0_3V3LDO_EN_R → EN
RF012 100K 5% 1/20W MF 201
CF010 1.0UF 20% 6.3V X5R 0201-1
CF015 1.0UF 20% 6.3V X5R 0201-1
OUT → PP3V3_S2SW_USBC0

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:LARGER_PITCH
UF015 TLV75533 WSON 353S02395
IN, EN, OUT, GND, EPAD; NC NC

BOM_COST_GROUP=TBT

SYNC_MASTER	ref_usbc_ace2
SYNC_DATE	04/24/2020
PAGE TITLE	USB-C: High Speed ATC0
Apple Inc.	
DRAWING NUMBER	051-05392
SIZE	D
REVISION	4.0.0
BRANCH	evt-1
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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
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USBC HIGH-SPEED AC COUPLING

USBC_ATC1_R2D_C_P<1>	CF120	0.22UF	USBC_ATC1_R2D_P<1>	GND_VOID=TRUE
USBC_ATC1_R2D_C_N<1>	CF121	0.22UF	USBC_ATC1_R2D_N<1>	GND_VOID=TRUE
USBC_ATC1_R2D_C_P<2>	CF124	0.22UF	USBC_ATC1_R2D_P<2>	GND_VOID=TRUE
USBC_ATC1_R2D_C_N<2>	CF125	0.22UF	USBC_ATC1_R2D_N<2>	GND_VOID=TRUE
USBC_ATC1_D2R_P<1>	CF122	0.22UF	USBC_ATC1_D2R_C_P<1>	GND_VOID=TRUE
USBC_ATC1_D2R_N<1>	CF123	0.22UF	USBC_ATC1_D2R_C_N<1>	GND_VOID=TRUE
USBC_ATC1_D2R_P<2>	CF126	0.22UF	USBC_ATC1_D2R_C_P<2>	GND_VOID=TRUE
USBC_ATC1_D2R_N<2>	CF127	0.22UF	USBC_ATC1_D2R_C_N<2>	GND_VOID=TRUE
USBC_ATC1_AUX_P	CF128	0.1UF	USBC_ATC1_AUX_C_P	
USBC_ATC1_AUX_N	CF129	0.1UF	USBC_ATC1_AUX_C_N	

All 0.22UF: 20% 6.3V X5R 0201. All 0.1UF: 10% 6.3V CERM-X5R 0201.

RF128 33K 5% 1/20W MF 201 — RF129 33K 5% 1/20W MF 201

CIO_ATC1_LSTX_3V3 — NOSTUFF RF108 100K 5% 1/20W MF 201 — CIO_ATC1_LSRX_3V3

RF109 100K 5% 1/20W MF 201

UF100 9999HH BGA SYM 1 OF 2 — 338S00561

CRITICAL OMIT_TABLE

USBC_ATC1_R2D_P<1>	ASSRXP1	J1
USBC_ATC1_R2D_N<1>	ASSRXN1	J2
USBC_ATC1_R2D_P<2>	ASSRXP2	C1
USBC_ATC1_R2D_N<2>	ASSRXN2	C2
USBC_ATC1_D2R_C_P<1>	ASSTXP1	G1
USBC_ATC1_D2R_C_N<1>	ASSTXN1	G2
USBC_ATC1_D2R_C_P<2>	ASSTXP2	E1
USBC_ATC1_D2R_C_N<2>	ASSTXN2	E2
USBC_ATC1_AUX_C_P	PA_AUX_P	L8
USBC_ATC1_AUX_C_N	PA_AUX_N	M8
	PA_LSTX_SBU1	M7
	PA_LSRX_SBU2	L7
INT_I2C_ATCRTMR1_L	I2C_INT	A10
I2C_UPC1_ATCRTMR1_SCL	I2C_SCL	C9
I2C_UPC1_ATCRTMR1_SDA	I2C_SDA	E7
ATCRTMR1_GPIO_5	POC_GPIO_5	B9
ATCRTMR1_GPIO_6	POC_GPIO_6	A8
ATCRTMR1_FLASH_SHARE_EN	POC_GPIO_10 (IPU - 65K)	A4
ATCRTMR01_FLASH_SLV_L	POC_GPIO_11 (IPU - 65K)	A5
ATCRTMR1_GPIO_12	POC_GPIO_12 (IPU - 65K)	A6
ATCRTMR1_THERM_DP	THERMDA	M11
ATCRTMR1_XTAL25M_IN	XTAL_25_IN	L9
ATCRTMR1_XTAL25M_OUT	XTAL_25_OUT	M9
	MONDC_SVR	L12
	MONDC	A11
	TEST_EDM	M12
	NC_A12	A12
	NC_J6	J6
	NC_L3	L3
	NC_J5	J5

USBC1_D2R_P<1>	BSSRXP1	J12
USBC1_D2R_N<1>	BSSRXN1	J11
USBC1_D2R_P<2>	BSSRXP2	C12
USBC1_D2R_N<2>	BSSRXN2	C11
USBC1_R2D_CR_P<1>	BSSTXP1	G12
USBC1_R2D_CR_N<1>	BSSTXN1	G11
USBC1_R2D_CR_P<2>	BSSTXP2	E12
USBC1_R2D_CR_N<2>	BSSTXN2	E11
USBC1_AUXLSX_P	BSBU1	M10
USBC1_AUXLSX_N	BSBU2	L10
ATCRTMR01_ACTIVE_READY_3V3	PERST*	B8
ATCRTMR1_RESET_L	RESET*	L11
JTAG_ATCRTMR01_TDI	TDI	A3
JTAG_ATCRTMR1_TMS	TMS	C3
JTAG_ATCRTMR01_TCK	TCK	B5
JTAG_ATCRTMR01_TDO	TDO	C5
SPI_ATCRTMR1_R_MOSI	EE_DI	C6
SPI_ATCRTMR1_R_MISO	EE_DO	B4
SPI_ATCRTMR1_R_CS_L	EE_CS*	B6
SPI_ATCRTMR1_R_CLK	EE_CLK	C7
	TEST_EN	B11
ATCRTMR1_TEST_PWR_GOOD	TEST_PWR_GOOD	B3
ATCRTMR1_RBIAS	RBIAS	L4
ATCRTMR1_RSENSE	RSENSE	L5
	ATEST_P	A1
	ATEST_N	A2
ATCRTMR1_FORCE_PWR	FORCE_PWR	B10
FLASH_BUSY_USBC01_L	FLASH_BUSY*	A9
	FUSE_VQPS_64	B2
NC_SMBUS_ATCRTMR1_SCL	SMBUS_SCL	A7
NC_SMBUS_ATCRTMR1_SDA	SMBUS_SDA	B7

To SPI Flash

RF106 100 5% 1/20W MF 201

RF107 4.75K 0.5% 1/20W TF 0201 — PLACE_NEAR=UF100.L5:2MM, PLACE_NEAR=UF100.L4:2MM

PP3V3_S2SW_USBC1 — ATCRTMR01_ACTIVE_READY_3V3 pull-up network

NOSTUFF	RF150 100K 5% 1/20W MF 201	ATCRTMR1_GPIO_5
NOSTUFF	RF141 100K 5% 1/20W MF 201	ATCRTMR1_GPIO_6
ATCRTMR01_ACTIVE_READY_3V3	RF140 0 5% 1/20W MF 0201	
NOSTUFF	RF151 100K 5% 1/20W MF 201	
NOSTUFF	RF143 100K 5% 1/20W MF 201	ATCRTMR1_FLASH_SHARE_EN
NOSTUFF	RF145 100K 5% 1/20W MF 201	ATCRTMR1_GPIO_12

ATCRTMR1_XTAL25M_OUT_R — ATCRTMR1_XTAL25M_IN_R

RF102 0 5% 1/20W 0201 MF — ATCRTMR1_XTAL25M_OUT

CF102 20PF 5% 25V C0G 0201

CRITICAL YF100 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM

CF103 20PF 5% 25V C0G 0201

RF103 0 5% 1/20W 0201 MF — ATCRTMR1_XTAL25M_IN

MIN_LINE_WIDTH=0.1400
MIN_NECK_WIDTH=0.0750

PP0V9_ATCRTMR1_SVR — CRITICAL decoupling

CF165 20UF 20% 2.5V X6S-CERM 0402 — CF164 20UF 20% 2.5V X6S-CERM 0402 — CF163 20UF 20% 2.5V X6S-CERM 0402 — CF162 20UF 20% 2.5V X6S-CERM 0402 — CF161 4UF 20% 6.3V CER-X5R 0201 — CF160 4UF 20% 6.3V CER-X5R 0201 — CF150 4UF 20% 6.3V CER-X5R 0201 — CF151 4UF 20% 6.3V CER-X5R 0201 — CF152 4UF 20% 6.3V CER-X5R 0201 — CF153 4UF 20% 6.3V CER-X5R 0201

UF100 9999HH BGA SYM 2 OF 2 — 338S00561

CRITICAL OMIT_TABLE

PP0V9_ATCRTMR1_SVR	VCC0P9_SVR_ANA	F6
	VCC0P9_SVR_PB_ANA	G6
		E9
		G9
PP0V9_ATCRTMR1_LVR (VOLTAGE=0.9V)	VCC0P9_LVR	L6
	VCC0P9_LVR_SENSE	M6
PP3V3_ATCRTMR1_ANA (VOLTAGE=3.3V)	VCC3P3_LC	E5
	VCC3P3_ANA	L2
PP0V9_ATCRTMR1_LC (VOLTAGE=0.9V)	VCC0P9_LC	J3
	VSS	F3
		F5
		G5
	VSS_ANA	B1
		B12
		D1
		D11
		D12
		D2
		F1
		F11
		F12
		F2
	VCC3P3_SX	E6
PP3V3_ATCRTMR1_VCCA (VOLTAGE=3.3V)	VCC3P3A	J7
PP3V3_ATCRTMR1_SVR (VOLTAGE=3.3V)	VCC3P3_SVR	M4
		M5
P0V9_ATCRTMR1_SVR_PGND (VOLTAGE=0V)	VCC0P9_SVR	E3
		G3
PP0V9_ATCRTMR1_SVR_IND (VOLTAGE=0.9V, DIDT=TRUE)	SVR_IND	L1
		M1
	SVR_VSS	M2
		M3
		F7
		F9
		G7
		H1
		H11
		H12
		H2
		J9
		K1
	VSS_ANA	K11
		K12
		K2

PP3V3_ATCRTMR1_VCCA (VOLTAGE=3.3V)

RF100 0 5% 1/16W 402 MF-LF

CF143 12PF 5% 25V NP0-C0G 0201 — CF130 2.2UF 20% 6.3V X5R-CERM 0201 — CF131 10UF 20% 6.3V CERM 0402

FROM USB-C PORT CONTROLLER (UPC) — PP3V3_S2SW_USBC1

CF136 2.2UF 20% 6.3V X5R-CERM 0201 — CF137 2.2UF 20% 6.3V X5R-CERM 0201 — NOSTUFF CF142 47UF 20% 6.3V CER-X5R 0603

PP3V3_ATCRTMR1_SVR (VOLTAGE=3.3V)

RF101 0 5% 1/16W 402 MF-LF

XWF101 SM — NO_XNET_CONNECTION=1 — PP3V3_S2SW_USBC1

CF132 10UF 20% 6.3V CERM 0402 — CF133 10UF 20% 6.3V CERM 0402 — CF134 10UF 20% 6.3V CERM 0402 — CF135 10UF 20% 6.3V CERM 0402

BYPASS=UF100.M4:M3:3MM

XWF100 SM — P0V9_ATCRTMR1_SVR_PGND (VOLTAGE=0V)

PLACE_NEAR=CF132.2:2MM, NO_XNET_CONNECTION=1 — PP0V9_ATCRTMR1_SVR (VOLTAGE=0.9V)

CF138 12PF 5% 25V NP0-C0G 0201 — CF139 4UF 20% 6.3V CER-X5R 0201 — CF141 4UF 20% 6.3V CER-X5R 0201

CRITICAL LF100 0.68UH-20%-4.3A-0.043OHM 0805

CF140 47UF 20% 6.3V CER-X5R 0603

PP0V9_ATCRTMR1_SVR_IND (VOLTAGE=0.9V, DIDT=TRUE)

XWF130 SM — ATCRTMR1_THERM_DN

PLACE_NEAR=UF100.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN CLOSEST TO THERMDA PIN

3.3V LDO

PACK_OPTION=PKGS:SMALL_PITCH
ALLOW_APPLE_PREFIX=U

UF115 TLV75533 X2SON-COMBO 353S02112 — IN: PP3V8_AON_VDDMAIN — EN: USBC1_3V3LDO_EN_R — OUT: PP3V3_S2SW_USBC1

RF112 100K 5% 1/20W MF 201 — CF110 1.0UF 20% 6.3V X5R 0201-1 — CF115 1.0UF 20% 6.3V X5R 0201-1

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:LARGER_PITCH

UF115 TLV75533 WSON — IN, EN, OUT, NC, GND, EPAD

BOM_COST_GROUP=TBT

SYNC_MASTER	rvf_usbc_acc2
SYNC_DATE	04/24/2020
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Apple Inc.	
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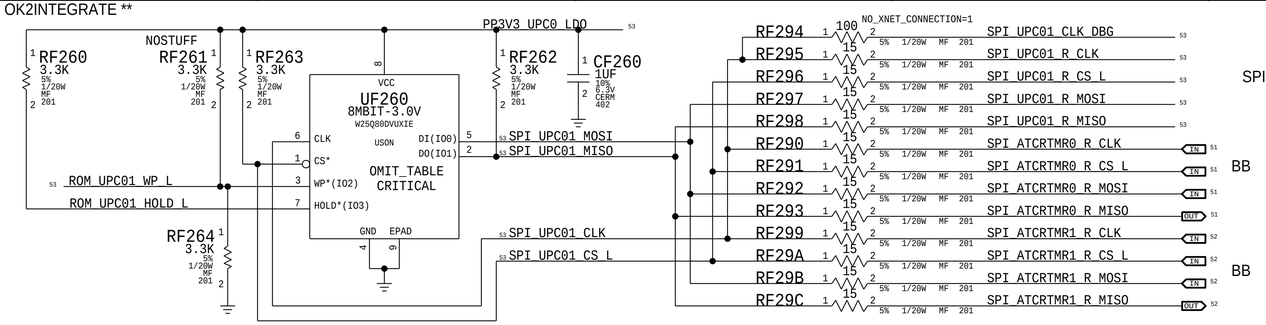
** OK2INTEGRATE **



NO_XNET_CONNECTION=1

SPI Ace

RF294 100	SPI_UPC01_CLK_DBG	
RF295 15	SPI_UPC01_R_CLK	
RF296 15	SPI_UPC01_R_CS_L	
RF297 15	SPI_UPC01_R_MOSI	
RF298 15	SPI_UPC01_R_MISO	
RF290 15	SPI_ATCRTMR0_R_CLK	IN
RF291 15	SPI_ATCRTMR0_R_CS_L	IN
RF292 15	SPI_ATCRTMR0_R_MOSI	IN
RF293 15	SPI_ATCRTMR0_R_MISO	OUT
RF299 15	SPI_ATCRTMR1_R_CLK	IN
RF29A 15	SPI_ATCRTMR1_R_CS_L	IN
RF29B 15	SPI_ATCRTMR1_R_MOSI	IN
RF29C 15	SPI_ATCRTMR1_R_MISO	OUT

BB

BB

Ace 0 is SPI Ace?

PACK_OPTION=USBC_SPI_UPC0

SPI_UPC01_R_CLK	MAKE_BASE=TRUE	SPI_UPC01_R_CLK IN
SPI_UPC01_R_CS_L	MAKE_BASE=TRUE	SPI_UPC01_R_CS_L IN
SPI_UPC01_R_MOSI	MAKE_BASE=TRUE	SPI_UPC01_R_MOSI IN
SPI_UPC01_R_MISO	MAKE_BASE=TRUE	SPI_UPC01_R_MISO OUT
ROM_UPC01_WP_L	MAKE_BASE=TRUE	ROM_UPC01_WP_L IN
SWD_UPC_SWCLK	MAKE_BASE=TRUE	SWD_UPC_SWCLK IN
SWD_UPC_SWDIO0	MAKE_BASE=TRUE	SWD_UPC_SWDIO0 BI
PP3V3_UPC0_LDO	MAKE_BASE=TRUE	PP3V3_UPC0_LDO OUT

Ace 1 is SPI Ace?

PACK_IGNORE=TRUE
PACK_OPTION=USBC_SPI_UPC1

GND	IN
GND	IN
GND	IN
GND	OUT
PD_UPC1_HPD	IN
SWD_UPC01_UART_CLK	IN
SWD_UPC01_UART_DATA	BI
PP3V3_UPC1_LDO MAKE_BASE=TRUE	OUT

(Internal pull-up) Master should be on SPI Ace2.

PP3V3_S2SW_USBC0 — NOSTUFF — 100K — RF244 — ATCRTMR01_FLASH_MSTR (OUT)

FLASH_BUSY_USBC01_L (BI) — MAKE_BASE=TRUE

(Internal pull-up) Master should be on SPI Ace2.

PP3V3_S2SW_USBC1 — NOSTUFF — 100K — RF244 — ATCRTMR01_FLASH_SLV_L (OUT)

ATCRTMR01_FLASH_MSTR — MAKE_BASE=TRUE

PD_UPC1_GPIO1 (BI)

Ace 1 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0

GND	MAKE_BASE=TRUE	IN
GND	MAKE_BASE=TRUE	IN
GND	MAKE_BASE=TRUE	IN
GND	MAKE_BASE=TRUE	OUT
SWD_UPC01_UART_CLK	MAKE_BASE=TRUE	IN
SWD_UPC01_UART_DATA	MAKE_BASE=TRUE	BI

ATCRTMR01_FLASH_SLV_L

RF247 2.2K	ATCRTMR01_FLASH_SLV_L	OUT
RF272 100K	PD_UPC1_GPIO1	BI
RF273 100K	PD_UPC1_HPD	OUT

Ace 0 is UART Ace?

PACK_IGNORE=TRUE
PACK_OPTION=USBC_SPI_UPC1

SPI_UPC01_R_CLK	MAKE_BASE=TRUE	IN
SPI_UPC01_R_CS_L	MAKE_BASE=TRUE	IN
SPI_UPC01_R_MOSI	MAKE_BASE=TRUE	IN
SPI_UPC01_R_MISO	MAKE_BASE=TRUE	OUT
SWD_UPC_SWCLK	MAKE_BASE=TRUE	IN
SWD_UPC_SWDIO0	MAKE_BASE=TRUE	BI

ATCRTMR01_FLASH_SLV_L

RF247 2.2K	ATCRTMR01_FLASH_MSTR	OUT
RF272 100K	FLASH_BUSY_USBC01_L	BI
RF273 100K	ROM_UPC01_WP_L	OUT

UART_UPC01_TX	SPI Ace	UART_UPC01_TX	MAKE_BASE=TRUE	UART_UPC01_TX OUT
UART_UPC01_RX	SPI Ace	UART_UPC01_RX	MAKE_BASE=TRUE	UART_UPC01_RX IN
UART_UPC01_RX	SPI Ace	UART_UPC01_RX		UART_UPC01_RX OUT
UART_UPC01_TX	SPI Ace	UART_UPC01_TX		UART_UPC01_TX IN

ACE ARKANOID CONN

JF200 — USBC_DBG — 505070-1222 M-ST-SM

SMC		SOC
ATCRTMR0_RESET_L	1 2	UPC_I2C_INT_L
I2C_SMC_UPC_SCL	3 4	I2C_UPC_SDA
I2C_SMC_UPC_SDA	5 6	I2C_UPC_SCL
UPC_SMC_I2C_INT_L	7 8	UPC0_SER_DBG
SPI_UPC01_CLK_DBG	9 10	UPC1_SER_DBG
UART_UPC01_TX	11 12	UART_UPC01_RX
SPI Ace	15 16	SPI Ace

BRIDGE ARKANOID CONN

JF201 — USBC_DBG — 505070-1222 M-ST-SM

ATCRTMR0_FORCE_PWR	1 2	INT_I2C_UPC0_ATCRTMR0_L
PP3V3_S2SW_USBC0	3 4	I2C_UPC0_ATCRTMR0_SCL
PP0V9_ATCRTMR0_LC	5 6	I2C_UPC0_ATCRTMR0_SDA
ATCRTMR01_ACTIVE_READY_3V3	7 8	ATCRTMR1_FORCE_PWR
PP3V3_S2SW_USBC1	9 10	INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SDA	11 12	I2C_UPC1_ATCRTMR1_SCL
	15 16	

USBC_DBG

RF280 200K — VREFB_ARDV01 — PP3V3_S2_UPC

PP1V25_S2 — CF281 0.1UF 10% 6.3V CERM-X5R 0201

PACK_OPTION=PKGS:SMALL_PITCH

UF280 LSF0102 X2SON 311S00234 — VREF_A VREF_B — EN A1 A2 B1 B2 GND

CF280 0.1UF 10% 6.3V CERM-X5R 0201

RF282 5.1K 5% 1/20W MF 201 — RF283 5.1K 5% 1/20W MF 201

I2C_UPC_SCL — I2C_UPC01_3V3_SCL

I2C_UPC_SDA — I2C_UPC01_3V3_SDA

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:LARGER_PITCH

UF280 LSF0102 VSSOP 311S00257 — USBC_DBG

AARDVARKANOID CONN

JF202 — USBC_DBG — 505070-1222 M-ST-SM

SPI ACE

PP1V25_S2	1 2	SPI_UPC01_CS_L
SWD_UPC_SWDIO0	3 4	SPI_UPC01_CLK
SWD_UPC_SWCLK	5 6	SPI_UPC01_MOSI
SPI_UPC01_MISO	7 8	SWD_UPC01_UART_CLK
I2C_UPC01_3V3_SDA	9 10	SWD_UPC01_UART_DATA
I2C_UPC01_3V3_SCL	11 12	PP1V25_S2
	15 16	

UART ACE

BOM_COST_GROUP=USB-C

ATC0: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 pull-downs

GND — NC_UPC1_I2C_ADDR — MAKE_BASE=TRUE — NC_UPC1_I2C_ADDR — NO_TEST=1

Configure to enable VDDIO and use it for SWD.

GND — GND — MAKE_BASE=TRUE

PP3V3_UPC0_LDO — 10K — RF242 — FLASH_BUSY_USBC01_L — MAKE_BASE=TRUE

INT_I2C_ATCRTMR0_L	UPC_ATCRTMR_INT	RF210 0	INT_I2C_UPC0_ATCRTMR0_L
INT_I2C_EUSBLS0_L	UPC_EUSBLS_INT	RF211 0	
INT_I2C_ATCRTMR1_L	UPC_ATCRTMR_INT	RF215 0	INT_I2C_UPC1_ATCRTMR1_L
INT_I2C_EUSBLS1_L	UPC_EUSBLS_INT	RF216 0	

Is UPCx_5V_EN being used?

UPC0_5V_EN — RF234 100K

UPC1_5V_EN — RF235 100K

PACK_OPTION=USBC01_VR5V_LOCAL_NO

PP3V3_S2_UPC

RF220 10K	JTAG_ATCRTMR01_TCK	JTAG_ATCRTMR01_TCK OUT
RF221 10K	JTAG_ATCRTMR0_TMS	JTAG_ATCRTMR0_TMS OUT
RF222 100K	JTAG_ATCRTMR1_TMS	JTAG_ATCRTMR01_TDI OUT
RF223 100K	JTAG_ATCRTMR01_TDI	JTAG_ATCRTMR01_TDO IN
RF224 10K	JTAG_ATCRTMR01_TDO	JTAG_ATCRTMR01_TCK OUT
		JTAG_ATCRTMR1_TMS OUT
		JTAG_ATCRTMR01_TDI OUT
		JTAG_ATCRTMR01_TDO IN

PP1V25_S2 — CF230 0.1UF 10% 6.3V CERM-X5R 0201

PP3V3_S2_UPC — CF231 0.1UF 10% 6.3V CERM-X5R 0201

311S00243 UF230 SN74AXC1T45 SOT-5X3 — VCCA VCCB DIR A B GND

PMU_ACTIVE_READY — ATCRTMR01_ACTIVE_READY_3V3

HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

CRITICAL 0603-1 FF200 6A-32V — PPDCIN_AONSW — PPHV_INT0_AONSW — PLACE_NEAR=UF400:5MM — MAKE_BASE=TRUE VOLTAGE=20V

RF200 0 — PPHV_INT0_AONSW

CRITICAL 0603-1 FF201 6A-32V — PPHV_INT1_AONSW — PLACE_NEAR=UF500:5MM — MAKE_BASE=TRUE VOLTAGE=20V

RF201 0 — PPHV_INT1_AONSW

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.

PPVBUS_USBC0 — MAKE_BASE=TRUE — PPVBUS_USBC0

PPVBUS_USBC1 — MAKE_BASE=TRUE — PPVBUS_USBC1

SYNC_MASTER=ref_usbc_acc2 SYNC_DATE=04/24/2020

PAGE TITLE

USB-C: Support 1 ATC01

Apple Inc.

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** OK2INTEGRATE **

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC0 / UPC0 / RTMR0

UART_DEBUGPRT_R2D	MAKE_BASE=TRUE	IN	7	=	UART_DEBUGPRT_R2D	IN	54	55
UART_DEBUGPRT_D2R	MAKE_BASE=TRUE	OUT	7	=	UART_DEBUGPRT_D2R	IN	54	55
SWD_SOC_SWCLK	MAKE_BASE=TRUE	BI	10	=	SWD_SOC_SWCLK	OUT	54	55
SWD_SOC_SWDIO	MAKE_BASE=TRUE	BI	10	=	SWD_SOC_SWDIO	OUT	54	55
UART_SMC_DEBUGPRT_R2D	MAKE_BASE=TRUE	IN	10	=	UART_SMC_DEBUGPRT_R2D	OUT	54	55
UART_SMC_DEBUGPRT_D2R	MAKE_BASE=TRUE	OUT	10	=	UART_SMC_DEBUGPRT_D2R	IN	54	55
USB_DBG_LS_P	MAKE_BASE=TRUE	BI	80	=	USB_DBG_LS_P	BI	54	55
USB_DBG_LS_N	MAKE_BASE=TRUE	BI	80	=	USB_DBG_LS_N	BI	54	55
PP1V8_S2		BI		=	PP1V8_S2	BI	54	55 58
PP1V8_S2		BI		=	PP1V8_S2	BI	54	58
SOC_DOCK_CONNECT		OUT	80	=	SOC_DOCK_CONNECT	IN	54	55
SOC_DFU_STATUS	MAKE_BASE=TRUE	IN	82 20 6	=	SOC_DFU_STATUS	OUT	54	55
SOC_FORCE_DFU	MAKE_BASE=TRUE	OUT	82 34 6	=	SOC_FORCE_DFU	IN	54	55

Ace 1 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC1

ATC1 / UPC1 / RTMR1

PD_UPC1_DBG0_R		OUT	54	=	PD_UPC1_DBG0_R		56		
PD_UPC1_DBG1_R		IN	54	=	PD_UPC1_DBG1_R		56		
PD_UPC1_DBG2_R		IN	54	=	PD_UPC1_DBG2_R		56		
PD_UPC1_DBG3_R		IN	54	=	PD_UPC1_DBG3_R		56		
PD_UPC1_DBG4_R		OUT	54	=	PD_UPC1_DBG4_R		56		
PD_UPC1_DBG5_R		IN	54	=	PD_UPC1_DBG5_R		56		
PD_UPC1_USBP2_RP		BI	54	=	PD_UPC1_USBP2_RP		56		
PD_UPC1_USBP2_RN		BI	54	=	PD_UPC1_USBP2_RN		56		
PP1V8_S2		BI	54	=	PP1V8_S2		56		58
PP1V8_S2		BI	54	=	PP1V8_S2		58		
PD_UPC1_GPIO7		OUT	54	=	PD_UPC1_GPIO7		56		
PD_UPC1_GPIO9		OUT	54	=	PD_UPC1_GPIO9		56		
PD_UPC1_GPIO10		OUT	54	=	PD_UPC1_GPIO10		56		

Main Debug Port

Ace2 GPIOs

Ace 1 is non-debug Port?

ATC1 / UPC1 / RTMR1

PACK_OPTION=USBC_DEBUG_UPC0

PP1V8_S2		BI		=	PP1V8_S2	BI	54	56	58
PP1V8_S2		BI		=	PP1V8_S2	BI	54	58	
RF320 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG0_R		=	PD_UPC1_DBG0_R	BI	54	56	
RF321 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG1_R		=	PD_UPC1_DBG1_R	BI	54	56	
RF322 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG2_R		=	PD_UPC1_DBG2_R	BI	54	56	
RF323 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG3_R		=	PD_UPC1_DBG3_R	BI	54	56	
RF324 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG4_R		=	PD_UPC1_DBG4_R	BI	54	56	
RF325 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG5_R		=	PD_UPC1_DBG5_R	BI	54	56	
RF328 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_USBP2_RP		=	PD_UPC1_USBP2_RP	BI	54	56	
RF329 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_USBP2_RN		=	PD_UPC1_USBP2_RN	BI	54	56	

Ace2 GPIOs

RF373 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_GPIO7		=	PD_UPC1_GPIO7	OUT	54	56	
RF374 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_GPIO9		=	PD_UPC1_GPIO9	OUT	54	56	
RF375 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_GPIO10		=	PD_UPC1_GPIO10	OUT	54	56	

CKPLUS_WATVE=SINGLE_NODENET
on all nets above.

Ace 0 is non-debug Port?

ATC0 / UPC0 / RTMR0

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DEBUG_UPC1

PP1V8_S2		BI		=	PP1V8_S2	BI	54	55	58
PP1V8_S2		BI		=	PP1V8_S2	BI	54	58	
RF310 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG0_R		=	UART_DEBUGPRT_R2D	BI	54	55	
RF311 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG1_R		=	UART_DEBUGPRT_D2R	BI	54	55	
RF312 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG2_R		=	SWD_SOC_SWCLK	BI	54	55	
RF313 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG3_R		=	SWD_SOC_SWDIO	BI	54	55	
RF314 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG4_R		=	UART_SMC_DEBUGPRT_R2D	BI	54	55	
RF315 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG5_R		=	UART_SMC_DEBUGPRT_D2R	BI	54	55	
RF318 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_USBP2_RP		=	USB_DBG_LS_P	BI	54	55	
RF319 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_USBP2_RN		=	USB_DBG_LS_N	BI	54	55	

Ace2 GPIOs

RF363 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_GPIO7		=	SOC_DOCK_CONNECT	OUT	54	55	
RF364 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_GPIO9		=	SOC_DFU_STATUS	OUT	54	55	
RF365 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_GPIO10		=	SOC_FORCE_DFU	OUT	54	55	

CKPLUS_WATVE=SINGLE_NODENET
on all nets above.

Non-debug Port

Unused ports

RF316 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG6_R		=	PD_UPC0_DBG6_R	BI		55	
RF317 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_DBG7_R		=	PD_UPC0_DBG7_R	BI		55	
RF31A 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_USBP3_RP		=	PD_UPC0_USBP3_RP	BI		55	
RF31B 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC0_USBP3_RN		=	PD_UPC0_USBP3_RN	BI		55	
RF326 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG6_R		=	PD_UPC1_DBG6_R	BI		56	
RF327 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_DBG7_R		=	PD_UPC1_DBG7_R	BI		56	
RF32A 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_USBP3_RP		=	PD_UPC1_USBP3_RP	BI		56	
RF32B 1/20W 5% MF 201 100K	MAKE_BASE=TRUE	PD_UPC1_USBP3_RN		=	PD_UPC1_USBP3_RN	BI		56	

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

PP3V3_UPC0_LDO	MAKE_BASE=TRUE	OUT	55	=	PP3V3_UPC0_LDO	IN	53	55	
USBC0_CC1	MAKE_BASE=TRUE	BI	55	=	USBC0_CC1	BI	55	57	
USBC0_CC2	MAKE_BASE=TRUE	BI	55	=	USBC0_CC2	BI	55	57	
PP3V3_UPC1_LDO	MAKE_BASE=TRUE	OUT	56	=	PP3V3_UPC1_LDO	IN	53	56	
USBC1_CC1	MAKE_BASE=TRUE	BI	56	=	USBC1_CC1	BI	56	57	
USBC1_CC2	MAKE_BASE=TRUE	BI	56	=	USBC1_CC2	BI	56	57	

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP

MAKE_BASE=TRUE

BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_ace2 SYNC_DATE=04/24/2020

PAGE TITLE

USB-C: Support 2 ATC01

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D

REVISION 4.0.0

BRANCH evt-1

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SHEET 54 OF 92

** OK2INTEGRATE **

PP3V3_UPC0_LDO 53 54 55

Internal Pull-ups
Enabled after reading straps

RF409 1M 5% 1/20W MF 201 — I2C_UPC0_ATCRTMR0_SCL (CKPLUS_WAIVE=I2C_PULLUP) 51 53 55 58
RF408 1M 5% 1/20W MF 201 — I2C_UPC0_ATCRTMR0_SDA (CKPLUS_WAIVE=I2C_PULLUP) 51 53 55 58
RF407 10K 5% 1/20W MF 201 — INT_I2C_UPC0_ATCRTMR0_L 53 55
RF404 100K 5% 1/20W MF 201 — UPC_FORCE_PWR (PACK_OPTION=ACE2_GPIO6_PD, PACK_IGNORE=TRUE) 55 59
RF405 1M 5% 1/20W MF 201 — UART_UPC01_RX 53 55
RF406 100K 5% 1/20W MF 201 — PD_UPC0_MRESET 55
RF402 100K 5% 1/20W MF 201 — PD_UPC0_GPIO5 55

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

GND I2C_ADDR
PRIMARY ONLY

CRITICAL
RF403 15K 0.1% 1/20W TF-LF 0201

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

53 PPHV_INT0_AONSW

MAX 100uF TOTAL ON RAIL

79 56 PP5V_S2
79 56 PP5V_S2
CAP FOR PP_5V0 ON VR PAGE

K9 L10 M9 M10 K11 L12 M11 N12 — PP_5V0
M14 M13 — PP_CABLE
G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4 — PP_HV
G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8 — VBUS

UF400
CD3217B12BCE
FCBGA
353S02158
CRITICAL
OMIT_TABLE

	B13	HRESET		
55 PD_UPC0_MRESET	A14	MRESET		
58 53 51 OUT ATCRTMR0_RESET_L	B17	RESET*		
53 OUT UPC0_SER_DBG	A2			
	B1	GPIO0		
53 OUT FLASH_BUSY_USBC01_L	D1	GPIO1		
55 53 IN INT_I2C_UPC0_ATCRTMR0_L	F1	GPIO2		
53 OUT UPC0_5V_EN	C2	GPIO3		
53 51 OUT ATCRTMR0_FORCE_PWR	E2	GPIO4		
55 PD_UPC0_GPIO5	B3	GPIO5		
59 55 IN UPC_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL	
54 OUT SOC_DOCK_CONNECT	D3	GPIO7		
56 35 OUT UPC_PMU_RESET_3V3	E4	GPIO8		
54 IN SOC_DFU_STATUS	F3	GPIO9		
54 OUT SOC_FORCE_DFU	F7	GPIO10		
54 PP3V3_UPC0_LDO	A18	BUSPOWER		
53 GND	M19	I2C_ADDR	IPU-BOOT	
UPC0_R_OSC	M21	R_OSC		
58 55 53 51 B1 I2C_UPC0_ATCRTMR0_SDA	A16	I2CM_SDA_CNFG		
58 55 53 51 B1 I2C_UPC0_ATCRTMR0_SCL	B15	I2CM_SCL_CNFG		
53 41 B1 I2C_UPC_SDA	B5	I2C_SDA1		
53 41 B1 I2C_UPC_SCL	A4	I2C_SCL1		
53 41 OUT UPC_I2C_INT_L	D7	I2C_IRQ1*		
53 43 B1 I2C_SMC_UPC_SDA	B7	I2C_SDA2		
53 43 B1 I2C_SMC_UPC_SCL	A6	I2C_SCL2		
53 43 OUT UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*		
53 OUT SPI_UPC01_R_CLK	B9	SPI_CLK		
53 OUT SPI_UPC01_R_MOSI	B11	SPI_MOSI		
58 IN SPI_UPC01_R_MISO	A10	SPI_MISO		
53 OUT SPI_UPC01_R_CS_L	A8	SPI_SSZ		
53 B1 SWD_UPC_SWDIO0	E20	SWD_DATA	IPU	
53 B1 SWD_UPC_SWCLK	E16	SWD_CLK	IPU	
55 58 IN UART_UPC01_RX	B19	UART_RX		
53 OUT UART_UPC01_TX	A20	UART_TX		
59 B1 USB2_UPC0_P1_P	H19	USB_RP1_P		
59 B1 USB2_UPC0_P1_N	H21	USB_RP1_N		
54 B1 USB_DBG_LS_P	G20	USB_RP2_P		
54 B1 USB_DBG_LS_N	G22	USB_RP2_N		
54 B1 PD_UPC0_USBP3_RP	F19	USB_RP3_P		
54 B1 PD_UPC0_USBP3_RN	F21	USB_RP3_N		
52 B1 USBC0_AUXLSX_P	J12	AUX_P		
52 B1 USBC0_AUXLSX_N	H11	AUX_N		
53 OUT ROM_UPC01_WP_L	C12	HPD		
54 B1 UART_DEBUGPRT_R2D	G12	DEBUG0		
54 B1 UART_DEBUGPRT_D2R	F11	DEBUG1		
54 OUT SWD_SOC_SWCLK	E8	DEBUG2		
54 B1 SWD_SOC_SWDIO	E12	DEBUG3		
54 B1 UART_SMC_DEBUGPRT_R2D	G16	DEBUG4		
54 B1 UART_SMC_DEBUGPRT_D2R	F15	DEBUG5		
54 IN PD_UPC0_DBG6_R	D15	DEBUG6		
54 OUT PD_UPC0_DBG7_R	D19	DEBUG7		

PORT_MUX

VIN_3V3	C20	PPVBUS_USBC0	53 57
VDDIO	A12	PP3V3_S2_UPC	53 56 78
VDDIO_CFG	D11	GND	53
LDO_3V3	C22	PP3V3_UPC0_LDO	53 54 55
	D21		
VIN_LV	L20	PP1V8_S2	54 58
VOUT_LV	L18	USBC0_3V3LDO_EN	59
VREF	C16		
SS	L22	UPC0_SS	
LDO_CORE	E22	PP1V5_UPC0_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC0	53
PP_HV_OPT	F5	PPHV_INT0_AONSW	53
C_CC1	M15 N16	USBC0_CC1	B1 54 57
C_CC2	M17 N18	USBC0_CC2	B1 54 57
RPD_G1	L14	USBC0_CC1	B1 54
RPD_G2	L16	USBC0_CC2	B1 54
C_USB_TP	K19	USBC0_USB_TOP_P	B1 57
C_USB_TN	K21	USBC0_USB_TOP_N	B1 57
C_USB_BP	J20	USBC0_USB_BOT_P	B1 57
C_USB_BN	J22	USBC0_USB_BOT_N	B1 57
C_SBU1	J16	USBC0_SBU1	B1 57
C_SBU2	H15	USBC0_SBU2	B1 57

POWER

TYPE-C

GND

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

GND
A22 H9 N20 B21 K15 N22

CF401 1UF 10% 25V X5R 0402 — PPVBUS_USBC0
CF400 10UF 20% 6.3V CERM 0402 — PP3V3_S2_UPC
CF402 1.0UF 20% 6.3V X5R 0201-1 — PP1V25_S2
CF408 10UF 20% 6.3V CERM 0402 — PP3V3_UPC0_LDO (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V)
CF403 0.1UF 10% 6.3V CERM-X5R 0201 — PP1V8_S2
USBC0_3V3LDO_EN (cap needed when used as power source)
CF405 10UF 20% 6.3V CERM 0402 — PP1V5_UPC0_LDO_CORE (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.0750)
CF409 0.68UF 20% 6.3V X6S 0402 — PACK_OPTION=ACE2_SS_CAP; PACK_OPTION=ACE2_SS_GND → GND (MAKE_BASE=TRUE)
CF414 220PF 5% 50V C0G 0201-1 — MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.1500
CF413 220PF 5% 50V C0G 0201-1 — MIN_LINE_WIDTH=0.4000, MIN_NECK_WIDTH=0.1500

BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_ace2 SYNC_DATE=04/24/2020

PAGE TITLE
USB-C: Port Controller ATC0

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
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** OK2INTEGRATE **

PP3V3_UPC1_LDO 53 54 56

RF509 1M 5% 1/20W MF 201 — I2C_UPC1_ATCRTMR1_SCL 52 53 56 58 — CKPLUS_WAIVE=I2C_PULLUP
RF508 1M 5% 1/20W MF 201 — I2C_UPC1_ATCRTMR1_SDA 52 53 56 58 — CKPLUS_WAIVE=I2C_PULLUP
RF507 10K 5% 1/20W MF 201 — INT_I2C_UPC1_ATCRTMR1_L 53 56
RF504 100K 5% 1/20W MF 201 — UPC_FORCE_PWR 56 59 — PACK_OPTION=ACE2_GPIO6_PD, PACK_IGNORE=TRUE
RF505 1M 5% 1/20W MF 201 — UART_UPC01_TX 53 56
RF506 100K 5% 1/20W MF 201 — PD_UPC1_MRESET 56
RF502 100K 5% 1/20W MF 201 — PD_UPC1_GPIO5 56

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL
RF503 15K 0.1% 1/20W TF 0201

GND I2C_ADDR PRIMARY ONLY

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

53 PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

79 55 PP5V_S2
79 55 PP5V_S2
CAP FOR PP_5V0 ON VR PAGE

K9 L10 M9 M10 K11 L12 M11 M12 — PP_5V0
N14 M13 — PP_CABLE
G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4 — PP_HV
G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8 — VBUS

UF500
CD3217B12BCE
FCBGA
353S02158
CRITICAL
OMIT_TABLE

		B13	HRESET	
56	PD_UPC1_MRESET	A14	MRESET	
58 52 OUT	ATCRTMR1_RESET_L	B17	RESET*	
53 OUT	UPC1_SER_DBG	A2	GPIO0	
		B1		
53 OUT	PD_UPC1_GPIO1	D1	GPIO1	
56 53 IN	INT_I2C_UPC1_ATCRTMR1_L	F1	GPIO2	
53 OUT	UPC1_5V_EN	C2	GPIO3	
53 52 OUT	ATCRTMR1_FORCE_PWR	E2	GPIO4	
56	PD_UPC1_GPIO5	B3	GPIO5	
59 56 IN	UPC_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL
54 OUT	PD_UPC1_GPIO7	D3	GPIO7	
55 35 OUT	UPC_PMU_RESET_3V3	E4	GPIO8	
54 IN	PD_UPC1_GPIO9	F3	GPIO9	
54 OUT	PD_UPC1_GPIO10	F7	GPIO10	
54	PP3V3_UPC1_LDO	A18	BUSPOWER	
53	NC_UPC1_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
	UPC1_R_OSC	M21	R_OSC	
58 56 53 52 BI	I2C_UPC1_ATCRTMR1_SDA	A16	I2CM_SDA_CNFG	
58 56 53 52 BI	I2C_UPC1_ATCRTMR1_SCL	B15	I2CM_SCL_CNFG	
41 BI	I2C_UPC_SDA	B5	I2C_SDA1	
41 BI	I2C_UPC_SCL	A4	I2C_SCL1	
41 OUT	UPC_I2C_INT_L	D7	I2C_IRQ1*	
43 BI	I2C_SMC_UPC_SDA	B7	I2C_SDA2	
43 BI	I2C_SMC_UPC_SCL	A6	I2C_SCL2	
43 OUT	UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*	
53 OUT	GND	B9	SPI_CLK	
53 OUT	GND	B11	SPI_MOSI	
53 IN	GND	A10	SPI_MISO	
53 OUT	GND	A8	SPI_SSZ	
53 BI	SWD_UPC01_UART_DATA	E20	SWD_DATA	IPU
53 BI	SWD_UPC01_UART_CLK	E16	SWD_CLK	IPU
56 53 IN	UART_UPC01_TX	B19	UART_RX	
53 OUT	UART_UPC01_RX	A20	UART_TX	
59 BI	USB2_UPC1_P1_P	H19	USB_RP1_P	
59 BI	USB2_UPC1_P1_N	H21	USB_RP1_N	
54 BI	PD_UPC1_USBP2_RP	G20	USB_RP2_P	
54 BI	PD_UPC1_USBP2_RN	G22	USB_RP2_N	PORT_MUX
54 BI	PD_UPC1_USBP3_RP	F19	USB_RP3_P	
54 BI	PD_UPC1_USBP3_RN	F21	USB_RP3_N	
52 BI	USBC1_AUXLSX_P	J12	AUX_P	
52 BI	USBC1_AUXLSX_N	H11	AUX_N	
53 OUT	PD_UPC1_HPD	C12	HPD	
54 BI	PD_UPC1_DBG0_R	G12	DEBUG0	
54 BI	PD_UPC1_DBG1_R	F11	DEBUG1	
54 OUT	PD_UPC1_DBG2_R	E8	DEBUG2	
54 BI	PD_UPC1_DBG3_R	E12	DEBUG3	
54 BI	PD_UPC1_DBG4_R	G16	DEBUG4	
54 BI	PD_UPC1_DBG5_R	F15	DEBUG5	
54 IN	PD_UPC1_DBG6_R	D15	DEBUG6	
54 OUT	PD_UPC1_DBG7_R	D19	DEBUG7	

POWER

TYPE-C

GND

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	53
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC1_SS	
LDO_CORE	E22	PP1V5_UPC1_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC1	53
PP_HV_OPT	F5	PPHV_INT1_AONSW	53
C_CC1	M15	USBC1_CC1	
	N16		
C_CC2	M17	USBC1_CC2	
	N18		
RPD_G1	L14	USBC1_CC1	BI 54
RPD_G2	L16	USBC1_CC2	BI 54
C_USB_TP	K19	USBC1_USB_TOP_P	BI 57
C_USB_TN	K21	USBC1_USB_TOP_N	BI 57
C_USB_BP	J20	USBC1_USB_BOT_P	BI 57
C_USB_BN	J22	USBC1_USB_BOT_N	BI 57
C_SBU1	J16	USBC1_SBU1	BI 57
C_SBU2	H15	USBC1_SBU2	BI 57

GND_OPT C18, E18, D17, G18

GND A22 H9 N20 B21 K15 N22

PPVBUS_USBC1 53 57
CF501 1UF 10% 35V X5R 0402

PP3V3_S2_UPC 53 55 78
CF500 10UF 20% 6.3V CERM 0402

PP1V25_S2 53 55 78
CF502 1.0UF 20% 6.3V X5R 0201-1

PP3V3_UPC1_LDO 53 54 56
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
CF508 10UF 20% 6.3V CERM 0402

PP1V8_S2 54 58
CF503 0.1UF 10% 6.3V CERM-X5R 0201

USBC1_3V3LDO_EN 59
(cap needed when used as power source)

PACK_OPTION=ACE2_SS_CAP
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
CF505 10UF 20% 6.3V CERM 0402
CF509 0.68UF 5% 6.3V X6S 0402
PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
BI 54 57

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
BI 54 57

CF514 220PF 5% 50V C0G 0201-1
CF513 220PF 5% 50V C0G 0201-1

BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_ace2 SYNC_DATE=04/24/2020

PAGE TITLE
USB-C: Port Controller ATC1

Apple Inc.

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---- Reference only ----

Left Rear Port

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

PLACE VBUS CAP NEAR EACH VBUS PIN

516S00457
Mates with:
x on y
(NO LANE REVERSALS ALLOWED)

JF600
20875-056E-01
F-ST-SM

TPT_USBC0_PP20V — TP-P4 — TPF600

TPT_USBC1_PP20V — TP-P4 — TPF601

PPVBUS_USBC0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

DF622 TVS2200 WSON — ALLOW_APPLE_PREFIX=D

CRITICAL DZF620 X3-WLB1608-1 SDM2U40CSP

USBC0_CC1 — USBC0_R2D_CR_N<1> — USBC0_R2D_CR_P<1> — USBC0_D2R_N<1> — USBC0_D2R_P<1> — USBC0_SBU2 — USBC0_USB_BOT_N — USBC0_USB_BOT_P

USBC1_USB_BOT_N — USBC1_USB_BOT_P — USBC1_SBU1 — USBC1_R2D_CR_P<2> — USBC1_R2D_CR_N<2> — USBC1_D2R_P<2> — USBC1_D2R_N<2> — USBC1_CC2

USBC0_CC2 — USBC0_R2D_CR_N<2> — USBC0_R2D_CR_P<2> — USBC0_USB_TOP_P — USBC0_USB_TOP_N — USBC0_D2R_CR_N<2> — USBC0_D2R_CR_P<2> — USBC0_SBU1

USBC1_SBU2 — USBC1_R2D_CR_P<1> — USBC1_R2D_CR_N<1> — USBC1_USB_TOP_P — USBC1_USB_TOP_N — USBC1_D2R_CR_P<1> — USBC1_D2R_CR_N<1> — USBC0_CC1

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

PLACE VBUS CAP NEAR EACH VBUS PIN

PPVBUS_USBC1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

CRITICAL DZF600 X3-WLB1608-1 SDM2U40CSP

DF602 TVS2200 WSON — ALLOW_APPLE_PREFIX=D

Left Front Port

Cowling Bosses

860-01443

SHF600 3.10D1.65ID-1.12H-SM — ALLOW_APPLE_PREFIX=SH

SHF601 3.10D1.65ID-1.12H-SM — ALLOW_APPLE_PREFIX=SH

BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_ace2 SYNC_DATE=09/26/2019

PAGE TITLE: USB-C: Connector(s)

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
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BRANCH: evt-1
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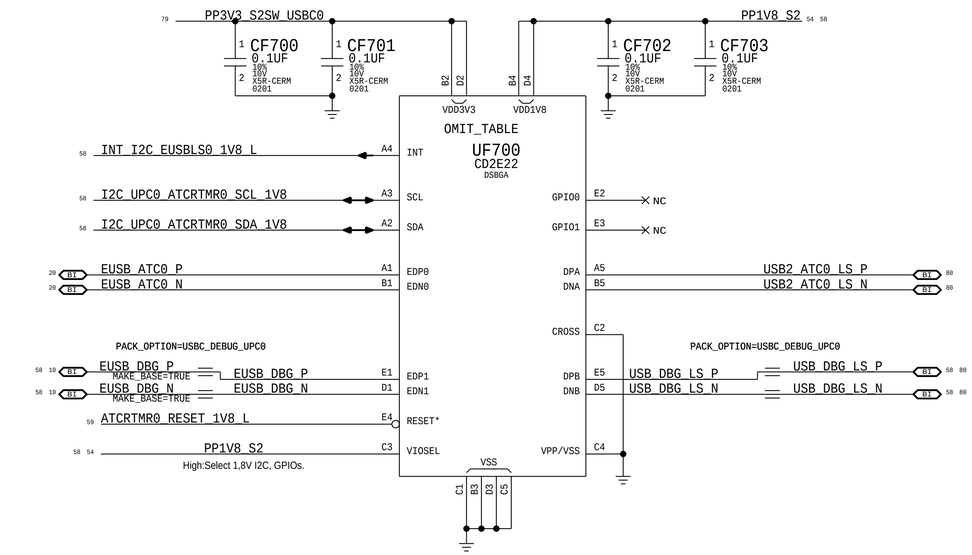
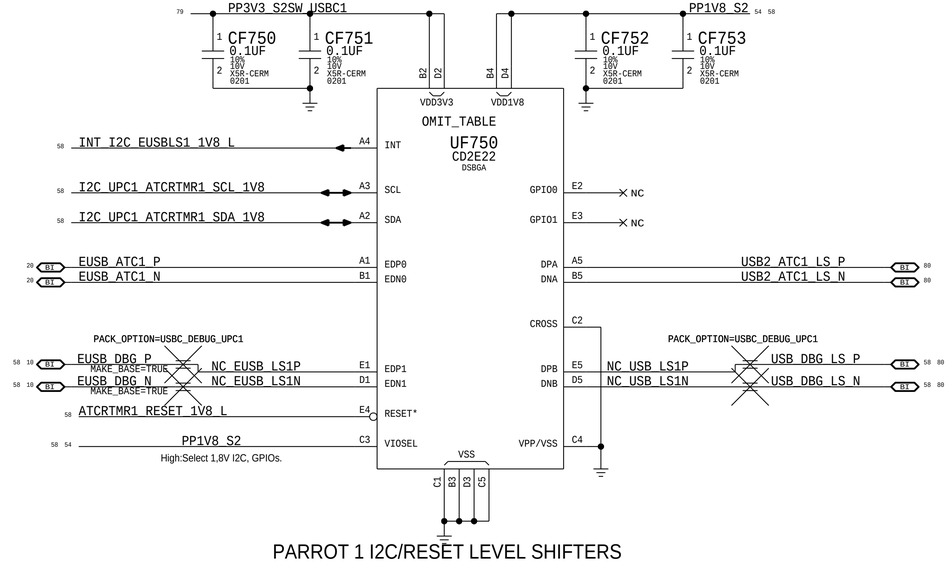
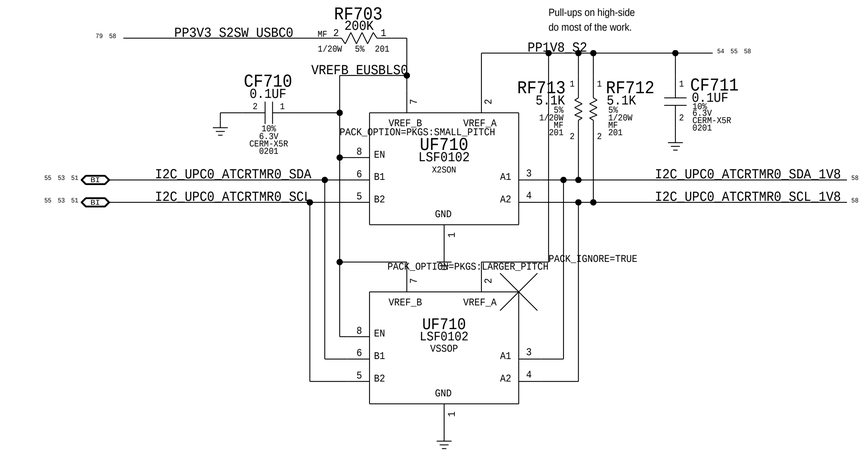
SHEET: 57 OF 92

** OK2INTEGRATE **

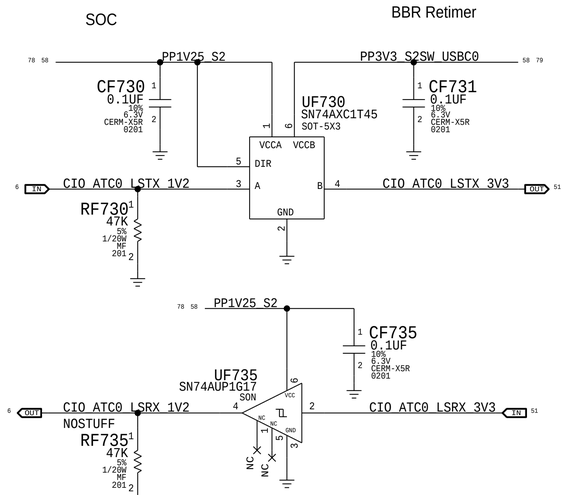




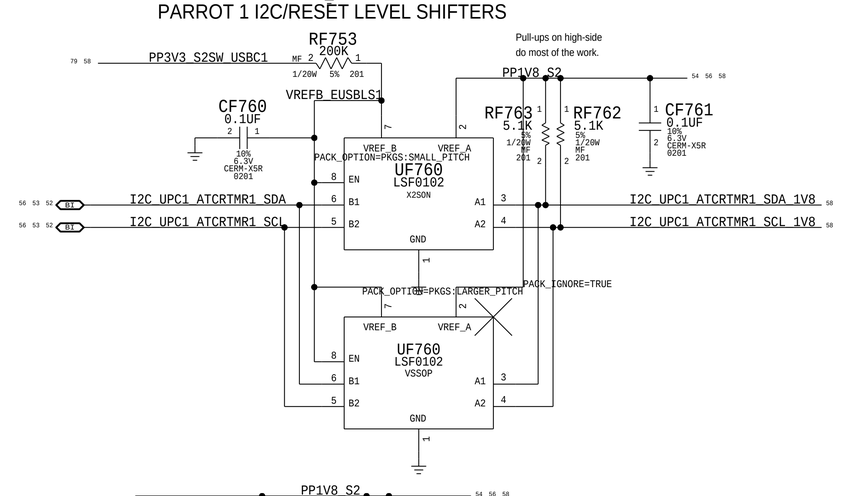
PARROT 0 I2C/RESET LEVEL SHIFTERS

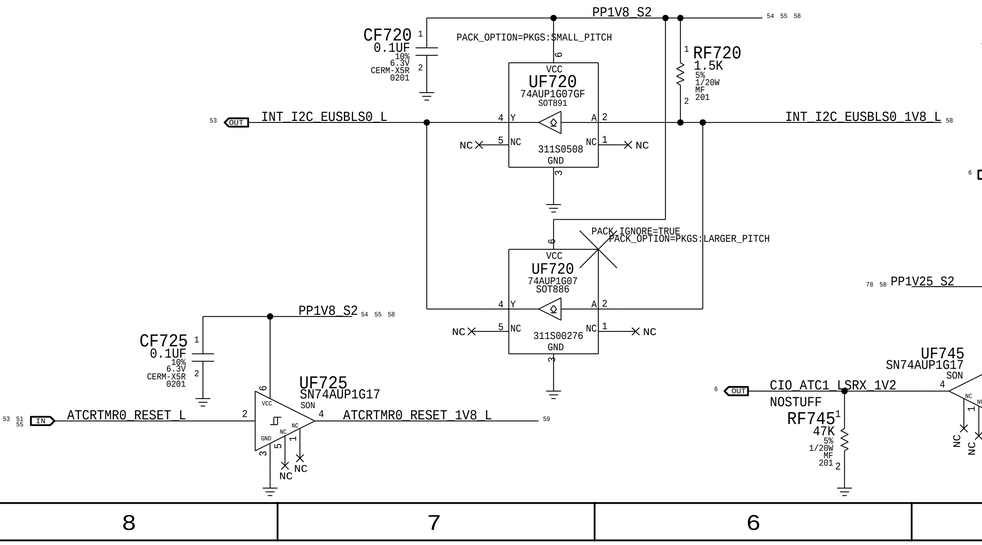


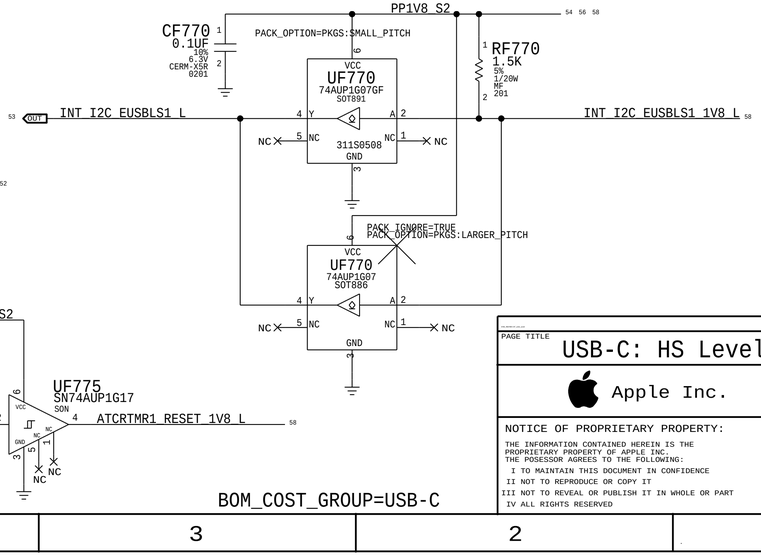
TBT LS RX/TX LEVEL SHIFTERS



PARROT 1 I2C/RESET LEVEL SHIFTERS







BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: HS Level Shifters

Apple Inc.

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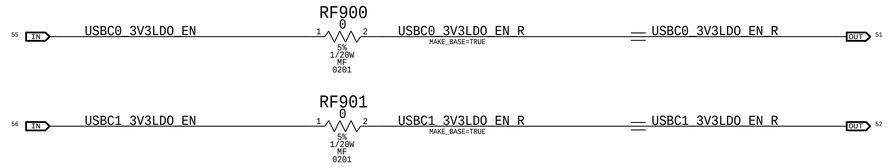
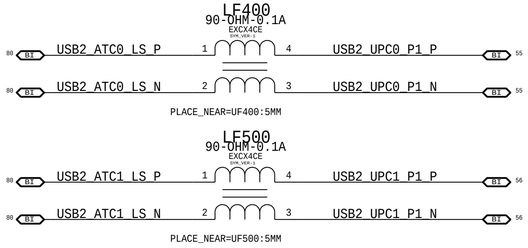
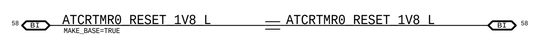
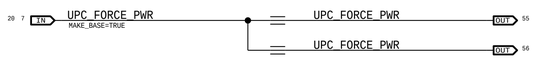




Alias Debug Reset signal to ATC0 Debug Level Shifter (UF700)



Tie ACE2 Pin C4 (GPIO6) together and alias to UPC_FORCE_PWR.



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Project Specific

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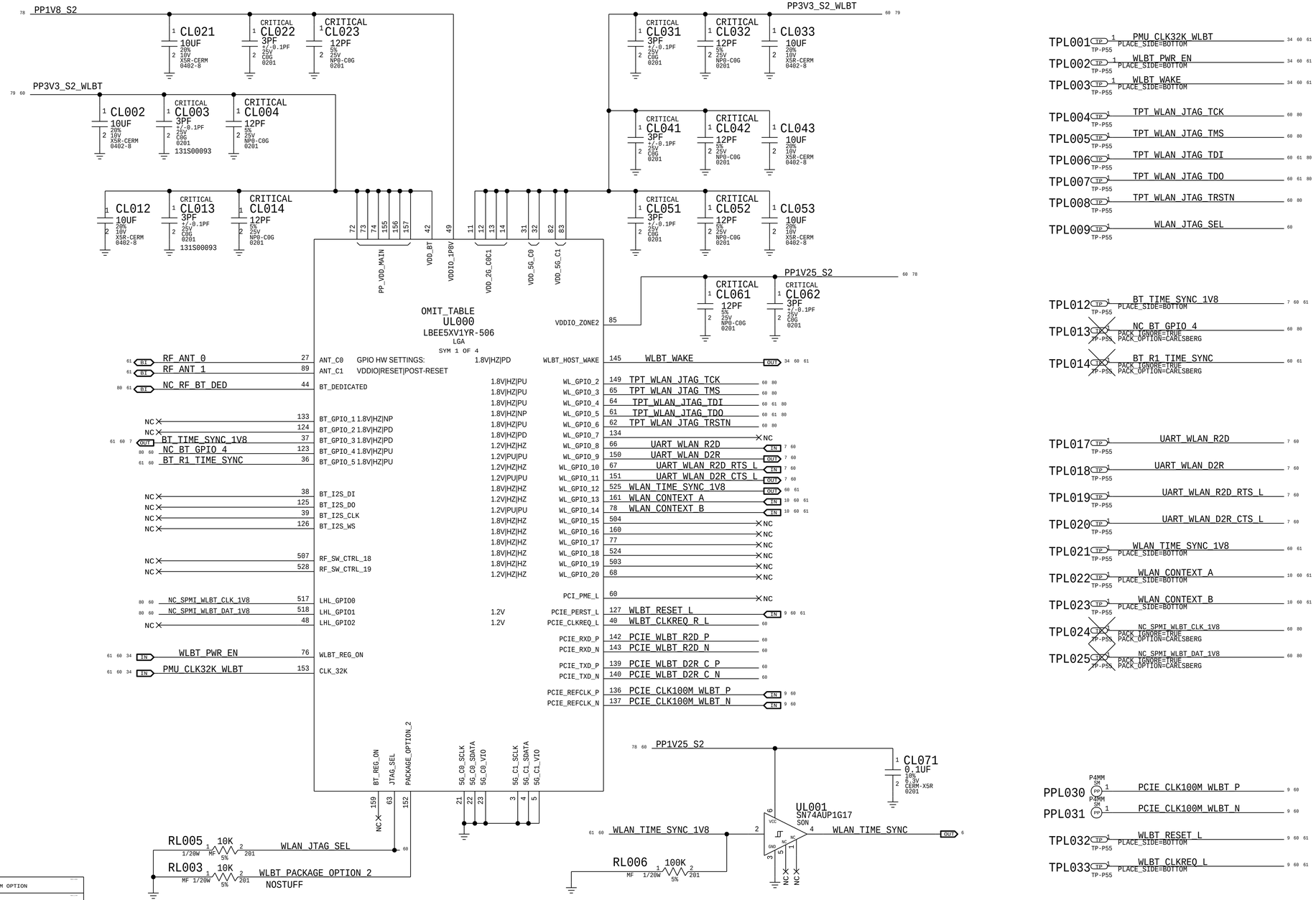
RASPUTIN WIFI/BT MODULE

FOR HOSTINTERFACE TABLES REFER TO:
RDAR://PROBLEM/53187294

FOR DESIGN, DOCUMENTATION,
SYSTEM INTEGRATION QUESTIONS:
RDAR://PROBLEM/44786407



RASPUTIN BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00763	1	MODULE, WLAN BT, RASPUTIN, ES6.11, M, LGA549	UL000	CRITICAL	

RASPUTIN ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00758	339S00763	ANY	UL000	RASPUTIN USI ES6.5

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RASPUTIN WIFI/BT MODULE GND

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 2 OF 4

1			119
2			120
6			121
7			122
8			128
9			129
10			130
15			131
16			132
17			135
18			138
19			141
20			144
24			146
25			147
26			148
28			154
29			158
30			162
33			163
34			164
35			165
41			166
43			167
45			168
46			169
47			170
50			171
51			172
52			173
53			174
54			175
55			176
56			177
57			178
58	GND	GND	179
59			180
69			181
70			182
71			183
75			184
79			185
80			186
81			187
84			188
			189
86			190
87			191
88			192
90			193
91			194
92			195
93			196
94			197
95			198
96			199
97			200
98			201
99			202
100			203
101			204
102			205
103			206
104			207
105			208
106			209
107			210
108			211
109			212
110			213
111			214
112			215
113			216
114			217
115			218
116			219
117			220
118			221

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 3 OF 4

222			303
223			304
224			305
225			306
226			307
227			308
228			309
229			310
230			311
231			312
232			313
233			314
234			315
235			316
236			317
237			318
238			319
239			320
240			321
241			322
242			323
243			324
244			325
245			326
246			327
247			328
248			329
249			330
250			331
251			332
252			333
253			334
254			335
255			336
256			337
257	GND	GND	338
258			339
259			340
260			341
261			342
262			343
263			344
264			345
265			346
266			347
267			348
268			349
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270			351
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272			353
273			354
274			355
275			356
276			357
277			358
278			359
279			360
280			361
281			362
282			363
283			364
284			365
285			366
286			367
287			368
288			369
289			370
290			371
291			372
292			373
293			374
294			375
295			376
296			377
297			378
298			379
299			380
300			381
301			382
302			383

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
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384			463
385			464
386			465
387			466
388			467
389			468
390			469
391			470
392			471
393			472
394			473
395			474
396			475
397			476
398			477
399			478
400			479
401			480
402			481
403			482
404			483
405			484
406			485
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408			487
409			488
410			489
411			490
412			491
413			492
414			493
415			494
416			495
417			496
418			497
419	GND	GND	498
420			499
421			500
422			501
423			502
424			505
425			506
426			508
427			509
428			510
429			511
430			512
431			513
432			514
433			515
434			516
435			519
436			520
437			521
438			522
439			523
440			526
441			527
442			529
443			530
444			531
445			532
446			533
447			534
448			535
449			536
450			537
451			538
452			539
453			540
454			541
455			542
456			543
457			544
458			545
459			546
460			547
461			548
462			549

ANTENNA CONNECTORS

2G_C1
5G_C0
BT_C0

JL100
IR050D15010C
F-ST-SM
1 RF_ANT_0 BI 60 61
2 3 4
PACK_OPTION=SUNWAY

JL100
20449-001E-03
F-ST-SM
1 RF_ANT_0 60 61
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=T664_IPEX

JL110
20449-001E-03
F-ST-SM
1 RF_ANT_0 60 61
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=IPEX

JL120
20431-001E-01
F-ST-SM
2 GND SIGNAL 1 RF_ANT_0 60 61
3 4
PACK_IGNORE=TRUE
PACK_OPTION=ANT_MAC_MINI

2G_C0
5G_C1
BT_C1

JL101
IR050D15010C
F-ST-SM
1 RF_ANT_1 BI 60 61
2 3 4
PACK_OPTION=SUNWAY

JL101
20449-001E-03
F-ST-SM
1 RF_ANT_1 60 61
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=T664_IPEX

JL111
20449-001E-03
F-ST-SM
1 RF_ANT_1 60 61
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=IPEX

JL121
20431-001E-01
F-ST-SM
2 GND SIGNAL 1 RF_ANT_1 60 61
3 4
PACK_IGNORE=TRUE
PACK_OPTION=ANT_MAC_MINI

BT_C0_DED

JL102
20449-001E-03
F-ST-SM
1 61 RF_BT_DED_ANT
2 3 4
PACK_IGNORE=TRUE
PACK_OPTION=T664_IPEX

PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

RL102 1/20W MF 0 5% 0201
1 2
RF_BT_DED_FOUT

CL101 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
1 2
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

CL102 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
1 2
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

UL101
2.4G
0603
1 IN GND OUT 3
2 4
RF_BT_DED_FIN

PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

RL104 1/20W MF 0 5% 0201
1 2
NC_RF_BT_DED BI 60 80

CL103 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
1 2
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

CL105 0.3PF +/-0.1PF 25V C0G-CERM 201 NOSTUFF
1 2
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA

JL122
20431-001E-01
F-ST-SM
2 GND SIGNAL 1 61 RF_BT_DED_ANT
3 4
PACK_IGNORE=TRUE
PACK_OPTION=ANT_MAC_MINI

WLBT DEBUG CONNECTOR

JL103
505070-1222
M-ST-SM

		14	13		
60	WLAN_TIME_SYNC_1V8	2	1	TPT_WLAN_JTAG_TDI	60 80
60 18	WLAN_CONTEXT_A	4	3	TPT_WLAN_JTAG_TDO	60 80
60 18	WLAN_CONTEXT_B	6	5	BT_R1_TIME_SYNC	60
60 34	WLBT_WAKE	8	7	WLBT_CLKREQ_L	9 60
60 34	WLBT_PWR_EN	10	9	BT_TIME_SYNC_1V8	7 60
60 9	WLBT_RESET_L	12	11	PMU_CLK32K_WLBT	34 60
		16	15		

BOMOPTION=WLBT_DBG
PACK_OPTION=WLBT_DBG_CONN

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

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NAND0 S5E0

PP0V88_AWAKE_NAND

CN010 20UF 20% 10V X5R 0402
CN011 20UF 20% 10V X5R 0402
CN012 2.2UF 20% 10V X5R 0201
CN013 2.2UF 20% 10V X5R 0201
CN014 2.2UF 20% 10V X5R 0201
CN015 0.1UF 10% 6.3V CERM-X5R 0201
CN016 0.1UF 10% 6.3V CERM-X5R 0201
CN017 0.1UF 10% 6.3V CERM-X5R 0201

PP1V25_AWAKE_NAND

CN032 20UF 20% 10V X5R 0402
CN030 4.3UF 20% 4V CERM 0402
CN034 2.2UF 20% 10V X5R 0201
CN035 2.2UF 20% 10V X5R 0201
CN036 2.2UF 20% 10V X5R 0201
CN037 2.2UF 20% 10V X5R 0201
CN038 2.2UF 20% 10V X5R 0201
CN039 2.2UF 20% 10V X5R 0201
CN03A 2.2UF 20% 10V X5R 0201

TPT_NAND0_S5E0_ANI1_VREF
TPT_NAND0_S5E0_ANI0_VREF

PP2V5_AWAKE_NAND

CN020 20UF 20% 10V X5R 0402
CN022 2.2UF 20% 10V X5R 0201
CN023 2.2UF 20% 10V X5R 0201
CN024 2.2UF 20% 10V X5R 0201
CN025 2.2UF 20% 10V X5R 0201

PP1V25_AWAKE_NAND

RN010 2 1% 1/20W MF 0201
PLACE_NEAR=UN000.L2:10MM

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V

PP1V2_NAND0_S5E0_AVDD1X_PLL

CN047 2.2UF 20% 10V X5R 0201
CN046 0.1UF 10% 6.3V CERM-X5R 0201

FLN000 10OHM-50%-1A-0.05OHM 0201
PLACE_NEAR=UN000.J6:10MM

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V

PP1V2_NAND0_S5E0_PCI_AVDD_H

CN045 4.7UF 20% 4V CER-X5R 0201
CN044 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0.9V

PP0V9_NAND0_S5E0_VDD_PLL

NC_NAND0_S5E0_VPP

FLN001 10OHM-50%-1A-0.05OHM 0201
PLACE_NEAR=UN000.R4:10MM

PP0V88_AWAKE_NAND
PLACE_NEAR=FLN001.2:5MM

CN083 4.7UF 20% 4V CER-X5R 0201

J6	J8	M9	N6	N8	L2	G12	J4	G6	G8	L6	L8	R6	R8	J2	K9	T5	E10	E2	N2	P9	D3	E12	G4	L12	R2	R4	F3	F5
PCIE_AVDD_H	PCIE_VDD	PCIE_VDD	PCIE_VDD	PCIE_VDD	AVDD1X_PLL	ANI0_VREF	ANI1_VREF	VDD						VDDIO_1				VDDIO_2				VCC				VDD_PLL	VPP	VDP5

OMIT_TABLE

UN000
S5E-MCP-STUDY
LGA

CN085 10PF 5% 25V C0G 0201
RN004 200 0.1% 1/20W TF 0201-1

NAND0_CLK24M_0	M3	CLK_IN	
PCIE_CLK100M_NAND0_0_P	K11	PCIE_REFCLK_P	
PCIE_CLK100M_NAND0_0_N	J12	PCIE_REFCLK_N	
NAND0_CLKREQ0_R_L	P5	PCIE_CLKREQ*	
NAND0_S5E0_PCIE_RESREF	H7	PCIE_RESREF	
PCIE_NAND0_R2D_C_P<0>	CN003 0.22UF	PCIE_NAND0_R2D_P<0>	M11
PCIE_NAND0_R2D_C_N<0>	CN004 0.22UF	PCIE_NAND0_R2D_N<0>	N12
PCIE_NAND0_D2R_P<0>	CN001 0.22UF	PCIE_NAND0_D2R_C_P<0>	R12
PCIE_NAND0_D2R_N<0>	CN002 0.22UF	PCIE_NAND0_D2R_C_N<0>	T11
		PCIE_RX0_P	M11
		PCIE_RX0_N	N12
		PCIE_TX0_P	R12
		PCIE_TX0_N	T11

GND_VOID=TRUE
10% 6.3V X5R-CERM 0201

NAND0_RESET_L	L4	RESET*	
NAND0_JTAG_TRST_L	G10	TRST*	
NAND0_S5E0_ZQ_0	C10	ZQ_0	
NAND0_S5E0_ZQ_1	K3	ZQ_1	

RN006 300 1% 1/20W MF 201
PLACE_NEAR=UN000.C10:15MM

RN005 300 1% 1/20W MF 201
PLACE_NEAR=UN000.K3:15MM

EXT_D0/BOOT0	B3	NAND0_LPB_L	IN
EXT_D1/BOOT1	C4	NAND_BFH	IN
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND0_BOOT2	
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND0_S5E0_SWD_UID0	
EXT_D4/SPI_CS	B7		
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND0_S5E0_SWD_UID1	
EXT_D6/BOOT3	B9		
EXT_D7/SPF	B11	NAND0_PFN_L	IN
EXT_DQS/BCM*	D11	NAND0_BCM_L	IN
EXT_NCE/PERST*	E8	NAND0_PCIE_RESET_L	IN
EXT_NRE/JTAG_TMS	D7	SWD_NAND0_SWDIO	IN
EXT_NWE/JTAG_TCK	E6	SWD_NAND0_SWCLK	IN
EXT_RNB/JTAG_TDO	E4	NAND0_S5E0_JTAG_TDO	OUT
EXT_CLE/JTAG_TDI	D5	TPT_NAND0_S5E0_JTAG_TDI	IN
EXT_ALE/JTAG_SEL	D9	NAND0_JTAG_SEL	IN
DROOP*	T3	TPT_NAND0_S5E0_DROOP_L	
WP*	G2	NAND0_WP_L	IN

A12	A2	B1	B13	C12	C2	D1	D13	F1	F11	F13	F7	F9	H1	H11	H13	H3	H5	H9	J10	K1	K13	K5	K7	L10	M1	M13	M5	M7	N10	N4	P1	P11	P13	P3	P7	R10	T1	T13	T7	T9	U12	U2	A10	A4	A6	A8	U10	U4	U6	U8
VSS																																										VSS_R								

NAND0_BOOT2
NAND0_JTAG_SEL
NAND0_JTAG_TRST_L

RN000 47K 1% 1/20W MF 201
RN002 47K 1% 1/20W MF 201
RN021 0 5% 1/20W MF 0201

Spec recommends to tie Boot2 directly to Gnd

PP1V25_AWAKE_NAND

RN001 0 5% 1/20W MF 0201
RN007 0 5% 1/20W MF 0201

NAND0_BCM_L
NAND0_WP_L

Spec recommends to tie BCM, WP directly to 1.2V rail

NAND0_S5E0_SWD_UID0
NAND0_S5E0_SWD_UID1

RN009 47K 1% 1/20W MF 201
RN008 47K 1% 1/20W MF 201

BOM_COST_GROUP=SSD

SYNC_MASTER=ref_storage_s5e
SYNC_DATE=05/02/2020

PAGE TITLE: STORAGE: SSD0 S5E <0>

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*** OK2INTEGRATE ***

NAND0 S5E1

PP0V88_AWAKE_NAND

SSD_2L CN110 20UF 20% 10V X5R 0402
SSD_2L CN111 20UF 20% 10V X5R 0402
SSD_2L CN112 2.2UF 20% 10V X5R 0201
SSD_2L CN113 2.2UF 20% 10V X5R 0201
SSD_2L CN114 2.2UF 20% 10V X5R 0201
SSD_2L CN115 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN116 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN117 0.1UF 10% 6.3V CERM-X5R 0201

PP1V25_AWAKE_NAND

SSD_2L CN132 20UF 20% 10V X5R 0402
SSD_2L CN130 4.3UF 20% 4V CERM 0402
SSD_2L CN134 2.2UF 20% 10V X5R 0201
SSD_2L CN135 2.2UF 20% 10V X5R 0201
SSD_2L CN136 2.2UF 20% 10V X5R 0201
SSD_2L CN137 2.2UF 20% 10V X5R 0201
SSD_2L CN138 2.2UF 20% 10V X5R 0201
SSD_2L CN139 2.2UF 20% 10V X5R 0201
SSD_2L CN13A 2.2UF 20% 10V X5R 0201

TPT_NAND0_S5E1_ANI1_VREF
TPT_NAND0_S5E1_ANI0_VREF

PP2V5_AWAKE_NAND

SSD_2L CN120 20UF 20% 10V X5R 0402
SSD_2L CN122 2.2UF 20% 10V X5R 0201
SSD_2L CN123 2.2UF 20% 10V X5R 0201
SSD_2L CN124 2.2UF 20% 10V X5R 0201
SSD_2L CN125 2.2UF 20% 10V X5R 0201

PP1V25_AWAKE_NAND
SSD_2L RN110 2 1% 1/20W MF 0201
PLACE_NEAR=UN100.L2:10MM

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V

SSD_2L CN147 2.2UF 20% 10V X5R 0201
SSD_2L CN146 0.1UF 10% 6.3V CERM-X5R 0201

PP1V2_NAND0_S5E1_AVDD1X_PLL

SSD_2L FLN100 10OHM-50%-1A-0.05OHM 0201
PLACE_NEAR=UN100.J6:10MM

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V

SSD_2L CN145 4.7UF 20% 6.3V CER-X5R 0201
SSD_2L CN144 0.1UF 10% 6.3V CERM-X5R 0201

PP1V2_NAND0_S5E1_PCI_AVDD_H

MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0.9V

PP0V9_NAND0_S5E1_VDD_PLL

SSD_2L FLN101 10OHM-50%-1A-0.05OHM 0201
PLACE_NEAR=UN100.R4:10MM

PP0V88_AWAKE_NAND
PLACE_NEAR=FLN101.2:5MM
SSD_2L CN183 4.7UF 20% 4V CER-X5R 0201

NC_NAND0_S5E1_VPP

The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

J6 PCIE_AVDD_H
J8 M9 N6 N8 PCIE_VDD
L2 PCIE_VDD
G12 PCIE_VDD
AVDD1X_PLL
J4 ANI0_VREF
ANI1_VREF
G6 G8 L6 L8 R6 R8 VDD
J2 VDDIO_1
K9 T5 E10 VDDIO_2
E2 N2 P9
D3 E12 G4 L12 R2 VCC
R4 VDD_PLL
F3 VPP
F5 VDP5

SSD_2L CN185 10PF 5% 25V C0G 0201
SSD_2L RN104 200 0.1% 1/20W TF 0201-1

NAND0_CLK24M_1	M3	CLK_IN	
PCIE_CLK100M_NAND0_1_P	K11	PCIE_REFCLK_P	
PCIE_CLK100M_NAND0_1_N	J12	PCIE_REFCLK_N	
NAND0_CLKREQ1_R_L	P5	PCIE_CLKREQ*	
NAND0_S5E1_PCIE_RESREF	H7	PCIE_RESREF	
PCIE_NAND0_R2D_C_P<1>	M11	PCIE_RX0_P	
PCIE_NAND0_R2D_C_N<1>	N12	PCIE_RX0_N	
PCIE_NAND0_D2R_P<1>	R12	PCIE_TX0_P	
PCIE_NAND0_D2R_N<1>	T11	PCIE_TX0_N	
NAND0_RESET_L	L4	RESET*	
NAND0_JTAG_TRST_L	G10	TRST*	
NAND0_S5E1_ZQ_0	C10	ZQ_0	
NAND0_S5E1_ZQ_1	K3	ZQ_1	

SSD_2L CN103 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE
SSD_2L CN104 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE
SSD_2L CN101 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE
SSD_2L CN102 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE

PLACE_NEAR=UN100.C10:15MM
SSD_2L RN106 300 1% 1/20W MF 201

PLACE_NEAR=UN100.K3:15MM
SSD_2L RN105 300 1% 1/20W MF 201

OMIT_TABLE

UN100
S5E-MCP-STUDY
LGA

EXT_D0/BOOT0	B3	NAND0_LPB_L	IN 34 62
EXT_D1/BOOT1	C4	NAND_BFH	IN 7 62
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND0_BOOT2	62
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND0_S5E1_SWD_UID0	63
EXT_D4/SPI_CS	B7		
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND0_S5E1_SWD_UID1	63
EXT_D6/BOOT3	B9		
EXT_D7/SPF	B11	NAND0_PFN_L	IN 62 65
EXT_DQS/BCM*	D11	NAND0_BCM_L	IN 62
EXT_NCE/PERST*	E8	NAND0_PCIE_RESET_L	IN 9 62
EXT_NRE/JTAG_TMS	D7	SWD_NAND0_SWDIO	IN 20
EXT_NWE/JTAG_TCK	E6	SWD_NAND0_SWCLK	IN 20
EXT_RNB/JTAG_TDO	E4	TPT_NAND0_S5E1_JTAG_TDO	OUT 65
EXT_CLE/JTAG_TDI	D5	NAND0_S5E0_JTAG_TDO	IN 62
EXT_ALE/JTAG_SEL	D9	NAND0_JTAG_SEL	IN 62
DROOP*	T3	TPT_NAND0_S5E1_DROOP_L	65
WP*	G2	NAND0_WP_L	IN 62

A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2 — VSS
A10 A4 A6 A8 U10 U4 U6 U8 — VSS_R

PP1V25_AWAKE_NAND
SSD_2L RN108 47K 1% 1/20W MF 201
NAND0_S5E1_SWD_UID0

NAND0_S5E1_SWD_UID1
SSD_2L RN109 47K 1% 1/20W MF 201

BOM_COST_GROUP=SSD

SYNC_MASTER=ref_storage_s5e
SYNC_DATE=05/02/2020
PAGE TITLE
STORAGE: SSD0 S5E <1>

Apple Inc.

DRAWING NUMBER 051-05392
SIZE D
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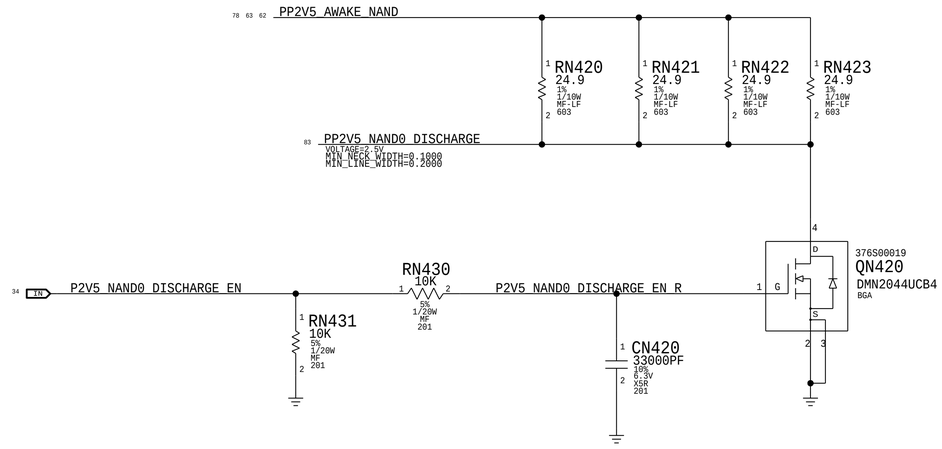
OK2INTEGRATE

THIS EXTERNAL NAND VCC DISCHARGE CIRCUITRY IS FOR SYSTEM THAT DOES NOT USE OCARINA



SYNC_MASTER=evt_storage_non_ocarina_support SYNC_DATE=02/17/2020

PAGE TITLE
STORAGE: NON OCARINA SUPPORT

Apple Inc.

DRAWING NUMBER 051-05392
SIZE D
REVISION 4.0.0
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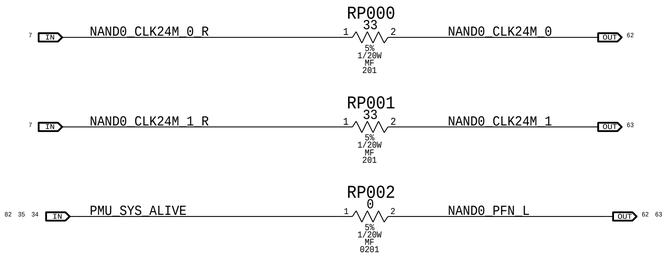
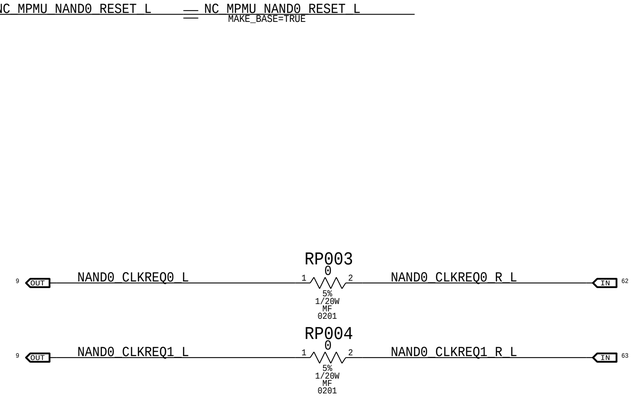
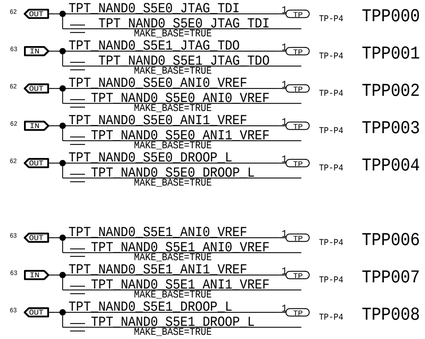
SSD 24M CLOCK TERMINATIONS

TOPOLOGY TBD







BOM_COST_GROUP=SSD

SYNC_MASTER=T668 SYNC_DATE=08/01/2019

PAGE TITLE

STORAGE: SSD Support

Apple Inc.

DRAWING NUMBER 051-05392

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REVISION 4.0.0

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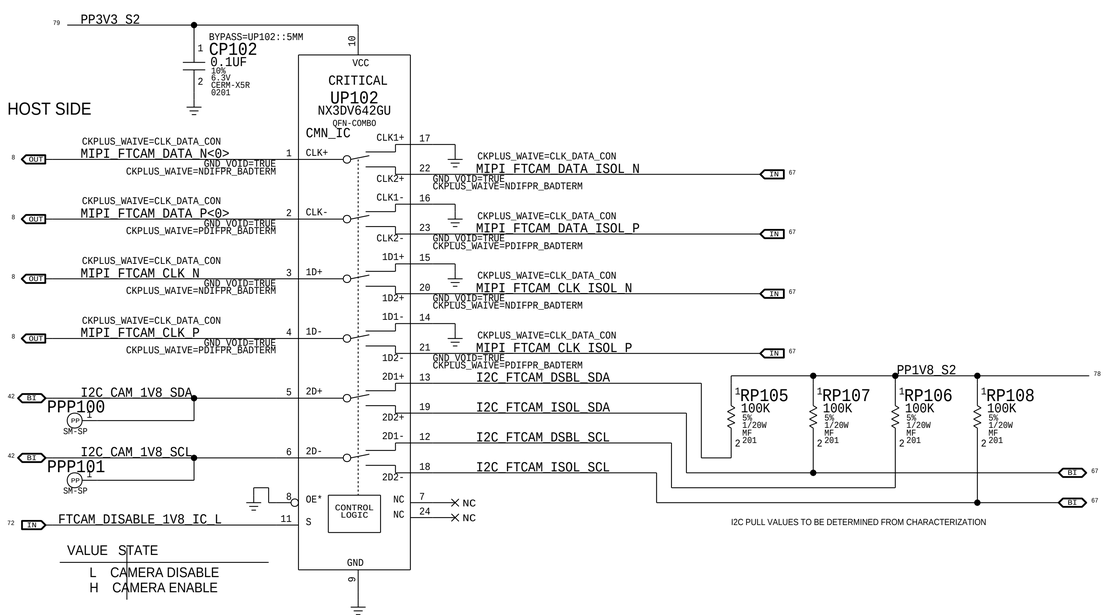
*** OK2INTEGRATE ***

CAMERA SECURE DISABLE



VALUE	STATE
L	CAMERA DISABLE
H	CAMERA ENABLE

BOM_COST_GROUP=SECURITY

PAGE TITLE
SECDIS: MIPI MUX

Apple Inc.

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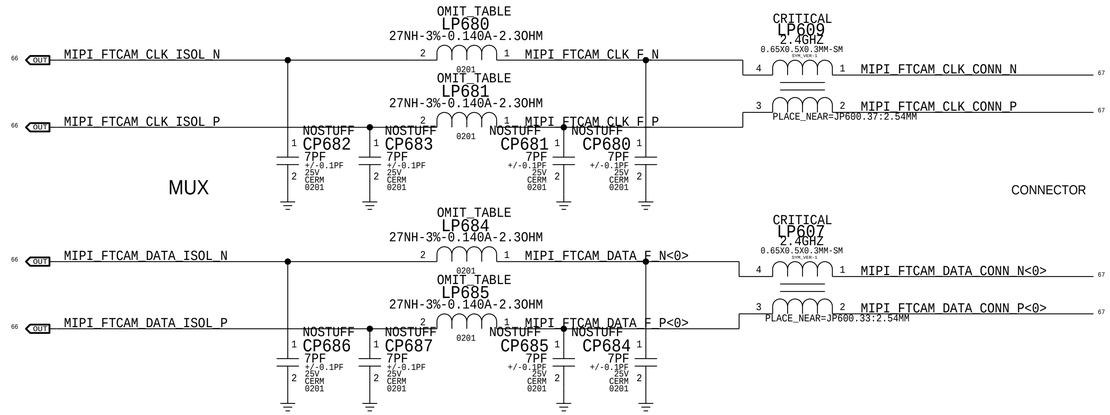
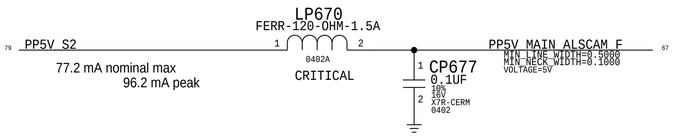
LCD PANEL INTERFACE (eDP) + Camera (MIPI)

A MIPI Clock and Data

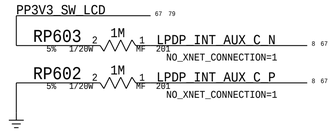
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0201	4	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	LP680,LP681,LP684,LP685		



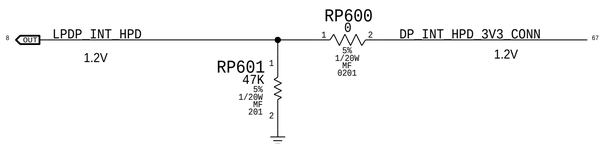
B ALS & Camera 5V Filter



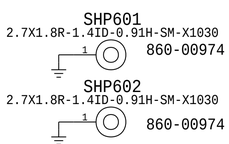
C LCD Panel AUX Straps



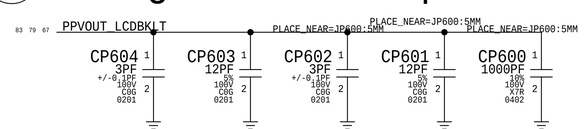
D TCON HPD Voltage Divider



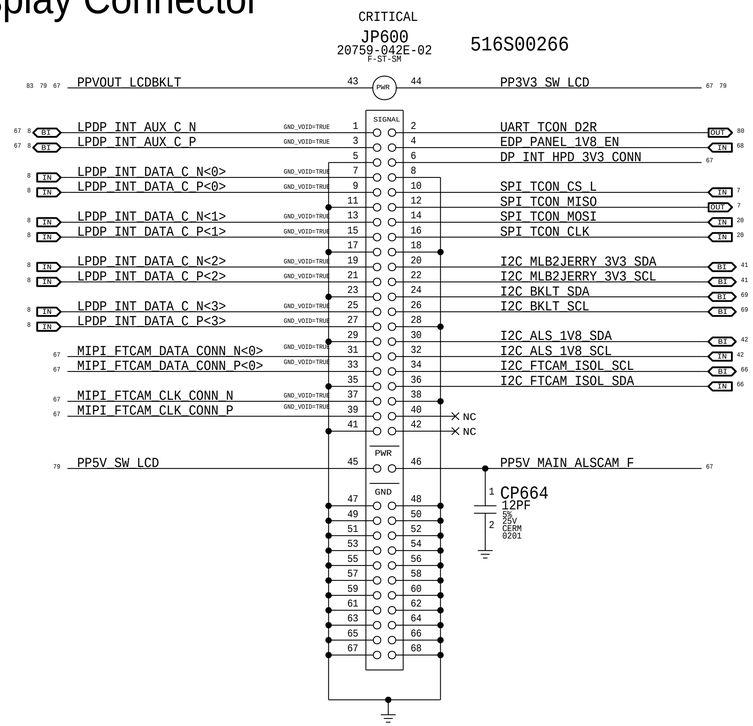
E Cowling Bosses



F Backlight Desense Capacitors



G eDP Display Connector



BOM_COST_GROUP=DISPLAY

SYNC_MASTER=tga_140	SYNC_DATE=05/31/2019
PAGE TITLE	eDP Display Connector
Apple Inc.	DRAWING NUMBER 051-05392 · SIZE D
	REVISION 4.0.0
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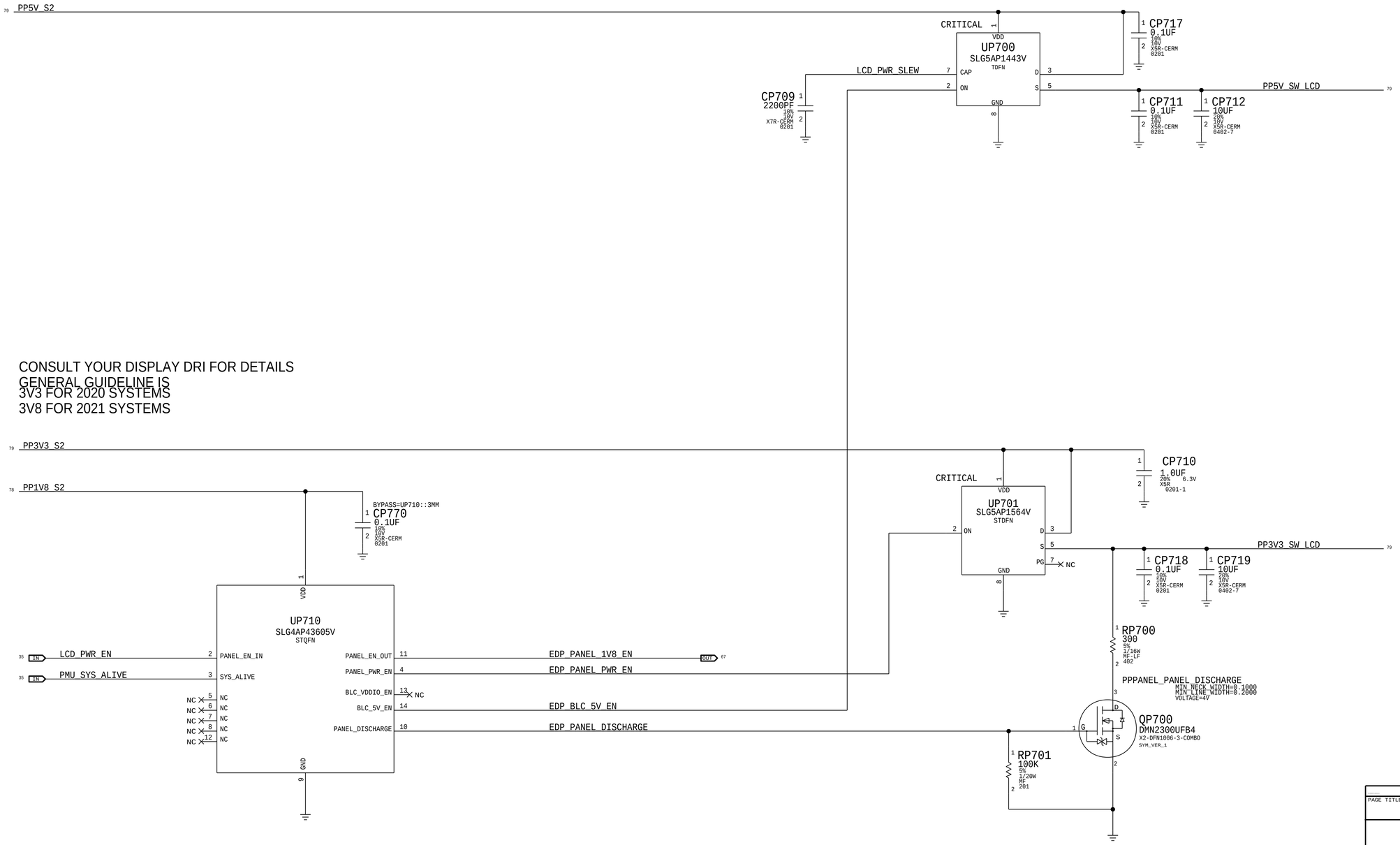
*** OK2INTEGRATE ***



CONSULT YOUR DISPLAY DRI FOR DETAILS
GENERAL GUIDELINE IS
3V3 FOR 2020 SYSTEMS
3V8 FOR 2021 SYSTEMS

BOM_COST_GROUP=DISPLAY

PAGE TITLE
DISPLAY POWER SEQUENCER

Apple Inc.

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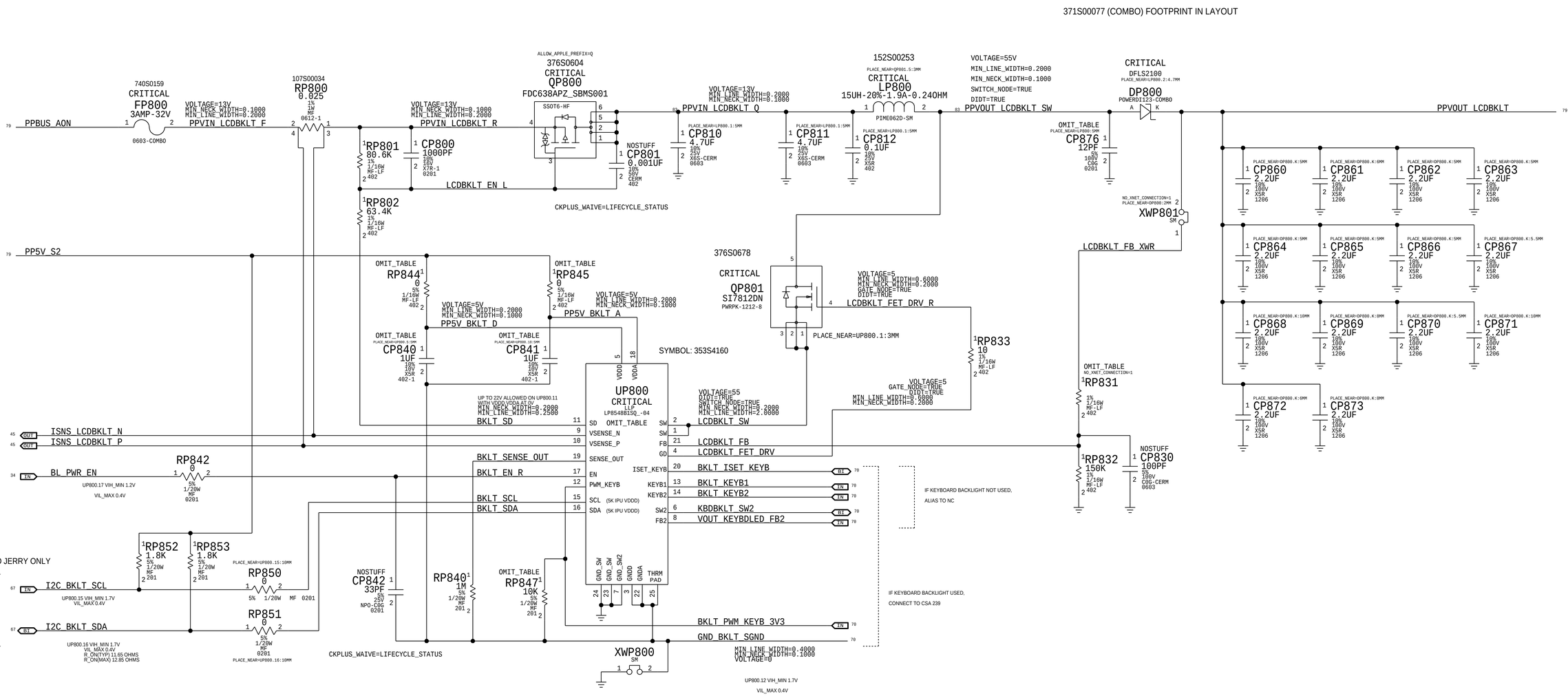
*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER



BEN IC VERSION TO MATCH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4160	1	IC,LP8548B1-04,DC/DC CVTR,BOOST,QFN-24	UP800		BLC_BEN_IC:V4
353S02256	1	IC,LP8548B1A-07,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V7

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (J132, J213)
100K IF KEYBOARD PWM INPUT IS PRESENT (J152)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0007	1	RES,MF,1/20W,10K OHM,5,0201,SMD	RP847		BLC_KBD_BOOST_USED:NO
118S0014	1	RES,MF,100KOHM,1,1/20W,0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0339	1	RES,MTL FILM,1/16W,18.2K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:16
114S0359	1	RES,MTL FILM,1/16W,28.7K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR://50682942>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	RP844,RP845		BLC_5V_SERIES:0_OHM
114S0023	2	RES,MTL FILM,1/16W,10 OHM,1,0402,SMD,LF	RP844,RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=ref_blc_ben SYNC_DATE=11/20/2019

PAGE TITLE
BEN: CONTROLLER

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
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BRANCH evt-1
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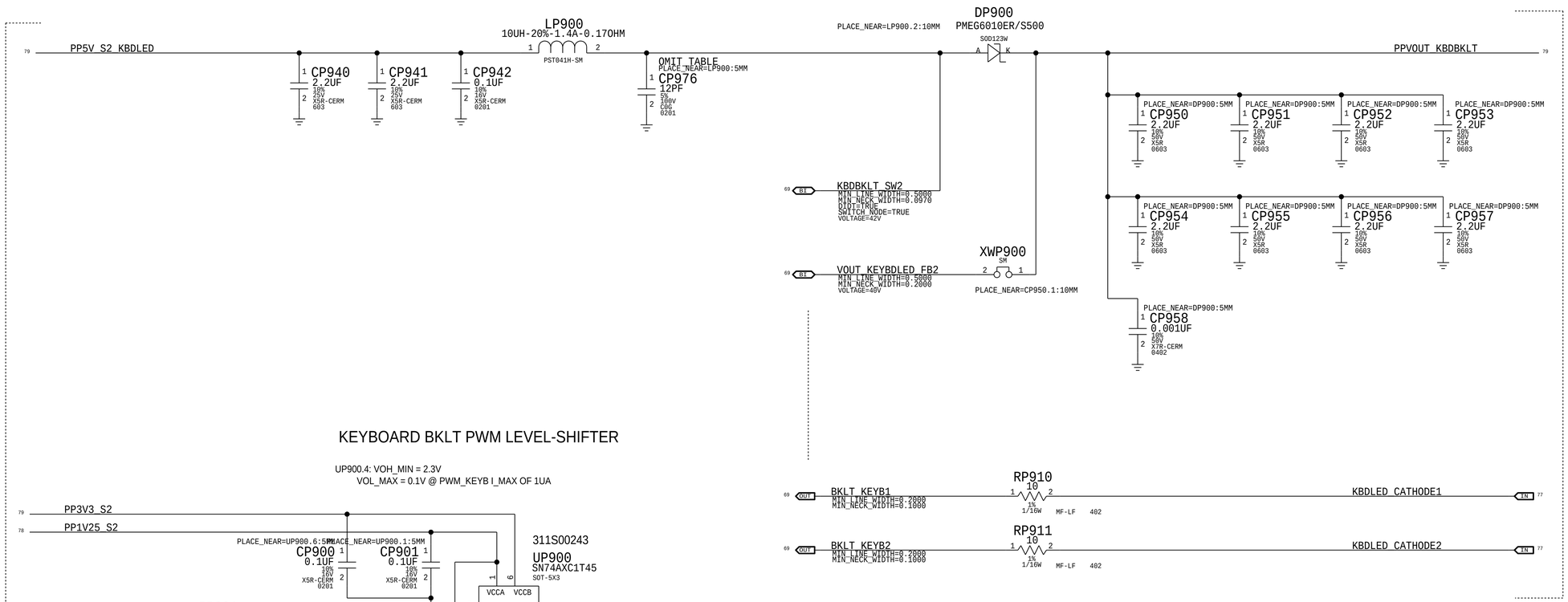
*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

THIS PAGE IS ONLY TO BE INCLUDED IF THE KEYBOARD BACKLIGHT
IS CONTROLLED BY THE BEN ON PAGE 238

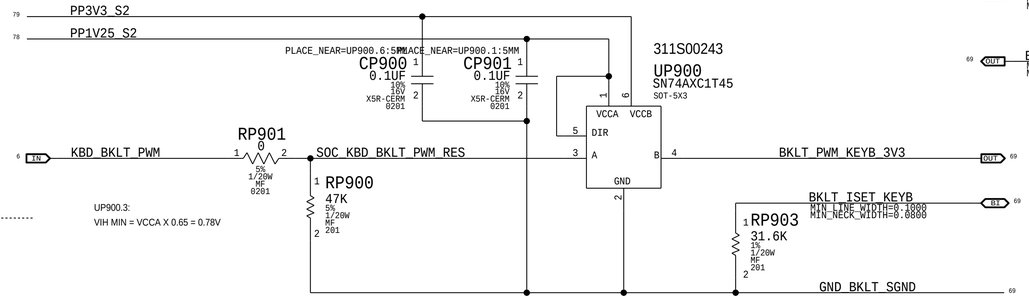
KEYBOARD BACKLIGHT
POWER & CONTROL
SIGNALS FROM
SYSTEM



KEYBOARD BACKLIGHT
CONNECTOR SIGNALS

KEYBOARD BKLT PWM LEVEL-SHIFTER

UP900.4: VOH_MIN = 2.3V
VOL_MAX = 0.1V @ PWM_KEYB I_MAX OF 1UA



UP900.3:
VIH MIN = VCCA X 0.65 = 0.78V

OFF=PAGE SIGNALS ON THIS VERTICAL LINE CONNECT TO BEN UP800
ON PAGE 238

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP976		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=ref_blc_ben SYNC_DATE=11/20/2019

PAGE TITLE: BEN: KEYBOARD

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
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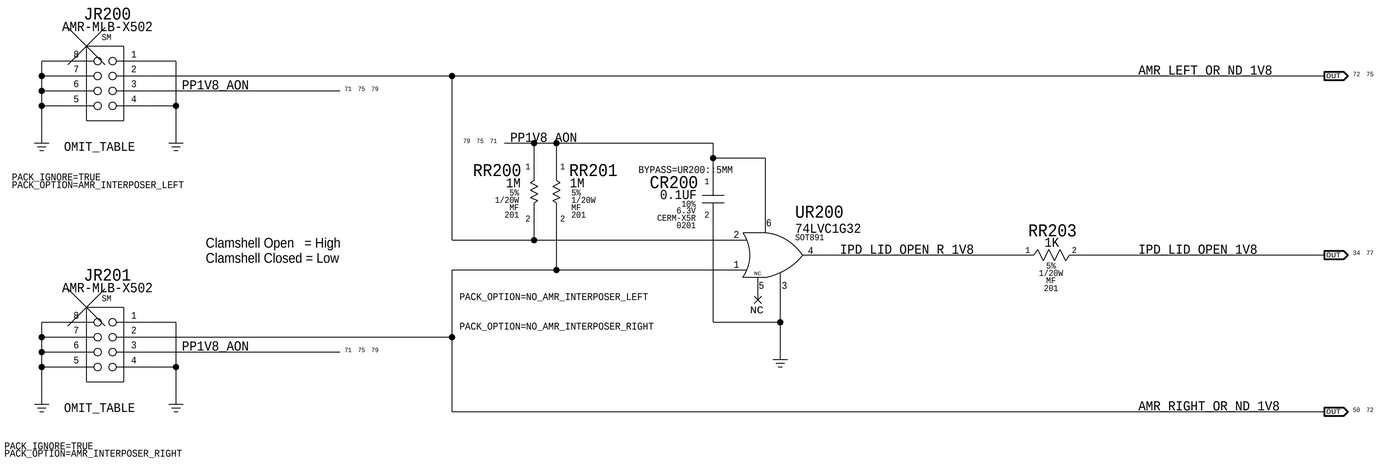
*** OK2INTEGRATE ***

Lid Detect Sensors



BOM_COST_GROUP=SYSTEM

SYNC_MASTER=ref_secdis_amr SYNC_DATE=10/21/2019

PAGE TITLE

SECDIS: AMR

Apple Inc.

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REVISION 4.0.0

BRANCH evt-1

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*** OK2INTEGRATE ***

UNLESS 1V8 IS NOTED, SIGNALS ARE 1.2V

CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	0.8MA	33MA
1.8 S2	0.8MA	14MA

SUPER IMPORTANT PACK OPTIONS:

NOTES ARE ON CSA 2 OF THE REFERENCE DESIGN
READ, LEARN, IMPLEMENT

FTCAM_DISABLE_L — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
NC_IRCAM_ENABLE_IN_IC — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
DMIC_DISABLE_L — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
NC_DMIC_DATA2_SEC_OUT_IC — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
PMU_RESET_L — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS_NOTMIPI
FTCAM_RESET_L — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS_NOTMIPI
PDM_DMIC_DATA4 — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
PDM_DMIC_DATA3 — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
NC_SEP_IRCAM_DISABLE_IC_L — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
LID_OPEN — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
DISABLE_STROBE — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS
PDM_DMIC_CLK4 — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS

RR313 1K 5% 1/20W MF 201

CKPLUS_WAIVE=TERMSHORTED
PACK_IGNORE=TRUE
PACK_OPTION=DEV_SECDIS
ROOM=SECURE_DISABLE
RR300 0 5% 1/20W MF 0201
PACK_OPTION=PROD_SECDIS

ROOM=SECURE_DISABLE
RR301 10 5% 1/20W MF 201
DMIC_CLK1_1V8_OUT — OMIT_TABLE — PLACE_NEAR=UR300.C6:15MM

ROOM=SECURE_DISABLE
RR302 10 5% 1/20W MF 201
DMIC_CLK0_1V8_OUT — OMIT_TABLE — PLACE_NEAR=UR300.E6:15MM

CKPLUS_WAIVE=TERMSHORTED
PACK_IGNORE=TRUE
PACK_OPTION=DEV_SECDIS
ROOM=SECURE_DISABLE
RR303 0 5% 1/20W MF 0201
PDM_DMIC_CLK3 — MAKE_BASE=TRUE — PACK_OPTION=PROD_SECDIS

PP1V8_S2
PP1V2_S2
ROOM=SECURE_DISABLE

UR300
LCMXO2-2000ZE-1UWAP9
WLCSP

PB3A (IPD)*	E7	PT10A	D5 — NC
PB3B (IPD)	F7	PT10B	D4
NC — PB5A/CSSPIN	G7	PT12C/TDO	A6 — SECDIS_TDO_IC
PB8A/MCLK/CCLK (IPD)*	F6	PT12D/TDI	C5 — PP1V8_S2
PB8B/SO/SPISO	F5	PT16C/TCK	B4 — GND
PB11A/PCLKT2_0	E4	PT16D/TMS	B5 — PP1V8_S2
PB11B/PCLKC2_0 (IPD)	E3	PT17A/PCLKT0_1 (IPD)	C4 — MGL_1V8
PB16A/PCLKT2_1	G4	PT17B/PCLKC0_1 (IPD)	D3 — AMR_RIGHT_OR_ND_1V8
PB16B/PCLKC2_1	G3	PT18C/SCL/PCLKT0_0	B3 — CLK_2MHZ_SECDIS_1V8
PB12A	F4	PT18D/SDA/PCLKC0_0	C3 — NC_DMIC_CLK2_1V8_OUT_R_IC
PB12B (IPD)	F3	PT20A	A3 — DMIC_CLK_ENABLE
		PT20B	B2 — NC_IRCAM_ENABLE_SEC_1V8_OUT_IC
SECDIS_SN_TIE_OFF — PB25A/SN	G2		
NC — PB25B/SI_SISPI	G1	PT20C/JTAGENB	F2 — NC_FTCAM_ENABLE_SEC_1V8_OUT_IC
NC — PL2A/L_GPLLT_IN	A7	PT20D/PROGRAMN	F1 — NC
PL2B/L_GPLLC_IN (IPD)*	B6	PT23A	E2 — DMIC_DATA0_1V8_IN
PL3A/PCLKT5_0 (IPD)*	C7	PT23B	C2 — DMIC_DATA1_1V8_IN
PL3B/PCLKC5_0	C6	PT24A	C1 — FTCAM_DISABLE_1V8_IC_L
PL5A	E6	PT24B (IPD)	D2 — NC_DMIC_DATA2_1V8_IN_IC
PL5B (IPD)*	E5	PT24C/INITN	B1 — AMR_LEFT_OR_ND_1V8
		PT24D/DONE — NC	A1

VCCIO8 A2, VCCIO8 A5, VCCIO2 G6, VCCIO5 B7, VCC D1, VCC D7, GND A4, GND D6, GND E1, GND G5

FTCAM_DISABLE_L
DMIC_DISABLE_L
NC_FTCAM_ENABLE_IN
PDM_DMIC_DATA4 — CKPLUS_WAIVE=CLK_DATA_CON
PDM_DMIC_DATA3 — CKPLUS_WAIVE=CLK_DATA_CON
SMC_LID_OPEN_R
SECDIS_SN_TIE_OFF
DISABLE_STROBE
PDM_DMIC_CLK4 — CKPLUS_WAIVE=SYNOVK_CHECK
DMIC_CLK1_1V8_OUT_R — CKPLUS_WAIVE=SYNOVK_CHECK
DMIC_CLK0_1V8_OUT_R
PDM_DMIC_CLK3 — CKPLUS_WAIVE=SYNOVK_CHECK

RR310 47K 1% 1/20W MF 201 — PACK_OPTION=PROTO_PULLDOWN_SECDIS
RR311 47K 1% 1/20W MF 201 — PACK_OPTION=PROTO_PULLDOWN_SECDIS
RR312 47K 1% 1/20W MF 201 — PACK_OPTION=PROTO_PULLDOWN_SECDIS

PINS MARKED (IPD)* ONLY HAVE INTERNAL PULLDOWNS IN THE SECDIS_EVT VERSION OF THE PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
336S00038	1	IC,PLD,MACHXO2,2112 LUT,1.2V,ANN,WLCSP49	UR300	SECDIS_PROTO
336S00039	1	IC,PLD,MACHXO2,2112 LUT,1.2V,APS,WLCSP49	UR300	SECDIS_EVT
336S00041	1	IC,PLD,MACHXO2,2112 LUT,1.2V,XXX,WLCSP49	UR300	SECDIS_EXT_CLK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0004	2	RES,MF,1/20W,10 OHM,5,0201,SMD	RR301,RR302	DMIC_CLK_10OHM
117S0080	2	RES,MF,1/20W,33 OHM,5,0201,SMD	RR301,RR302	DMIC_CLK_33OHM

PP1V8_S2 — CR306 0.1UF 10% 6.3V CERM-X5R 0201 — ROOM=SECURE_DISABLE, BYPASS=UR301.1::5MM

UR301 SLG4AP44010 STQFN
NC, NC, NC, NC, NC, NC
CLK_2MHZ — CLK_2MHZ_SECDIS_1V8_R — RR314 10 5% 1/20W MF 201 — ROOM=SECURE_DISABLE — PLACE_NEAR=UR301.7:15MM
VDD, GND

JTAG SIGNALS ARE 1.8V
INPUTS ARE HARD-TIED TO RAILS IN POR DESIGNS
THE OUTPUT (TDO) IS NC'D IN POR DESIGNS

RR309 10 1% 1/20W MF 201 — ROOM=SECURE_DISABLE — PLACE_NEAR=UR300.C3:15MM
DMIC_CLK2_1V8_OUT_IC — PACK_IGNORE=TRUE, PACK_OPTION=PROD_SECDIS_3DMIC

JTAG FOR DEV & PROTO0 BOARDS ONLY

JR300 505070-1222 M-ST-SM — ROOM=SECURE_DISABLE — PACK_IGNORE=TRUE, PACK_OPTION=JTAG_SECDIS:YES

SECDIS_TDO_IC	PP1V8_S2
PP1V8_S2	GND
GND	PP1V8_S2
PP1V8_S2	SECDIS_TDO_IC

APN: 516S00115
I HAVE ROTATIONAL SYMMETRY

ROOM=SECURE_DISABLE — PACK_OPTION=JTAG_SECDIS:NO

PP1V8_S2 — CKPLUS_WAIVE=TERMSHORTED — PACK_IGNORE=TRUE — PACK_OPTION=JTAG_SECDIS:YES — RR304 4.7K 5% 1/20W MF 201
PP1V8_S2 — RR305 4.7K 5% 1/20W MF 201
PP1V8_S2
GND

JTAG PORT TIE-OFFS
PACK_IGNORE=TRUE, PACK_OPTION=JTAG_SECDIS:YES, CKPLUS_WAIVE=TERMSHORTED — RR306 4.7K 5% 1/20W MF 201 — PACK_OPTION=JTAG_SECDIS:NO — GND — MAKE_BASE=TRUE

ROOM=SECURE_DISABLE

PP1V2_S2 — SERIAL PROGRAMMING DISABLE — RR307 4.7K 5% 1/20W MF 201 — SECDIS_SN_TIE_OFF

PP1V8_S2 — MUST BE SAME RAIL AS DMICS — RR308 47K 1% 1/20W MF 201 — DMIC_CLK_ENABLE

BOM_COST_GROUP=SOC

ROOM=SECURE_DISABLE, BYPASS=UR300.D7::5MM
ROOM=SECURE_DISABLE, BYPASS=UR300.D1::5MM
ROOM=SECURE_DISABLE, BYPASS=UR300.G6::5MM
PP1V2_S2 — CR300 0.1UF, CR301 0.1UF, CR302 0.1UF — 10% 6.3V CERM-X5R 0201

ROOM=SECURE_DISABLE, BYPASS=UR300.B7::5MM
ROOM=SECURE_DISABLE, BYPASS=UR300.A2::5MM
ROOM=SECURE_DISABLE, BYPASS=UR300.A5::5MM
PP1V8_S2 — CR303 0.1UF, CR304 0.1UF, CR305 0.1UF — 10% 6.3V CERM-X5R 0201

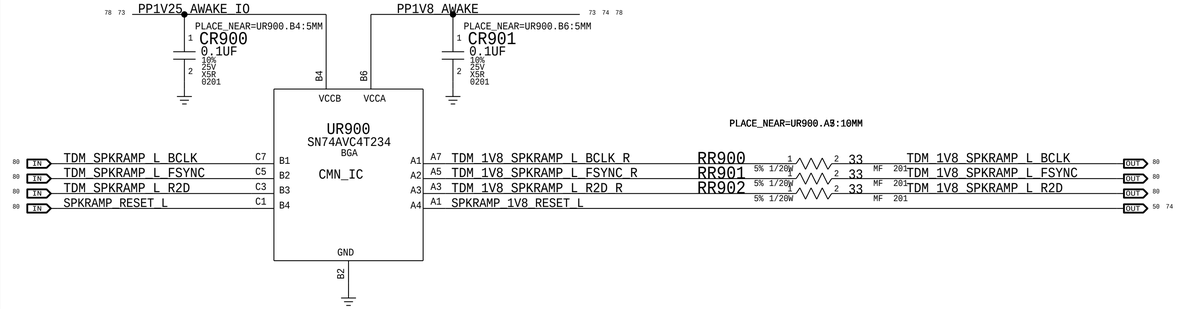
SYNC_MASTER=ref_secdis_sak — SYNC_DATE=04/28/2020

PAGE TITLE: SECDIS: FPGA

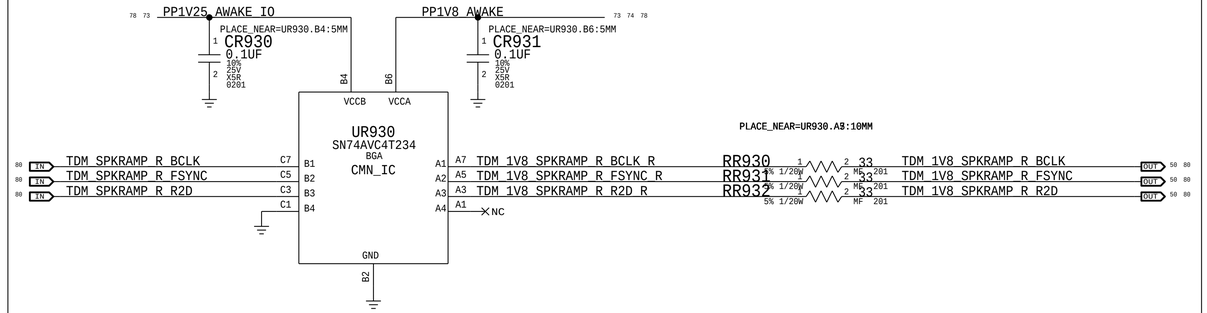
Apple Inc.

DRAWING NUMBER: 051-05392 — SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
PAGE: 243 OF 801
SHEET: 72 OF 92

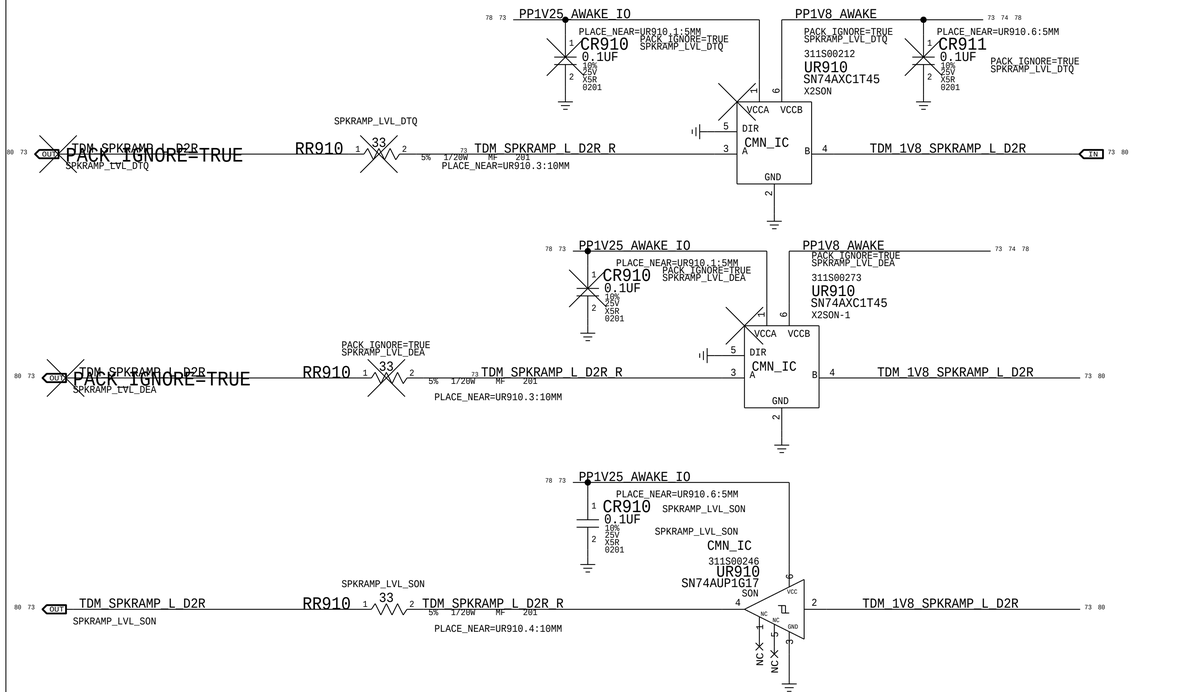
A Left Speaker Amplifier TDM Level Translator



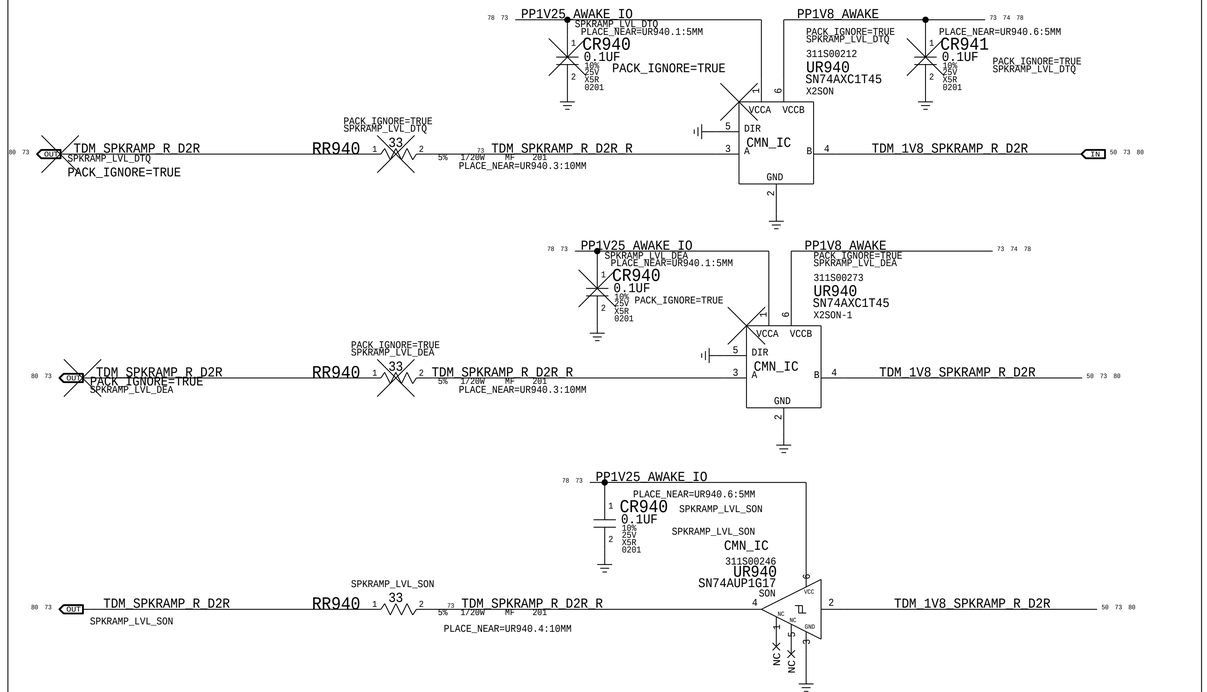
C Right Speaker Amplifier TDM Level Translator



B Left Speaker Amplifier TDM Output Level Translator



D Right Speaker Amplifier TDM Output Level Translator



BOM_COST_GROUP=AUDIO

SYNC_MASTER=ref_spkramp_tas5770 SYNC_DATE=11/18/2019

PAGE TITLE: Audio Level Shifters

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

REVISION: 4.0.0

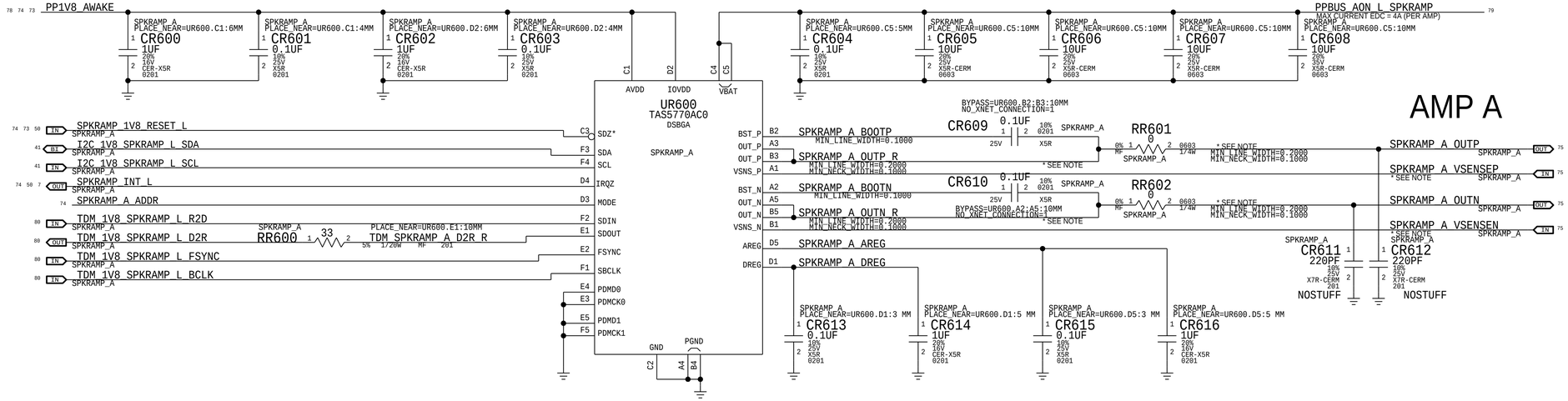
BRANCH: evt-1

PAGE: 244 OF 801

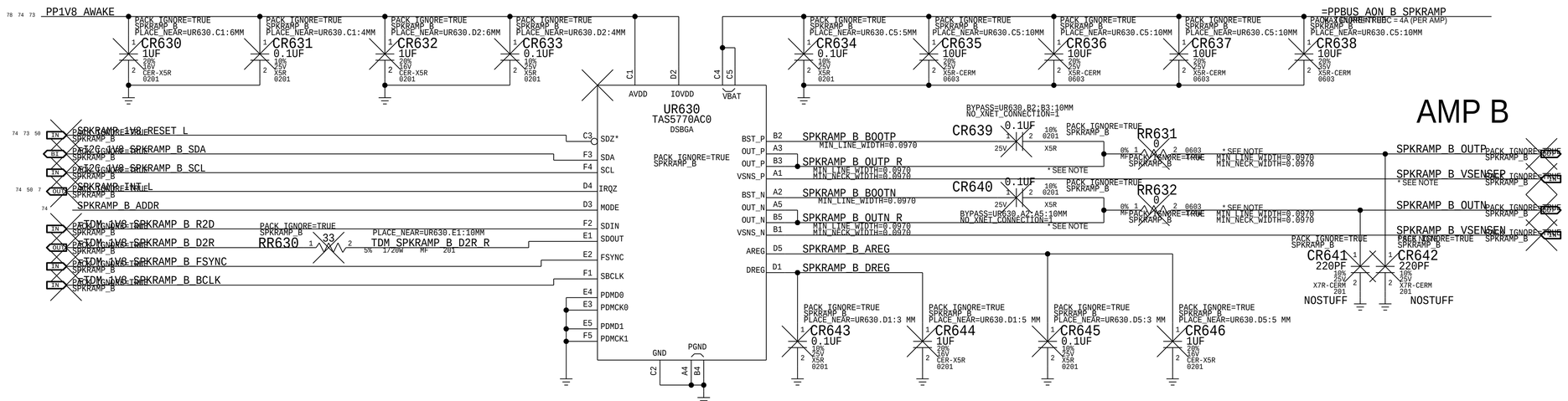
SHEET: 73 OF 92

*** OK2INTEGRATE ***

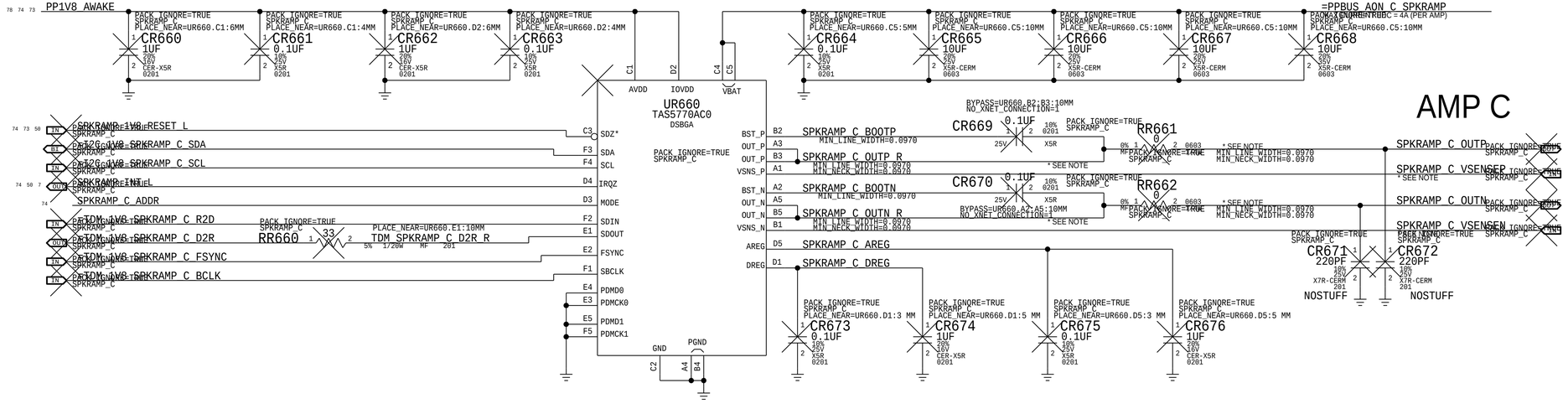
AMP A

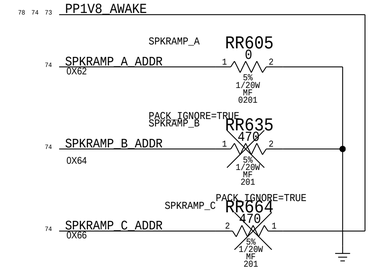


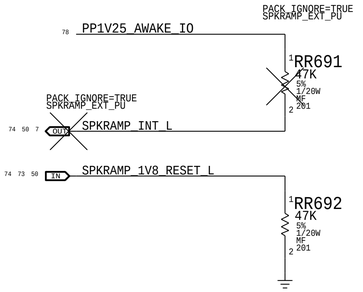
AMP B



AMP C







NOTES:

- CHECK THAT SPKRAMP_INT_L HAS IPU ON SOC SIDE.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

BOM_COST_GROUP=AUDIO

SYNC_MASTER=rref_spkramp_tas5770 SYNC_DATE=04/20/2020

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
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BRANCH: evt-1
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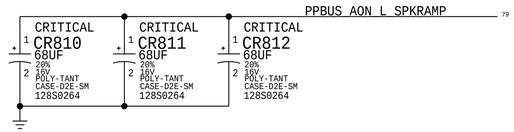
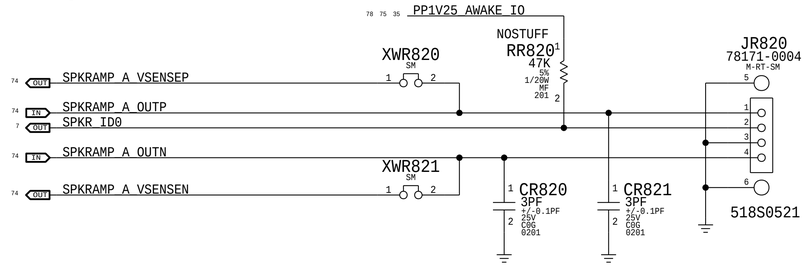
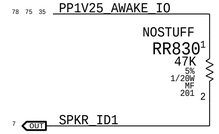
A Left Speaker Amplifier Bulk Capacitors



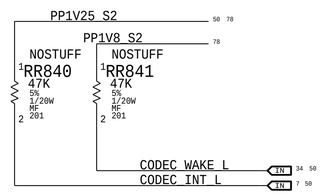
B Left Speaker Connector



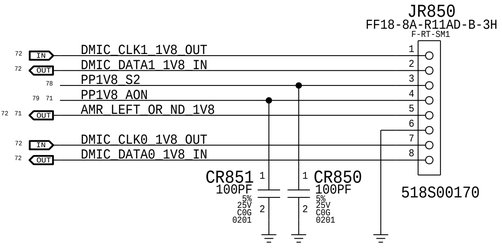
C Right Speaker ID



D Audio Jack CODEC Pull-Ups



E DMic Connector



BOM_COST_GROUP=AUDIO

DESIGN: T651/MLB
LAST CHANGE: Fri Oct 11 18:06:02 2019

PAGE TITLE
Audio Connectors

Apple Inc.

DRAWING NUMBER 051-05392
SIZE D
REVISION 4.0.0
BRANCH evt-1
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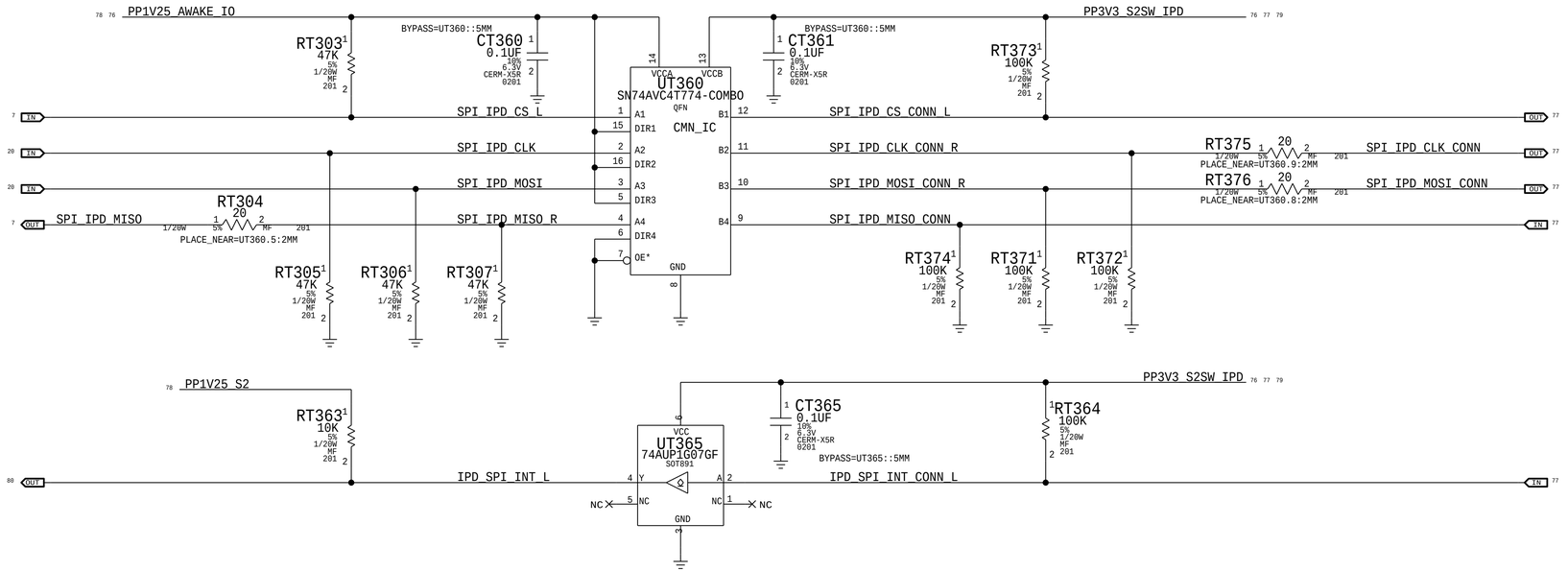
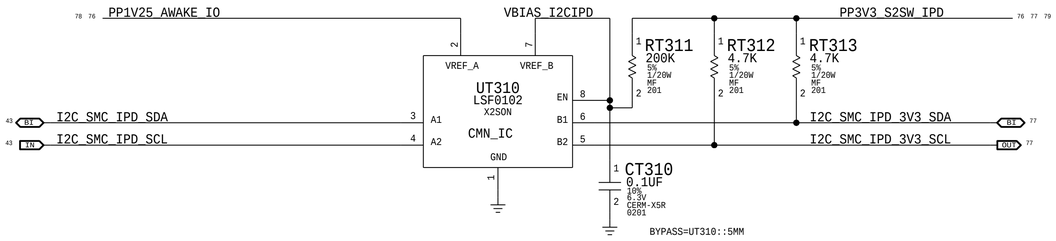
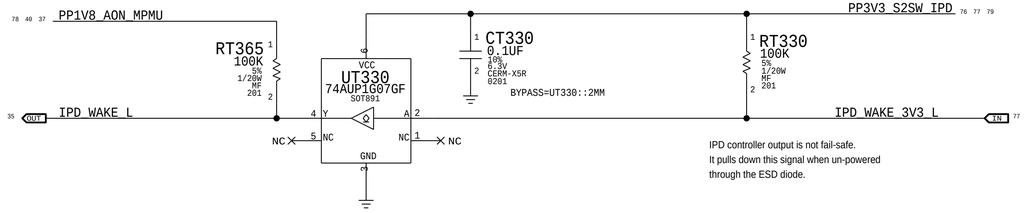
A Trackpad SPI Bus Level Shifter (+1.2V to +3.3V)



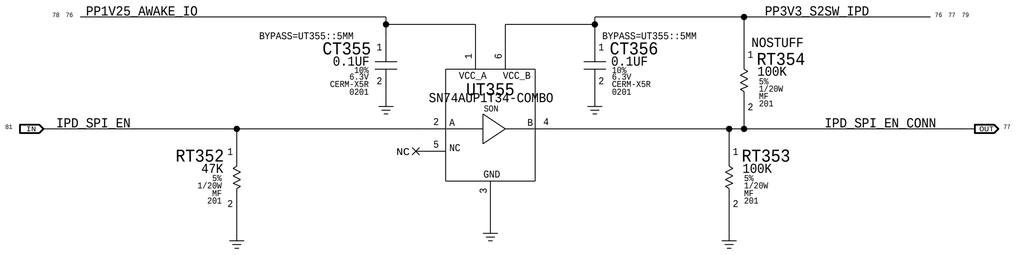
B Trackpad I2C Bus Level Shifter



C Trackpad Wake Level Shifter



D Trackpad SPI Enable Level Shifter



BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=ref_ipd_oregano SYNC_DATE=08/01/2019

PAGE TITLE: Trackpad Support

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

REVISION: 4.0.0

BRANCH: evt-1

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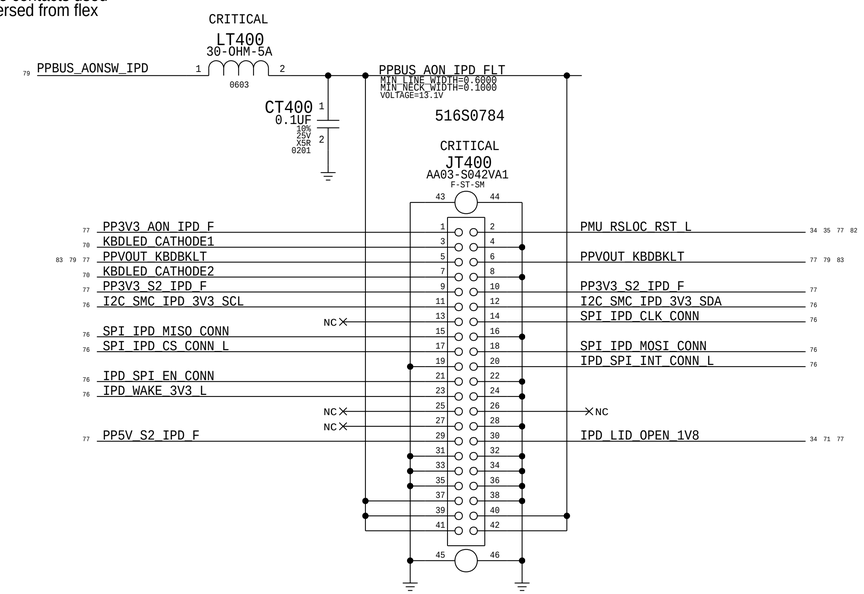
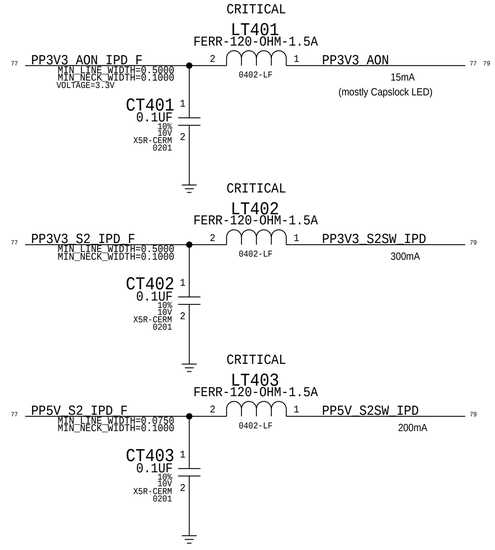
SHEET: 76 OF 92

A IPD B2B CONNECTOR

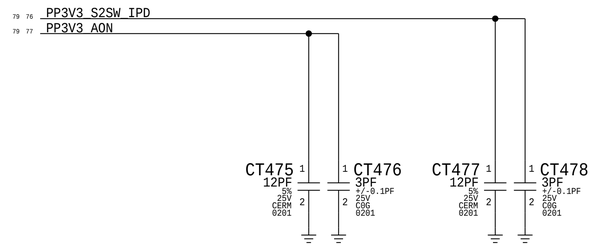
Bottom side contacts used
Pinout reversed from flex



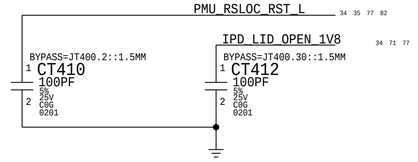
B IPD Power Filters



C IPD Desense

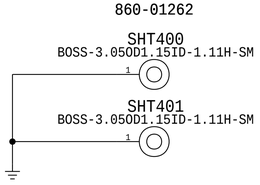


D IPD Control



F IPD Connector Bosses

860-01262



BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=card_ipd_oregano SYNC_DATE=08/01/2019

PAGE TITLE
IPD Combined Connector

Apple Inc.

DRAWING NUMBER 051-05392
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BRANCH evt-1
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POWER CONNECTIONS

SERA BUCK0 (ACTIVE)

PPVDD_PCPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
→ PPVDD_PCPU_AWAKE 32
→ PPVDD_PCPU_AWAKE 13 18

SERA BUCK1 (SW CTRL)

83 PPVDD_GPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
→ PPVDD_GPU_AWAKE 32
→ PPVDD_GPU_AWAKE 13 18

SERA BUCK2 (SLEEP1)

83 PPVDD_SOC_S1
MAKE_BASE=TRUE
VOLTAGE=0.86V
→ PPVDD_SOC_S1 32 35
→ PPVDD_SOC_S1 13

SERA BUCK3 (SLEEP3)

PP1V8_S2
MAKE_BASE=TRUE
VOLTAGE=1.8V
→ PP1V8_S2 33
→ PP1V8_S2 54
→ PP1V8_S2 54
72 PP1V8_S2 → PP1V8_S2 29
21 PP1V8_S2 → PP1V8_S2 28
54 PP1V8_S2 → PP1V8_S2 32
78 54 PP1V8_S2 → PP1V8_S2 40
78 75 PP1V8_S2 → PP1V8_S2 33
78 54 PP1V8_S2 → PP1V8_S2 75 78
60 PP1V8_S2 → PP1V8_S2 75
→ PP1V8_S2 23 24
49 PP1V8_S2
49 PP1V8_S2 → PP1V8_S2 68
→ PP1V8_S2 42
→ PP1V8_S2 66
→ PP1V8_S2 42
→ PP1V8_S2 43

SIMETRA BUCK4 (SLEEP3)

83 PP1V06_S2SW_DRAM
MAKE_BASE=TRUE
VOLTAGE=1.1V
→ PP1V06_S2SW_DRAM 28
→ PP1V06_S2SW_DRAM 11 18
→ PP1V06_S2SW_DRAM 29

SIMETRA BUCK5 (SLEEP1)

PP0V764_S1_SRAM
MAKE_BASE=TRUE
VOLTAGE=0.8V
→ PP0V764_S1_SRAM 28
→ PP0V764_S1_SRAM 14 18

SIMETRA BUCK6 (ACTIVE)

83 31 PP2V5_AWAKE_NAND
MAKE_BASE=TRUE
VOLTAGE=2.63V
→ PP2V5_AWAKE_NAND 28
→ PP2V5_AWAKE_NAND 62 63 64

SERA BUCK7 (ACTIVE)

PPVDD_CPU_SRAM_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.1V
→ PPVDD_CPU_SRAM_AWAKE 33
→ PPVDD_CPU_SRAM_AWAKE 14 18

SERA BUCK8 (SW CTRL)

83 PPVDD_DISP_S1
MAKE_BASE=TRUE
VOLTAGE=0.94V
→ PPVDD_DISP_S1 33
→ PPVDD_DISP_S1 13 18

SERA BUCK9 (SLEEP1)

PPVDD_DCS_S1
MAKE_BASE=TRUE
VOLTAGE=0.85V
→ PPVDD_DCS_S1 33
→ PPVDD_DCS_S1 14 18

SIMETRA BUCK10 (SLEEP1)

83 PP0V6_S1_VDDQL
MAKE_BASE=TRUE
VOLTAGE=0.6V
→ PP0V6_S1_VDDQL 28
→ PP0V6_S1_VDDQL 11 18

SERA BUCK11 (ACTIVE)

83 PPVDD_ECPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
→ PPVDD_ECPU_AWAKE 33
→ PPVDD_ECPU_AWAKE 13 18

SIMETRA BUCK12 (ACTIVE)

PP0V88_S1
MAKE_BASE=TRUE
VOLTAGE=0.88V
→ PP0V88_S1 28
→ PP0V88_S1 29

SIMETRA BUCK13 (ACTIVE)

82 PP1V25_S2
MAKE_BASE=TRUE
VOLTAGE=1.25V
→ PP1V25_S2 28
→ PP1V25_S2 10 12
42 PP1V25_S2 → PP1V25_S2 12
42 PP1V25_S2 → PP1V25_S2 15
76 PP1V25_S2 → PP1V25_S2 15
49 PP1V25_S2 → PP1V25_S2 15
43 PP1V25_S2 → PP1V25_S2 21
43 PP1V25_S2 → PP1V25_S2 28
43 PP1V25_S2 → PP1V25_S2 29 30
41 PP1V25_S2 → PP1V25_S2 33
→ PP1V25_S2 32
→ PP1V25_S2 53 55 56
→ PP1V25_S2 24
→ PP1V25_S2 70
75 50 PP1V25_S2 → PP1V25_S2 29
34 PP1V25_S2 → PP1V25_S2 35
60 PP1V25_S2
58 PP1V25_S2

SERA BUCK14 (ACTIVE)

PP1V4_LDO_PREREG
MAKE_BASE=TRUE
VOLTAGE=1.40V
→ PP1V4_LDO_PREREG 35
→ PP1V4_LDO_PREREG 35

SERA LDO1 (SLEEP2)

NC_MPMU_VLDO1
MAKE_BASE=TRUE
→ NC_MPMU_VLDO1 34

SERA LDO2 (SLEEP2)

SERA LDO3 (SLP_S2R)

PP1V2_S2
MAKE_BASE=TRUE
VOLTAGE=1.2V
→ PP1V2_S2 34
→ PP1V2_S2 72

SIMETRA LDO4 (SW CTRL)

83 PP0V72_S2_VDD_LOW
MAKE_BASE=TRUE
VOLTAGE=0.72V
→ PP0V72_S2_VDD_LOW 29
→ PP0V72_S2_VDD_LOW 15 18
→ PP0V72_S2_VDD_LOW 15
→ PP0V72_S2_VDD_LOW 15
→ PP0V72_S2_VDD_LOW 15
→ PP0V72_S2_VDD_LOW 15

SERA LDO7 (SW CTRL)

PP3V3_S2_UPC
MAKE_BASE=TRUE
VOLTAGE=3.3V
→ PP3V3_S2_UPC 34
→ PP3V3_S2_UPC 53 55 56

SIMETRA LDO8 (SLEEP2)

83 PP1V2_AWAKE_PLL
MAKE_BASE=TRUE
VOLTAGE=1.2V
→ PP1V2_AWAKE_PLL 29
→ PP1V2_AWAKE_PLL 15
→ PP1V2_AWAKE_PLL 11
→ PP1V2_AWAKE_PLL 15
→ PP1V2_AWAKE_PLL 15

SERA LDO9 (ACTIVE)

PP1V8_AON_MPMU
MAKE_BASE=TRUE
→ PP1V8_AON_MPMU 34
→ PP1V8_AON_MPMU 30 34
→ PP1V8_AON_MPMU 24
→ PP1V8_AON_MPMU 36
→ PP1V8_AON_MPMU 37 40 76

SERA LDO10 (ACTIVE)

SIMETRA LDO11 (SLEEP2)

PP0V855_S2SW_CIO
MAKE_BASE=TRUE
VOLTAGE=0.86V
→ PP0V855_S2SW_CIO 29
→ PP0V855_S2SW_CIO 15
→ PP0V855_S2SW_CIO 15

SIMETRA LDO12 (SLEEP2)

83 PP0V805_S1_VDD_FIXED
MAKE_BASE=TRUE
VOLTAGE=0.805V
→ PP0V805_S1_VDD_FIXED 29
→ PP0V805_S1_VDD_FIXED 15 18
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15 18
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15
→ PP0V805_S1_VDD_FIXED 15

SERA LDO13 (SW CTRL)

SERA LDO16 (SW CTRL)

SERA LDO19 (SPARE)

SIMETRA LDO20 (SW CTRL)

83 PP1V2_S2_CIO
MAKE_BASE=TRUE
→ PP1V2_S2_CIO 29
→ PP1V2_S2_CIO 15
→ PP1V2_S2_CIO 15

SERA SW1 (ACTIVE)

PP1V8_AWAKE
MAKE_BASE=TRUE
→ PP1V8_AWAKE 33
→ PP1V8_AWAKE 12
→ PP1V8_AWAKE 73 74
→ PP1V8_AWAKE 5
→ PP1V8_AWAKE 19
→ PP1V8_AWAKE 19
→ PP1V8_AWAKE 50
→ PP1V8_AWAKE 41

SERA SW3 (ACTIVE)

83 PP1V25_AWAKE_IO
MAKE_BASE=TRUE
→ PP1V25_AWAKE_IO 33
→ PP1V25_AWAKE_IO 15
→ PP1V25_AWAKE_IO 5 6 7 9 12
→ PP1V25_AWAKE_IO 15
→ PP1V25_AWAKE_IO 15
→ PP1V25_AWAKE_IO 15
→ PP1V25_AWAKE_IO 74
→ PP1V25_AWAKE_IO 15
→ PP1V25_AWAKE_IO 35 75
→ PP1V25_AWAKE_IO 76
→ PP1V25_AWAKE_IO 73
→ PP1V25_AWAKE_IO 50
→ PP1V25_AWAKE_IO 5
→ PP1V25_AWAKE_IO 19
→ PP1V25_AWAKE_IO 41
→ PP1V25_AWAKE_IO 41
→ PP1V25_AWAKE_IO 41

SIMETRA SW4 (SLEEP2)

SIMETRA SW5 (SLEEP2)

83 PP1V25_AWAKE_NAND
MAKE_BASE=TRUE
VOLTAGE=1.25V
→ PP1V25_AWAKE_NAND 29
→ PP1V25_AWAKE_NAND 62 63

SIMETRA SW6 (SLEEP2) PARALLEL
SIMETRA SW7 (SLEEP2) PARALLEL

83 PP0V88_AWAKE_NAND
MAKE_BASE=TRUE
VOLTAGE=0.88V
→ PP0V88_AWAKE_NAND 29
→ PP0V88_AWAKE_NAND 62
→ PP0V88_AWAKE_NAND 63

SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE
Power Aliases - 1

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
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PBUS Rails

U7000 - PBUS

23 PPBUS_AON
- PPBUS_AON (83) — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_AON (27)
- PPBUS_AON (69)
- PPBUS_AON (46)
- PPBUS_AON (50)
- PPBUS_AON (40)
- PPBUS_AON (44)
- PPBUS_AON (25 26)
- PPBUS_AON (32)
- PPBUS_AON (44)
- PPBUS_AON (44)

44 PPBUS_5VS2_VIN
- PPBUS_5VS2_VIN — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_5VS2_VIN (38)

44 PPBUS_3V3S2_VIN
- PPBUS_3V3S2_VIN — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_3V3S2_VIN (39)

46 PPBUS_AON_L_SPKRAMP
- PPBUS_AON_L_SPKRAMP (83) — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_AON_L_SPKRAMP (75)
- PPBUS_AON_L_SPKRAMP (74)

46 PPBUS_AONSW_IPD
- PPBUS_AONSW_IPD — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_AONSW_IPD (77)

53 PPDCIN_AONSW
- PPDCIN_AONSW — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=20V, MAKE_BASE=TRUE
- PPDCIN_AONSW (23)
- PPDCIN_AONSW (44)

U7550 - 5V G3S

38 PP5V_S2

Sourced from PBus
Enabled by P5VG3S_EN

- PP5V_S2 (83) — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S2 (37)
- PP5V_S2 (46)
- PP5V_S2 (67)
- PP5V_S2 (69)
- PP5V_S2 (38)
- PP5V_S2 (68)
- PP5V_S2 (55 56)
- PP5V_S2 (55 56)
- PP5V_S2 (40)
- PP5V_S2 (27)

46 PP5V_S2_KBDLED
- PP5V_S2_KBDLED (83) — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S2_KBDLED (70)

25 PP5V_AON_P3V8VRLDO
- PP5V_AON_P3V8VRLDO — MIN_LINE_WIDTH=0.0980, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_AON_P3V8VRLDO (25)

68 PP5V_SW_LCD
- PP5V_SW_LCD (67) — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE

48 PP5V_S2SW_IPD
- PP5V_S2SW_IPD — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S2SW_IPD (77)
- PP5V_S2SW_IPD (46)

3V3 Rails

UXXXX - 3V3_S2

39 PP3V3_S2

Sourced from PBus
Enabled by ????

- PP3V3_S2 (82) — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S2 (46)
- PP3V3_S2 (37)
- PP3V3_S2 (66)
- PP3V3_S2 (70)
- PP3V3_S2 (40)
- PP3V3_S2 (68)
- PP3V3_S2 (40)
- PP3V3_S2 (39)
- PP3V3_S2 (43)

46 PP3V3_S2_WLBT
- PP3V3_S2_WLBT — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S2_WLBT (60)

40 PP3V3_S2SW_SNS
- PP3V3_S2SW_SNS — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S2SW_SNS (44 45 46)

40 PP3V3_S2SW_IPD
- PP3V3_S2SW_IPD — MIN_LINE_WIDTH=0.0970, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S2SW_IPD (76 77)
- PP3V3_S2SW_IPD (77)

68 PP3V3_SW_LCD
- PP3V3_SW_LCD (67) — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_SW_LCD (41)

36 PP3V3_AON

Sourced from PBus

- PP3V3_AON (82) — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_AON (77)
- PP3V3_AON (43)
- PP3V3_AON (35)

PP1V8_AON — MAKE_BASE=TRUE, VOLTAGE=1.8V
- PP1V8_AON (36)
- PP1V8_AON (50)
- PP1V8_AON (40)
- PP1V8_AON (35)
- PP1V8_AON (71 75)

PP1V8_S2SW_VDD1 — MAKE_BASE=TRUE, VOLTAGE=1.8V
- PP1V8_S2SW_VDD1 (40)
- PP1V8_S2SW_VDD1 (11 18)

NEED TO CHECK THE SPLIT
TO DIFFERENT SWITCH OUTPUTS.

CHARGER MAIN

83 82 PP3V8_AON_VDDMAIN — MAKE_BASE=TRUE, VOLTAGE=3.8V
- PP3V8_AON_VDDMAIN (26)
- PP3V8_AON_VDDMAIN (32 34 35)
- PP3V8_AON_VDDMAIN (28 29)
- PP3V8_AON_VDDMAIN (50)
- PP3V8_AON_VDDMAIN (40)
- PP3V8_AON_VDDMAIN (36)
- PP3V8_AON_VDDMAIN (36)
- PP3V8_AON_VDDMAIN (27)
- PP3V8_AON_VDDMAIN (21)
- PP3V8_AON_VDDMAIN (51)
- PP3V8_AON_VDDMAIN (52)
- PP3V8_AON_VDDMAIN (22)
- PP3V8_AON_VDDMAIN (32)
- PP3V8_AON_VDDMAIN (37)

Digital Ground

GND — VOLTAGE=0V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800

PPVOUT_LCDBKLT — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE
- PPVOUT_LCDBKLT (67 83)
- PPVOUT_LCDBKLT (69)

PPVOUT_KBDBKLT — MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V, MAKE_BASE=TRUE
- PPVOUT_KBDBKLT (77 83)
- PPVOUT_KBDBKLT (70)

PP3V3_S2SW_USBC0 — MAKE_BASE=TRUE
- PP3V3_S2SW_USBC0 (51)
- PP3V3_S2SW_USBC0 (51 53)
- PP3V3_S2SW_USBC0 (51 53)
- PP3V3_S2SW_USBC0 (58)
- PP3V3_S2SW_USBC0 (58)

PP3V3_S2SW_USBC1 — MAKE_BASE=TRUE
- PP3V3_S2SW_USBC1 (52)
- PP3V3_S2SW_USBC1 (52 53)
- PP3V3_S2SW_USBC1 (52 53)
- PP3V3_S2SW_USBC1 (58)
- PP3V3_S2SW_USBC1 (58)

PAGE TITLE
Power Aliases - 2

Apple Inc.

DRAWING NUMBER 051-05392
SIZE D
REVISION 4.0.0
BRANCH evt-1
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Ref	Net	Properties		Alias	Ref
7	NC_DFR_1V8_DISP_INT	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_DISP_INT	
7	NC_DFR_1V8_DISP_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_DISP_RESET_L	
7	NC_DFR_1V8_TOUCH_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_TOUCH_RESET_L	
8	NC_DFR_DISP_TE	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_DISP_TE	
7	NC_DFR_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_PWR_EN	
10	NC_HDMI_CEC_AOP_RX	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_CEC_AOP_RX	
10	NC_HDMI_CEC_AOP_TX	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_CEC_AOP_TX	
10	NC_HDMI_HPD_AOP	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_HPD_AOP	
8	NC_MIPI_DFR_CLKN	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_CLKN	
8	NC_MIPI_DFR_CLKP	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_CLKP	
8	NC_MIPI_DFR_DATAN	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_DATAN	
8	NC_MIPI_DFR_DATAP	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_DATAP	
9	NC_PCIE_CLK100M_ENETN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENETN	
9	NC_PCIE_CLK100M_ENETP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENETP	
9	NC_PCIE_CLK100M_USBHCN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_USBHCN	
9	NC_PCIE_CLK100M_USBHCP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_USBHCP	
9	NC_PCIE_ENET_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2RN	
9	NC_PCIE_ENET_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2RP	
9	NC_PCIE_ENET_R2DCN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2DCN	
9	NC_PCIE_ENET_R2DCP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2DCP	
9	NC_PCIE_USBHC_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_D2RN	
9	NC_PCIE_USBHC_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_D2RP	
9	NC_PCIE_USBHC_R2DCN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_R2DCN	
9	NC_PCIE_USBHC_R2DCP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_R2DCP	
10	NC_SMC_FAN_PWM_SMC_SIL_LED_PWM	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_PWM_SMC_SIL_LED_PWM	
10	NC_SMC_FAN_TACH	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_TACH	
8	NC_SPI_DISP_BKLT_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DISP_BKLT_MOSI	
8	NC_SPI_DISP_BKLT_MISO	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DISP_BKLT_MISO	
10	NC_SPI_DP2HDMI_HOLD_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DP2HDMI_HOLD_L	
10	NC_NUB_SWD_TMS1	MAKE_BASE=TRUE	NO_TEST=1	NC_NUB_SWD_TMS1	
21	NC_I2C_SE_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_SE_SCL	
21	NC_I2C_SE_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_SE_SDA	
7	NC_DFR_TOUCH_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_INT_L	
7	NC_UART_TCON_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_TCON_R2D	
10	NC_ACDC_BURST_EN_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ACDC_BURST_EN_L	
10	NC_ACDC_ID	MAKE_BASE=TRUE	NO_TEST=1	NC_ACDC_ID	
10	NC_CCG_SMC_I2C_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CCG_SMC_I2C_INT_L	
8	NC_BKLT_FAULT_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_BKLT_FAULT_INT_L	
8	NC_DISP_BKLT_LSYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_BKLT_LSYNC	
9	NC_ENET_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_CLKREQ_L	
9	NC_ENET_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_RESET_L	
9	NC_USBHC_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_USBHC_RESET_L	
10	NC_DFR_TOUCH_CLK32K_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_CLK32K_RESET_L	
10	NC_AOP_FUNC0	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC0	
10	NC_AOP_FUNC3	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC3	
10	NC_AOP_FUNC2	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC2	
10	NC_SPI_R1_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_R1_CS_L	
10	NC_BKLT_PWR_ON	MAKE_BASE=TRUE	NO_TEST=1	NC_BKLT_PWR_ON	
61 60	NC_RF_BT_DED	MAKE_BASE=TRUE	NO_TEST=1	NC_RF_BT_DED	
8	NC_MIPI_FTCAM_DATA1P	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_FTCAM_DATA1P	
8	NC_MIPI_FTCAM_DATA1N	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_FTCAM_DATA1N	
72	NC_DMIC_CLK2_1V8_OUT_R_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_CLK2_1V8_OUT_R_IC	
72	NC_DMIC_CLK2_IN_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_CLK2_IN_IC	
72	NC_DMIC_DATA2_1V8_IN_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_DATA2_1V8_IN_IC	
72	NC_DMIC_DATA2_SEC_OUT_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_DATA2_SEC_OUT_IC	
72	NC_FTCAM_ENABLE_SEC_1V8_OUT_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_ENABLE_SEC_1V8_OUT_IC	
72	NC_IRCAM_ENABLE_IN_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_IRCAM_ENABLE_IN_IC	
72	NC_IRCAM_ENABLE_SEC_1V8_OUT_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_IRCAM_ENABLE_SEC_1V8_OUT_IC	
72 8	FTCAM_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	FTCAM_RESET_L	
72	NC_SEP_IRCAM_DISABLE_IC_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SEP_IRCAM_DISABLE_IC_L	
72	NC_FTCAM_ENABLE_IN	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_ENABLE_IN	
7	NC_ENET_SYNC_1588	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_SYNC_1588	
7	NC_SPI_DFR_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DFR_CS_L	
7	NC_SWD_UPC_SWDIO1	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_UPC_SWDIO1	
10	NC_ALS_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ALS_INT_L	
7	NC_SOC_TRIGGER2	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_TRIGGER2	
60	NC_BT_GPIO_4	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_GPIO_4	
60	NC_SPMI_WLBT_CLK_1V8	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI_WLBT_CLK_1V8	
60	NC_SPMI_WLBT_DAT_1V8	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI_WLBT_DAT_1V8	
7	TOUCHID_PWR_EN	MAKE_BASE=TRUE		TOUCHID_PWR_EN	50

Ref	Net	Properties	Alias	Ref
58	USB2_ATC0_LS_P	MAKE_BASE=TRUE	USB2_ATC0_LS_P	59
58	USB2_ATC0_LS_N	MAKE_BASE=TRUE	USB2_ATC0_LS_N	59
58	USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P	59
58	USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N	59
58	USB_DBG_LS_P	MAKE_BASE=TRUE	USB_DBG_LS_P	54
58	USB_DBG_LS_N	MAKE_BASE=TRUE	USB_DBG_LS_N	54
10	CHGR_INT_L	MAKE_BASE=TRUE	CHGR_INT_L	24
51	USBC_ATC0_R2D_P<1>	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<1>	51
51	USBC_ATC0_R2D_N<1>	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<1>	51
51	USBC0_D2R_P<1>	MAKE_BASE=TRUE	USBC0_D2R_P<1>	57
51	USBC0_D2R_N<1>	MAKE_BASE=TRUE	USBC0_D2R_N<1>	57
51	USBC_ATC0_R2D_P<2>	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<2>	51
51	USBC_ATC0_R2D_N<2>	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<2>	51
51	USBC0_D2R_P<2>	MAKE_BASE=TRUE	USBC0_D2R_P<2>	57
51	USBC0_D2R_N<2>	MAKE_BASE=TRUE	USBC0_D2R_N<2>	57
51	USBC_ATC0_D2R_C_P<1>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<1>	51
51	USBC_ATC0_D2R_C_N<1>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<1>	51
51	USBC0_R2D_CR_P<1>	MAKE_BASE=TRUE	USBC0_R2D_CR_P<1>	57
51	USBC0_R2D_CR_N<1>	MAKE_BASE=TRUE	USBC0_R2D_CR_N<1>	57
51	USBC_ATC0_D2R_C_P<2>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<2>	51
51	USBC_ATC0_D2R_C_N<2>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<2>	51
51	USBC0_R2D_CR_P<2>	MAKE_BASE=TRUE	USBC0_R2D_CR_P<2>	57
51	USBC0_R2D_CR_N<2>	MAKE_BASE=TRUE	USBC0_R2D_CR_N<2>	57
52	USBC_ATC1_R2D_P<1>	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<1>	52
52	USBC_ATC1_R2D_N<1>	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<1>	52
52	USBC1_D2R_P<1>	MAKE_BASE=TRUE	USBC1_D2R_P<1>	57
52	USBC1_D2R_N<1>	MAKE_BASE=TRUE	USBC1_D2R_N<1>	57
52	USBC_ATC1_R2D_P<2>	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<2>	52
52	USBC_ATC1_R2D_N<2>	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<2>	52
52	USBC1_D2R_P<2>	MAKE_BASE=TRUE	USBC1_D2R_P<2>	57
52	USBC1_D2R_N<2>	MAKE_BASE=TRUE	USBC1_D2R_N<2>	57
52	USBC_ATC1_D2R_C_P<1>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<1>	52
52	USBC_ATC1_D2R_C_N<1>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<1>	52
52	USBC1_R2D_CR_P<1>	MAKE_BASE=TRUE	USBC1_R2D_CR_P<1>	57
52	USBC1_R2D_CR_N<1>	MAKE_BASE=TRUE	USBC1_R2D_CR_N<1>	57
52	USBC_ATC1_D2R_C_P<2>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<2>	52
52	USBC_ATC1_D2R_C_N<2>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<2>	52
52	USBC1_R2D_CR_P<2>	MAKE_BASE=TRUE	USBC1_R2D_CR_P<2>	57
52	USBC1_R2D_CR_N<2>	MAKE_BASE=TRUE	USBC1_R2D_CR_N<2>	57
7	UART_TCON_D2R	MAKE_BASE=TRUE	UART_TCON_D2R	67
10	IPD_SPI_INT_L	MAKE_BASE=TRUE	IPD_SPI_INT_L	76
54 IN	SOC_DOCK_CONNECT	MAKE_BASE=TRUE	SOC_DOCK_CONNECT	OUT 10
73	SPKRAMP_RESET_L	MAKE_BASE=TRUE	SPKRAMP_RESET_L	7
73	TDM_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	TDM_SPKRAMP_L_BCLK	20
73	TDM_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	TDM_SPKRAMP_L_FSYNC	20
73	TDM_SPKRAMP_L_R2D	MAKE_BASE=TRUE	TDM_SPKRAMP_L_R2D	20
73	TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_L_D2R	7
74	TDM_1V8_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_BCLK	73
74	TDM_1V8_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_FSYNC	73
74	TDM_1V8_SPKRAMP_L_R2D	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_R2D	73
74	TDM_1V8_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_D2R	73
73	TDM_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	TDM_SPKRAMP_R_BCLK	20
73	TDM_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	TDM_SPKRAMP_R_FSYNC	20
73	TDM_SPKRAMP_R_R2D	MAKE_BASE=TRUE	TDM_SPKRAMP_R_R2D	20
73	TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_R_D2R	7
	TDM_1V8_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_BCLK	50 73
	TDM_1V8_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_FSYNC	50 73
	TDM_1V8_SPKRAMP_R_R2D	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_R2D	50 73
	TDM_1V8_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_D2R	50 73
60	TPT_WLAN_JTAG_TCK	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TCK	
60	TPT_WLAN_JTAG_TMS	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TMS	
60	TPT_WLAN_JTAG_TRSTN	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TRSTN	
61 60	TPT_WLAN_JTAG_TDI	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDI	
61 60	TPT_WLAN_JTAG_TDO	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDO	
	TPT_P3V8AON_PU_RAIL	MAKE_BASE=TRUE	TPT_P3V8AON_PU_RAIL	25

PAGE TITLE

Signal Aliases 1

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D

REVISION 4.0.0

BRANCH evt-1

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NC_FPWM2	MAKE_BASE=TRUE	NO_TEST=1	NC_FPWM2		
NC_SWD_TMS3	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_TMS3		
NC_SWD_TMS4	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_TMS4		
NC_I2S3_BCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_BCLK		
NC_I2S3_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_D2R		
NC_I2S3_LRCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_LRCLK		
NC_I2S3_MCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_MCLK		
NC_I2S3_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_R2D		
NC_SOC_GPIO01	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO01		
IPD_SPI_EN	MAKE_BASE=TRUE	NO_TEST=1	IPD_SPI_EN		
NC_SOC_GPIO09	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO09		
NC_SOC_GPIO10	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO10		
NC_SOC_GPIO15	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO15		
NC_SOC_GPIO16	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO16		
NC_SOC_I2S0_MCK	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S0_MCK		
NC_SOC_I2S1_MCK	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S1_MCK		
NC_SOC_I2S2_MCK	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S2_MCK		
NC_SOC_SPI2_SSIN	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_SPI2_SSIN		
NC_SPMI2_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI2_CLK		
NC_SPMI2_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI2_DATA		
NC_SSPI0_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SSPI0_MOSI		
NC_UART3_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_D2R		
NC_UART3_D2R_CTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_D2R_CTS_L		
NC_UART3_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_R2D		
NC_UART3_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_R2D_RTS_L		
NC_UART4_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_D2R		
NC_UART4_D2R_CTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_D2R_CTS_L		
NC_UART4_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_R2D		
NC_UART4_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_R2D_RTS_L		
NC_UART7_RXD	MAKE_BASE=TRUE	NO_TEST=1	NC_UART7_RXD		
NC_UART7_TXD	MAKE_BASE=TRUE	NO_TEST=1	NC_UART7_TXD		
NC_DISP_FSYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_FSYNC		
NC_DISP_SPMI_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_SPMI_CLK		
NC_DISP_SPMI_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_SPMI_DATA		
NC_DISP_TOUCH_BSYNC0	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_BSYNC0		
NC_DISP_TOUCH_BSYNC1	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_BSYNC1		
NC_DISP_TOUCH_EB	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_EB		
NC_DISPLAY_POL	MAKE_BASE=TRUE	NO_TEST=1	NC_DISPLAY_POL		
NC_ISP_GPIO1	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO1		
NC_ISP_GPIO2	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO2		
NC_ISP_GPIO3	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO3		
NC_ISP_I2C0_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C0_SCL		
NC_ISP_I2C0_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C0_SDA		
NC_ISP_I2C1_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C1_SCL		
NC_ISP_I2C1_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C1_SDA		
NC_ISP_I2C3_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C3_SCL		
NC_ISP_I2C3_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C3_SDA		
NC_ISP_SPMI0_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI0_CLK		
NC_ISP_SPMI0_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI0_DATA		
NC_ISP_SPMI1_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI1_CLK		
NC_ISP_SPMI1_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI1_DATA		
NC_LPDP_TX4N	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX4N		
NC_LPDP_TX4P	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX4P		
NC_LPDP_TX5N	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX5N		
NC_LPDP_TX5P	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX5P		
NC_LPDPRX_AUX0	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX0		
NC_LPDPRX_AUX1	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX1		
NC_LPDPRX_AUX2	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX2		
NC_LPDPRX_AUX3	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX3		
NC_LPDPRX_AUX4	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX4		
NC_LPDPRX_AUX5	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX5		
NC_LPDPRX_AUX6	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX6		
NC_LPDPRX_AUX7	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX7		
NC_LPDPRX_AUX8	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX8		
NC_LPDPRX_AUX9	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX9		
NC_LPDPRX_AUX10	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX10		
NC_LPDPRX_AUX11	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX11		
NC_MIPI0C_CLKN	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_CLKN		
NC_MIPI0C_CLKP	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_CLKP		
NC_MIPI0C_DATAN0	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAN0		
NC_MIPI0C_DATAN1	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAN1		
NC_MIPI0C_DATAP0	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAP0		
NC_MIPI0C_DATAP1	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAP1		
NC_SENSOR0_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR0_CLK		
NC_SENSOR1_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR1_CLK		
NC_SENSOR2_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR2_CLK		
NC_SENSOR3_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR3_CLK		
NC_NAND0_PCIE_RESET1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_PCIE_RESET1_L		
NC_PAD_MTR_ANALOG_TEST_NEG	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_ANALOG_TEST_NEG		
NC_PAD_MTR_ANALOG_TEST_POS	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_ANALOG_TEST_POS		
NC_PAD_MTR_VREF_NEG	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_VREF_NEG		
NC_PAD_MTR_VREF_POS	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_VREF_POS		
NC_AON_SLEEP1_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_AON_SLEEP1_RESET_L		
NC_AOP_FUNC1	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC1		
NC_AOP_FUNC5	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC5		
NC_AOP_FUNC10	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC10		
NC_AOP_FUNC14	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC14		
NC_AOP_SPMI0_SCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_SPMI0_SCLK		
NC_AOP_SPMI0_SDATA	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_SPMI0_SDATA		
NC_AOP_UART2_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_UART2_D2R		
NC_AOP_UART2_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_UART2_R2D		

NC_PDM_CLK1	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK1
NC_PDM_CLK2	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK2
NC_PDM_CLK5	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK5
NC_PDM_CLK6	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK6
NC_PDM_DATA1	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_DATA1
NC_PDM_DATA2	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_DATA2
NC_SMC_GPIO1	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GPIO1

NC_CHGR_CBC_ON	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_CBC_ON
NC_CHGR_EN_VR1	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_EN_VR1
NC_CHGR_SMC_RST_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_SMC_RST_L
NC_EUSB_LS1N	MAKE_BASE=TRUE	NO_TEST=1	NC_EUSB_LS1N
NC_EUSB_LS1P	MAKE_BASE=TRUE		NC_EUSB_LS1P
NC_SE_GPIO0	MAKE_BASE=TRUE	NO_TEST=1	NC_SE_GPIO0
NC_SMBUS_ATCRTMR0_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR0_SCL
NC_SMBUS_ATCRTMR0_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR0_SDA
NC_SMBUS_ATCRTMR1_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR1_SCL
NC_SMBUS_ATCRTMR1_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR1_SDA
NC_USB_LS1N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB_LS1N
NC_USB_LS1P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB_LS1P
NC_LPDPRX_RXN0	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN0
NC_LPDPRX_RXN1	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN1
NC_LPDPRX_RXN2	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN2
NC_LPDPRX_RXN3	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN3
NC_LPDPRX_RXN4	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN4
NC_LPDPRX_RXN5	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN5
NC_LPDPRX_RXN6	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN6
NC_LPDPRX_RXN7	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN7
NC_LPDPRX_RXN8	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN8
NC_LPDPRX_RXN9	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN9
NC_LPDPRX_RXN10	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN10
NC_LPDPRX_RXN11	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN11
NC_LPDPRX_RXP0	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP0
NC_LPDPRX_RXP1	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP1
NC_LPDPRX_RXP2	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP2
NC_LPDPRX_RXP3	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP3
NC_LPDPRX_RXP4	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP4
NC_LPDPRX_RXP5	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP5
NC_LPDPRX_RXP6	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP6
NC_LPDPRX_RXP7	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP7
NC_LPDPRX_RXP8	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP8
NC_LPDPRX_RXP9	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP9
NC_LPDPRX_RXP10	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP10
NC_LPDPRX_RXP11	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP11
NC_NAND0_S5E0_VPP	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_S5E0_VPP
NC_NAND0_S5E1_VPP	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_S5E1_VPP

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Signal Aliases 2

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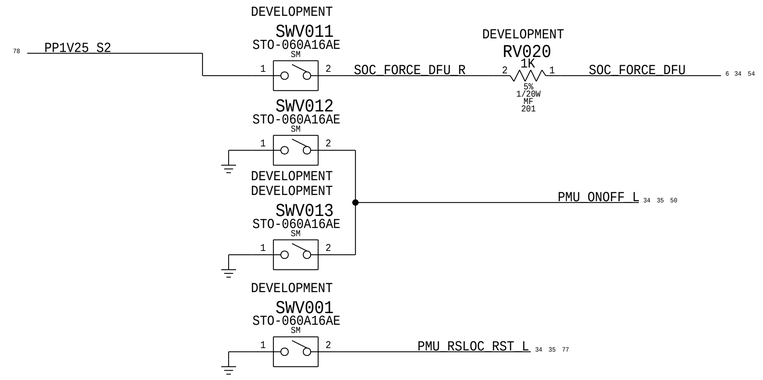
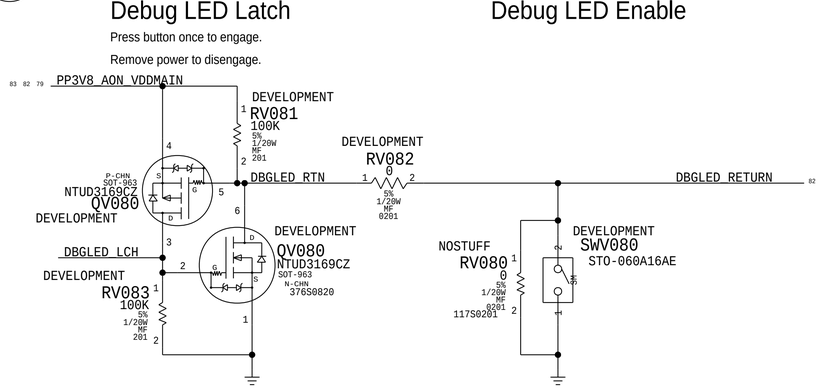
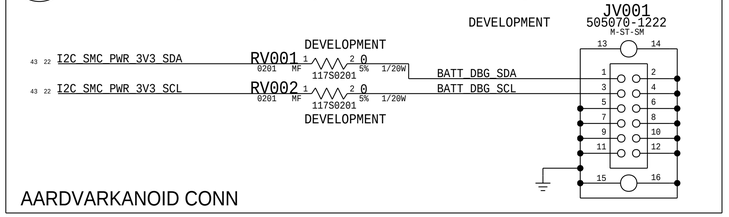
A Debug Push-Buttons



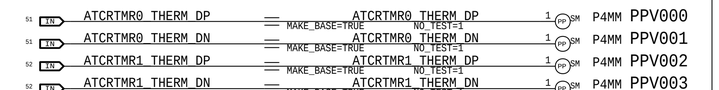
B Debug LED Control



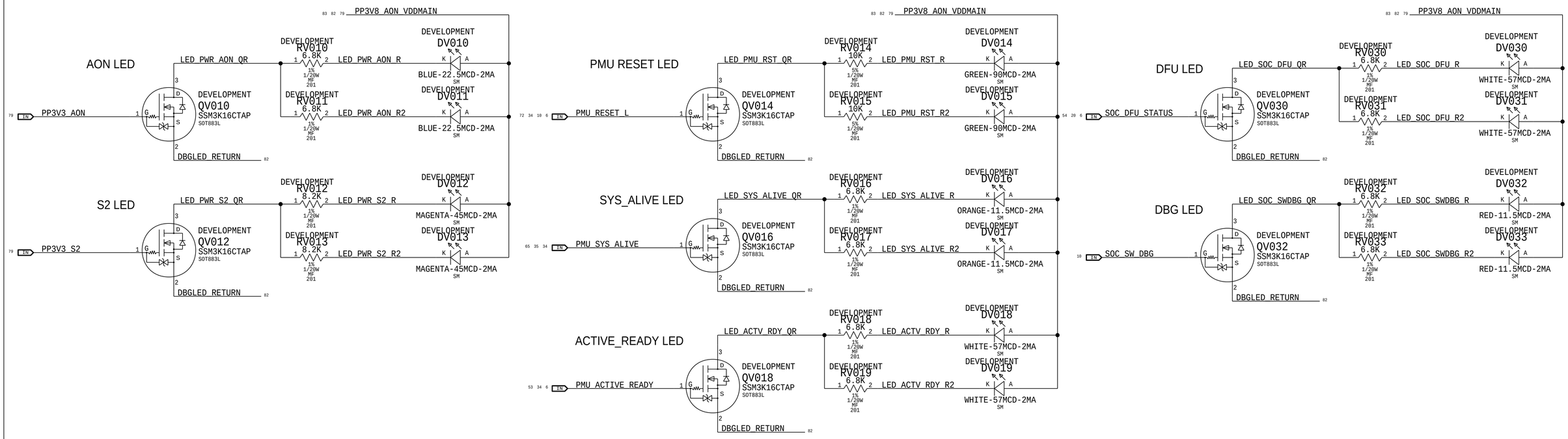
C Battery Sub-System Debug Connector



D Thermal Diode Test Points



E Debug LEDs



SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

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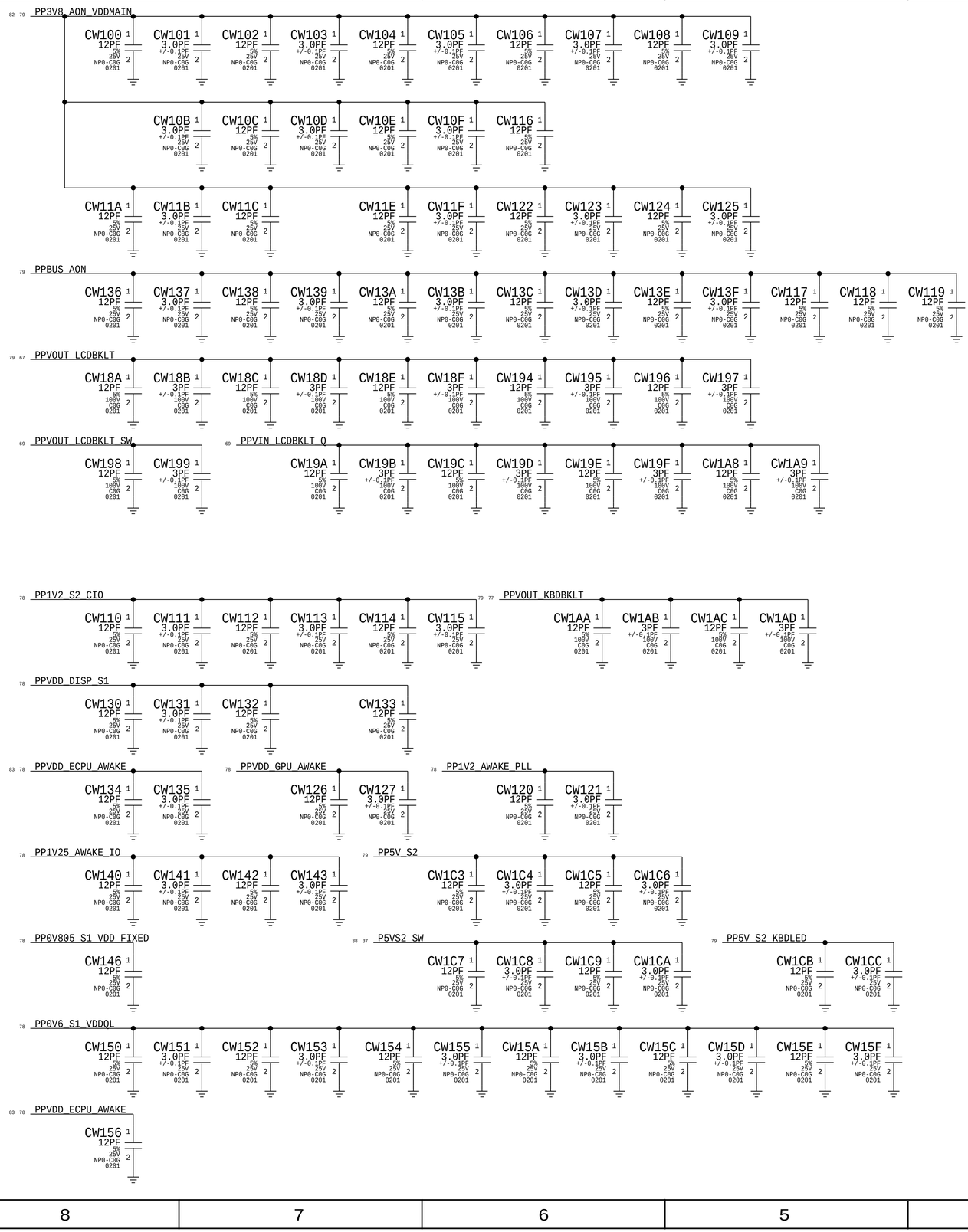
BOM_COST_GROUP=DEBUG



BOM_COST_GROUP=DESENSE

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculate dielectric distance from startup, shortest distance is used unless 'x' is defined	EXAMPLE: 1,2.5,3,4.5
A_DIELECTRIC_(N)XD XV,XVL,X Calculate dielectric distance from hybrid table and standup, shortest distance is used unless 'x' defined	2-10 EXAMPLE: 2.5V,3V,3.5V,4V,4.5V PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculate dielectric distance from standup, shortest distance is used unless 'x' is defined	EXAMPLE: 2,4,6,8

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17.2 RULES

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PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR WARNINGS
CLASS NAME	DIFF P,N,S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_XTAL24M*,SOC_24M_O_R,NAND0_CLK24M*	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
CIO_D2R	P	A_85_OHM_DIFF	DP:DP_USBC*_D2R*	Y
CIO_R2D	P	A_85_OHM_DIFF	DP:DP_USBC*_R2D*	Y
PCIE_NAND_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_D2R*	Y
PCIE_NAND_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_R2D*	Y
PCIE_WLBT_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_R2D*	Y
PCIE_WLBT_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_D2R*	Y
LPDP	P	A_85_OHM_DIFF	DP:DP_LPDP_INT_DATA*	Y
PCIE_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M*	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
MIPI_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_CLK*,DP_MIPI_CLOCK*	Y
MIPI_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_DATA*,DP_MIPI_DATA*	Y
EUSB	P	A_85_OHM_DIFF	DP:DP_EUSB*	Y
GROUND	P	DEFAULT	GND	Y
POWER	P	POWER	PP*	Y

PHYSICAL CONSTRAINT SET, NET ASSIGNMENT

DDR(0:3,4:7)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)

SYNC_MASTER=ev11 SYNC_DATE=10/15/2018

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17.2 PHYSICAL CSETS

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR ASSIGNED
CLASS NAME	NONE S,A,X	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLOCK_24M	S	A_DIELECTRIC_3X	=	Y
CLOCK_32K	S	A_DIELECTRIC_3X	=	Y
CIO_D2R	S	A_DIELECTRIC_9X	=	Y
CIO_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_D2R	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_WLBT_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WLBT_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_CLK	S	A_DIELECTRIC_6X	=	Y
LPDP	S	A_DIELECTRIC_6X	=	Y
MIPI_CLK	S	A_DIELECTRIC_5X	=	Y
MIPI_DATA	S	A_DIELECTRIC_5X	=	Y
EUSB	S	A_DIELECTRIC_5X	=	Y
GROUND	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y

RF	S	RF	RF_ANT*	Y

SYNC_MASTER=e11 SYNC_DATE=10/15/2018

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
MIPI_DATA	GROUND	DEFAULT_WITH_4X_TO_SHAPE
MIPI_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
MIPI_DATA	POWER	DEFAULT_WITH_4X_TO_SHAPE
MIPI_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	CIO_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	MIPI_CLK	A_DIELECTRIC_4X
CIO_D2R	MIPI_DATA	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_7X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	MIPI_DATA	A_DIELECTRIC_4X
PCIE_NAND_D2R	MIPI_CLK	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_7X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	MIPI_DATA	A_DIELECTRIC_4X
PCIE_WLBT_D2R	MIPI_CLK	A_DIELECTRIC_4X
MIPI_DATA	MIPI_CLK	A_DIELECTRIC_2X
CIO_R2D	CIO_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X

SYNC_MASTER=11 SYNC_DATE=10/15/2018

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17.2 SPACING CSETS, CLASS-CLASS

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CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-08813	1	PCBA,KANHA,X1711	U0600	CRITICAL	CPU:INTERPOSER

A1 BEST

998-21412	1	SOC,TGA A1+8G,1Y,8C,DEV,CX,H,ATK,MCM2502	U0600	CRITICAL	CPU:SOC_A1_HYNIX_8GB_BEST
998-21413	998-21412	CPU:SOC_A1_HYNIX_8GB_BEST	ALL	SCK	
998-21414	1	SOC,TGA A1+8G,1Y,8C,DEV,CX,H,ATK,MCM2502	U0600	CRITICAL	CPU:SOC_A1_MICRON_8GB_BEST
998-21415	998-21414	CPU:SOC_A1_MICRON_8GB_BEST	ALL	SCK	
998-21416	1	SOC,TGA A1+16G,1Y,8C,DEV,DX,H,ATK,MC2502	U0600	CRITICAL	CPU:SOC_A1_HYNIX_16GB_BEST
998-21417	998-21416	CPU:SOC_A1_HYNIX_16GB_BEST	ALL	SCK	
998-21418	1	SOC,TGA A1+16G,1X,8C,DEV,DX,M,ATK,MC2502	U0600	CRITICAL	CPU:SOC_A1_MICRON_16GB_BEST
998-21420	998-21418	CPU:SOC_A1_MICRON_16GB_BEST	ALL	SCK	

A1 GOOD

998-21421	1	SOC,TGA A1+8G,1Y,7C,DEV,CX,H,ATK,MCM2502	U0600	CRITICAL	CPU:SOC_A1_HYNIX_8GB_GOOD
998-21422	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	SCK	
998-21412	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	ACK	
998-21413	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	SCK	
998-21423	1	SOC,TGA A1+8G,1Y,7C,DEV,CX,H,ATK,MCM2502	U0600	CRITICAL	CPU:SOC_A1_MICRON_8GB_GOOD
998-21424	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	SCK	
998-21414	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	ACK	
998-21415	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	SCK	
998-21426	1	SOC,TGA A1+16G,1Y,7C,DEV,DX,H,ATK,MC2502	U0600	CRITICAL	CPU:SOC_A1_HYNIX_16GB_GOOD
998-21427	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	SCK	
998-21416	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	ACK	
998-21417	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	SCK	
998-21428	1	SOC,TGA A1+16G,1X,7C,DEV,DX,M,ATK,MC2502	U0600	CRITICAL	CPU:SOC_A1_MICRON_16GB_GOOD
998-21429	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	SCK	
998-21418	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	ACK	
998-21420	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	SCK	

B0 BEST

998-22388	1	SOC,TGA B0+8G,1Y,8C,LP,DEV,CX,H,A,M2502	U0600	CRITICAL	CPU:SOC_HYNIX_8GB_BEST
998-22387	998-22388	CPU:SOC_HYNIX_8GB_BEST	ALL	SCK	
998-22386	1	SOC,TGA B0+8G,1Y,8C,LP,DEV,CX,M,A,M2502	U0600	CRITICAL	CPU:SOC_MICRON_8GB_BEST
998-22385	998-22386	CPU:SOC_MICRON_8GB_BEST	ALL	SCK	
998-22392	1	SOC,TGA B0+16G,1Y,8C,LP,DEV,DX,H,A,M2502	U0600	CRITICAL	CPU:SOC_HYNIX_16GB_BEST
998-22391	998-22392	CPU:SOC_HYNIX_16GB_BEST	ALL	SCK	
998-22390	1	SOC,TGA B0+16G,1X,8C,LP,DEV,DX,M,A,M2502	U0600	CRITICAL	CPU:SOC_MICRON_16GB_BEST
998-22389	998-22390	CPU:SOC_MICRON_16GB_BEST	ALL	SCK	

B0 GOOD

998-22404	1	SOC,TGA B0+8G,1Y,7C,LP,DEV,CX,H,A,M2502	U0600	CRITICAL	CPU:SOC_HYNIX_8GB_GOOD
998-22403	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	SCK	
998-22388	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	ACK	
998-22387	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	SCK	
998-22402	1	SOC,TGA B0+8G,1Y,7C,LP,DEV,CX,M,A,M2502	U0600	CRITICAL	CPU:SOC_MICRON_8GB_GOOD
998-22401	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	SCK	
998-22386	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	ACK	
998-22385	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	SCK	
998-22409	1	SOC,TGA B0+16G,1Y,7C,LP,DEV,DX,H,A,M2502	U0600	CRITICAL	CPU:SOC_HYNIX_16GB_GOOD
998-22408	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	SCK	
998-22392	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	ACK	
998-22391	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	SCK	
998-22407	1	SOC,TGA B0+16G,1X,7C,LP,DEV,DX,M,A,M2502	U0600	CRITICAL	CPU:SOC_MICRON_16GB_GOOD
998-22406	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	SCK	
998-22390	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	ACK	
998-22389	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	SCK	

NAND Landing 0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND_L0:S5E_STUDY
335S00462	1	NAND,3DV4,128GBT,XXX,S5E,256G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_TO
335S00470	1	NAND,3DV4,128GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_SD
335S00437	1	NAND,3DV5,128GB,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_HY
335S00489	1	NAND,3DV4,160GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_SD
335S00480	1	NAND,3DV4,160GBT,XXX,S5E,256G,K,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_TO
335S00482	1	NAND,3DV5,320GB,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_HY
335S00481	1	NAND,3DV4,288GBT,XXX,S5E,256G,K,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_TO
335S00474	1	NAND,3DV4,512GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_SD
335S00466	1	NAND,3DV4,512GBT,XXX,S5E,256G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_TO
335S00468	1	NAND,3DV4,1TBT,XXX,S5E,512G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_TO
335S00458	1	NAND,3DV5,1024GBT,S5E,512G,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND_L0:INTERPOSER

NAND Landing 1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND_L1:S5E_STUDY
335S00437	1	NAND,3DV5,128GB,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_HY
335S00470	1	NAND,3DV4,128GBT,XXX,S5E,256G,SD,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_SD
335S00462	1	NAND,3DV4,128GBT,XXX,S5E,256G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_TO
335S00438	1	NAND,3DV5,256GB,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_HY
335S00464	1	NAND,3DV4,256GBT,XXX,S5E,256G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_TO
335S00474	1	NAND,3DV4,512GBT,XXX,S5E,256G,SD,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_SD
335S00466	1	NAND,3DV4,512GBT,XXX,S5E,256G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_TO
335S00468	1	NAND,3DV4,1TBT,XXX,S5E,512G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_TO
335S00458	1	NAND,3DV5,1024GBT,S5E,512G,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND_L1:INTERPOSER

SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20066	1	IC,PMU,SPMU,A0,OTP-JPC,WLCSP196	U7700	CRITICAL	SPMU_IC:DEV
998-22526	1	IC,PMU,SIMETRA,A1,OTP-JPE,WLCSP196	U7700	CRITICAL	SPMU_IC:A1

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20064	1	IC,PMU,MPMU,A0,OTP-JPE,WLCSP440	U8100	CRITICAL	MPMU_IC:DEV
998-22614	1	IC,PMU,SERA,B0,OTP-JPF,WLCSP440	U8100	CRITICAL	MPMU_IC:B0

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BOM OPTION TABLES

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BOM GROUP	BOM OPTIONS
NANDCFG:ITLC_S5E_128G_TO	NAND_L0:ITLC_128G_TO
NANDCFG:ITLC_S5E_128G_SD	NAND_L0:ITLC_128G_SD
NANDCFG:ITLC_S5E_256G_HY	NAND_L0:ITLC_256G_HY,NAND_L1:ITLC_256G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_256G_SD	NAND_L0:ITLC_256G_SD,NAND_L1:ITLC_256G_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_256G_TO	NAND_L0:ITLC_256G_TO,NAND_L1:ITLC_256G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_HY	NAND_L0:ITLC_512G_HY,NAND_L1:ITLC_512G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_TO	NAND_L0:ITLC_512G_TO,NAND_L1:ITLC_512G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_SD	NAND_L0:ITLC_1P0T_SD,NAND_L1:ITLC_1P0T_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_TO	NAND_L0:ITLC_1P0T_TO,NAND_L1:ITLC_1P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_TO	NAND_L0:ITLC_2P0T_TO,NAND_L1:ITLC_2P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_HY	NAND_L0:ITLC_2P0T_HY,NAND_L1:ITLC_2P0T_HY,PARTS_SSDNAND1
NANDCFG:INTERPOSER	NAND_L0:INTERPOSER,NAND_L1:INTERPOSER,PARTS_SSDNAND1
NANDCFG:NONE	NAND_L0:OFF,NAND_L1:OFF,PARTS_SSDNAND1

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BOM GROUPS

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Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
353S01346	353S01320		ALL	rdar://problem/57736570	On Semi	NXP
138S0738	138S1101		ALL	rdar://problem/59471401	Samsung	Murata
138S0846	138S0811		ALL	rdar://problem/59474499	Samsung	Murata
376S1053	376S0604		ALL	rdar://problem/59475163	Diodes Inc	On Semi
152S00359	152S00253		ALL	rdar://problem/57204466	Chilisin	Cyntec
740S00041	740S0159		ALL	rdar://problem/59438907	Bourns	LittleFuse
371S00077	371S00180		ALL	rdar://problem/59475330	NXP	Diodes Inc
376S1106	376S0678		ALL	rdar://problem/59442581	On Semi	Vishay
107S00033	107S00034		ALL	rdar://problem/59471007	TFT	Cyntec
138S00087	138S1086		ALL	rdar://problem/59439865	Taiyo Yuden	Murata
152S00812	152S1701		ALL	rdar://problem/59465659	Chilisin	Cyntec
371S00217	371S00079		ALL	rdar://problem/57739774	ROHM CORP	Nexperia
376S0948	376S00076		ALL	rdar://problem/59134310	Diodes Inc	Toshiba
128S00031	128S00011		ALL	rdar://problem/59071370	ROHM CORP	Kemet
128S00026	128S00011		ALL	rdar://problem/59071370	NEC/Kemet	Kemet
128S00087	128S00011		ALL	rdar://problem/59071370	Panasonic	Kemet
128S0445	128S0436		ALL	rdar://problem/59071568	Panasonic	Kemet
128S0364	128S0264		ALL	rdar://problem/59071705	Kemet	Panasonic
128S00094	128S00067		ALL	rdar://problem/59072397	Tokin/Kemet	Panasonic
128S00039	128S00038		ALL	rdar://problem/59075402	NEC/Kemet	Kemet
128S0302	128S00038		ALL	rdar://problem/59075402	Panasonic	Kemet
152S00680	152S00198		ALL	rdar://problem/59075547	Chilisin	Cyntec
152S00383	152S00198		ALL	rdar://problem/59075547	Vishay	Cyntec
152S00708	152S00265		ALL	rdar://problem/59075783	Chilisin	Cyntec
152S00367	152S01248		ALL	rdar://problem/59076041	NEC	Cyntec
376S00204	376S00203		ALL	rdar://problem/59076791	Diodes Inc	Vishay
376S00226	376S00203		ALL	rdar://problem/59076791	Vishay	Vishay
376S00227	376S00203		ALL	rdar://problem/59076791	Fairchild	Vishay
376S00228	376S1179		ALL	rdar://problem/59077240	On Semi	Vishay
376S00007	376S1179		ALL	rdar://problem/59077240	AOS	Vishay
376S00303	376S00012		ALL	rdar://problem/59077463	Diodes Inc	TI
376S1147	376S00281		ALL	rdar://problem/59077684	On Semi	AOS
107S00071	107S00053		ALL	rdar://problem/59078523	Yageo	Cyntec
107S00029	107S00087		ALL	rdar://problem/59081345	TFT	Yageo
138S00332	138S00328		ALL	rdar://problem/59112527	Kyocera	Murata
138S00047	138S00073		ALL	rdar://problem/59118124	Taiyo	Murata
138S0863	138S0853		ALL	rdar://problem/59118514	Taiyo	Murata
138S00077	138S00035		ALL	rdar://problem/59119189	Taiyo	Murata
138S00093	138S00035		ALL	rdar://problem/59119189	Kyocera	Murata
138S00116	138S00071		ALL	rdar://problem/59119528	Taiyo	Murata
138S00117	138S00071		ALL	rdar://problem/59119528	Kyocera	Murata
138S00229	138S00107		ALL	rdar://problem/59123589	Kyocera	Murata
138S00022	138S0801		ALL	rdar://problem/59124126	Taiyo	Murata
152S00398	152S00204		ALL	rdar://problem/59129606	Taiyo	Cyntec
152S00963	152S00885		ALL	rdar://problem/59129928	Taiyo	Cyntec
152S00343	152S00839		ALL	rdar://problem/59130255	Murata	Cyntec
152S01317	152S01268		ALL	rdar://problem/59130415	Taiyo	Cyntec
152S00997	152S00476		ALL	rdar://problem/59130875	Chilisin	Murata
152S01090	152S01085		ALL	rdar://problem/59131117	Chilisin	Murata
107S00055	107S00090		ALL	rdar://problem/59082308	Cyntec	TFT
107S00365	107S00373		ALL	rdar://problem/59081538	Cyntec	TFT
152S01344	152S00883		ALL	rdar://problem/59353109	Chilisin	Cyntec
152S00979	152S00874		ALL	rdar://problem/59364196	Taiyo	Cyntec
197S00046	197S00036		ALL	rdar://problem/59408673	Epson	TXC
197S00047	197S00036		ALL	rdar://problem/59408673	Kyocera	TXC
197S00048	197S00036		ALL	rdar://problem/59408673	Murata	TXC
138S00181	138S0835		ALL	rdar://problem/59408752	Samsung	Murata
138S00291	138S0835		ALL	rdar://problem/59408752	Kyocera	Murata
377S00166	377S00160		ALL	rdar://problem/59407974	Semtech	On Semi
138S00330	138S00081		ALL	rdar://problem/59408911	SEMCO	Murata
740S0118	740S00028		ALL	rdar://problem/59408586	Polytronics	Bussmann
377S00123	377S00031		ALL	rdar://problem/59407768	Semtech	On Semi
377S00186	377S00060		ALL	rdar://problem/59407847	Semtech	ST Micro

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
371S00220	371S00181		ALL	rdar://problem/59404055	On Semi	Diodes Inc
371S00085	371S00190		ALL	rdar://problem/59404601	On Semi	Diodes Inc
353S00852	353S4262		ALL	rdar://problem/59403423	On Semi	Diodes Inc
311S00156	311S00129		ALL	rdar://problem/59489090	Nexperia	TI
376S1080	376S0820		ALL	rdar://problem/59489026	Diodes Inc	On Semi
138S00049	138S0831		ALL	rdar://problem/59408798	Kyocera	Murata
311S00269	311S00234		ALL	rdar://problem/59489341	Nexperia	TI
311S00176	311S00153		ALL	rdar://problem/59489111	Diodes Inc	TI
311S00178	311S00177		ALL	rdar://problem/59489119	On Semi	TI
376S1128	376S00282		ALL	rdar://problem/59489044	Diodes Inc	On Semi
376S00224	376S00282		ALL	rdar://problem/59489044	Nexperia	On Semi
128S00093	128S00009		ALL	rdar://problem/59125761	Tokin/Kemet	Kemet
128S00103	128S00009		ALL	rdar://problem/59125761	Samsung	Kemet
128S00106	128S00009		ALL	rdar://problem/59361958	Tokin/Kemet	Kemet
128S00107	128S00009		ALL	rdar://problem/59361958	Kemet	Kemet
128S00110	128S00009		ALL	rdar://problem/59361958	Samsung	Kemet
376S1137	376S00019		ALL	rdar://problem/59489062	Vishay	Diodes Inc
107S00101	107S00005		ALL	TBD	Yageo	Cyntec
107S00102	107S00017		ALL	TBD	Yageo	Cyntec
107S0276	107S00020		ALL	TBD	Cyntec	TFT
107S00370	107S00371		ALL	TBD	Yageo	Cyntec
107S00372	107S00371		ALL	TBD	Vishay	Cyntec
107S00298	107S0208		ALL	TBD	TDK	Murata
107S0150	107S0208		ALL	TBD	Panasonic	Murata
116S00007	116S00006		ALL	TBD	Vishay	Yageo
132S0409	132S00064		ALL	TBD	Taiyo Yuden	Murata
132S00012	132S0401		ALL	TBD	Murata	Taiyo Yuden
138S00084	138S00060		ALL	TBD	Taiyo Yuden	Murata
138S0750	138S00097		ALL	TBD	Murata	Taiyo Yuden
138S00284	138S00136		ALL	TBD	Kyocera	Murata
138S0852	138S0818		ALL	TBD	Samsung	Murata
138S0789	138S0941		ALL	TBD	Samsung	Murata
155S0275	155S00188		ALL	TBD	Taiyo Yuden	Murata
155S0706	155S0302		ALL	TBD	Taiyo Yuden	Murata
155S0741	155S0361		ALL	TBD	Murata	TDK
155S0823	155S0644		ALL	TBD	TDK and Taiyo	Murata
155S00007	155S0667		ALL	TBD	Taiyo Yuden	Panasonic
155S00190	155S0914		ALL	TBD	Taiyo Yuden	Panasonic
138S0706	138S0739		ALL	rdar://problem/59571431	Murata	Samsung
311S00267	311S00244		ALL	TBD	Nexperia	TI
311S00268	311S00246		ALL	TBD	Nexperia	TI
311S00060	311S0273		ALL	TBD	Diodes Inc	Philips
311S00013	311S0508		ALL	TBD	Diodes Inc	NXP
353S02402	353S1429		ALL	TBD	ON Semi	TI
353S02440	353S3698		ALL	rdar://problem/59682314	ON Semi	TI
740S0144	740S00028		ALL	TBD	Bussman	LittleFuse
138S00343	138S00329		ALL	rdar://problem/60090733	Kyocera	Murata
376S00292	376S1140		ALL	rdar://problem/60290671	Nexperia	Diodes Inc.
740S00081	740S00053		ALL	rdar://problem/60394183	Bourns	AEMI

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EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
	685-00339	COMMON PARTS,MLB,X1757	MLB_COMMON
	685-00377	PARTS,SSDNAND1,MLB,X1757	SSD_2L
PP22	939-08408	PCBA,MLB,DCDC,X1757	DCDC_COMMON,DEV_PARTS_BOM,ALTERNATE,NANDCFG:INTERPOSER,CPU:INTERPOSER
	985-01176	DEV PARTS,MLB,X1757	MLB_DEV
Pxxx	939-10388	PCBA,MLB,MSQ,X1757	CMN_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY

SOC (BEST), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PNR5	639-10741	PCBA,MLB,BEST,SOC,HY-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1P6	639-11700	PCBA,MLB,BEST,SOC,HY-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PNR7	639-10743	PCBA,MLB,BEST,SOC,HY-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1P7	639-11701	PCBA,MLB,BEST,SOC,HY-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1P8	639-11702	PCBA,MLB,BEST,SOC,HY-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1P9	639-11703	PCBA,MLB,BEST,SOC,HY-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY
PNR9	639-10745	PCBA,MLB,BEST,SOC,HY-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1PC	639-11704	PCBA,MLB,BEST,SOC,HY-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
PNRD	639-10747	PCBA,MLB,BEST,SOC,HY-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
PNRG	639-10749	PCBA,MLB,BEST,SOC,HY-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1PD	639-11705	PCBA,MLB,BEST,SOC,HY-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PVD4	639-10924	PCBA,MLB,BEST,SOC,MI-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1PF	639-11706	PCBA,MLB,BEST,SOC,MI-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PVD6	639-10926	PCBA,MLB,BEST,SOC,MI-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1PG	639-11707	PCBA,MLB,BEST,SOC,MI-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1PH	639-11708	PCBA,MLB,BEST,SOC,MI-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1PJ	639-11709	PCBA,MLB,BEST,SOC,MI-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY
Q1PK	639-11710	PCBA,MLB,BEST,SOC,MI-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1PL	639-11711	PCBA,MLB,BEST,SOC,MI-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
Q1PM	639-11712	PCBA,MLB,BEST,SOC,MI-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
Q1PN	639-11713	PCBA,MLB,BEST,SOC,MI-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1PP	639-11714	PCBA,MLB,BEST,SOC,MI-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2D9	639-11752	PCBA,MLB,GOOD,SOC,HY-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2DC	639-11753	PCBA,MLB,GOOD,SOC,HY-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2DD	639-11754	PCBA,MLB,GOOD,SOC,HY-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2DF	639-11755	PCBA,MLB,GOOD,SOC,HY-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2DG	639-11756	PCBA,MLB,GOOD,SOC,HY-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2DH	639-11757	PCBA,MLB,GOOD,SOC,HY-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2DJ	639-11758	PCBA,MLB,GOOD,SOC,HY-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2DK	639-11759	PCBA,MLB,GOOD,SOC,HY-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2DL	639-11760	PCBA,MLB,GOOD,SOC,HY-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2DM	639-11761	PCBA,MLB,GOOD,SOC,HY-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2DN	639-11762	PCBA,MLB,GOOD,SOC,HY-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2DP	639-11763	PCBA,MLB,GOOD,SOC,MI-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2DQ	639-11764	PCBA,MLB,GOOD,SOC,MI-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2DR	639-11765	PCBA,MLB,GOOD,SOC,MI-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2DT	639-11766	PCBA,MLB,GOOD,SOC,MI-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2DV	639-11767	PCBA,MLB,GOOD,SOC,MI-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2DW	639-11768	PCBA,MLB,GOOD,SOC,MI-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2DX	639-11769	PCBA,MLB,GOOD,SOC,MI-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2DY	639-11770	PCBA,MLB,GOOD,SOC,MI-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2F0	639-11771	PCBA,MLB,GOOD,SOC,MI-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2F1	639-11772	PCBA,MLB,GOOD,SOC,MI-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2F2	639-11773	PCBA,MLB,GOOD,SOC,MI-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

SOC (BEST), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PNR6	639-10742	PCBA,MLB,BEST,SOC,HY-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1PQ	639-11715	PCBA,MLB,BEST,SOC,HY-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PNR8	639-10744	PCBA,MLB,BEST,SOC,HY-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1PR	639-11716	PCBA,MLB,BEST,SOC,HY-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1PT	639-11717	PCBA,MLB,BEST,SOC,HY-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1PV	639-11718	PCBA,MLB,BEST,SOC,HY-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_512G_HY
PNRC	639-10746	PCBA,MLB,BEST,SOC,HY-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1PW	639-11719	PCBA,MLB,BEST,SOC,HY-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
PNRF	639-10748	PCBA,MLB,BEST,SOC,HY-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
PNRH	639-10750	PCBA,MLB,BEST,SOC,HY-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1PX	639-11720	PCBA,MLB,BEST,SOC,HY-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PVD5	639-10925	PCBA,MLB,BEST,SOC,MI-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1PY	639-11721	PCBA,MLB,BEST,SOC,MI-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PVD7	639-10927	PCBA,MLB,BEST,SOC,MI-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1Q0	639-11722	PCBA,MLB,BEST,SOC,MI-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1Q1	639-11723	PCBA,MLB,BEST,SOC,MI-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1Q2	639-11724	PCBA,MLB,BEST,SOC,MI-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_512G_HY
Q1Q3	639-11725	PCBA,MLB,BEST,SOC,MI-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1Q4	639-11726	PCBA,MLB,BEST,SOC,MI-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
Q1Q5	639-11727	PCBA,MLB,BEST,SOC,MI-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
Q1Q6	639-11728	PCBA,MLB,BEST,SOC,MI-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1Q7	639-11729	PCBA,MLB,BEST,SOC,MI-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2F3	639-11774	PCBA,MLB,GOOD,SOC,HY-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2F4	639-11775	PCBA,MLB,GOOD,SOC,HY-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2F5	639-11776	PCBA,MLB,GOOD,SOC,HY-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2F6	639-11777	PCBA,MLB,GOOD,SOC,HY-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2F7	639-11778	PCBA,MLB,GOOD,SOC,HY-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2F8	639-11779	PCBA,MLB,GOOD,SOC,HY-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2F9	639-11780	PCBA,MLB,GOOD,SOC,HY-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2FC	639-11781	PCBA,MLB,GOOD,SOC,HY-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2FD	639-11782	PCBA,MLB,GOOD,SOC,HY-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2FF	639-11783	PCBA,MLB,GOOD,SOC,HY-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2FG	639-11784	PCBA,MLB,GOOD,SOC,HY-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2FH	639-11785	PCBA,MLB,GOOD,SOC,MI-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2FJ	639-11786	PCBA,MLB,GOOD,SOC,MI-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2FK	639-11787	PCBA,MLB,GOOD,SOC,MI-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2FL	639-11788	PCBA,MLB,GOOD,SOC,MI-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2FM	639-11789	PCBA,MLB,GOOD,SOC,MI-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2FN	639-11790	PCBA,MLB,GOOD,SOC,MI-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2FP	639-11791	PCBA,MLB,GOOD,SOC,MI-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2FQ	639-11792	PCBA,MLB,GOOD,SOC,MI-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2FR	639-11793	PCBA,MLB,GOOD,SOC,MI-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2FT	639-11794	PCBA,MLB,GOOD,SOC,MI-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2FV	639-11795	PCBA,MLB,GOOD,SOC,MI-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

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