

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.


T668 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
9	0024017707	ENGINEERING RELEASED		2020-06-23

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1	1	TABLE OF CONTENTS		
2	2	REFERENCE DESIGN SYNC TABLES	T668_MLB	07/17/2019
3	4	PD PARTS	T668_KSAITO_MLB_0.11.1	
4	5	SOC: Support	T585_REF_SOC_H13G_0.56.0	
5	6	SOC: CIO, USB, RESETS, CLOCKS, SWD	AITKEN_T668_MLB	10/08/2019
6	7	SOC: AP I/Os	T585_REF_SOC_H13G_0.56.0	
7	8	SOC: LPDP & MIPI	AITKEN_T668_MLB	10/08/2019
8	9	SOC: PCIE	ANDREW_T668_MLB	10/09/2019
9	10	SOC: AOP	T585_REF_SOC_H13G_0.56.0	
10	11	SOC: POWER (DDR,SRAM)	T585_REF_SOC_H13G_0.56.0	
11	12	SOC: POWER (IO)	T585_REF_SOC_H13G_0.56.0	
12	13	SOC: POWER (SOC, CPU, GPU)	T585_REF_SOC_H13G_0.56.0	
13	14	SOC: POWER (SRAM)	T585_REF_SOC_H13G_0.56.0	
14	15	SOC: POWER (Fixed, PLL's, Filtered)	T585_REF_SOC_H13G_0.56.0	
15	16	SOC: GND	T585_REF_SOC_H13G_0.56.0	
16	17	SOC: GND-2	T585_REF_SOC_H13G_0.56.0	
17	19	SPI NOR	REF_SOC_H13G	01/27/2020
18	21	PROJECT SUPPORT (1/2)	AITKEN_T668_MLB	09/18/2019
19	22	PROJECT SUPPORT (2/2)	AITKEN_T668_MLB	11/11/2019
20	50	Secure Element	REF_SR_CRRS	02/26/2020
21	51	BATTERY CONNECTORS	AITKEN_T668_MLB	09/18/2019
22	52	PBUS SUPPLY & BATTERY CHARGER	REF_CHARGER_SUONA	06/23/2020
23	53	BATTERY CHARGER SUPPORT	REF_CHARGER_SUONA	06/23/2020
24	54	PBUS SUPPORT	KELVIN_T668_MLB	05/12/2020
25	57	POWER: 3V8 AON (1/2)	REF_VR_ICEMAN	06/15/2020
26	58	POWER: 3V8 AON (2/2)	REF_VR_ICEMAN	06/15/2020
27	59	POWER: 3V8 AON SUPPORT	T585_REF_VR_ICEMAN_0.36.0	
28	77	PMU: SLAVE INPUT PWR & BUCKS	KELVIN_T668_MLB	04/07/2020
29	78	PMU: SLAVE LDO	KELVIN_T668_MLB	04/07/2020
30	79	PMU: SLAVE GPIO & GND	KELVIN_T668_MLB	05/09/2020
31	80	PMU: SLAVE SUPPORT	KELVIN_T668_MLB	01/27/2020
32	81	PMU: MASTER INPUT PWR & BUCKS	KELVIN_T668_MLB	04/02/2020
33	82	PMU: MASTER BUCKS & GND	KELVIN_T668_MLB	06/22/2020
34	83	PMU: MASTER LDO & GPIO	KELVIN_T668_MLB	06/04/2020
35	84	PMU: MASTER SUPPORT	KELVIN_T668_MLB	04/16/2020
36	121	POWER: EXTERNAL LDO	KELVIN_T668_MLB	09/23/2019
37	123	POWER: 5V S2	REF_VR_5V_TPS62135	04/16/2020
38	124	POWER: 3V3 S2, 5V S2 SUPPORT	T668_MLB	03/26/2020
39	127	POWER: 3V3 S2	REF_VR_3V3_TPS62135	01/09/2020
40	128	POWER: FETS	KELVIN_T668_MLB	09/10/2019
41	130	I2C: SIO, DISP	T668_MLB	06/20/2019
42	131	I2C: ISP, AOP	T668_MLB	06/20/2019
43	132	I2C: SMC	KELVIN_T668_MLB	12/20/2019
44	135	SENSORS: POWER HIGH SIDE (1/2)	KELVIN_T668_MLB	05/28/2020
45	136	SENSORS: POWER HIGH SIDE (2/2)	KELVIN_T668_MLB	05/26/2020
46	138	SENSORS: POWER LOW SIDE (1/2)	KELVIN_T668_MLB	05/26/2020
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48	140	SENSORS: POWER SUPPORT	KELVIN_T668_MLB	05/13/2020
49	141	SENSORS: THERMAL (1/2)	KELVIN_T668_MLB	04/02/2020
50	142	SENSORS: THERMAL (2/2)	KELVIN_T668_MLB	01/23/2020
51	144	SENSORS: MOTION	WUDI_T668_MLB	09/23/2019
52	145	FAN	AITKEN_T668_MLB	09/18/2019
53	150	USB-C: High Speed ATC0	REF_USBC_ACE2	02/14/2020
54	151	USB-C: High Speed ATC1	REF_USBC_ACE2	02/14/2020
55	152	USB-C: Support 1 ATC01	REF_USBC_ACE2	02/01/2020
56	153	USB-C: Support 2 ATC01	REF_USBC_ACE2	02/01/2020
57	154	USB-C: Port Controller ATC0	REF_USBC_ACE2	02/01/2020
58	155	USB-C: Port Controller ATC1	REF_USBC_ACE2	02/01/2020
59	156	USB-C: Connector(s)	KELVIN_T668_MLB	02/01/2020
60	157	USB-C: HS Level Shifters	REF_USBC_ACE2	02/04/2020

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61	158	USB-C: SUPPORT	T585_REF_USBC_ACE2_0.23.0	
62	200	WIFI/BT: MODULE	KELVIN_T668_MLB	05/05/2020
63	201	WIFI/BT: ANTENNA and GND	REF_WIRELESS_RASPUTIN	02/01/2020
64	220	STORAGE: SSD0 S5E <0>	REF_STORAGE_S5E	04/27/2020
65	221	STORAGE: SSD0 S5E <1>	REF_STORAGE_S5E	04/27/2020
66	224	STORAGE: NON OCARINA SUPPORT	REF_STORAGE_NON_OCARINA_SUPPORT02/25/2020	
67	230	STORAGE: SSD SUPPORT	WUDI_T668_MLB	01/28/2020
68	236	DISPLAY: CONNECTOR, PWR	AITKEN_T668_MLB	10/02/2019
69	237	DISPLAY POWER SEQUENCER	REF_PANELPWR_BNJ	04/22/2020
70	238	BEN: CONTROLLER	REF_BLC_BEN	11/21/2019
71	239	BEN: KEYBOARD	REF_BLC_BEN	11/21/2019
72	242	SECDIS: AMR	T585_REF_SECDIS_AMR_0.9.0	
73	243	SECDIS: FPGA	REF_SECDIS_SAK	06/18/2020
74	244	AUDIO SUPPORT	REF_SPKRAMP_TAS5770	04/16/2020
75	245	AUDIO JACK CODEC	REF_CODEC_CLIFDEN	04/13/2020
76	246	AUDIO AMPLIFIERS (1/2)	REF_SPKRAMP_TAS5770	04/16/2020
77	247	AUDIO AMPLIFIERS (2/2)	REF_SPKRAMP_TAS5770	04/16/2020
78	248	AUDIO CONNECTORS: AMPS	KELVIN_T668_MLB	09/18/2019
79	249	AUDIO CONNECTORS: DMIC, JACK	KELVIN_T668_MLB	09/24/2019
80	250	KEYBOARD BLC CONNECTORS	T668_MLB	05/16/2019
81	251	KEYBOARD IOX, SUPPORT	WUDI_T668_MLB	06/16/2020
82	252	KEYBOARD SIGNAL CONNECTOR, ESD	WUDI_T668_MLB	01/28/2020
83	253	TRACKPAD SUPPORT	WUDI_T668_MLB	05/21/2020
84	254	TRACKPAD CONNECTOR	WUDI_T668_MLB	04/16/2020
85	256	TOUCHID SUPPORT	T585_REF_MESA_SUPPORT_0.11.0	
86	257	DFR SUPPORT 1	T585_REF_DFR_V3_SUPPORT_0.25.0	
87	258	DFR SUPPORT 2	T585_REF_DFR_V3_SUPPORT_0.25.0	
88	266	FCT	KELVIN_T668_MLB	01/29/2020
89	270	DEBUG: BUTTONS	T668_MLB	06/20/2019
90	271	DEBUG: MISC	T668_MLB	06/20/2019
91	278	DEBUG: LEDS (1/3)	T668_MLB	07/24/2019
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93	280	DEBUG: LEDS (3/3)	T668_MLB	07/24/2019
94	282	DEBUG: P3V8AON ISENSE	T668_MLB	06/20/2019
95	294	DEBUG: VITAMIN-C	MANAN_T668_MLB	02/03/2020
96	300	DESENSE (1/3)	KELVIN_T668_MLB	11/04/2019
97	301	DESENSE (2/3)	KELVIN_T668_MLB	09/30/2019
98	302	DESENSE (3/3)	KELVIN_T668_MLB	09/30/2019
99	310	EMC	KELVIN_T668_MLB	10/02/2019
100	400	POWER ALIASES 1	KELVIN_T668_MLB	11/06/2019
101	401	POWER ALIASES 2	KELVIN_T668_MLB	11/06/2019
102	402	POWER ALIASES 3	T668_MLB	06/05/2019
103	403	POWER ALIASES 4	KELVIN_T668_MLB	11/06/2019
104	404	POWER ALIASES 5	KELVIN_T668_MLB	09/12/2019
105	405	SIGNAL ALIASES 1	AITKEN_T668_MLB	09/18/2019
106	406	SIGNAL ALIASES 2	T668_MLB	05/29/2019
107	500	17.2 RULES	T668_MLB	05/13/2019
108	501	17.2 PHYSICAL CSETS	T668_MLB	05/13/2019
109	502	17.2 SPACING CSETS, ISO	T668_MLB	05/13/2019
110	503	17.2 SPACING CSETS, CLASS-CLASS	T668_MLB	05/13/2019
111	600	BOM VARIANT TABLES	T668_MLB	06/05/2018
112	601	BOM OPTION TABLES	T668_MLB	06/05/2018
113	602	BOM GROUPS	T668_MLB	06/05/2018
114	610	BOM ALTS	T668_MLB	06/05/2018
115	611	BOM CUSTOMIZATIONS	T668_MLB	06/05/2018
116	700	PACK OPTIONS	T668_MLB	06/05/2018
117	999	CHECKPLUS SUPPORT	T668_MLB	08/29/2019

LAST_MODIFICATION=Mon Jun 22 13:41:32 2020

DRAWING TITLE		SCHEM, MLB, X1799	
 Apple Inc.	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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REFERENCE DESIGNS J293 SYNC FROM

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
T585	REF_VR_ICEMAN	57,58	1.18.0		2020/05/11
T585	REF_CHARGER_SUONA	52,53	0.39.0		2020/05/15
T585	REF_STORAGE_NON_OCARINA_SUPPORT	224	0.5.0		2020/04/27
T585	REF_SPKRAMP_TAS5770	244,246,247	0.8.0		2020/04/27
T585	REF_VR_3V3_TP862135	127	0.8.0		2020/04/27
T585	REF_VR_5V_LT8642S	123	0.13.0		2020/04/27
T585	REF_DFR_V3_SUPPORT	257,258	0.25.0		2020/04/27
T585	REF_SR_CERES	50	0.13.0		2020/04/27
T585	REF_PANELPWR_BNJ	237	0.9.0		2020/04/27
T585	REF_SECDIS_SAK	243	0.42.0		2020/04/30
T585	REF_STORAGE_S5E	220,221	0.34.0		2020/04/27


REFERENCE DESIGNS J293 NO LONGER SYNC FROM

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
T585	REF_SOC_H13G	5-17,19			
T585	REF_PMU_SERA_SIMETRA	77-79,81-83			
T585	REF_BLC_BEN	238,239			
T585	REF_DEBUG_STUFF	294			
T585	REF_SECDIS_AMR	242			
T585	REF_USBC_ACE2	150-155,157			
T585	REF_WIRELESS_RASPUTIN	200-201			
T585	REF_MESA_SUPPORT	256			
T585	REF_KBD_SUPPORT	251			
T585	REF_CODEC_CLIPDEN	245			

<-- WE STOPPED SYNCING SOC AT 0.56.0 DUE TO REF DESIGN DESENSE CAP ADDITIONS CONFLICTING WITH DESENSE TEAM'S REQUESTS FOR J293
 <-- WE STOPPED SYNCING PMU AT 0.57.0 DUE TO SLOW UPDATES
 <-- WE STOPPED SYNCING BLC AT 0.16.0 TO RELAX PLACE NEARS
 <-- WE STOPPED SYNCING VITAMIN C AT 0.1.0 SINCE THE REF DESIGN IS INCOMPLETE AND MANY CHANGES ARE NEEDED TO SUPPORT VIT C MK II
 <-- WE STOPPED SYNCING AMR REF SINCE THE REF HAS A DIFFERENT APN FOR AMR FOOTPRINT THAN PD USES IN J293'S MCO
 <-- WE STOPPED SYNCING USB AT 0.31.0 AS THE 50V CC CAPS WHICH ARE 2.8X MORE EXPENSIVE THAN THE 25V ONES, ALSO LSF0102 COMBO ADDED
 <-- WE STOPPED SYNCING RASPUTIN TO ADD RF CONN BOM OPTION, CHANGE 100M CLK TPS TO PPS, AND FIX OVERLAPPING IPU TEXT NOTES
 <-- WE STOPPED SYNCING MESA SUPPORT AT 0.11.0 SINCE THE REF DESIGN REMOVED A PULL UP AND WE NEED 1V85 ON THE LDO, ALSO RT650 VALUE
 <-- WE STOPPED SYNCING KBD AT 0.25.0 TO FIX CREP GENERATION ERROR ON PIN Y8
 <-- WE STOPPED SYNCING CLIPDEN AT 1.6.0 TO ADD A PULL UP TO FIX A GLITCH <RDAR://63982608>

REFERENCE DESIGNS WHERE NET NUDGE WAS NEEDED TO REMOVE CREFER ERRORS
S5E, USBC, SECDIS SAK

REFERENCE DESIGNS WHERE BYPASS CONSTRAINTS WERE RELAXED
DFR, CODEC, AMPS

SYNC_MASTER=T668_MLB		SYNC_DATE=07/17/2019	
PAGE TITLE REFERENCE DESIGN SYNC TABLES			
 Apple Inc.	DRAWING NUMBER	051-05399	
	REVISION	9.0.0	
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TOP SIDE STANDOFFS

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0400
2.80D1.2ID-1.49H-SM
860-01216

ALLOW_APPLE_PREFIX=Z
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2.80D1.2ID-1.49H-SM
860-01216

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0402
2.80D1.2ID-1.49H-SM
860-01216

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0403
2.80D1.2ID-1.49H-SM
860-01216

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0404
2.80D1.2ID-1.49H-SM
860-01216

ALLOW_APPLE_PREFIX=Z
CRITICAL
Z0405
2.80D1.2ID-1.49H-SM
860-01216

DFR WASHER

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4.75OD2.73ID-H0.2
RING-TH
860-01519

USB-C BOSS

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860-00392

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3.40D1.75ID-1.12H-SM
860-00392

DFR BOSS

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CRITICAL
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3.40D1.75ID-1.5H-SM
860-01484

BOTTOM SIDE STANDOFFS

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860-01485

ALLOW_APPLE_PREFIX=Z
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860-01485

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860-01485

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860-01485

TRACKPAD BOSS

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860-00381

ALLOW_APPLE_PREFIX=Z
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860-00381

CPU THERM STAGE HOLE 3.15 MM

OMIT
CRITICAL
ZT0400
3P9R3P15
998-0845
CORNER NEAREST KEYBOARD

CPU THERM STAGE HOLES 3.6 MM

OMIT
CRITICAL
ZT0401
4.0R3.6-NSP
998-03850

OMIT
CRITICAL
ZT0402
4.0R3.6-NSP
998-03850

CPU THERM STAGE HOLE OVAL

OMIT
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TH-NSP
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WIFI COAX STANDOFF

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FAN MTG HOLE 2.0X2.6 MM

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MLB MTG HOLES 2.1X3.51 MM

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998-19711

OMIT
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SL-2.1X3.51-4.6X6.01
998-19711

OMIT
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WIFI WASHER

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RING-TH
860-01519

AJ FLEX COWLING BOSS

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OMIT
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998-04440

OMIT
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998-04440

OMIT
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998-04440

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998-04440

OMIT
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TH-NSP
SL-1.2X0.4-1.5X0.7
998-04440

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SM-1
870-09667

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SM-1
870-09667

ALLOW_APPLE_PREFIX=PP
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POGO-2.30D-4.0H-SM
SM-1
870-09667

ALLOW_APPLE_PREFIX=PP
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POGO-2.30D-4.0H-SM
SM-1
870-09667

FENCE SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-24457	1	FENCE,SPMU,X1727	FENCE_SPMU	CRITICAL	FENCE_SPMU_C770
806-24550	1	FENCE,SPMU,SUS,SBP,X1727	FENCE_SPMU	CRITICAL	FENCE_SPMU_SUS

FENCE COMBO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-27099	1	FENCE,COMBO,X1727	FENCE_COMBO	CRITICAL	FENCE_COMBO

FENCE USBC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-24455	1	FENCE,BURNSIDE BRIDGE,X1727	FENCE_USBC	CRITICAL	FENCE_USBC_C770
806-24548	1	FENCE,BURNSIDE BRIDGE,SUS,SBP,X1727	FENCE_USBC	CRITICAL	FENCE_USBC_SUS

METAL SLED <RDAR://63760455>

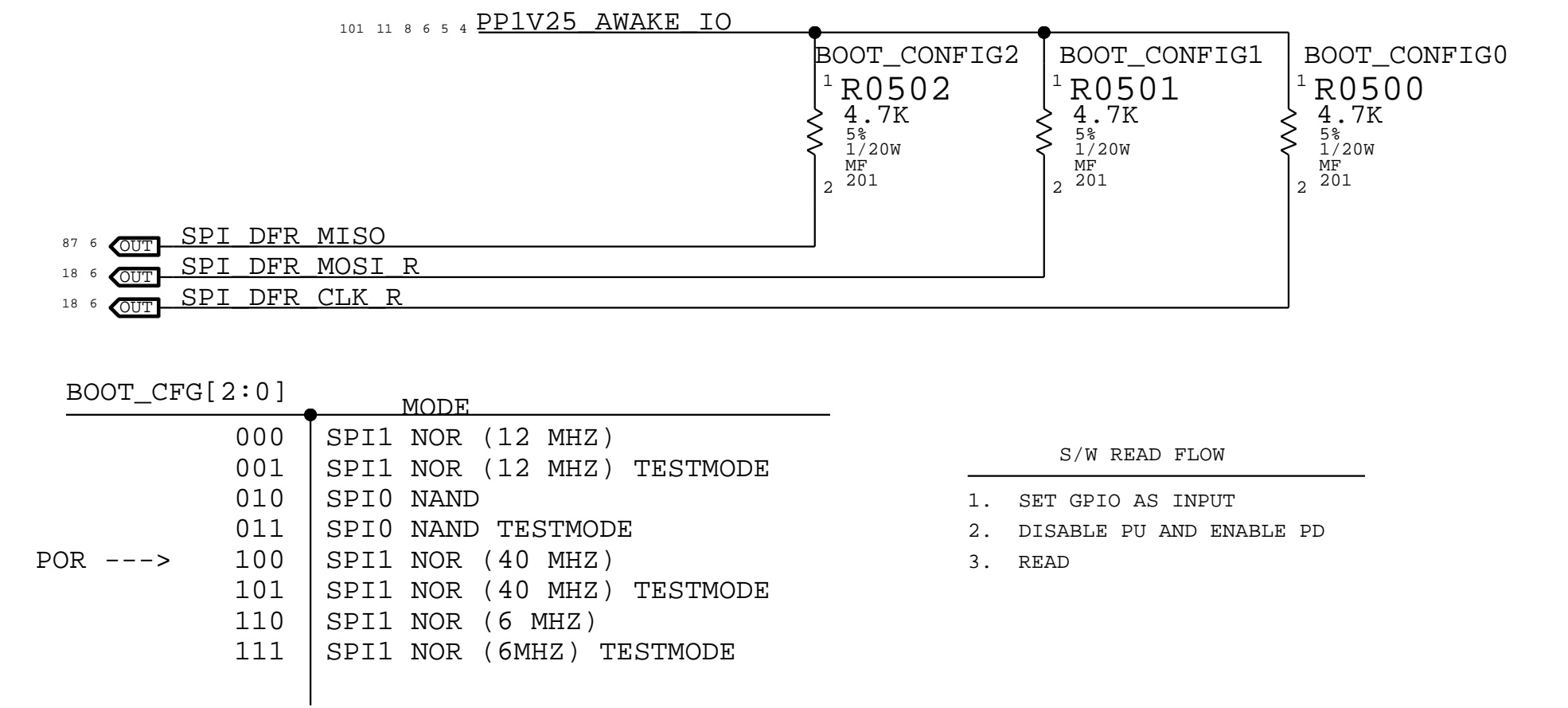
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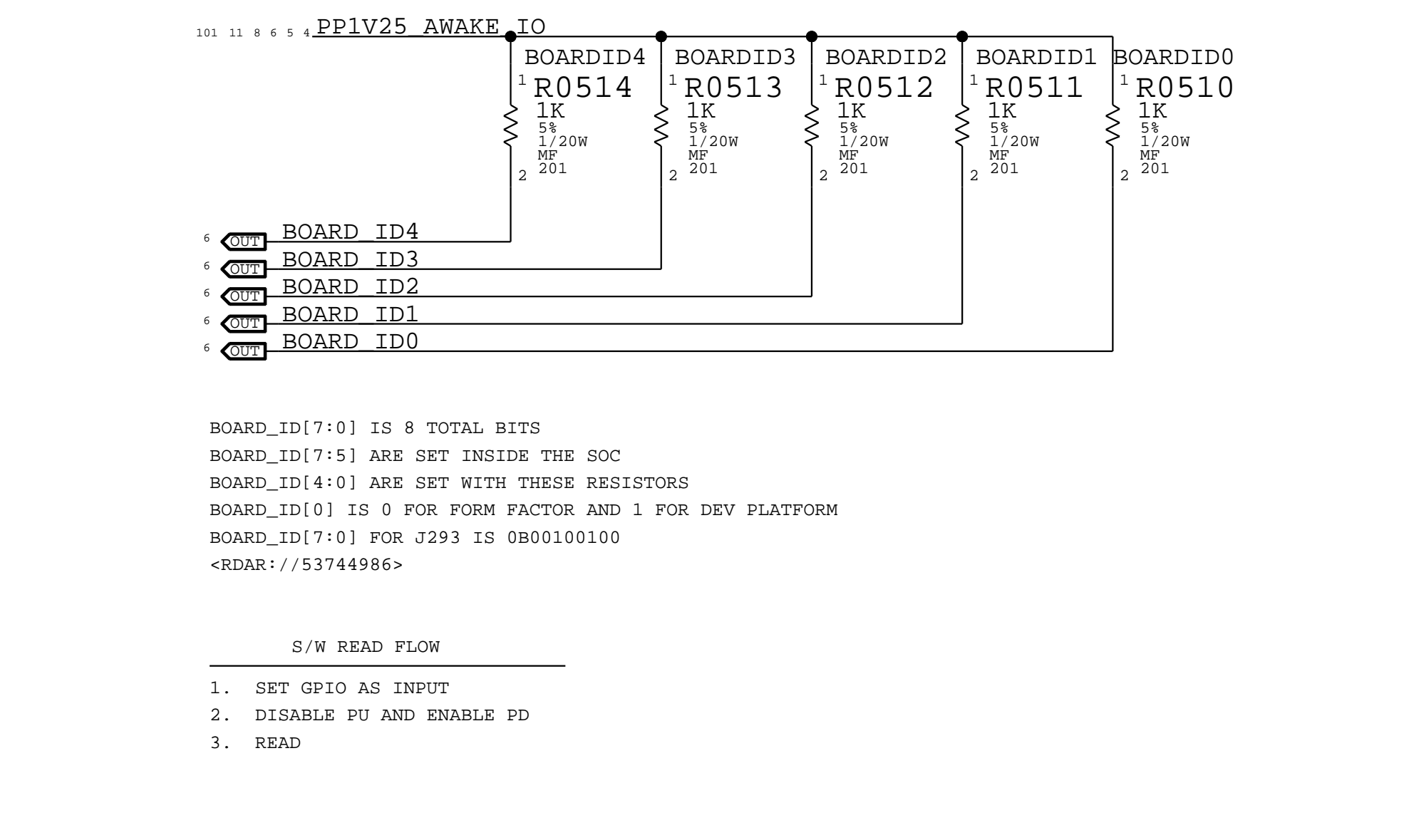
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OK2INTEGRATE

BOOT CONFIG ID

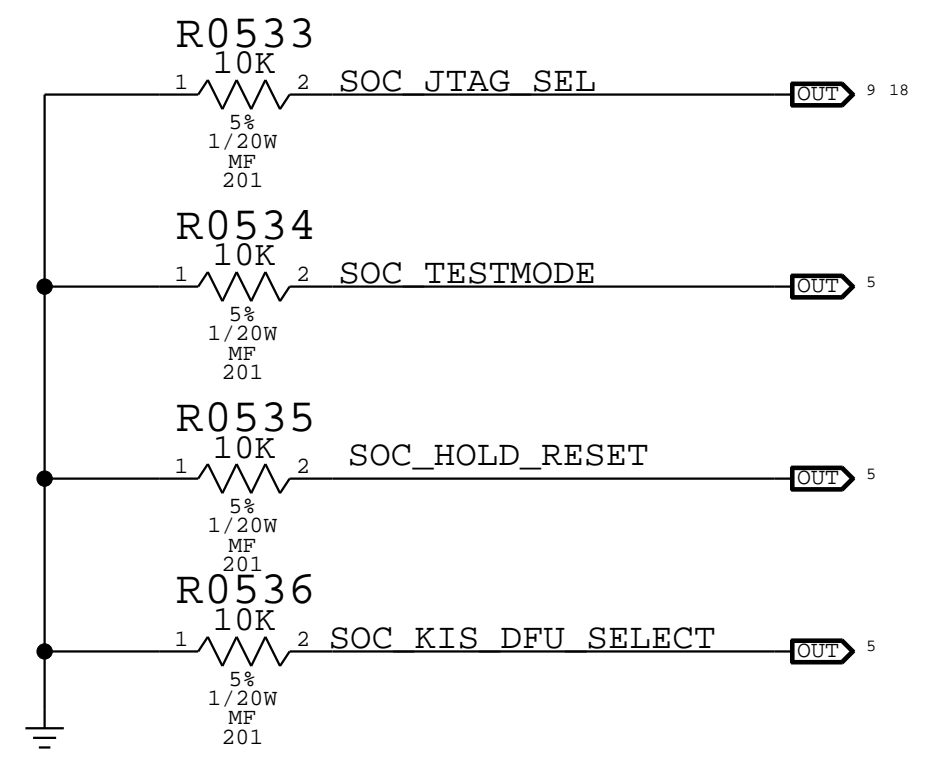
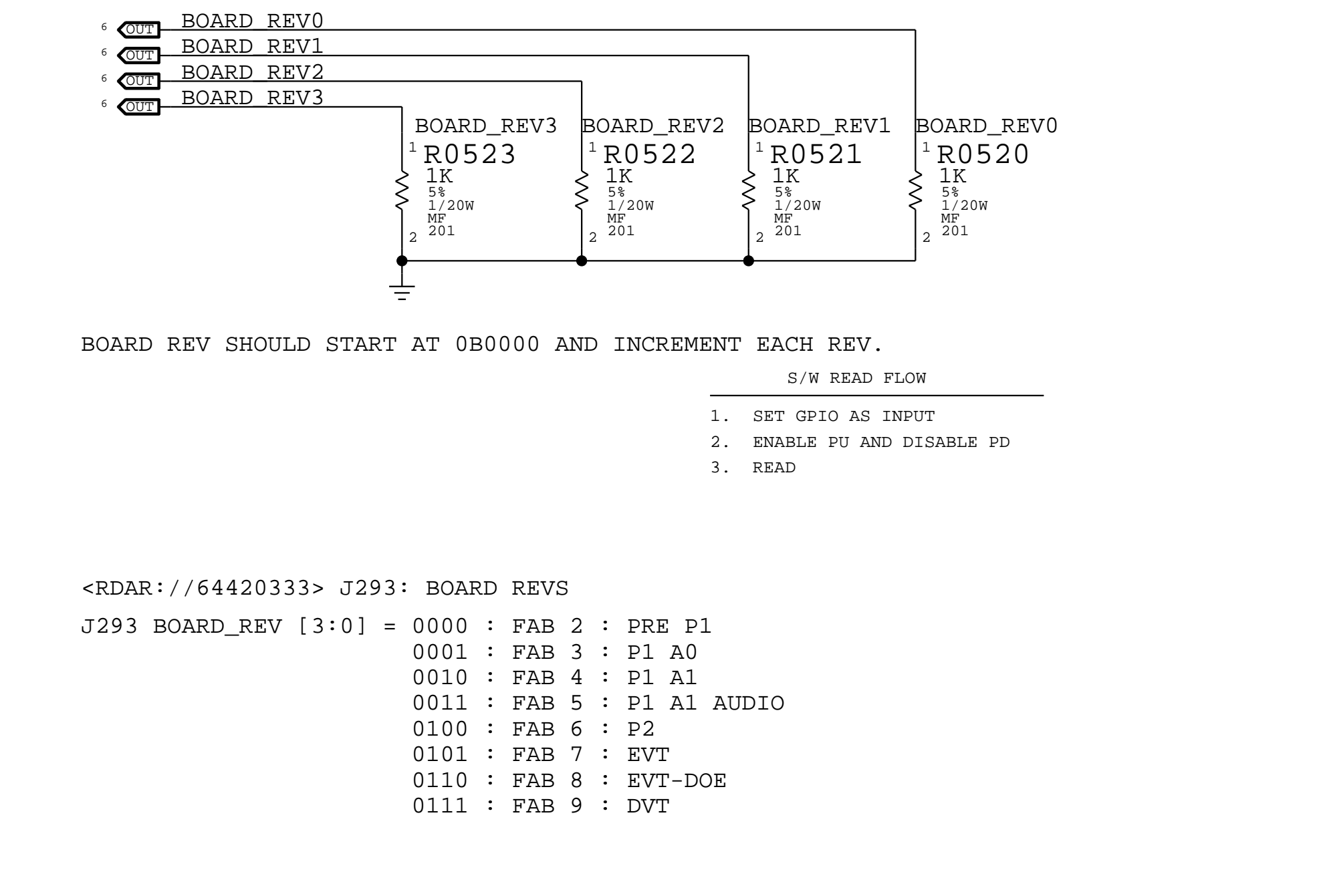


BOARD ID



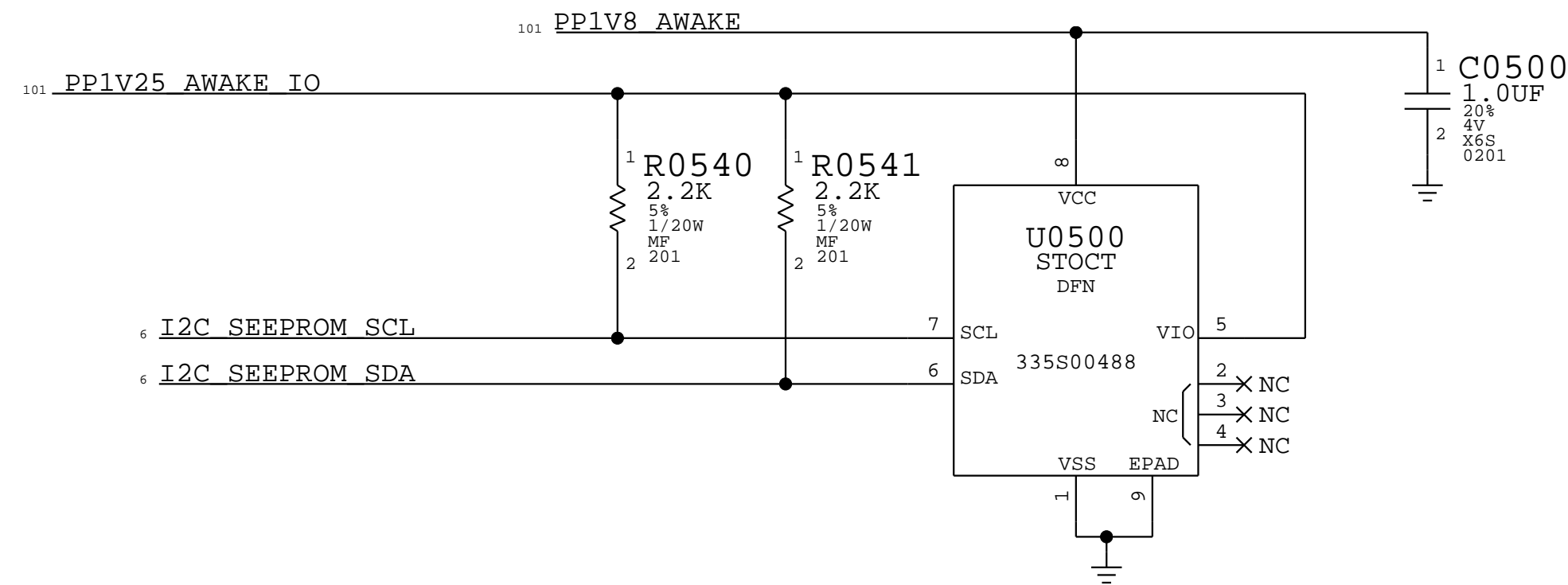
BOARD REVISION

NOTE: STUFFING RESISTOR MEANS 0



SEP EEPROM (128-Kbit)

(Write: 0xA2, Read 0xA3)
A1 PER <RDAR://59029073>



BOM_COST_GROUP=SOC

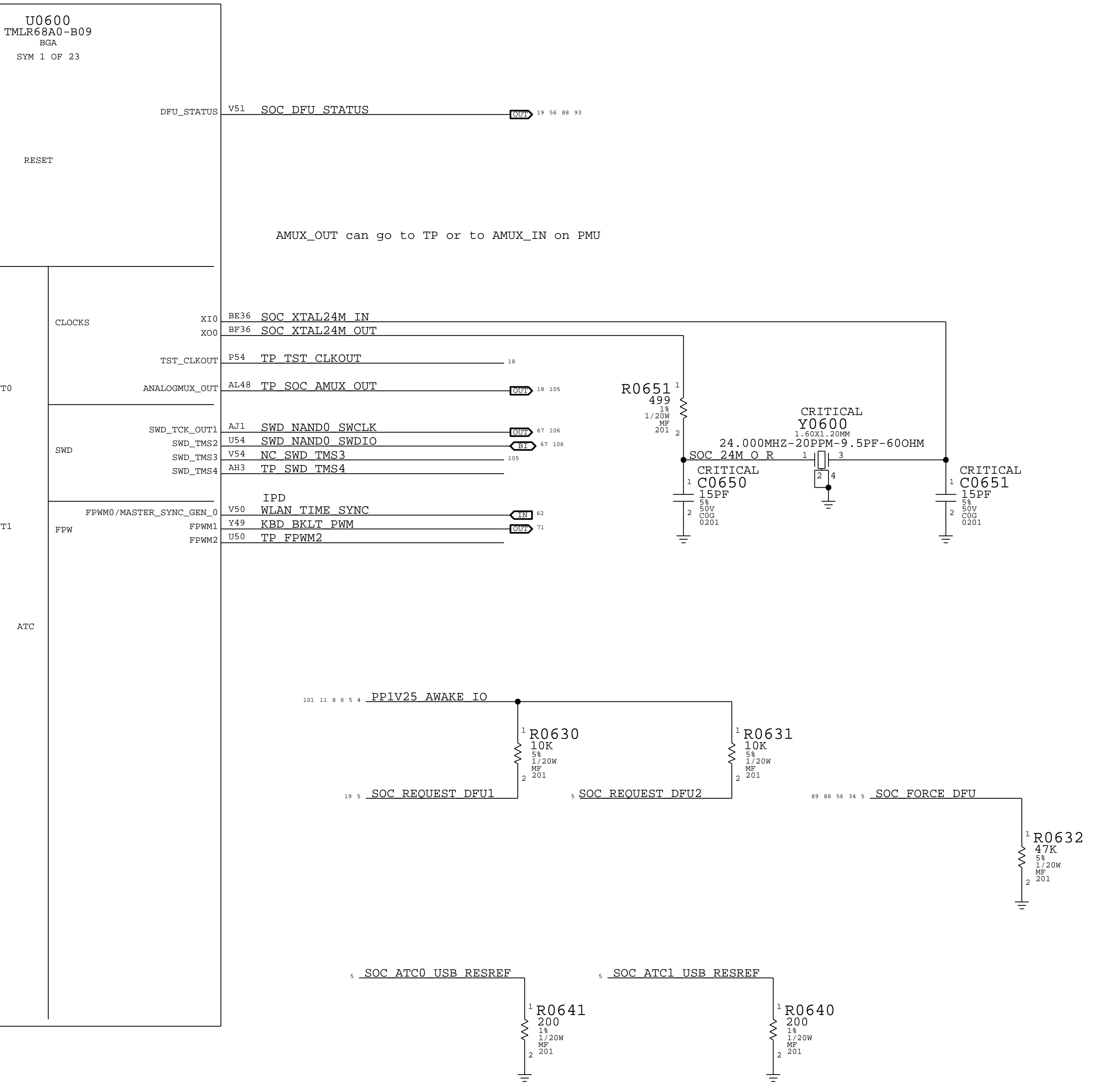
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	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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	SHEET	4 OF 117

SOC: CIO, USB, DRAM, RESETS, CLOCKS, SWD, FPWM

OMIT_TABLE

U0600
TMLR68A0-B09
BGA
SYM 1 OF 23

99 89 88 73 34 9	PMU RESET L	R2	LP4_IN_RESET_N
89 88 56 34 5	SOC FORCE DFU	AA49	FORCE_DFU
19 5	SOC REQUEST DFU1	AK55	REQUEST_DFU1
5	SOC REQUEST DFU2	AJ54	REQUEST_DFU2
4	SOC TESTMODE	AD2	TESTMODE_IPD
93 88 55 34	PMU ACTIVE READY	AL54	CFSB
4	SOC HOLD RESET	AC1	HOLD_RESET_IPD
4	SOC KIS DFU SELECT	AB49	KIS_DFU_SELECT
18	EUSB ATC0 P	BB54	ATC0_USB_EDP
18	EUSB ATC0 N	BB55	ATC0_USB_EDM
60	CIO ATC0 LSRX 1V2	BE18	USB_C0_LSRX
60	CIO ATC0 LSTX 1V2	BE13	USB_C0_LSTX
5	SOC ATC0 USB RESREF	BB53	ATC0_USB_RESREF
106	TMU CLKOUT 0	V48	USB_C0_HPD/TMU_CLK_OUT0
18	EUSB ATC1 P	BC54	ATC1_USB_EDP
18	EUSB ATC1 N	BC55	ATC1_USB_EDM
60	CIO ATC1 LSRX 1V2	BD3	USB_C1_LSRX
60	CIO ATC1 LSTX 1V2	BE10	USB_C1_LSTX
5	SOC ATC1 USB RESREF	BC53	ATC1_USB_RESREF
106	TMU CLKOUT 1	R48	USB_C1_HPD/TMU_CLK_OUT1
5	USB VBUS DETECT	AG1	EUSB_VBUS_DETECT
53	USBC ATC0 D2R P<1>	GND_VOIDD=TRUE	BE50
53	USBC ATC0 D2R N<1>	GND_VOIDD=TRUE	BF50
53	USBC ATC0 R2D C P<1>	GND_VOIDD=TRUE	BC49
53	USBC ATC0 R2D C N<1>	GND_VOIDD=TRUE	BD49
53	USBC ATC0 D2R P<2>	GND_VOIDD=TRUE	BE48
53	USBC ATC0 D2R N<2>	GND_VOIDD=TRUE	BF48
53	USBC ATC0 R2D C P<2>	GND_VOIDD=TRUE	BC47
53	USBC ATC0 R2D C N<2>	GND_VOIDD=TRUE	BD47
53	USBC ATC0 AUX P	AY51	ATCPHY0_AUX_P
53	USBC ATC0 AUX N	AY52	ATCPHY0_AUX_N
5	SOC ATCPHY0 RCAL POS	BE52	ATCPHY0_RCAL_P
5	SOC ATCPHY0 RCAL NEG	BF52	ATCPHY0_RCAL_N
54	USBC ATC1 D2R P<1>	GND_VOIDD=TRUE	BF44
54	USBC ATC1 D2R N<1>	GND_VOIDD=TRUE	BE44
54	USBC ATC1 R2D C P<1>	GND_VOIDD=TRUE	BD43
54	USBC ATC1 R2D C N<1>	GND_VOIDD=TRUE	BC43
54	USBC ATC1 D2R P<2>	GND_VOIDD=TRUE	BF46
54	USBC ATC1 D2R N<2>	GND_VOIDD=TRUE	BE46
54	USBC ATC1 R2D C P<2>	GND_VOIDD=TRUE	BD45
54	USBC ATC1 R2D C N<2>	GND_VOIDD=TRUE	BC45
54	USBC ATC1 AUX P	BA52	ATCPHY1_AUX_P
54	USBC ATC1 AUX N	BA51	ATCPHY1_AUX_N
5	SOC ATCPHY1 RCAL POS	BF42	ATCPHY1_RCAL_P
5	SOC ATCPHY1 RCAL NEG	BE42	ATCPHY1_RCAL_N



OK2INTEGRATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON, 24MHZ, XTAL
197S0588	197S0591		Y0600	TXC, 24MHZ, XTAL

SYNCH: MASTER-ATTRIB: 0600_0600
SYNCH: DATE: 10/08/2014

PAGE TITLE
SOC: CIO, USB, RESETS, CLOCKS, SWD

Apple Inc.

DRAWING NUMBER	051-05399	SIZE	D
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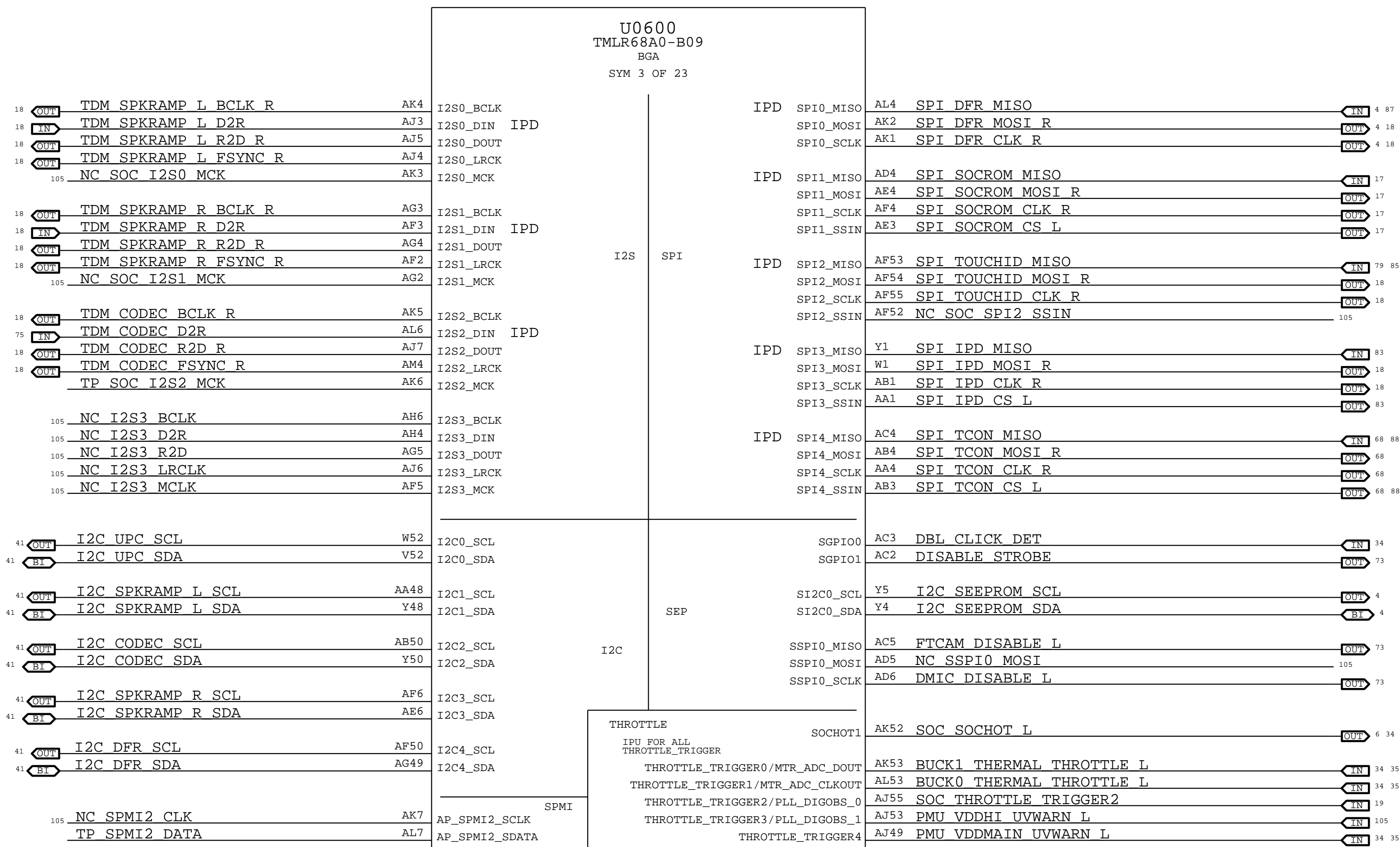
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OK2INTEGRATE

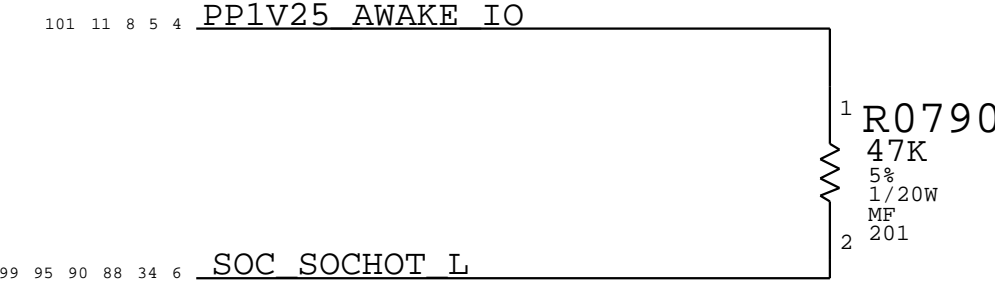
all signals are 1.2 unless otherwise specified.
all signals on this page reference PP1V2_AWAKE_GRP if they are 1.2V
if they are 1.8V they reference PP1V8_AWAKE_GRP

SOC: I/Os



1.8V IO

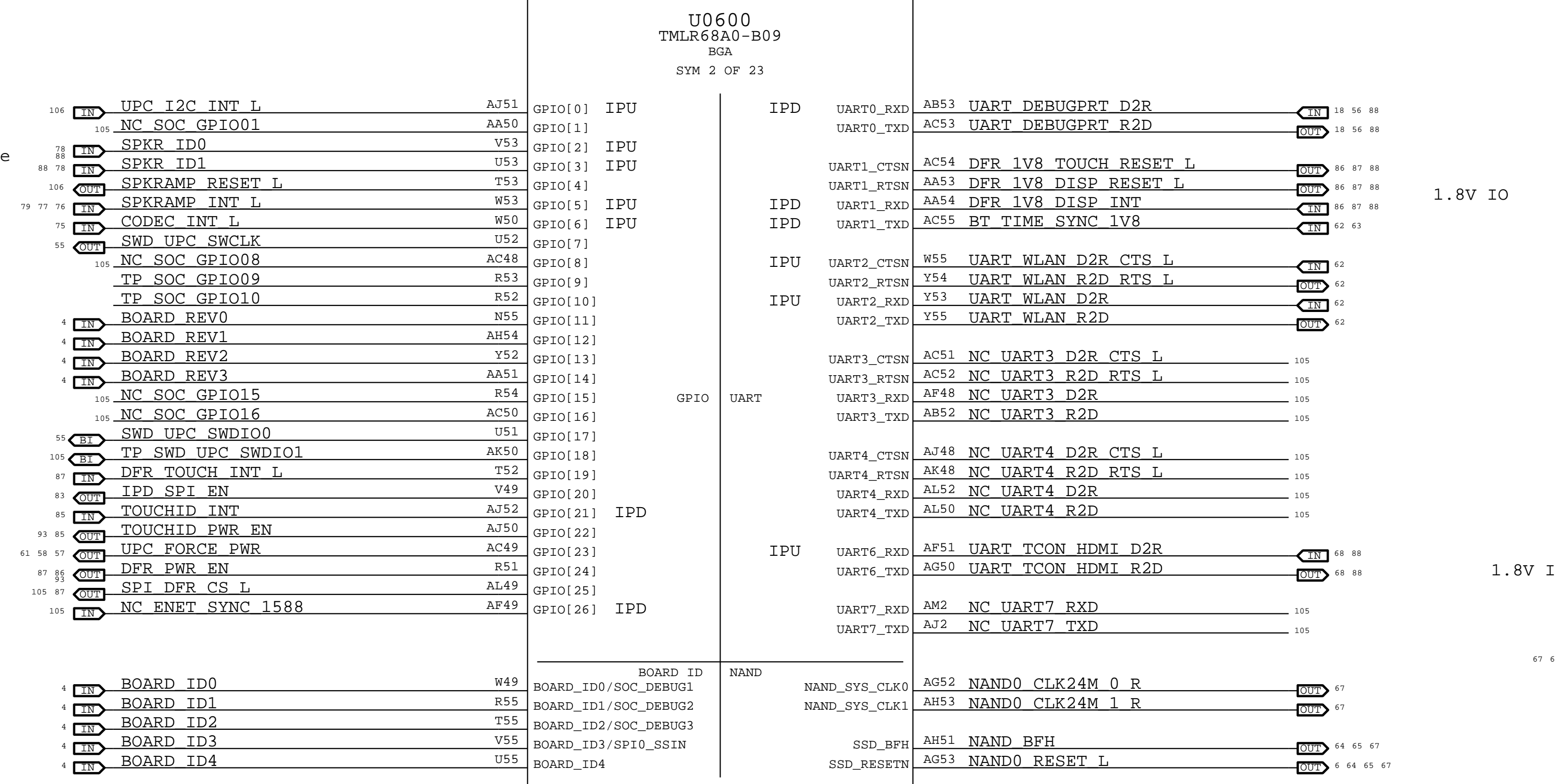
1.8V IO



UPC_FORCE_PWR will likely be removed in the future

TOUCHID_PWR_EN gets pulled up to S2 on TOUCHID page
This is OK because the GPIO is failsafe

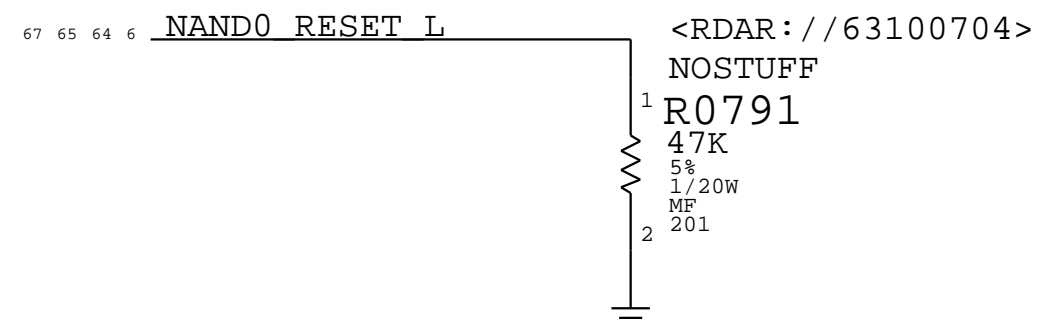
PD needed on DFR PAGE



1.8V IO

Use UART2 if your wireless module is 1.2V IO

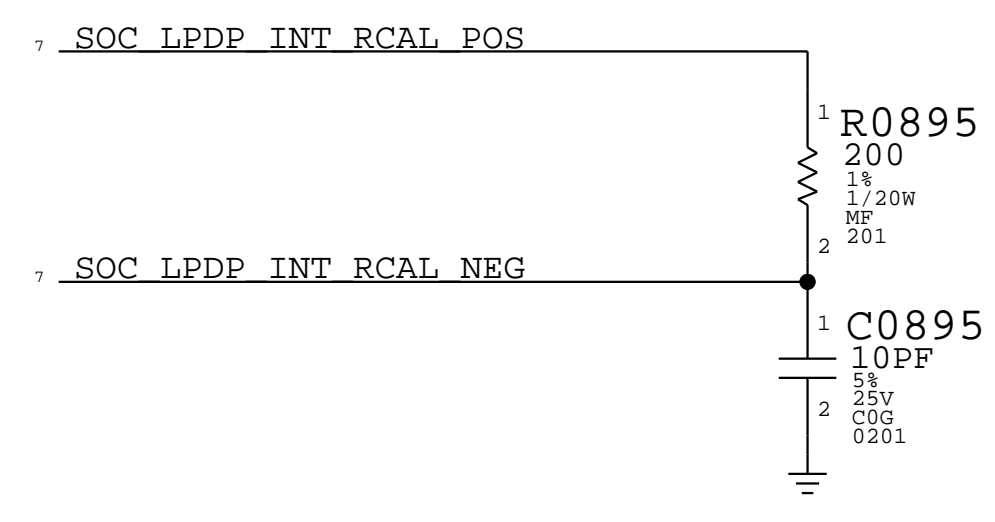
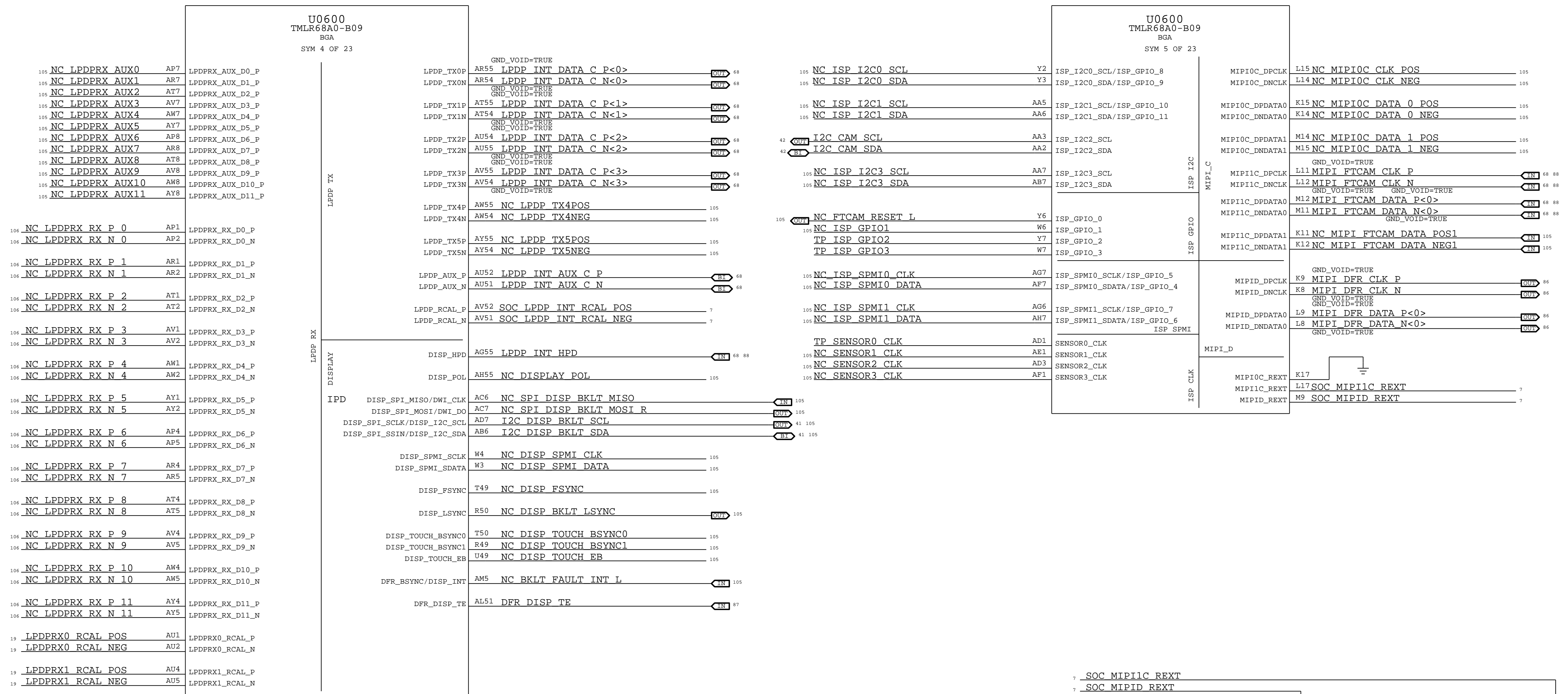
1.8V IO R2D is for desktop only



BOM_COST_GROUP=SOC

PAGE TITLE		
SOC: AP I/Os		
Apple Inc.		DRAWING NUMBER 051-05399
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SOC: LPDP & MIPI



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SOC: LPDP & MIPI		
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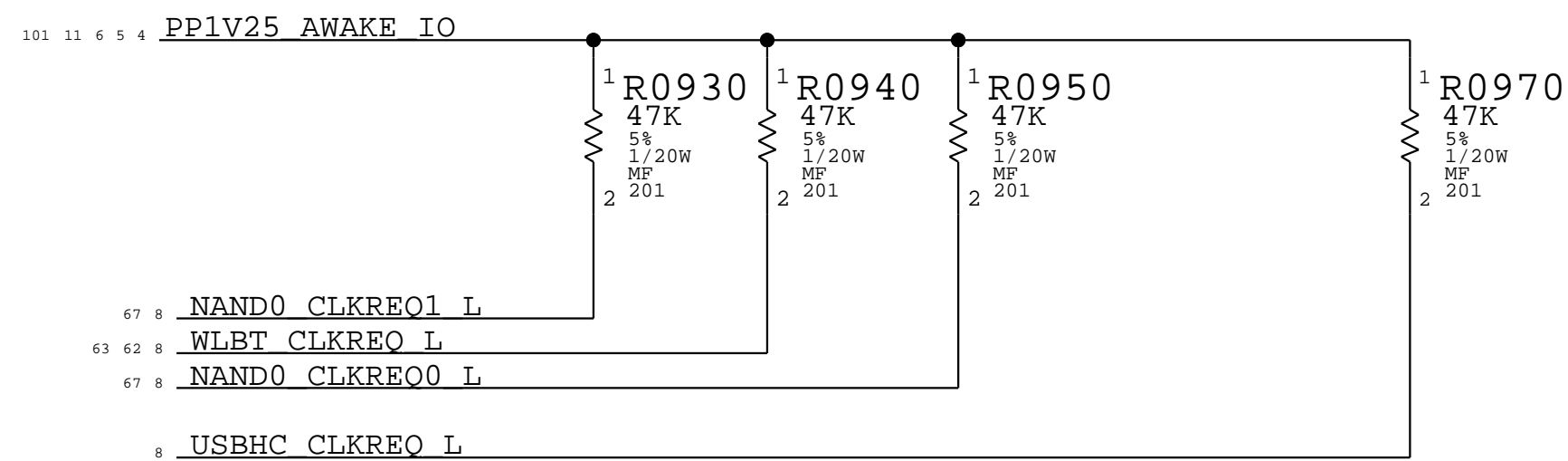
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SOC: PCIE

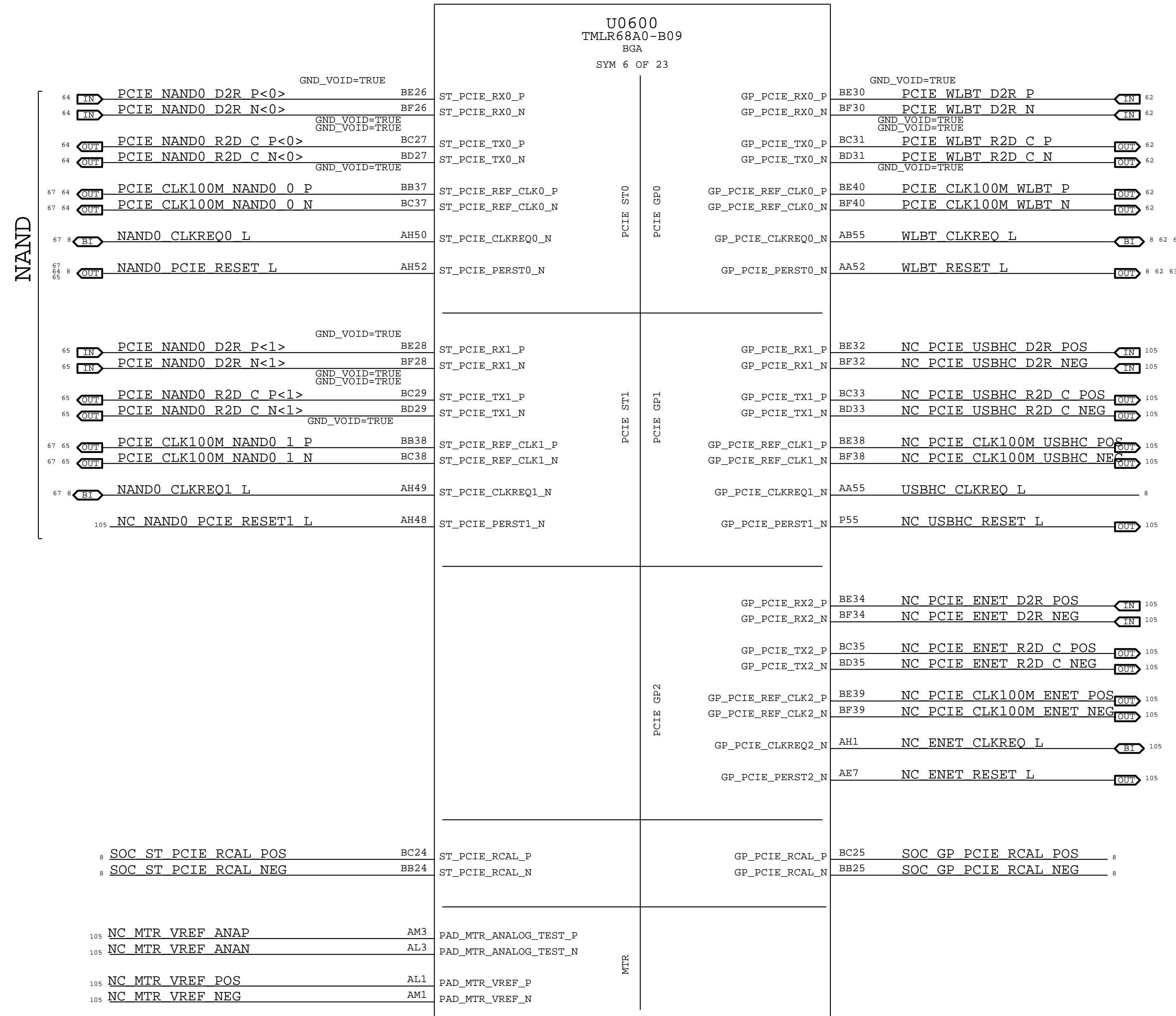
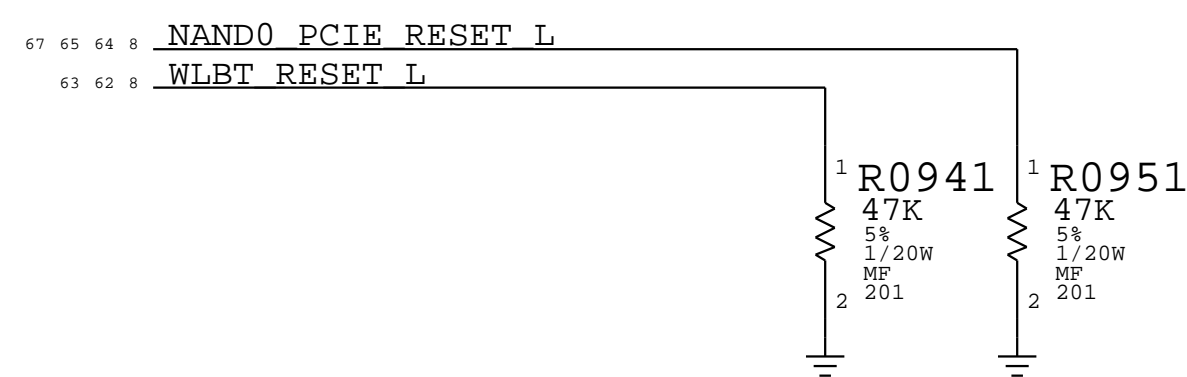
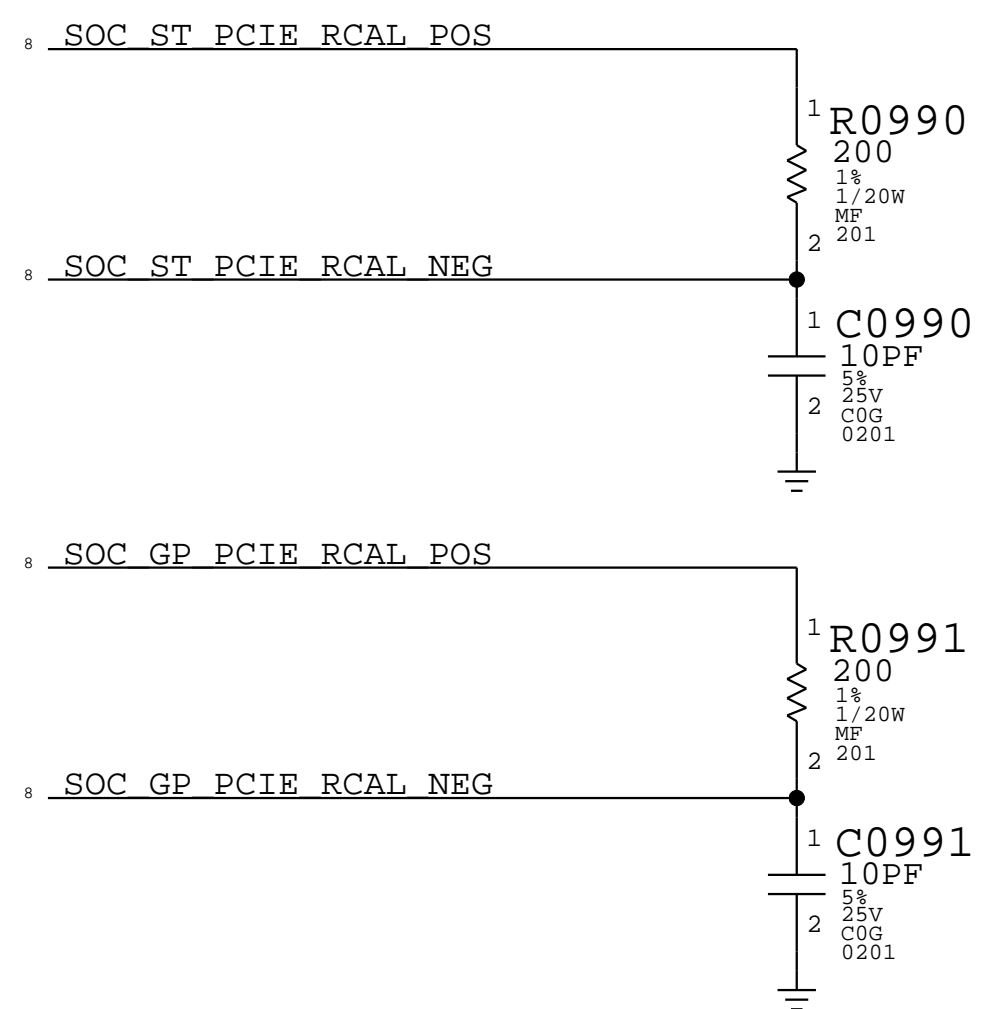
OK2INTEGRATE

PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
75 NF AND 265 NF FOR GEN1/2 AND BETWEEN
176 NF AND 265 NF FOR GEN 3/4

R0970 IS NEEDED DUE TO RDAR://53793006



TO BE CHECKED WITH SEG- DO NOT MATCH WITH SILVAL
IS THE PULL-UP VOLTAGE CORRECT?



WLAN/BT

USB3 CTLR

ENET/SD

PAGE TITLE		SOC: PCIE	
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BOM_COST_GROUP=SOC

SOC: AOP

U0600
TMLR68A0-B09
BGA

SYM 7 OF 23

D

D

output if gyro, input for radar

I2C0 is ALS for portables

C

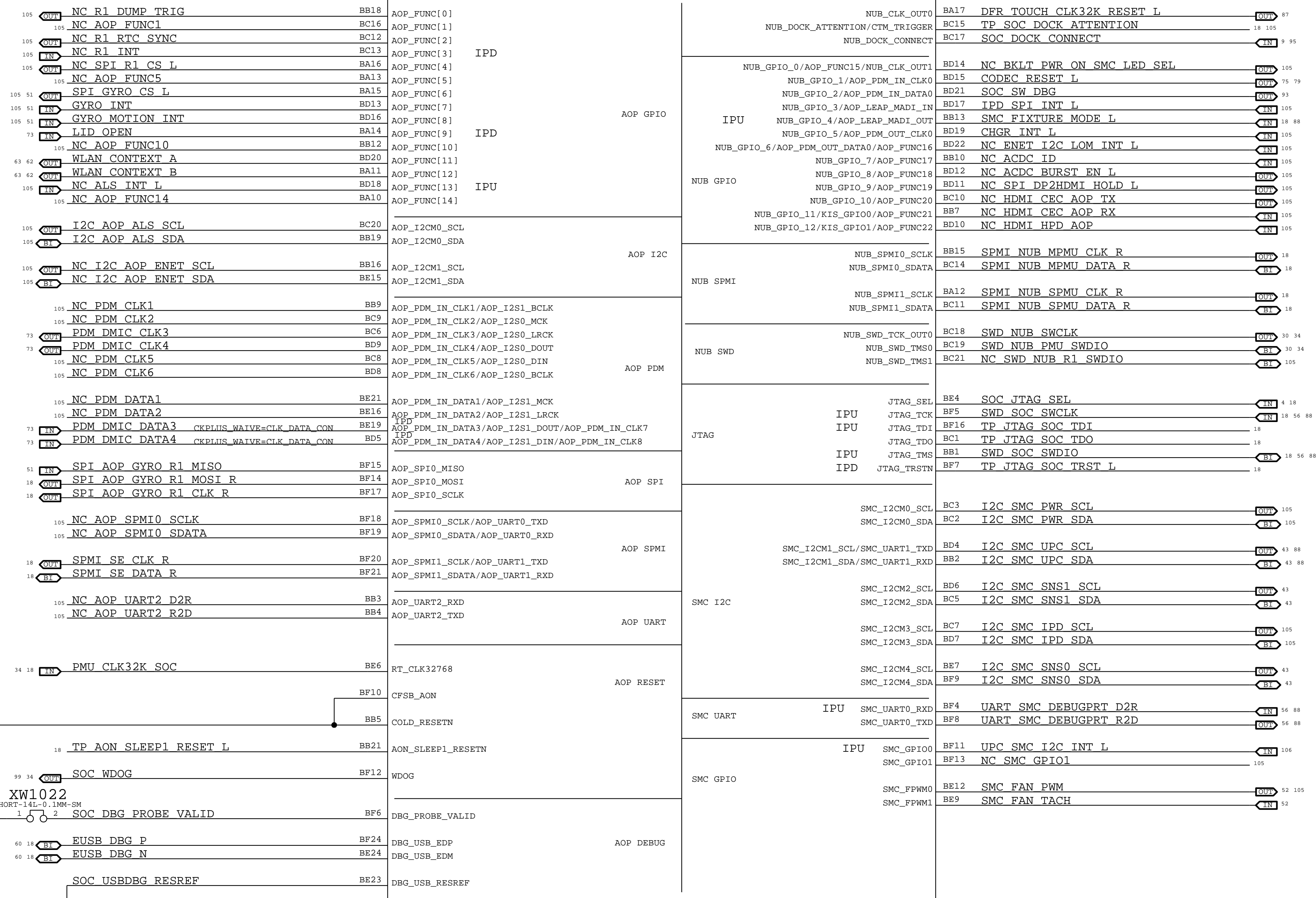
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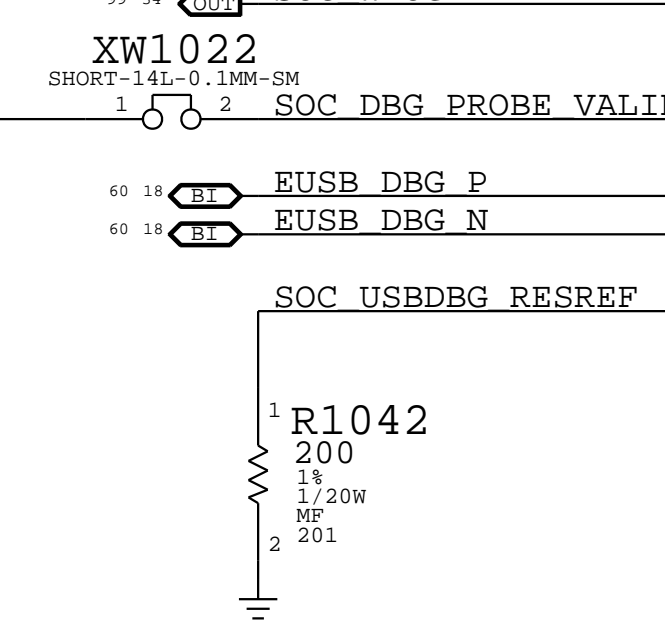
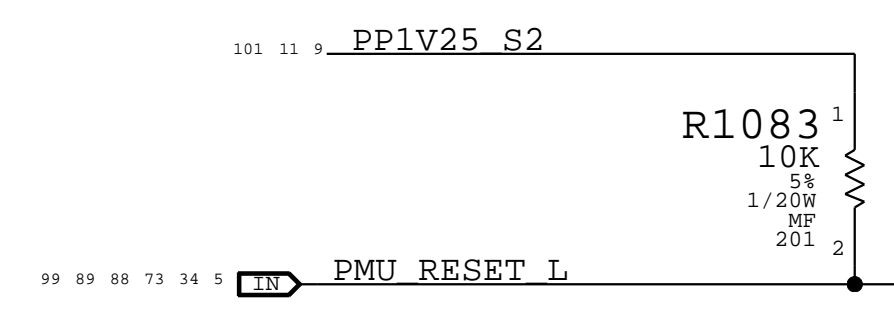
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DOC_ATTENTION should be a TP for non dev programs,

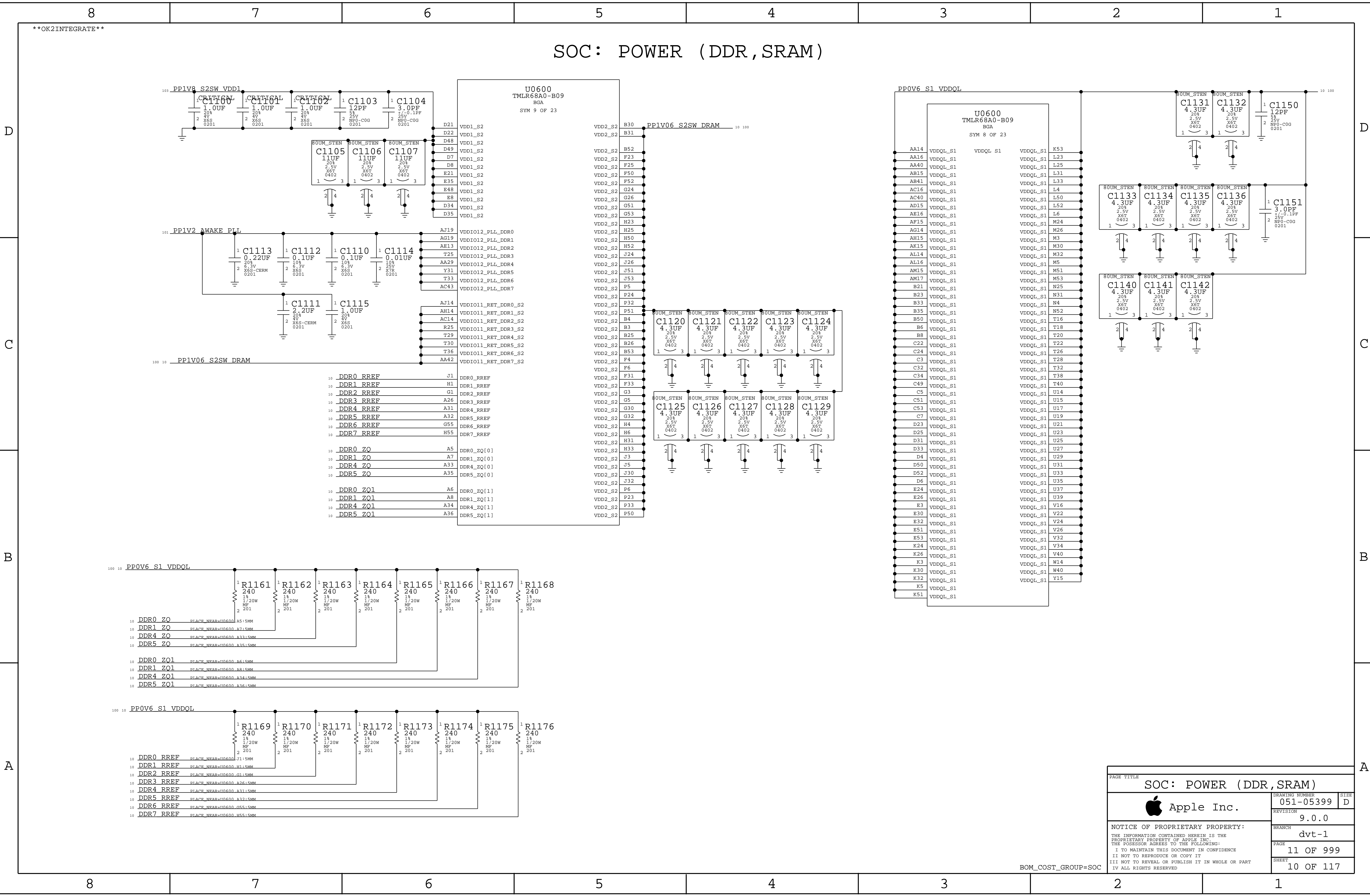
SOC_SW_DBG SHOULD GO TO A LED IF POSSIBLE. NEEDS A TEST POINT AT MINIMUM

FIXTURE_MODE_L should be aliased to a TP for non dev programs, The TP is required



PAGE TITLE		
SOC: AOP		
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SOC: POWER (DDR, SRAM)



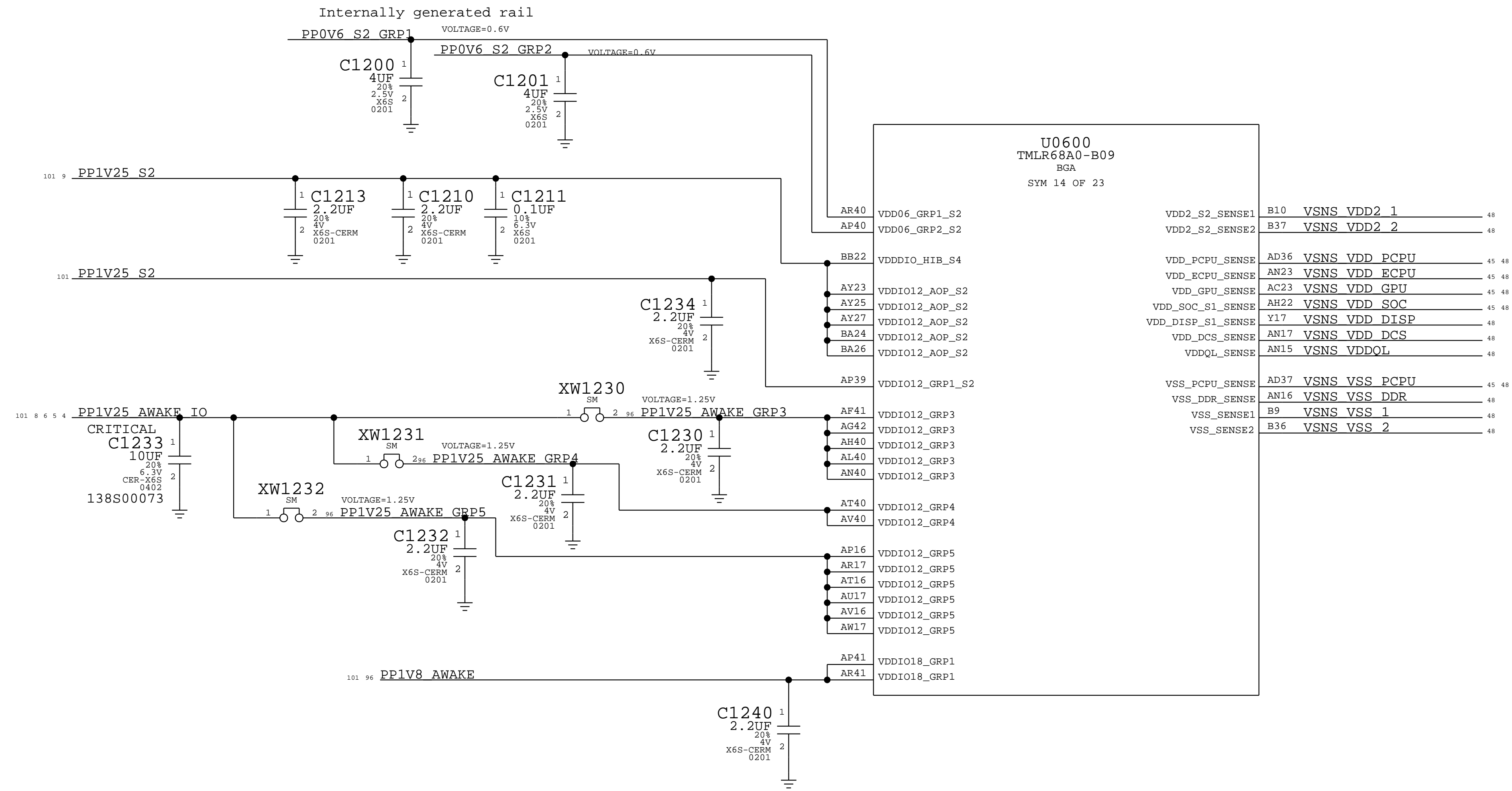
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SOC: POWER (DDR, SRAM)		
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BOM_COST_GROUP=SOC

OK2INTEGRATE

SOC: POWER (IO)

OK2INTEGRATE

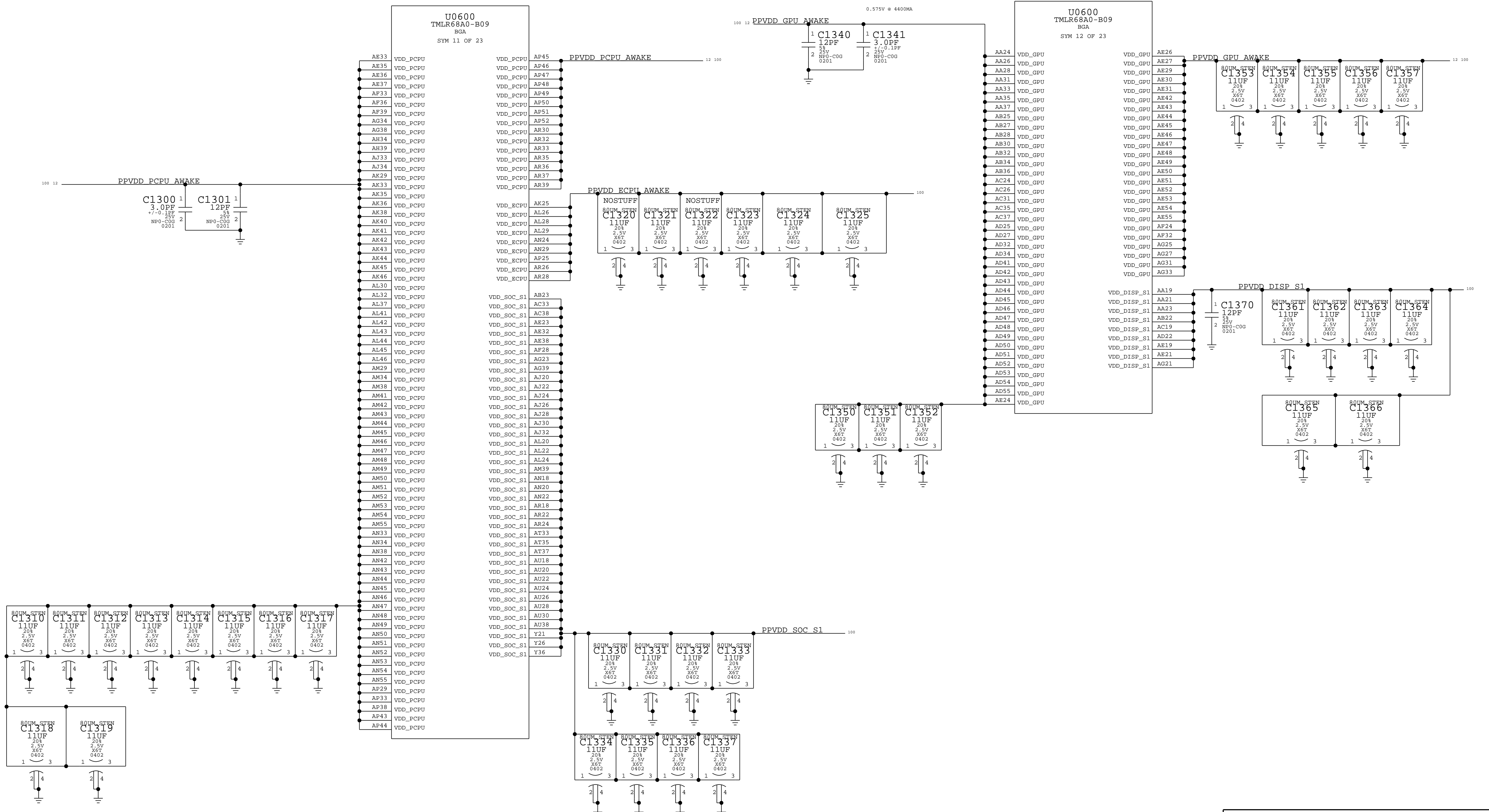


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BOM_COST_GROUP=SOC

SOC: POWER (CPU, GPU)

OK2INTEGRATE

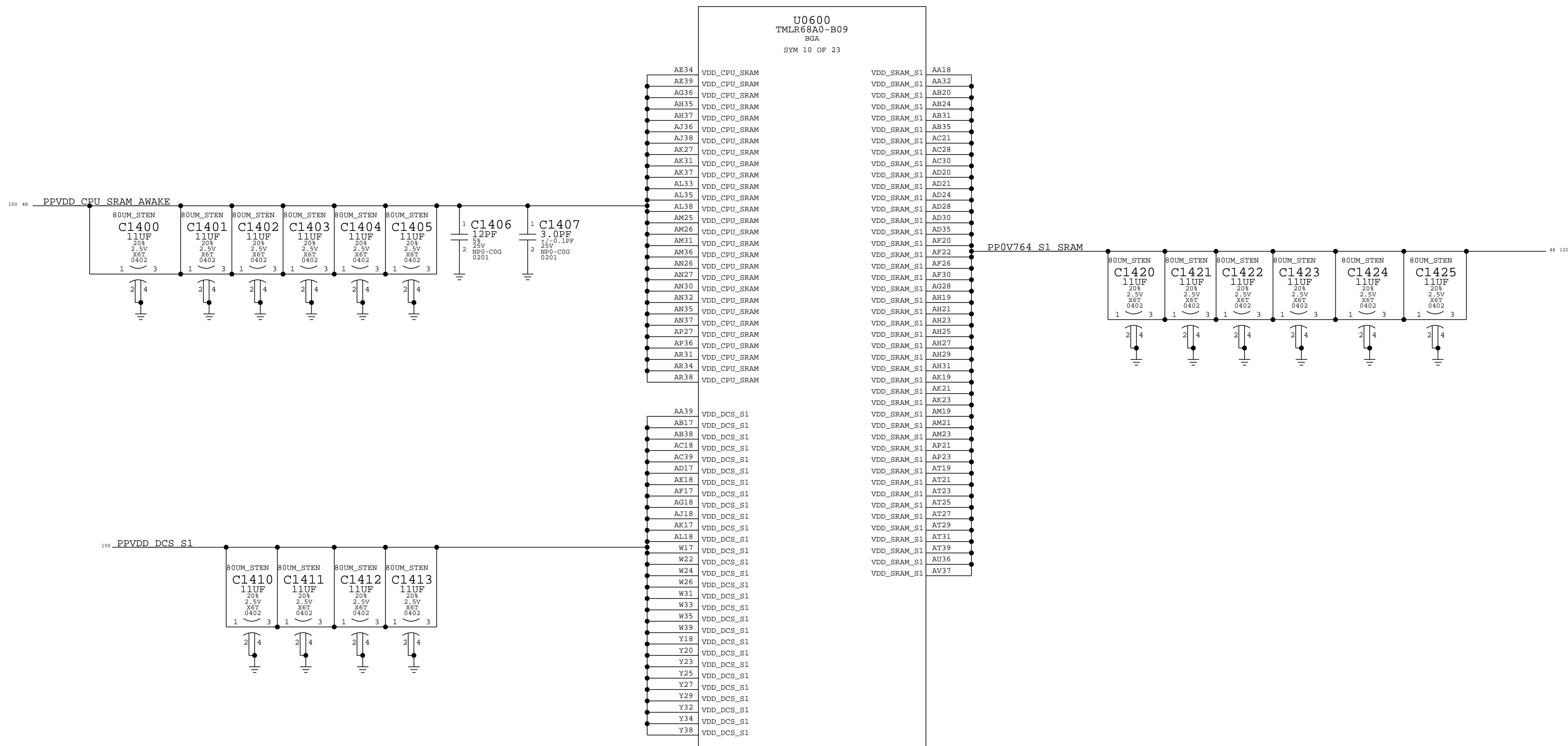


PAGE TITLE		
SOC: POWER (SOC, CPU, GPU)		
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BOM_COST_GROUP=SOC

SOC: POWER (SRAM, SOC)

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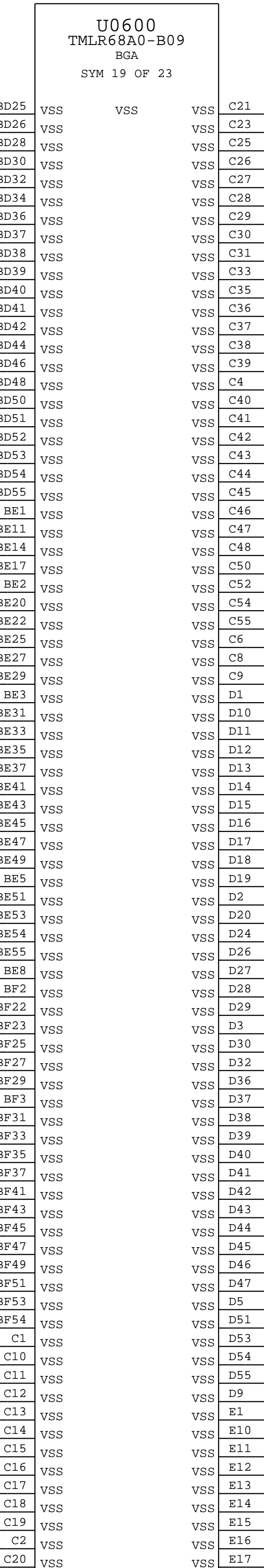
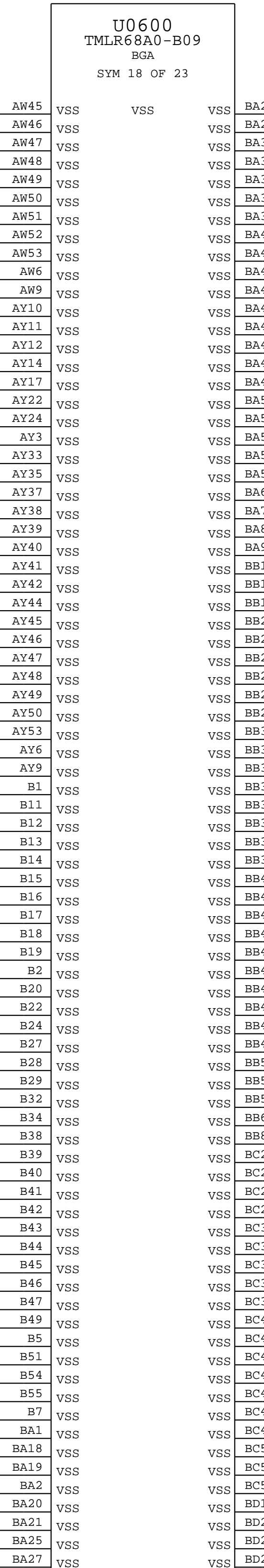
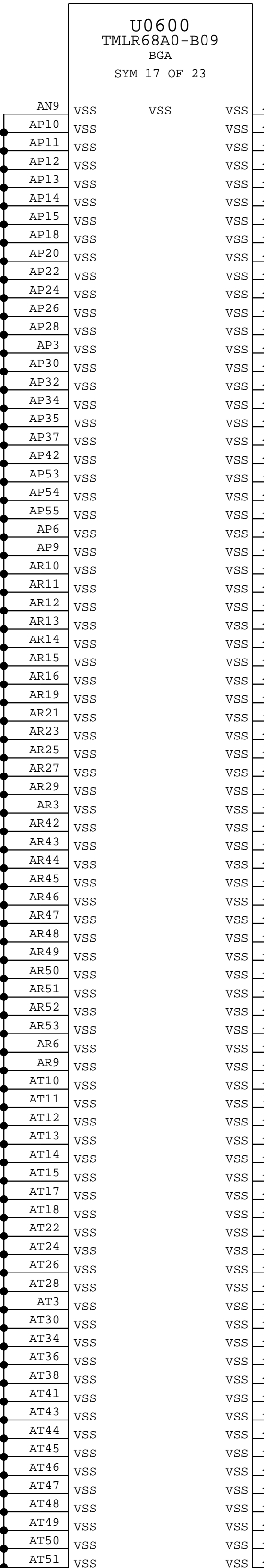
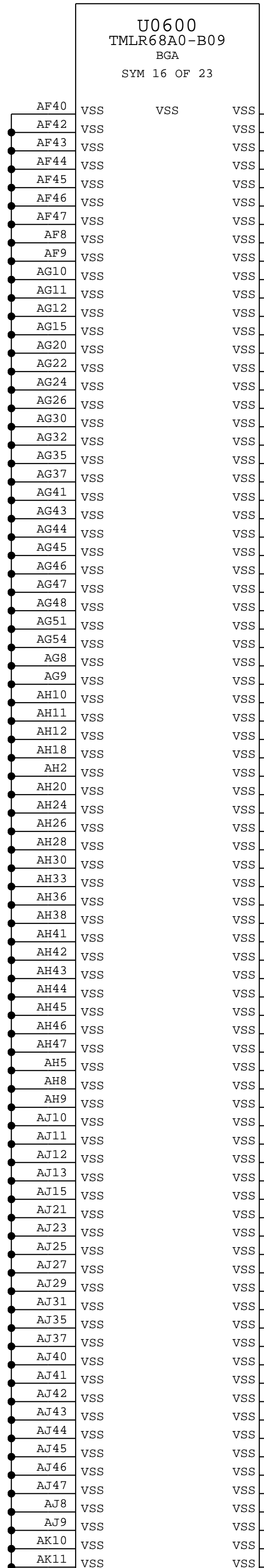
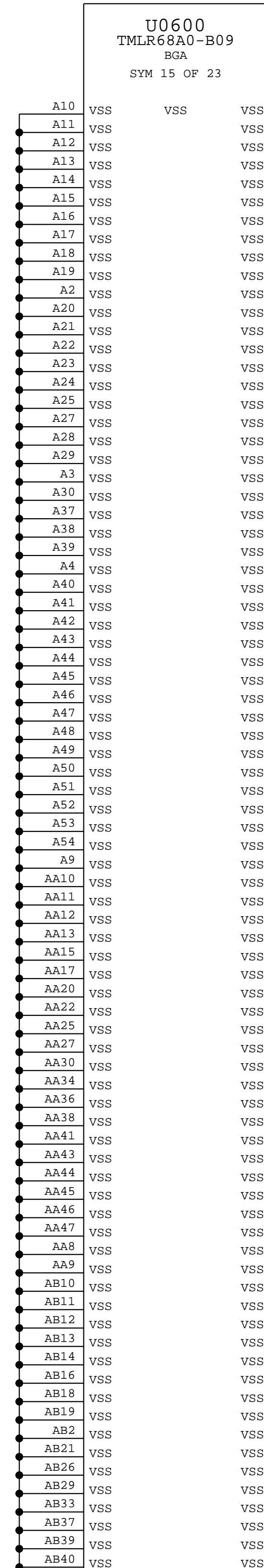


PAGE TITLE		
SOC: POWER (SRAM)		
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SOC: GND (1)



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SOC: GND (2)

OK2INTEGRATE

D

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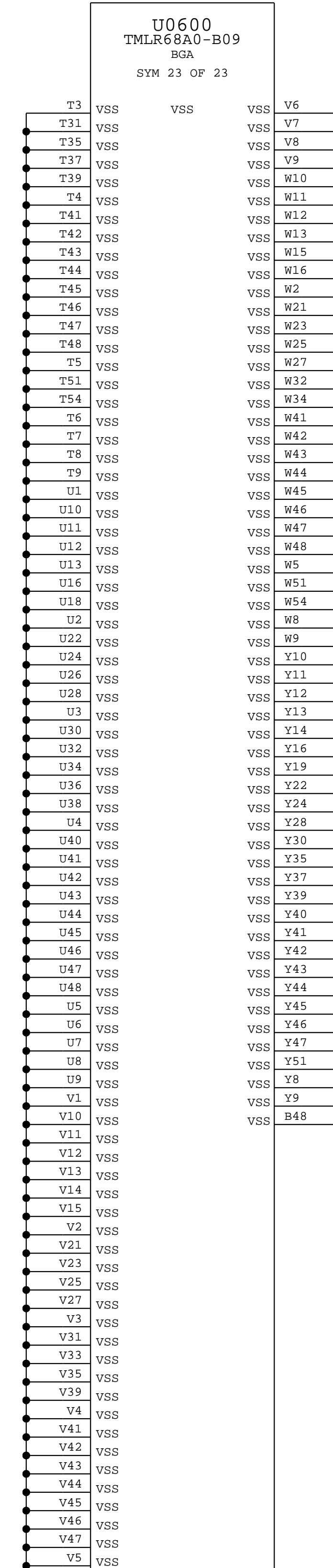
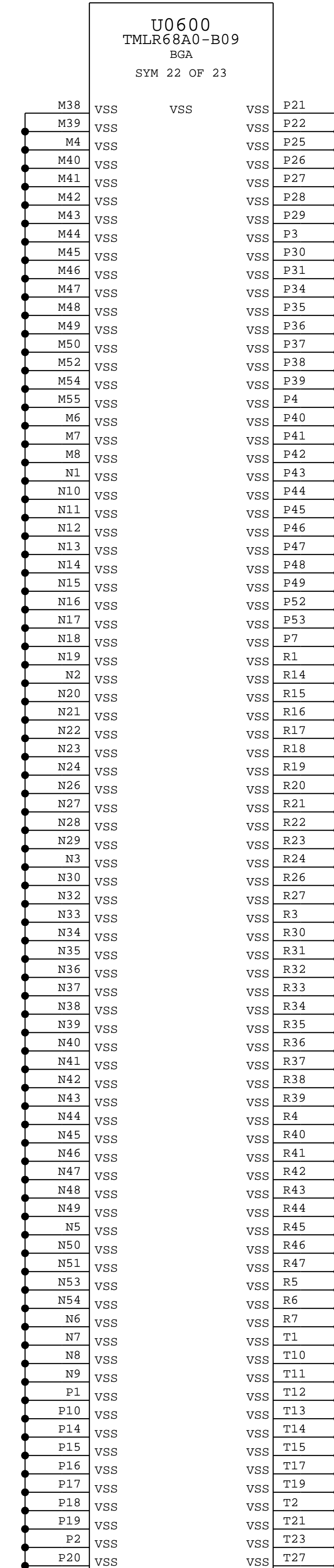
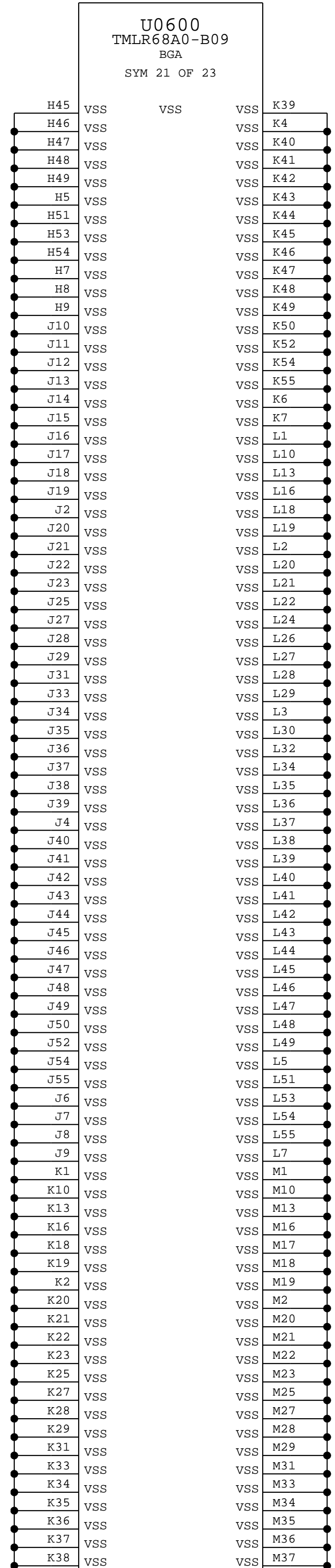
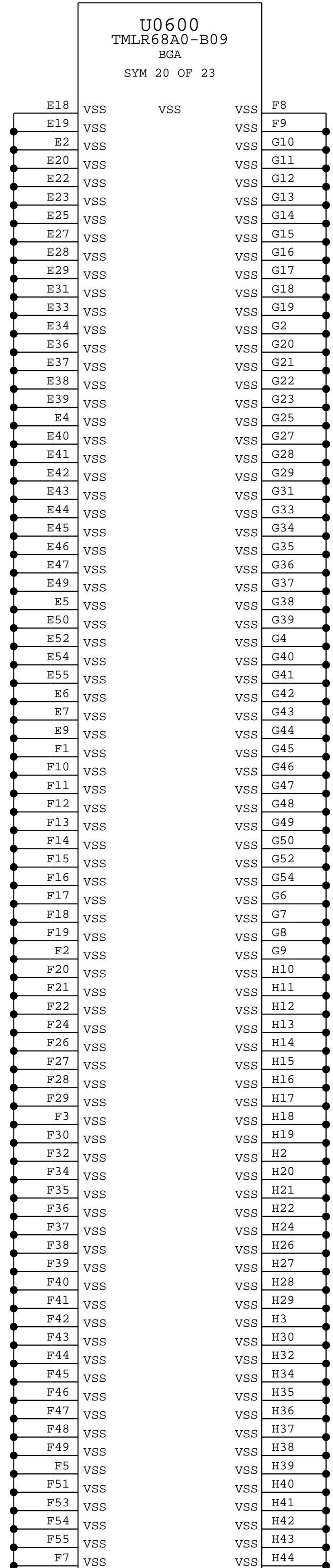
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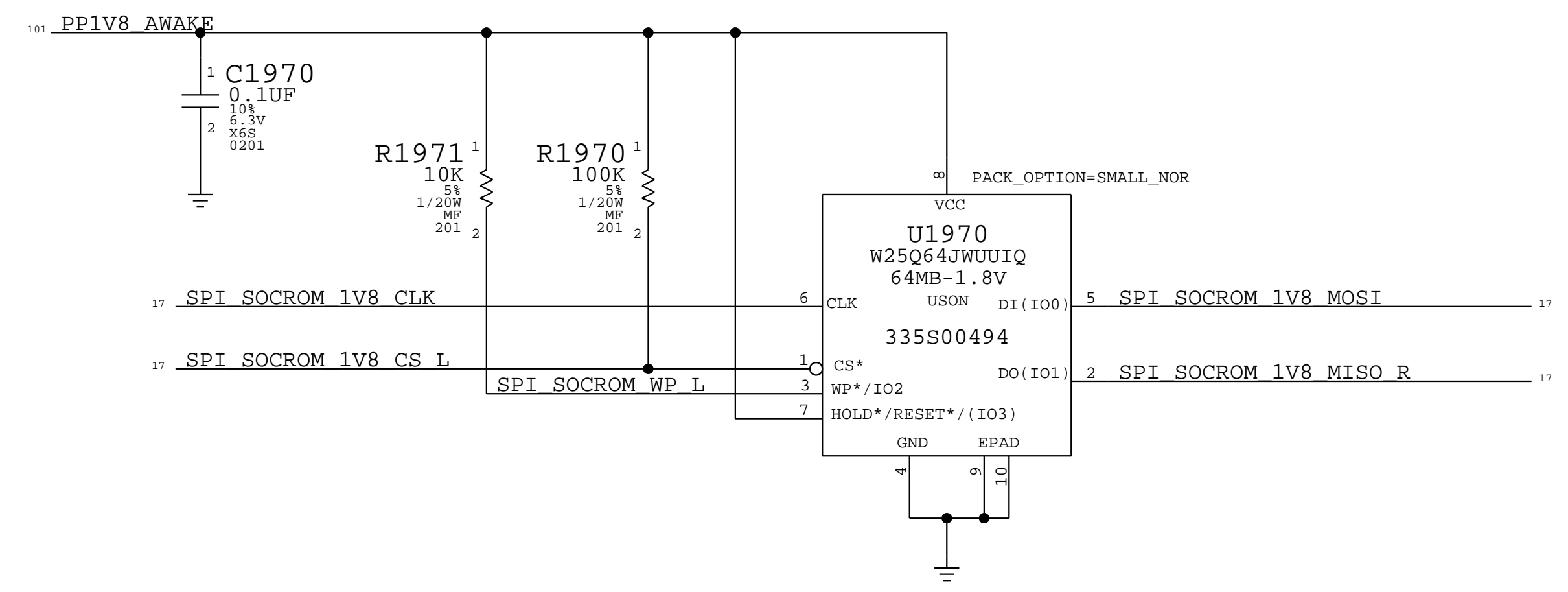
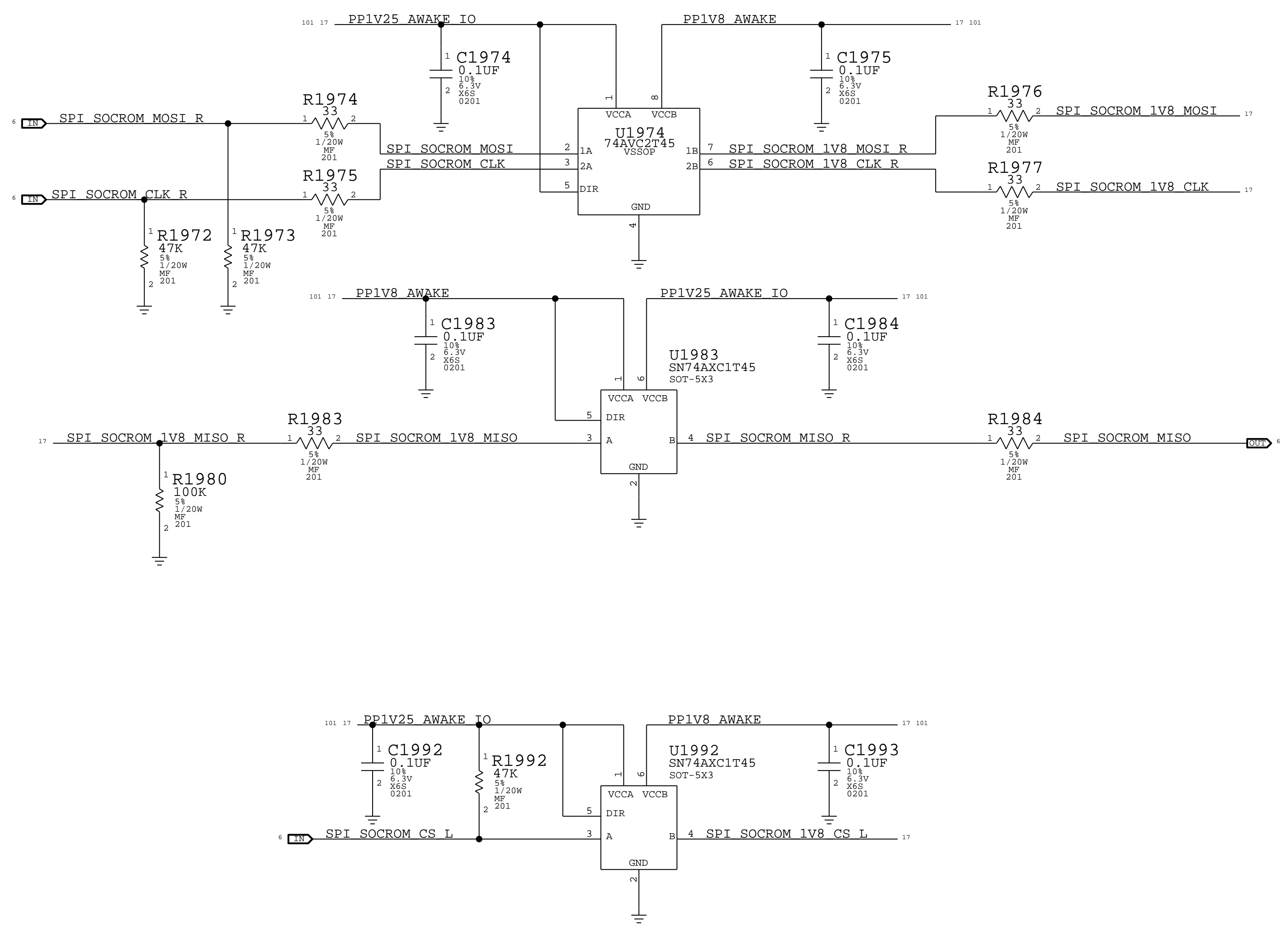
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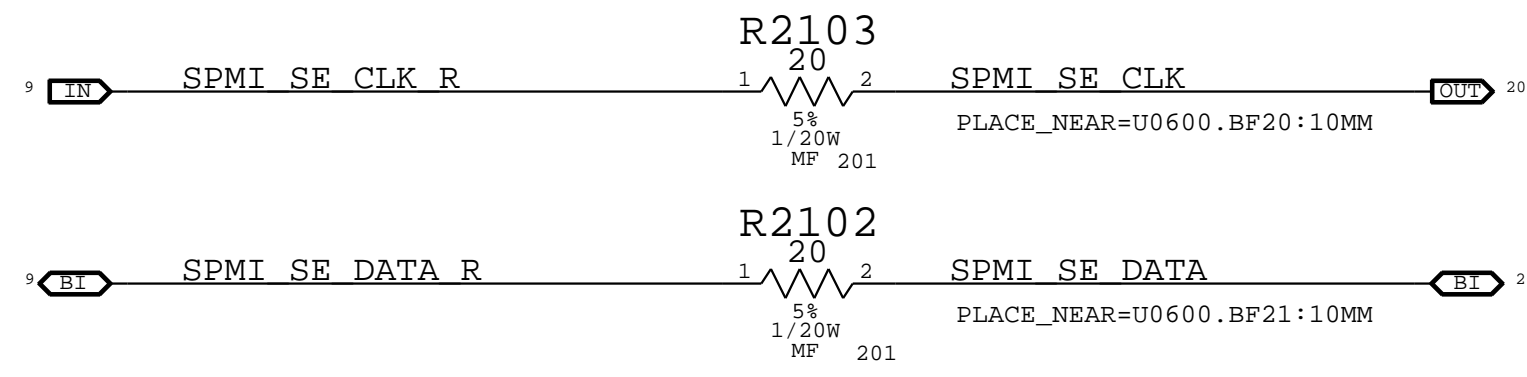
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SPI NOR (1.8V 64 M-BIT)

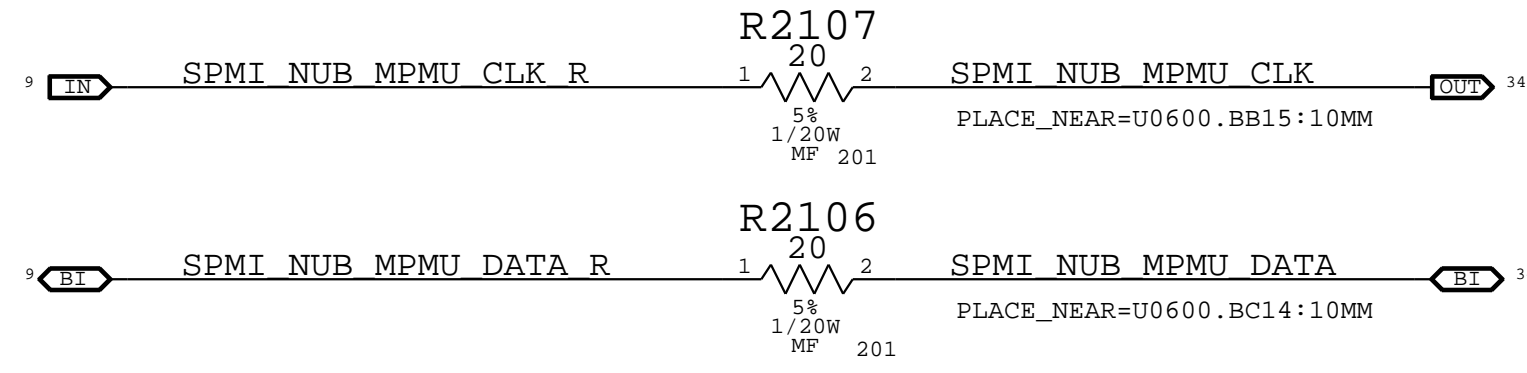


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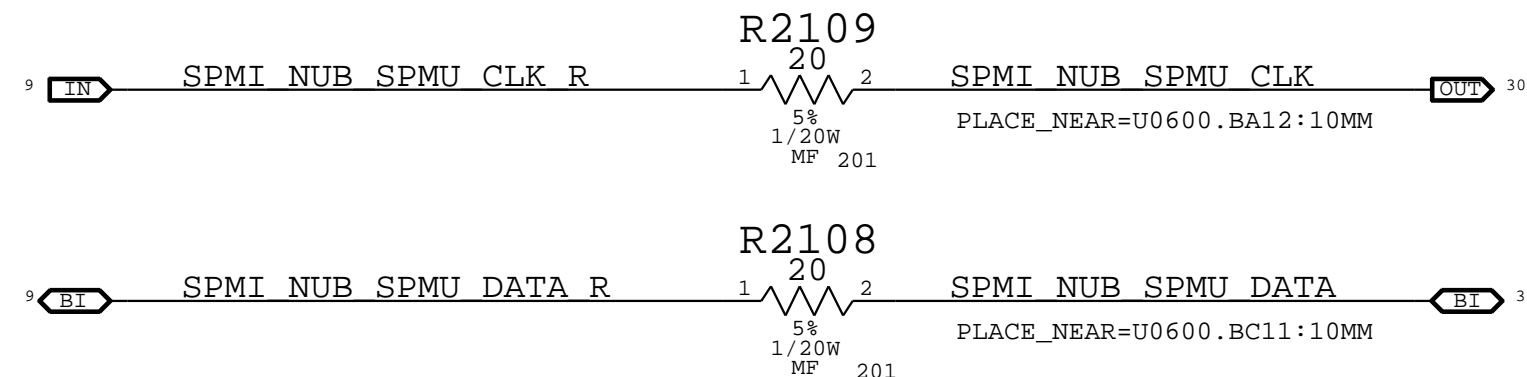
TGA SPMI SE SOURCE TERMINATIONS



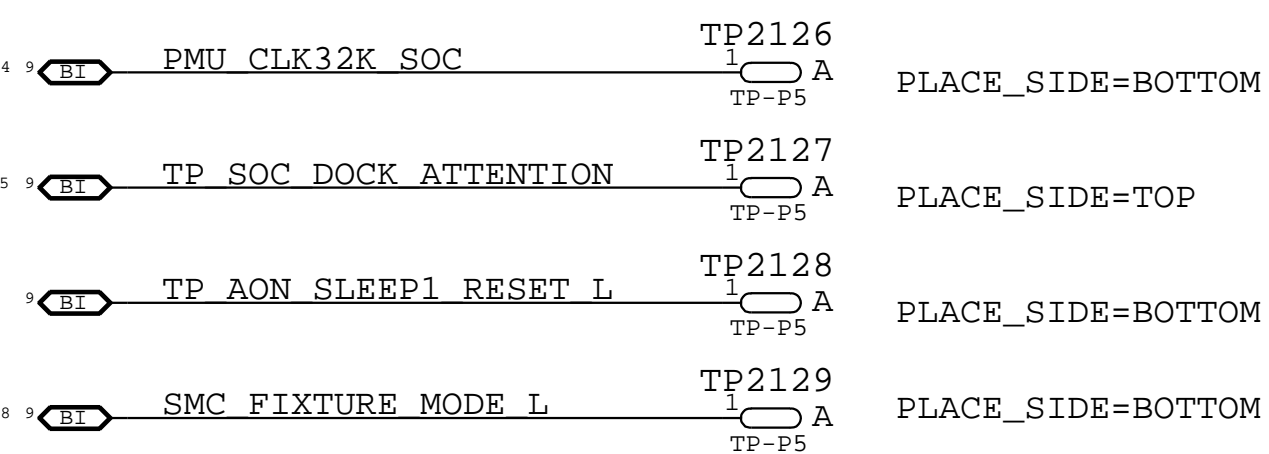
TGA SPMI MPMU SOURCE TERMINATIONS



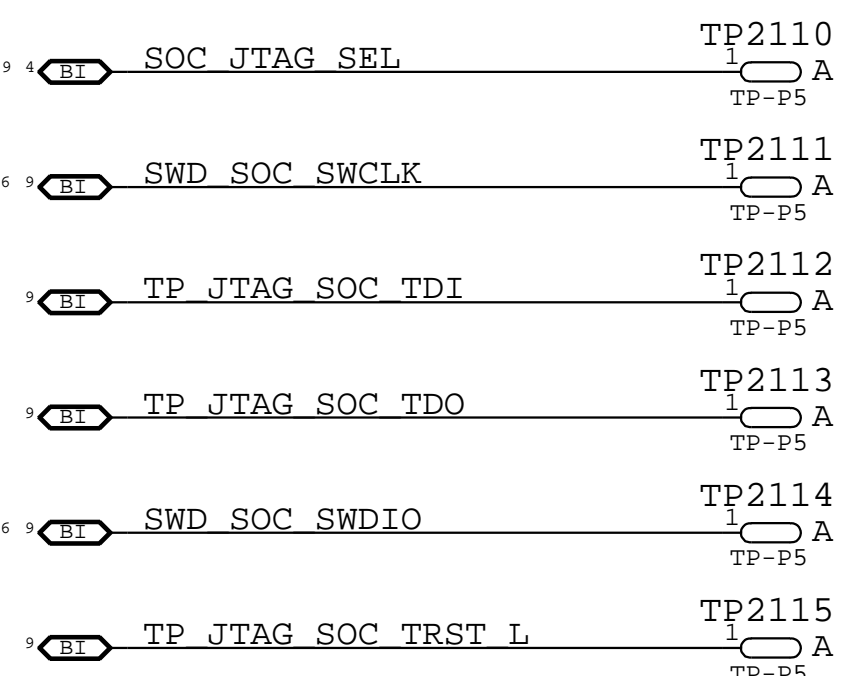
TGA SPMI SPMU SOURCE TERMINATIONS



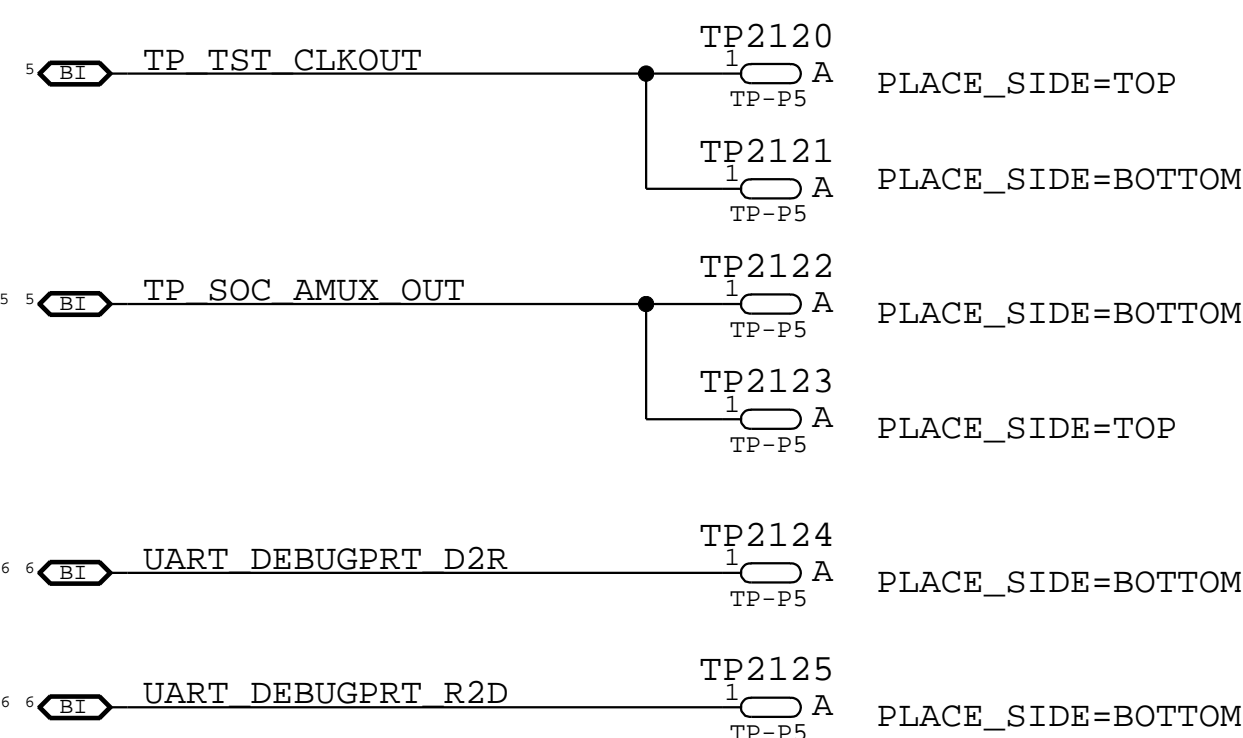
TGA MISC DEBUG TEST-POINTS



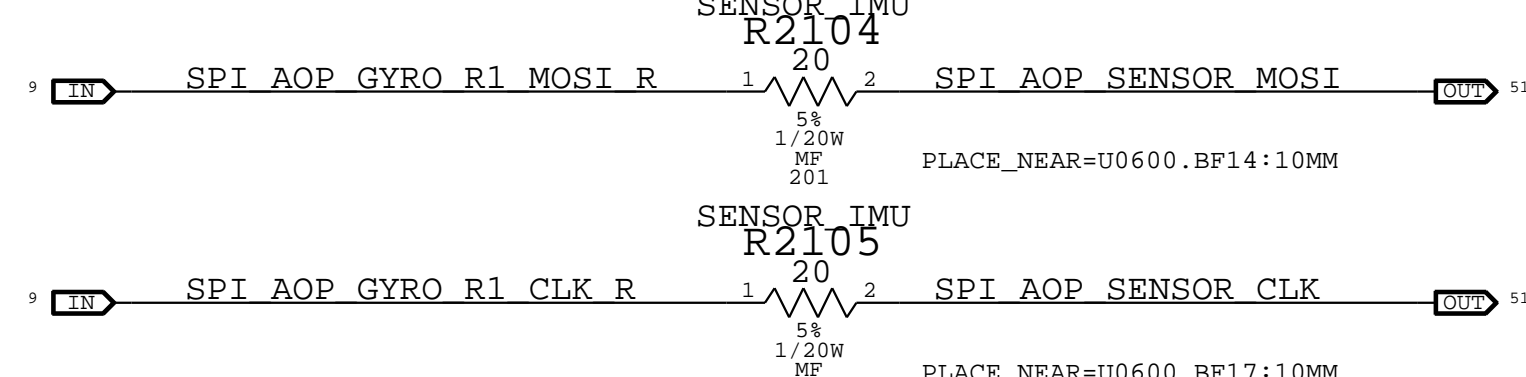
TGA JTAG TEST-POINTS



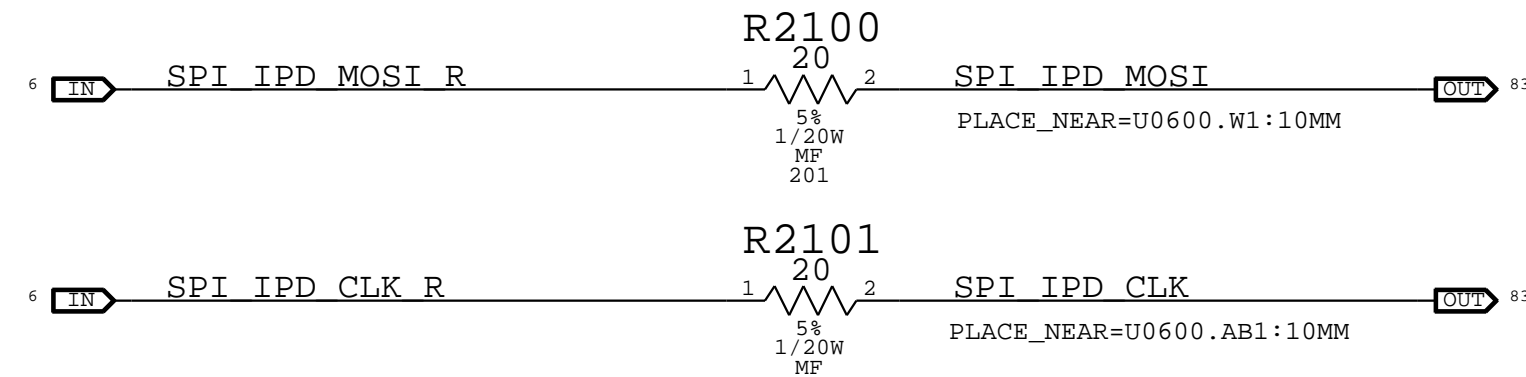
TGA DEBUG TEST-POINTS



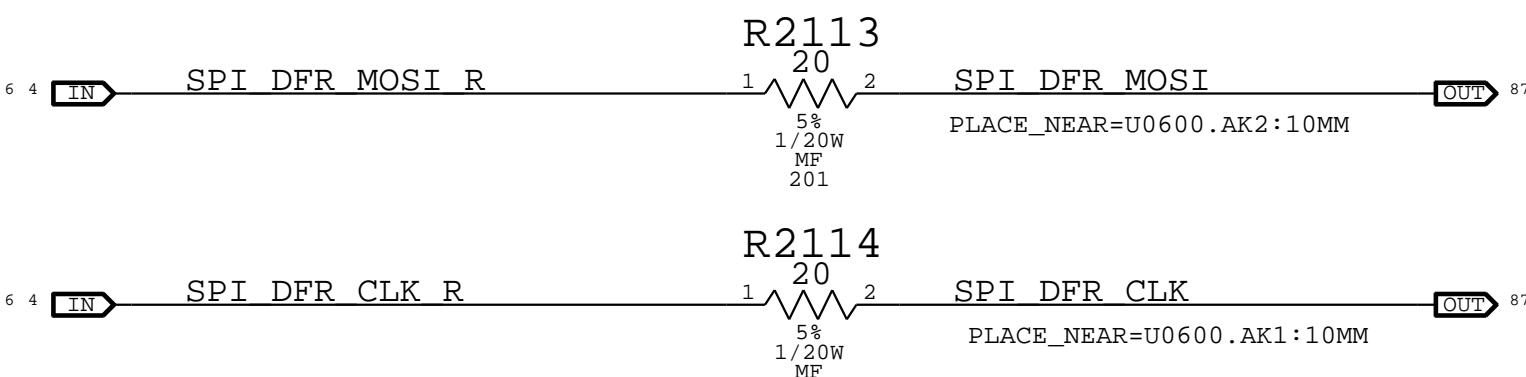
TGA SPI SENSOR SOURCE TERMINATIONS



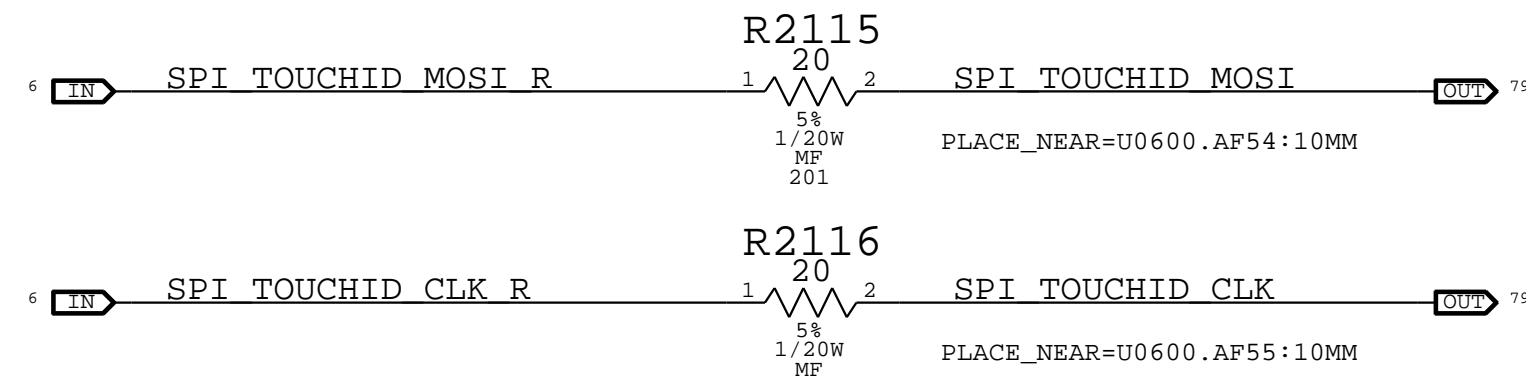
TGA SPI IPD SOURCE TERMINATIONS



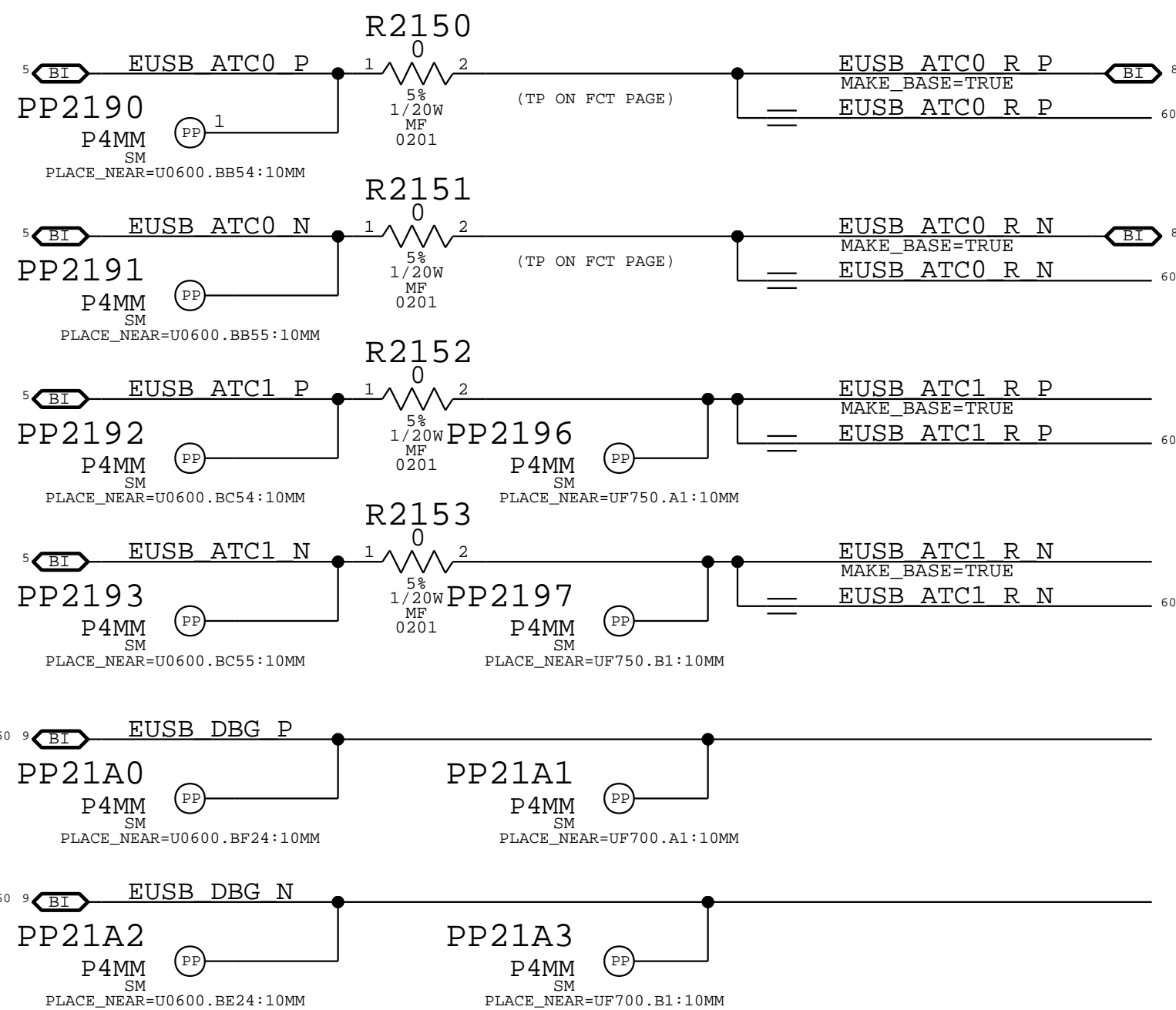
TGA SPI DFR SOURCE TERMINATIONS



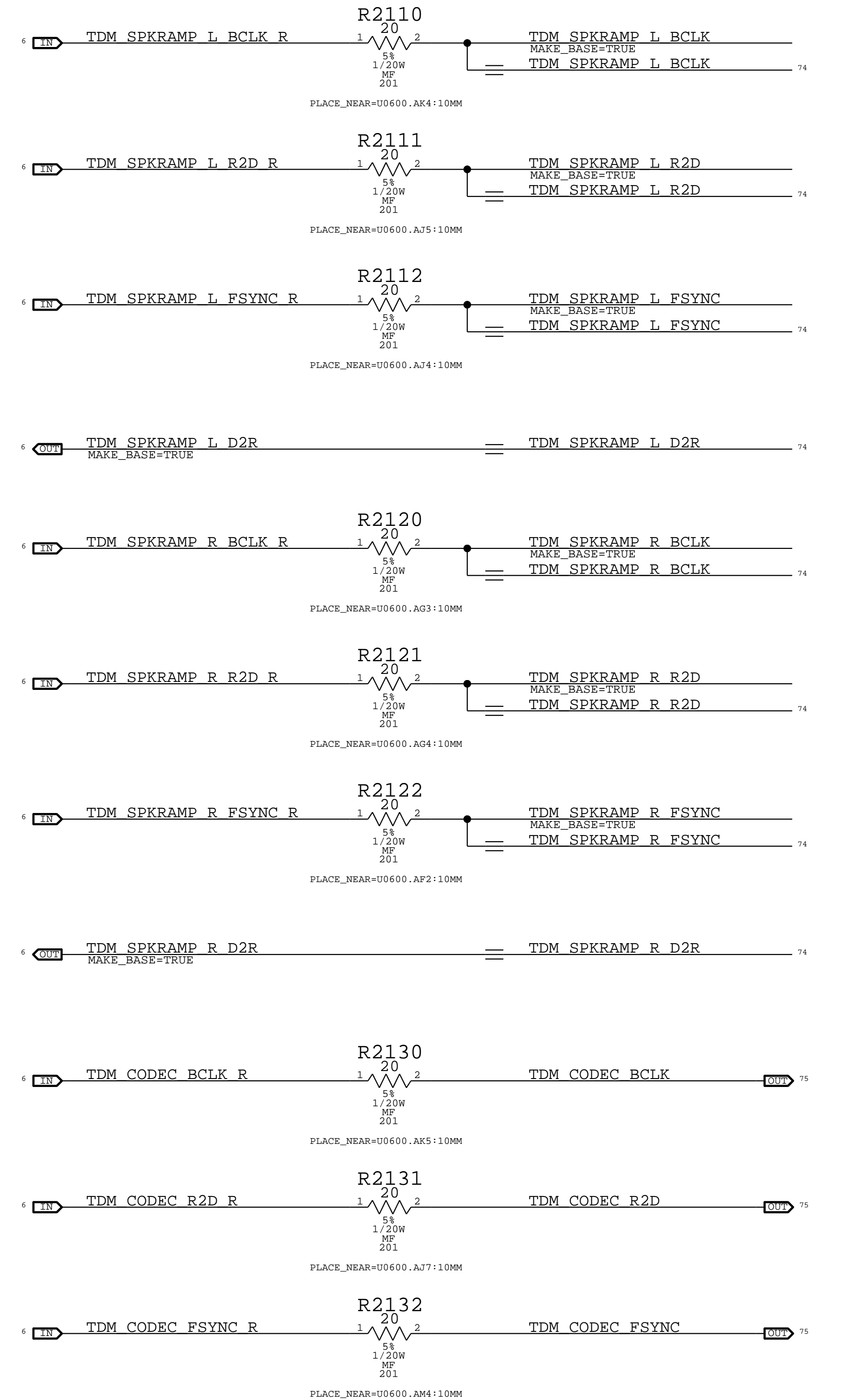
TGA SPI TOUCHID SOURCE TERMINATIONS



EUSB SERIES RESISTORS AND TEST POINTS



TGA 1V2 TDM SOURCE TERMINATIONS



PROJECT SUPPORT (1/2)	
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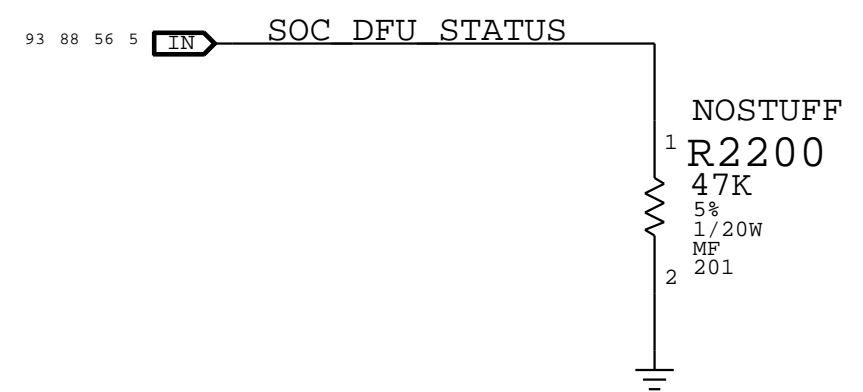
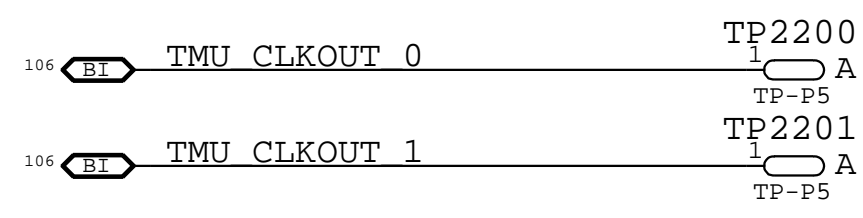
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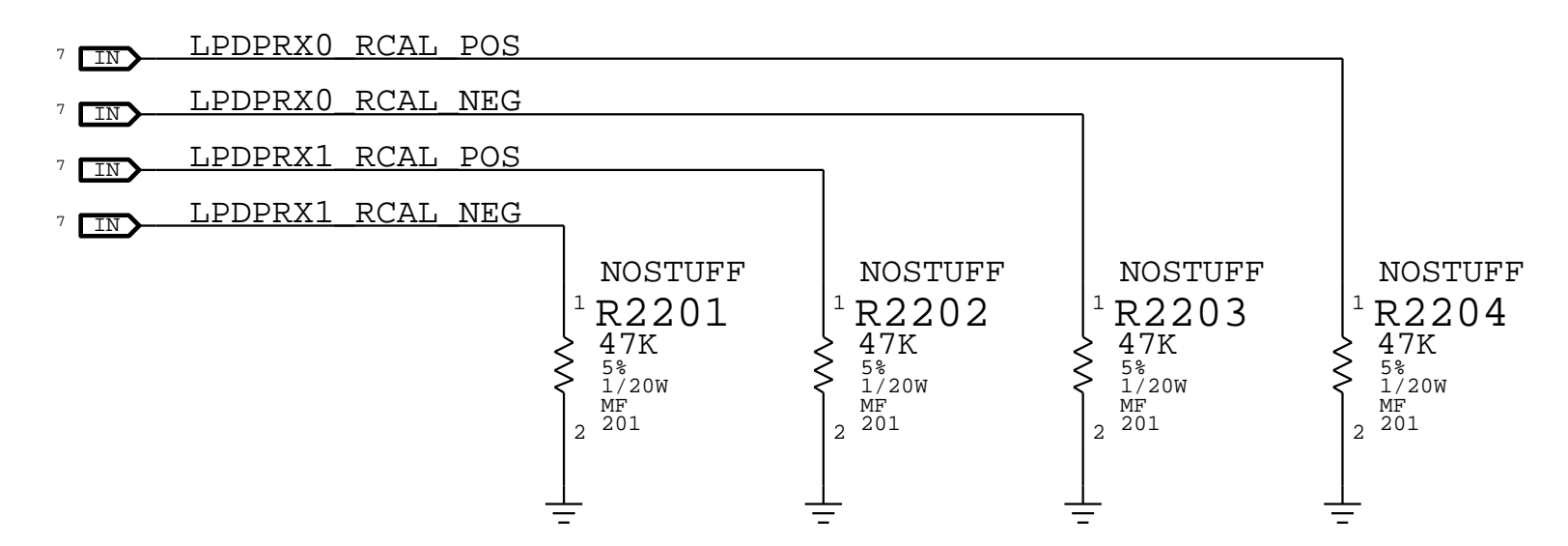
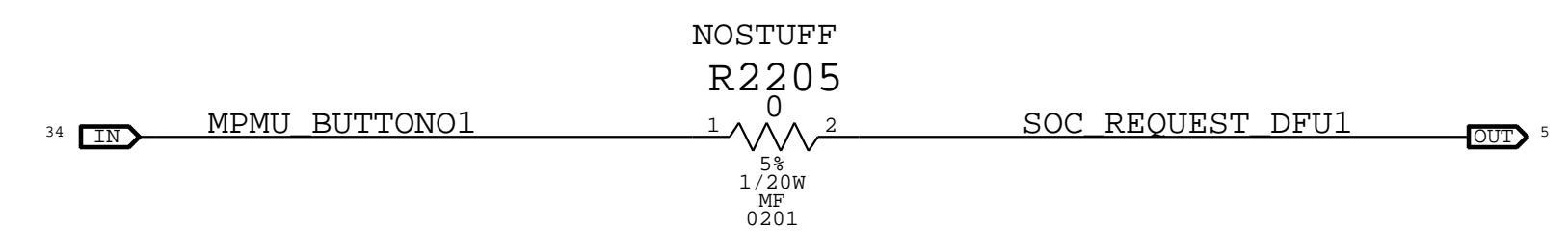
B

A

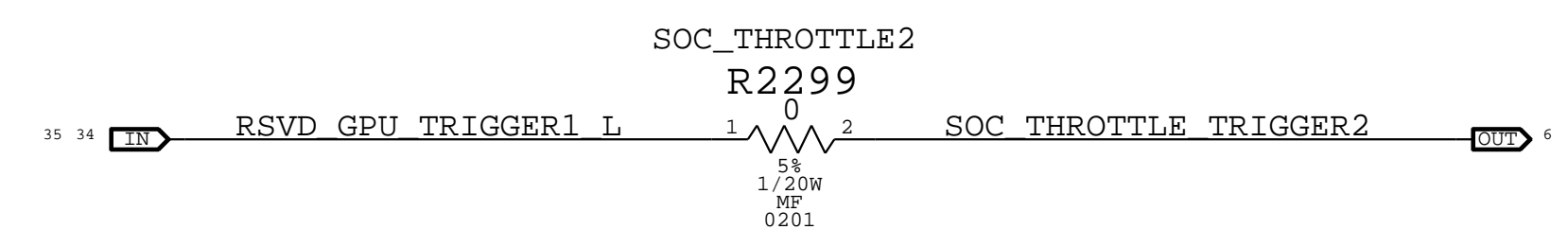
USB4 DEBUG ACCESS <RDAR://62994337>



OPTION FOR SW TO READ POWER BUTTON, NOT USED



<RDAR://59954844>



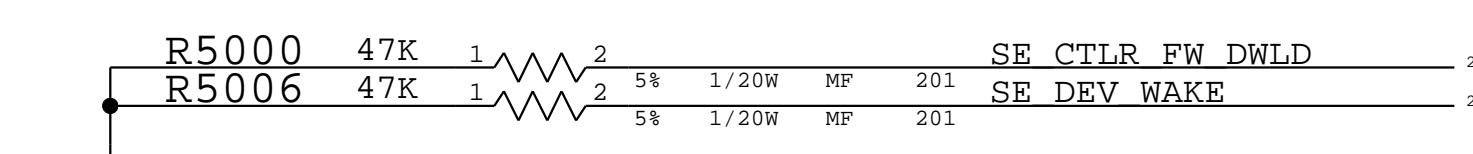
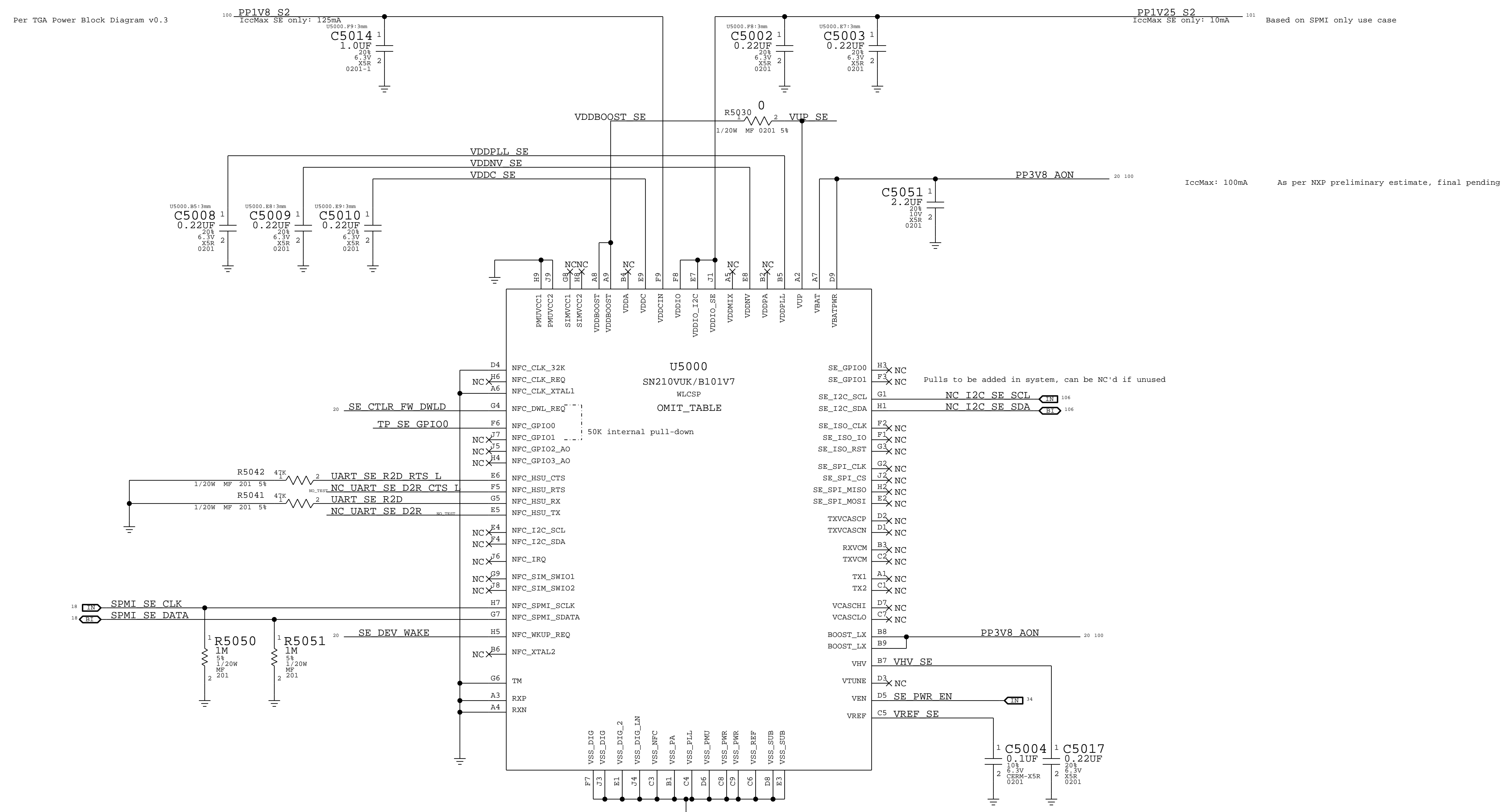
BOM_COST_GROUP=SOC

PAGE TITLE		PROJECT SUPPORT (2/2)	
	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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		PAGE	22 OF 999
		SHEET	19 OF 117

Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***

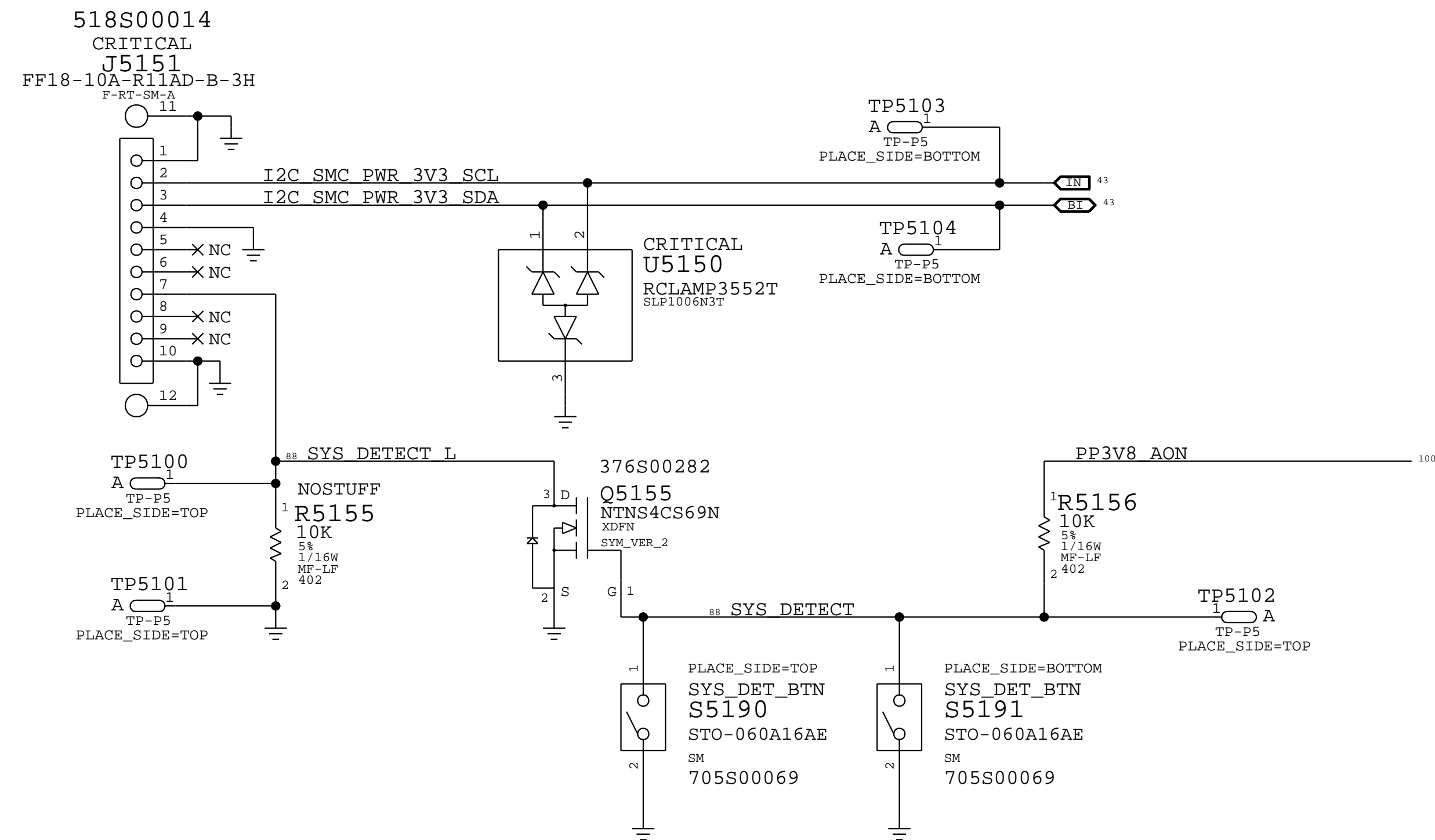


<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
 <rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

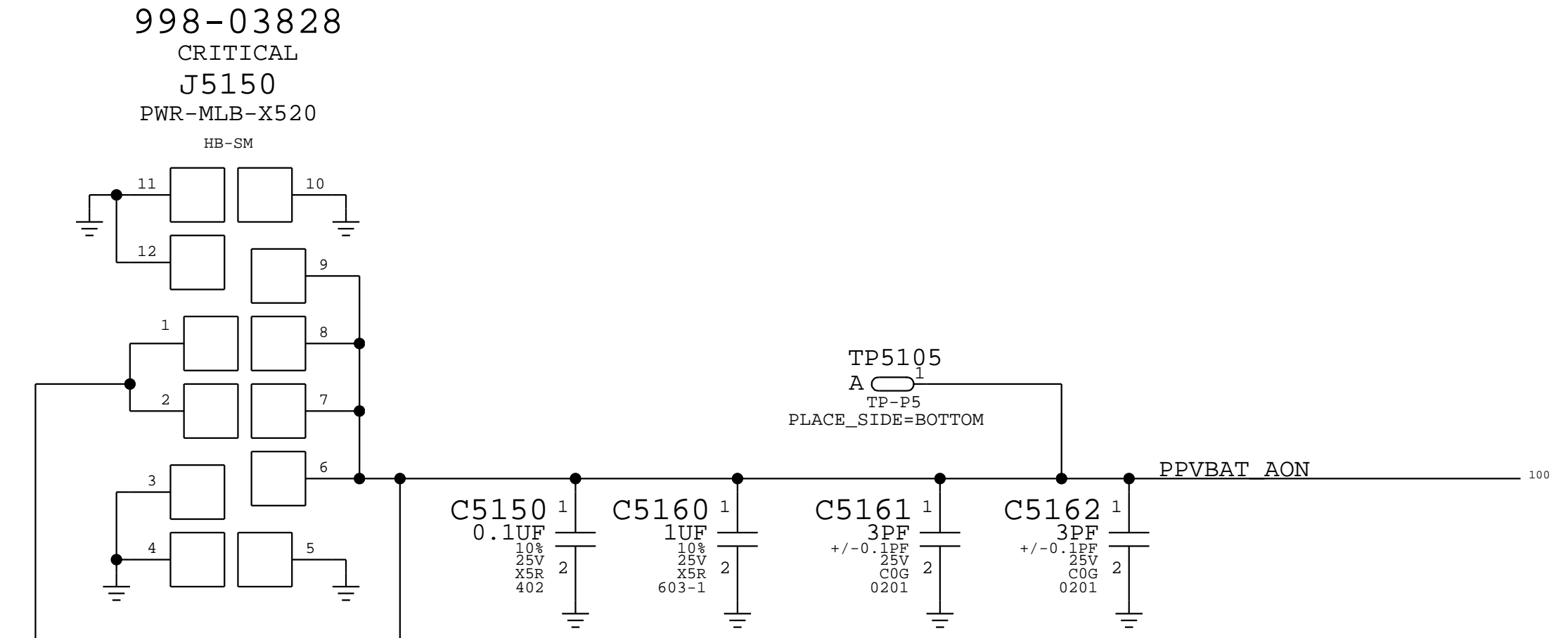
PAGE TITLE		Secure Element	
DRAWING NUMBER	051-05399	SIZE	D
	REVISION		9.0.0
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BATTERY (BMU) LOGIC CONNECTOR



BATTERY (BMU) FLEX SOLDER PADS

BMU POWER FLEX IS SOLDERED TO MLB.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA, FLEX, BMU PWR, X502	J5150	CRITICAL	

SYNC_MASTER=AITKEN_T668_MLB

PAGE TITLE

BATTERY CONNECTORS

	DRAWING NUMBER	051-05399	SIZE	D
	REVISION	9.0.0		
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		SHEET	21 OF 117	

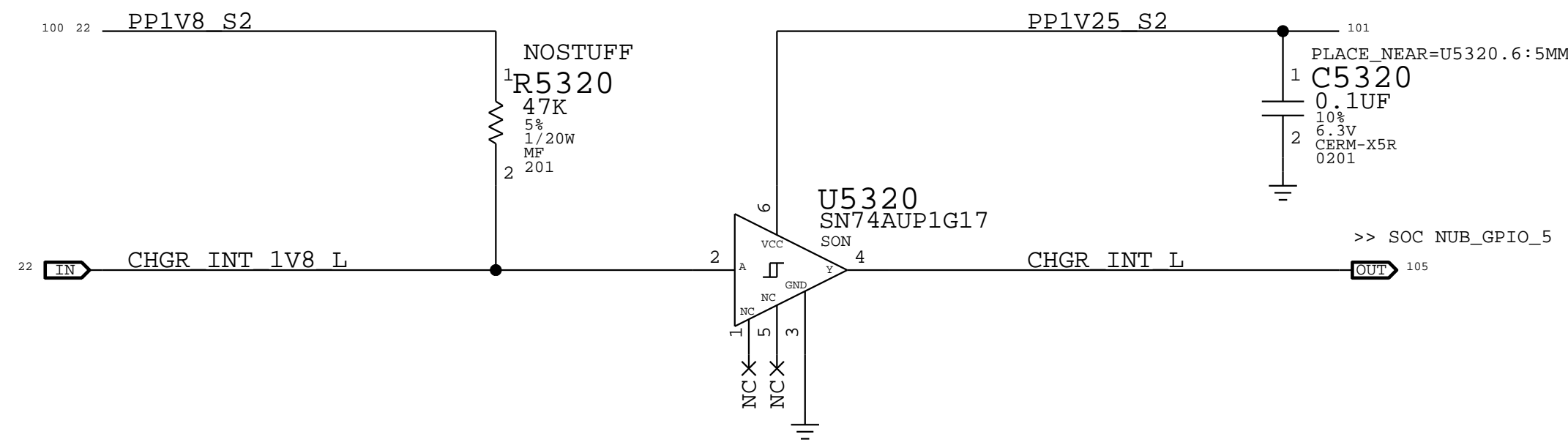
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_IV8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

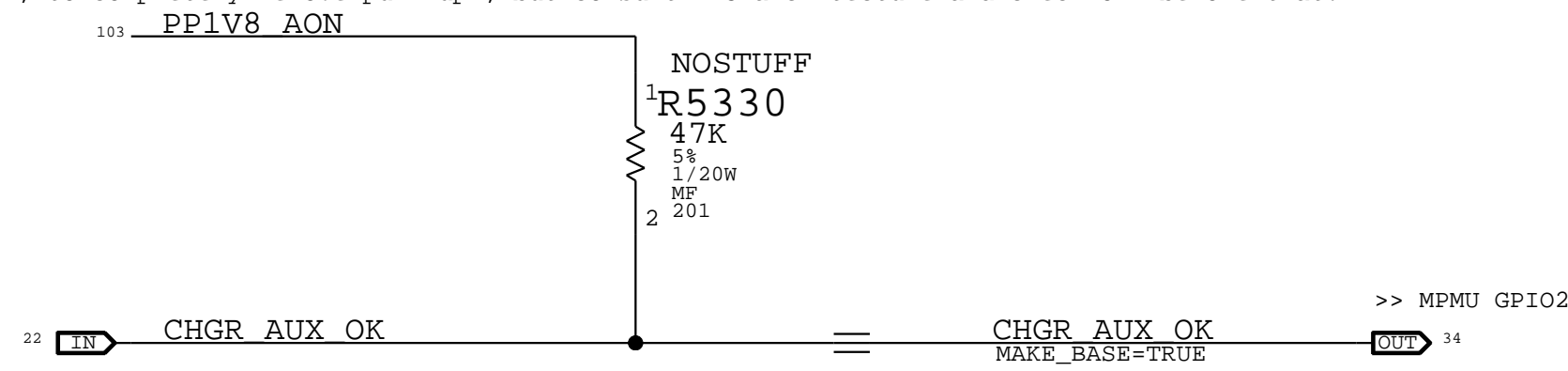
CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.



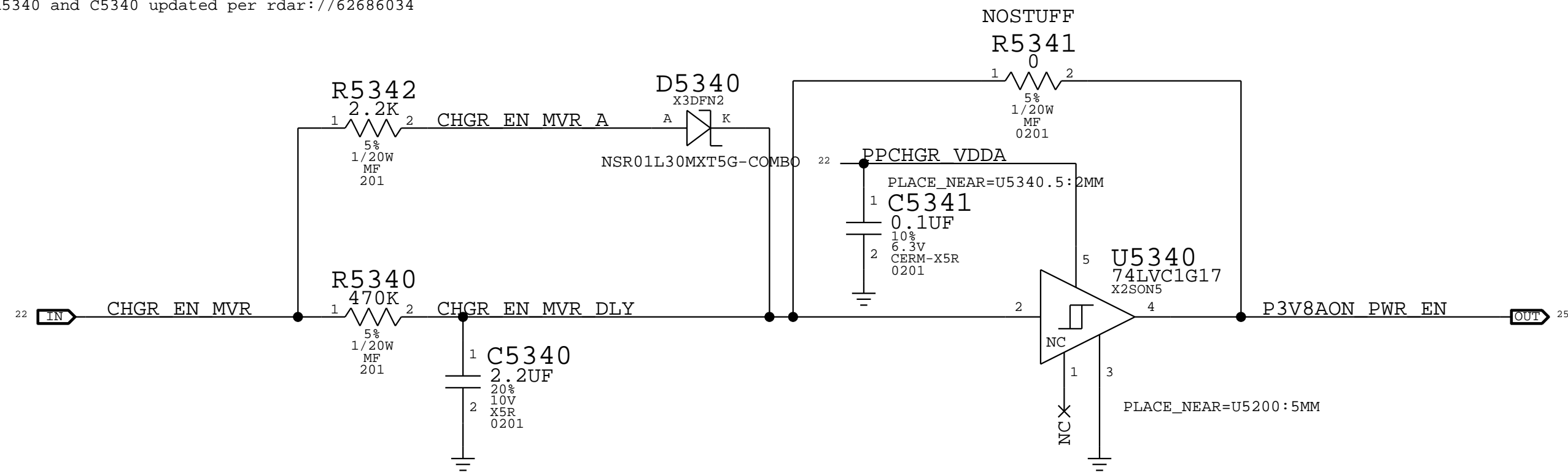
CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.
OK, to completely remove pull up, but consult PMU architecture and check OTP before that.



Delay for 3.8V VR Enable

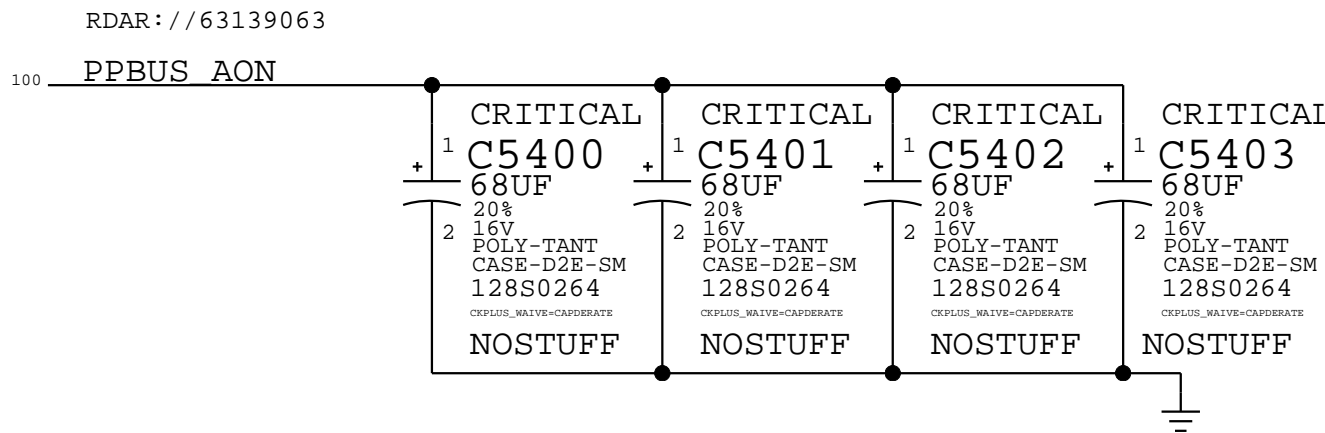
R5340 and C5340 updated per rdar://62686034



PAGE TITLE		BATTERY CHARGER SUPPORT	
Apple Inc.	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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	PAGE	53 OF 999	
	SHEET	23 OF 117	

BOM_COST_GROUP=BATTERY

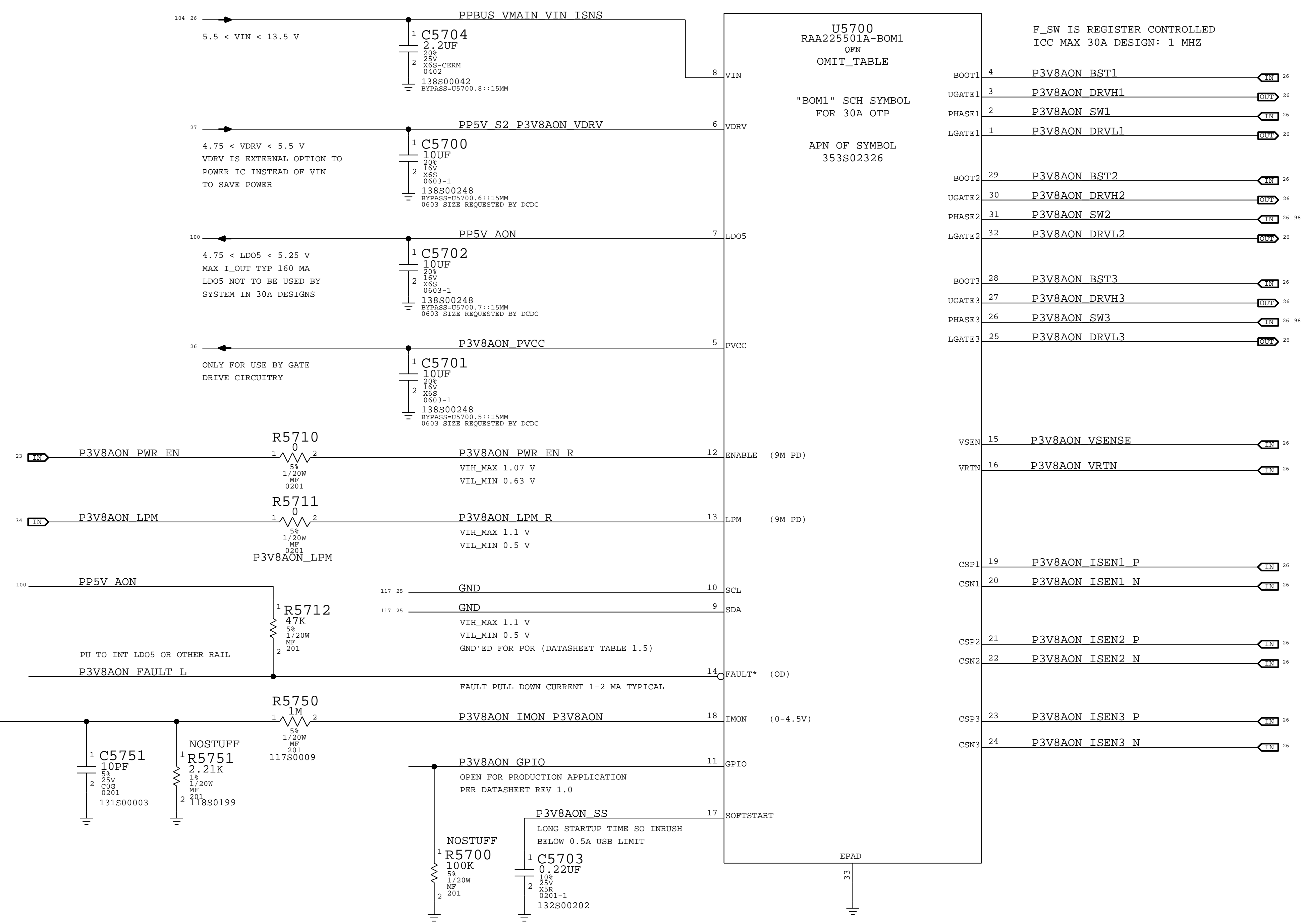
PBUS SUPPORT FOR SPF COMPLIANCE



PAGE TITLE		DRAWING NUMBER		SIZE
PBUS SUPPORT		051-05399		D
Apple Inc.		REVISION		9.0.0
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BOM_COST_GROUP=PLATFORM POWER

3V8 AON CONTROLLER 30A ICC MAX



F_SW IS REGISTER CONTROLLED
ICC MAX 30A DESIGN: 1 MHZ

U5700
RAA225501A-BOM1
QFN
OMIT_TABLE

"BOM1" SCH SYMBOL
FOR 30A OTP

APN OF SYMBOL
353S02326

P3V8AON IMON
IMON NOT TO BE USED SYSTEM SIDE
<RDAR://58648650>
IMON IS 2.52 V @ 30 A
VENDOR REQUIRES R > 1M, C < 50 PF

30A OTP CHANGES DOCUMENTED IN <RDAR://61519509>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02326	1	IC,RAA225501.3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R080,QFN32	U5700	CRITICAL	P3V8AON_IC:A1 ROB0
353S02544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R081,QFN32	U5700	CRITICAL	P3V8AON_IC:A1 ROB1
353S02560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R082,QFN32	U5700	CRITICAL	P3V8AON_IC:A1 ROB2

SYNC_MASTER=REF_VR_ICEMAN SYNC_DATE=06/15/2020

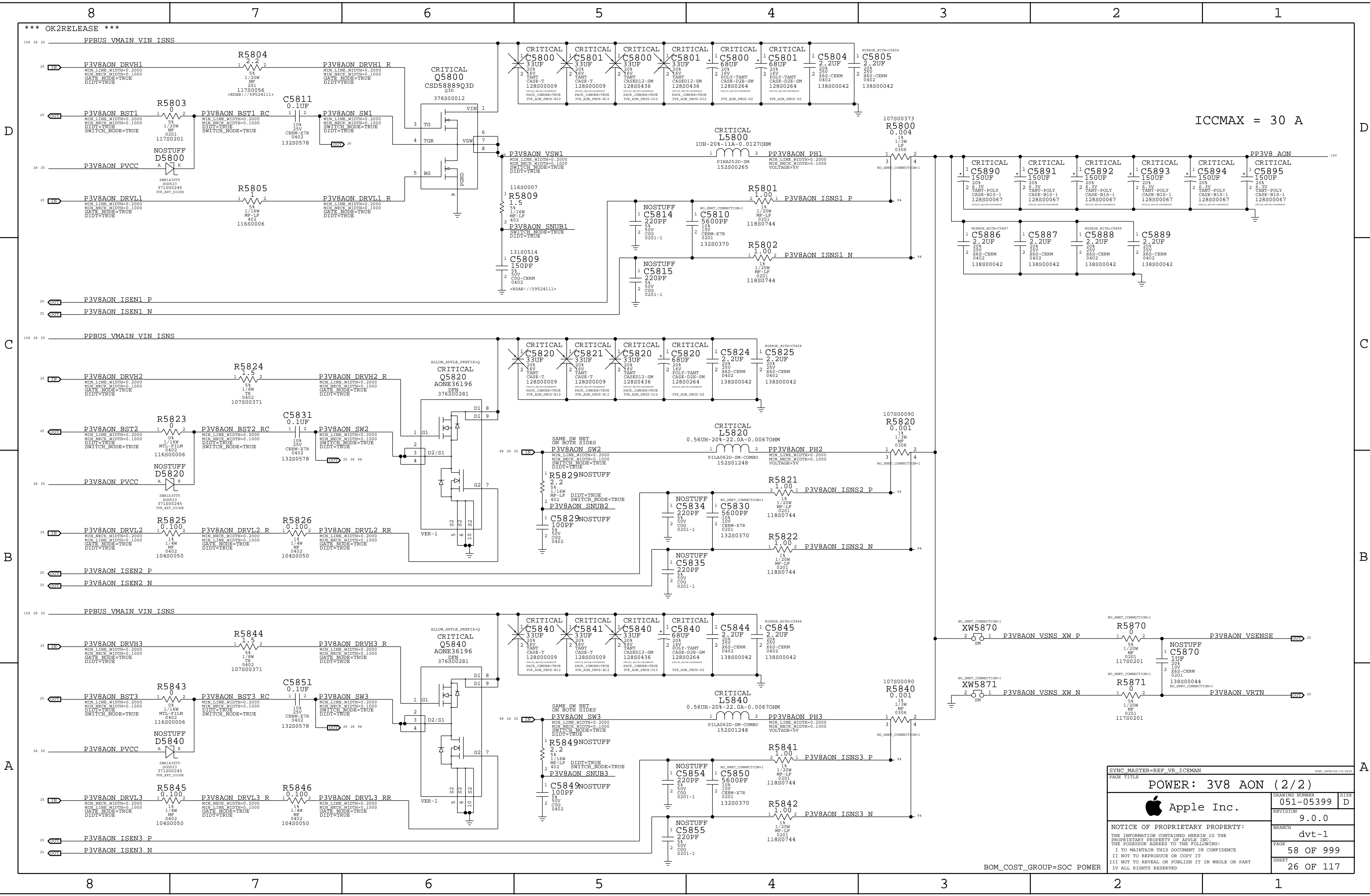
POWER: 3V8 AON (1/2)

Apple Inc.

DRAWING NUMBER	051-05399	SIZE	D
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BOM_COST_GROUP=SOC POWER



ICCMAX = 30 A

SYNC_MASTER=REF_VR_ICEMAN		PAGE TITLE	
POWER: 3V8 AON (2/2)			
Apple Inc.		DRAWING NUMBER	051-05399
		REVISION	9.0.0
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		PAGE	58 OF 999
		SHEET	26 OF 117

BOM_COST_GROUP=SOC POWER

8

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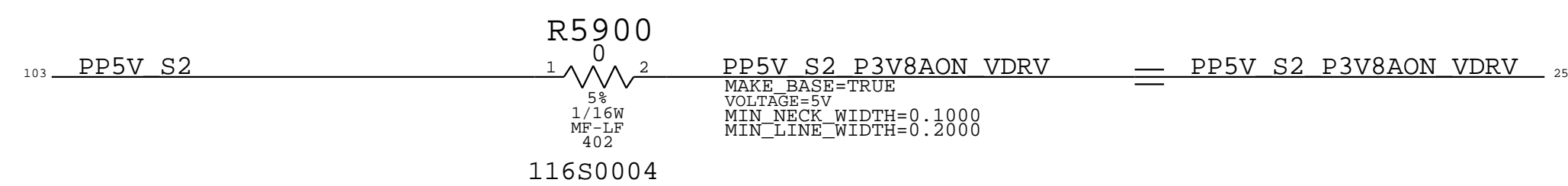
B

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ZERO OHM RESISTOR TO ALLOW ACCESS TO VDRV



PAGE TITLE POWER: 3V8 AON SUPPORT		
	DRAWING NUMBER 051-05399	SIZE D
	REVISION 9.0.0	BRANCH dvt-1
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BOM_COST_GROUP=SOC POWER

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1

SLAVE PMU LDO, SWITCHES & BOOST

LDO/SW INPUTS

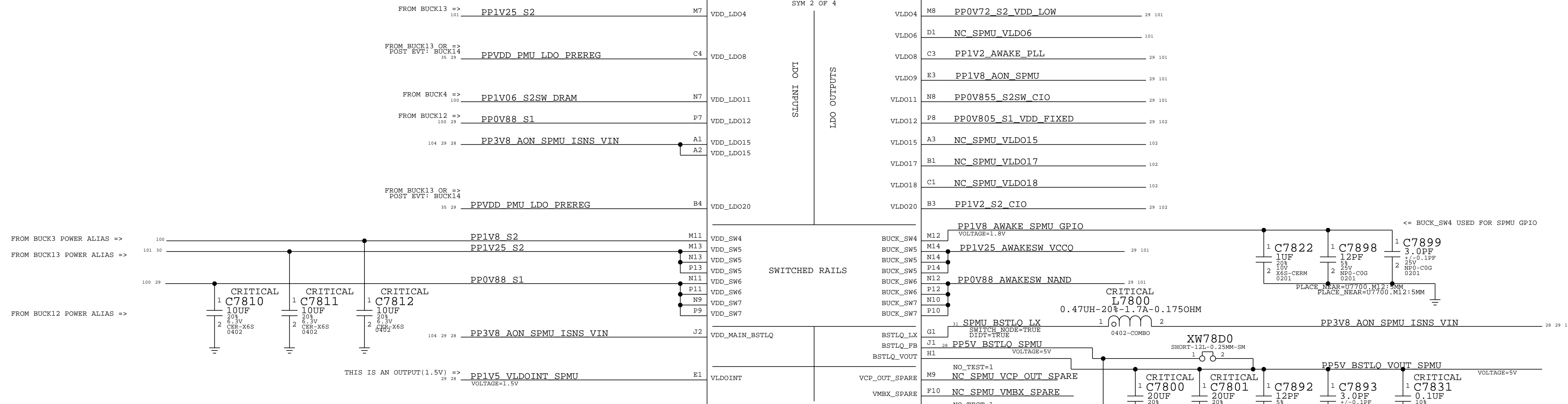
LDO/SW OUTPUTS

998-22526
OMIT_TABLE

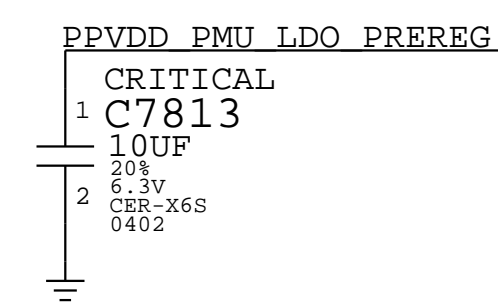
U7700
TMLT47A1-JPE
WLCSP
SYM 2 OF 4

LDO INPUTS
LDO OUTPUTS

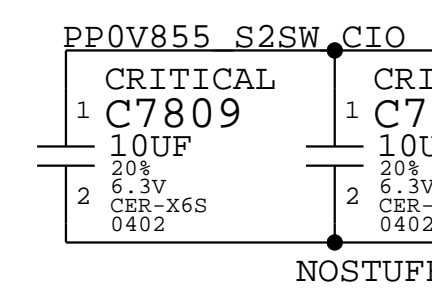
SWITCHED RAILS



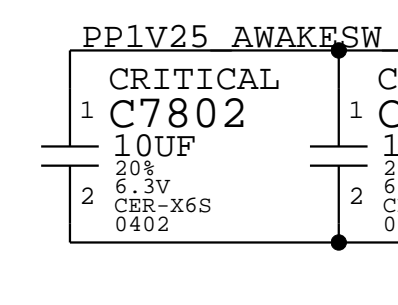
Decoupling: VDD_LDO8



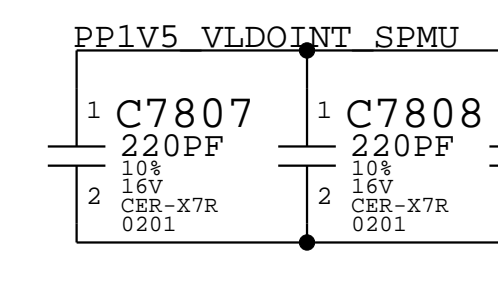
Decoupling: LDO11



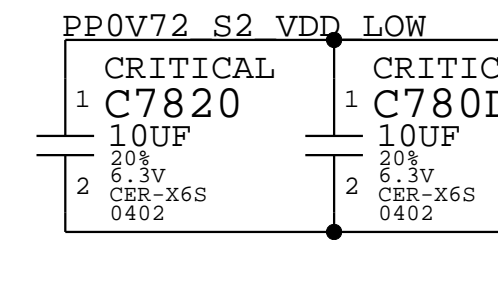
Decoupling: SW5



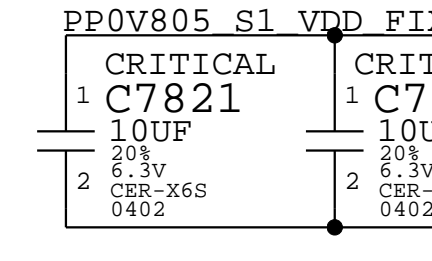
Decoupling: LDO.INT



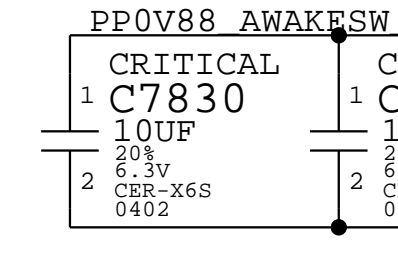
Decoupling: LDO4



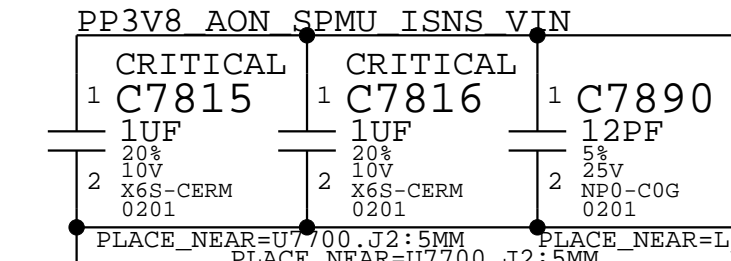
Decoupling: LDO12



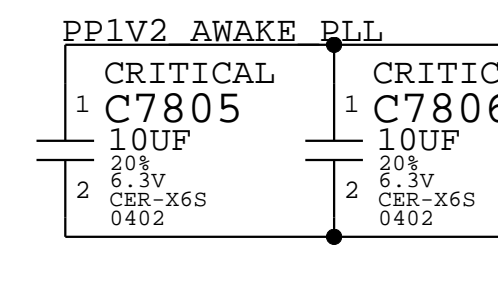
Decoupling: SW6/7



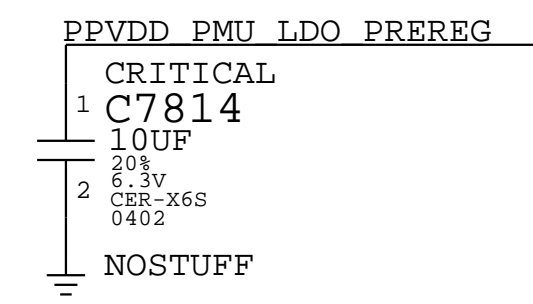
Decoupling and Desense: BSTLQ



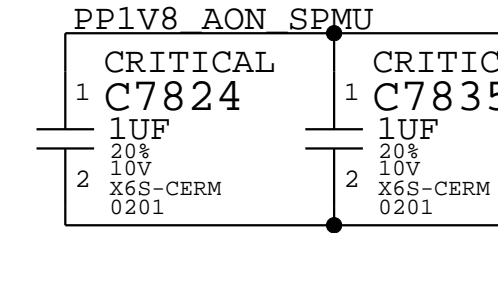
Decoupling: LDO8



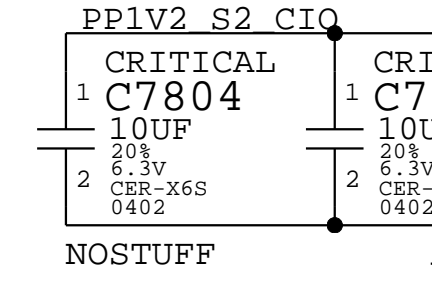
Decoupling: VDD_LDO20



Decoupling: LDO9



Decoupling: LDO20

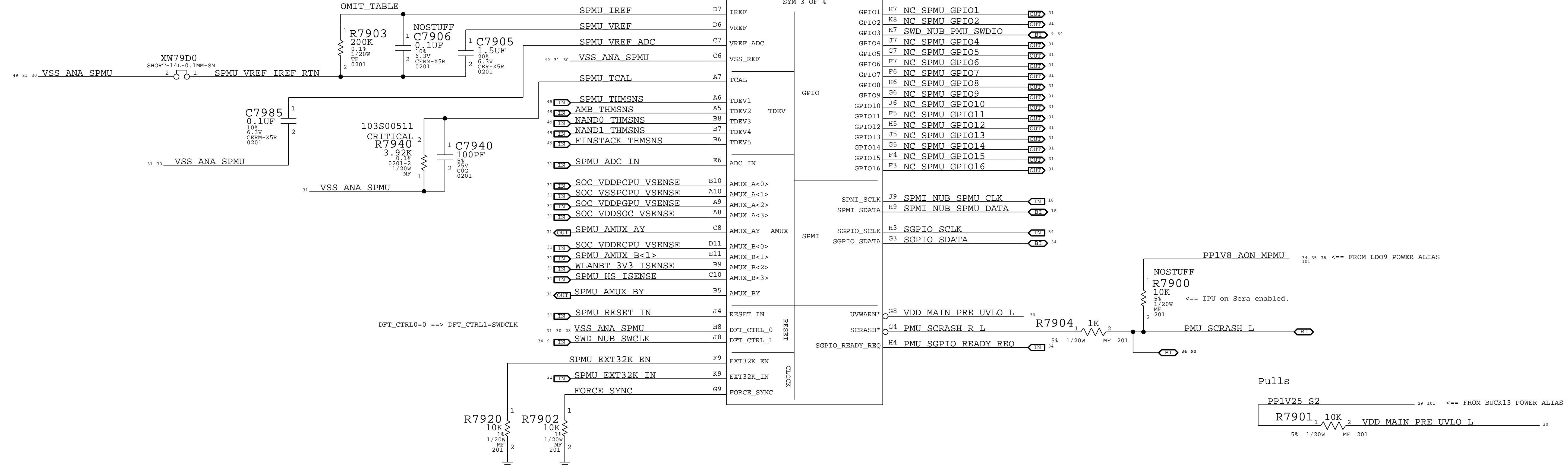


PAGE TITLE		
PMU: SLAVE LDO		
	DRAWING NUMBER	SIZE
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9.0.0		
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BOM_COST_GROUP=SOC POWER

SLAVE PMU GND, ADC, & GPIO

PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_BTN
BACK FROM THE VREF / IREF PASSIVES

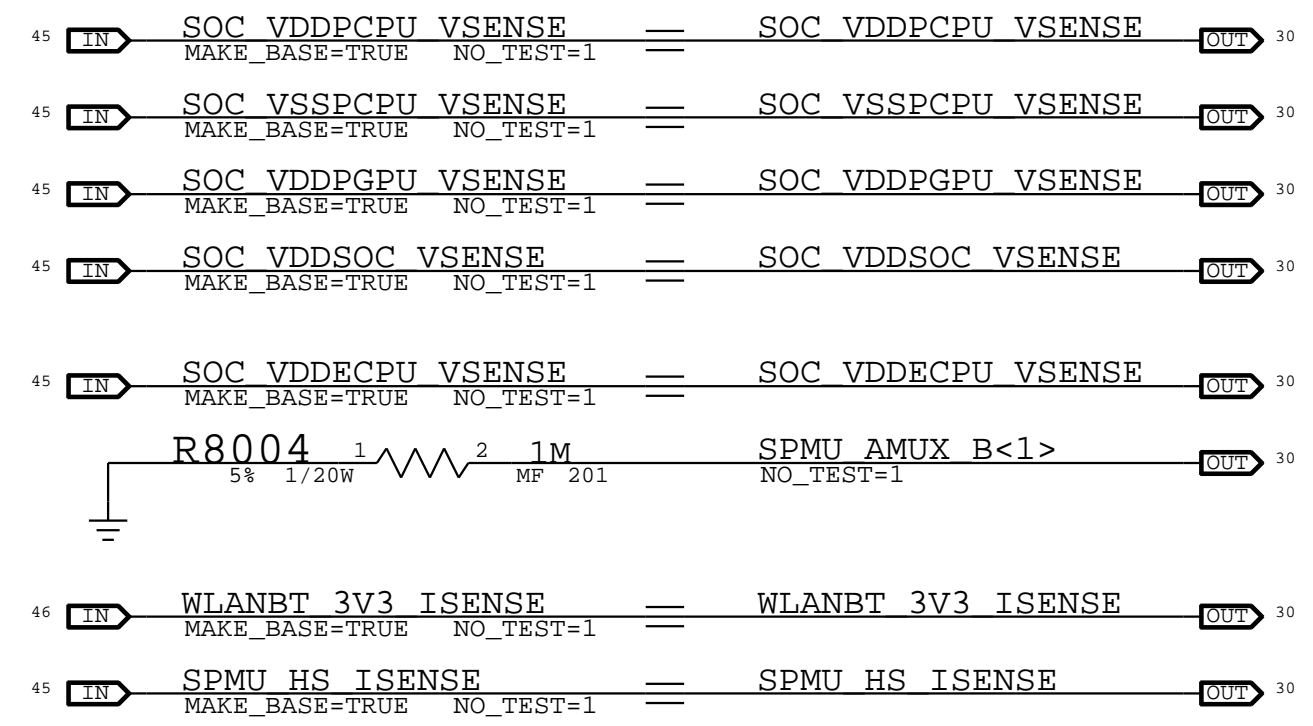


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11850738	1	RES_THICKFILM,200KOHM,0.1%,1/20W,0201	R7903	CRITICAL	PMU_IREF:EXT
11750201	1	RES_MF,1A MAX, 0.0 OHM,5%,0201,BLACK	R7903	CRITICAL	PMU_IREF:INT

PAGE TITLE		
PMU: SLAVE GPIO & GND		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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BOM_COST_GROUP=SOC POWER

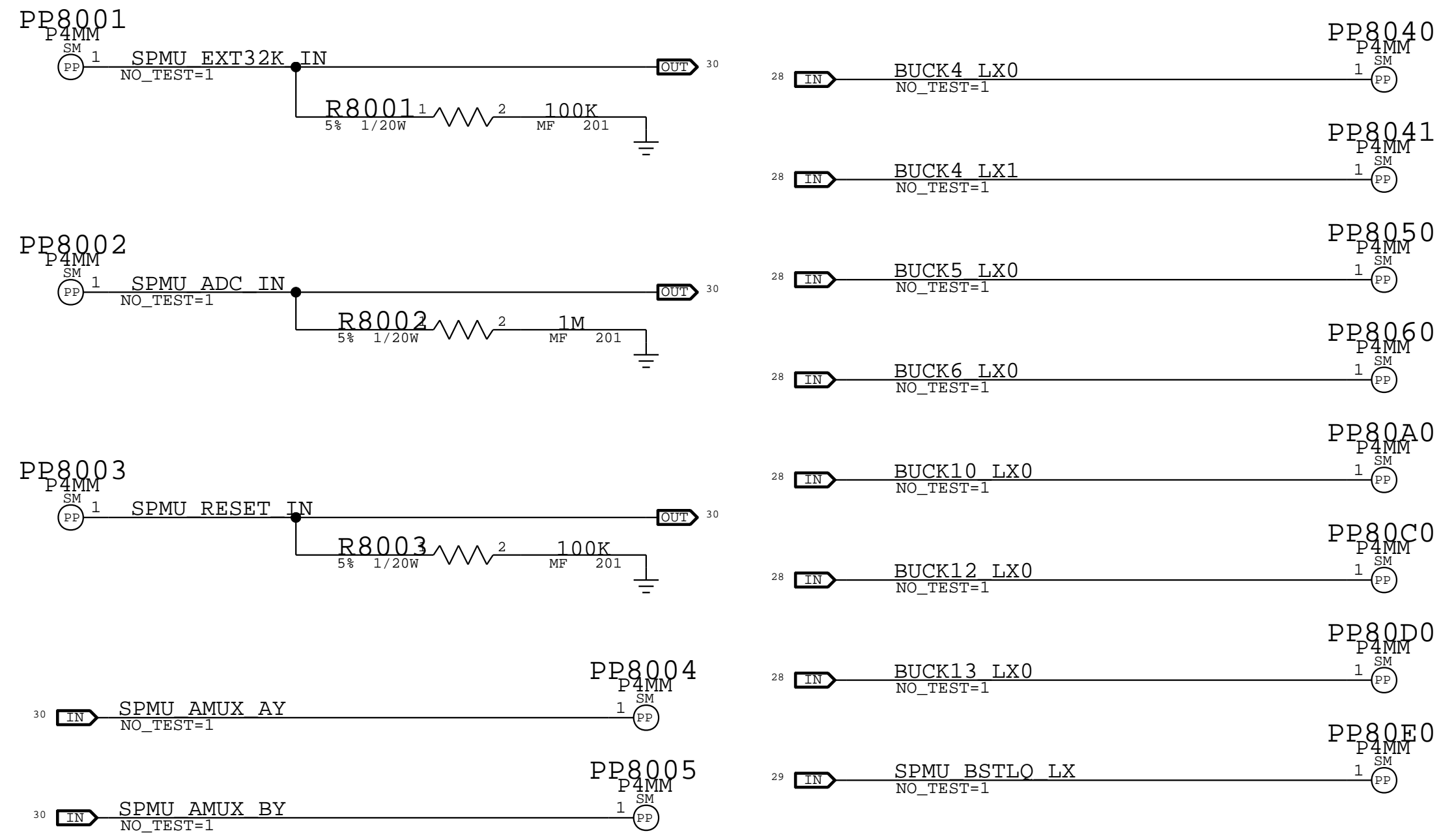
SLAVE PMU AMUX ALIAS



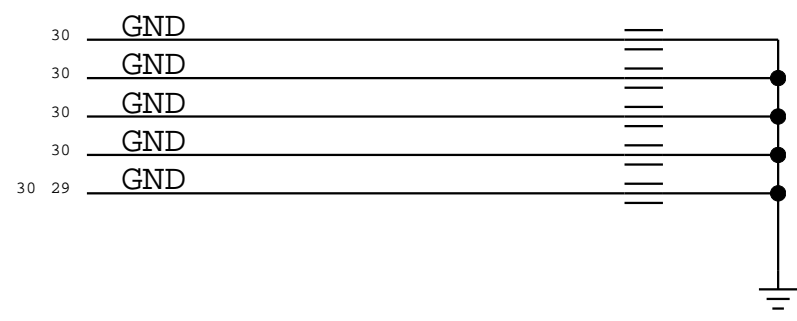
SLAVE PMU GPIOs



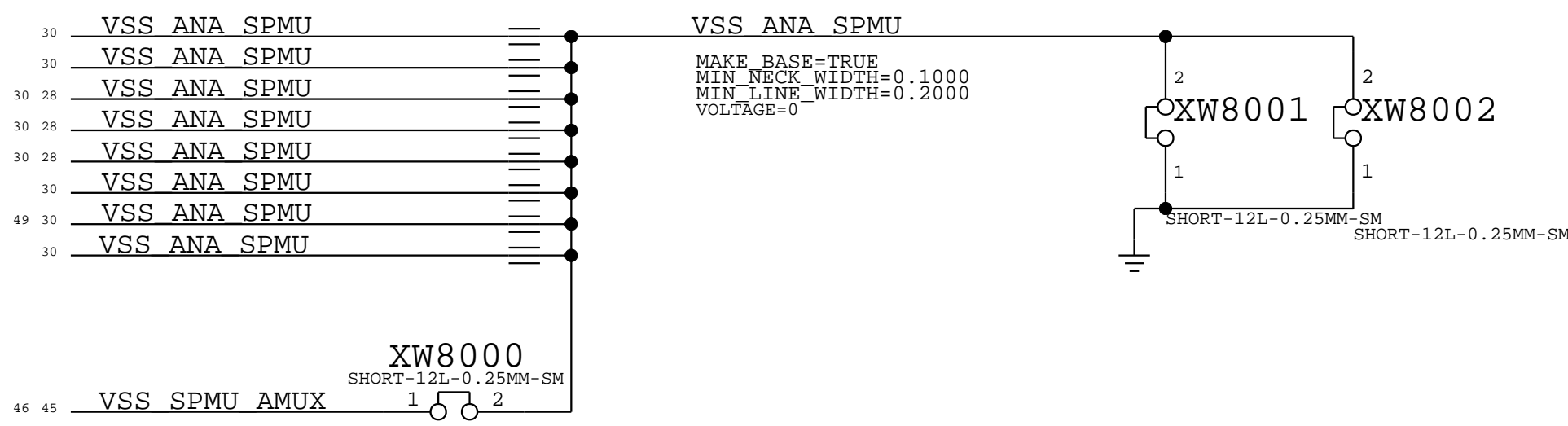
SLAVE PMU PROBE POINTS



VSS alias connection



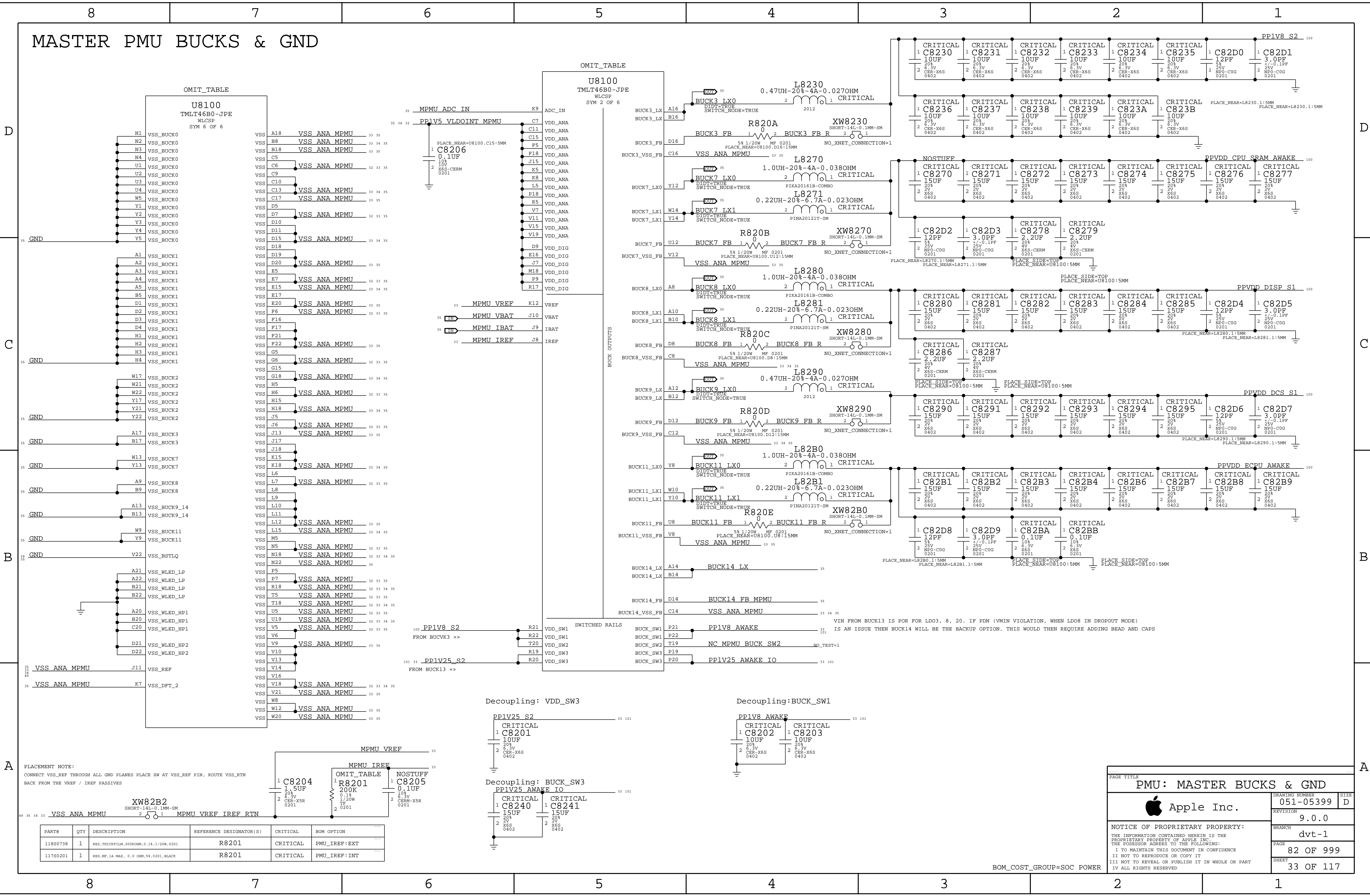
& WIDTH XW IS LAYOUT DEPENDENT



PAGE TITLE		
PMU: SLAVE SUPPORT		
Apple Inc.	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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BOM_COST_GROUP=SOC POWER

MASTER PMU BUCKS & GND



PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN BACK FROM THE VREF / IREF PASSIVES

BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11850738	1	RES, THICKFILM, 200KOHM, 0.1%, 1/20W, 0201	R8201	CRITICAL	PMU_IREF:EXT
11750201	1	RES, MF, 1A MAX, 0.0 OHM, 5%, 0201, BLACK	R8201	CRITICAL	PMU_IREF:INT

PMU: MASTER BUCKS & GND

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	BRANCH	
	dvt-1	
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	82 OF 999	
	SHEET	
	33 OF 117	

BOM_COST_GROUP=SOC POWER

MASTER PMU LDO, ADC, & GPIO

D

C

B

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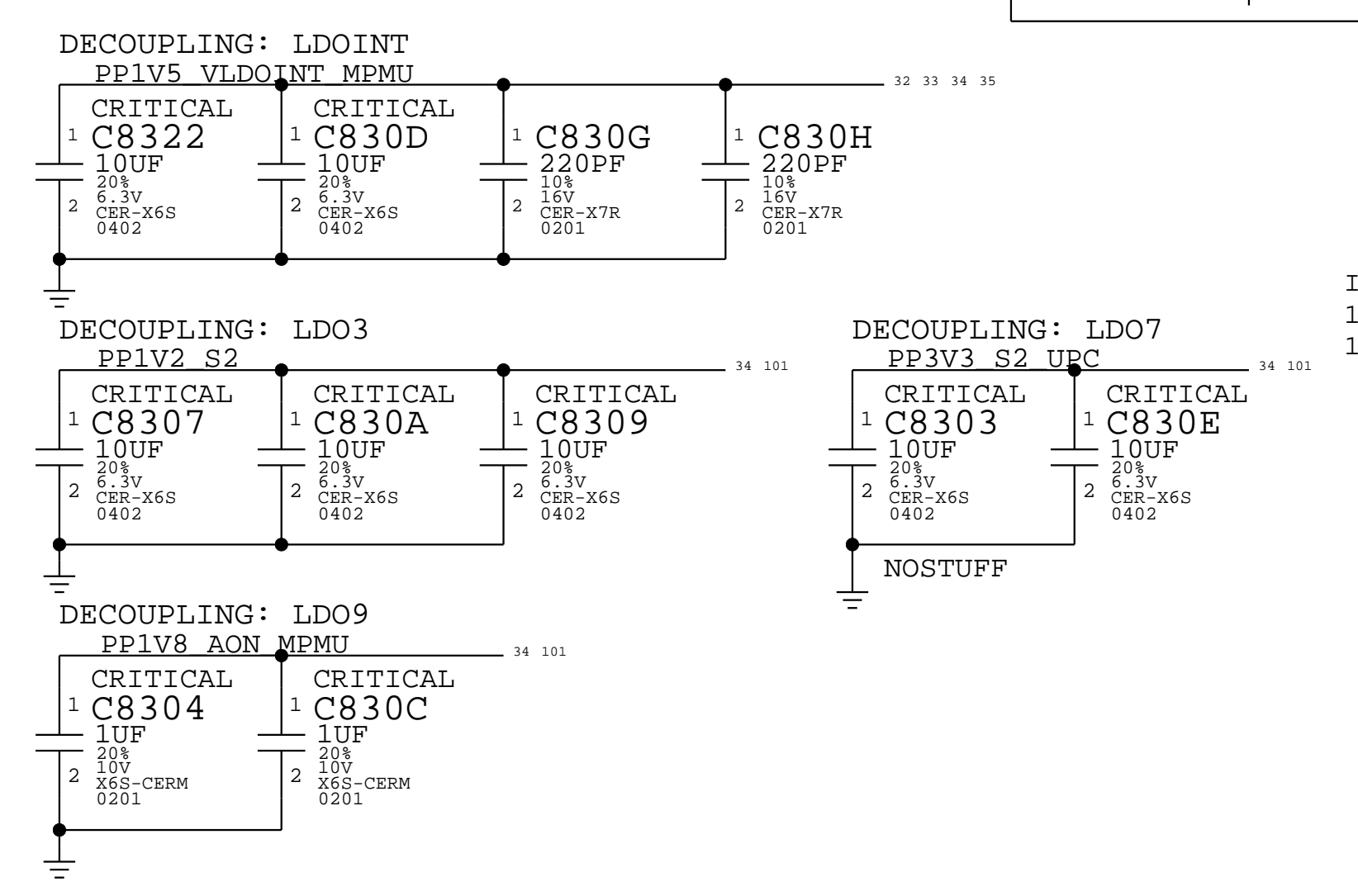
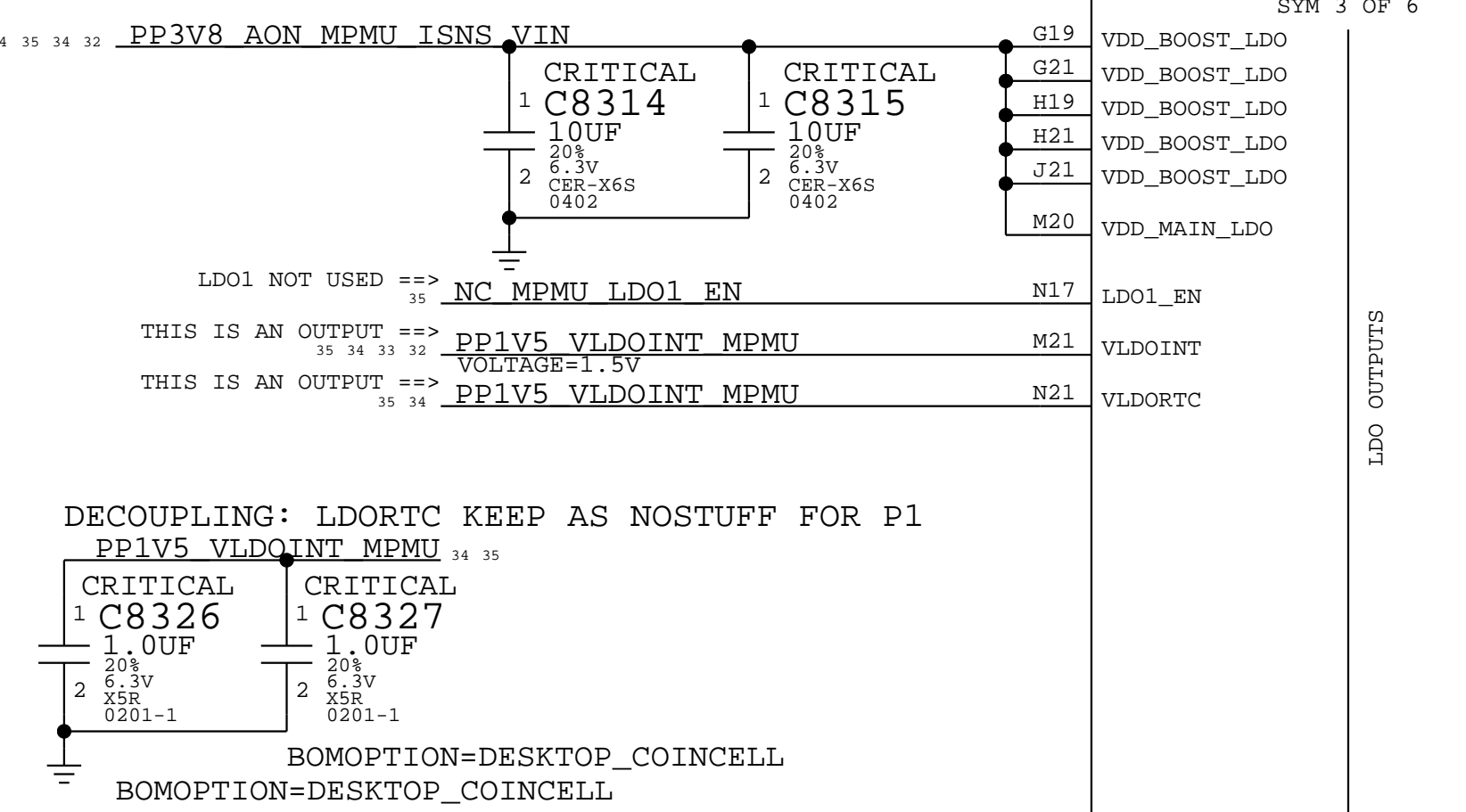
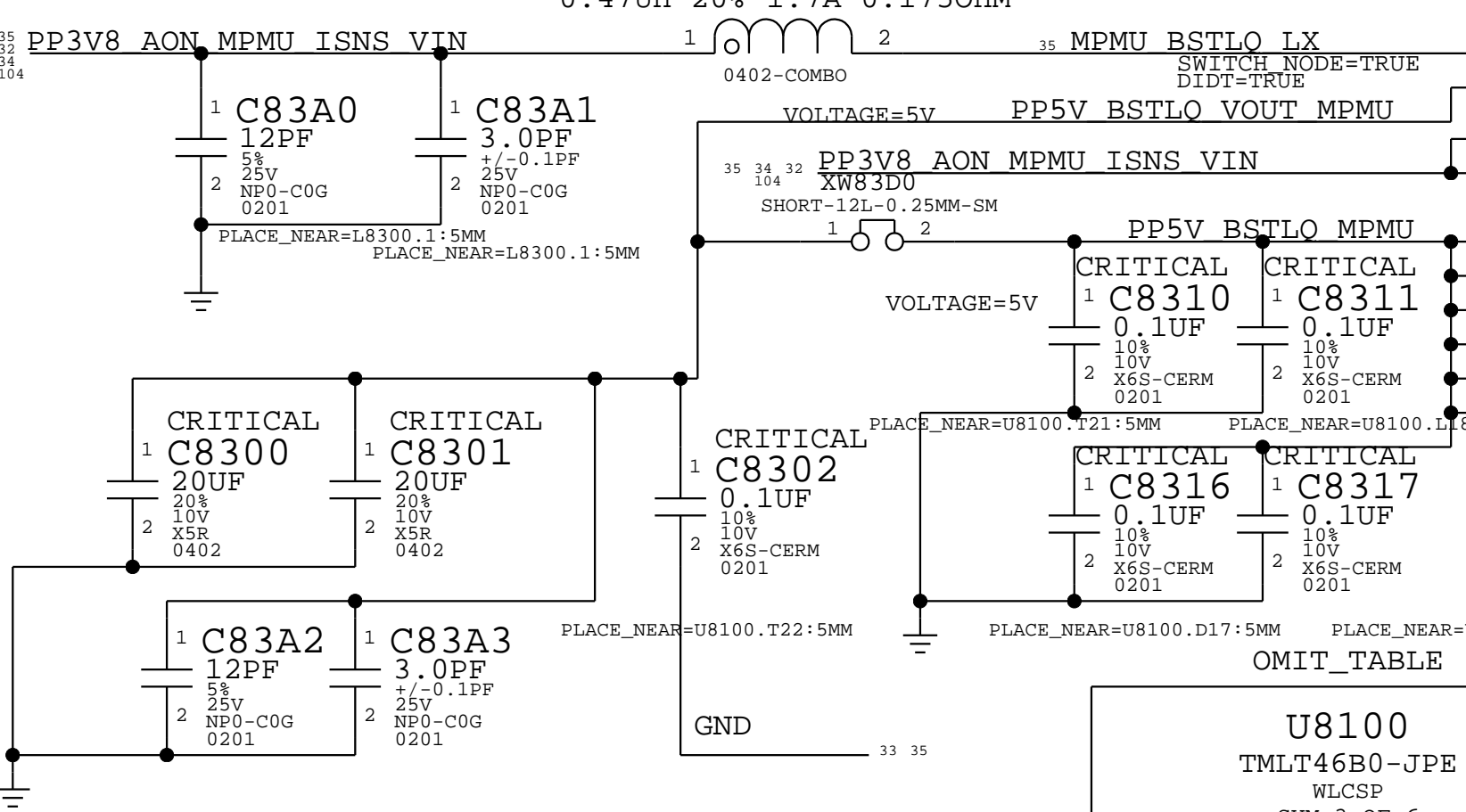
D

C

B

A

NO_TEST=1	NC MPMU IDAC OUT<0>	G17	IDAC_OUT<0>	WLED_LP_LX	C21	NC MPMU WLED LP LX 0	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<1>	G16	IDAC_OUT<1>	WLED_LP_LX <td>C22</td> <td>NC MPMU WLED LP LX 1</td> <td>NO_TEST=1</td>	C22	NC MPMU WLED LP LX 1	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<2>	G14	IDAC_OUT<2>				
NO_TEST=1	NC MPMU IDAC OUT<3>	G13	IDAC_OUT<3>				
NO_TEST=1	NC MPMU IDAC OUT<4>	H17	IDAC_OUT<4>	WLED_HP1_LX <td>A19</td> <td>NC MPMU WLED HP1 LX 0</td> <td>NO_TEST=1</td>	A19	NC MPMU WLED HP1 LX 0	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<5>	H16	IDAC_OUT<5>	WLED_HP1_LX <td>B19</td> <td>NC MPMU WLED HP1 LX 1</td> <td>NO_TEST=1</td>	B19	NC MPMU WLED HP1 LX 1	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<6>	H14	IDAC_OUT<6>	WLED_HP1_LX <td>C19</td> <td>NC MPMU WLED HP1 LX 2</td> <td>NO_TEST=1</td>	C19	NC MPMU WLED HP1 LX 2	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<7>	H13	IDAC_OUT<7>				
NO_TEST=1	NC MPMU IDAC OUT<8>	J16	IDAC_OUT<8>				
NO_TEST=1	NC MPMU IDAC OUT<9>	J14	IDAC_OUT<9>				
NO_TEST=1	NC MPMU IDAC OUT<10>	K17	IDAC_OUT<10>	WLED_HP2_LX <td>E21</td> <td>NC MPMU WLED HP2 LX 0</td> <td>NO_TEST=1</td>	E21	NC MPMU WLED HP2 LX 0	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<11>	K16	IDAC_OUT<11>	WLED_HP2_LX <td>E22</td> <td>NC MPMU WLED HP2 LX 1</td> <td>NO_TEST=1</td>	E22	NC MPMU WLED HP2 LX 1	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<12>	K14	IDAC_OUT<12>				
NO_TEST=1	NC MPMU IDAC OUT<13>	K13	IDAC_OUT<13>				
NO_TEST=1	NC MPMU IDAC OUT<14>	L17	IDAC_OUT<14>				
NO_TEST=1	NC MPMU IDAC OUT<15>	L16	IDAC_OUT<15>				
NO_TEST=1	NC MPMU IDAC OUT<16>	L14	IDAC_OUT<16>	WLED_VOUT_FB <td>E18</td> <td>NC MPMU WLED VOUT_FB</td> <td>NO_TEST=1</td>	E18	NC MPMU WLED VOUT_FB	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<17>	L13	IDAC_OUT<17>	VCP_OUT_SPARE <td>U21</td> <td>NC MPMU VCP_OUT_SPARE</td> <td>NO_TEST=1</td>	U21	NC MPMU VCP_OUT_SPARE	NO_TEST=1
NO_TEST=1	NC MPMU IDAC OUT<17>	L13	IDAC_OUT<17>	VMBX_SPARE <td>J12</td> <td>NC MPMU VMBX_SPARE</td> <td>NO_TEST=1</td>	J12	NC MPMU VMBX_SPARE	NO_TEST=1



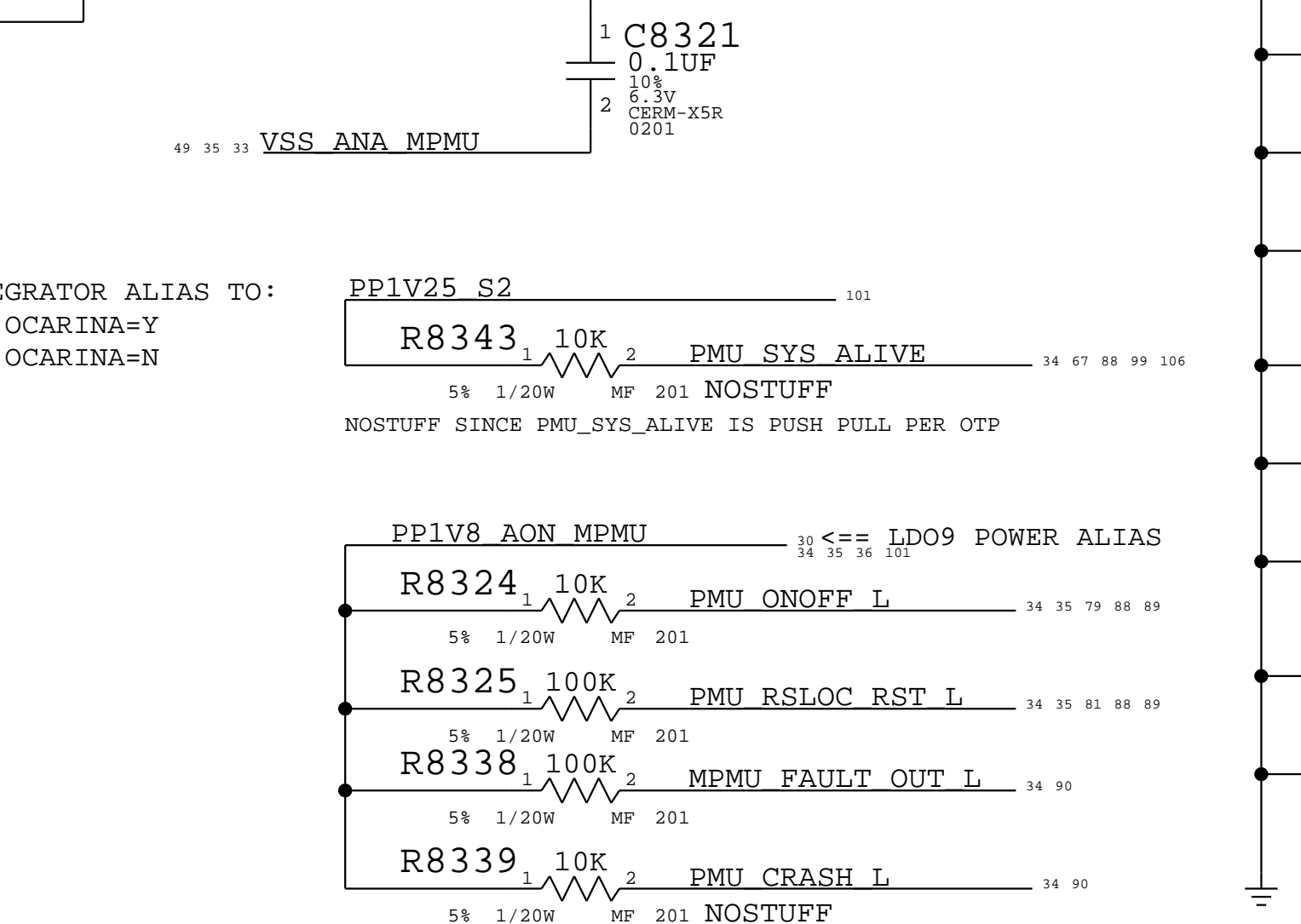
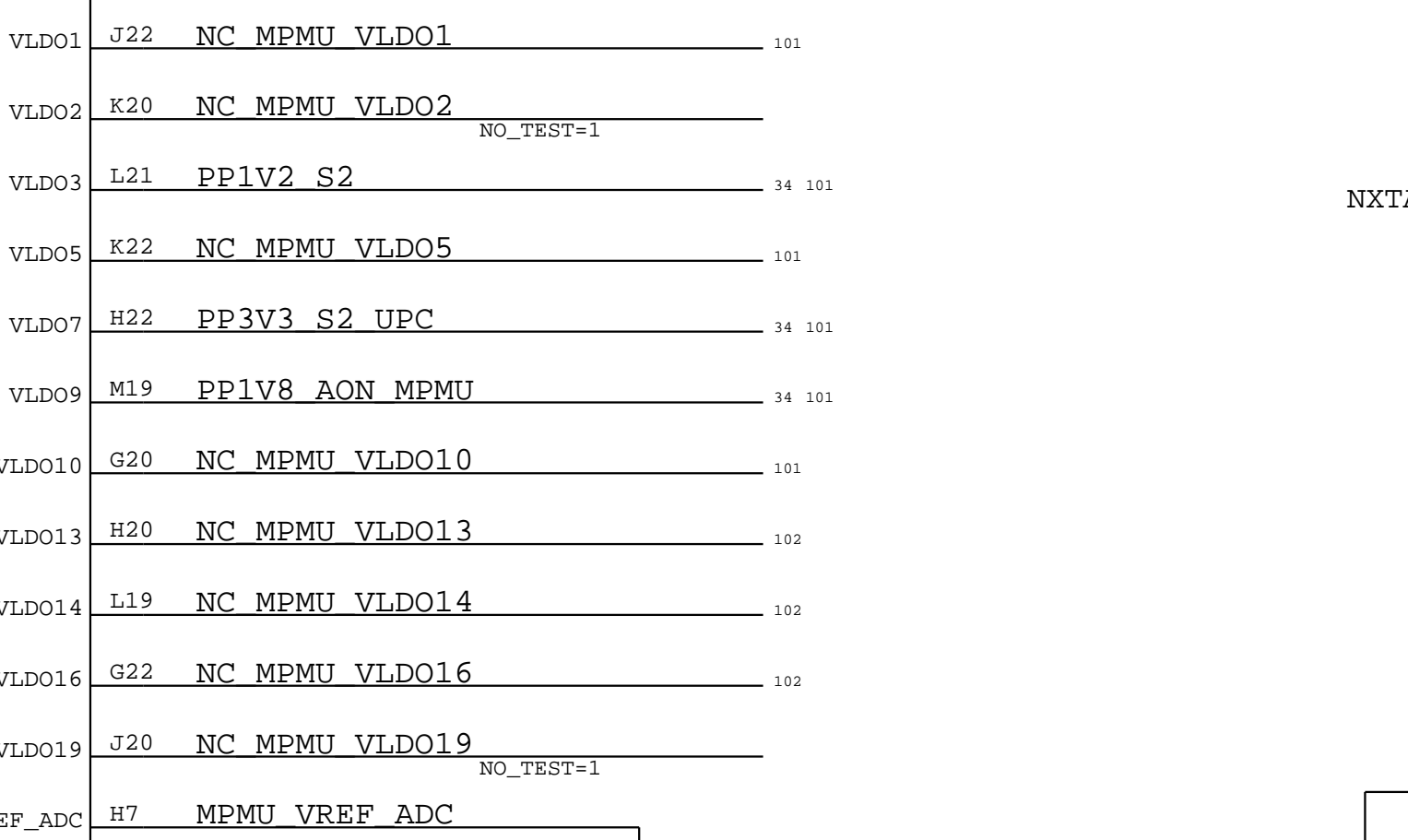
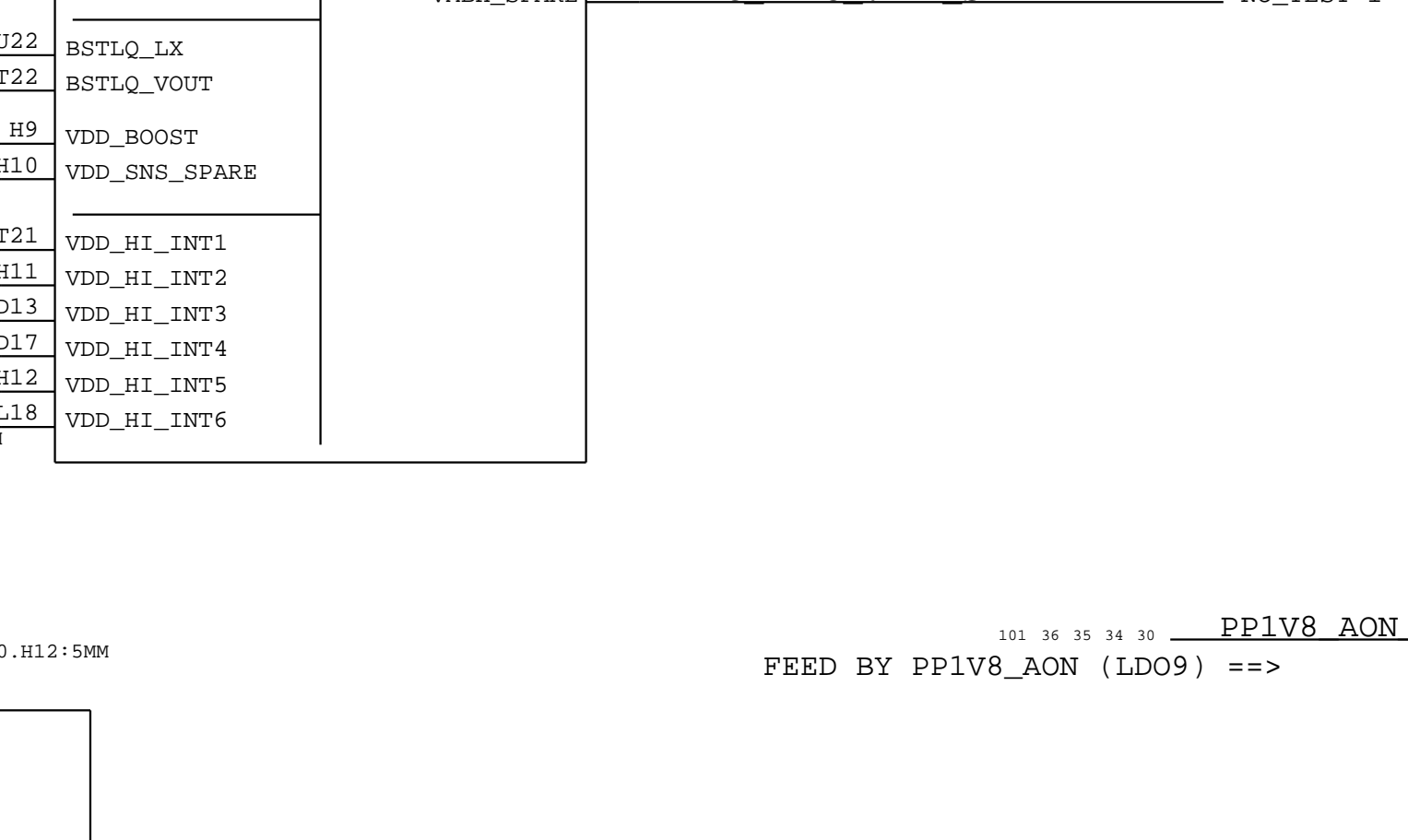
BOM_COST_GROUP=SOC POWER

8 7 6 5 4 3 2 1

OMIT_TABLE

U8100
TMLT46B0-JPE
WLCSP
SYM 5 OF 6

U8100	U8100	U8100	U8100	U8100	U8100	U8100	U8100
WLED_LP_LX	C21	NC MPMU WLED LP LX 0	NO_TEST=1	WLED_LP_LX	C22	NC MPMU WLED LP LX 1	NO_TEST=1
WLED_HP1_LX	A19	NC MPMU WLED HP1 LX 0	NO_TEST=1	WLED_HP1_LX	B19	NC MPMU WLED HP1 LX 1	NO_TEST=1
WLED_HP1_LX	C19	NC MPMU WLED HP1 LX 2	NO_TEST=1	WLED_HP2_LX	E21	NC MPMU WLED HP2 LX 0	NO_TEST=1
WLED_HP2_LX	E22	NC MPMU WLED HP2 LX 1	NO_TEST=1	WLED_VOUT_FB	E18	NC MPMU WLED VOUT_FB	NO_TEST=1
VCP_OUT_SPARE	U21	NC MPMU VCP_OUT_SPARE	NO_TEST=1	VMBX_SPARE	J12	NC MPMU VMBX_SPARE	NO_TEST=1



BOM_COST_GROUP=SOC POWER

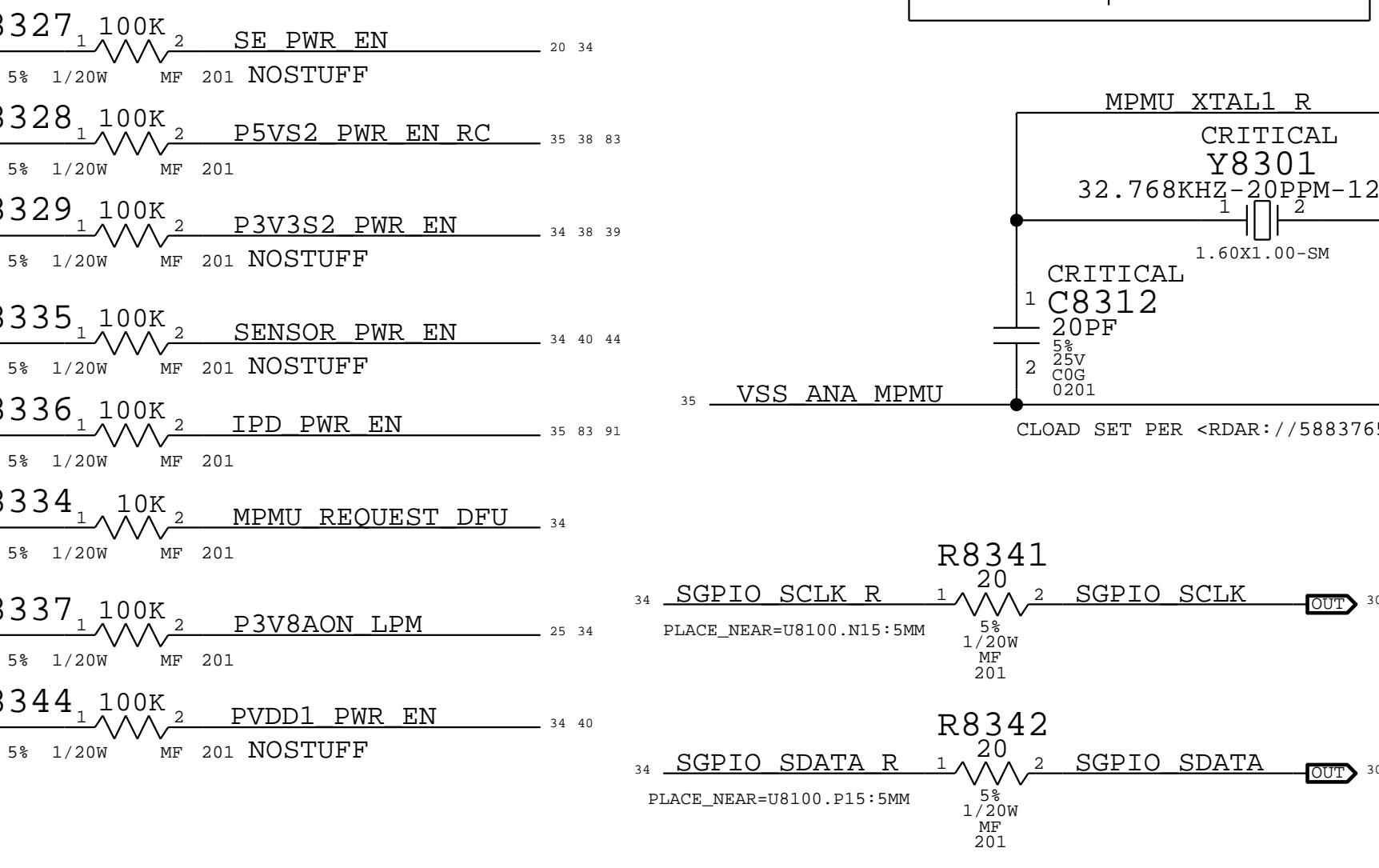
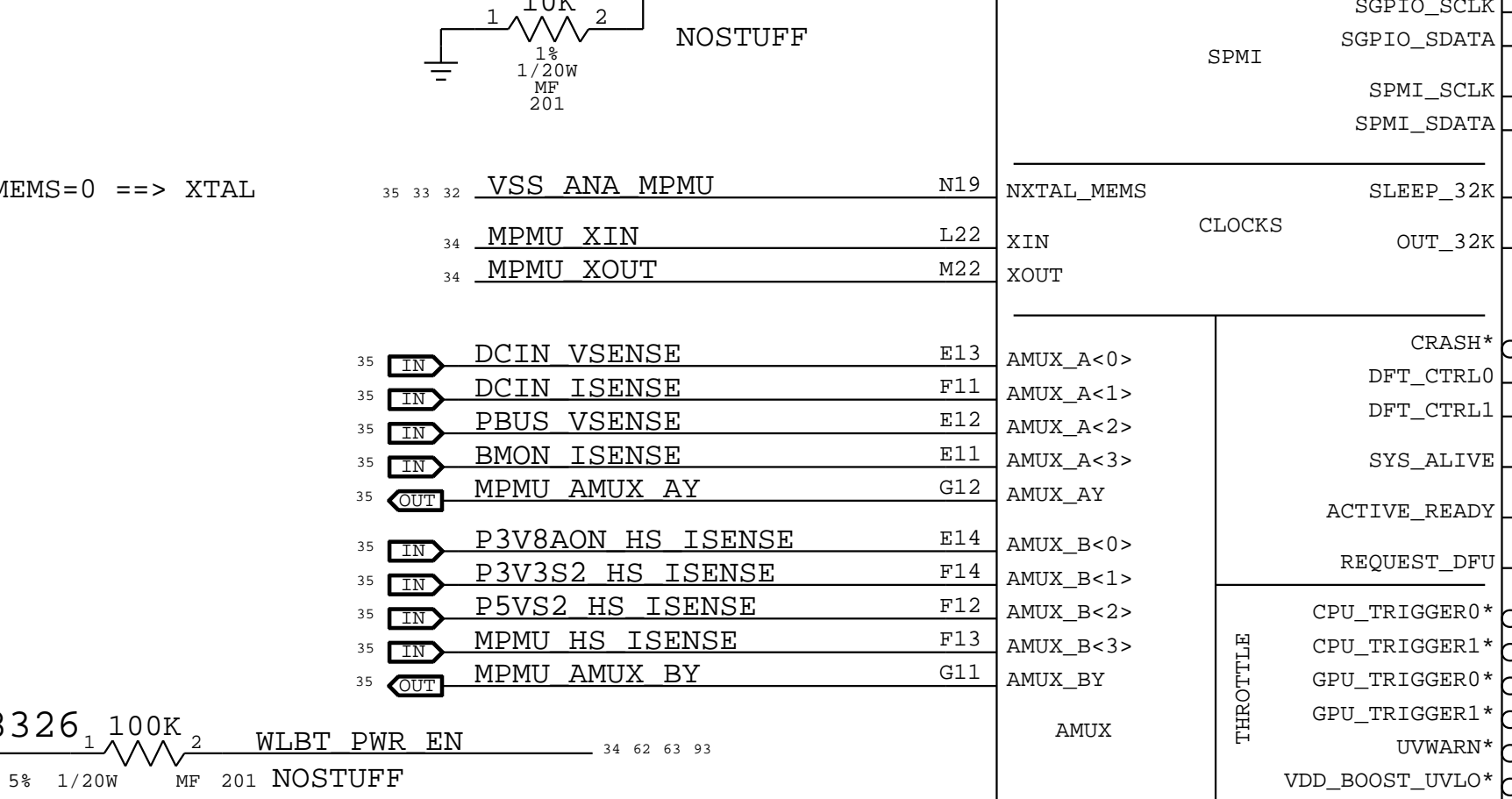
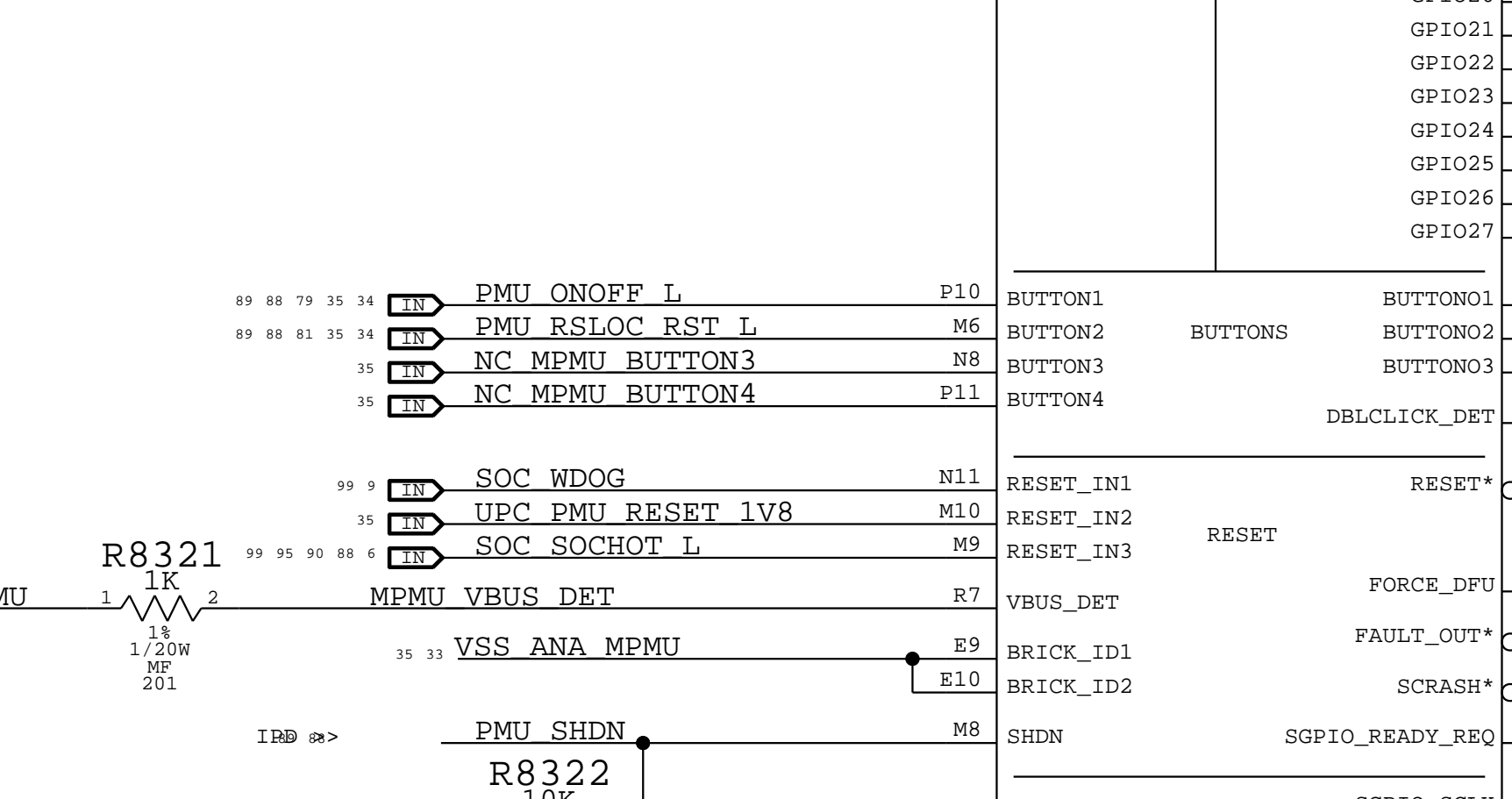
8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

OMIT_TABLE

U8100
TMLT46B0-JPE
WLCSP
SYM 4 OF 6

U8100	U8100	U8100	U8100	U8100	U8100	U8100	U8100
TDEV1	P16	IPD LID OPEN LV8	GPIO1	TDEV2	T9	CHGR AUX OK	GPIO2
TDEV3	T7	SWD NUB PMU SWDIO	GPIO3	TDEV4	R11	CODEC WAKE L	GPIO4
TDEV5	T8	WLBT WAKE	GPIO5	TDEV6	U7	MPMU GPIO6	GPIO6
TDEV7	T11	NC HDMI CEC IRO	GPIO7	TDEV8	U10	NC USB3 WAKE	GPIO8
TCAL	U9	MPMU GPIO10	GPIO10	TCAL	U11	PVDD1 PWR EN	GPIO11
TCAL	U12	P3V3S2 PWR EN	GPIO12	TCAL	U13	WLBT PWR EN	GPIO13
TCAL	U15	MPMU GPIO14	GPIO14	TCAL	U17	NC USB3 PWR EN	GPIO17
TCAL	U18	SE PWR EN	GPIO18	TCAL	U19	MPMU GPIO20	GPIO19
TCAL	U21	MPMU GPIO22	GPIO22	TCAL	U22	NC USB3 PWR EN	GPIO23
TCAL	U23	MPMU GPIO26	GPIO26	TCAL	U24	NC UWB PWR EN	GPIO24
TCAL	U25	MPMU GPIO27	GPIO27	TCAL	U26	NC MPMU GPIO26	GPIO26
TCAL	U27	NC MPMU GPIO27	GPIO27	TCAL	U28	NC MPMU GPIO27	GPIO27



BOM_COST_GROUP=SOC POWER

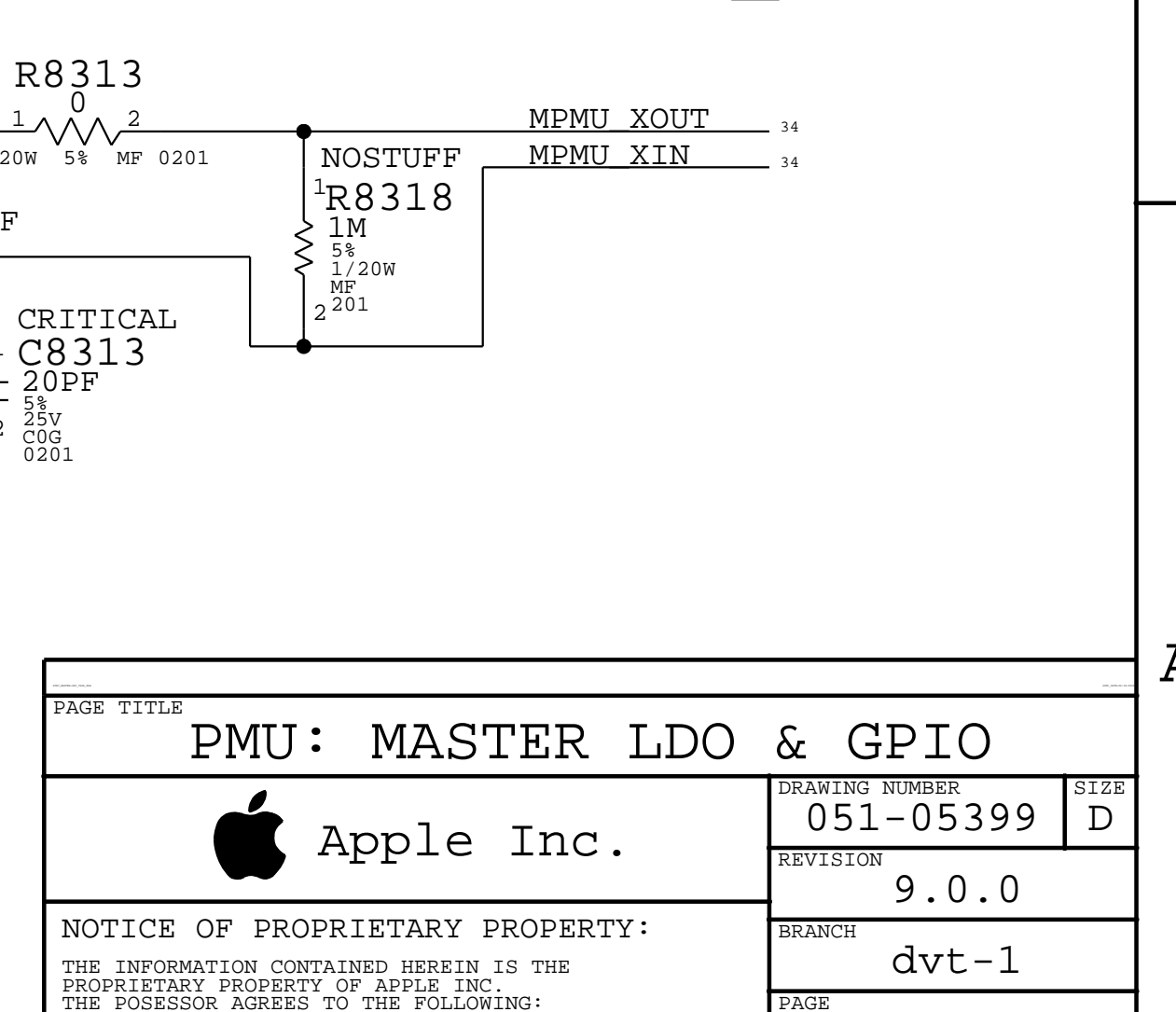
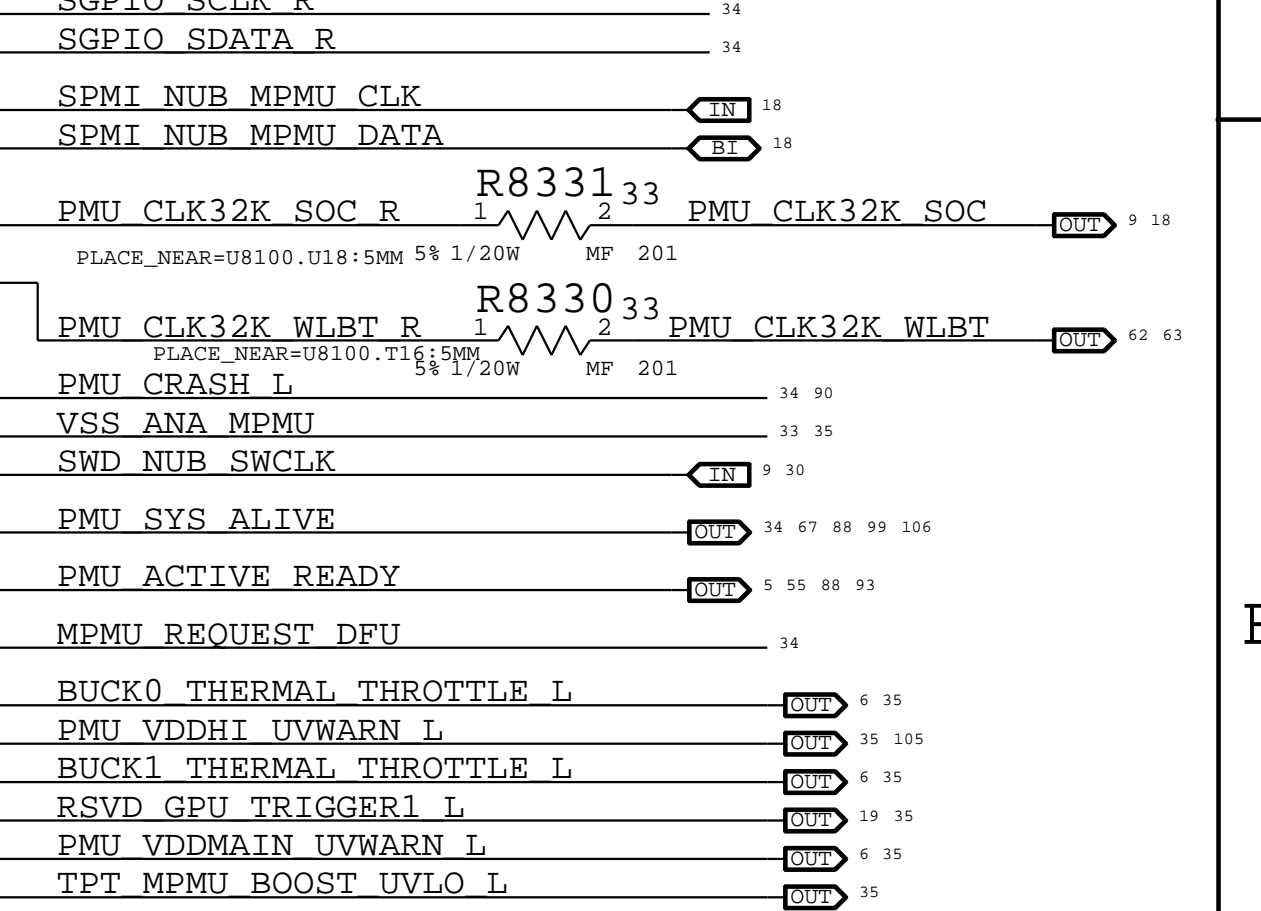
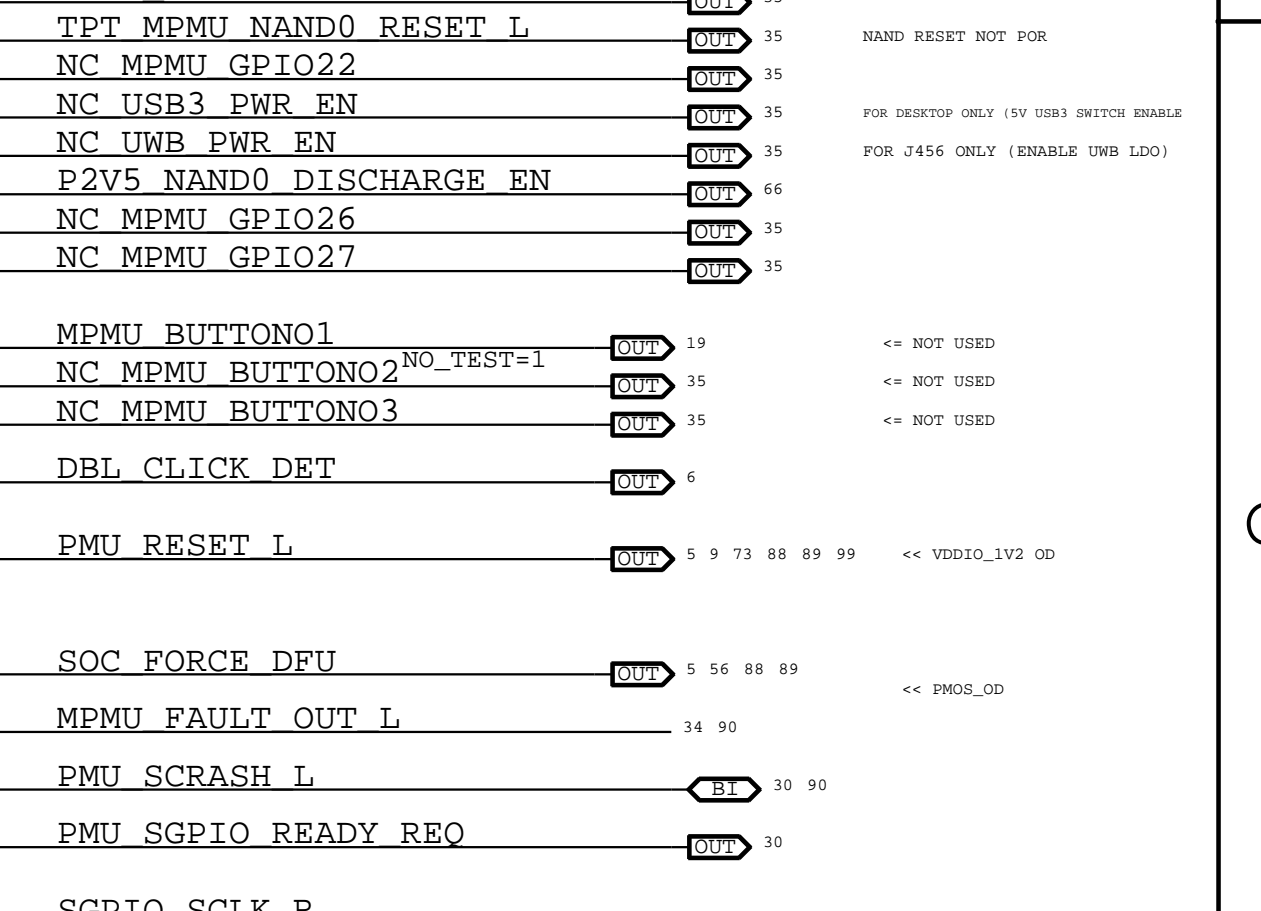
8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

OMIT_TABLE

U8100
TMLT46B0-JPE
WLCSP
SYM 4 OF 6

U8100	U8100	U8100	U8100	U8100	U8100	U8100	U8100
GPIO1	P16	IPD LID OPEN LV8	GPIO1	GPIO2	T9	CHGR AUX OK	GPIO2
GPIO3	T7	SWD NUB PMU SWDIO	GPIO3	GPIO4	R11	CODEC WAKE L	GPIO4
GPIO5	T8	WLBT WAKE	GPIO5	GPIO6	U7	MPMU GPIO6	GPIO6
GPIO7	T11	NC HDMI CEC IRO	GPIO7	GPIO8	U10	NC USB3 WAKE	GPIO8
GPIO9	U9	MPMU GPIO10	GPIO10	GPIO11	U11	PVDD1 PWR EN	GPIO11
GPIO12	U12	P3V3S2 PWR EN	GPIO12	GPIO13	U13	WLBT PWR EN	GPIO13
GPIO14	U15	MPMU GPIO14	GPIO14	GPIO15	U17	NC USB3 PWR EN	GPIO17
GPIO18	U18	SE PWR EN	GPIO18	GPIO19	U19	MPMU GPIO20	GPIO19
GPIO22	U21	MPMU GPIO22	GPIO22	GPIO23	U22	NC USB3 PWR EN	GPIO23
GPIO24	U23	MPMU GPIO26	GPIO26	GPIO26	U24	NC UWB PWR EN	GPIO24
GPIO27	U25	MPMU GPIO27	GPIO27	GPIO27	U26	NC MPMU GPIO26	GPIO26
GPIO27	U27	NC MPMU GPIO27	GPIO27	GPIO27	U28	NC MPMU GPIO27	GPIO27



BOM_COST_GROUP=SOC POWER

8 7 6 5 4 3 2 1

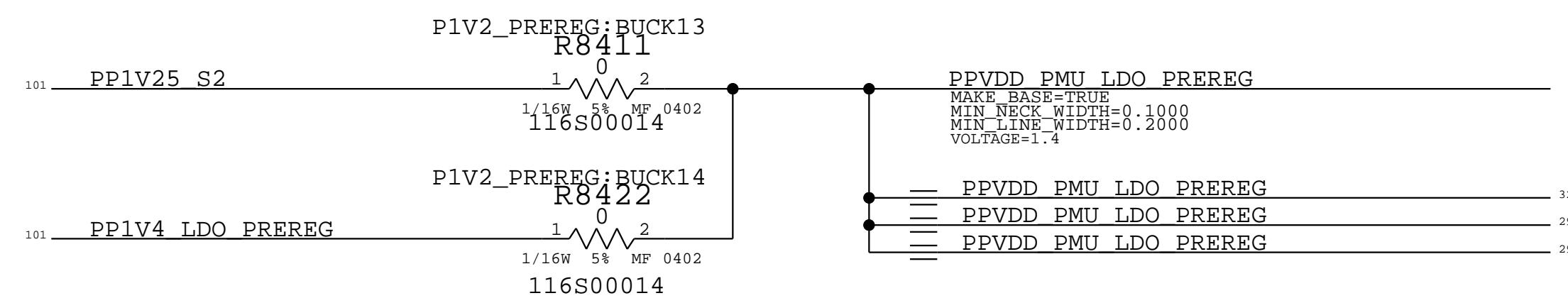
8 7 6 5 4 3 2 1

PAGE TITLE		PMU: MASTER LDO & GPIO	
DRAWING NUMBER		051-05399	
REVISION		9.0.0	
BRANCH		dvt-1	
PAGE		83 OF 999	
SHEET		34 OF 117	

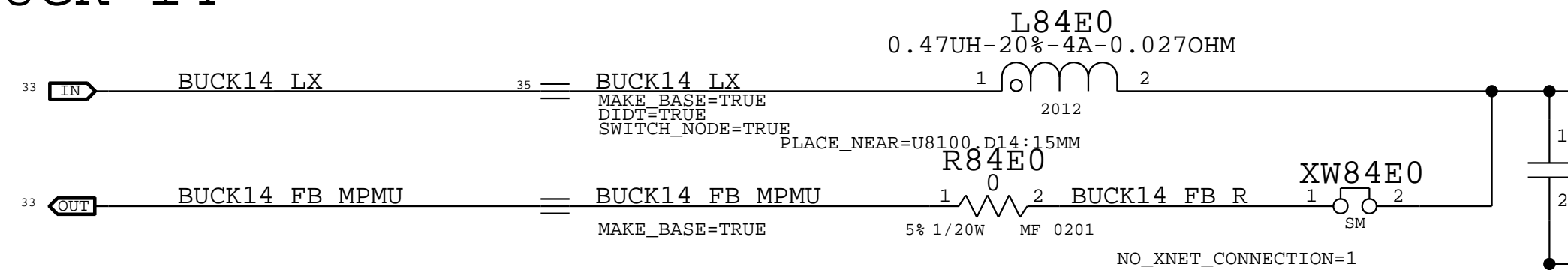
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I ALL RIGHTS RESERVED

PP1V2 LDO VDD IN option (LDO3, 8, 20)

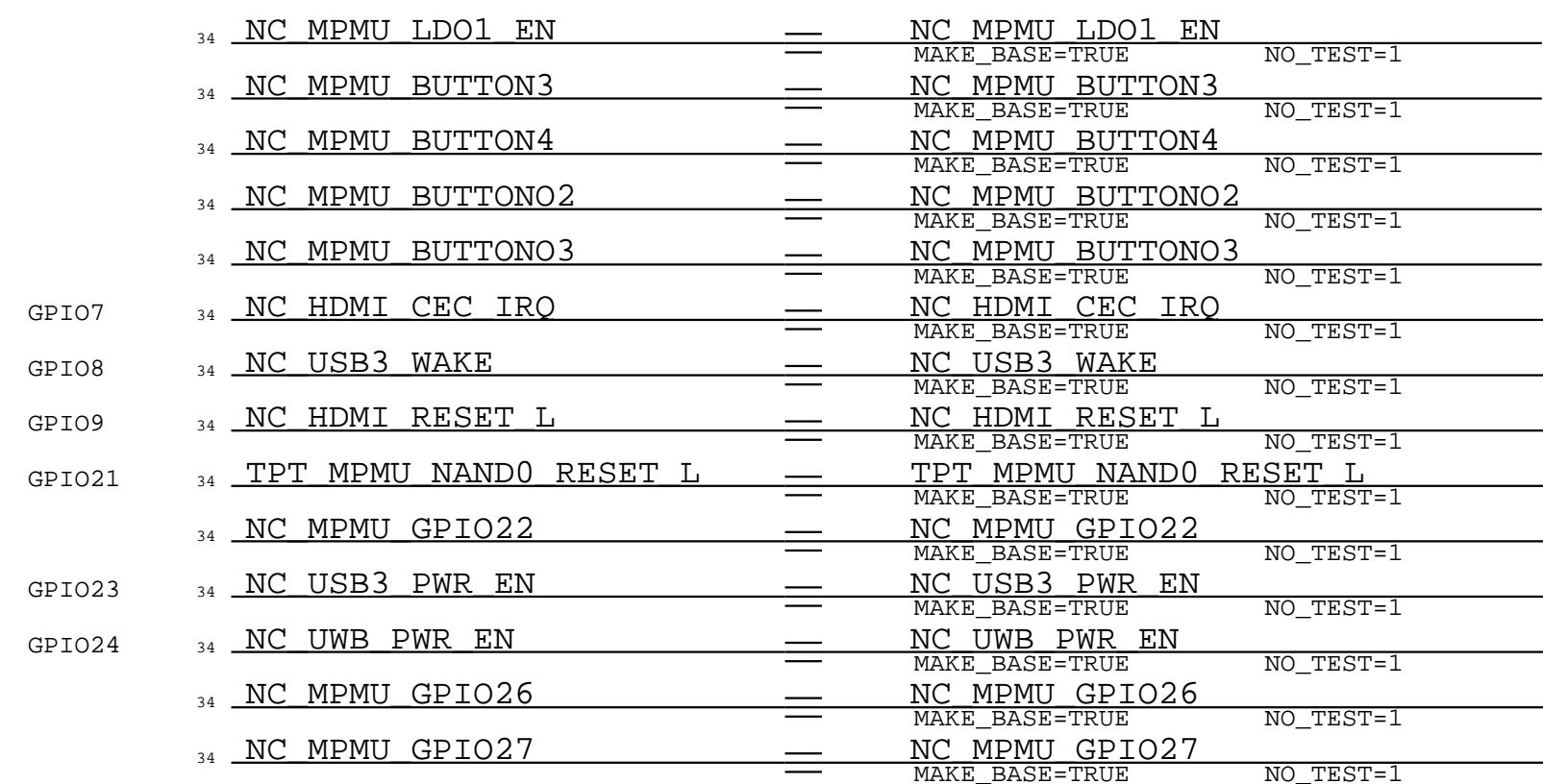
Stuff R8422 for BUCK14 pre-regulator (Proto2 and later)



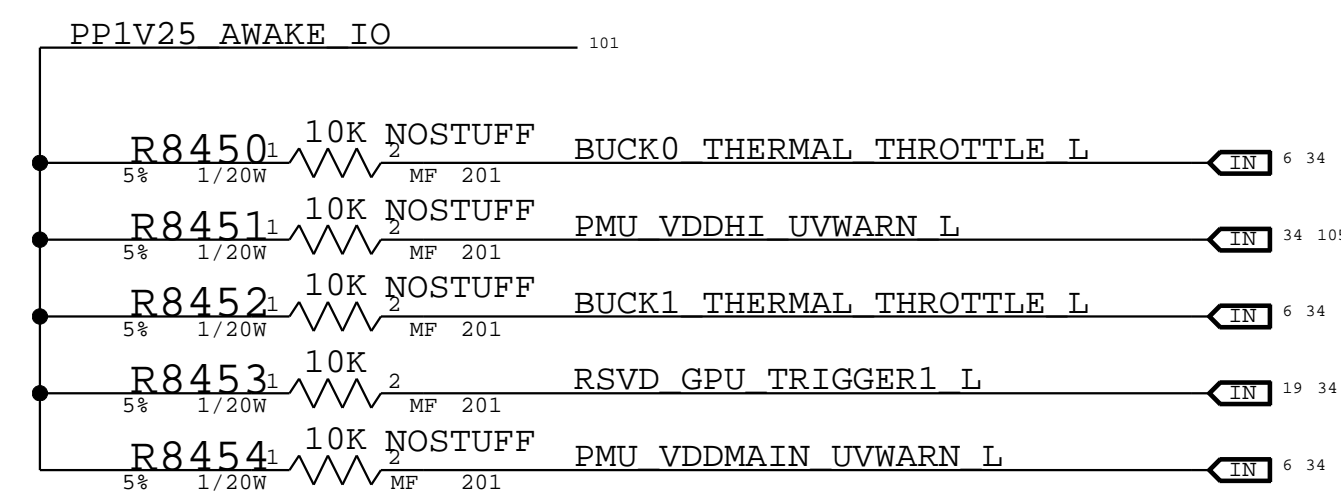
BUCK 14



MASTER PMU SIGNALS

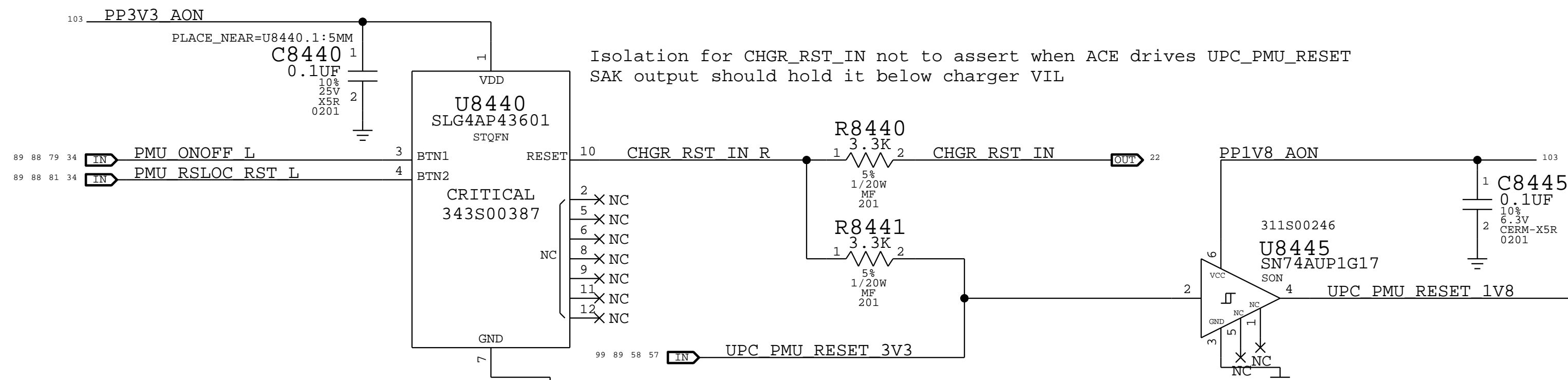


EXTERNAL PULL UPS FOR THROTTLE SIGNALS: SOC HAS IPU

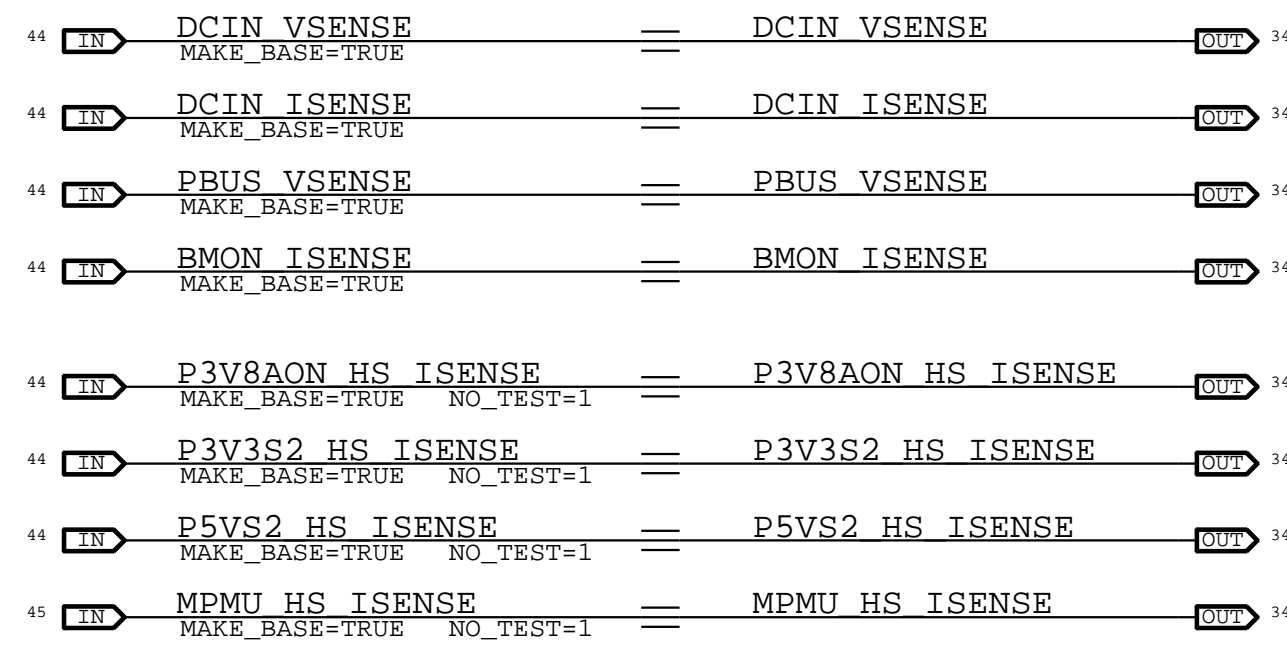


CHARGER RESET CIRCUIT

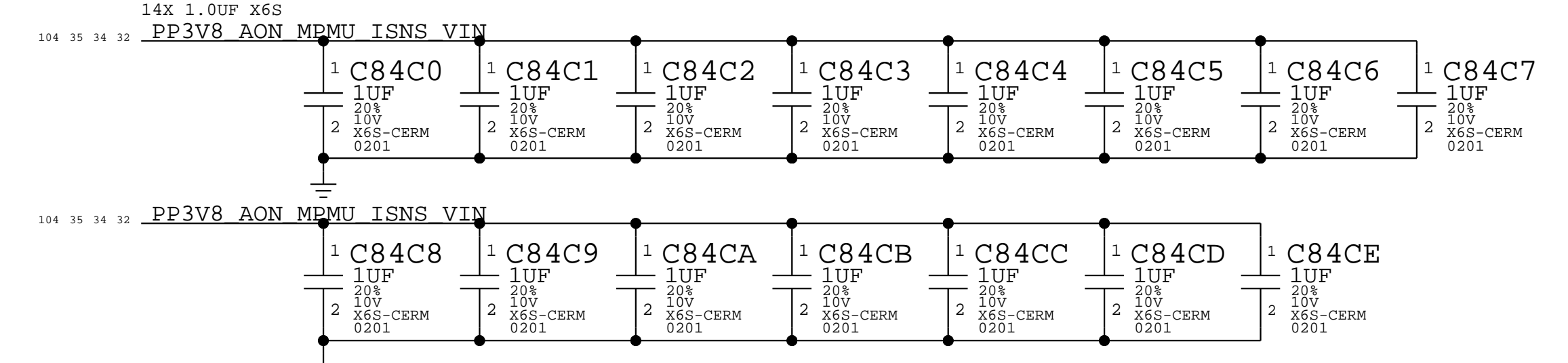
RIGHT SHIFT & LEFT OPTION CONTROL (RSLOC) FOLLOWED BY ON-OFF BUTTON PRESS. NEW APN 343S00387 can take 1.8V as BTN1/2 inputs.



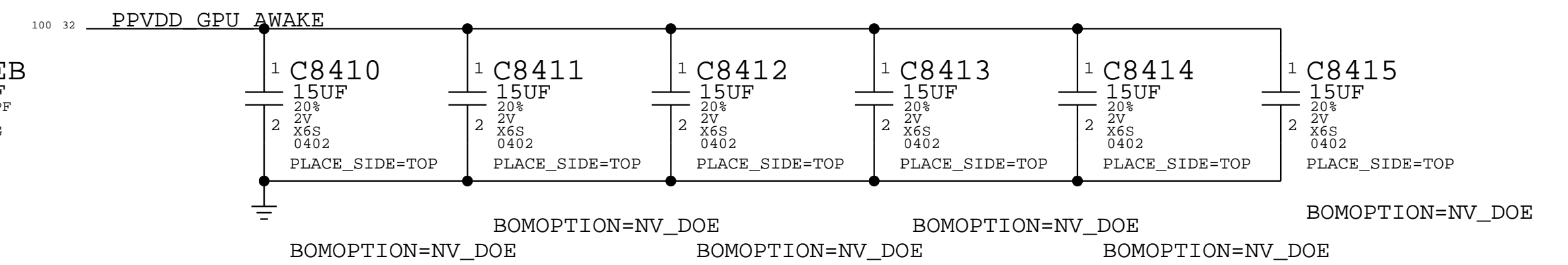
MASTER PMU AMUX ALIAS



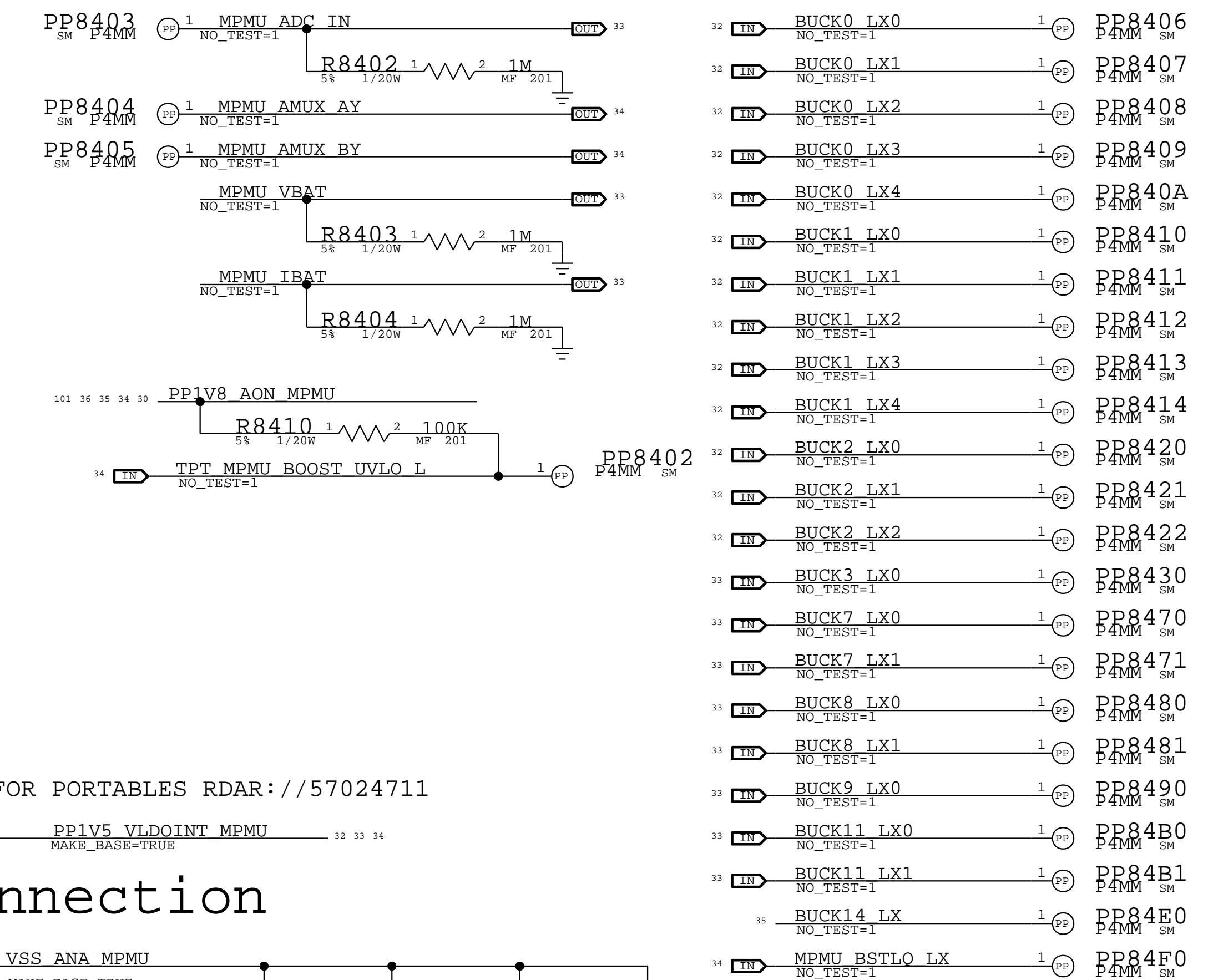
ADDITIONAL VDD_MAIN DECOUPLING CAPS



GPU RAIL N&V DOE CAPS



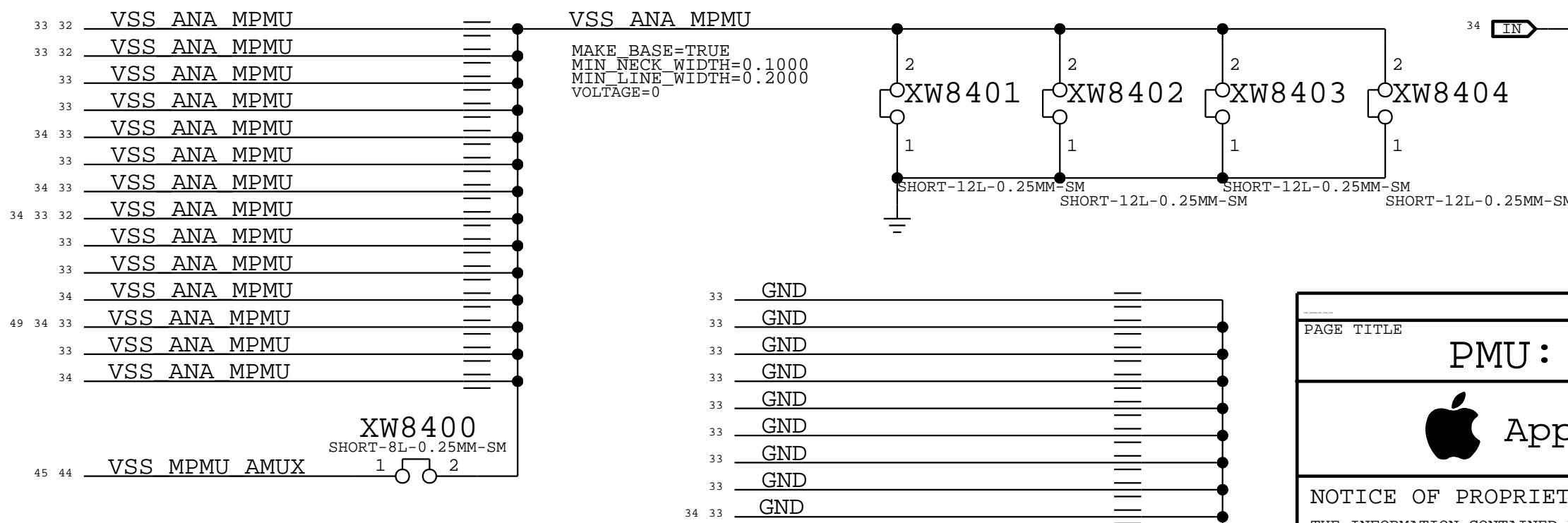
MASTER PMU PROBE POINTS



VLDORTC SHORTED TO VDD_ANA FOR PORTABLES RDAR://57024711

VSS alias connection

& WIDTH OF XW IS LAYOUT DEPENDENT



BOM_COST_GROUP=SOC POWER

PAGE TITLE		PMU: MASTER SUPPORT	
DRAWING NUMBER		051-05399	
REVISION		9.0.0	
BRANCH		dvt-1	
PAGE		84 OF 999	
SHEET		35 OF 117	

8

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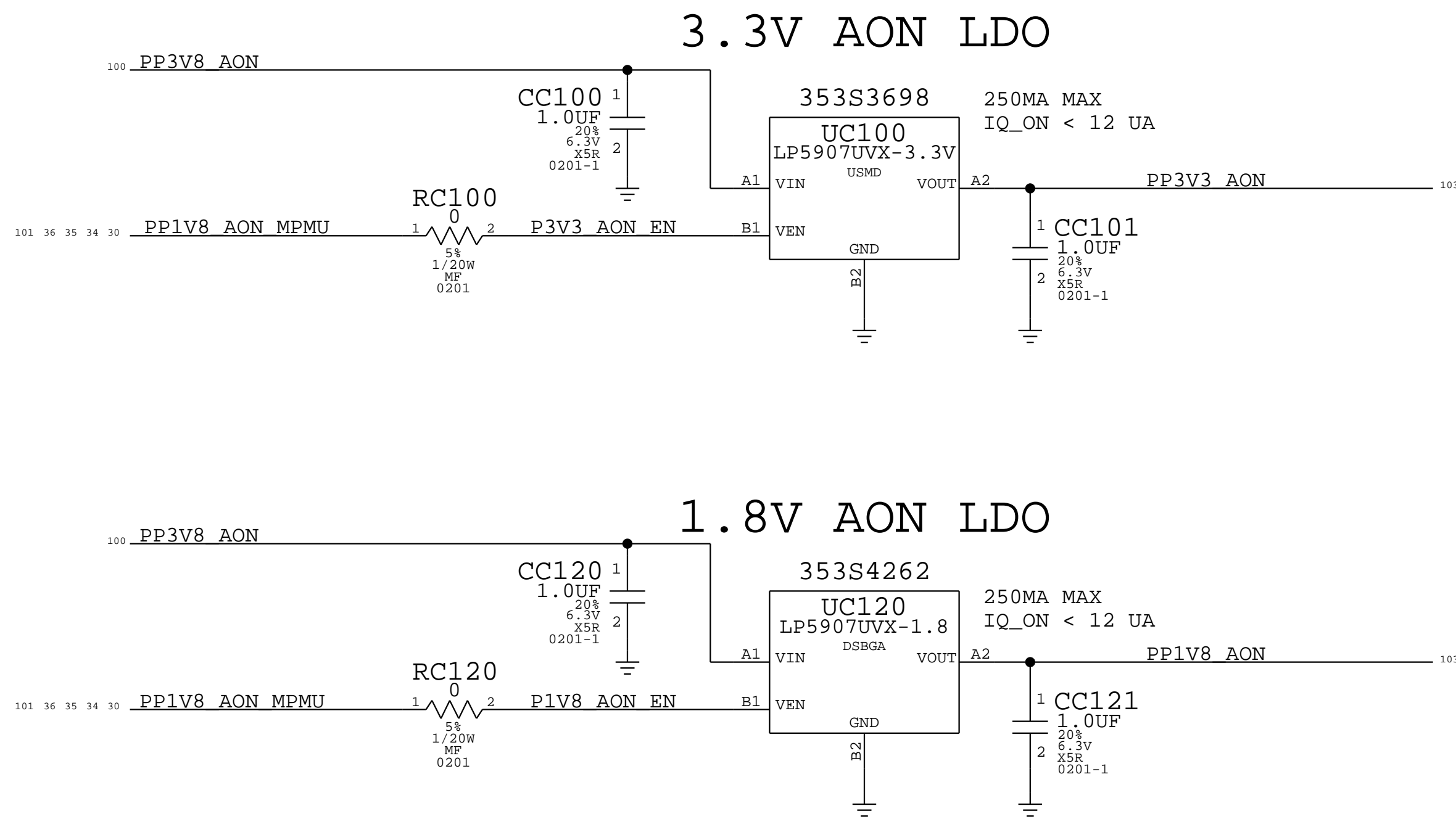
C

B

B

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A



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE		DRAWING NUMBER		SIZE
POWER: EXTERNAL LDO		051-05399		D
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		BRANCH	dvt-1	
		PAGE	121 OF 999	
		SHEET	36 OF 117	

8

7

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3

2

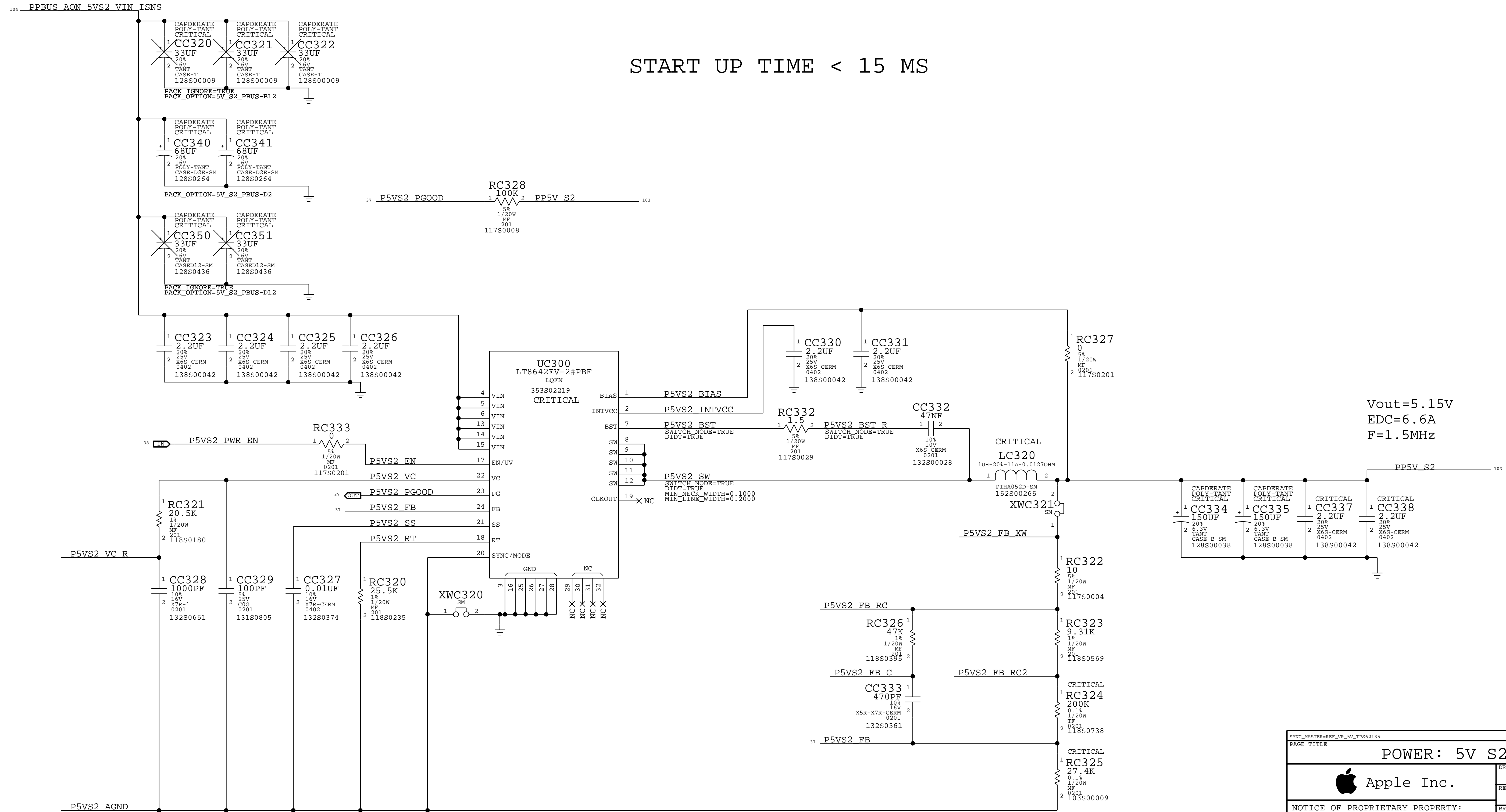
1

* OK2INTEGRATE *

5V_S2 Voltage Regulator

SET ONE OPTION FOR PBUS CAPS
PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12

START UP TIME < 15 MS

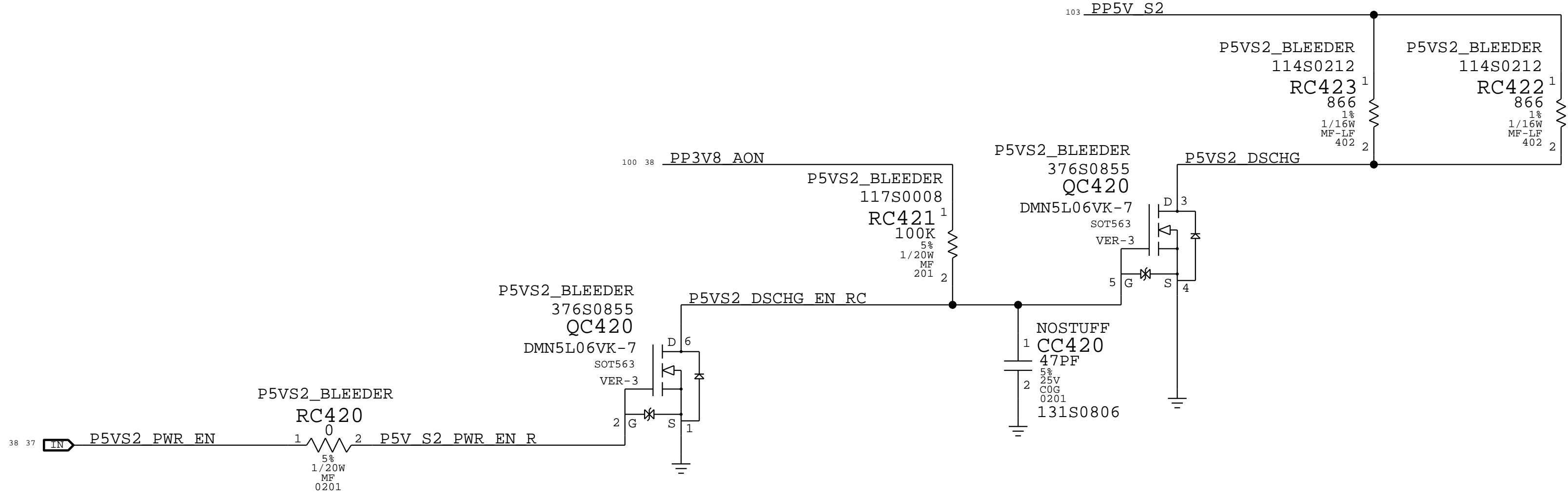


Vout=5.15V
EDC=6.6A
F=1.5MHz

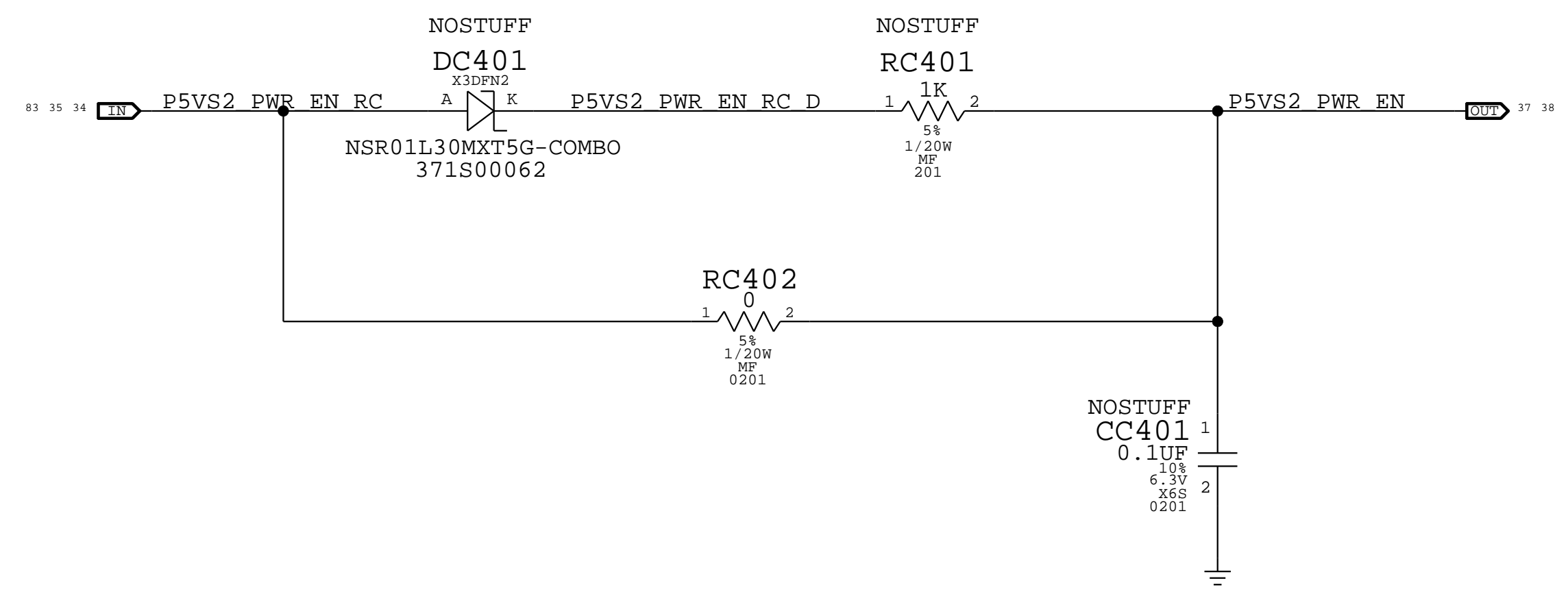
PAGE TITLE		POWER: 5V S2	
DRAWING NUMBER		051-05399	SIZE
REVISION		9.0.0	D
BRANCH		dvt-1	
PAGE		123 OF 999	
SHEET		37 OF 117	
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BOM_COST_GROUP=PLATFORM POWER

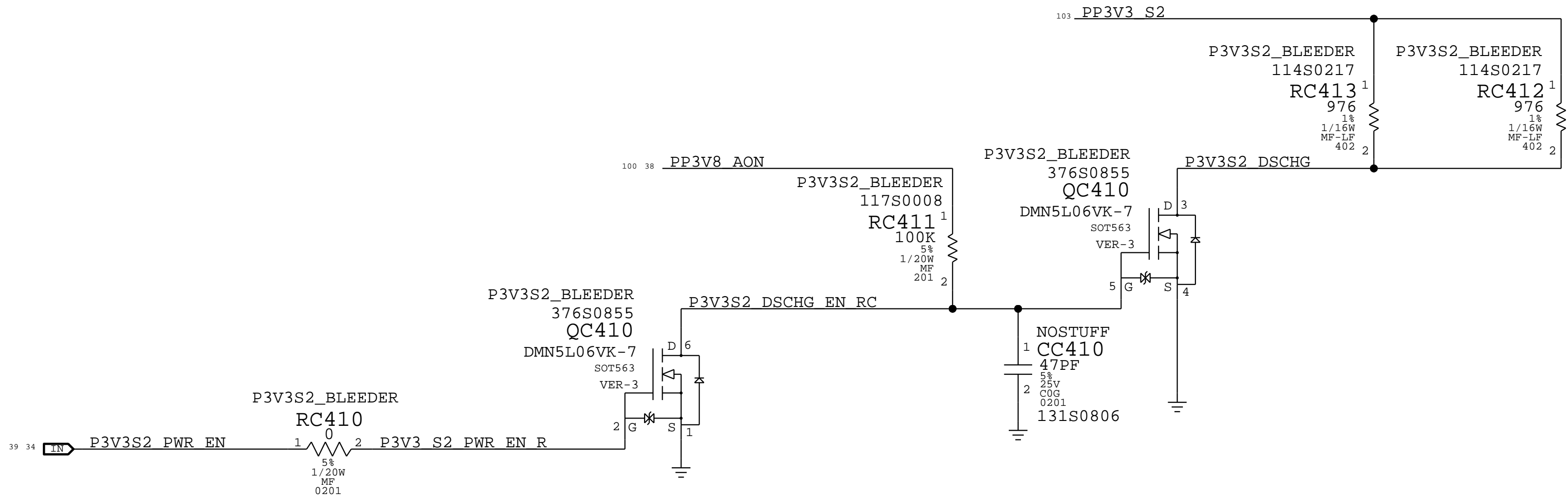
PP5V_S2 DISCHARGE CIRCUIT
<RDAR://62278898>



5VS2_EN TURN OFF DELAY 13-16MS
<RDAR://60892314>



PP3V3_S2 DISCHARGE CIRCUIT
<RDAR://62278916>



PAGE TITLE		DRAWING NUMBER		SIZE
POWER: 3V3 S2, 5V S2 SUPPORT		051-05399		D
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		BRANCH	dvt-1	
		PAGE	124 OF 999	
		SHEET	38 OF 117	

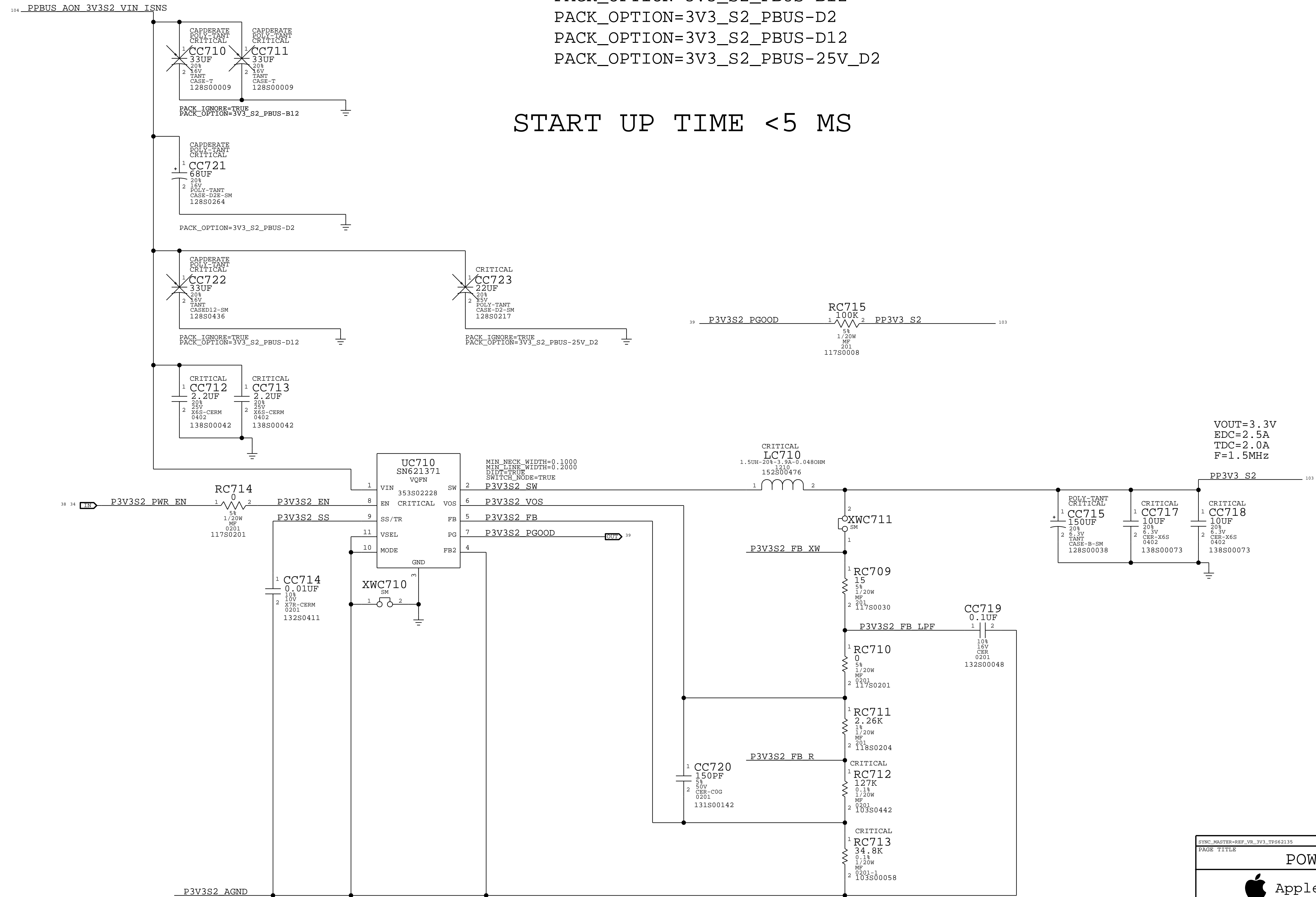
* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

- PACK_OPTION=3V3_S2_PBUS-B12
- PACK_OPTION=3V3_S2_PBUS-D2
- PACK_OPTION=3V3_S2_PBUS-D12
- PACK_OPTION=3V3_S2_PBUS-25V_D2

START UP TIME <5 MS



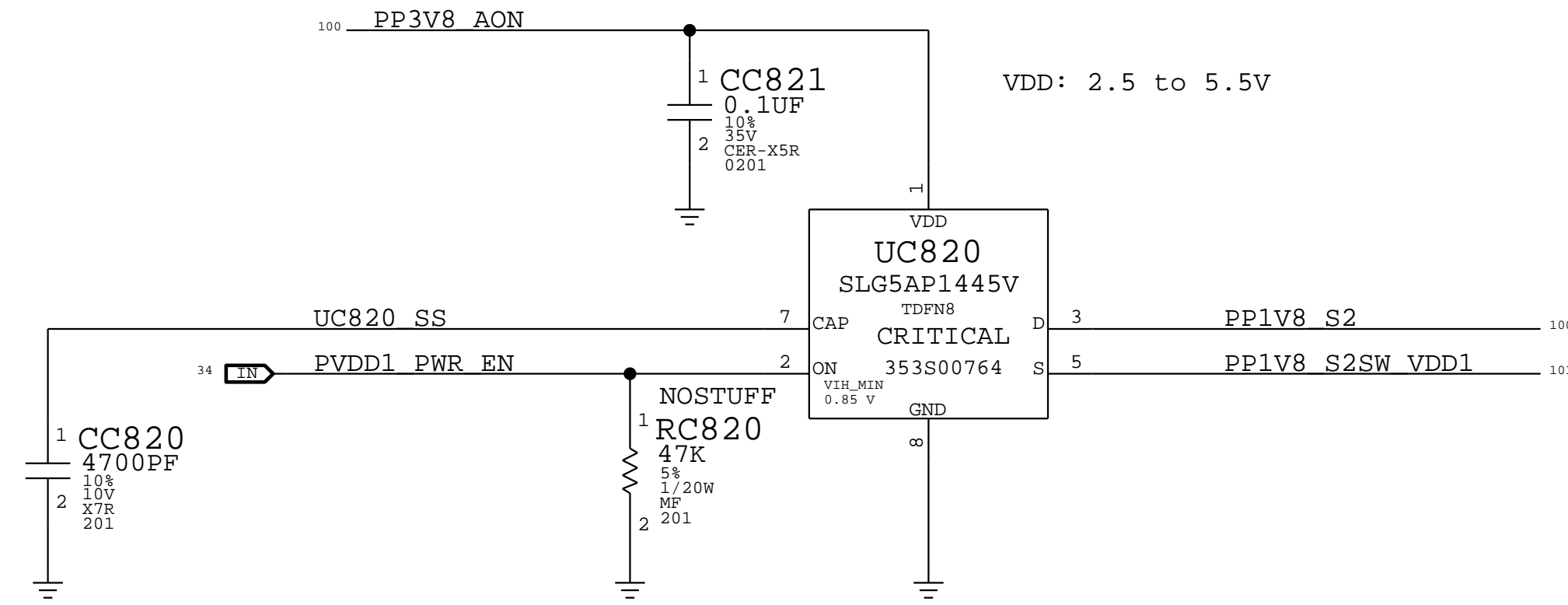
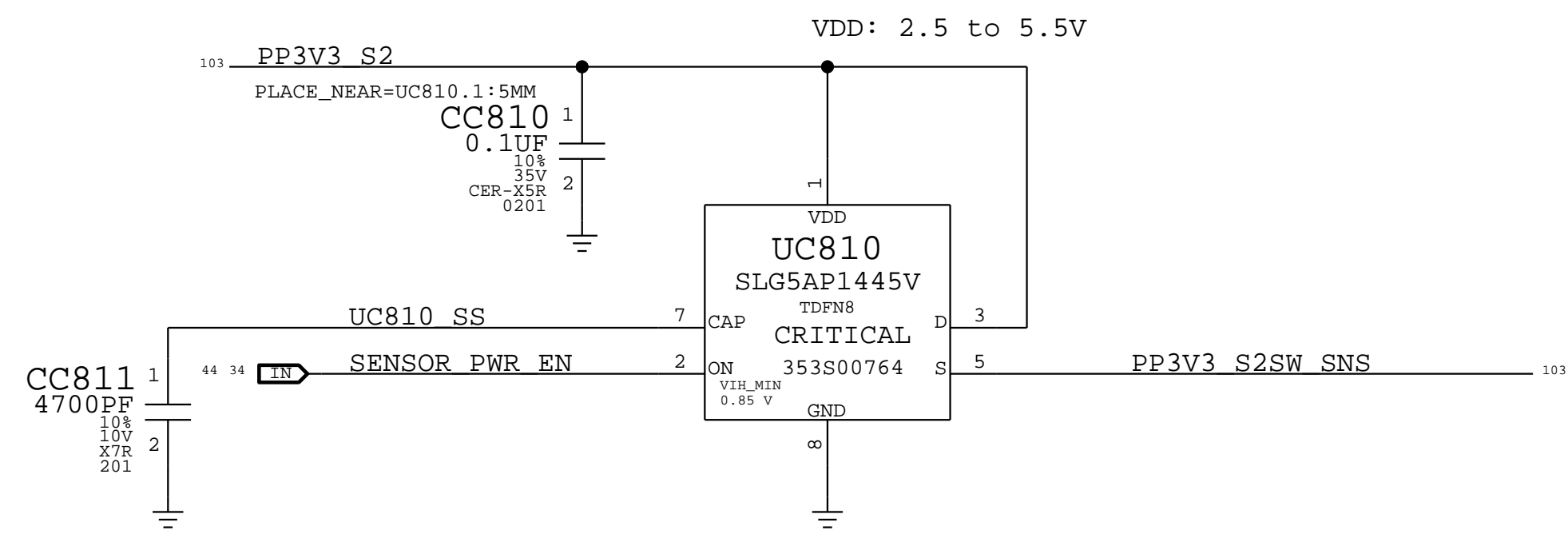
VOUT=3.3V
EDC=2.5A
TDC=2.0A
F=1.5MHZ

PAGE TITLE		POWER: 3V3 S2	
DRAWING NUMBER		051-05399	SIZE
REVISION		9.0.0	D
BRANCH		dvt-1	
PAGE		127 OF 999	
SHEET		39 OF 117	

BOM_COST_GROUP=PLATFORM POWER

3.3V SENSOR SWITCH

1V8_S2 SWITCH (FROM J213 1V8 G3S)

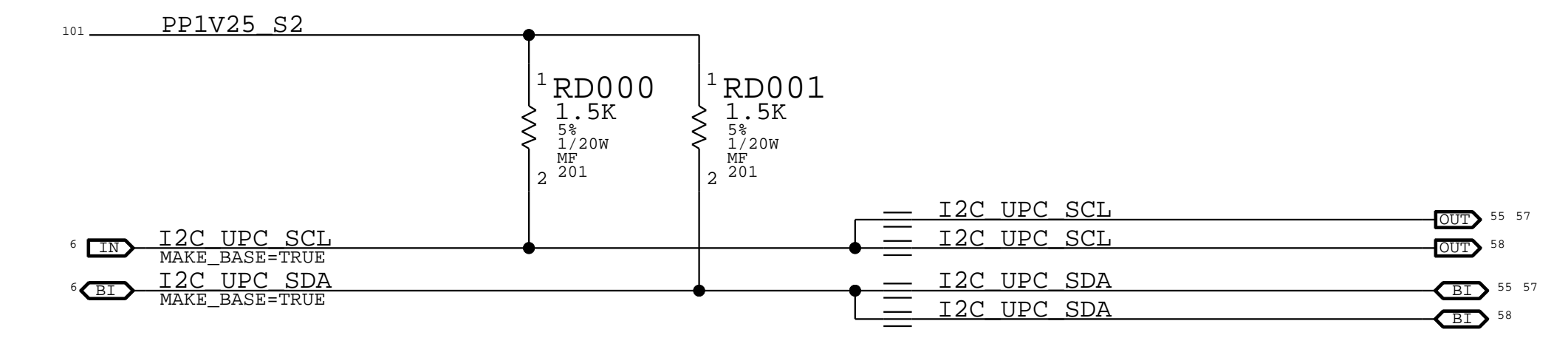


PAGE TITLE		POWER: FETS	
Apple Inc.	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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	PAGE	128 OF 999	
	SHEET	40 OF 117	

BOM_COST_GROUP=PLATFORM POWER

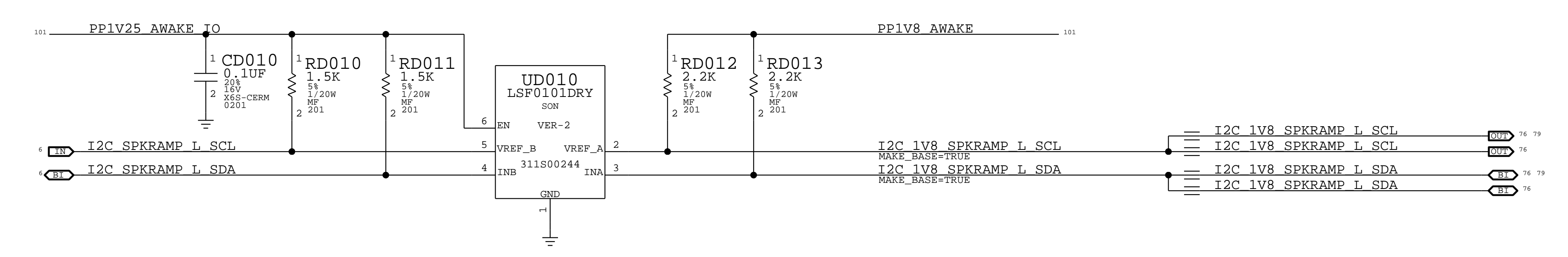
D

SIO I2C0
 DIAGS BUS: 0
 DEVICE 7-BIT
 ACE 0 0X38
 ACE 1 0X3F



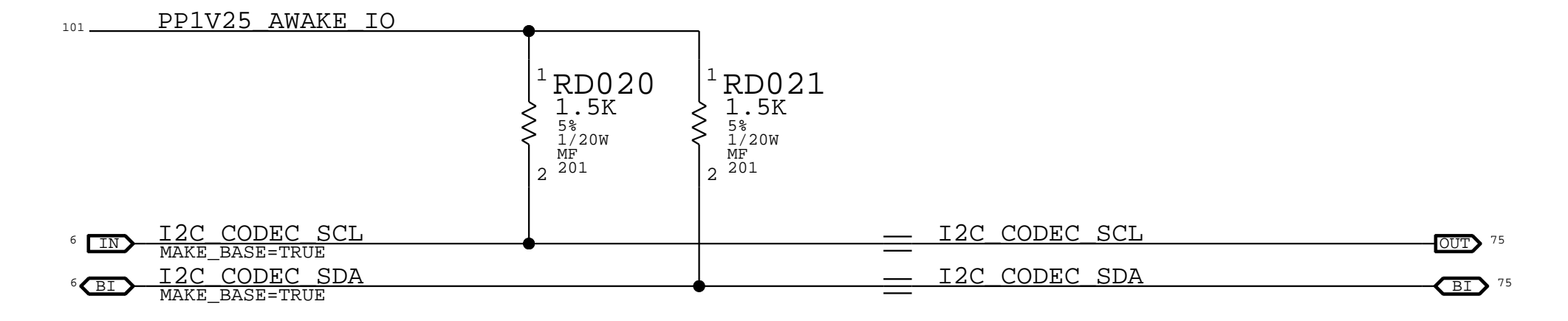
C

SIO I2C1
 DIAGS BUS: 1
 DEVICE 7-BIT
 SPKRAMP L (A) 0X31
 SPKRAMP L (B) 0X32



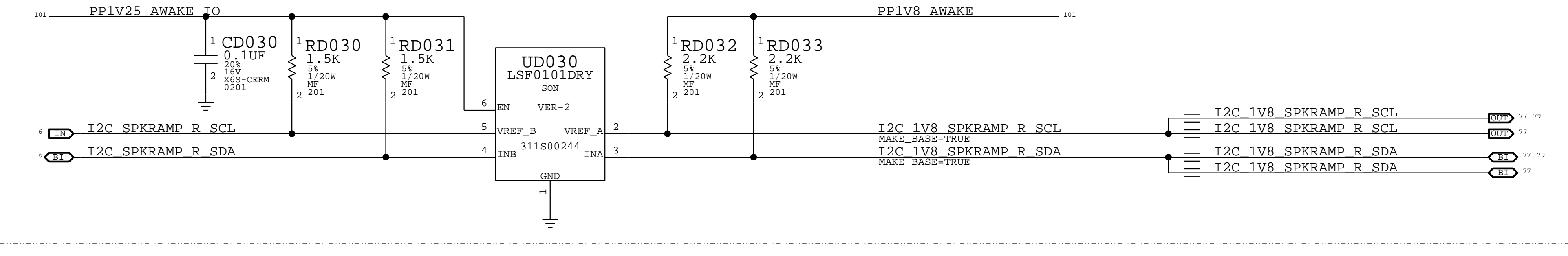
B

SIO I2C2
 DIAGS BUS: 2
 DEVICE 7-BIT
 CS42L83A 0X48

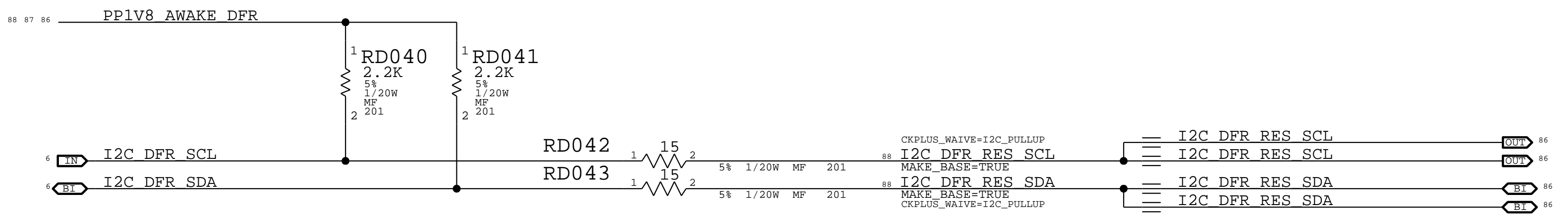


A

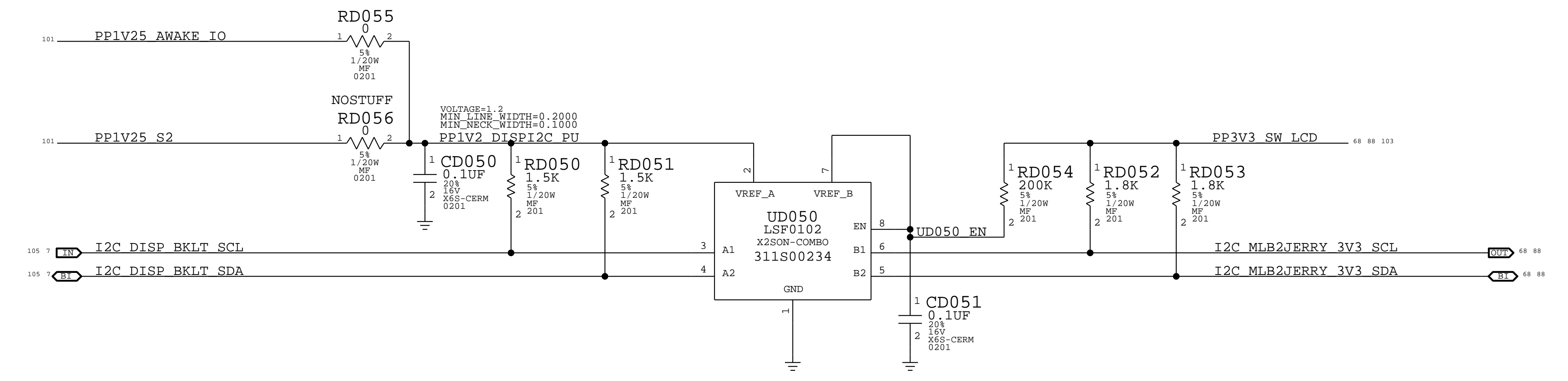
SIO I2C3
 DIAGS BUS: 3
 DEVICE 7-BIT
 SPKRAMP R (D) 0X34
 SPKRAMP R (E) 0X35



SIO I2C4
 DIAGS BUS: 4
 DEVICE 7-BIT
 DFR DISPLAY 0X--
 DFR TOUCH 0X--



DISP I2C
 DIAGS BUS: 12
 DEVICE 7-BIT
 JERRY 0X--



BOM_COST_GROUP=SMC

SYNC_MASTER=T668_MLB		SYNC_DATE=06/20/2019	
PAGE TITLE			
I2C: SIO, DISP			
		DRAWING NUMBER	051-05399
		REVISION	9.0.0
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		PAGE	130 OF 999
		SHEET	41 OF 117

ISP I2C0

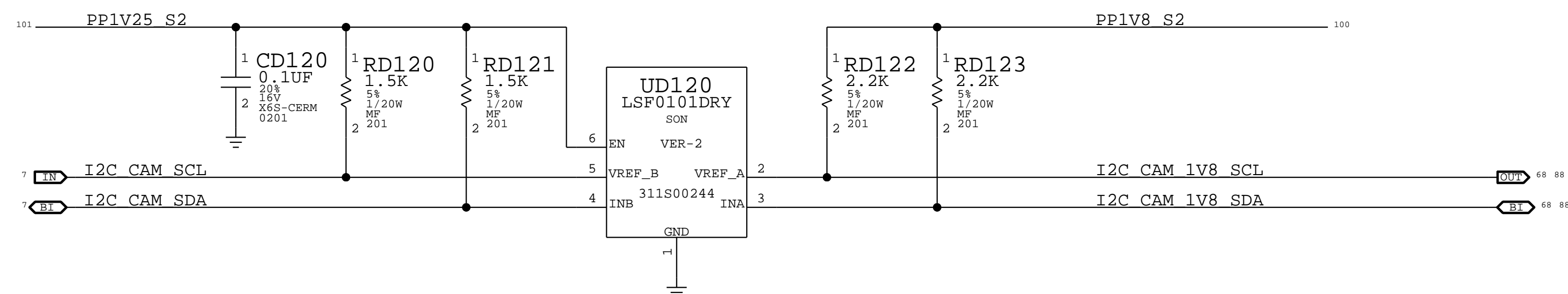
UNUSED

ISP I2C1

UNUSED

ISP I2C2

DIAGS BUS: TBD
DEVICE 7-BIT
CAMERA PMU 0X--
CAMERA SENSOR 0X--

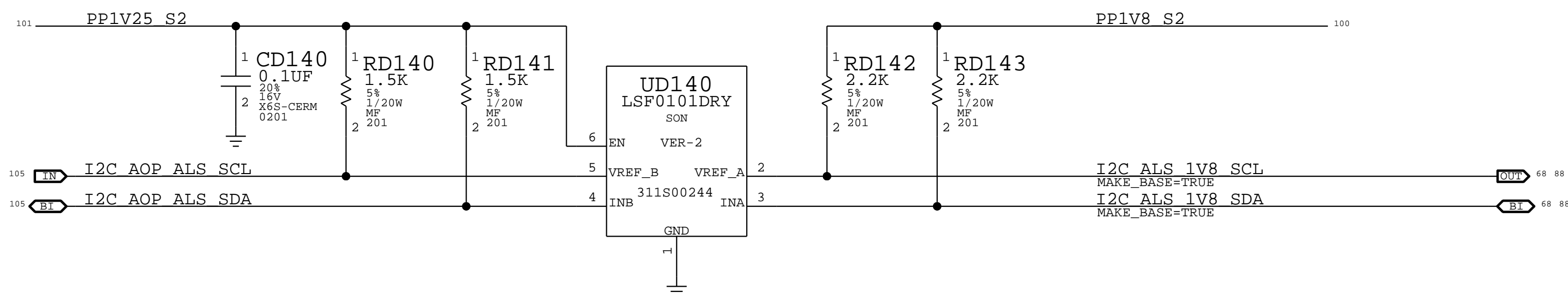


ISP I2C3

UNUSED

AOP I2C0

DIAGS BUS: 5
DEVICE 7-BIT
ALS CT720SW 0X29



AOP I2C1

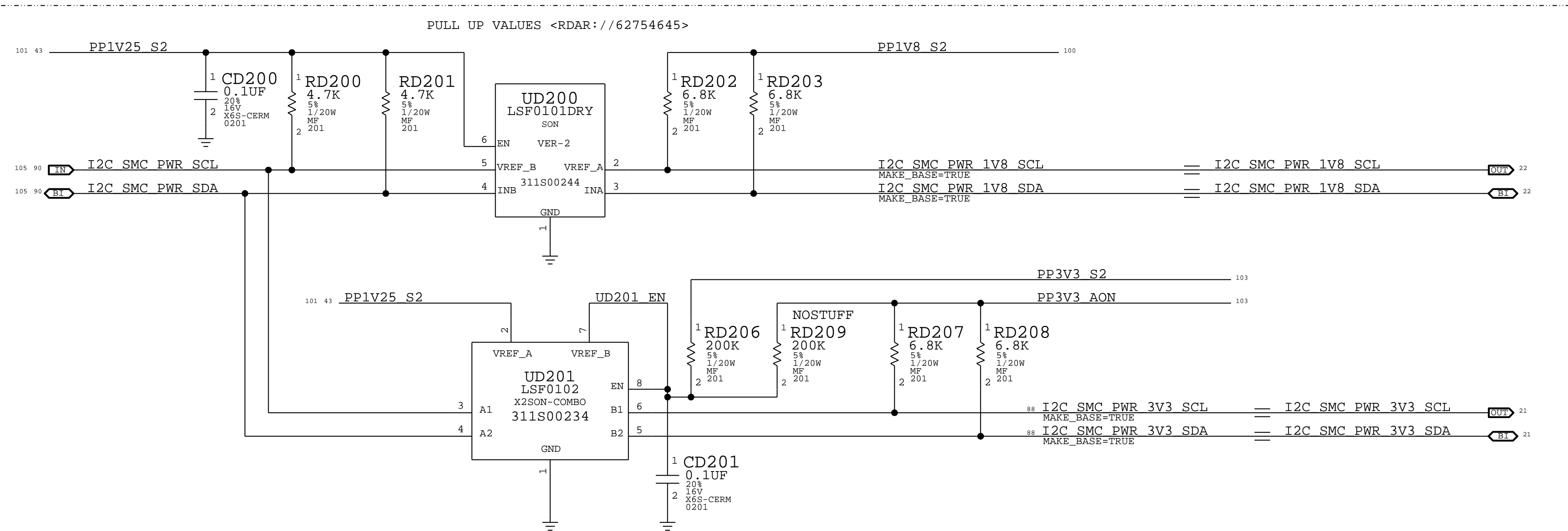
UNUSED

PAGE TITLE		I2C: ISP, AOP	
Apple Inc.	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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		PAGE	131 OF 999
		SHEET	42 OF 117

D

D

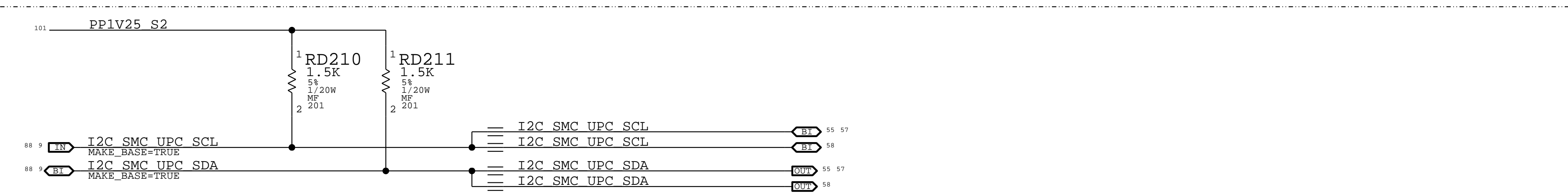
SMC I2CM0
 DIAGS BUS: 7
 DEVICE 7-BIT
 CHGR ISL9240HI 0X9
 EMU BQ40Z651 0XB



C

C

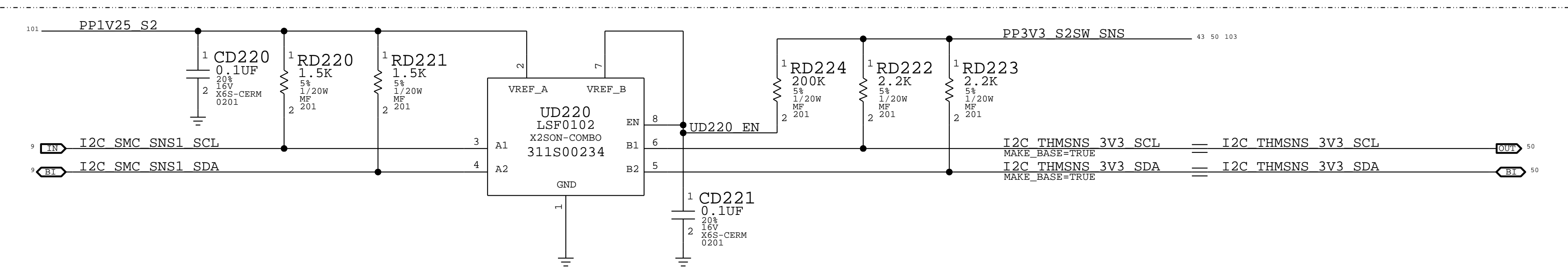
SMC I2CM1
 DIAGS BUS: 8
 DEVICE 7-BIT
 ACE 0 0X38
 ACE 1 0X3F



B

B

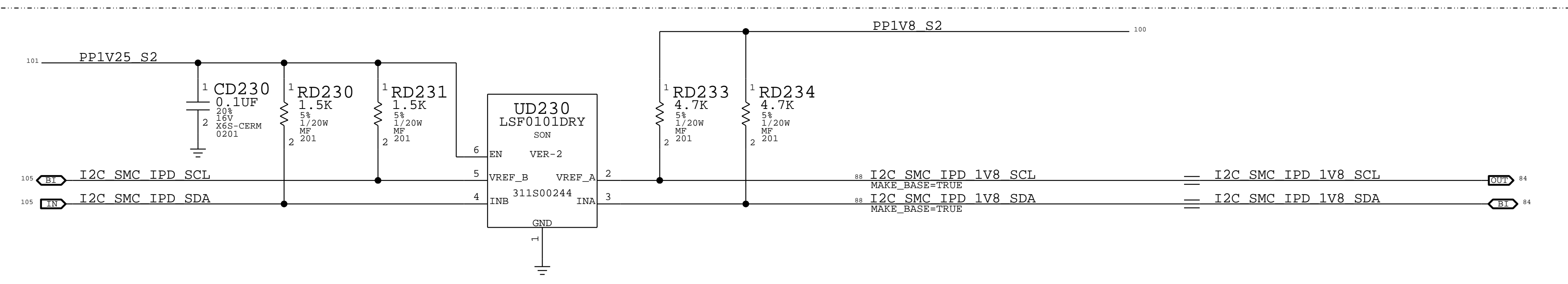
SMC I2CM2
 DIAGS BUS: 9
 DEVICE 7-BIT
 TMP464 0X48



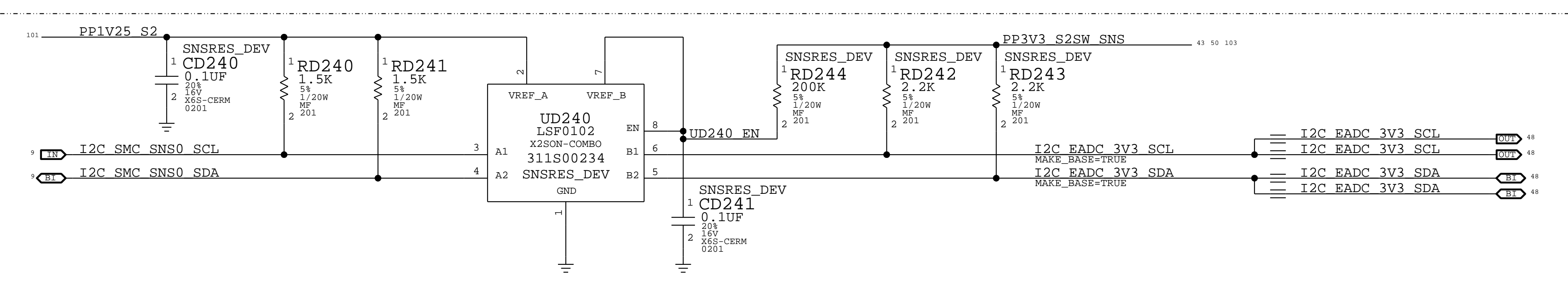
A

A

SMC I2CM3
 DIAGS BUS: 10
 DEVICE 7-BIT
 PALM TMP461 0X4C



SMC I2CM4
 DIAGS BUS: 11
 DEVICE 7-BIT
 TLA2528 EADC1 0X17
 TLA2528 EADC2 0X10

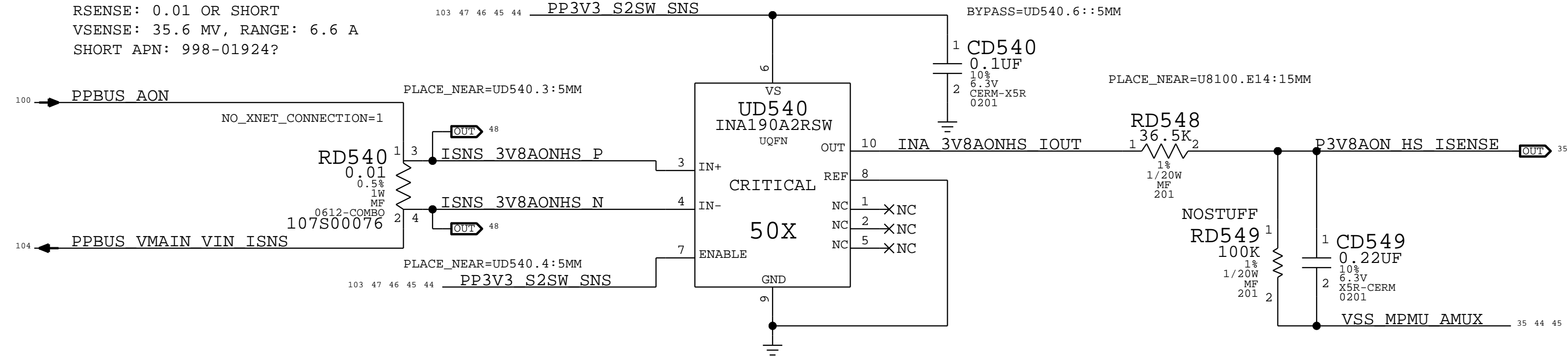


BOM_COST_GROUP=SMC

PAGE TITLE		I2C: SMC	
DRAWING NUMBER		051-05399	SIZE D
REVISION		9.0.0	
BRANCH		dvt-1	
PAGE		132 OF 999	
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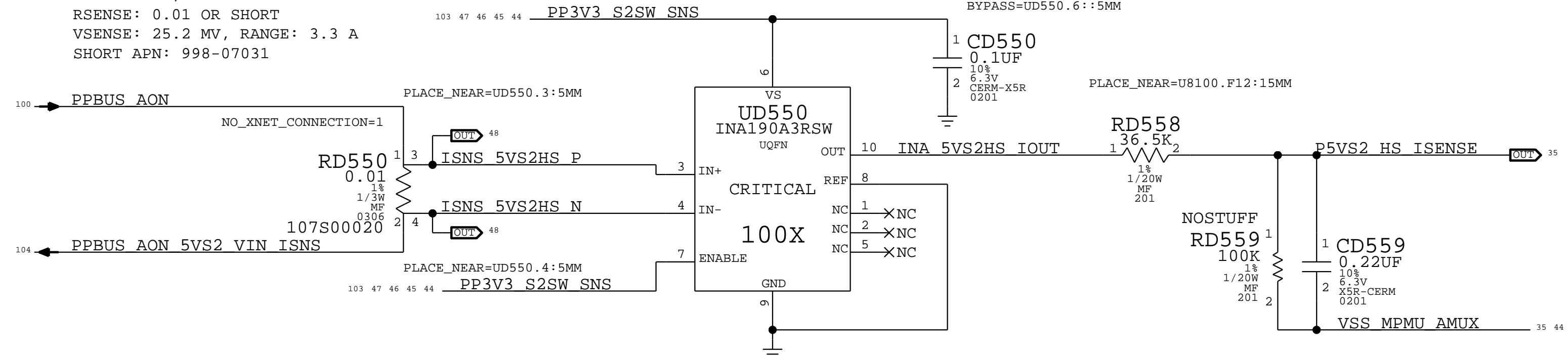
P3V8 AON HIGH SIDE CURRENT SENSE (IMVR)

GAIN: 50X, TDP: 3.55 A
 RSENSE: 0.01 OR SHORT
 VSENSE: 35.6 MV, RANGE: 6.6 A
 SHORT APN: 998-019247



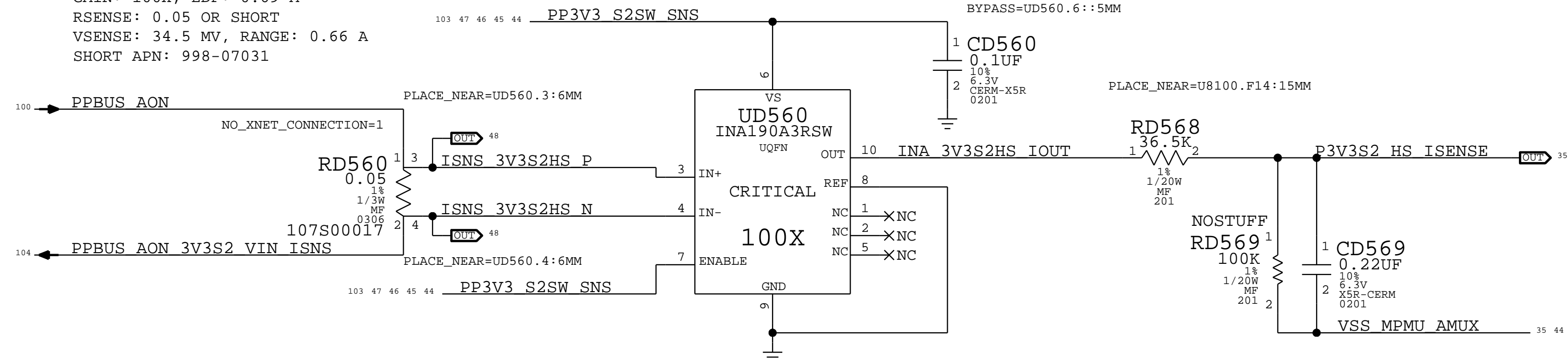
5V S2 VR HIGH SIDE CURRENT SENSE (IO5R)

GAIN: 100X, EDP: 2.52 A
 RSENSE: 0.01 OR SHORT
 VSENSE: 25.2 MV, RANGE: 3.3 A
 SHORT APN: 998-07031



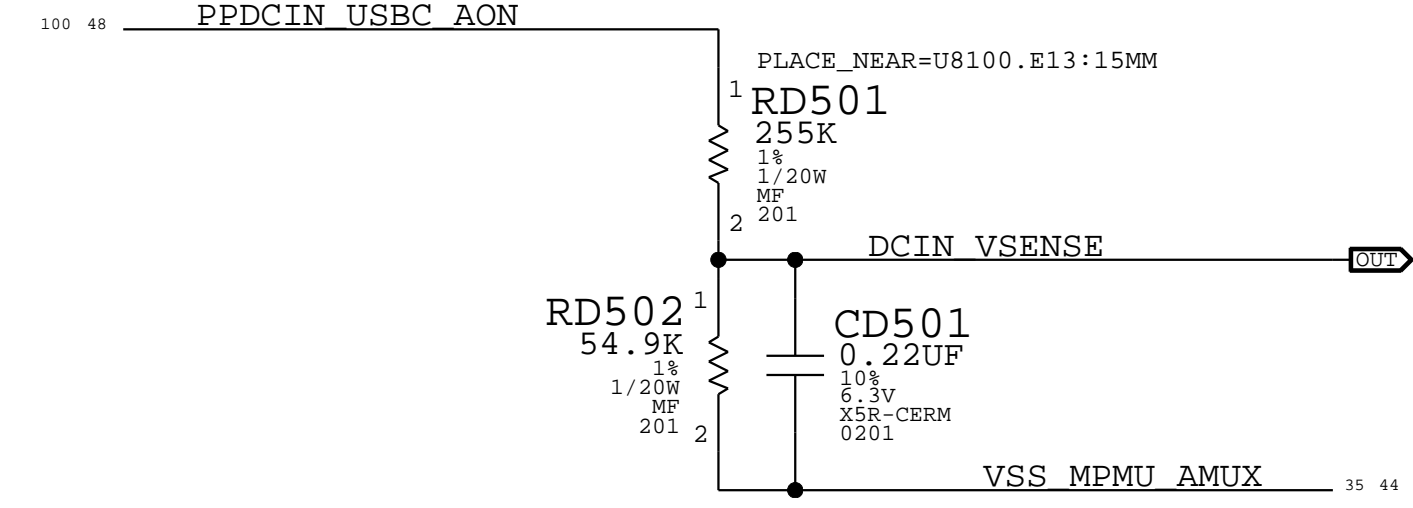
3V3 S2 VR HIGH SIDE CURRENT SENSE (IO3R)

GAIN: 100X, EDP: 0.69 A
 RSENSE: 0.05 OR SHORT
 VSENSE: 34.5 MV, RANGE: 0.66 A
 SHORT APN: 998-07031

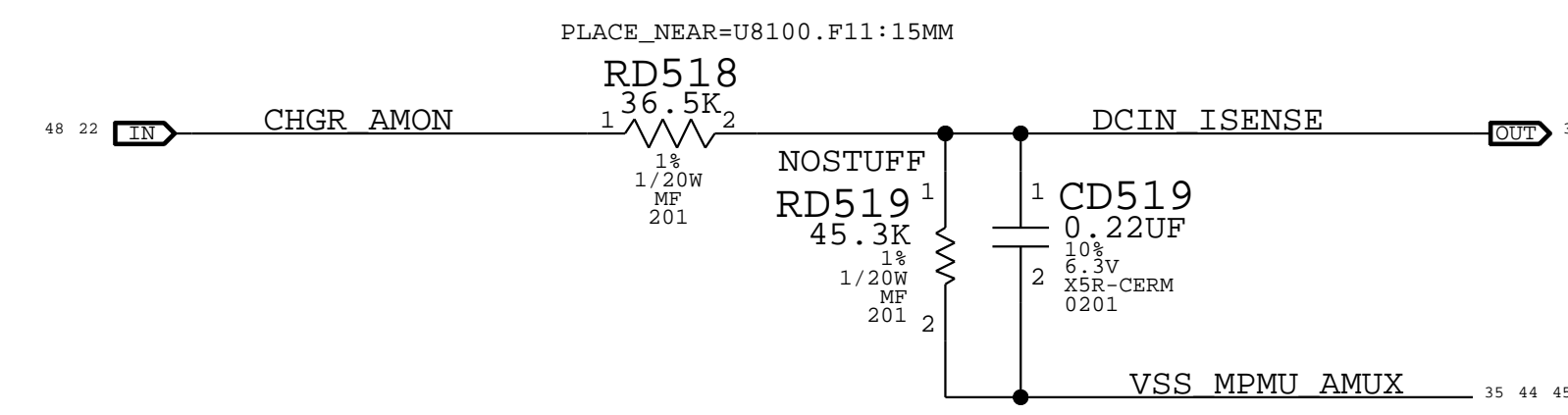


DCIN VOLTAGE SENSE (VDOR)

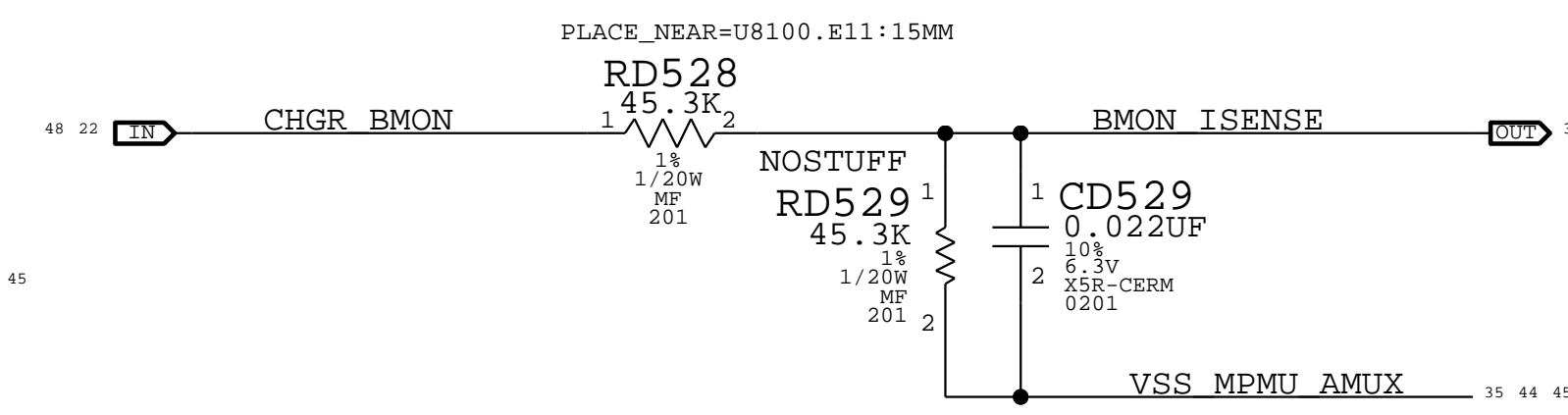
PMU AMUX inputs are not fail safe but RD501 limits the current rdar://60591705



DCIN CURRENT SENSE [AMON] (IDOR)

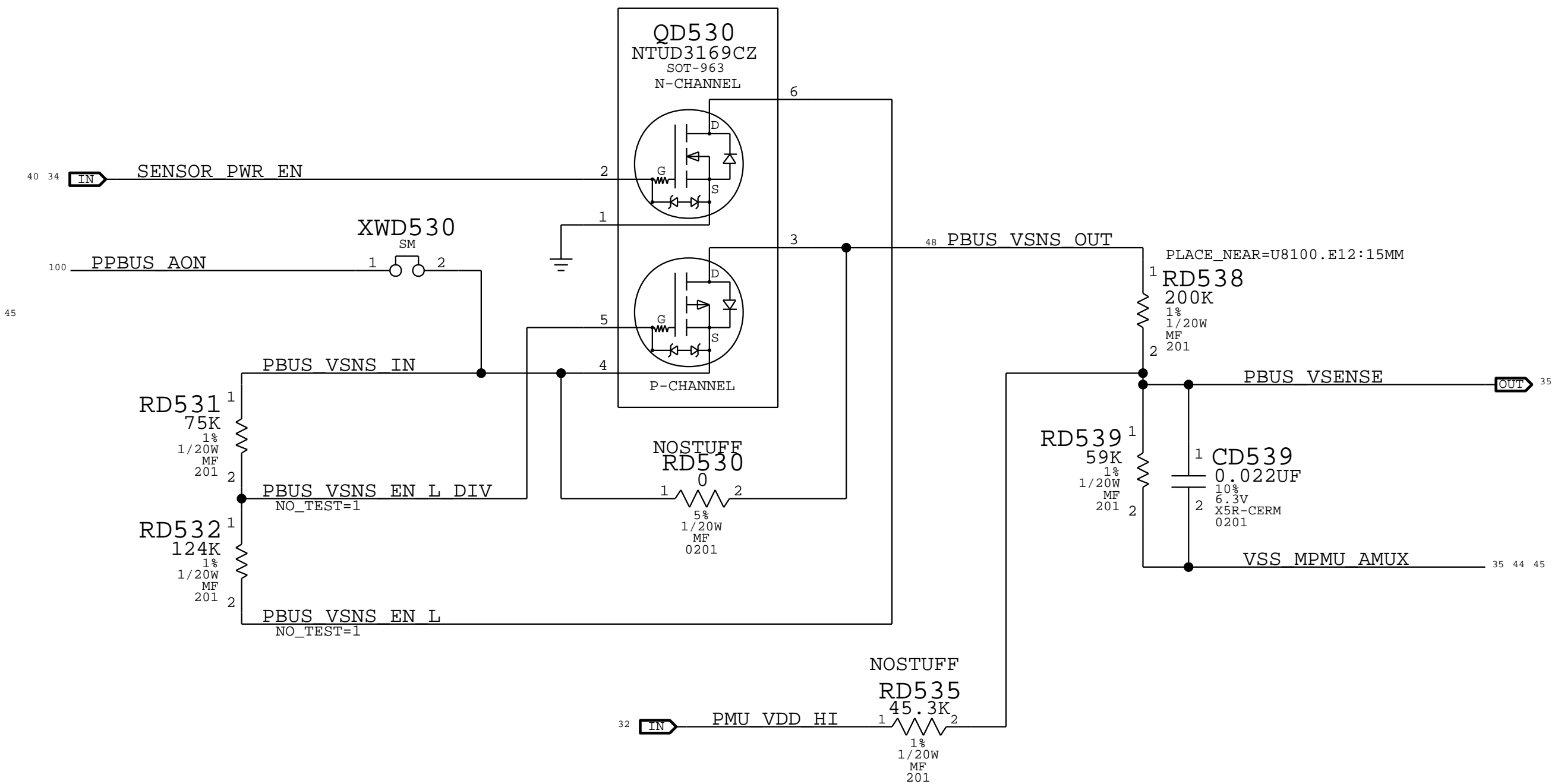


BATTERY CHARGER CURRENT SENSE [BMON] (IPBR)



PBUS VOLTAGE SENSE (VPOR)

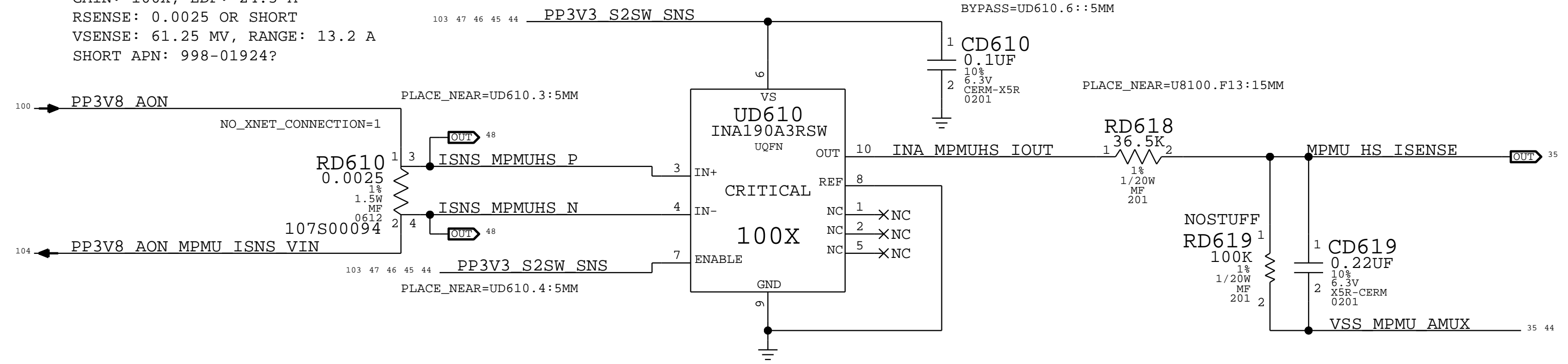
RD531/RD532 updated per rdar://60591705



PAGE TITLE		
SENSORS: POWER HIGH SIDE (1/2)		
	DRAWING NUMBER	051-05399
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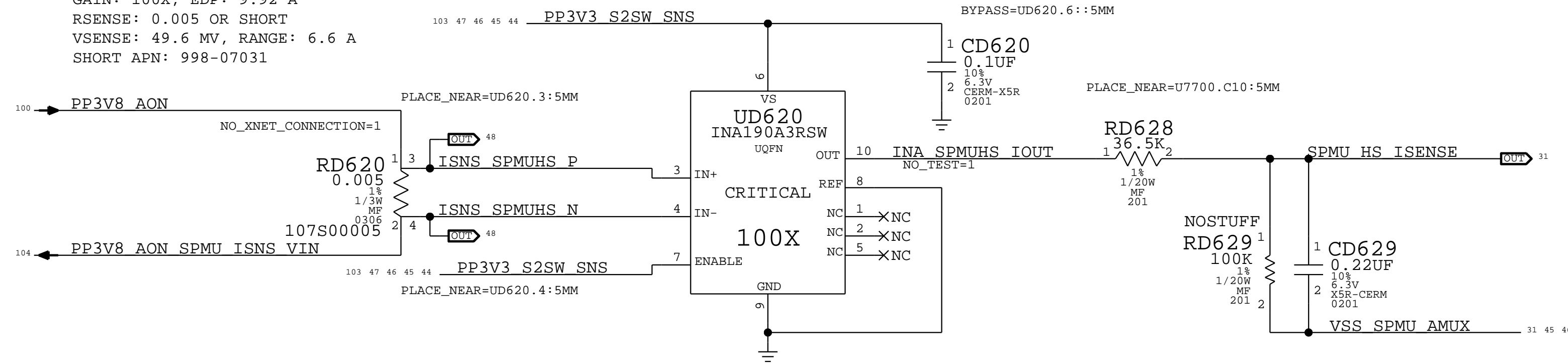
MASTER PMU HIGH SIDE CURRENT SENSE (IPMR)

GAIN: 100X, EDP: 24.5 A
 RSENSE: 0.0025 OR SHORT
 VSENSE: 61.25 MV, RANGE: 13.2 A
 SHORT APN: 998-019247



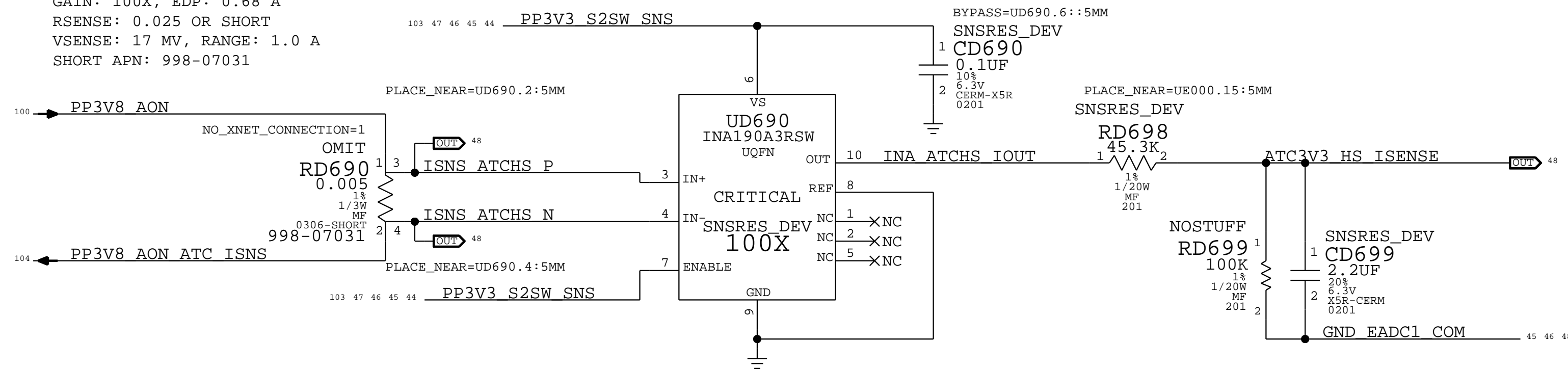
SLAVE PMU HIGH SIDE CURRENT SENSE (IPSR)

GAIN: 100X, EDP: 9.92 A
 RSENSE: 0.005 OR SHORT
 VSENSE: 49.6 MV, RANGE: 6.6 A
 SHORT APN: 998-07031



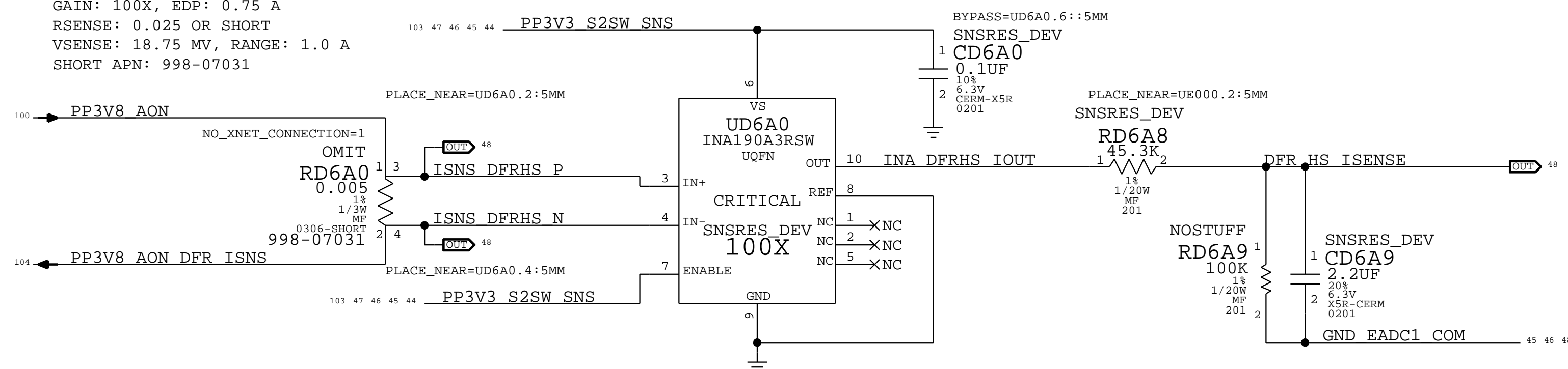
ATC 3V3 LDO HIGH SIDE CURRENT SENSE (IULR)

GAIN: 100X, EDP: 0.68 A
 RSENSE: 0.025 OR SHORT
 VSENSE: 17 MV, RANGE: 1.0 A
 SHORT APN: 998-07031

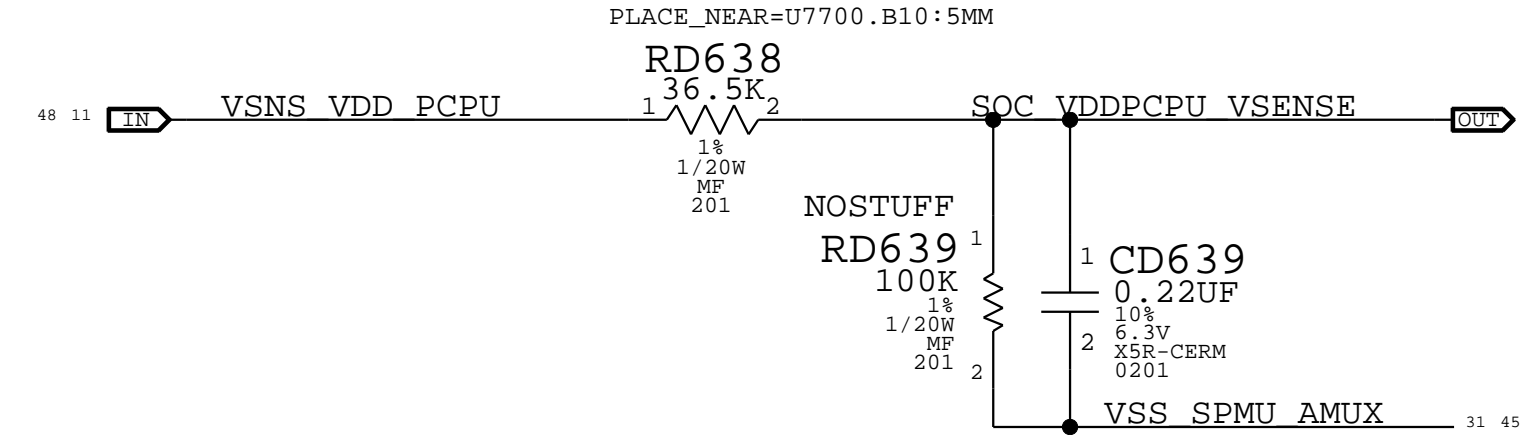


DFR 1.8/3.3V HIGH SIDE CURRENT SENSE (IFDC)

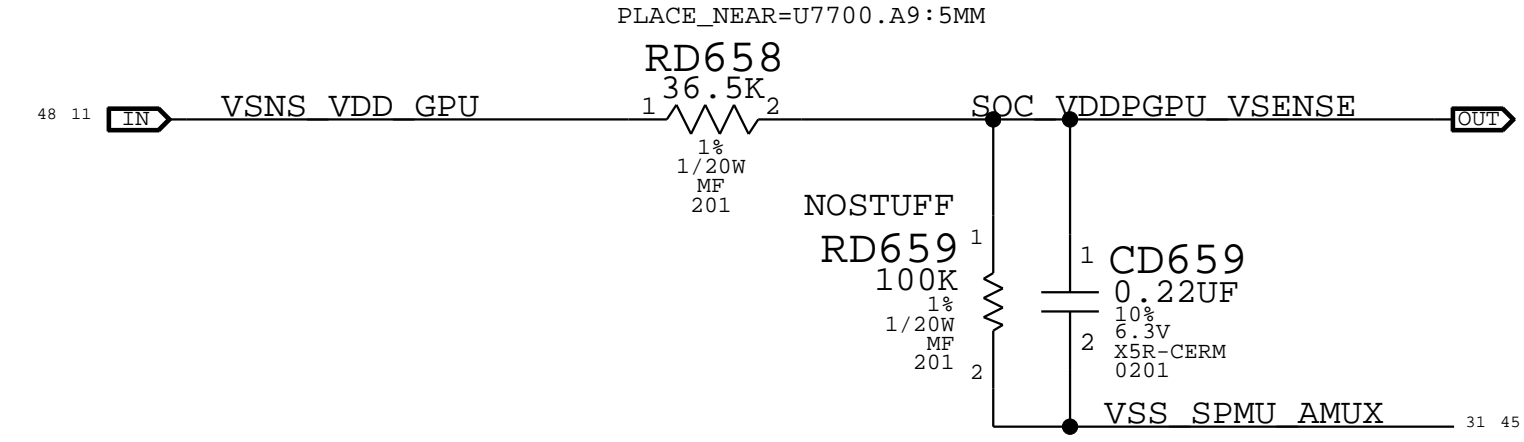
GAIN: 100X, EDP: 0.75 A
 RSENSE: 0.025 OR SHORT
 VSENSE: 18.75 MV, RANGE: 1.0 A
 SHORT APN: 998-07031



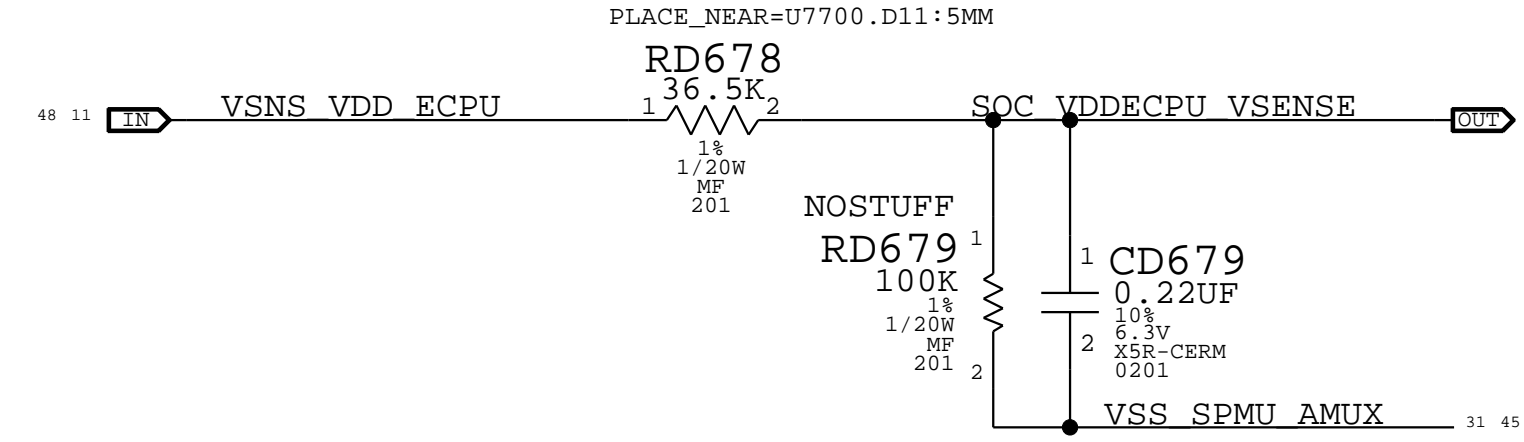
SOC VDD PCPU VSENSE (VCDP)



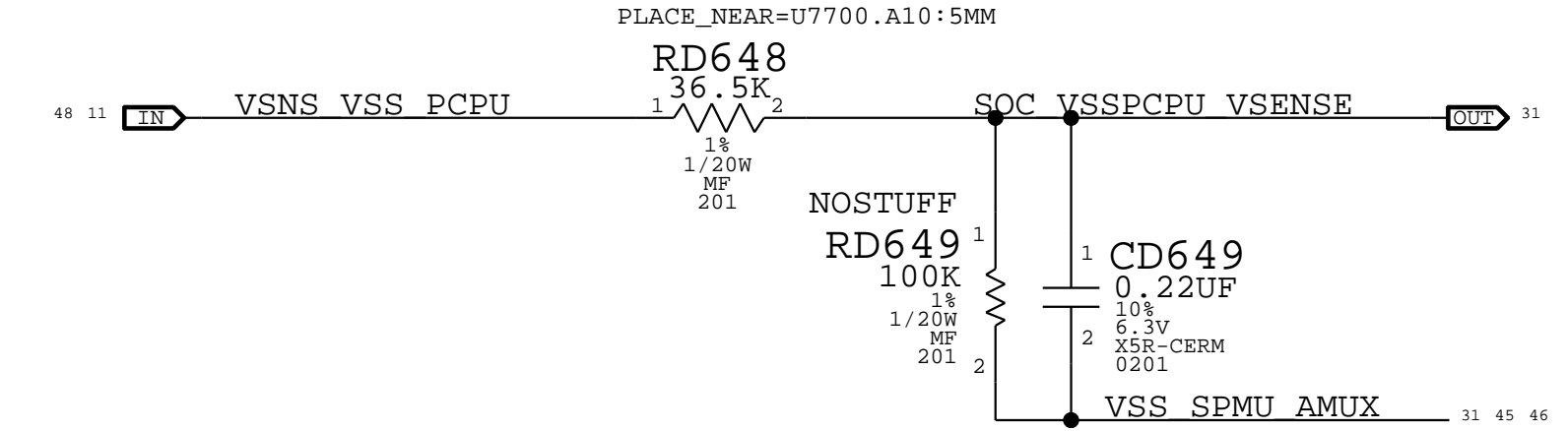
SOC VDD GPU VSENSE (VGDR)



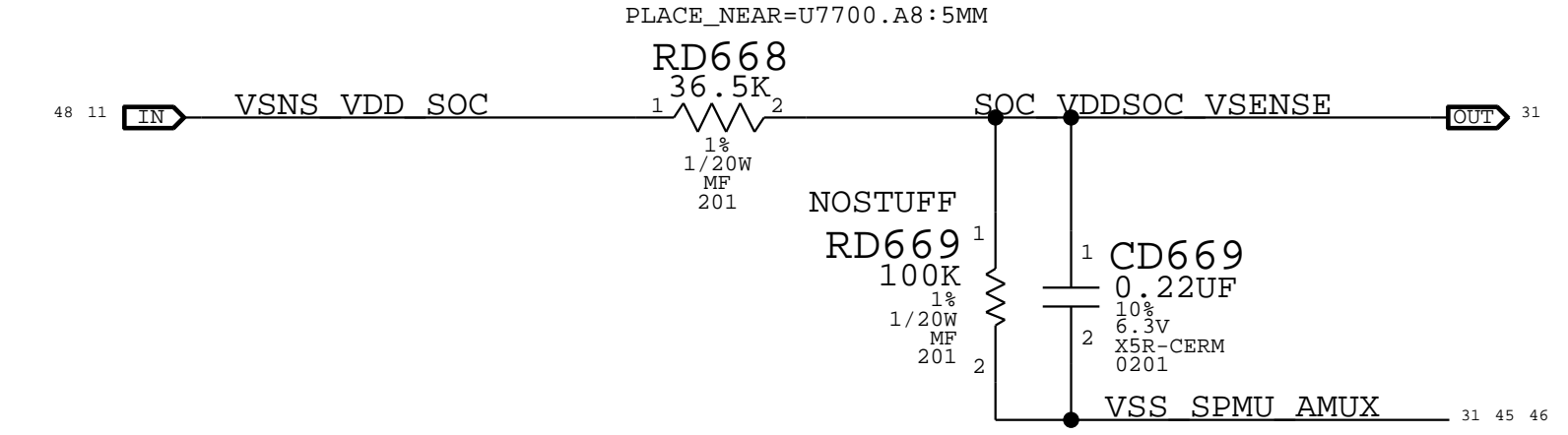
SOC VDD ECPU VSENSE (VCDE)



SOC VSS PCPU VSENSE (VCSP)

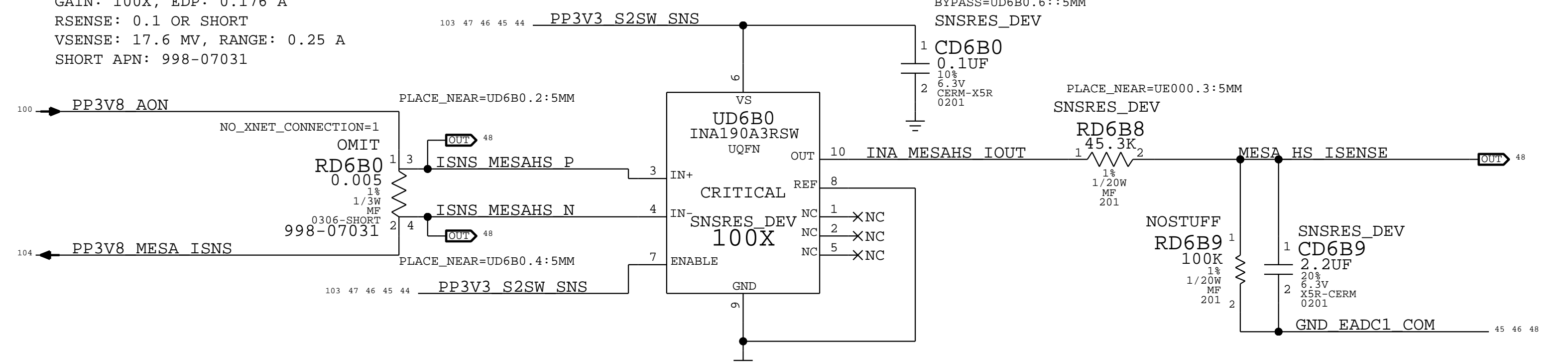


SOC VDD SOC VSENSE (VSDR)



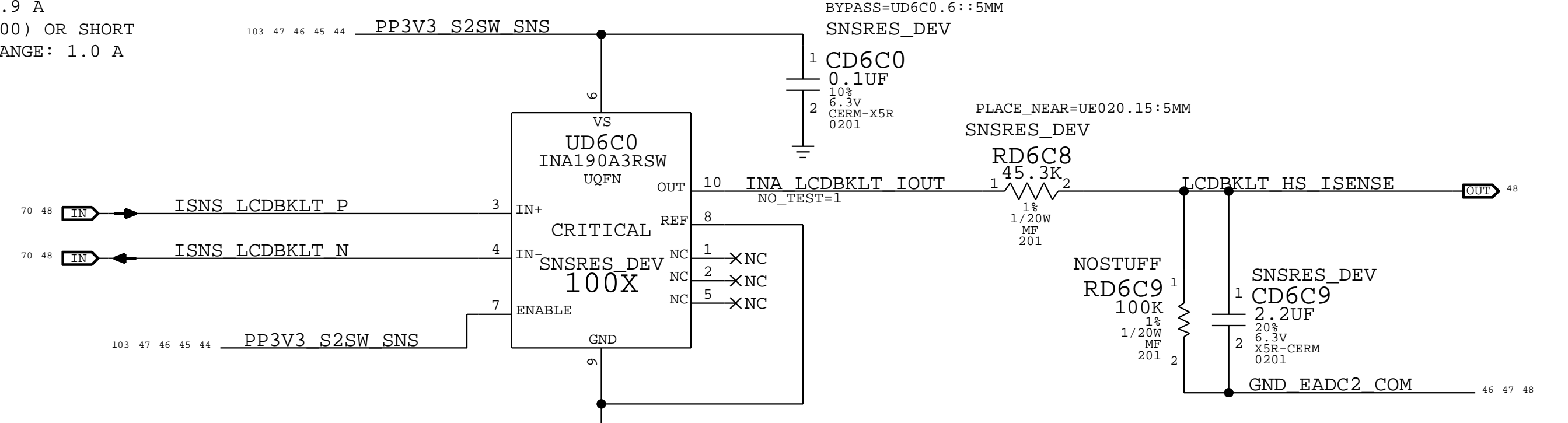
MESA 1.8/3.3/16V HIGH SIDE CURRENT SENSE (IIDR)

GAIN: 100X, EDP: 0.176 A
 RSENSE: 0.1 OR SHORT
 VSENSE: 17.6 MV, RANGE: 0.25 A
 SHORT APN: 998-07031



LCD BACKLIGHT HIGH SIDE CURRENT SENSE (IBLR)

GAIN: 100X, EDP: 0.9 A
 RSENSE: 0.025 (RP800) OR SHORT
 VSENSE: 22.6 MV, RANGE: 1.0 A

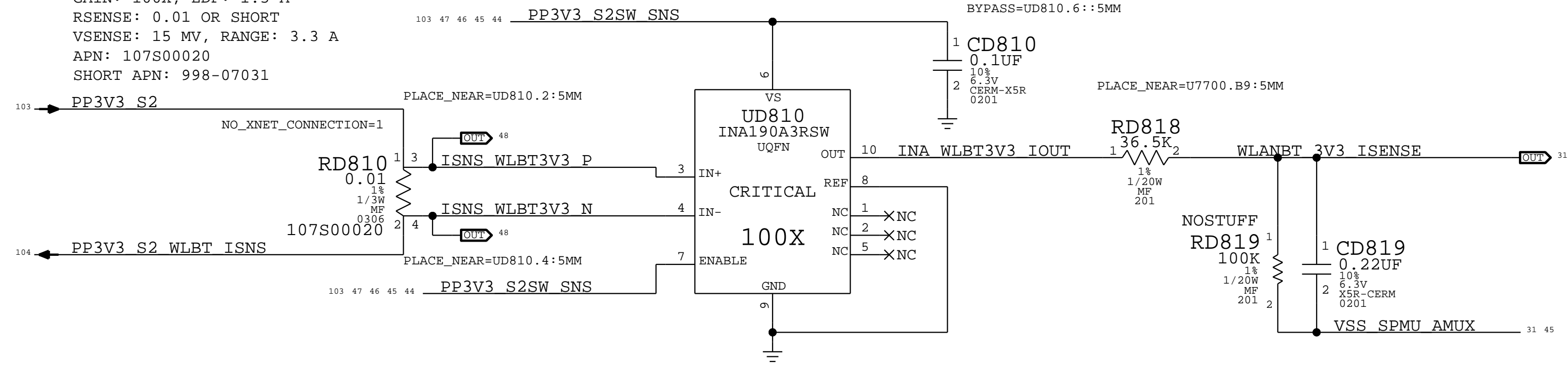


SENSORS: POWER HIGH SIDE (2/2)

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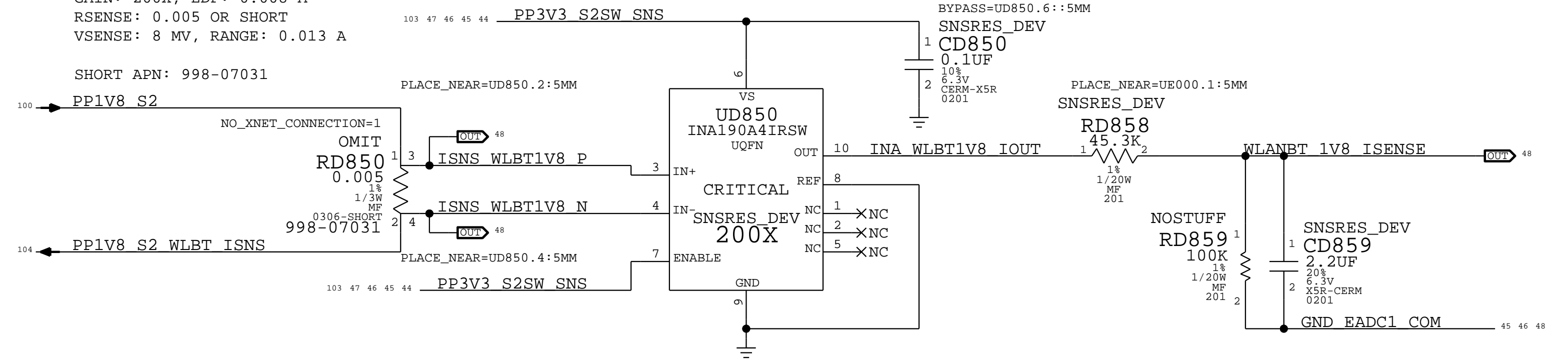
WLAN BT 3V3 S2 CURRENT SENSE (IW3C)

GAIN: 100X, EDP: 1.5 A
RSENSE: 0.01 OR SHORT
VSENSE: 15 MV, RANGE: 3.3 A
APN: 107S00020
SHORT APN: 998-07031



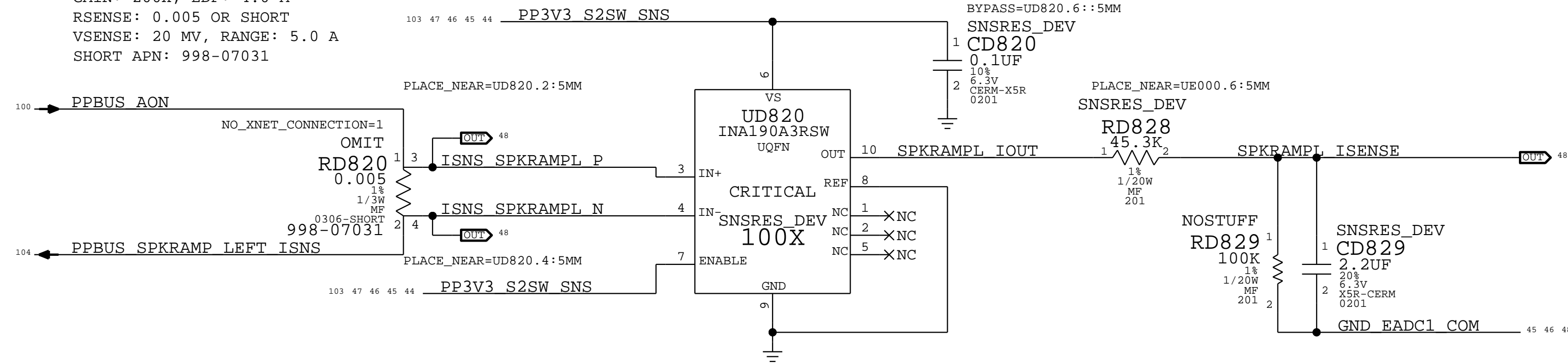
WLAN BT 1V8 S2 CURRENT SENSE (IW2C)

GAIN: 200X, EDP: 0.008 A
RSENSE: 0.005 OR SHORT
VSENSE: 8 MV, RANGE: 0.013 A
SHORT APN: 998-07031



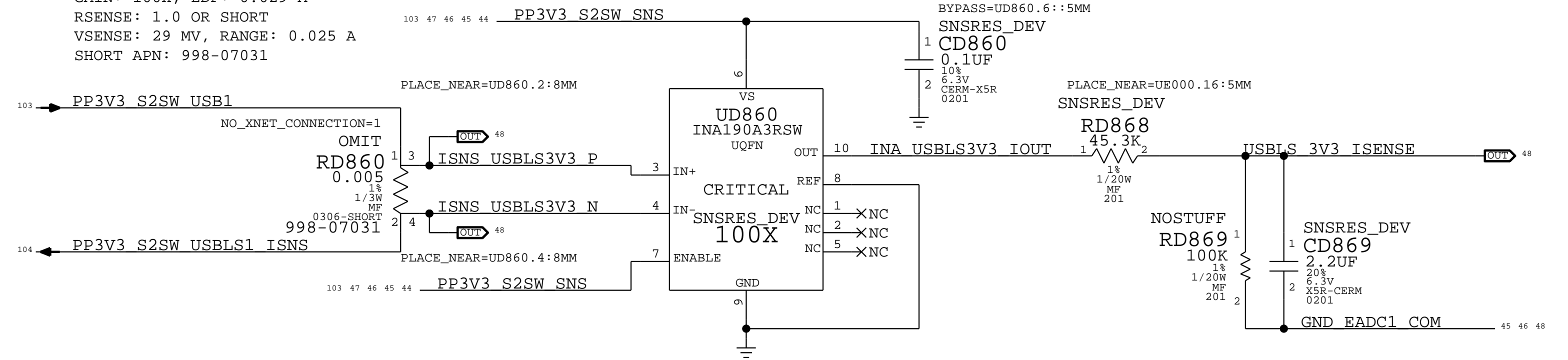
LEFT AMP CURRENT SENSE (IALR)

GAIN: 200X, EDP: 4.0 A
RSENSE: 0.005 OR SHORT
VSENSE: 29 MV, RANGE: 5.0 A
SHORT APN: 998-07031



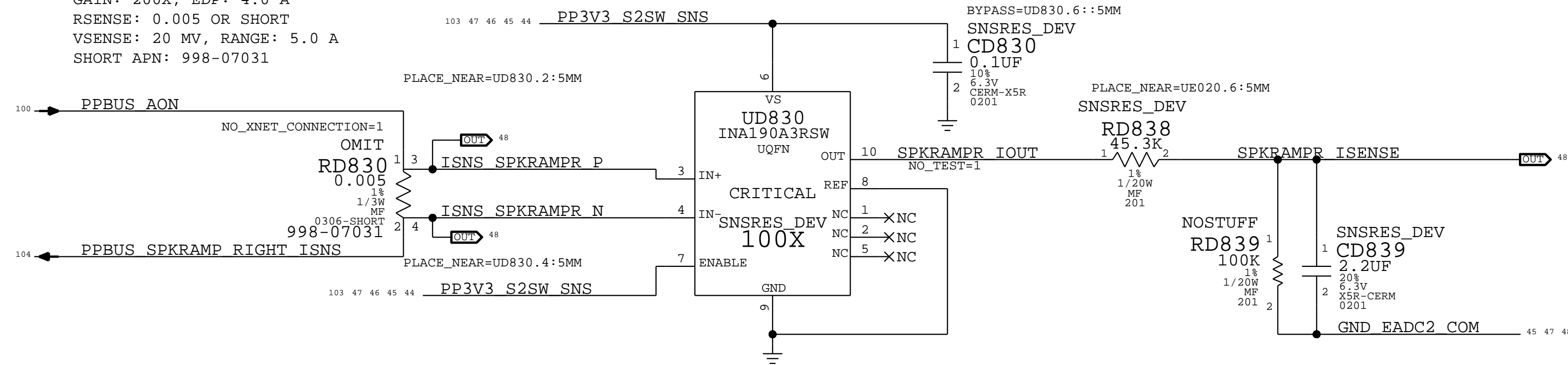
USB2 LEVEL SHIFTER 3.3V (UF750) CURRENT SENSE (IU3C)

GAIN: 100X, EDP: 0.029 A
RSENSE: 1.0 OR SHORT
VSENSE: 29 MV, RANGE: 0.025 A
SHORT APN: 998-07031



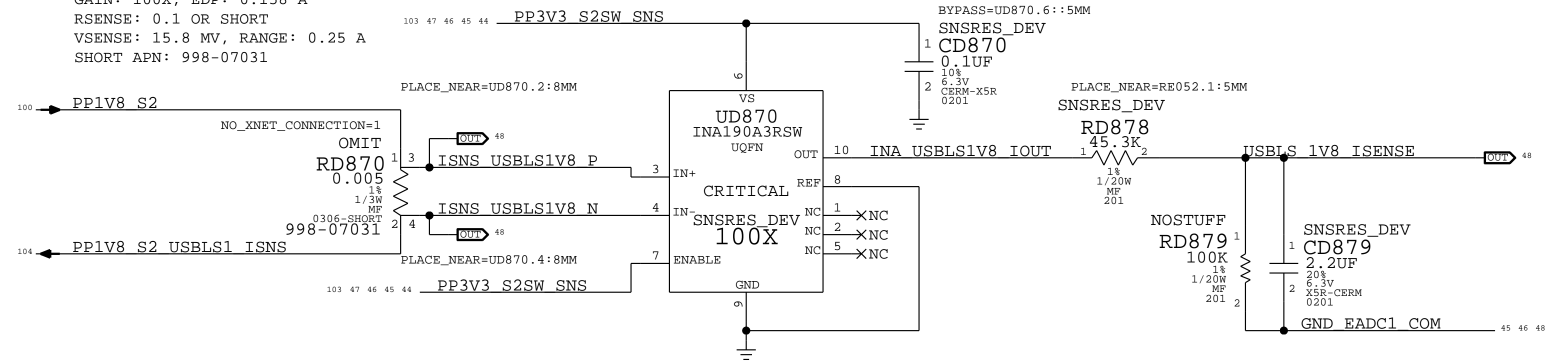
RIGHT AMP CURRENT SENSE (IARR)

GAIN: 200X, EDP: 4.0 A
RSENSE: 0.005 OR SHORT
VSENSE: 20 MV, RANGE: 5.0 A
SHORT APN: 998-07031



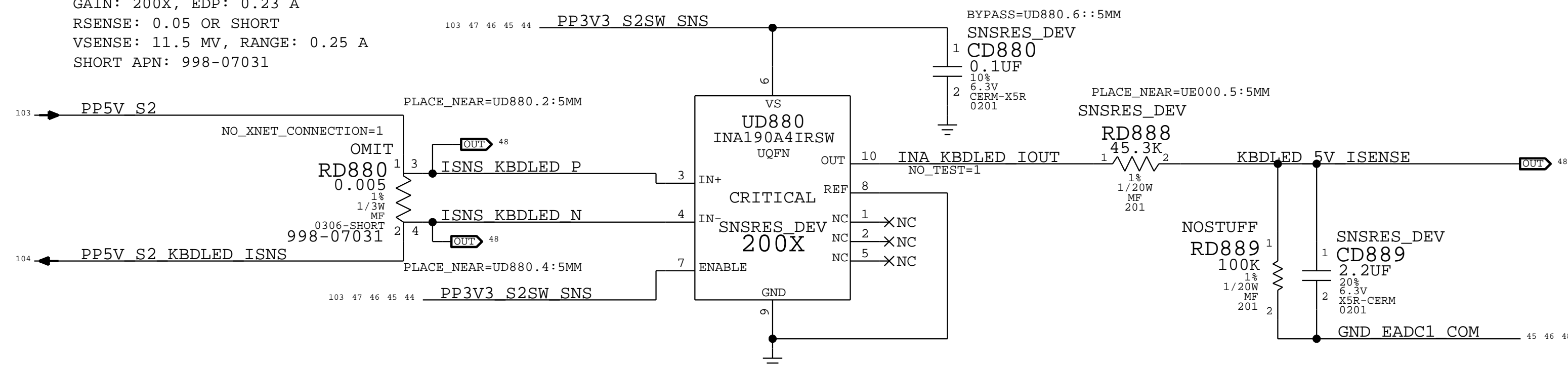
USB2 LEVEL SHIFTER 1.8V (UF750) CURRENT SENSE (N/A)

GAIN: 100X, EDP: 0.158 A
RSENSE: 0.1 OR SHORT
VSENSE: 15.8 MV, RANGE: 0.25 A
SHORT APN: 998-07031



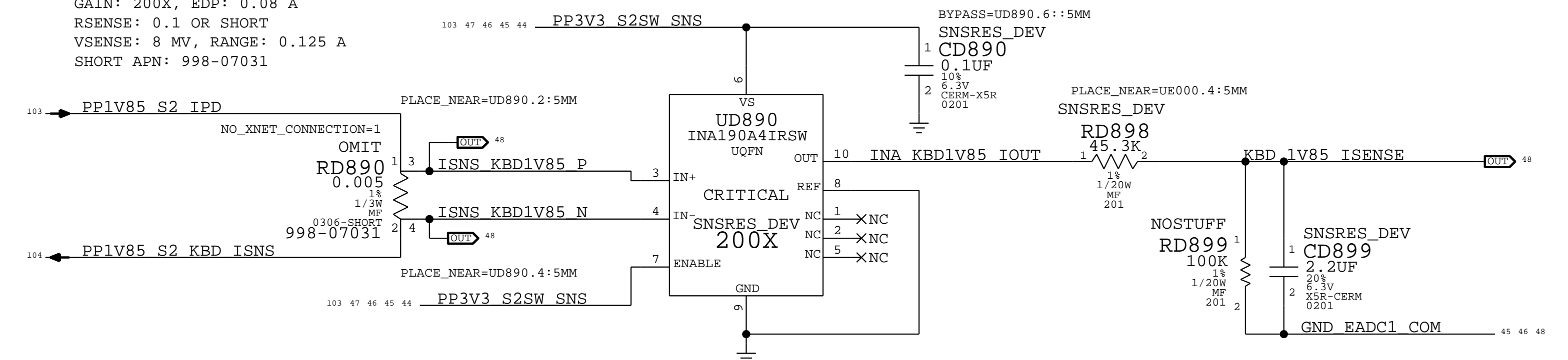
KEYBOARD BACKLIGHT 5V CURRENT SENSE (IKBC)

GAIN: 200X, EDP: 0.23 A
RSENSE: 0.05 OR SHORT
VSENSE: 11.5 MV, RANGE: 0.25 A
SHORT APN: 998-07031



KEYBOARD 1.85V CURRENT SENSE (IK2C)

GAIN: 200X, EDP: 0.08 A
RSENSE: 0.1 OR SHORT
VSENSE: 8 MV, RANGE: 0.125 A
SHORT APN: 998-07031



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SENSORS: POWER LOW SIDE (1/2)



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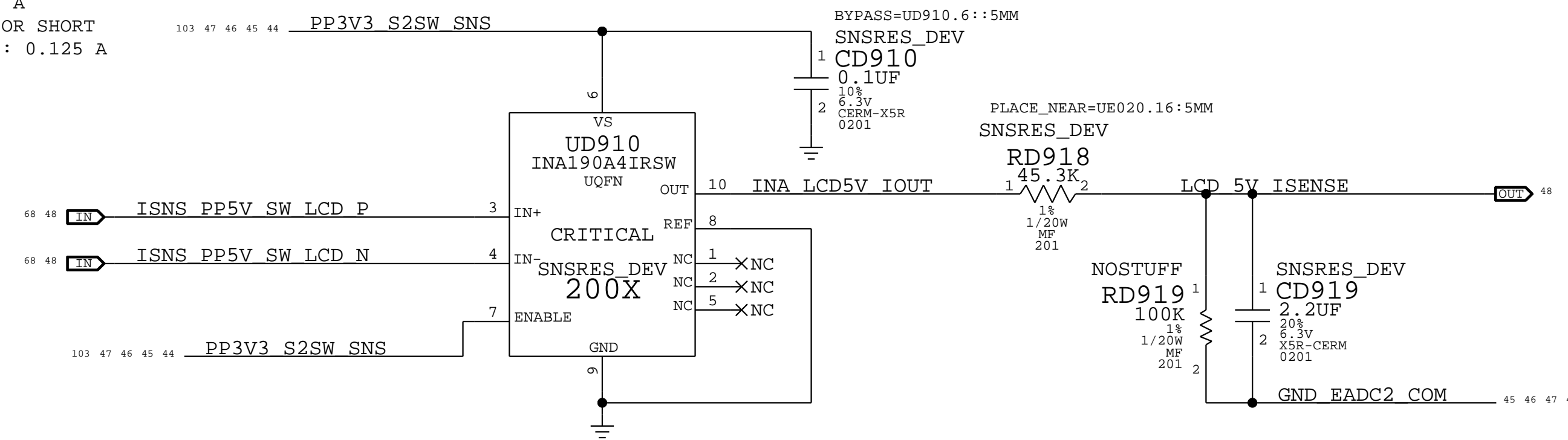
SHEET
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BOM_COST_GROUP=SENSORS

TODO: UPDATE PLACE NEAR

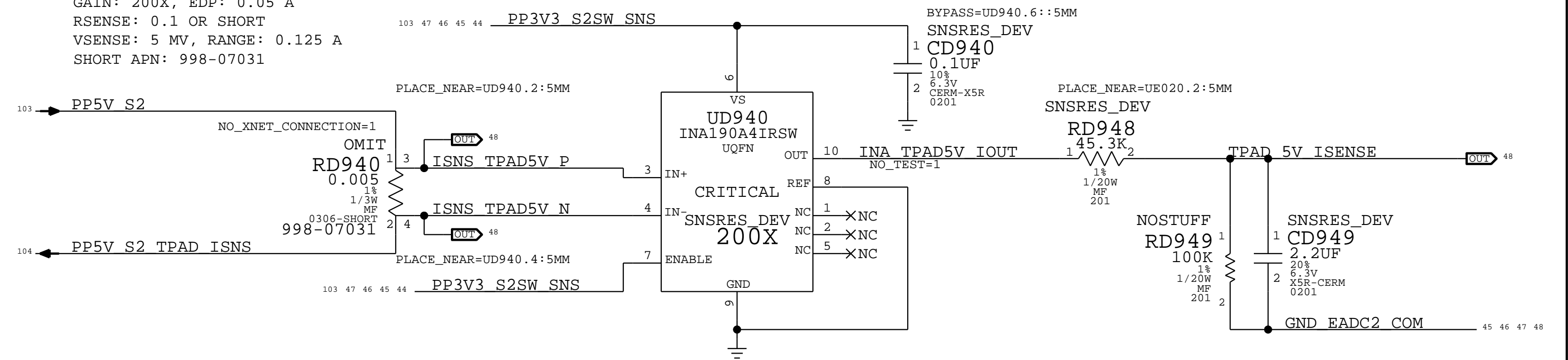
LCD PANEL 5V CURRENT SENSE (IL5C)

GAIN: 200X, EDP: 0.1 A
RSENSE: 0.1 (RP621) OR SHORT
VSENSE: 10 MV, RANGE: 0.125 A
SHORT APN: 998-07031



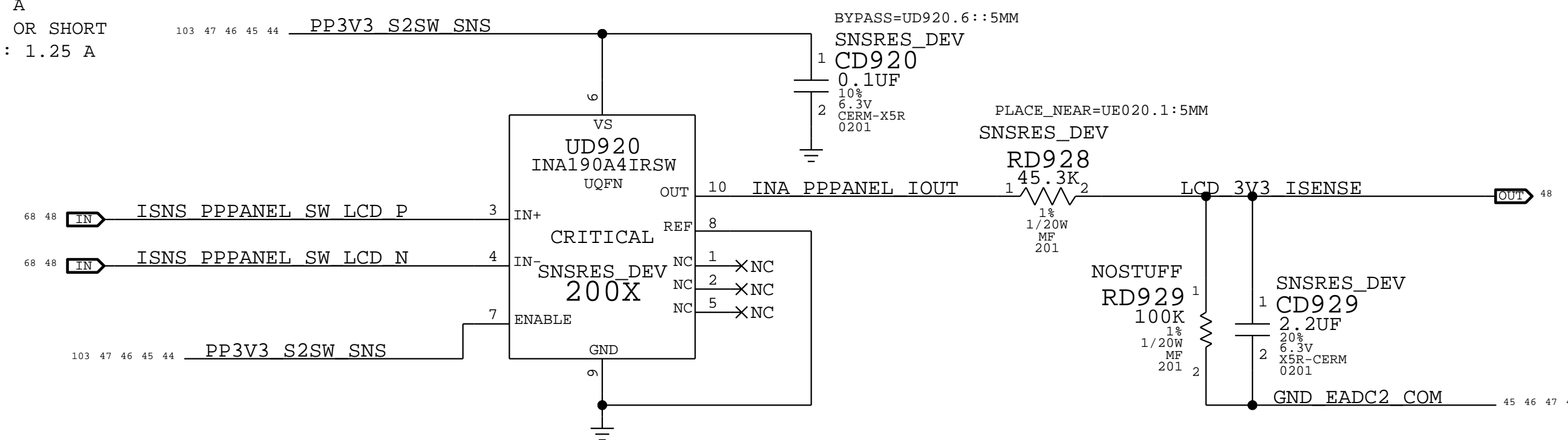
TPAD 5V CURRENT SENSE (IT5C)

GAIN: 200X, EDP: 0.05 A
RSENSE: 0.1 OR SHORT
VSENSE: 5 MV, RANGE: 0.125 A
SHORT APN: 998-07031



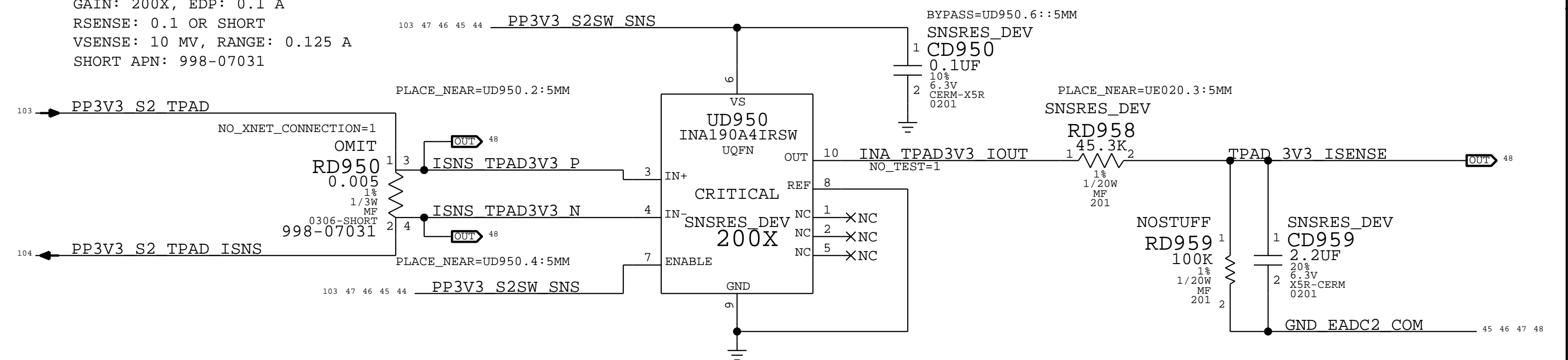
LCD PANEL 3.3/3.8V CURRENT SENSE (IL3C)

GAIN: 200X, EDP: 1.0 A
RSENSE: 0.01 (RP620) OR SHORT
VSENSE: 10 MV, RANGE: 1.25 A
SHORT APN: 998-07031



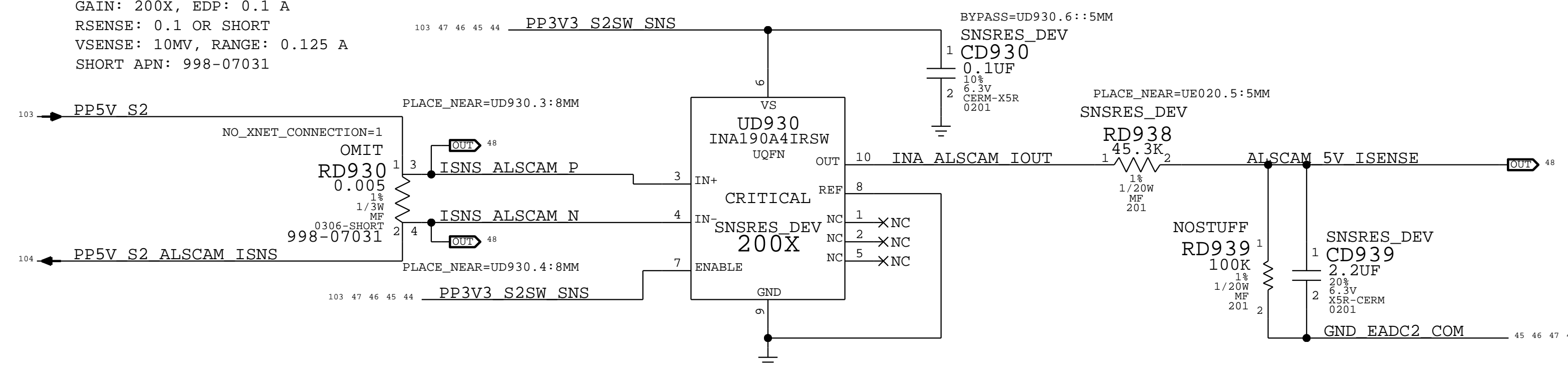
TPAD 3.3V S2 CURRENT SENSE (IT3C)

GAIN: 200X, EDP: 0.1 A
RSENSE: 0.1 OR SHORT
VSENSE: 10 MV, RANGE: 0.125 A
SHORT APN: 998-07031



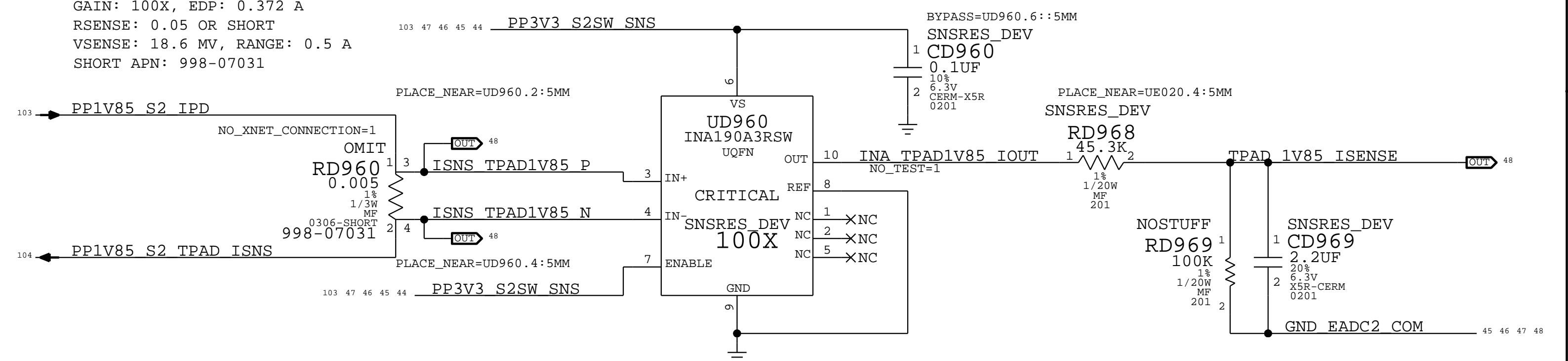
ALSCAM 5V CURRENT SENSE (ICMC)

GAIN: 200X, EDP: 0.1 A
RSENSE: 0.1 OR SHORT
VSENSE: 10MV, RANGE: 0.125 A
SHORT APN: 998-07031



TPAD 1.85V S2 CURRENT SENSE (IT2C)

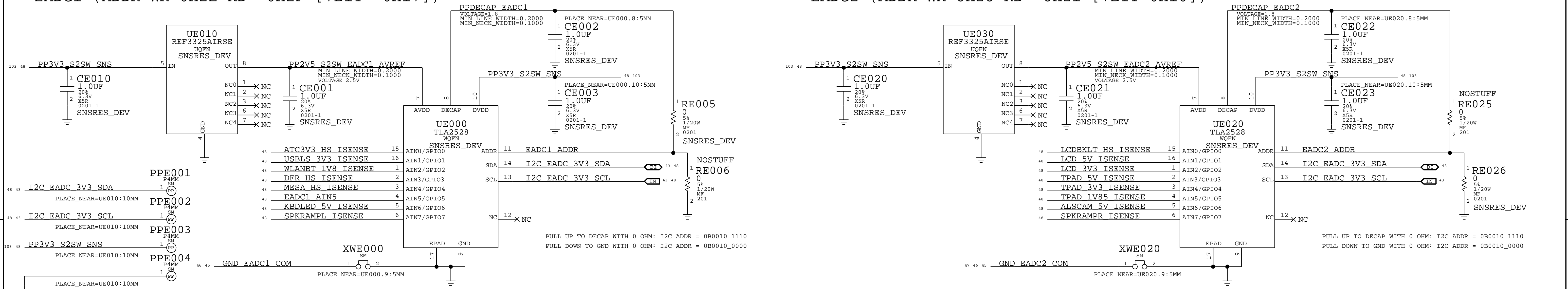
GAIN: 100X, EDP: 0.372 A
RSENSE: 0.05 OR SHORT
VSENSE: 18.6 MV, RANGE: 0.5 A
SHORT APN: 998-07031



PAGE TITLE		
SENSORS: POWER LOW SIDE (2/2)		
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EADC1 (ADDR WR:0X2E RD: 0X2F [7BIT: 0X17])

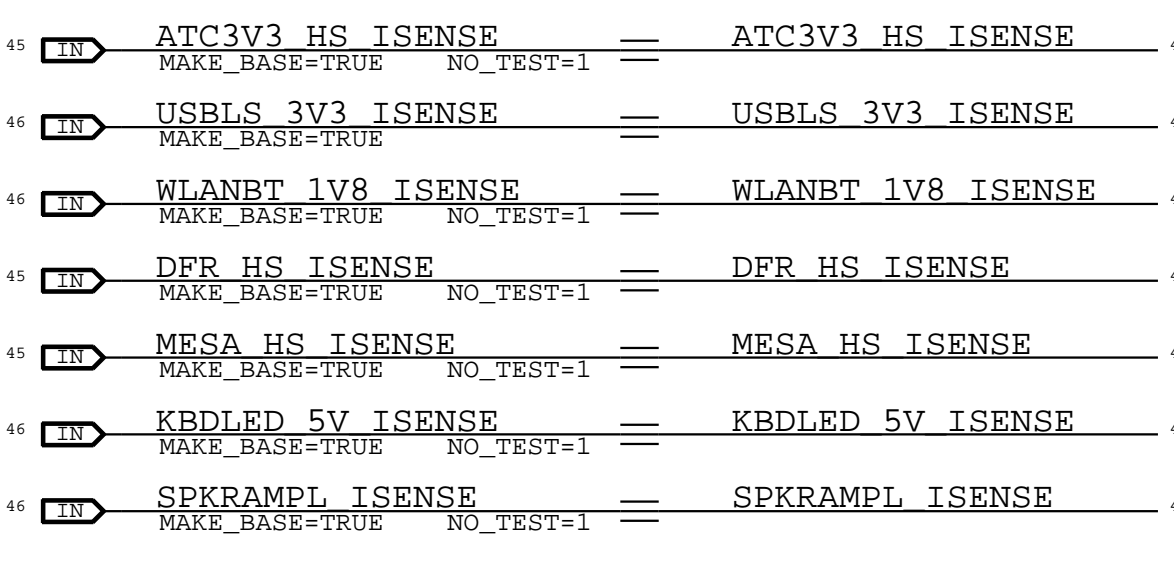
EADC2 (ADDR WR:0X20 RD: 0X21 [7BIT 0X10])



PULL UP TO DECAP WITH 0 OHM: I2C ADDR = 0B0010_1110
 PULL DOWN TO GND WITH 0 OHM: I2C ADDR = 0B0010_0000

PULL UP TO DECAP WITH 0 OHM: I2C ADDR = 0B0010_1110
 PULL DOWN TO GND WITH 0 OHM: I2C ADDR = 0B0010_0000

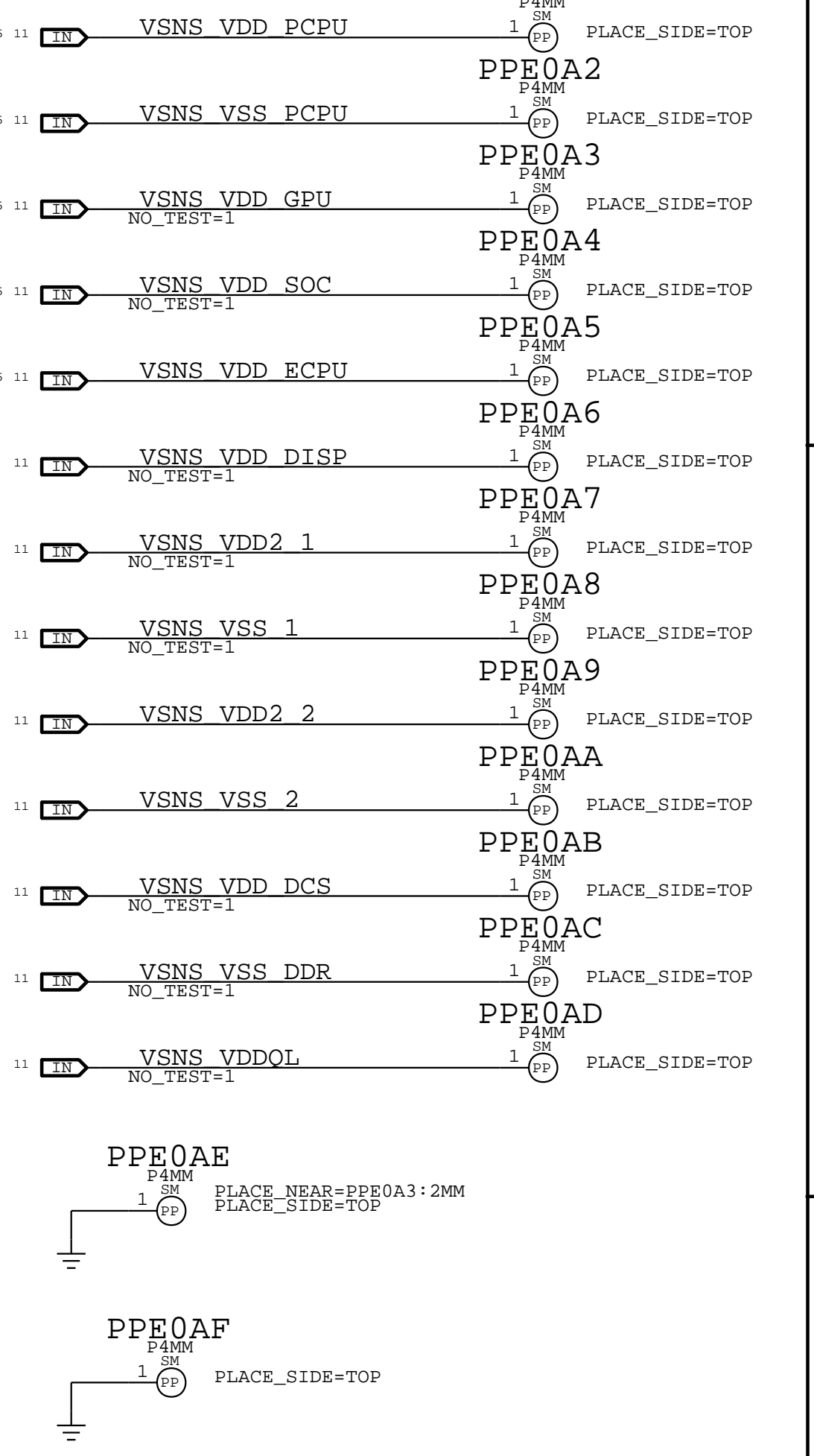
EADC1 AIN ALIAS



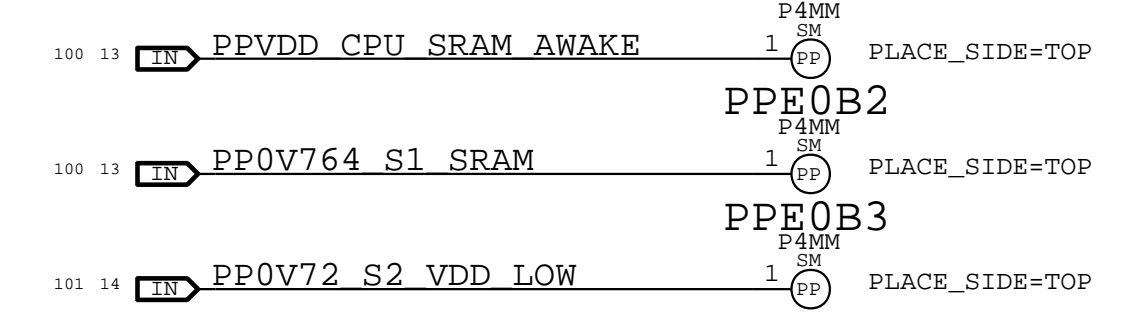
POWER VALIDATION TEST POINTS (WIP)



SOC SENSE LINES



PROBE POINTS

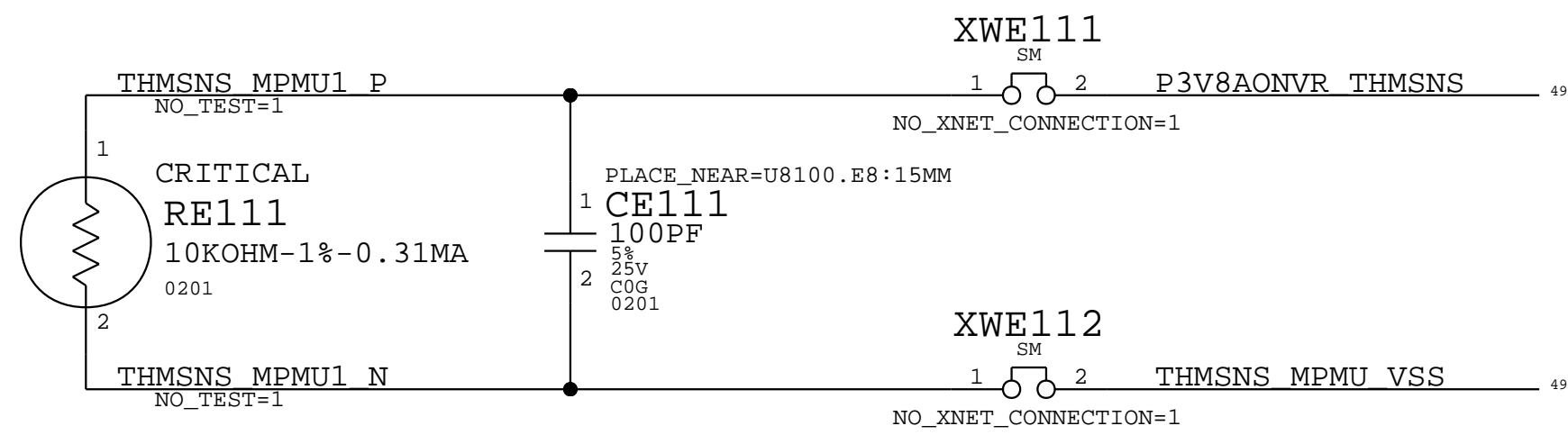


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BOM_COST_GROUP=SENSORS

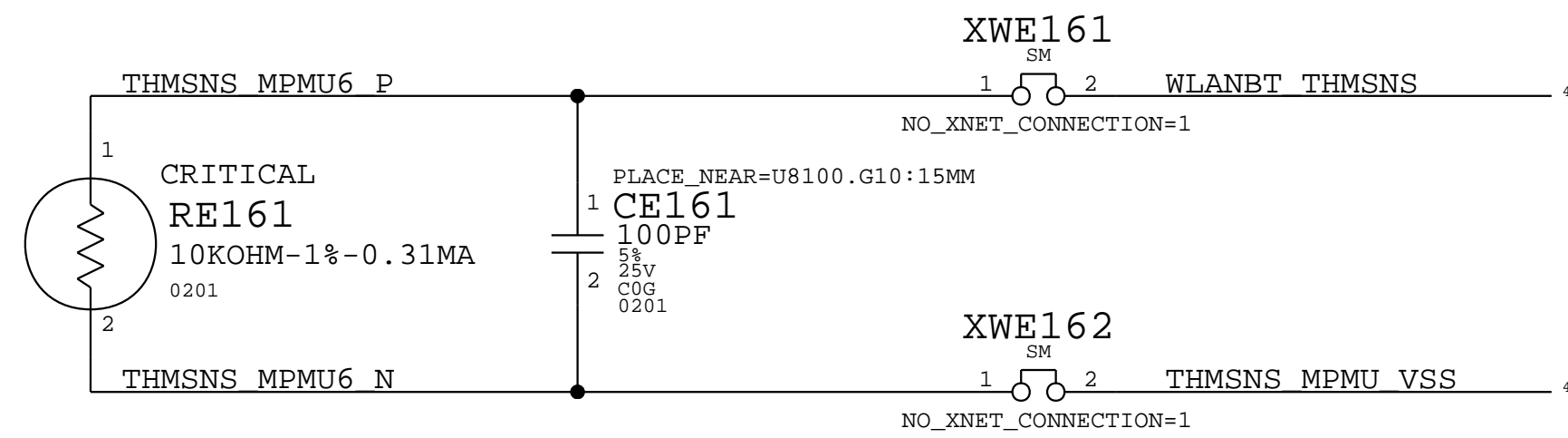
MASTER PMU TDEV1 [TMVR]

LOCATION: 3.8V AON VR BETWEEN PHASE 2 AND PHASE3 MOSFETS



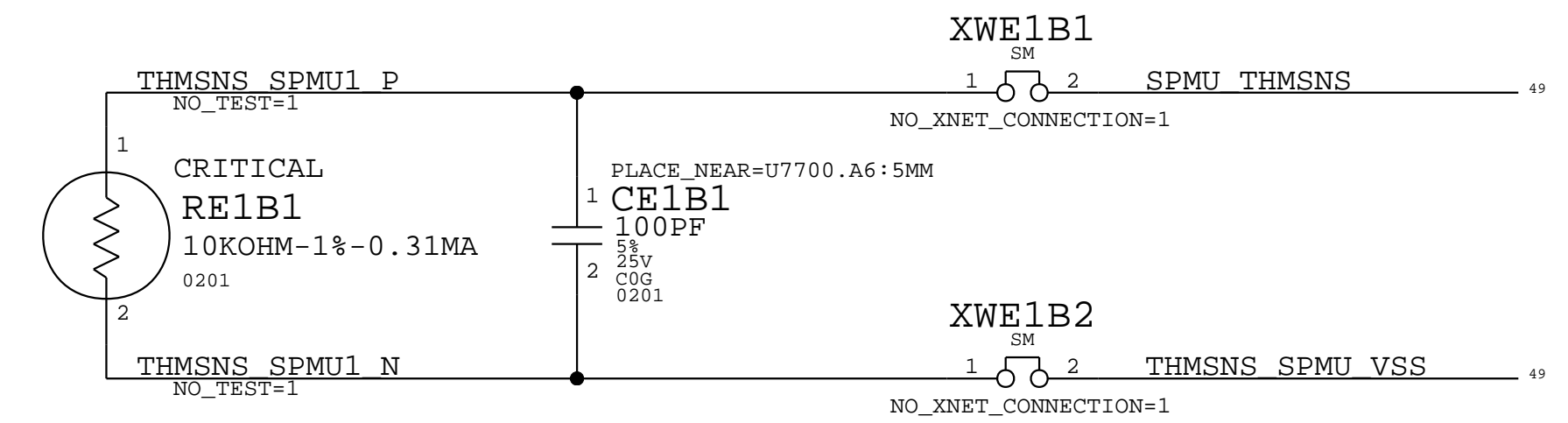
MASTER PMU TDEV6 [TWOP]

LOCATION: WLANBT, BACKSIDE



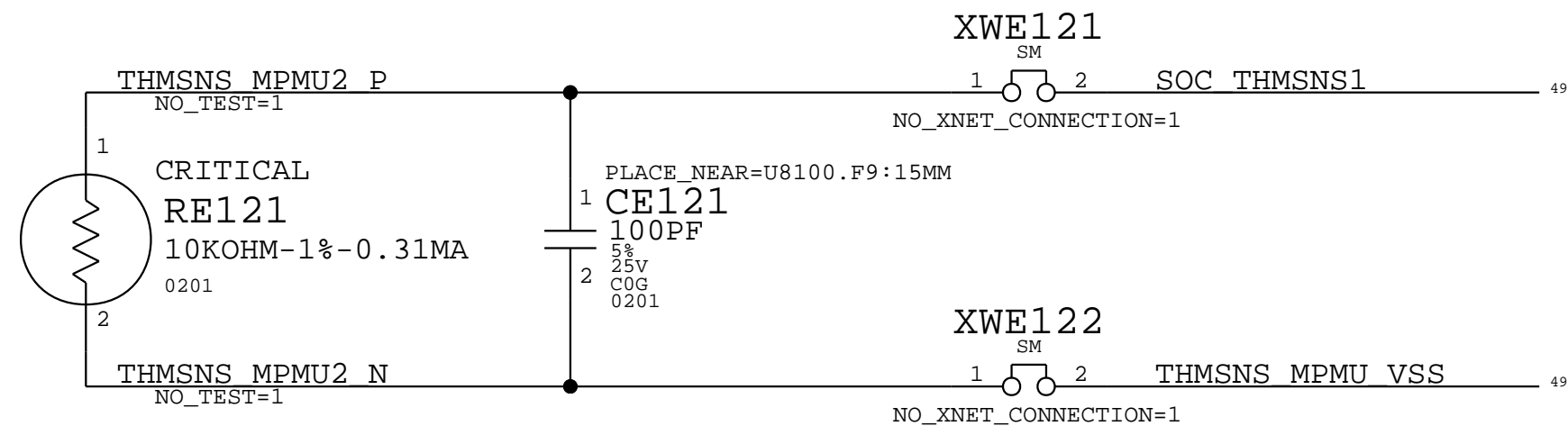
SLAVE PMU TDEV1 [TPSP]

LOCATION: SLAVE PMU, BUCK10 INDUCTOR PROXIMITY



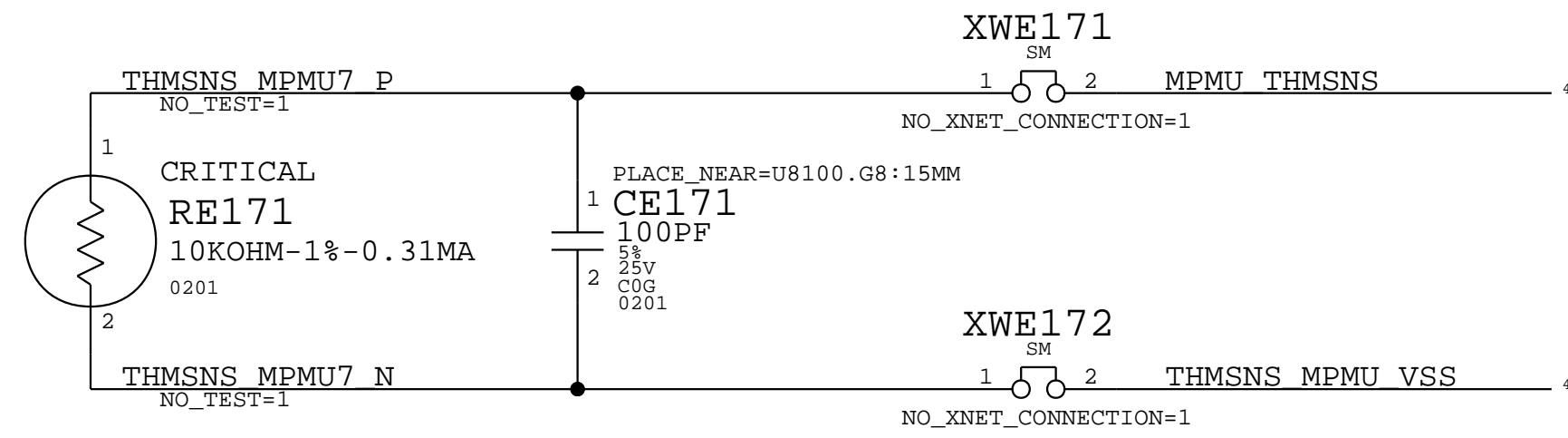
MASTER PMU TDEV2 [TSDD]

LOCATION: SOC DRAM AREA, BACKSIDE (TOP)



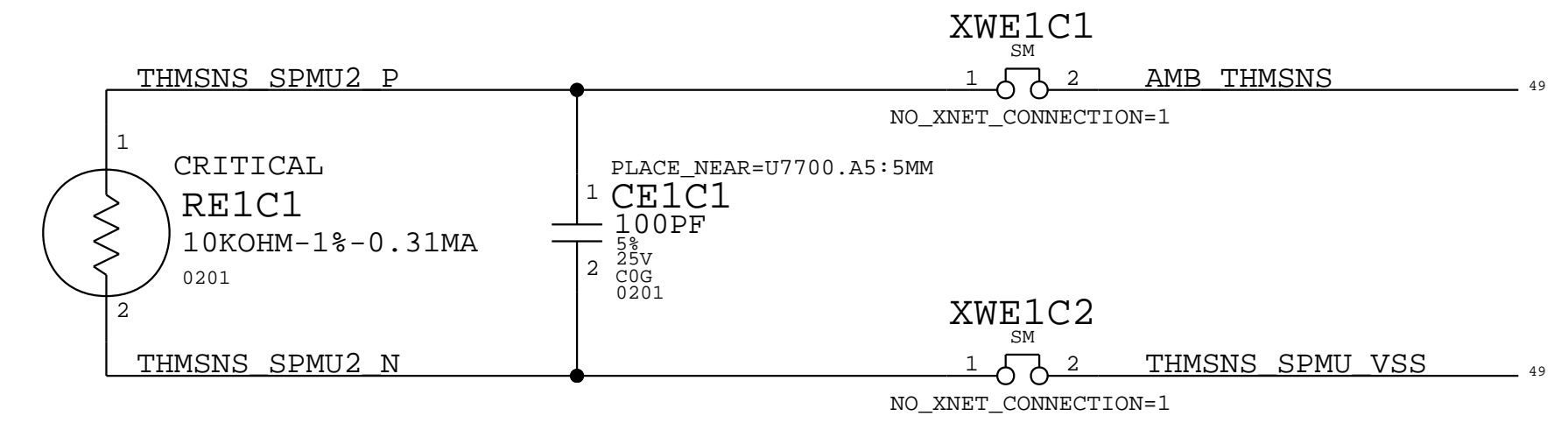
MASTER PMU TDEV7 [TPMP]

LOCATION: MASTER PMU, BETWEEN BUCK0 AND BUCK1 INDUCTORS



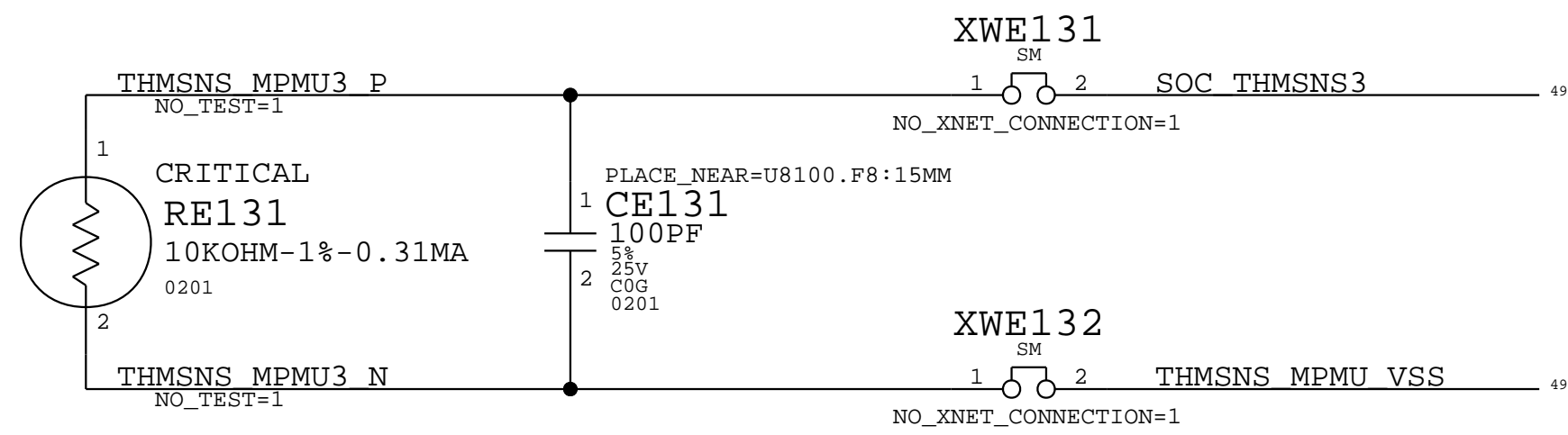
SLAVE PMU TDEV2 [TaMP]

LOCATION: MLB AIR INTAKE PROXIMITY



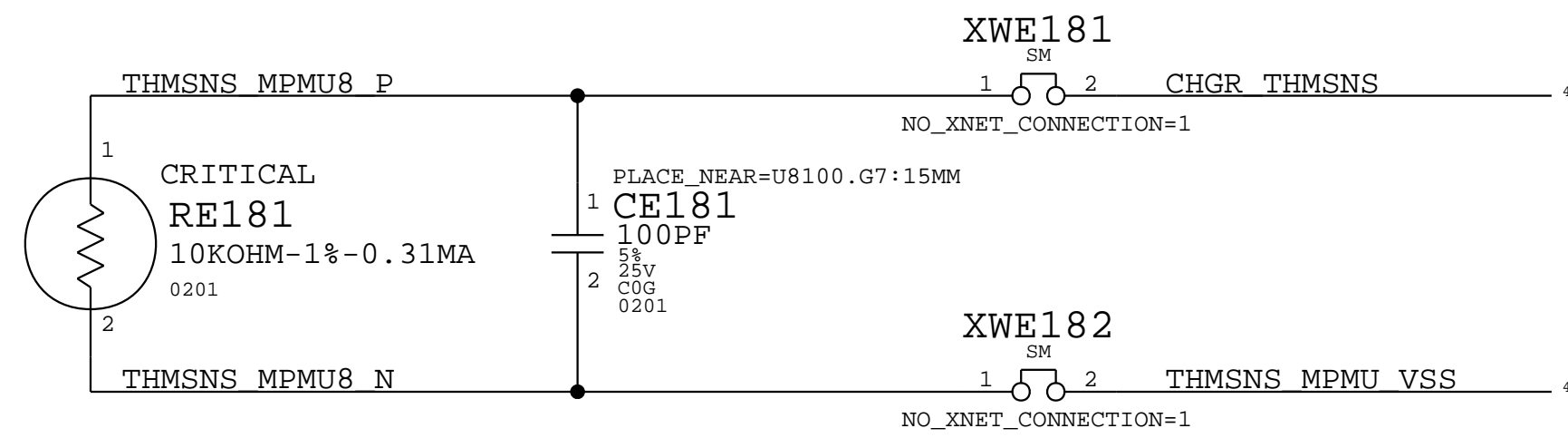
MASTER PMU TDEV3 [TSCD]

LOCATION: SOC CORE AREA BACKSIDE (TOP)



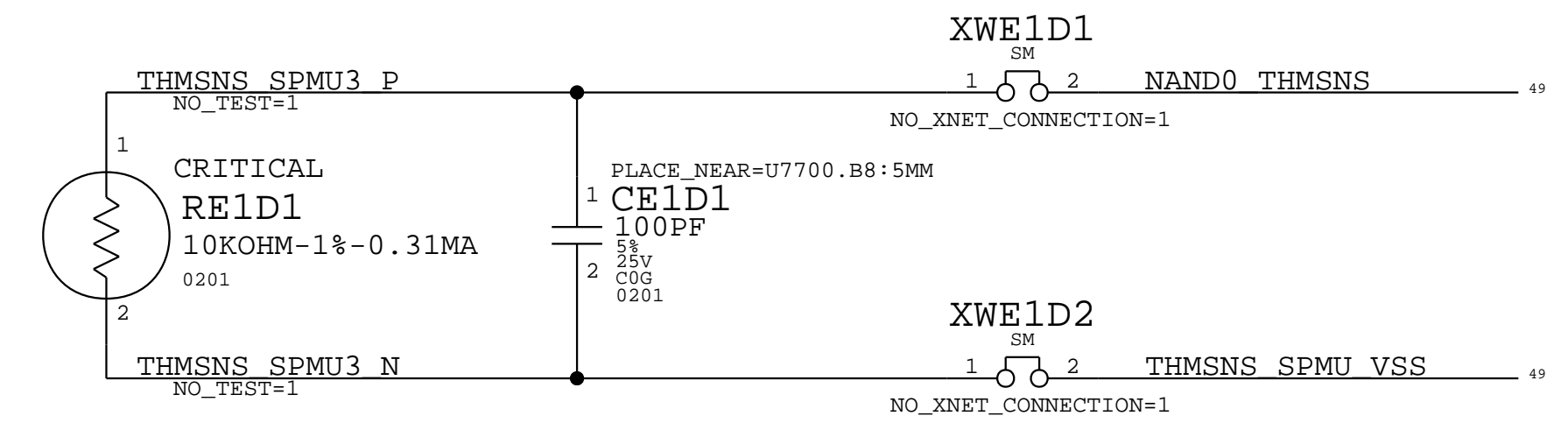
MASTER PMU TDEV8 [TCHP]

LOCATION: CHARGER, BETWEEN INDUCTOR AND MOSFETS



SLAVE PMU TDEV3 [TH0T]

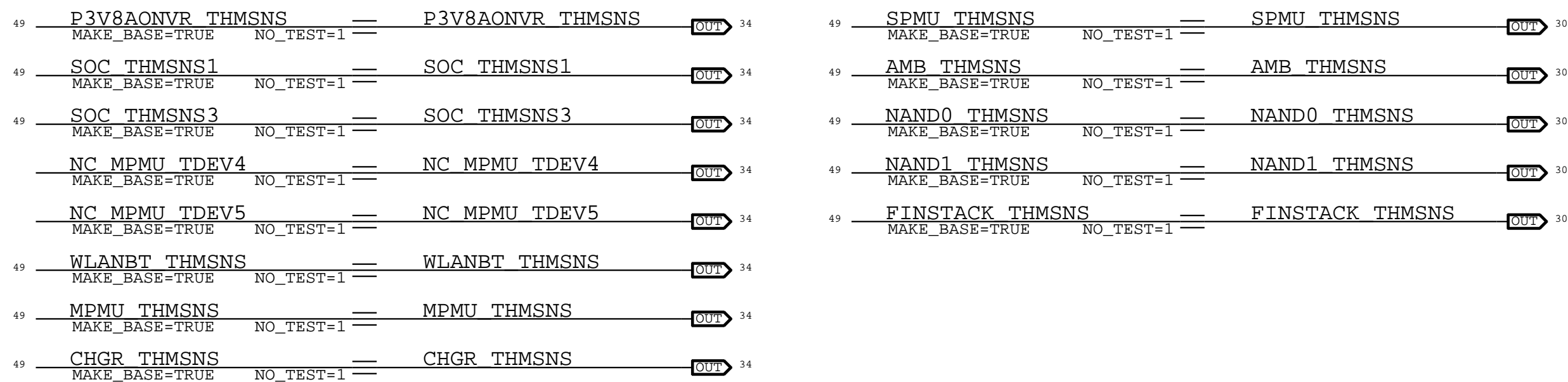
LOCATION: LOWER LEFT CORNER OF NAND DEVICES



MASTER PMU TDEV4 & TDEV5

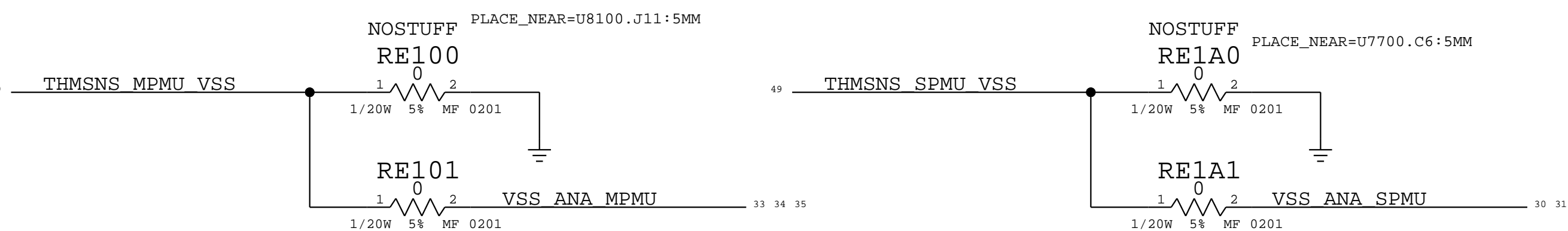
LOCATION: DOES NOT EXIST

PMU TDEV MAPPING



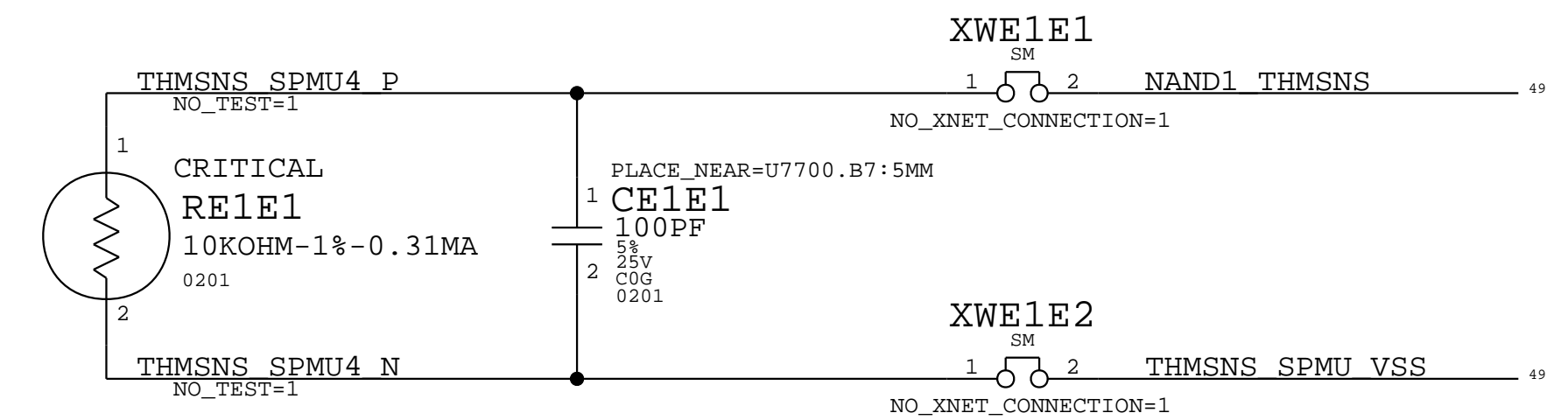
TAP NEGATIVE CLOSE TO VSS_REF

ADDED OPTION PER RDAR://60203428



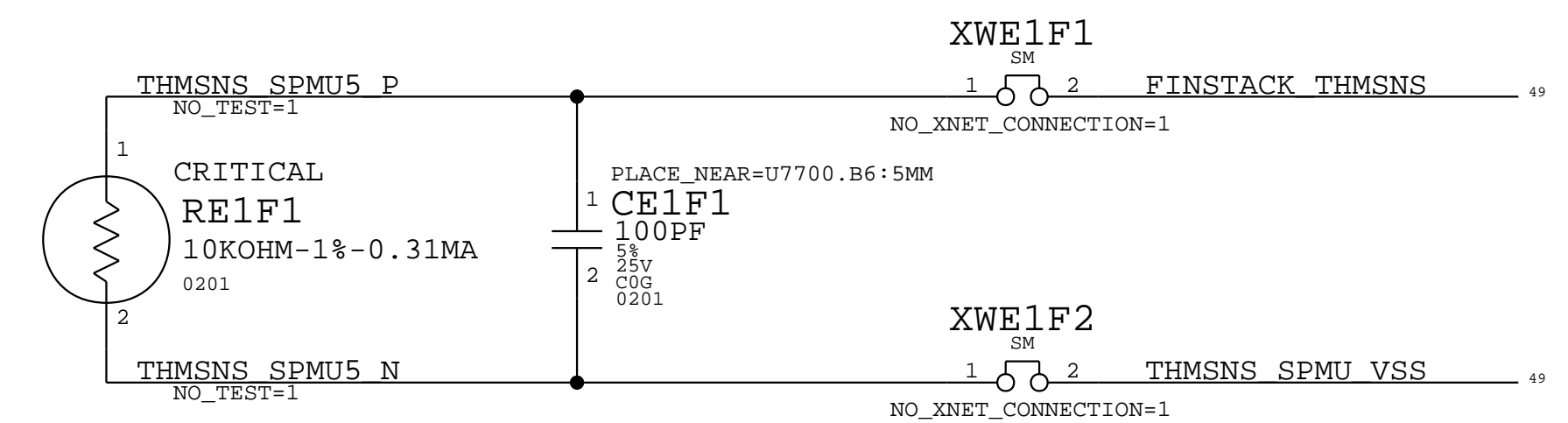
SLAVE PMU TDEV4 [TH0B]

LOCATION: UPPER RIGHT CORNER OF NAND DEVICES



SLAVE PMU TDEV5 [Th1H]

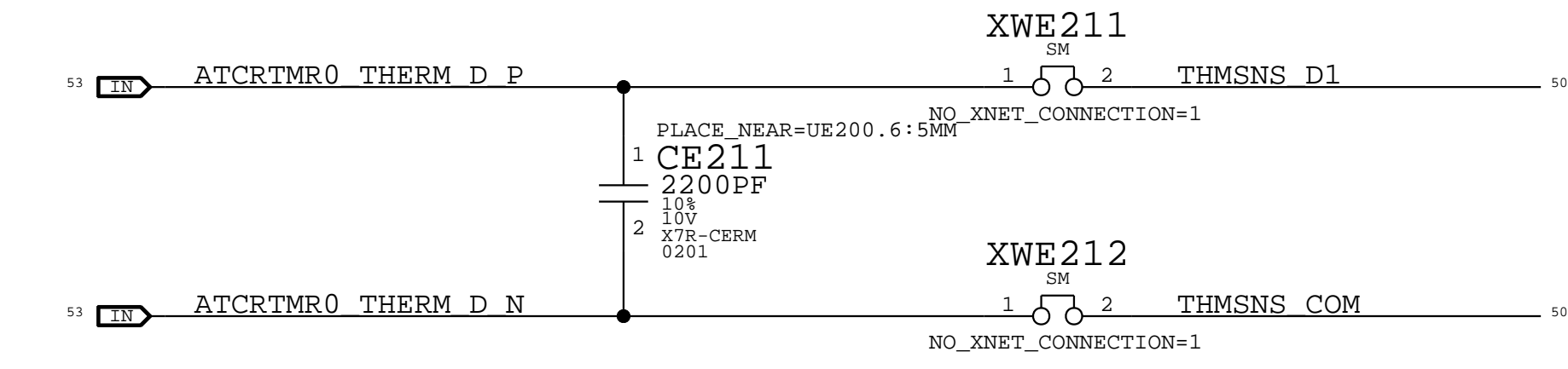
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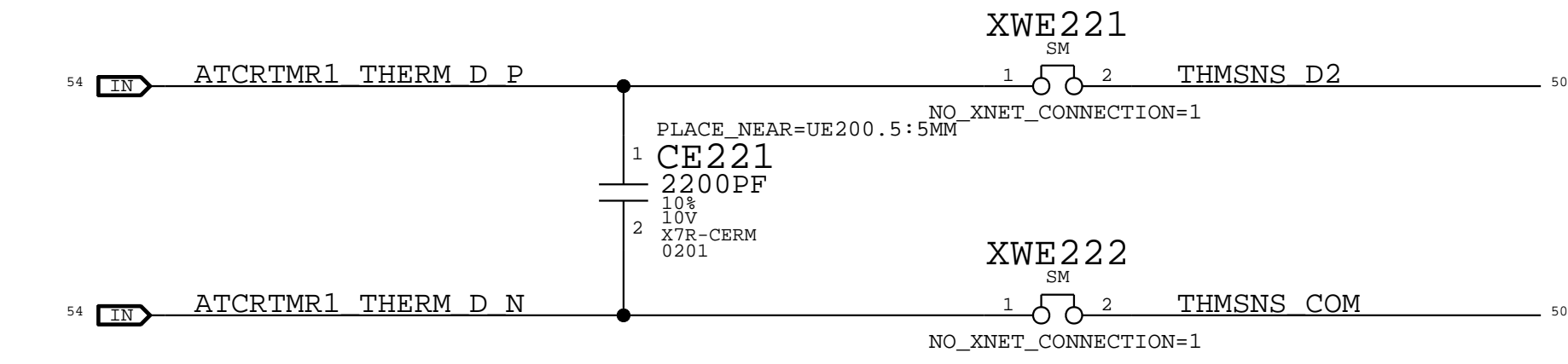
RETIMER ATC0 [TT0D]

LOCATION: ON CHIP



RETIMER ATC1 [TT1D]

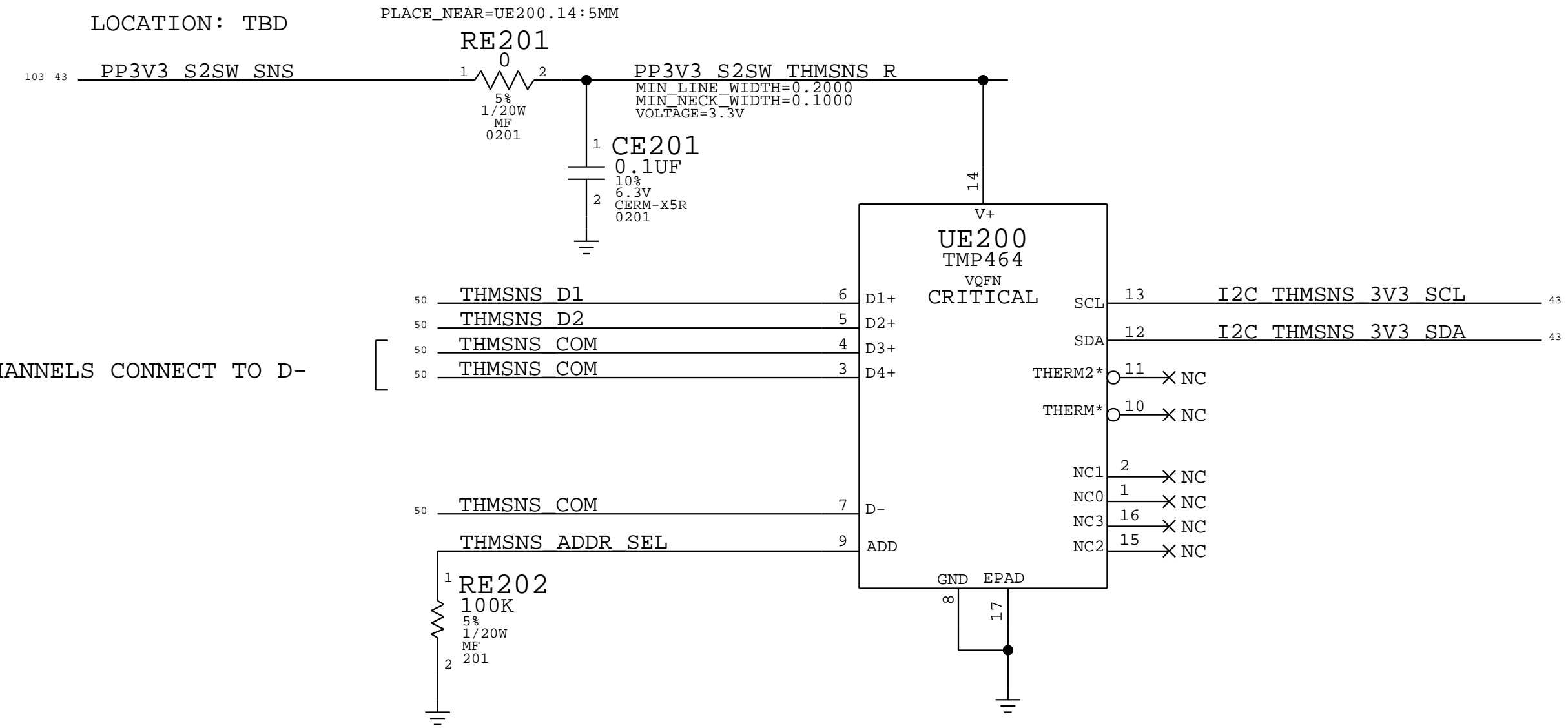
LOCATION: ON CHIP



I/O PROXIMITY [TIOP]

I2C ADDR WR:0X90 RD: 0X91

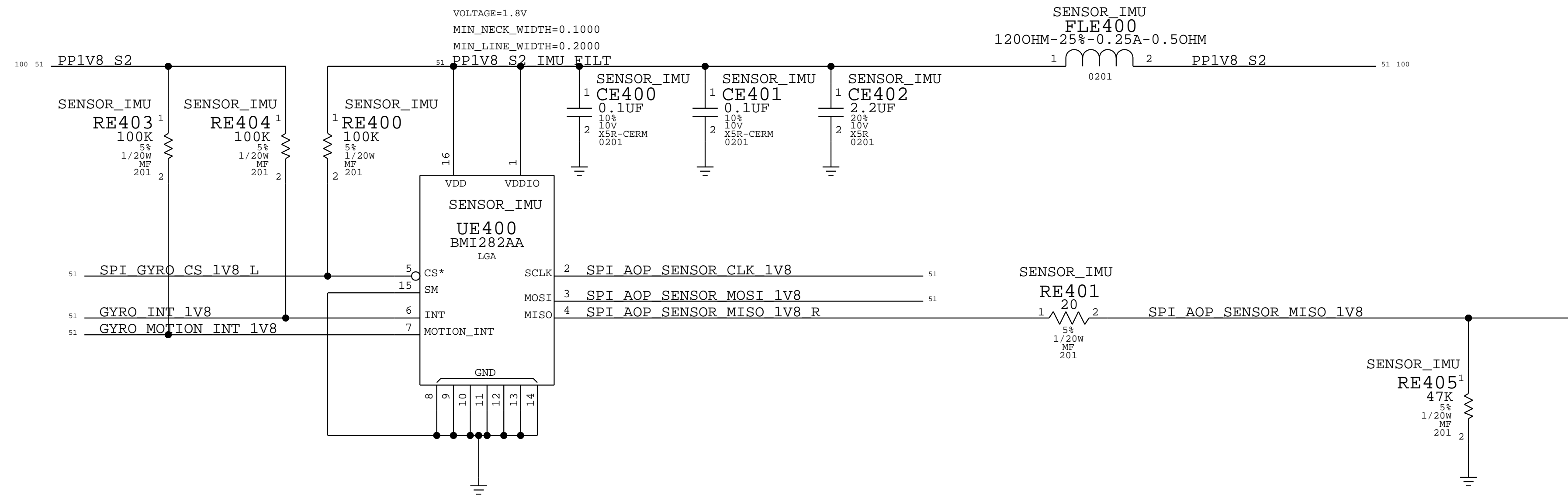
LOCATION: TBD



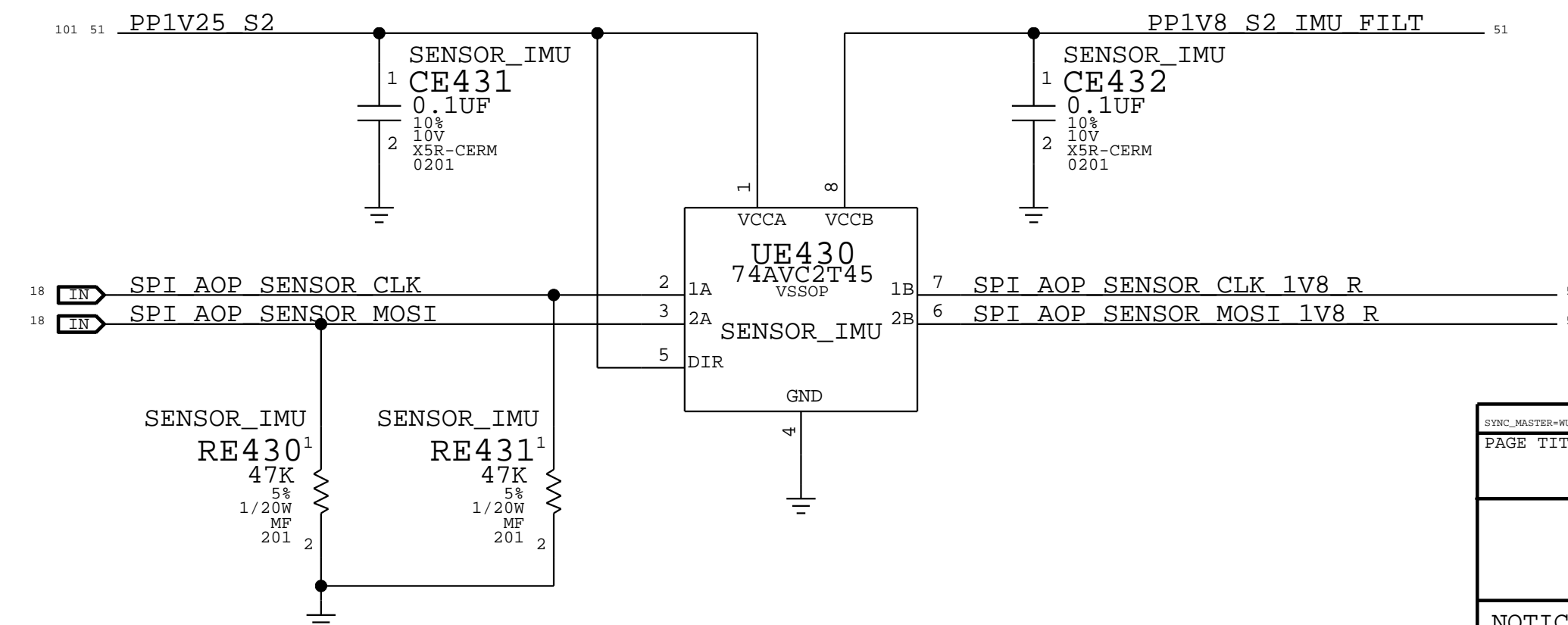
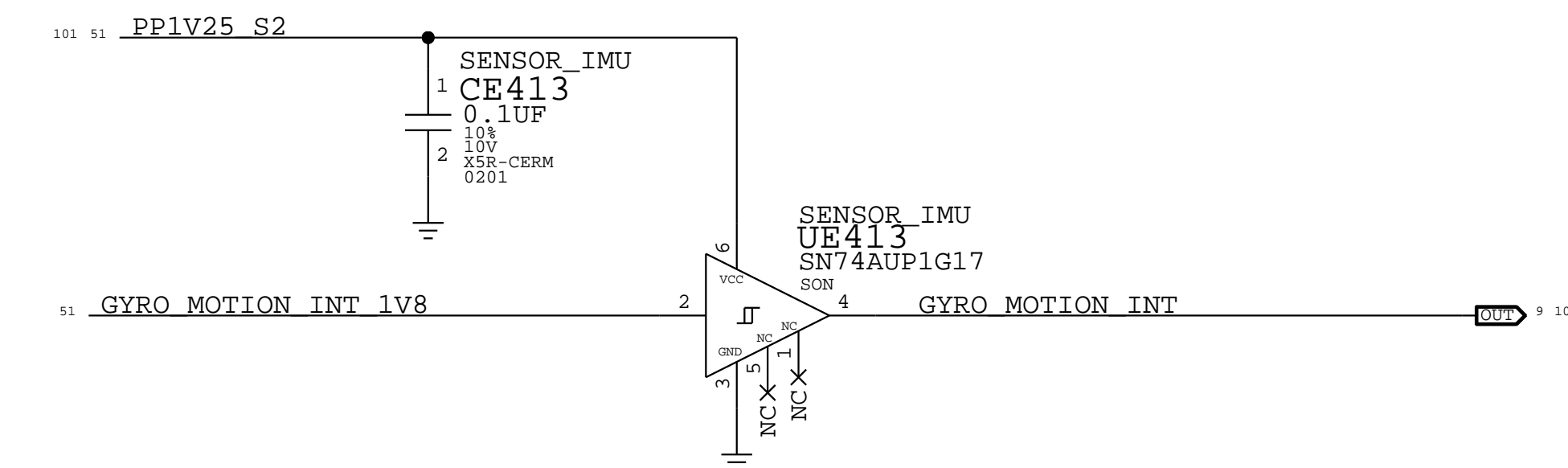
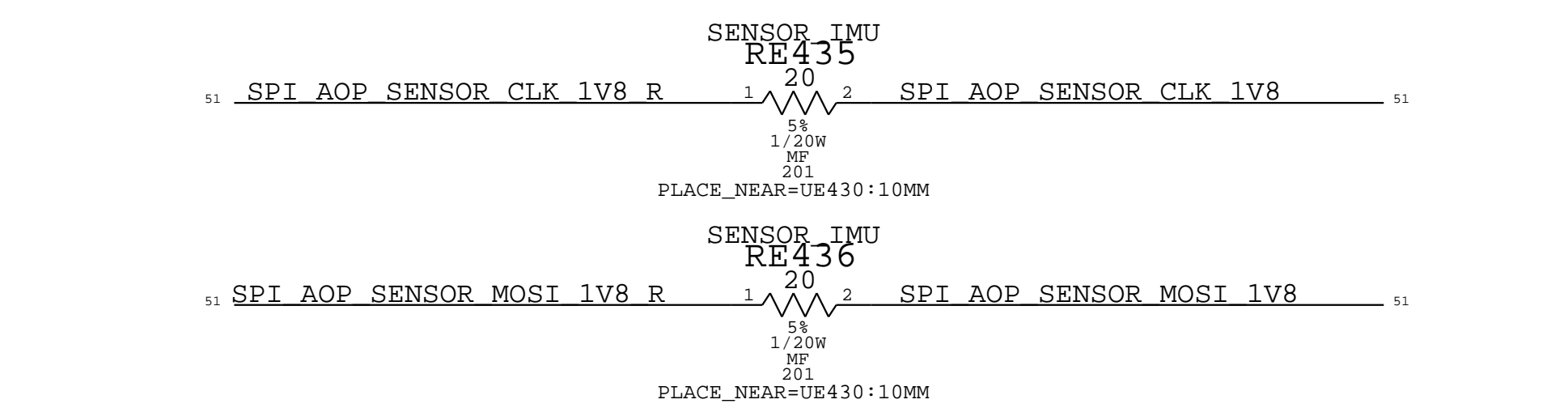
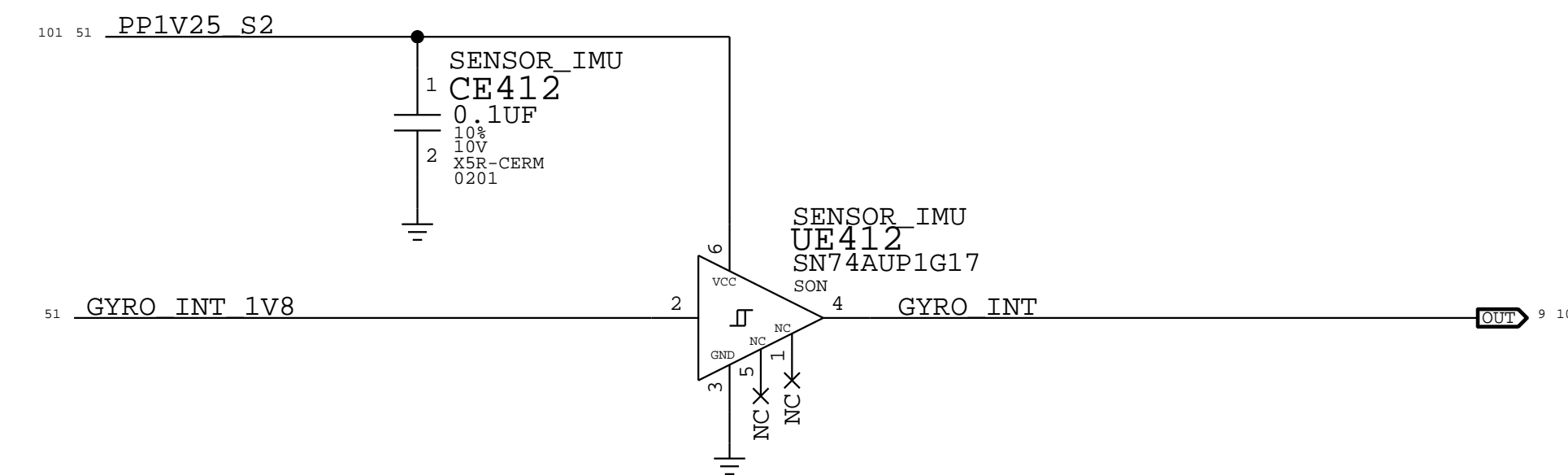
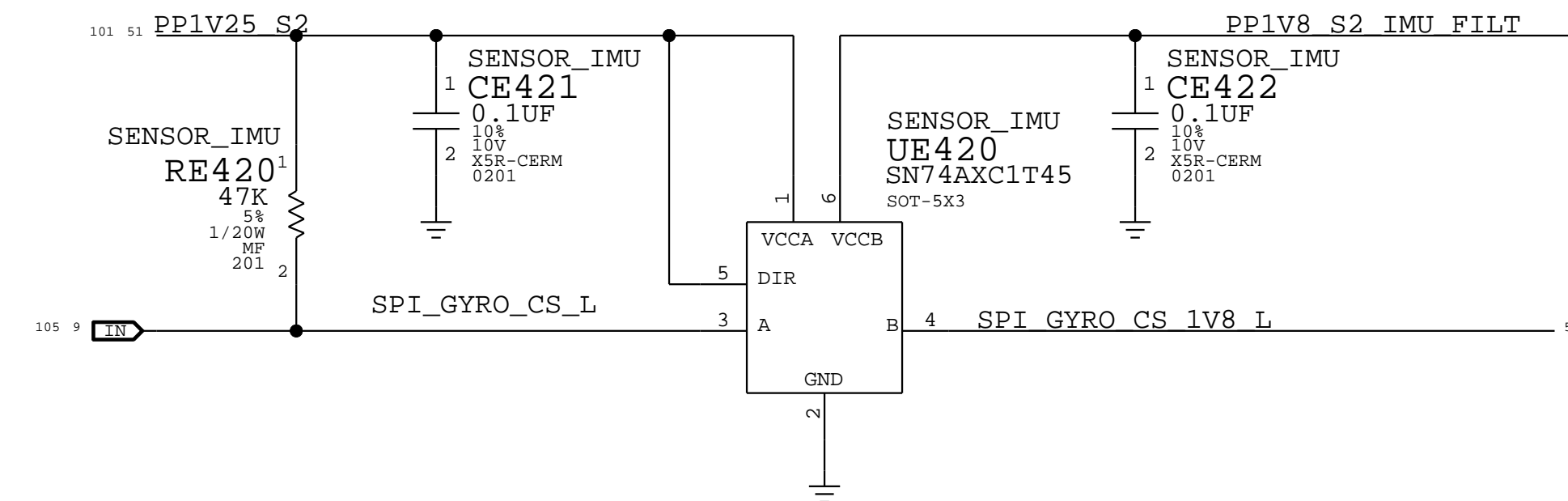
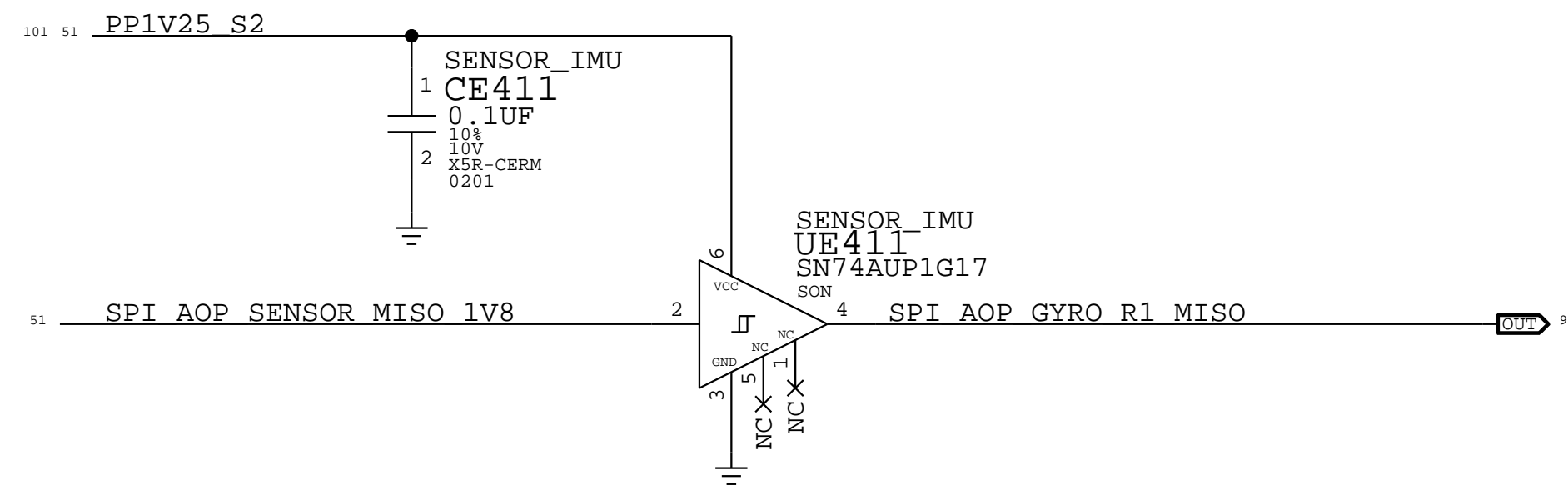
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BOM_COST_GROUP=SENSORS

KOBOL: ACCEL & GYRO



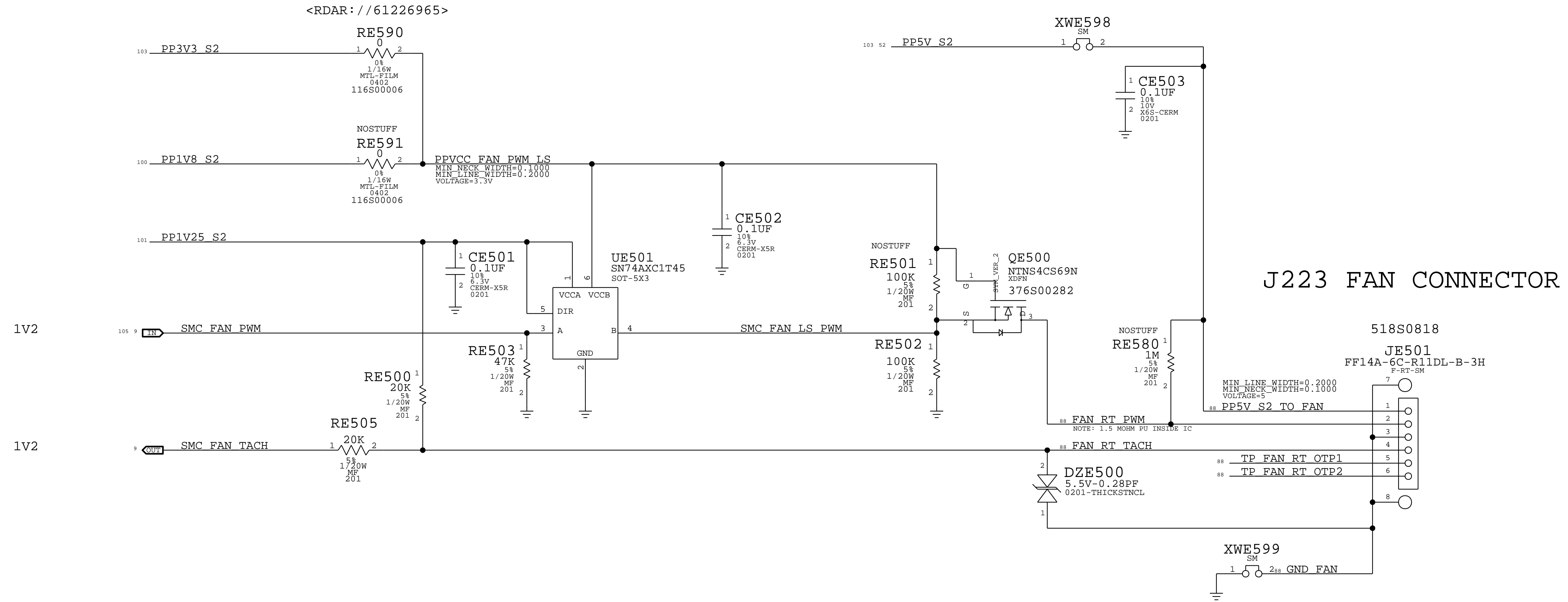
SPI LEVEL TRANSLATION



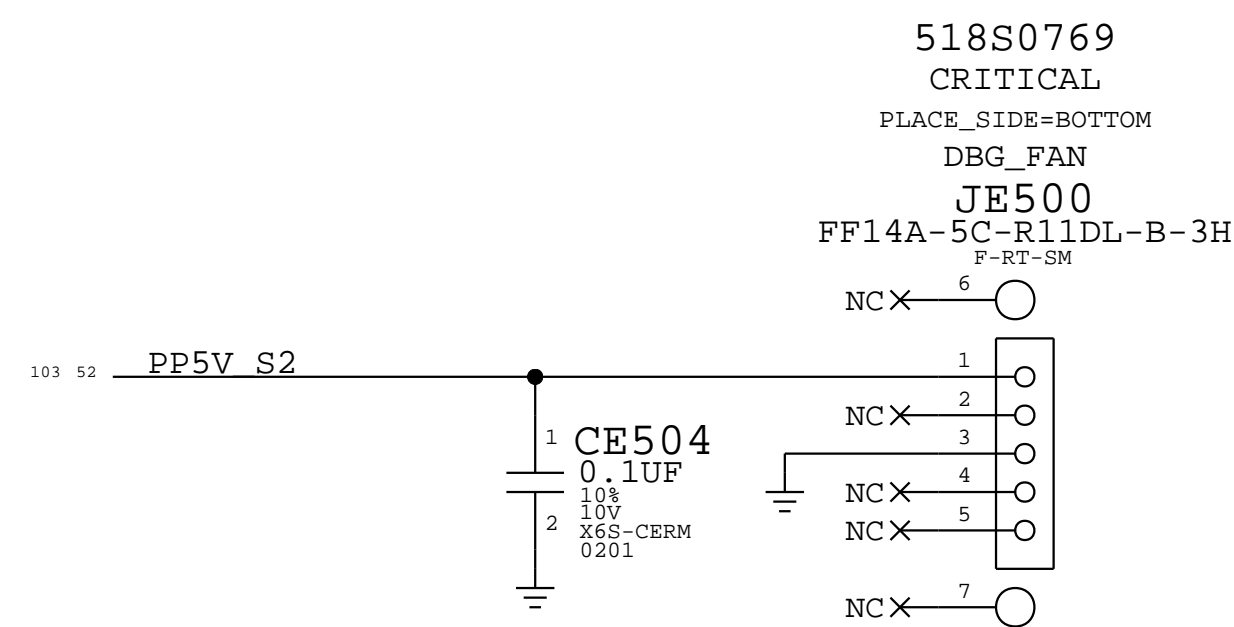
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	PAGE	144 OF 999
	SHEET	51 OF 117

BOM_COST_GROUP=SENSORS

FAN CONTROL



5V POWER FOR A DEBUG FAN



DRAWING NUMBER		SIZE
051-05399		D
REVISION		BRANCH
9.0.0		dvt-1
PAGE		SHEET
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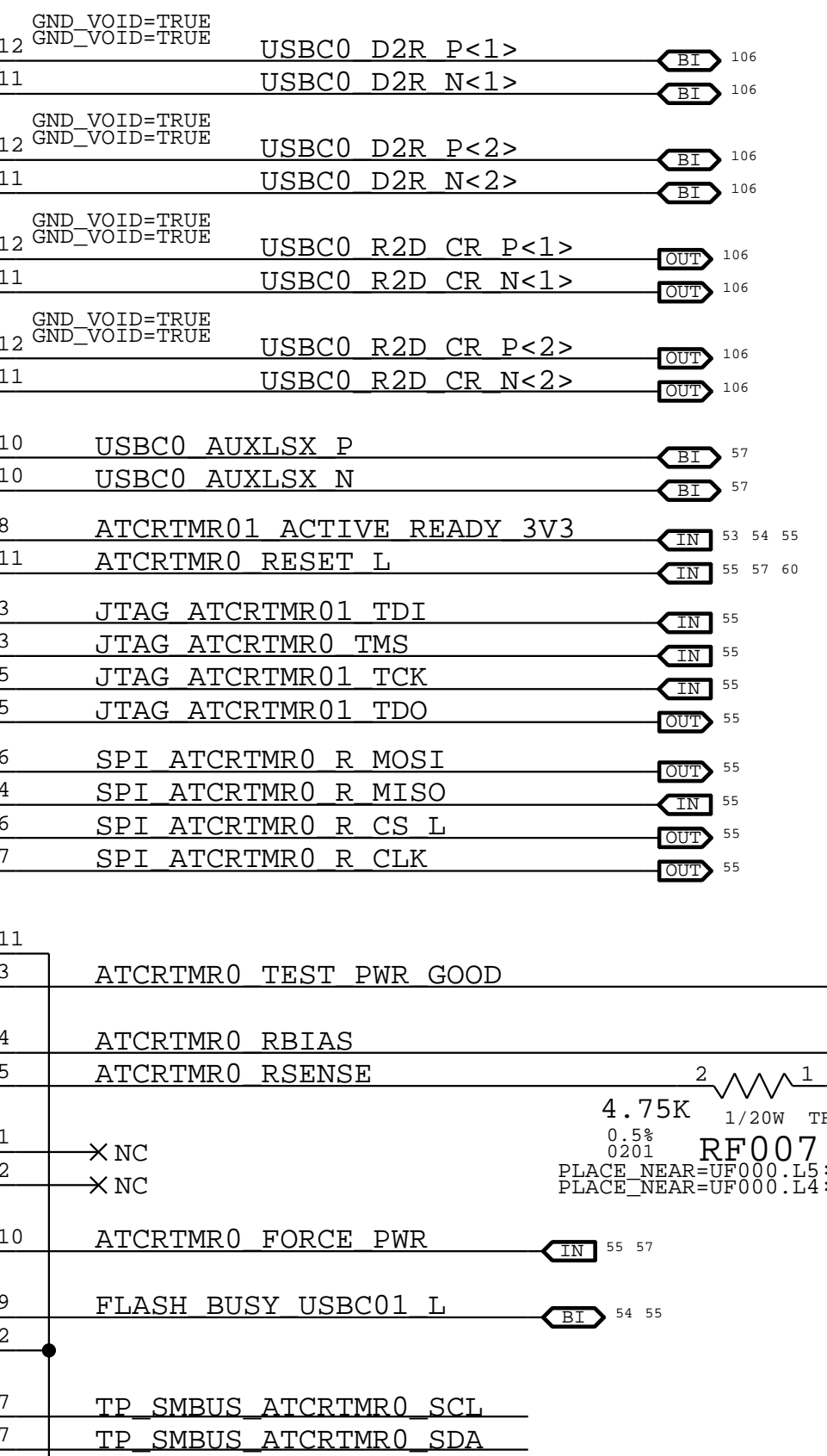
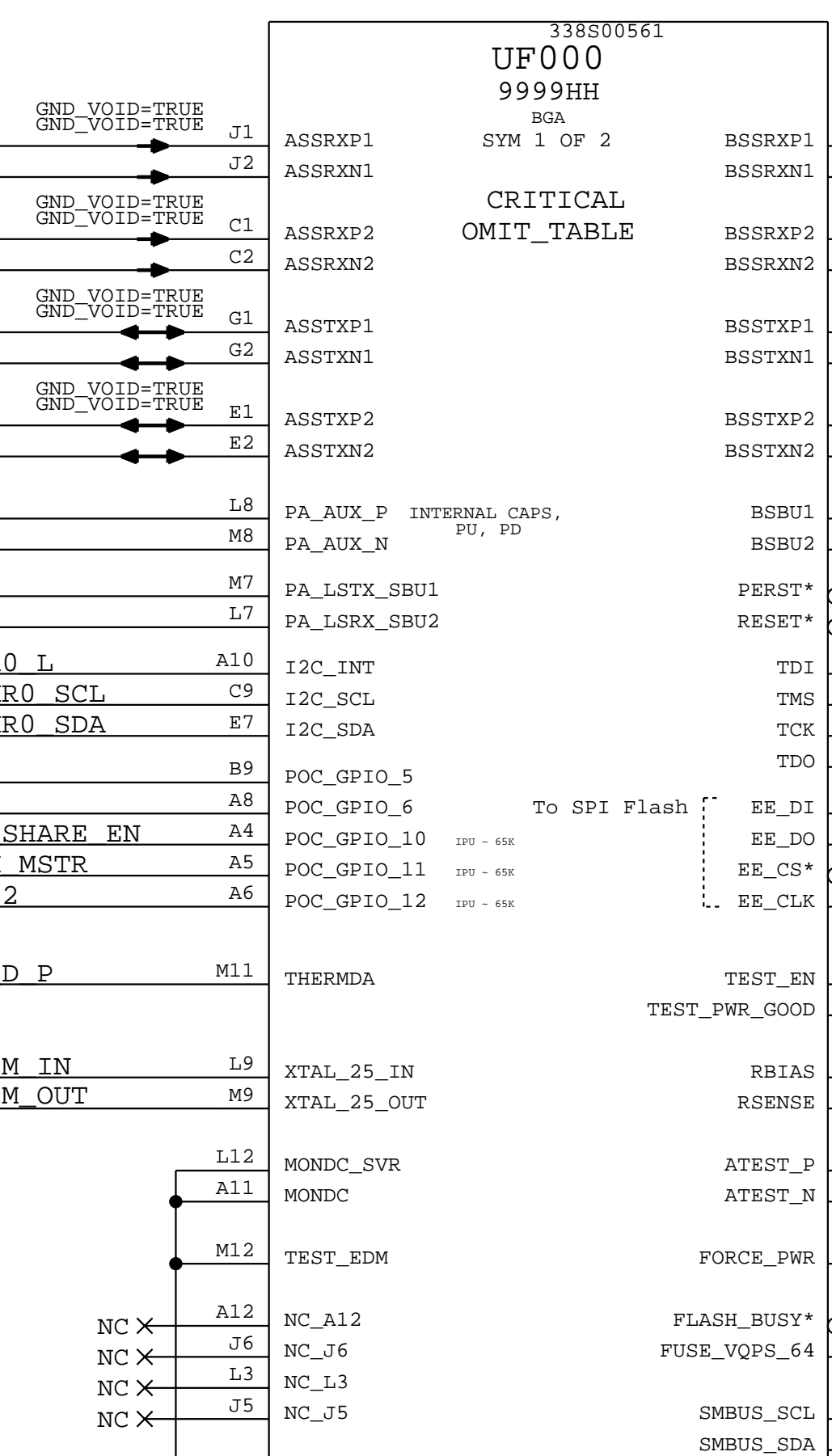
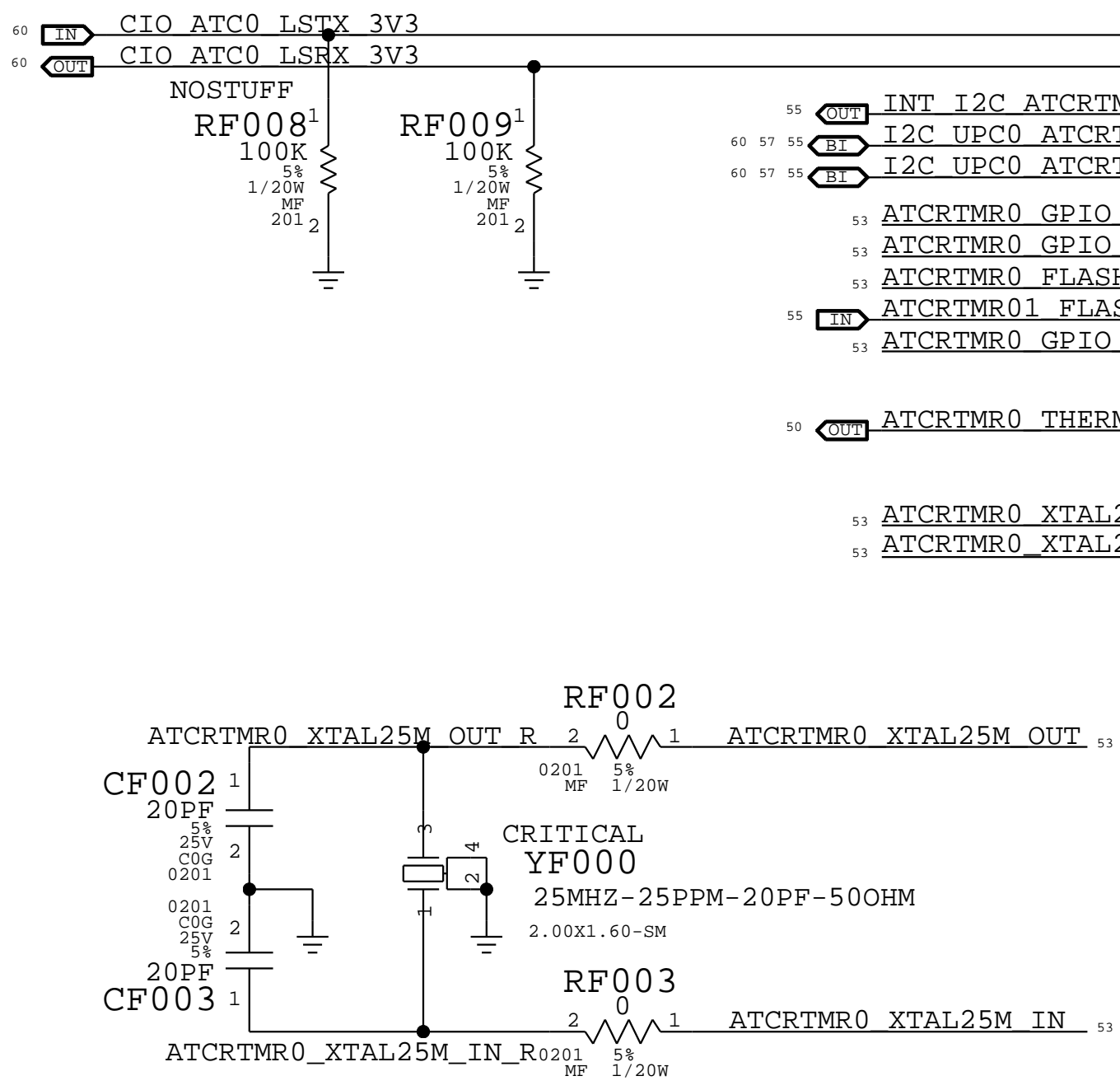
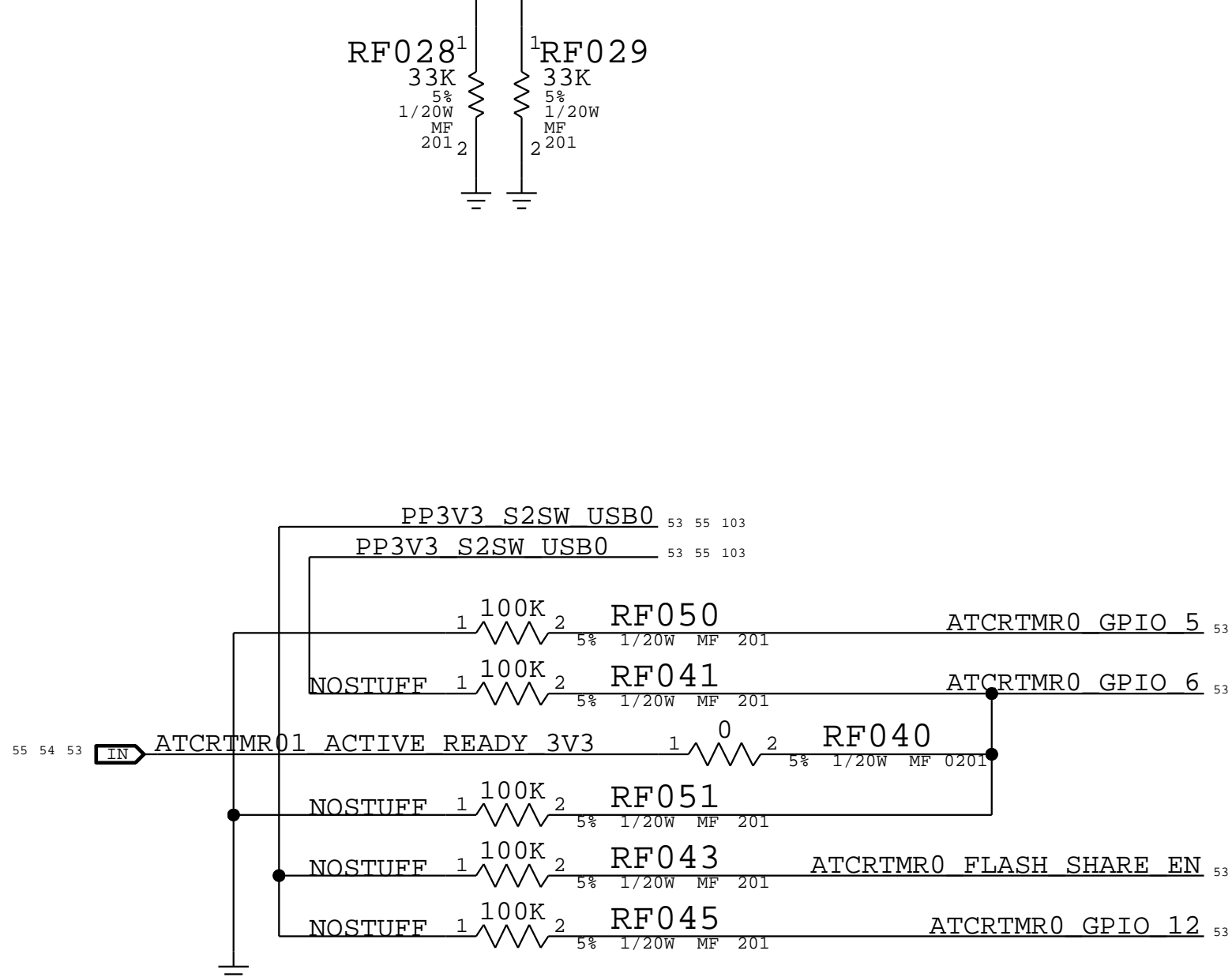
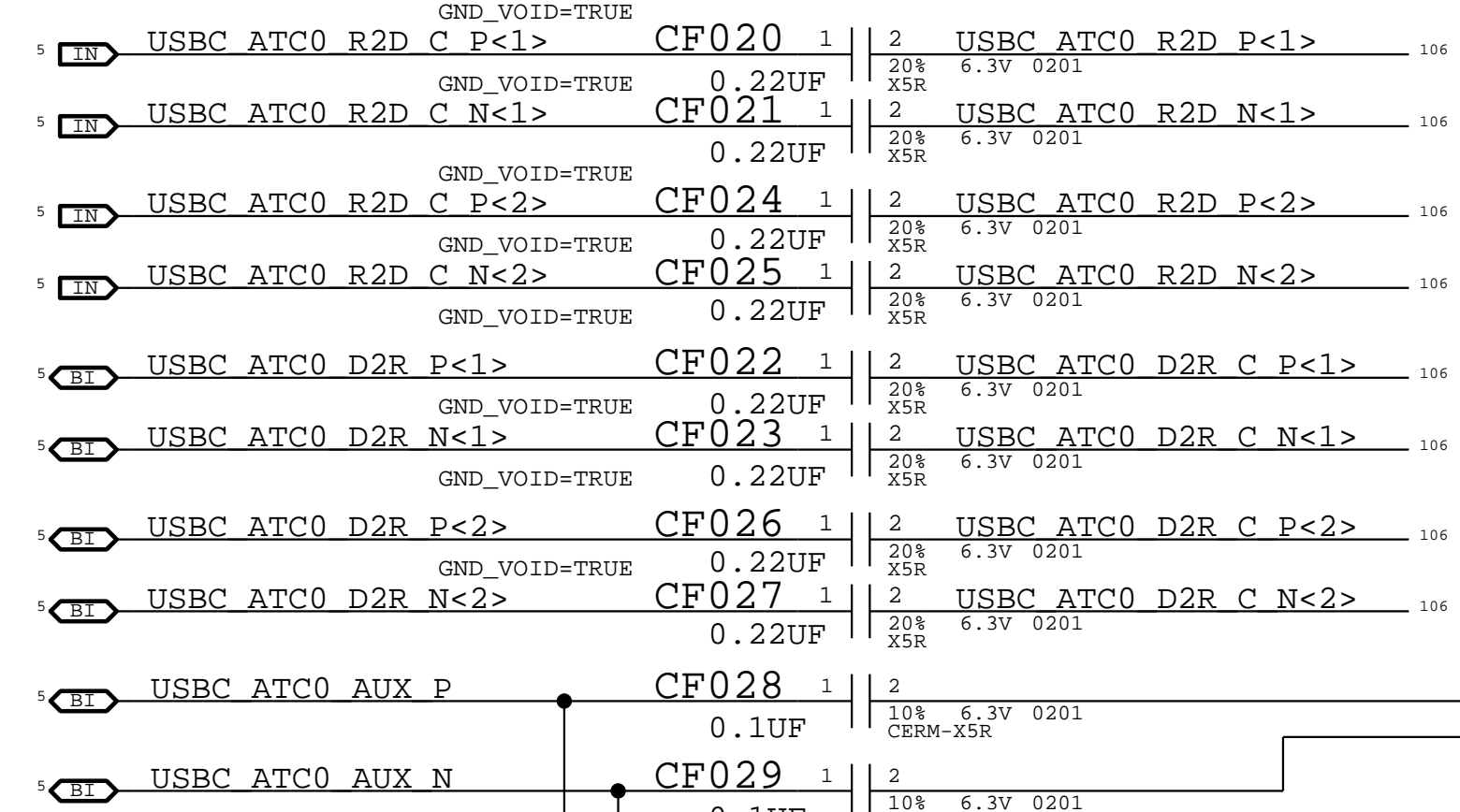
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BOM_COST_GROUP=FAN

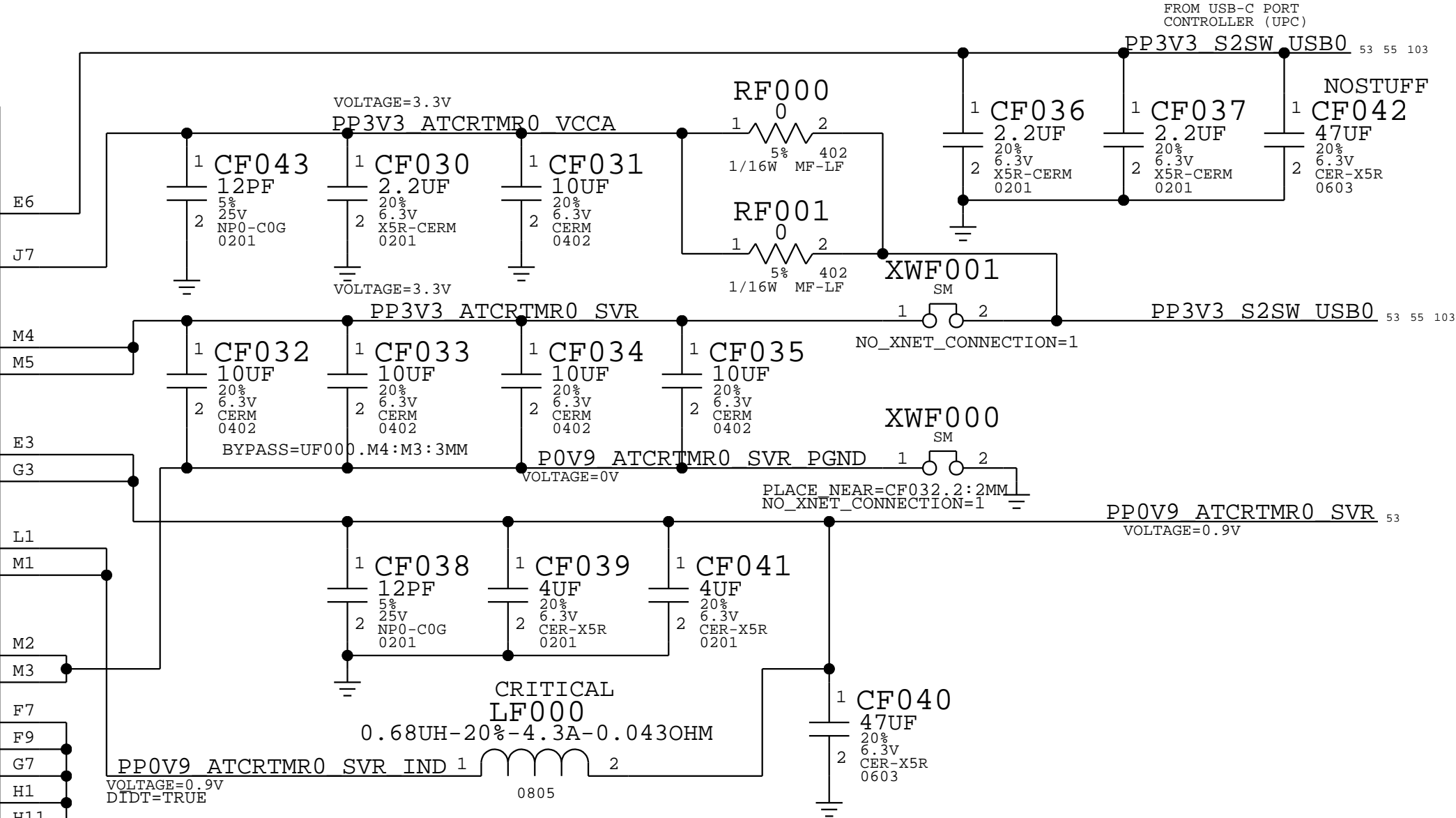
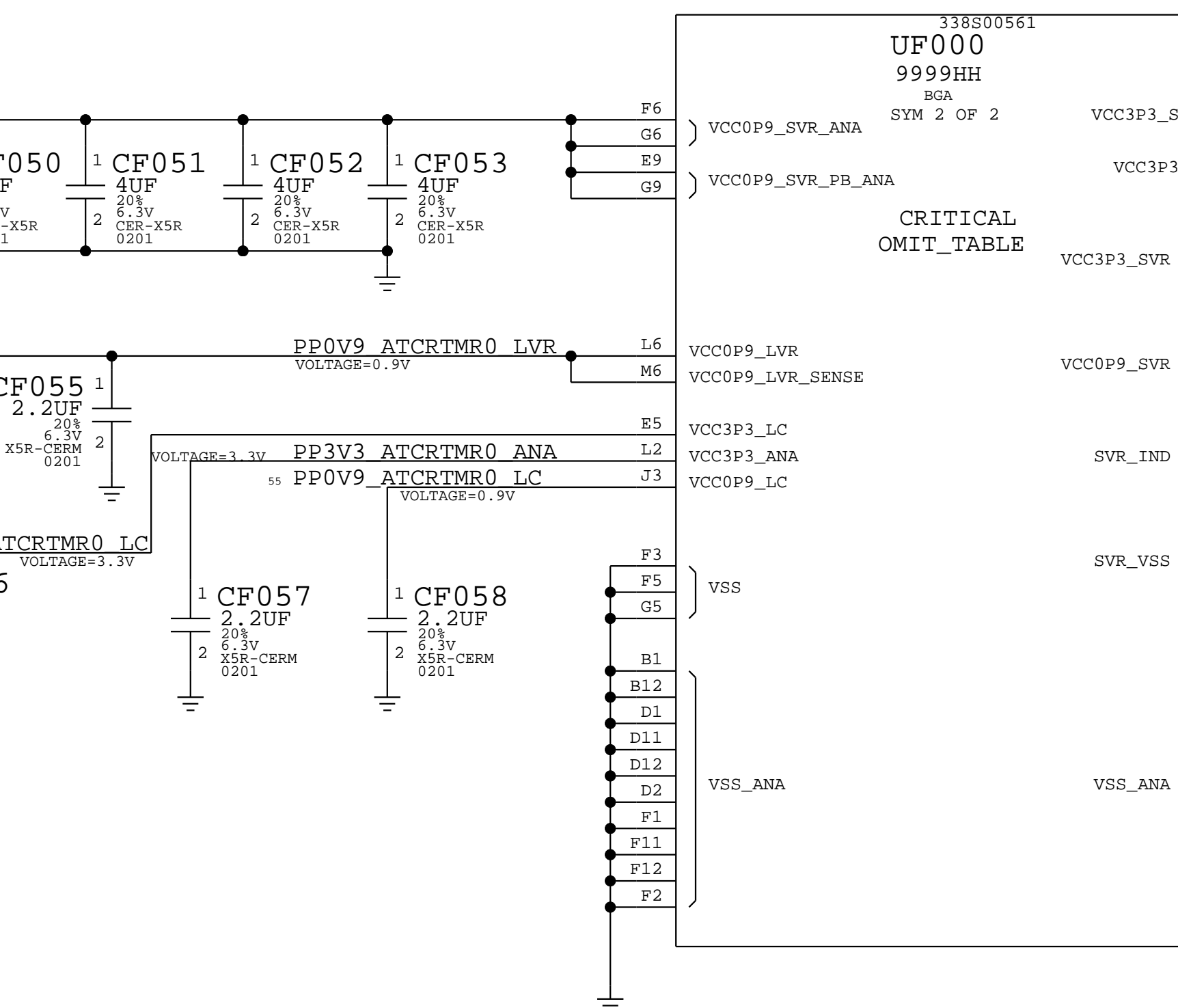
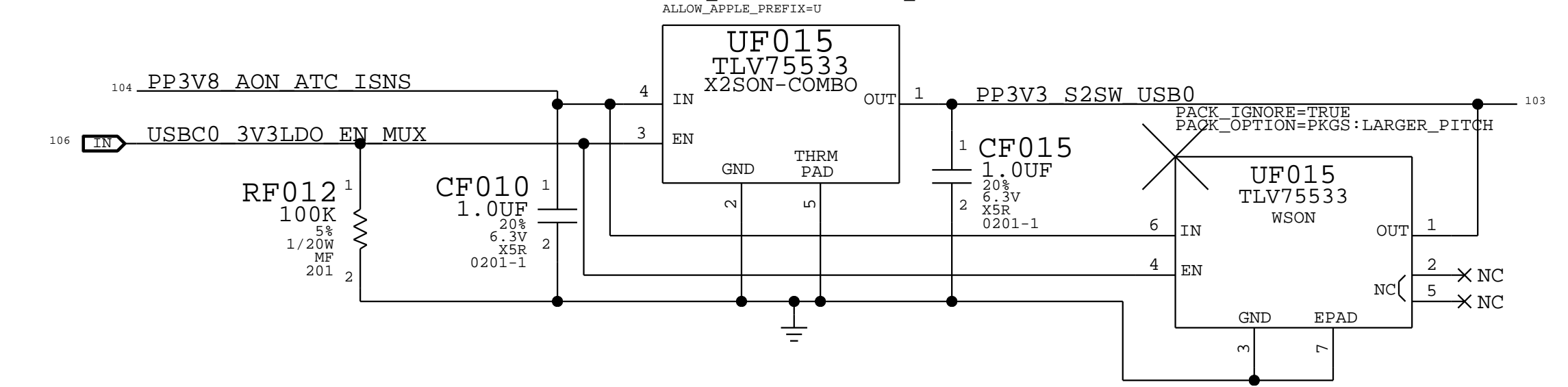
** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING



3.3V LDO



DRAWING NUMBER 051-05399			SIZE D
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PAGE 150 OF 999			SHEET 53 OF 117

Apple Inc.

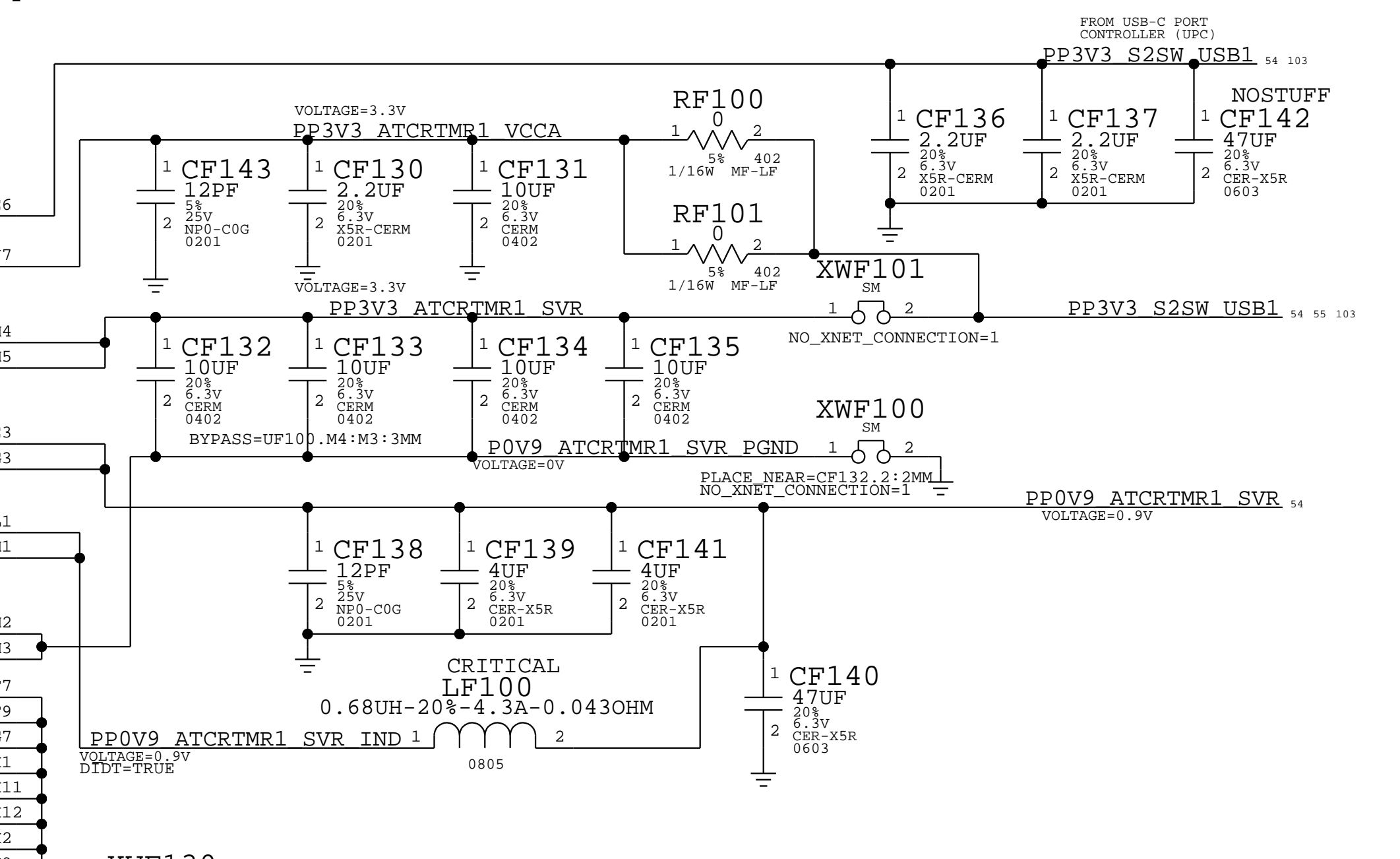
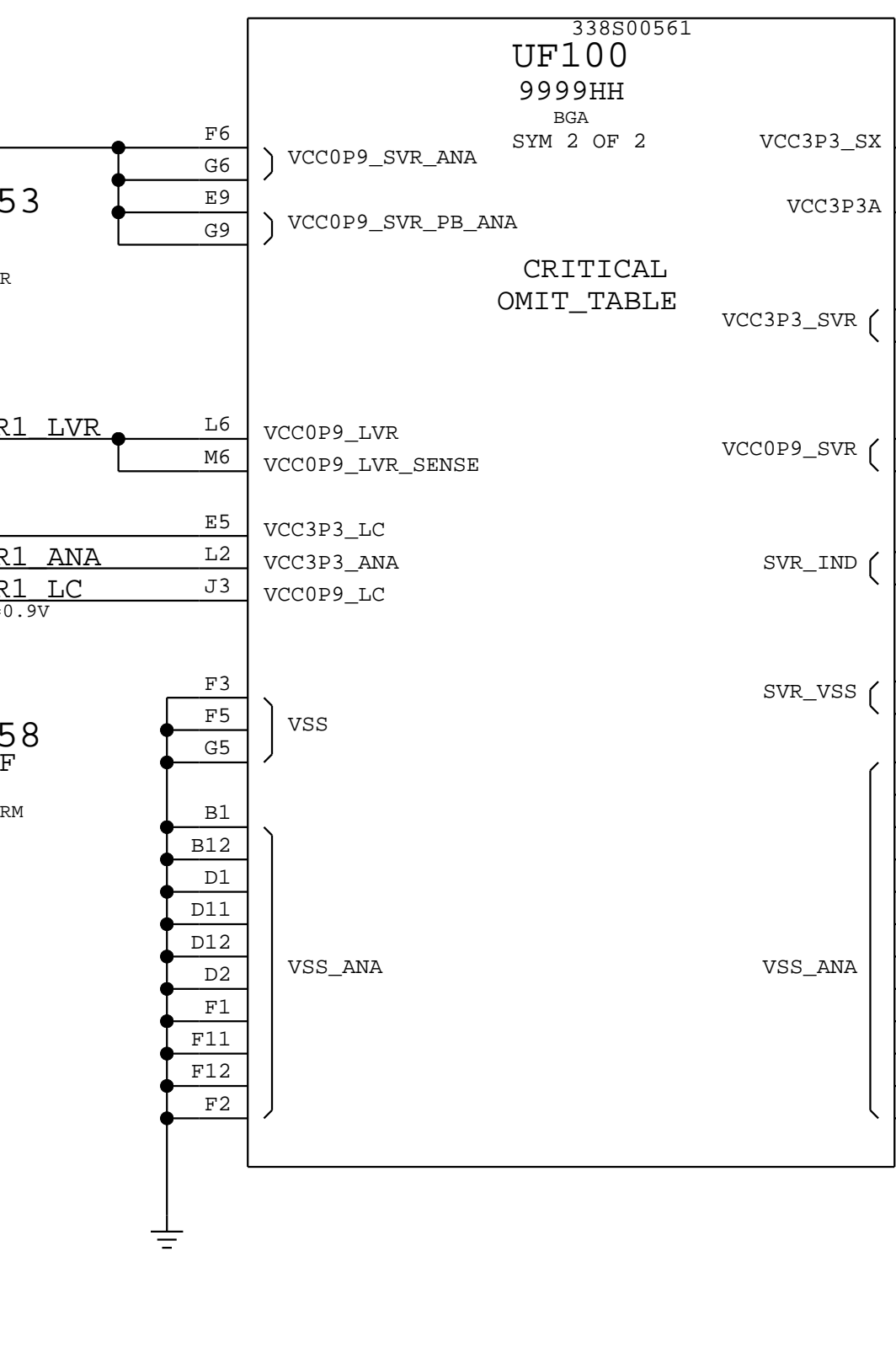
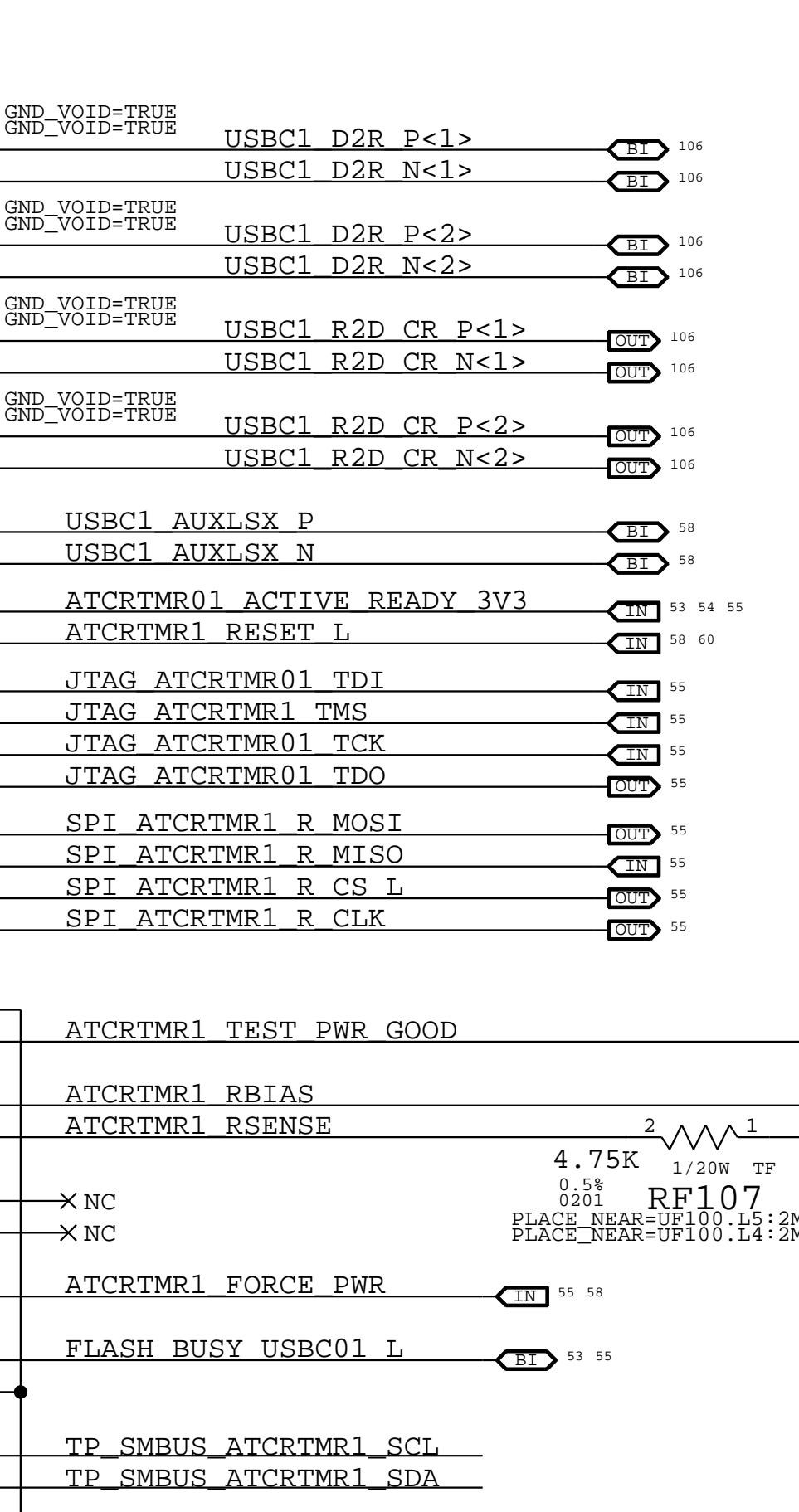
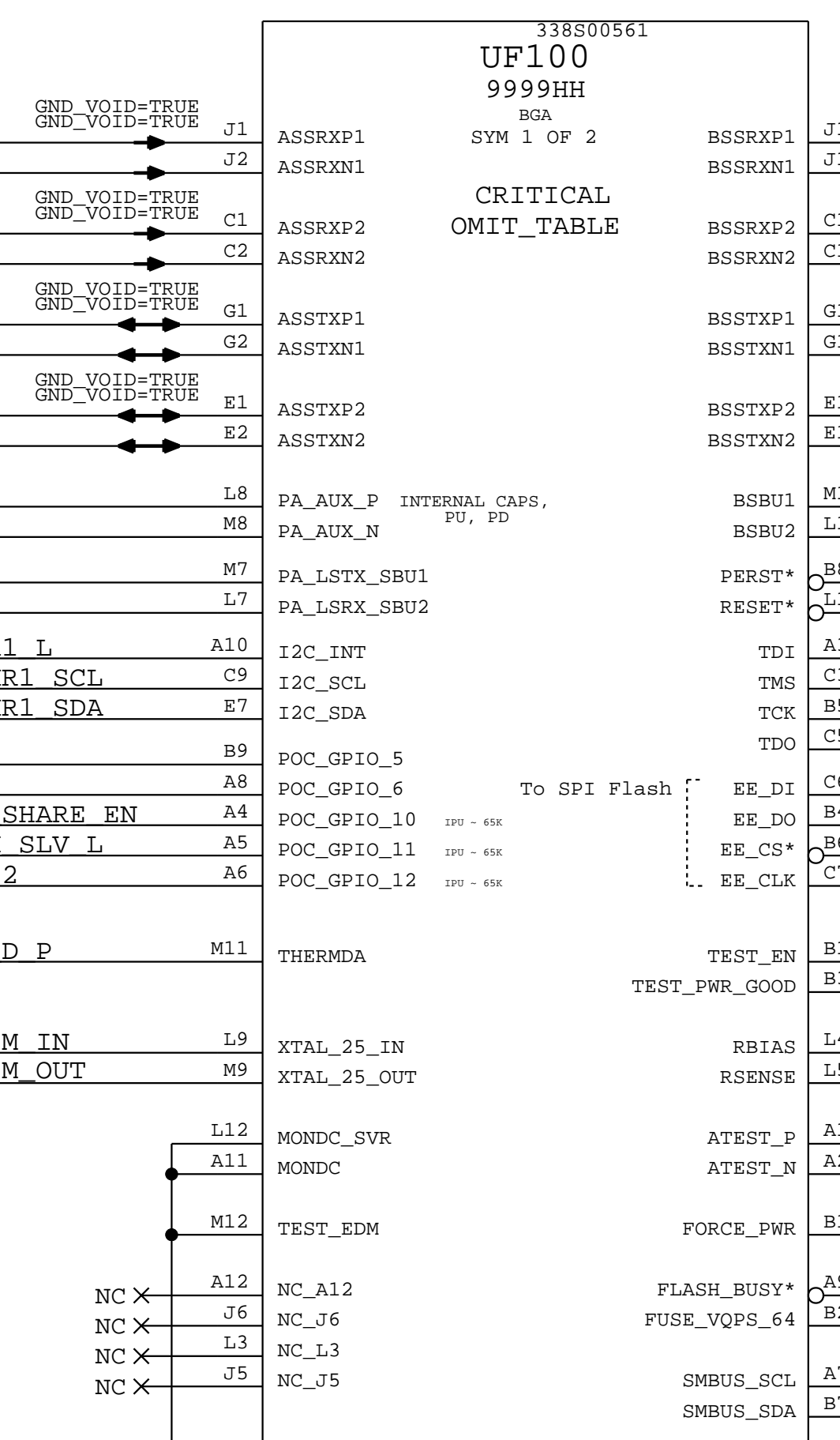
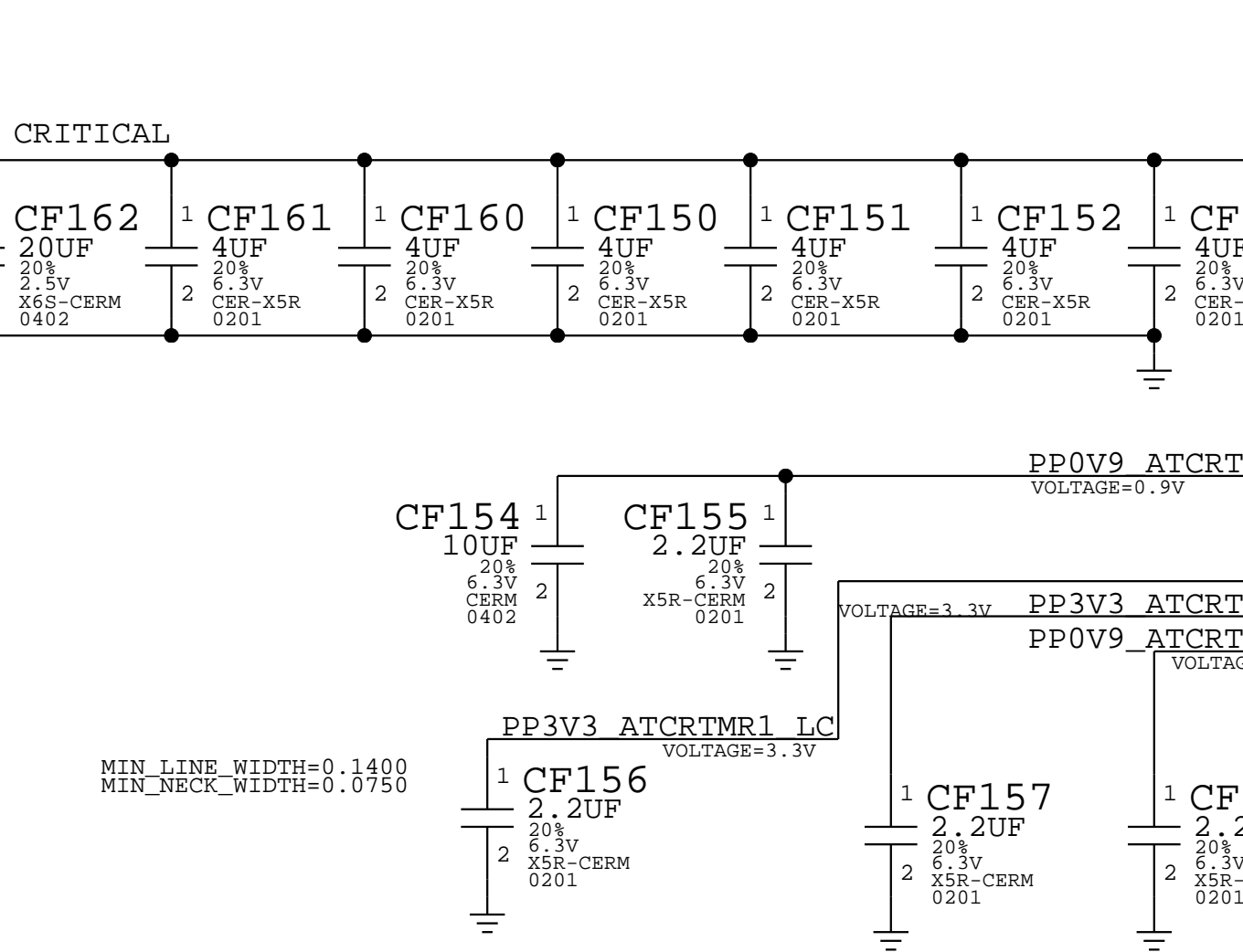
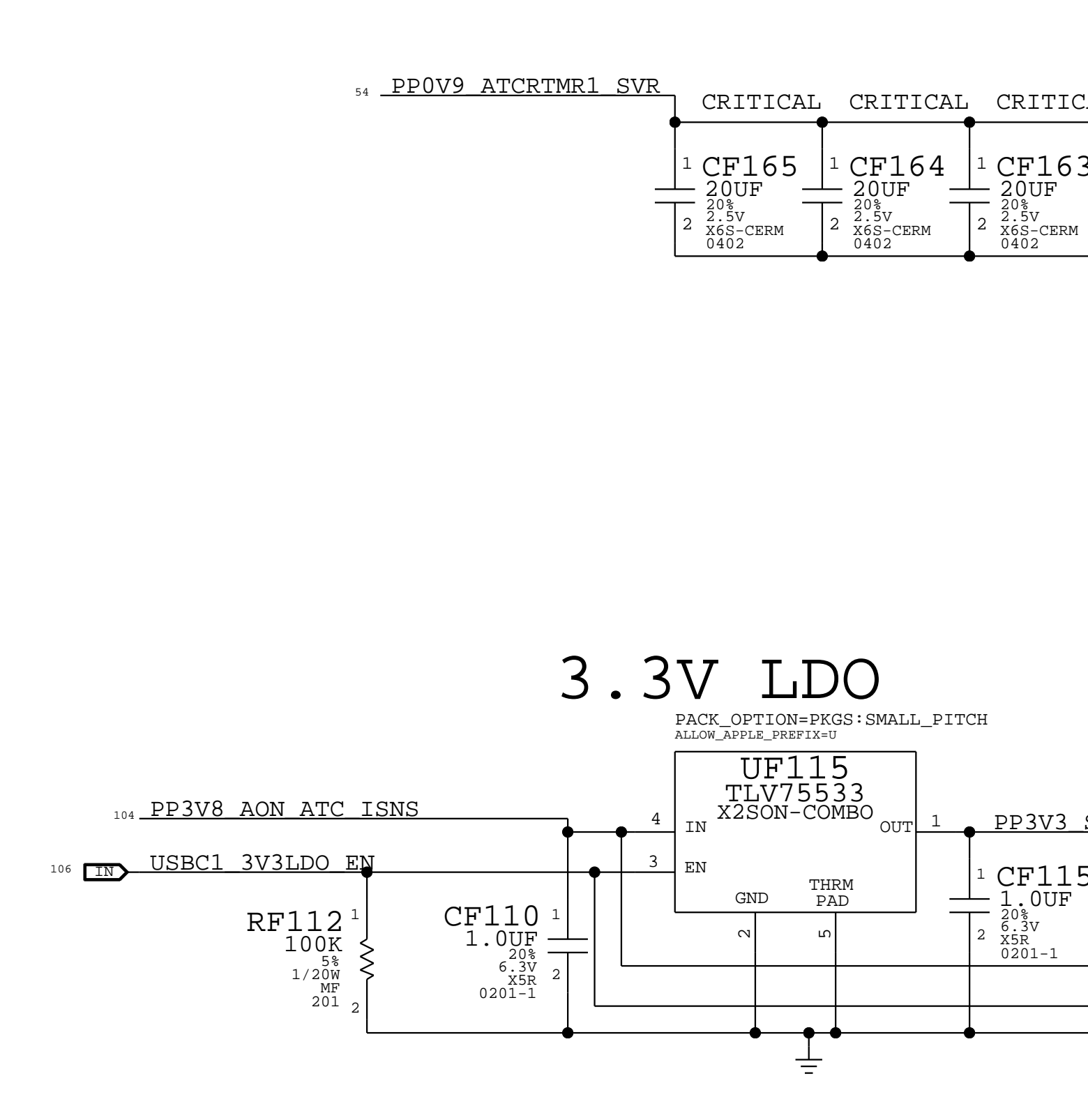
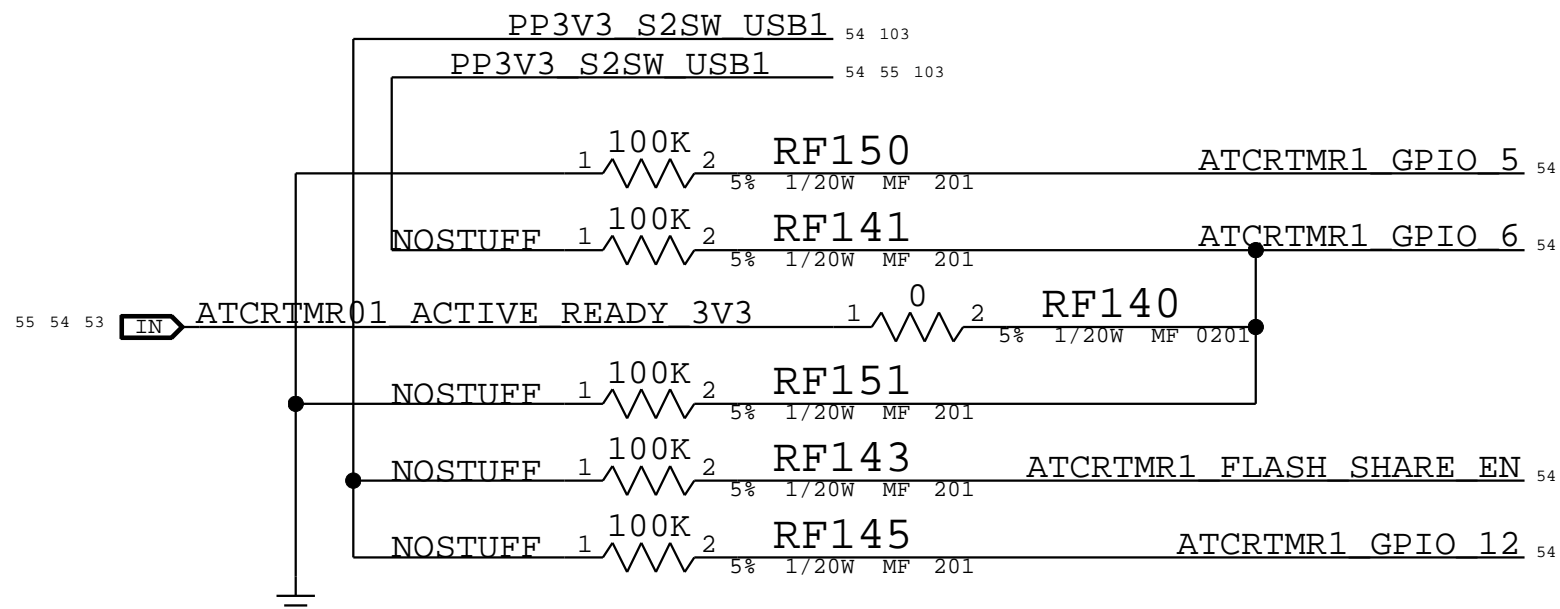
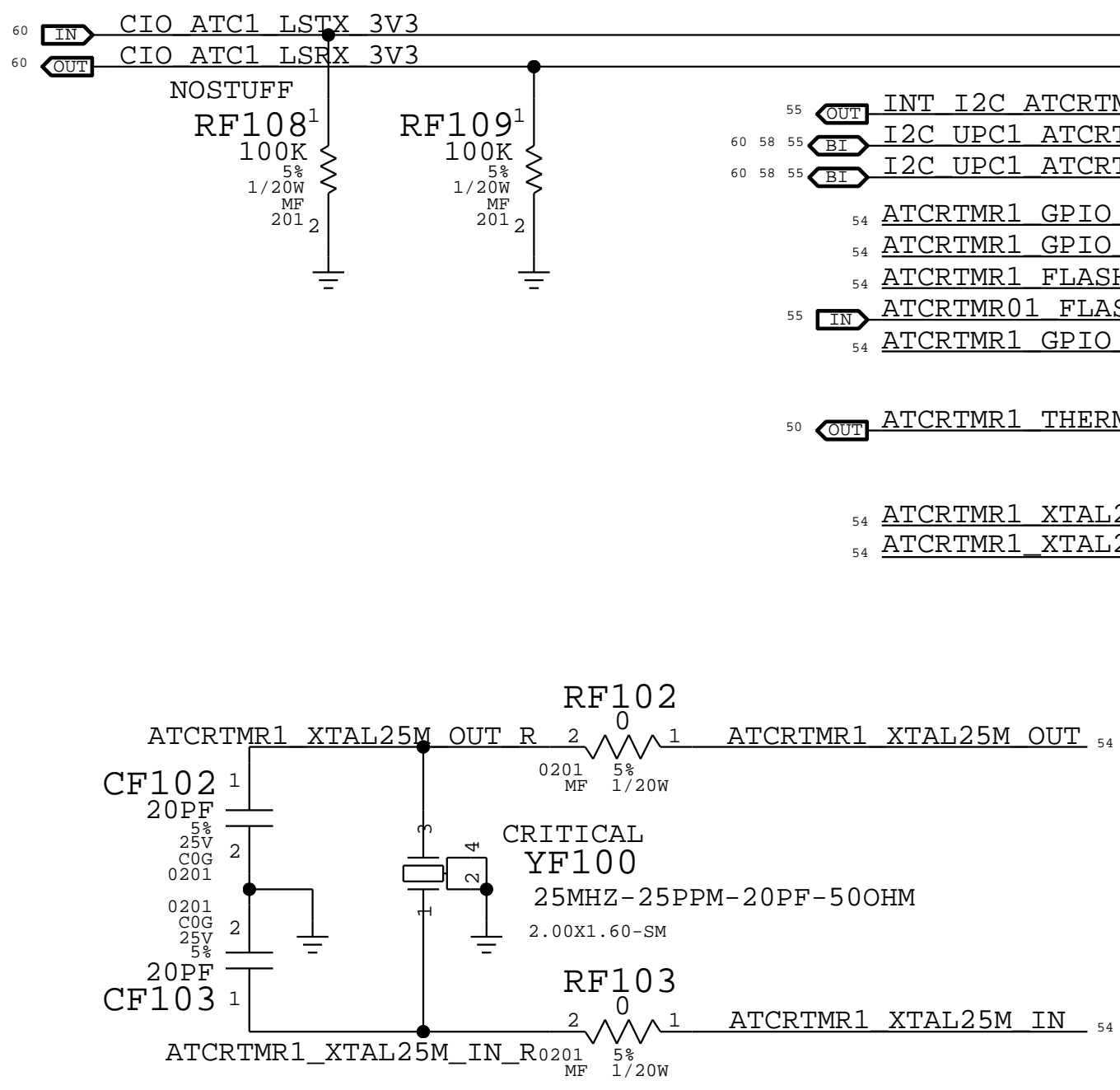
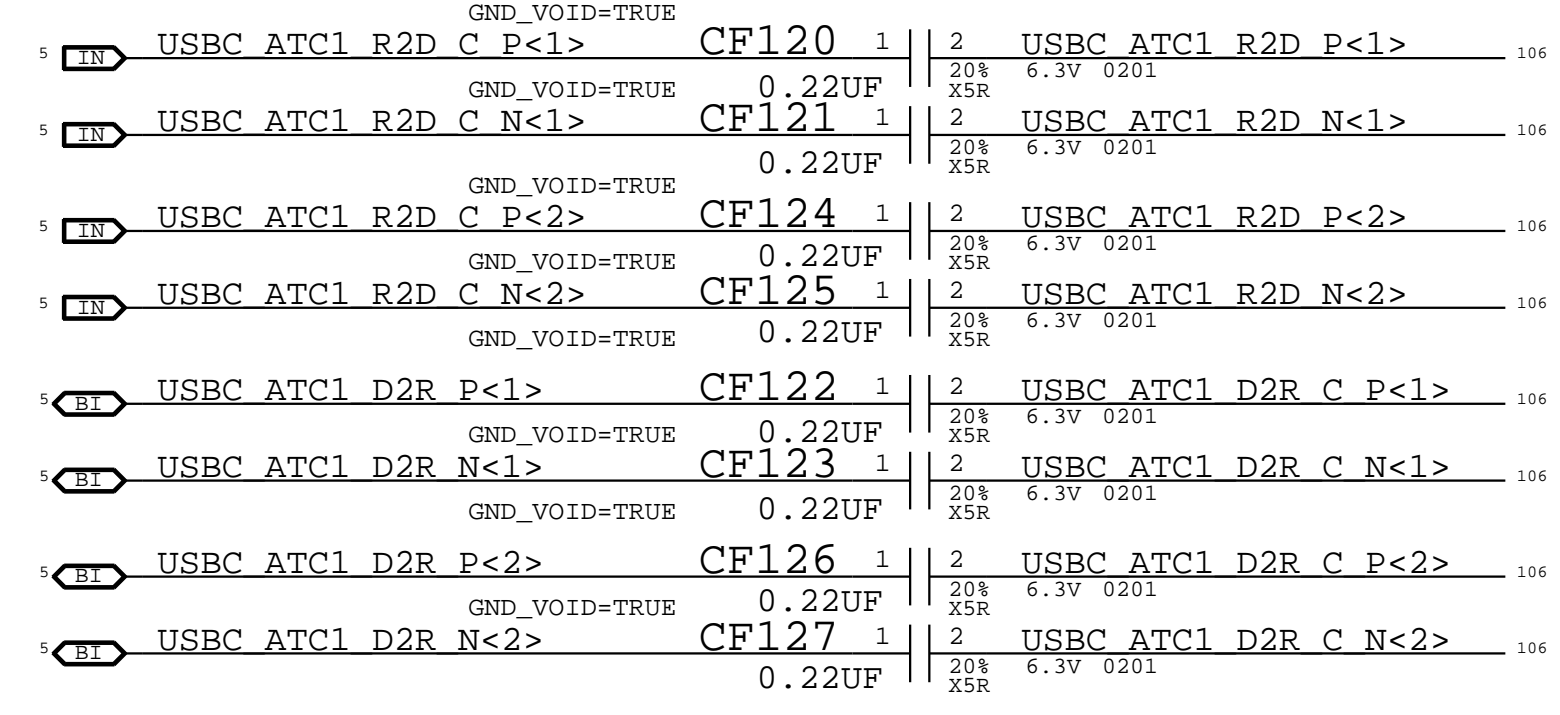
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BOM_COST_GROUP=TBT

** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
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Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING

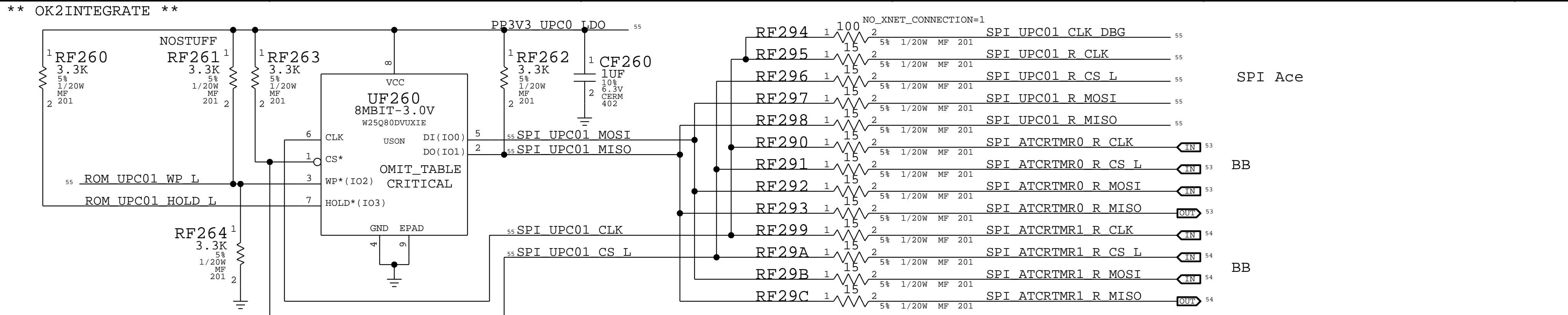


DRAWING NUMBER		051-05399	SIZE	D
REVISION		9.0.0		
BRANCH		dvt-1		
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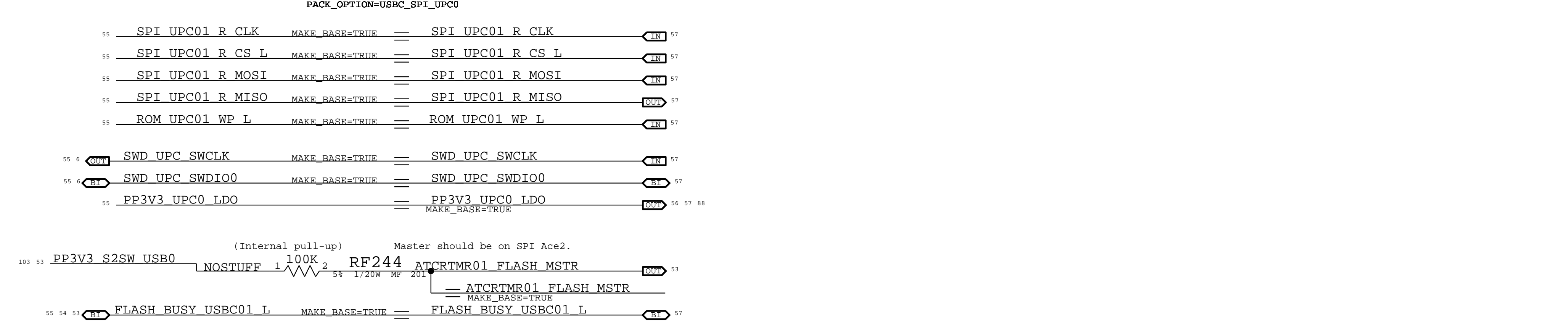
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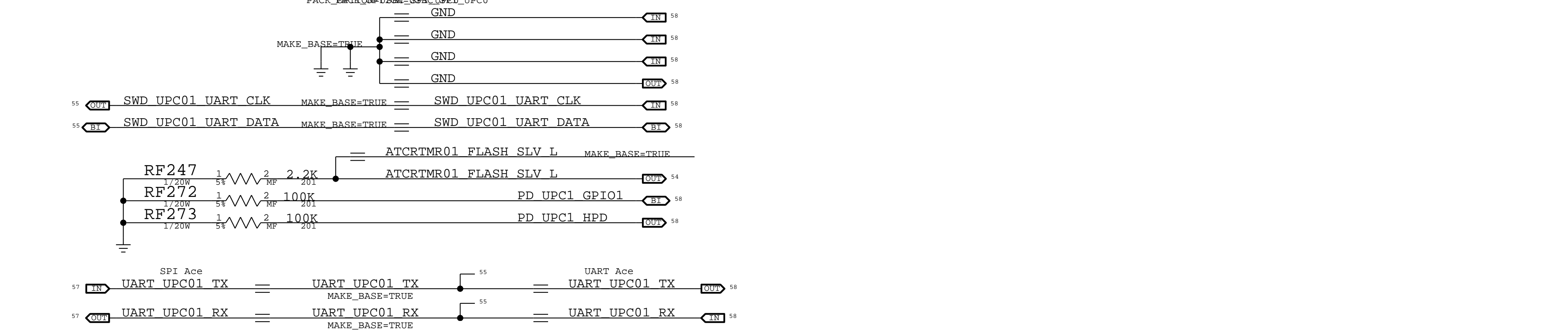
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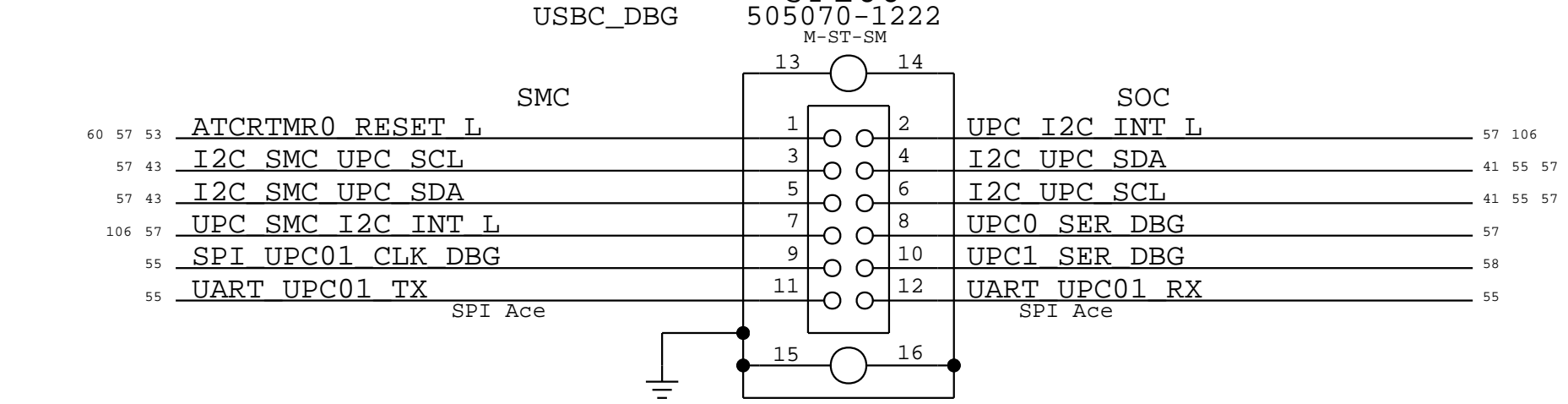
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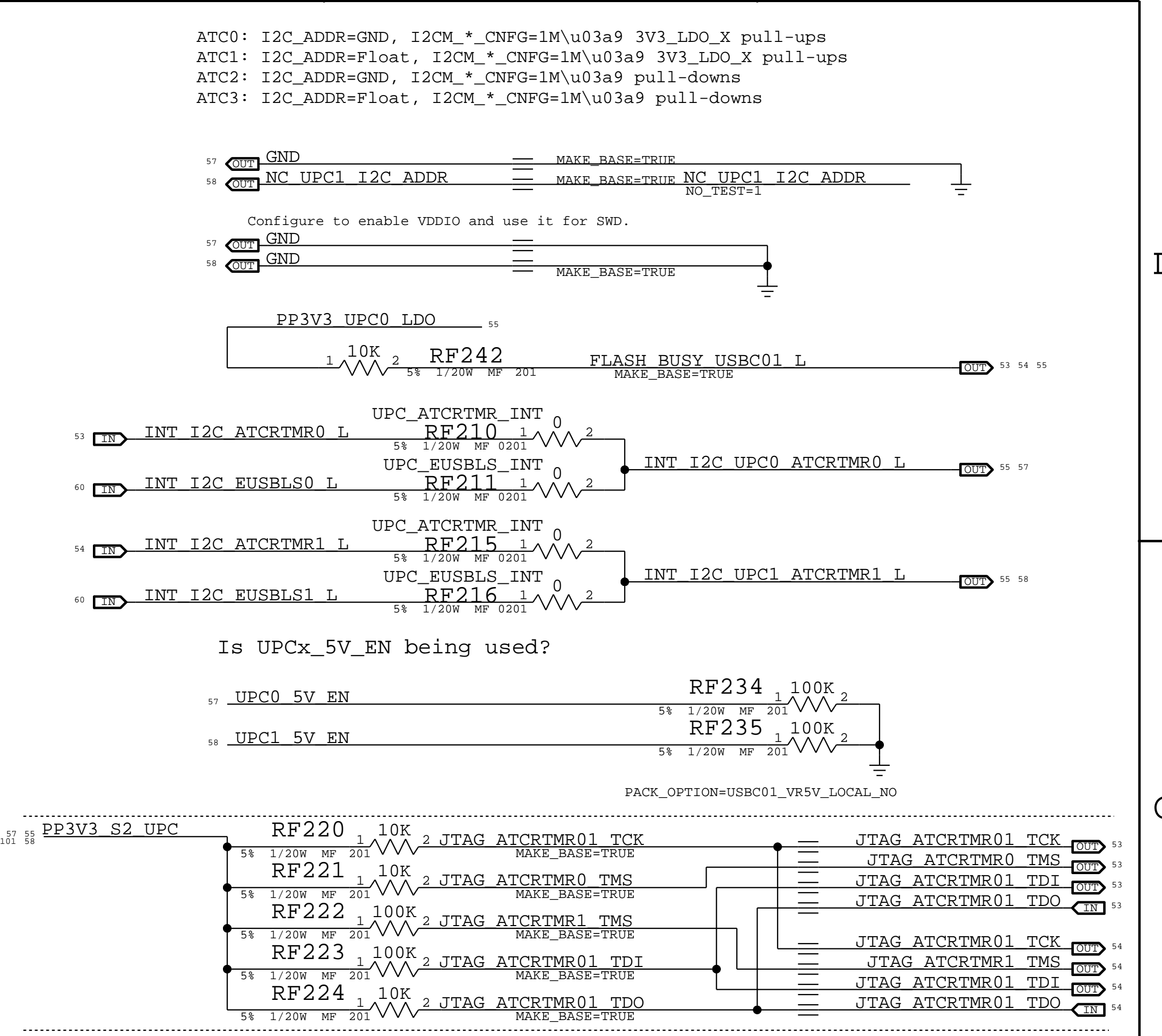
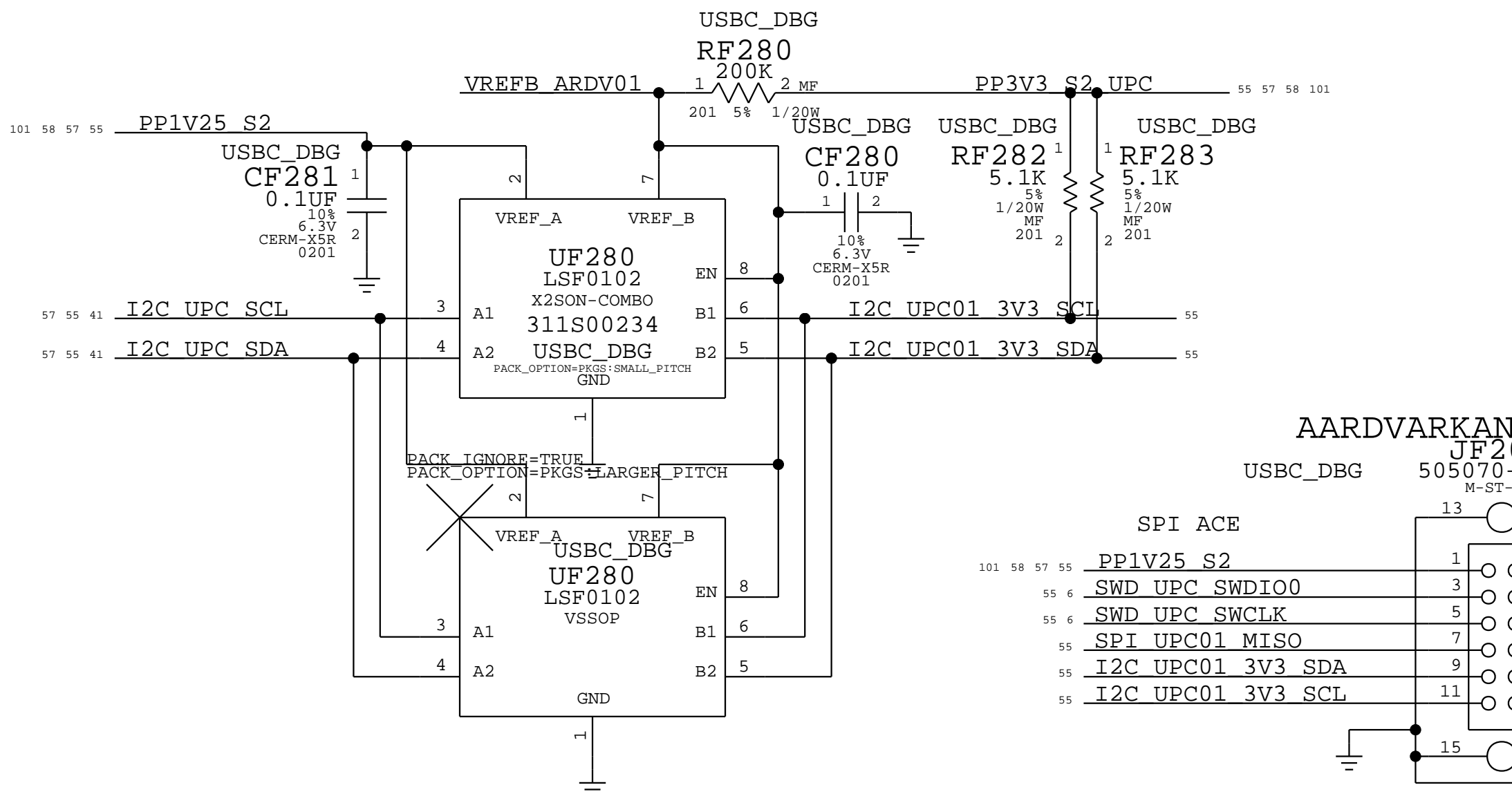
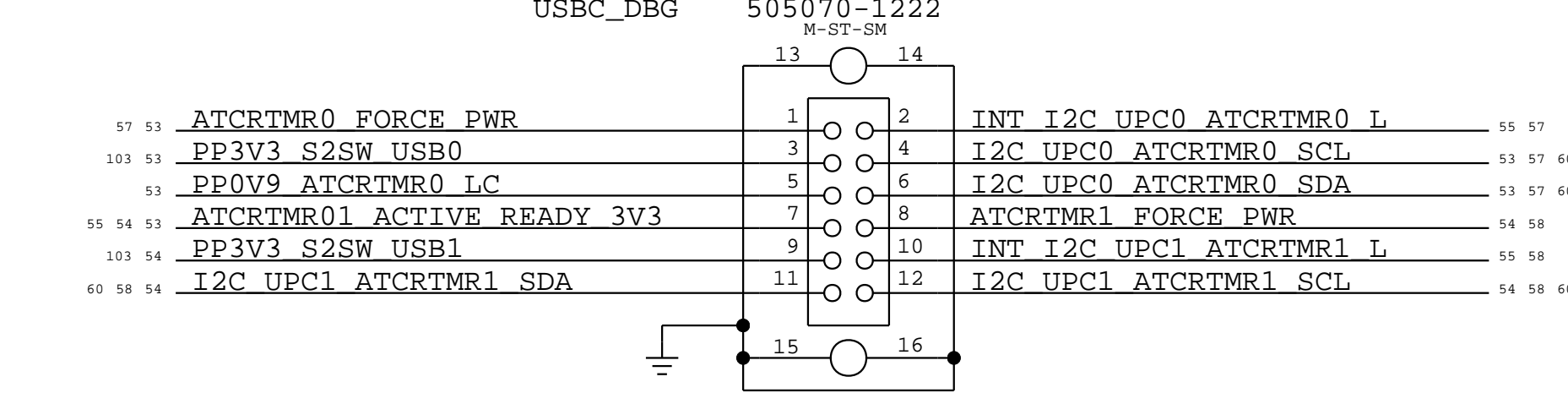
ACE 1 IS UART ACE



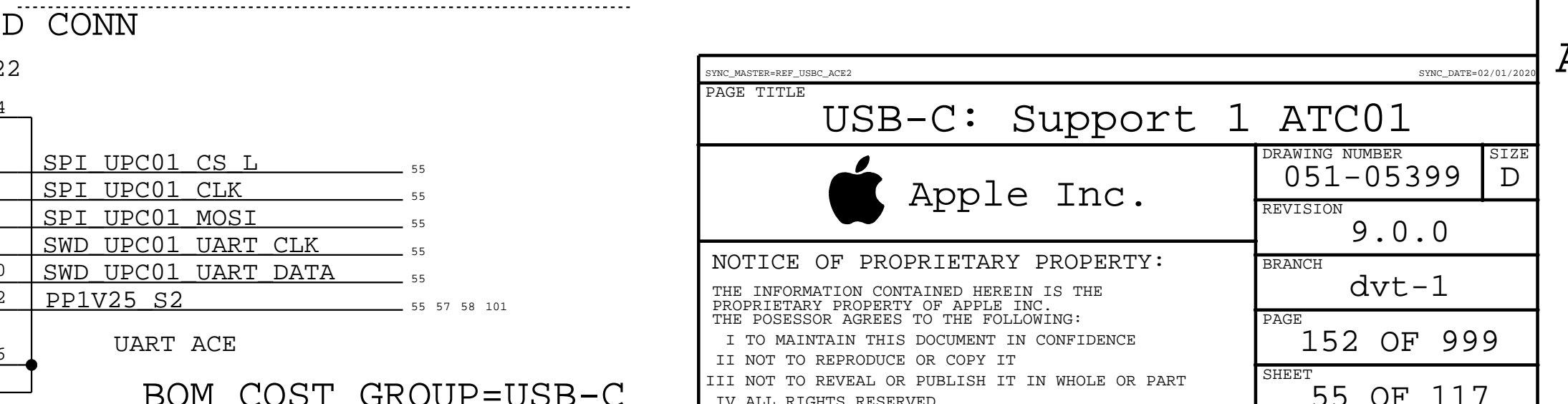
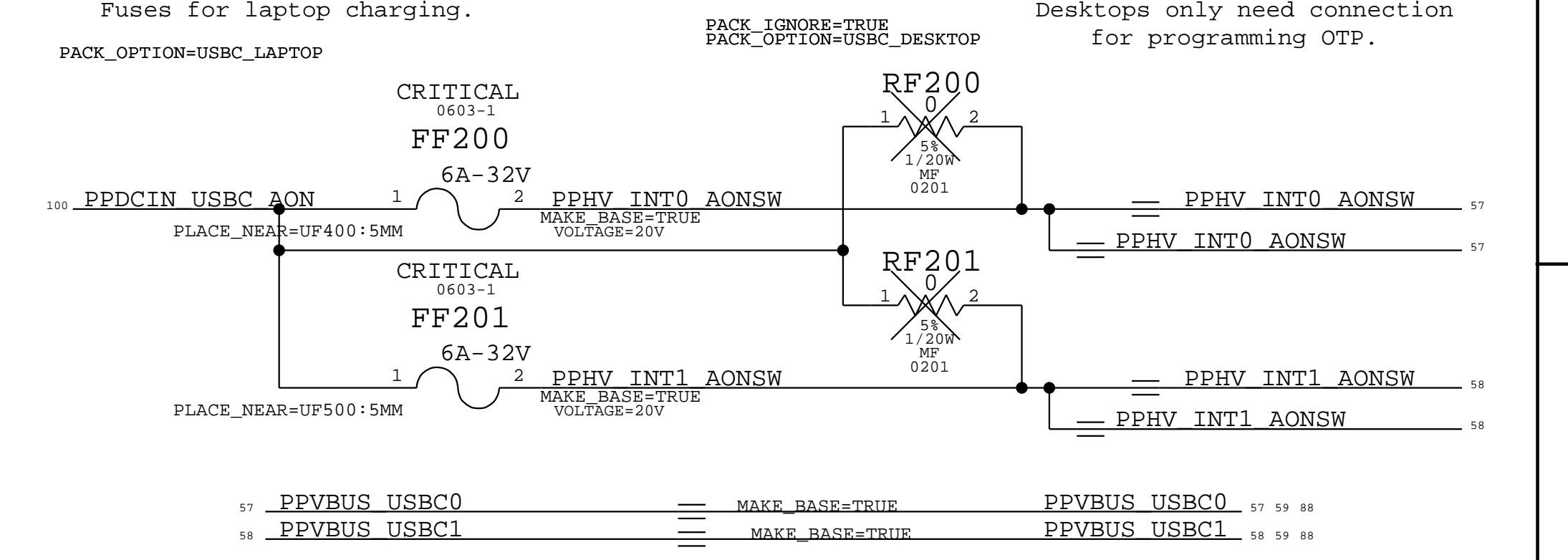
ACE ARKANOID CONN



BRIDGE ARKANOID CONN



HV POWER ALIASES



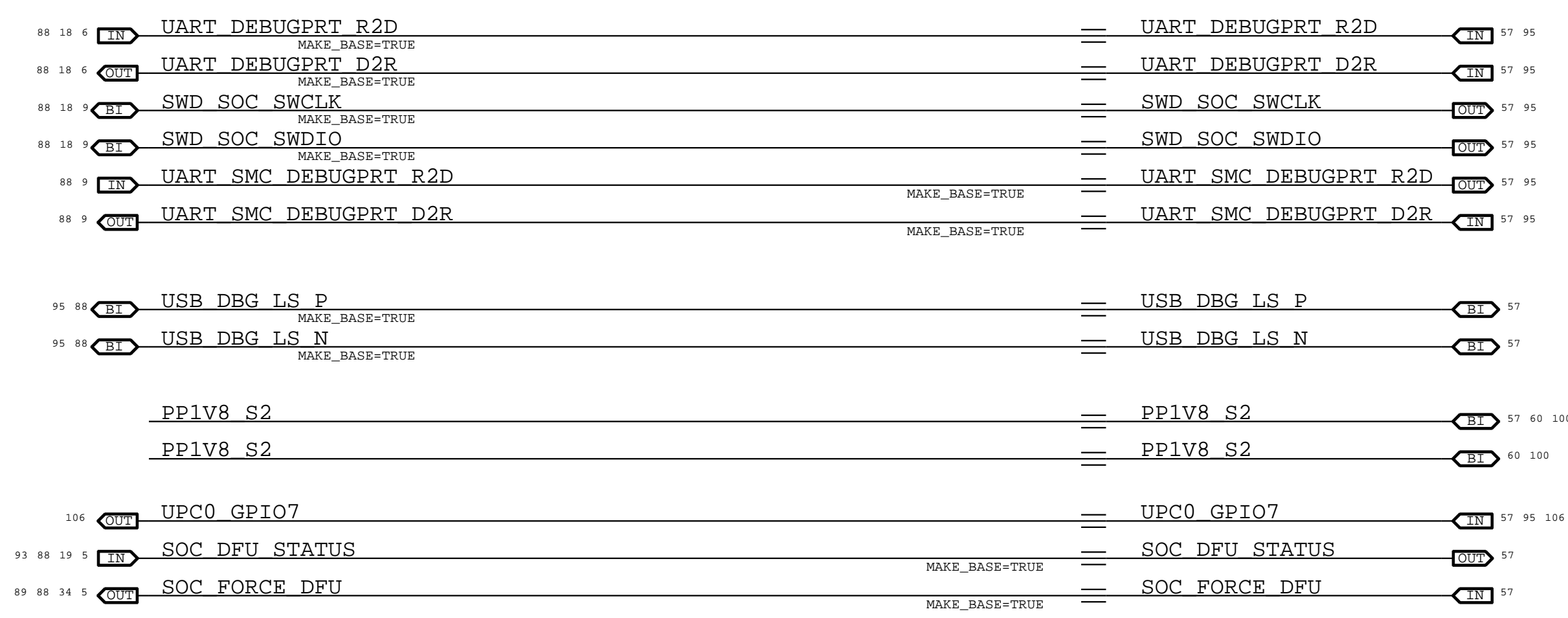
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USB-C: Support 1 ATC01		
DRAWING NUMBER		SIZE
051-05399		D
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SHEET		
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BOM_COST_GROUP=USB-C

** OK2INTEGRATE **

ACE 0 (LEFT REAR) IS DEBUG PORT

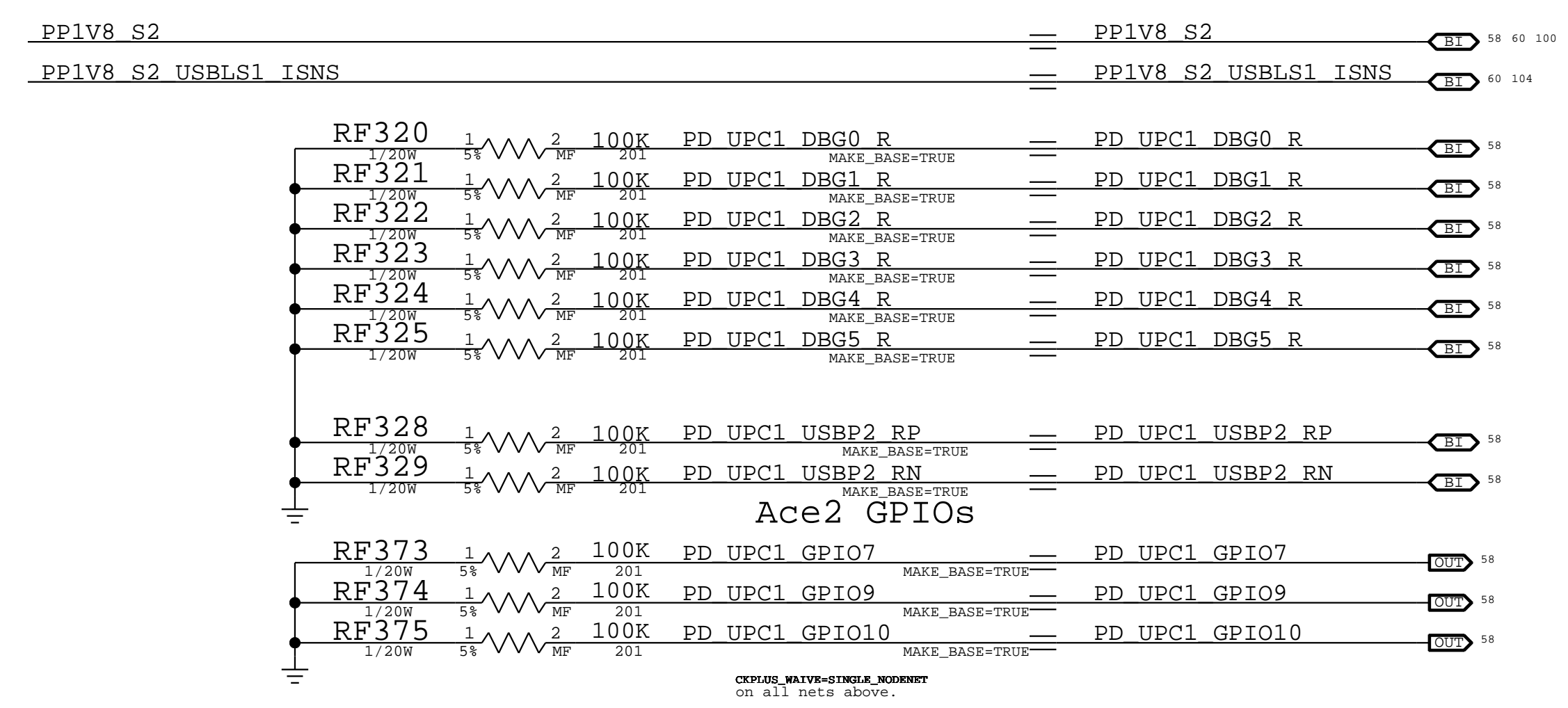
PACK_OPTION=USBC_DEBUG_UPCO ATC0 / UPCO / RTMR0



Main Debug Port

ACE 1 IS NON-DEBUG PORT

PACK_OPTION=USBC_DEBUG_UPCO ATC1 / UPC1 / RTMR1

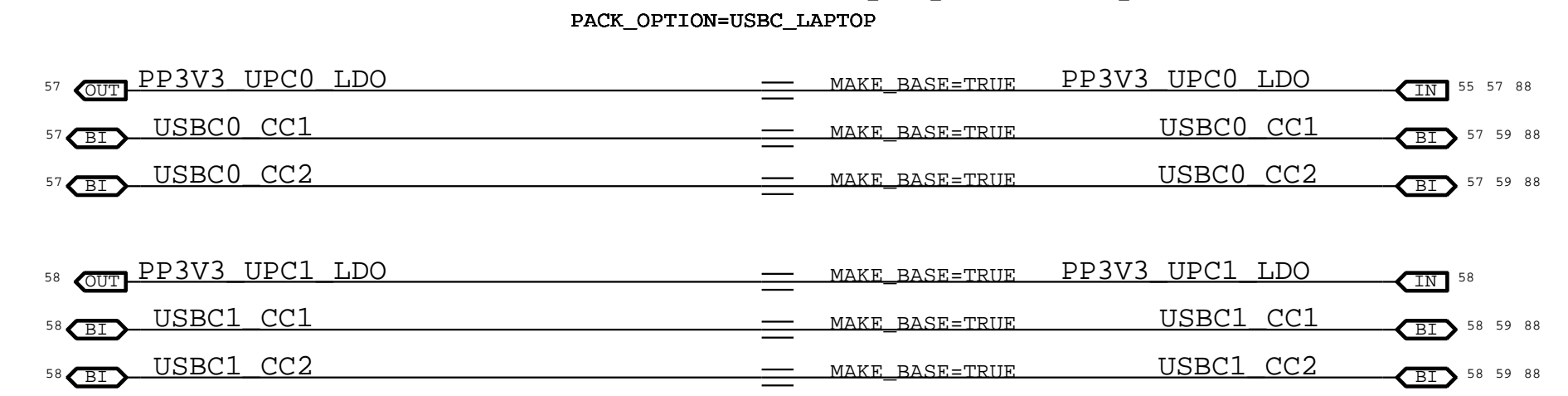


Non-debug Port

Unused ports



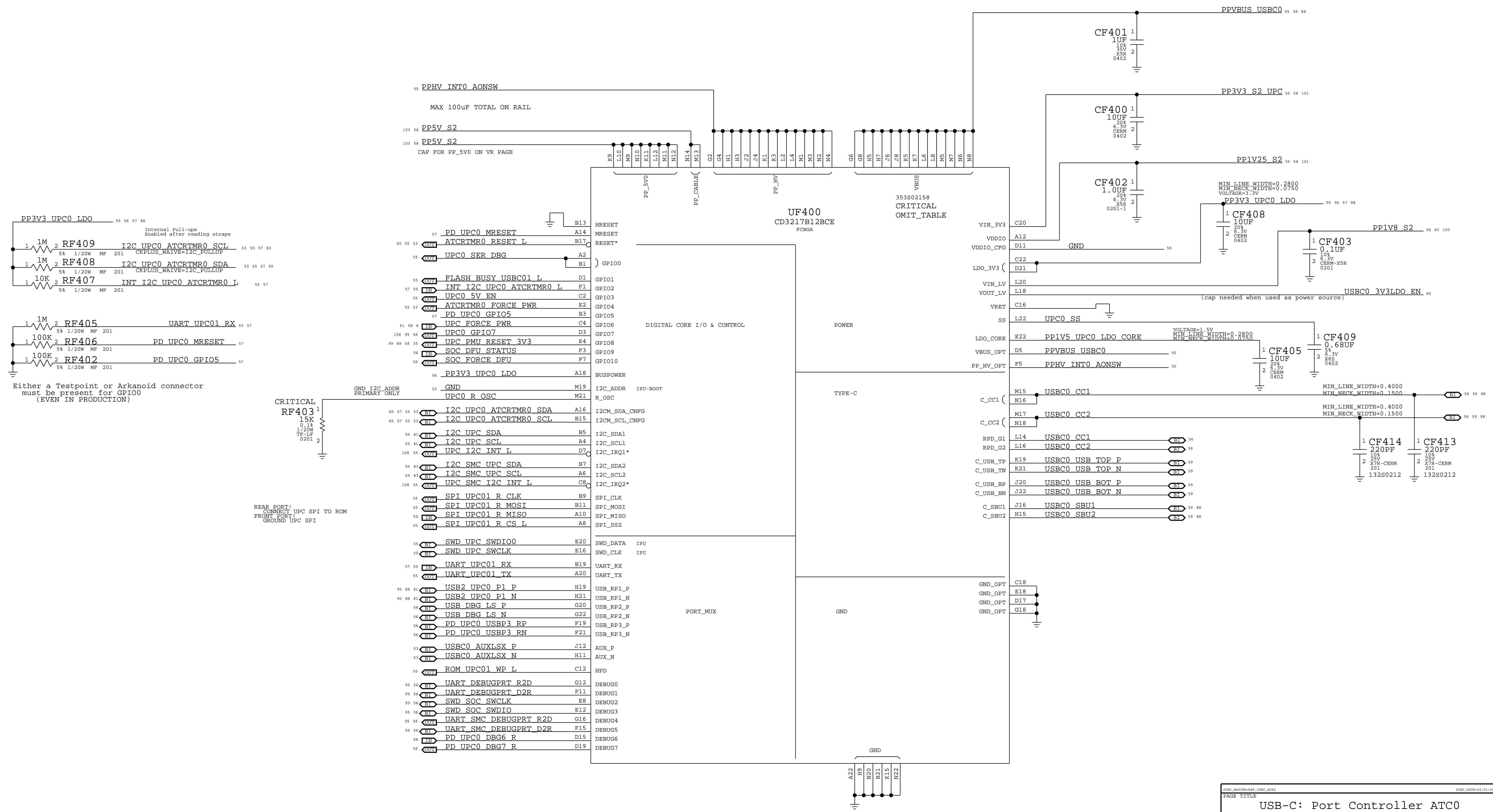
Connections for Laptops (USBC power in)



BOM_COST_GROUP=USB-C

PAGE TITLE		USB-C: Support 2 ATC01	
DRAWING NUMBER	051-05399	SIZE	D
REVISION	9.0.0	BRANCH	dvt-1
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		SHEET	56 OF 117

** OK2INTEGRATE **



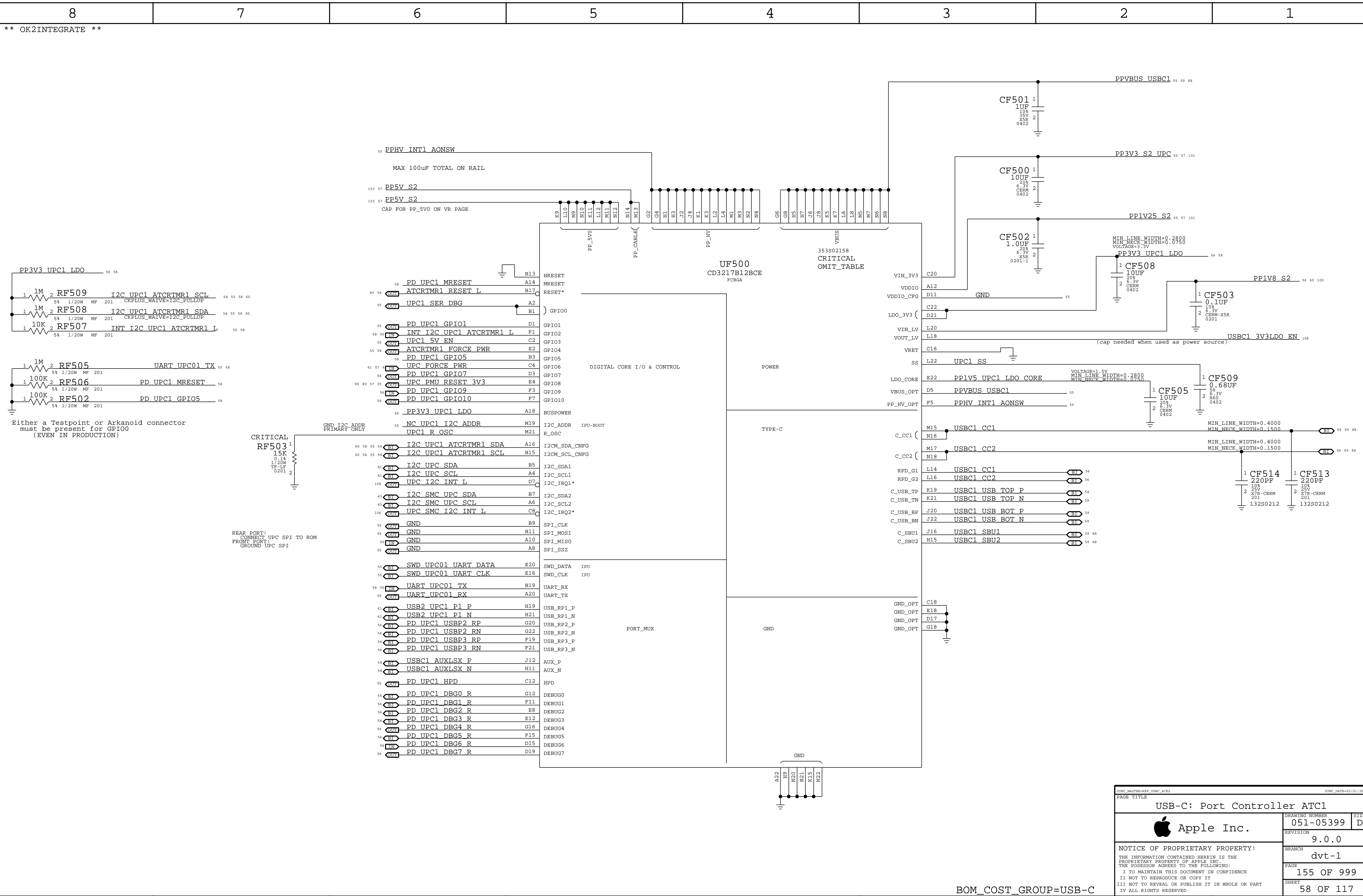
Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

REAR PORT: CONNECT UPC SPI TO ROM FRONT PORT: GROUND UPC SPI

BOM_COST_GROUP=USB-C

PAGE TITLE		DRAWING NUMBER		SIZE
USB-C: Port Controller ATC0		051-05399		D
Apple Inc.		REVISION		9.0.0
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** OK2INTEGRATE **



Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

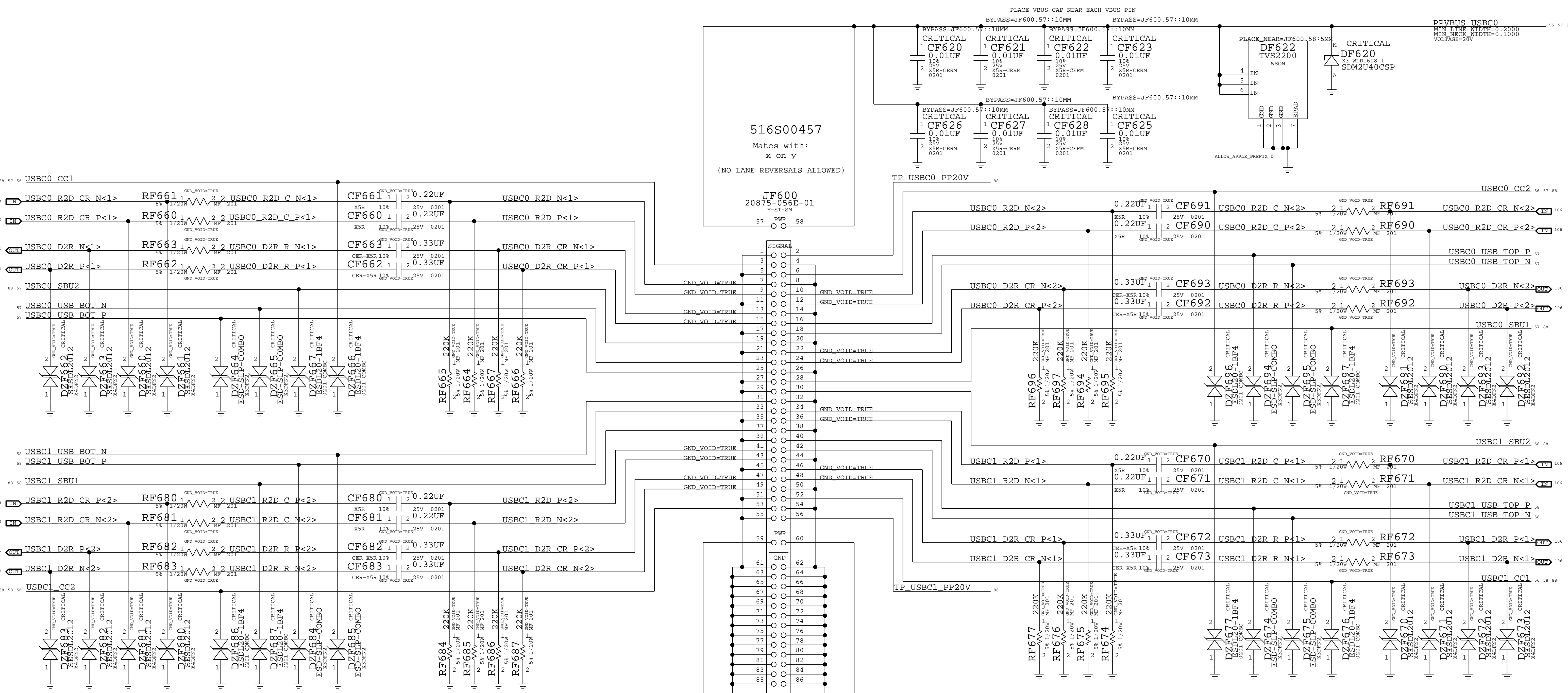
REAR PORT: CONNECT UPC SPI TO ROM FRONT PORT: GROUND UPC SPI

BOM_COST_GROUP=USB-C

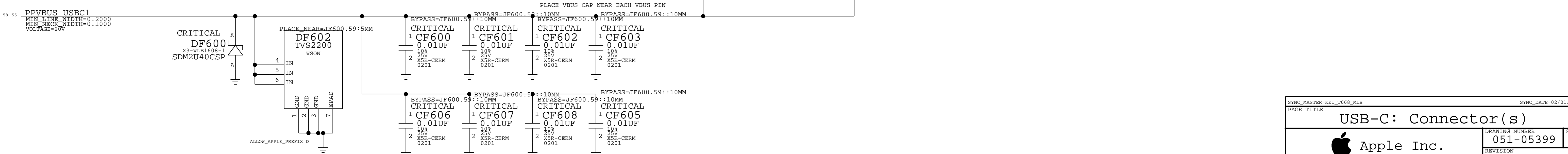
PAGE TITLE		DRAWING NUMBER		SIZE
USB-C: Port Controller ATC1		051-05399		D
Apple Inc.		REVISION		9.0.0
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LEFT REAR PORT (DEBUG PORT)

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK



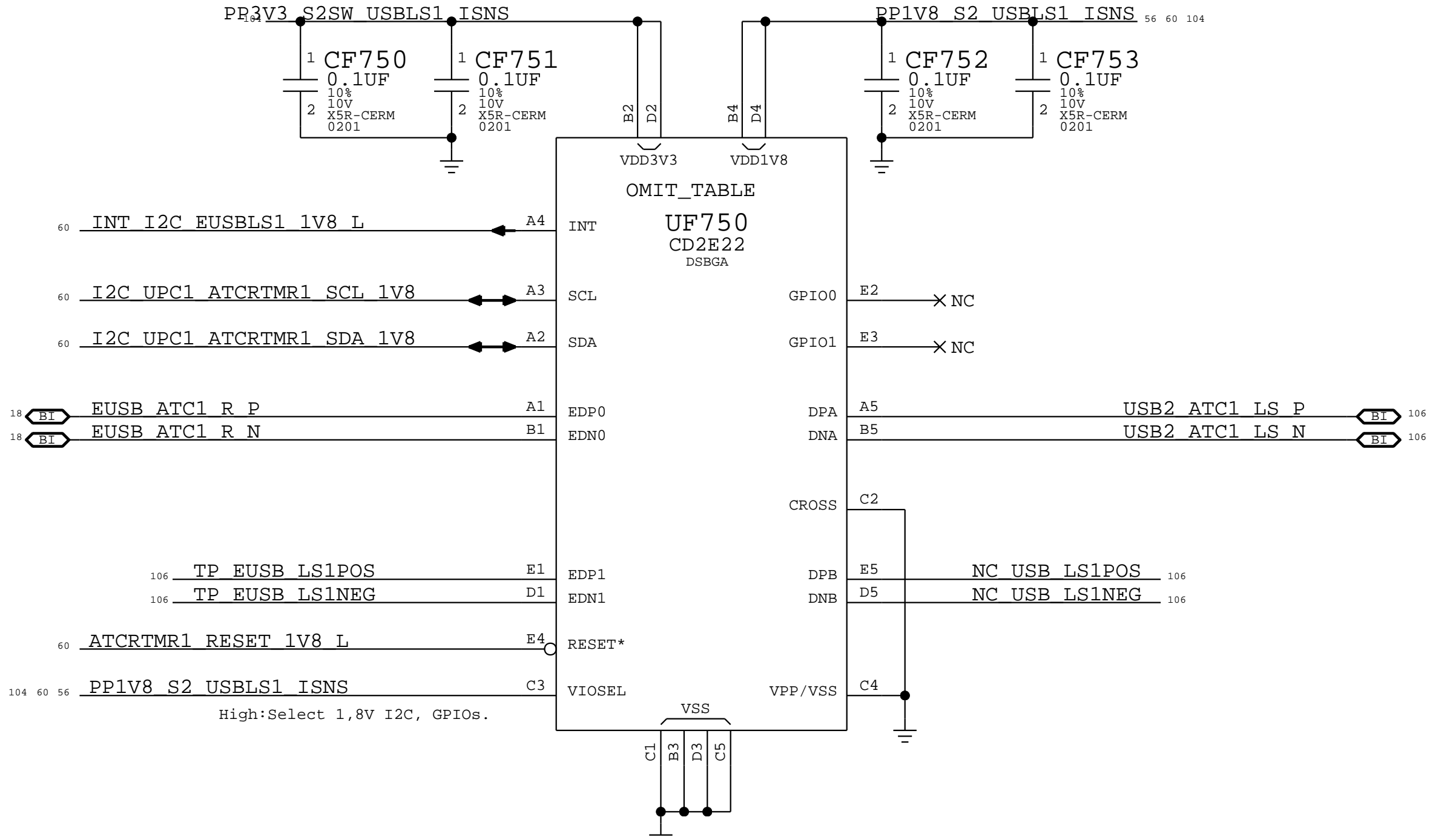
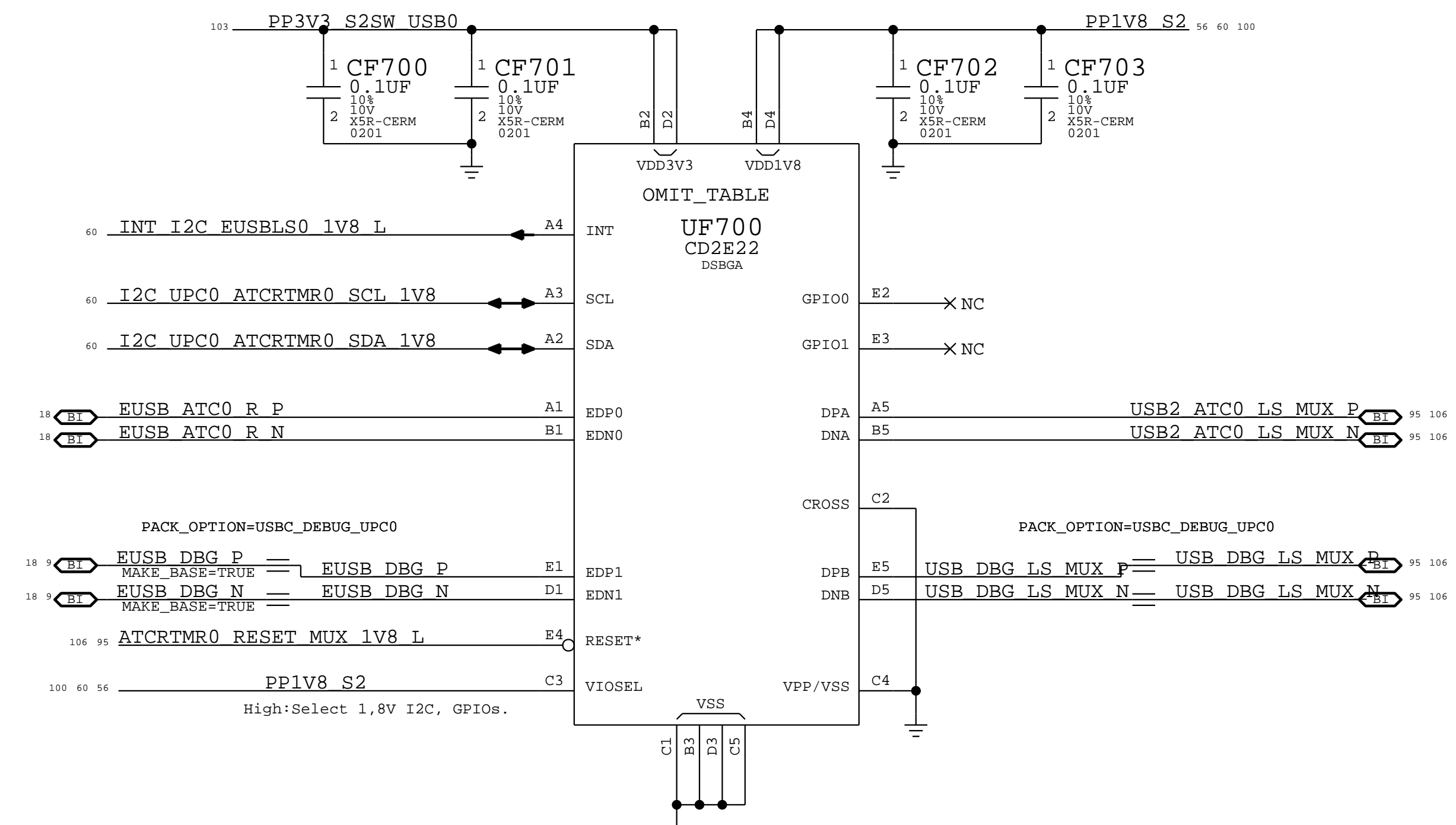
FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK



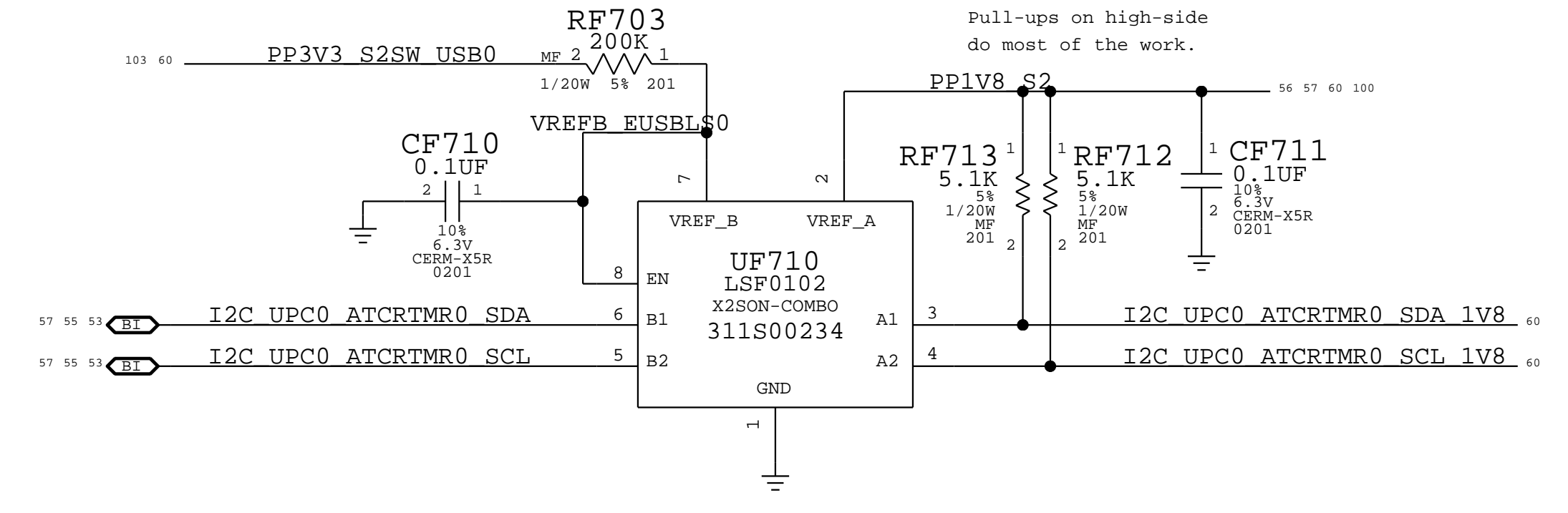
LEFT FRONT PORT

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USB-C: Connector(s)			
Apple Inc.		DRAWING NUMBER	051-05399
		REVISION	9.0.0
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		PAGE	156 OF 999
		SHEET	59 OF 117
		BOM_COST_GROUP=USB-C	

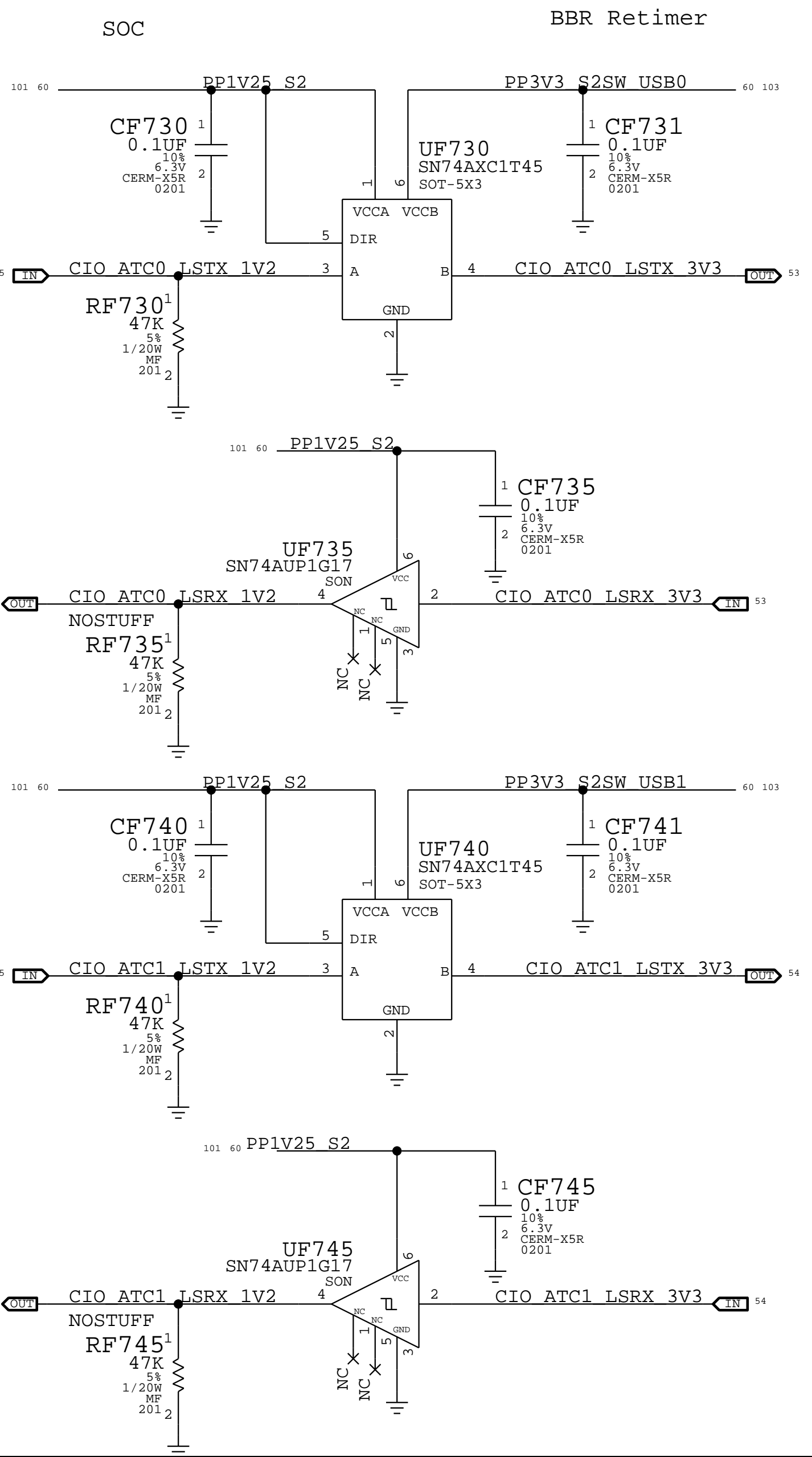
** OK2INTEGRATE **



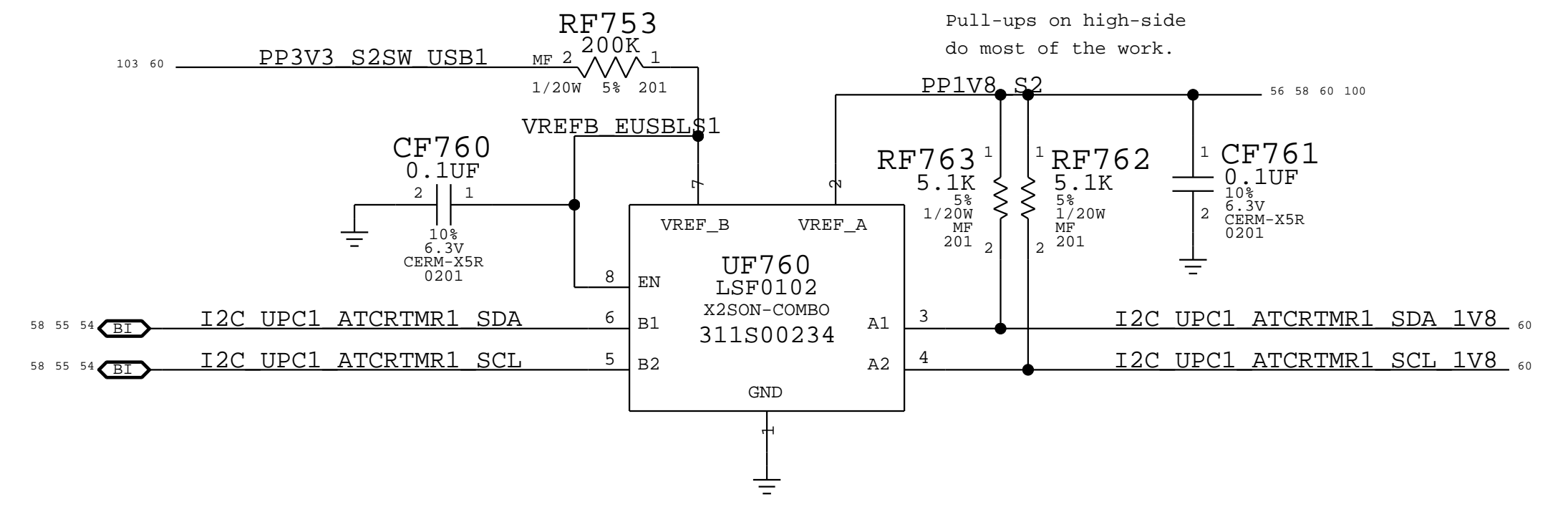
PARROT 0 I2C/RESET LEVEL SHIFTERS



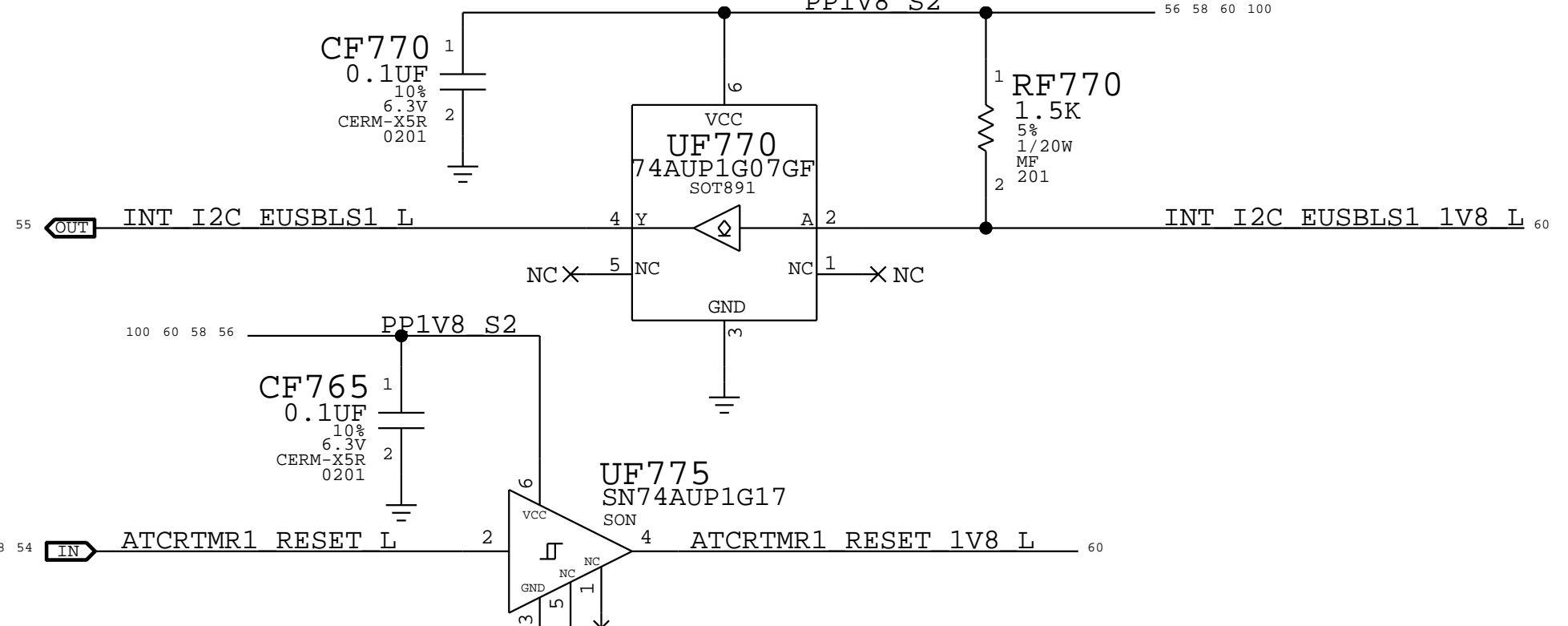
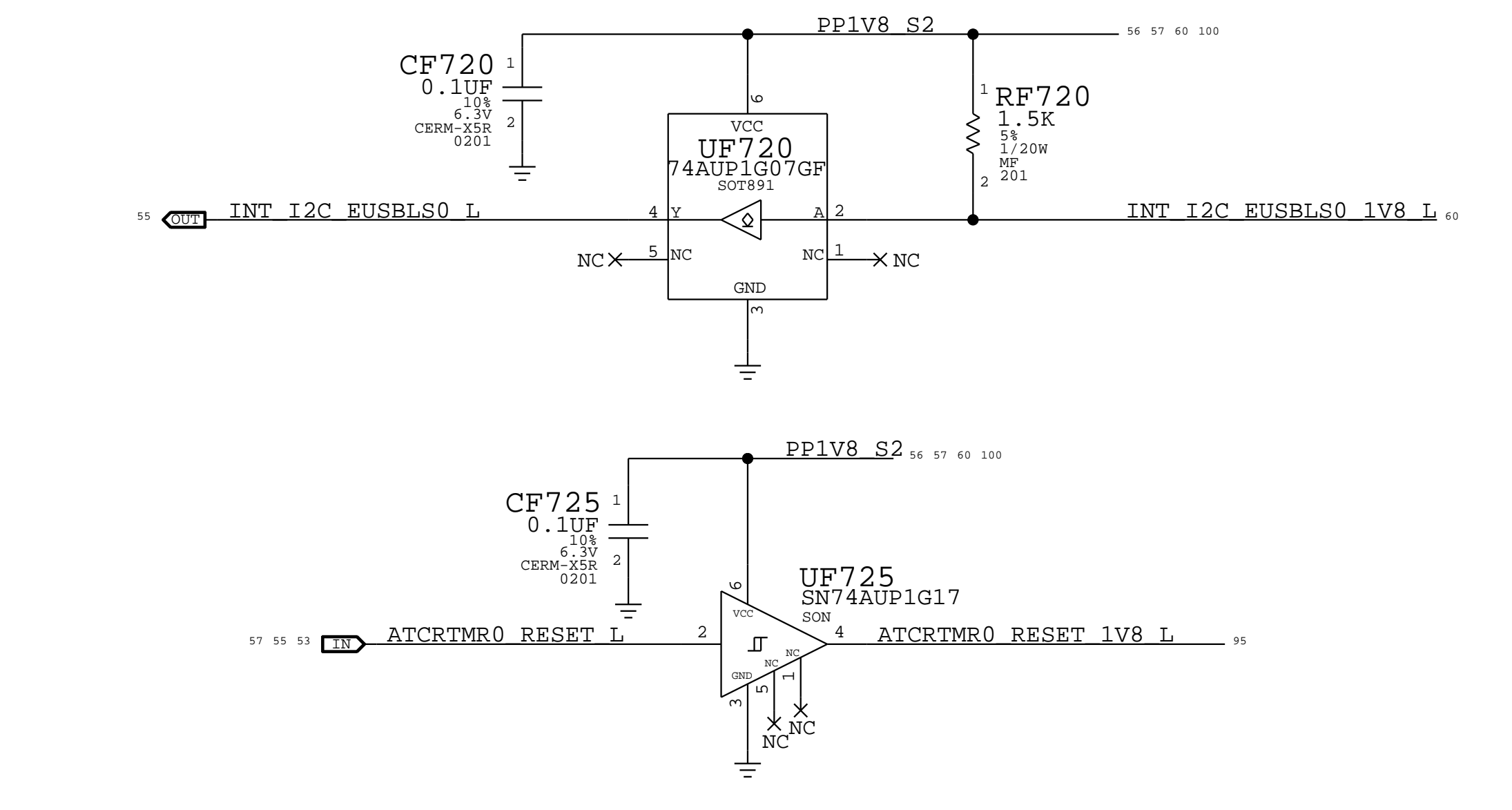
TBT LS RX/TX LEVEL SHIFTERS



PARROT 1 I2C/RESET LEVEL SHIFTERS



PARROT 1 I2C/RESET LEVEL SHIFTERS



PAGE TITLE		
USB-C: HS Level Shifters		
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BOM_COST_GROUP=USB-C

8

7

6

5

4

3

2

1

D

D

C

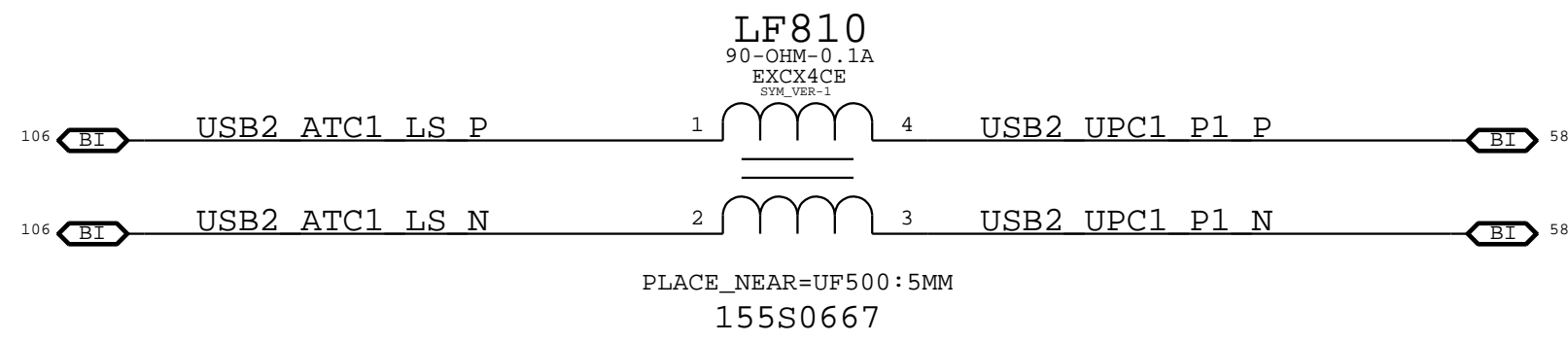
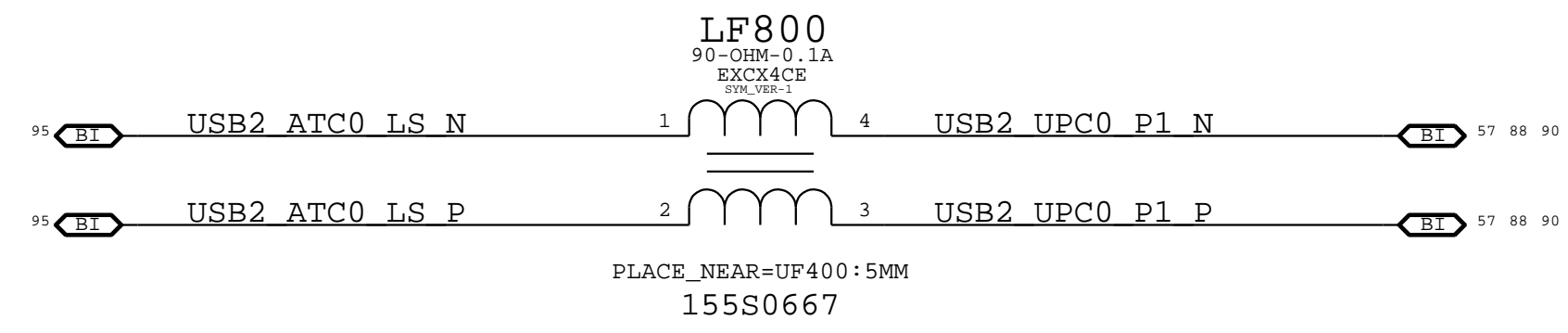
C

B

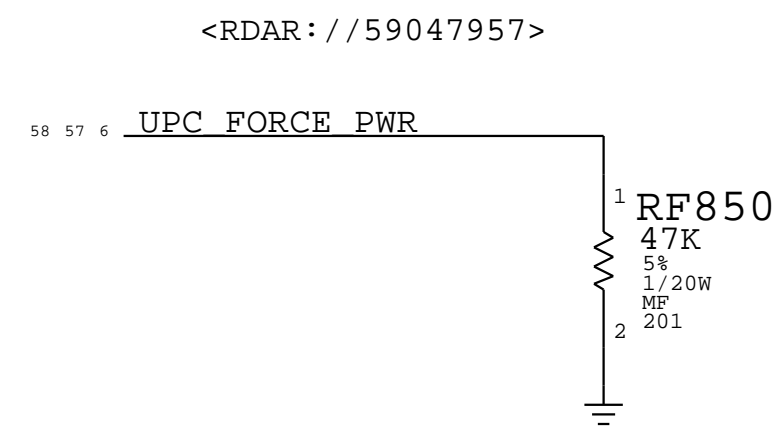
B

A

A



NOTE: CHOKE PINOUT IS DIFFERENT BETWEEN LANE 0 AND LANE 1 FOR EASE OF ROUTING



BOM_COST_GROUP=USB-C

PAGE TITLE		
USB-C: SUPPORT		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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8

7

6

5

4

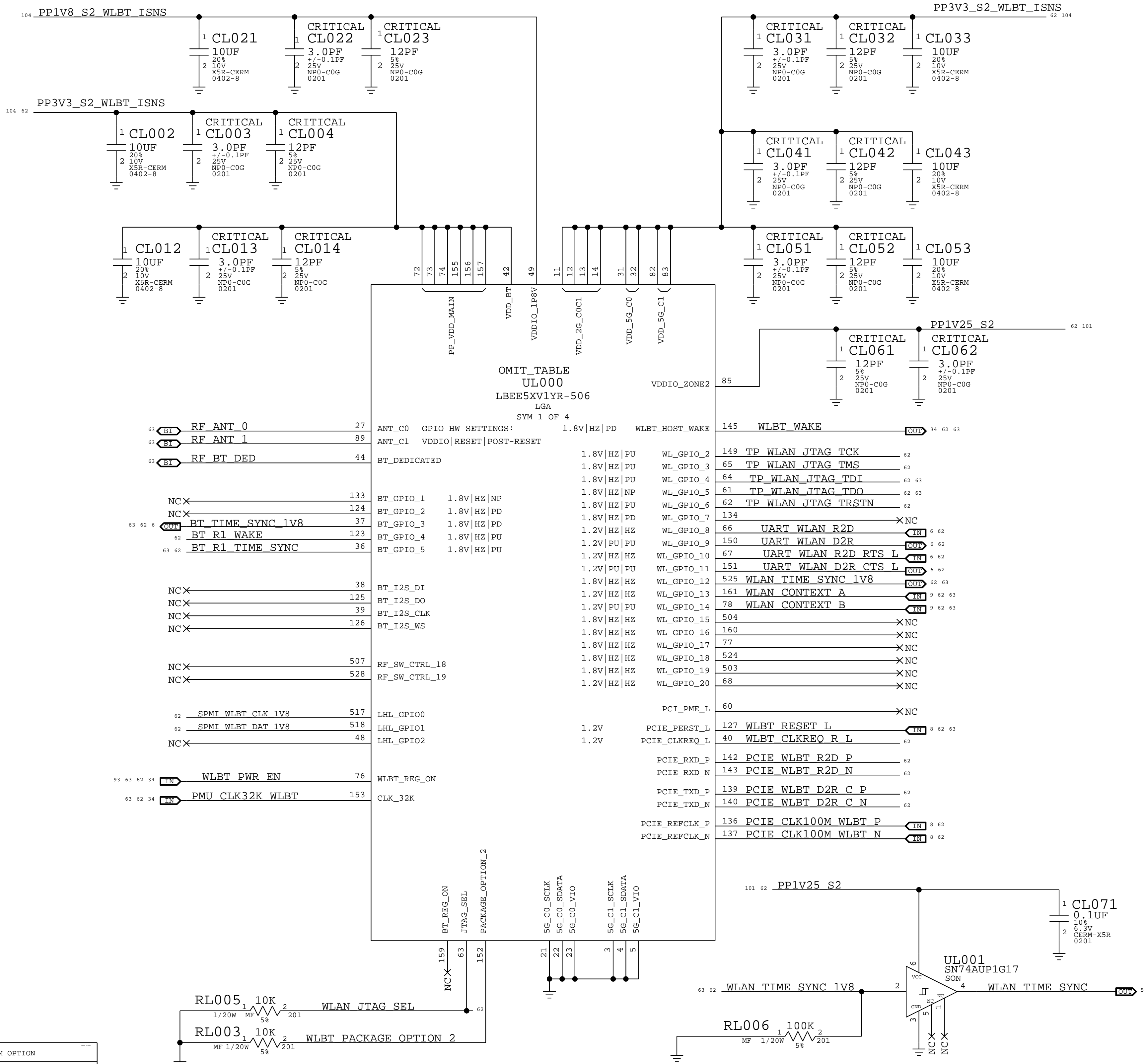
3

2

1

RASPUTIN WIFI/BT MODULE

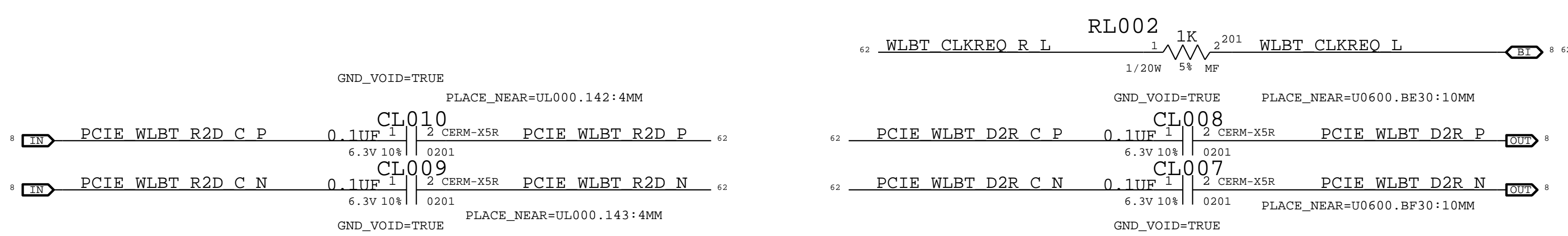
FOR HOSTINTERFACE TABLES REFER TO
RDAR://PROBLEM/53187294



TPL001	PMU CLK32K WLBT	34 62 63
TPL002	WLBT_PWR_EN	34 62 63 93
TPL003	WLBT_WAKE	34 62 63
TPL004	TP WLAN JTAG TCK	62
TPL005	TP WLAN JTAG TMS	62
TPL006	TP WLAN JTAG TDI	62 63
TPL007	TP WLAN JTAG TDO	62 63
TPL008	TP WLAN JTAG TRSTN	62
TPL009	WLAN JTAG_SEL	62
TPL012	BT TIME SYNC IV8	6 62 63
TPL013	BT R1 WAKE	62
TPL014	BT R1 TIME SYNC	62 63
TPL017	UART WLAN R2D	6 62
TPL018	UART WLAN D2R	6 62
TPL019	UART WLAN R2D RTS L	6 62
TPL020	UART WLAN D2R CTS L	6 62
TPL021	WLAN_TIME_SYNC_IV8	62 63
TPL022	WLAN_CONTEXT_A	9 62 63
TPL023	WLAN_CONTEXT_B	9 62 63
TPL024	SPMI WLBT_CLK_IV8	62
TPL025	SPMI WLBT_DAT_IV8	62
PPL030	PCIE_CLK100M_WLBT_P	8 62
PPL031	PCIE_CLK100M_WLBT_N	8 62
TPL032	WLBT_RESET_L	8 62 63
TPL033	WLBT_CLKREO_L	8 62 63

RASPUTIN BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00763	1	MODULE, WLAN BT, RASPUTIN, 88.11, N, L04549	UL000	CRITICAL	



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DRAWING NUMBER		051-05399	SIZE D
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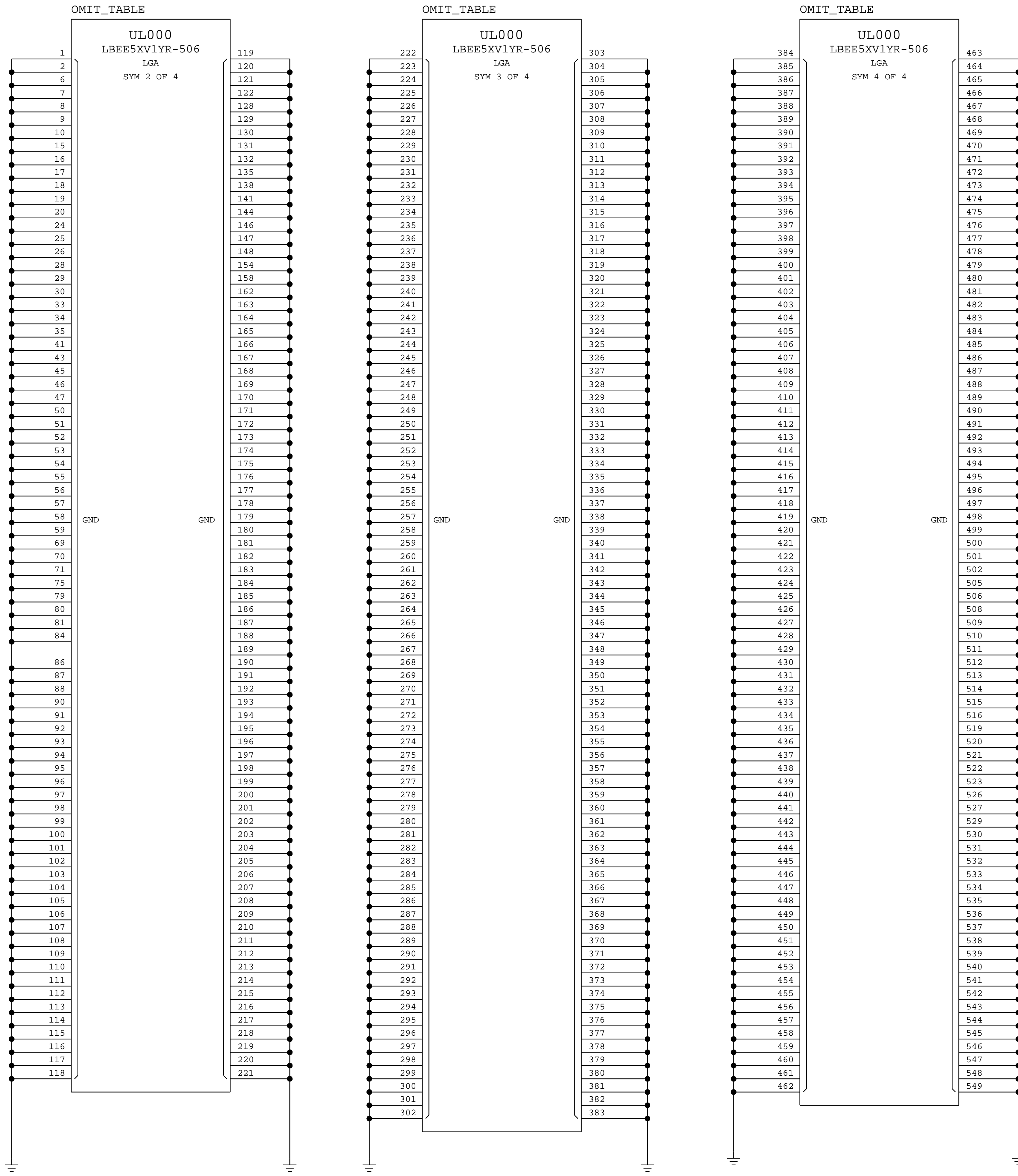
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BOM_COST_GROUP=WIRELESS

THIS PAGE IS NOT SYNCED TO THE REF DESIGN

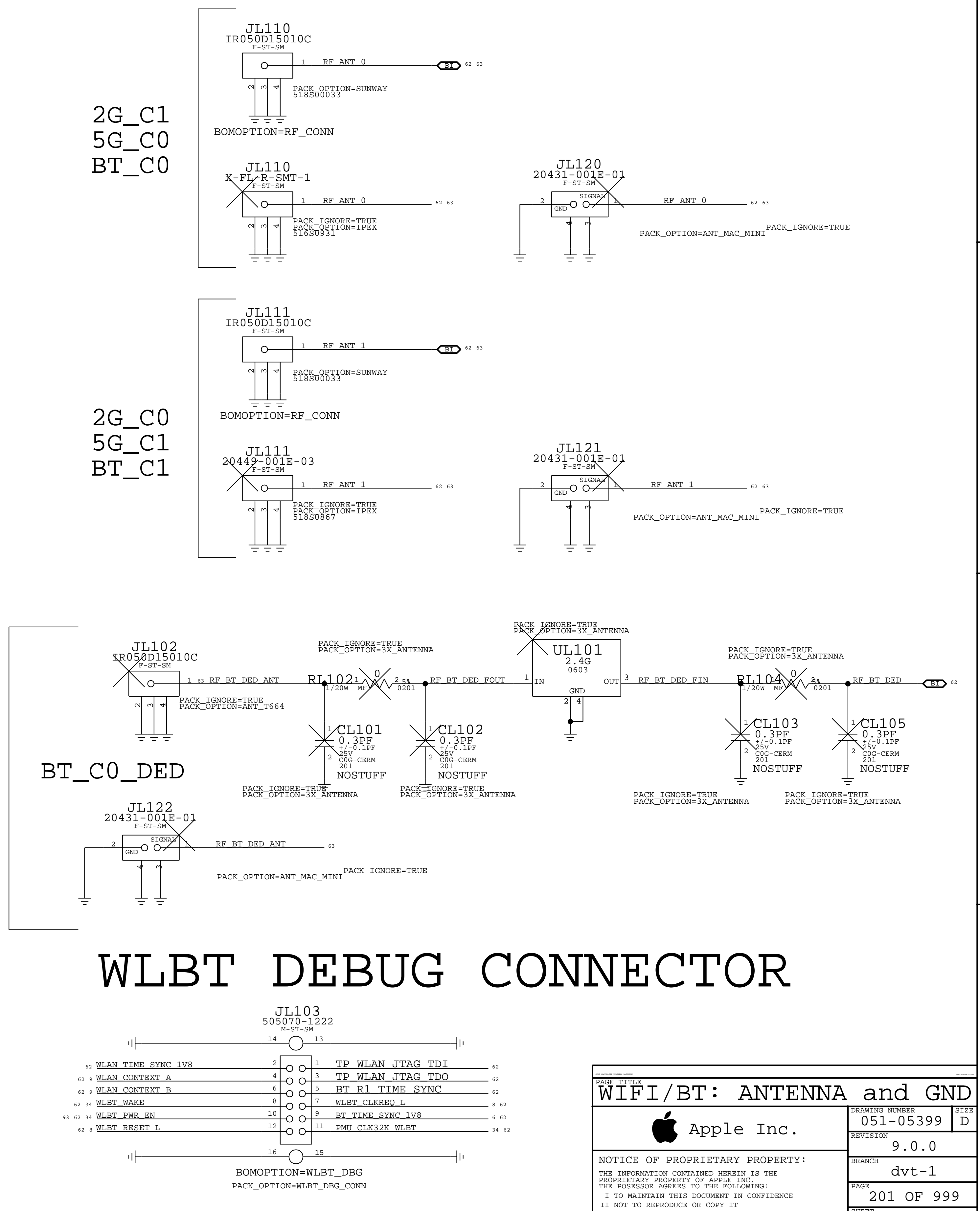
ANTENNA CONNECTORS

SUNWAY SINGLE SOURCE FOR J293 <RDAR://60156088>

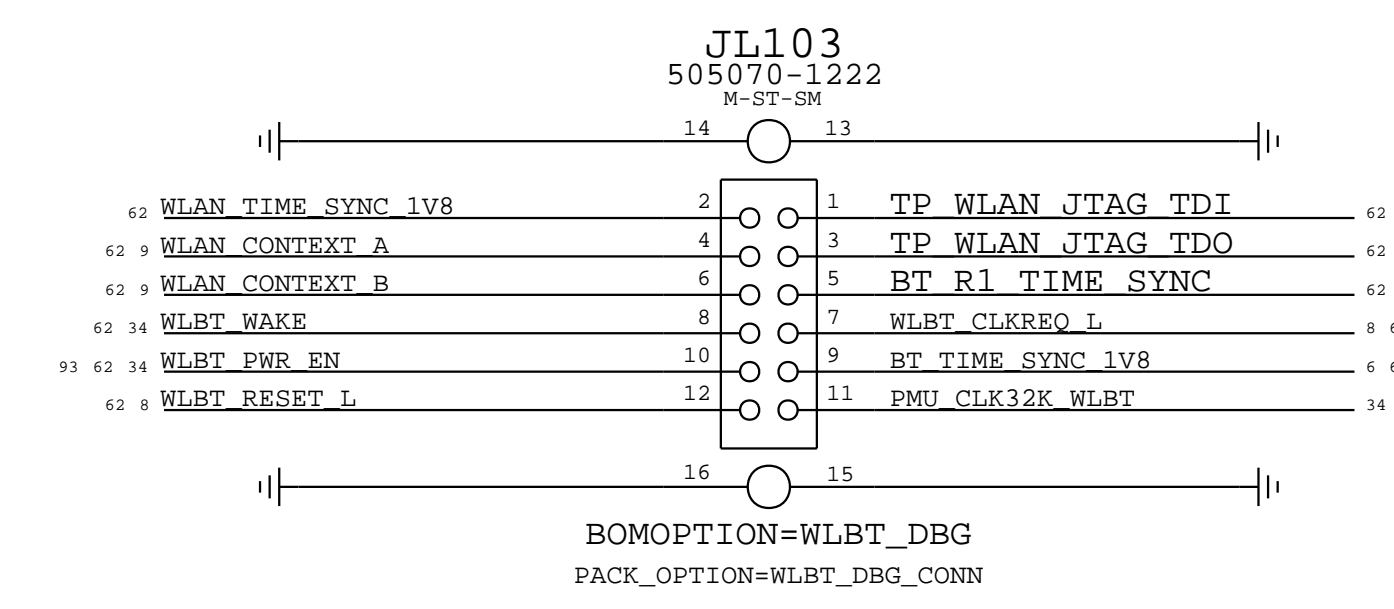


2G_C1
5G_C0
BT_C0

2G_C0
5G_C1
BT_C1



WLBT DEBUG CONNECTOR

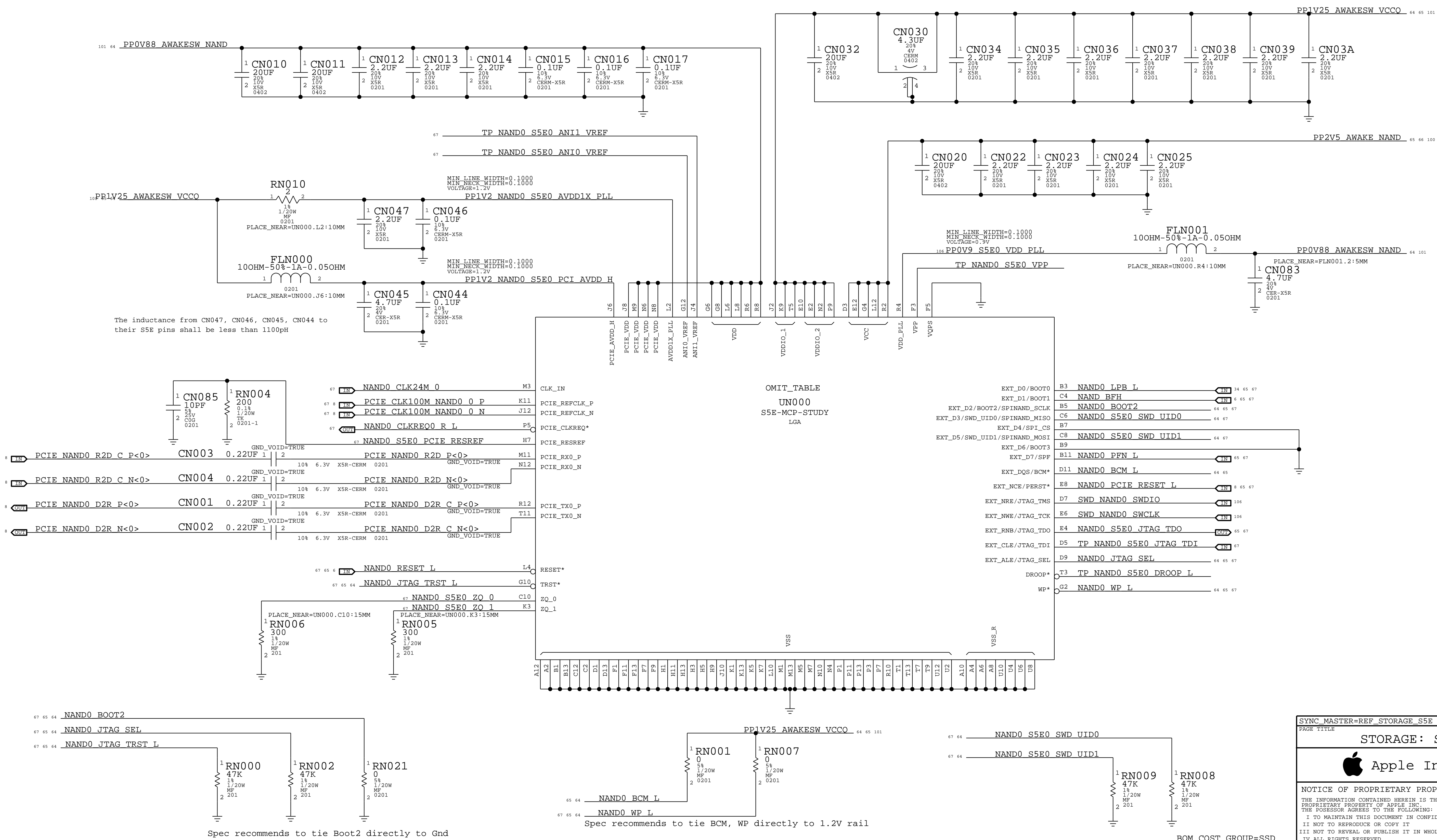


PAGE TITLE		DRAWING NUMBER		SIZE
WIFI/BT: ANTENNA and GND		051-05399		D
REVISION		9.0.0		
BRANCH		dvt-1		
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BOM_COST_GROUP=WIRELESS

*** OK2 INTEGRATE ***

NANDO S5E0



The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

Spec recommends to tie Boot2 directly to Gnd

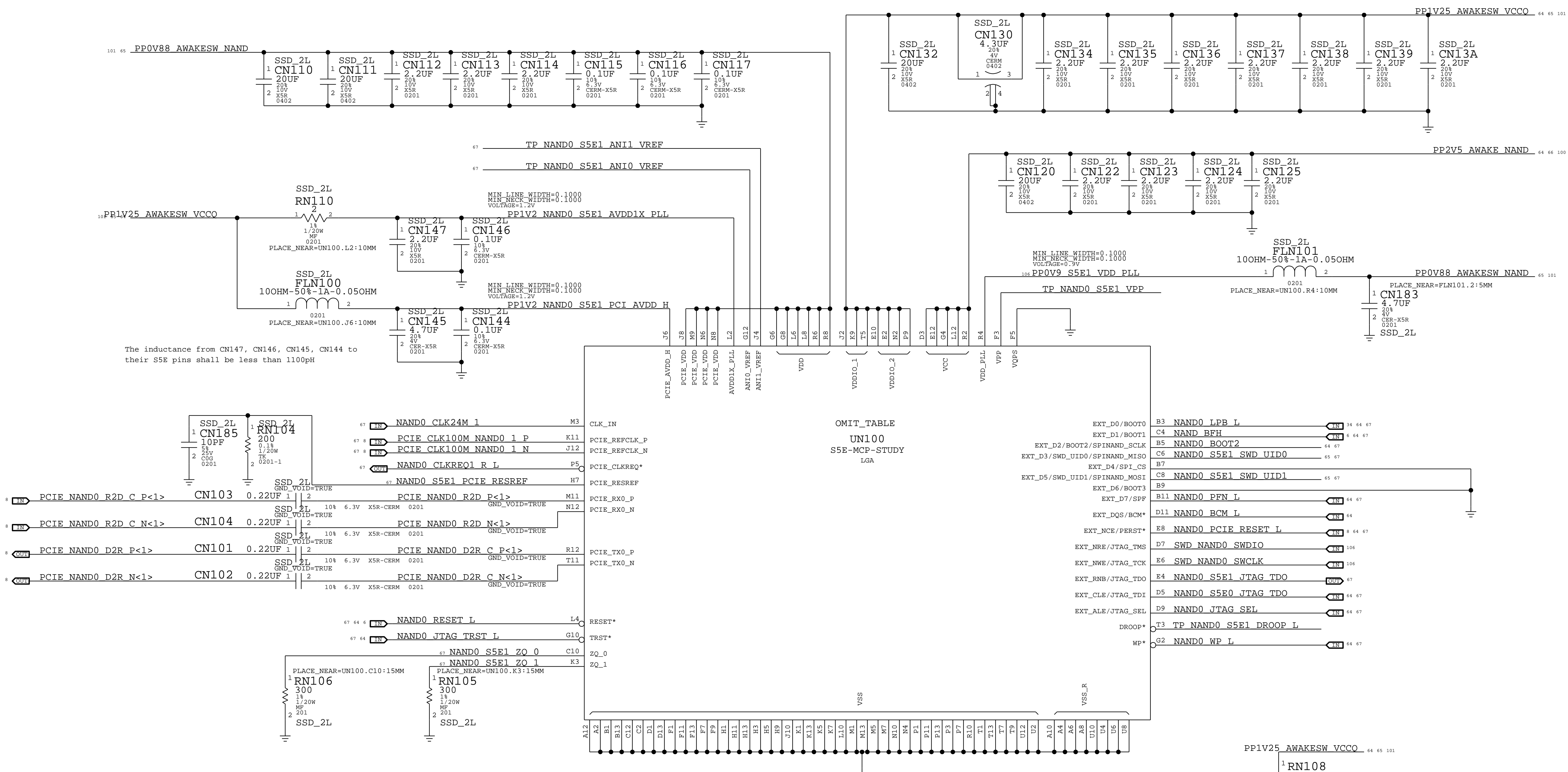
Spec recommends to tie BCM, WP directly to 1.2V rail

BOM_COST_GROUP=SSD

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STORAGE: SSD0 S5E <0>			
DRAWING NUMBER		SIZE	
051-05399		D	
REVISION		9.0.0	
BRANCH		dvt-1	
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*** OK2 INTEGRATE ***

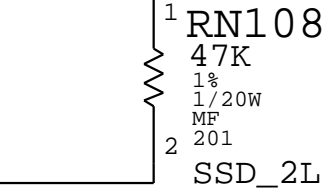
NAND0 S5E1



The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

OMIT_TABLE
UN100
S5E-MCP-STUDY
LGA

PP1V25 AWAKESW VCCO 64 65 101

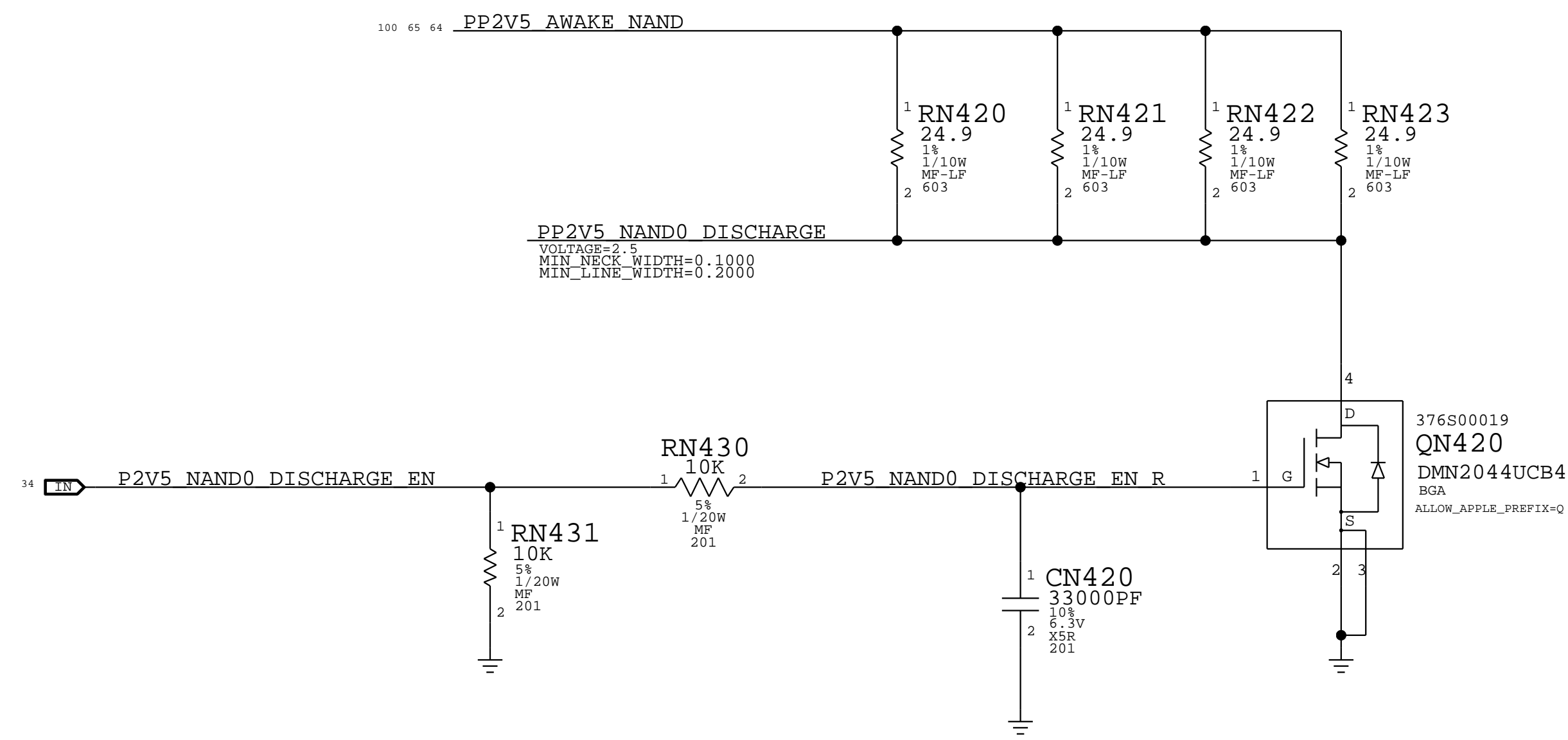


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STORAGE: SSD0 S5E <1>		REVISION	9.0.0
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		SHEET	65 OF 117

OK2INTEGRATE

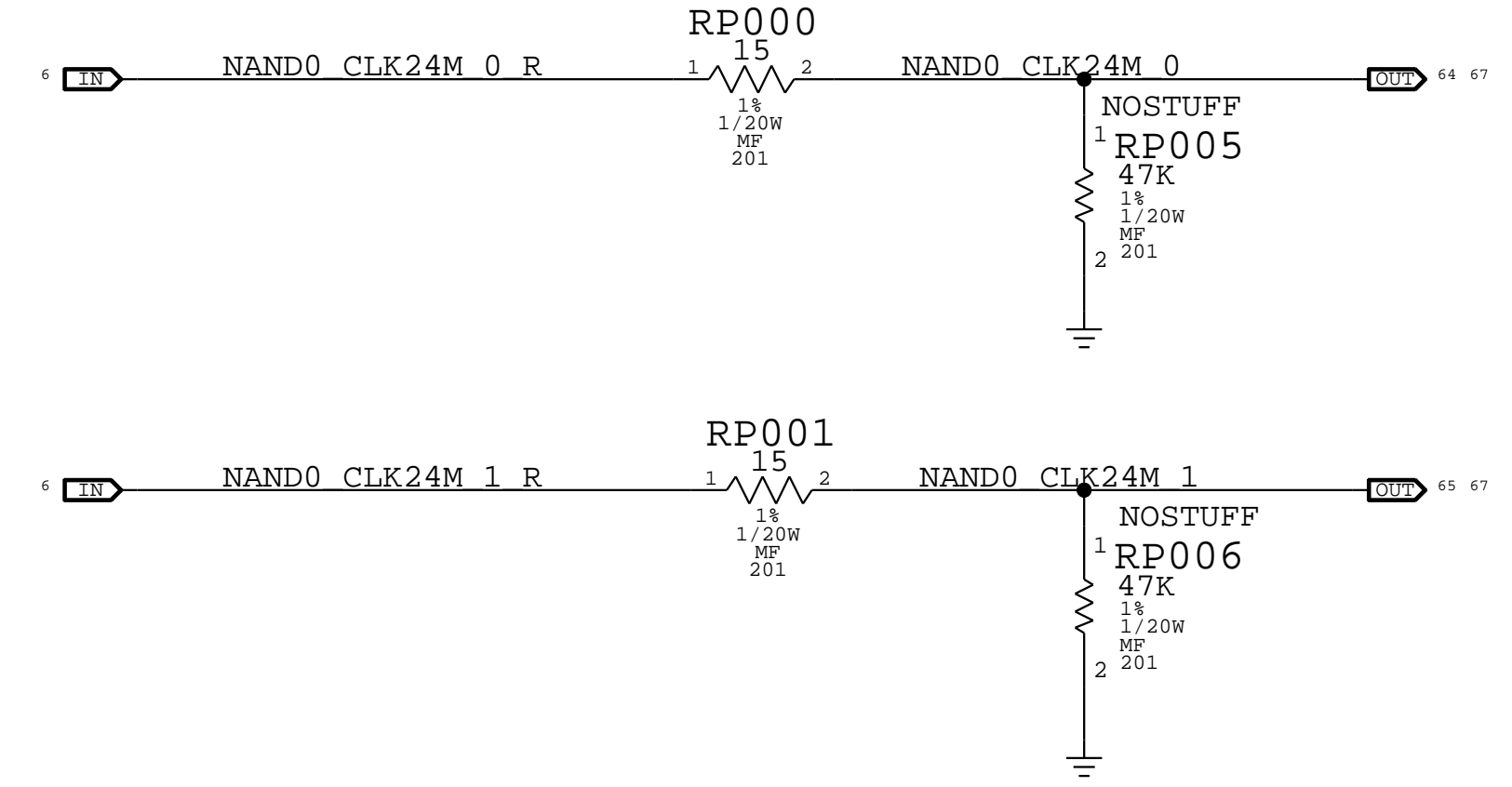
THIS EXTERNAL NAND VCC DISCHARGE CIRCUITRY IS FOR SYSTEM THAT DOES NOT USE OCARINA



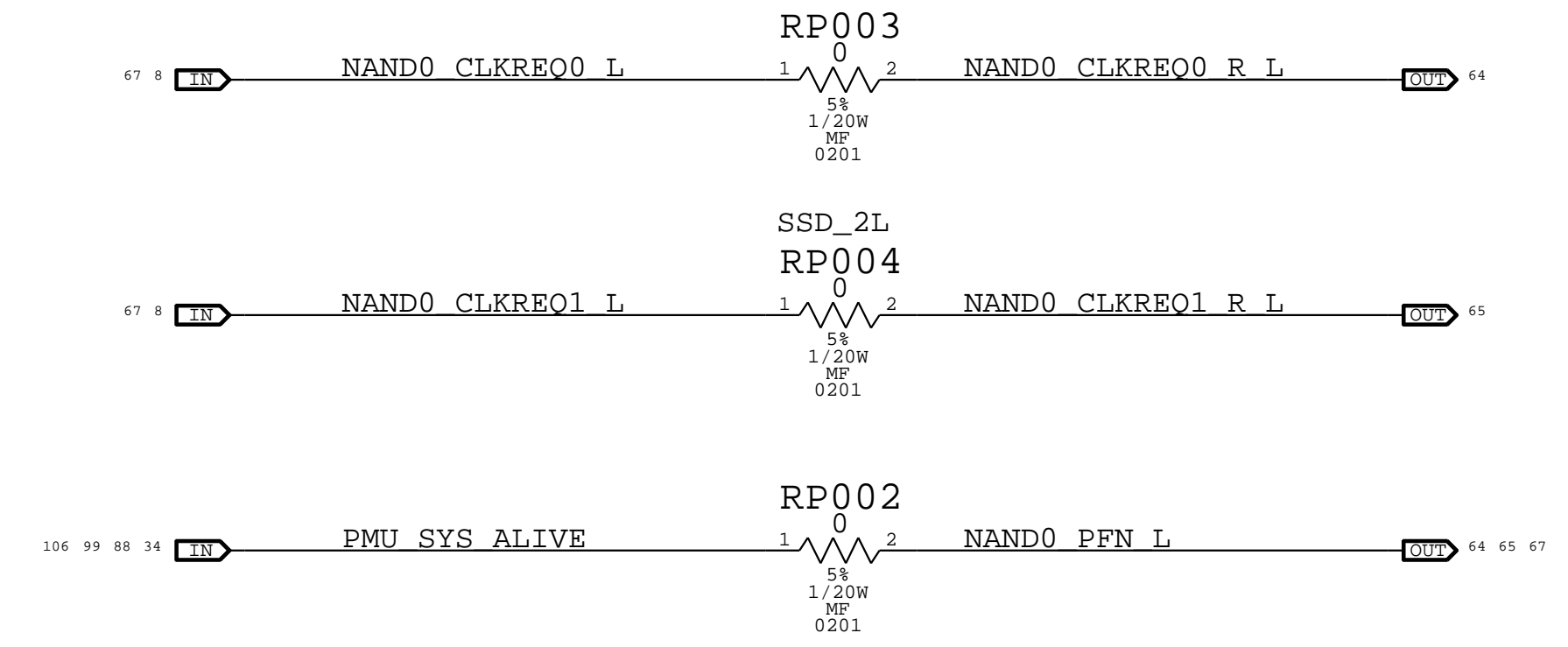
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	PAGE	224 OF 999
	SHEET	66 OF 117

SSD 24M CLOCK TERMINATIONS

- 67 64 NAND0_CLK24M_0
- 67 65 NAND0_CLK24M_1
- 64 8 PCIE_CLK100M_NAND0_0_N
- 64 8 PCIE_CLK100M_NAND0_0_P
- 65 8 PCIE_CLK100M_NAND0_1_N
- 65 8 PCIE_CLK100M_NAND0_1_P



- 106 8 PPOV9_S5E0_VDD_PLL
- 106 8 PPOV9_S5E1_VDD_PLL
- 65 64 34 NAND0_LPB_L
- 65 64 6 NAND_BFH
- 65 64 NAND_BOOT2
- 64 8 NAND_S5E0_SWD_UID0
- 65 8 NAND_S5E1_SWD_UID0
- 64 8 NAND_S5E0_SWD_UID1
- 65 8 NAND_S5E1_SWD_UID1
- 67 65 64 NAND_PFN_L
- 65 64 8 NAND_PCIE_RESET_L
- 106 5 SWD_NAND0_SWDIO
- 106 5 SWD_NAND0_SWCLK
- 65 64 NAND_S5E0_JTAG_TDO
- 64 8 TP_NAND0_S5E0_JTAG_TDI
- 65 8 NAND_S5E1_JTAG_TDO
- 65 64 NAND_JTAG_SEL
- 67 8 NAND_WP_L
- 67 8 NAND_CLKREQ0_L
- 67 8 NAND_CLKREQ1_L
- 64 8 NAND_S5E0_PCIE_RESREF
- 65 8 NAND_S5E1_PCIE_RESREF
- 65 64 6 NAND_RESET_L
- 65 8 NAND_S5E1_ZQ_0
- 64 8 NAND_S5E0_ZQ_0
- 64 8 NAND_S5E0_ZQ_1
- 65 8 NAND_S5E1_ZQ_1
- 65 64 NAND_JTAG_TRST_L
- 64 8 TP_NAND0_S5E0_ANI1_VREF
- 64 8 TP_NAND0_S5E0_ANI0_VREF
- 65 8 TP_NAND0_S5E1_ANI1_VREF
- 65 8 TP_NAND0_S5E1_ANI0_VREF



D
C
B
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D
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PAGE TITLE		
STORAGE: SSD SUPPORT		
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	PAGE	230 OF 999
	SHEET	67 OF 117

D

C

B

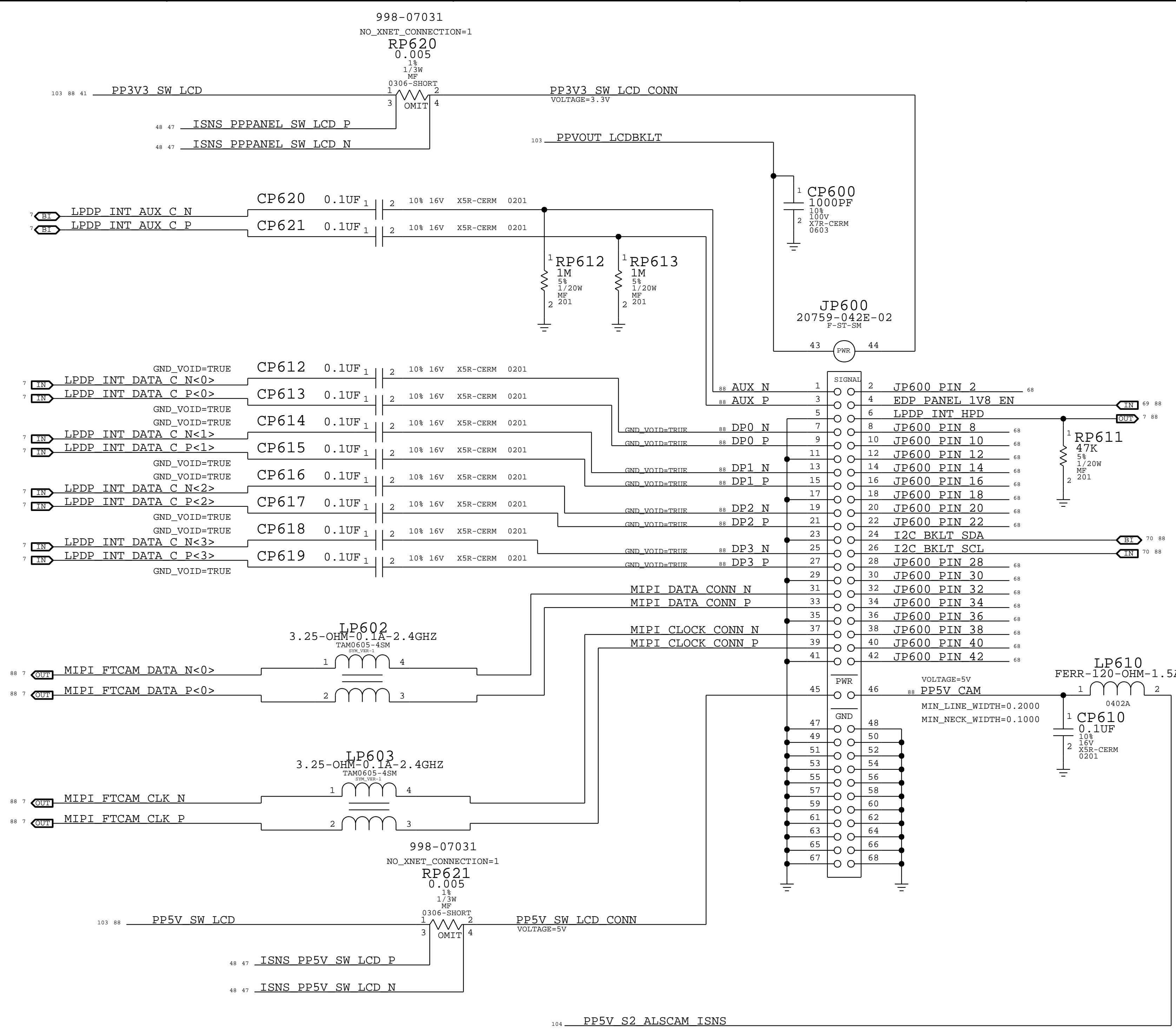
A

D

C

B

A



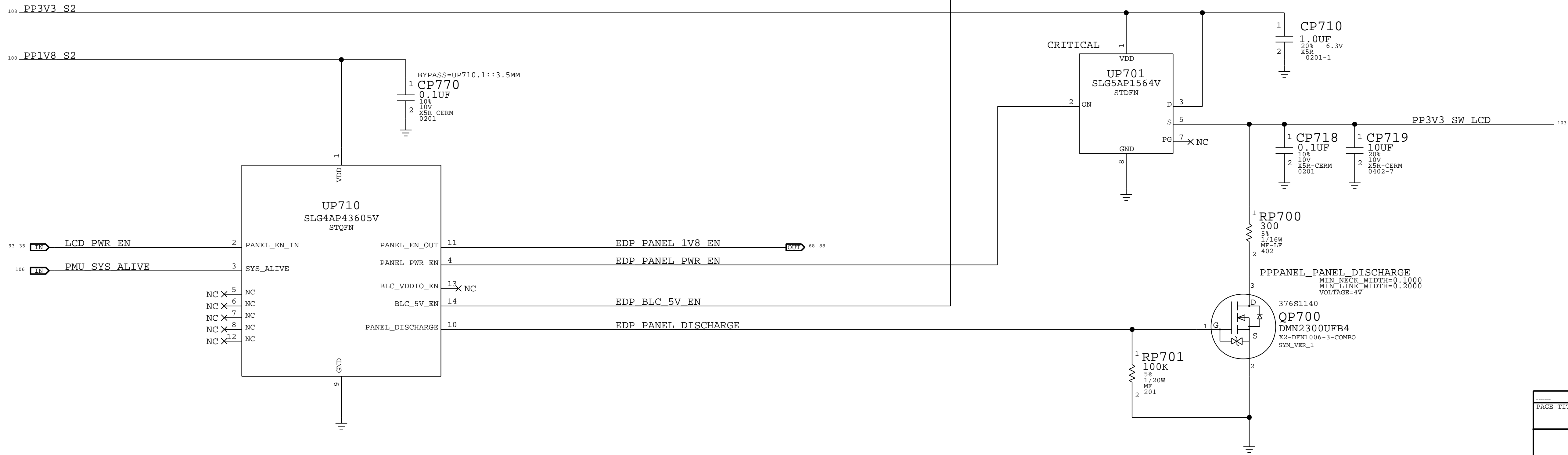
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DISPLAY: CONNECTOR, PWR		
	DRAWING NUMBER	SIZE
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REVISION	BRANCH	PAGE
9.0.0	dvt-1	236 OF 999
SHEET		68 OF 117

*** OK2INTEGRATE ***



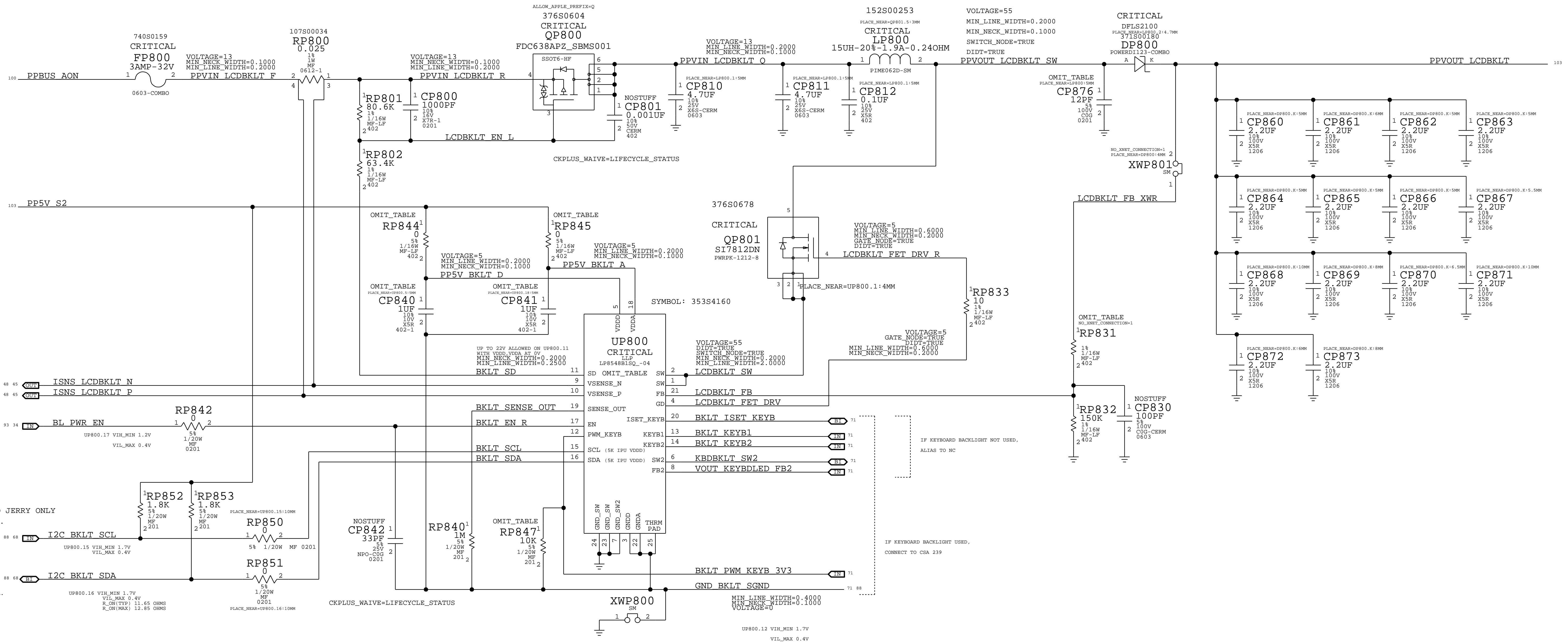
CONSULT YOUR DISPLAY DRI FOR DETAILS
 GENERAL GUIDELINE IS
 3V3 FOR 2020 SYSTEMS
 3V8 FOR 2021 SYSTEMS



PAGE TITLE		
DISPLAY POWER SEQUENCER		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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	PAGE	237 OF 999
	SHEET	69 OF 117

*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER



BEN IC VERSION TO MATCH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35384160	1	IC,LP8548B1-04,DC/DC CVT,BOOST,0.9V-24	UP800		BLC_BEN_IC:V4
353802256	1	IC,LP8548B1A-07,DC/DC BOOST CVT,0.9V24	UP800		BLC_BEN_IC:V7

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5A,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (J132, J213)
100K IF KEYBOARD PWM INPUT IS PRESENT (J152)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0007	1	RES,MTL,1/20W,10K,08M,5,0201,SMD	RP847		BLC_KBD_BOOST_USED:NO
118S0014	1	RES,MP,100KOHM,1,1/20W,0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0339	1	RES,MTL FILM,1/16W,18.2K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:16
114S0359	1	RES,MTL FILM,1/16W,28.7K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDD5 & VDDA, SEE <RDAR://50682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.08M,1A MAX,0402,SMD	RP844,RP845		BLC_5V_SERIES:0_OHM
114S0023	2	RES,MTL FILM,1/16W,10 OHM,1,0402,SMD,LF	RP844,RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,XSR,1UF,10V,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,XSR,4.7UF,20V,25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

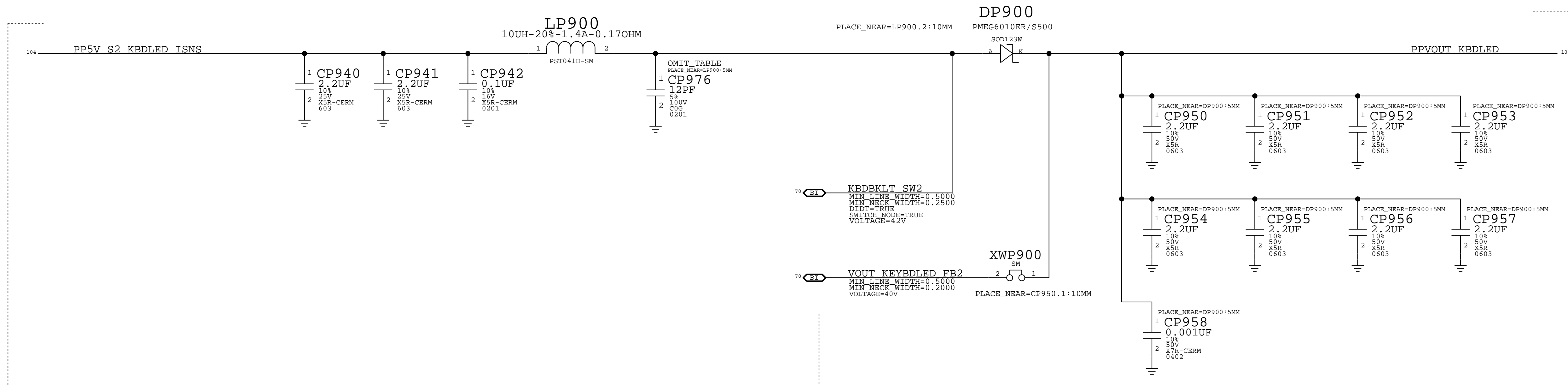
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BEN: CONTROLLER			
		DRAWING NUMBER	051-05399
		REVISION	9.0.0
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		PAGE	238 OF 999
		SHEET	70 OF 117

*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

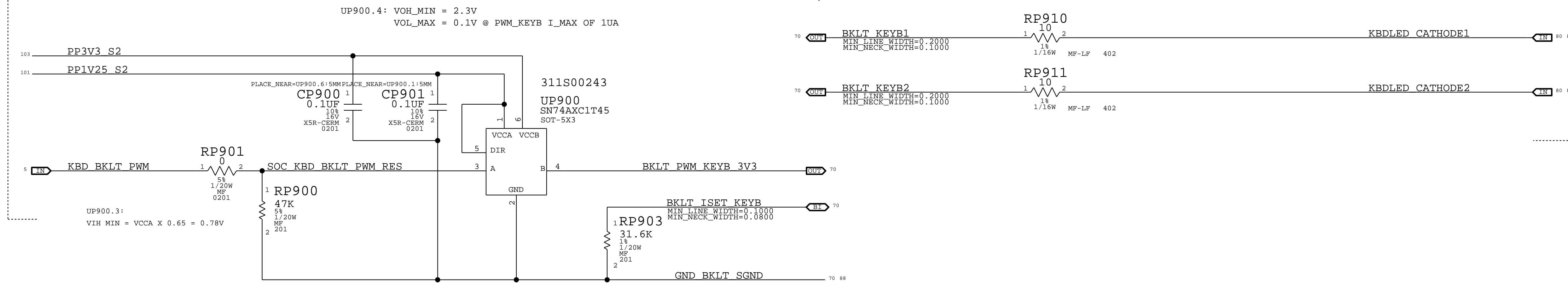
THIS PAGE IS ONLY TO BE INCLUDED IF THE KEYBOARD BACKLIGHT IS CONTROLLED BY THE BEN ON PAGE 238



KEYBOARD BACKLIGHT
POWER & CONTROL
SIGNALS FROM
SYSTEM

KEYBOARD BACKLIGHT
CONNECTOR SIGNALS

KEYBOARD BKLT PWM LEVEL-SHIFTER



OFF=PAGE SIGNALS ON THIS VERTICAL LINE CONNECT TO BEN UP800
ON PAGE 238

KEYBOARD SWITCH NODE DESENSE OPTION

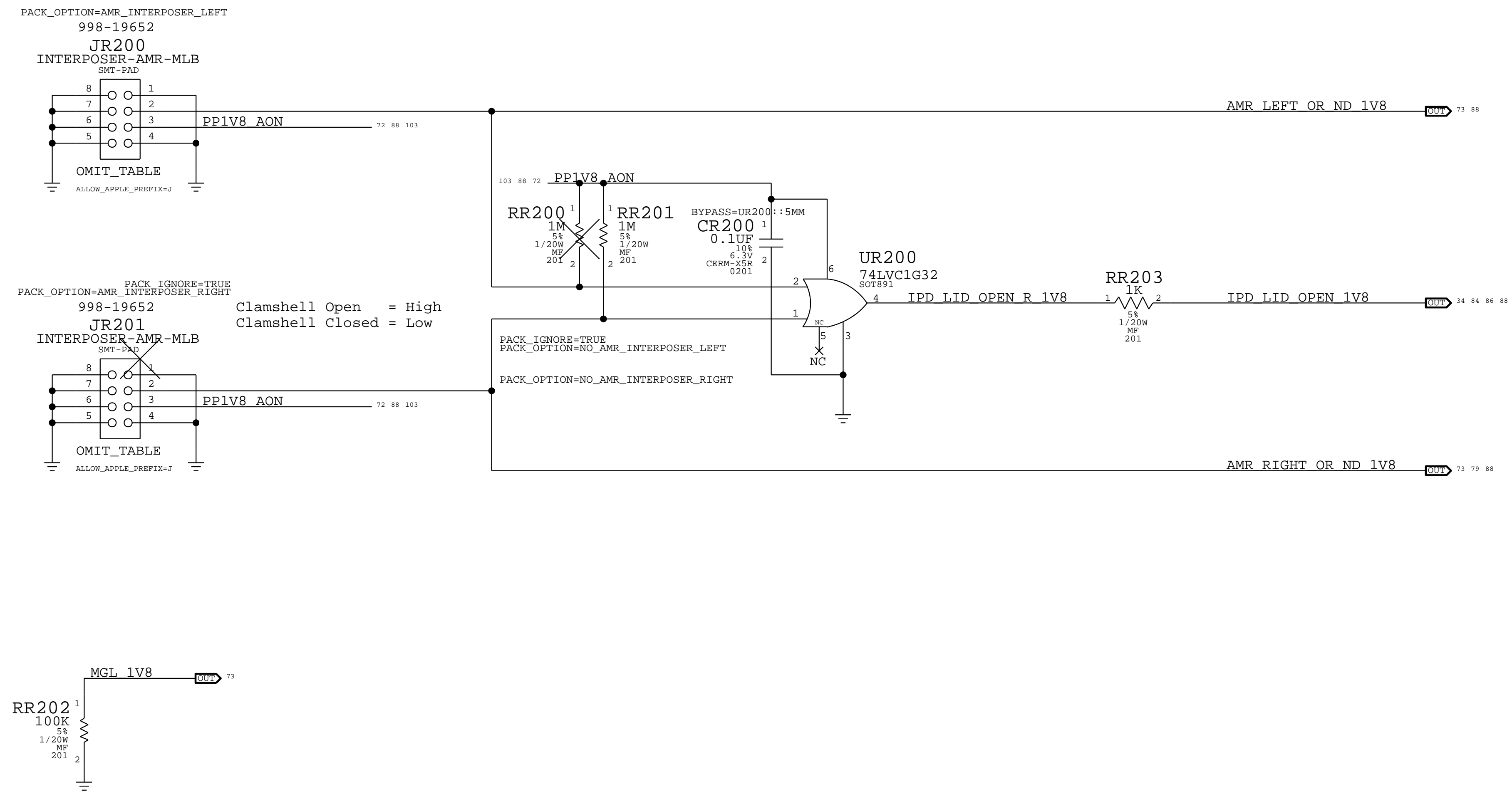
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP976		BLC_KBD_SW_NODE_DESENSE

SYNC_MASTER=REF_BLC_BEN		SYNC_DATE=11/21/2019	
PAGE TITLE			
BEN: KEYBOARD			
		DRAWING NUMBER	051-05399
		REVISION	9.0.0
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		PAGE	239 OF 999
		SHEET	71 OF 117

BOM_COST_GROUP=DISPLAY

*** OK2INTEGRATE ***

Lid Detect Sensors



PAGE TITLE		
SECDIS: AMR		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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	PAGE	242 OF 999
	SHEET	72 OF 117
	BOM_COST_GROUP=SOC	

*** OK2INTEGRATE ***

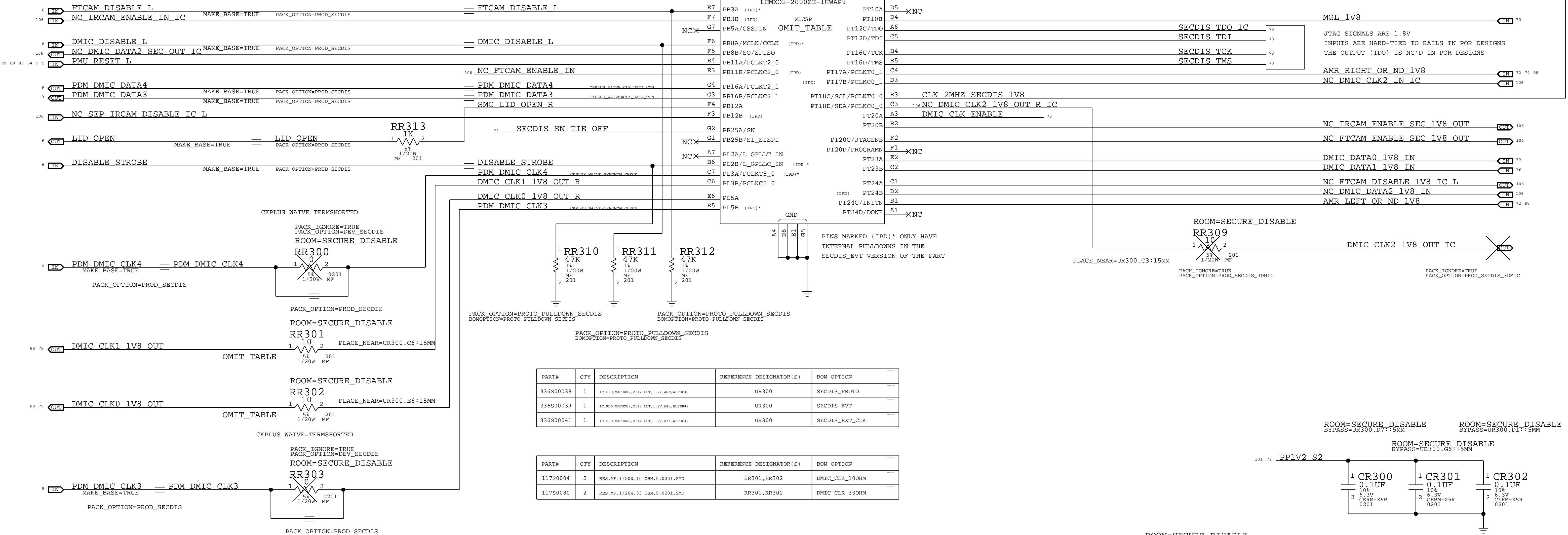
UNLESS 1V8 IS NOTED, SIGNALS ARE 1.2V

CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	0.8MA	33MA
1.8 S2	0.8MA	14MA

SUPER IMPORTANT PACK OPTIONS:

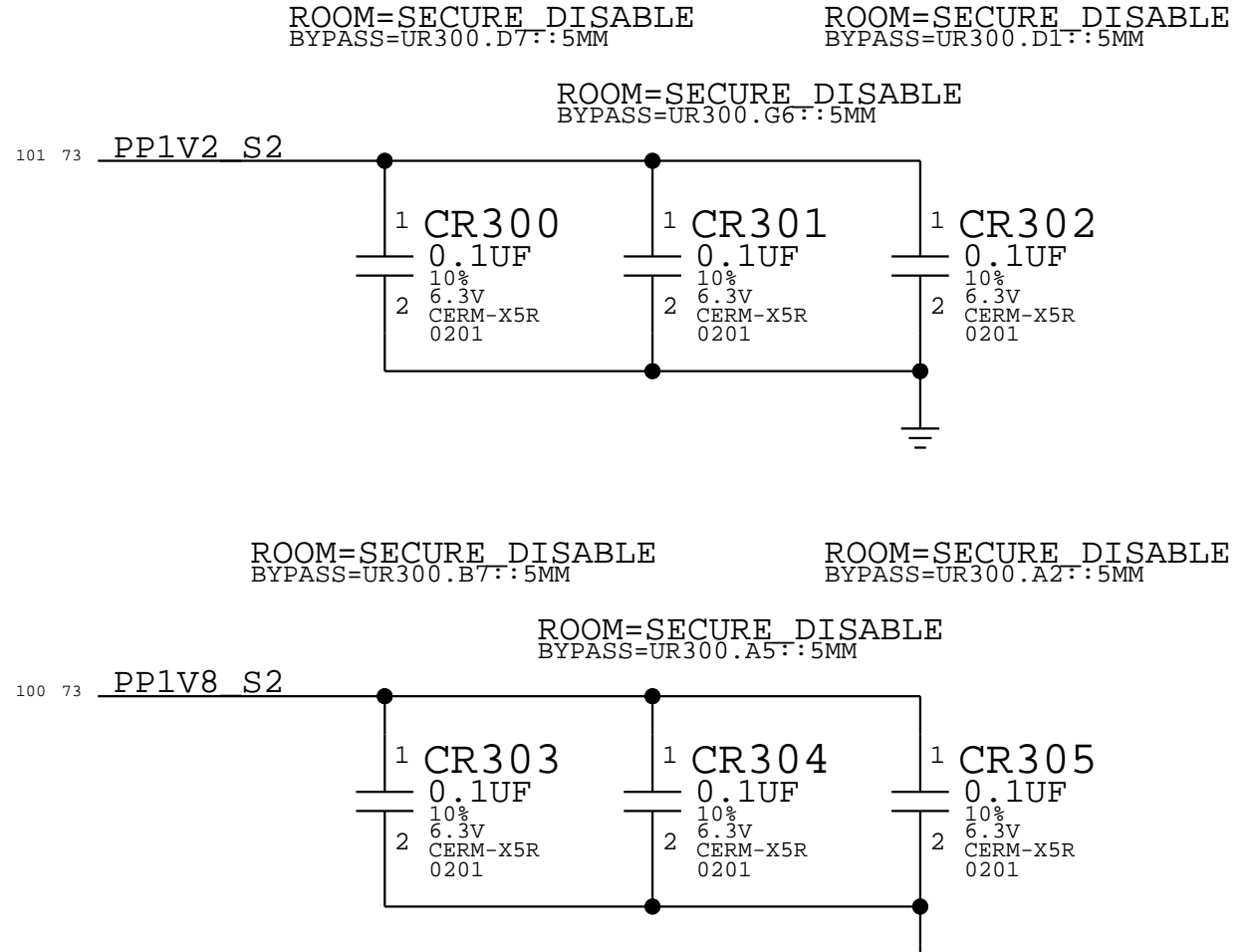
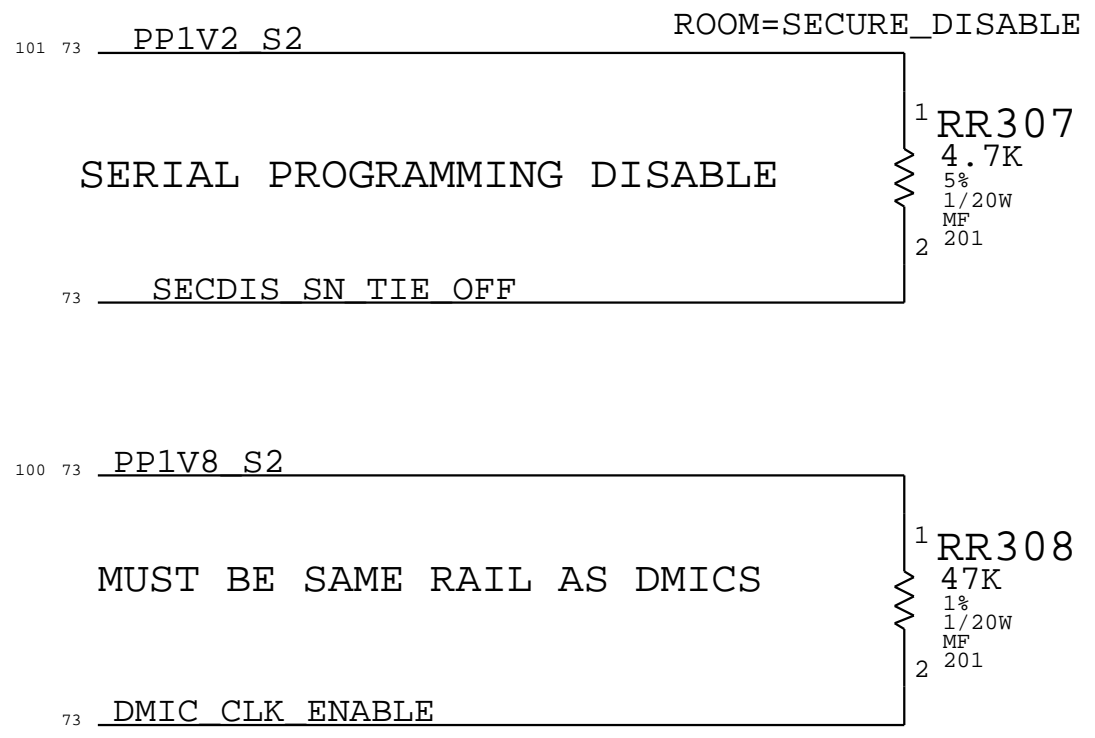
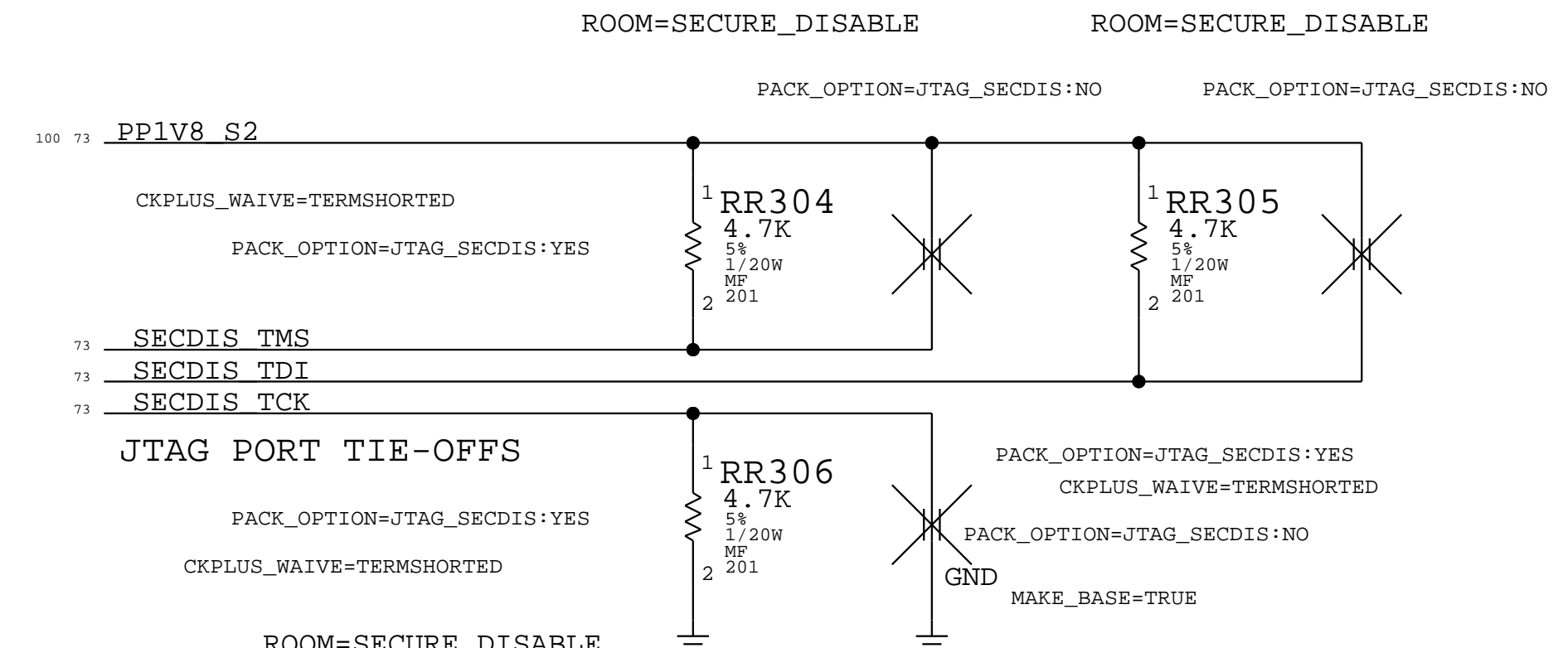
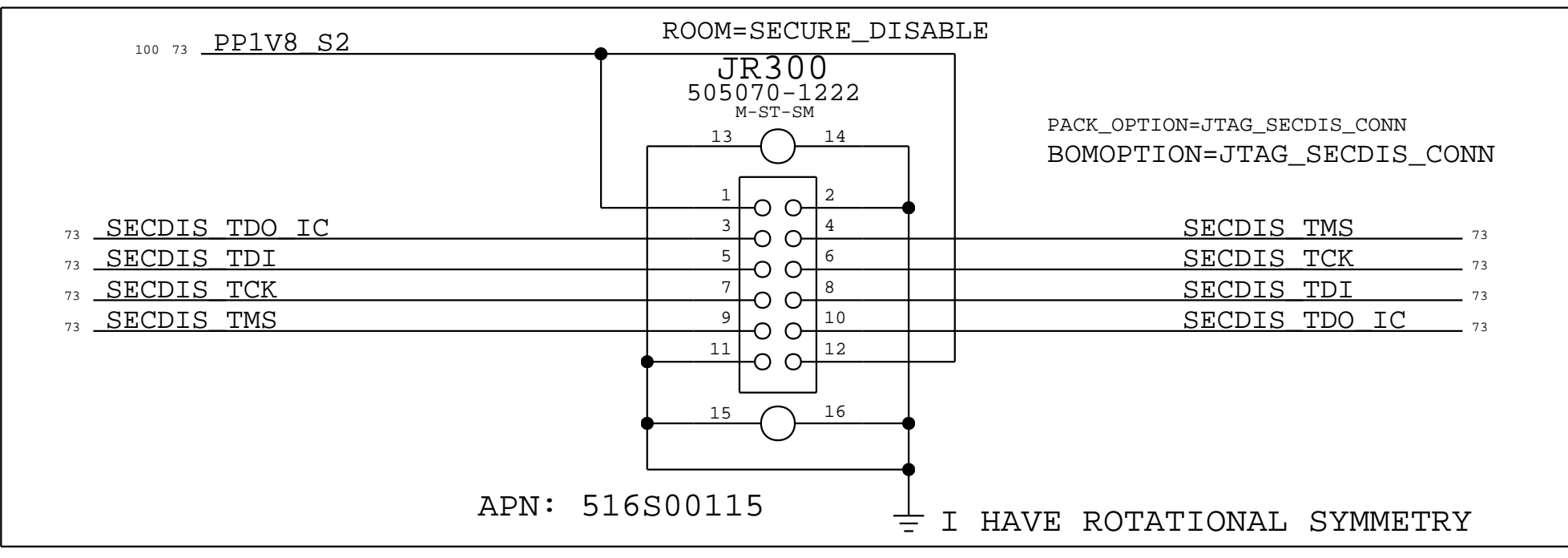
NOTES ARE ON CSA 2 OF THE REFERENCE DESIGN
READ, LEARN, IMPLEMENT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
336S00038	1	IC, PLS, MAC9802, 2112 IUT, 1.2V, ANV, WLCSP49	UR300	SECDIS_PROTO
336S00039	1	IC, PLS, MAC9802, 2112 IUT, 1.2V, APS, WLCSP49	UR300	SECDIS_EVT
336S00041	1	IC, PLS, MAC9802, 2112 IUT, 1.2V, DXX, WLCSP49	UR300	SECDIS_EXT_CLK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0004	2	RES, MF, 1/20W, 10 OHM, 5, 0201, SMD	RR301, RR302	DMIC_CLK_10OHM
117S0080	2	RES, MF, 1/20W, 33 OHM, 5, 0201, SMD	RR301, RR302	DMIC_CLK_33OHM

JTAG FOR DEV & PROTOO BOARDS ONLY



SYNC_MASTER=REF_SECDIS_SAK SYNC_DATE=06/18/2020

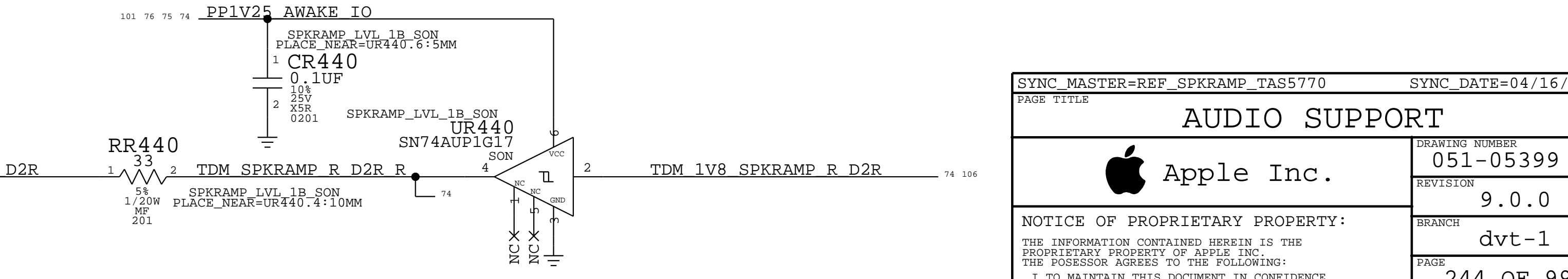
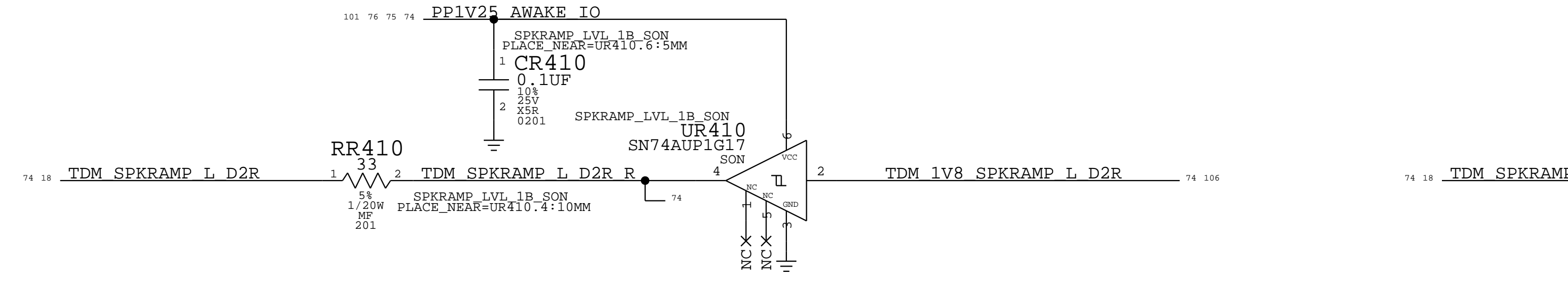
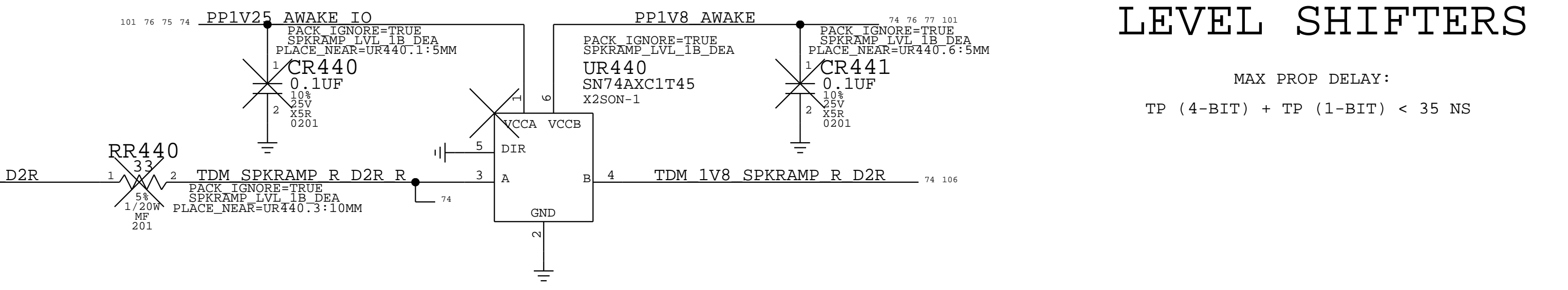
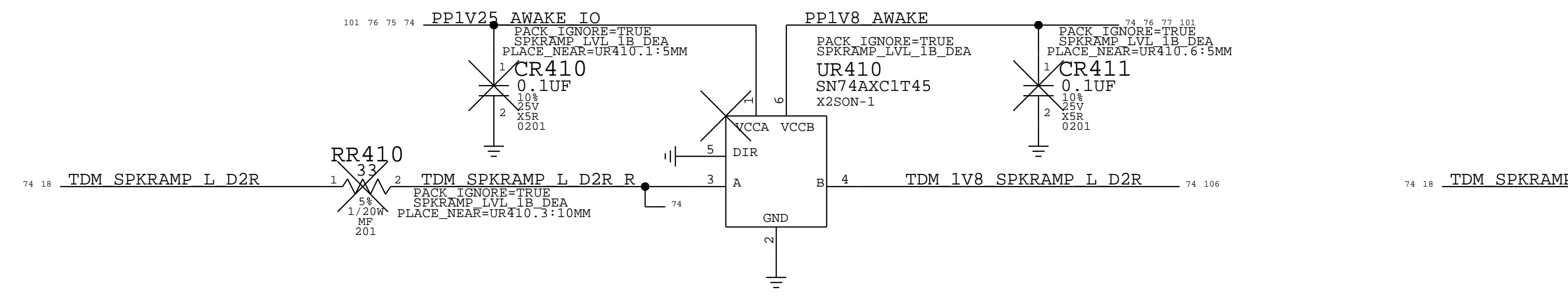
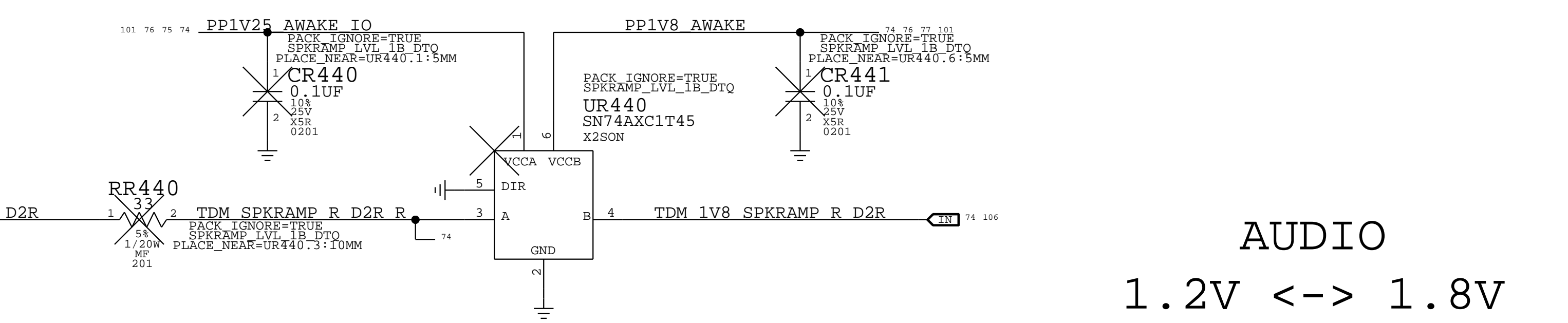
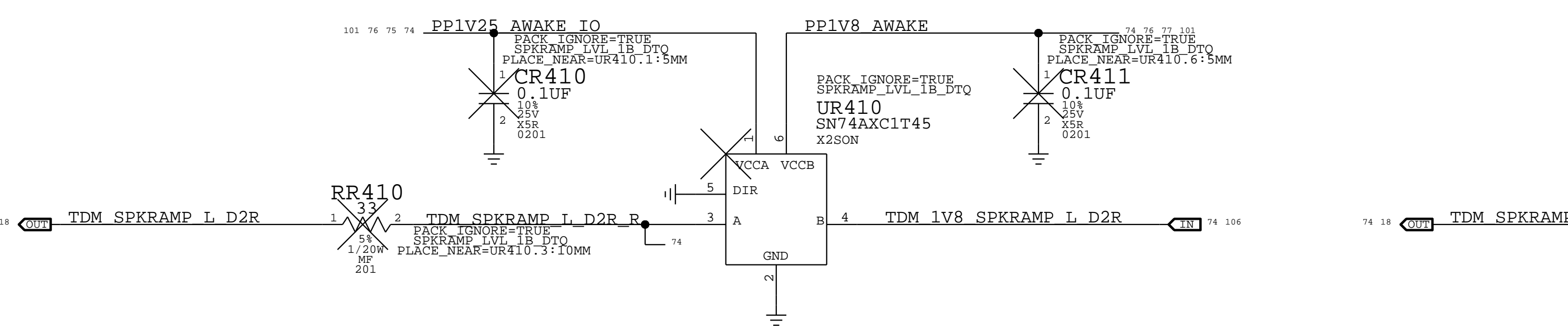
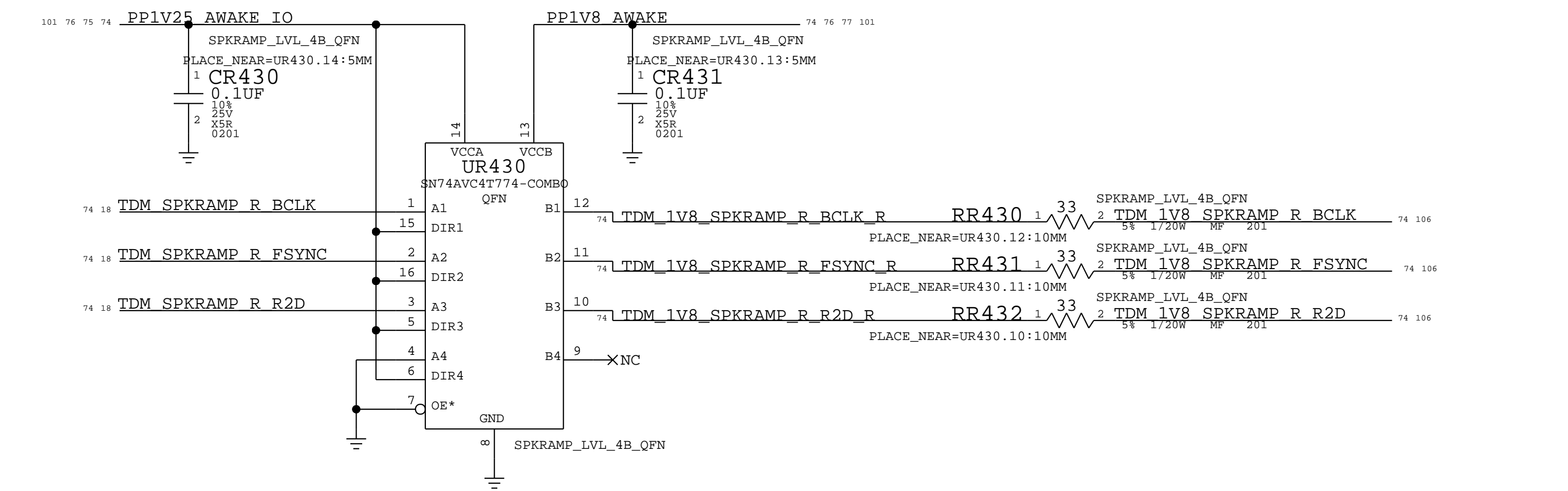
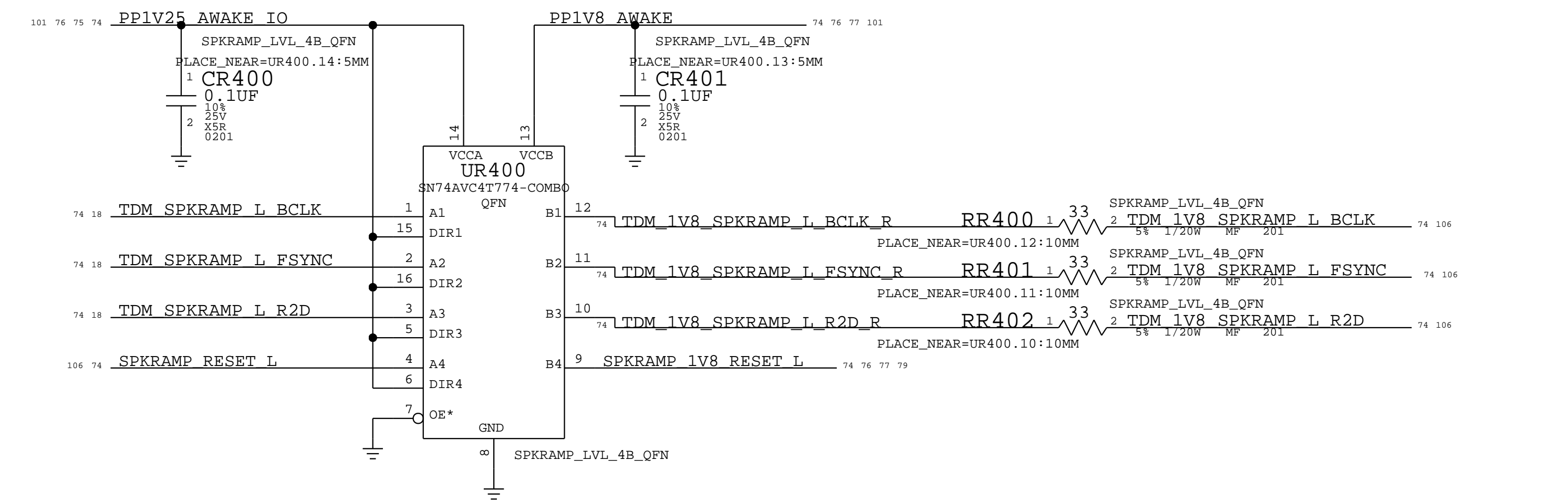
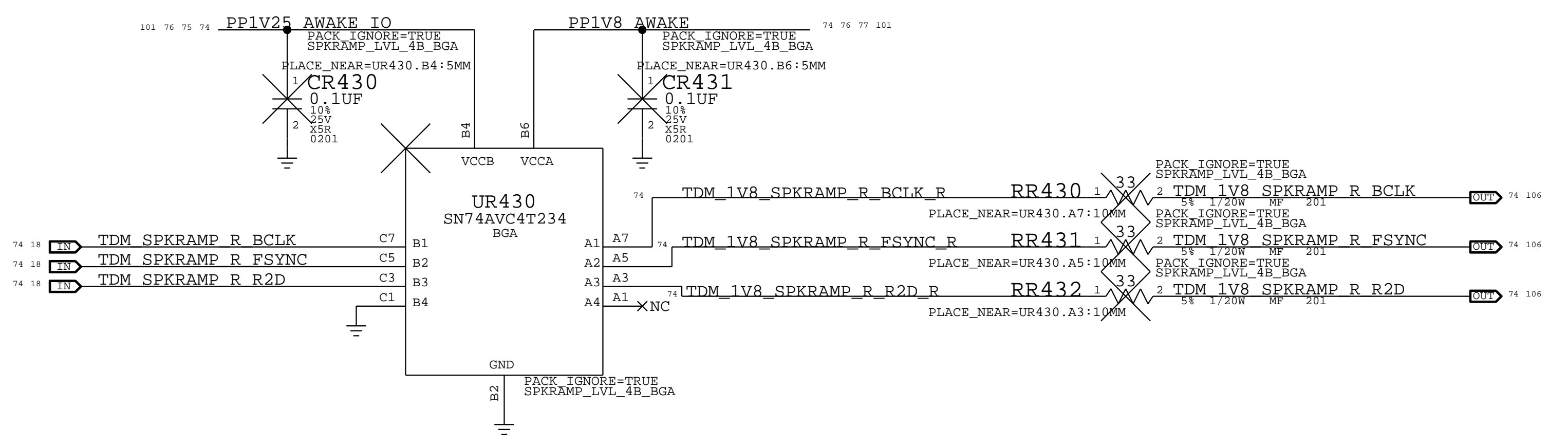
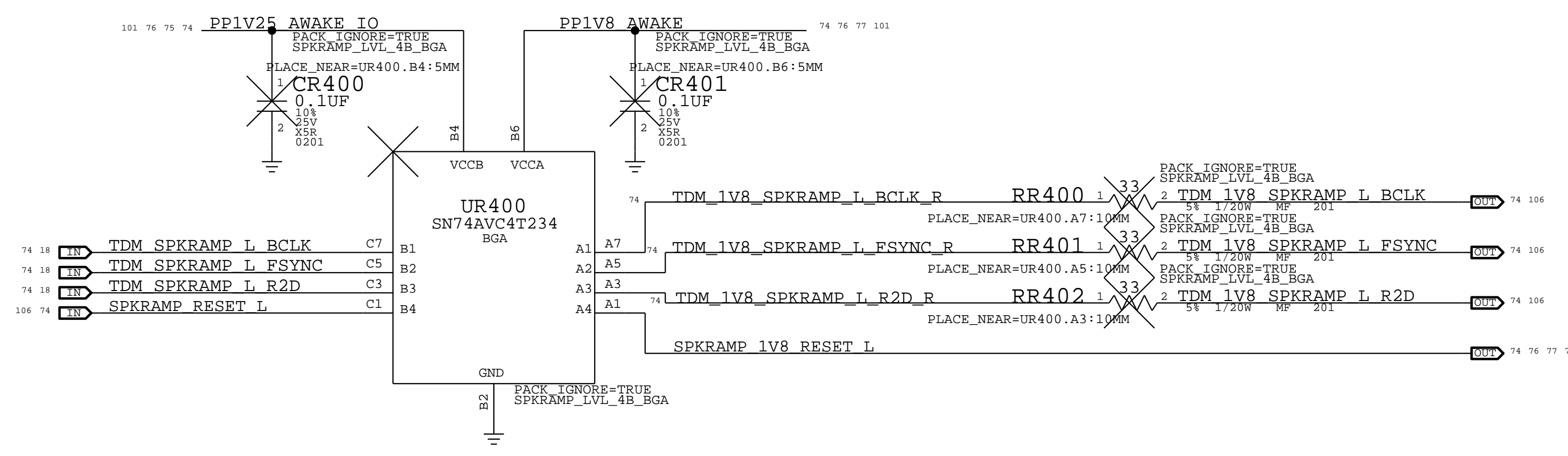
PAGE TITLE: SECDIS: FPGA

Apple Inc.

DRAWING NUMBER: 051-05399	SIZE: D
REVISION: 9.0.0	
BRANCH: dvt-1	
PAGE: 243 OF 999	
SHEET: 73 OF 117	

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BOM_COST_GROUP=SOC



AUDIO
1.2V <-> 1.8V
LEVEL SHIFTERS

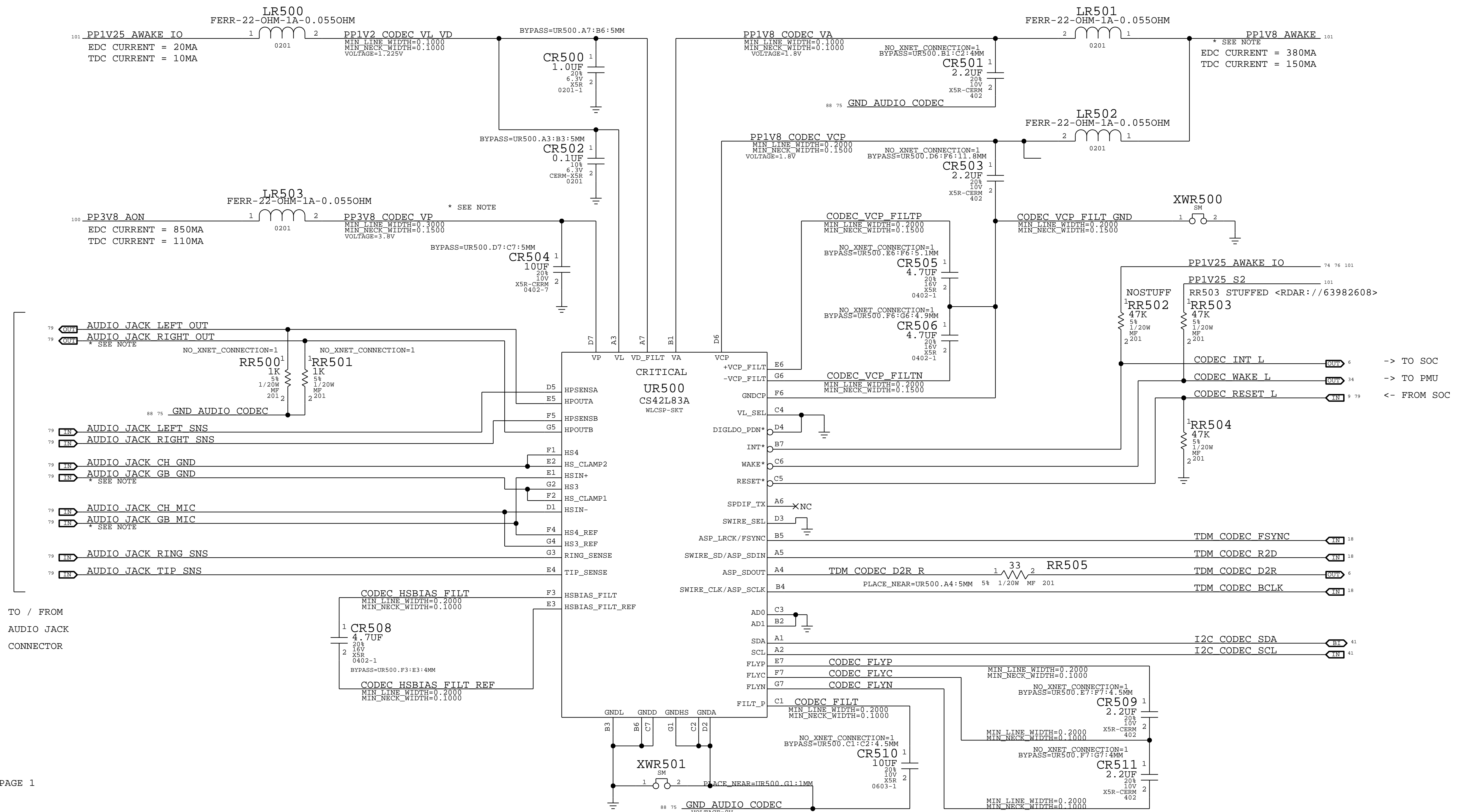
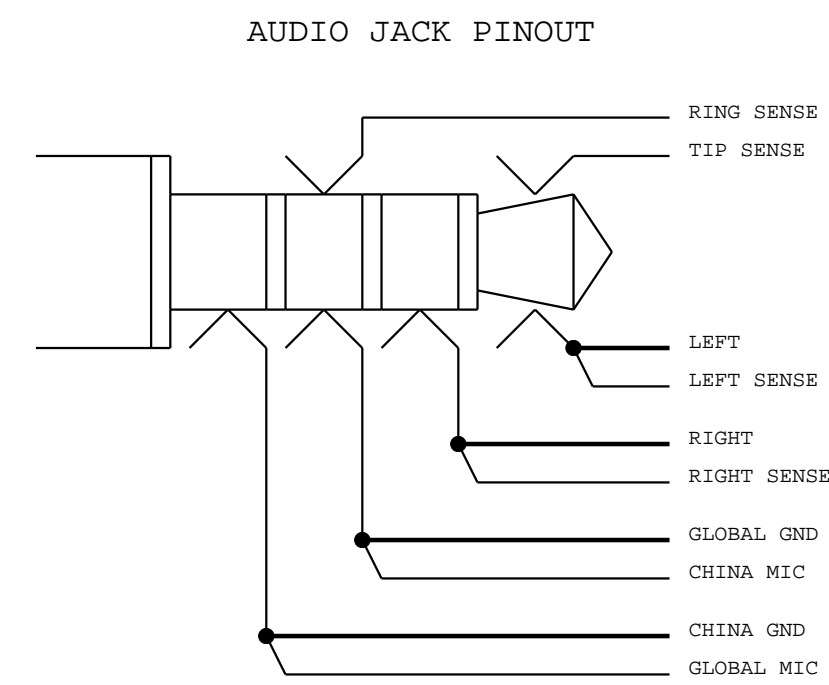
MAX PROP DELAY:
 TP (4-BIT) + TP (1-BIT) < 35 NS

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PAGE TITLE			
AUDIO SUPPORT			
		DRAWING NUMBER	051-05399
		REVISION	9.0.0
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		PAGE	244 OF 999
		SHEET	74 OF 117

*** OK2INTEGRATE ***

AUDIO JACK CODEC	I2C ADDRESS	
AD1	AD0	ADDRESS
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B

CHANGES FROM PREVIOUS DESIGNS:
 - REMOVED LDO TO GENERATE LOCAL 1.8V <RDAR://50645294>
 - CHANGED VL SUPPLY FROM 1.8V TO 1.2V <RDAR://TBD>
 - SUPPLIED VD_FILT EXTERNALLY <RDAR://TBD>
 - CHANGED VP SUPPLY FROM 3.3V TO 3.8V <RDAR://TBD>



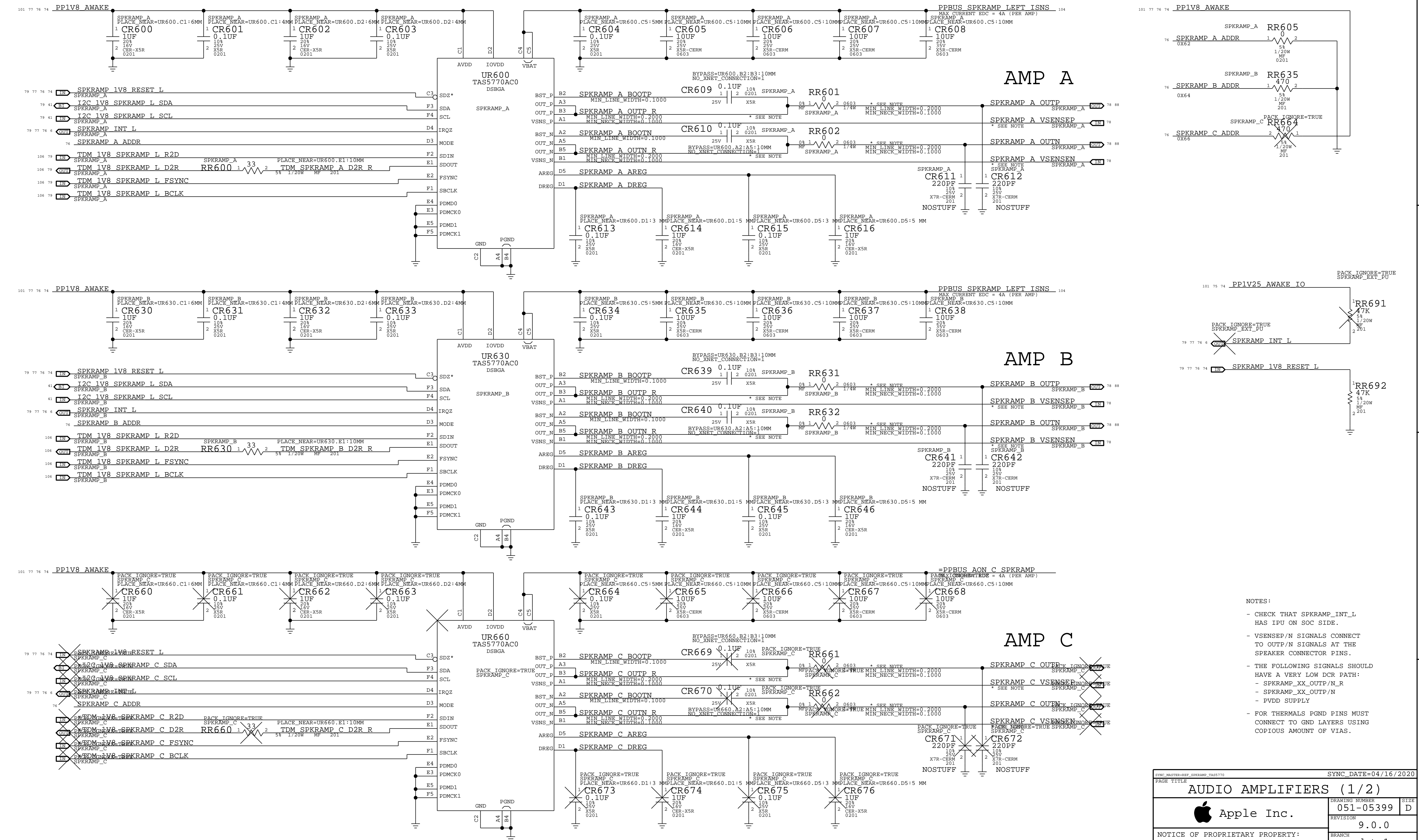
TO / FROM
AUDIO JACK
CONNECTOR

- NOTES:
- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1
 - THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
 - VP SUPPLY
 - VCP SUPPLY
 - AUDIO_JACK_LEFT/RIGHT_OUT
 - AUDIO_JACK_GB/CH_GND
 - GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.
 - VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP WHEN THE OTHER RAILS GO DOWN)
 - VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
 - 3.1UA (1V8 OFF, RST# LOW)
 - 3.6UA (1V8 ON, RST# LOW)
 - 36UA (1V8 ON, RST# HIGH)

SYNC_MASTER=REF_CODEX_CLIFDEN		SYNC_DATE=04/13/2020	
PAGE TITLE			
AUDIO JACK CODEC			
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		REVISION	9.0.0
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		PAGE	245 OF 999
		SHEET	75 OF 117

BOM_COST_GROUP=AUDIO

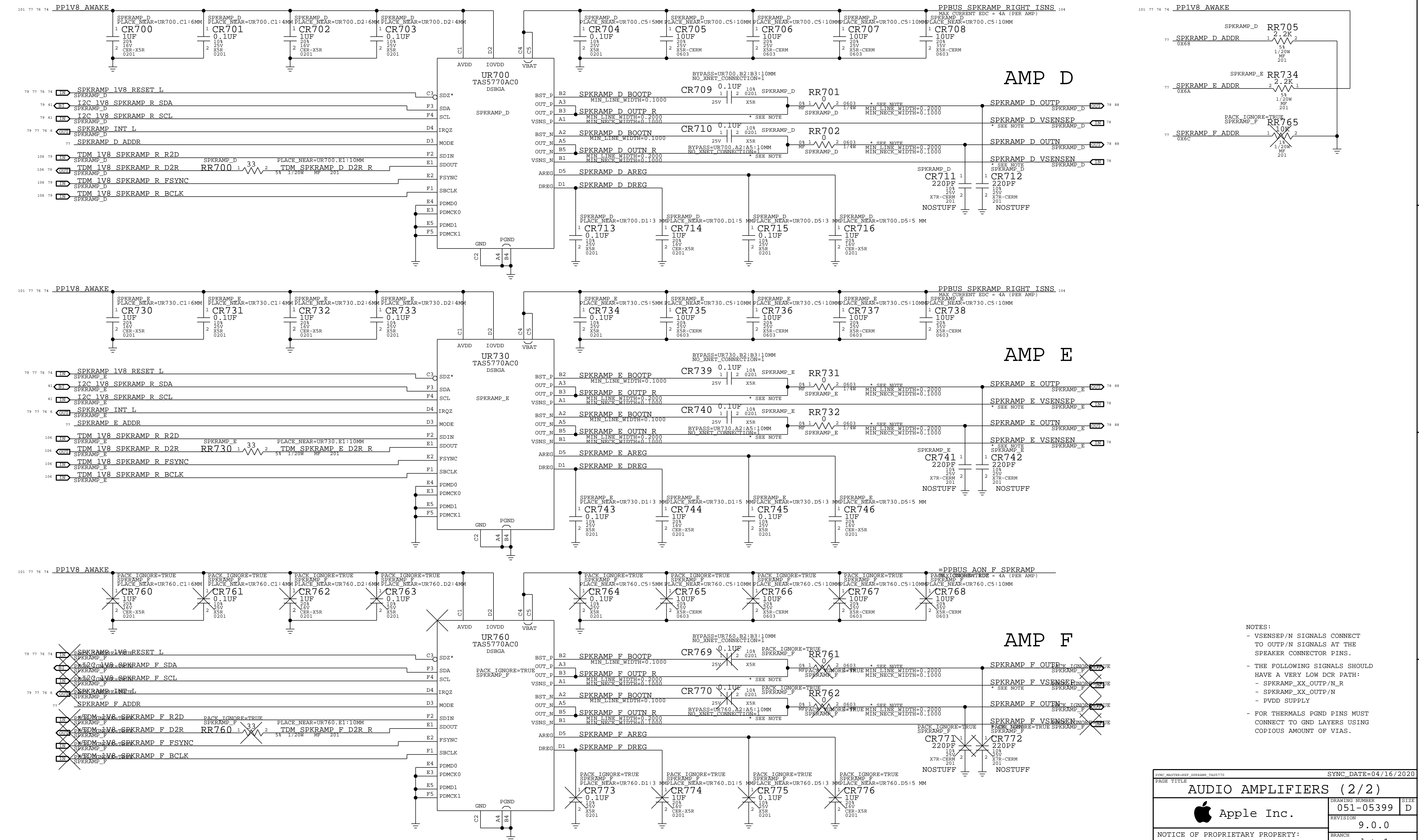
*** OK2INTEGRATE ***



- NOTES:
- CHECK THAT SPKRAMP_INT_L HAS IPU ON SOC SIDE.
 - VSENSE/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
 - THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
 - SPKRAMP_XX_OUTP/N_R
 - SPKRAMP_XX_OUTP/N
 - PVDD SUPPLY
 - FOR THERMAL PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

SYNC_MASTER=REF_SPKRAMP_TAS5770		SYNC_DATE=04/16/2020	
PAGE TITLE			
AUDIO AMPLIFIERS (1/2)		DRAWING NUMBER	SIZE
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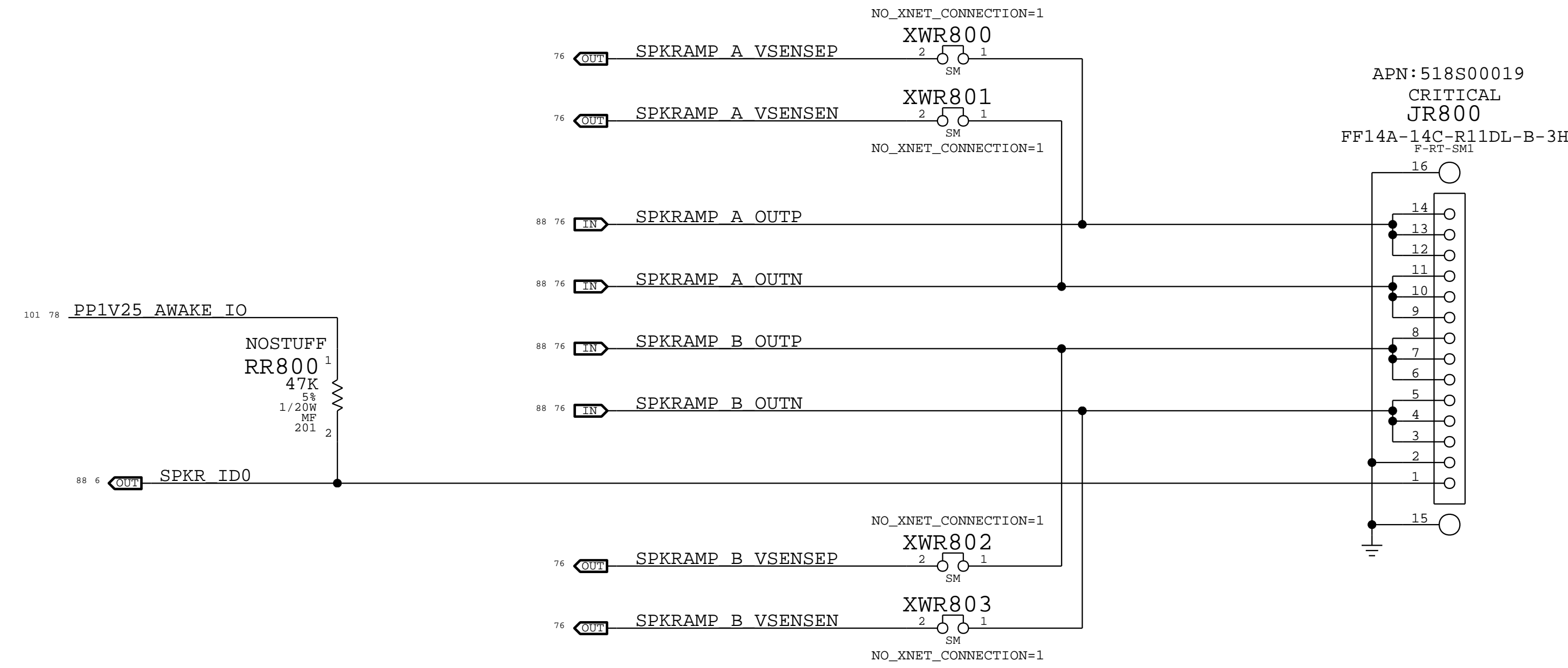
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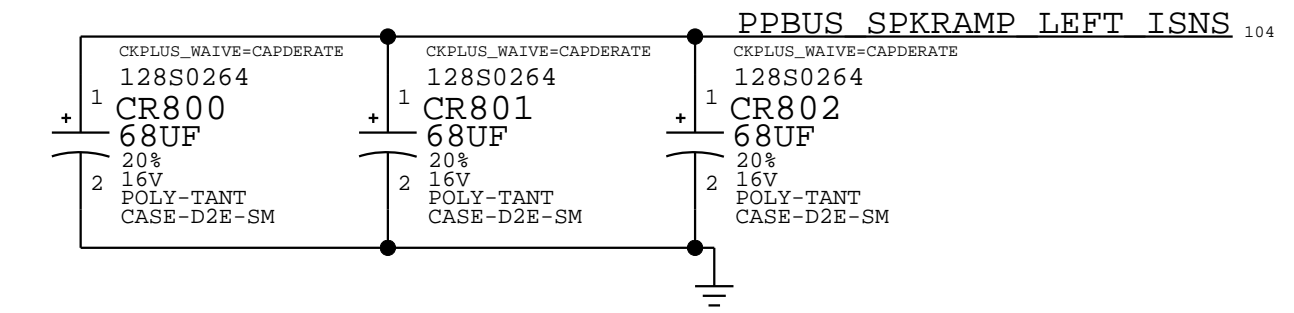
- NOTES:
- VSENSE/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
 - THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
 - SPKRAMP_XX_OUTP/N_R
 - SPKRAMP_XX_OUTP/N
 - PVDD SUPPLY
 - FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

SYNC_MASTER=REF_SPKRAMP_TAS5770		SYNC_DATE=04/16/2020	
PAGE TITLE			
AUDIO AMPLIFIERS (2/2)		DRAWING NUMBER	SIZE
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		REVISION	9.0.0
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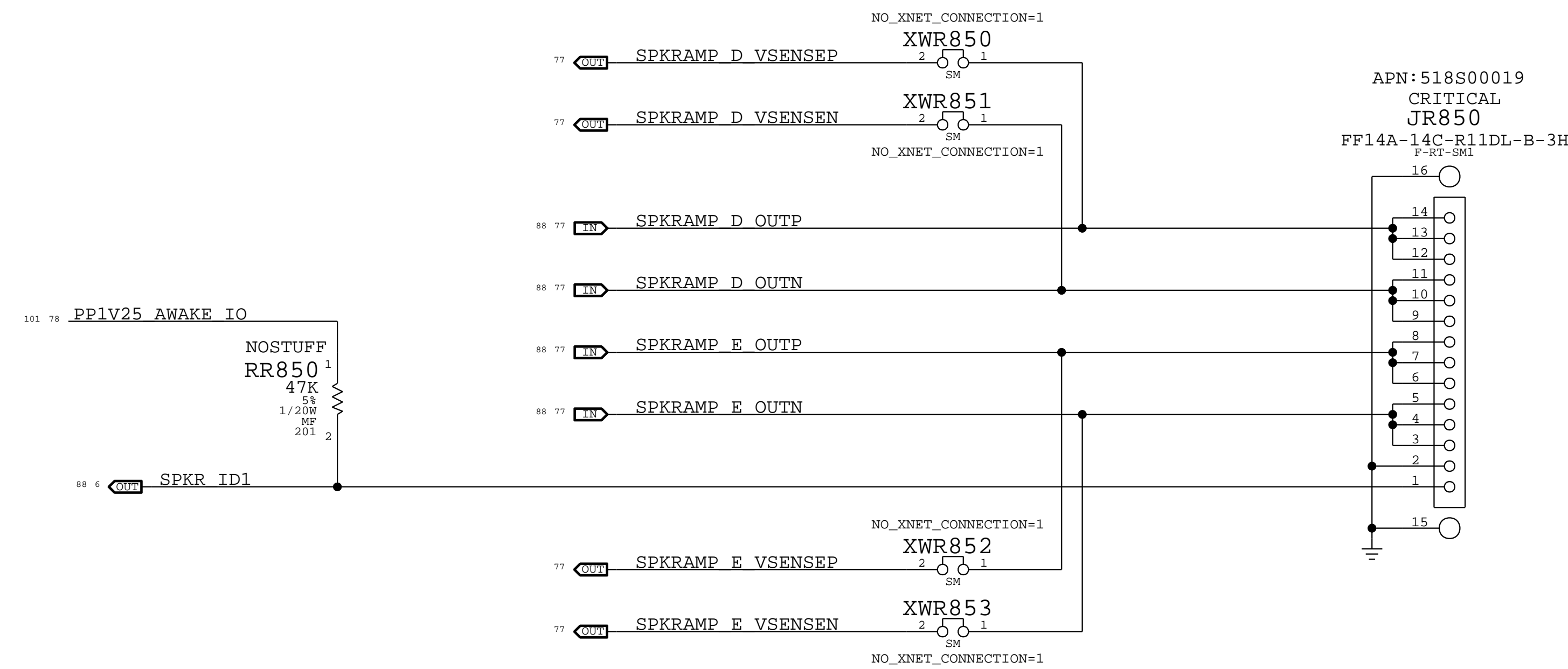
LEFT AUDIO AMP CONNECTOR



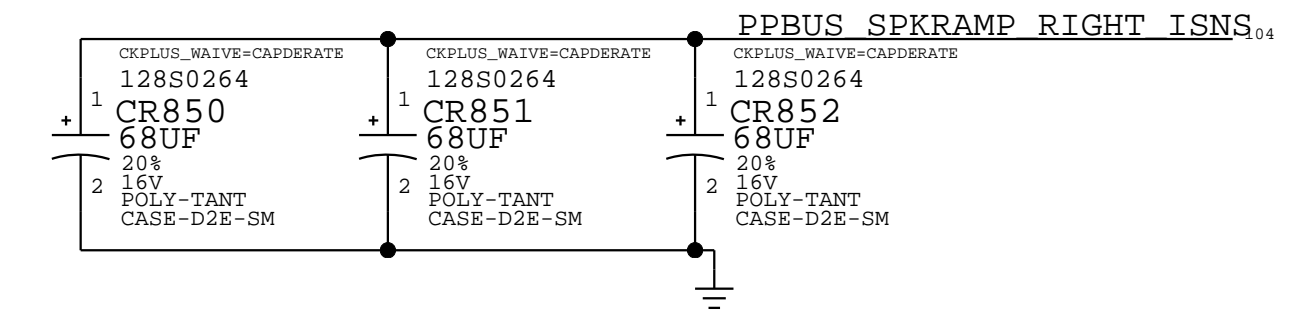
LEFT AUDIO AMP PBUS BULK CAPS



RIGHT AUDIO AMP CONNECTOR



RIGHT AUDIO AMP PBUS BULK CAPS

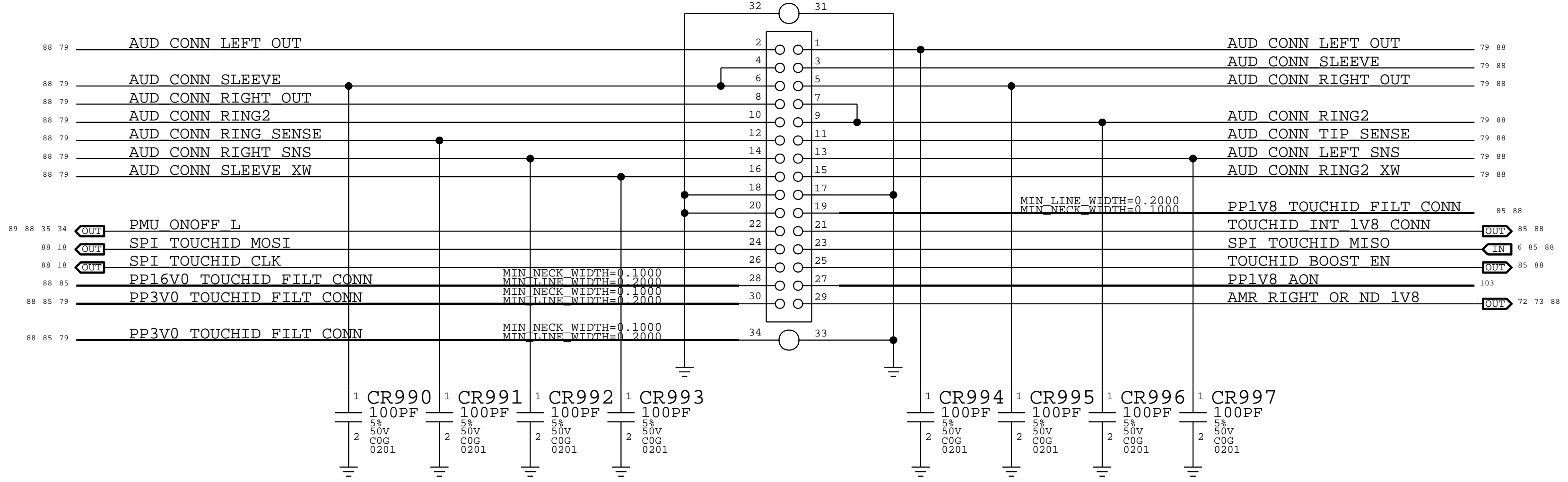


PAGE TITLE		
AUDIO CONNECTORS: AMPS		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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	PAGE	248 OF 999
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AUDIO JACK FLEX CONNECTOR

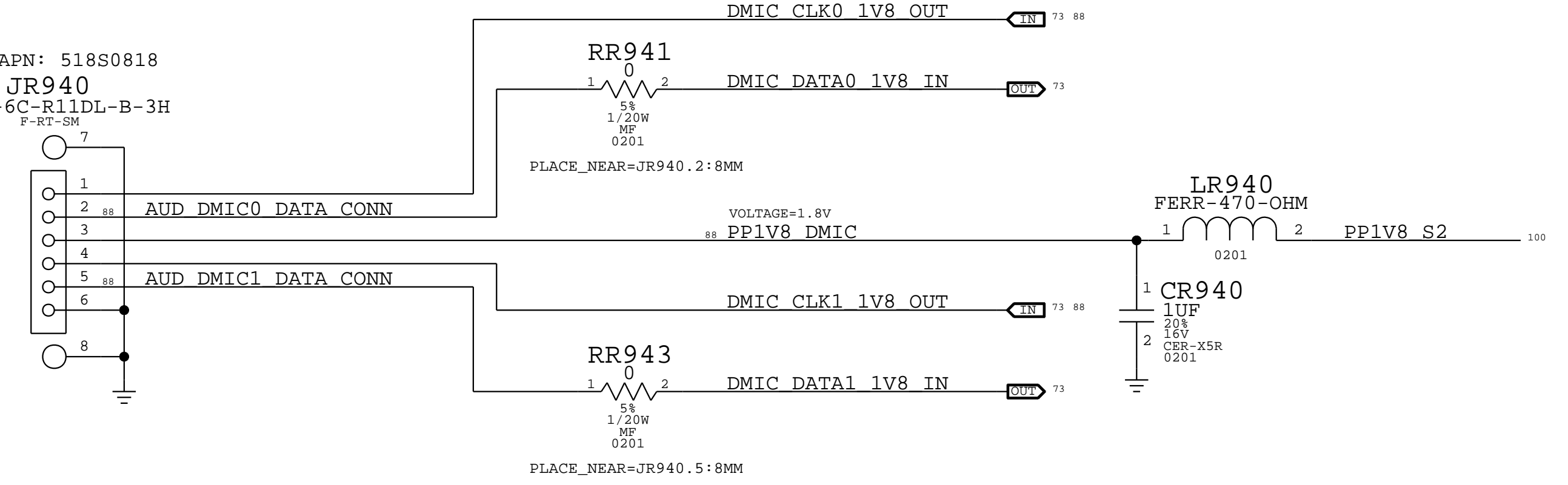
APN: 516S1064
MATES WITH APN: 516S0573 ON FLEX

JR900
51338-0374
F-ST-SM

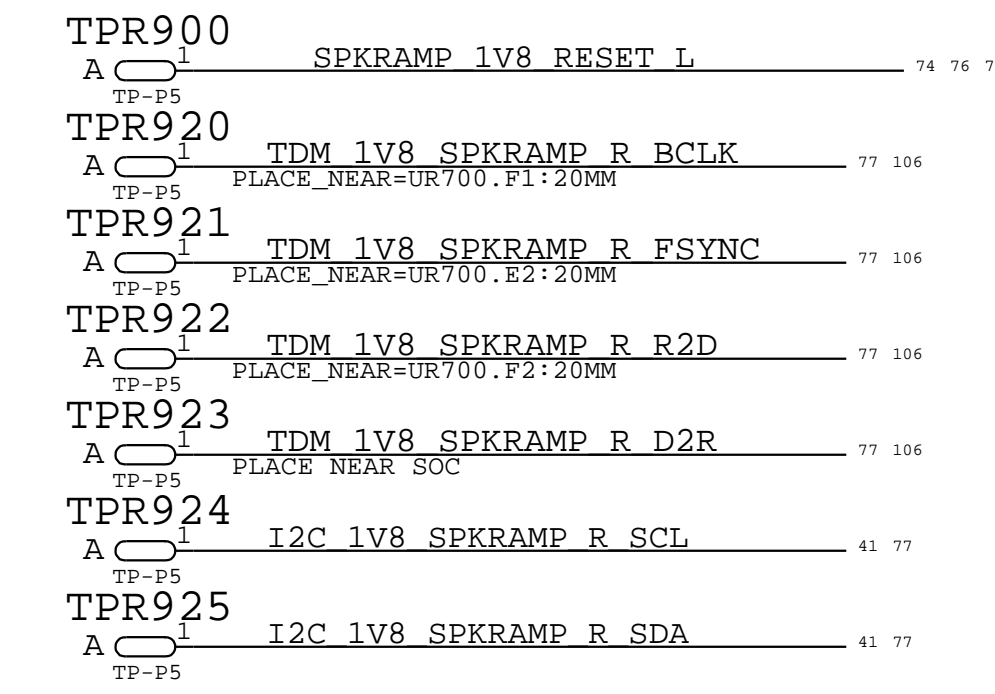
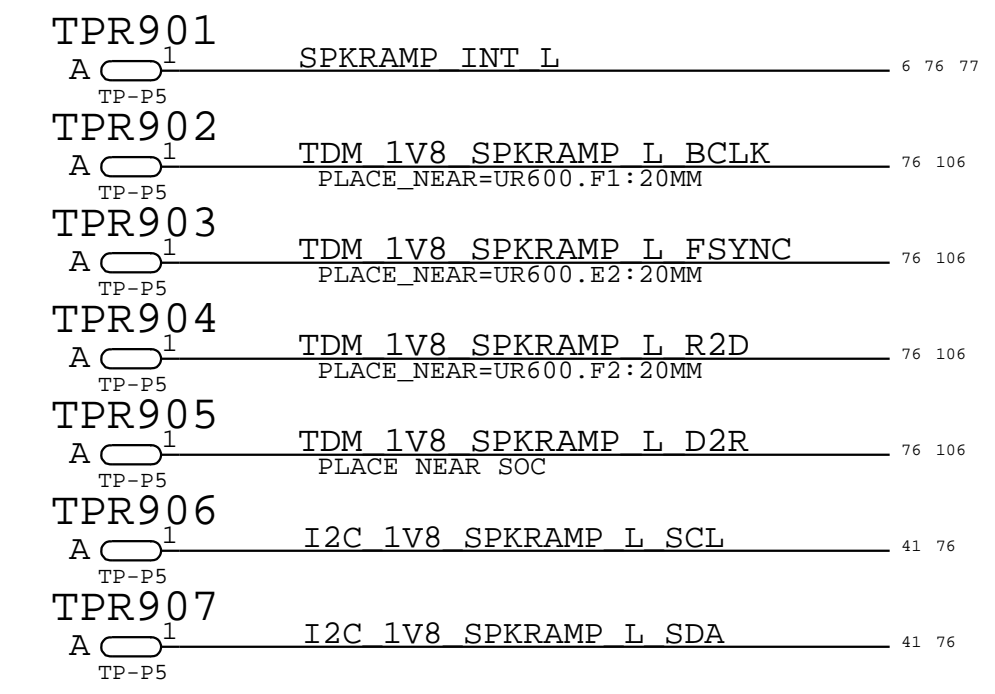
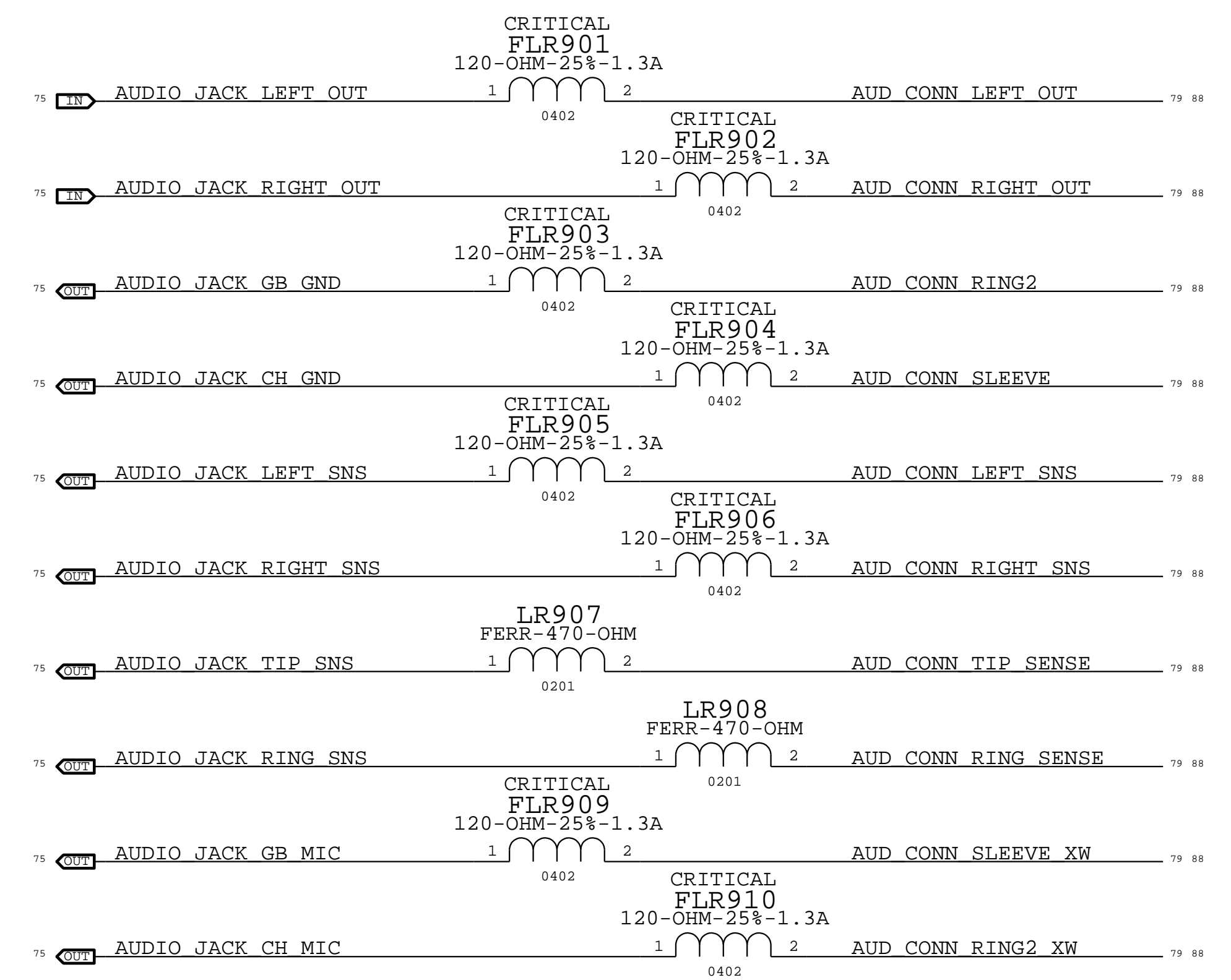
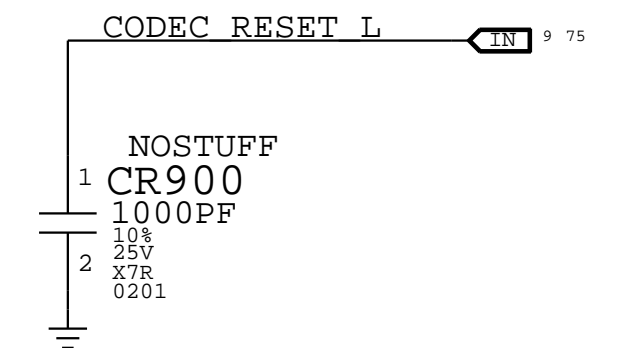


DIGITAL MIC FLEX CONNECTOR

APN: 518S0818
JR940
FF14A-6C-R11DL-B-3H
F-RT-SM



ESD: PROJECT DEPENDENT



PAGE TITLE AUDIO CONNECTORS: DMIC, JACK		
	DRAWING NUMBER 051-05399	SIZE D
	REVISION 9.0.0	BRANCH dvt-1
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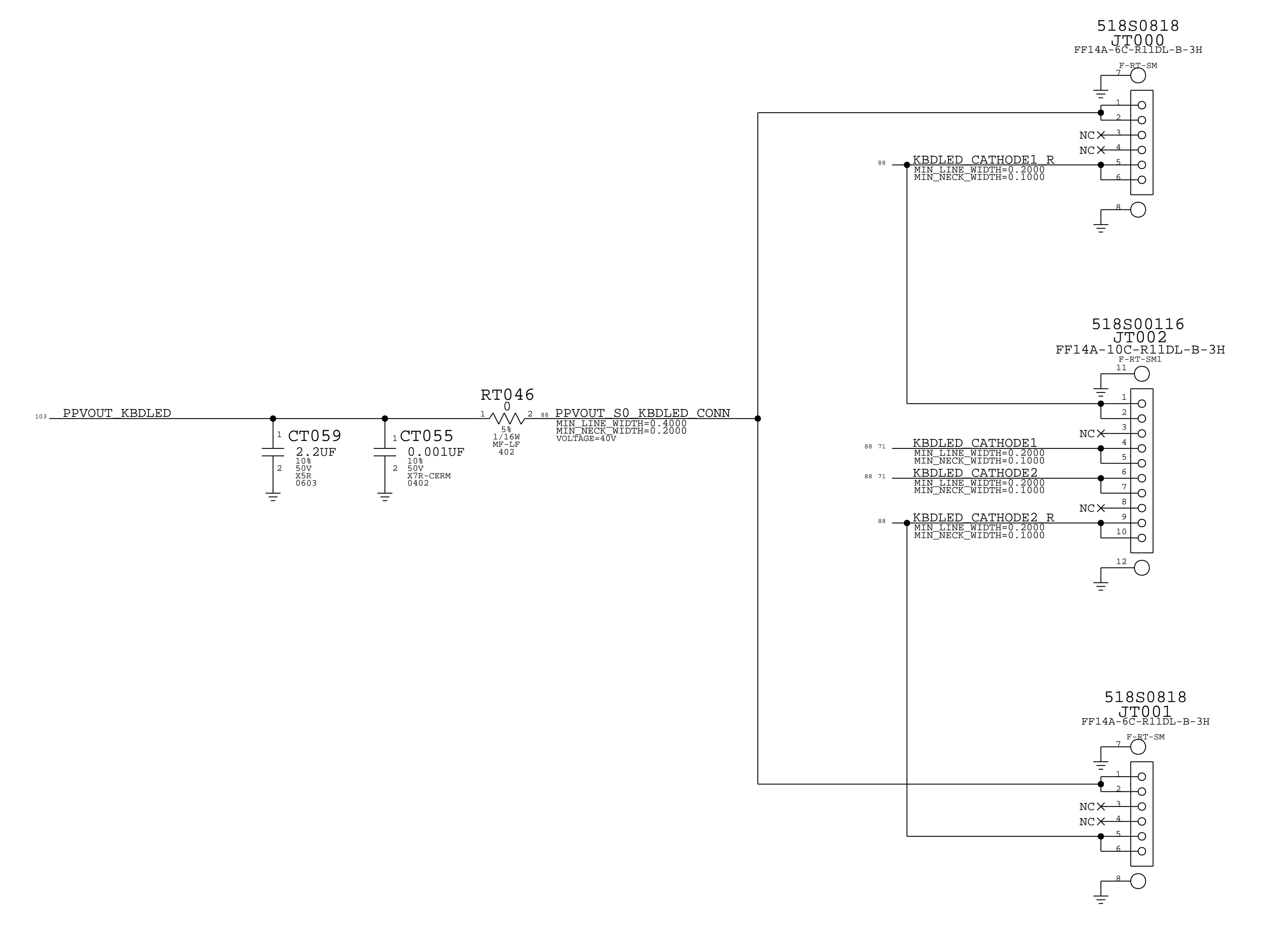
8 7 6 5 4 3 2 1

D

C

B

A



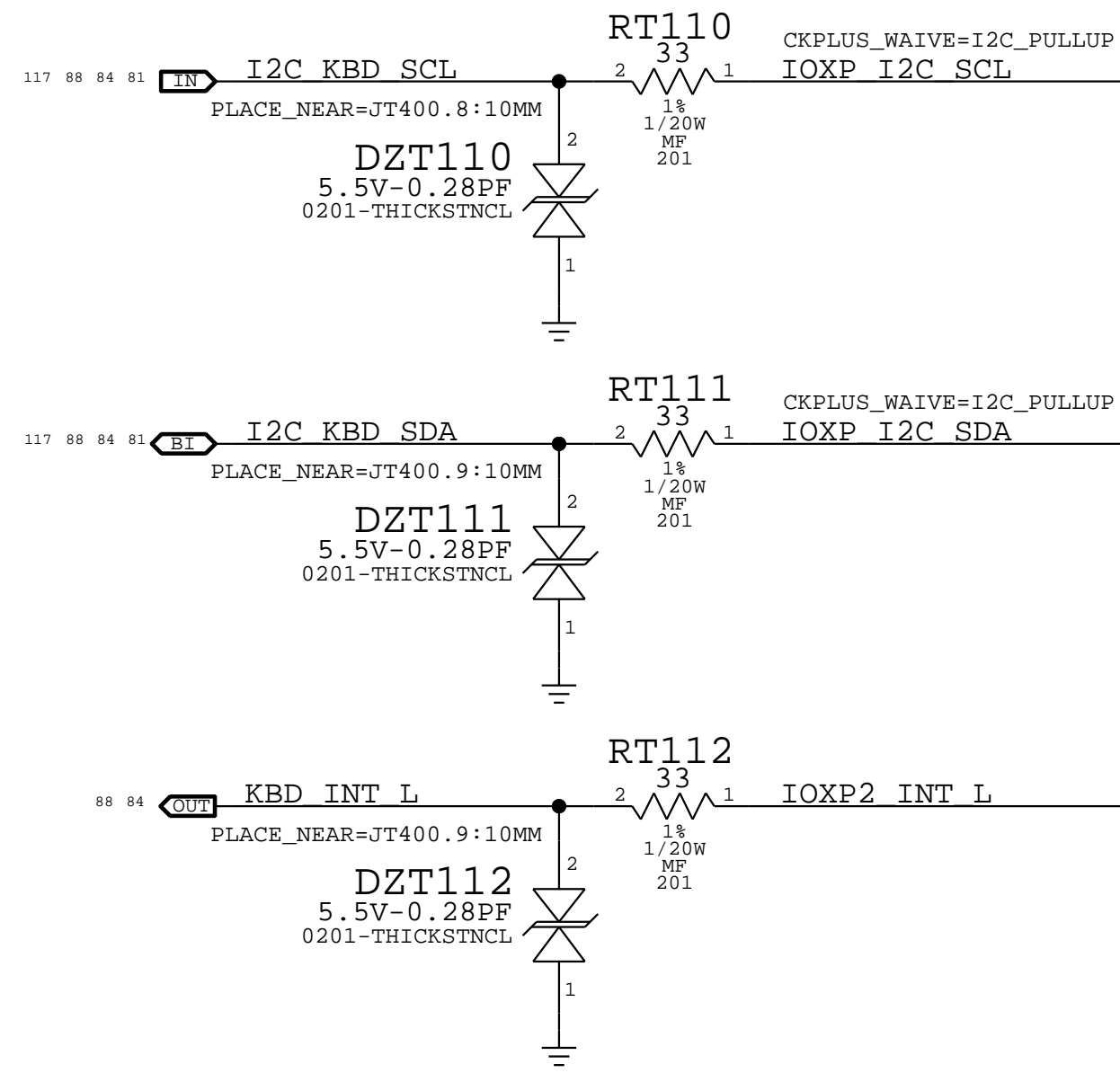
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PAGE TITLE KEYBOARD BLC CONNECTORS			
Apple Inc.	DRAWING NUMBER	051-05399	SIZE D
	REVISION	9.0.0	
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	PAGE	250 OF 999	
	SHEET	80 OF 117	

BOM_COST_GROUP=DISPLAY

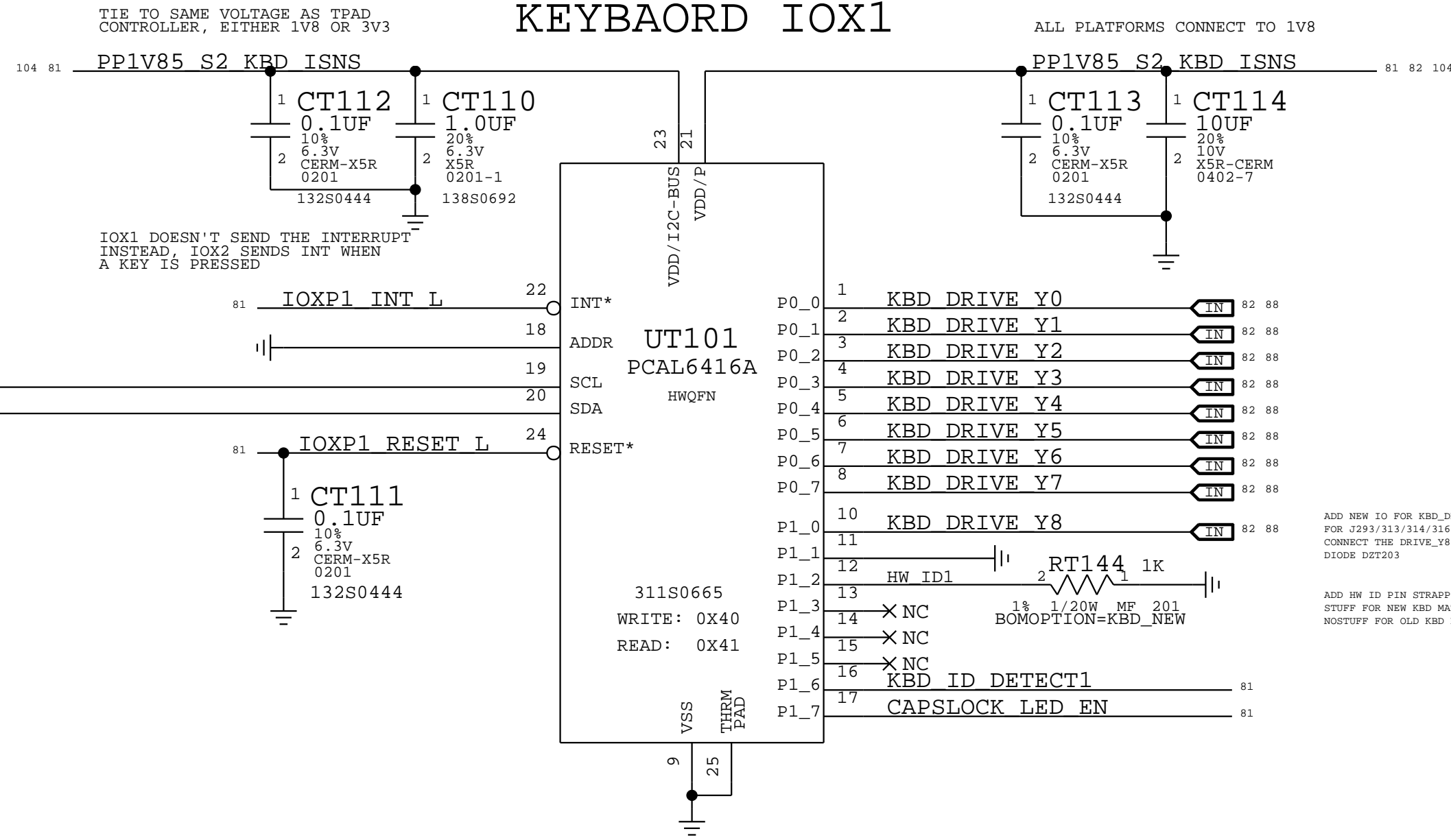
8 7 6 5 4 3 2 1

*** OK2PLACE ***

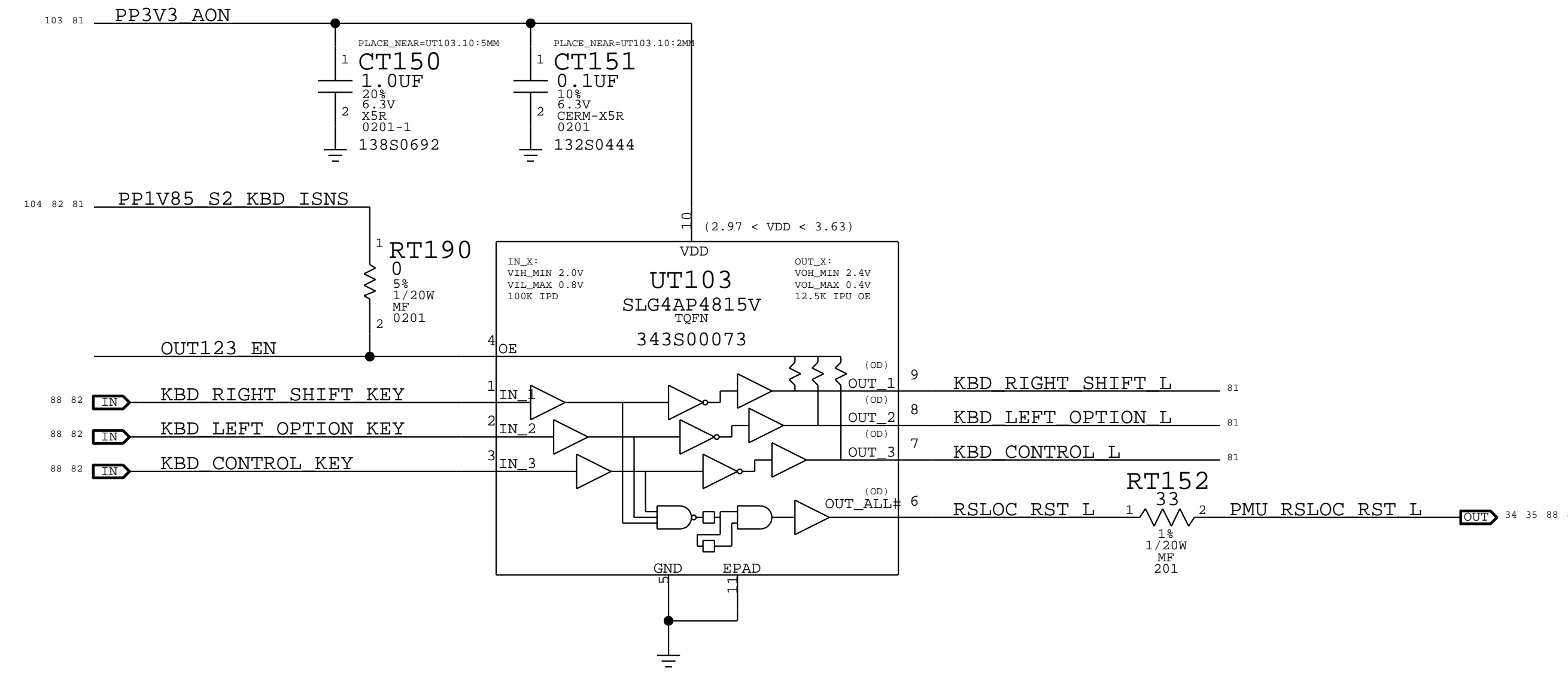
TO/FROM TRACKPAD



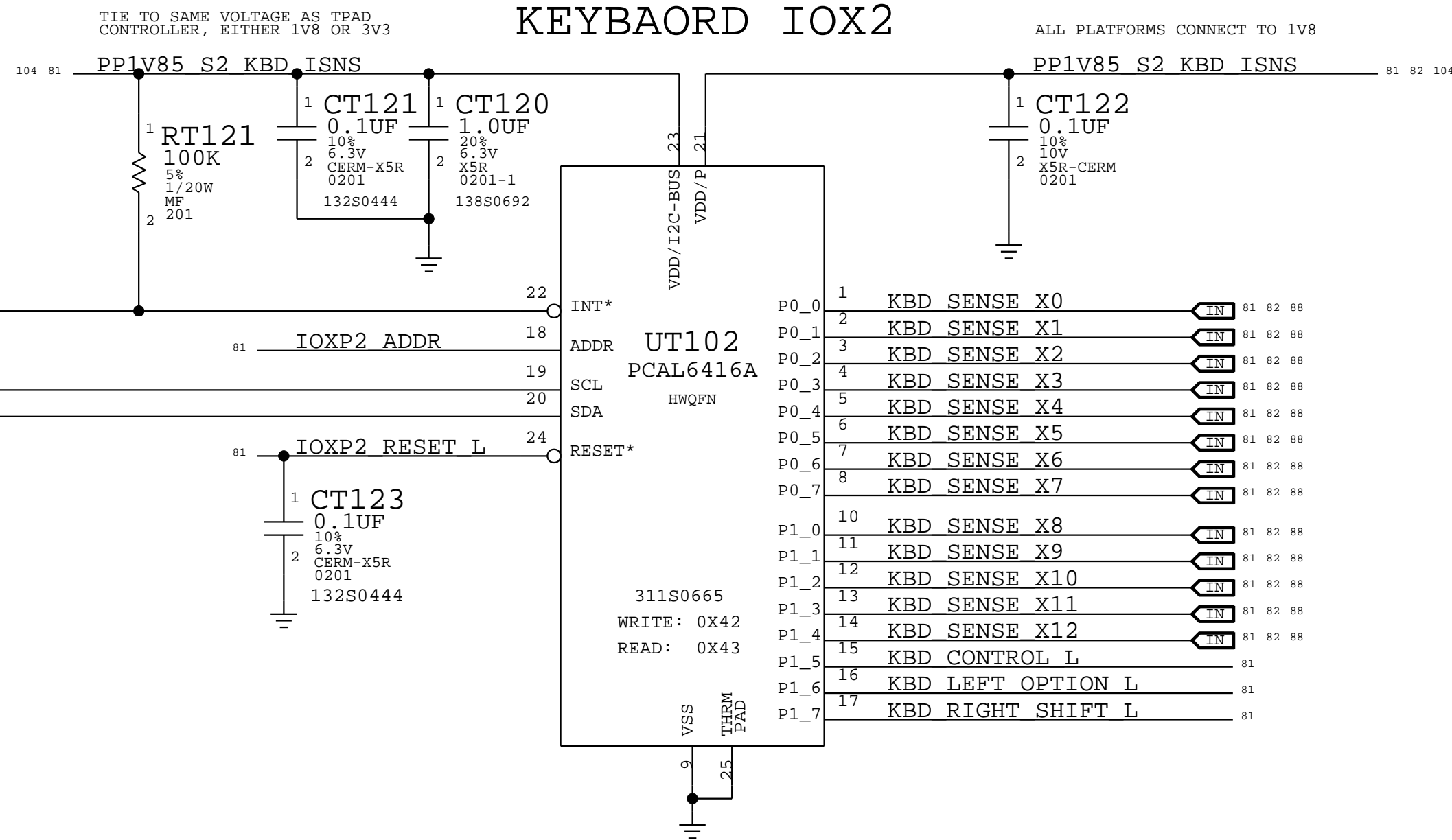
KEYBOARD IOX1



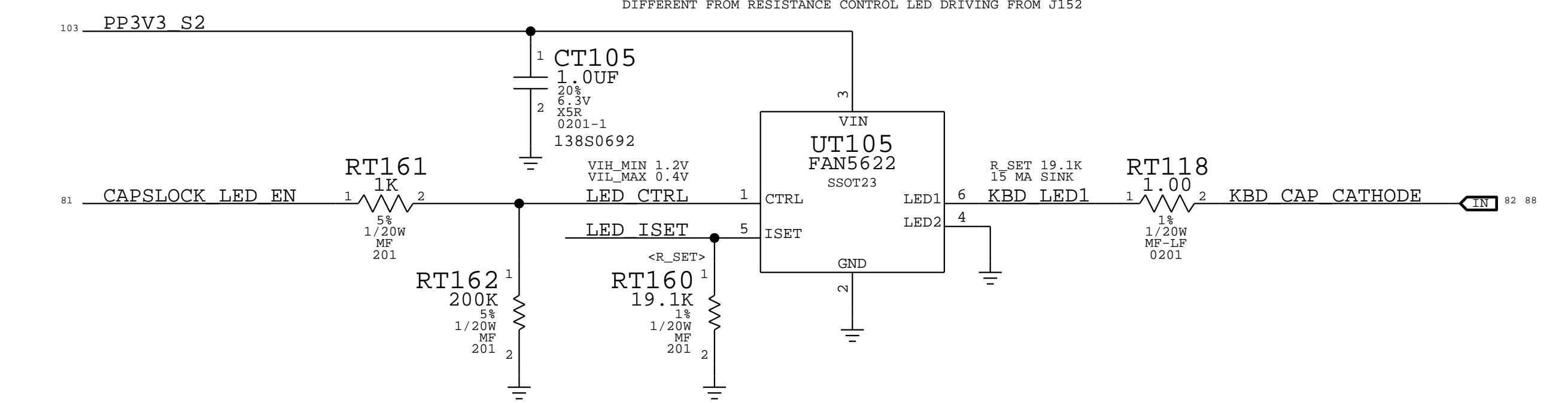
3.3V RSLOC ISOLATION KEYS/ASIC RESET



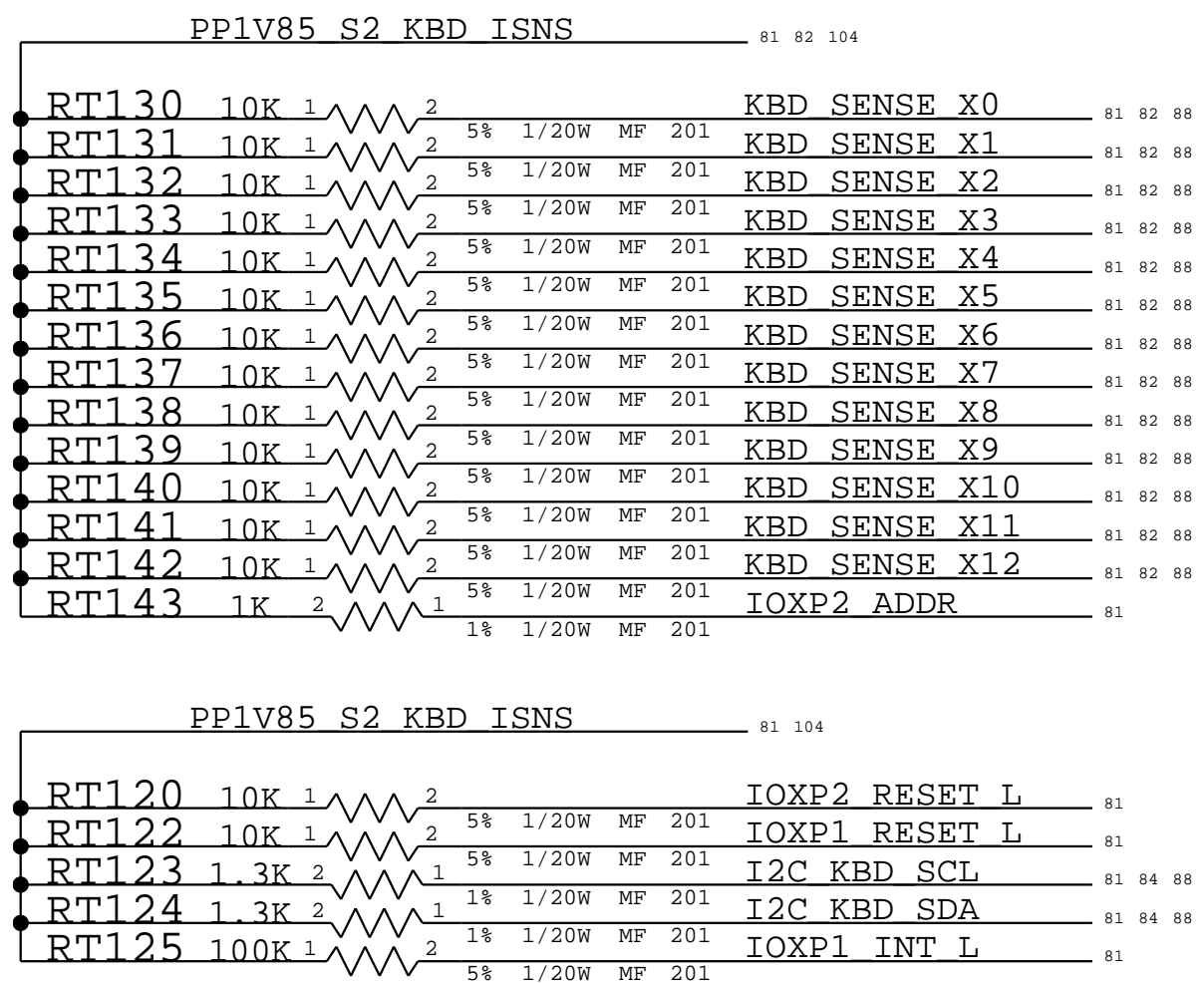
KEYBOARD IOX2



CAPSLOCK LED DRIVER



3V3 KBD CONN SERIES R



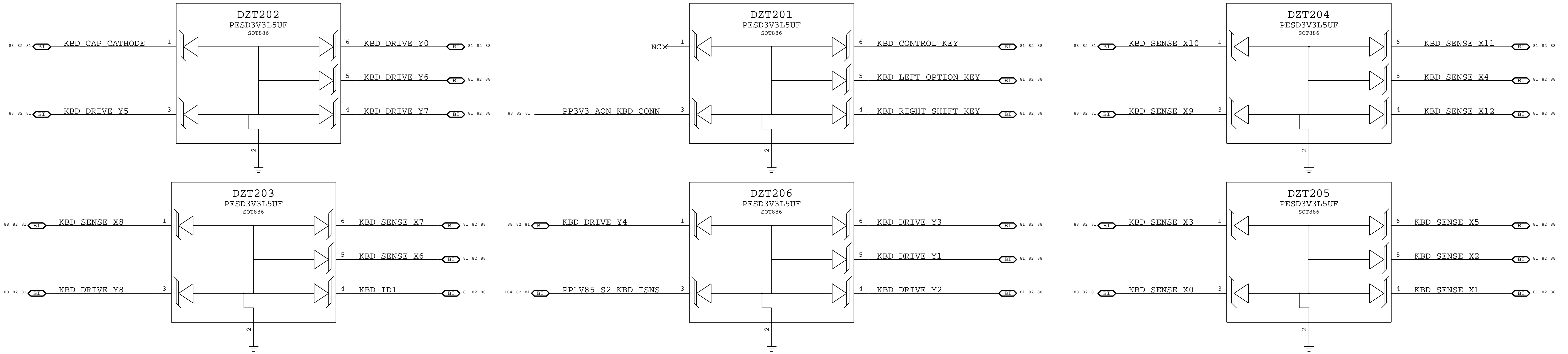
ID_DETECT SERIES R



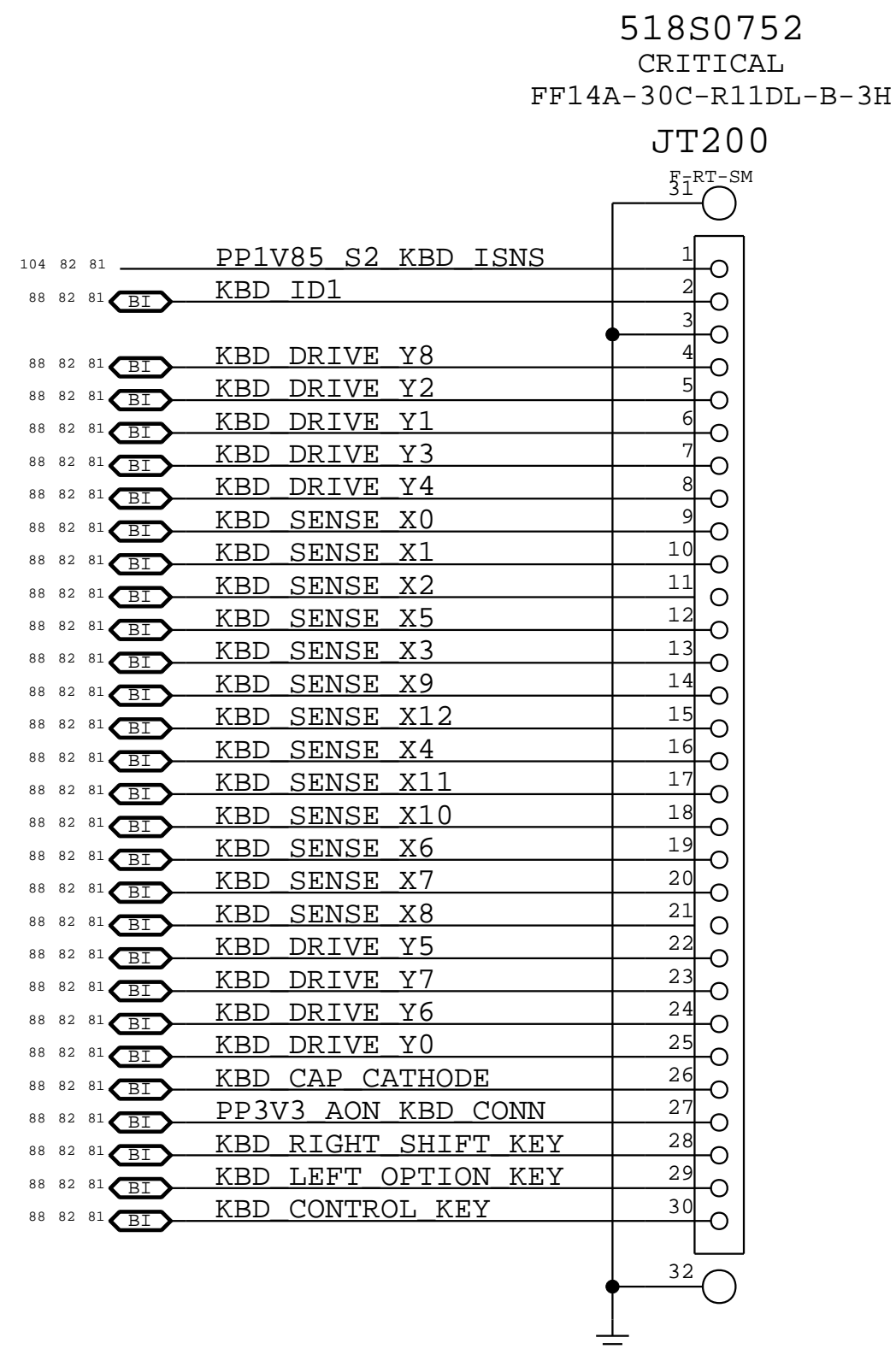
SYNC_MASTER=WUDI_T668_MLB		SYNC_DATE=06/16/2020	
PAGE TITLE			
KEYBOARD IOX, SUPPORT			
		DRAWING NUMBER	051-05399
		REVISION	9.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		BRANCH	dvt-1
		PAGE	251 OF 999
		SHEET	81 OF 117

BOM_COST_GROUP=KEYBOARD

KEYBOARD ESD



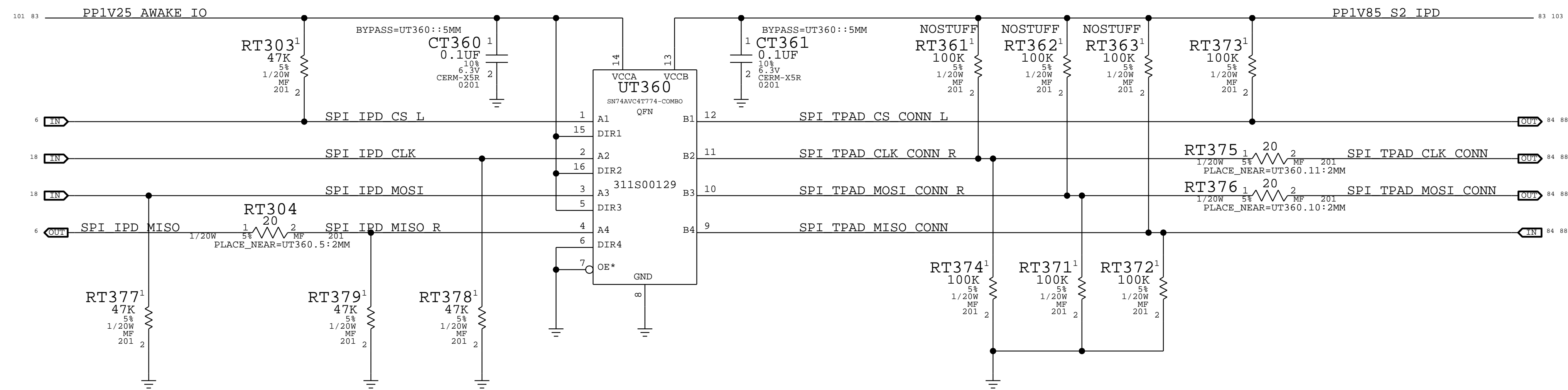
MEMBRANE ZIF CONNECTOR



PAGE TITLE		KEYBOARD SIGNAL CONNECTOR, ESD	
DRAWING NUMBER		051-05399	SIZE
REVISION		9.0.0	D
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		PAGE	252 OF 999
		SHEET	82 OF 117

BOM_COST_GROUP=KEYBOARD

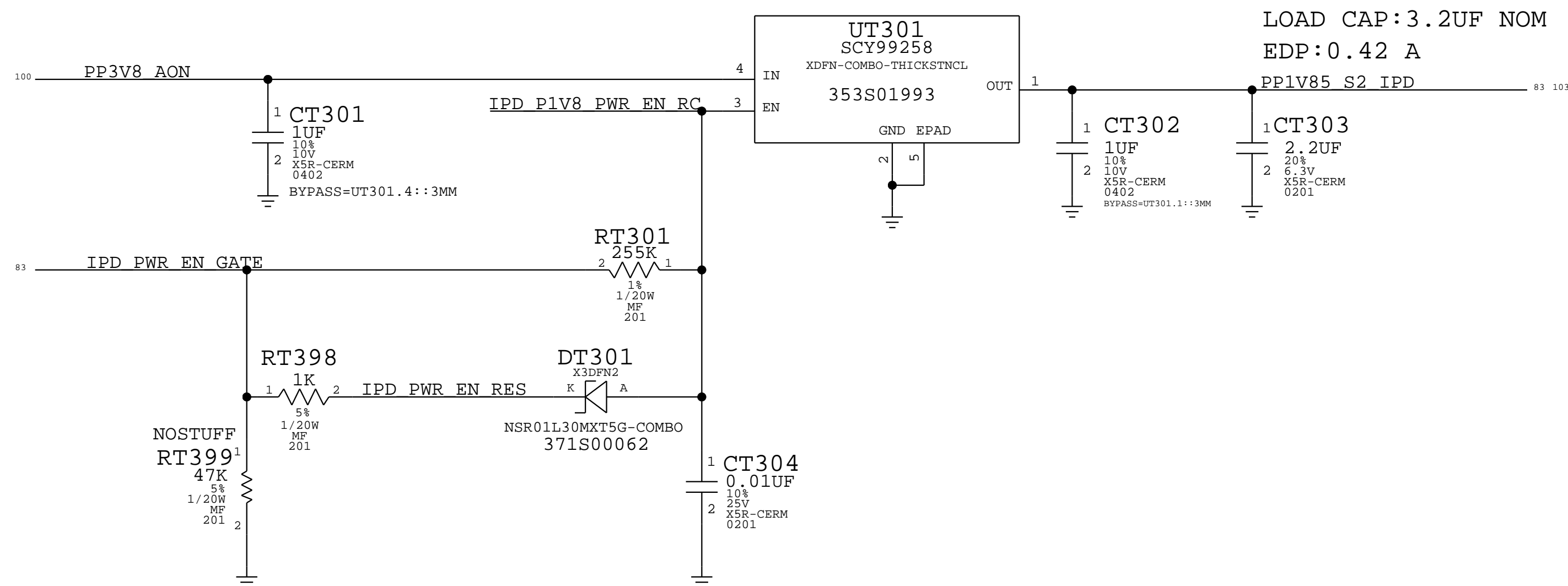
TRACKPAD SPI BUS LEVEL SHIFTER (+1.2V TO +1.8V)



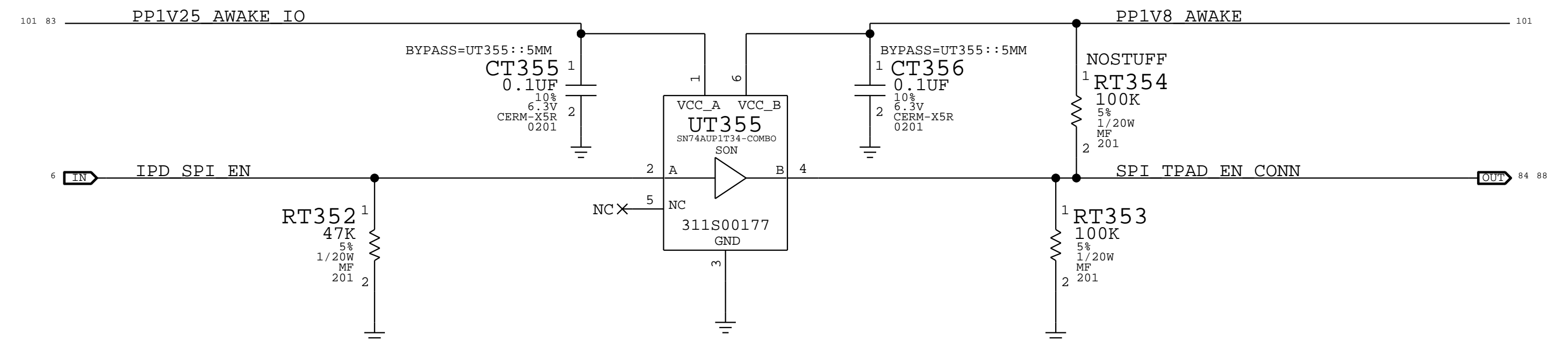
SN74AVC4T774 Truth Table

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

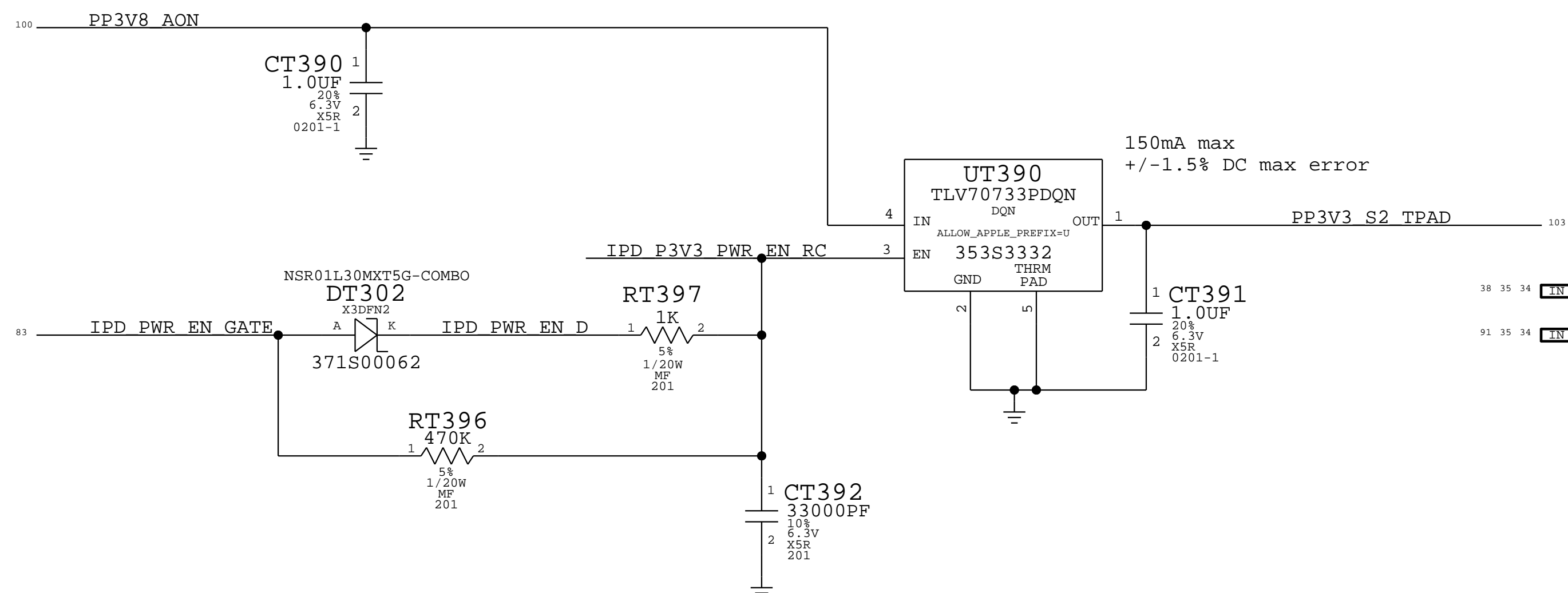
IPD LDO 1.85 V FOR TRACKPAD AND KEYBOARD IOX



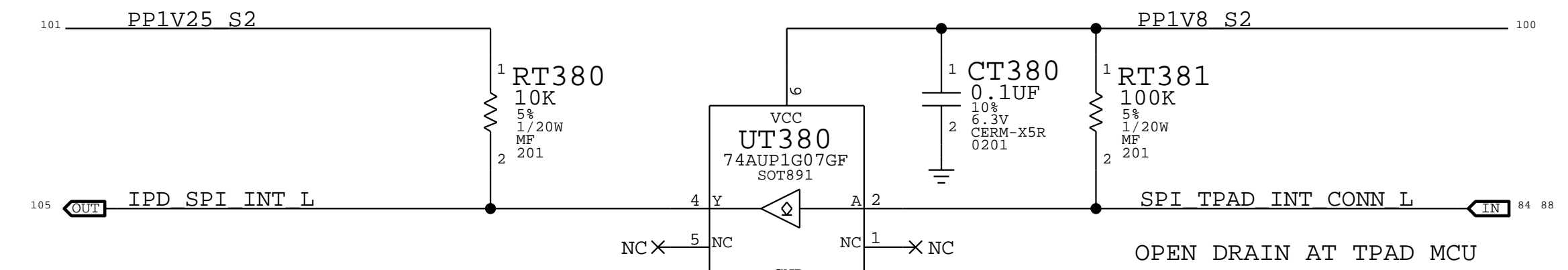
TRACKPAD SPI ENABLE LEVEL SHIFTER



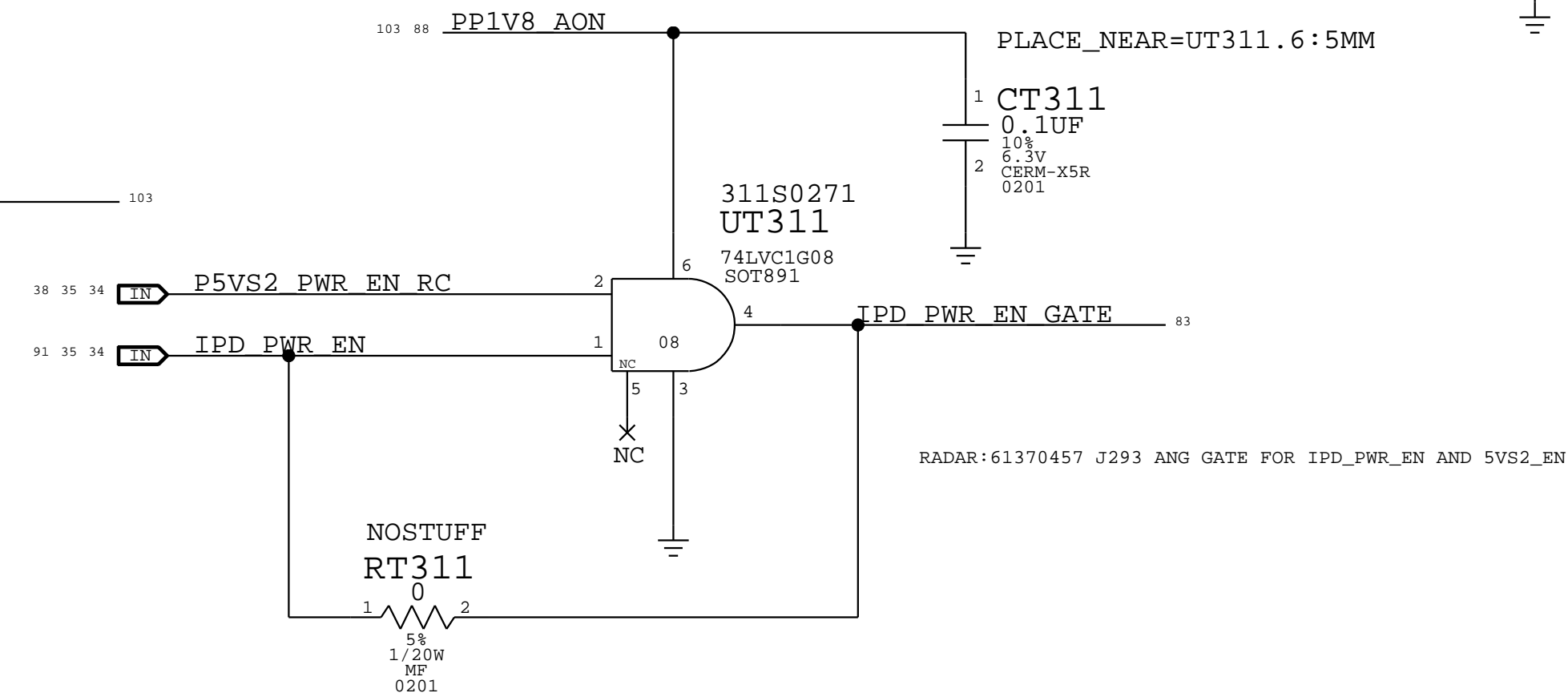
3.3V S2 LDO FOR TPAD



IPD SPI INTERRUPT LEVEL SHIFTER



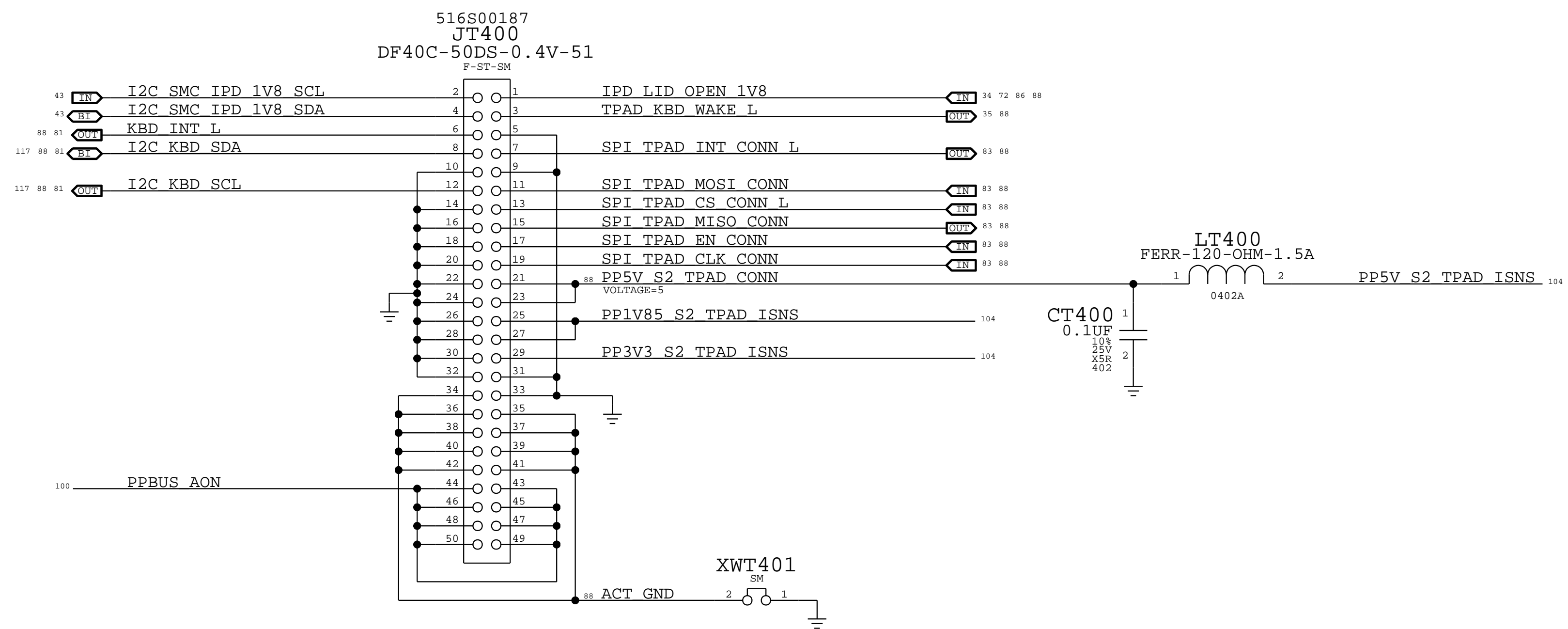
AND GATE FOR IPD_PWR_EN



TRACKPAD SUPPORT		
Apple Inc.		
DRAWING NUMBER	051-05399	SIZE
REVISION	9.0.0	D
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MATES WITH 518S00080 ON TRACKPAD FLEX

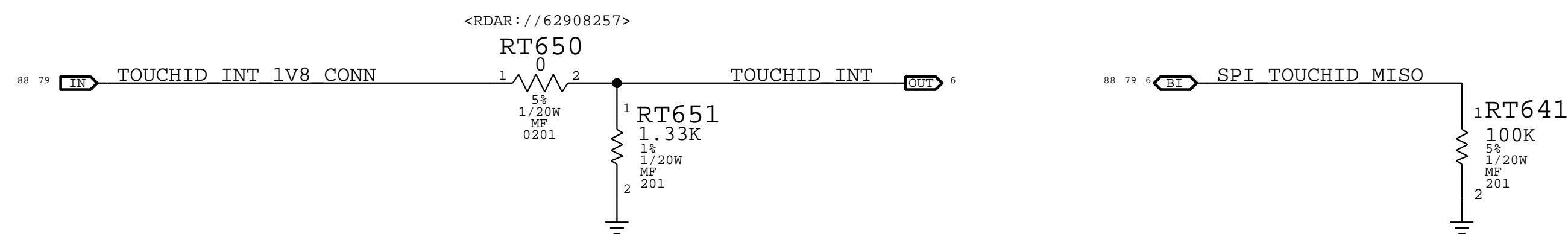
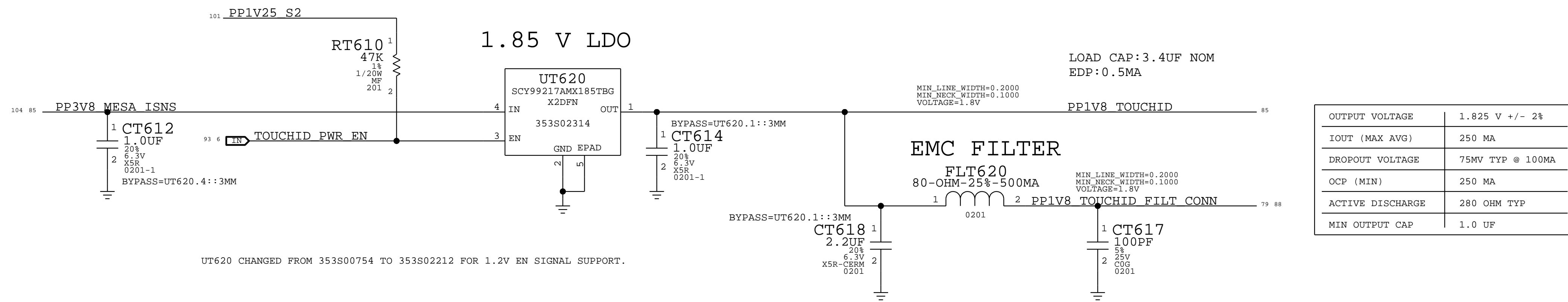
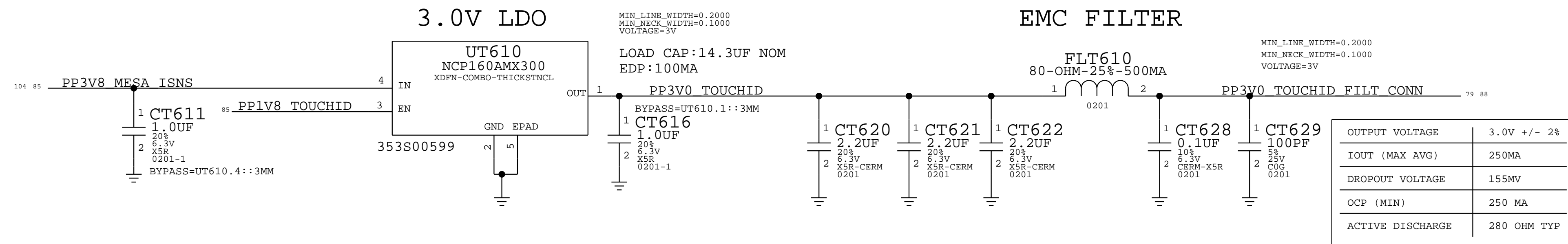
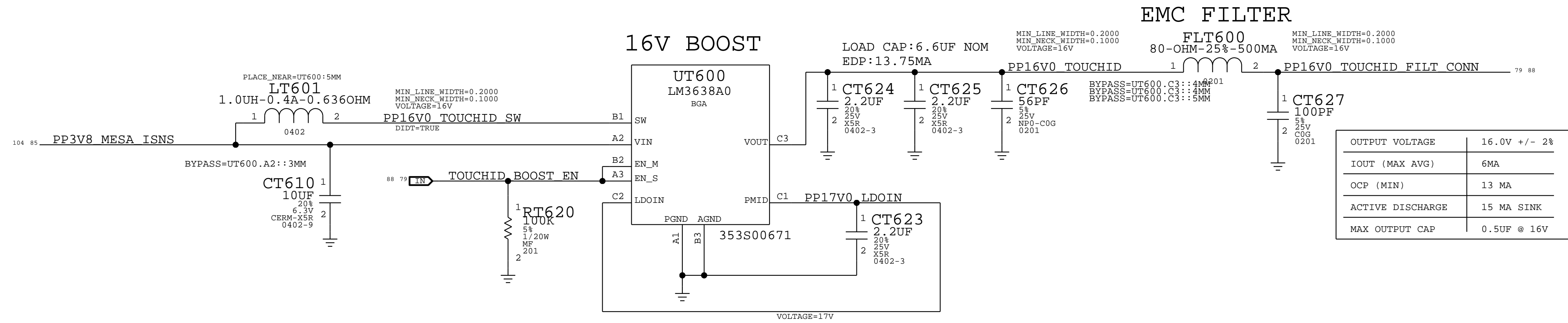


BOM_COST_GROUP=TRACKPAD

PAGE TITLE		
TRACKPAD CONNECTOR		
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	REVISION	9.0.0
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	PAGE	254 OF 999
	SHEET	84 OF 117

*** OK2INTEGRATE ***

TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0

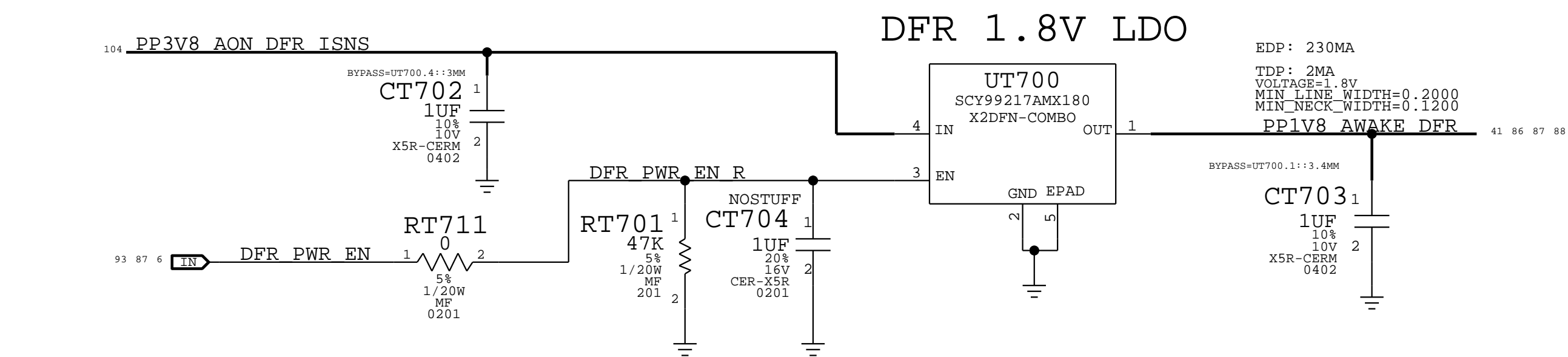
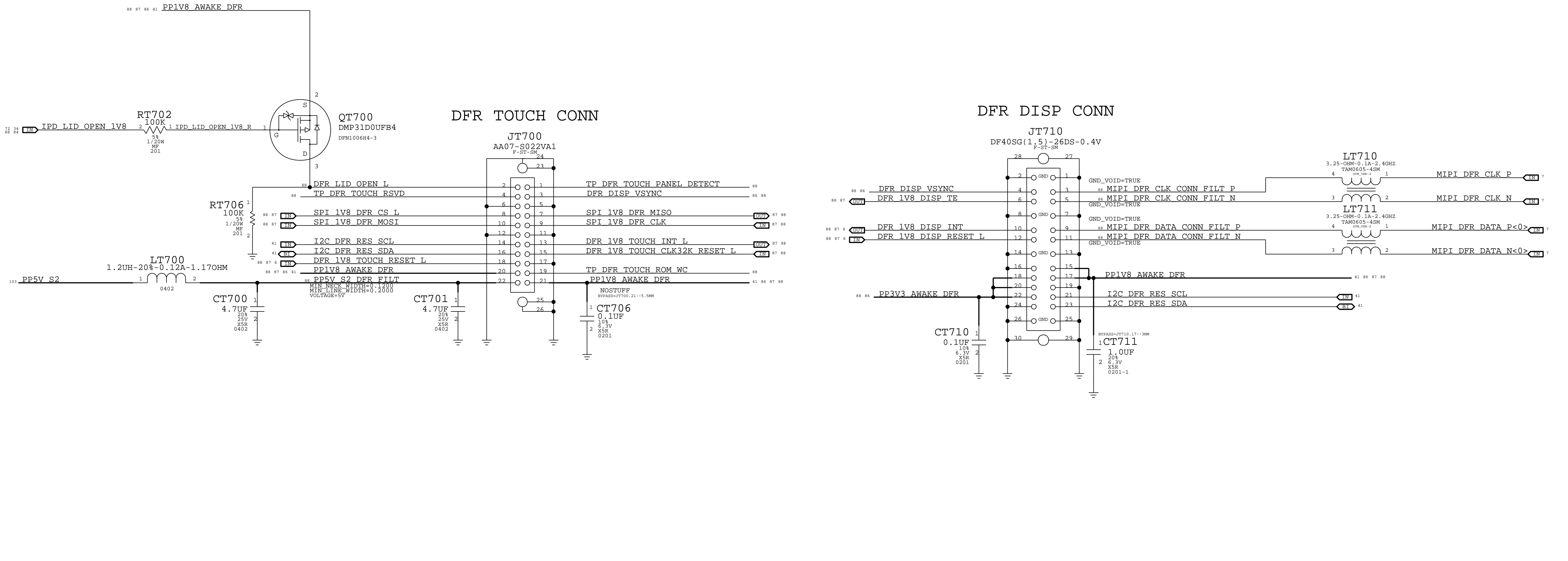


PAGE TITLE TOUCHID SUPPORT		
Apple Inc.	DRAWING NUMBER	051-05399
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	PAGE	256 OF 999
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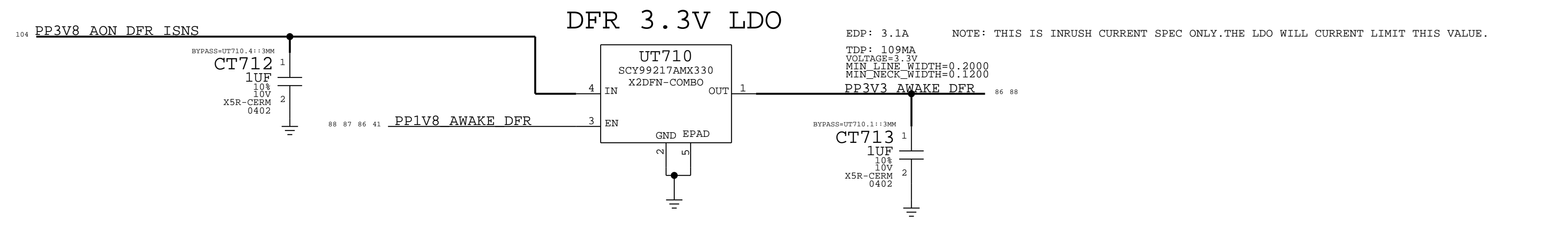
BOM_COST_GROUP=TOUCH ID

OK2INTEGRATE

DFR V3 SUPPORT



OUTPUT VOLTAGE	1.8V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	80MV TYP @ 250MA
OCF (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MAX OUTPUT CAP	



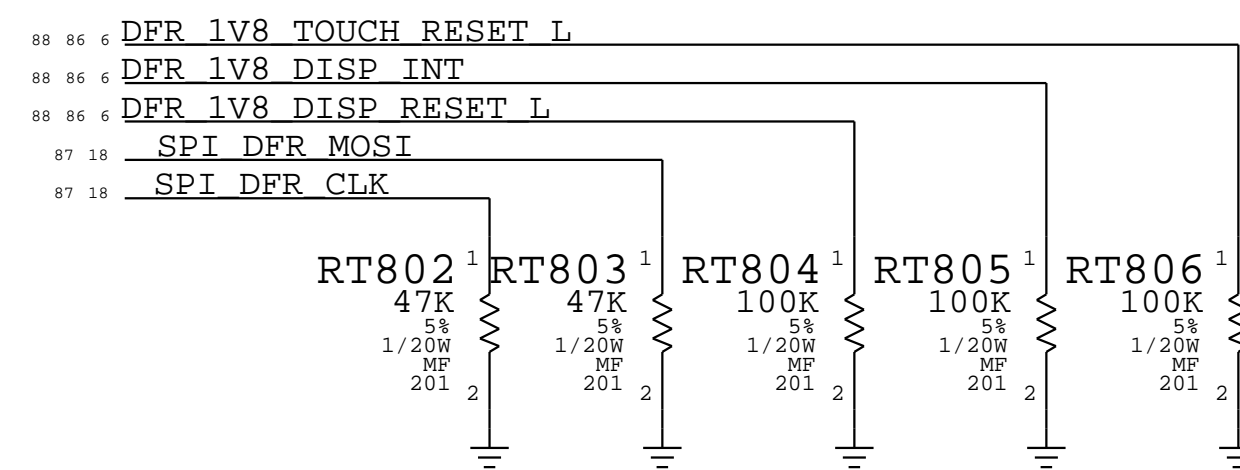
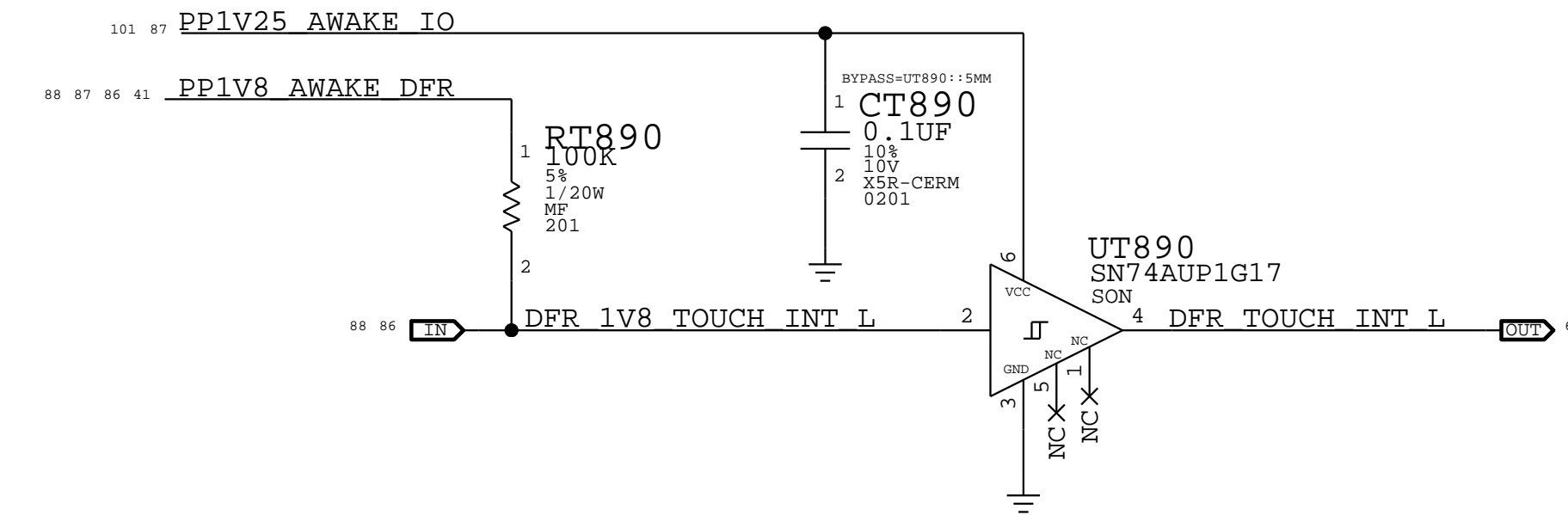
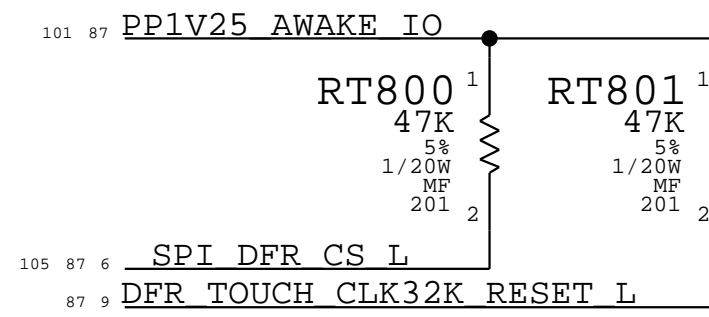
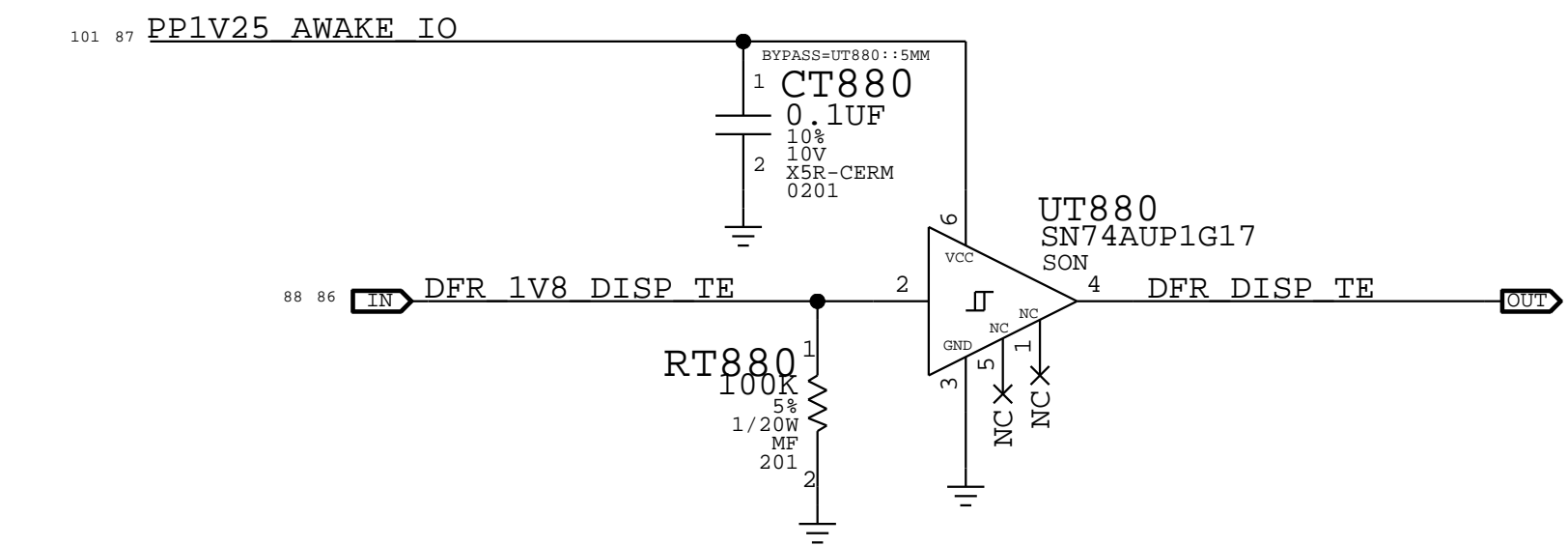
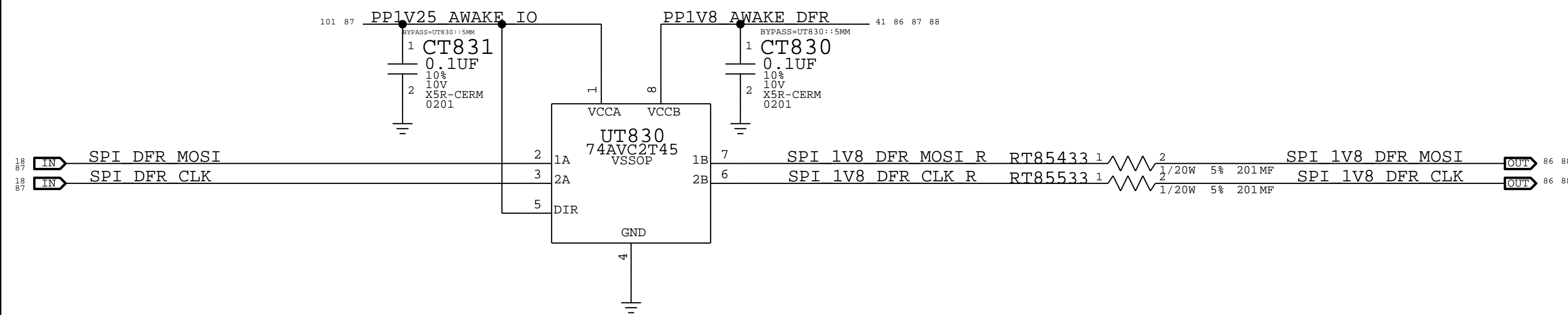
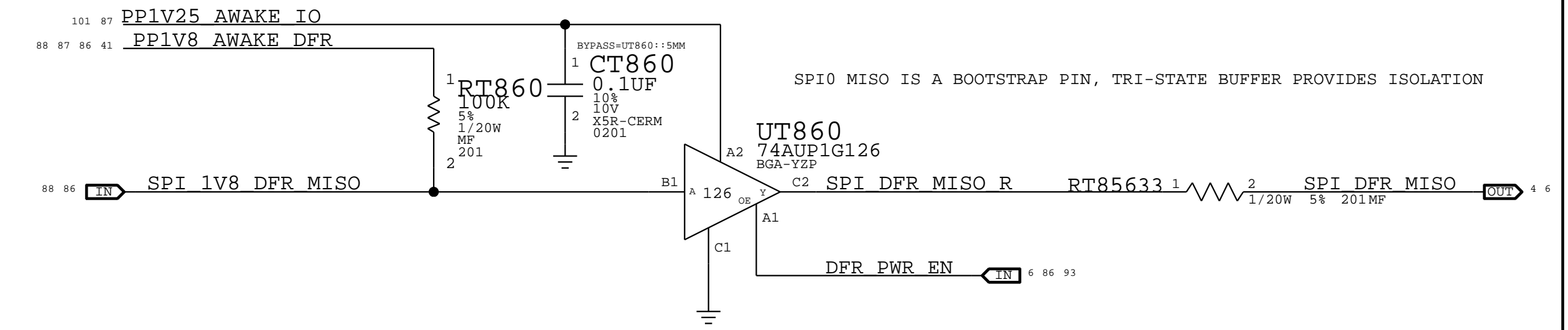
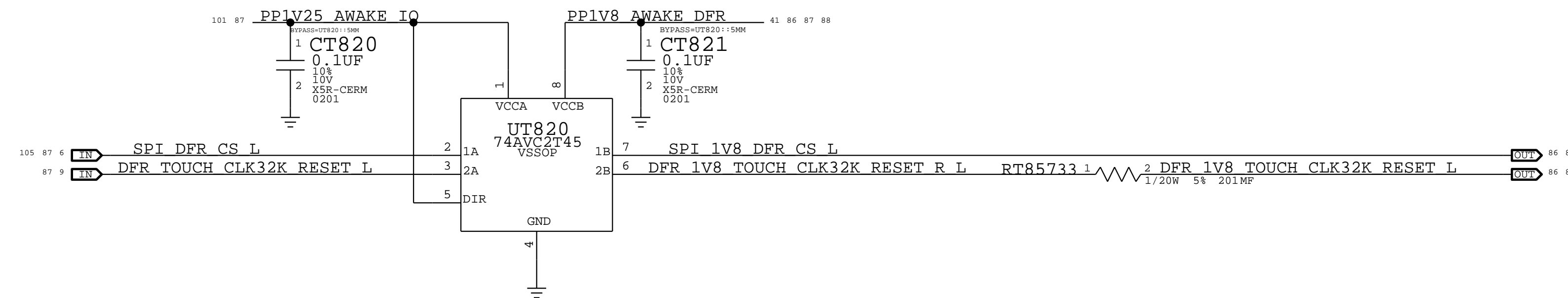
OUTPUT VOLTAGE	3.3V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	80MV TYP @ 250MA
OCF (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MAX OUTPUT CAP	

PAGE TITLE		
DFR SUPPORT 1		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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	PAGE	257 OF 999
	SHEET	86 OF 117

BOM_COST_GROUP=TOUCH BAR

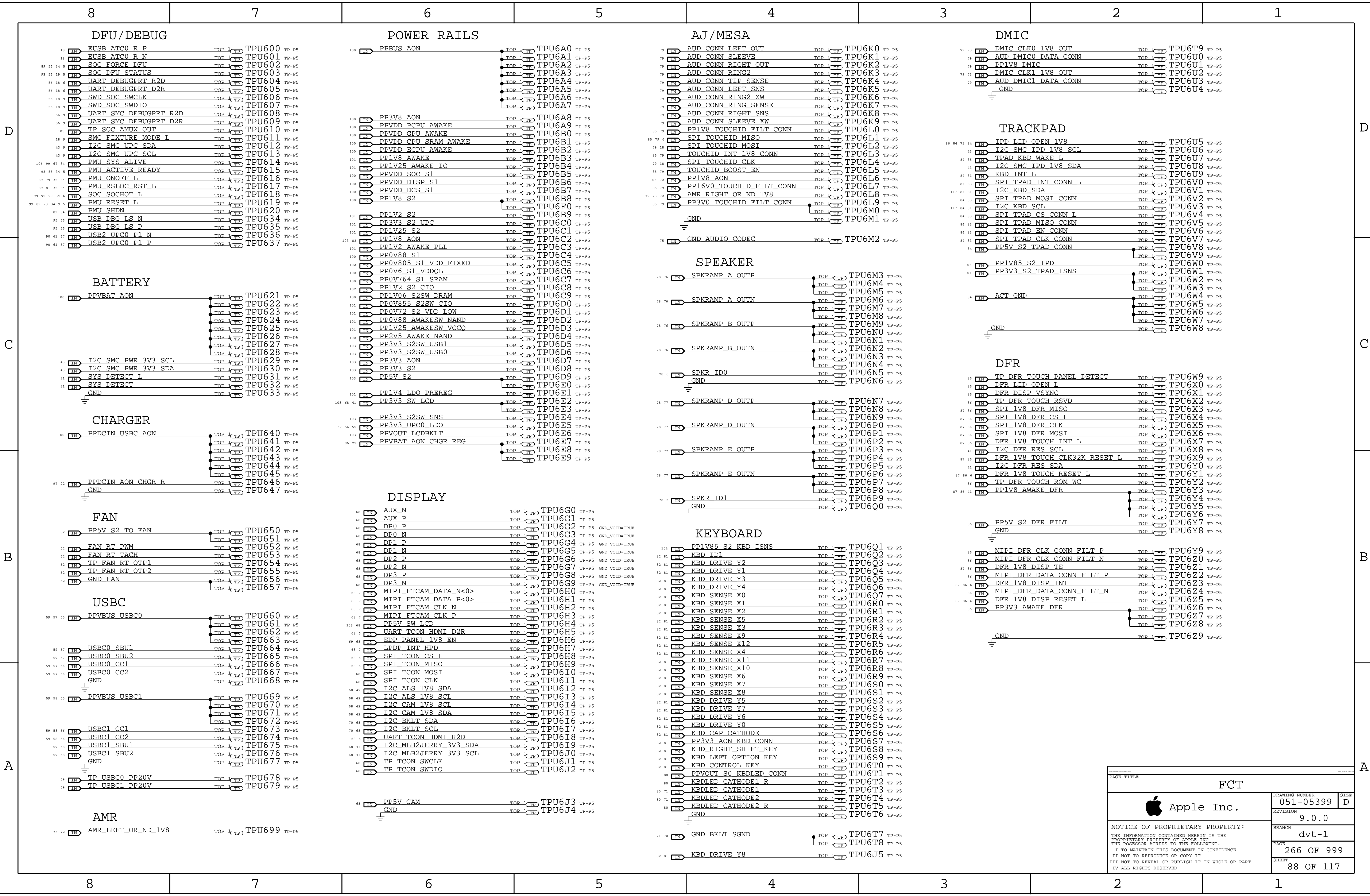
OK2INTEGRATE

DFR V3 SUPPORT



PAGE TITLE		
DFR SUPPORT 2		
	DRAWING NUMBER	051-05399
	REVISION	9.0.0
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	PAGE	258 OF 999
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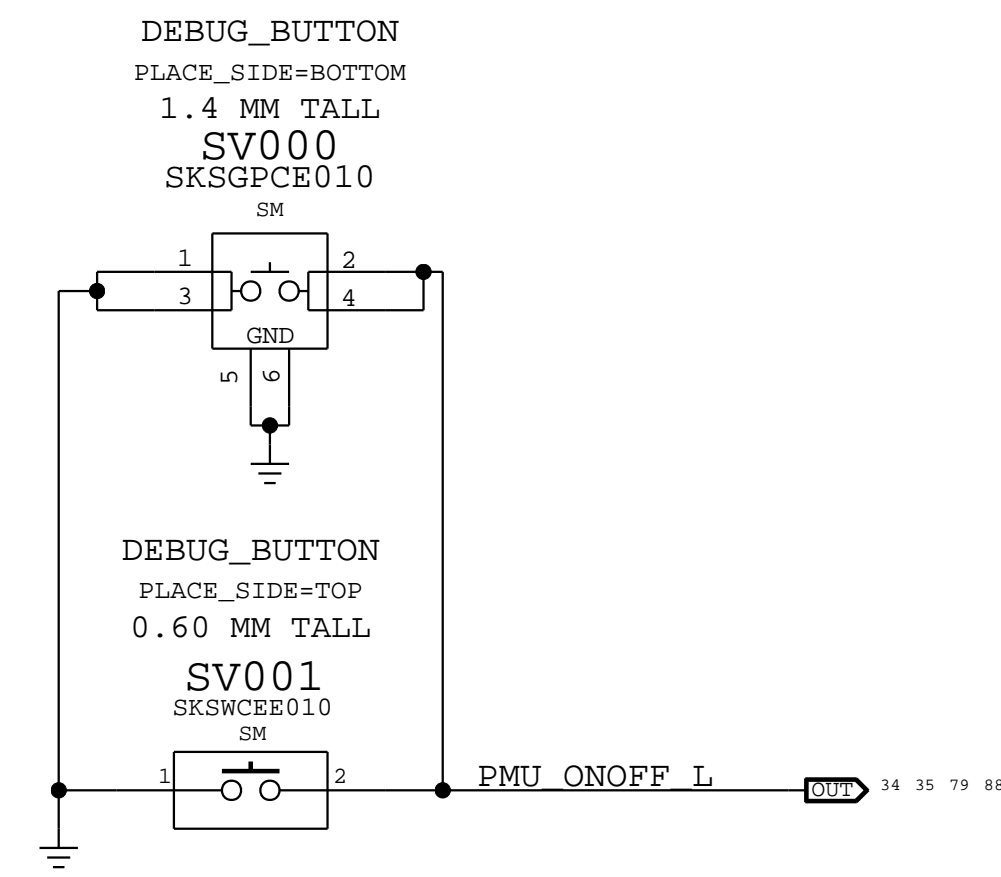
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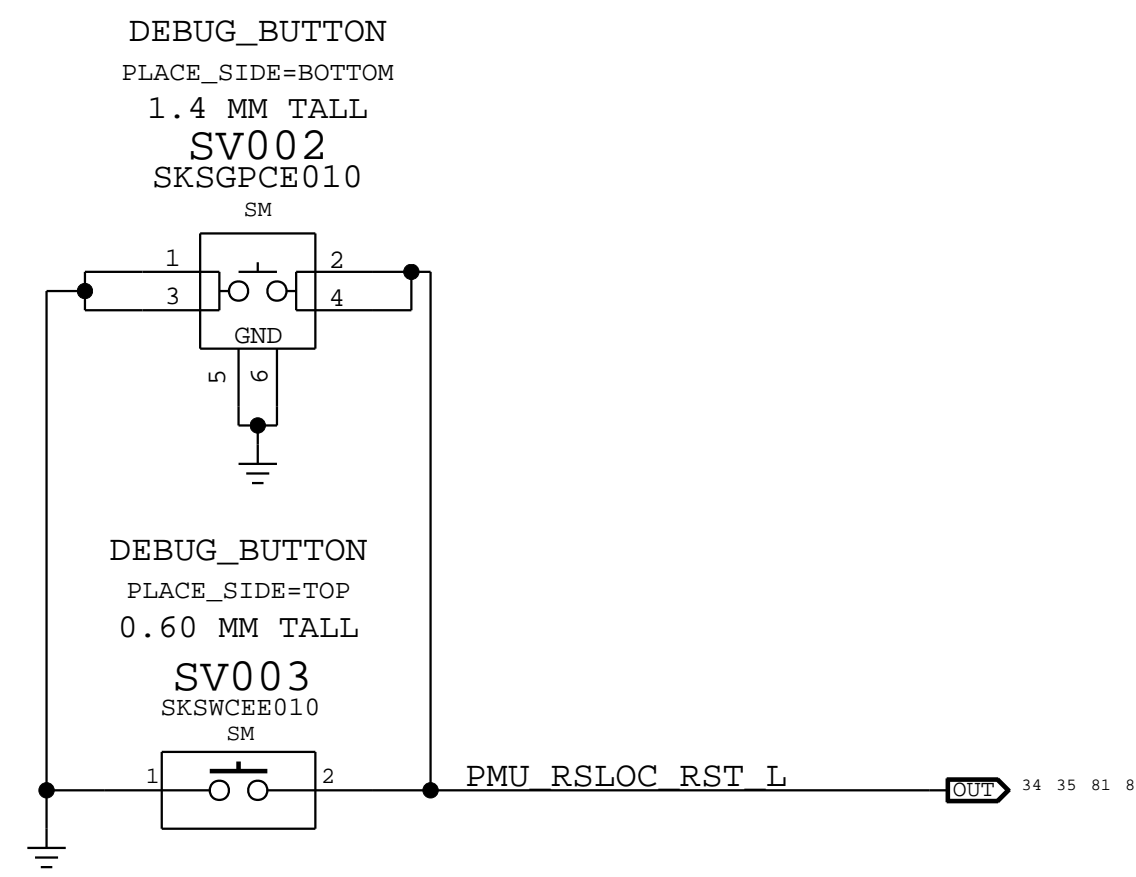
PAGE TITLE		FCT	
DRAWING NUMBER		051-05399	
REVISION		9.0.0	
BRANCH		dvt-1	
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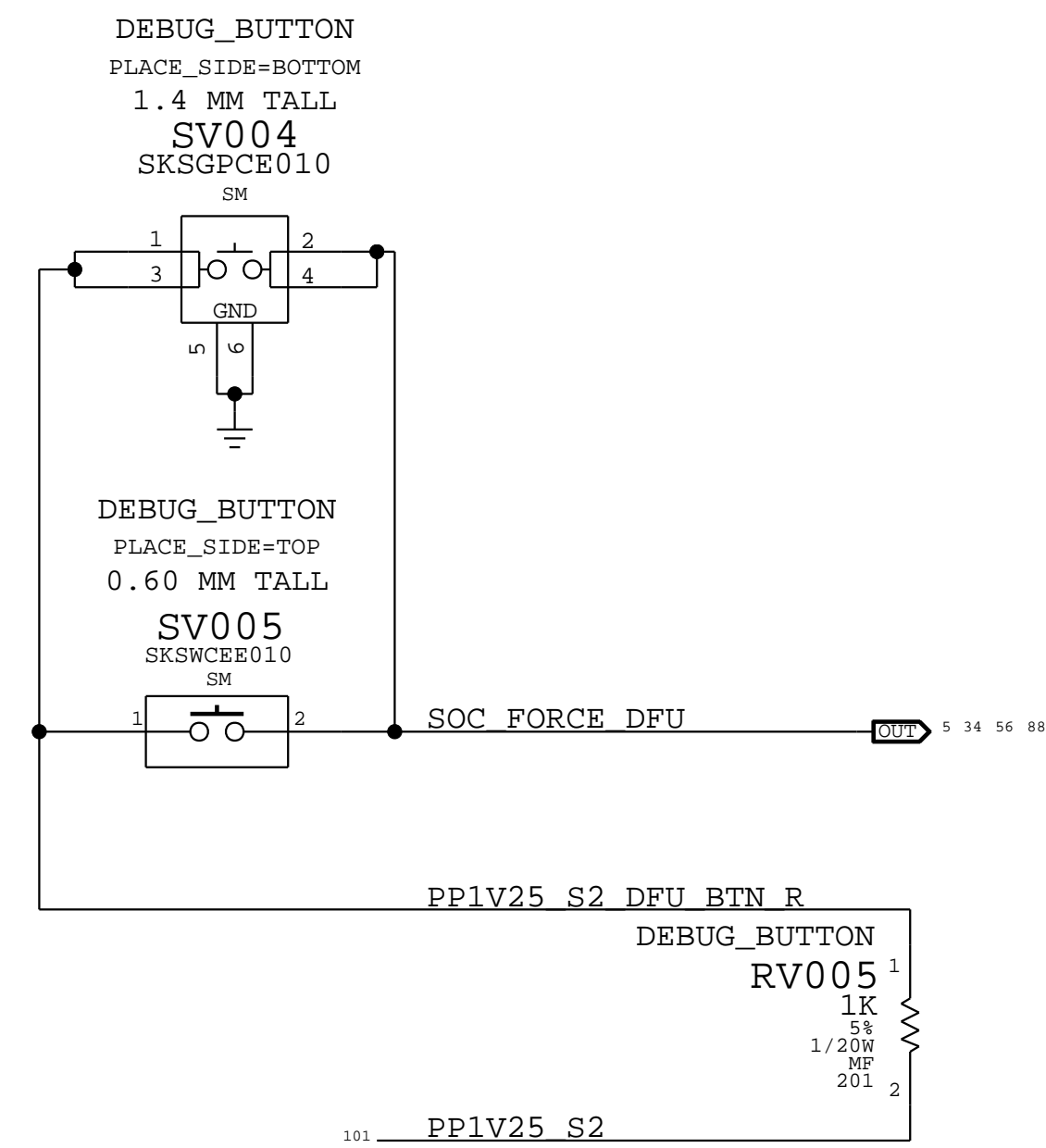
POWER BUTTON



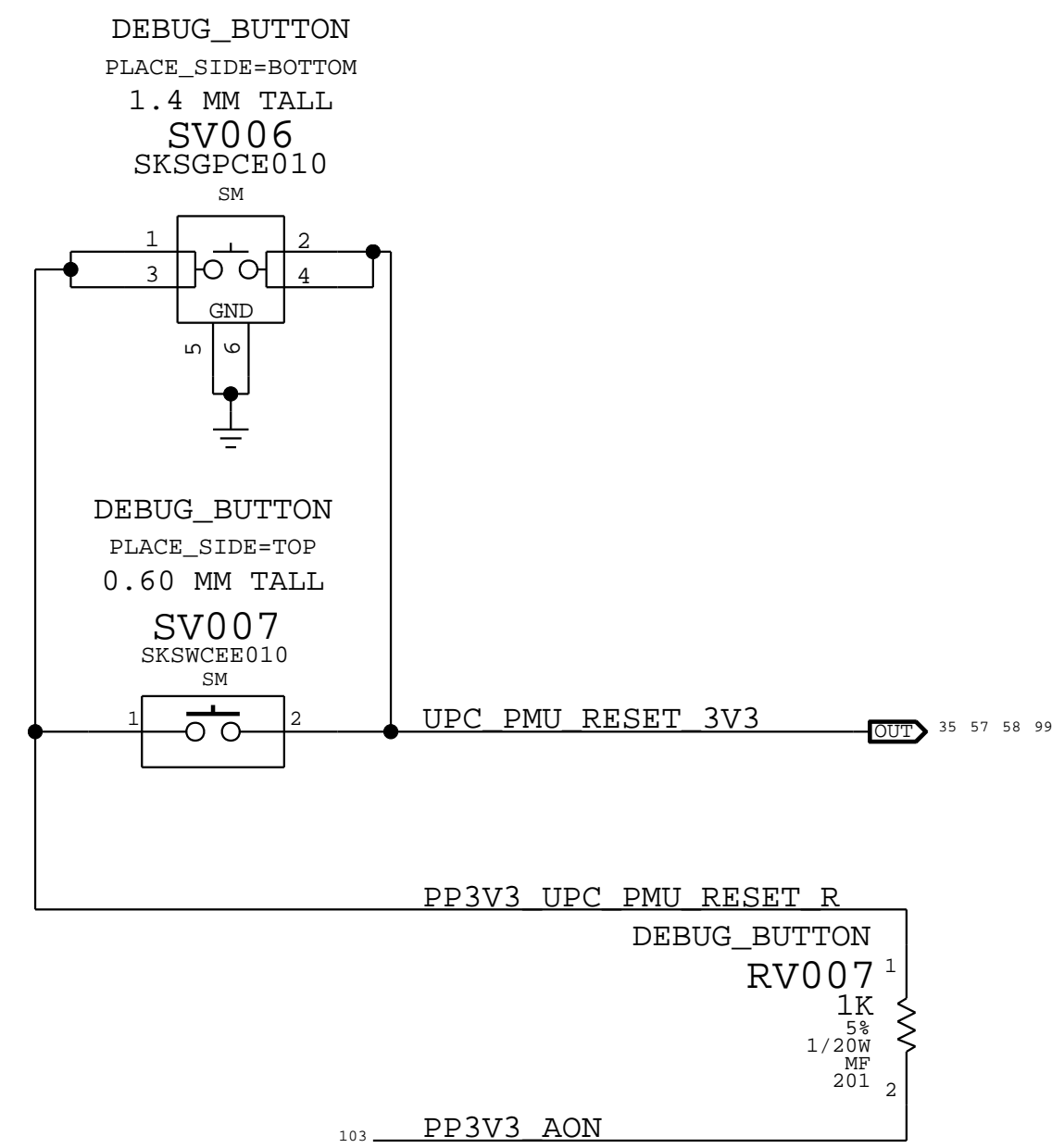
RSLOC



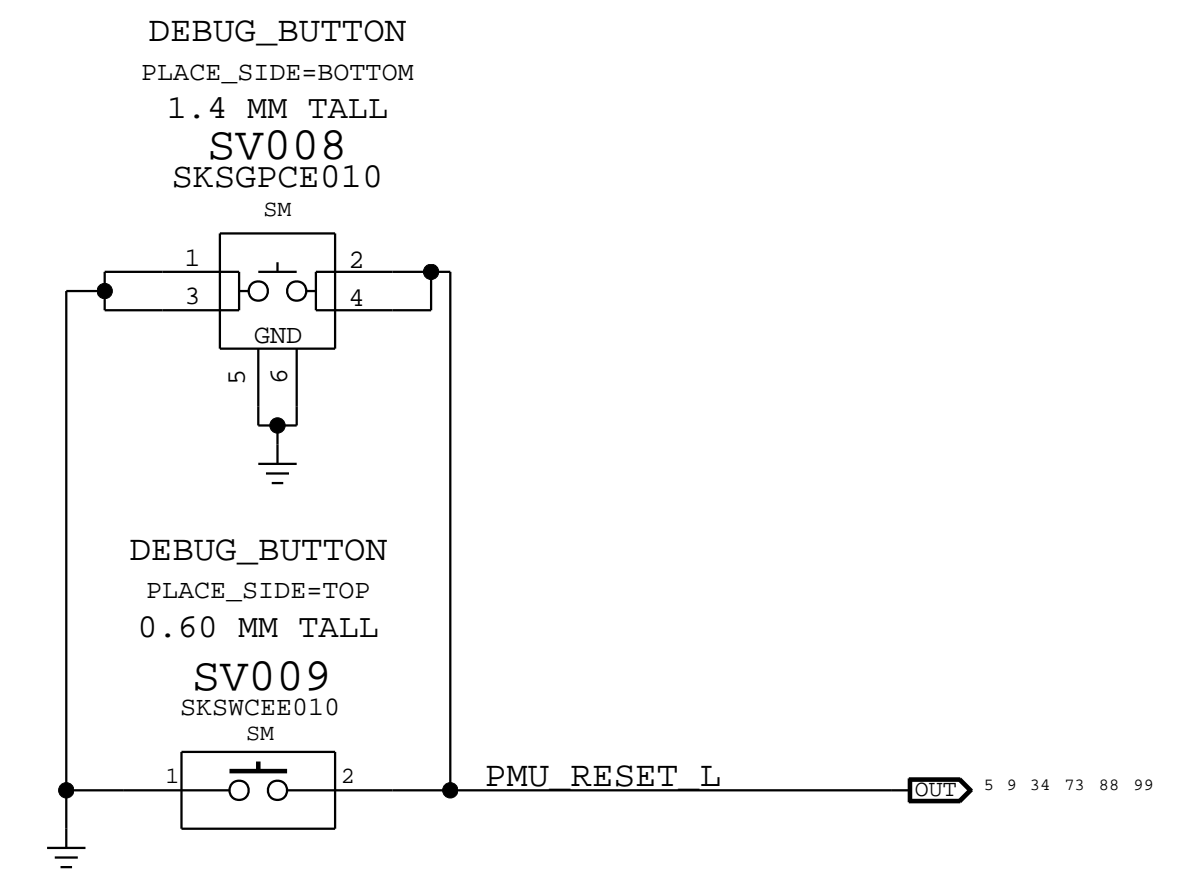
FORCE DFU



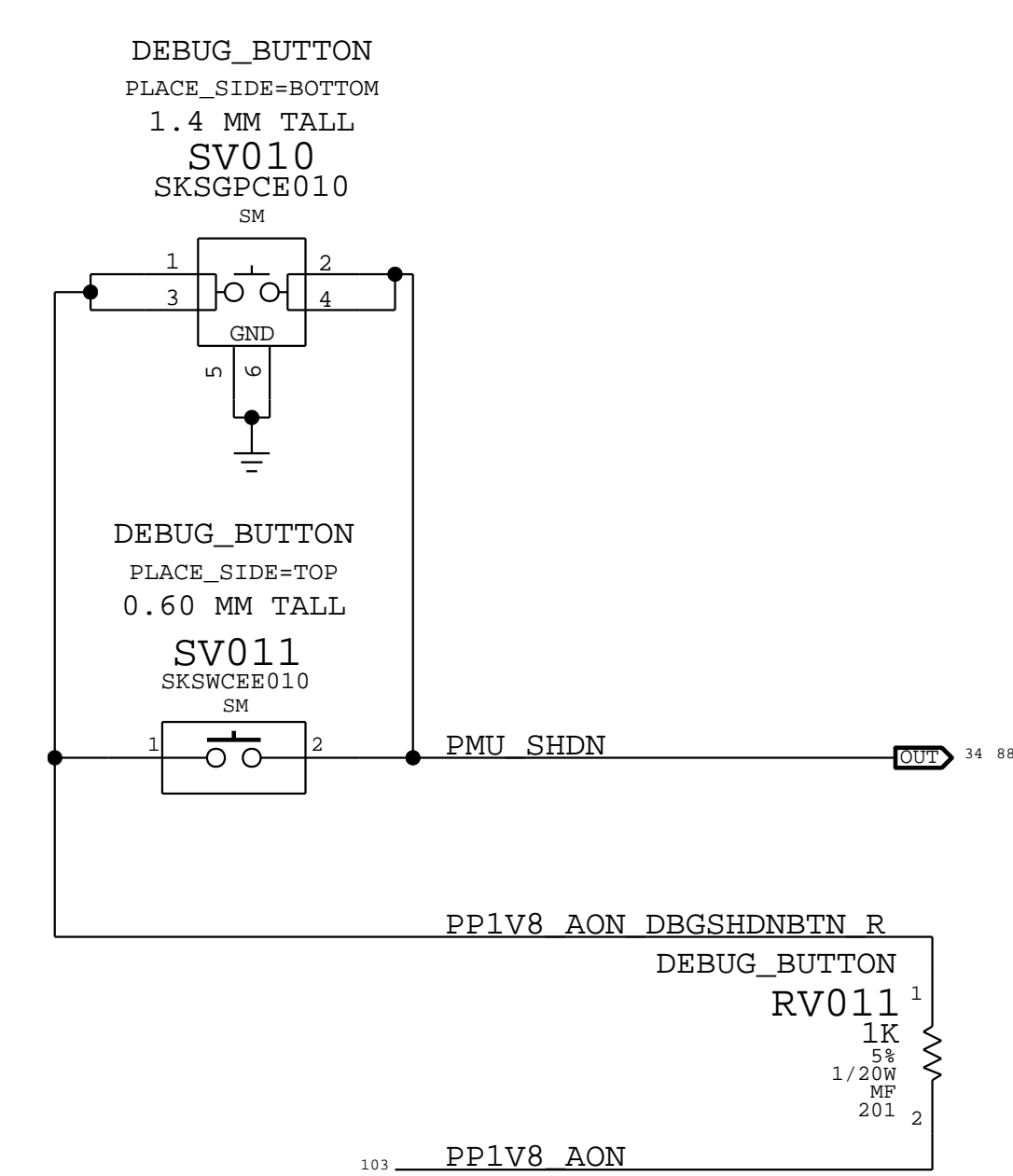
**UPC RESET
(RESET PMU)**



**RESET
(RESET SOC ONLY)**



PMU SHUTDOWN



PAGE TITLE		DEBBUG: BUTTONS	
DRAWING NUMBER		051-05399	
REVISION		9.0.0	
BRANCH		dvt-1	
PAGE		270 OF 999	
SHEET		89 OF 117	

BOM_COST_GROUP=DEBUG

8

7

6

5

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3

2

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D

C

C

B

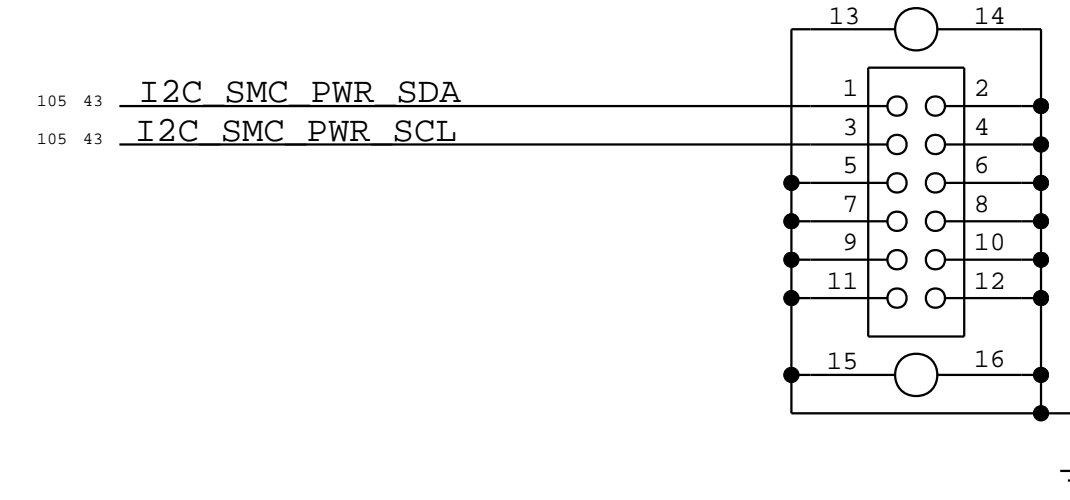
B

A

A

CHARGER ARKANOID CONN

CHGR_DBG
JV100
505070-1222
N-ST-SM



- 99 95 88 34 6 SOC SOCHOT L TPV190
TP-P55 PLACE_SIDE=TOP
- 34 MPMU FAULT OUT L TPV191
TP-P55 PLACE_SIDE=TOP
- 34 30 PMU SCRASH L TPV192
TP-P55 PLACE_SIDE=TOP
- 34 PMU CRASH L TPV194
TP-P55 PLACE_SIDE=TOP

- 88 61 57 USB2 UPC0 P1 P 1 DPV100
P4MM SM
- 88 61 57 USB2 UPC0 P1 N 1 DPV101
P4MM SM

PAGE TITLE		DEBUG: MISC	
	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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		PAGE	271 OF 999
		SHEET	90 OF 117

BOM_COST_GROUP=DEBUG

8

7

6

5

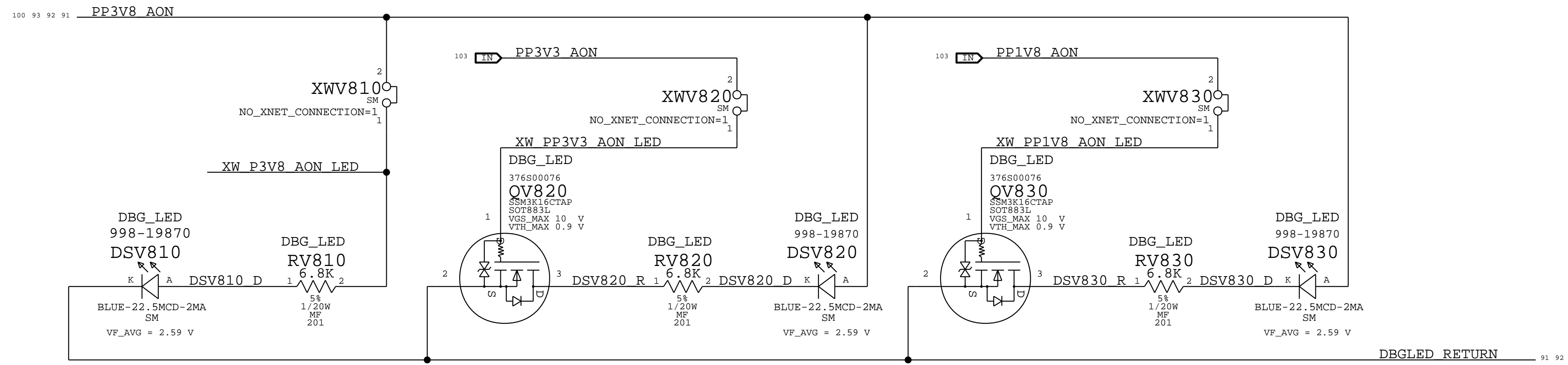
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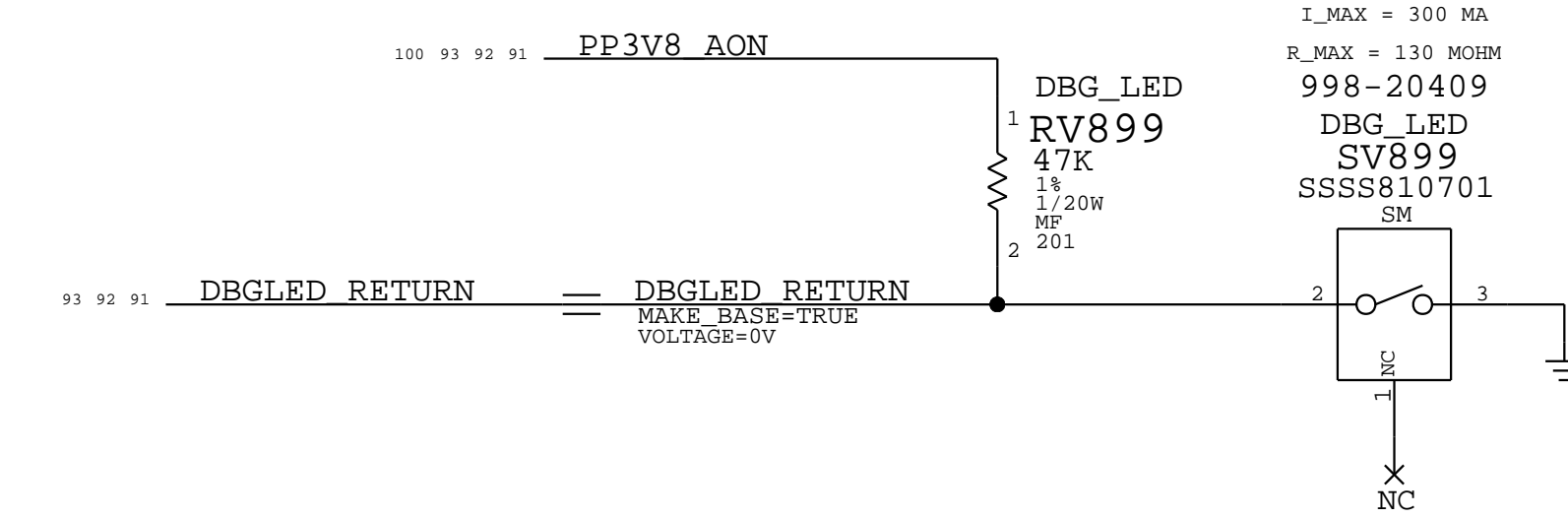
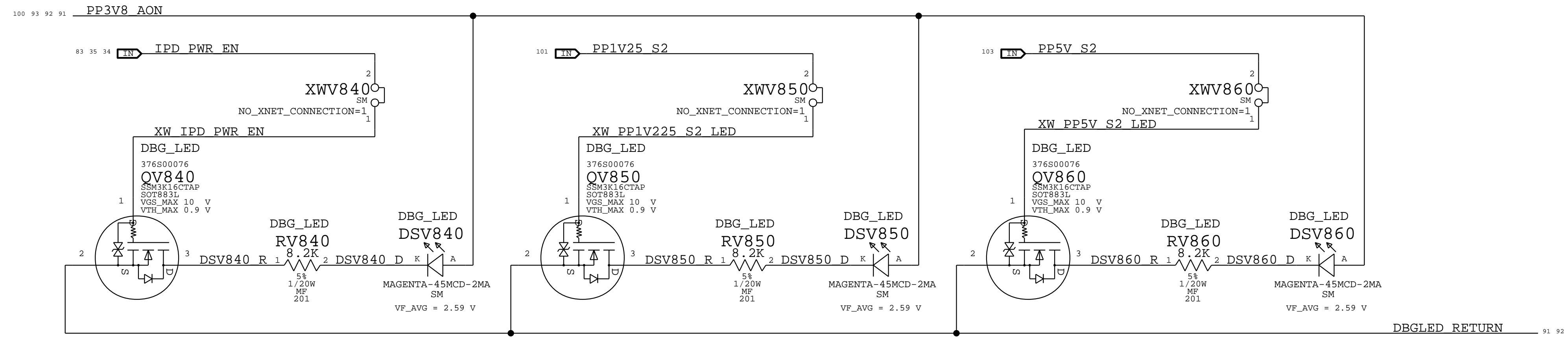
2

1

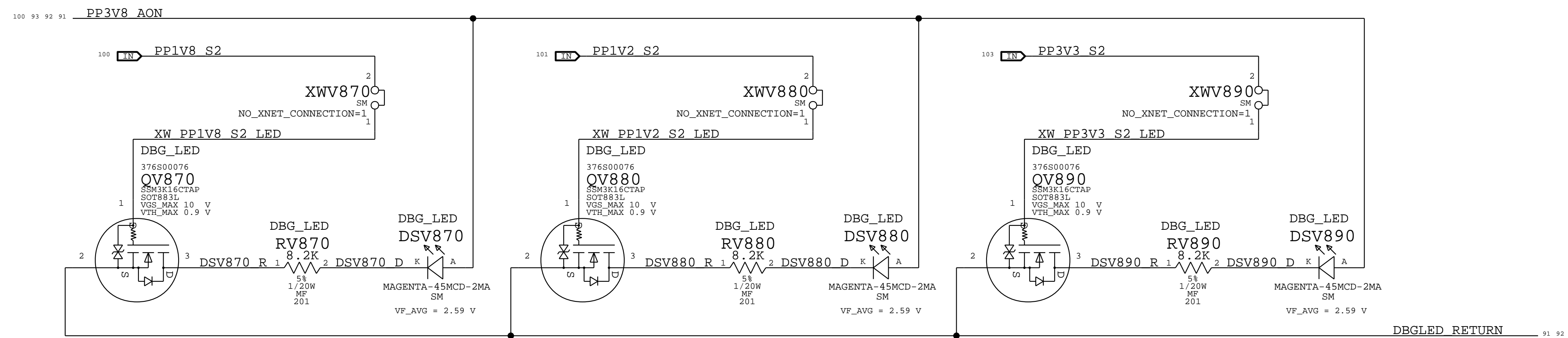
AON LEDS (BLUE)



S2 LEDS (MAGENTA)



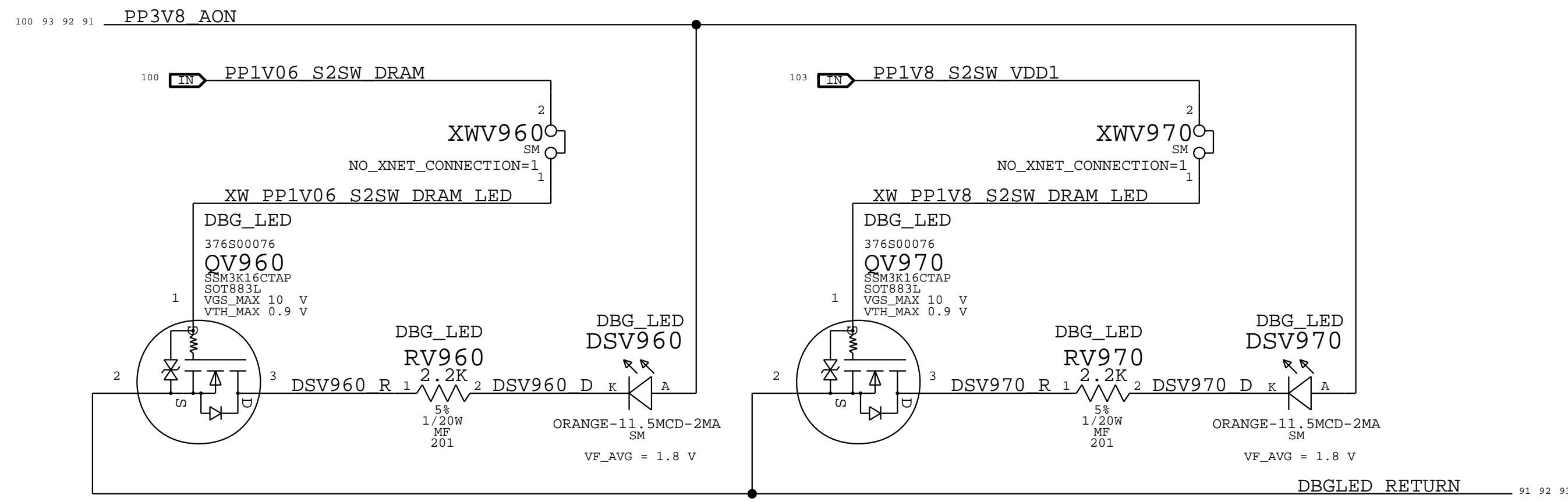
S2 LEDS (MAGENTA)



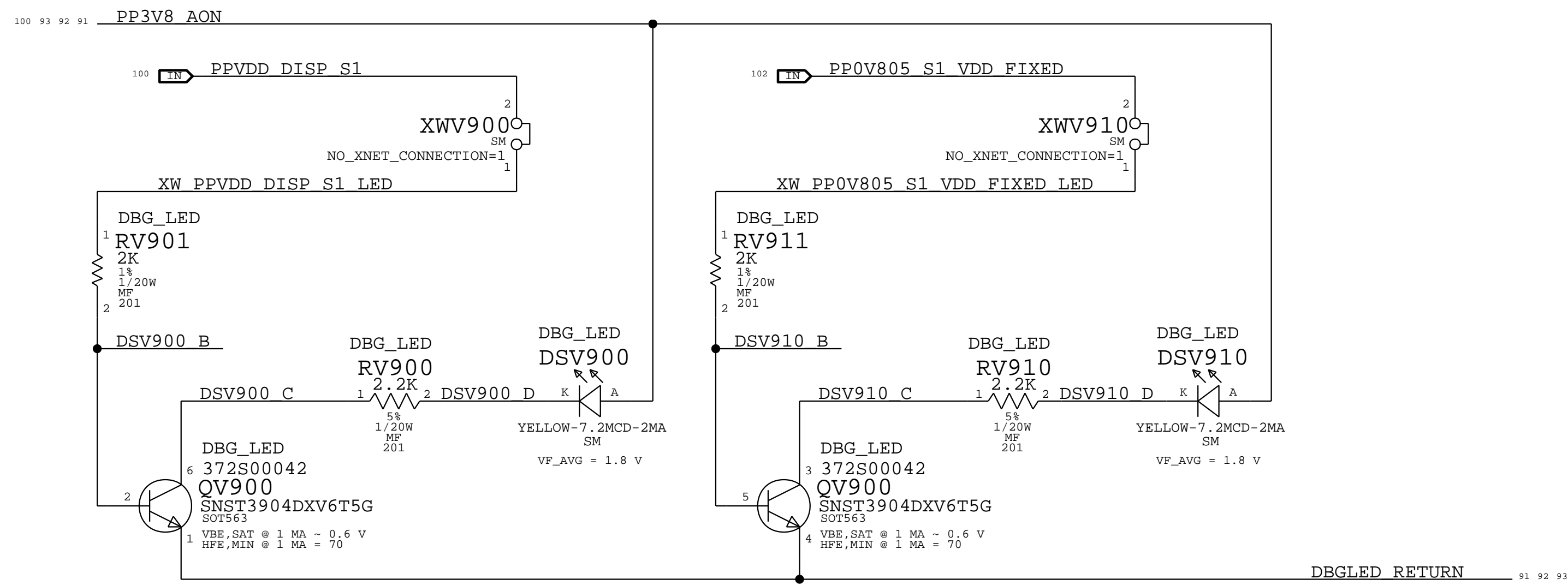
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PAGE TITLE			
DEBUG: LEDS (1/3)		DRAWING NUMBER	051-05399
REVISON		9.0.0	
BRANCH		dvt-1	
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BOM_COST_GROUP=DEBUG

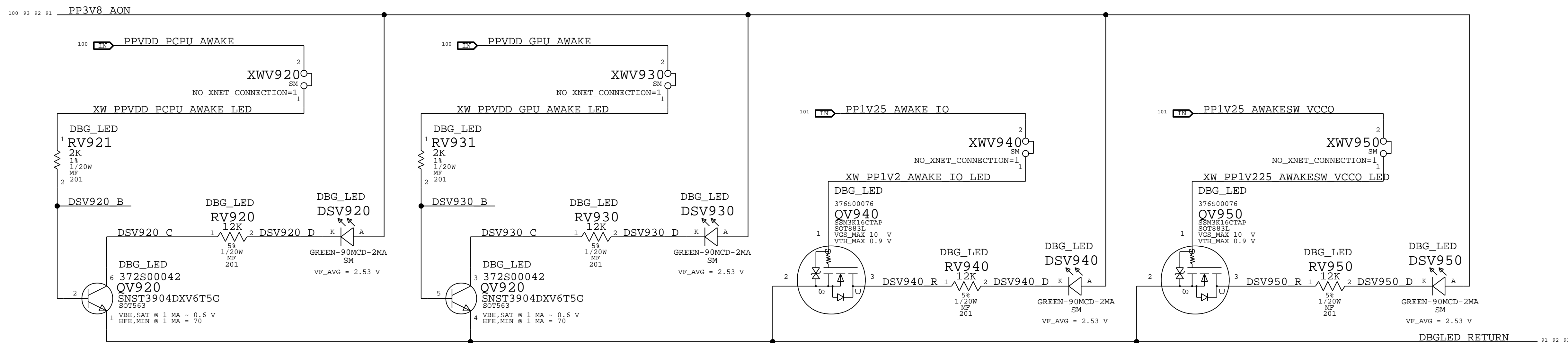
S2SW LEDS (ORANGE)



S1 LEDS (YELLOW)



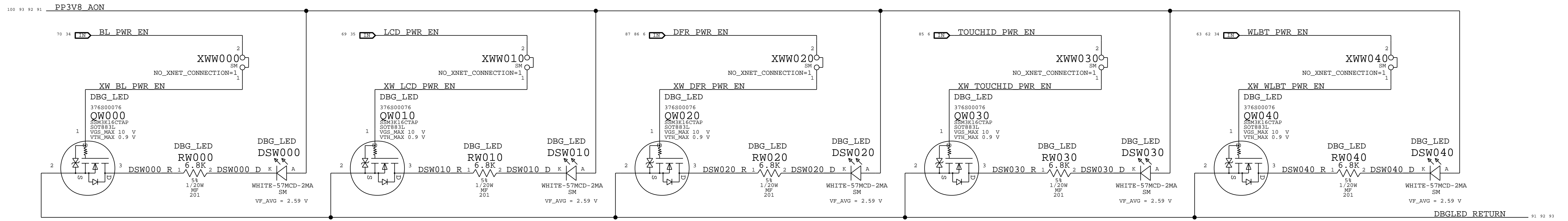
AWAKE LEDS (GREEN)



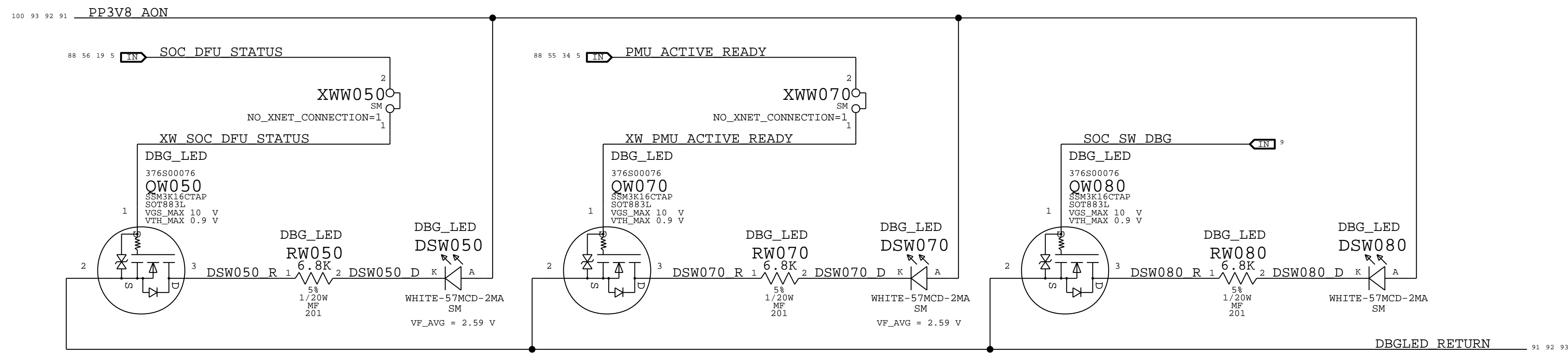
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PAGE TITLE			
DEBUG: LEDS (2/3)			
	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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	PAGE	279 OF 999	
	SHEET	92 OF 117	

BOM_COST_GROUP=DEBUG

MODULE LEDS (WHITE)



STATUS LEDS (WHITE)

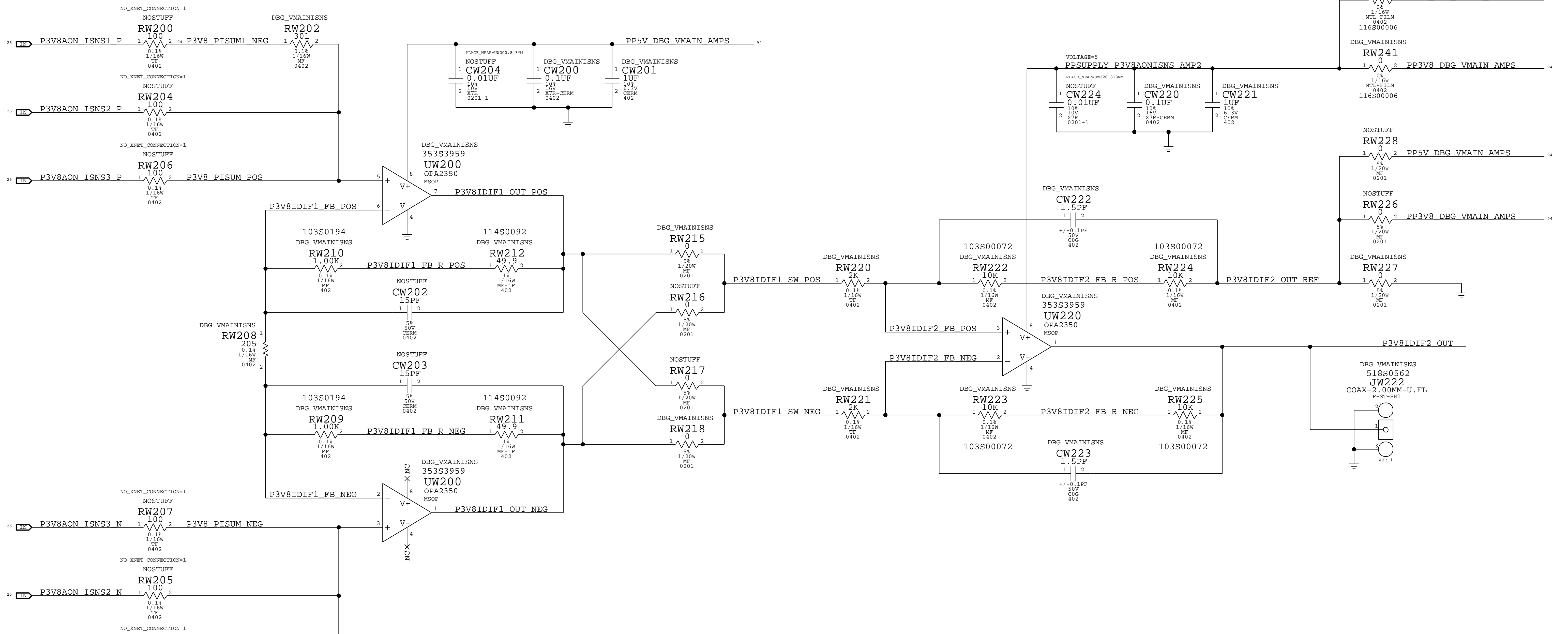


SYNC_MASTER=T668_MLB		SYNC_DATE=07/24/2019	
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NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	dvt-1
		PAGE	280 OF 999
		SHEET	93 OF 117

BOM_COST_GROUP=DEBUG

THE OPA2350 HAVE LEAKY INPUTS
<RDAR://63520263>

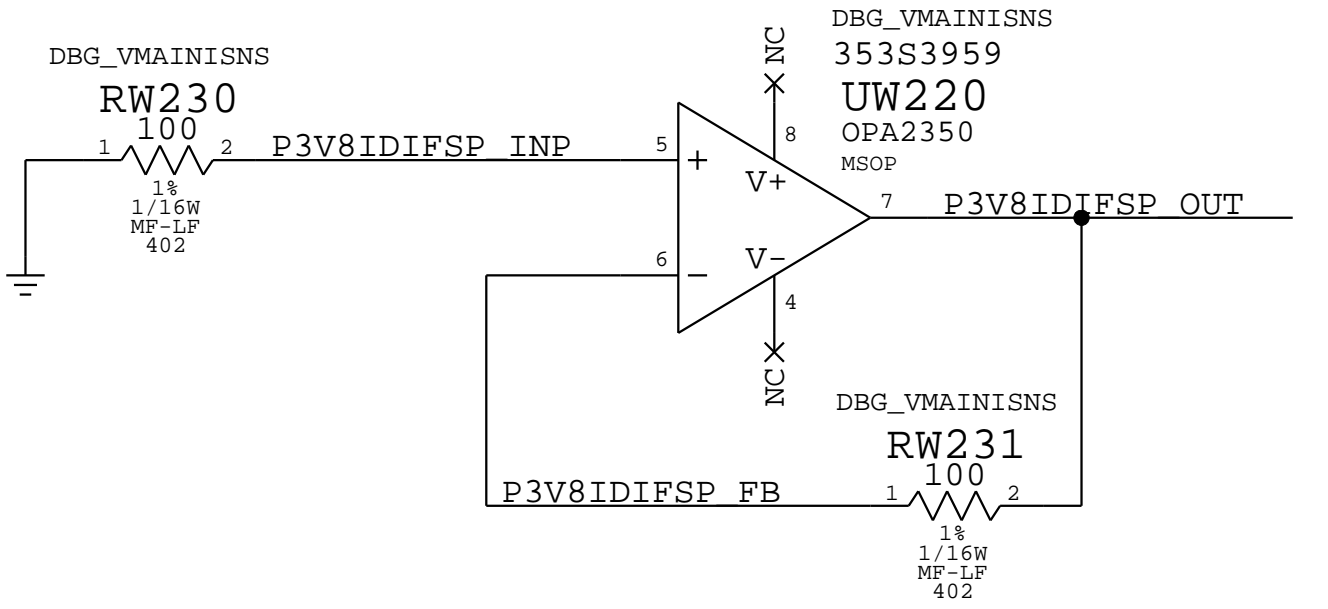
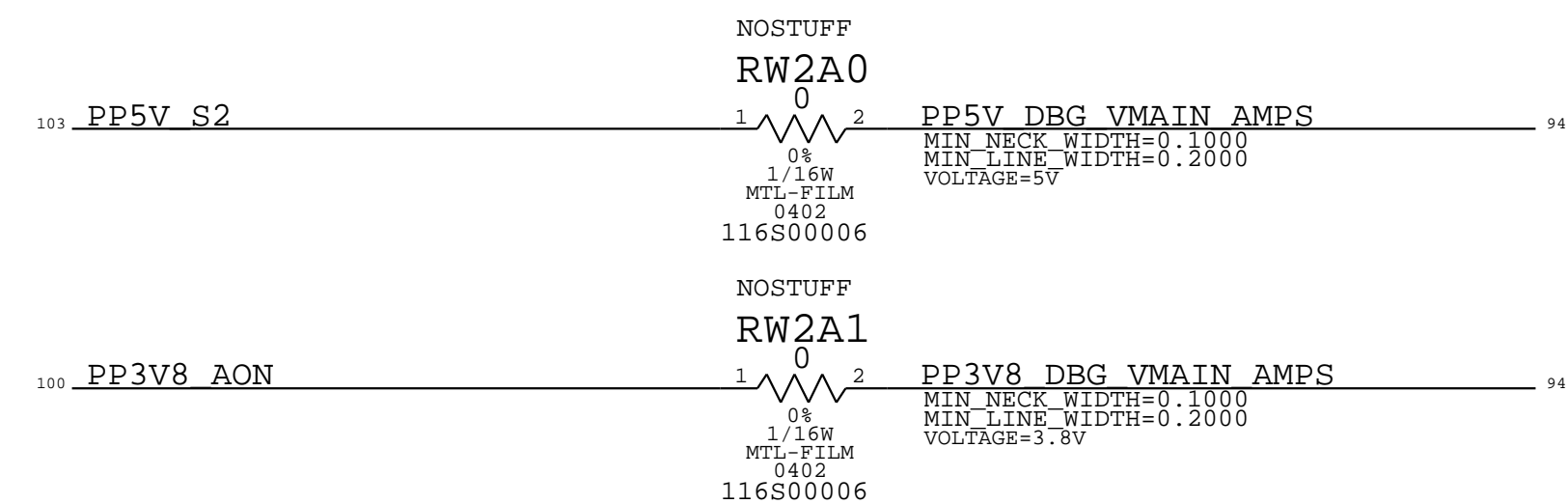
P3V8AON HIGH BANDWIDTH CURRENT SENSE AMPLIFIER



STUFF THESE TO ENABLE VMAIN SENSE AMP

NOTE: IF THESE ARE STUFFED, THEN THERE WILL BE SOME LEAKAGE IN OFF ONTO 5V_S2 THROUGH UW200
<RDAR://57211269>

CHAD NOTES:
EFFECTIVE CURRENT SENSE R = 0.4444 MOHM
1 MOHM || 1 MOHM || 4 MOHM
STAGE 1 GAIN = 11.243
STAGE 1 BANDWIDTH ~ 3.38 MHZ
STAGE 1 OUTPUT SCALE = 5.00 MV/A
STAGE 2 GAIN = 10.00
STAGE 2 BANDWIDTH ~ 3.80 MHZ
STAGE 2 OUTPUT SCALE = 50.0 MV/A



PAGE TITLE		DRAWING NUMBER		SIZE
DEBUG: P3V8AON ISENSE		051-05399		D
REVISION		9.0.0		
BRANCH		dvt-1		
PAGE		282 OF 999		
SHEET		94 OF 117		

D

D

C

C

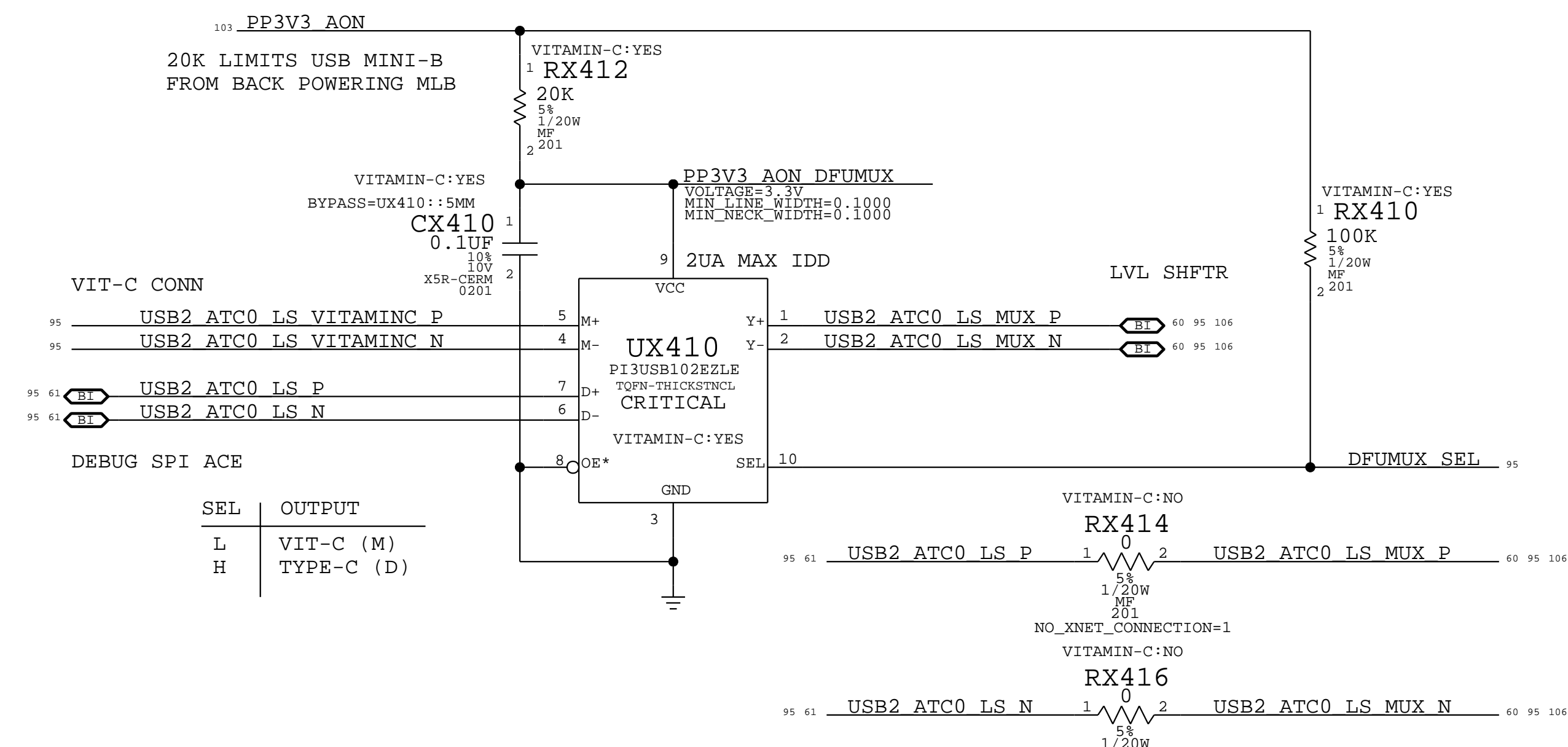
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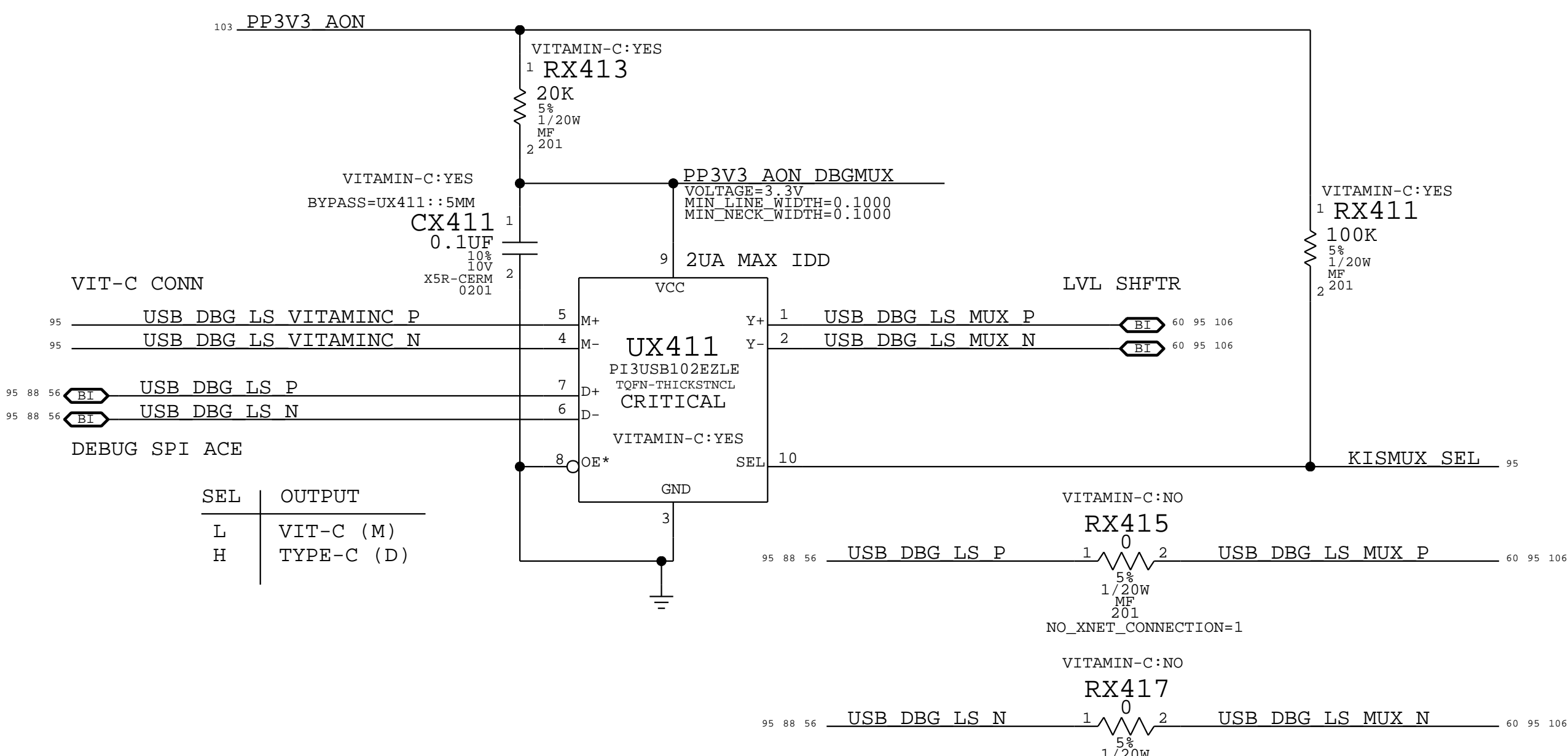
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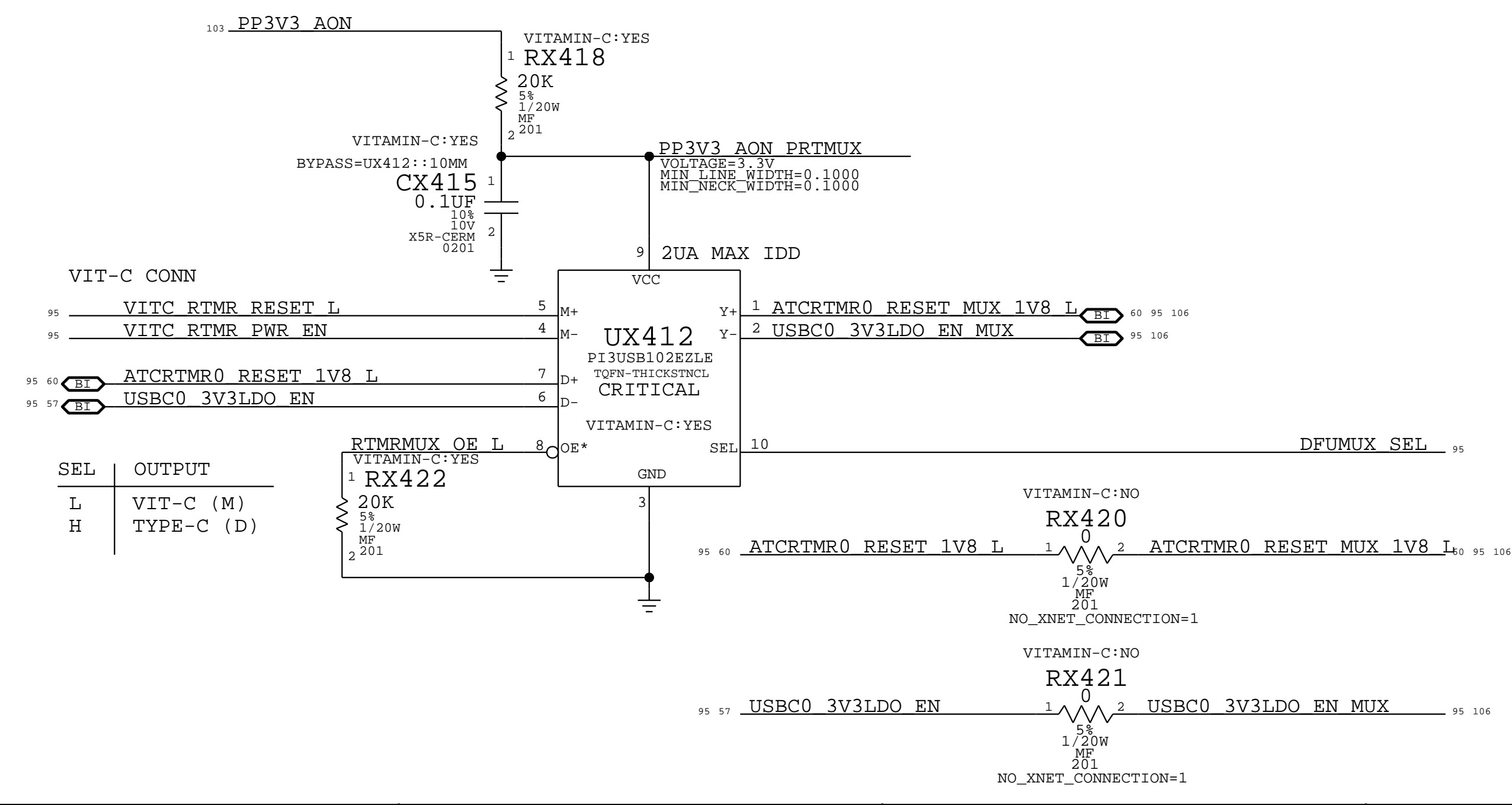
SOC USB DFU MUX



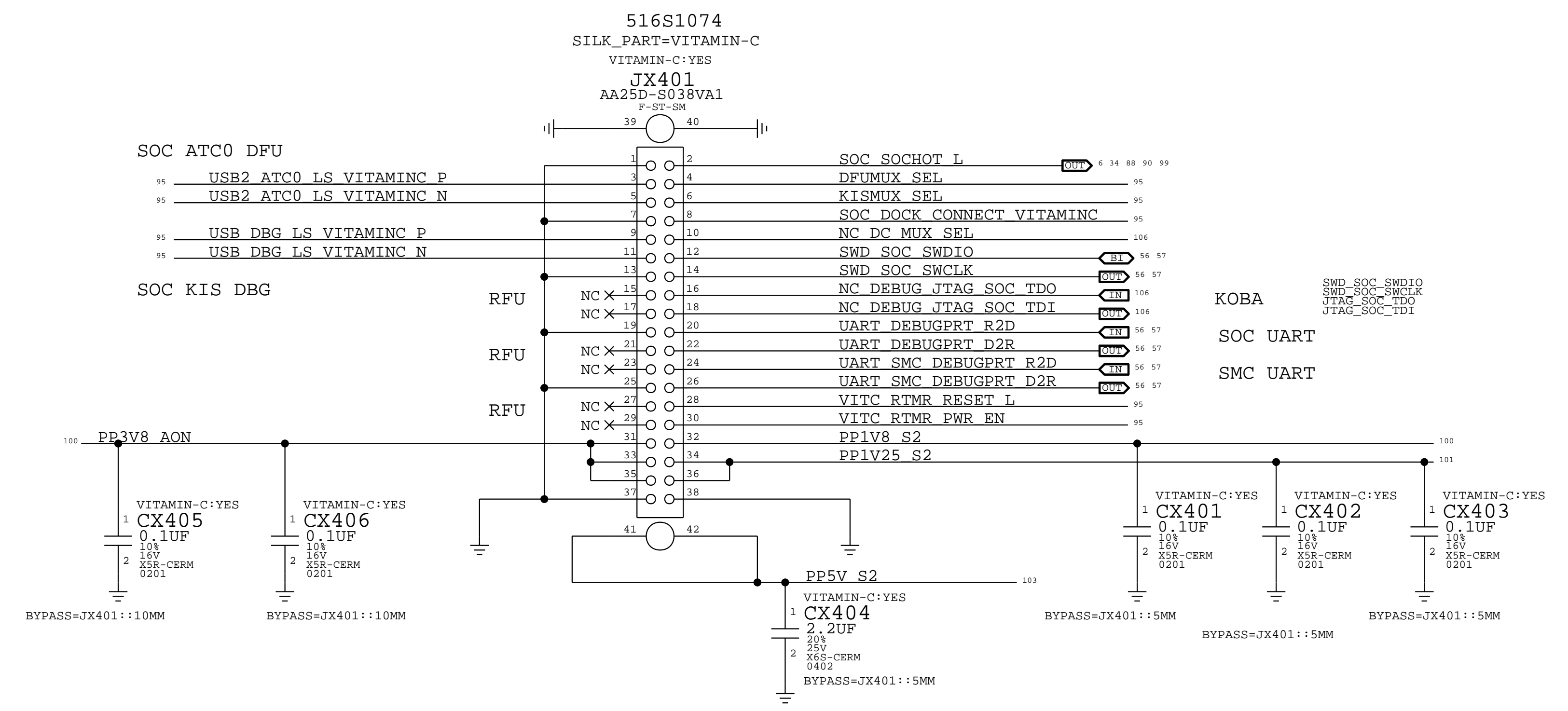
SOC DBG MUX



PARROT DBG MUX



VITAMIN-C MK2 CONNECTOR



SYNC_MASTER=MANAN_T668_MLB		SYNC_DATE=02/03/2020	
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	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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		PAGE	294 OF 999
		SHEET	95 OF 117

BOM_COST_GROUP=DEBUG

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C

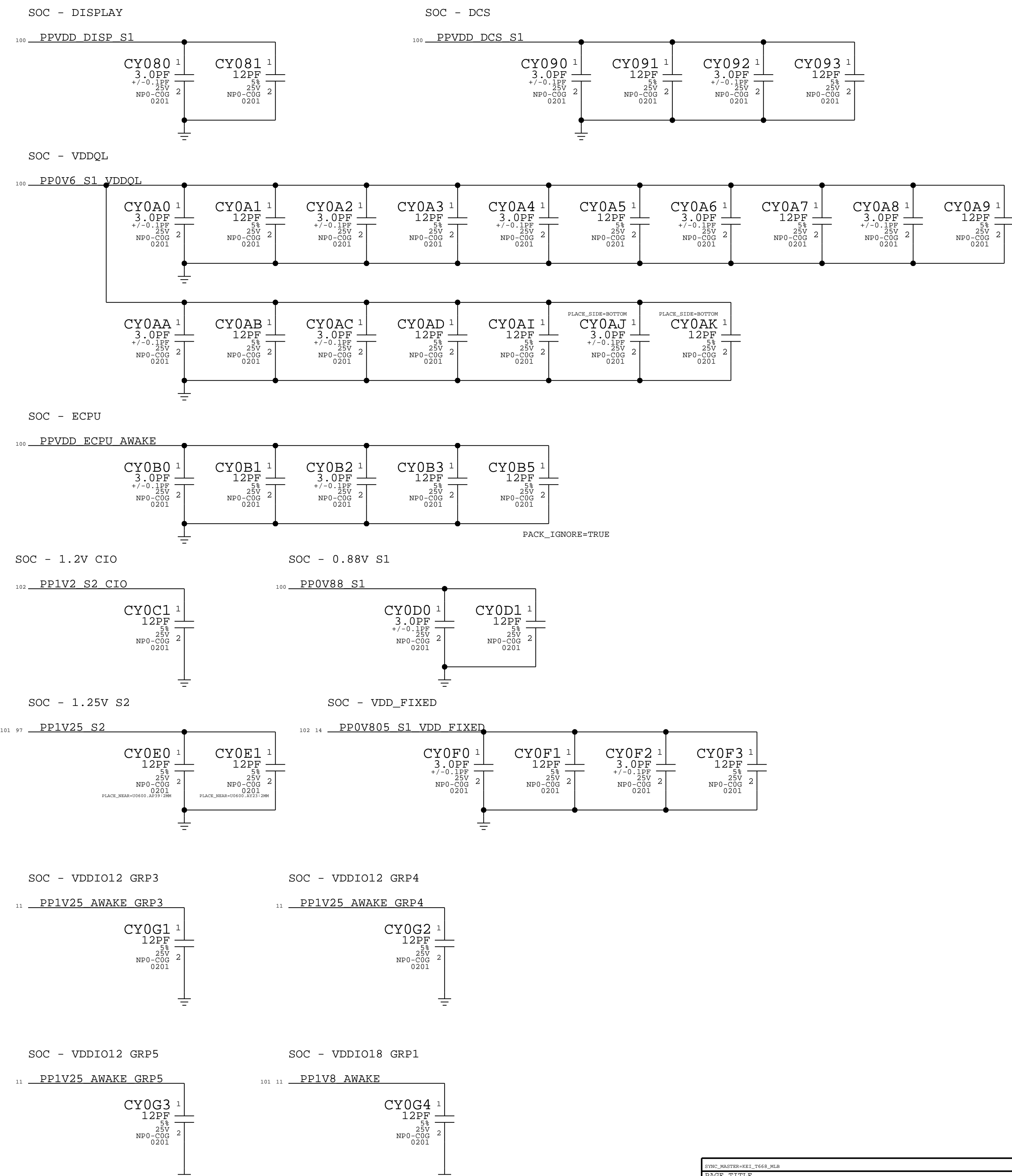
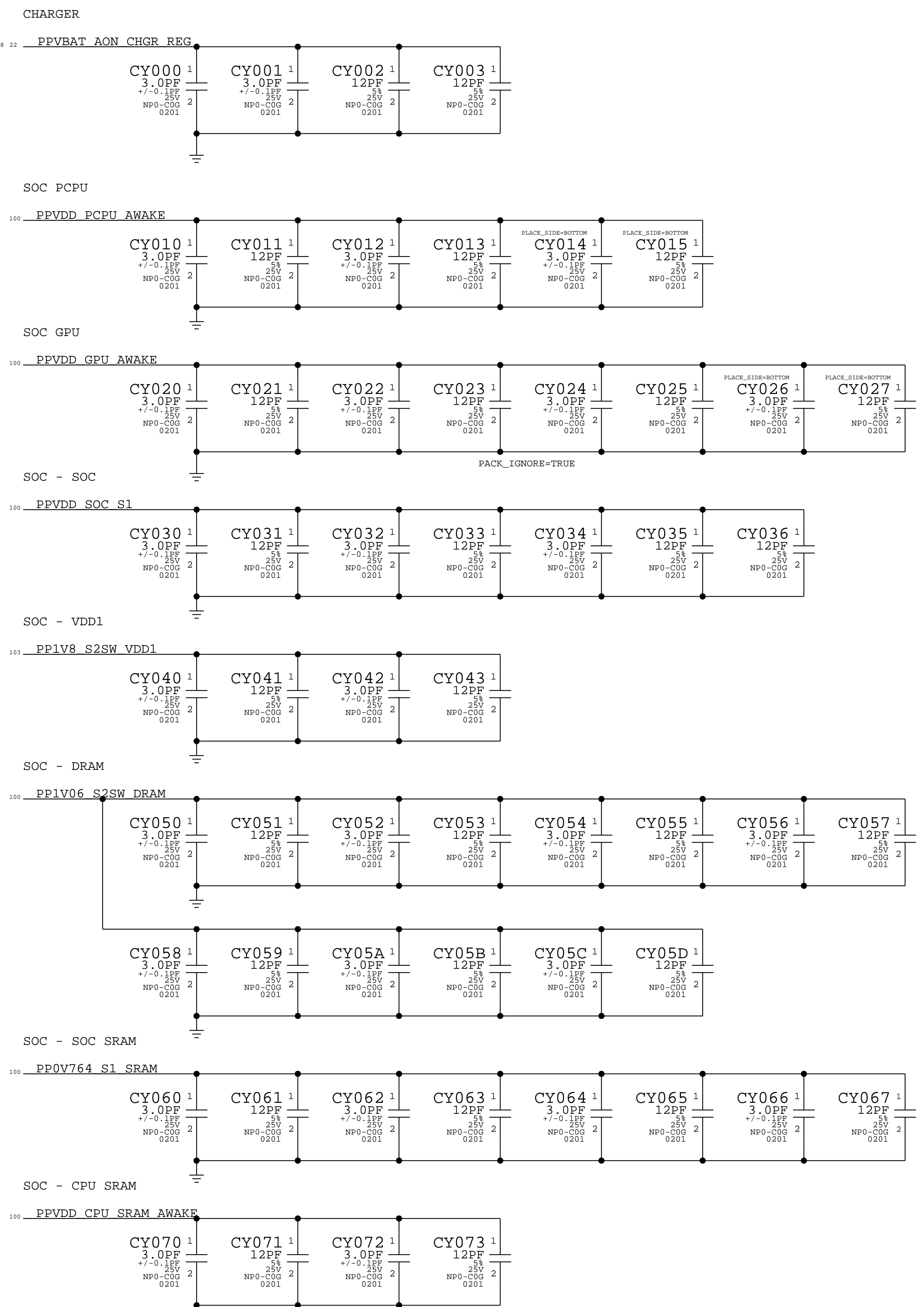
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BOM_COST_GROUP=DESENSE

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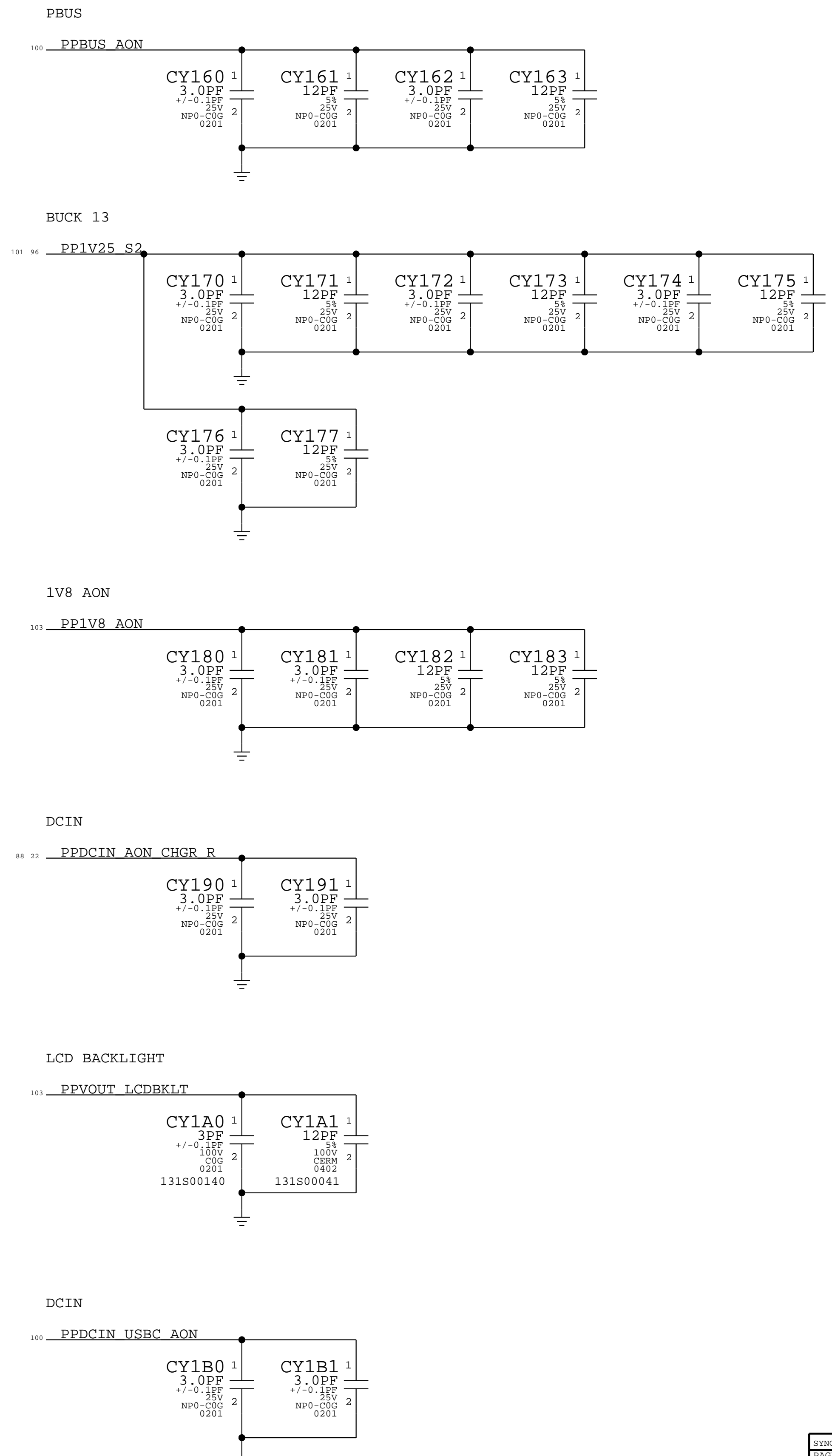
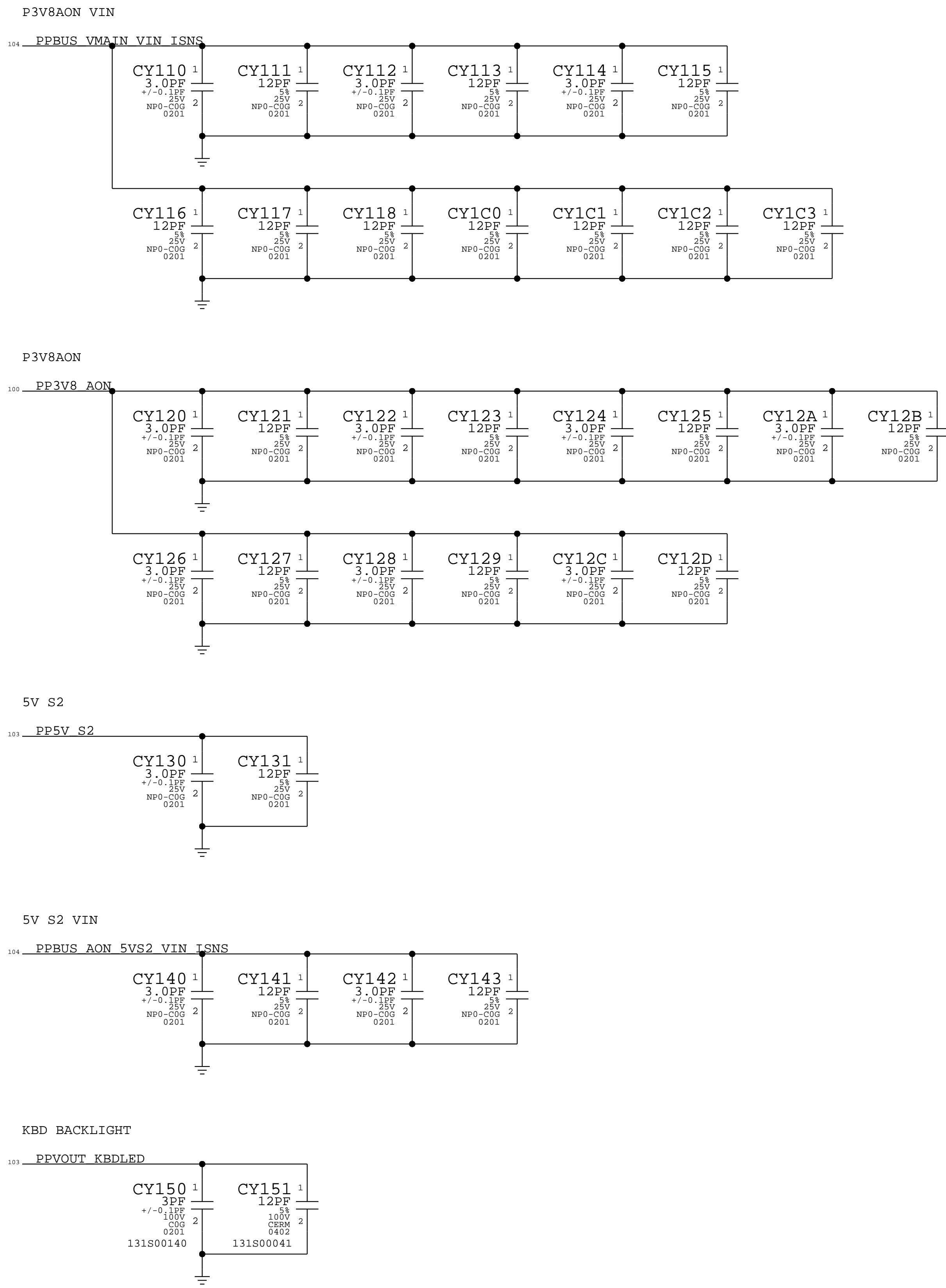
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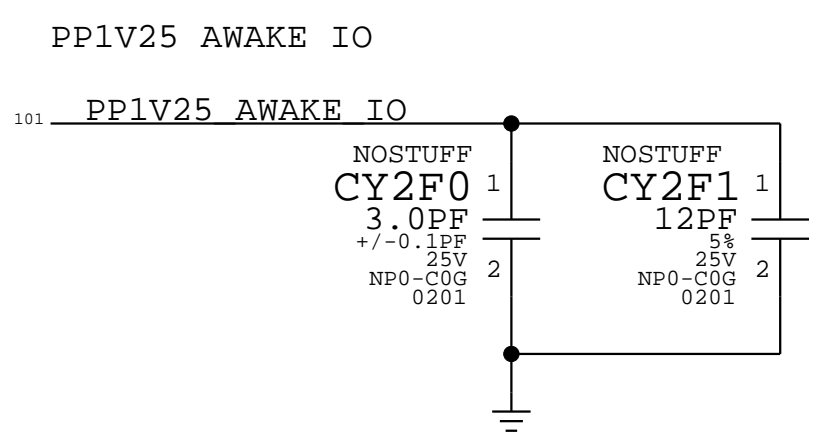
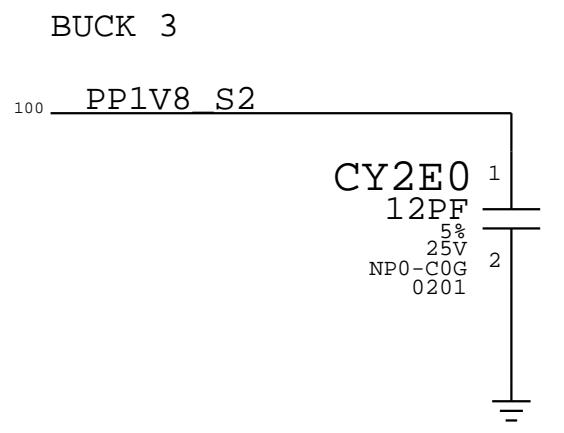
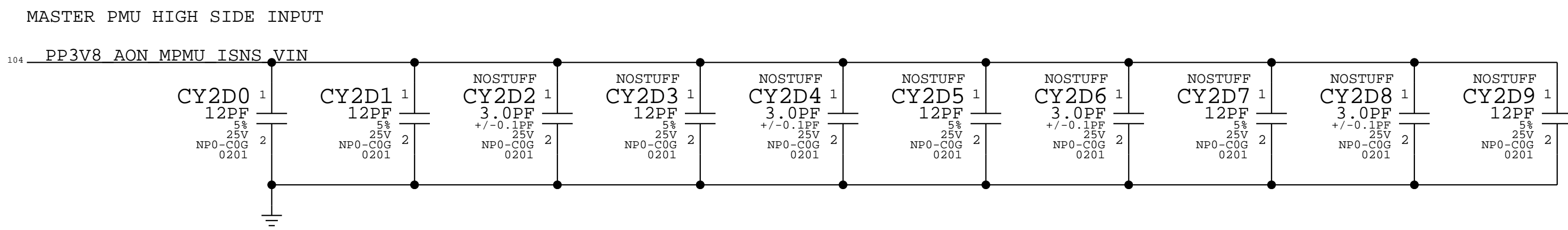
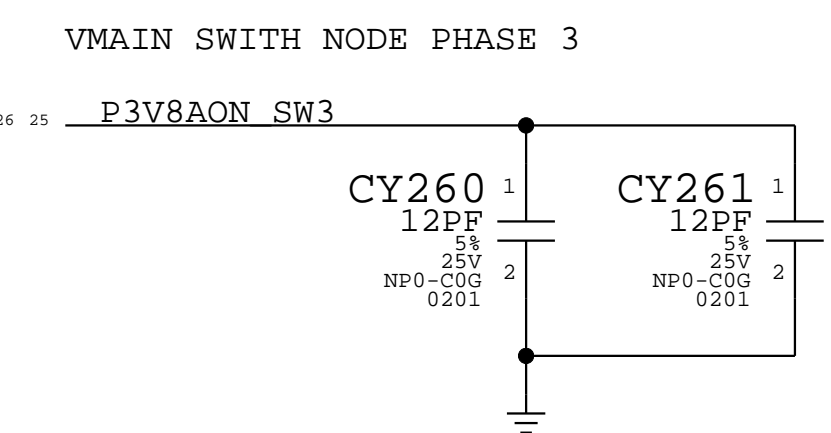
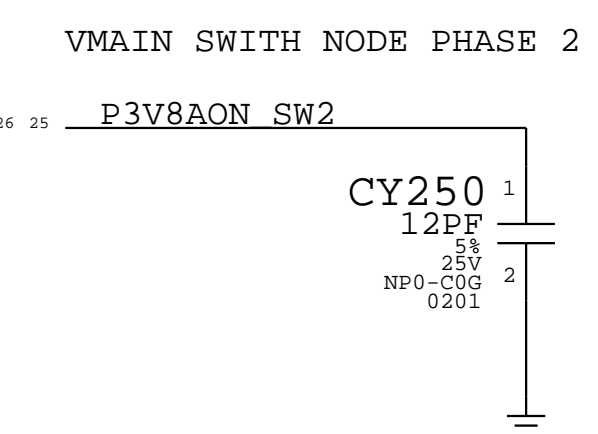
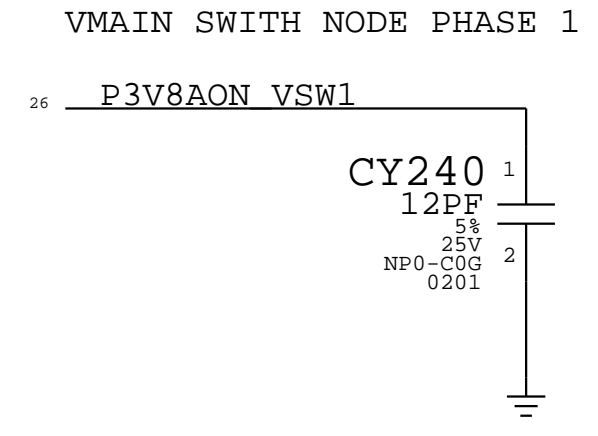
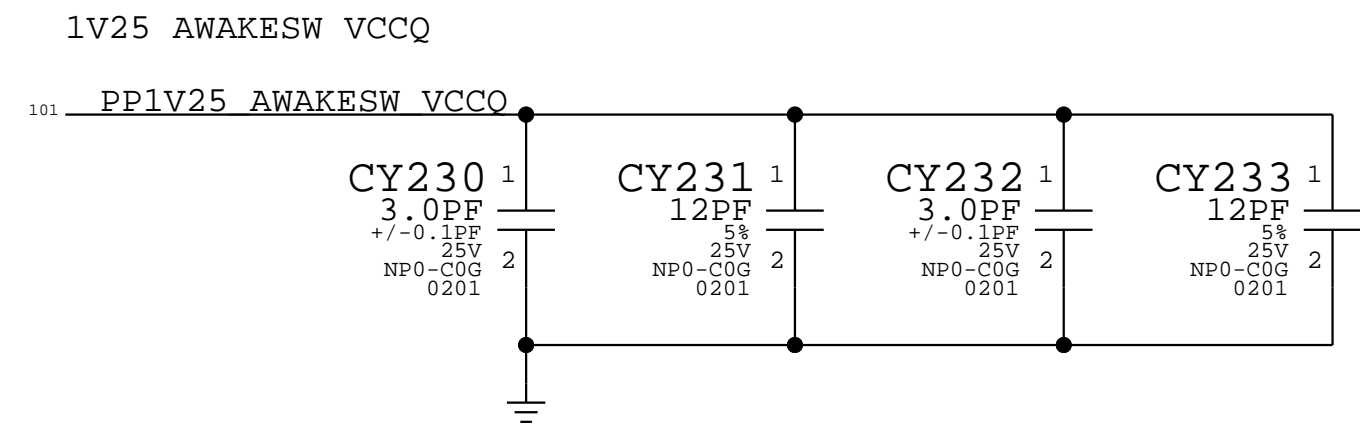
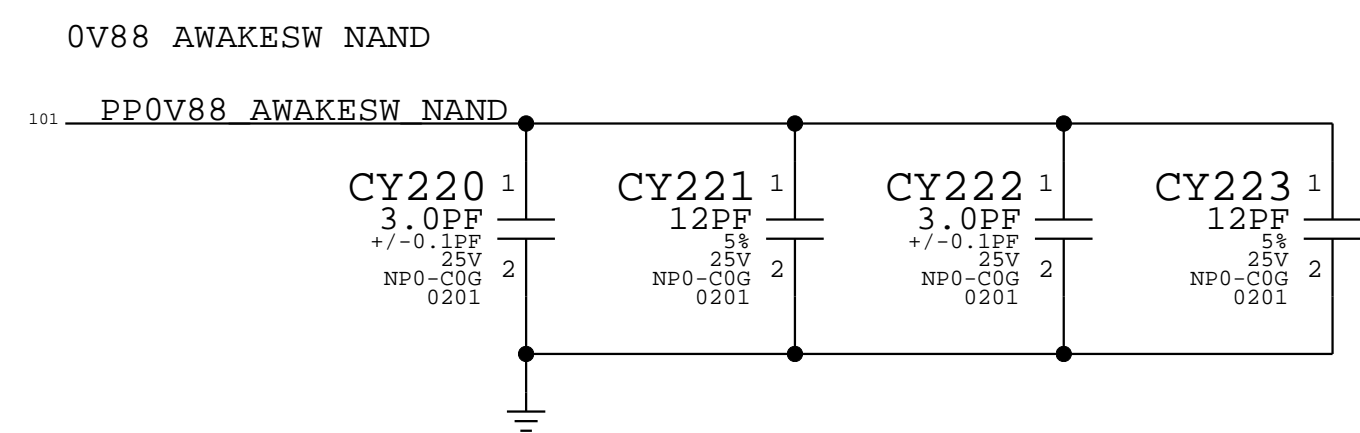
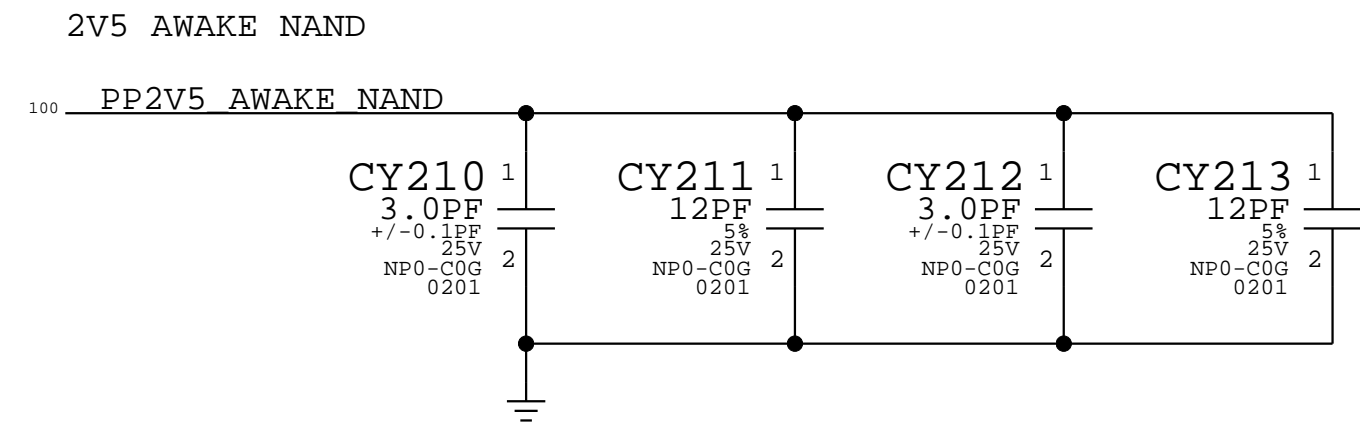
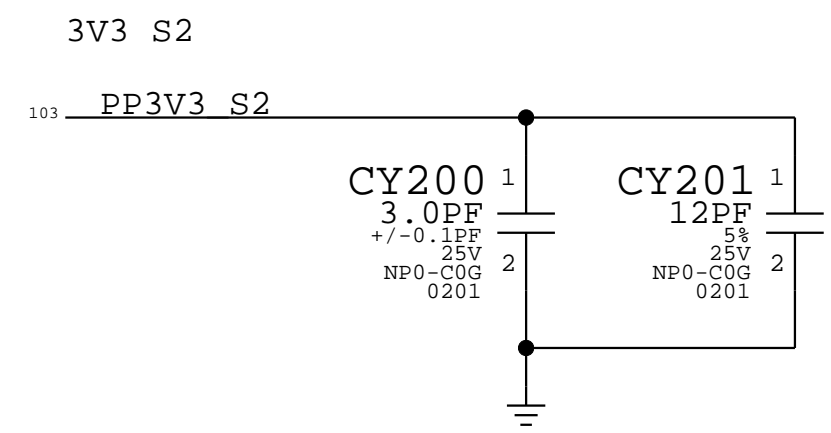
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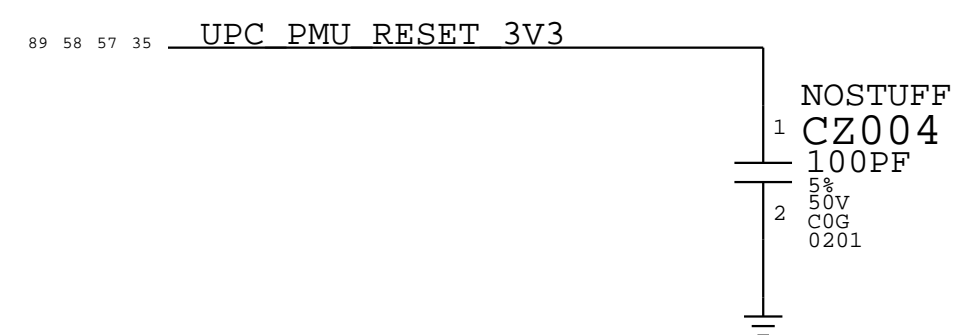
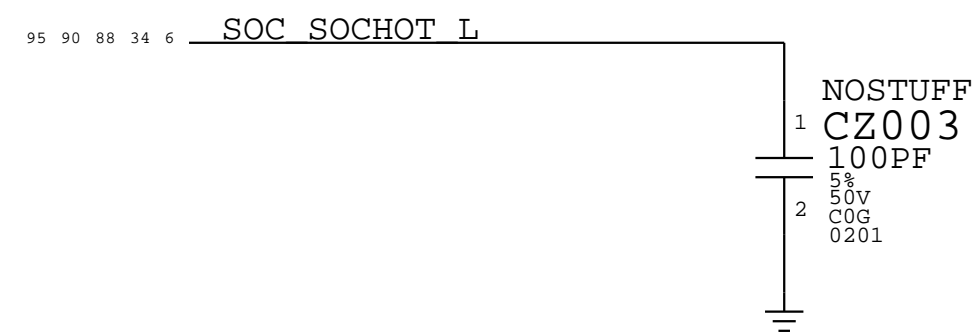
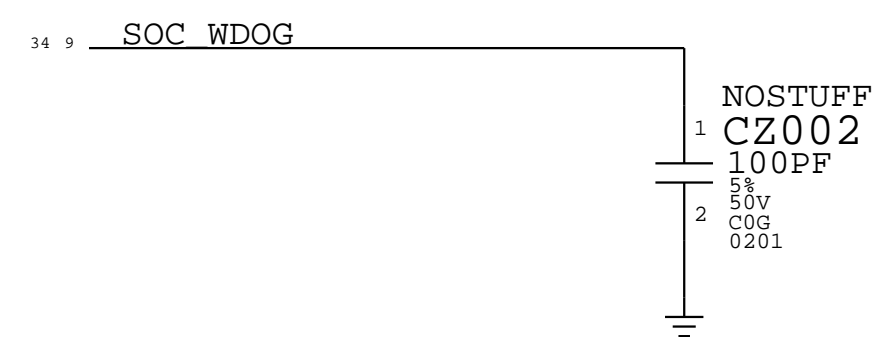
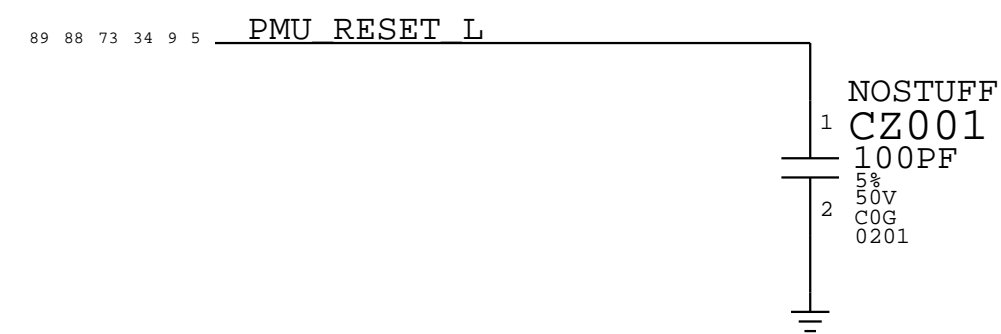
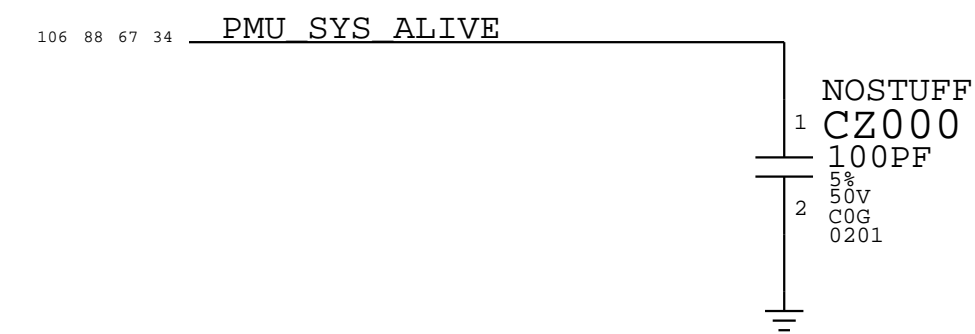
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		PAGE	301 OF 999
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BOM_COST_GROUP=DESENSE

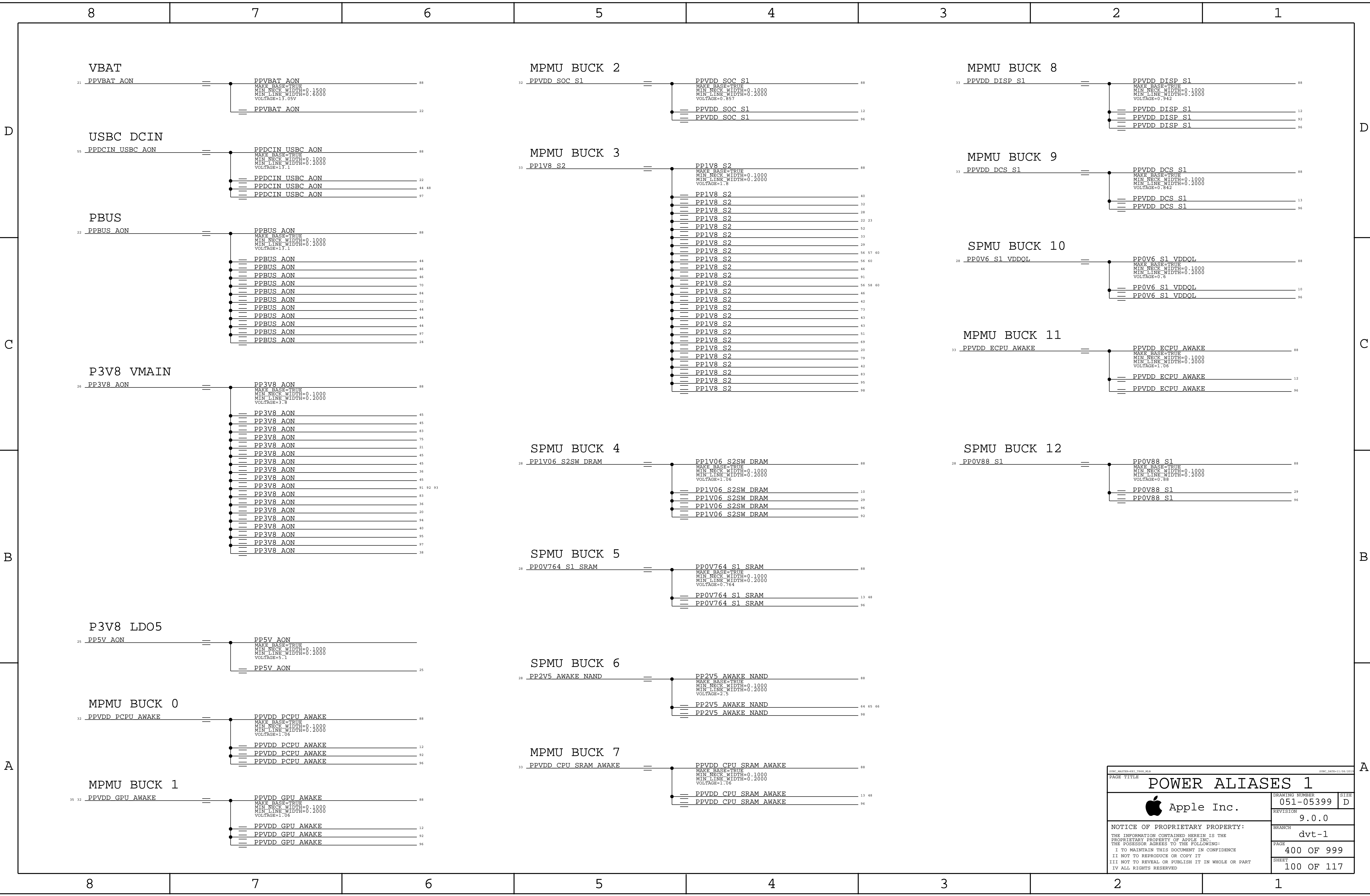
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PAGE TITLE			
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EMC REQUESTS FOR CAPS ON SOME SIGNALS
 NO-STUFF'ED UNTIL WE GET CONFIRMATION / DATA IF THEY ARE NEEDED
 <RDAR://58576418>



BOM_COST_GROUP=EMC

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	DRAWING NUMBER	051-05399	SIZE
	REVISION	9.0.0	D
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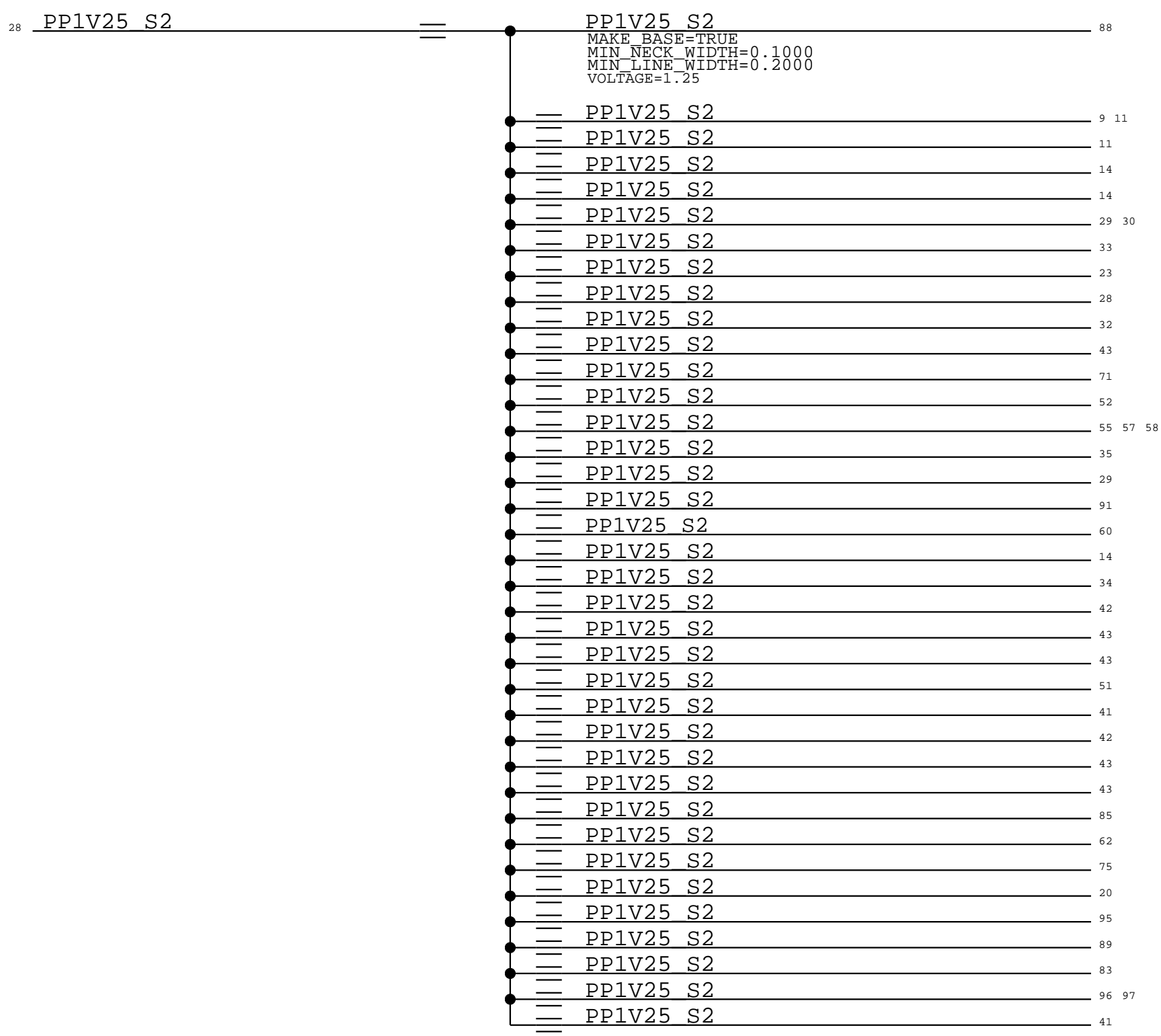
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PAGE: 400 OF 999			SHEET: 100 OF 117

POWER ALIASES 1

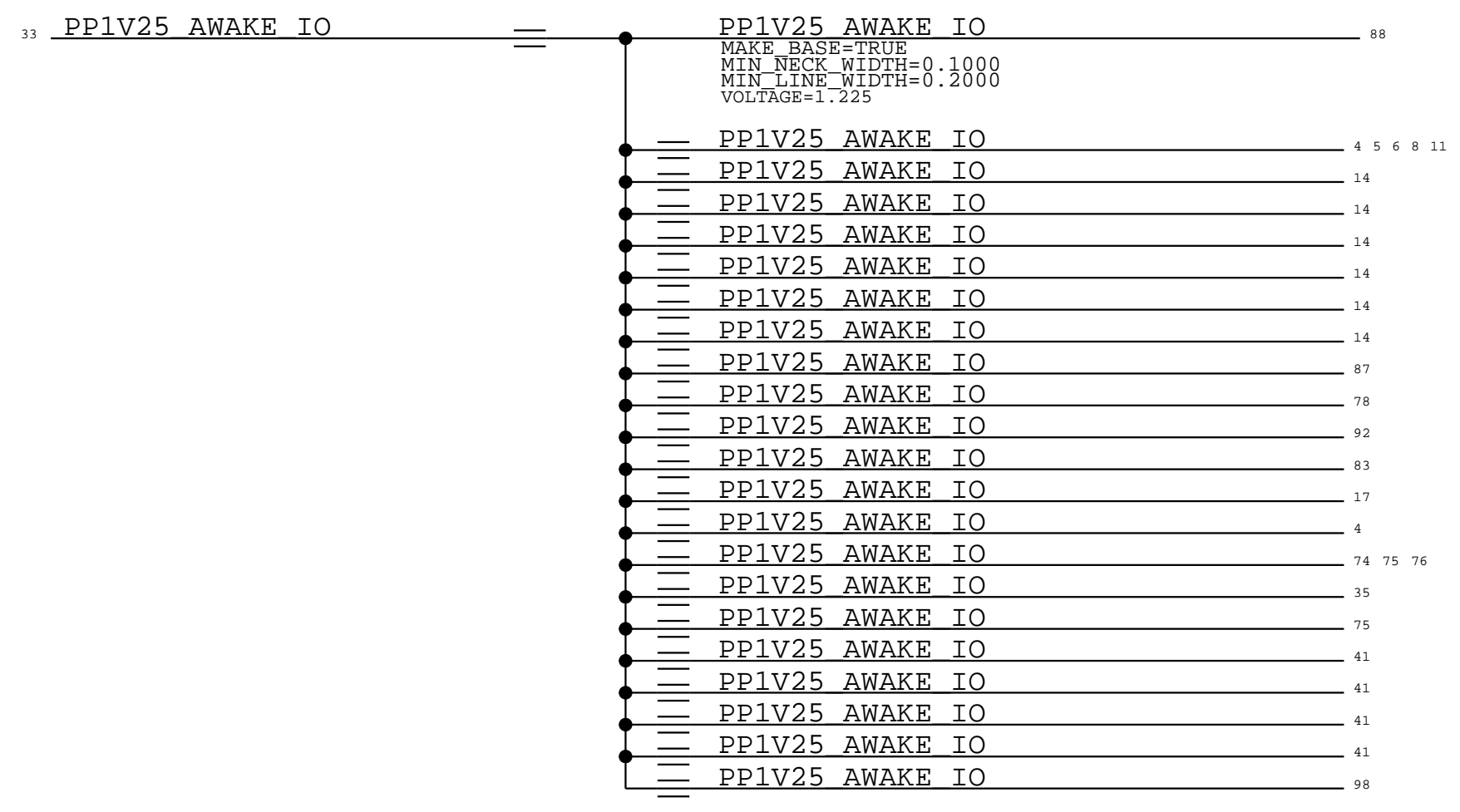
Apple Inc.

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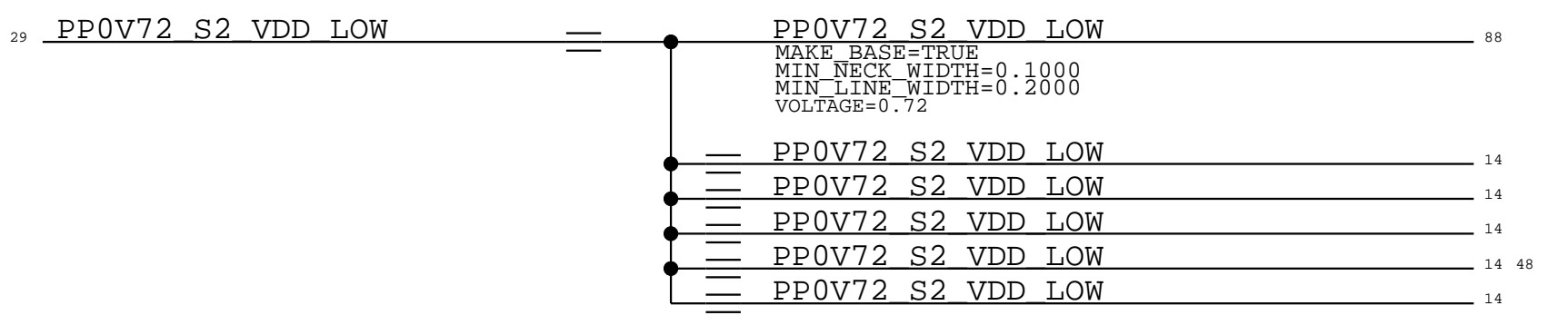
SPMU BUCK 13



MPMU BUCK 13 SW 3



SPMU LDO 4



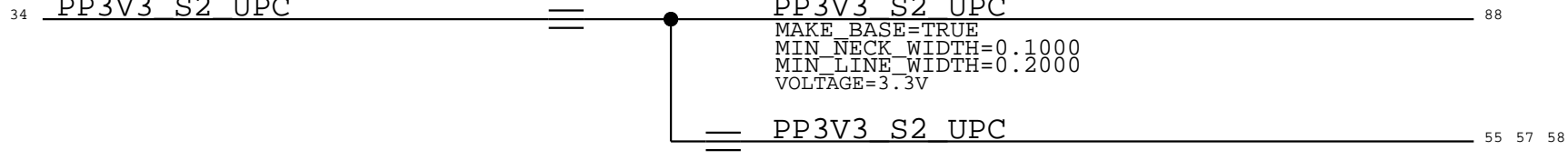
MPMU LDO 5



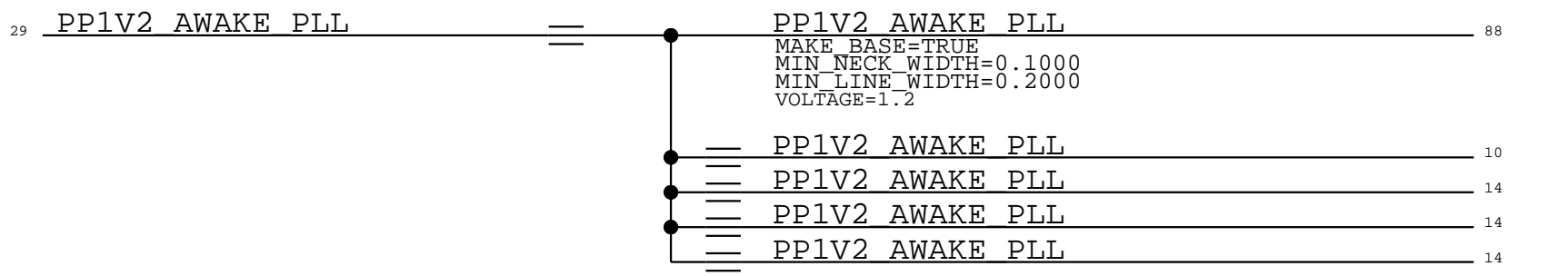
SPMU LDO 6



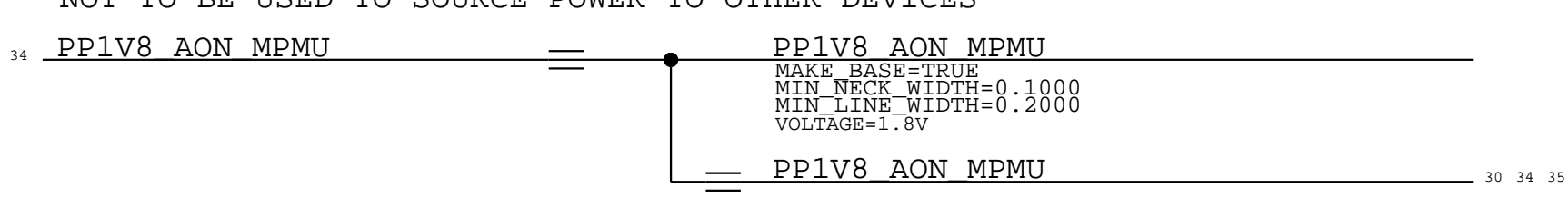
MPMU LDO 7



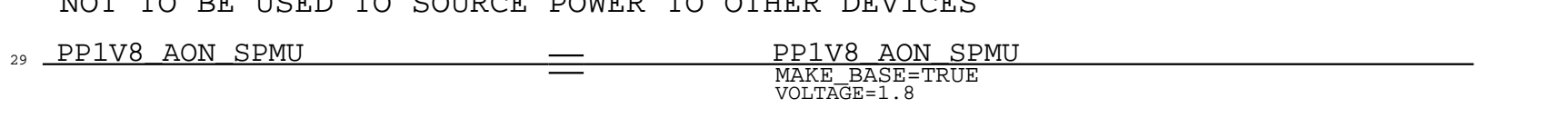
SPMU LDO 8



MPMU LDO 9



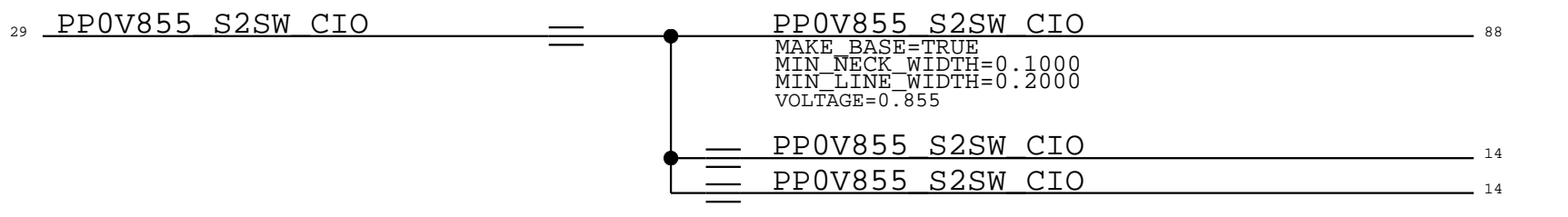
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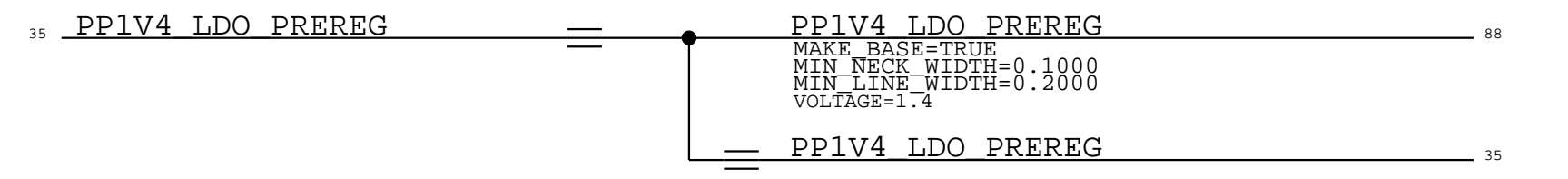
MPMU LDO 10



SPMU LDO 11



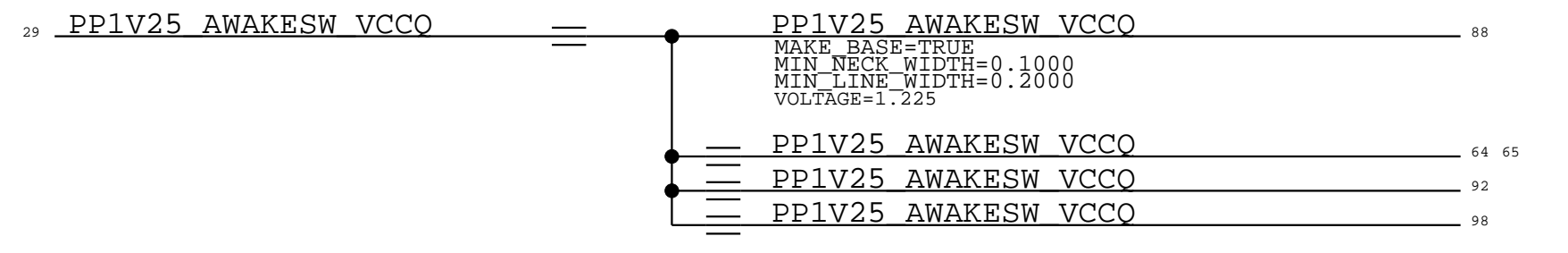
MPMU BUCK 14



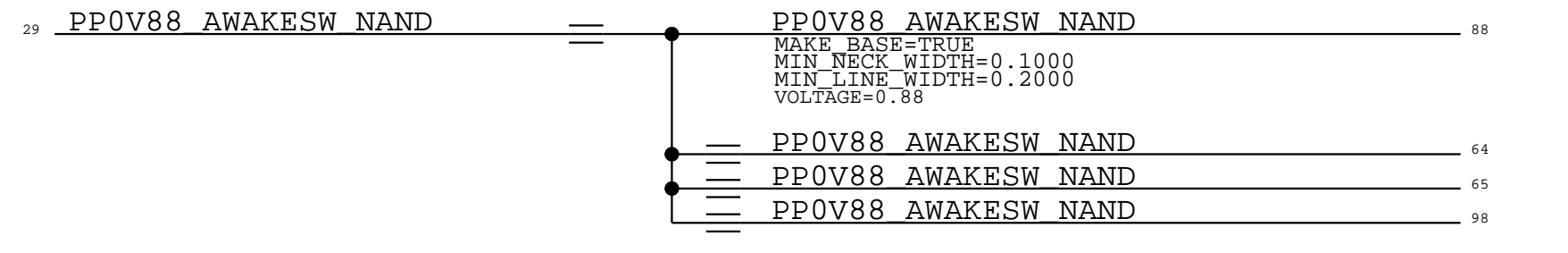
SPMU BUCK 3 SW 4

(NOT USED EXTERNALLY, SPMU GPIOs ONLY)

SPMU BUCK 13 SW 5



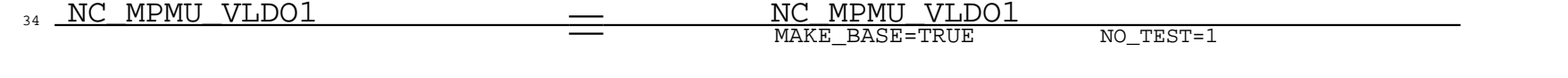
SPMU BUCK 12 SW 6



SPMU BUCK 12 SW 7

TIED TO SW6

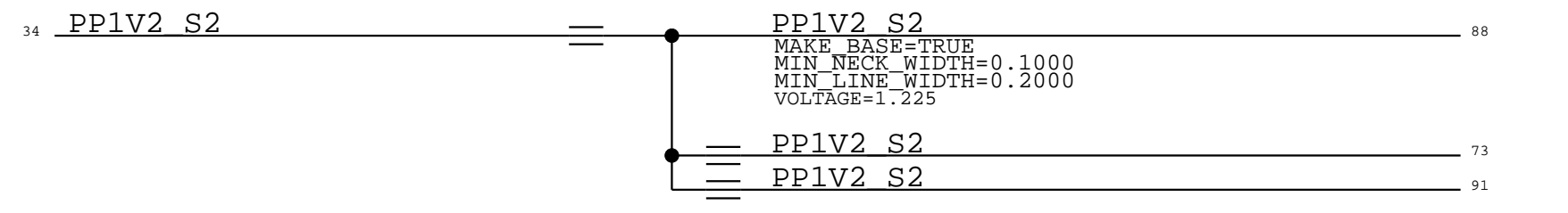
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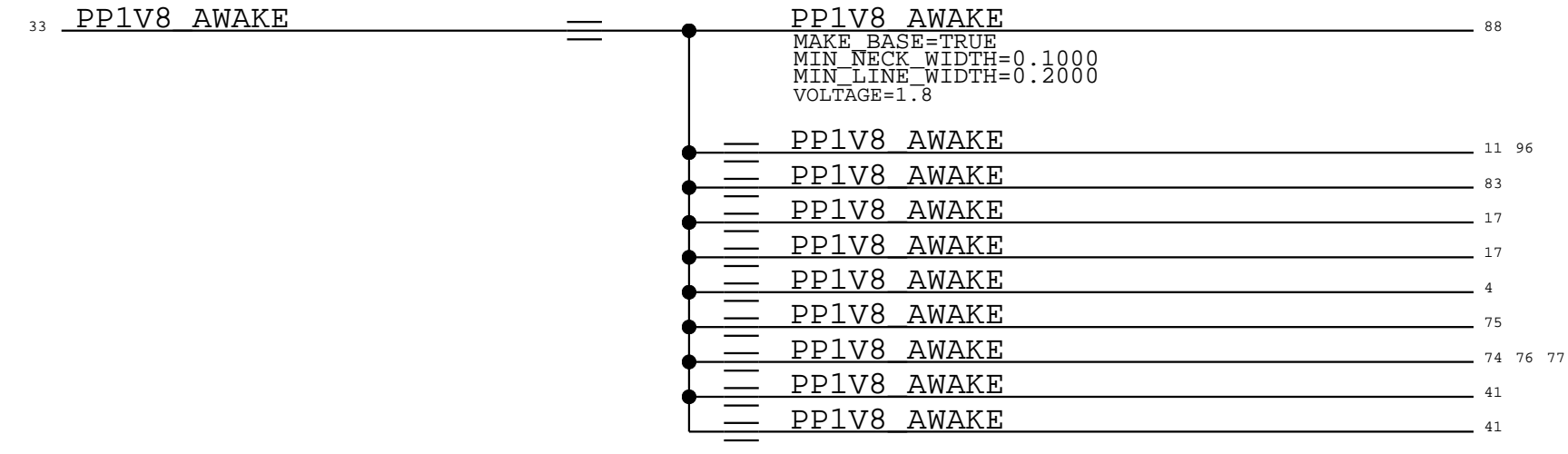
MPMU LDO 2

(NOT USED)

MPMU LDO 3



MPMU BUCK 3 SW 1

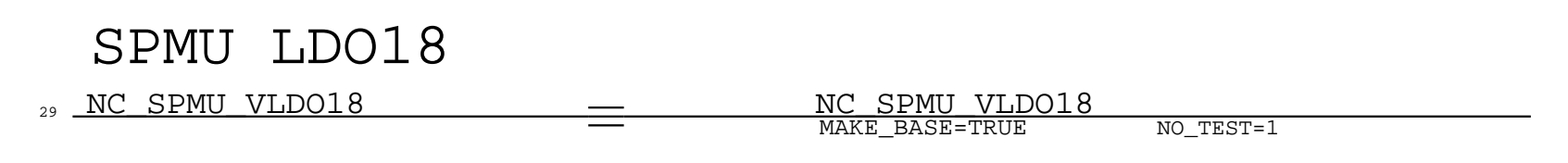
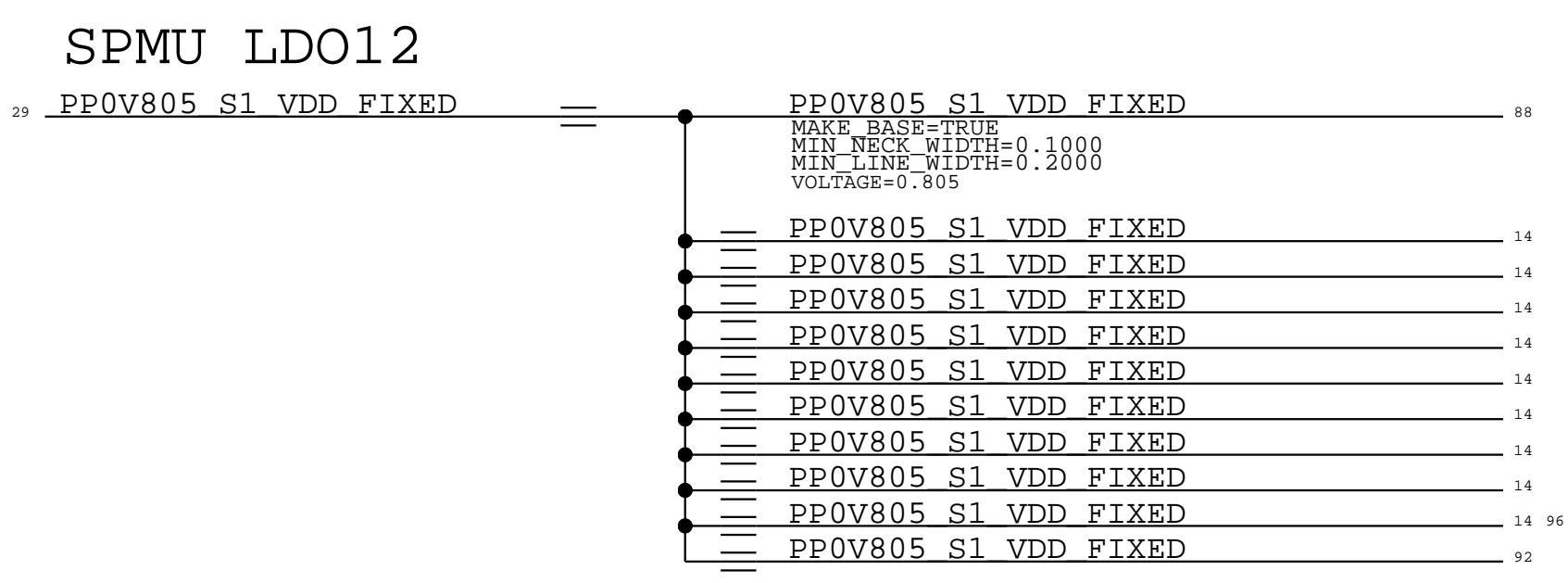


MPMU BUCK 3 SW 2

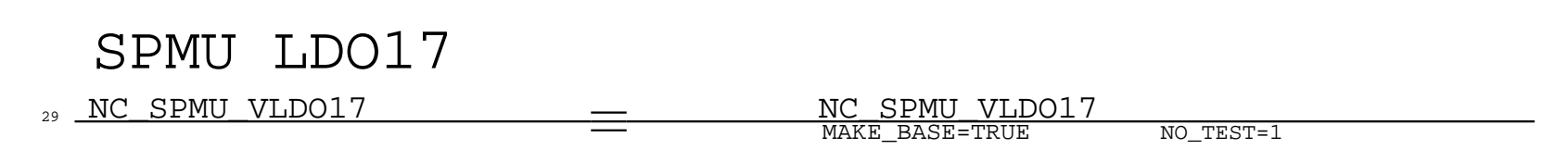
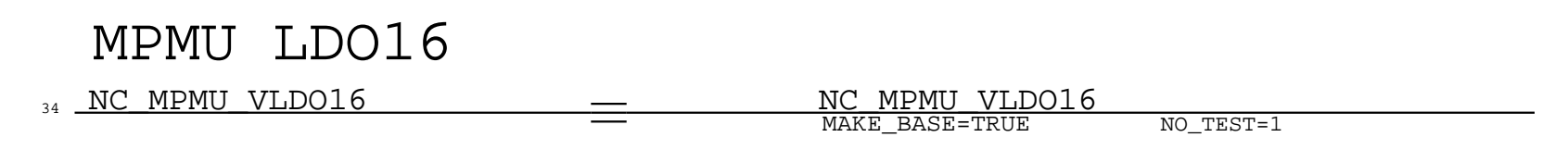
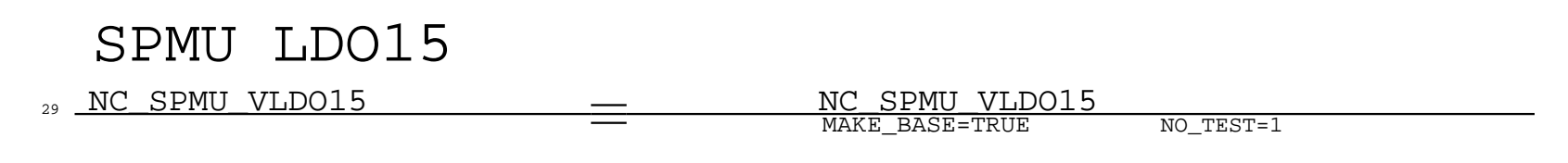
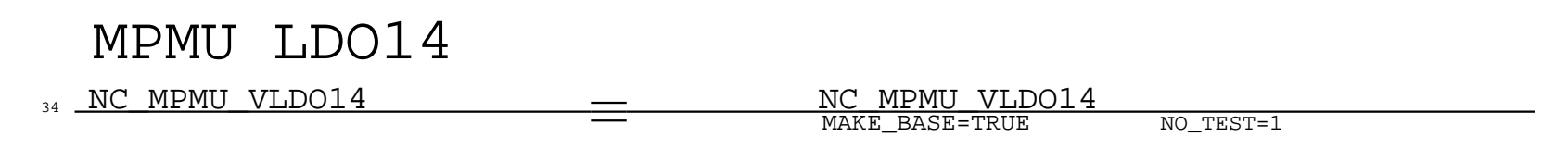
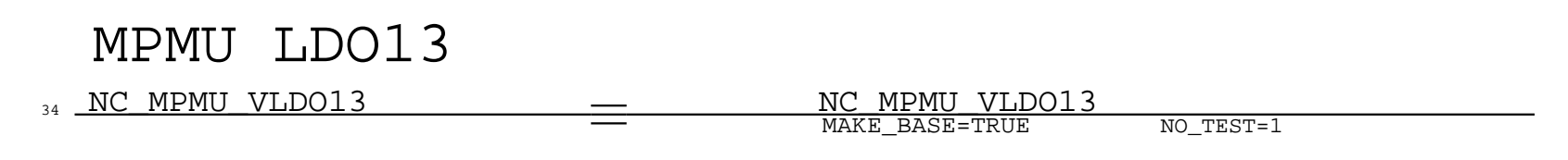
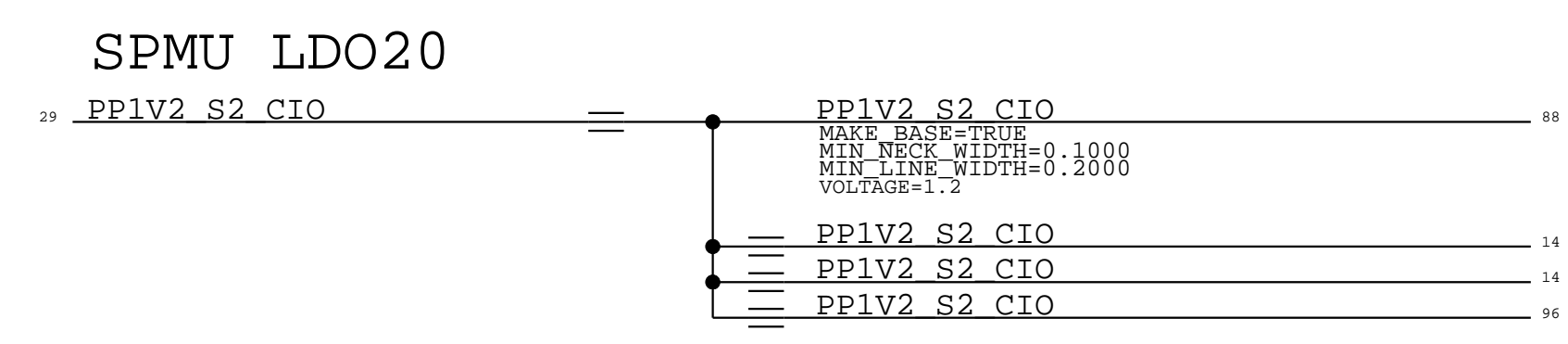
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BRANCH		dvt-1		
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MPMU LDO19
(NOT USED)



PAGE TITLE		POWER ALIASES 3	
DRAWING NUMBER	051-05399		SIZE
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REVISION	9.0.0		
BRANCH	dvt-1		
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<small>NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED</small>			

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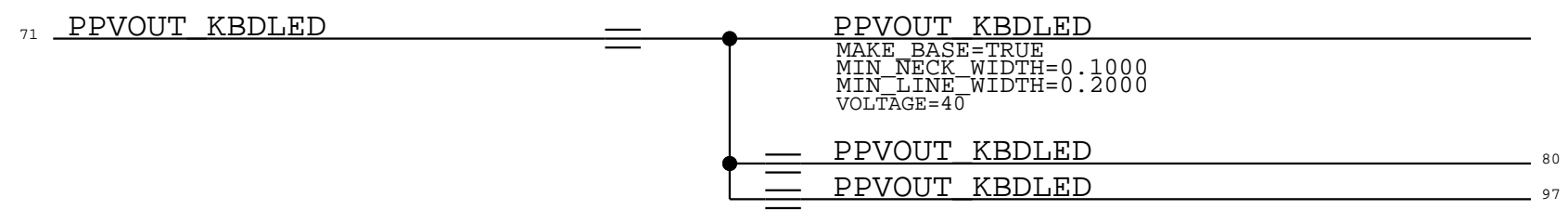
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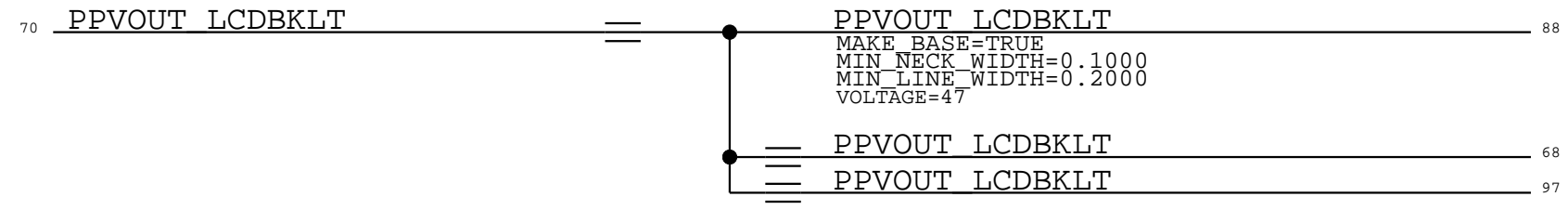
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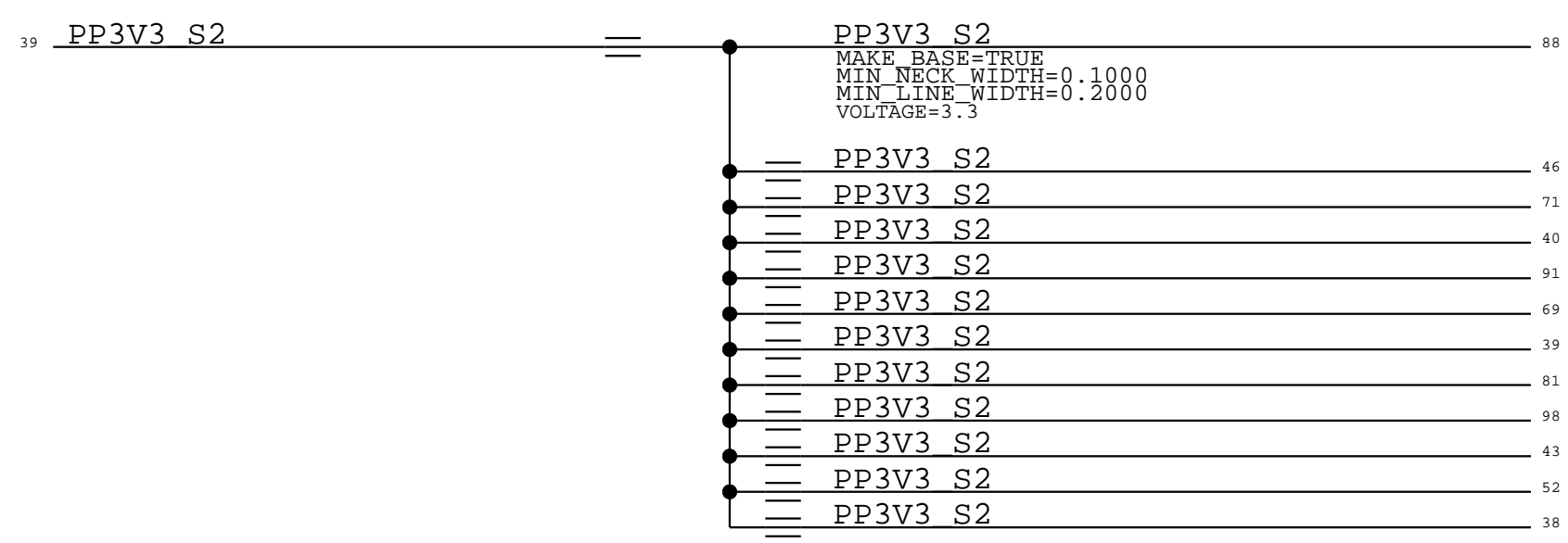
KEYBOARD BACKLIGHT



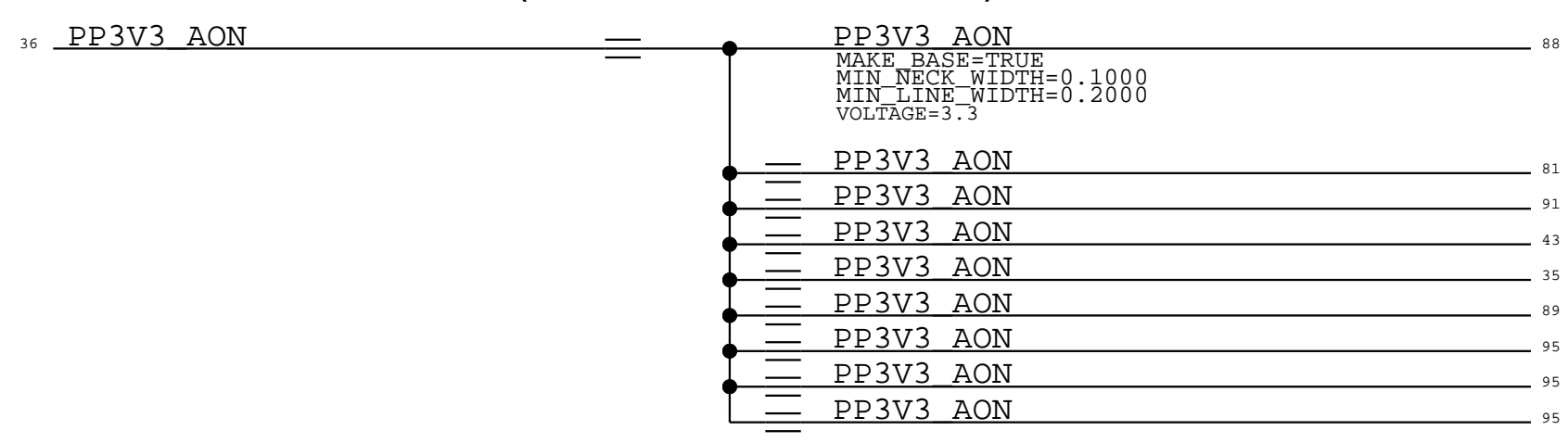
DISPLAY BACKLIGHT



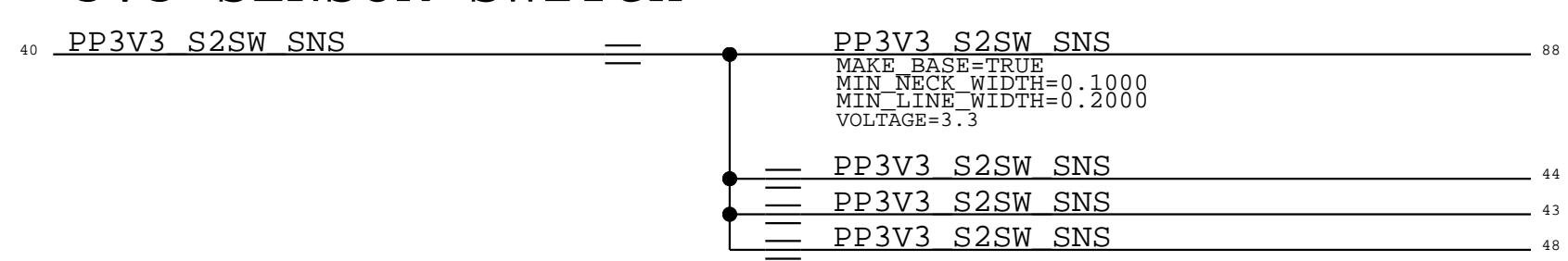
3V3 S2 VR



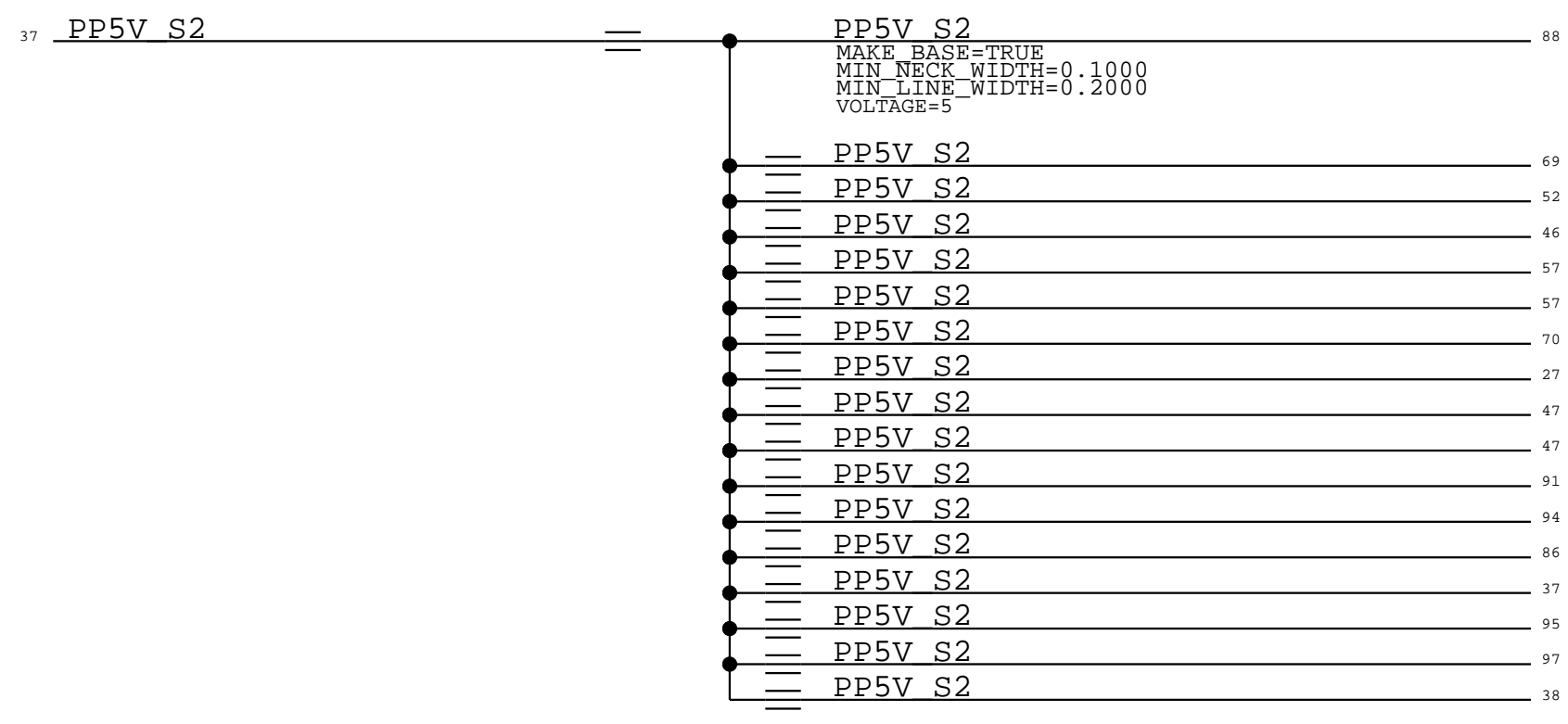
3V3 AON LDO (NEEDS REVIEW)



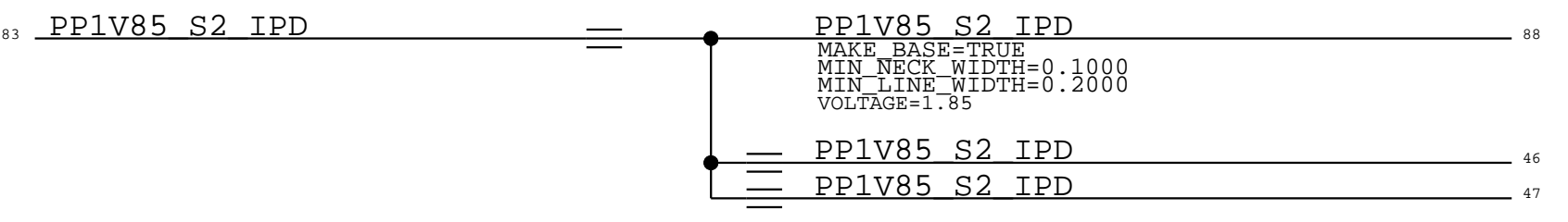
3V3 SENSOR SWITCH



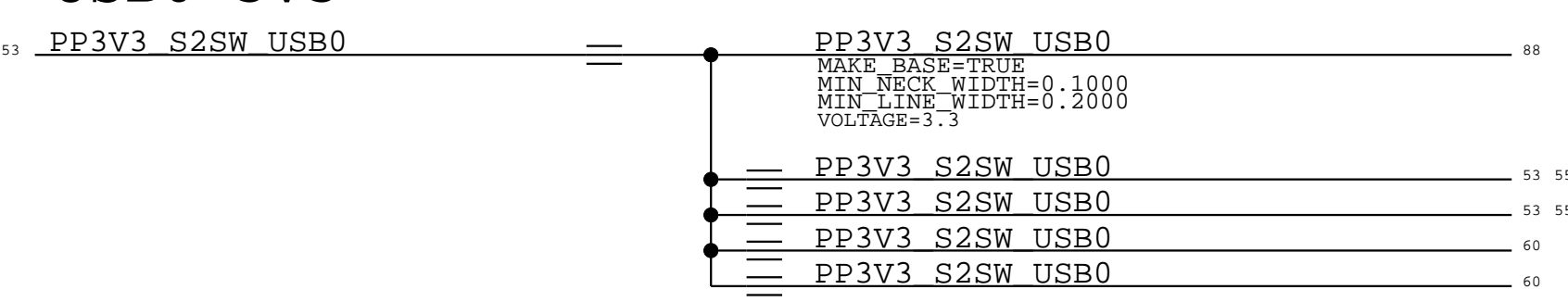
5V S2



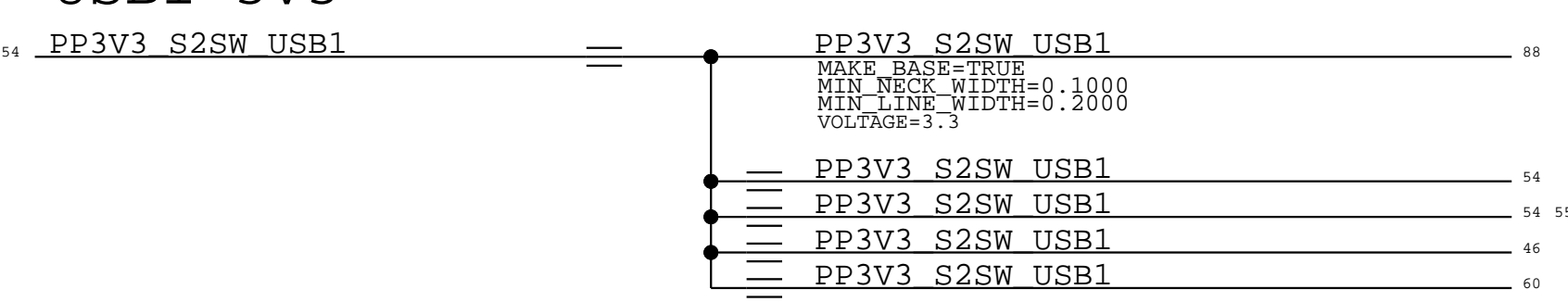
1V85 IPD



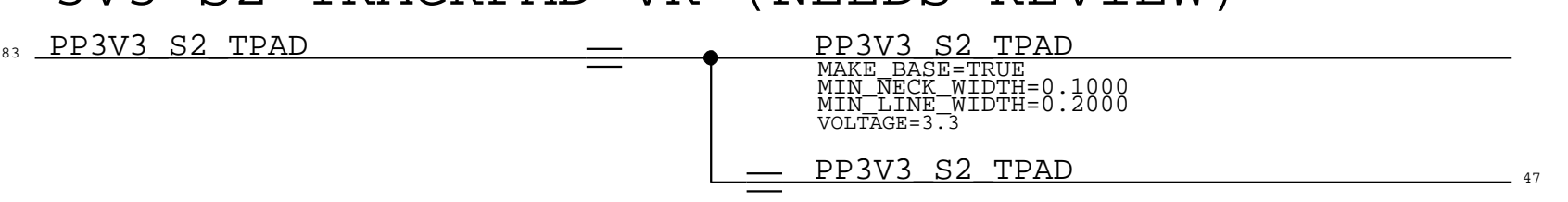
USB0 3V3



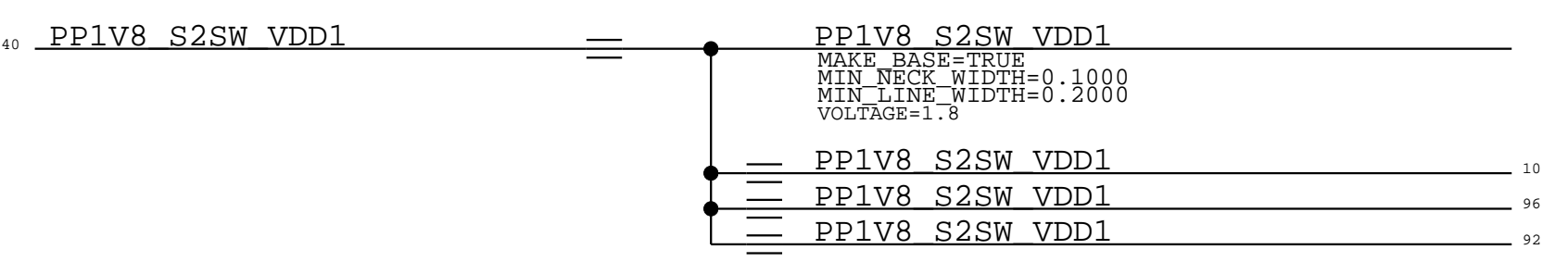
USB1 3V3



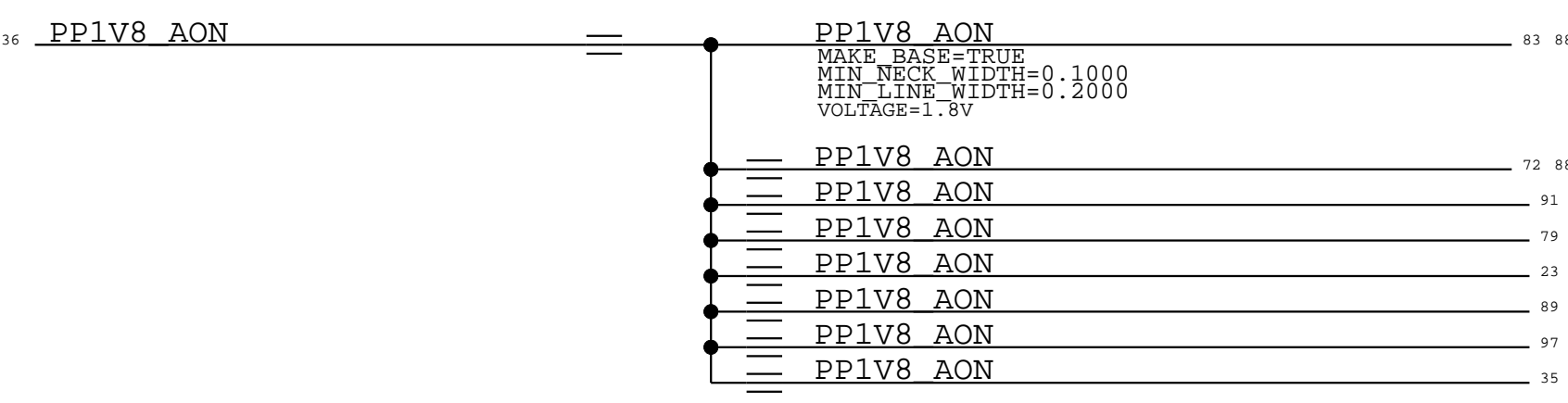
3V3 S2 TRACKPAD VR (NEEDS REVIEW)



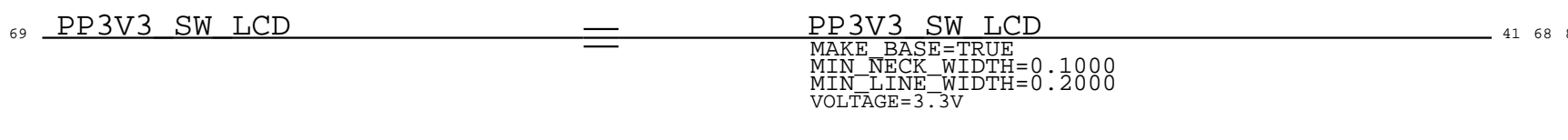
1V8 S2 SWITCH



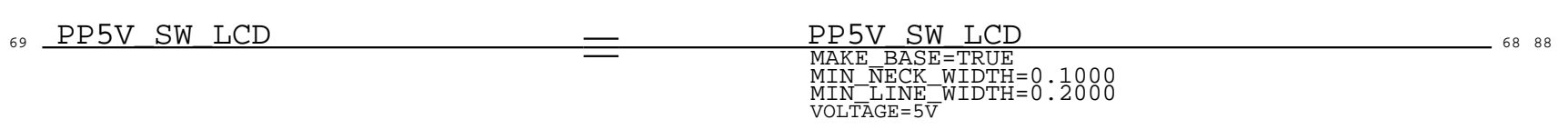
1V8 AON LDO



3V3 PANEL SWITCH

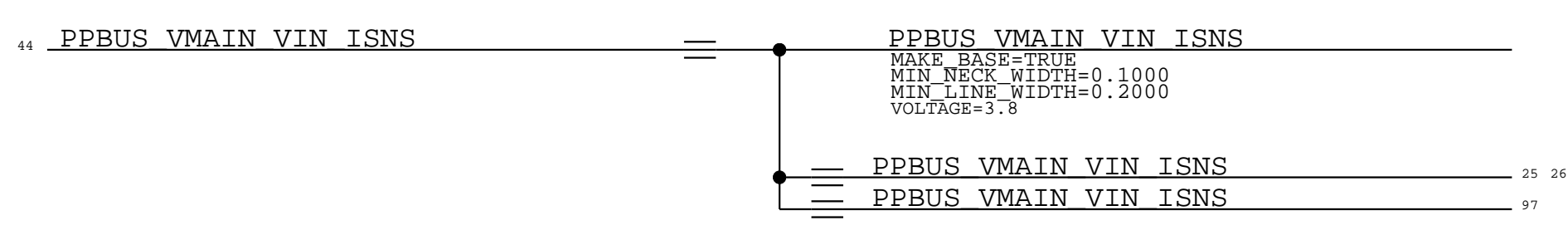


5V PANEL SWITCH

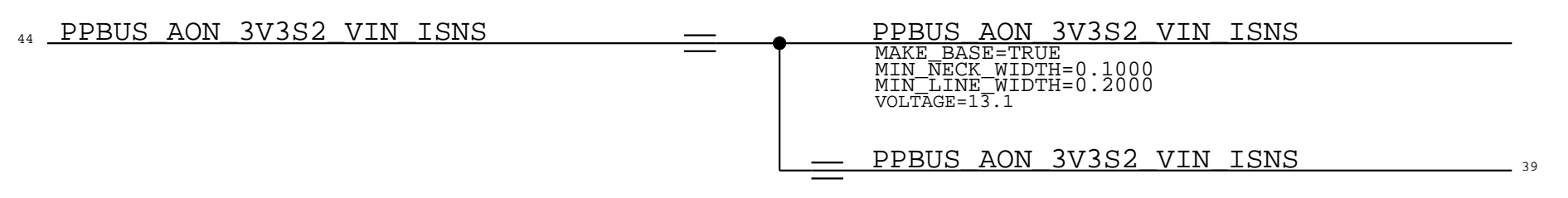


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DRAWING NUMBER		051-05399	SIZE
REVISION		9.0.0	D
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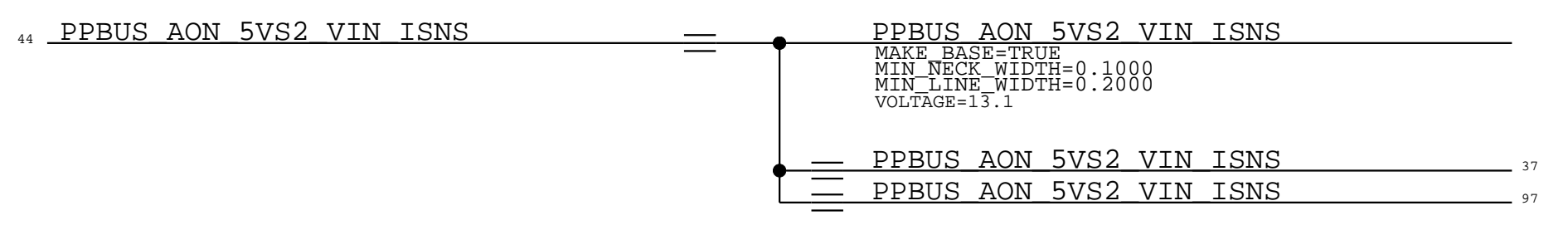
3V8 AON SENSE RESISTOR



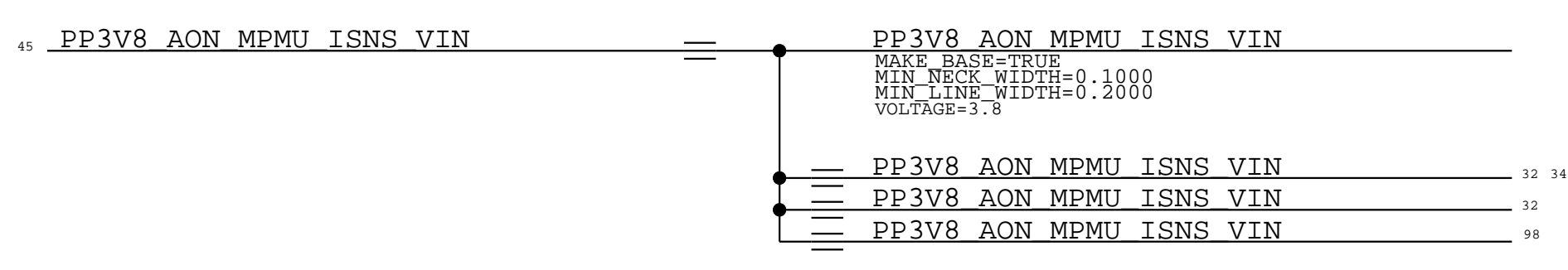
3V3 S2 VR HIGH SIDE SENSE RESISTOR



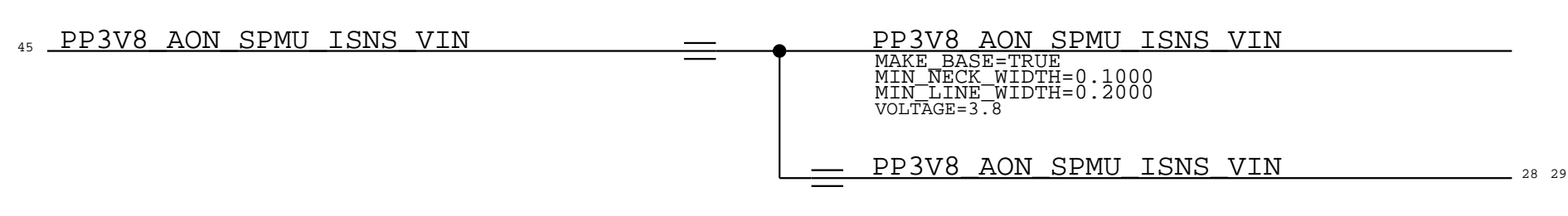
5V S2 VR HIGH SIDE SENSE RESISTOR



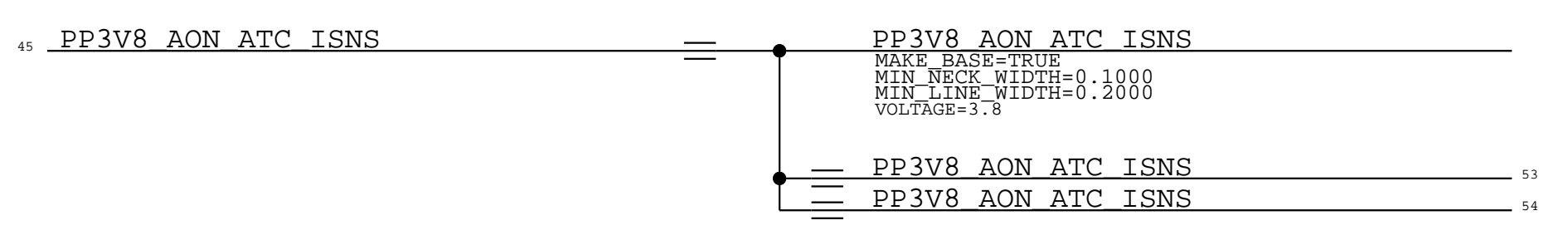
MASTER PMU HIGH SIDE SENSE RESISTOR



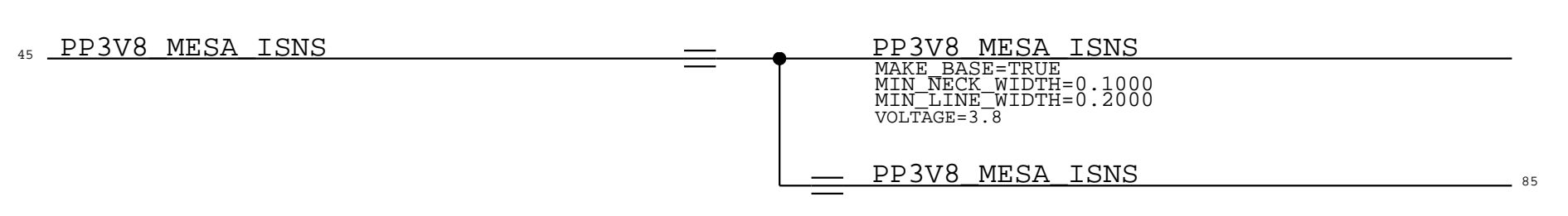
SLAVE PMU HIGH SIDE SENSE RESISTOR



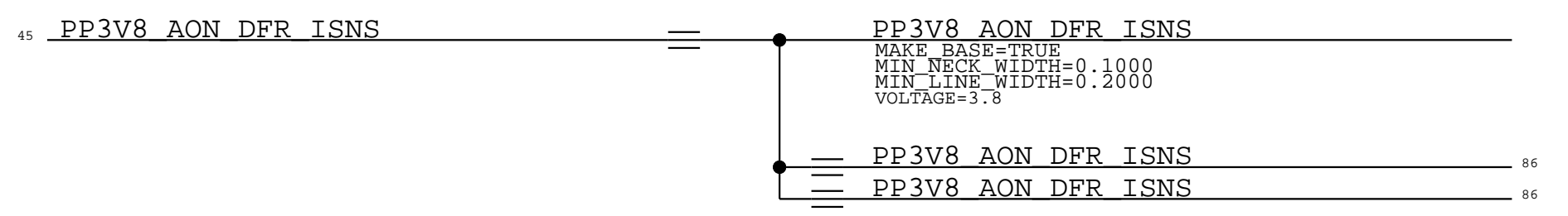
ATC 3V3 LDO HIGH SIDE SENSE RESISTOR



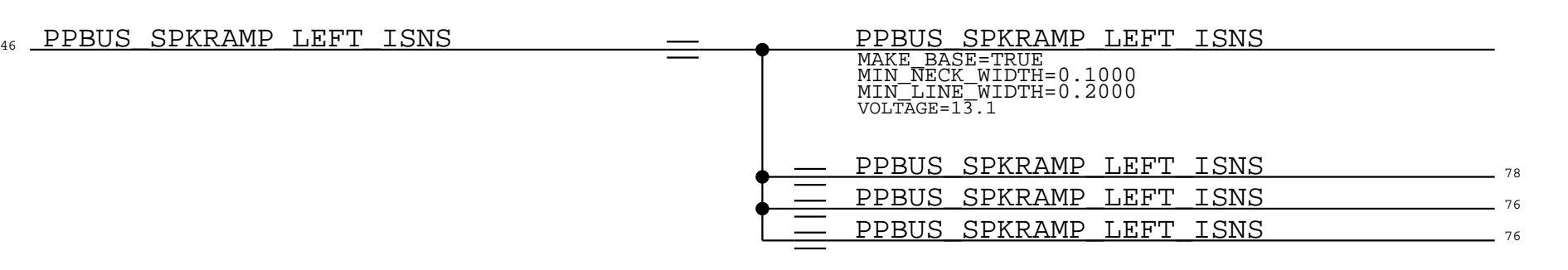
MESA HIGH SIDE SENSE RESISTOR



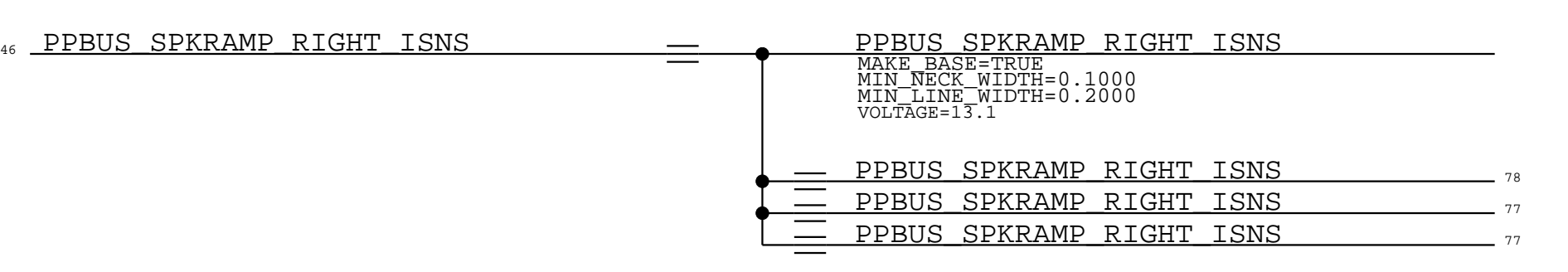
DFR 1.8/3.3V HIGH SIDE CURRENT SENSE (Ixxx)



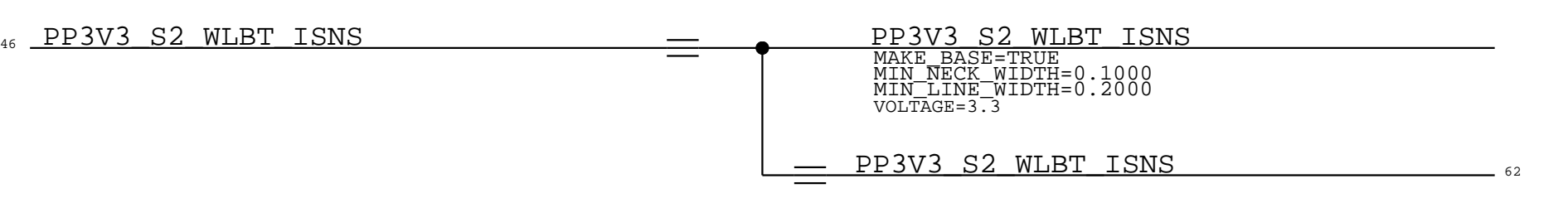
LEFT AMP SENSE RESISTOR



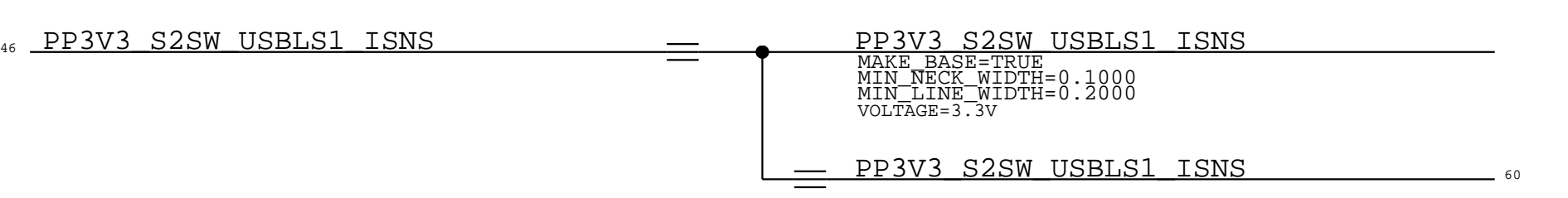
RIGHT AMP SENSE RESISTOR



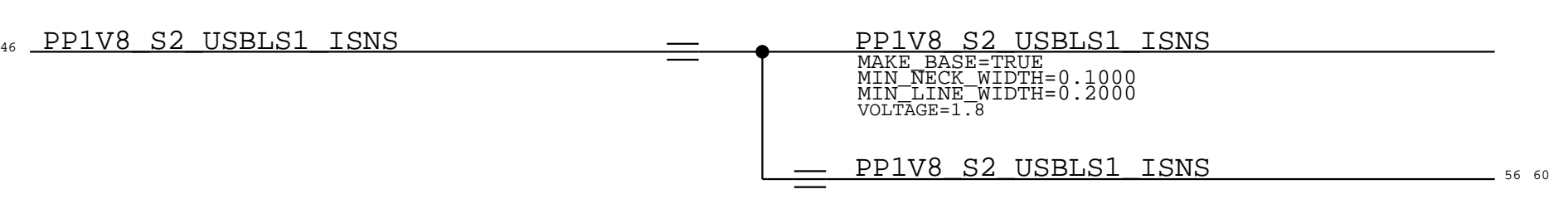
3V3 S2 WLANBT LOAD SIDE SENSE RESISTOR



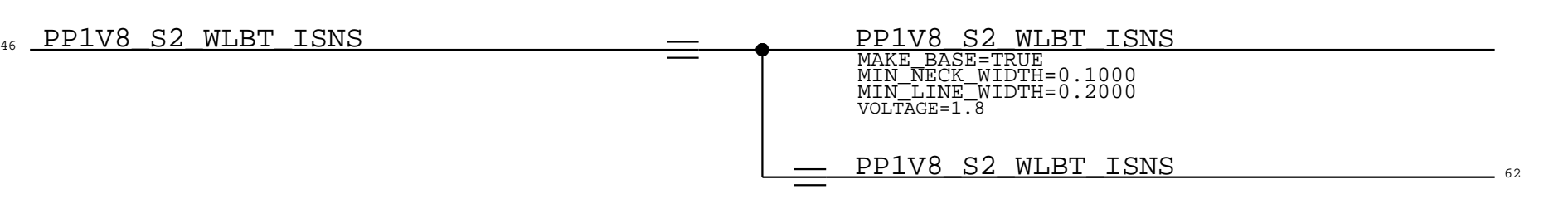
USB2 LEVEL SHIFTER 3.3V (UF750) SENSE RESISTOR



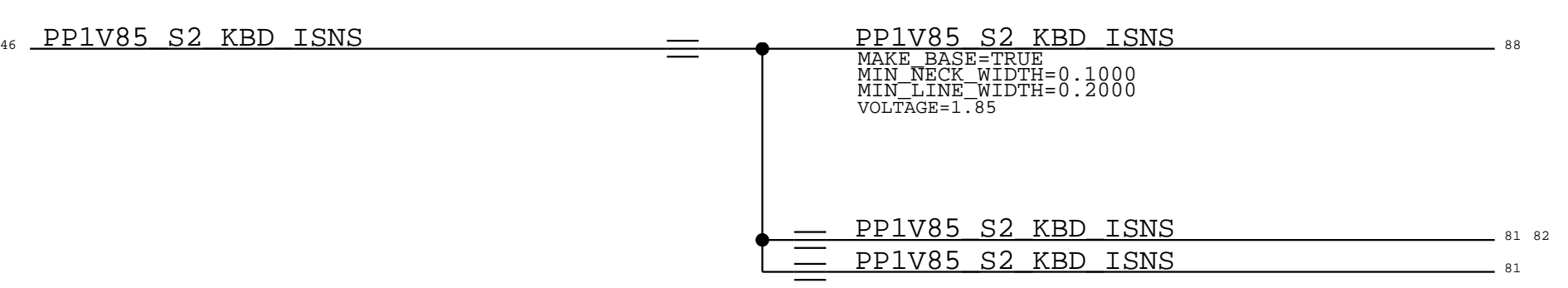
USB2 LEVEL SHIFTER 1.8V (UF750) SENSE RESISTOR



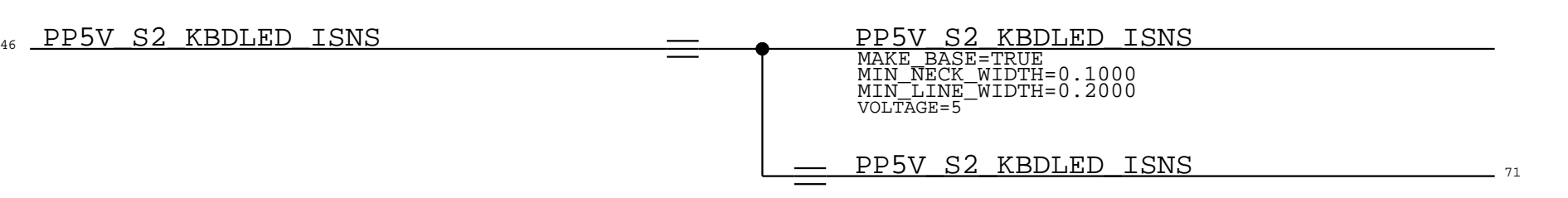
WLAN BT 1V8 S2 CURRENT SENSE (Ixxx)



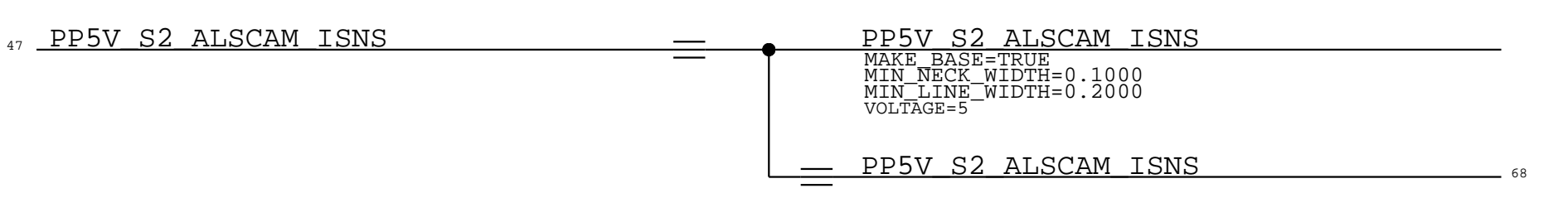
KEYBOARD 1.85V SENSE RESISTOR



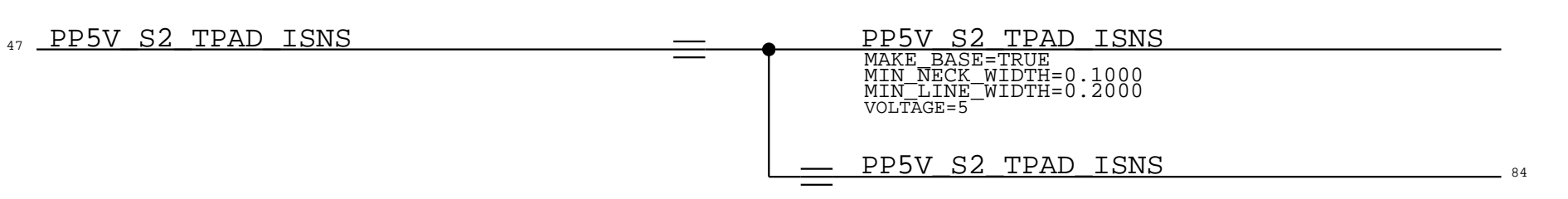
KEYBOARD LED 5V SENSE RESISTOR



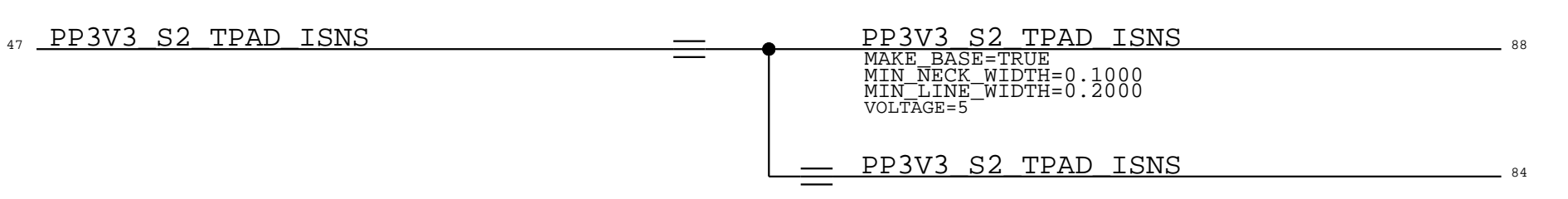
ALSCAM 5V SENSE RESISTOR



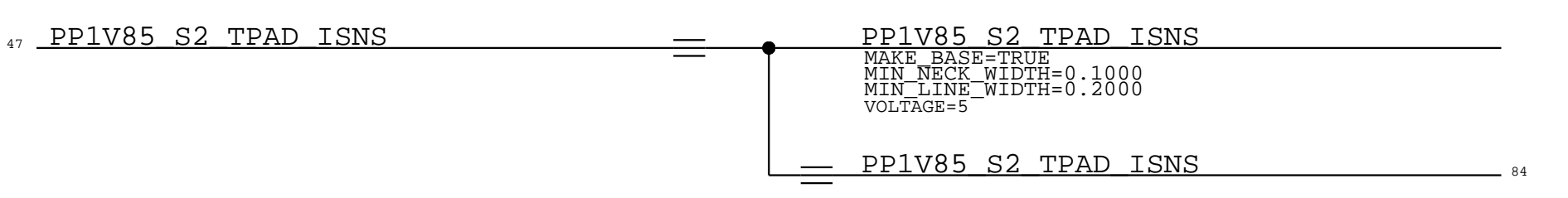
TPAD 5V SENSE RESISTOR



TPAD 3.3V RESISTOR



TPAD 1.85V SENSE RESISTOR



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8	7	6	5	4	3	2	1
TGA PCIE GP1 NC		TGA AP GPIO NC & TP		TGA GPIO NC			
NC PCIE USBHC D2R POS	NC PCIE USBHC D2R POS	NC SOC GPIO08	NC SOC GPIO08	NC SOC GPIO01	NC SOC GPIO01		
NC PCIE USBHC D2R NEG	NC PCIE USBHC D2R NEG	TP SWD UPC SWDIO1	TP SWD UPC SWDIO1	NC SOC GPIO15	NC SOC GPIO15		
NC PCIE USBHC R2D C POS	NC PCIE USBHC R2D C POS	TGA AOP GPIO NC & RESOLVE		NC SOC GPIO16	NC SOC GPIO16		
NC PCIE USBHC R2D C NEG	NC PCIE USBHC R2D C NEG	NC R1 DUMP TRIG	NC R1 DUMP TRIG	NC ENET SYNC 1588	NC ENET SYNC 1588		
NC PCIE CLK100M USBHC POS	NC PCIE CLK100M USBHC POS	NC AOP FUNC1	NC AOP FUNC1	TGA SOC			
NC PCIE CLK100M USBHC NEG	NC PCIE CLK100M USBHC NEG	NC R1 RTC SYNC	NC R1 RTC SYNC	TP SOC AMUX OUT	TP SOC AMUX OUT		
NC USBHC RESET L	NC USBHC RESET L	NC R1 INT	NC R1 INT	TGA UART NC			
TGA PCIE GP2 NC		NC SPI R1 CS L	NC SPI R1 CS L	NC UART3 D2R CTS L	NC UART3 D2R CTS L		
NC PCIE ENET D2R POS	NC PCIE ENET D2R POS	NC AOP FUNC5	NC AOP FUNC5	NC UART3 R2D RTS L	NC UART3 R2D RTS L		
NC PCIE ENET D2R NEG	NC PCIE ENET D2R NEG	SPI GYRO CS L	SPI GYRO CS L	NC UART3 D2R	NC UART3 D2R		
NC PCIE ENET R2D C POS	NC PCIE ENET R2D C POS	GYRO INT	GYRO INT	NC UART3 R2D	NC UART3 R2D		
NC PCIE ENET R2D C NEG	NC PCIE ENET R2D C NEG	GYRO MOTION INT	GYRO MOTION INT	NC UART4 D2R CTS L	NC UART4 D2R CTS L		
NC PCIE CLK100M ENET POS	NC PCIE CLK100M ENET POS	NC AOP FUNC10	NC AOP FUNC10	NC UART4 R2D RTS L	NC UART4 R2D RTS L		
NC PCIE CLK100M ENET NEG	NC PCIE CLK100M ENET NEG	NC ALS INT L	NC ALS INT L	NC UART4 D2R	NC UART4 D2R		
NC ENET CLKREQ L	NC ENET CLKREQ L	NC AOP FUNC14	NC AOP FUNC14	NC UART4 R2D	NC UART4 R2D		
NC ENET RESET L	NC ENET RESET L	TGA AOP PDM NC		NC UART7 RXD	NC UART7 RXD		
TGA BOARD ID RESOLVE		SPI DFR CS L	NC PDM CLK1	NC UART7 TXD	NC UART7 TXD		
TGA SSPIO		NC PDM DATA1	NC PDM DATA1	TGA MIPI NC			
NC SSPIO MOSI	NC SSPIO MOSI	NC PDM CLK2	NC PDM CLK2	NC MIPI0C CLK POS	NC MIPI0C CLK POS		
TGA SOC I2S NC		NC PDM CLK5	NC PDM CLK5	NC MIPI0C CLK NEG	NC MIPI0C CLK NEG		
NC SOC I2S1 MCK	NC SOC I2S1 MCK	NC PDM CLK6	NC PDM CLK6	NC MIPI0C DATA 0 POS	NC MIPI0C DATA 0 POS		
NC SOC I2S0 MCK	NC SOC I2S0 MCK	NC PDM DATA2	NC PDM DATA2	NC MIPI0C DATA 0 NEG	NC MIPI0C DATA 0 NEG		
TGA I2S3 NC		TGA AOP I2C		NC MIPI0C DATA 1 POS	NC MIPI0C DATA 1 POS		
NC I2S3 BCLK	NC I2S3 BCLK	I2C AOP ALS SCL	I2C AOP ALS SCL	NC MIPI0C DATA 1 NEG	NC MIPI0C DATA 1 NEG		
NC I2S3 D2R	NC I2S3 D2R	I2C AOP ALS SDA	I2C AOP ALS SDA	NC MIPI FTCCAM DATA POS1	NC MIPI FTCCAM DATA POS1		
NC I2S3 R2D	NC I2S3 R2D	TGA AOP SPMI NC		NC MIPI FTCCAM DATA NEG1	NC MIPI FTCCAM DATA NEG1		
NC I2S3 LRCLK	NC I2S3 LRCLK	NC AOP SPMI0 SCLK	NC AOP SPMI0 SCLK	TGA LPDP AUX, TX NC			
NC I2S3 MCLK	NC I2S3 MCLK	NC AOP SPMI0 SDATA	NC AOP SPMI0 SDATA	NC LPDPX AUX0	NC LPDPX AUX0		
TGA ISP GPIOS NC		TGA NUB & NUB GPIO & NUB SWD		NC LPDPX AUX1	NC LPDPX AUX1		
NC ISP GPIO1	NC ISP GPIO1	TP SOC DOCK ATTENTION	TP SOC DOCK ATTENTION	NC LPDPX AUX2	NC LPDPX AUX2		
NC FTCAM RESET L	NC FTCAM RESET L	NC BKLT PWR ON SMC LED SEL	NC BKLT PWR ON SMC LED SEL	NC LPDPX AUX3	NC LPDPX AUX3		
TGA SMC I2C RESOLVE		IPD SPI INT L	IPD SPI INT L	NC LPDPX AUX4	NC LPDPX AUX4		
I2C SMC PWR SCL	I2C SMC PWR SCL	CHGR INT L	CHGR INT L	NC LPDPX AUX5	NC LPDPX AUX5		
I2C SMC PWR SDA	I2C SMC PWR SDA	NC ENET I2C LOM INT L	NC ENET I2C LOM INT L	NC LPDPX AUX6	NC LPDPX AUX6		
I2C SMC IPD SCL	I2C SMC IPD SCL	NC ACDC ID	NC ACDC ID	NC LPDPX AUX7	NC LPDPX AUX7		
I2C SMC IPD SDA	I2C SMC IPD SDA	NC ACDC BURST EN L	NC ACDC BURST EN L	NC LPDPX AUX8	NC LPDPX AUX8		
TGA DISPLAY NC & RESOLVE		NC SPI DP2HDMI HOLD L	NC SPI DP2HDMI HOLD L	NC LPDPX AUX9	NC LPDPX AUX9		
NC SPI DISP BKLT MISO	NC SPI DISP BKLT MISO	NC HDMI CEC AOP TX	NC HDMI CEC AOP TX	NC LPDPX AUX10	NC LPDPX AUX10		
NC SPI DISP BKLT MOSI R	NC SPI DISP BKLT MOSI R	NC HDMI CEC AOP RX	NC HDMI CEC AOP RX	NC LPDP TX4POS	NC LPDP TX4POS		
NC DISP BKLT LSYNC	NC DISP BKLT LSYNC	NC HDMI HPD AOP	NC HDMI HPD AOP	NC LPDP TX4NEG	NC LPDP TX4NEG		
NC BKLT FAULT INT L	NC BKLT FAULT INT L	NC SWD NUB R1 SWDIO	NC SWD NUB R1 SWDIO	NC LPDP TX5POS	NC LPDP TX5POS		
I2C DISP BKLT SCL	I2C DISP BKLT SCL	TGA MISC		NC LPDP TX5NEG	NC LPDP TX5NEG		
I2C DISP BKLT SDA	I2C DISP BKLT SDA	NC SWD TMS3	NC SWD TMS3	TGA ISP SPMI NC			
NC DISPLAY POL	NC DISPLAY POL	NC NAND0 PCIE RESET1 L	NC NAND0 PCIE RESET1 L	NC ISP SPMI0 CLK	NC ISP SPMI0 CLK		
NC DISP FSYNC	NC DISP FSYNC	PMU VDDHI UVWARN L	PMU VDDHI UVWARN L	NC ISP SPMI0 DATA	NC ISP SPMI0 DATA		
NC DISP TOUCH EB	NC DISP TOUCH EB	TGA SPI		NC ISP SPMI1 CLK	NC ISP SPMI1 CLK		
NC DISP TOUCH BSYNC0	NC DISP TOUCH BSYNC0	NC SOC SPI2 SSIN	NC SOC SPI2 SSIN	NC ISP SPMI1 DATA	NC ISP SPMI1 DATA		
NC DISP TOUCH BSYNC1	NC DISP TOUCH BSYNC1			NC SENSOR1 CLK	NC SENSOR1 CLK		
NC DISP SPMI CLK	NC DISP SPMI CLK			NC SENSOR2 CLK	NC SENSOR2 CLK		
NC DISP SPMI DATA	NC DISP SPMI DATA			NC SENSOR3 CLK	NC SENSOR3 CLK		
				NC SPMI2 CLK	NC SPMI2 CLK		
				TGA MTR			
				NC MTR VREF NEG		NC MTR VREF NEG	
				NC MTR VREF POS		NC MTR VREF POS	
				NC MTR VREF ANAP		NC MTR VREF ANAP	
				NC MTR VREF ANAN		NC MTR VREF ANAN	
				TGA AOP I2CM1 NC			
				NC I2C AOP ENET SCL		NC I2C AOP ENET SCL	
				NC I2C AOP ENET SDA		NC I2C AOP ENET SDA	
				TGA PDM NC			
				NC PDM CLK2		NC PDM CLK2	
				NC PDM CLK5		NC PDM CLK5	
				NC PDM CLK6		NC PDM CLK6	
				NC PDM DATA2		NC PDM DATA2	
				TGA SMC GPIO NC & RESOLVE			
				NC SMC GPIO1		NC SMC GPIO1	
				SMC FAN PWM		SMC FAN PWM	
				TGA AOP UART2 NC			
				NC AOP UART2 D2R		NC AOP UART2 D2R	
				NC AOP UART2 R2D		NC AOP UART2 R2D	
				TGA ISP I2C0/1/3 NC			
				NC ISP I2C0 SCL		NC ISP I2C0 SCL	
				NC ISP I2C0 SDA		NC ISP I2C0 SDA	
				NC ISP I2C1 SCL		NC ISP I2C1 SCL	
				NC ISP I2C1 SDA		NC ISP I2C1 SDA	
				NC ISP I2C3 SCL		NC ISP I2C3 SCL	
				NC ISP I2C3 SDA		NC ISP I2C3 SDA	

SYNCH MASTER: ALTERN. 7648. MLC
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SIGNAL ALIASES 1

Apple Inc.

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LATTICE SECDIS FPGA

Table with 2 columns: Signal Name and Alias Name. Includes signals like NC_SEP_IRCAM_DISABLE_IC_L, NC_IRCAM_ENABLE_IN_IC, etc.

ACE2 GPIOs

Table with 2 columns: Signal Name and Alias Name. Includes signals like UPC_SMC_I2C_INT_L, UPC_I2C_INT_L, etc.

TGA LPDPRX RX NC

Table with 2 columns: Signal Name and Alias Name. Includes signals like NC_LPDPRX_RX_P_0, NC_LPDPRX_RX_N_0, etc.

USB LEVEL SHIFTER

Table with 2 columns: Signal Name and Alias Name. Includes signals like TP_EUSB_LS1NEG, TP_EUSB_LS1POS, etc.

AUDIO AMPLIFIER TDM

Table with 2 columns: Signal Name and Alias Name. Includes signals like TDM_1V8_SPKRAMP_L_BCLK, TDM_1V8_SPKRAMP_L_FSYNC, etc.

SPEAKERAMP RESET

Table with 2 columns: Signal Name and Alias Name. Includes signal SPKRAMP_RESET_L.

USBC LDO ENABLES

Table with 2 columns: Signal Name and Alias Name. Includes signals like USBC0_3V3LDO_EN_MUX, USBC1_3V3LDO_EN.

USBC LDO HPD

Table with 2 columns: Signal Name and Alias Name. Includes signals TMU_CLKOUT_1, TMU_CLKOUT_0.

CHARGER

Table with 2 columns: Signal Name and Alias Name. Includes signal NC_CHGR_EN_VR1.

NAND REFERENCE

Table with 2 columns: Signal Name and Alias Name. Includes signals SWD_NAND0_SWCLK, SWD_NAND0_SWDIO, PPOV9_S5E0_VDD_PLL, etc.

SE

Table with 2 columns: Signal Name and Alias Name. Includes signals NC_I2C_SE_SCL, NC_I2C_SE_SDA.

DISPLAY POWER SEQUENCER

Table with 2 columns: Signal Name and Alias Name. Includes signal PMU_SYS_ALIVE.

VITAMIN C

Table with 2 columns: Signal Name and Alias Name. Includes signals NC_DEBUG_JTAG_SOC_TDO, NC_DEBUG_JTAG_SOC_TDI, etc.

USBC CIO

Large table with 2 columns: Signal Name and Alias Name. Includes signals like USBC_ATC0_R2D_P<1>, USBC_ATC0_R2D_N<1>, etc.

ATC0 LANE SWAP

USBC0 LANE SWAP

Metadata box containing: SIGNAL ALIASES 2, Apple Inc. logo, DRAWING NUMBER 051-05399, REVISION 9.0.0, PAGE 406 OF 999, SHEET 106 OF 117.

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_MIX <small>Minimum dielectric based spacing from conductive surfaces to conductive surfaces in and within 10 mils</small>	2-10
A_DIELECTRIC_MIXD_VV_X <small>Minimum dielectric based spacing from conductive surfaces to conductive surfaces in and within 10 mils</small>	PLEASE USE HYBRID TABLE
A_DIELECTRIC_MIXIN_MIXOUT <small>Minimum dielectric based spacing from conductive surfaces to conductive surfaces in and within 10 mils</small>	

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PAGE TITLE			
17.2 RULES			
 Apple Inc.	DRAWING NUMBER	051-05399	SIZE D
	REVISION	9.0.0	
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1

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

Table with columns: CLASS NAME, CONSTRAINT SET, COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*, DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:), Y/N. Rows include I2C, SPI, SPMI, SWD, JTAG, CLOCK_24M, SOC_XTAL_24M_IN, SOC_XTAL_24M_OUT, CLOCK_32K, TDM_LEFT, TDM_RIGHT, TDM_CODEC, SPKR_ICC, UART, RESETS, WDOG, SOCHOT, POWER_BUTTON, FAULT, DMIC_PDM, FAN_CTRL, USB_C, USB_D, USB_E, USB_F, USB_G, USB_H, USB_I, USB_J, USB_K, USB_L, USB_M, USB_N, USB_O, USB_P, USB_Q, USB_R, USB_S, USB_T, USB_U, USB_V, USB_W, USB_X, USB_Y, USB_Z, MIPI, PCIE, PCIE_CLKREQ, PANEL, RCAL, RCAL_CIO, RCAL_MIPI, RCAL_EUSB, BOARD_ID, BOARD_REV, WIRELESS_TIME_SYNC, KBD_PWM.

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

Table with columns: CLASS NAME, CONSTRAINT SET, COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*, DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:), Y/N. Rows include GROUND, ANALOG_GROUND, AUDIO_CONN_HEADPHONE_OUT, AUDIO_CONN_RETURN, AUDIO_CONN_SENSE, SPEAKERAMP_OUTPUT, SENSE_DIFF, RF_ANTENNA, PMU_BUCK_FB, POWER, CAPSLOCK_LED, DBGLED_RETURN.

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Metadata box containing: SYNC_MASTER=7666_MLB, SYNC_DATE=05/13/2019, PAGE TITLE: 17.2 PHYSICAL CSETS, Apple Inc. logo, DRAWING NUMBER: 051-05399, REVISION: 9.0.0, BRANCH: dvt-1, PAGE: 501 OF 999, SHEET: 108 OF 117. Includes a NOTICE OF PROPRIETARY PROPERTY section.

SPACING CONSTRAINT SET, CLASS ASSIGNMENT

SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS		COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*		CLASS
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	S	A_DIELECTRIC_3X	=	Y
SPI	S	A_DIELECTRIC_3X	=	Y
SPMI	S	A_DIELECTRIC_3X	=	Y
SWD	S	A_DIELECTRIC_3X	=	Y
JTAG	S	A_DIELECTRIC_2X	=	Y
CLOCK_24M	S	A_DIELECTRIC_8X	=	Y
SOC_XTAL_24M_IN	S	A_DIELECTRIC_8X	=	Y
SOC_XTAL_24M_OUT	S	A_DIELECTRIC_8X	=	Y
CLOCK_32K	S	A_DIELECTRIC_8X	=	Y
TDM_LEFT	S	A_DIELECTRIC_3X	=	Y
TDM_RIGHT	S	A_DIELECTRIC_3X	=	Y
TDM_CODEC	S	A_DIELECTRIC_3X	=	Y
SPKR_ICC	S	A_DIELECTRIC_3X	=	Y
UART	S	A_DIELECTRIC_2X	=	Y
RESETS	S	A_DIELECTRIC_3X	=	Y
WDOG	S	A_DIELECTRIC_3X	=	Y
SOCHOT	S	A_DIELECTRIC_3X	=	Y
POWER_BUTTON	S	A_DIELECTRIC_3X	=	Y
FAULT	S	A_DIELECTRIC_3X	=	Y
DMIC_PDM	S	A_DIELECTRIC_3X	=	Y
FAN_CTRL	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_BSB0_D2R_1	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_D2R_2	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_R2D_1	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_R2D_2	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_AUX	S	A_DIELECTRIC_7X	=	Y
USBC_SOC_BSB0_LSX	S	A_DIELECTRIC_7X	=	Y
USBC_BSB0_CONN_D2R_1	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_D2R_2	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_R2D_1	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_R2D_2	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_AUXLSX	S	A_DIELECTRIC_7X	=	Y
USBC_UPC0_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
USBC_UPC0_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
USBC_UPC0_CONN_CC	S	A_DIELECTRIC_2X	=	Y
USBC_UPC0_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_RTMR0_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR0_MUX_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_UPC0_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_VITC_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_SOC_BSB1_D2R_1	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_D2R_2	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_R2D_1	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_R2D_2	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_AUX	S	A_DIELECTRIC_7X	=	Y
USBC_SOC_BSB1_LSX	S	A_DIELECTRIC_7X	=	Y
USBC_BSB1_CONN_D2R_1	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_D2R_2	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_R2D_1	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_R2D_2	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_AUXLSX	S	A_DIELECTRIC_7X	=	Y
USBC_UPC1_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
USBC_UPC1_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
USBC_UPC1_CONN_CC	S	A_DIELECTRIC_2X	=	Y
USBC_UPC1_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_RTMR1_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR1_UPC1_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_SOC_RTMR_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR_MUX_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_UPC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_VITC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_LSX	S	A_DIELECTRIC_6X	=	Y
MIPI_FTCAM_CLK	S	A_DIELECTRIC_6X	=	Y
MIPI_FTCAM_DATA	S	A_DIELECTRIC_6X	=	Y
MIPI_DFR_CLK	S	A_DIELECTRIC_6X	=	Y
MIPI_DFR_DATA	S	A_DIELECTRIC_6X	=	Y
PCIE_WIFI_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WIFI_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_WIFI_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_CLKREQ	S	A_DIELECTRIC_2X	=	Y
PANEL_LPDP_DATA	S	A_DIELECTRIC_6X	=	Y
PANEL_LPDP_AUX	S	A_DIELECTRIC_6X	=	Y
RCAL_PCIE	S	A_DIELECTRIC_2X	=	Y
RCAL_CIO	S	A_DIELECTRIC_2X	=	Y
RCAL_MIPI	S	A_DIELECTRIC_2X	=	Y
RCAL_EUSB	S	A_DIELECTRIC_2X	=	Y
BOARD_ID	S	A_DIELECTRIC_2X	=	Y
BOARD_REV	S	A_DIELECTRIC_2X	=	Y
WIRELESS_TIME_SYNC	S	A_DIELECTRIC_2X	=	Y
KBD_PWM	S	A_DIELECTRIC_2X	=	Y
GROUND	S	DEFAULT	=	Y
ANALOG_GROUND	S	DEFAULT	=	Y

CLASS DEFINITIONS		COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*		CLASS
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
AUDIO_CONN_HEADPHONE_OUT	S	A_DIELECTRIC_3X	=	Y
AUDIO_CONN_RETURN	S	A_DIELECTRIC_2X	=	Y
AUDIO_CONN_SENSE	S	A_DIELECTRIC_2X	=	Y
SPEAKERAMP_OUTPUT	S	A_DIELECTRIC_2X	=	Y
SENSE_DIFF	S	A_DIELECTRIC_2X	=	Y
RF_ANTENNA	S	RF_ANTENNA	=	Y
PMU_BUCK_FB	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y
CAPSLCK_LED	S	DEFAULT	=	Y
DBGLED_RETURN	S	DEFAULT	=	Y

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 Apple Inc.	DRAWING NUMBER	051-05399	
	REVISION	9.0.0	
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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	GROUND	DEFAULT
SPI	GROUND	DEFAULT
SPMI	GROUND	DEFAULT
SWD	GROUND	DEFAULT
JTAG	GROUND	DEFAULT
CLOCK_24M	GROUND	DEFAULT
CLOCK_32K	GROUND	DEFAULT
TDM_LEFT	GROUND	DEFAULT
TDM_RIGHT	GROUND	DEFAULT
TDM_CODEC	GROUND	DEFAULT
SPKR_ICC	GROUND	DEFAULT
UART	GROUND	DEFAULT
RESETS	GROUND	DEFAULT
WDOG	GROUND	DEFAULT
SOCHOT	GROUND	DEFAULT
POWER_BUTTON	GROUND	DEFAULT
FAULT	GROUND	DEFAULT
DMIC_PDM	GROUND	DEFAULT
FAN_CTRL	GROUND	DEFAULT
USBC_SOC_BSB0_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_AUX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_LSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_AUXLSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_TOP	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_BOT	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_CC	GROUND	DEFAULT
USBC_UPC0_CONN_SBU	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC0_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_AUX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_LSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_D2R_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_R2D_1	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_R2D_2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_AUXLSX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_TOP	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_BOT	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_CC	GROUND	DEFAULT
USBC_UPC1_CONN_SBU	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_DATA	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_DATA	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_D2R	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_R2D	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_D2R	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_R2D	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_D2R	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_R2D	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_CLK	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_CLKREQ	GROUND	DEFAULT
PANEL_LPDP_DATA	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
PANEL_LPDP_AUX	GROUND	DEFAULT_WITH_7X_LINE2SHAPE
RCAL_PCIE	GROUND	DEFAULT
RCAL_CIO	GROUND	DEFAULT
RCAL_MIPI	GROUND	DEFAULT
BOARD_ID	GROUND	DEFAULT
BOARD_REV	GROUND	DEFAULT
WIRELESS_TIME_SYNC	GROUND	DEFAULT
KBD_PWM	GROUND	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	GROUND	DEFAULT
AUDIO_CONN_RETURN	GROUND	DEFAULT
AUDIO_CONN_SENSE	GROUND	DEFAULT
SPEAKERAMP_OUTPUT	GROUND	DEFAULT
SENSE_DIFF	GROUND	DEFAULT
SOC_XTAL_24M_IN	GROUND	DEFAULT
SOC_XTAL_24M_OUT	GROUND	DEFAULT
POWER	GROUND	DEFAULT

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	POWER	DEFAULT
SPI	POWER	DEFAULT
SPMI	POWER	DEFAULT
SWD	POWER	DEFAULT
JTAG	POWER	DEFAULT
CLOCK_24M	POWER	DEFAULT
CLOCK_32K	POWER	DEFAULT
TDM_LEFT	POWER	DEFAULT
TDM_RIGHT	POWER	DEFAULT
TDM_CODEC	POWER	DEFAULT
SPKR_ICC	POWER	DEFAULT
UART	POWER	DEFAULT
RESETS	POWER	DEFAULT
WDOG	POWER	DEFAULT
SOCHOT	POWER	DEFAULT
POWER_BUTTON	POWER	DEFAULT
FAULT	POWER	DEFAULT
DMIC_PDM	POWER	DEFAULT
FAN_CTRL	POWER	DEFAULT
USBC_SOC_BSB0_D2R_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_D2R_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_R2D_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_R2D_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB0_AUX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB0_LSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_D2R_2	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_R2D_1	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_R2D_2	POWER	A_DIELECTRIC_7X
USBC_BSB0_CONN_AUXLSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_TOP	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_BOT	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC0_CONN_CC	POWER	DEFAULT
USBC_UPC0_CONN_SBU	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC0_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_D2R_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_R2D_1	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_R2D_2	POWER	A_DIELECTRIC_7X
USBC_SOC_BSB1_AUX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_BSB1_LSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_D2R_2	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_R2D_1	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_R2D_2	POWER	A_DIELECTRIC_7X
USBC_BSB1_CONN_AUXLSX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_TOP	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_BOT	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_UPC1_CONN_CC	POWER	DEFAULT
USBC_UPC1_CONN_SBU	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_FTCAM_DATA	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
MIPI_DFR_DATA	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_D2R	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_R2D	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_WIFI_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_D2R	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_R2D	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND0_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_D2R	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_R2D	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_NAND1_CLK	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PCIE_CLKREQ	POWER	DEFAULT
PANEL_LPDP_DATA	POWER	DEFAULT_WITH_7X_LINE2SHAPE
PANEL_LPDP_AUX	POWER	DEFAULT_WITH_7X_LINE2SHAPE
RCAL_PCIE	POWER	DEFAULT
RCAL_CIO	POWER	DEFAULT
RCAL_MIPI	POWER	DEFAULT
BOARD_ID	POWER	DEFAULT
BOARD_REV	POWER	DEFAULT
WIRELESS_TIME_SYNC	POWER	DEFAULT
KBD_PWM	POWER	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	POWER	DEFAULT
AUDIO_CONN_RETURN	POWER	DEFAULT
AUDIO_CONN_SENSE	POWER	DEFAULT
SPEAKERAMP_OUTPUT	POWER	DEFAULT
SENSE_DIFF	POWER	DEFAULT
SOC_XTAL_24M_IN	POWER	DEFAULT
SOC_XTAL_24M_OUT	POWER	DEFAULT
POWER	POWER	DEFAULT

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
USBC_SOC_BSB0_D2R_1	USBC_SOC_BSB0_D2R_2	A_DIELECTRIC_6X
USBC_SOC_BSB0_R2D_1	USBC_SOC_BSB0_R2D_2	A_DIELECTRIC_6X
USBC_BSB0_CONN_D2R_1	USBC_BSB0_CONN_D2R_2	A_DIELECTRIC_6X
USBC_BSB0_CONN_R2D_1	USBC_BSB0_CONN_R2D_2	A_DIELECTRIC_6X
USBC_SOC_BSB1_D2R_1	USBC_SOC_BSB1_D2R_2	A_DIELECTRIC_6X
USBC_SOC_BSB1_R2D_1	USBC_SOC_BSB1_R2D_2	A_DIELECTRIC_6X
USBC_BSB1_CONN_D2R_1	USBC_BSB1_CONN_D2R_2	A_DIELECTRIC_6X
USBC_BSB1_CONN_R2D_1	USBC_BSB1_CONN_R2D_2	A_DIELECTRIC_6X
PANEL_LPDP_DATA	PANEL_LPDP_DATA	A_DIELECTRIC_5X
SOC_XTAL_24M_IN	SOC_XTAL_24M_OUT	A_DIELECTRIC_2X

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	REVISION	9.0.0		
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POR BOM VARIANT TABLES

DRAM VENDOR, FAB SITE, AND LEAKAGE ARE ALTERNATES IN THE SAME 639

BOM NUMBER	BOM NAME	BOM OPTIONS
639-12952	MLB1, 8GB, TS-256GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_256GB_TS
639-12953	MLB1, 16GB, TS-256GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_256GB_TS
639-12954	MLB1, 8GB, HY-256GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_256GB_HY
639-12955	MLB1, 16GB, HY-256GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_256GB_HY
639-12956	MLB1, 8GB, TS-512GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_512GB_TS
639-12957	MLB1, 16GB, TS-512GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_512GB_TS
639-12958	MLB1, 8GB, WD-512GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_512GB_WD
639-12959	MLB1, 16GB, WD-512GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_512GB_WD
639-12960	MLB1, 8GB, HY-512GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_512GB_HY
639-12961	MLB1, 16GB, HY-512GB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_512GB_HY
639-12962	MLB1, 8GB, TS-1TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_1TB_TS
639-12963	MLB1, 16GB, TS-1TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_1TB_TS
639-12964	MLB1, 8GB, HY-1TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_1TB_HY
639-12965	MLB1, 16GB, HY-1TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_1TB_HY
639-12966	MLB1, 8GB, HY-2TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_2TB_HY
639-12967	MLB1, 16GB, HY-2TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_2TB_HY
639-12968	MLB1, 8GB, TS-2TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_08GB, X1799_NAND_2TB_TS
639-12969	MLB1, 16GB, TS-2TB, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: B0_16GB, X1799_NAND_2TB_TS

DEBUG BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS
939-09328	MLB, INT-CPU, INT-SSD, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: INTERPOSER, X1799_NAND_INTERPOSER
939-09329	MLB, NO-CPU, INT-SSD, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: OFF, X1799_NAND_INTERPOSER
939-09330	MLB, INT-CPU, NO-SSD, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: INTERPOSER, X1799_NO_NAND
939-09331	MLB, NO-CPU, NO-SSD, X1799	ALT_CMN, ALTERNATE: PART, X1799_CMN_BOM, CPU: OFF, X1799_NO_NAND
939-09510	MLB, RF-TUNING, X1799	SCH, PCB, RF_CONN

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BOM VARIANT TABLES			
 Apple Inc.	DRAWING NUMBER	051-05399	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-08813	1	PCBA,KANHA,X1711	U0600	CRITICAL	CPU:INTERPOSER
998-22385	1	SOC,TGA B0+89,1Y,8C,LP,DEV,CX,M,S,M2502	U0600	CRITICAL	CPU:B0_08GB
998-22389	1	SOC,TGA B0+16G,1X,8C,LP,DEV,DX,M,S,M2502	U0600	CRITICAL	CPU:B0_16GB

NOTE: PER <RDAR://55481499>, DRAM VENDOR, FAB SITE, AND LEAKAGE ARE NOT CUSTOMER FACING, SO DON'T NEED SEPARATE BOM'S
639 BOM'S WILL SET MICRON SCR LP AS THE PRIMARY, BUT ALL OTHER COMBINATIONS ARE SET AS ALTERNATES IN THE SAME 639 BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-13316	2	IC,BURNSIDE BRIDGE,USB/TB RETIMER,BGA105	UF000,UF100	CRITICAL	ATCRTMR:DEV
338S00561	2	IC,TBT,BBR,SLMN7,PRQ,A1,BGA105	UF000,UF100	CRITICAL	ATCRTMR:A1_PRQ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S02158	2	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500	CRITICAL	USBCPC:LAPTOP_B2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-19902	1	SUBASSY (T&R) PCBA,AMR INTERPOSER,X1795	JR200	CRITICAL	AMR:X1795
677-23569	1	SUBASSY (T&R) PCBA,AMR INTERPOSER,X1799	JR200	CRITICAL	AMR:X1799

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	TBT_ROM:BLANK_WINBOND
335S00232	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	TBT_ROM:BLANK_MACRONIX
341S01581	1	ROM,TBT/ACE (VXXXX) PRE-PROTO-1,X1740	UF260	CRITICAL	TBT_ROM:PRE_P1
341S01601	1	ROM,TBT/ACE (VXXXX) NEW, PRE-PROTO1,X1799	UF260	CRITICAL	TBT_ROM:PRE_P1_V2
341S01618	1	ROM,TBT/ACE (VXXXX), PROTO1,X1799	UF260	CRITICAL	TBT_ROM:P1
341S01672	1	ROM,TBT/ACE (VXXXX), PROTO2,X1799	UF260	CRITICAL	TBT_ROM:P2
341S01726	1	ROM,TBT/ACE (VXXXX) EVT,X1799	UF260	CRITICAL	TBT_ROM:EVT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20066	1	IC,PMU,SPMU,A0,OTP-JPC,WLCSF196	U7700	CRITICAL	SPMU_IC:A0_JPC
998-22526	1	IC,PMU,SPMU,A1,OTP-JPE,WLCSF196	U7700	CRITICAL	SPMU_IC:A1_JPE
998-22882	1	IC,PMU,SPMU,A1,OTP-JPF,WLCSF196	U7700	CRITICAL	SPMU_IC:A1_JPF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20064	1	IC,PMU,MPMU,A0,OTP-JPC,WLCSF440	U8100	CRITICAL	MPMU_IC:A0_DEV
998-22339	1	IC,PMU,MPMU,B0,OTP-JPE,WLCSF440	U8100	CRITICAL	MPMU_IC:B0_JPE
998-22614	1	IC,PMU,MPMU,B0,OTP-JPF,WLCSF440	U8100	CRITICAL	MPMU_IC:B0_JPF
998-22880	1	IC,PMU,MPMU,B0,OTP-JPG,WLCSF440	U8100	CRITICAL	MPMU_IC:B0_JPG
998-23159	1	IC,PMU,MPMU,B0,OTP-JPH,WLCSF440	U8100	CRITICAL	MPMU_IC:B0_JPH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20641	2	IC,FRT,CD2E224,B0,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_OTP6
338S00628	2	IC,PARROT,CD2E226B,B0,LSB1,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_LSB1_OTP6

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-19915	1	IC,SN210V,CERES,DEV KEY,B1,SW=V7,WLCSF81	U5000	CRITICAL	SE:DEV_SW_V7
998-21255	1	IC,SN210V,B1,CERES,DEV,SW=H3,WLCSF81	U5000	CRITICAL	SE:DEV_SW_H3
338S00630	1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSF81	U5000	CRITICAL	SE:PROD_SW_MU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,SSE MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND0:SSE_STUDY
335S00437	1	NAND,3DV5,128GB,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND0:128GB_2DP_HY
335S00462	1	NAND,3DV4,128GBT,XXX,SSE,256G,S,SLGA110	UN000	CRITICAL	NAND0:128GB_4DP_TS
335S00446	1	NAND,3DV5,128GB,SSE,256G,S,SLGA110	UN000	CRITICAL	NAND0:128GB_4DP_SS
335S00480	1	NAND,3DV4,160GBT,XXX,SSE,256G,K,SLGA110	UN000	CRITICAL	NAND0:160GB_5DP_TS
335S00438	1	NAND,3DV5,256GBT,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND0:256GB_4DP_HY
335S00464	1	NAND,3DV4,256GBT,XXX,SSE,256G,T,SLGA110	UN000	CRITICAL	NAND0:256GB_8DP_TS
335S00472	1	NAND,3DV4,256GBT,XXX,SSE,256G,SD,SLGA110	UN000	CRITICAL	NAND0:256GB_8DP_WD
335S00481	1	NAND,3DV4,288GBT,XXX,SSE,256G,K,SLGA110	UN000	CRITICAL	NAND0:288GB_9DP_TS
335S00490	1	NAND,3DV4,288GBT,XXX,SSE,256G,SD,SLGA110	UN000	CRITICAL	NAND0:288GB_9DP_WD
335S00482	1	NAND,3DV5,320GBT,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND0:320GB_5DP_HY
335S00439	1	NAND,3DV5,512GB,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND0:512GB_8DP_HY
335S00466	1	NAND,3DV4,512GBT,XXX,SSE,256G,T,SLGA110	UN000	CRITICAL	NAND0:512GB_16DP_TS
335S00483	1	NAND,3DV5,576GBT,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND0:576GB_9DP_HY
335S00468	1	NAND,3DV4,1TBT,XXX,SSE,512G,T,SLGA110	UN000	CRITICAL	NAND0:1TB_16DP_TS
335S00458	1	NAND,3DV5,1024GBT,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND0:1TB_16DP_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND0:INTERPOSER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,SSE MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND1:SSE_STUDY
335S00437	1	NAND,3DV5,128GB,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND1:128GB_2DP_HY
335S00462	1	NAND,3DV4,128GBT,XXX,SSE,256G,S,SLGA110	UN100	CRITICAL	NAND1:128GB_4DP_TS
335S00446	1	NAND,3DV5,128GB,SSE,256G,S,SLGA110	UN100	CRITICAL	NAND1:128GB_4DP_SS
335S00480	1	NAND,3DV4,160GBT,XXX,SSE,256G,K,SLGA110	UN100	CRITICAL	NAND1:160GB_5DP_TS
335S00438	1	NAND,3DV5,256GBT,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND1:256GB_4DP_HY
335S00464	1	NAND,3DV4,256GBT,XXX,SSE,256G,T,SLGA110	UN100	CRITICAL	NAND1:256GB_8DP_TS
335S00472	1	NAND,3DV4,256GBT,XXX,SSE,256G,SD,SLGA110	UN100	CRITICAL	NAND1:256GB_8DP_WD
335S00481	1	NAND,3DV4,288GBT,XXX,SSE,256G,K,SLGA110	UN100	CRITICAL	NAND1:288GB_9DP_TS
335S00490	1	NAND,3DV4,288GBT,XXX,SSE,256G,SD,SLGA110	UN100	CRITICAL	NAND1:288GB_9DP_WD
335S00482	1	NAND,3DV5,320GBT,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND1:320GB_5DP_HY
335S00439	1	NAND,3DV5,512GB,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND1:512GB_8DP_HY
335S00466	1	NAND,3DV4,512GBT,XXX,SSE,256G,T,SLGA110	UN100	CRITICAL	NAND1:512GB_16DP_TS
335S00483	1	NAND,3DV5,576GBT,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND1:576GB_9DP_HY
335S00468	1	NAND,3DV4,1TBT,XXX,SSE,512G,T,SLGA110	UN100	CRITICAL	NAND1:1TB_16DP_TS
335S00458	1	NAND,3DV5,1024GBT,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND1:1TB_16DP_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND1:INTERPOSER

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COMMON BOM GROUPS

BOM GROUP	BOM OPTIONS
X1799_COMMON_PARTS	SCH,PCB,ALT_CMN,COMMON,ALTERNATE:INSTANCE,X1799_GROUP1,X1799_GROUP2,X1799_GROUP3,X1799_GROUP4,X1799_GROUP5
X1799_GROUP1	ATCRIMR:A1_PRQ,USBCPC:LAPTOP_B2,EUSB_LS:B0_LSB1_OTP6,AMR:X1795,TBT_ROM:EVT,P3V8AON_IC:A1_R0B2,VITAMIN-C:NO
X1799_GROUP2	BLC_BEN_IC:V7,BLC_KBD_BOOST_USED:YES,BLC_LEDS_PER_STRING:16,BLC_5V_SERIES:10_OHM,BLC_5V_CAP:4F7_UF
X1799_GROUP3	BOARD_REV3,BOOT_CONFIG2,BOARDID2,SE:PROD_SW_MU,PBUS_3S,RF_CONN,SSD_2L,NAND_RESET:SOC
X1799_GROUP4	SPMU_IC:A1_JPF,MPMU_IC:B0_JPH,UFC_ATCRIMR_INT,UFC_EUSBLS_INT,SLED:YES,FENCE_USBC_C770,FENCE_COMBO,FENCE_SPMU_C770
X1799_GROUPS5	P1V2_PREREG:BUCK14,SECDIS_EXT_CLK,KBD_NEW,DISPLAY:P1,IPD_PMU_GPIO:EVT,P3V8AON_LPM,DMIC_CLK_330HM,PMU_IREF:INT

DEV BOM GROUPS

BOM GROUP	BOM OPTIONS
X1799_DEV_PARTS	ALT_CMN,ALTERNATE:INSTANCE,X1799_DEV_PARTS1,X1799_DEV_PARTS2
X1799_DEV_PARTS1	DBG_FAN,WLBT_DBG,USBC_DBG,DEBUG_BUTTON,SYS_DET_BTN,DBG_LED
X1799_DEV_PARTS2	SNSRES_DEV,CHGR_DBG,JTAG_SECDIS_CONN,SENSOR_IMU

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
X1799_NAND_256GB_TS	NAND0:160GB_5DP_TS,NAND1:128GB_4DP_TS
X1799_NAND_256GB_HY	NAND0:128GB_2DP_HY,NAND1:128GB_2DP_HY
X1799_NAND_512GB_TS	NAND0:288GB_9DP_TS,NAND1:256GB_8DP_TS
X1799_NAND_512GB_WD	NAND0:288GB_9DP_WD,NAND1:256GB_8DP_WD
X1799_NAND_512GB_HY	NAND0:320GB_5DP_HY,NAND1:256GB_4DP_HY
X1799_NAND_1TB_TS	NAND0:512GB_16DP_TS,NAND1:512GB_16DP_TS
X1799_NAND_1TB_HY	NAND0:576GB_9DP_HY,NAND1:512GB_8DP_HY
X1799_NAND_2TB_TS	NAND0:1TB_16DP_TS,NAND1:1TB_16DP_TS
X1799_NAND_2TB_HY	NAND0:1TB_16DP_HY,NAND1:1TB_16DP_HY
X1799_NAND_INTERPOSER	NAND0:INTERPOSER,NAND1:INTERPOSER
X1799_NO_NAND	NAND0:OFF,NAND1:OFF

SYSTEM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-05399	1	SCHEM,COFFEE,X1799	SCH	CRITICAL	SCH
820-02020	1	PCBF,MLB,X1799	PCB	CRITICAL	PCB
685-00341	1	COMMON PARTS,MLB,X1799	COMMON_PARTS	CRITICAL	X1799_CMN_BOM
985-01178	1	DEV PARTS,MLB,X1799	DEV_PARTS	CRITICAL	X1799_DEV_BOM

COMMON PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00341	COMMON PARTS,MLB,X1799	X1799_COMMON_PARTS

DEV PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
985-01178	DEV PARTS,MLB,X1799	X1799_DEV_PARTS

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SYSTEM EE

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Rows include parts like 376S1080, 107S0276, 311S00176, etc.

SYSTEM EE

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Rows include parts like 138S1068, 311S00269, 376S00292, etc.

WIFI MODULE

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Row includes part 339S00758.

BLC

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Rows include parts like 138S0738, 138S0846, 376S1053, etc.

SOC 8G

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Rows include parts like 998-22386, 998-22387, 998-22388, etc.

SOC 16G

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Rows include parts like 998-22390, 998-22391, 998-22392, etc.

AMR

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Row includes part 677-23569.

DCDC

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Rows include parts like 138S0863, 152S00398, 152S00963, etc.

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SYSTEM EE - EXCLUDE SOC ROM FOR 2 BIT LEVEL SHIFTER

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
311S00254	311S00245	UE430,UT820,UT830	<RDAR://58875674>	ALT_CMN

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PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A,SPKRAMP_B
SPKRAMP_D,SPKRAMP_E
SPKRAMP_LVL_4B_QFN
SPKRAMP_LVL_1B_SON

REF_SPKRAMP_TAS5770
 J293 HAS 4 AMPS, 2 LEFT AND 2 RIGHT.
 LEFT ARE A, B. RIGHT ARE D, E.
 USE SAME LEVEL SHIFTERS AS TRACKPAD SPI
 USE 1.2V BUFFER WITH 1.8V CAPABLE INPUT AS 1.8 TO 1.2 LEVEL SHIFTER

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_60W
CHGR_TP_TOP,CHGR_TP_BOT,CHGR_TP

REF_CHARGER_SUONA
 J293'S CHARGER IS B379 WHICH IS 61W, SO WE USE
 60-100W OPTION PER REF CHARGER SUONA CONFIG TABLE
 ENABLE ALL CHARGER TEST POINTS

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPCO
USBC_DEBUG_UPCO
USBC_LAPTOP
USBC01_VR5V_LOCAL_NO
PKGS:SMALL_PITCH

REF_USBC_ACE2
 SET SPI UPC TO BE 0, BACK LEFT
 SET DEBUG UPC TO BE 0, BACK LEFT
 ENABLE PORTS FOR CHARGING
 LEAVE ACE2 5V ENABLE GPIOs SEPARATE, AS 5V DEDICATED LOCAL VR NOT USED
 ENABLE SMALL PITCH PARTS ON USBC PAGES (OTHER PROJECTS USING BIGGER PITCH OPTIONS)

PACK_OPTIONS TO INCLUDE IN NETLIST
FTCAM
DFR
80UM_STEN
SMALL_NOR

REF_SOC_H13G
 J293 HAS A FTCAM, SO TURN ON FTCAM MIPI REXT RESISTOR
 J293 HAS A DFR, SO TURN ON DFR MIPI REXT RESISTOR
 J293 WILL USE 80 UM TOP SIDE STENCIL FOR SOC BYPASS CAPS
 SMALL NOR IS 4X3 SINGLE SOURCE PACKAGE, LARGE NOR IS 4X4 PACKAGE WITH MULTIPLE ALTERNATES

PACK_OPTIONS TO INCLUDE IN NETLIST
JTAG_SECDIS:YES
PROTO_PULLDOWN_SECDIS
PROD_SECDIS
JTAG_SECDIS_CONN

REF_SECDIS_SAK
 KEEP THE JTAG CONNECTOR AND DEBUG PULLS
 PULL DOWN SEP OUTPUTS WHEN SYSTEM IS IN S2 OR BELOW
 ALL PRODUCTION SYSTEMS CALL OUT PROD_SECDIS
 J293 WILL HAVE PADS FOR THE JTAG CONNECTOR

PACK_OPTIONS TO INCLUDE IN NETLIST
AMR_INTERPOSER_LEFT
NO_AMR_INTERPOSER_RIGHT

REF_SECDIS_AMR
 ON J293, THE LEFT AMR IS ON THE MLB, SO CALL OUT AMR_INTERPOSER_LEFT
 1M PULL DOWNS ON RIGHT SIDE ENABLED WITH NO_AMR_INTERPOSER_RIGHT, TO ENSURE
 NET IS LOW WHEN NO FLEX IS INSTALLED FOR THE RIGHT SIDE

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_DBG_CONN

REF_WIRELESS_RASPUTIN
 3X_ANTENNA PACK OPTION IS FOR PROGRAMS WITH DEDICATED BT ANTENNA, WHICH J293 DOESN'T HAVE
 J293 USES SUNWAY CONNECTOR <RDAR://63744679>
 J293 USES THE DEBUG WIFI CONNECTOR, SO WLBT_DBG_CONN IS CALLED OUT

PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-D2

REF_VR_3V3_TPS62135
 SETTING D2 CAP SIZE

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS-D2

REF_VR_5V_LT8642S
 SETTING D2 CAP SIZE

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-D2
3V8_AON_I2C-POR
3V8_EXT_DIODE

REF_VR_ICEMAN
 SETTING D2 CAP SIZE
 SHORT I2C TO GND FOR POR <RDAR://64007819>
 ENABLE EXTERNAL CHARGE PUMP DIODES

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CHECKPLUS WAIVES

88 04  I2C_KBD_SDA
CKPLUS_WAIVE=I2C_PULLUP

88 04  I2C_KBD_SCL
CKPLUS_WAIVE=I2C_PULLUP

25  GND
CKPLUS_WAIVE=I2C_PULLUP

25  GND
CKPLUS_WAIVE=I2C_PULLUP

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