<Variant Name>

Title

PCI-E RV370 128M TSOP VO-SV/DI

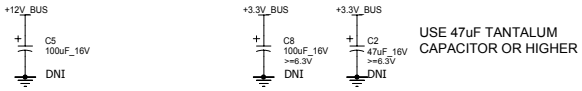
Schematic No.

105-A260xx-00C

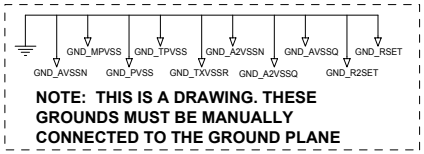
REVISION HISTORY

Sch Rev		Date	REVISION DESCRIPTION
0	00A	2003-09-10	PRELIMINARY BASED ON 105-A181xx-00A and 105-A200xx-00 - Use 402 R and C footprints as preferred - (pg1) Add 0R bypass for PERST#, and use XOR spared gate for buffer - (pg1) Keep only 1 100uF decoupling for +12V_BUS - (pg1) Connect B3 of edge connector directly to +12V_BUS - (pg2) Remove oscillator and change crystal to surface mount - (pg2) Hard pull-down on TEST_Y/MCLK - (pg2) Remove thermal interrupt, no provision for speed controlled fan - (pg2) Remove redundant TPs - (pg2) Pull-up on DVPCNTL_[3:0], remove RageTheater capture ports (VID/DVO[7:0]) - (pg2) DVOMode pull-up to 1.8V, set to 12-bit DVO (1.8V DVO I/O signalling) - (pg3) Memory interface based on A198, remove Channel B - (pg4) Remove power-up diodes - (pg5, 6, 7) Redesigned power regulators - (pg8, 9) Channel A only Series-Terminated TSOP interface (based on A200) - (pg11, 12, 13) Front-end based on Low-Profile VGA/DVI + VO design (based on A200)
		2003-09-22	- (pg5) Add RC snubber circuit on switching regulator - (pg7) Add R124 for power dissipation
		2003-10-16	- (pg14) Add MT2, second mounting hole - (pg6 and 7) Remove R817, option for sharing REG8 and REG9, due to layout concerns - (pg4) Add C979..C985 On request of EMI team. These are for decoupling ajacent planes. - (pg6) Make RP2 dual footprint with 0402 Caps C986..C989. Created a similar circuit using RP195 and C990..C993. The RP can be used to short +MVDDQ and +MVDDC, and the caps can be used to decouple the planes. - (pg6) Add C973..C978 Decoupling caps. These are placed accross +MVDDQ/+MVDDC plane splits - (pg11) Remove R994..R996 stitching GND to Chassis GND.
1	00B	2003/11/14	- (Layout) Change to 6-layer PCB - (Layout) Change PCIE test points - (pg1) Change PCIE test points, add 3.3V_BUS polymer cap, add R1244 - (pg2) Add R23 for DVO pull-down - (pg4) Add B15 for +3.3V_BUS VDDR4 alternate, change PCIE regulators filter from 100nF to 1uF - (pg5) Add stand-alone +PCIE_VDDR, +PCIE_PVDD12 and +PCIE_PVDD18 regulators, improve power sequence circuit - (pg5) Add R315 and R316 to select +12V_BUS or +5V for boot circuit, change R368 footprint to 603 - (pg6) Add C314 and C315 for MVDDC and MVDDQ, 1.8V from PCIE_PVDD18 - (pg7) Remove R124, add polymer cap for PCIE_PVDD18, add +PCIE_VDDR and +PCIE_PVDD12 tied option and single package FET for +PCIE_VDDR - (pg14) Add fan connector
2	00C	2004/03/05	- (pg02, 10) Fix pull-up +VDD_DVO to +VDDR4 - (Layout) TVO filters move close to connector - (pg04) Remove CP2, 3, 4, 5, 6 and 8 for dual footprint manufacturing issues (Capacitor packs sharing with 402 footprints) - (Layout) Components using the same foot print. (remove MC2) - (pg06) Remove C986, C987, C988, C989, C990, C991, C992 and C993 - (pg06) Add C800 for options - (pg11) +5V supply with current limiting for VESA DDC spec, remove F1, B21 - (pg05) Remove dual-packaged MOSFET - (Layout/EMI) C507, C508, C509, R513, R514, R515 (added), L60, L61 and L62 connect to digital Gnd instead of chassis Gnd.

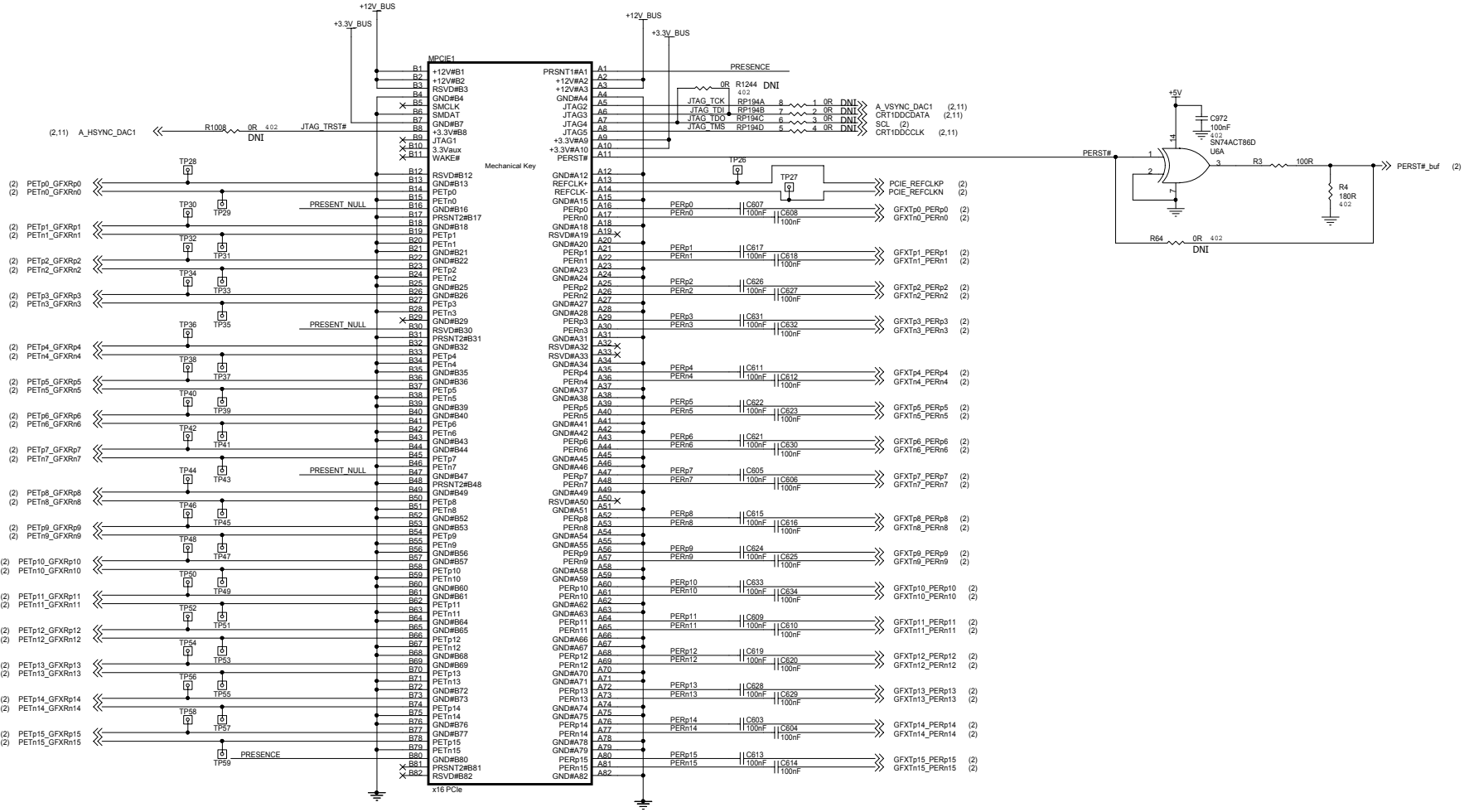
PCI-EXPRESS EDGE CONNECTOR

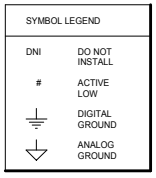


USE 47uF TANTALUM CAPACITOR OR HIGHER



NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE





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Title	PCI-E RV370 128M TSOP VO-SV/DI		
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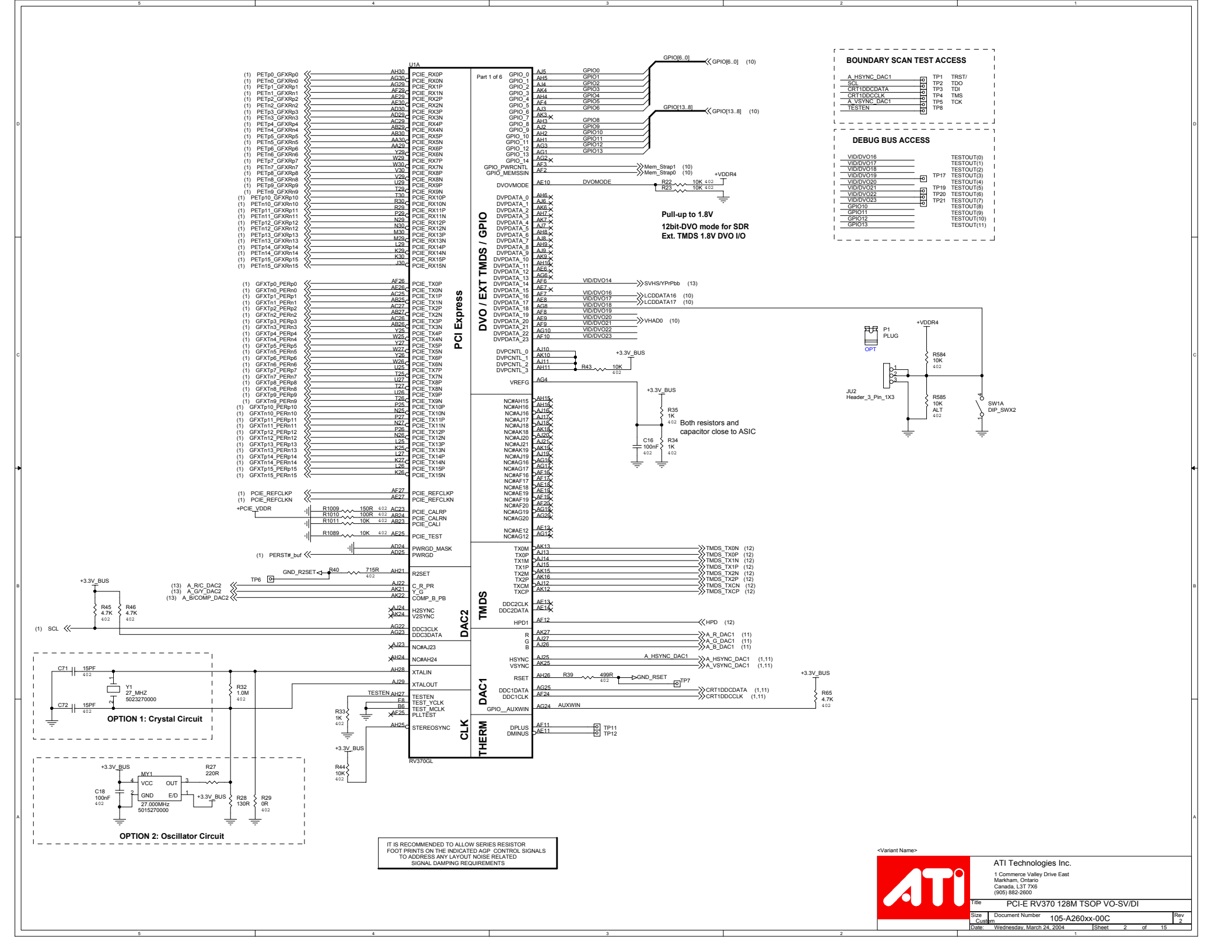
U1A
Part 1 of 6
PCI Express
DVO / EXT TMDS / GPIO
TMDS
DAC2
DAC1
CLK
THERM
RV370GL
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PWRGD_MASK
PWRGD
R2SET
C_R_PR
Y_G
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
NC#AJ23
NC#AH24
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
DPLUS
DMINUS
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_PWRCNTL
GPIO_MEMSSIN
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
GPIO__AUXWIN
GPIO[6..0]
GPIO[13..8]
Mem_Strap1
Mem_Strap0
VID/DVO14
VID/DVO16
VID/DVO17
VID/DVO18
VID/DVO19
VID/DVO20
VID/DVO21
VID/DVO22
VID/DVO23
SVHS/YPrPbb
LCDDATA16
LCDDATA17
VHAD0
TMDS_TX0N
TMDS_TX0P
TMDS_TX1N
TMDS_TX1P
TMDS_TX2N
TMDS_TX2P
TMDS_TXCN
TMDS_TXCP
HPD
A_R_DAC1
A_G_DAC1
A_B_DAC1
A_HSYNC_DAC1
A_VSYNC_DAC1
CRT1DDCDATA
CRT1DDCCLK
AUXWIN
Pull-up to 1.8V
12bit-DVO mode for SDR
Ext. TMDS 1.8V DVO I/O
Both resistors and capacitor close to ASIC
BOUNDARY SCAN TEST ACCESS
DEBUG BUS ACCESS
OPTION 1: Crystal Circuit
OPTION 2: Oscillator Circuit
IT IS RECOMMENDED TO ALLOW SERIES RESISTOR FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS TO ADDRESS ANY LAYOUT NOISE RELATED SIGNAL DAMPING REQUIREMENTS
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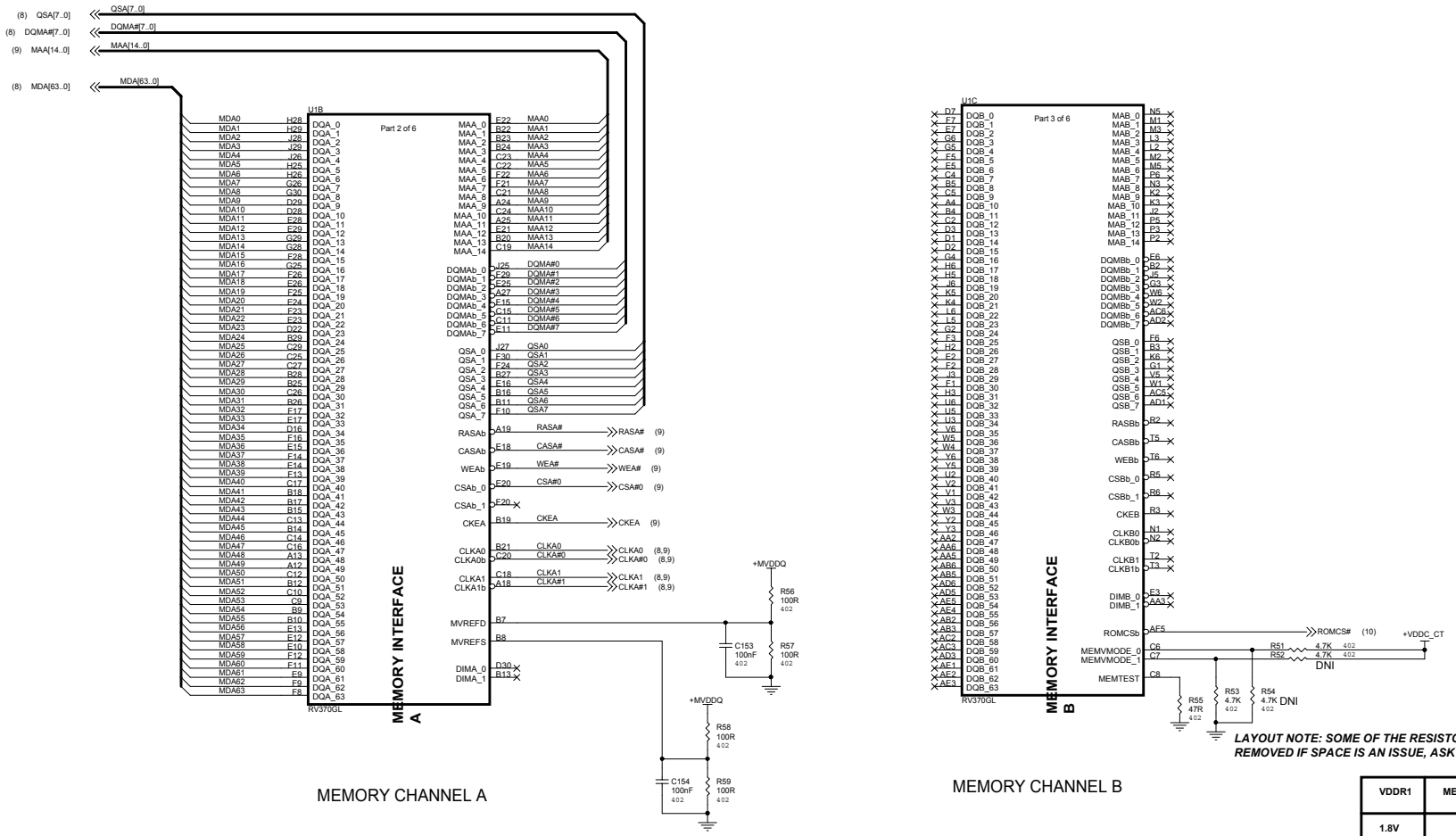
PCI-E RV370 128M TSOP VO-SV/DI
105-A260xx-00C
Wednesday, March 24, 2004



MEMORY CHANNEL A

PLACE C351/152 VERY CLOSE TO ASIC

R56/57/58/59 CLOSE TO ASIC AS WELL

MEMORY CHANNEL B

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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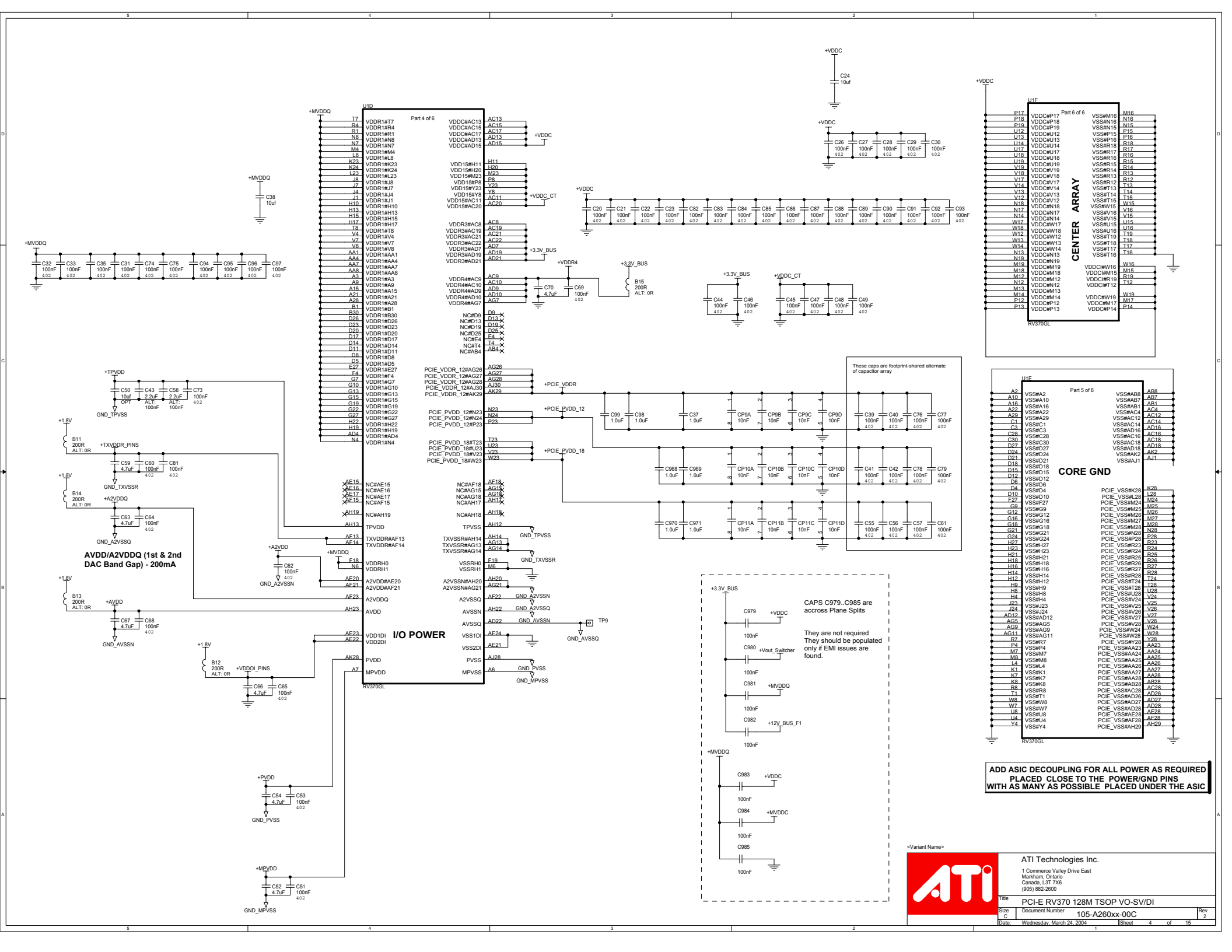
U1D
Part 4 of 6
RV370GL
I/O POWER
AVDD/A2VDDQ (1st & 2nd DAC Band Gap) - 200mA
U1F
Part 6 of 6
CENTER ARRAY
RV370GL
U1E
Part 5 of 6
CORE GND
RV370GL
These caps are footprint-shared alternate of capacitor array
CAPS C979..C985 are accross Plane Splits
They are not required They should be populated only if EMI issues are found.
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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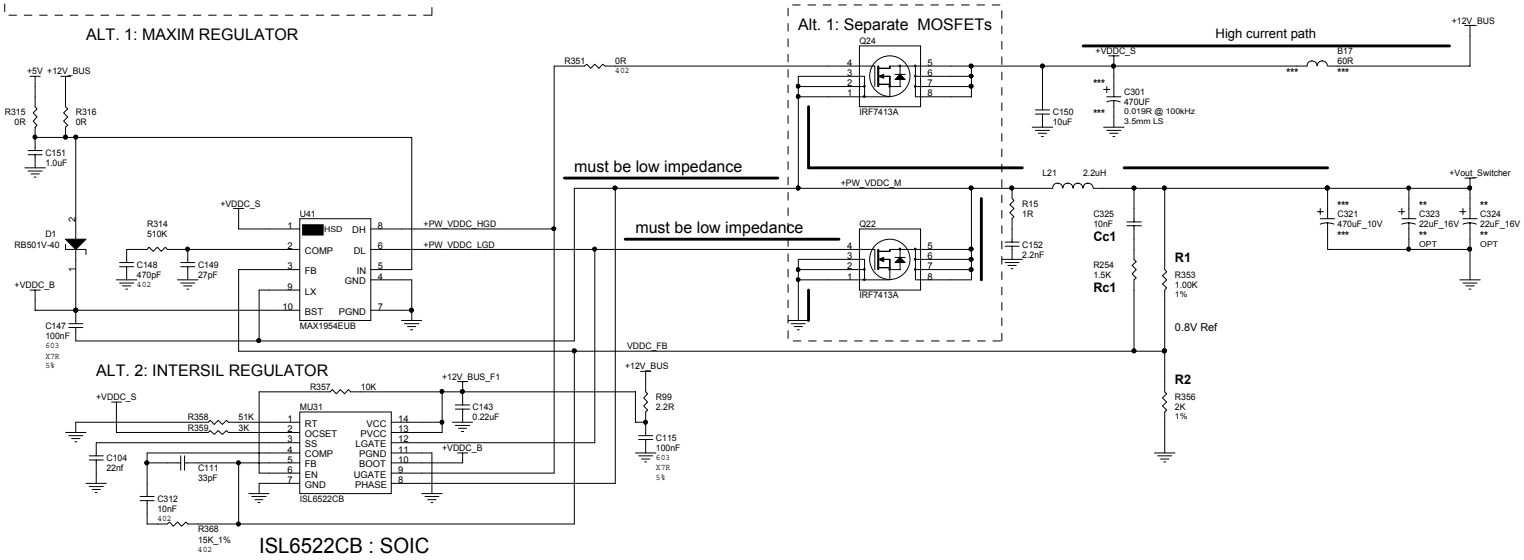
Regulator for VDDC (ASIC Core)
Vout = 1.2V ~ 1.3V

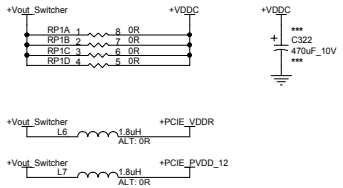
*** Indicate number of power via required for the connection

Part	NOTES
MAX1954	Do not install Cc1, Rc1
ISL6522	Install Cc1, Rc1

Part	Vout	R1	R2
MAX1954 ISL6522	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240200100
0.8V Ref	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N 3240162100

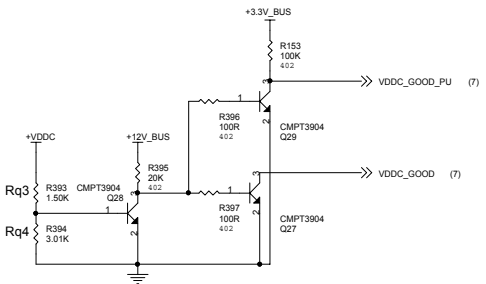


ISL6522CB : SOIC



Circuit to hold PCI-E voltage low and wait for +VDDC for proper power sequence

+VDDC	Rq3	Rq4
+1.3V	1.5K	2.4K
+1.2V	1.5K	3K



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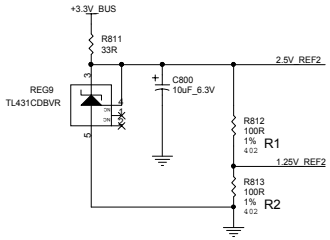
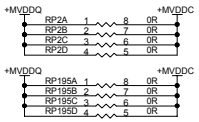
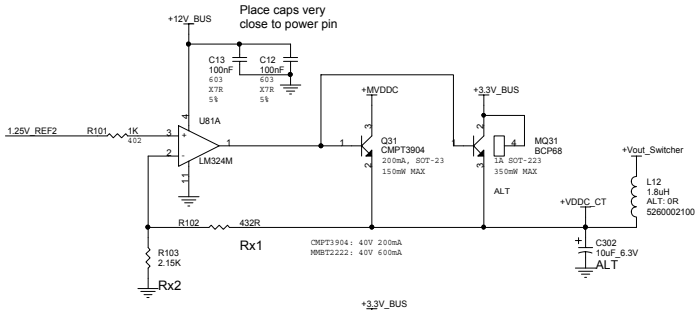


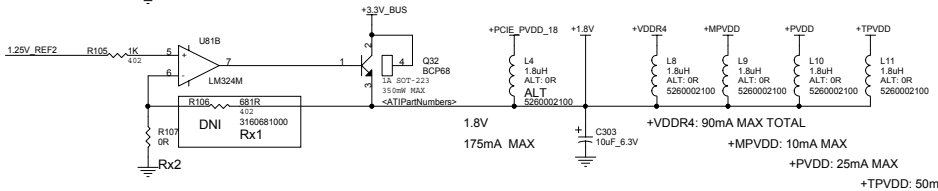
Voltage Req.	R1	R2
0.8V	150R P/N 3240150000	71.5R P/N 324075R500
1.25V	75R P/N 3240075000 603 P/N 316075R000 402	75R P/N 3240075000 603 P/N 316075R000 402
1.5V	49.9R P/N 3240049900	75R P/N 3240075000 603 P/N 316075R000 402
1.8V	54.9R P/N 3240054900	140R P/N 3240140000
1.84V	49.9R P/N 3240049900	140R P/N 3240140000

Voltage Req.	Rx1 for 1.25V Ref	Rx2 for 1.25V Ref
1.5	432R P/N 3240432000	2.15K P/N 3240215100
1.6V	432R P/N 3240432000	1.5K P/N 3240150100
1.7V	432R P/N 3240432000	1.21K P/N 3240121100
1.8175V	681R P/N 3240681000 603 P/N 3160681000 402	1.5K P/N 3240015200

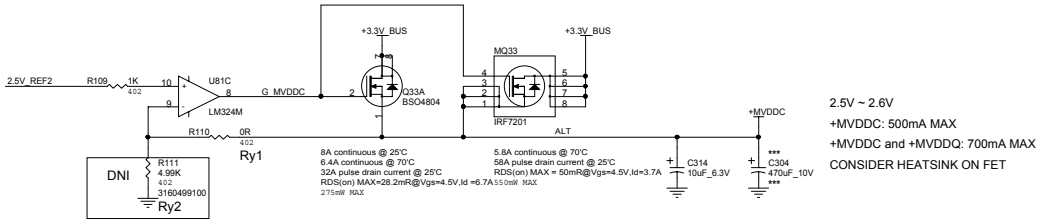
Voltage Req.	Ry1 for 2.5V Ref	Ry2 for 2.5V Ref
3.3V	1.07K P/N 3240107100	3.32K P/N 3240332100
2.7V	301R (402, 1%) P/N 3160301000	3.32K P/N 3240332100
2.65V	301R (402, 1%) P/N 3160301000	4.99K (402, 1%) P/N 3160499100
2.5V	0R P/N 3230000000 603 P/N 3150000000 402	DNI

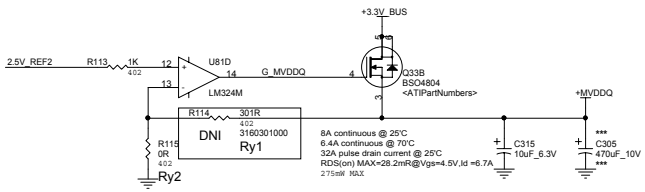


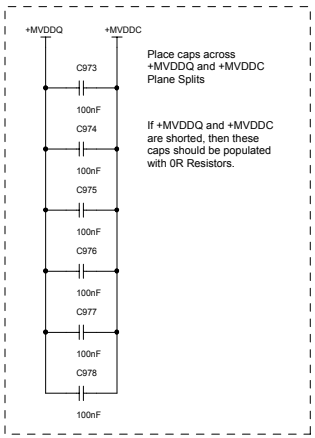




Rails derived from +VDDR4
+AVDD: 10mA MAX
+A2VDDQ: 20mA MAX
+VDDOI_PINS: 20mA MAX
+TXVDDR_PINS: 20mA MAX



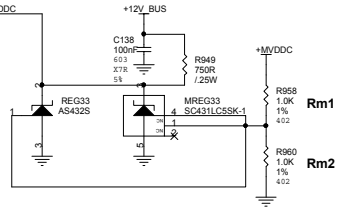




	Rt1	Rt2
1.52V	432R 3240432000 3160432000	2.15K 3160215100
1.61V	432R 3240432000	1.5K 3230015200 1.5K 3160150100
1.69V	432R 3240432000	1.21K 3240121100
1.718V	562R 3240562000	1.5K 3230015200 1.5K 3160150100
1.75V	604R 3160604000	1.5K 3230015200 1.5K 3160150100
1.8V	604R 3160604000	1.37K 3160137100

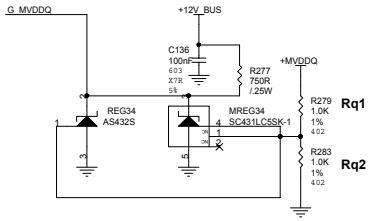
Alt. regulator for +MVDDC
Vout = 2.5V ~ 2.6V
Iout = 500mA MAX

Voltage Req.	Rm1	Rm2
3.34V [-0.04V/+0.04V]	4.32K	2.55K
3.45V [-0.04V/+0.04V]	4.32K	2.43K
2.5V [-0.03V/+0.03V]	1K 3240100100	1K 3240100100

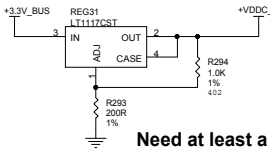


Alt regulator for +MVDDQ
Vout = 2.5V ~ 2.6V
Iout = 200mA MAX

Voltage Req.	Rq1	Rq2
1.8V [-0.09V/+0.18V]	681R 3240681000	1.5K 3230015200
2.5V	1K 3240100100	1K 3240100100
2.6V	4.75K 3240475100	4.32K 3240432100

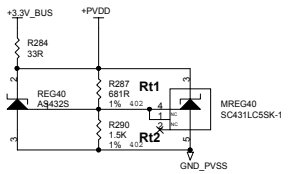


Alt regulator for +VDDC_CT
Vout = 1.5V
Iout = 150mA MAX

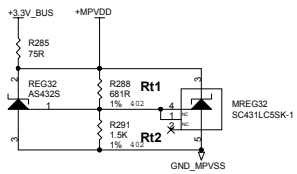


Need at least a 4.7uF output cap for stability

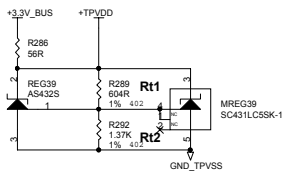
Alt. regulator for +PVDD
Vout = 1.8V
Iout = 30mA MAX



Alt regulator for +MPVDD
Vout = 1.8V
Iout = 10mA MAX



Alt. regulator for +TPVDD
Vout = 1.65V ~ 1.85V
Iout = 20mA MAX



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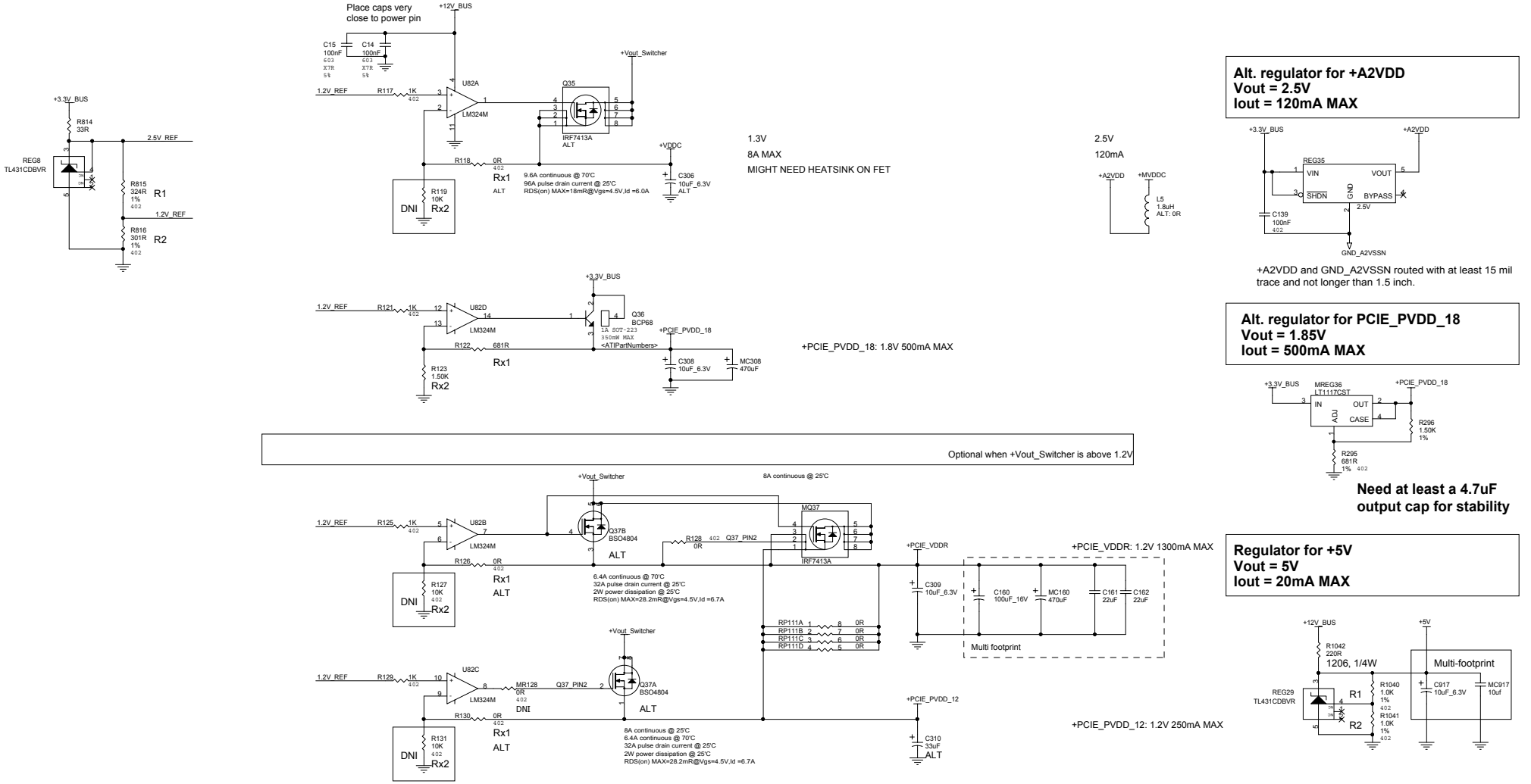

Part	Vout	R1	R2
MAX1935 0.8V Ref	1.2V	1.00K 1% 402 ATI P/N 3160100100	2.00K 1% 402 ATI P/N 3160200100
	1.79V	6.81K 1% ATI P/N 3160681100	5.49K 1% 402 ATI P/N 3160549100

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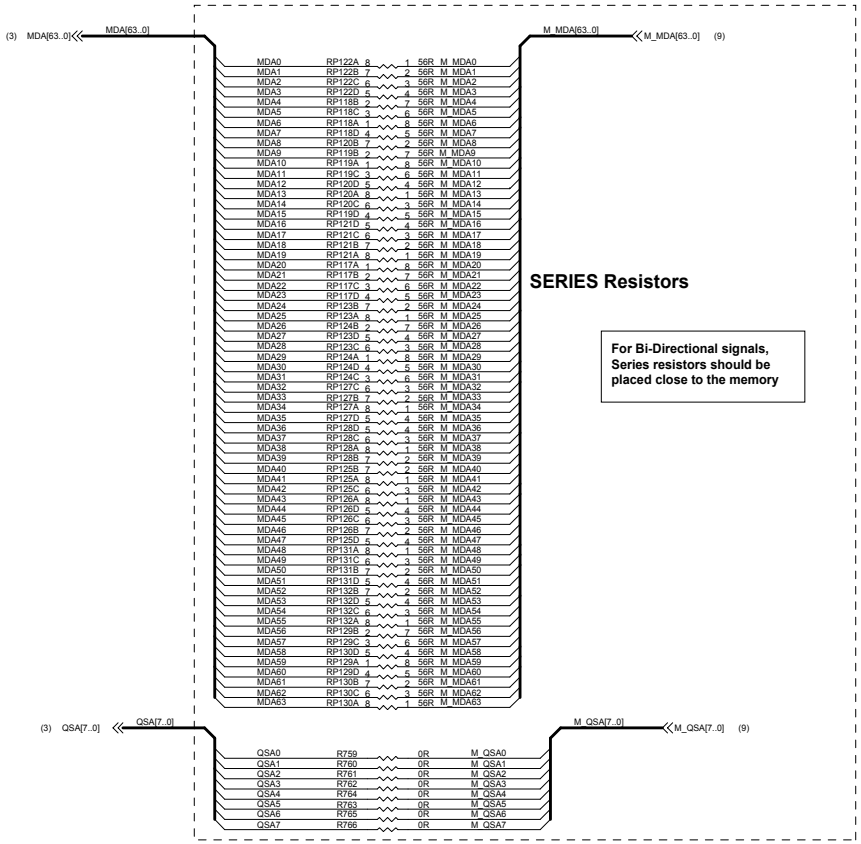

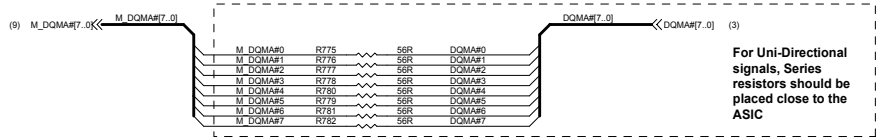

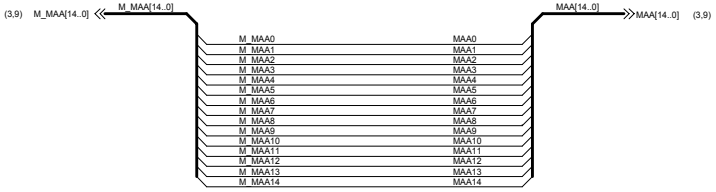

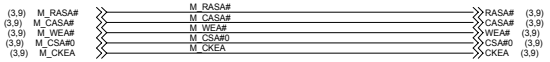

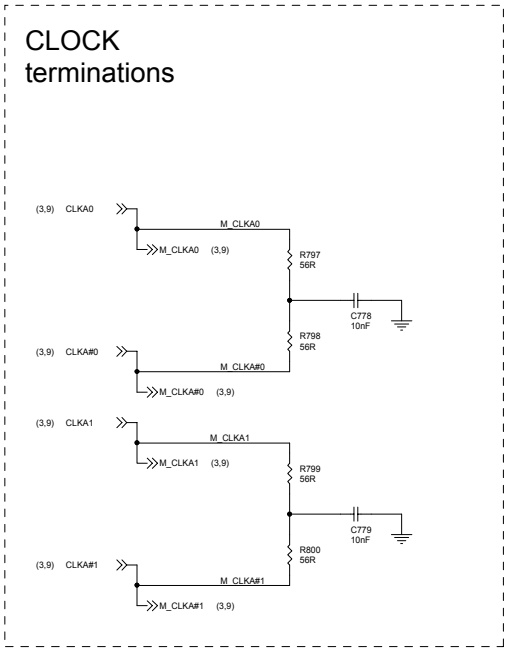

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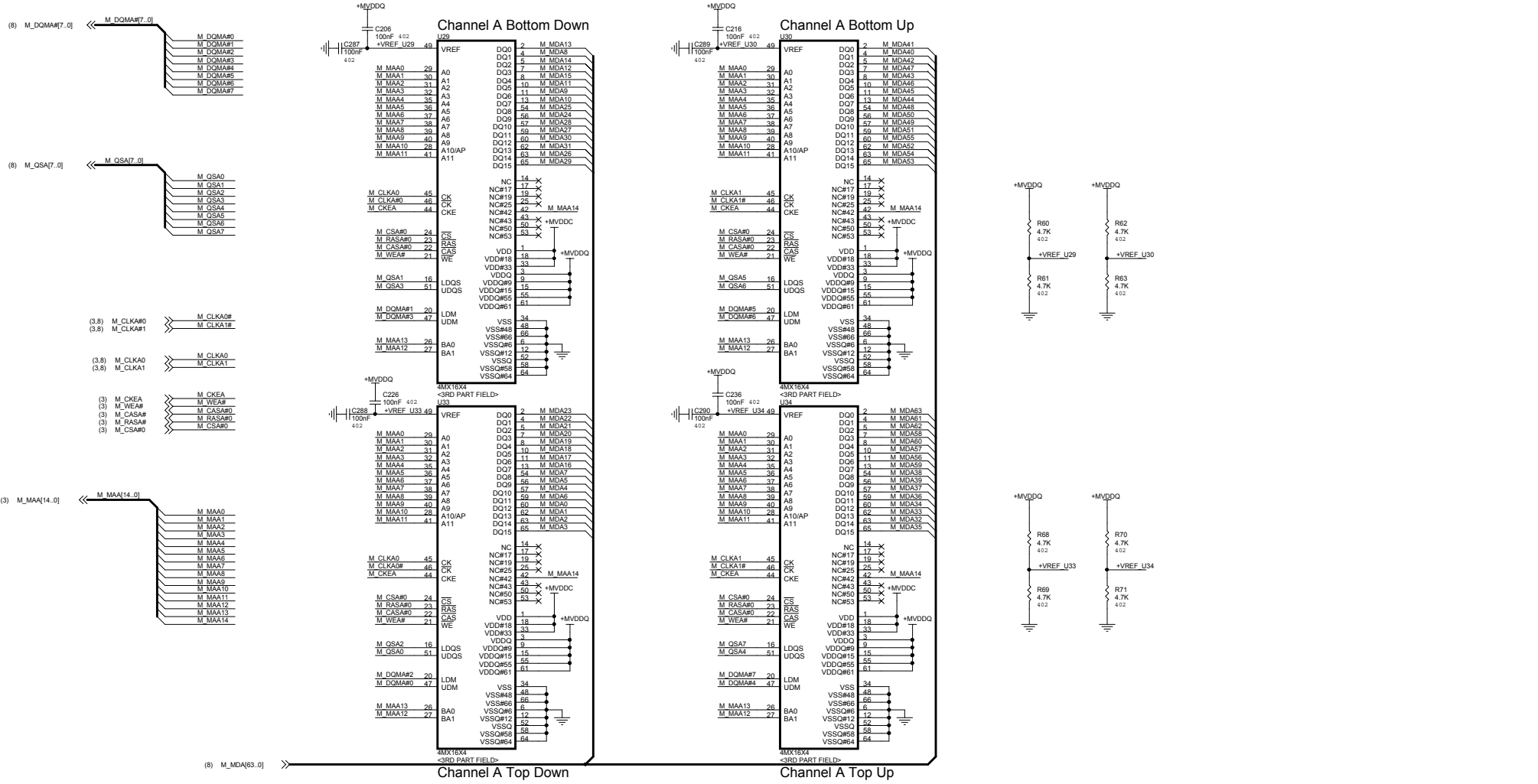
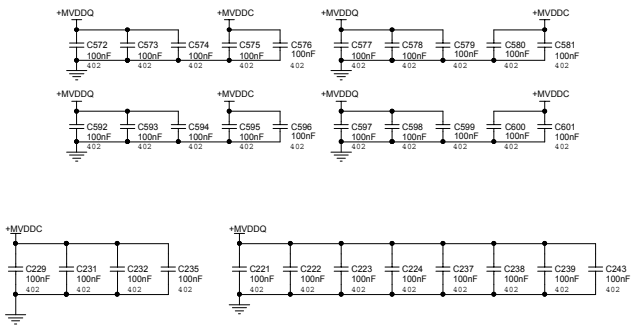


Put 1 1uF cap per power pin of memory



DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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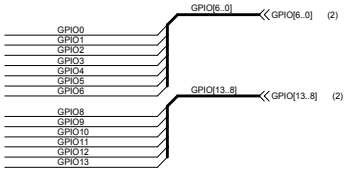
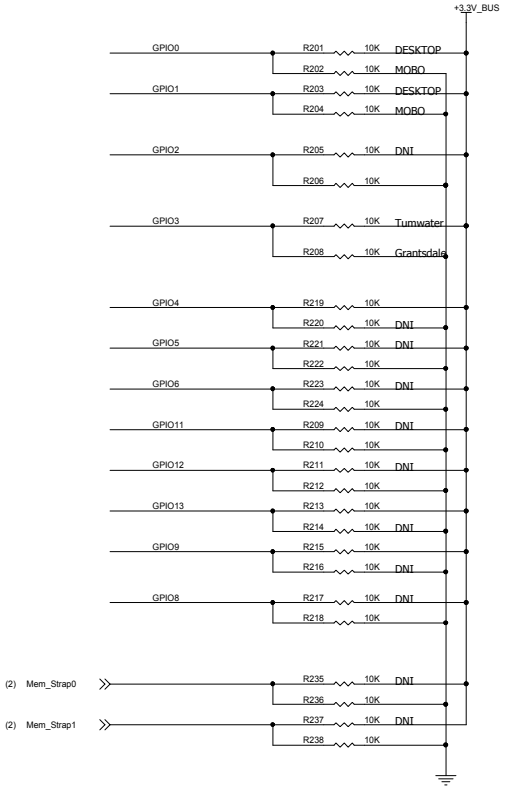
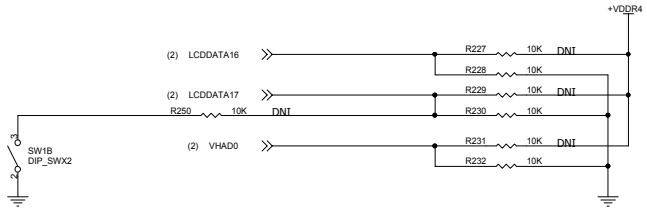
OPTION STRAPS





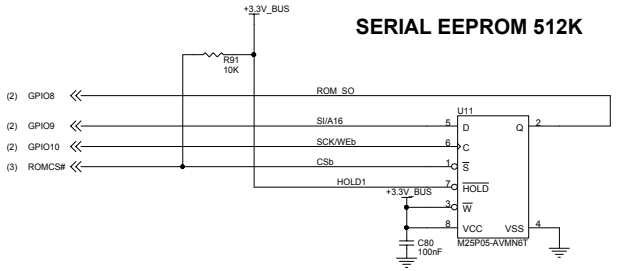


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
STRAP_B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
STRAP_B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode (Grantsdale) 01: Kyrene-compatible mode 10: PCI Express 1.0 mode (Tumwater) 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
STRAP_B_PTX_IEXT	GPIO4	Transmitter Extra Current 0: normal mode 1: extra current in Tx output stage - potential power savings for mobile mode	0
STRAP_FORCE_COMPLIANCE	GPIO5	Force chip to go to Compliance state quickly for Tester purposes 0: normal operational mode 1: compliance mode	0
STRAP_B_PPLL_BW	GPIO6	PLL Bandwidth 0: full PLL Bandwidth 1: reduced PLL bandwidth	0
STRAP_DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	DVPDATA_20 (VHAD0 net)	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

SERIAL EEPROM 512K



<Variant Name>

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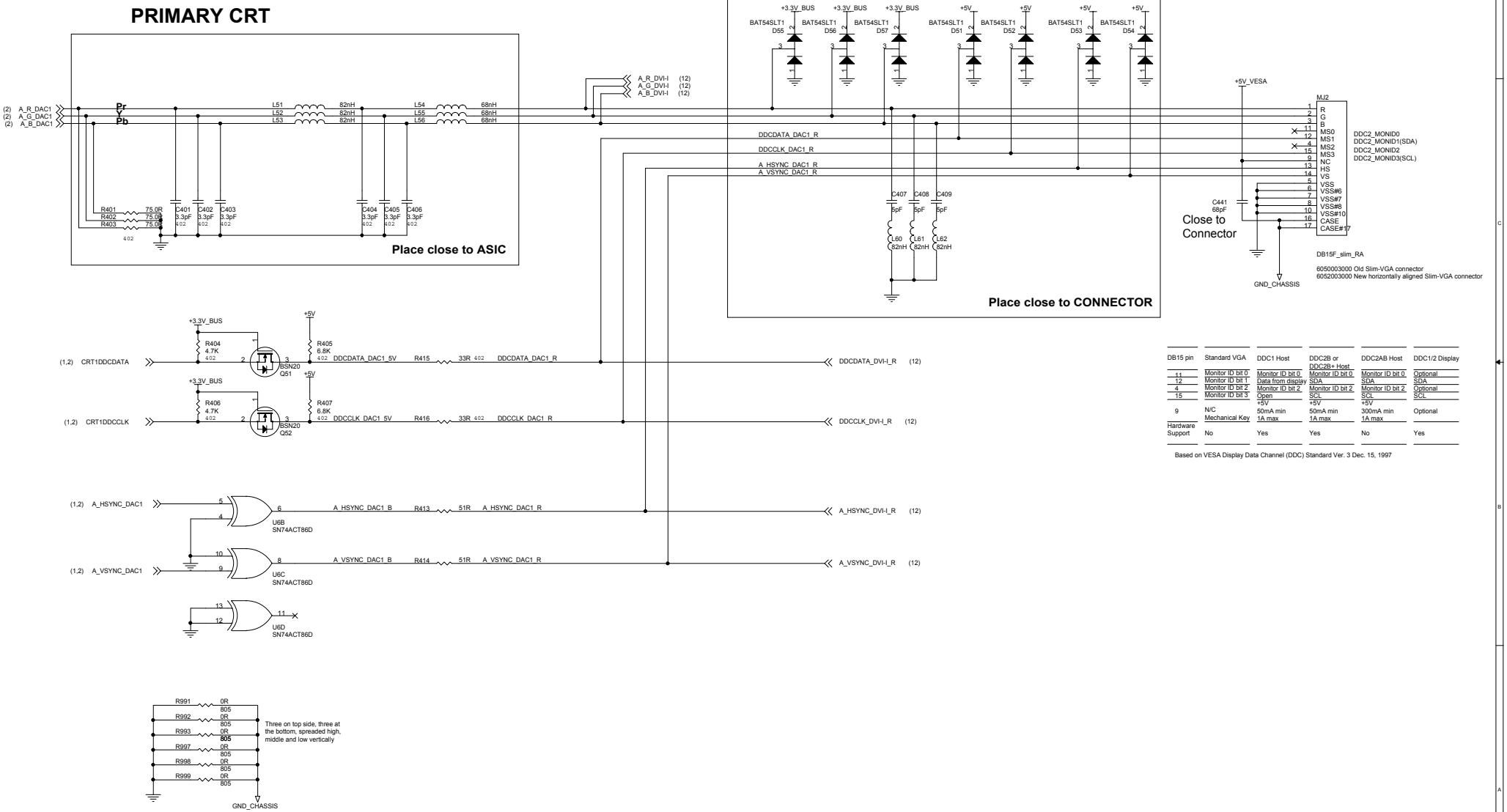
PRIMARY CRT



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from display	SDA	SDA	SDA
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	SCL	SCL	SCL
9	N/C	+5V 50mA min	+5V 50mA min	+5V 300mA min	Optional
Hardware Support	Mechanical Key	1A max	1A max	1A max	
	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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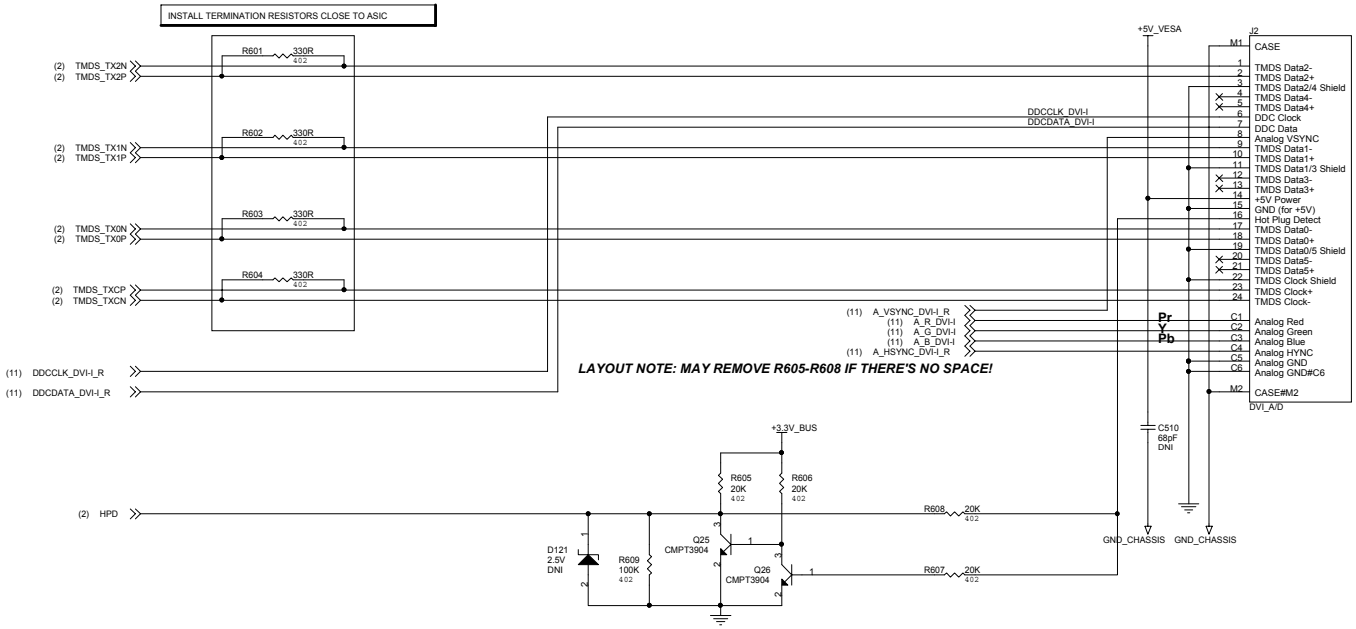
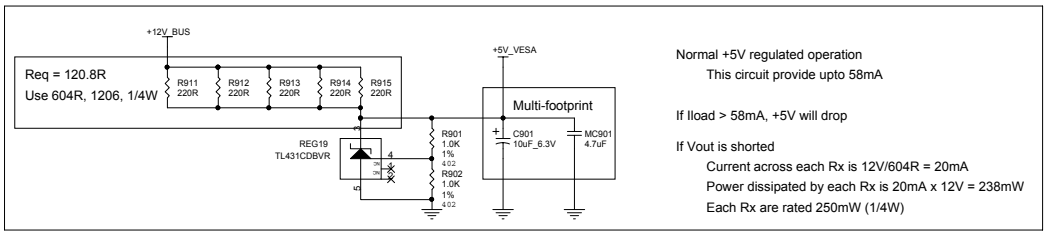
PRIMARY DVI-I CONNECTOR





Normal +5V regulated operation
This circuit provide upto 58mA

If Iload > 58mA, +5V will drop

If Vout is shorted
Current across each Rx is 12V/604R = 20mA
Power dissipated by each Rx is 20mA x 12V = 238mW
Each Rx are rated 250mW (1/4W)

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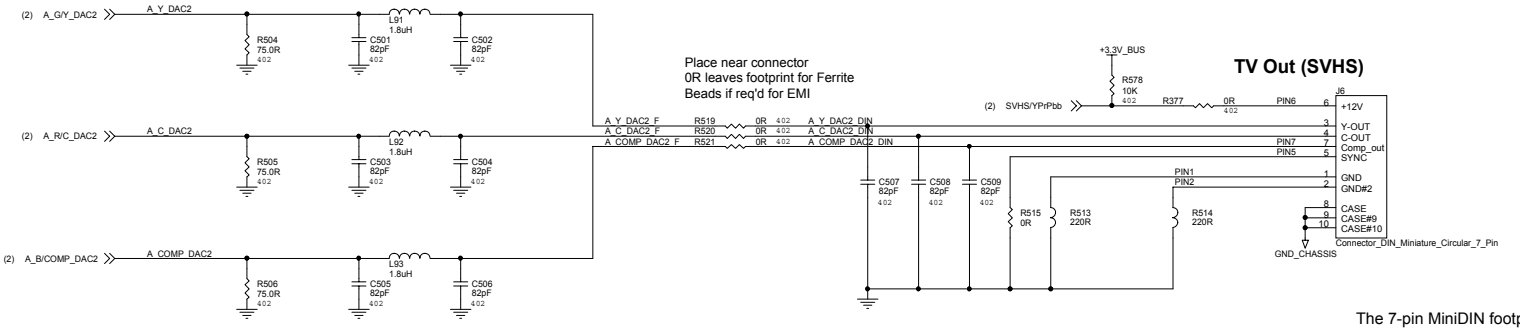
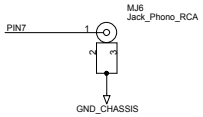
Place Resistors close to ASIC.



TV Out (SVHS)

The 7-pin MiniDIN footprint allows one of the two MiniDINs:
- 7-pin Svideo/Composite MiniDIN P/N 6071001500
- 4-pin Svideo MiniDIN P/N 6070001000



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DVI/VGA SCREWS

ASSY1
SCREW
JACKSCREW

ASSY2
SCREW
JACKSCREW

MISC. BOARD PARTS

ASSY7
ANTISTATIC BAG
6_X_11

REF5
ATI LOGO LABEL
ATI_LOGO_LABEL

ASSY8
BLANK LABEL
9050005900;9050005900;9050005900;9050005900

+12V_BUS
JU1

H101
heatsink
7120005800

H100
HEATSINK
7120005100
Spring push-pin

MH101
HEATSINK
7120002700

MH100
HEATSINK
7120008000
ITW push-pin

MT1
MT_Hole_0.136_in.
GND_CHASSIS

MT2
MT_Hole_0.136_in.
GND_CHASSIS

ATX Brackets

ASSY10
BRACKET
DVI ATX
NO TABS, DVI

ASSY11
BRACKET
DVI+MiniDIN ATX
TOP TAB (LP), DIN, DVI
8020033000

Slim-VGA ATX

80200329D0 is removed due to missing symbol

6052003000 New horizontally aligned Slim-VGA connector

ASSY13
BRACKET
Slim-VGA+MiniDIN ATX
Old Out Slim VGA

6052003000 New horizontally aligned Slim-VGA connector

LP Brackets

ASSY14
BRACKET
DVI LP
LP, NO TABS, DVI
8020032600

ASSY15
BRACKET
DVI+MiniDIN LP
LP, TOP TAB, DIN, DVI

ASSY16
BRACKET
Slim-VGA LP
LP VGA
80200328F0
6052003000 New horizontally aligned Slim-VGA connector

ASSY17
BRACKET
Slim-VGA+MiniDIN LP
LP VID OUT VGA

6052003000 New horizontally aligned Slim-VGA connector

MASSY16
BRACKET
Slim-VGA LP
LP, DUAL TABS, Slim VGA

6050003000 Old Slim-VGA connector

MASSY17
BRACKET
Slim-VGA+MiniDIN LP
LP, DUAL TABS, DIN, Slim VGA

6050003000 Old Slim-VGA connector

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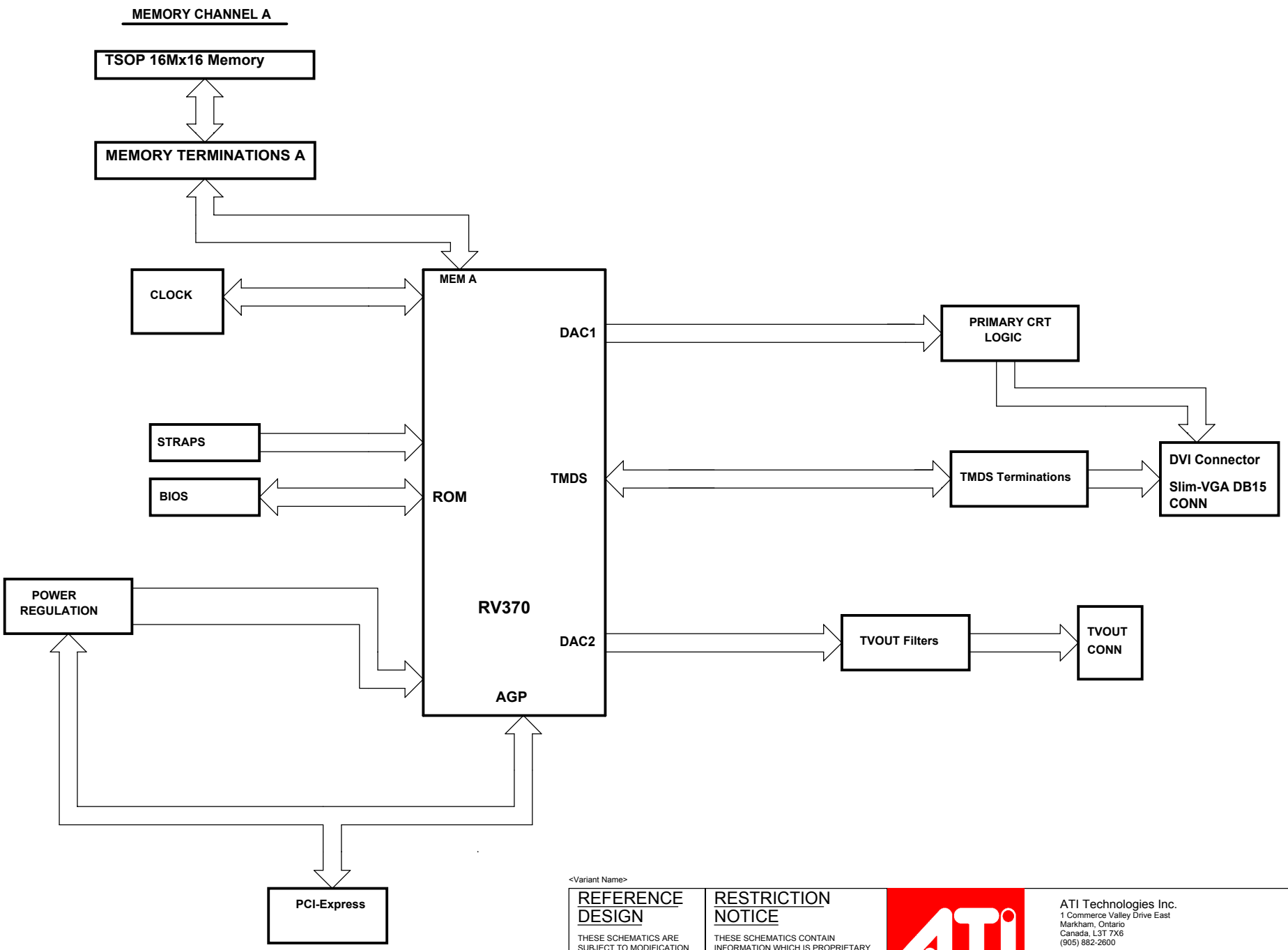

<Variant Name>

REFERENCE DESIGN

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RESTRICTION NOTICE

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