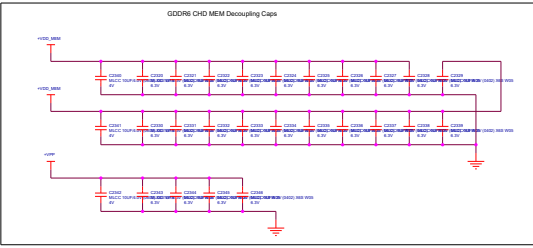
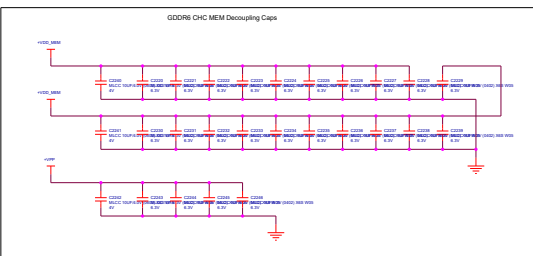
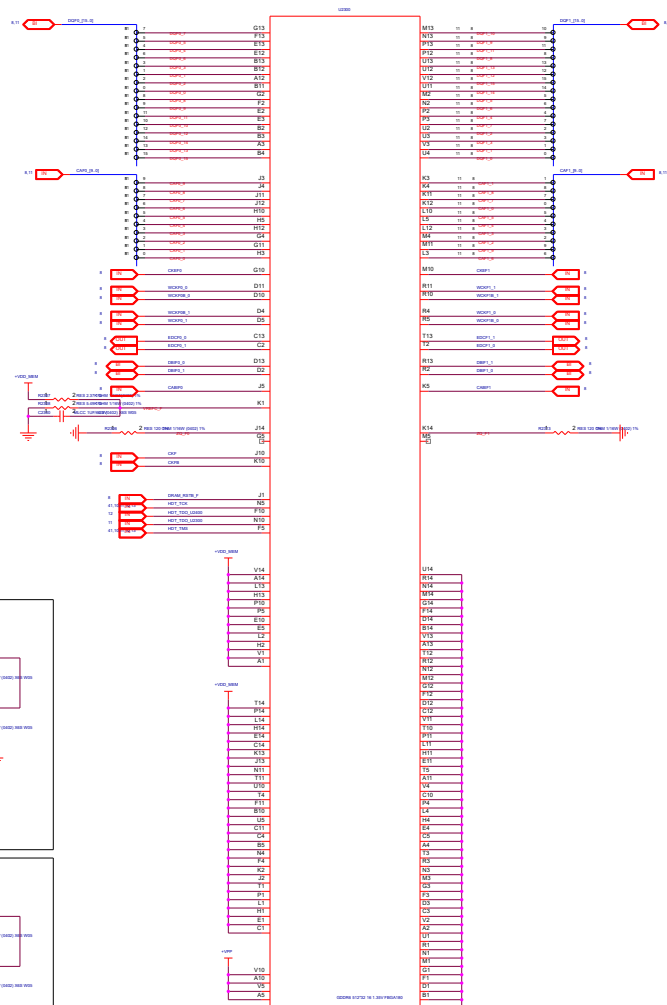
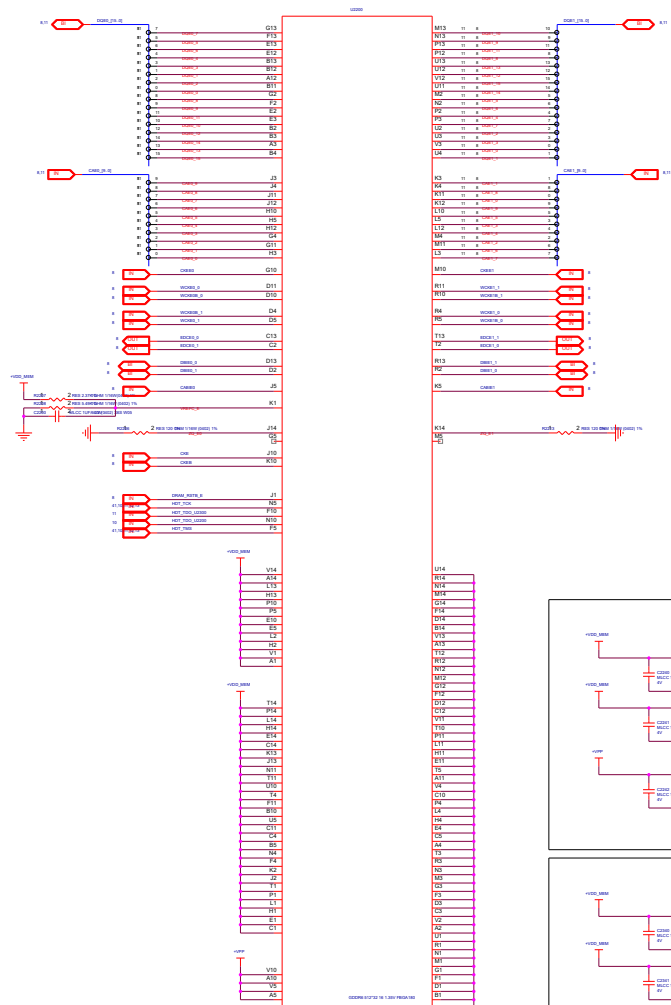


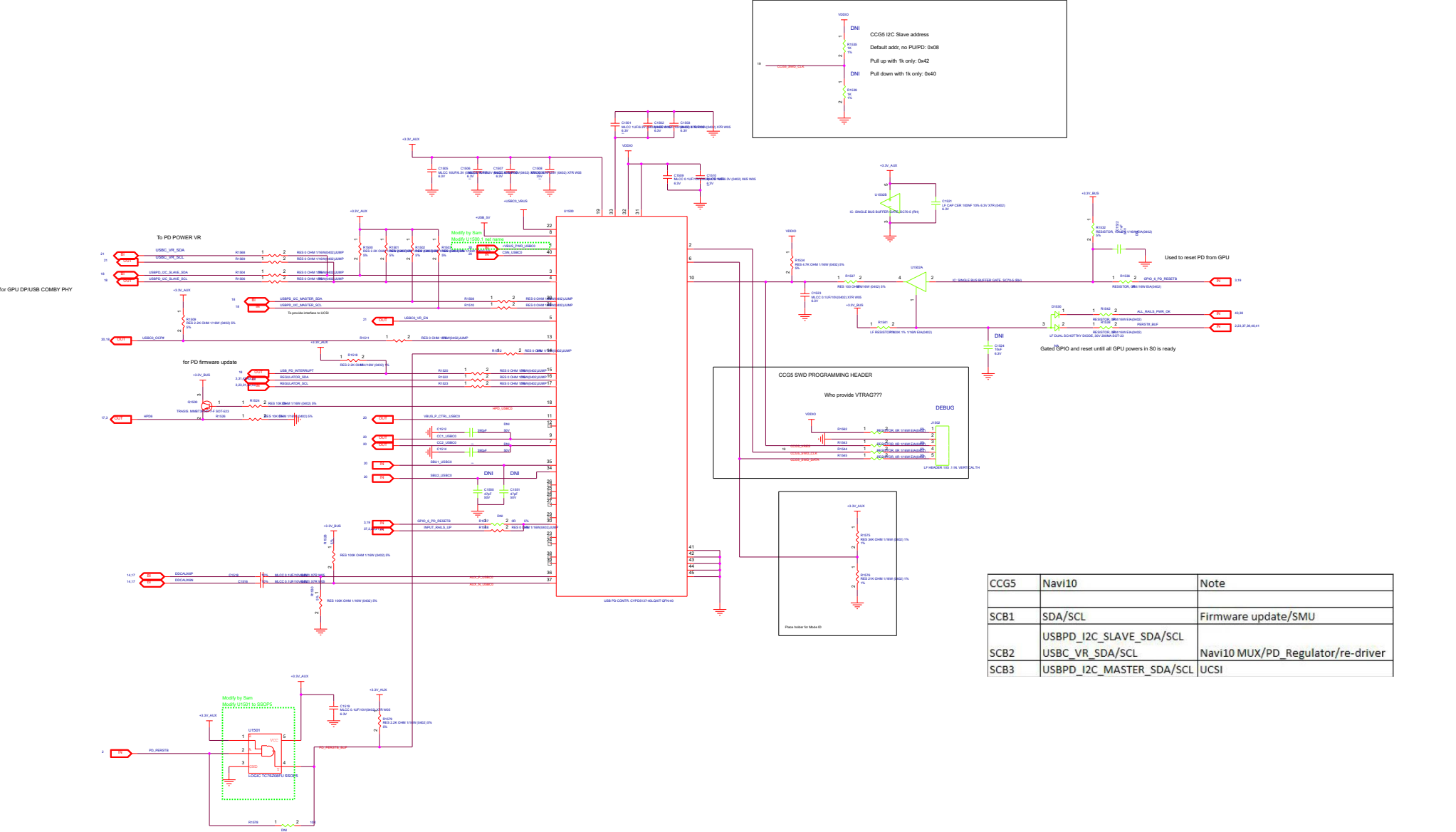
ASIC CH0 -> MEM CHA

ASIC CH1 -> MEM CHB

ASIC CH0 -> MEM CHA

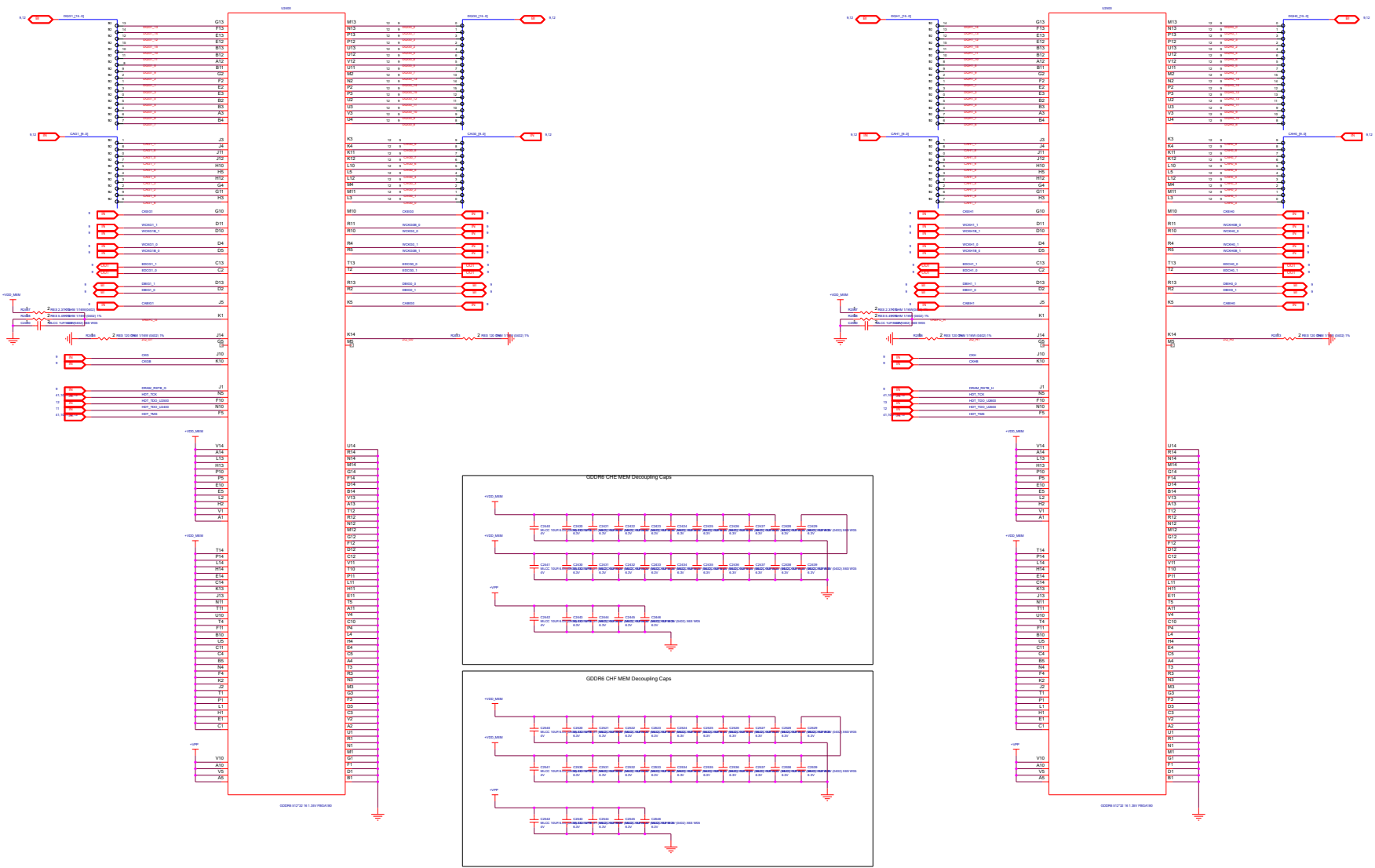
ASIC CH1 -> MEM CHB

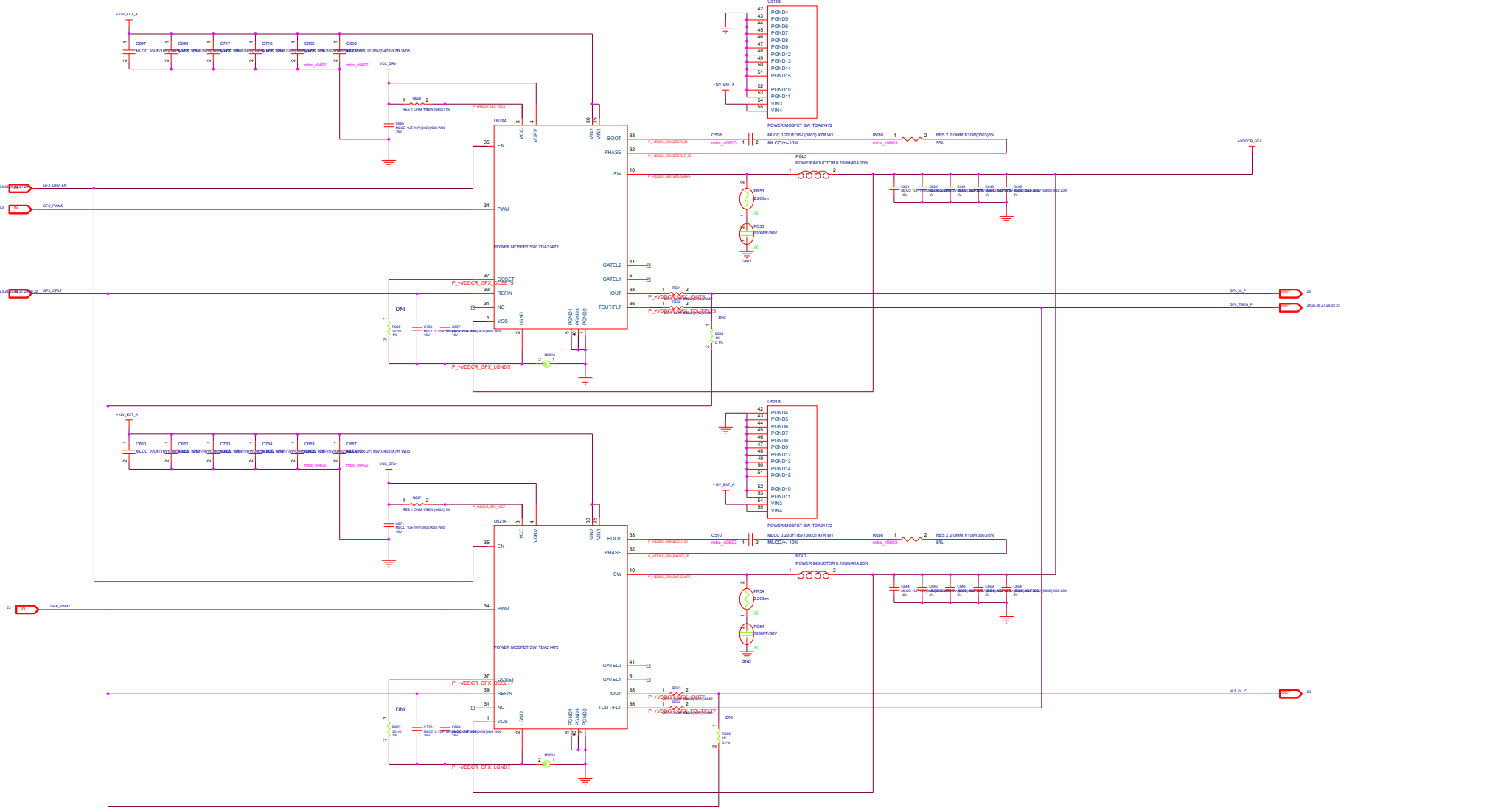


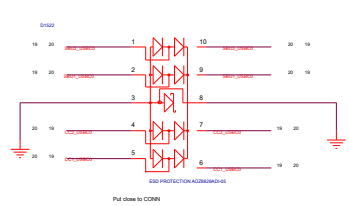
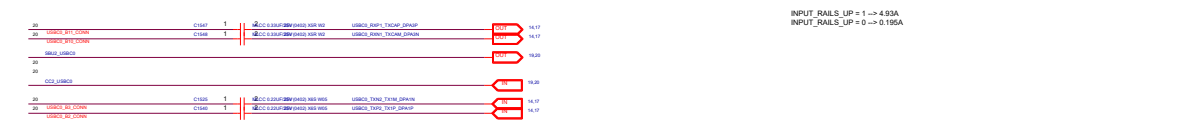
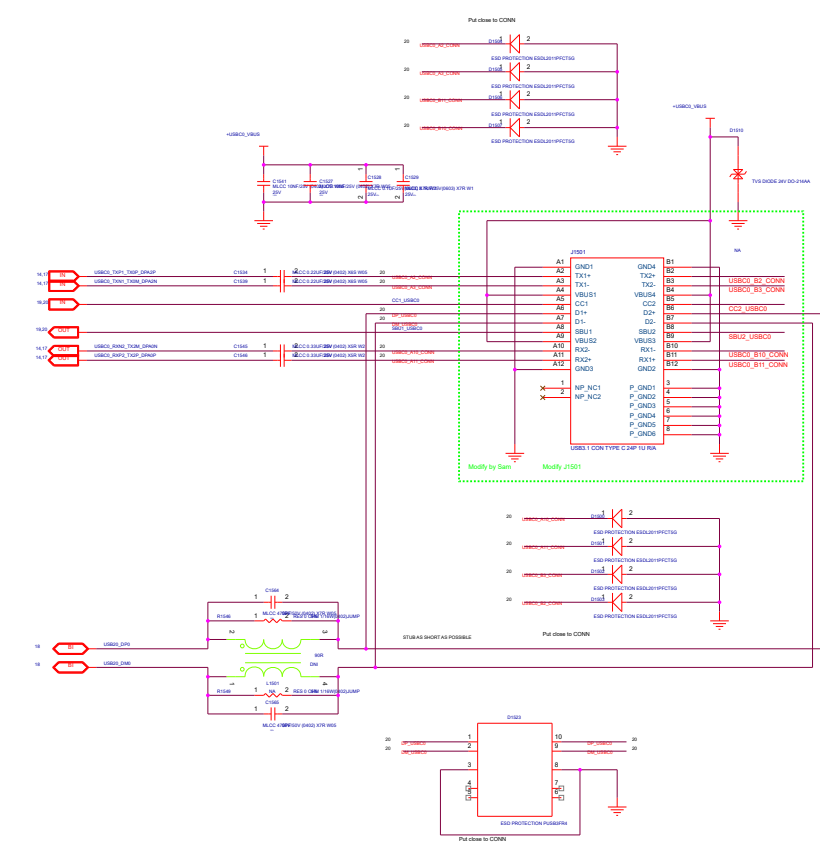
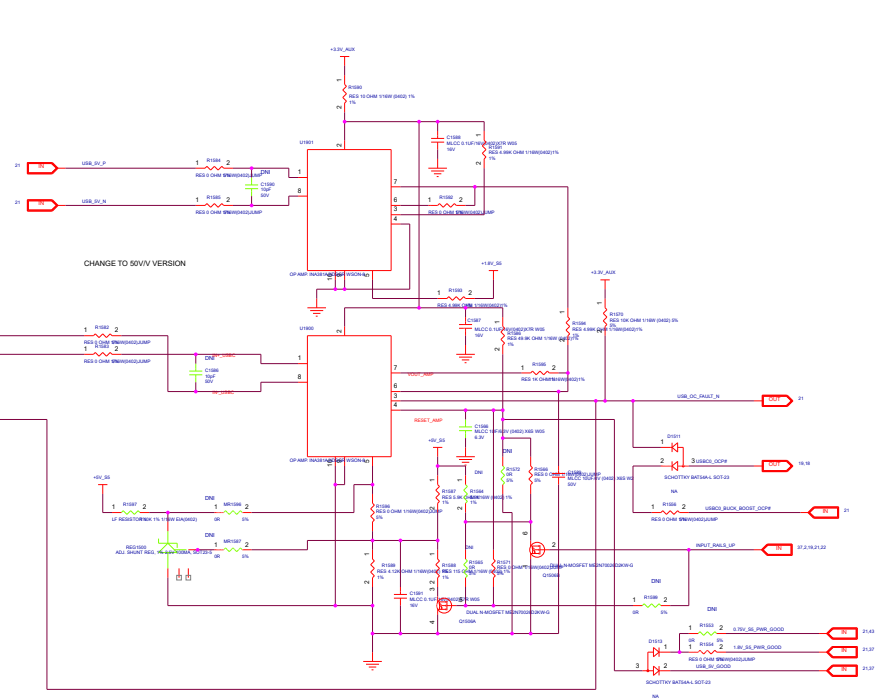
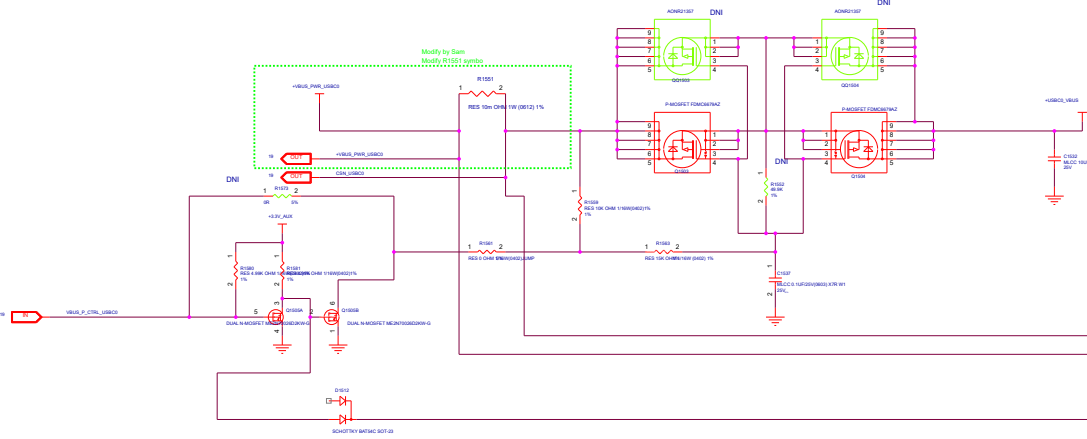


ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA

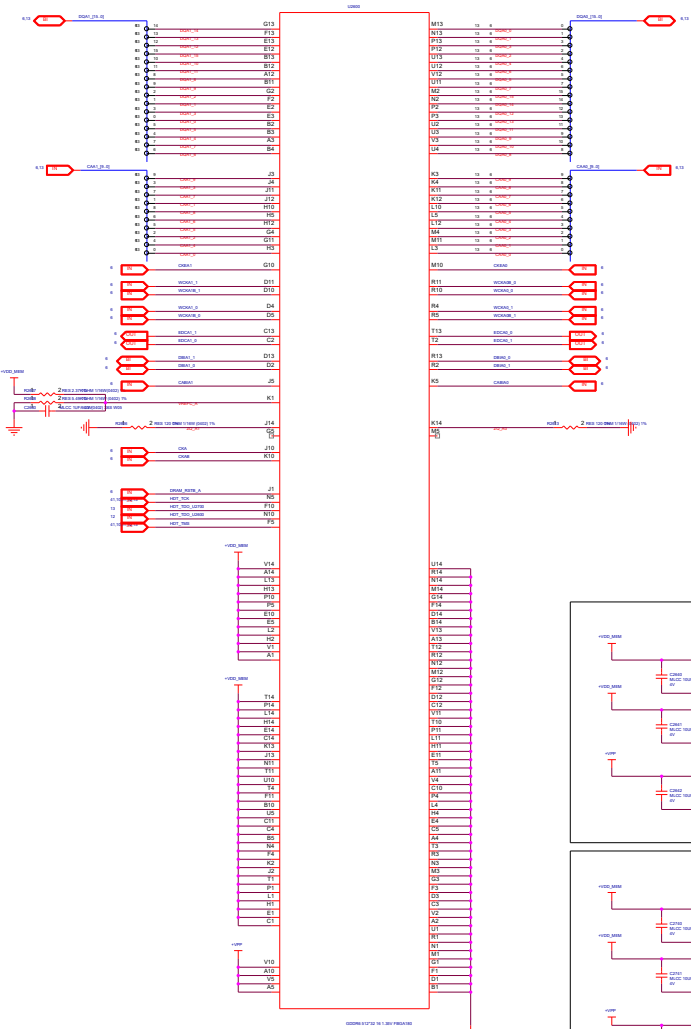
ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA



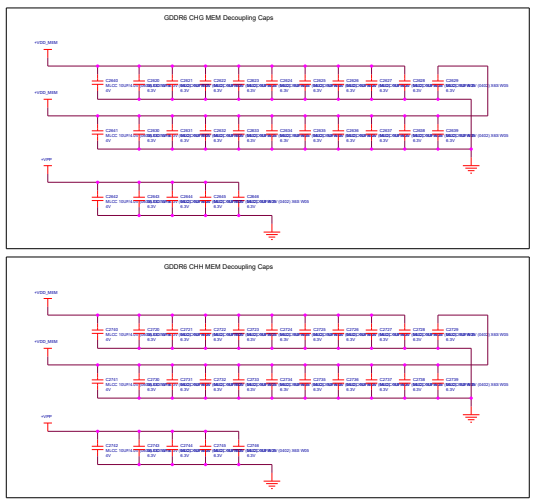
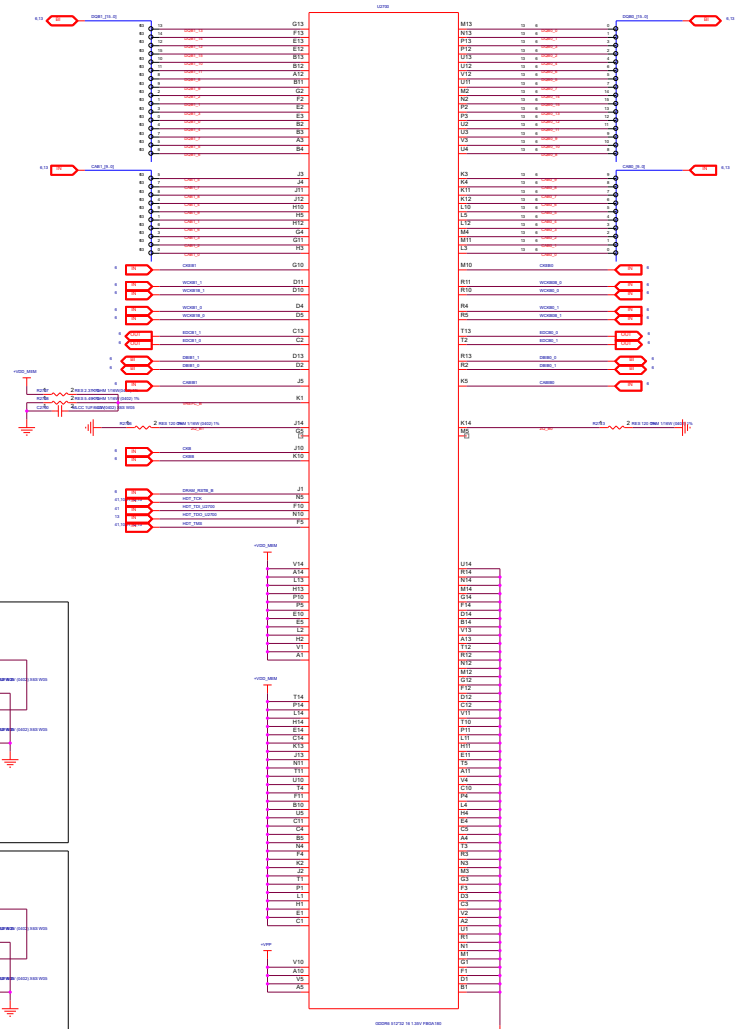


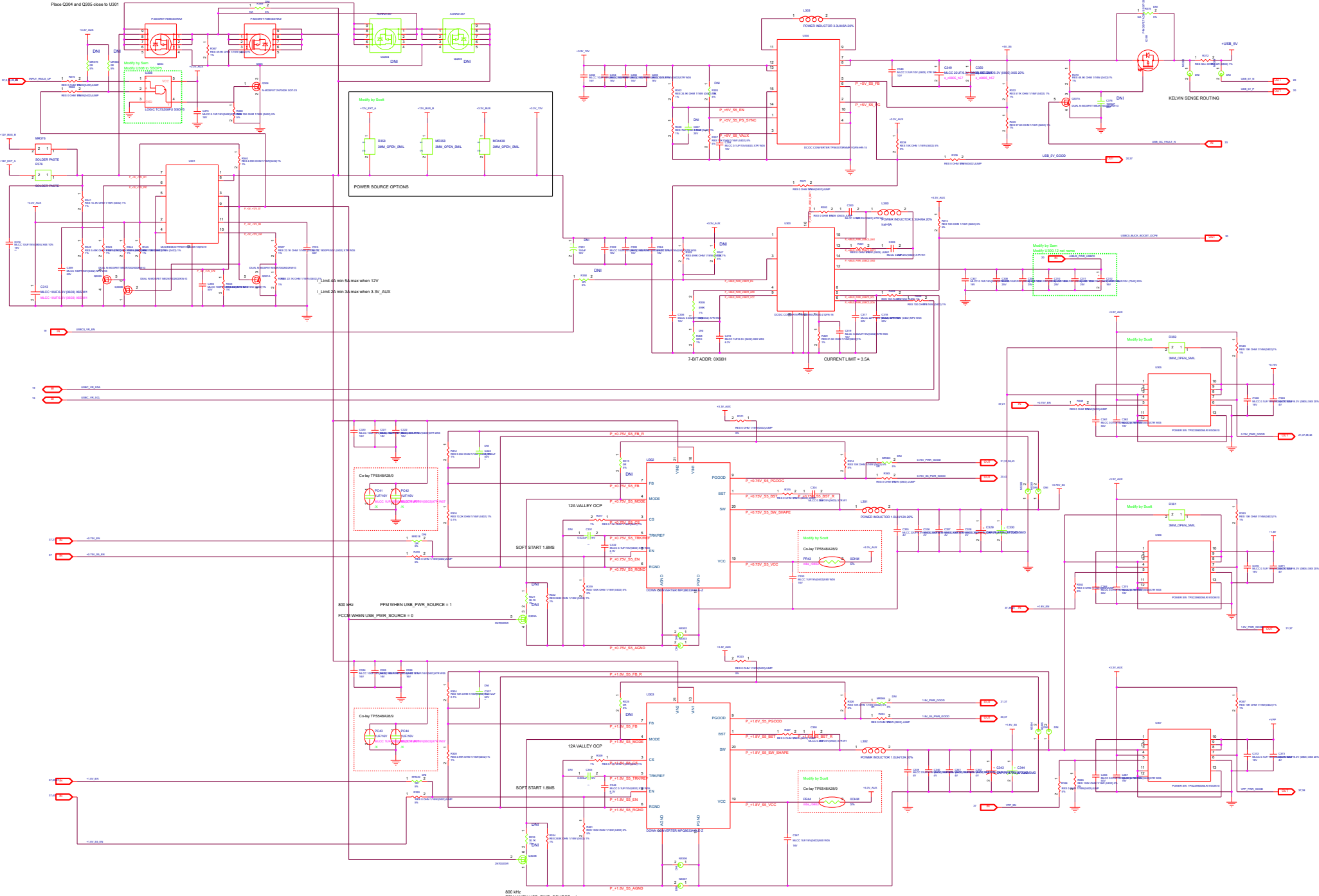


ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA



ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA





Place Q34 and Q35 close to U301

Limit 400mA when 12V
Limit 200mA when 3.3V_AUX

800 kHz PFM WHEN USB_PWR_SOURCE = 1
FCM WHEN USB_PWR_SOURCE = 0

800 kHz PFM WHEN USB_PWR_SOURCE = 1
FCM WHEN USB_PWR_SOURCE = 0

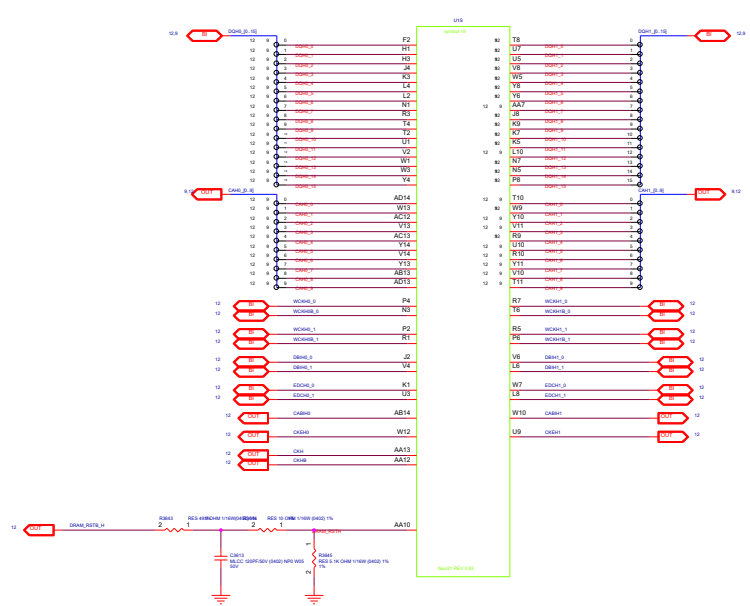
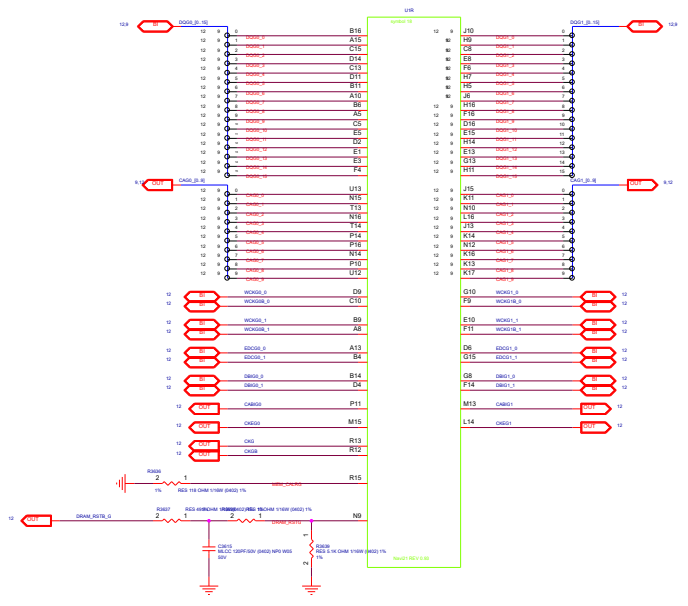
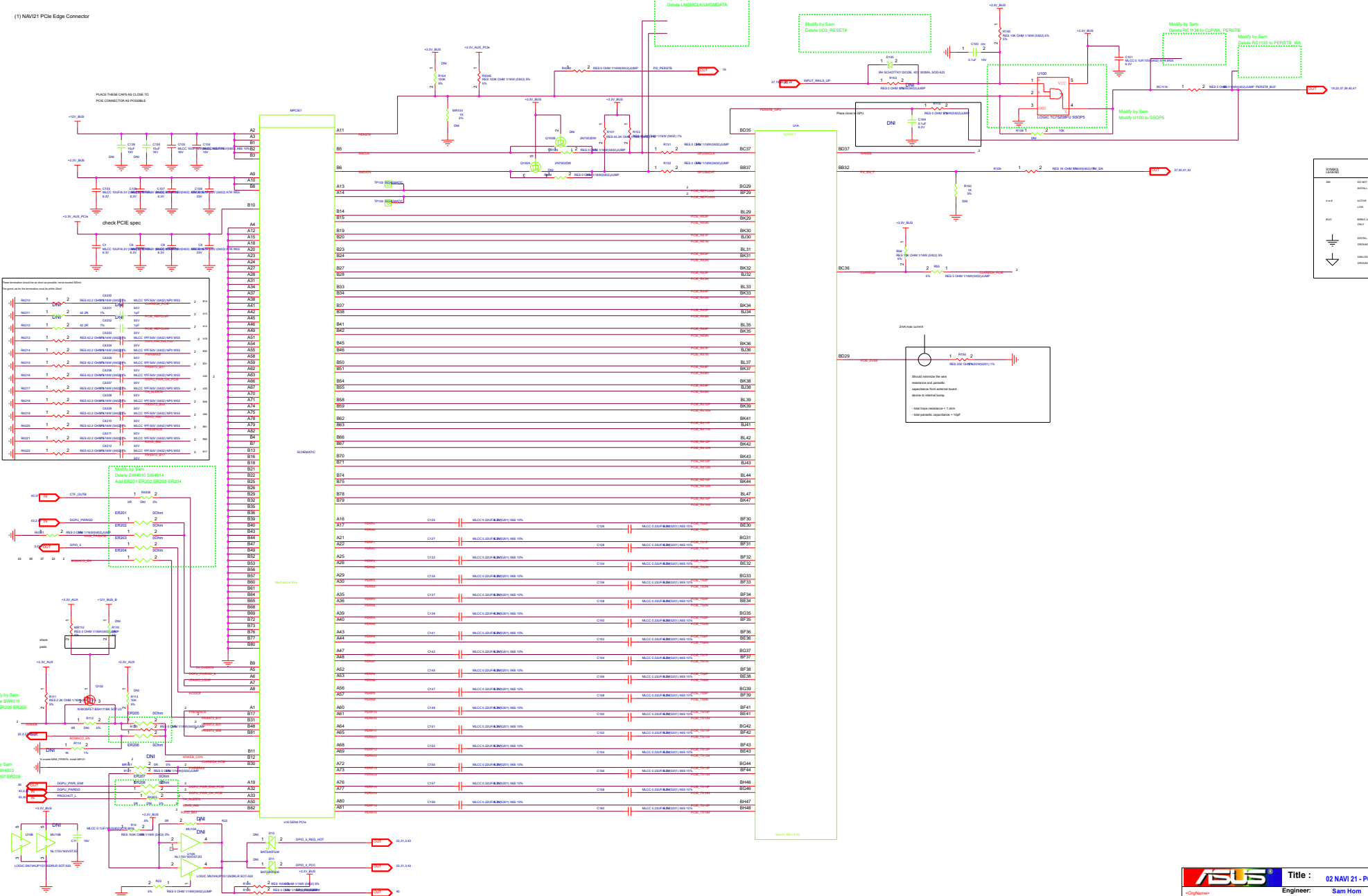
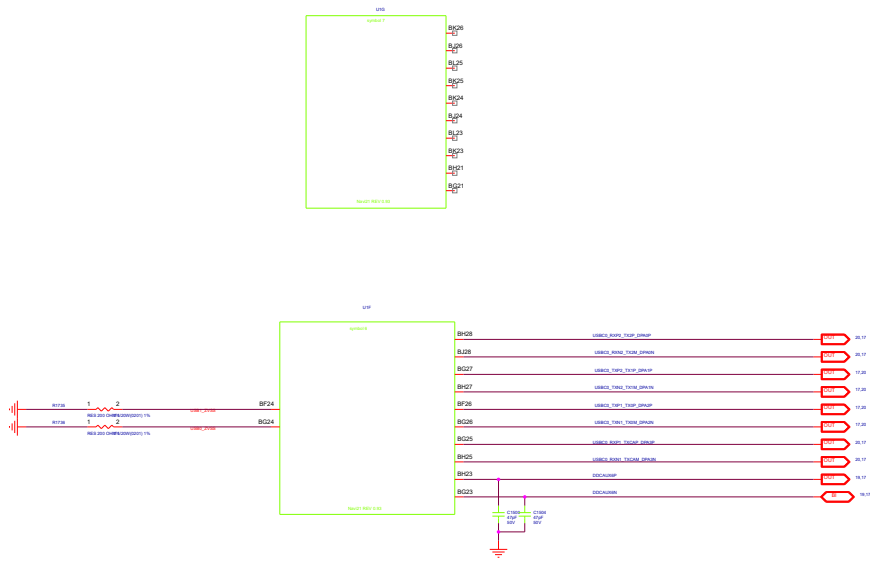
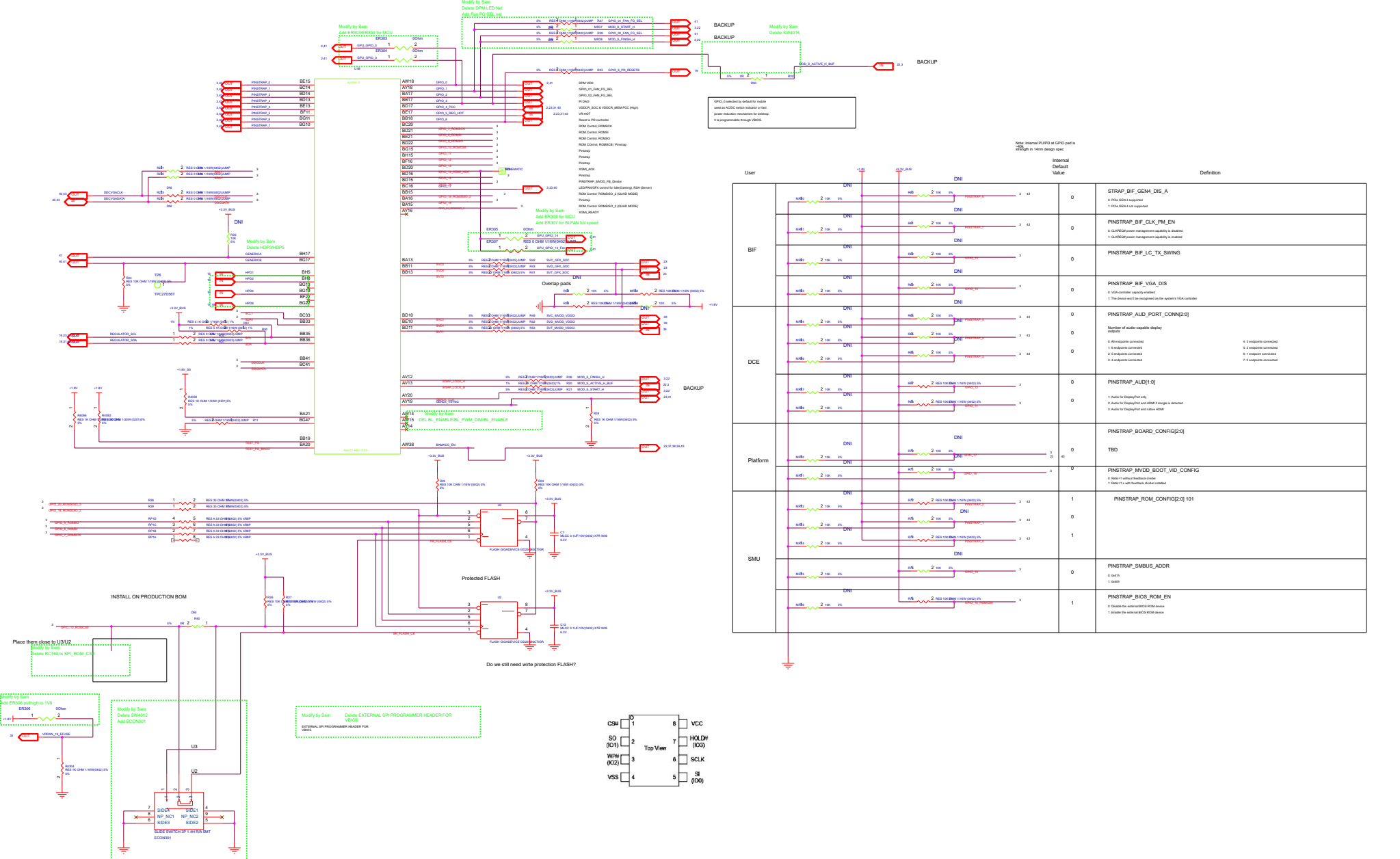


TABLE OF CONTENTS

SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	GFX PHASES 889
2	NAVI 21 - PCIe Interface	27	GFX PHASES 11
3	NAVI 21 - GPIOs	28	GFX PHASES 5&7
4	NAVI 21 XTAL	29	GFX PHASES 3&10
5	XGMI	30	SOC PHASE 1&2
6	NAVI 21 MEM CH AB	31	VDD_MEM & VDDCI CONTROLLER
7	NAVI 21 MEM CH CD	32	VDD_MEM PHASES 1&2
8	NAVI 21 MEM CH EF	33	VDDCI_MEM PHASE 1
9	NAVI 21 MEM CH GH	34	NAVI 21 DECAPS
10	GDDR6 MEM CH CD	35	NAVI 21 POWER
11	GDDR6 MEM CH EF	36	NAVI 21 POWER and GND
12	GDDR6 MEM CH GH	37	POWER_MANAGEMENT
13	GDDR6 MEM CH AB	38	ClampWA
14	NAVI21 TMDPA - USB-C	39	SVIZ & B&MACD
15	NAVI21 TMDPF - HDMI	40	THERMAL
16	NAVI21 TMDPC&E - DP	41	DPM_Status_LED & GDDR6_JTAG
17	NAVI21 TMDPA	42	PI Debug
18	NAVI21 USB	43	DEBUG
19	PD Controller	44	History
20	USB-C PORT 1		
21	USB_5V_1.8V_0.75V		
22	MODS CONTROL & POWER		
23	GFX & SOC CONTROLLER		
24	GFX PHASES 1&2		
25	GFX PHASES 4&6		



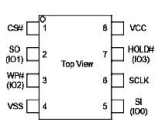


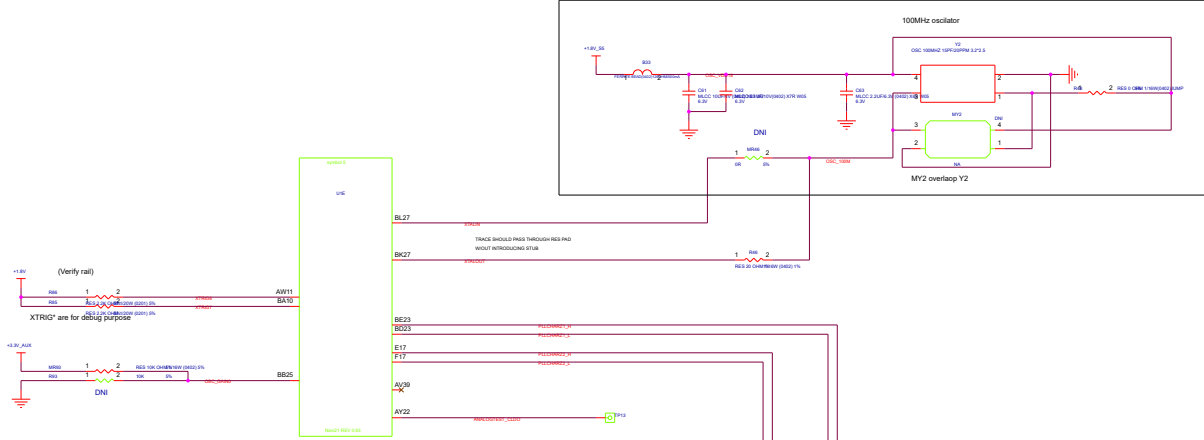


GPIOs selected by software to enable power reduction features for specific components through BIOS.

Note: Disabled PLUFG of GPIO pad is supported in 14nm design spec.

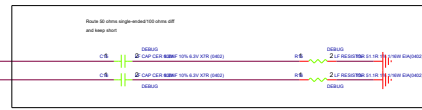
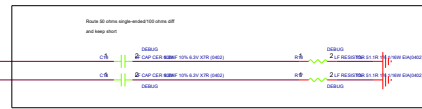
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: FPGAs is required 1: FPGAs is not required
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ power management capability is enabled 1: CLKREQ power management capability is disabled
	0	PINSTRAP_BIF_LC_TX_SWING
DCE	0	PINSTRAP_BIF_VGA_DIS 0: VGA interface capability is enabled 1: The device won't be recognized as the system's VGA controller
	0	PINSTRAP_AID_PORT_CONN2[0] Number of auto-capable display outputs 0: No outputs connected 1: 1 output connected 2: 2 outputs connected 3: 3 outputs connected
	0	PINSTRAP_AID_PORT_CONN2[1] 0: No outputs connected 1: 1 output connected 2: 2 outputs connected 3: 3 outputs connected
	0	PINSTRAP_AID_PORT_CONN2[2] 0: No outputs connected 1: 1 output connected 2: 2 outputs connected 3: 3 outputs connected
	0	PINSTRAP_AID[1:0] 1: Audio for DisplayPort only 0: Audio for DisplayPort and other outputs is disabled 2: Audio for DisplayPort and other outputs is disabled
Platform	0	PINSTRAP_BOARD_CONFIG[0] TBD
	0	PINSTRAP_INVDD_BOOT_VID_CONFIG 0: Reserve 11 with feedback driver 1: Reserve 11 with feedback driver disabled
SMU	1	PINSTRAP_ROM_CONFIG[0] 101
	0	PINSTRAP_SMBUS_ADDR 0: built-in 1: built-in
	1	PINSTRAP_BIOS_ROM_EN 0: Disable the optional BIOS ROM device 1: Enable the optional BIOS ROM device

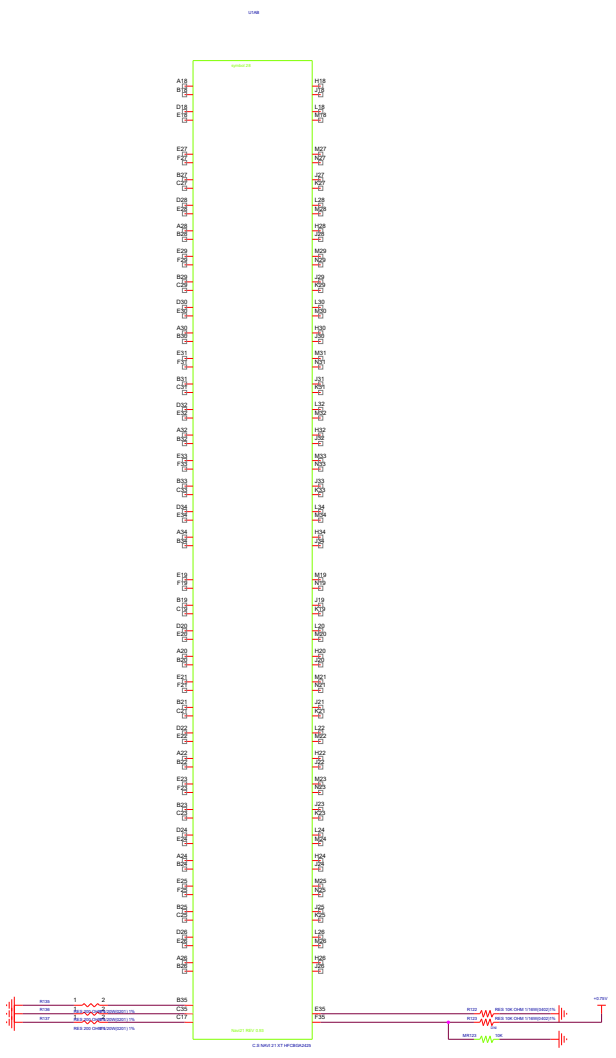


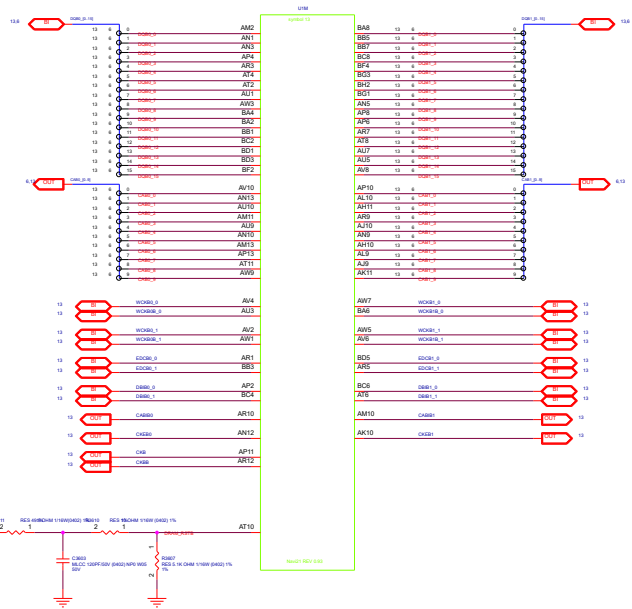
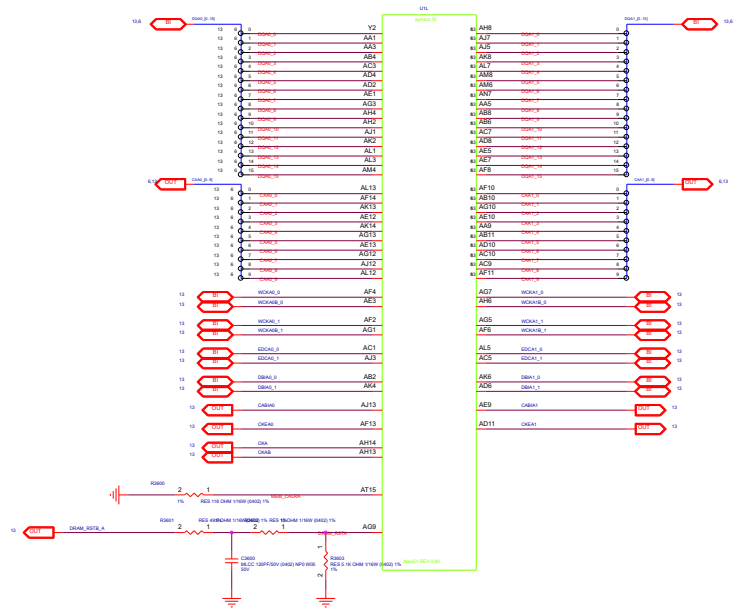


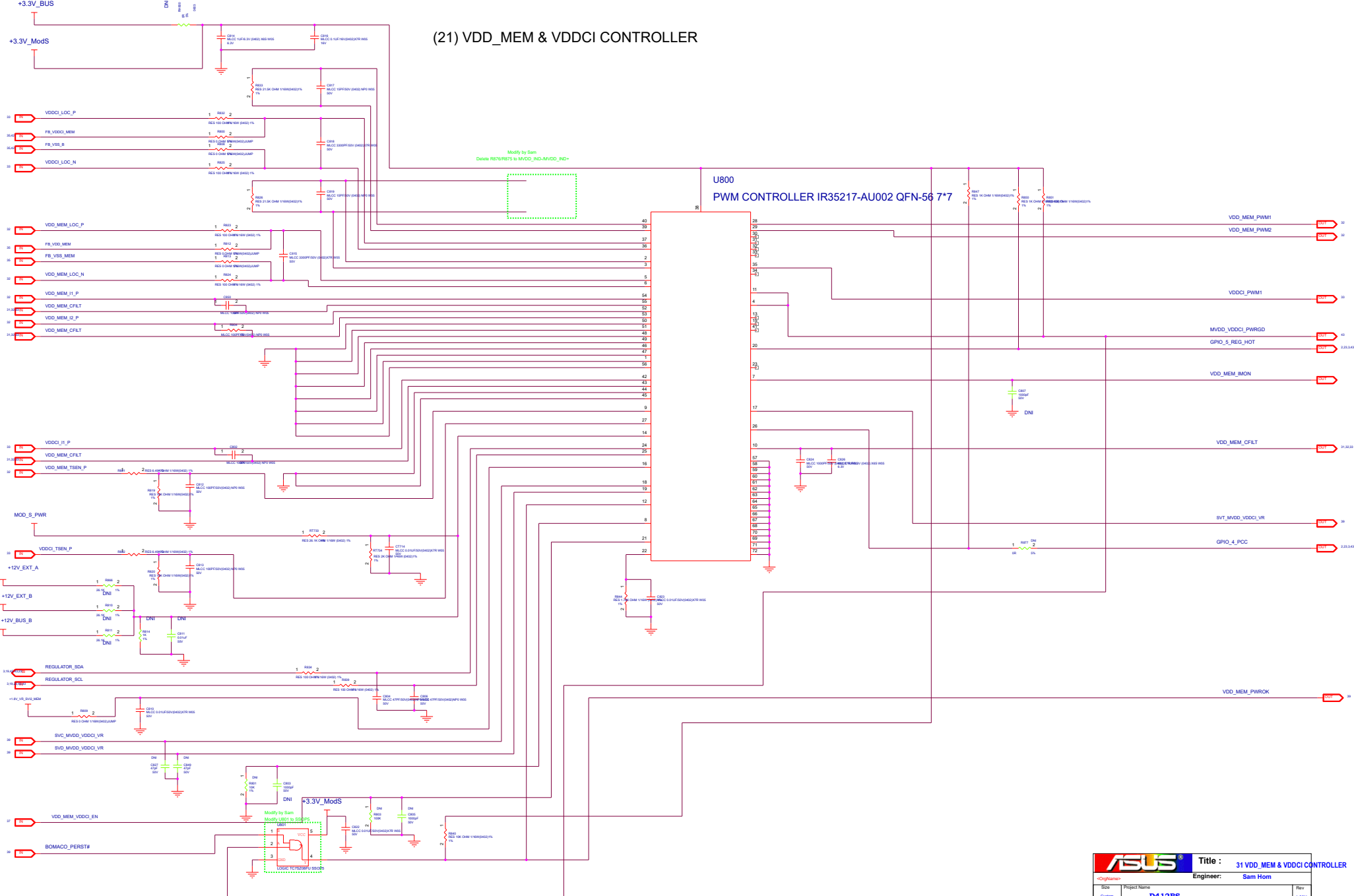
Default OSC_GAIN is 0x7. Pull-up OSC_GAIN to 3.3V_SSP

When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.





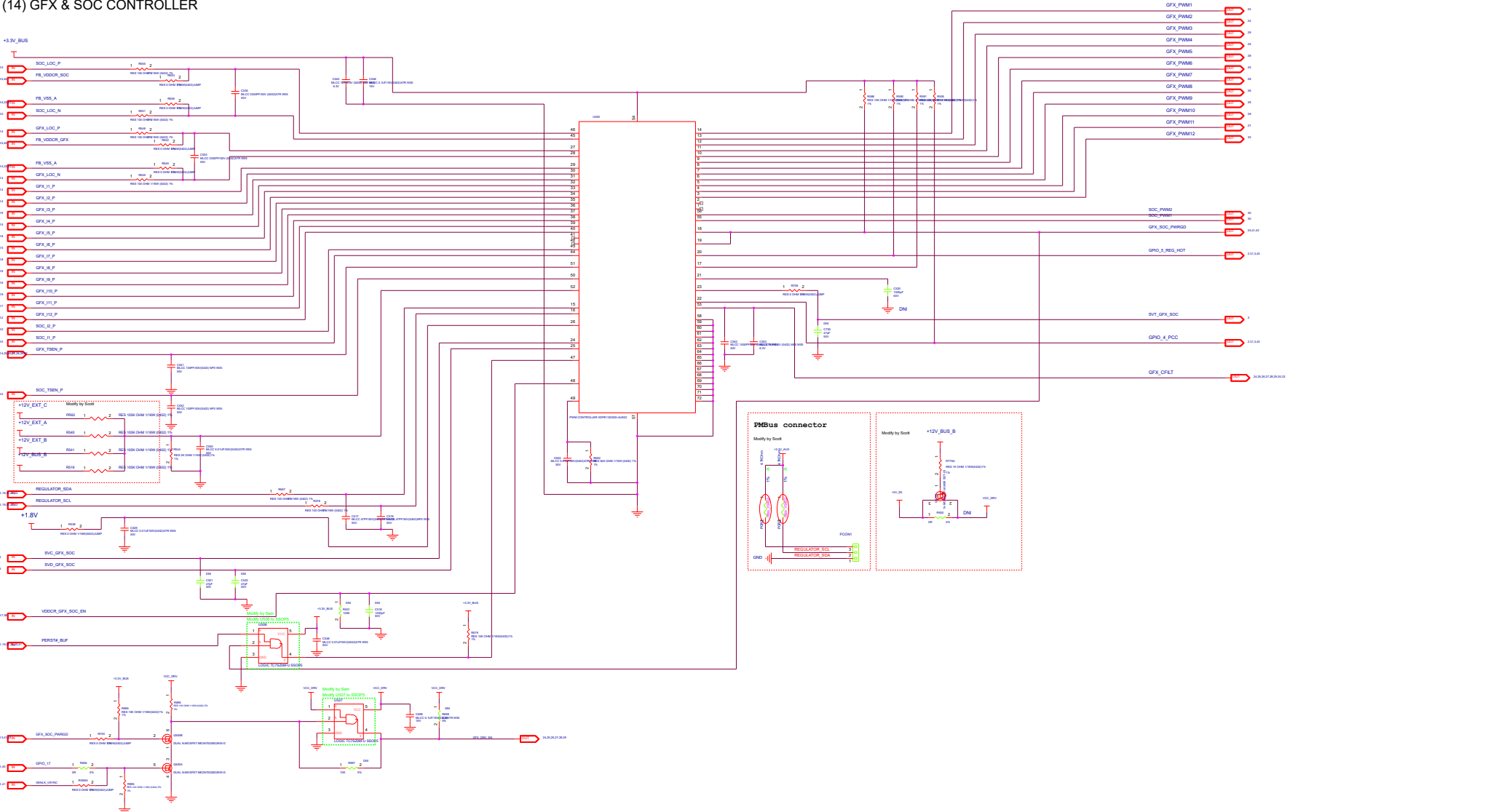




(21) VDD_MEM & VDDCI CONTROLLER

U800
PWM CONTROLLER IR35217-AU002 QFN-56 7*7

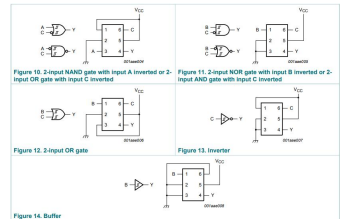
4) GFX & SOC CONTROLLER



Modify by Scott
Delete GC1119GC1139GC1116GC1149GC11156UC1119

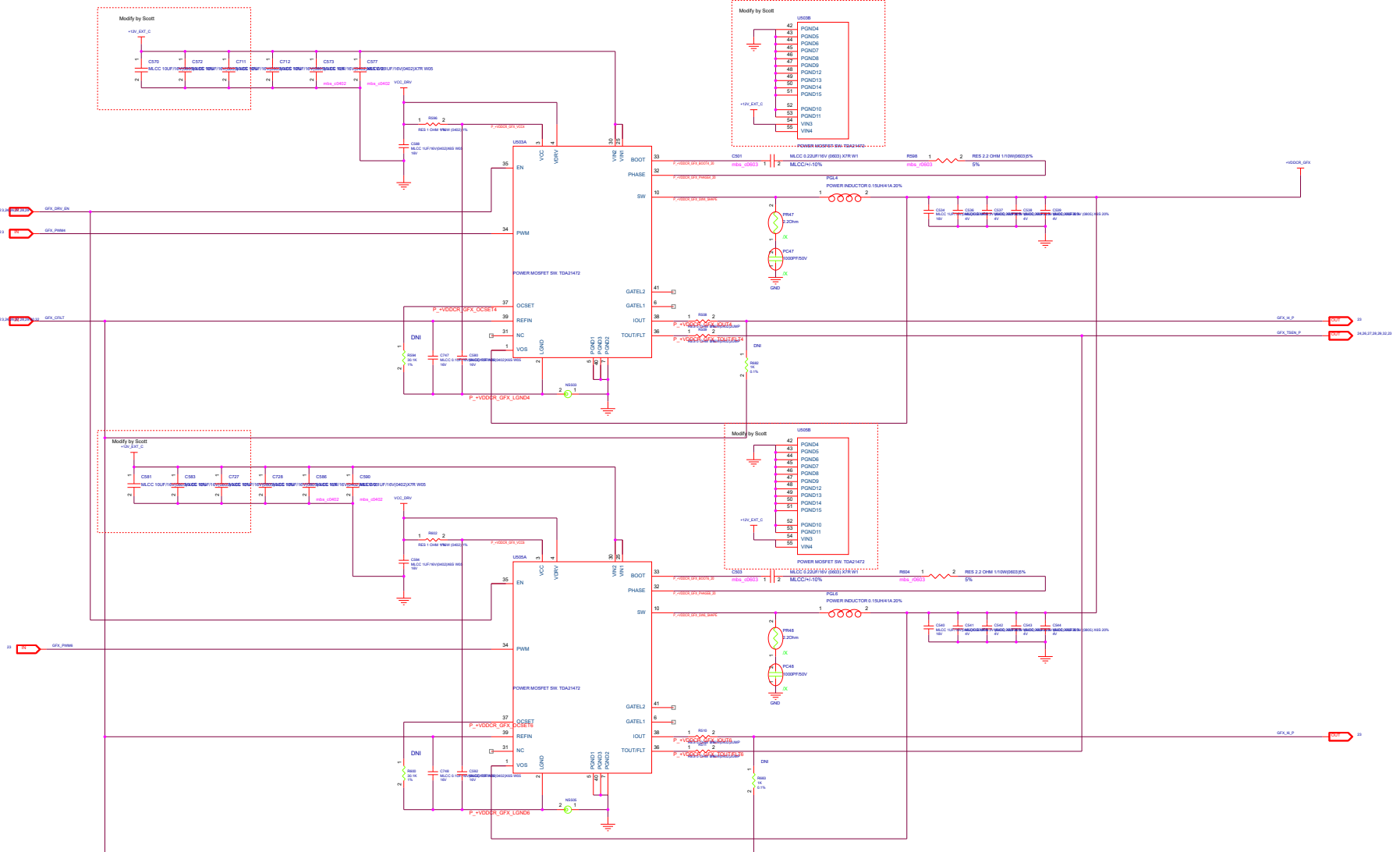
Modify by Scott

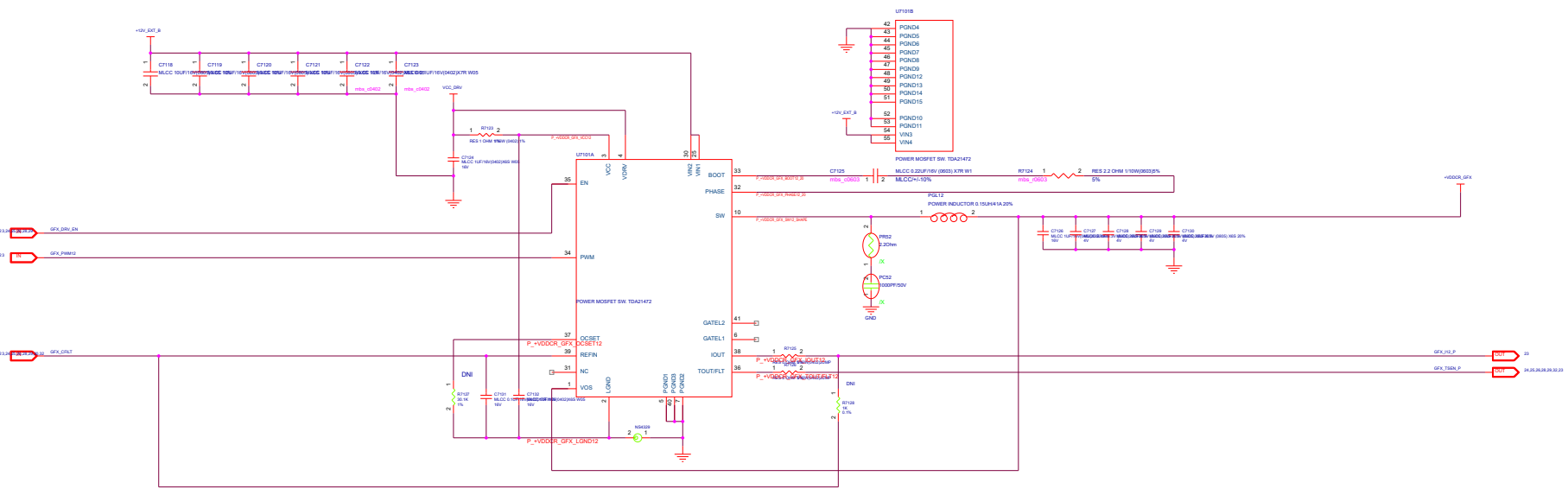
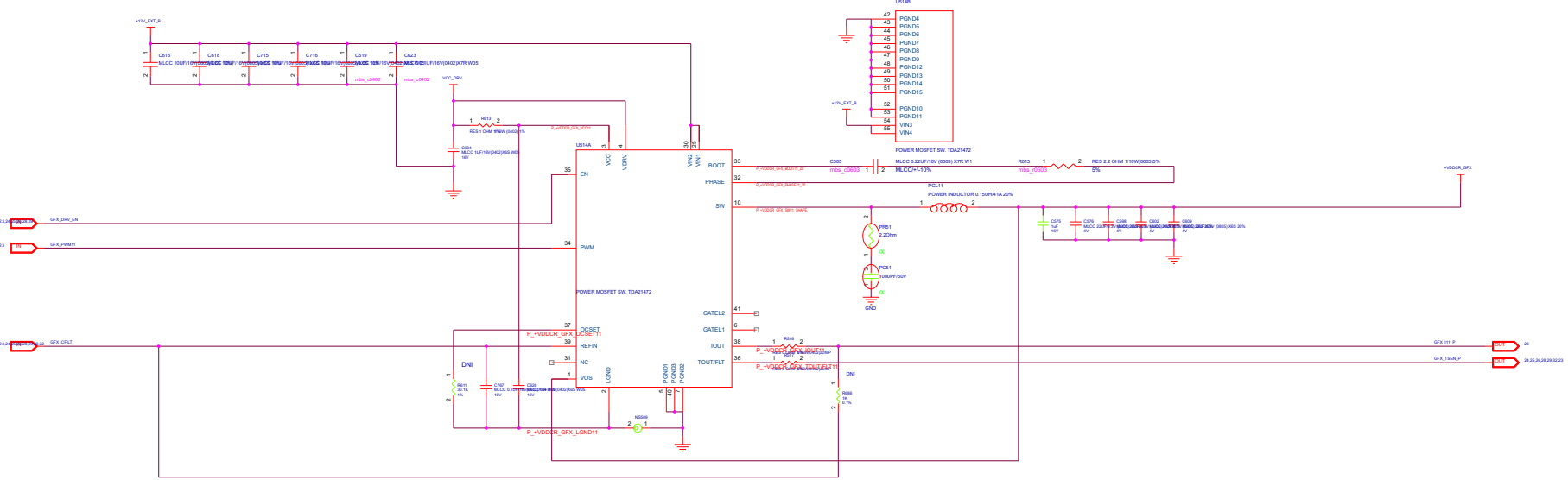
Delete UC1116GC1116GC1113GC1113GC1114
GC1116GC1116GC1117GC1116GC1119

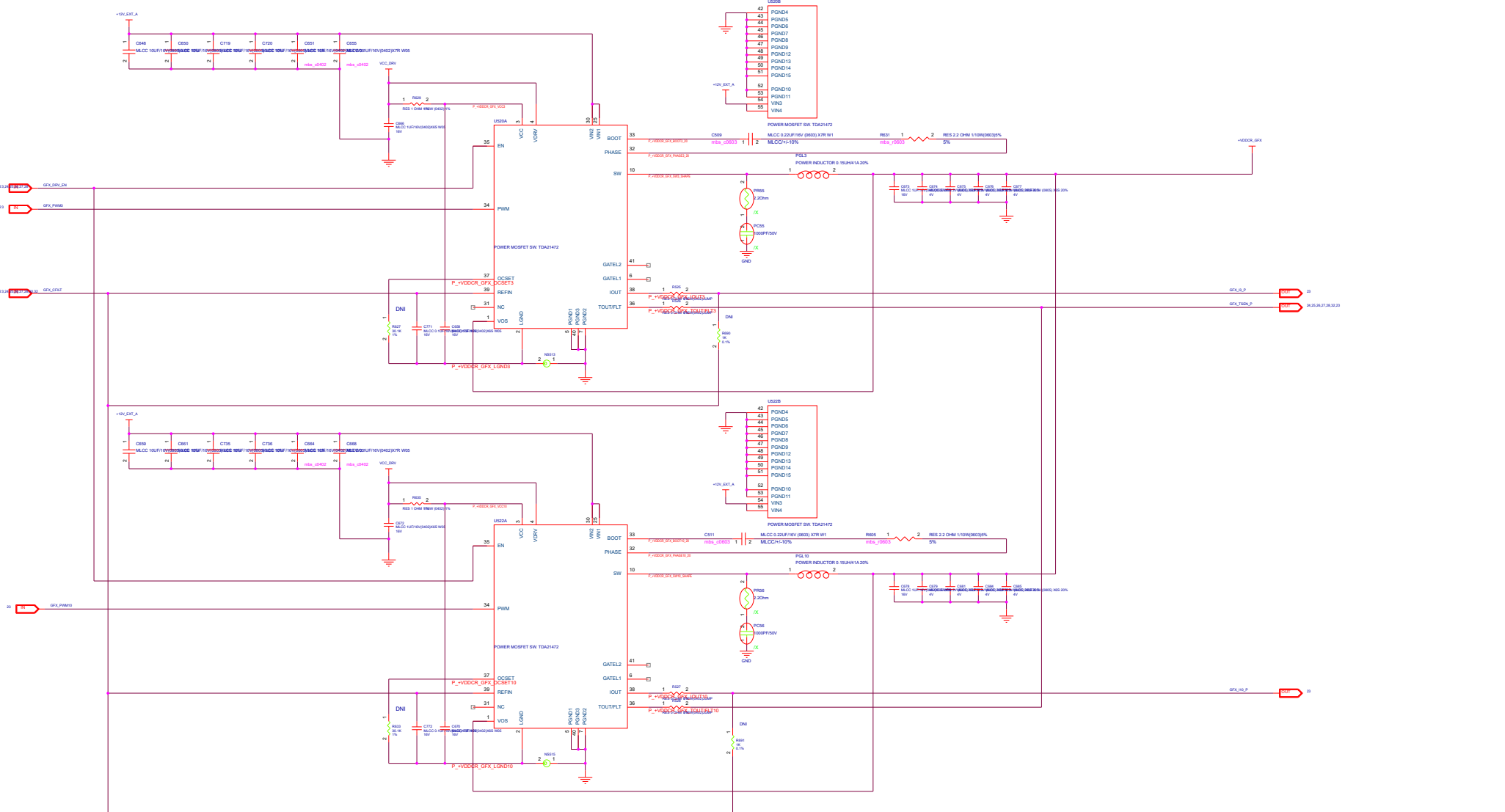


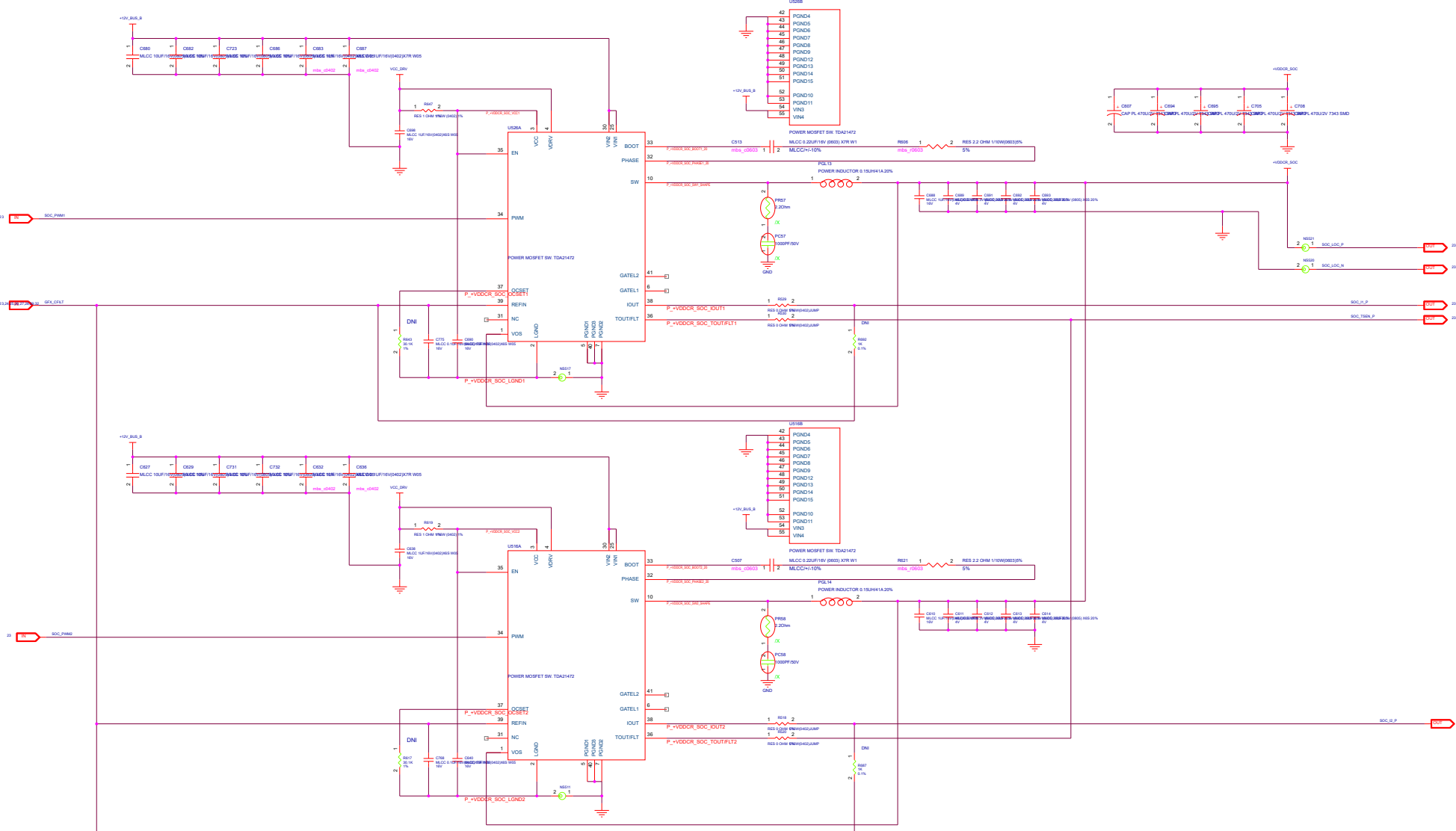
Modify by Scott

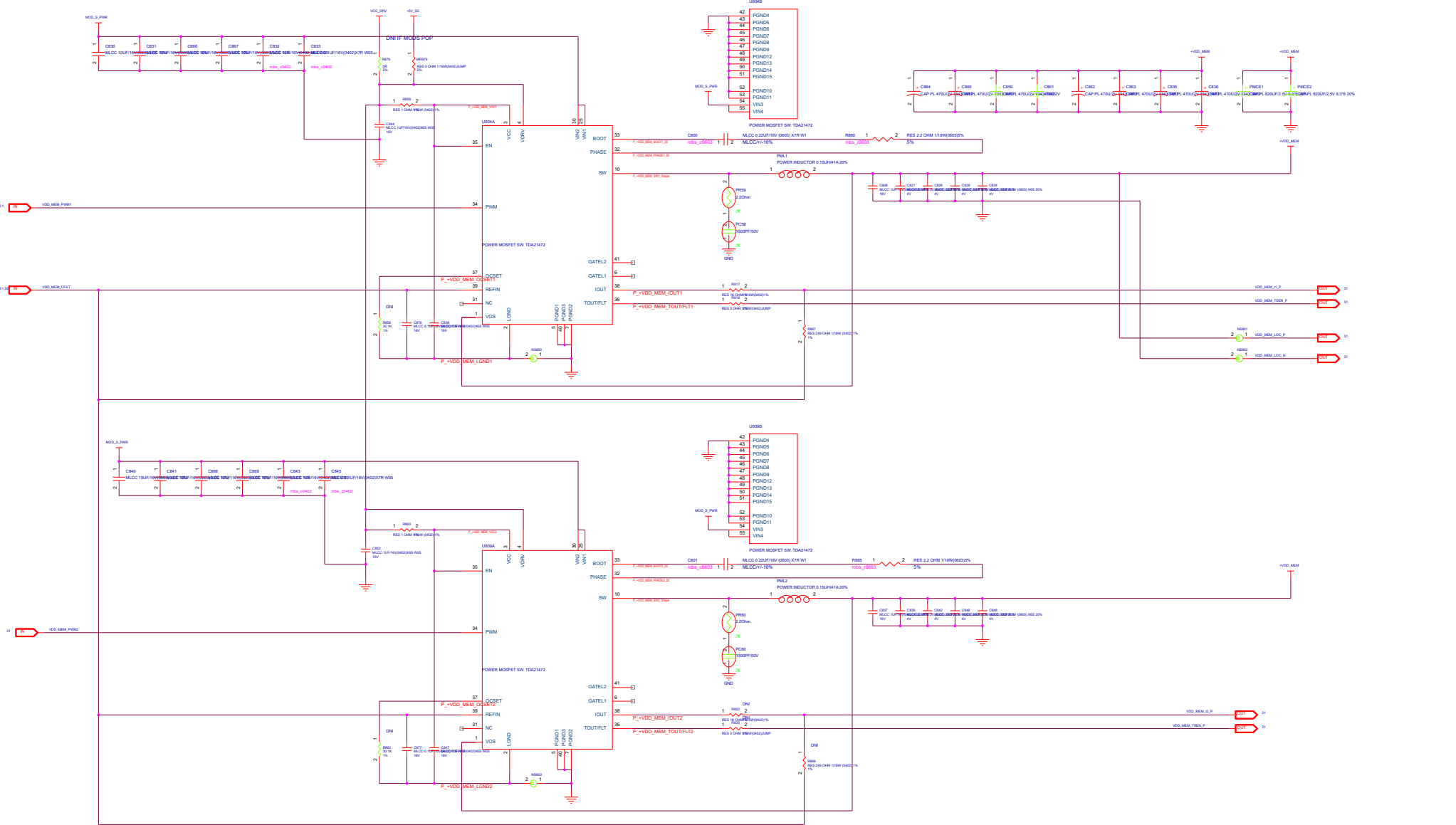
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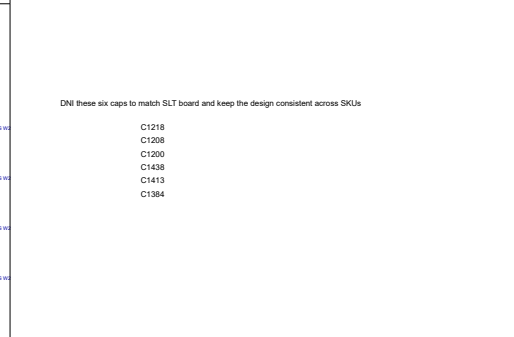
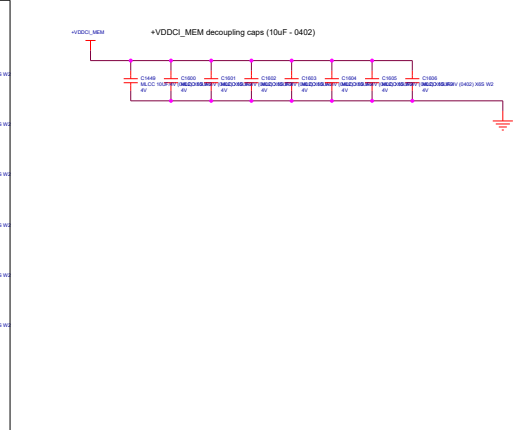
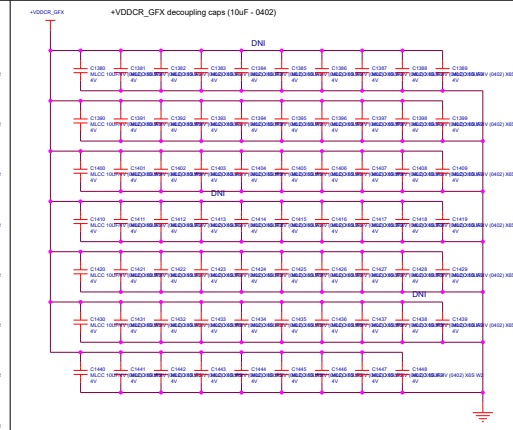






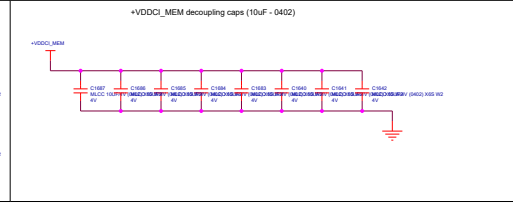
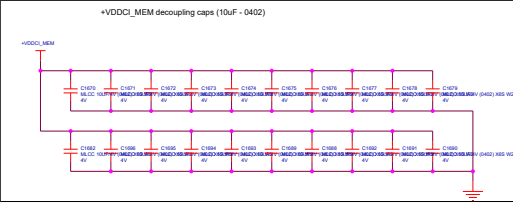
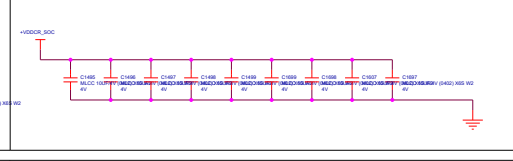
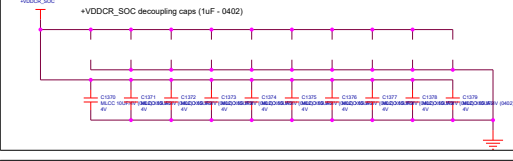
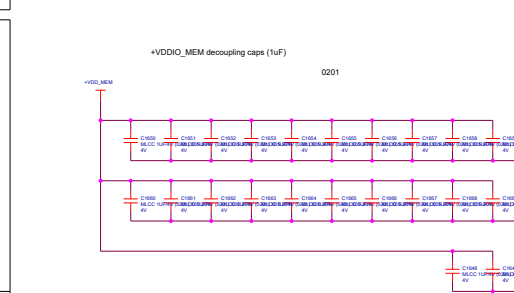
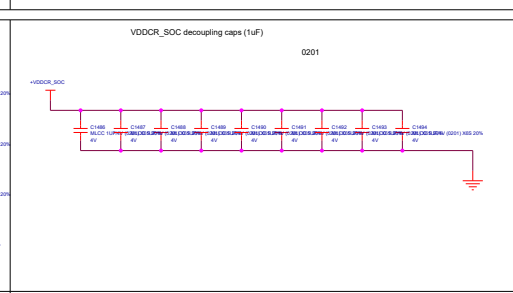
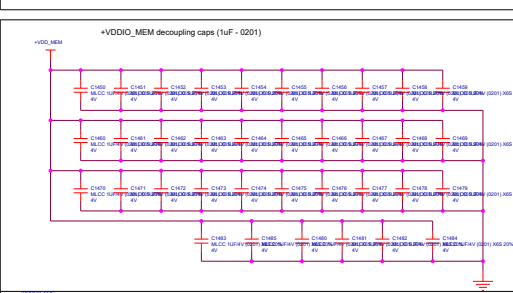


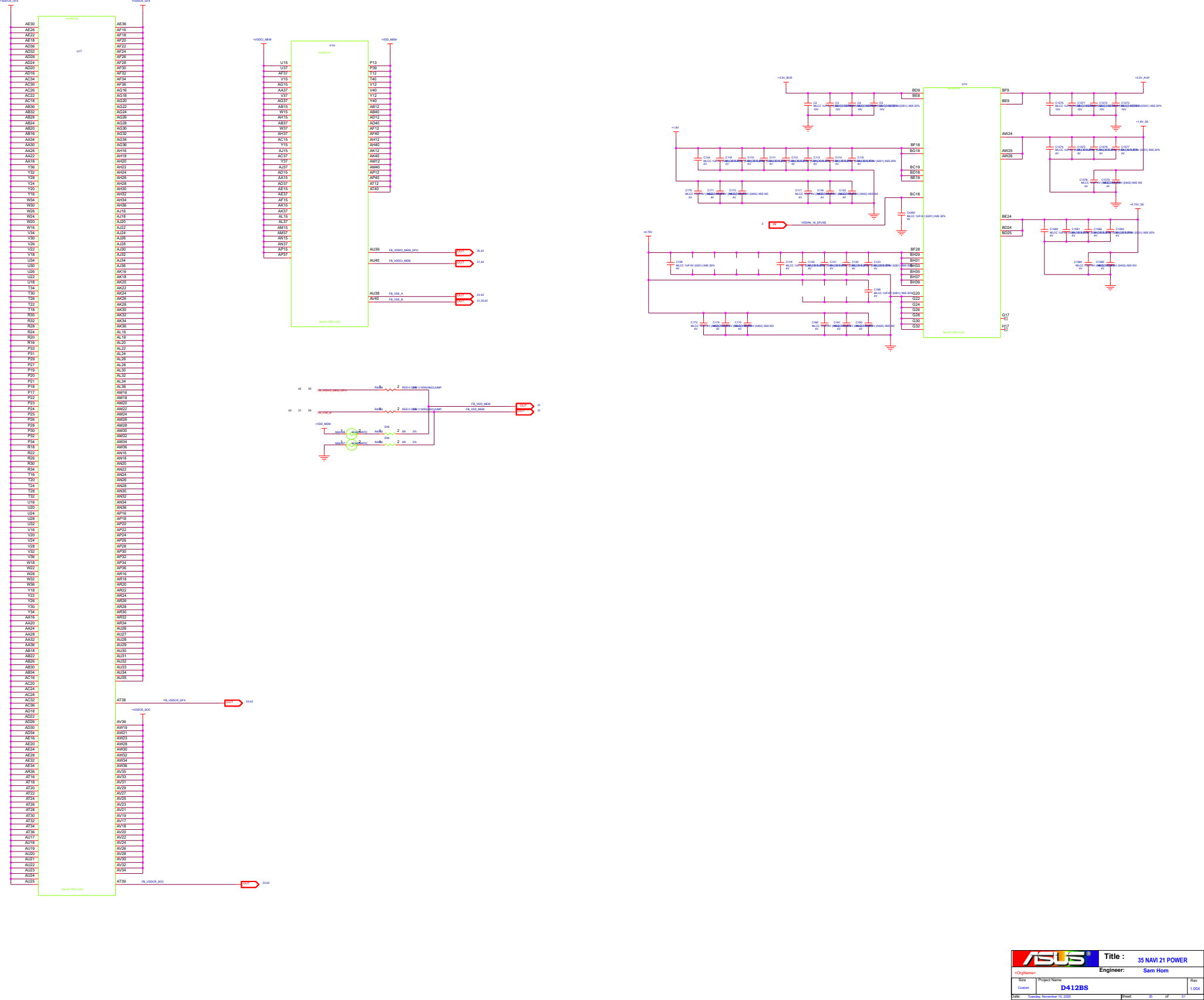




DNI these six caps to match SLT board and keep the design consistent across SKUs

- C1218
- C1208
- C1200
- C1438
- C1413
- C1384





FOR PI DAUGHTER CARD
Modify by Sam
Delete PI DAUGHTER CARD

+3.3V_ModS

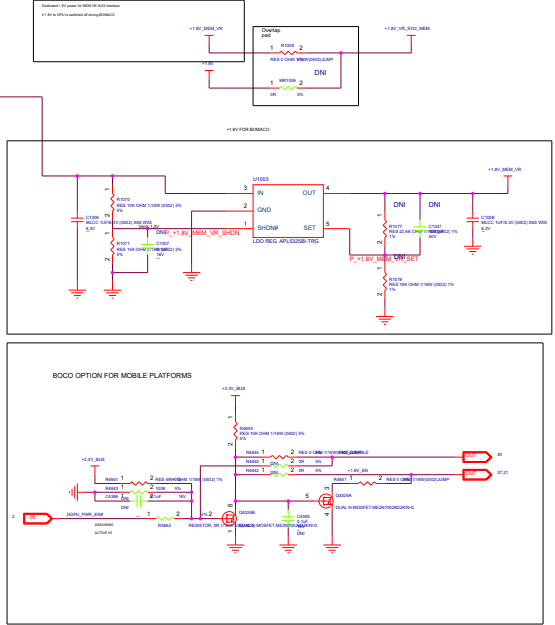
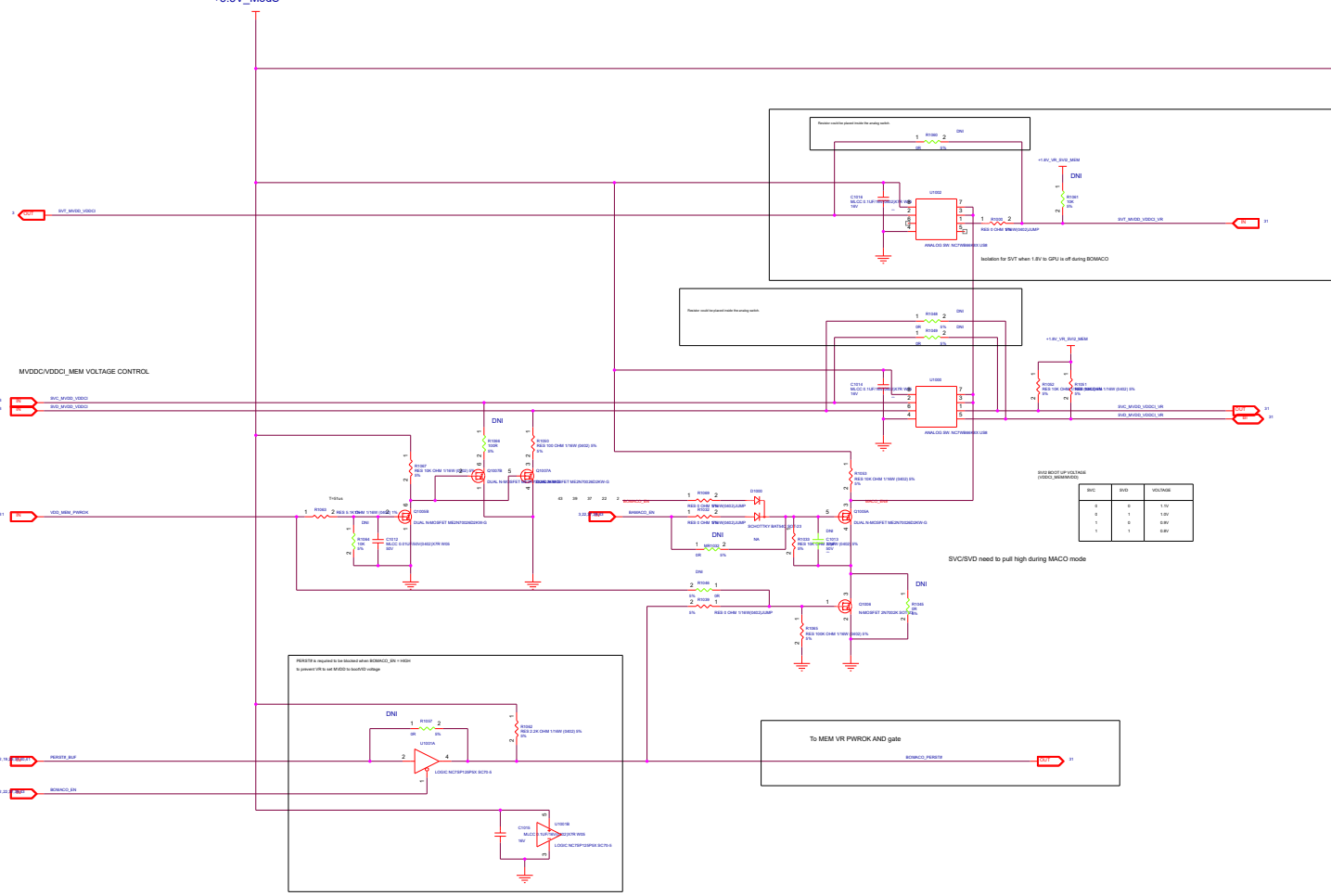


Table 3 Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN * EFUSE	EFUSE	ON
VDDCR_S5	USB	ON

Table 4 Key Signals at Different PM Modes

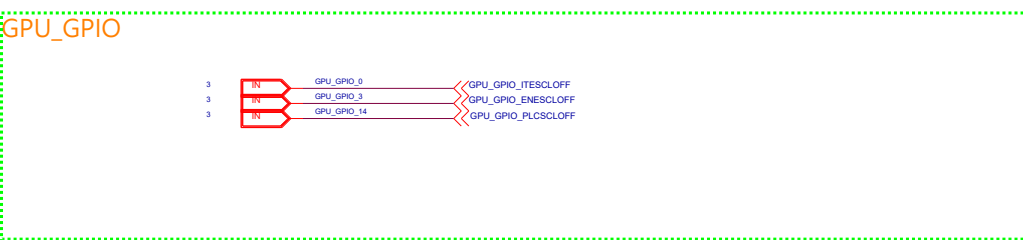
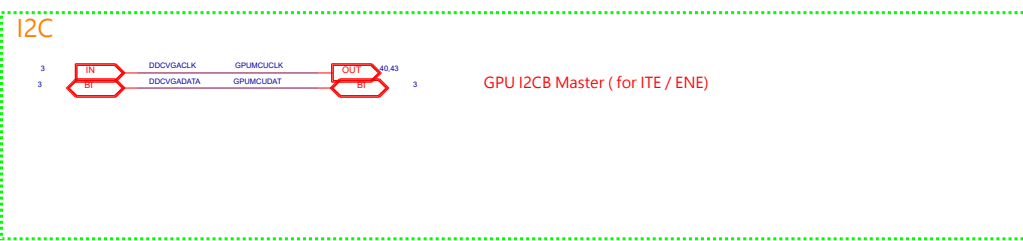
Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERSTb	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

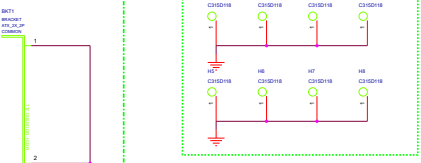
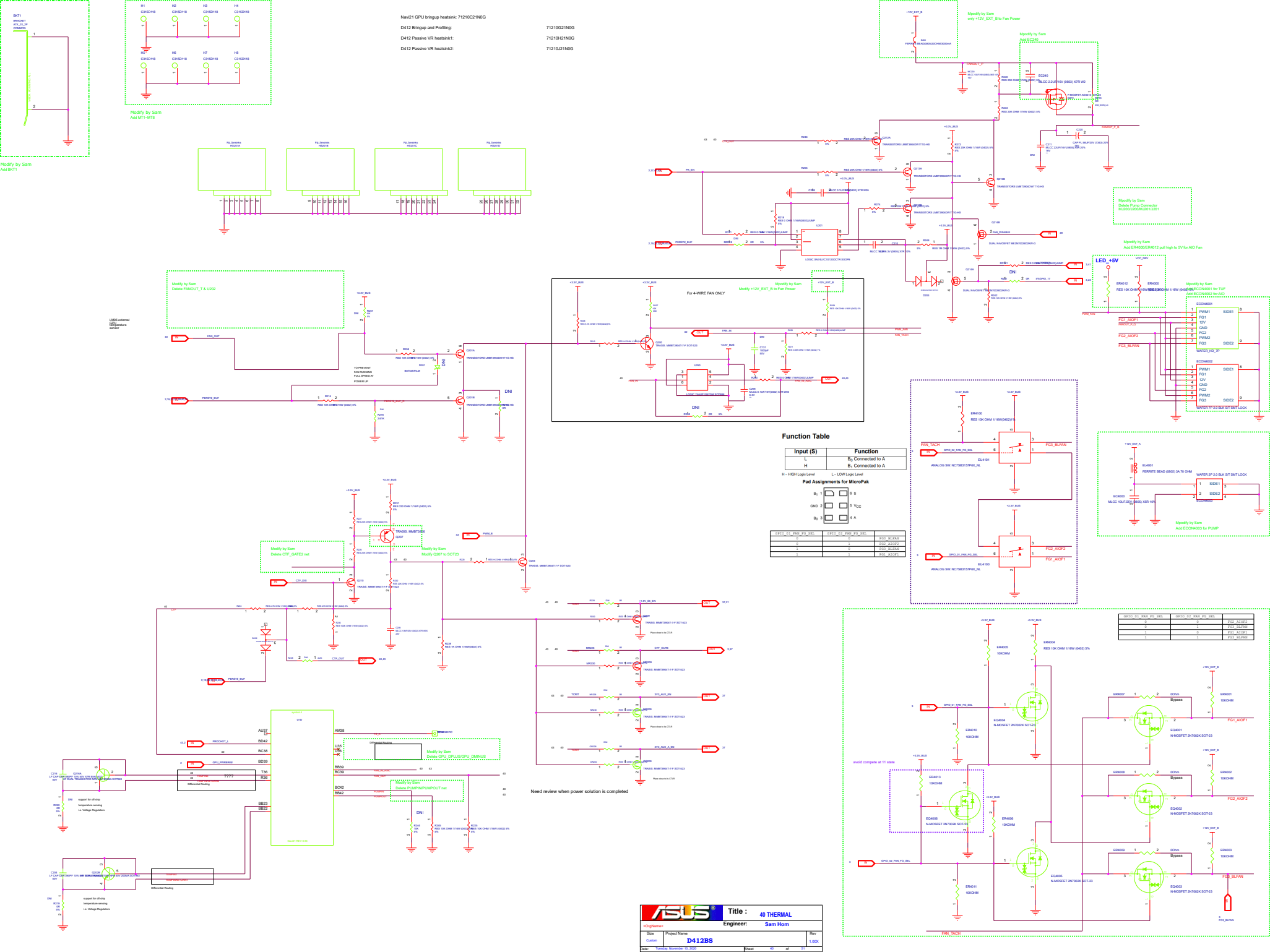
Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

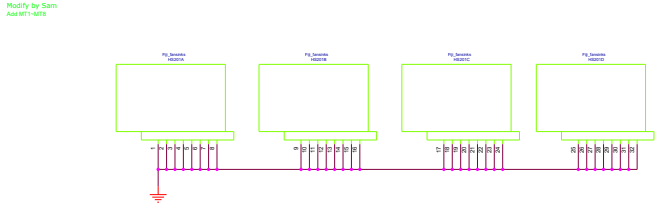
Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN * EFUSE	EFUSE	OFF
VDDCR_S5	USB	ON

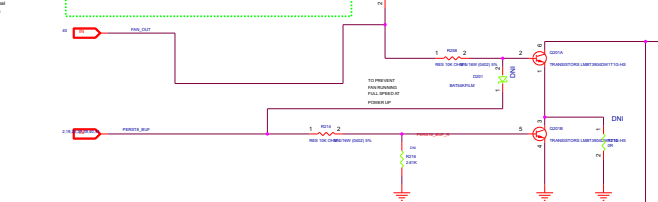




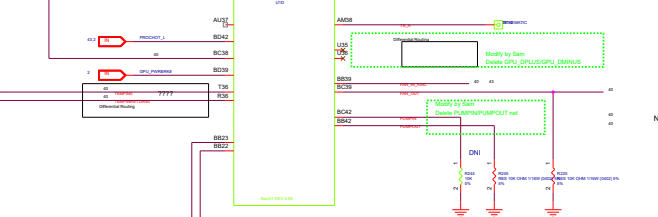
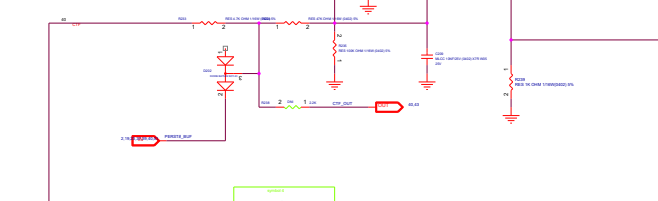
Modify by Sam
Add R117



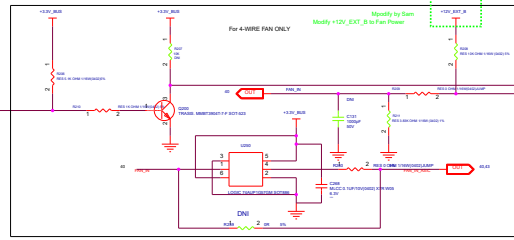
Modify by Sam
Delete FANOUT_1 & U2D2



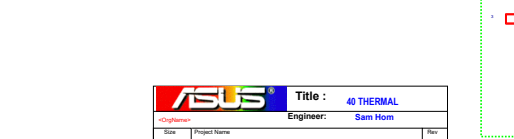
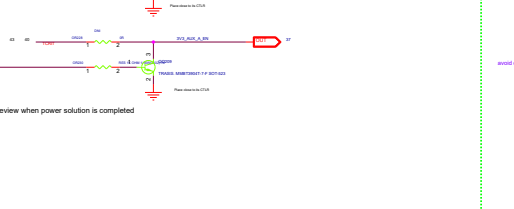
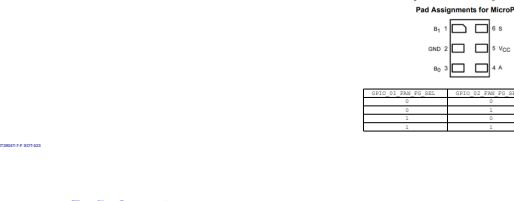
Modify by Sam
Delete C17, GATE2 net



71210021N0G
71210H21N0G
71210L21N0G



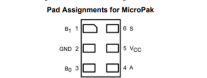
Modify by Sam
Modify +12V_EXT_B to Fan Power



Function Table

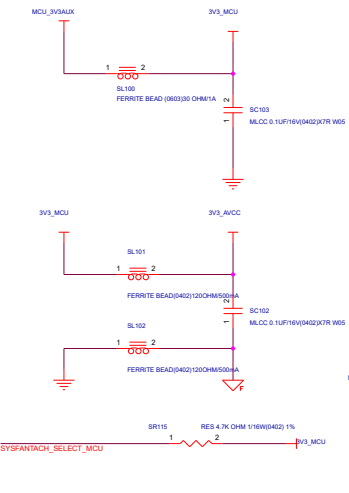
Input (S)	Function
L	B ₁ Connected to A
H	B ₂ Connected to A

H: HIGH Logic Level L: LOW Logic Level

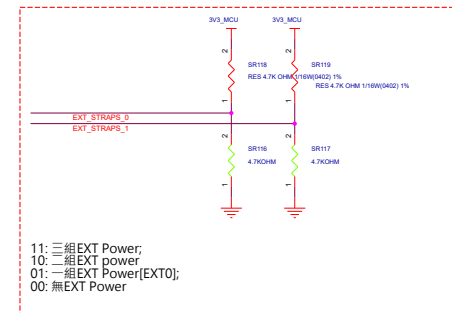
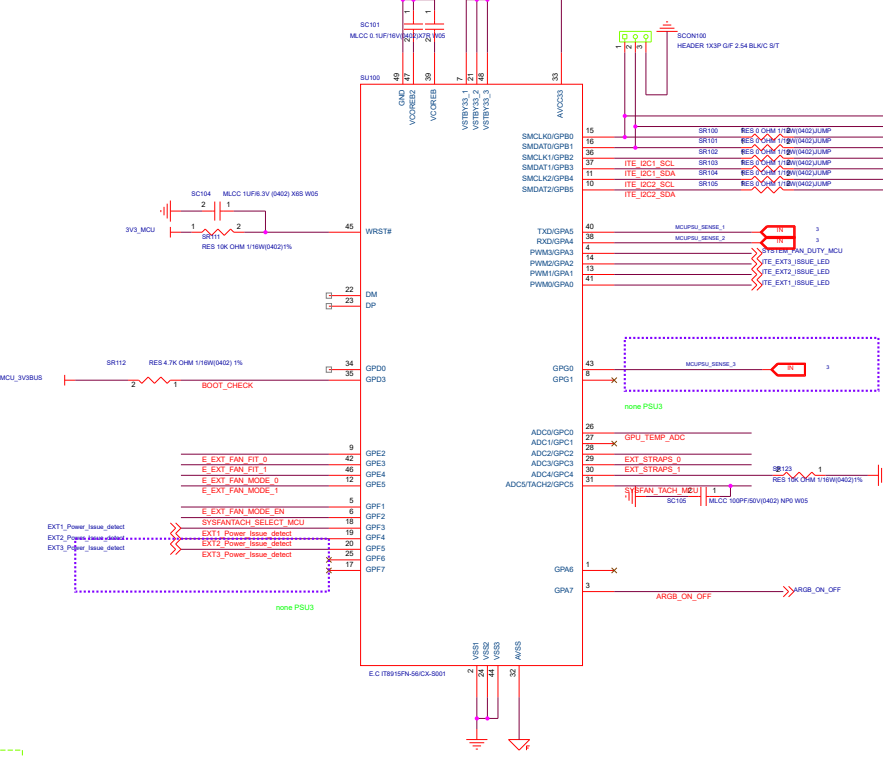


SPIC1_01	SPIC1_02	SPIC1_03	SPIC1_04	SPIC1_05	SPIC1_06	SPIC1_07	SPIC1_08	SPIC1_09	SPIC1_10
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

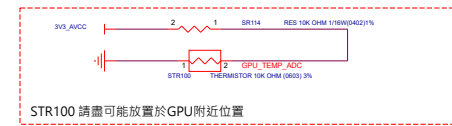
Need review when power solution is completed



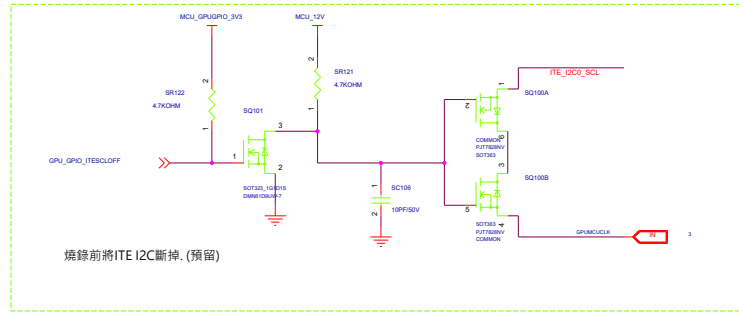
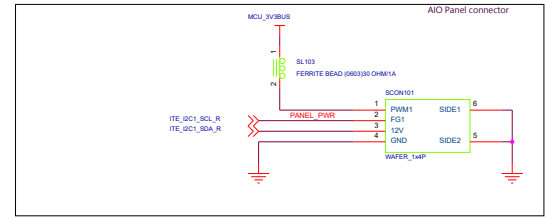
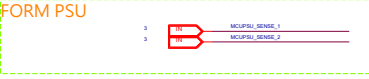
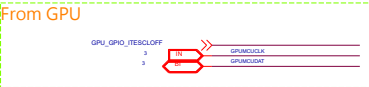
PSU DETECT



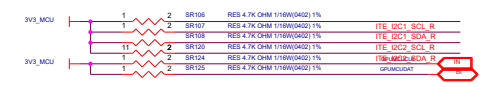
11: 二組EXT Power;
10: 一組EXT power;
01: 一組EXT Power[EXT0];
00: 無EXT Power



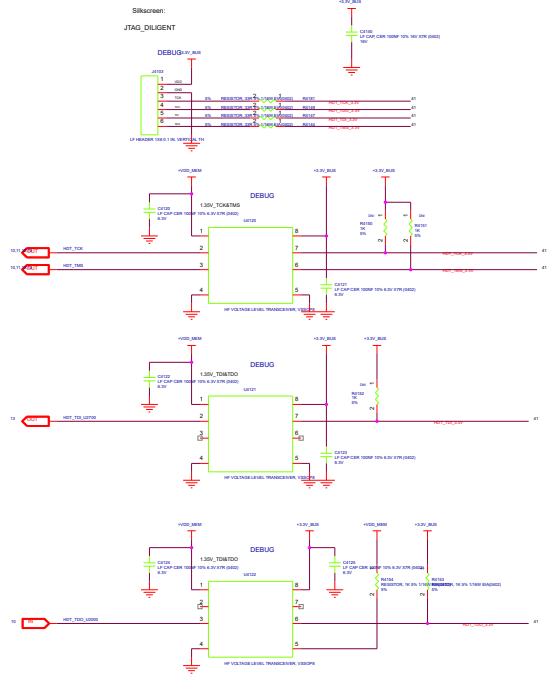
STR100 請盡可能放置於GPU附近位置



燒錄前將ITE I2C斷掉 (預留)

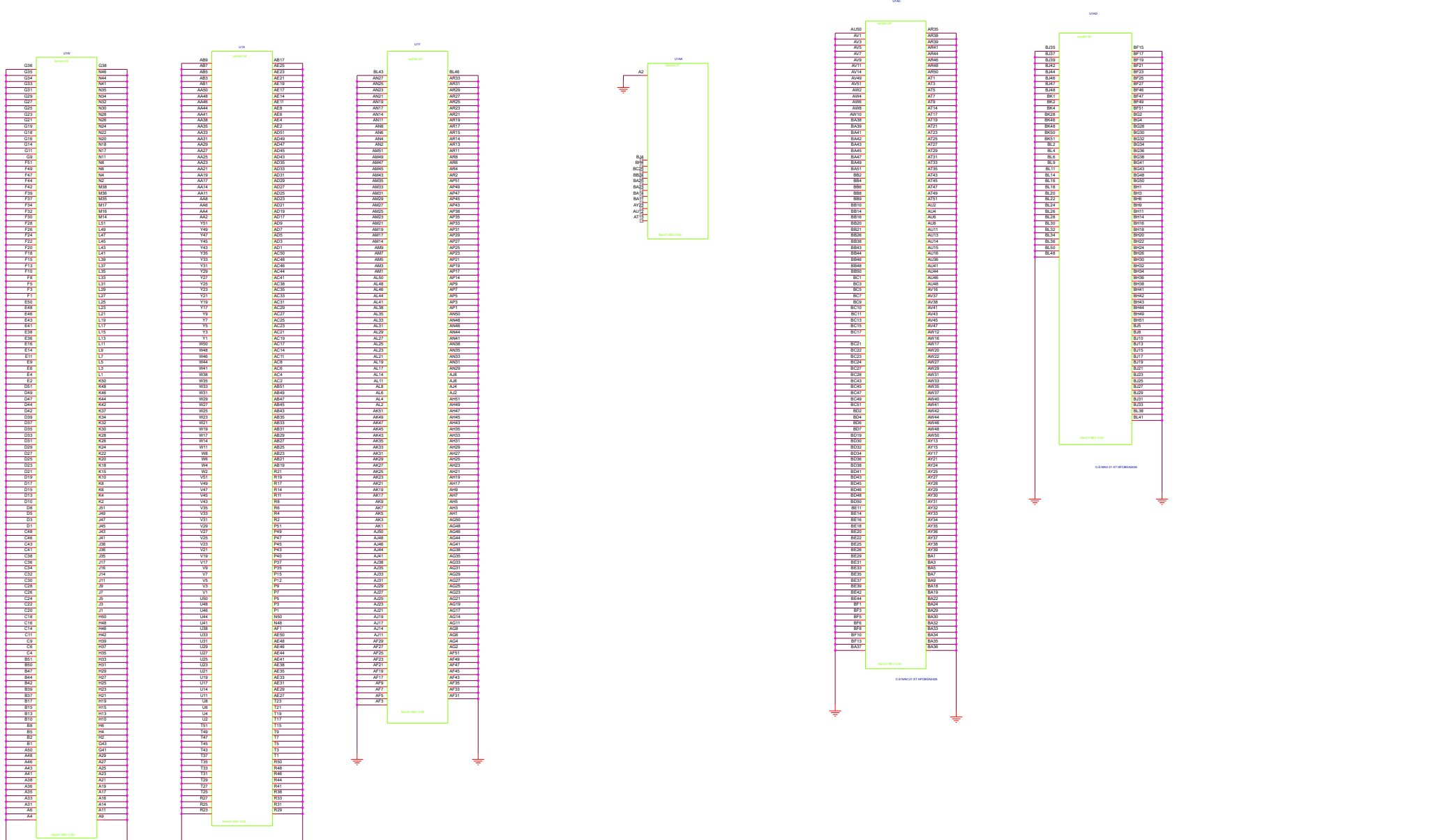


SIRACORN:
JTAG_DILIGENT



Modify by Sam
Delete DPM LED

Modify by Sam
Delete TSM LED Header
Delete RACEDON Lightbar Header



SWITCHES

Modify by Team
 Design 202406 10:11 AM
 Design 202406 10:11 AM

Yellow LED shows VFWICT

Modify by Team
 Design 202407 14:07

Adjustable Fan

Modify by Team
 Design Power Quality Hardware

PCC LED

Modify by Team
 Design PCC LED

LED RED ON indicates Fault

Modify by Team
 Design 2024 12:02
 Design 2024 12:02
 Design 202407 14:07
 Design 202407 14:07

Modify by Team
 Design 2024

ENM4103 by DAT TMON is Provide CAL AND OFFSET

Modify by Team
 Design 2024 12:02 is Provide CAL AND OFFSET

7-BIT I2C ADDRESS: 0x7C

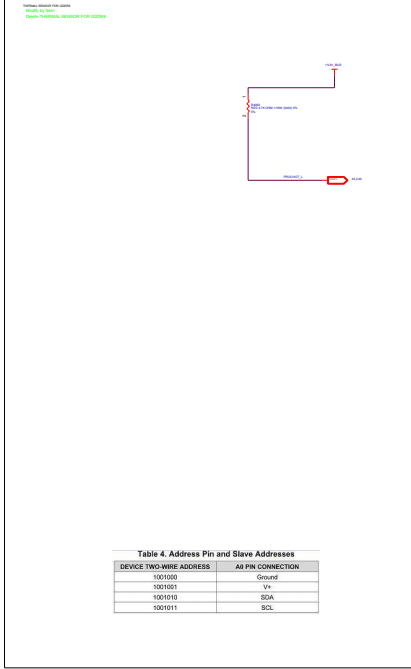
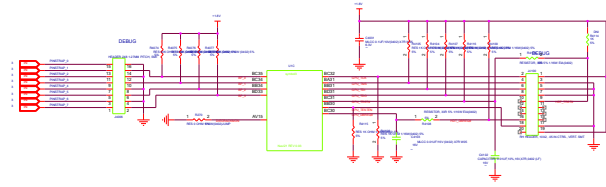


Table 4. Address Pin and Slave Addresses

DEVICE TWO WIRE ADDRESS	AI0 PIN CONNECTION
1001000	Ground
1001001	V _{CC}
1001010	SDA
1001011	SCL



Modify by Team
 Design Thermal_Sensor_VFW_VDDIO

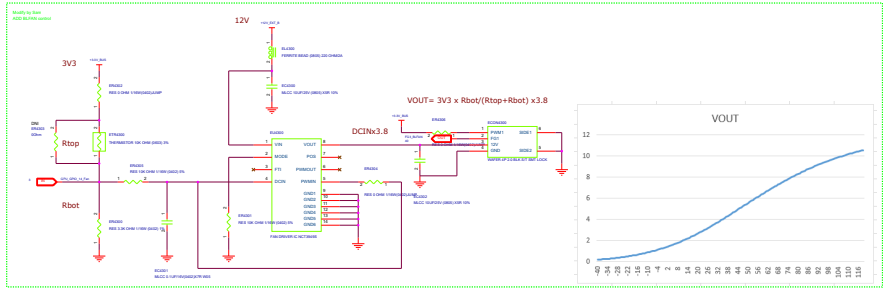
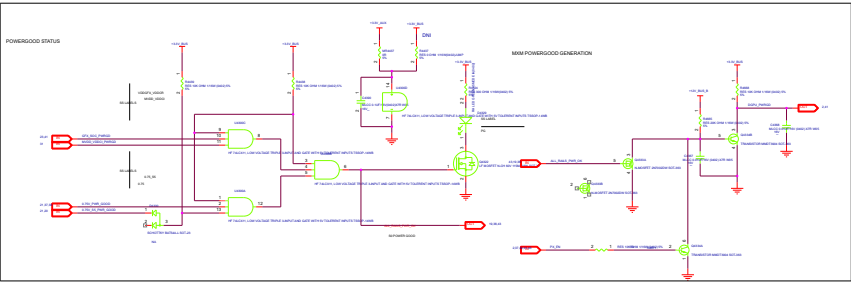
Thermal_Sensor_VFW_VDDIO

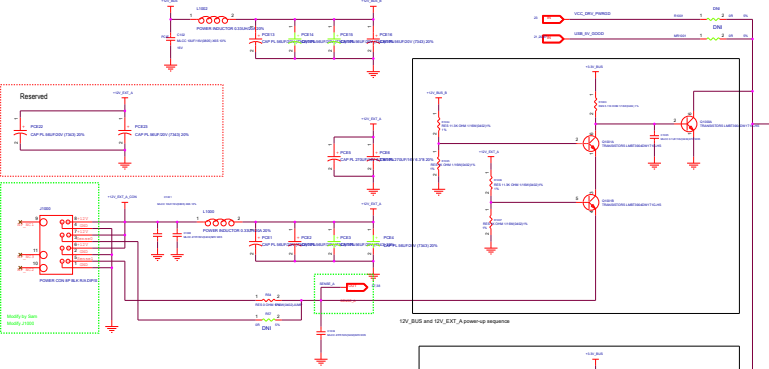
not an available pin

Modify by Team
 Design Thermal_Sensor_VFW_VDDIO

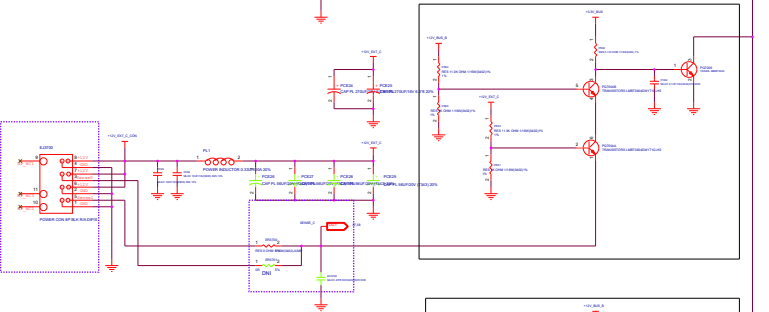
Thermal_Sensor_VFW_VDDIO

not an available pin

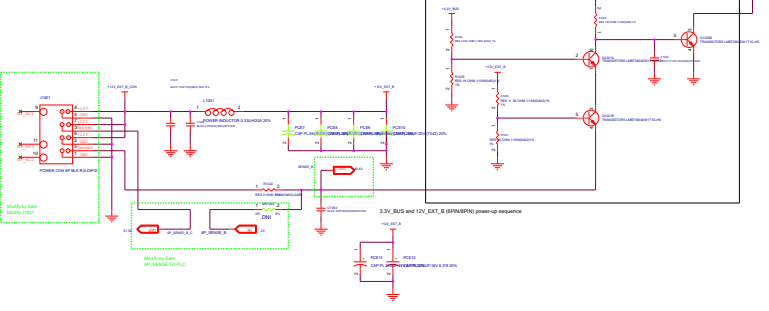




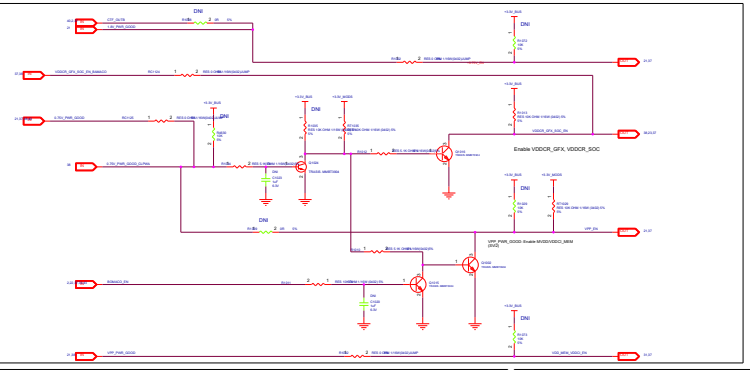
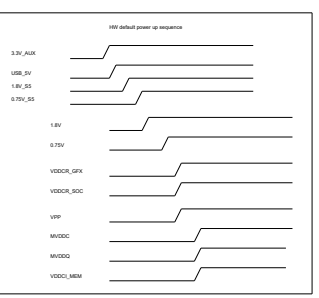
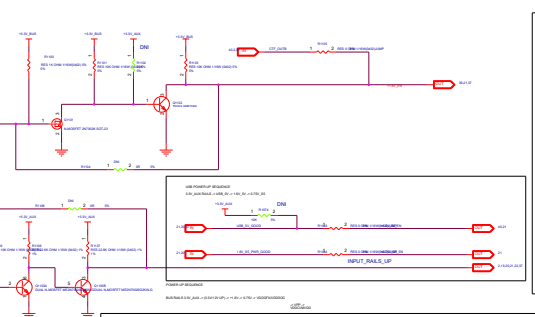
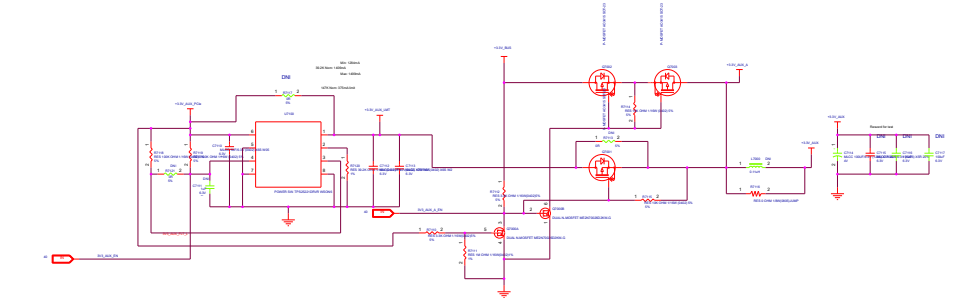
12V_AUX and 12V_EXT_A power-up sequence



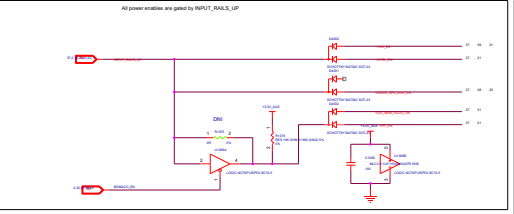
12V_AUX and 12V_EXT_B (OPINPIN) power-up sequence



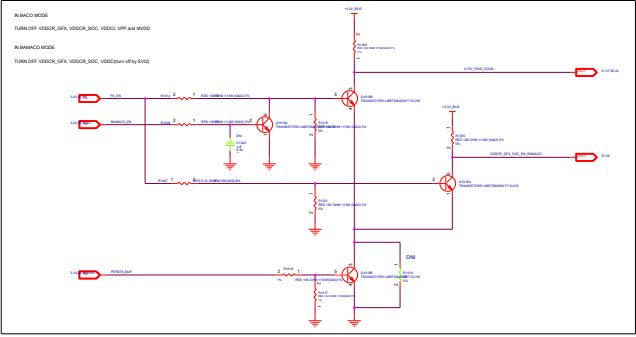
3.3V_AUX and 12V_EXT_B (OPINPIN) power-up sequence



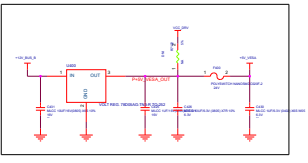
Enable VDDCR_GFX, VDDCR_SOC



All power enables are gated by INPUT_PMA5_LUP



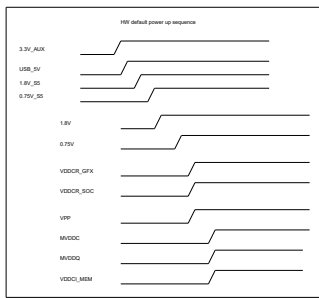
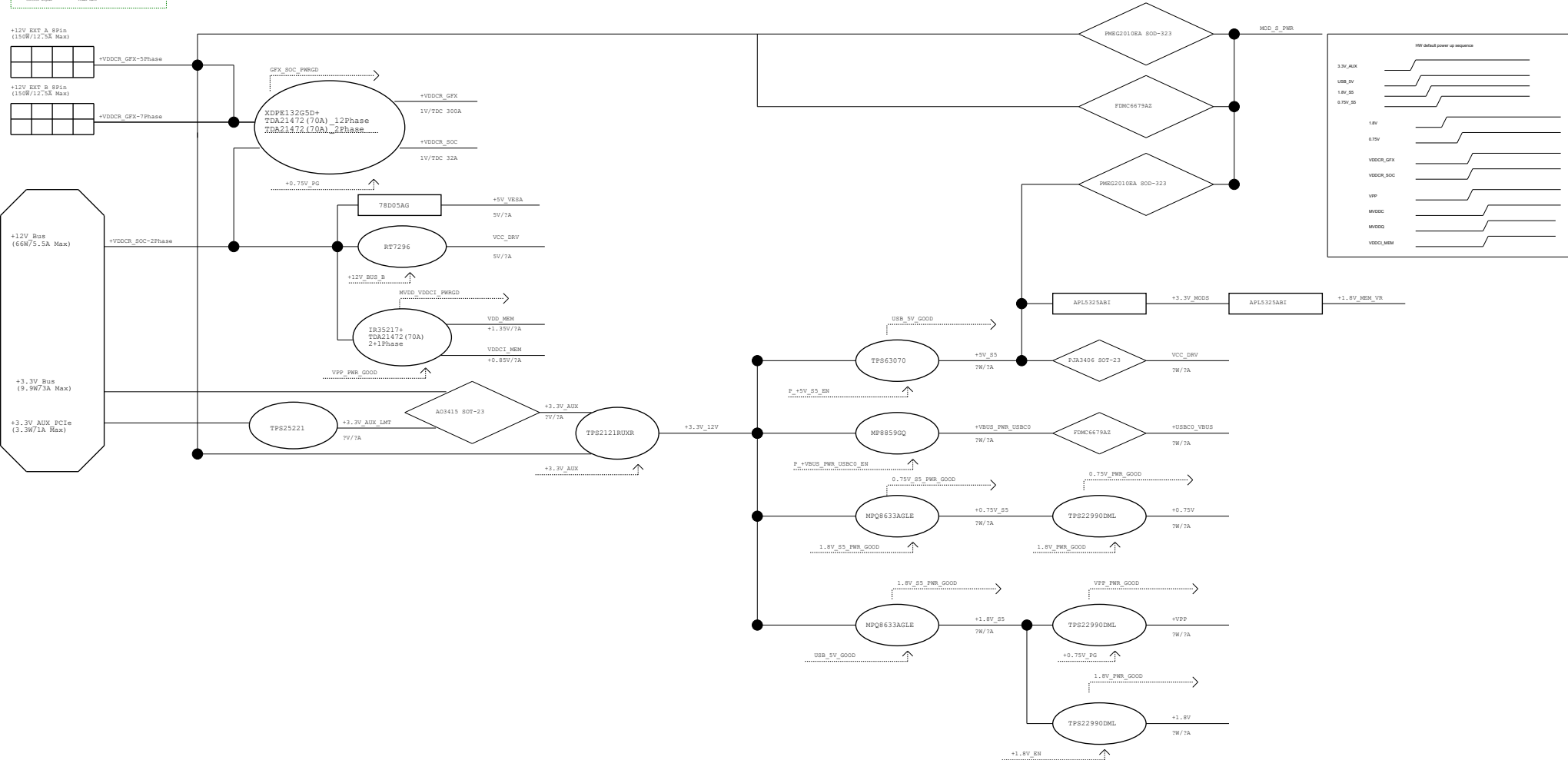
In SWD0 MODE
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCR_VPP and MVDCC
In SWDCC MODE
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCR_VPP only (VPP)

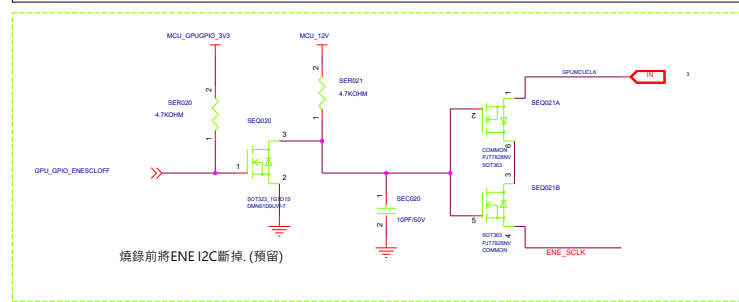
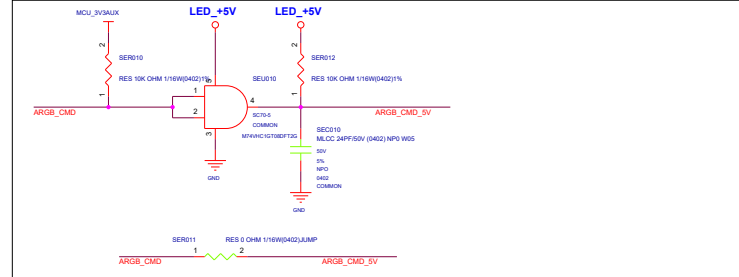
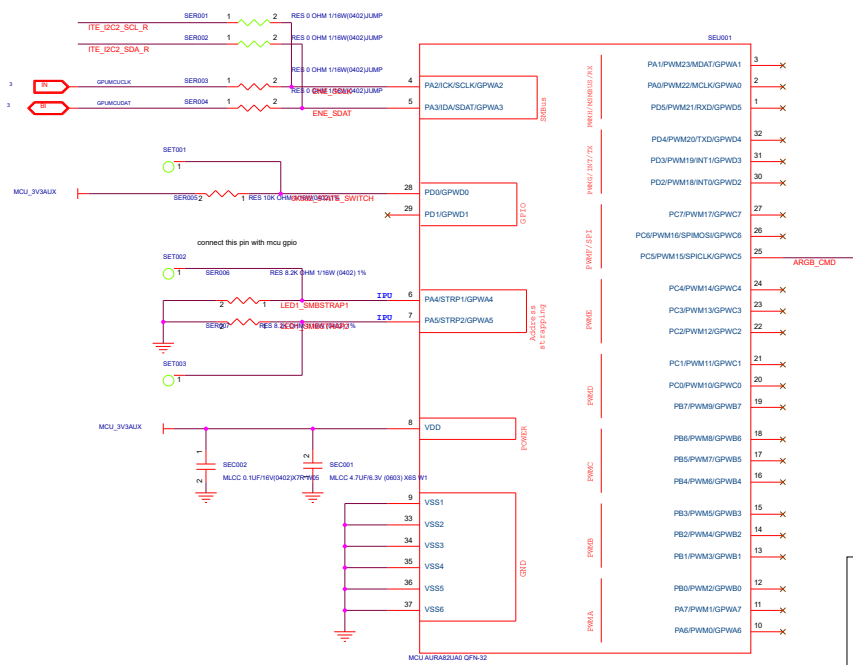


1	40B	06/17/18	Added MODE control
1	40C	06/21/18	Commented U1_PU_50 to OSC_VDD18 Global voltage_pins_028629 by 6241-05629 user protection removed

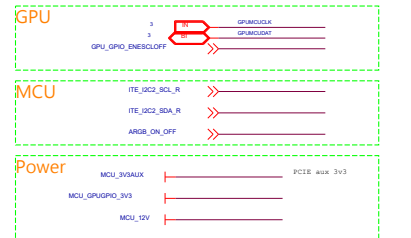
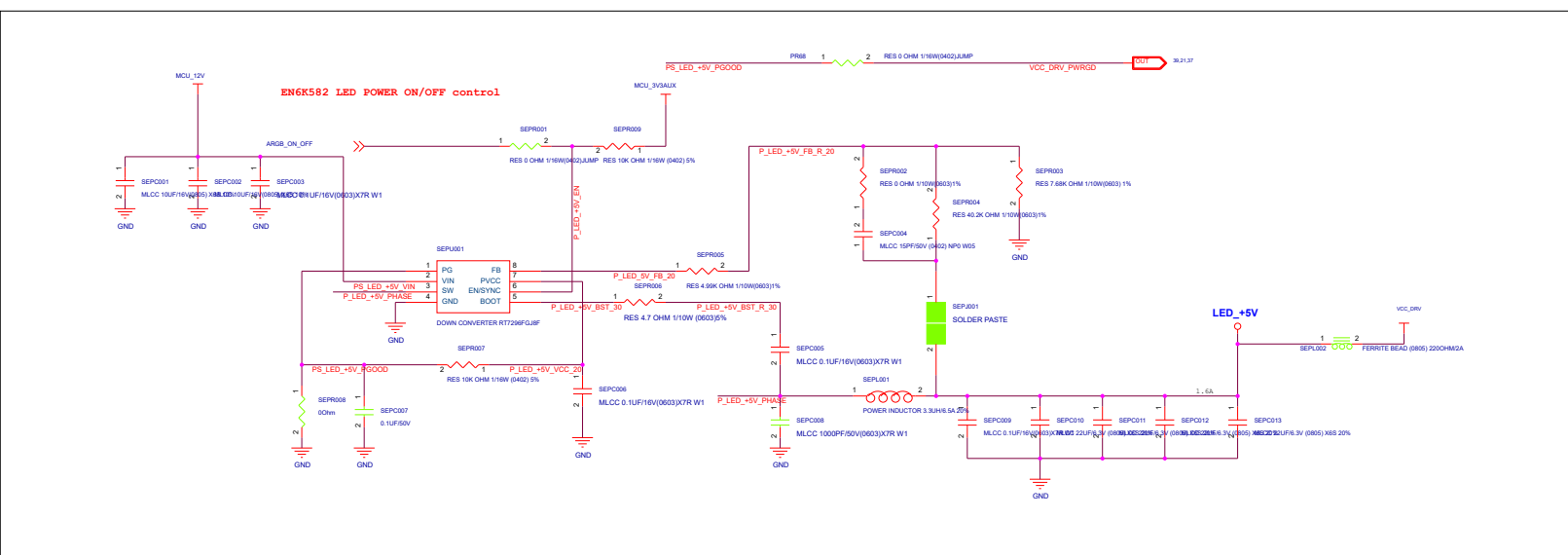
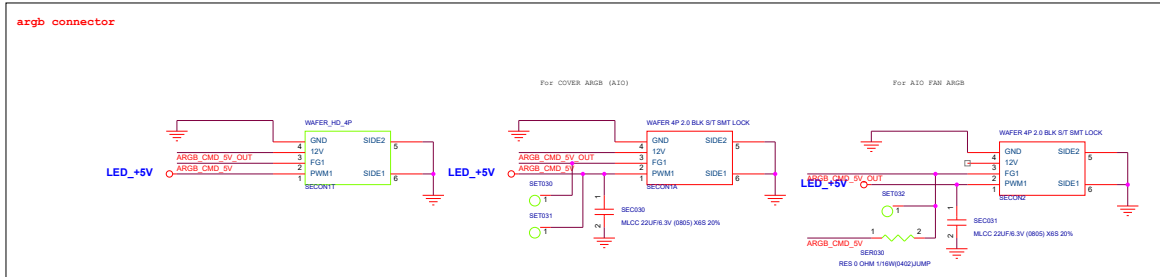
		Title : 44 History	
Engineer: Sam Hom			
Project Name	D412BS		Rev: 1.00X
Sheet	44	of	51

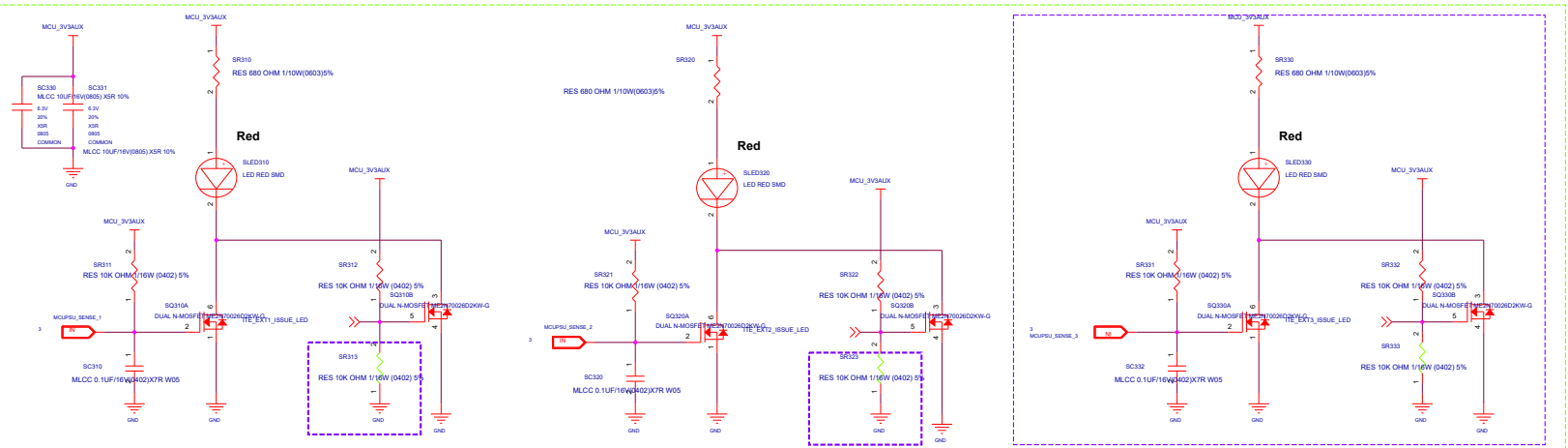
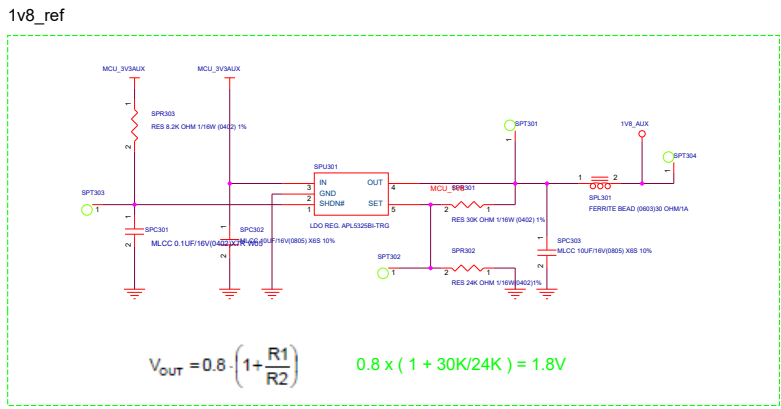
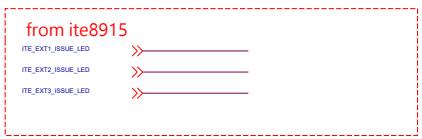
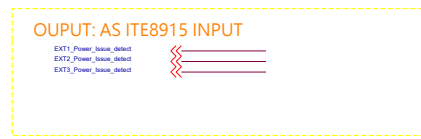
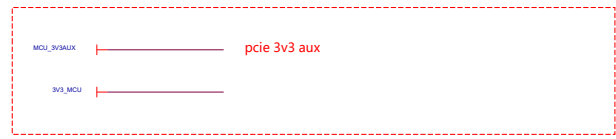
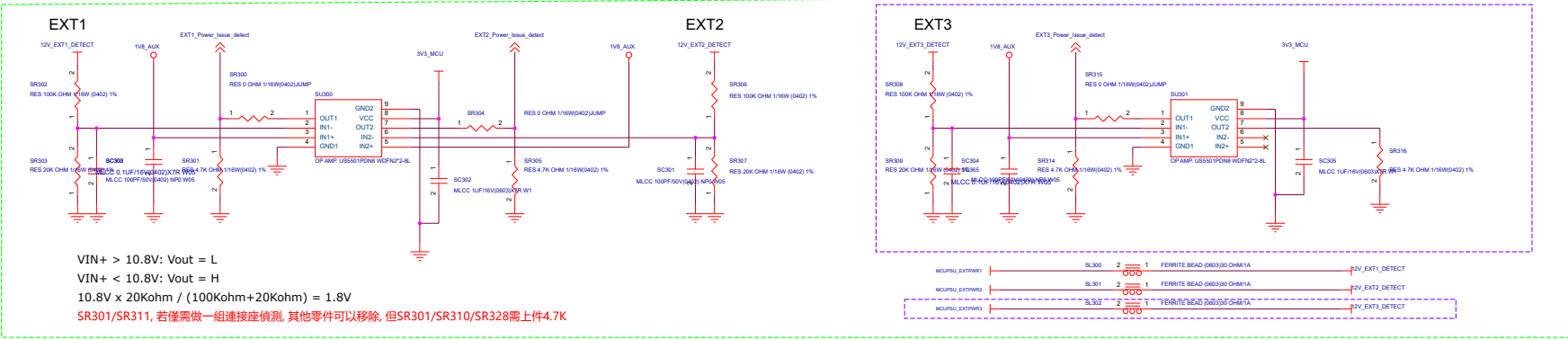
POWER FLOW



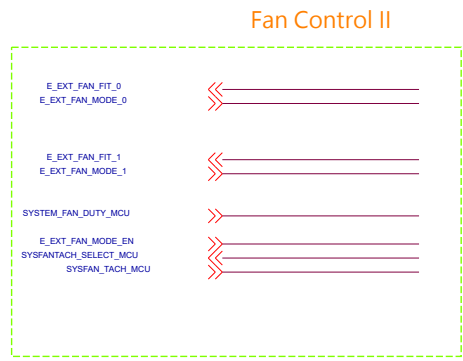
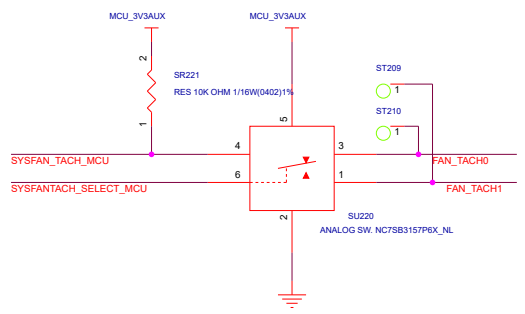
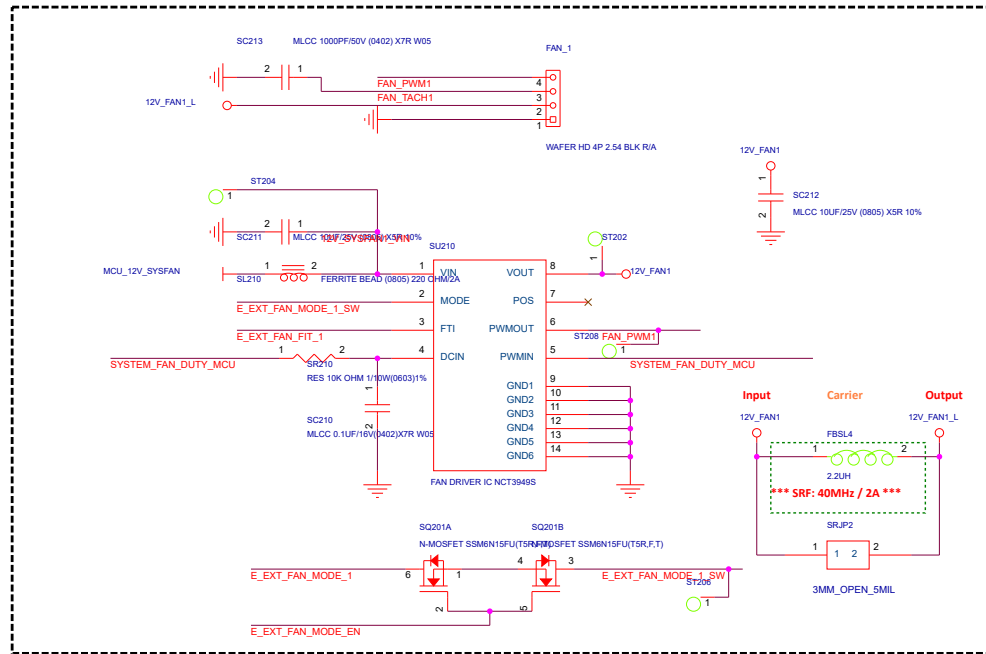
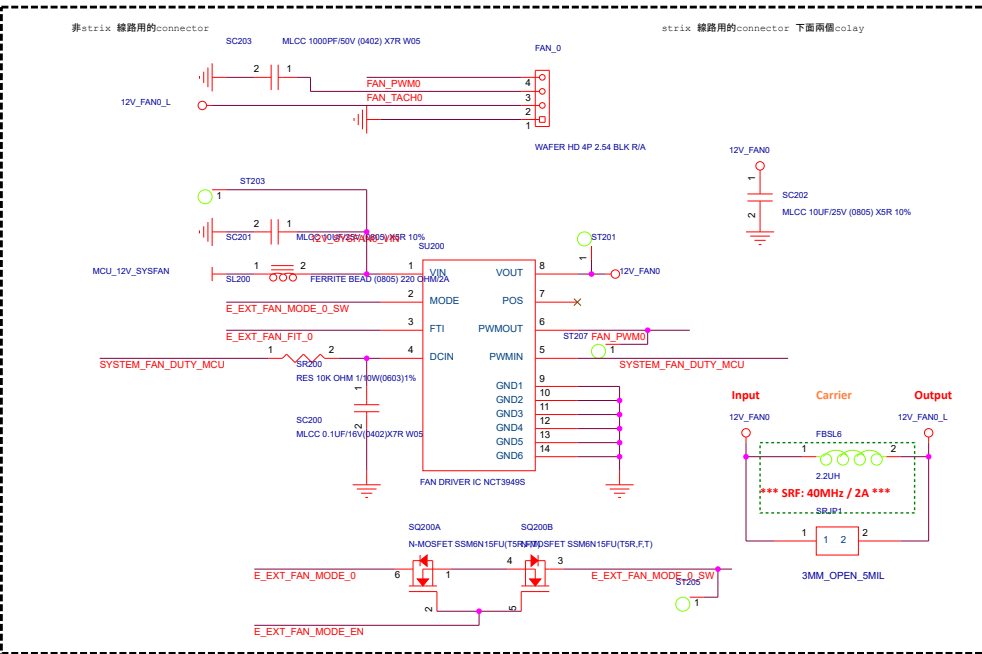


燒錄前將ENE I2C斷掉.(預留)





1.EXT power is not connected, the led is always on
 2.EXT power is connected
 EXT 12v is over 10.8V, the led turns off
 EXT 12v is below 10.8v,the led blink



ASUS VGA PCB Logo

LOG01
CE
CE



LOG08
UKRAINE
UKRAINE



LOG02
VCCI
VCCI



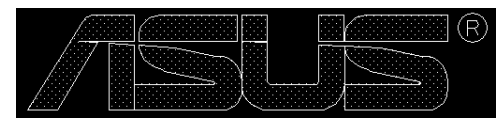
LOG09
PCB MADE IN CHINA
PCB_MADE_IN_CHINA



LOG03
EMI_D33005_H
EMI_D33005_H



LOG10
MARK_L
S_MARK_L



LOG04
FCC
FCC

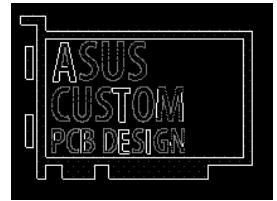


LOG011
WEEE_LOGO
WEEE_LOGO



ASUS Re-design logo
Do not place this on reference board

LOG013
ASUS
CUSTOM
PCB DESIGN
ASUS_CUSTOM_PCB



LOG05
RCM
RCM



LOG06
CAN ICES-3 (B)/NMB-3(B)
CAN_ICES_3B_NMB_3B



LOG012
SFIS
SFIS



LOG07
KC_R_R_LOGO
KC_R_R_LOGO



M1
PCB_RULER_ASUS
PCB_RULER_ASUS