

# PG210 B00

## GP107 128b GDDR5, 75W , PCB 5.7" DVI-D\_DL (DP + DP) + HDMI (DP) + DP

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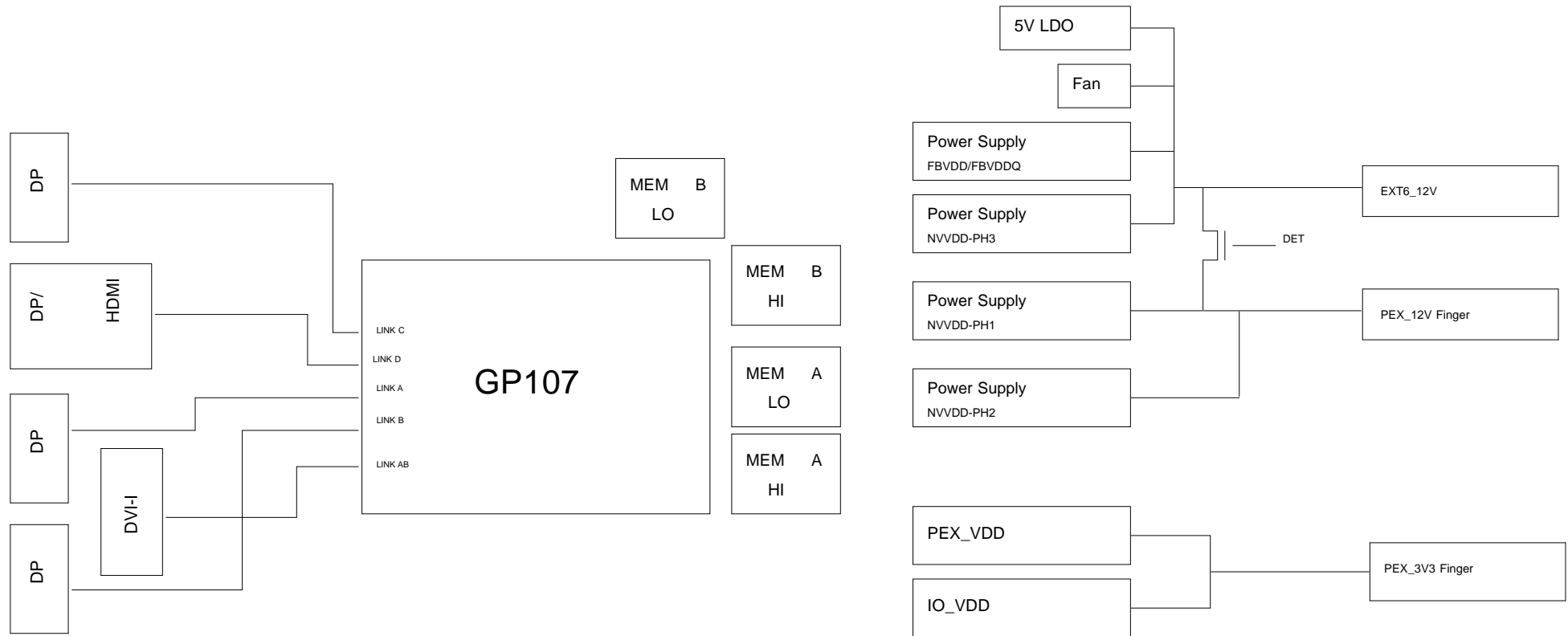
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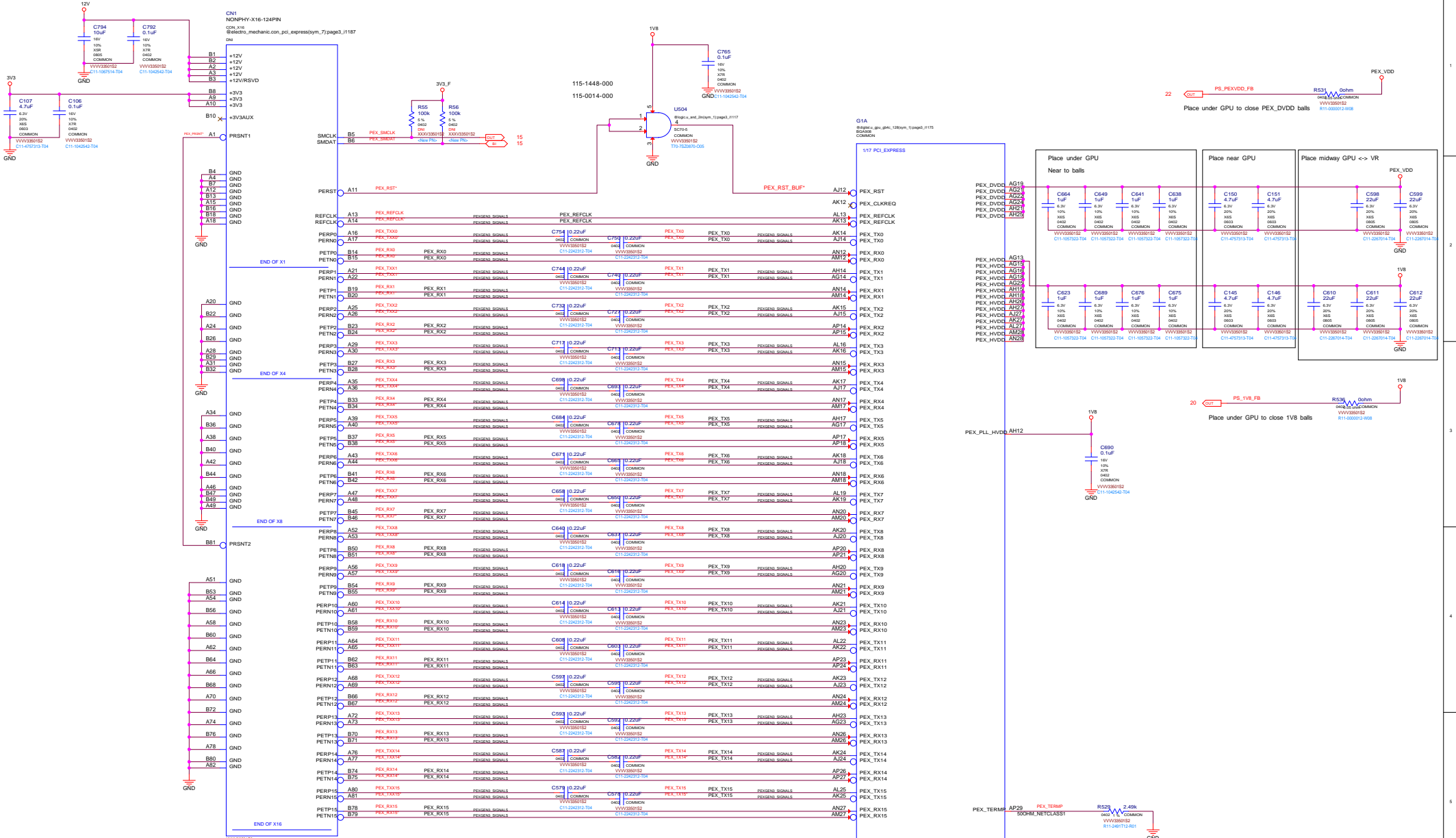
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	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-V335</b>		
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Block Diagram

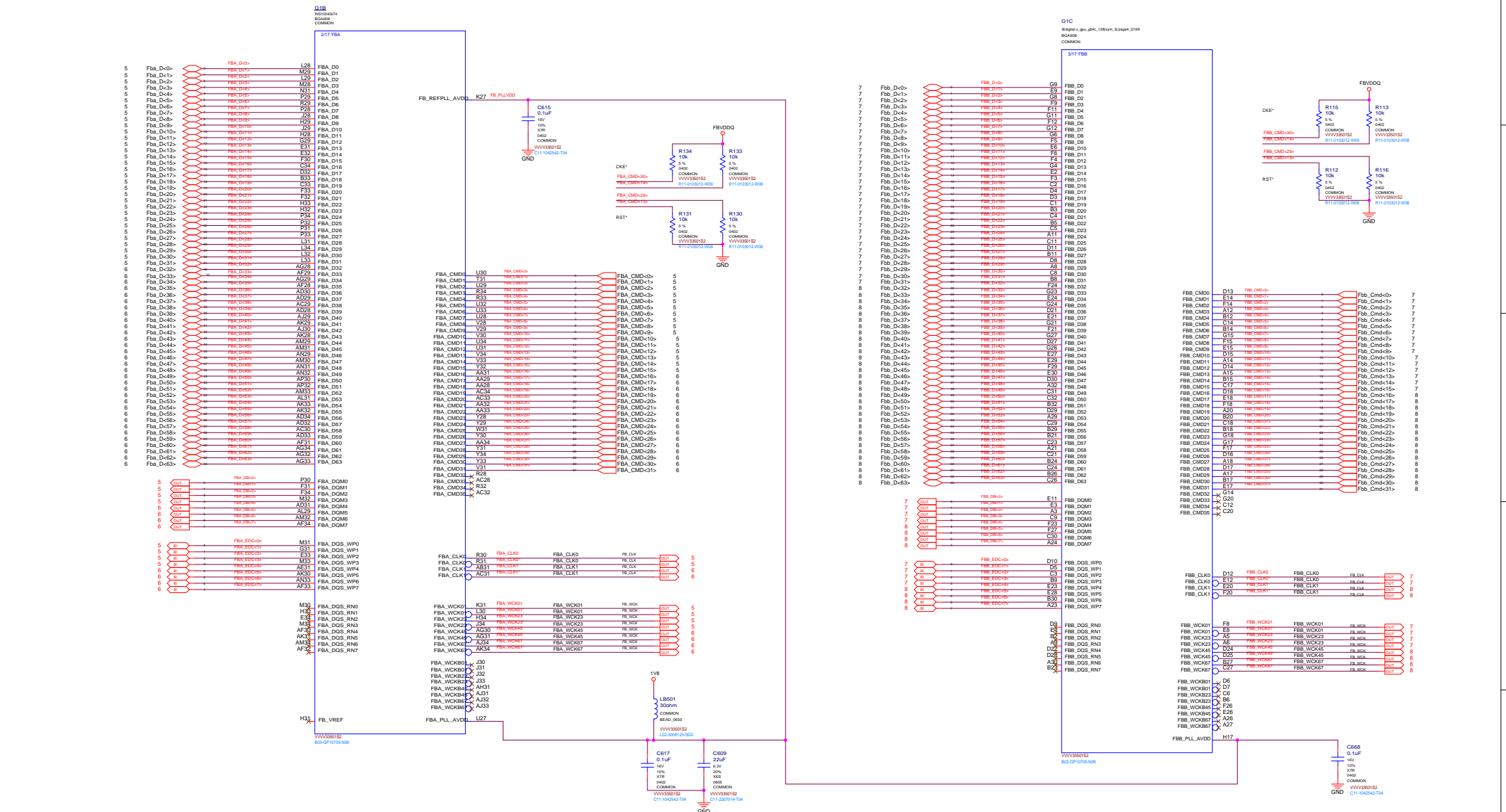


# PCI Express



		<b>MICRO-STAR INTL. CO., LTD</b>	
		<b>MS-V335</b>	
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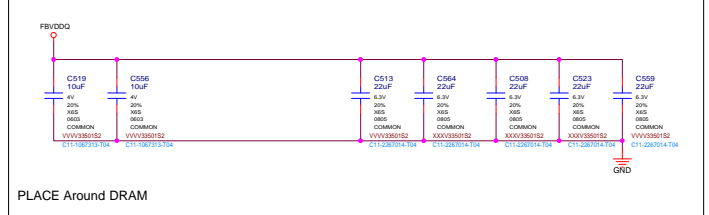
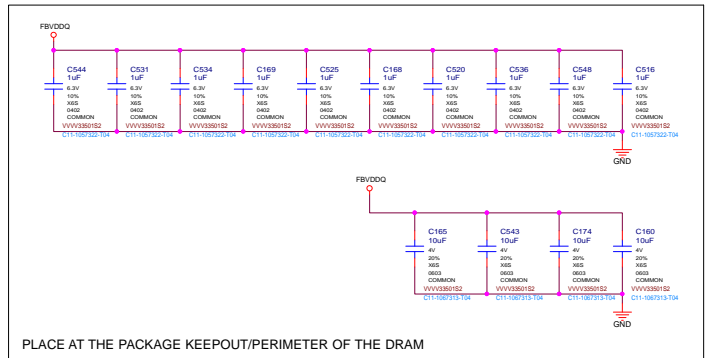
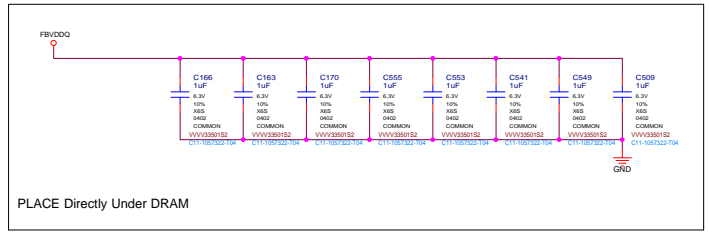
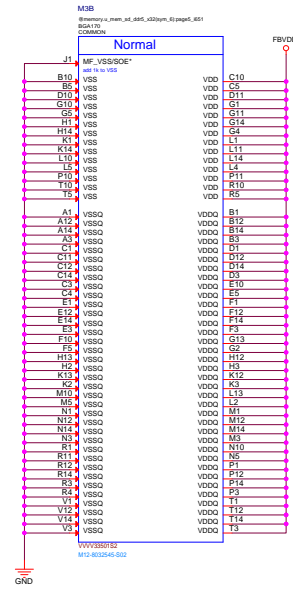
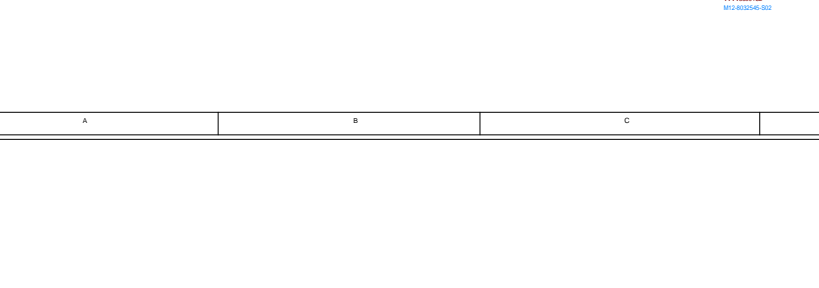
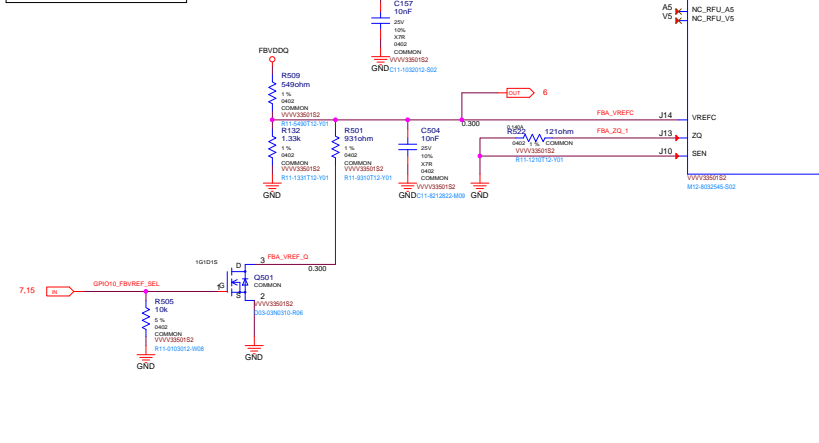
MEMORY: GPU Partition A/B



<b>MST</b>		
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-V335</b>		
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MEMORY: FBA Partition 31..0

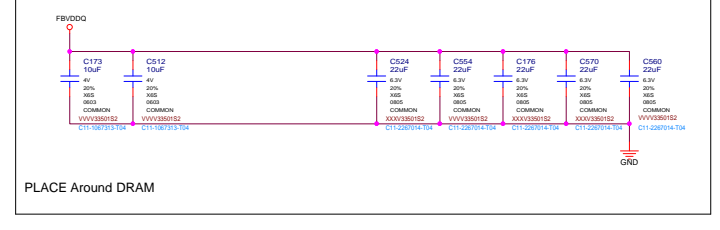
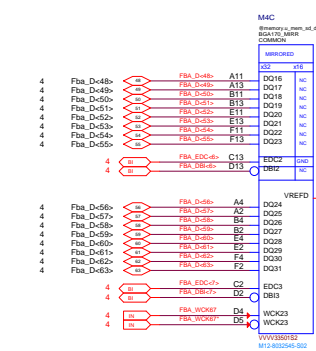
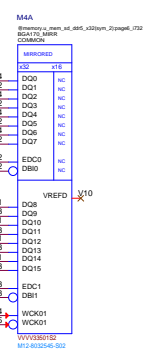
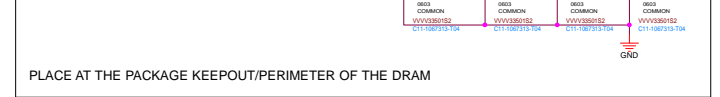
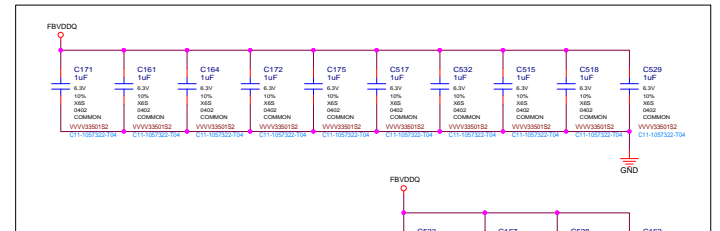
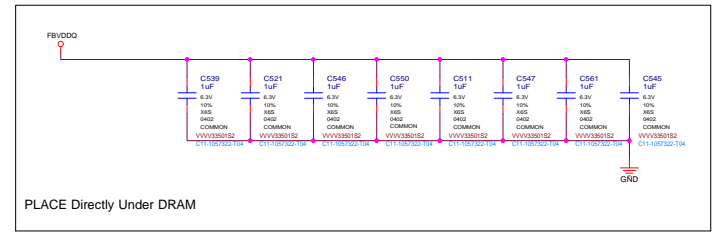
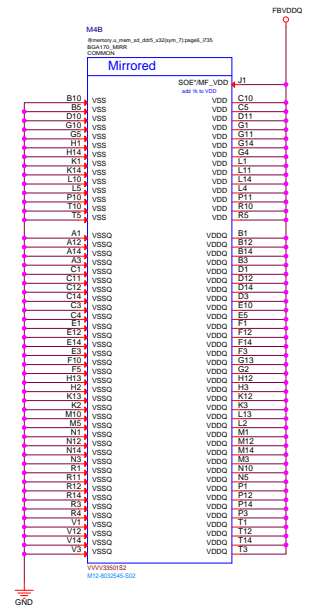
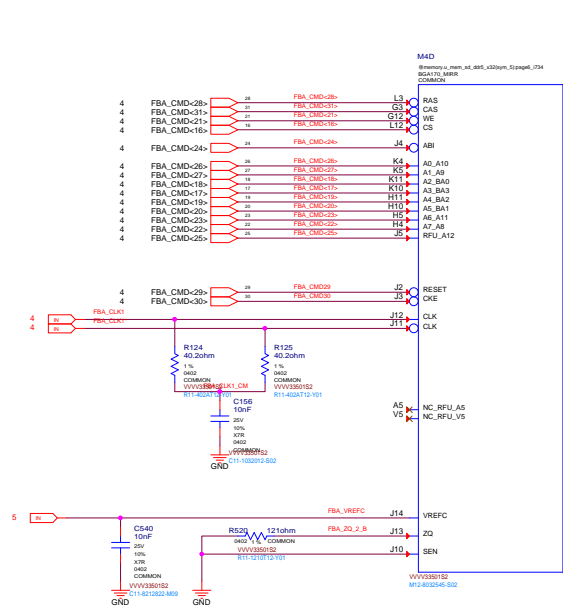
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CM00	CS*	
CM01	A3_BA3	
CM02	A2_BA2	
CM03	A4_BA2	
CM04	AS_BA1	
CM05	WE*	
CM06	AF_A8	
CM07	AB_A11	
CM08	AB*	
CM09	A12_RFU	
CM10	A0_A10	
CM11	A1_A9	
CM12	RA5*	
CM13	RS1*	
CM14	CKE*	
CM15	CAS*	
CM16		CS*
CM17		A3_BA3
CM18		A2_BA2
CM19		A4_BA2
CM20		AS_BA1
CM21		WE*
CM22		AF_A8
CM23		AB_A11
CM24		AB*
CM25		A12_RFU
CM26		A0_A10
CM27		A1_A9
CM28		RA5*
CM29		RS1*
CM30		CKE*
CM31		CAS*



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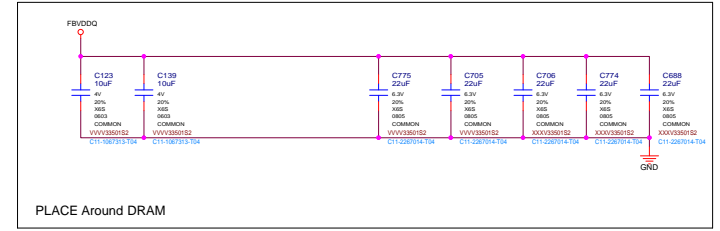
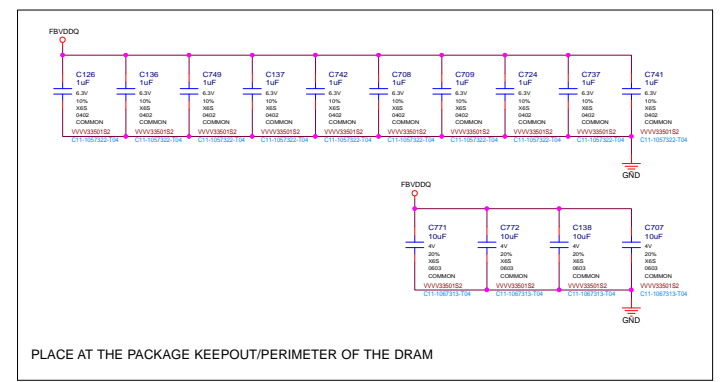
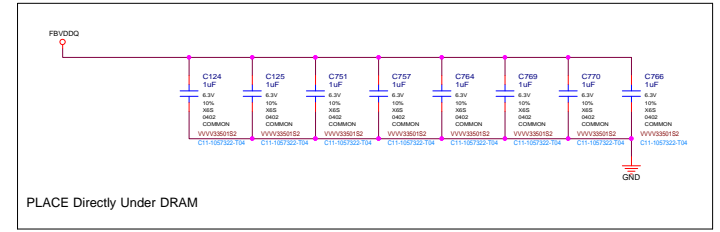
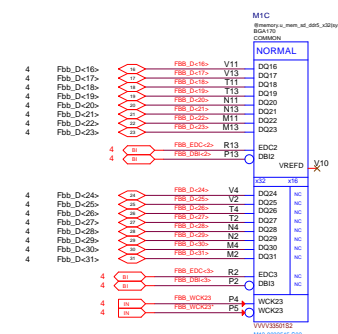
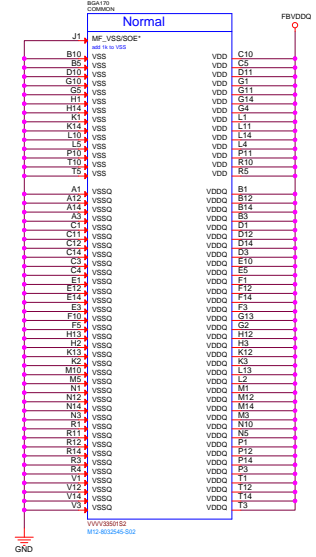
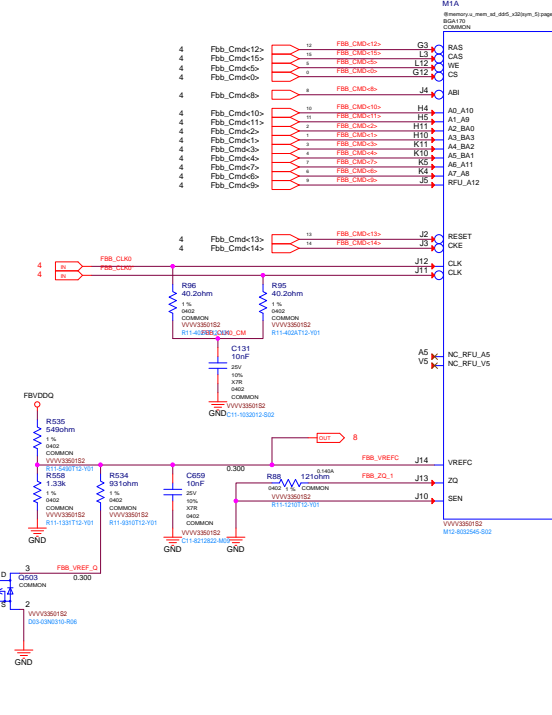
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CMD	0..31	32..63
CM00	CS*	CS*
CM01	A3_BA3	A3_BA3
CM02	A2_BA0	A2_BA0
CM03	A4_BA2	A4_BA2
CM04	A5_BA1	A5_BA1
CM05	WE*	WE*
CM06	A7_A8	A7_A8
CM07	AB_A11	AB_A11
CM08	AB*	AB*
CM09	A12_RFU	A12_RFU
CM10	A0_A10	A0_A10
CM11	A1_A9	A1_A9
CM12	RA0*	RA0*
CM13	R0*	R0*
CM14	CKE*	CKE*
CM15	CS*	CS*
CM16		
CM17	CS*	CS*
CM18	A3_BA3	A3_BA3
CM19	A2_BA0	A2_BA0
CM20	A4_BA2	A4_BA2
CM21	A5_BA1	A5_BA1
CM22	WE*	WE*
CM23	A7_A8	A7_A8
CM24	AB_A11	AB_A11
CM25	AB*	AB*
CM26	A12_RFU	A12_RFU
CM27	A0_A10	A0_A10
CM28	A1_A9	A1_A9
CM29	RA0*	RA0*
CM30	R0*	R0*
CM31	CKE*	CKE*
CM32	CS*	CS*



MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3..BA3	
CMD2	AA..BA2	
CMD3	AA..BA1	
CMD4	WE*	
CMD5	A12..A4	
CMD6	AE..A11	
CMD7	AB*	
CMD8	AS..RFU	
CMD9	A0..A10	
CMD10	A1..A6	
CMD11	RAS*	
CMD12	RST*	
CMD13	CE*	
CMD14	CAS*	
CMD15		
CMD16		CS*
CMD17		A3..BA3
CMD18		AA..BA2
CMD19		AA..BA1
CMD20		WE*
CMD21		A12..A4
CMD22		AE..A11
CMD23		AB*
CMD24		AS..RFU
CMD25		A0..A10
CMD26		A1..A6
CMD27		RAS*
CMD28		RST*
CMD29		CE*
CMD30		CAS*
CMD31		



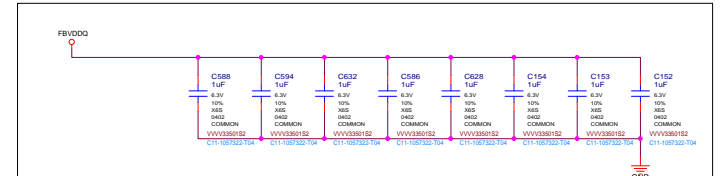
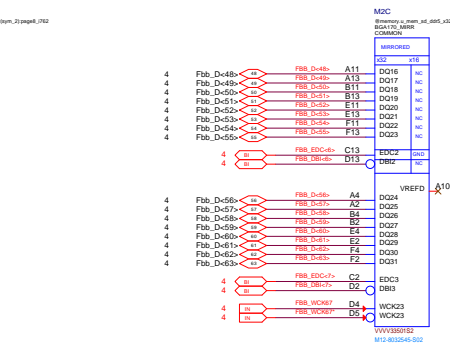
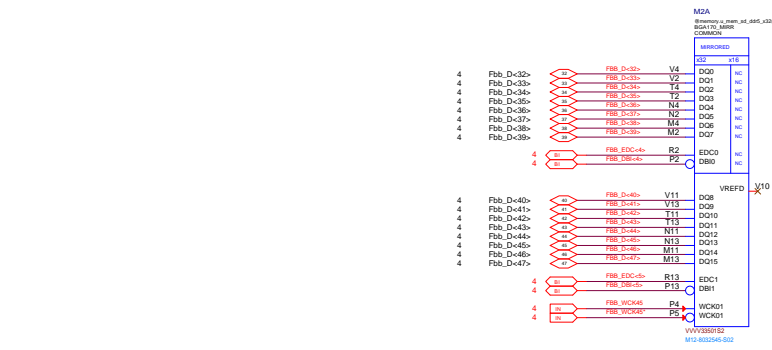
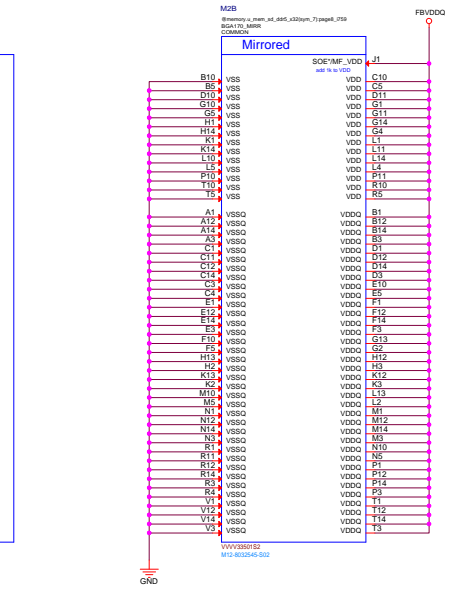
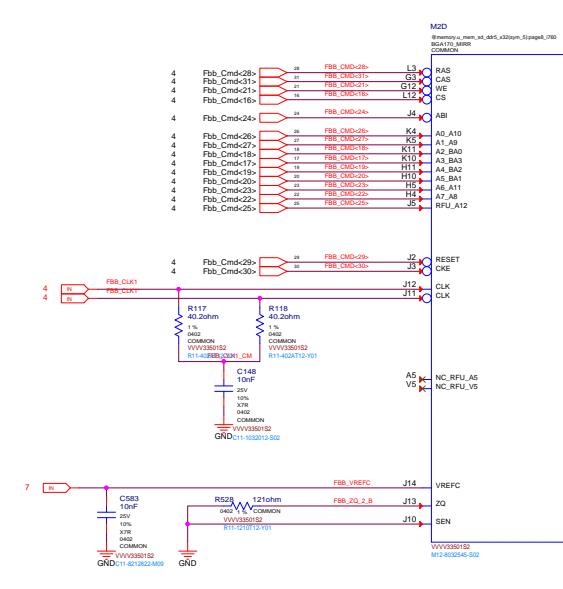
**MICRO-STAR INT'L CO.,LTD**

**MS-V335**

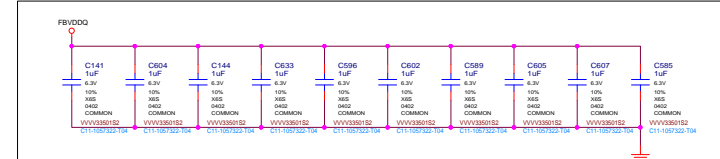
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MEMORY: FBB Partition 63..32

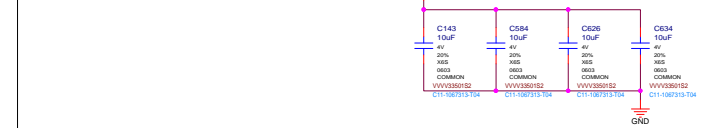
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA2	
CMD3	A4_BA4	
CMD4	A5_BA5	
CMD5	WE*	
CMD6	A7_A8	
CMD7	AA_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A8	
CMD12	RAS*	
CMD13	RST*	
CMD14	CHE*	
CMD15	CAS*	
CMD16		
CMD17	A3_BA3	CS*
CMD18	A2_BA2	A3_BA3
CMD19	A4_BA4	A4_BA2
CMD20	A5_BA5	A6_A11
CMD21	WE*	A7_A8
CMD22	AA_A11	A12_RFU
CMD23	AB*	A0_A10
CMD24	AB*	A1_A8
CMD25	A12_RFU	RAS*
CMD26	A0_A10	RST*
CMD27	A1_A8	CHE*
CMD28	RAS*	CAS*
CMD29	RST*	
CMD30	CHE*	
CMD31	CAS*	



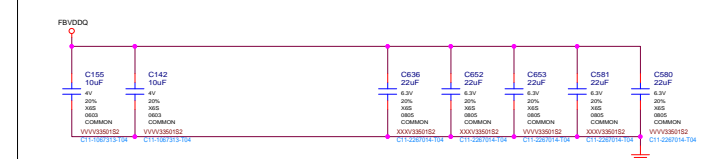
PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPUP/PERIMETER OF THE DRAM



PLACE AT THE PACKAGE KEEPUP/PERIMETER OF THE DRAM



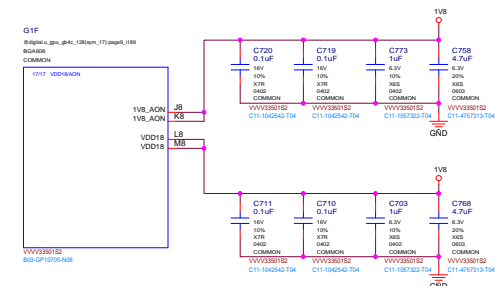
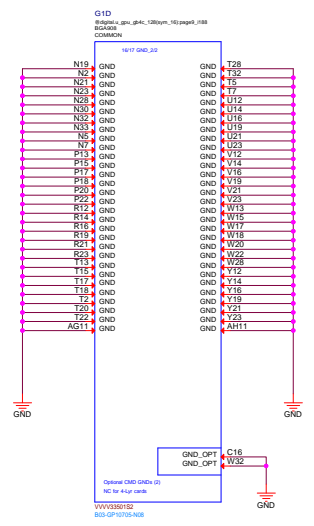
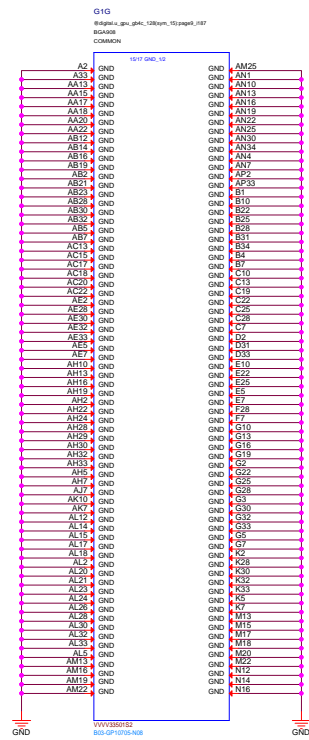
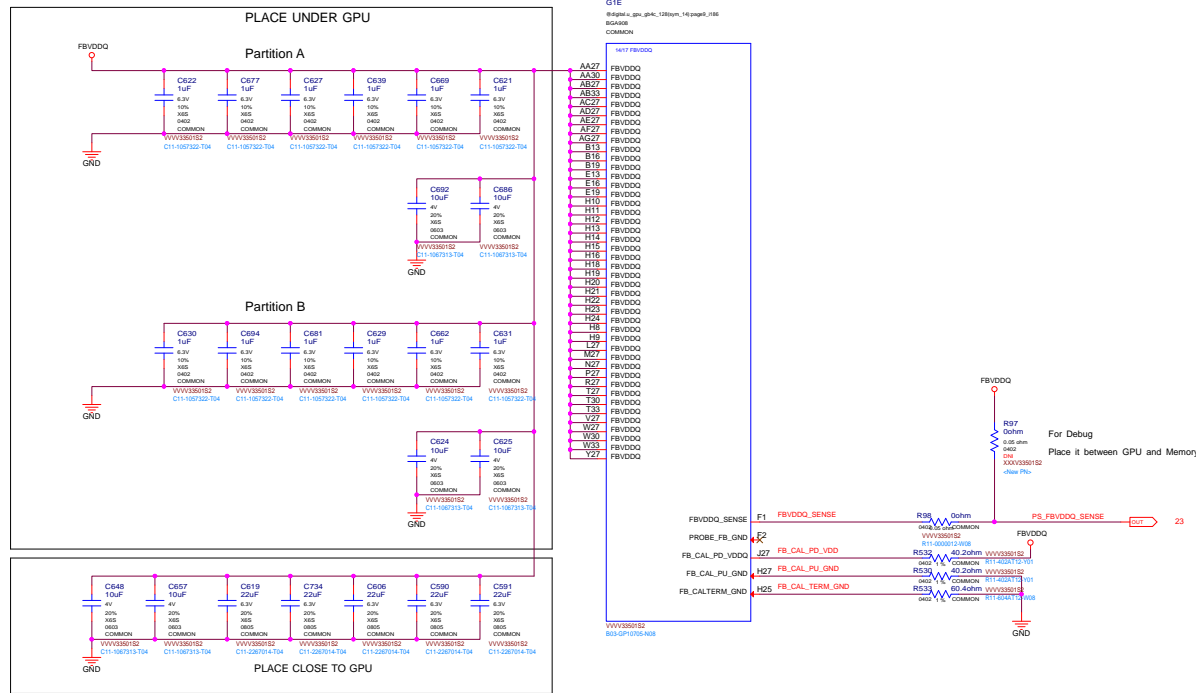
PLACE Around DRAM

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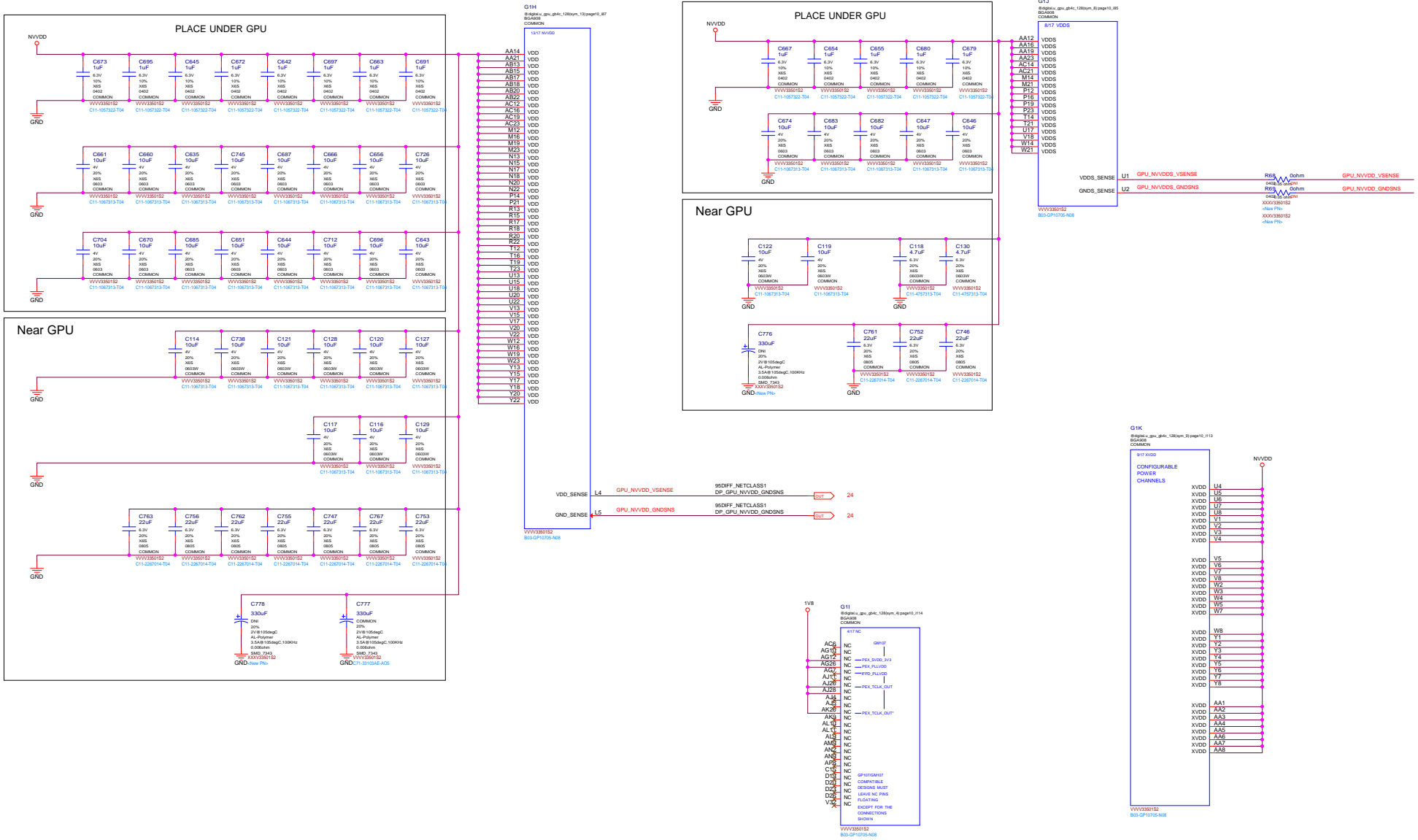
# GPU FBVDDQ & 1V8 Decoupling



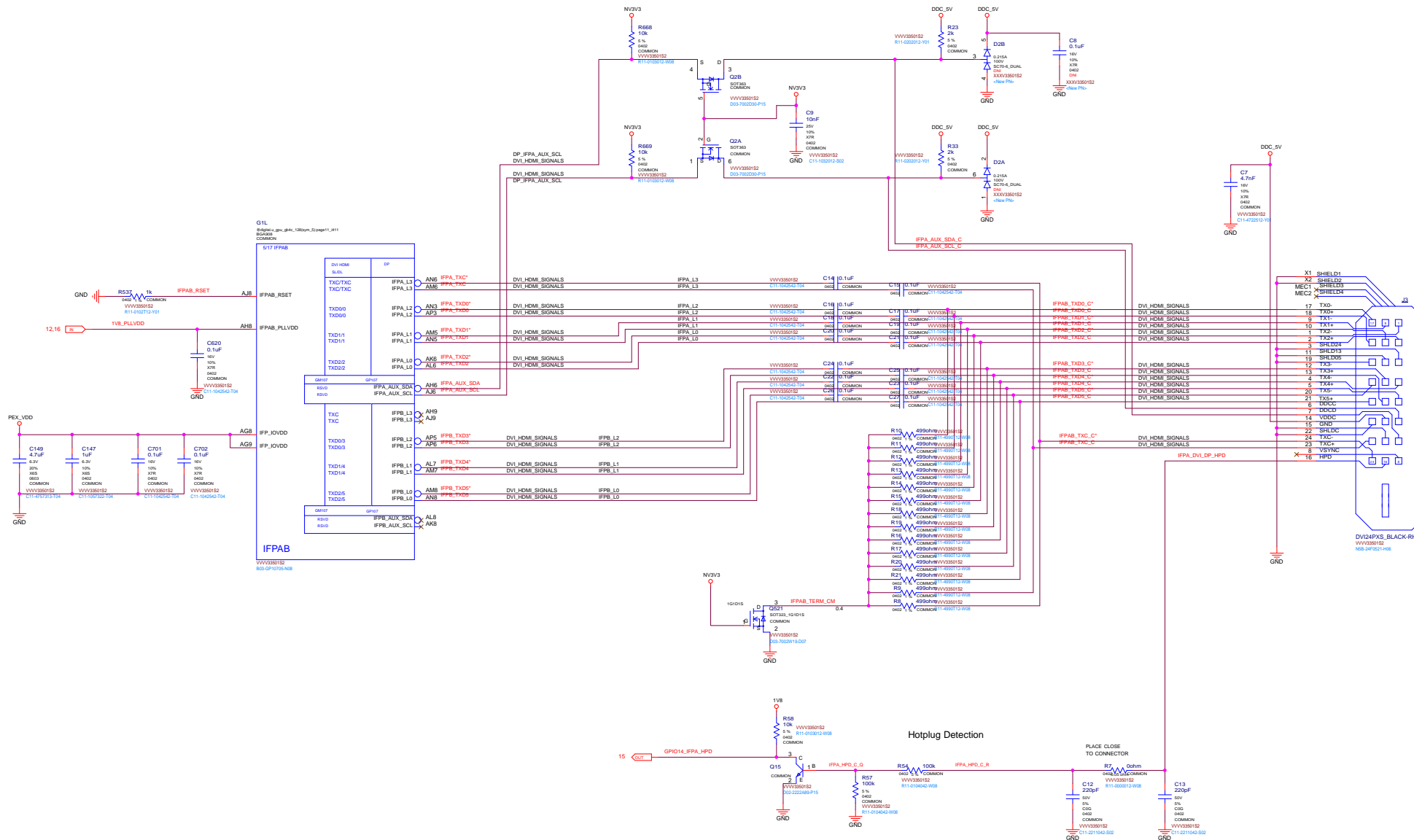
**MICRO-STAR INT'L CO.,LTD**  
**MS-V335**

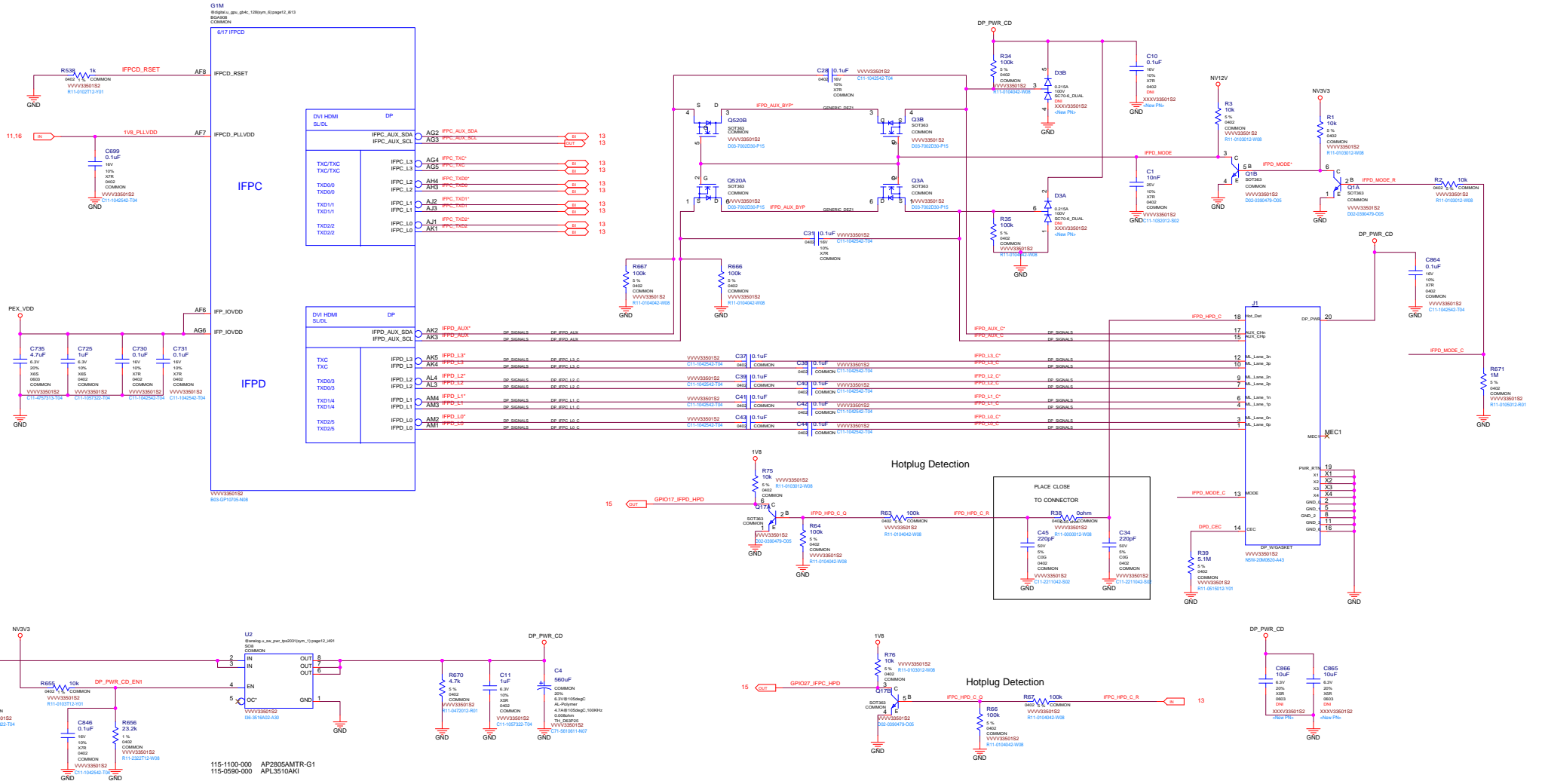
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# GPU NVVDD & NVVDDS Decoupling



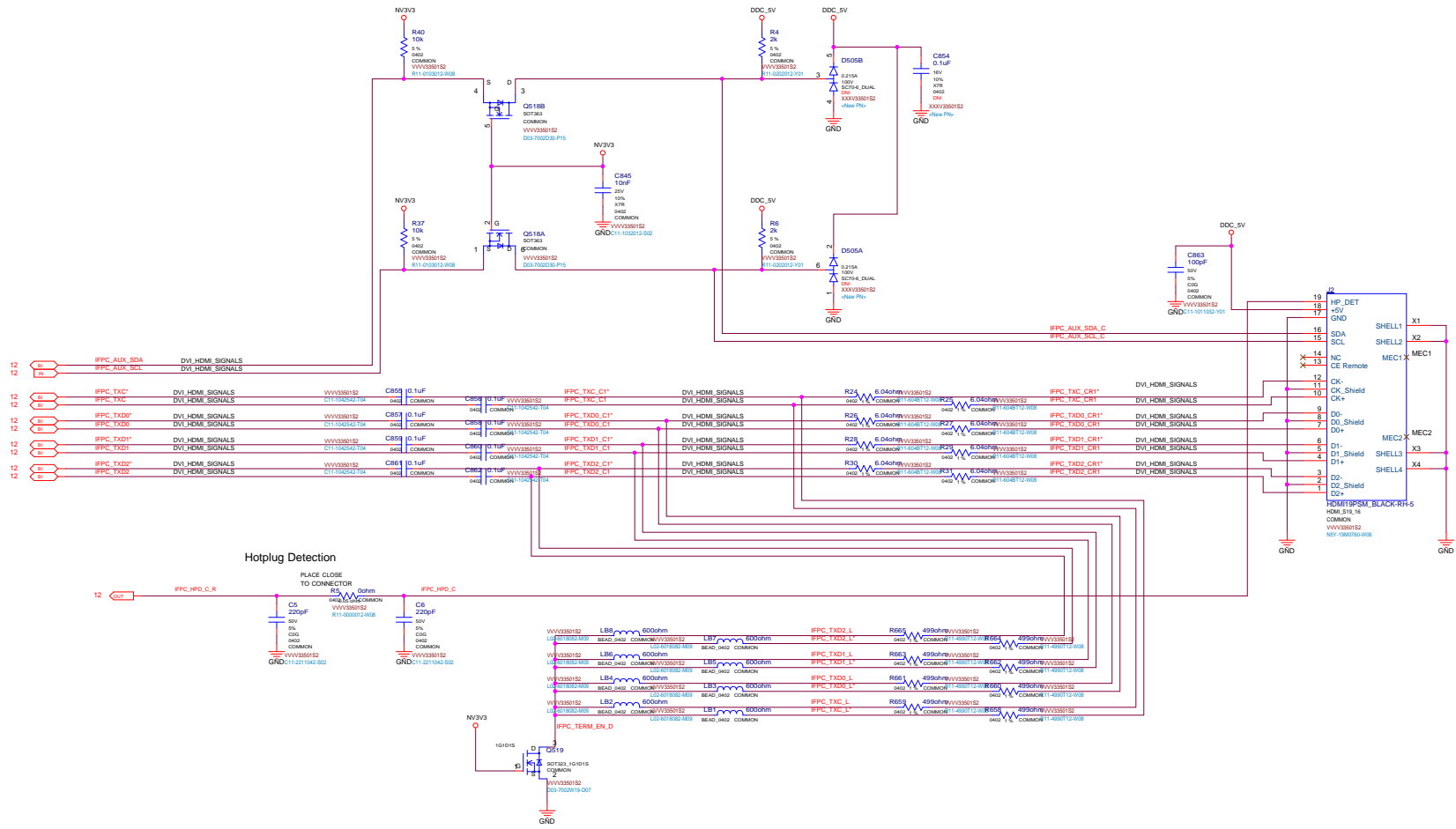
IFPAB DVI-DL



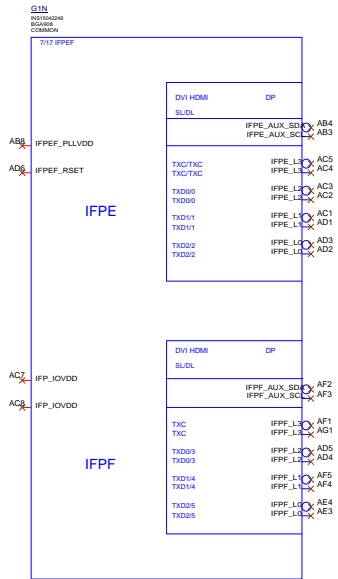


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115-0590-000 APL3510AK1

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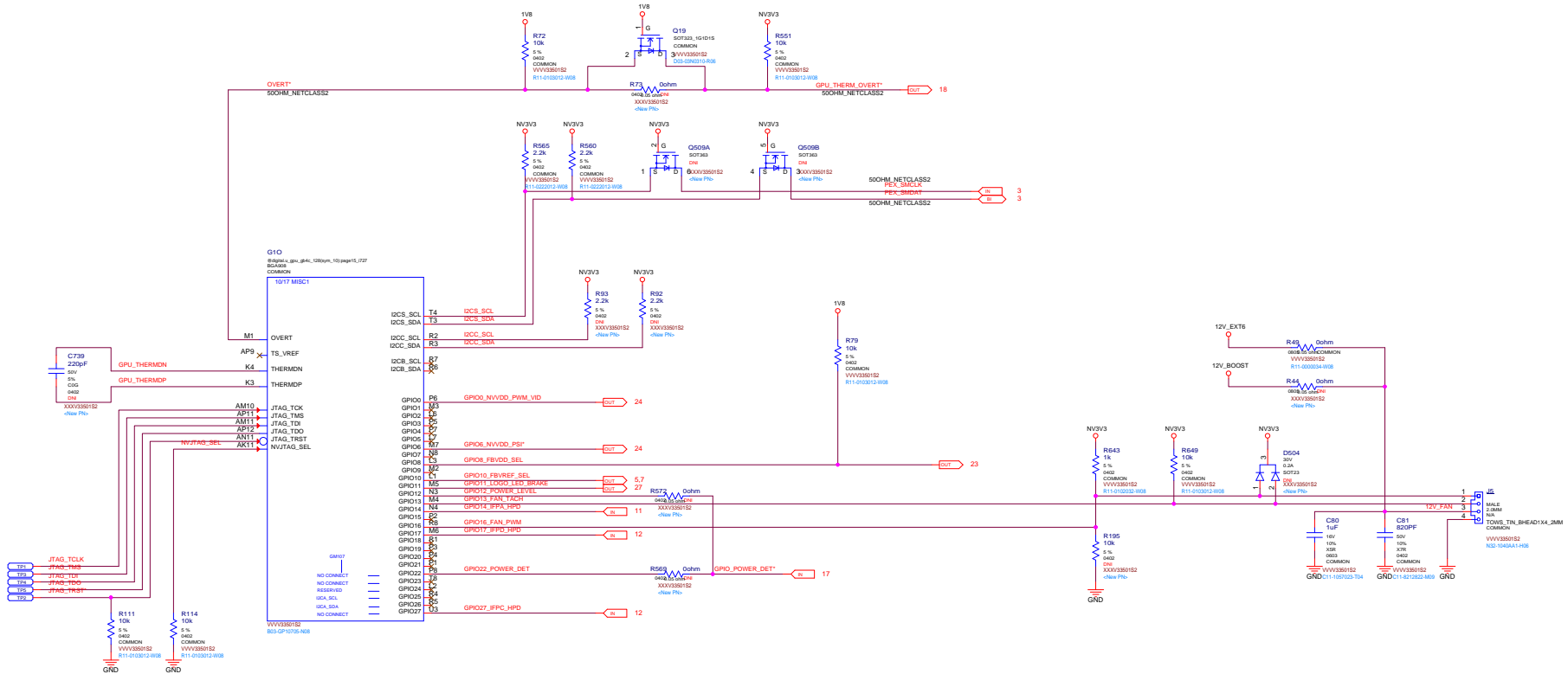


IFPEF UNUSED



MISC1: GPIO, Fan, Thermal, JTAG

PADS FOR DEBUGGING



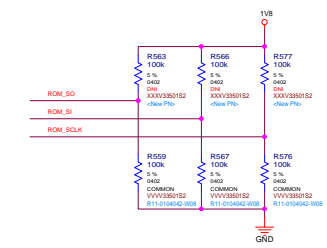
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<b>MS-V335</b>		
Site Custom	Document Description 15_MISC1: GPIO, Fan, Thermal, JTAG	Rev 1.1
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# MISC2: ROM, XTAL, Straps

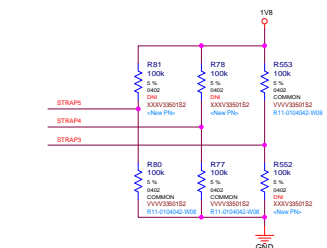
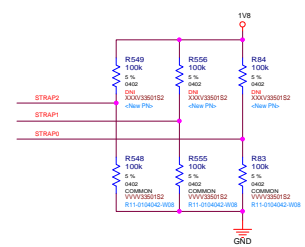
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L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	M	L	0011	
H	M	H	0010	
H	M	M	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

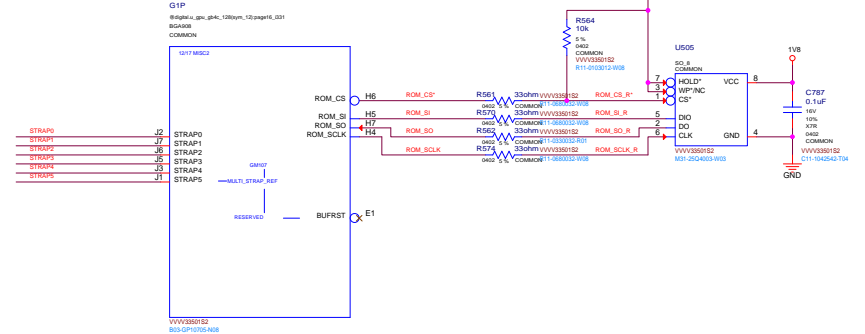
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M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	0	1
H	L	H	0	1	0	0
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0



H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

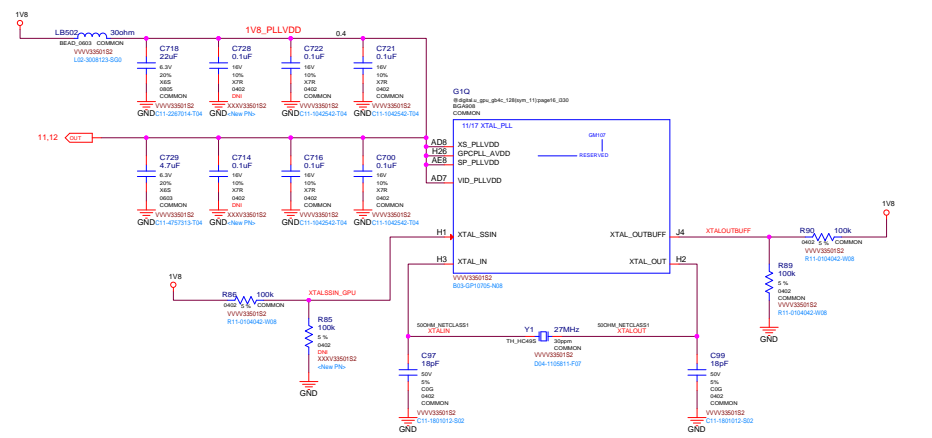


1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



## Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



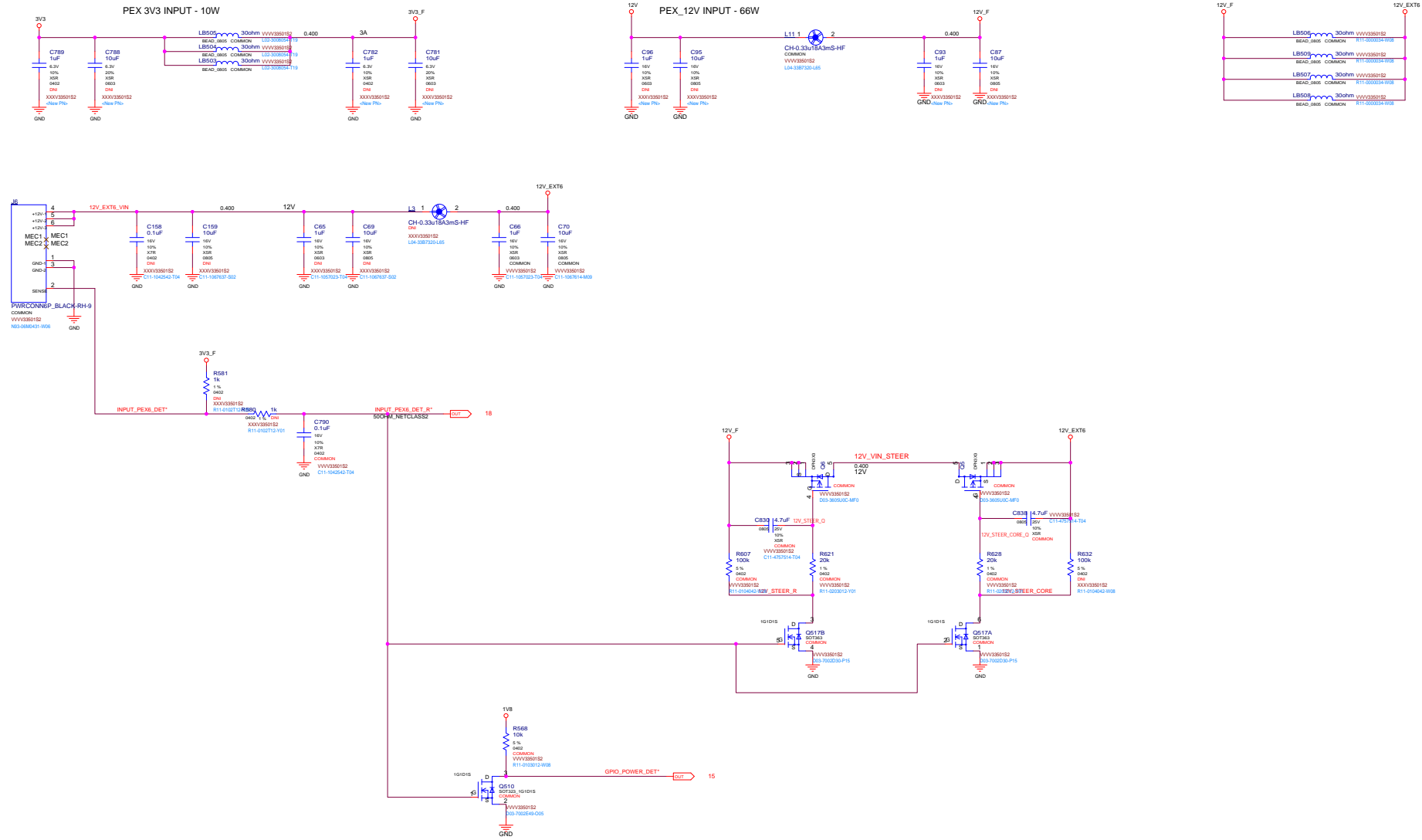
**MICRO-STAR INT'L CO.,LTD**

**MS-V335**

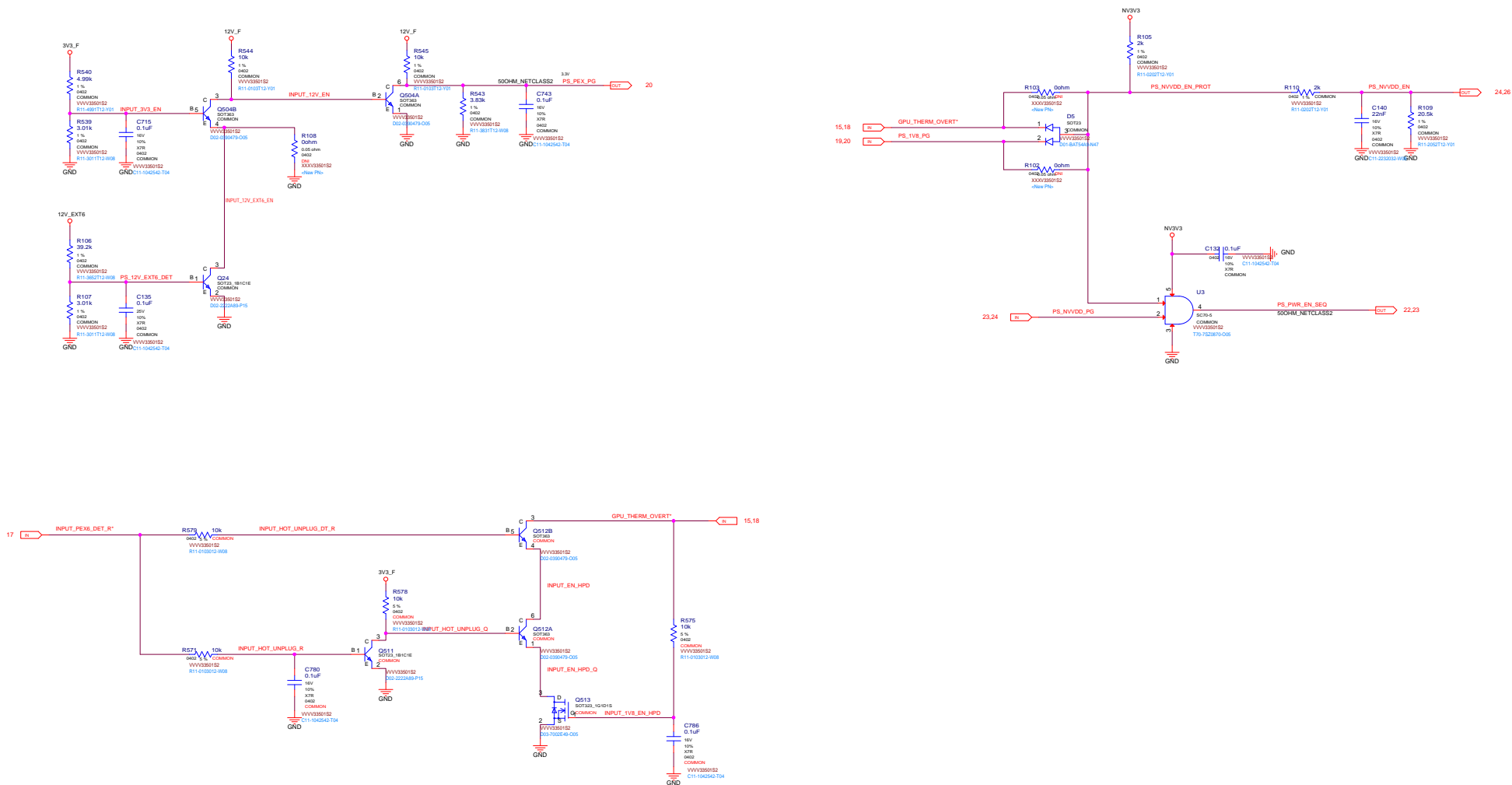
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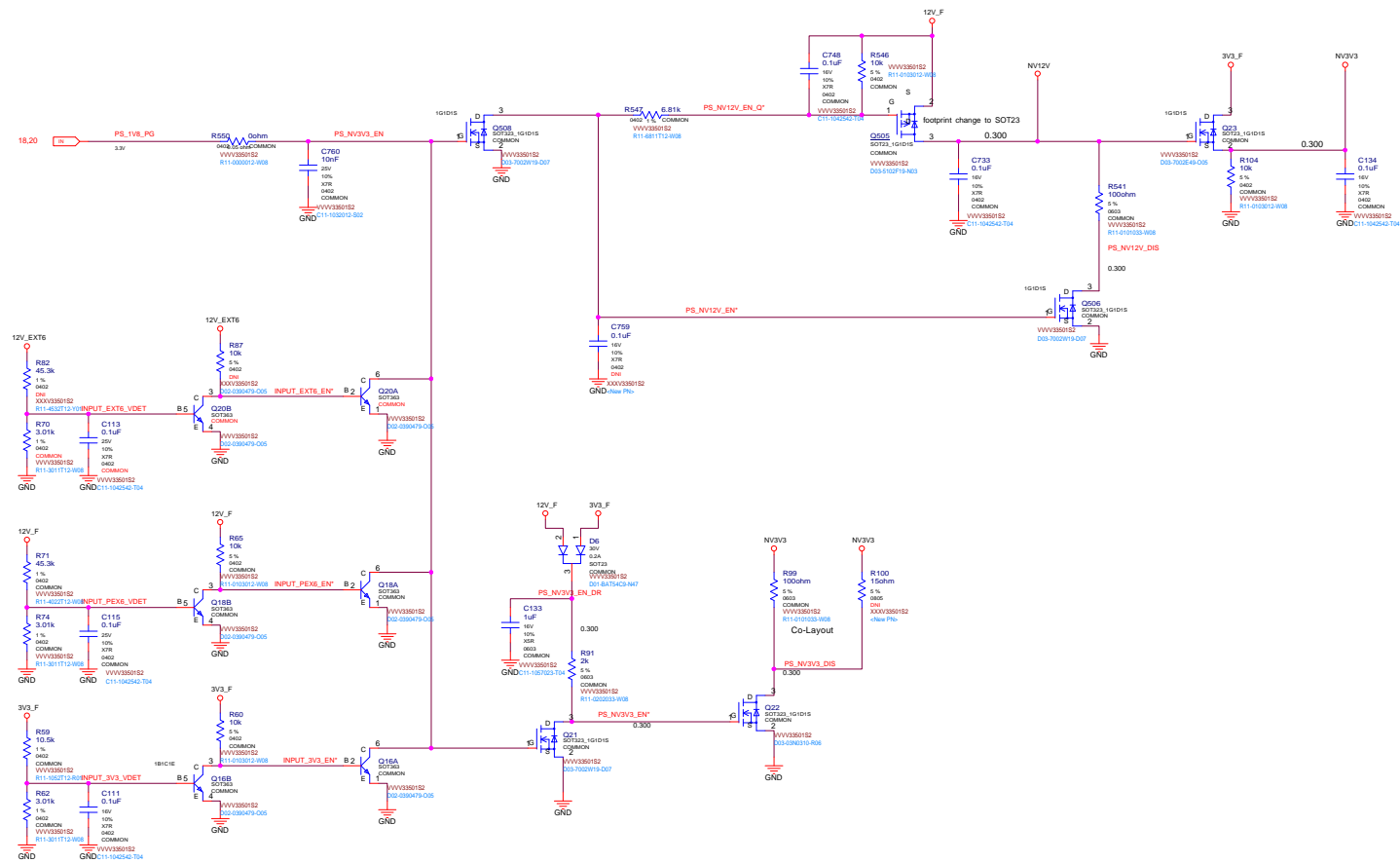
Power Inputs and Filtering



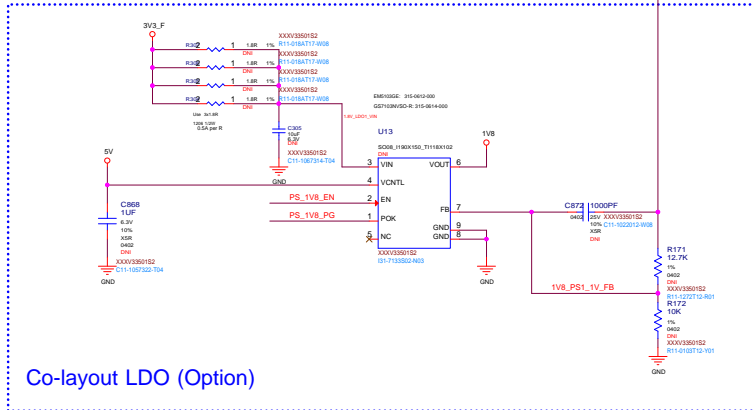
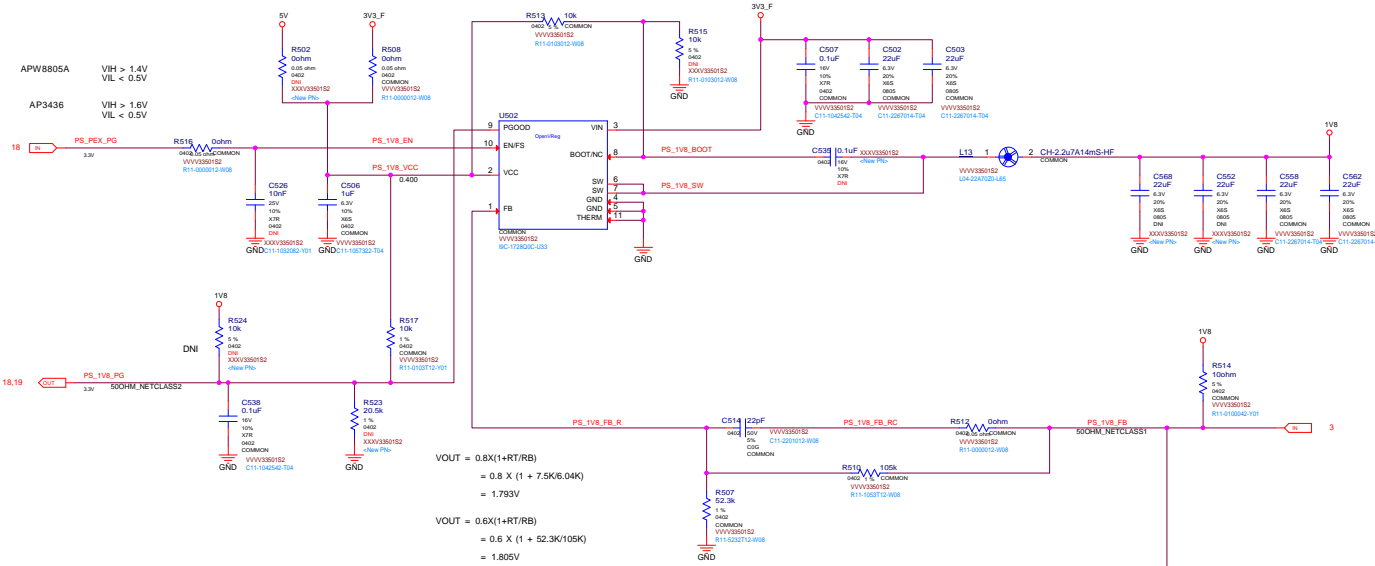
# Power sequence



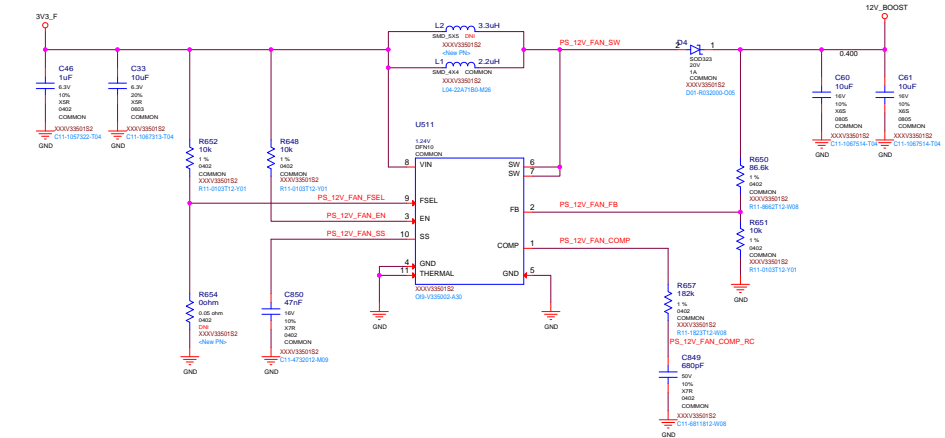
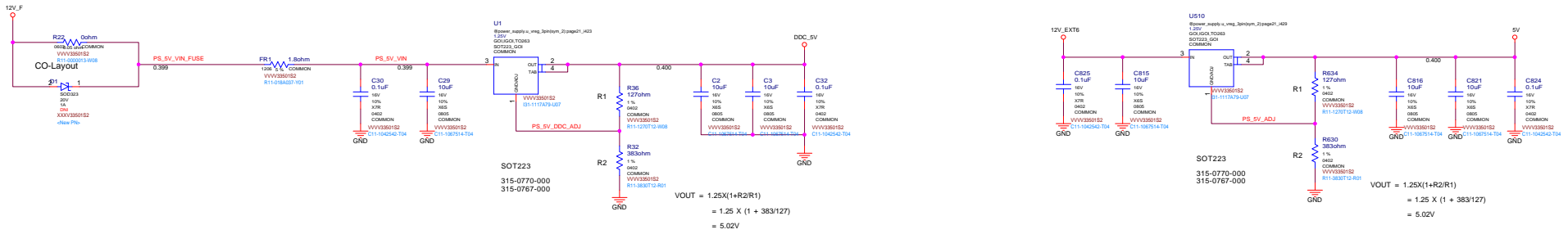
PS: NV3V3 & NV12V



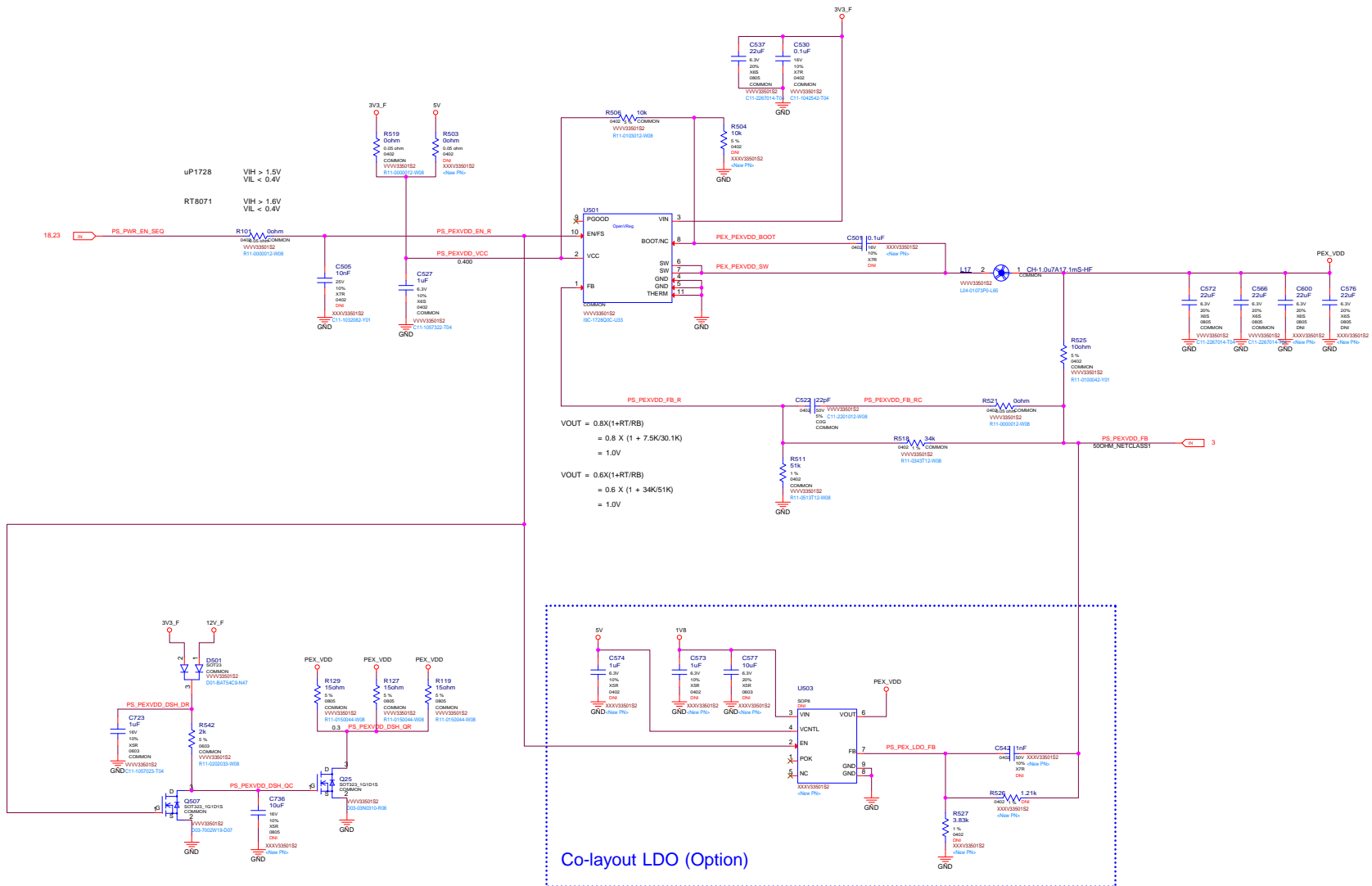
<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-V335</b>			
Rev	Description		
1.1	19_PS: NV3V3 & NV12V		
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# PSII:5V & 12V\_FAN

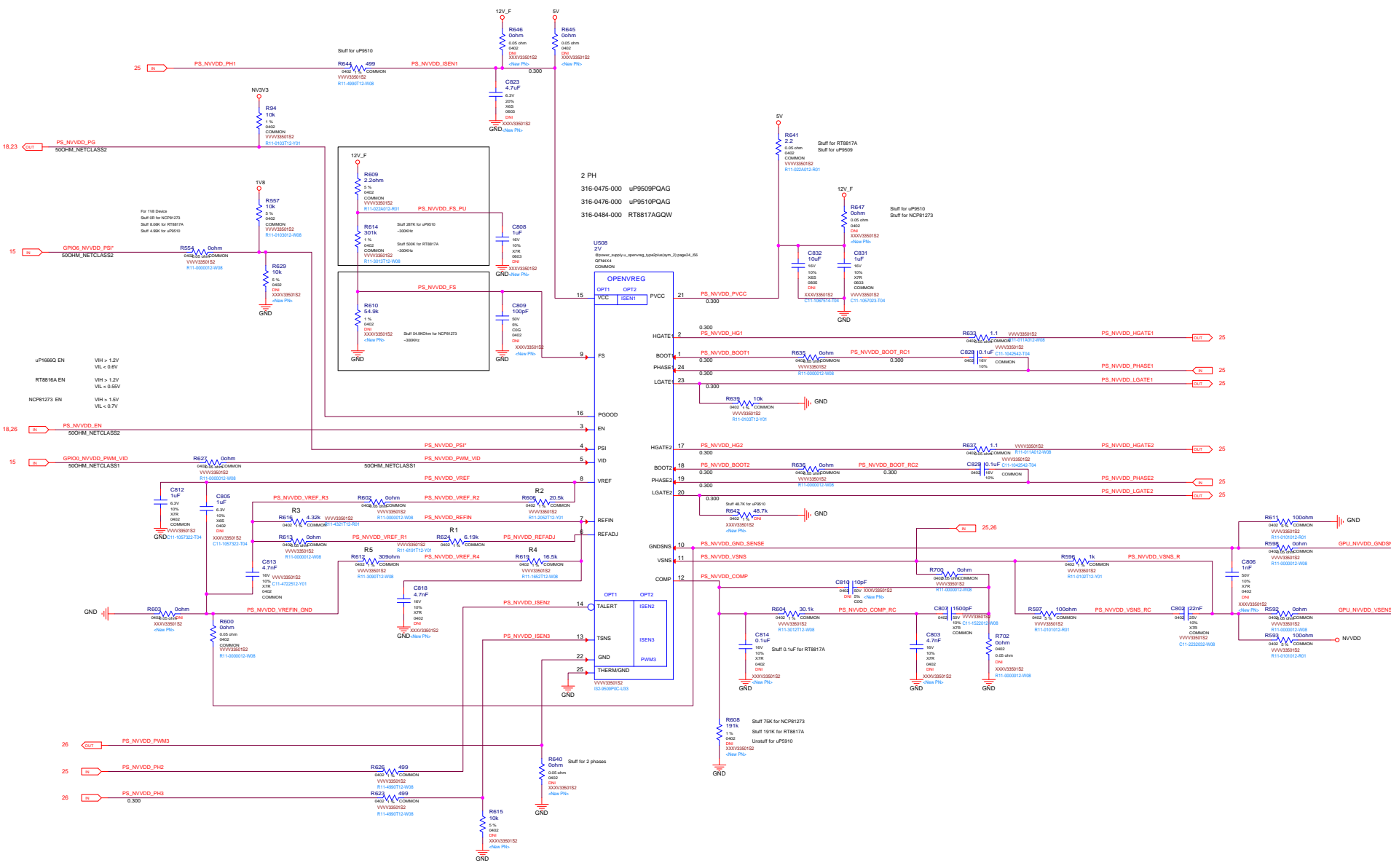


# PS III: PEXVDD



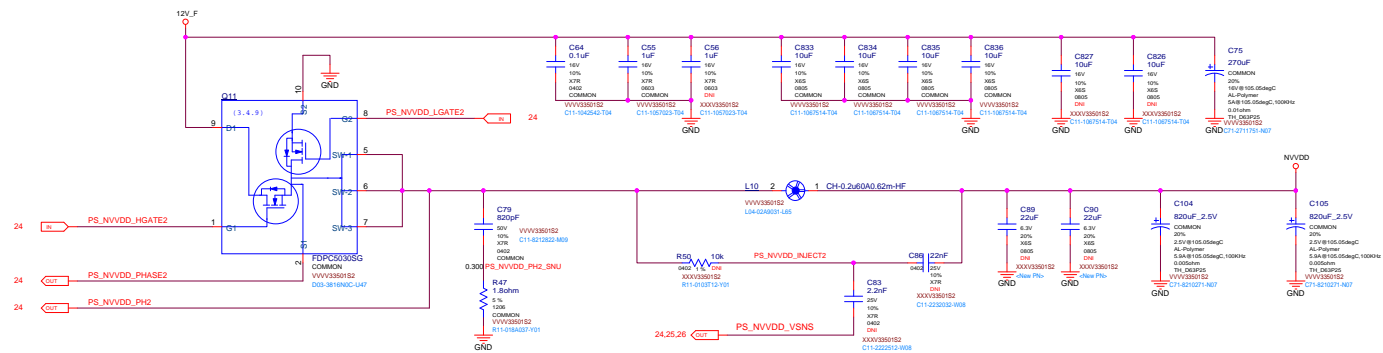
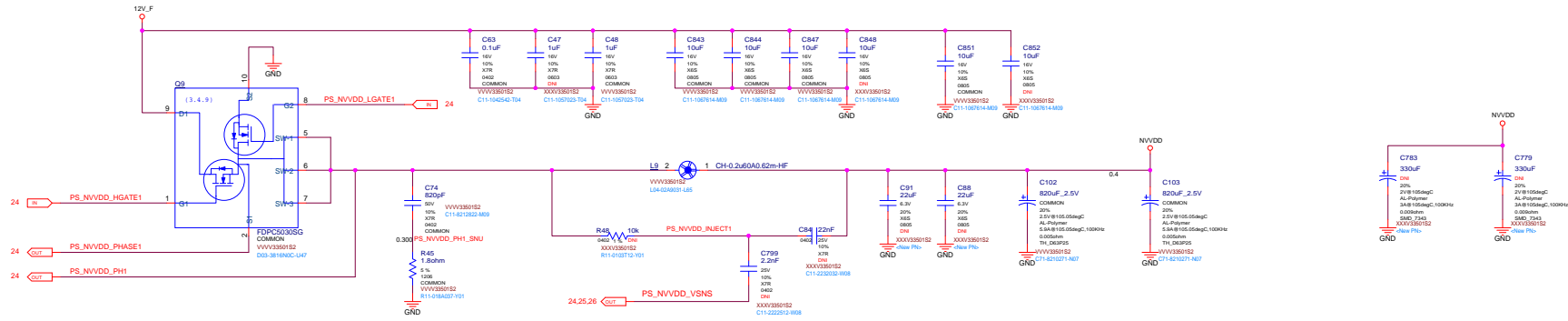


PS V: NVVDD OVR2+1



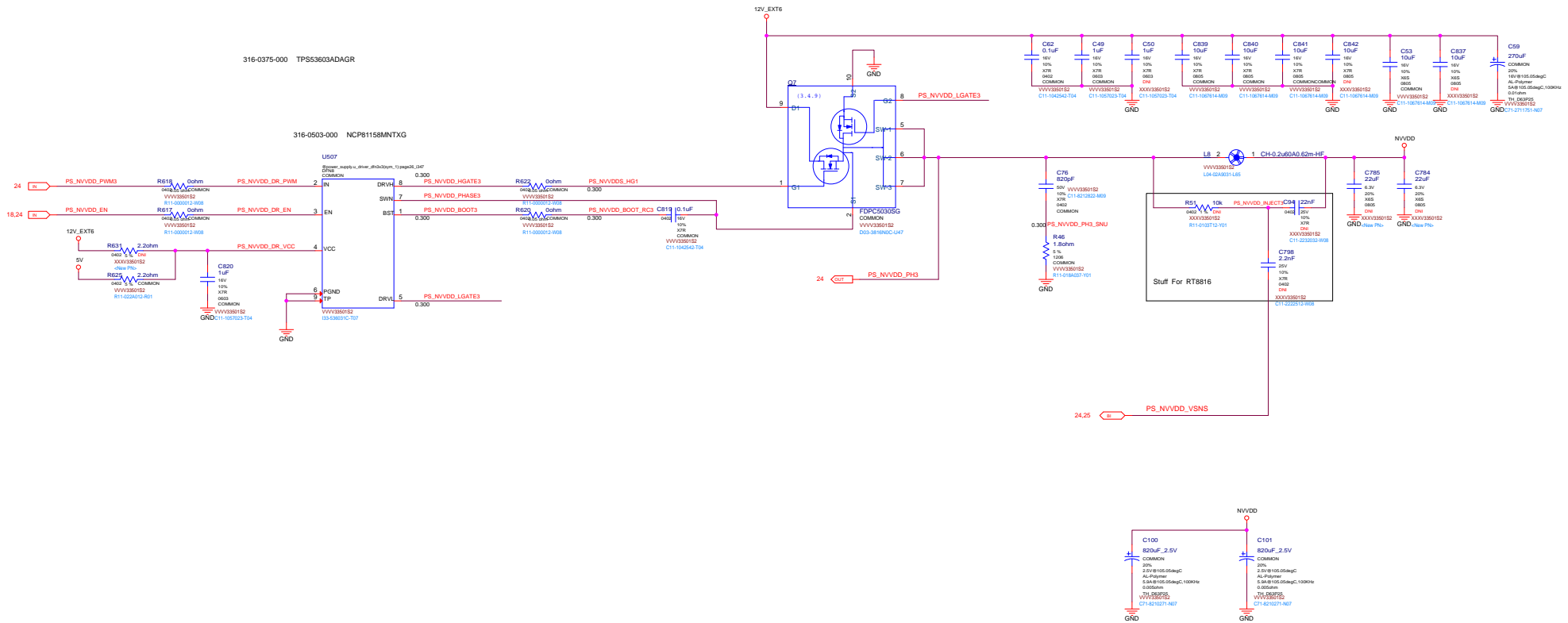


# PS V: NVVDD Phase 1,2

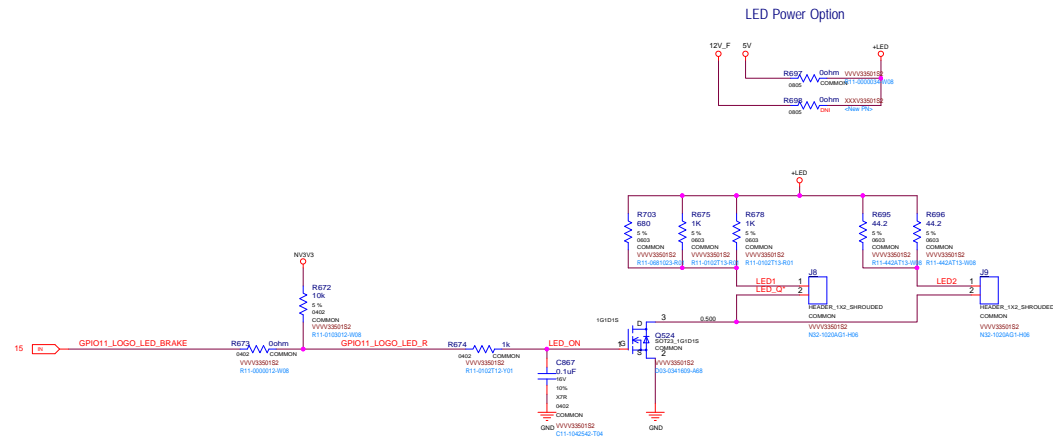


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Custom	25_PS_V: NVVDD Phase 1,2	1.1	
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PS V: NVDD Phase 3



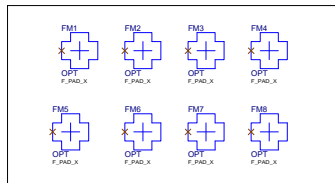
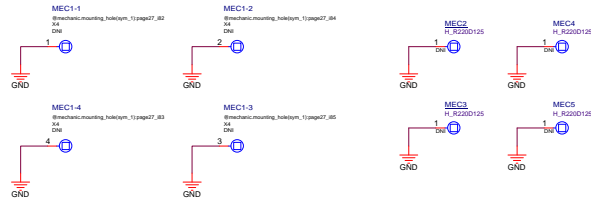
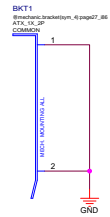
Logo LED



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Mechanical: Bracket/Thermal Solution

Brackets:



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