

PG142-B00

DP + DP + DP + HDMI/DP

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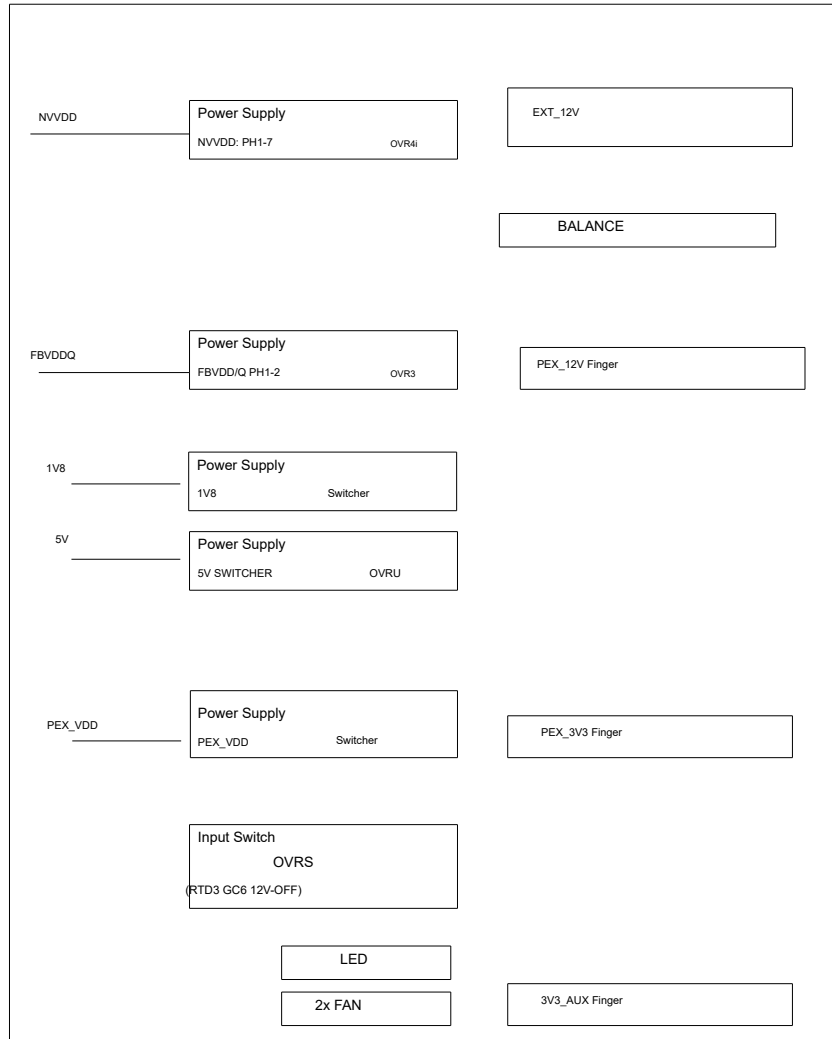
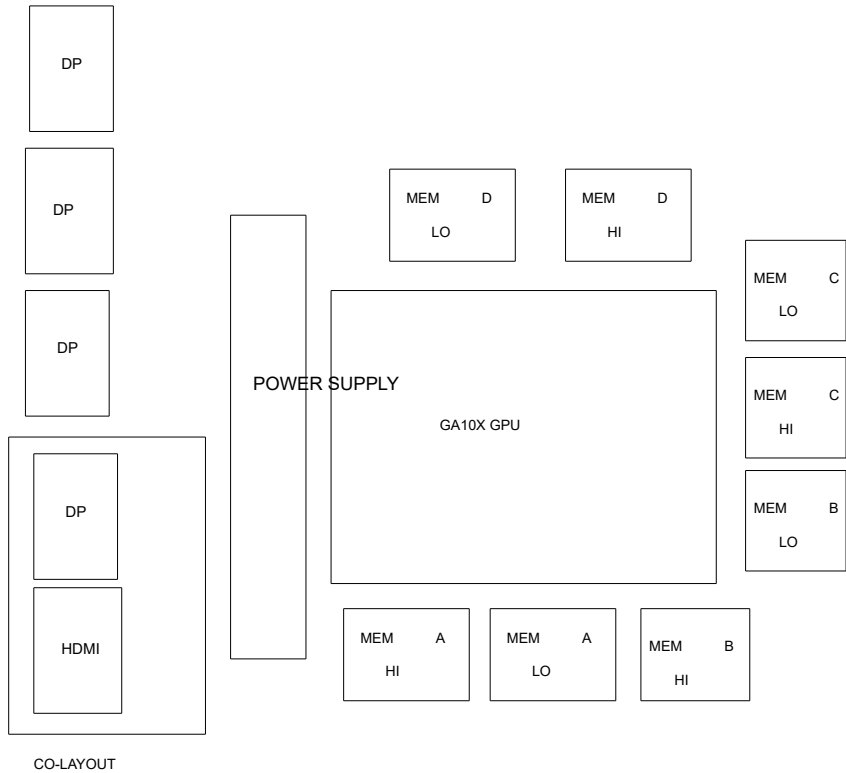
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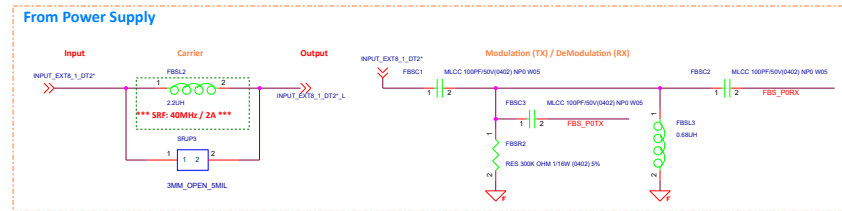
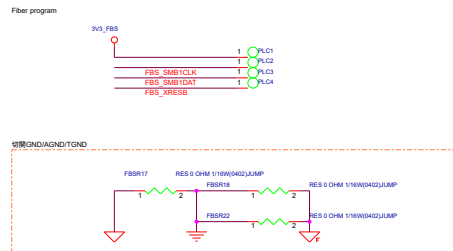
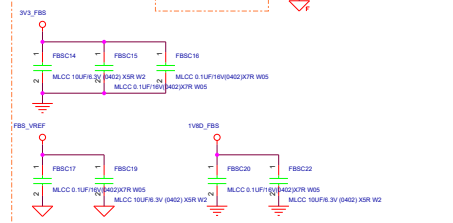
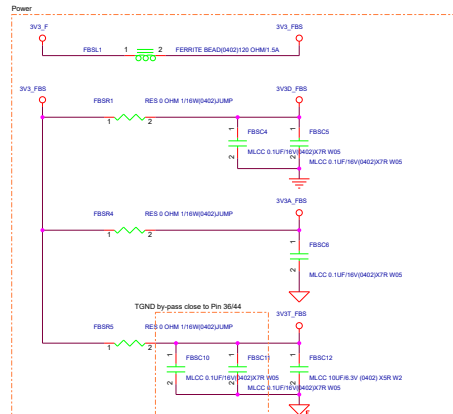
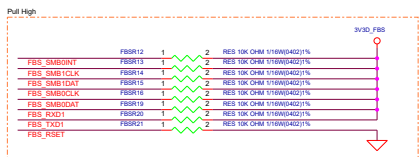
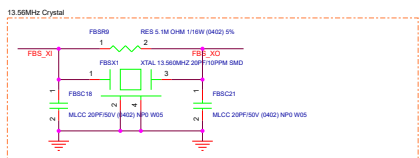
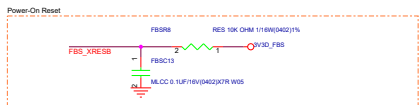
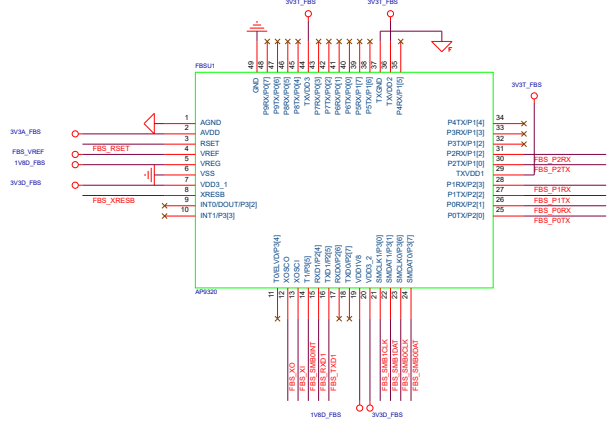
26	MISC1: ROM, XTAL, STRAPS
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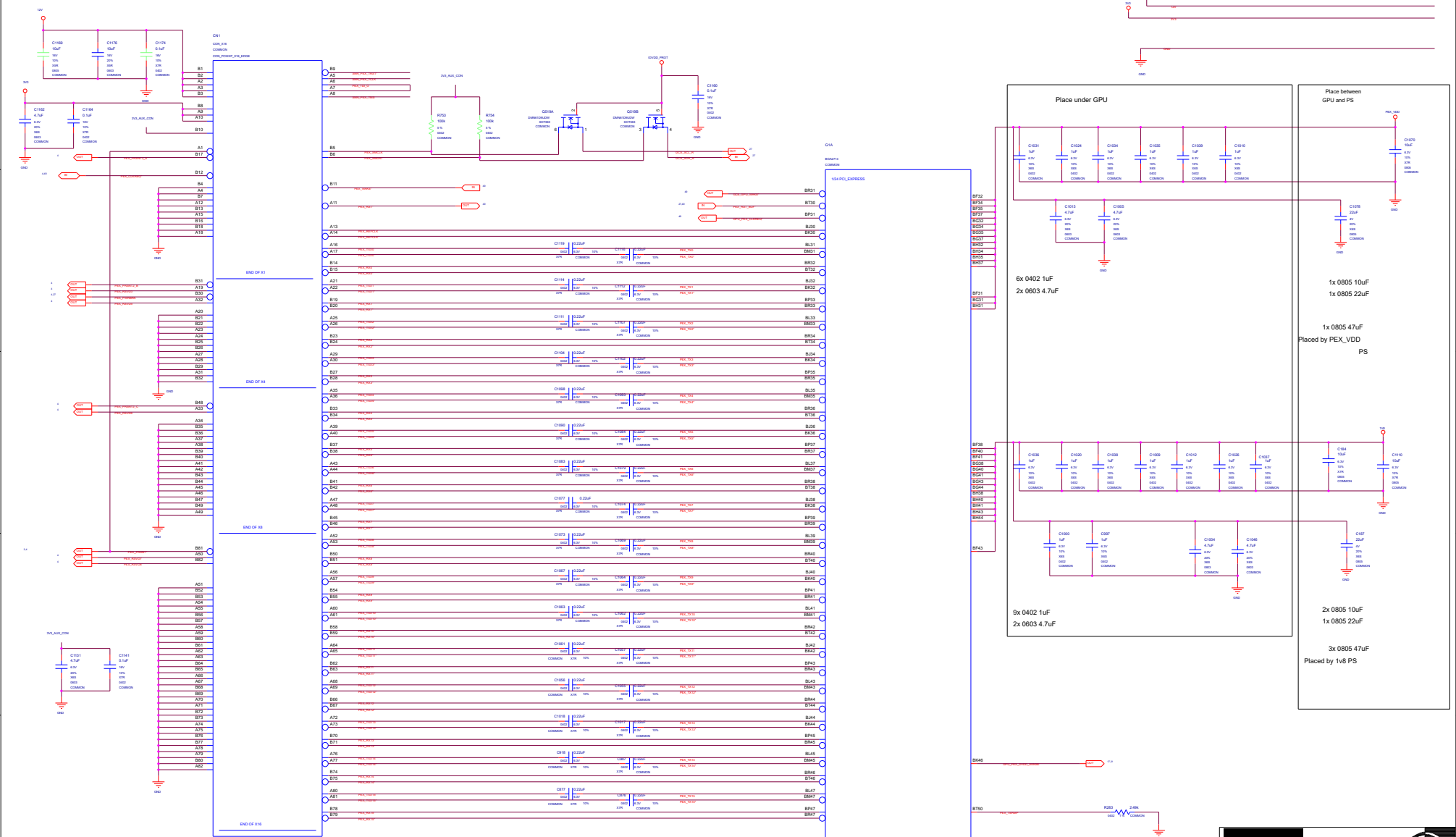
Page Description

51	FAN & LED
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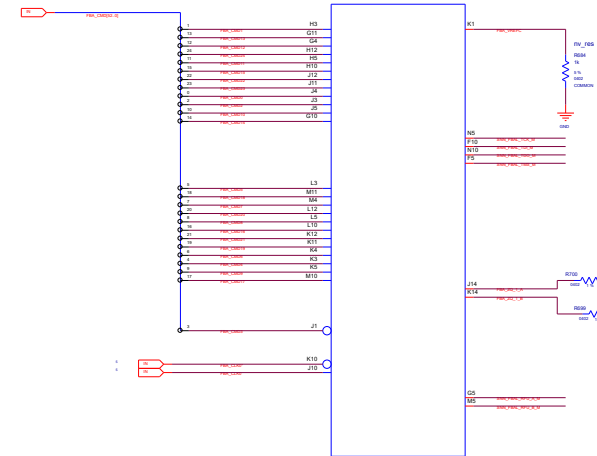
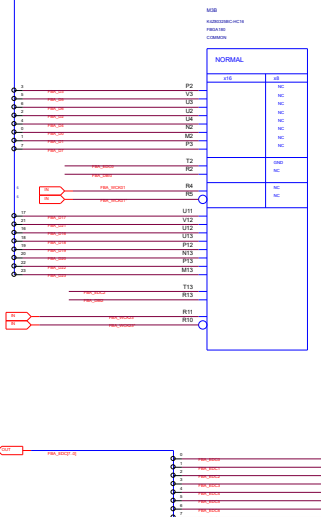
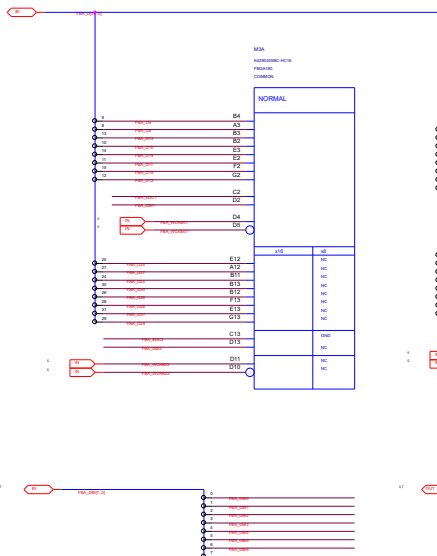
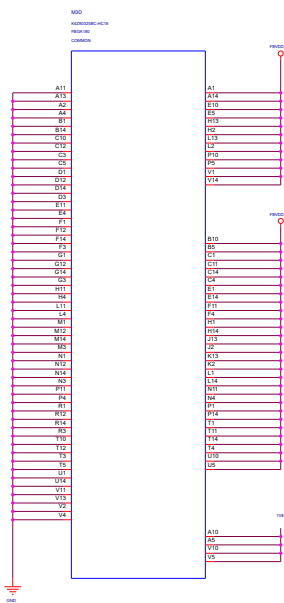




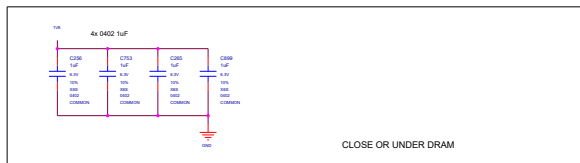
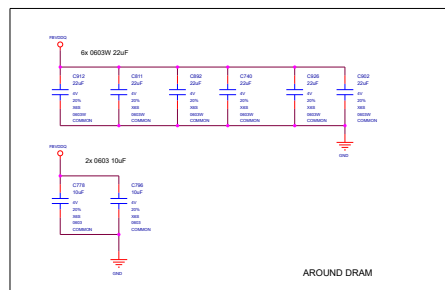
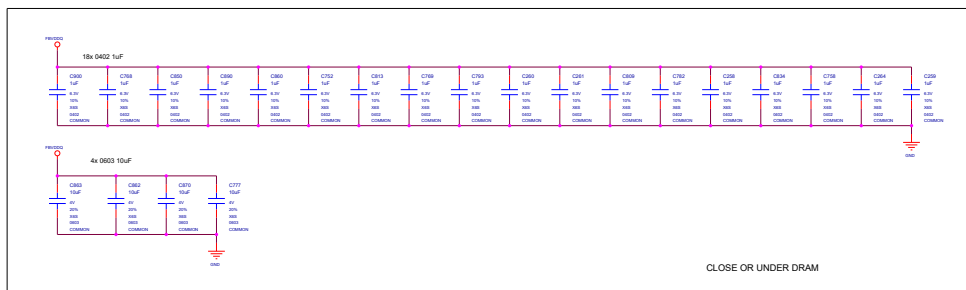
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PCIE GEN4	PCIE GEN4 RC TERMINATIONS

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	4 OF 24
PCB REV	76142B00	DATE	27-JUN-2017
SDR REV	A		



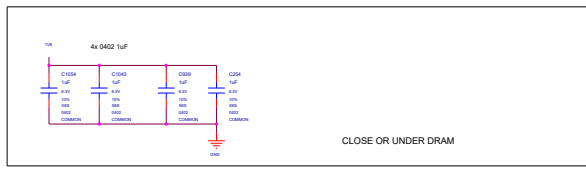
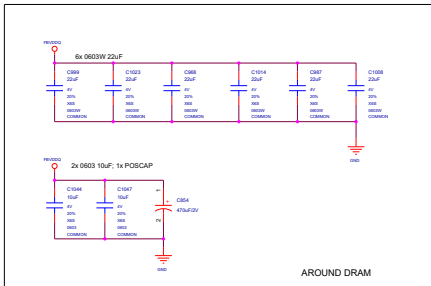
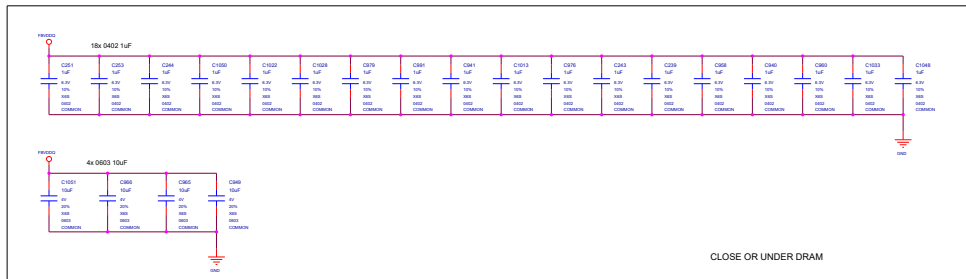
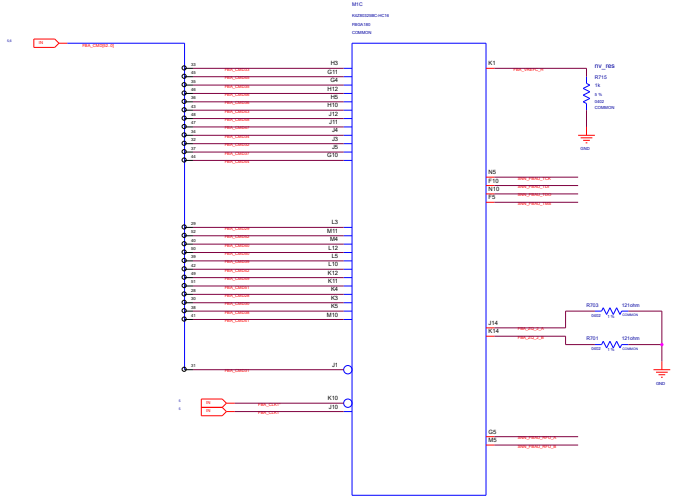
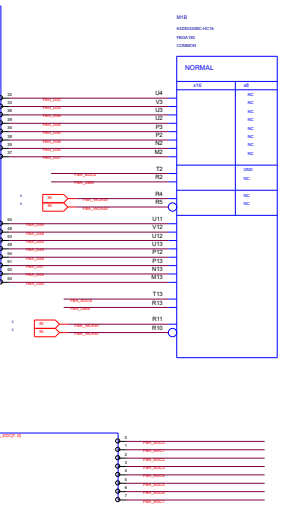
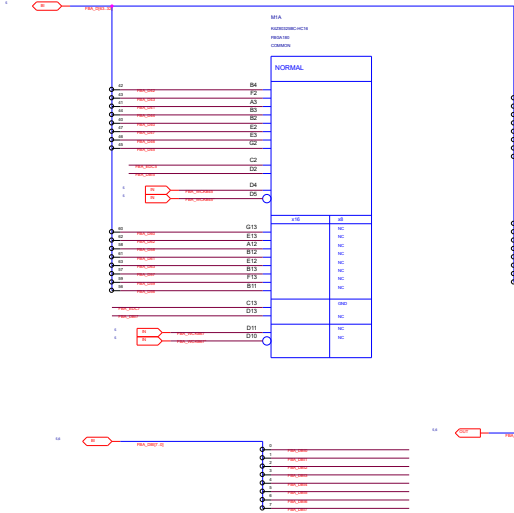
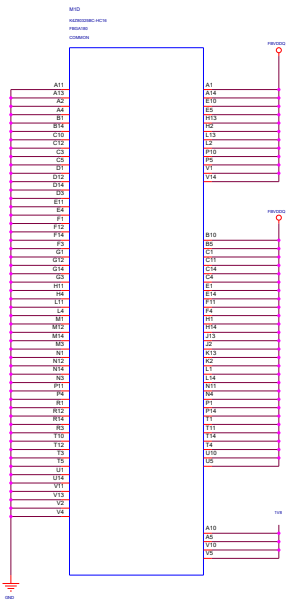


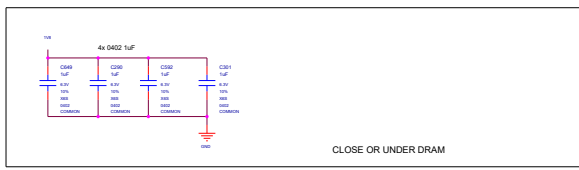
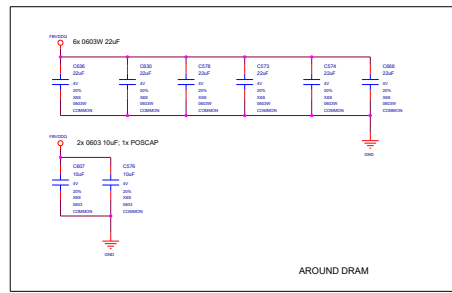
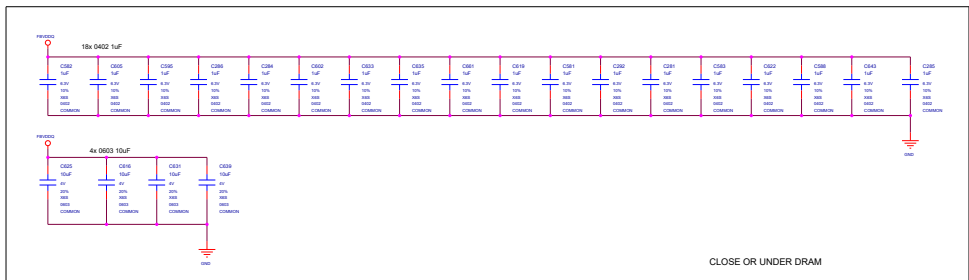
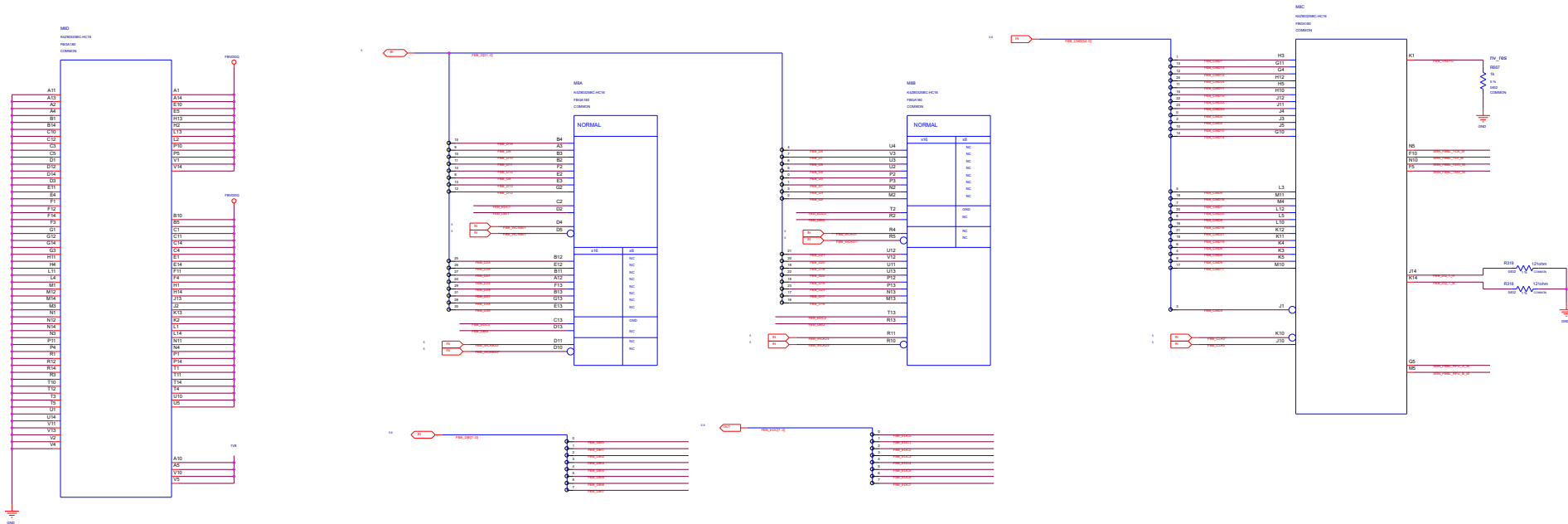
decap via : at least 2 grd vias and 2 power vias for each cap

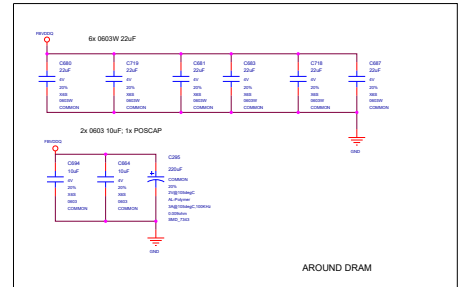
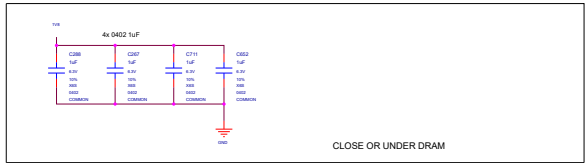
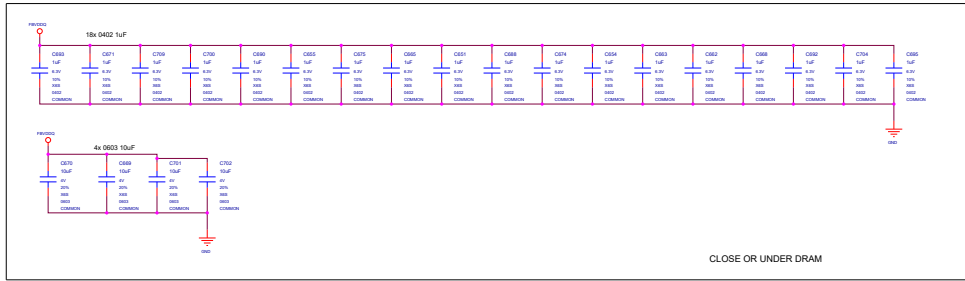
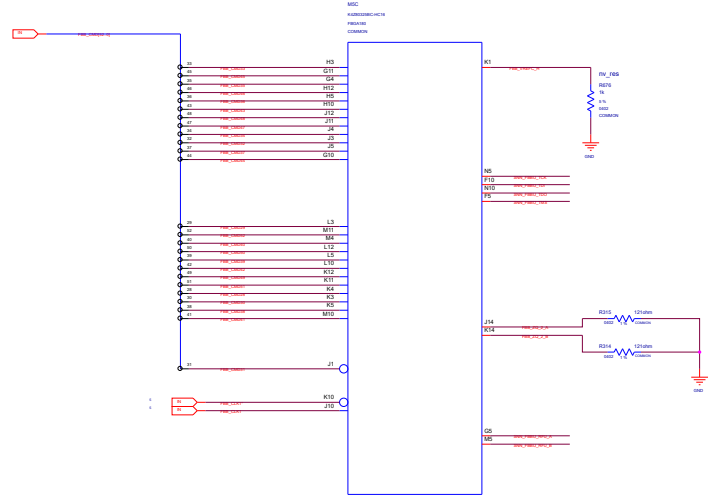
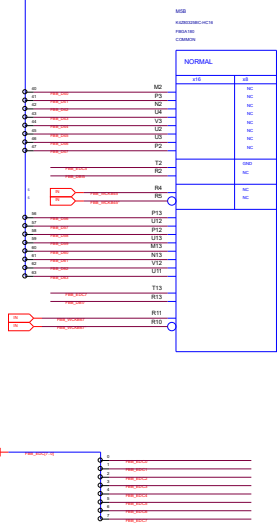
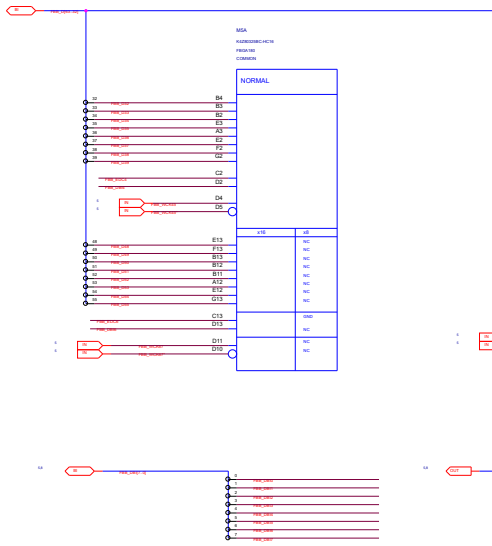
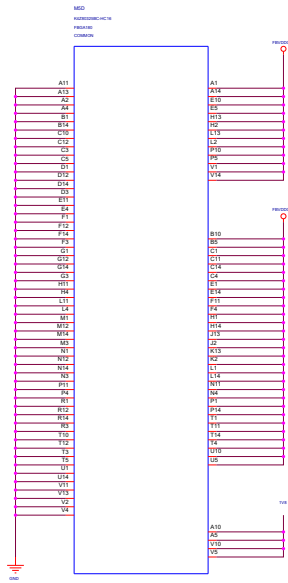


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FILE LOCAL	MEMORY HEALTH

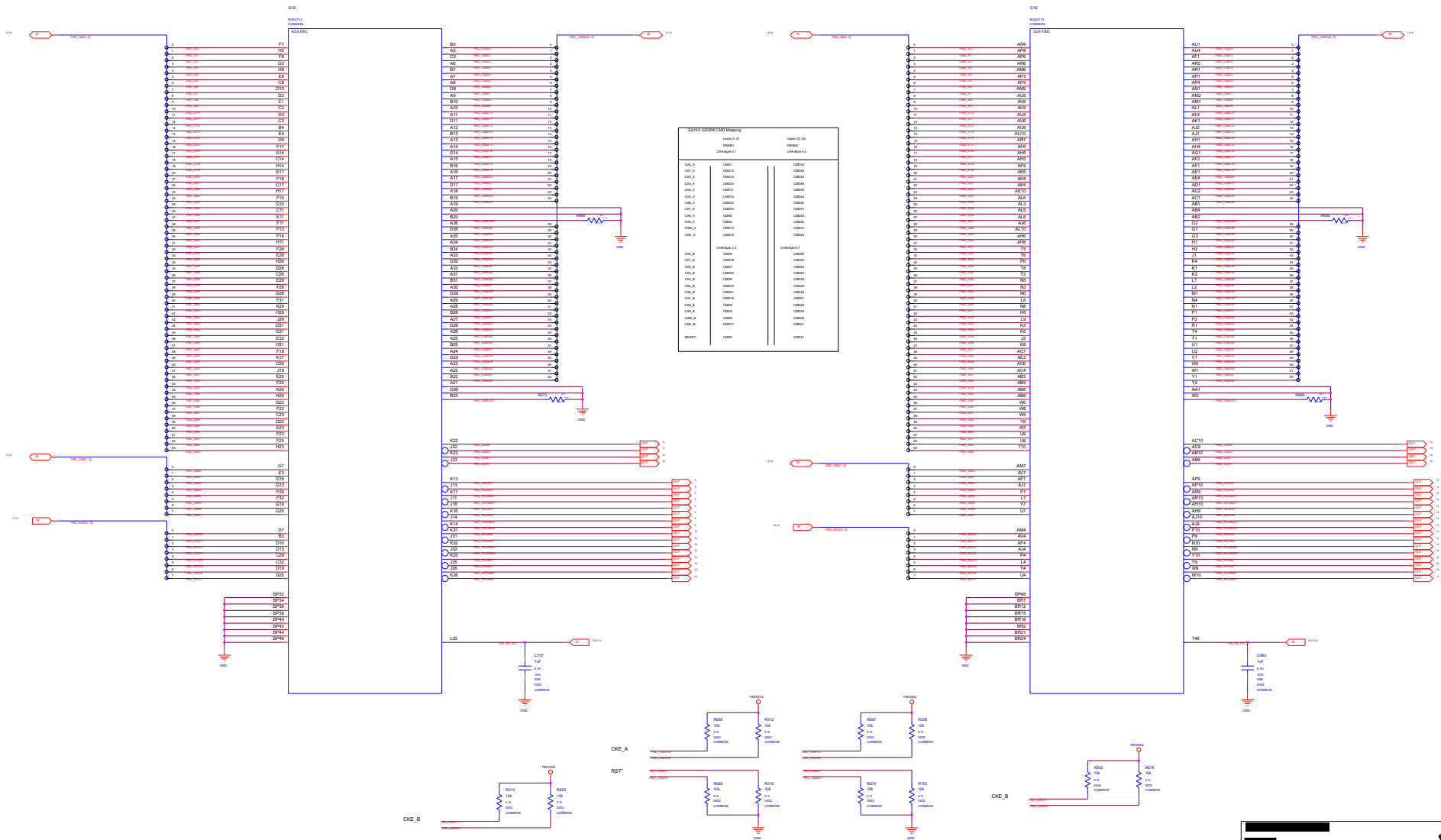
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NV_PN	600-1G142-BASE-100		
PCB rev	76142B00	PAGE	6 OF 24
SD rev	A	DATE	27-JUN-2007





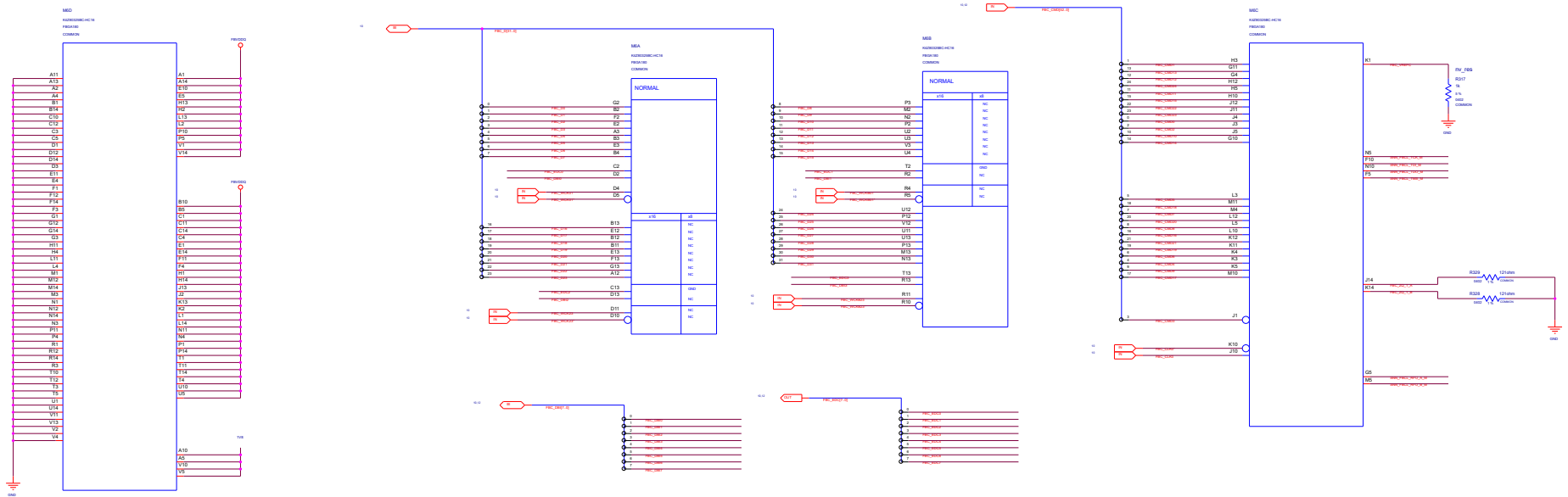


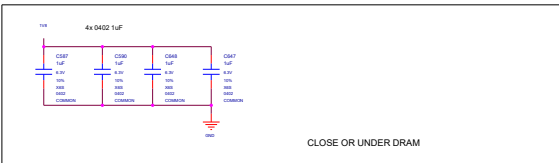
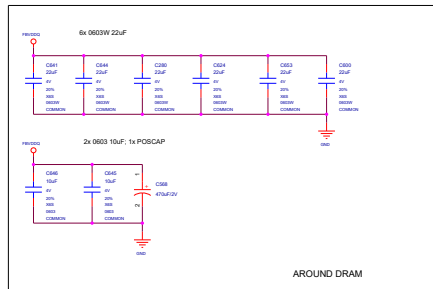
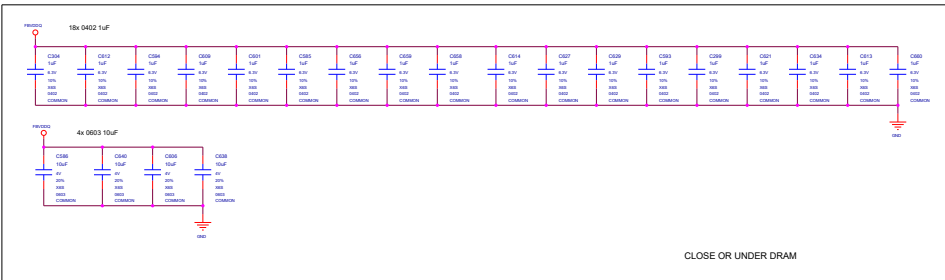
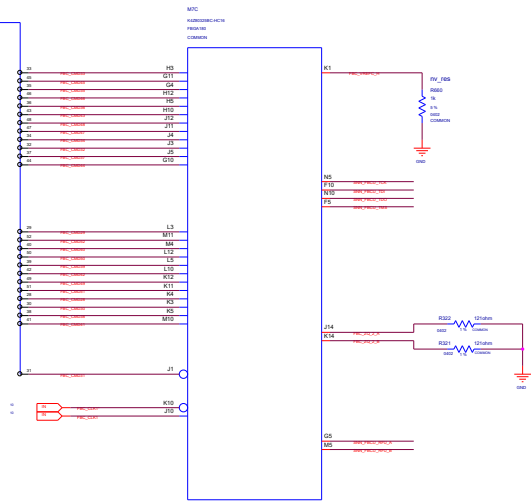
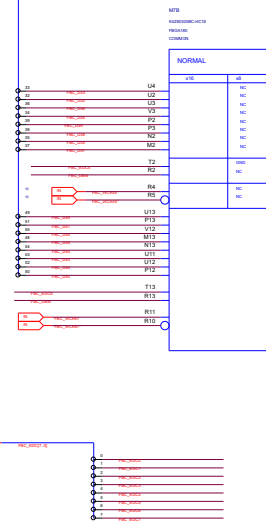
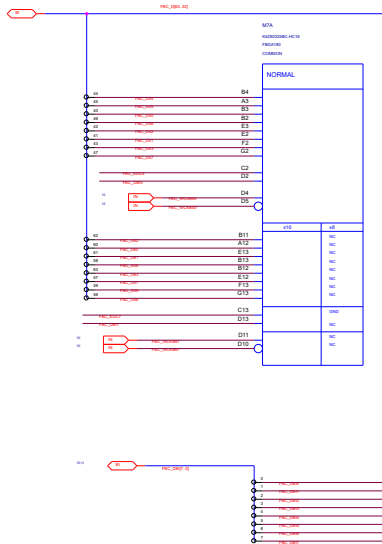
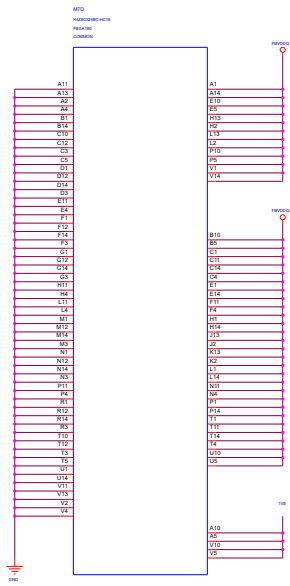
ASSEMBLY	ASSEMBLY DESCRIPTION	NV_PN	600-1G142-BASE-100
FILE LOCAL	MEMORY FRAMES	PCB REV	76142B00
		DATE	27-JUN-2007
		PAGE	9 OF 24

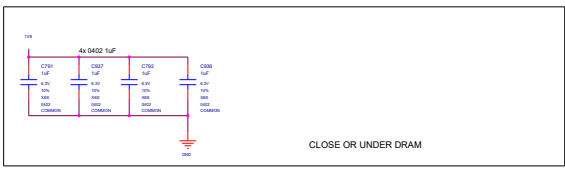
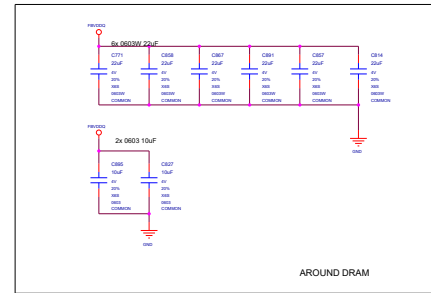
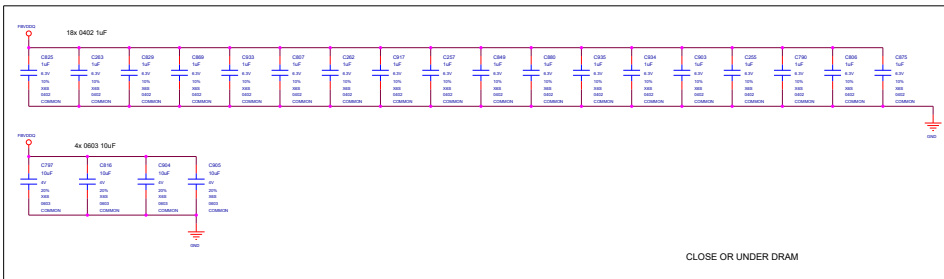
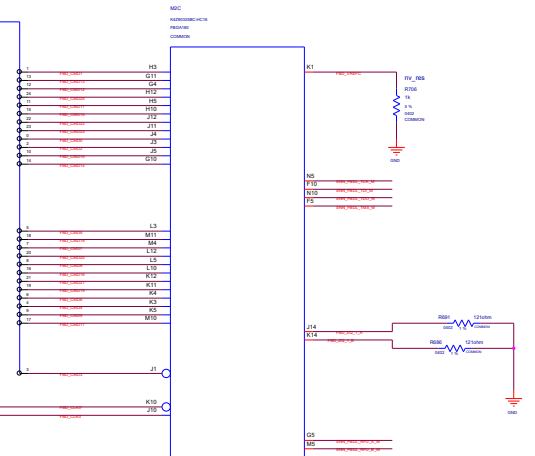
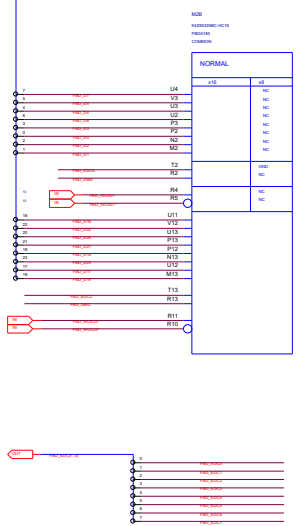
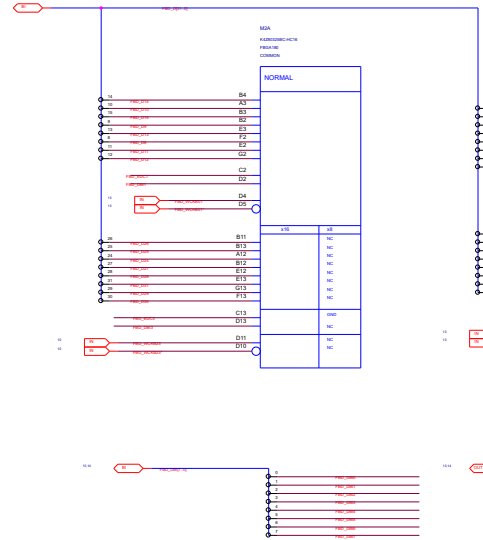
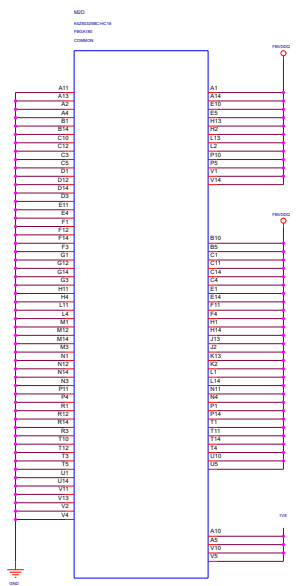


MEMORY BANK PIN MAPPING

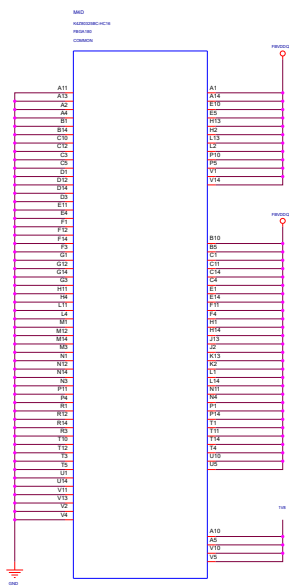
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Bank 0-15	BANK_0	BANK_16	BANK_16
	BANK_1	BANK_17	BANK_17
	BANK_2	BANK_18	BANK_18
	BANK_3	BANK_19	BANK_19
	BANK_4	BANK_20	BANK_20
	BANK_5	BANK_21	BANK_21
	BANK_6	BANK_22	BANK_22
	BANK_7	BANK_23	BANK_23
	BANK_8	BANK_24	BANK_24
	BANK_9	BANK_25	BANK_25
	BANK_10	BANK_26	BANK_26
	BANK_11	BANK_27	BANK_27
	BANK_12	BANK_28	BANK_28
	BANK_13	BANK_29	BANK_29
	BANK_14	BANK_30	BANK_30
Bank 16-31	BANK_16	BANK_31	BANK_31
	BANK_17	BANK_32	BANK_32
	BANK_18	BANK_33	BANK_33
	BANK_19	BANK_34	BANK_34
	BANK_20	BANK_35	BANK_35
	BANK_21	BANK_36	BANK_36
	BANK_22	BANK_37	BANK_37
	BANK_23	BANK_38	BANK_38
	BANK_24	BANK_39	BANK_39
	BANK_25	BANK_40	BANK_40
	BANK_26	BANK_41	BANK_41
	BANK_27	BANK_42	BANK_42
	BANK_28	BANK_43	BANK_43
	BANK_29	BANK_44	BANK_44

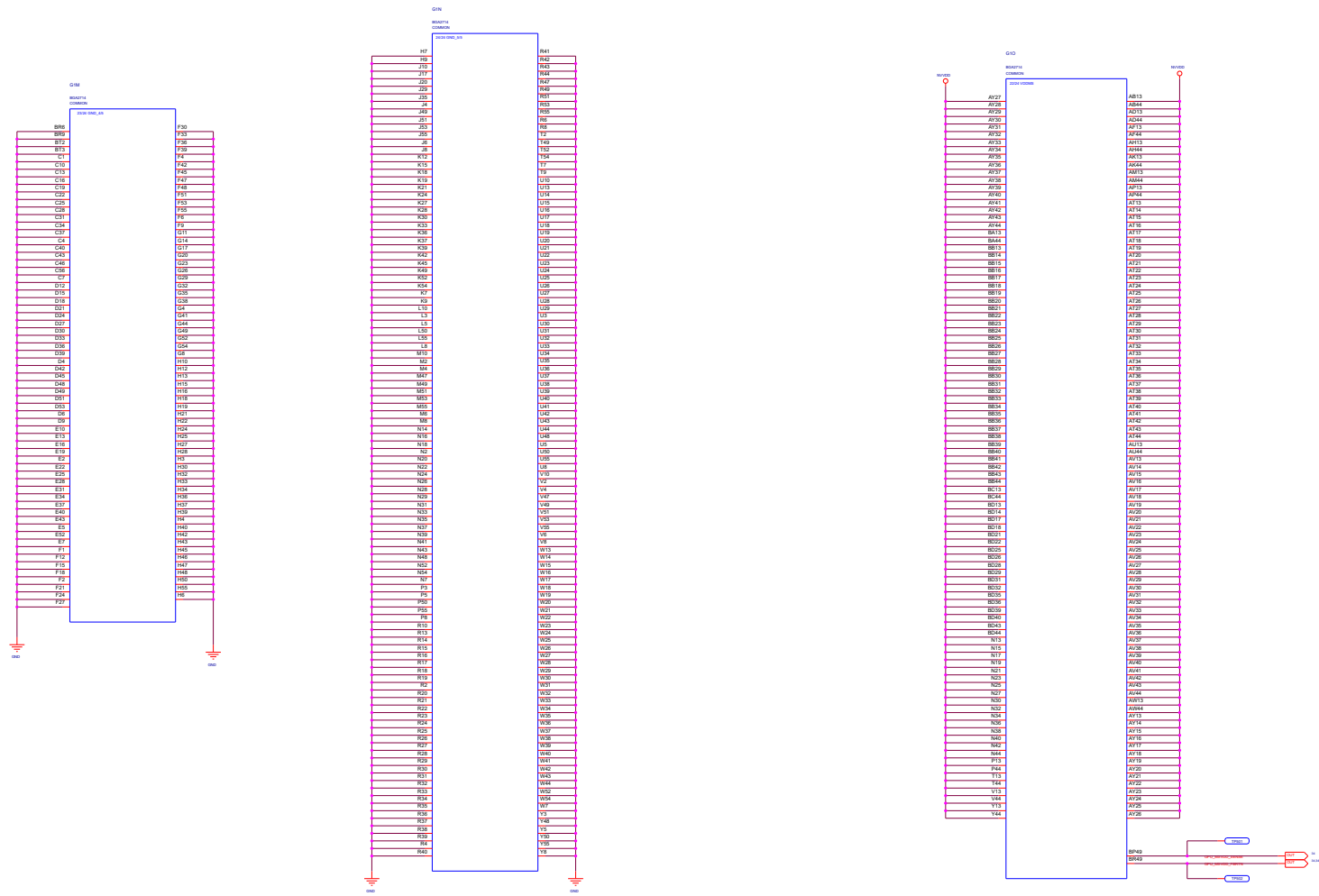






ASSEMBLY	ASSEMBLY DESCRIPTION	NV_PN	600-1G142-BASE-100
FILE LOCAL	MEMORY (FBD) (1)	PCB REV	76142B00
		REV	A
		DATE	27-JUN-2007
		PAGE	13 OF 24

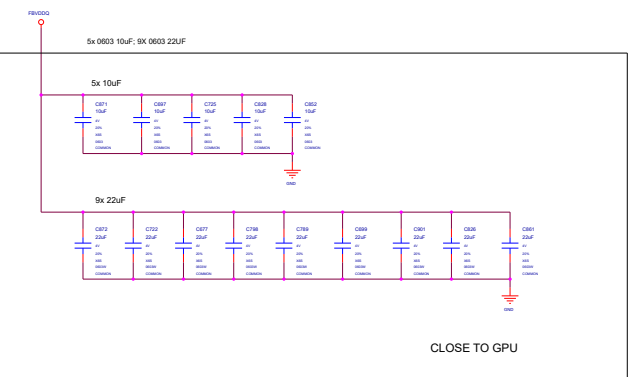
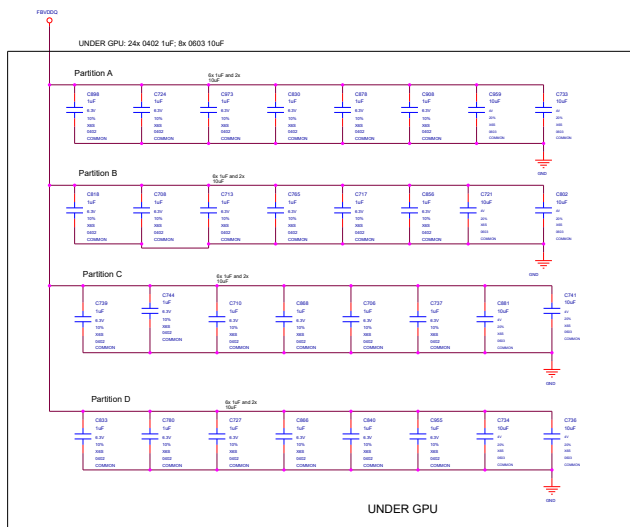




ASSEMBLY	ASSEMBLY DESCRIPTION
GPU PWR & GND	

[REDACTED]		[REDACTED]	
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PCB REV	70142B00	W OF 24	
SDR REV	A		

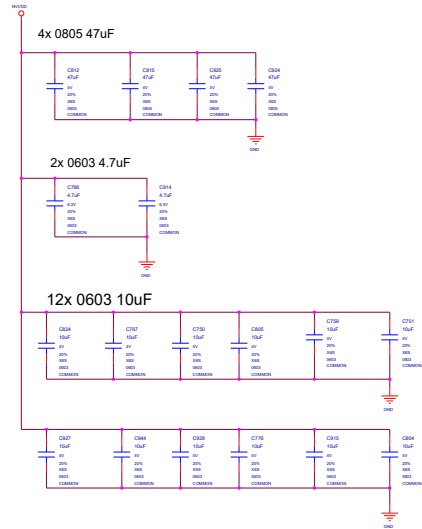
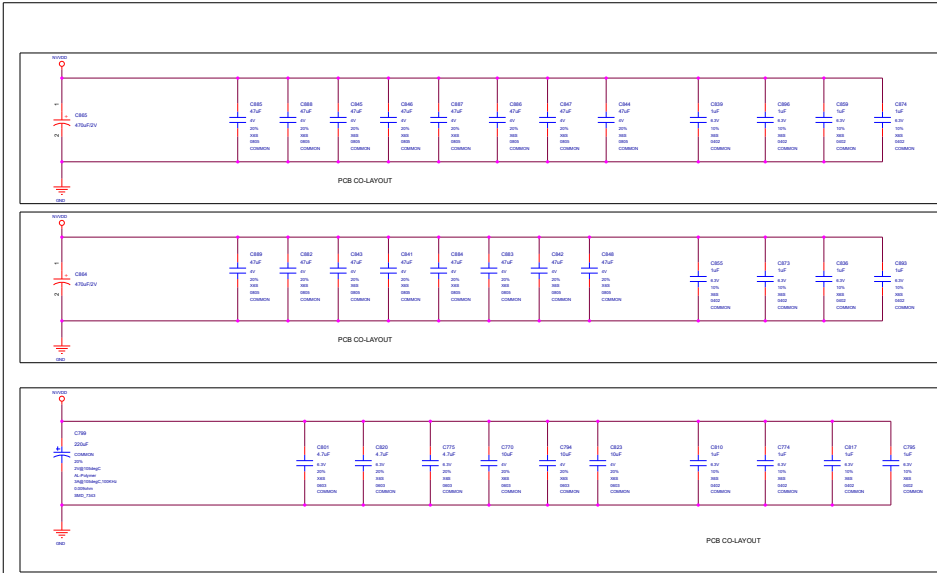
FBVDDQ



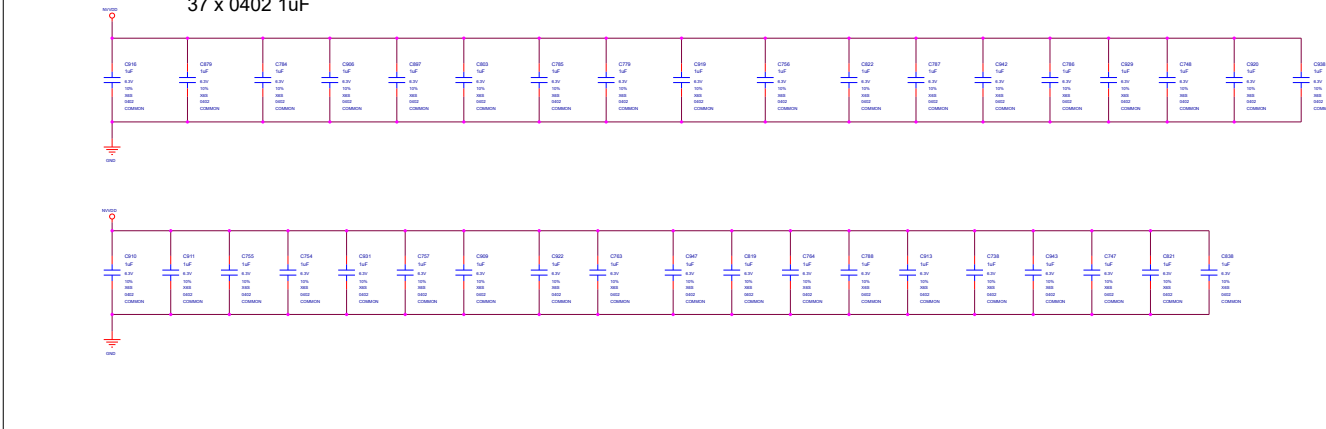
ASSEMBLY	ASSEMBLY DESCRIPTION
TRIAL DATA	GPU DECOUPLING FBVDDQ

[REDACTED]		[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100				
PCB Rev	76142B00	PAGE	18 OF 24		
SDV Rev	A	DATE	27-JUN-2007		





37 x 0402 1uF

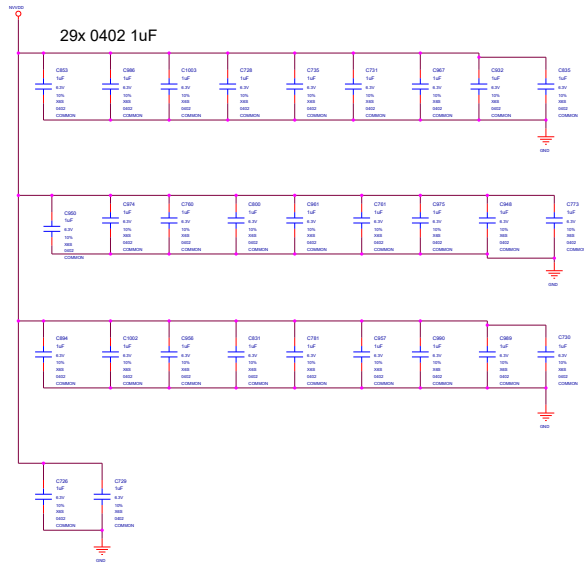
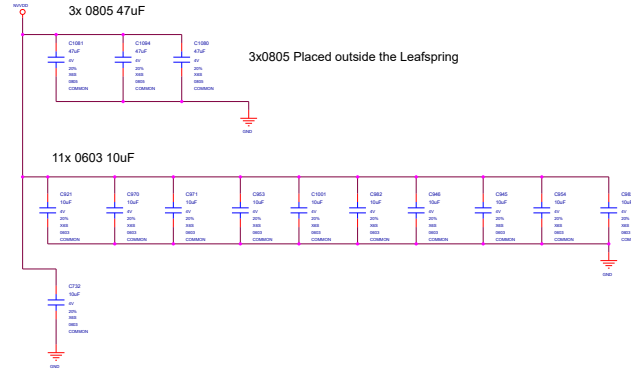
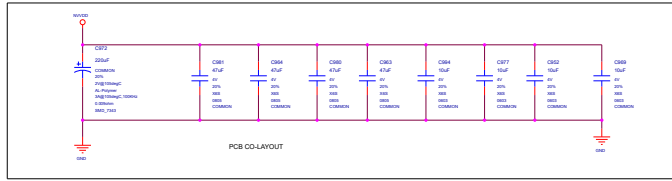


UNDER GPU

ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DESIGN	GPU DECOUPLING NVVDD

[REDACTED]		[REDACTED]	
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PCB REV	76142B00	PAGE	19 OF 24
DATE	27-JUN-2007		



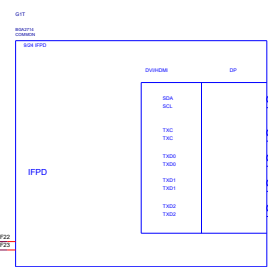
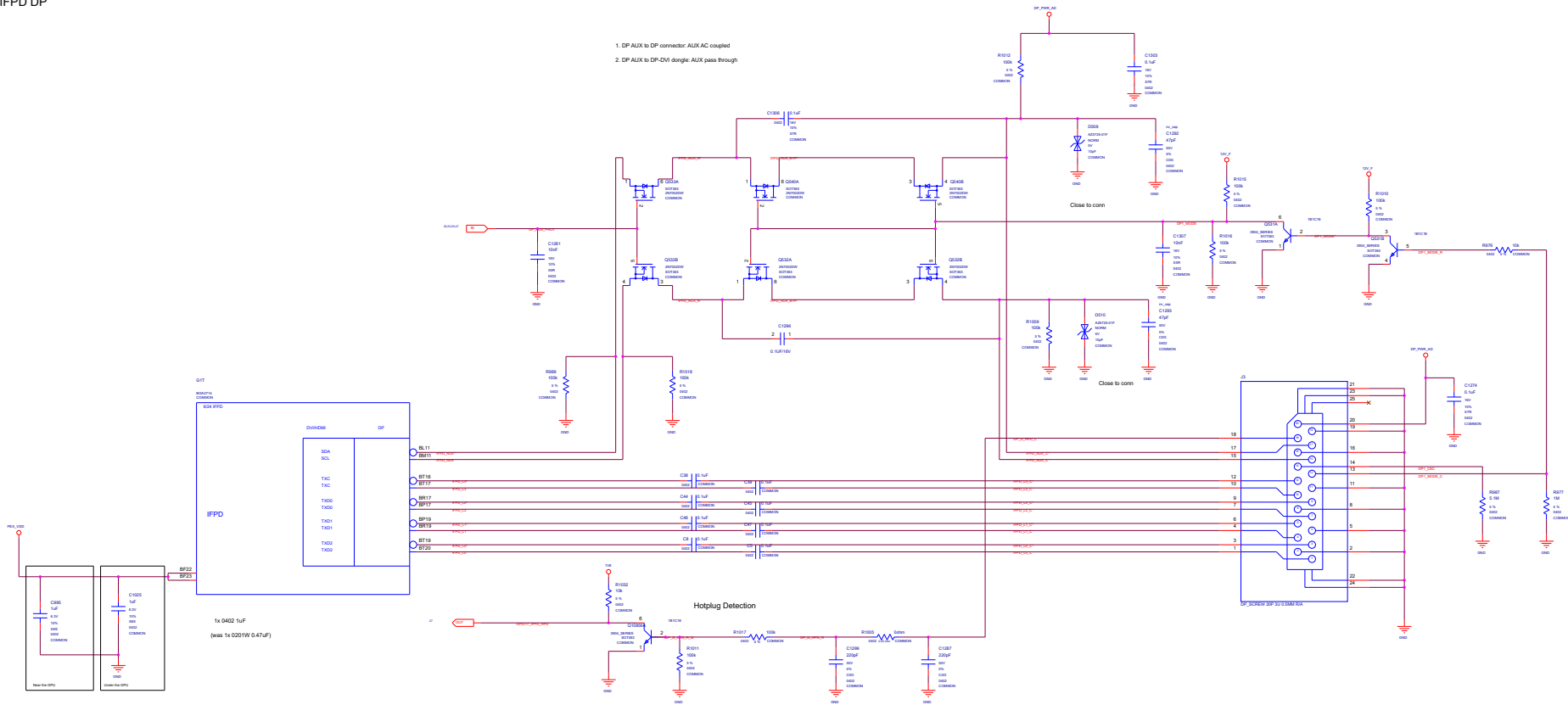


UNDER GPU

ASSEMBLY	ASSEMBLY DESCRIPTION	[REDACTED]	
PCB DETAIL	GPU DECOUPLING REVISED	[REDACTED]	
NV_P/N	600-1G142-BASE-100	DATE	27-JUN-2007
PCB REV	76142B30	PAGE	20 OF 24
SDR REV	A	DATE	27-JUN-2007

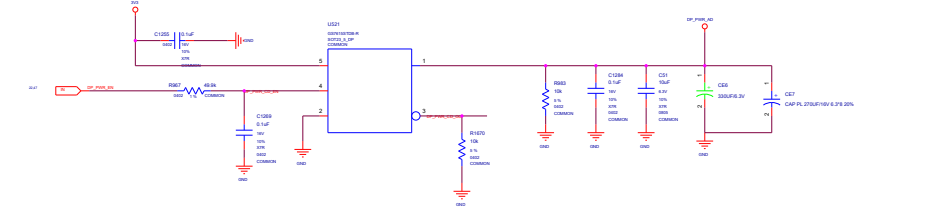


- 1. DP AUX to DP connector AUX AC coupled
- 2. DP AUX to DP-DVI dongle: AUX pass through



1x 5402 1uF
(use 1x 0201W 0.47uF)

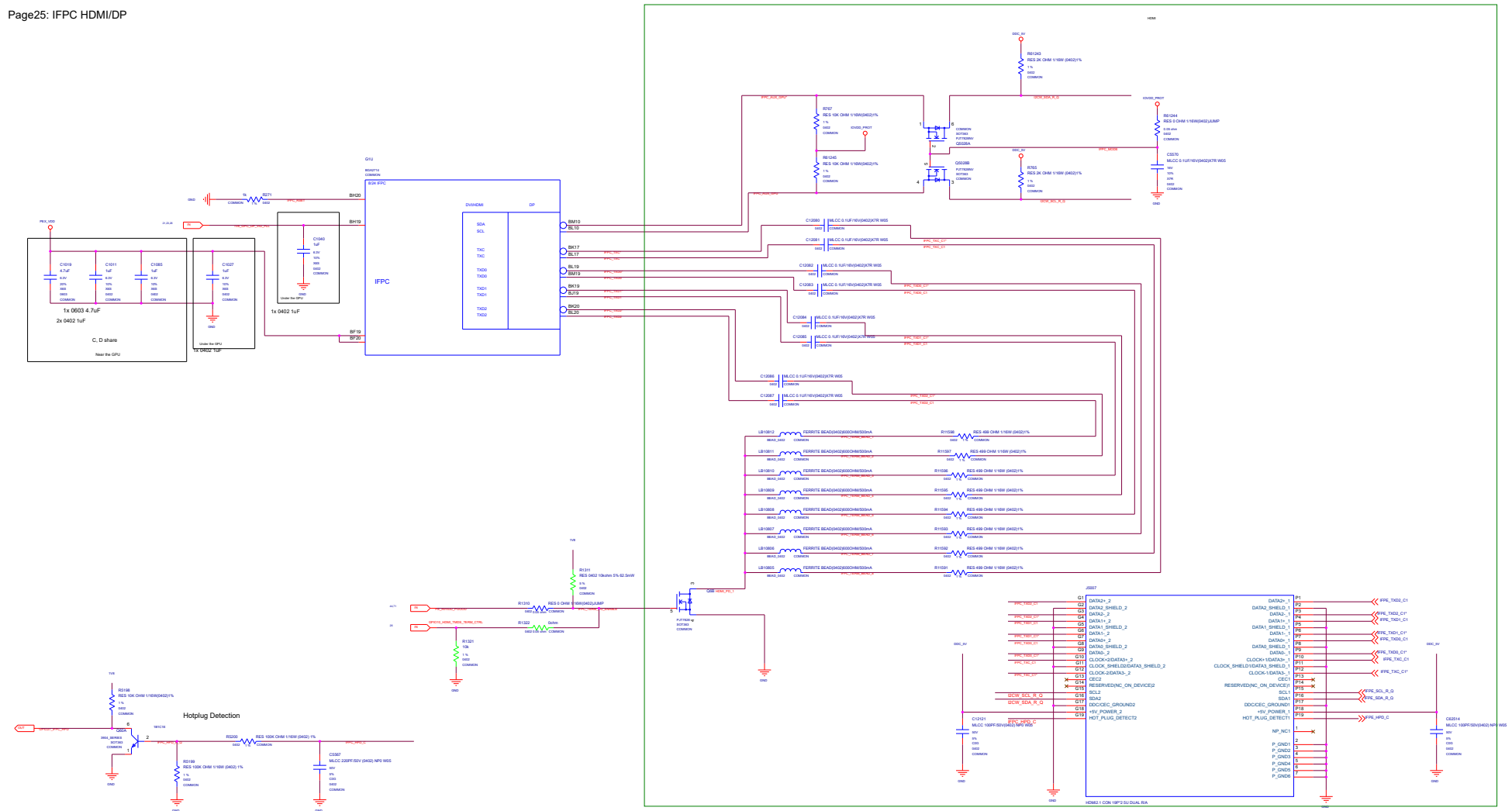
Fused DP_PWR



ASSEMBLY	ASSEMBLY DESCRIPTION
TABLE DETAIL	

ID: IFPD DP

[REDACTED]		[REDACTED]	
NV_P/N	600-1G142-BASE-100		
PCB REV	T0142B00	PAGE	24 OF 24
SDR REV	A	DATE	

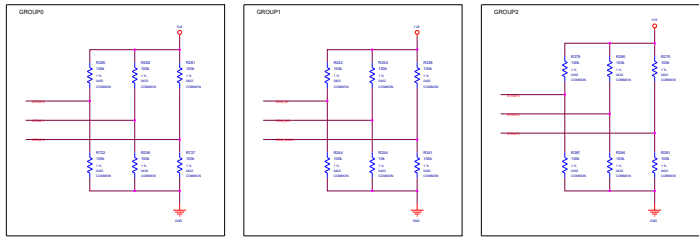


ASSEMBLY	ASSEMBLY_DESCRIPTION
FILE_LOCAL	IFPC_HDMI/DP

NV_PN	600-1G142-BASE-100
PCB Rev	TR142B00
SOA Rev	A
DATE	27-JUN-2007
PAGE	25 OF 24

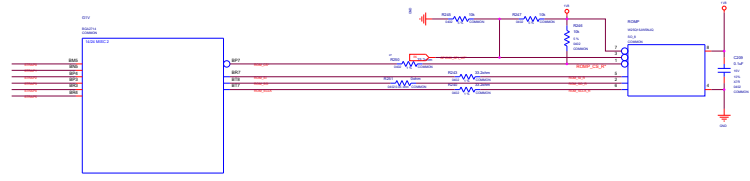
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L	L	L	0000	RAMCFG SAMSUNG 8GB 7GHz
L	L	H	0001	RAMCFG MICRON 8GB 7GHz
L	H	L	0010	RAMCFG HYUN 8GB 7GHz
H	H	L	0011	RAMCFG SAMSUNG 16GB 8GHz
TBD				

H:High Test to 1.8V
M:Middle Test to 0.9V
L:Low Test to 0V



ROM_CS	ROM_S	ROM_SCLK	SMARTFAND FS_OVERT	1 ENABLE 0 DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

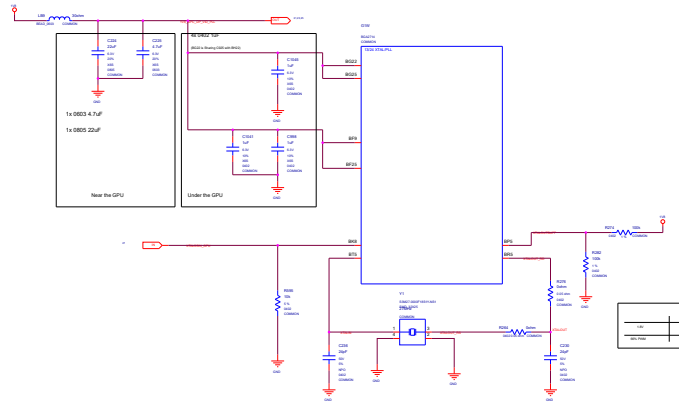
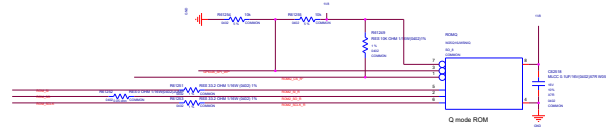
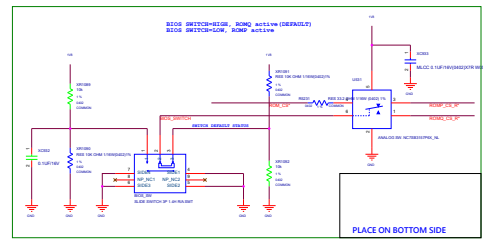
DEFAULT



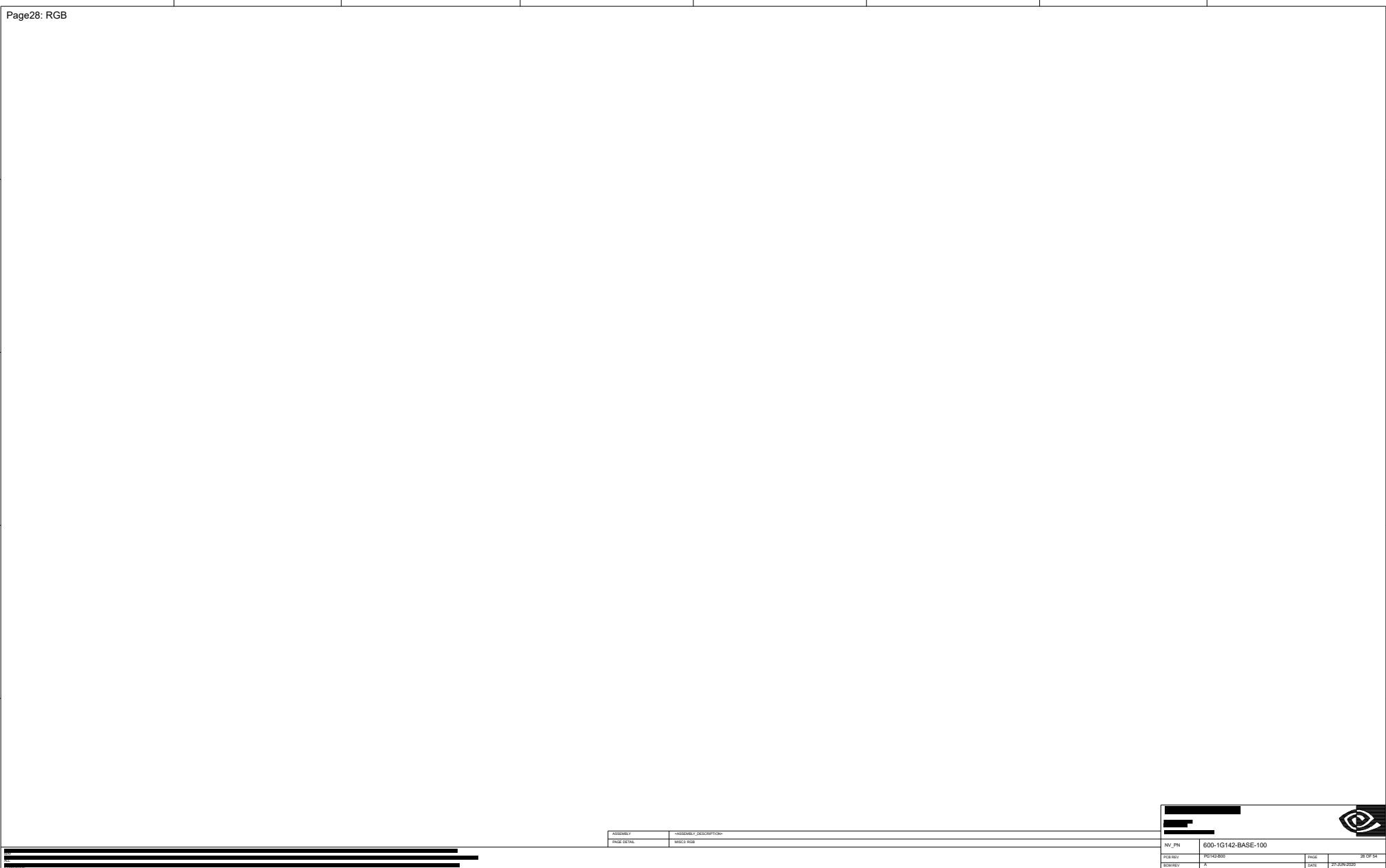
STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
L	L	L	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H:High Test to 1.8V
M:Middle Test to 0.9V
L:Low Test to 0V

1 SMB_ALT_ADDR ENABLE
0 SMB_ALT_ADDR DISABLE
1 DEVID_SEL RESFRMAD
0 DEVID_SEL_ORIGINAL
1 PCI_CFG LOW POWER
0 PCI_CFG HIGH POWER
1 VGA_DEVICE ENABLE
0 VGA_DEVICE_DISABLE



REVISION		
REV	DATE	DESCRIPTION



ASSEMBLY		ASSEMBLY DESCRIPTION		[REDACTED]	
PART DETAIL		MISC. RIB		[REDACTED]	
NV_PN	600-1G142-BASE-100				
PCB REV	70142B00				
REV	A	DATE	27-JUN-2007	PAGE	28 OF 24



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ASSEMBLY	ASSEMBLY DESCRIPTION	[REDACTED]		
PTRK DETAIL	BLANK PAGE	[REDACTED]		
NV_PN	600-1G142-BASE-100	PAGE	35 OF 34	
PCB REV	76142B01	DATE	27-JUN-2007	
SDV REV	A			



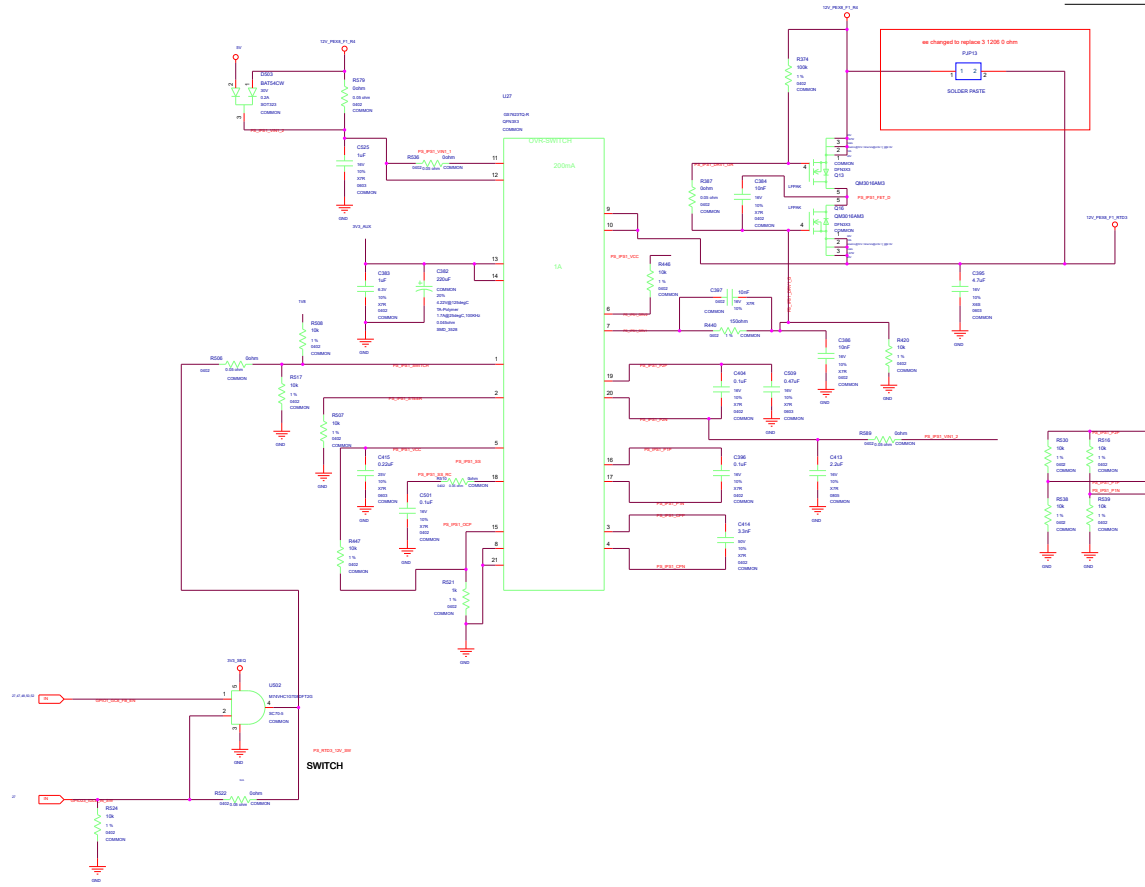
ASSEMBLY	ASSEMBLY DESCRIPTION
FRONT DETAIL	DC-DC INPUT POWER BAL SWICH

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	42 OF 54
PCB REV	70142B00	DATE	27-JUN-2007
SDR REV	A		



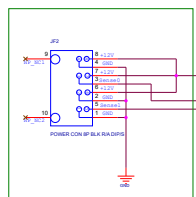
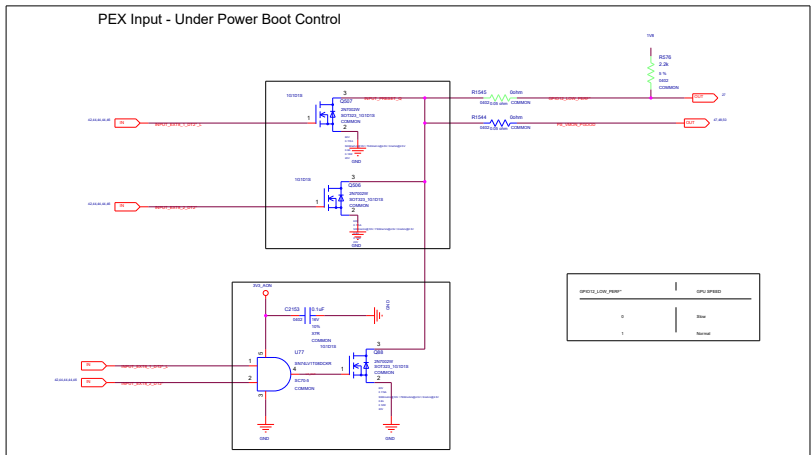
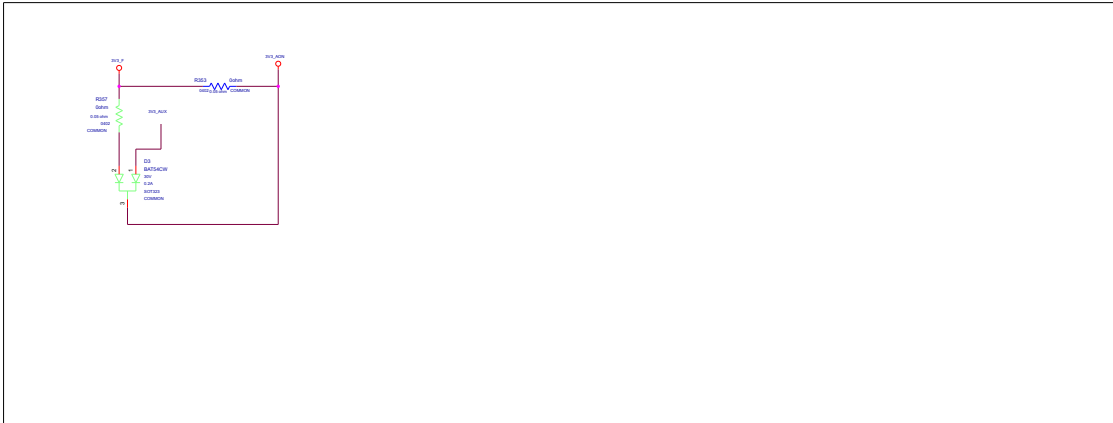
AND GATE LOGIC

GPI01	GPI029	SWITCH	VOUT	SWITCH	VOUT
0	0	0	12V	0	VOUT = VIN1
0	1	0	12V	1	VOUT = VIN2
1	0	0	12V		
1	1	1	3V3A		

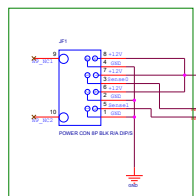


ASSEMBLY	ASSEMBLY DESCRIPTION
PNL03.001A	SW: RTD3 - 12V & 3V3A

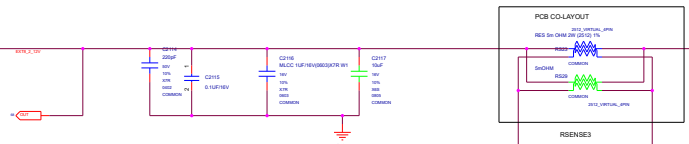
[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	43 OF 54
PCB rev	76142B00	DATE	27-JUN-2007
SD rev	A		



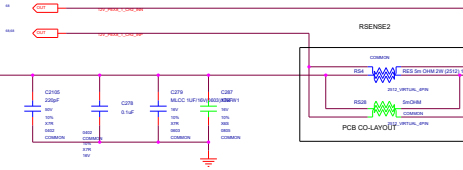
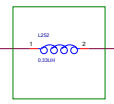
PEX8 INPUT 2 - 2x4 PCIe CON 150W



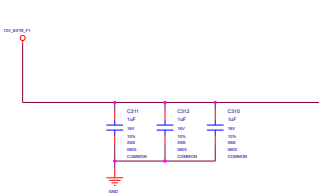
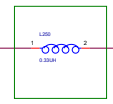
PEX8 INPUT 1 - 2x4 PCIe CON 150W



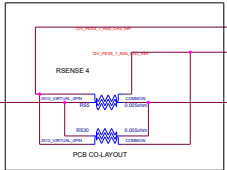
PCB CO-LAYOUT
RES 5k OHM 5% (2512) 1%
RSENSE3



PCB CO-LAYOUT
RES 5k OHM 5% (2512) 1%
RSENSE2



PCB CO-LAYOUT
RES 5k OHM 5% (2512) 1%
RSENSE4



ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PCB INPUTS FILTERING AND MONITORING

[REDACTED]		[REDACTED]	
NV_P/N	600-1G142-BASE-100		
PCB REV	70142B00	PAGE	44 OF 54
SDY REV	A	DATE	27-JUN-2007



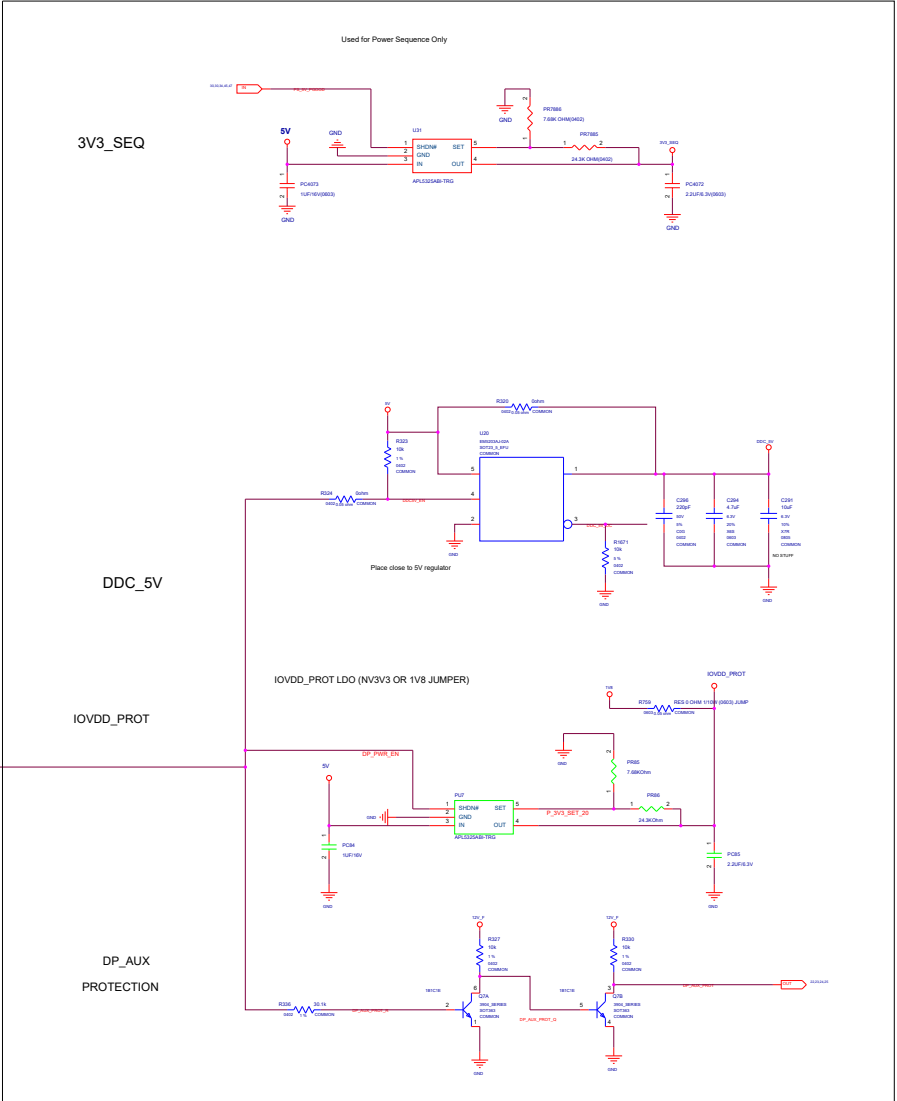
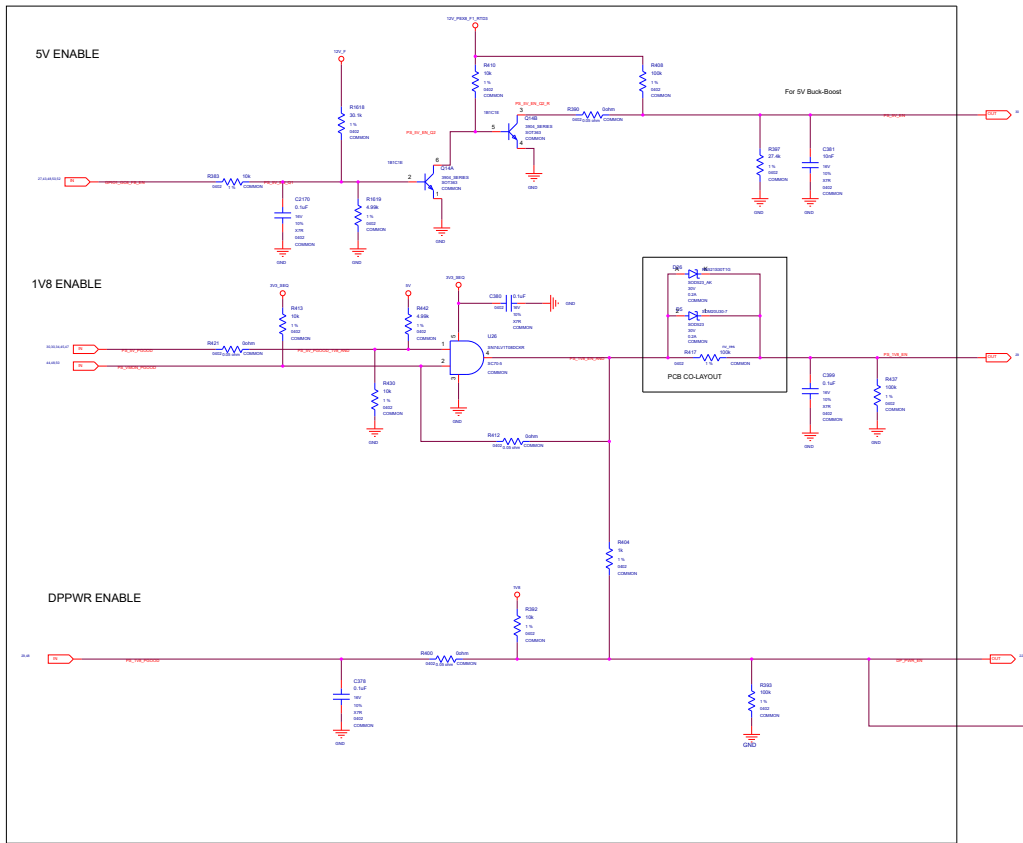
ASSEMBLY	ASSEMBLY DESCRIPTION
PIRE DETAIL	PIRE STEERING LINE HOT WIRE/PLUG

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	48 OF 54
PCB REV	70142B00	DATE	27-JUN-2007
SDW REV	A		



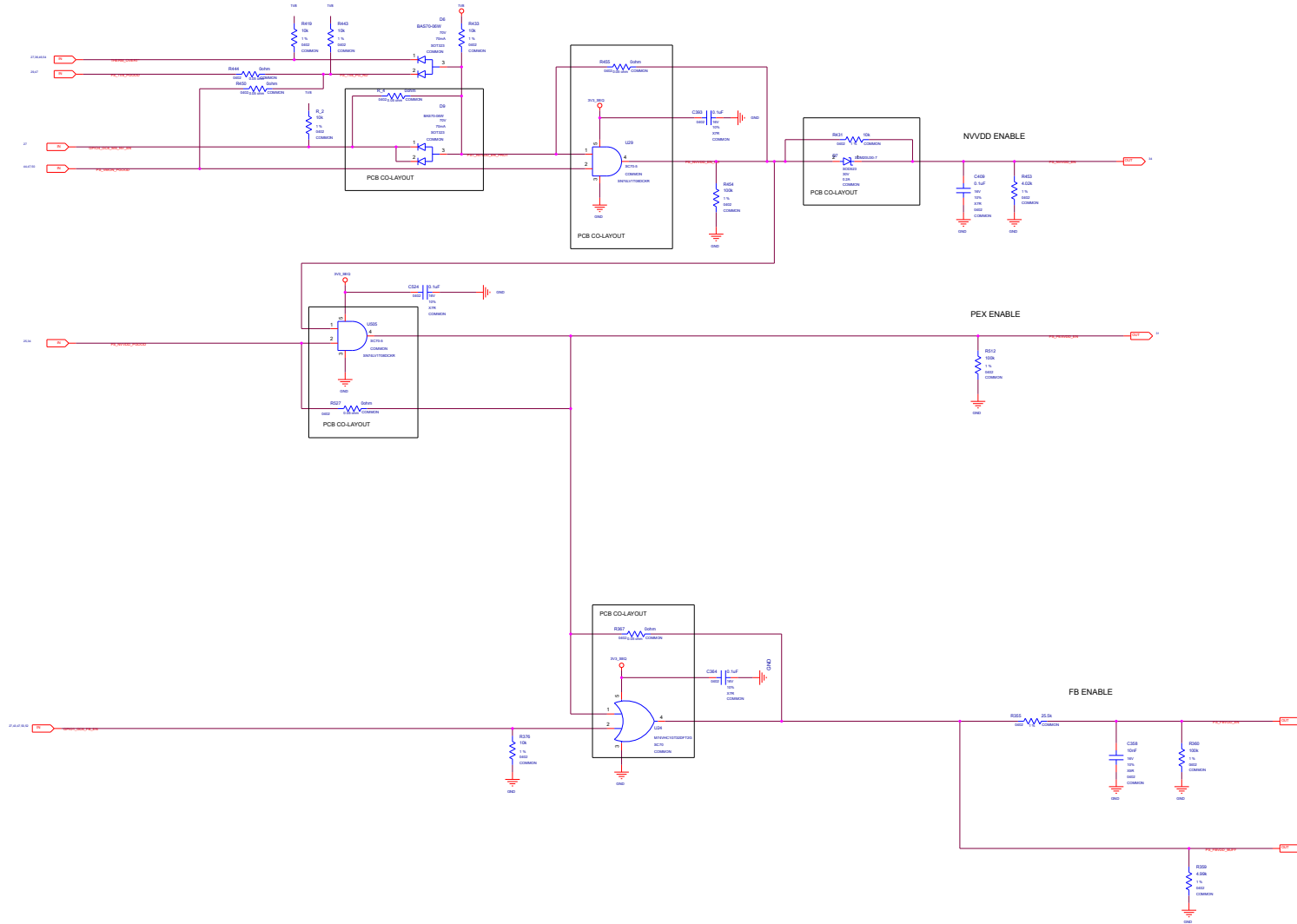
A B C D E F G H

[REDACTED]



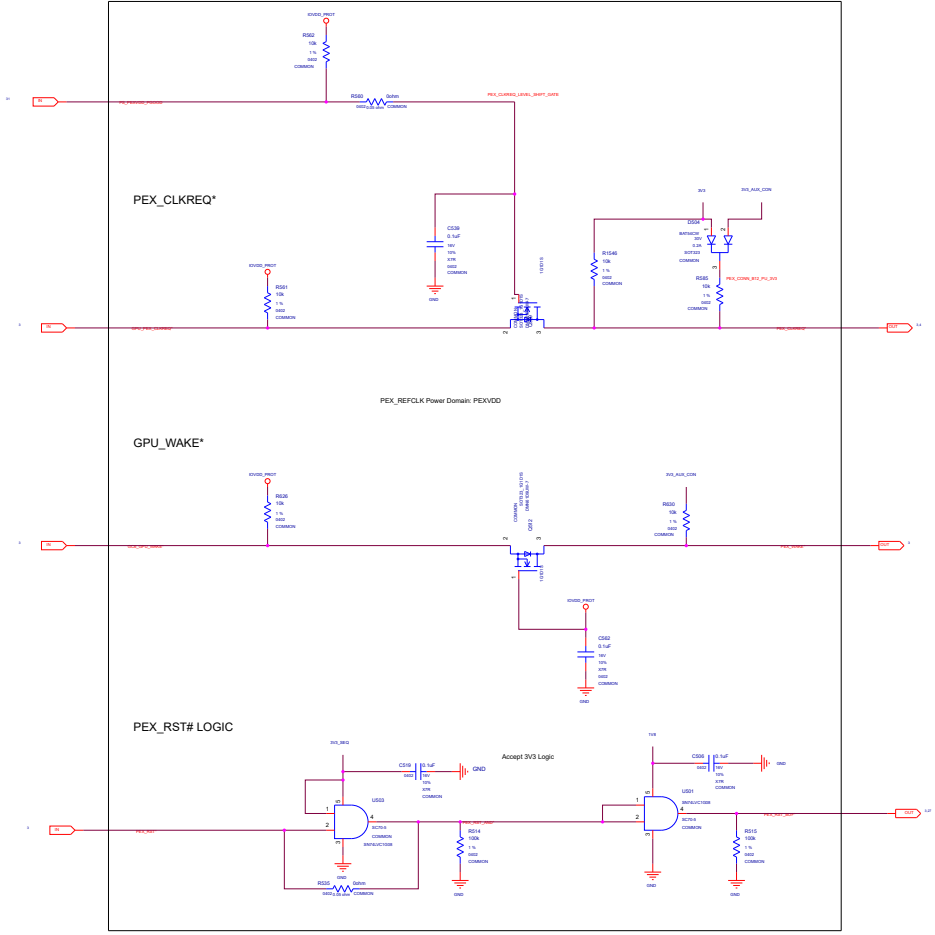
ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DESIGN	SEQ: 5V, 1V8, 3V3_SEQ

NV_PN	600-1G142-BASE-100
PCB REV	TG142B30
SDV REV	A
DATE	27-JUN-2007
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DESIGN	SEQ: NVVDD, PEX, FBVDDQ ENABLE

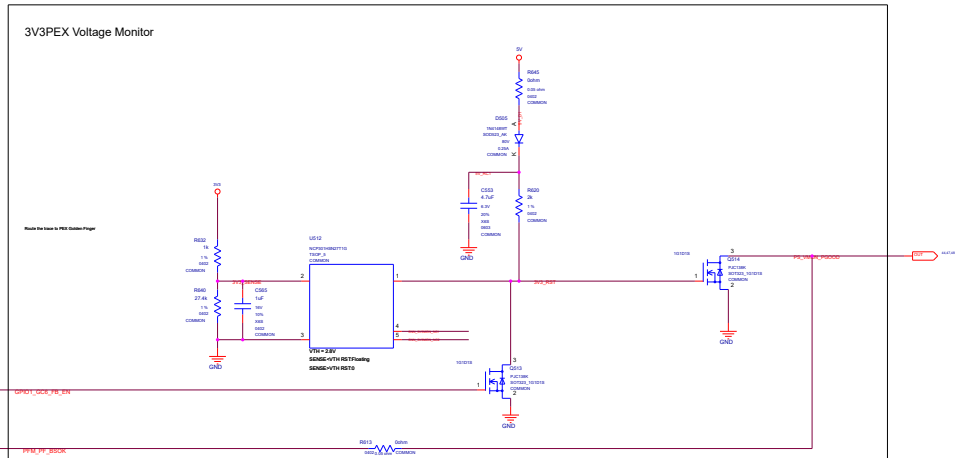
[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	DATE	27-JUN-2007
PCB REV	70142B00	PAGE	48 OF 54
SDV REV	A		



ASSEMBLY	ASSEMBLY DESCRIPTION
FILE: D:\A	SEQ: MISC

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	49 OF 54
PCB Rev	76142B00	DATE	27-JUN-2007
SDV Rev	A		





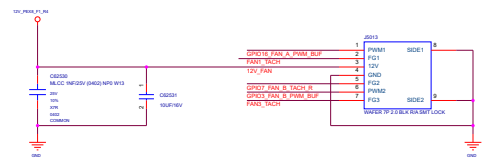
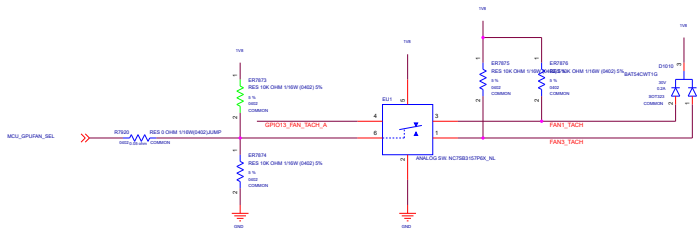
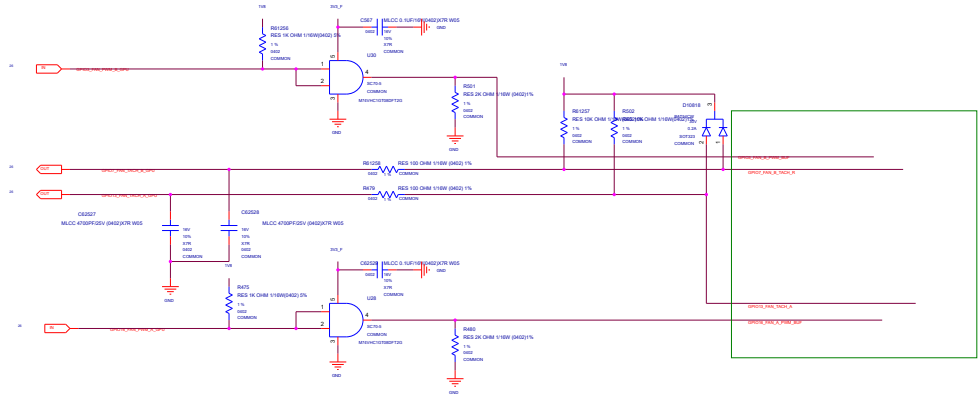
BOM Configuration

OPTIONS	PEX1V1_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PEX_VMON_POOOD	OPEN-DRAIN	Floating(I) once both 3V3 and 12V reach Vth
GOLDEN_EN	INPUT	Indicator for RTD3/GCE residence. Use to Mask the VMON_POOOD
PEX_FT_SHP	INPUT	From 9A3321(VP3) or Pre-Filter(SHP)
PEX_FT_BSDK	INPUT	From 9A3321(VP4) or Pre-Filter(BS_OK)

ASSEMBLY	ASSEMBLY DESCRIPTION
PRELIMINARY	3V3 VOLTAGE MONITOR

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	50 OF 54
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ASSEMBLY DESCRIPTION:
FAN & LED

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	31 OF 34
PCB rev	76142B01	DATE	27-JUN-2007
SD rev	A		

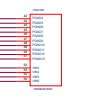
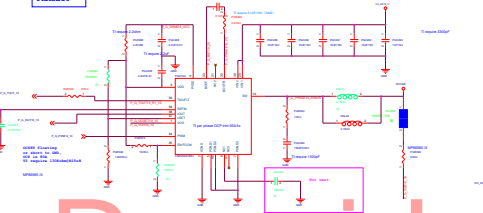
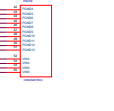
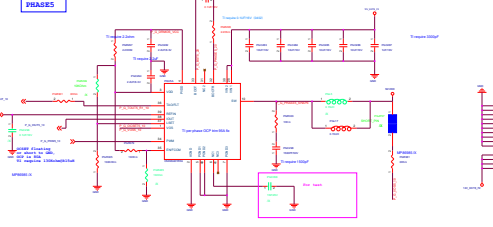
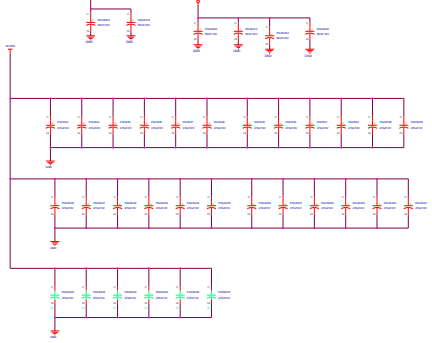
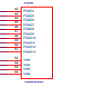
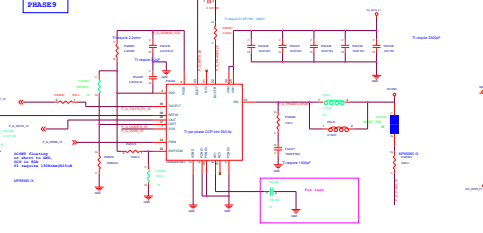
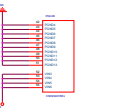
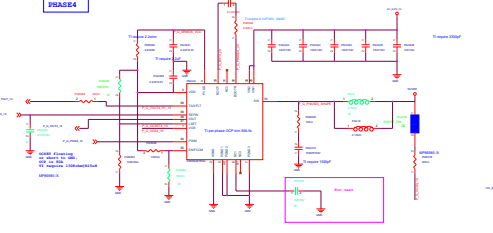
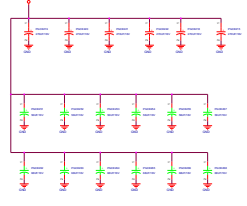
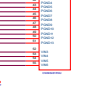
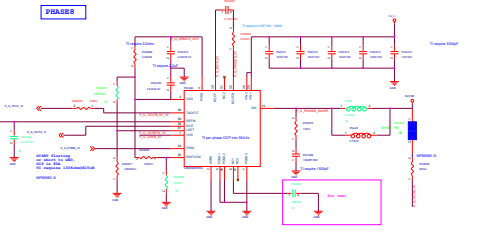
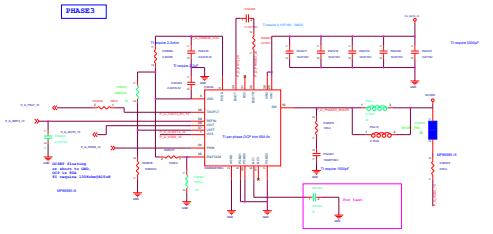
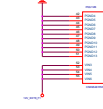
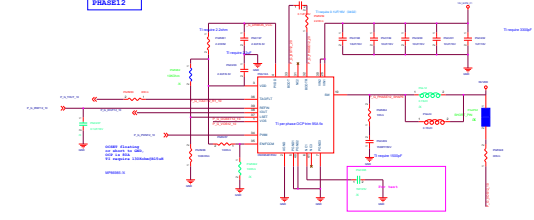
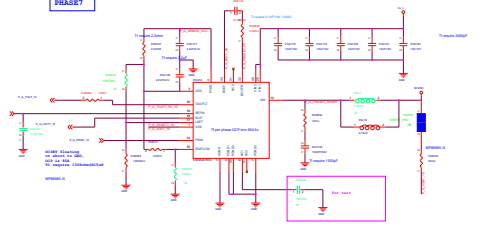
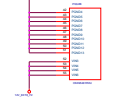
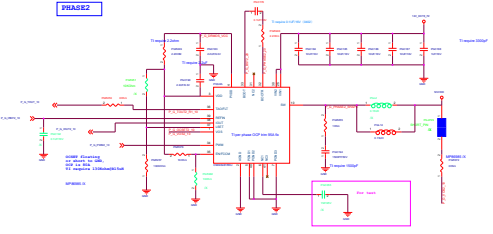
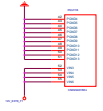
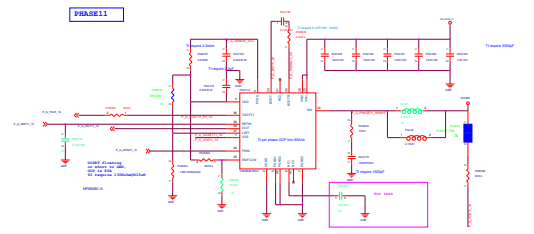
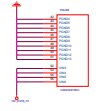
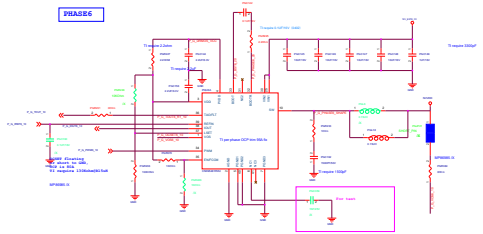
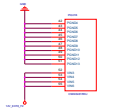
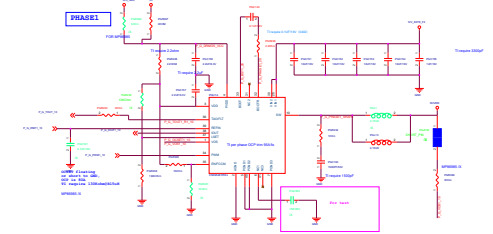


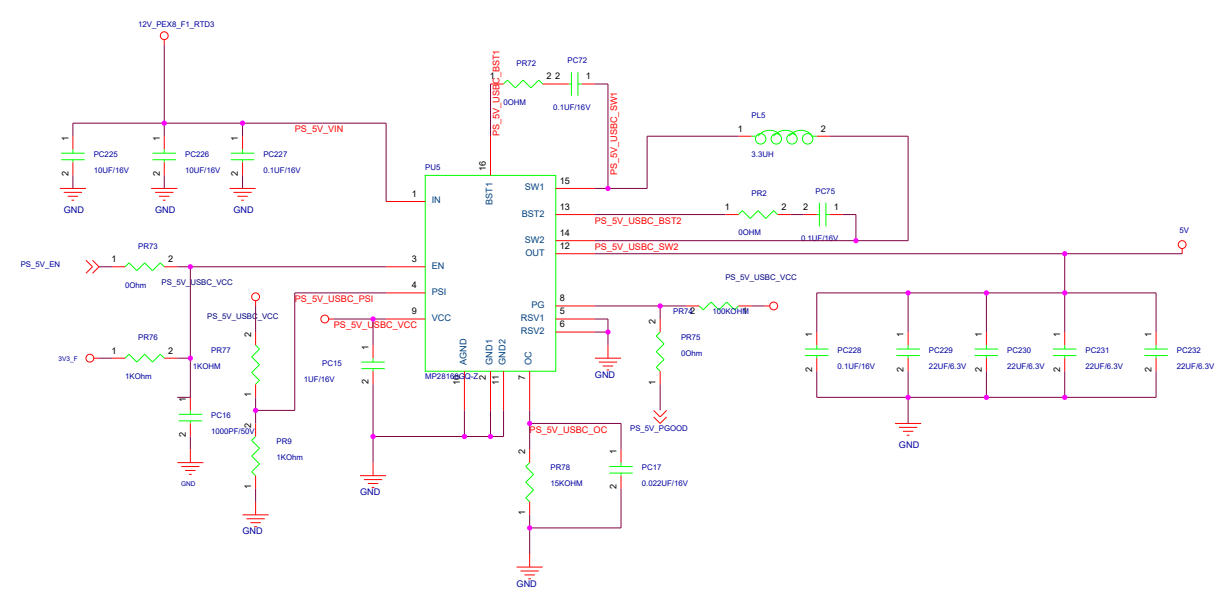
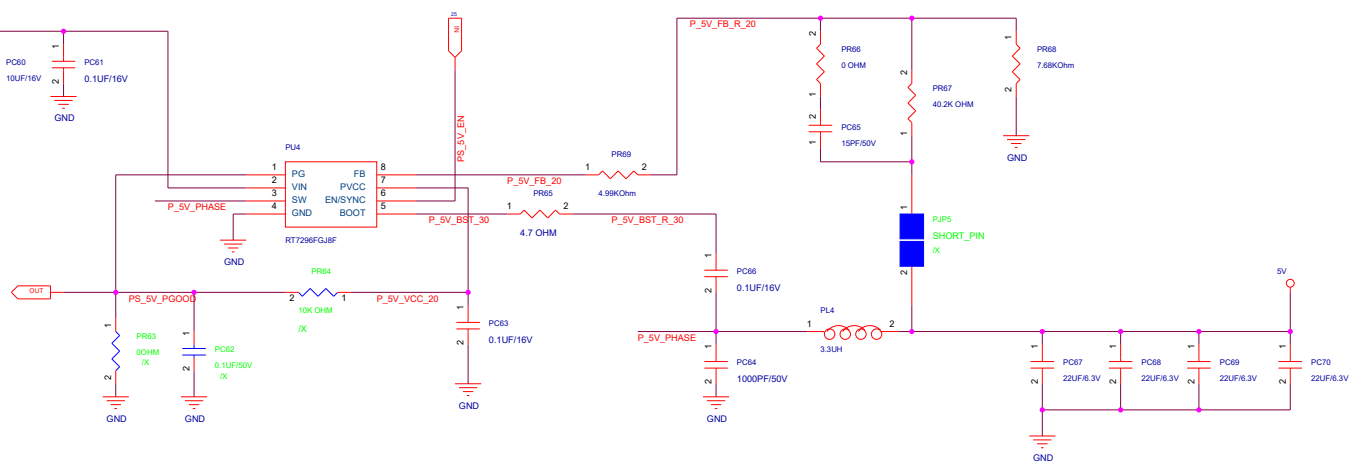
ASSEMBLY	ASSEMBLY DESCRIPTION
PTRK DETAIL	PTC

[REDACTED]		[REDACTED]	
NV_PN	600-1G142-BASE-100	PAGE	24 OF 24
PCB REV	70142B00	DATE	27-JUN-2007
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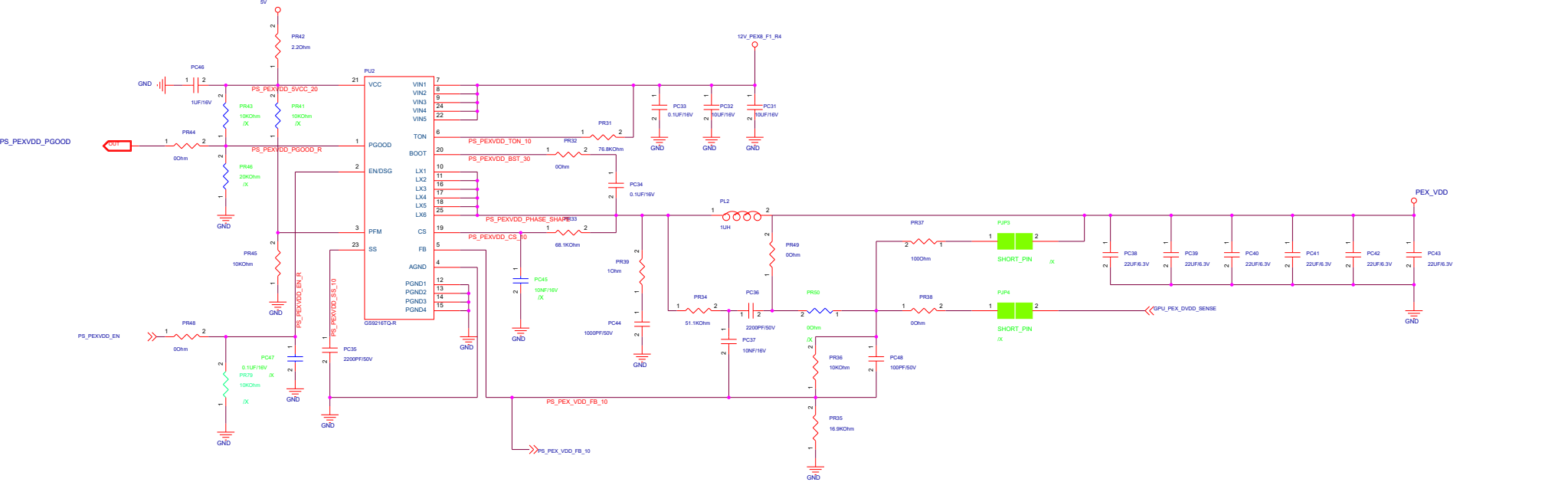


PHASE	TYPE	START	END
PHASE1	1	1	2
PHASE2	2	3	4
PHASE3	3	5	6
PHASE4	4	7	8
PHASE5	5	9	10

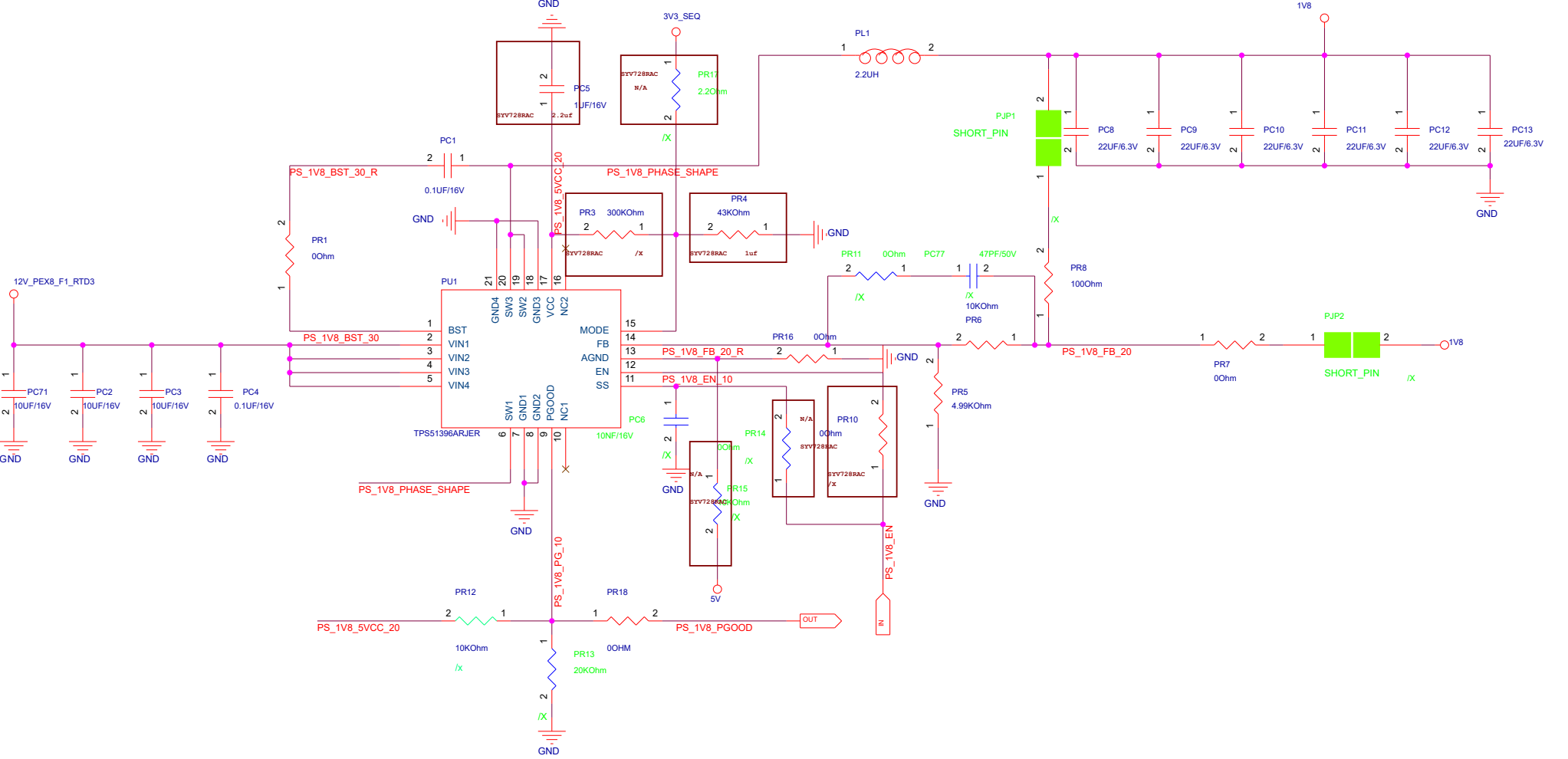




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Size	Document Number	Rev
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Date:	Monday, July 27, 2020	Sheet 1 of 1



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Engineer:

<OrgName>		Project Name	Rev
Size A4			

Power

