

# PG190-A02

## GA104/GA106 GB5256 DP + DP + DP + HDMI/DP


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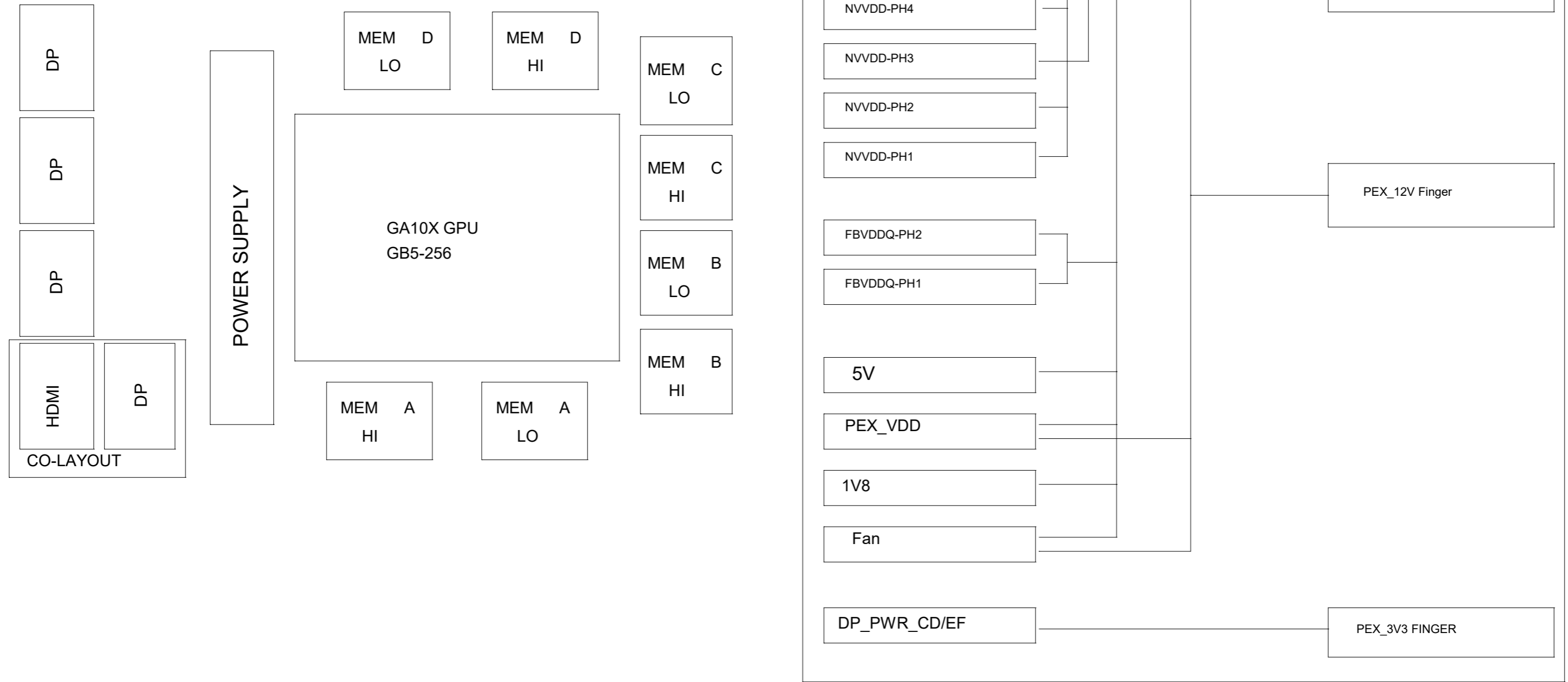
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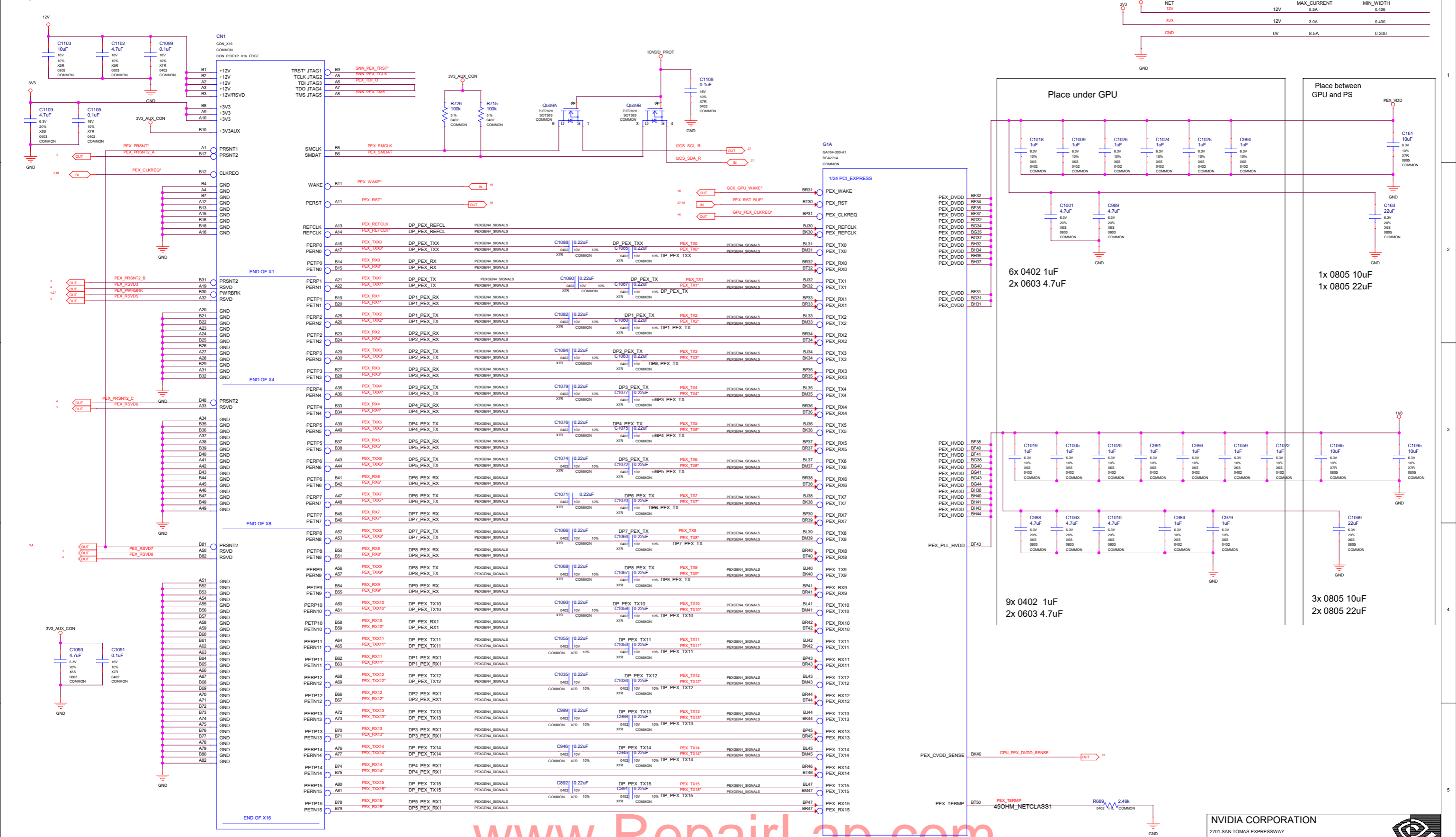
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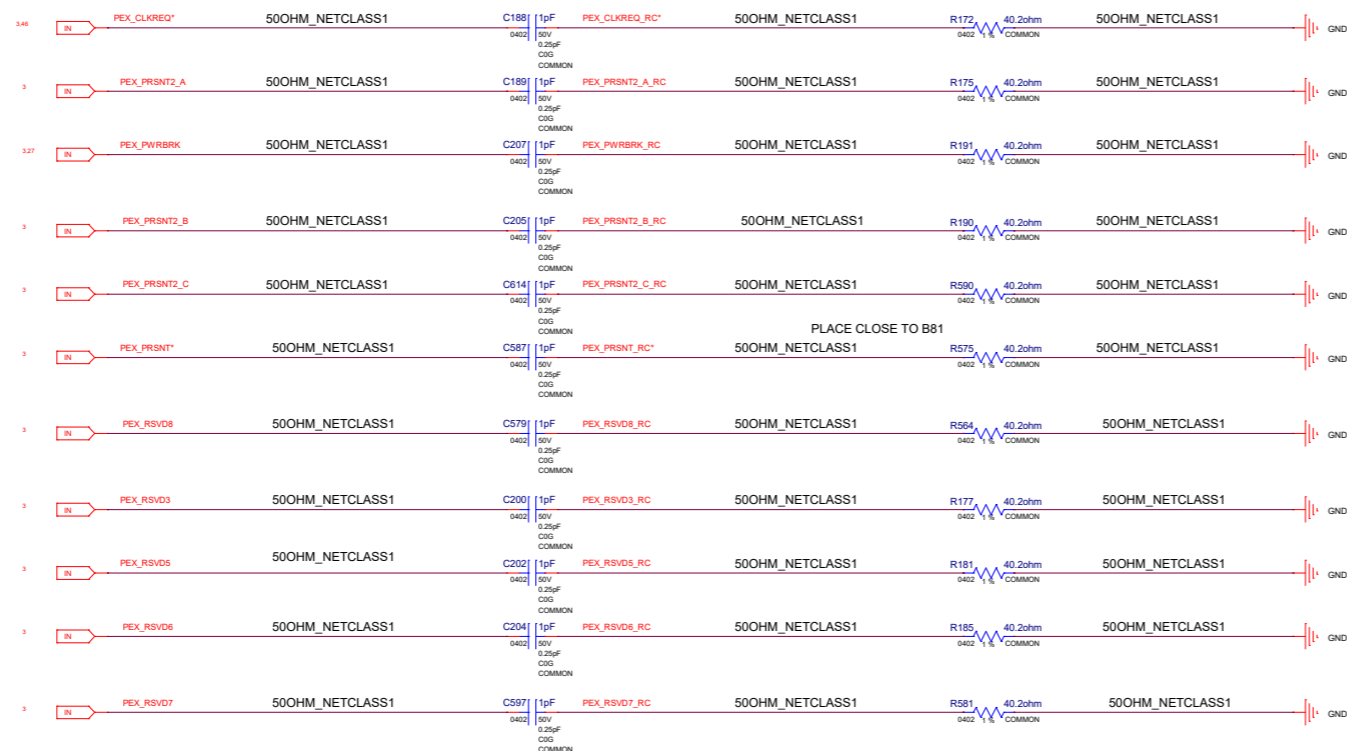
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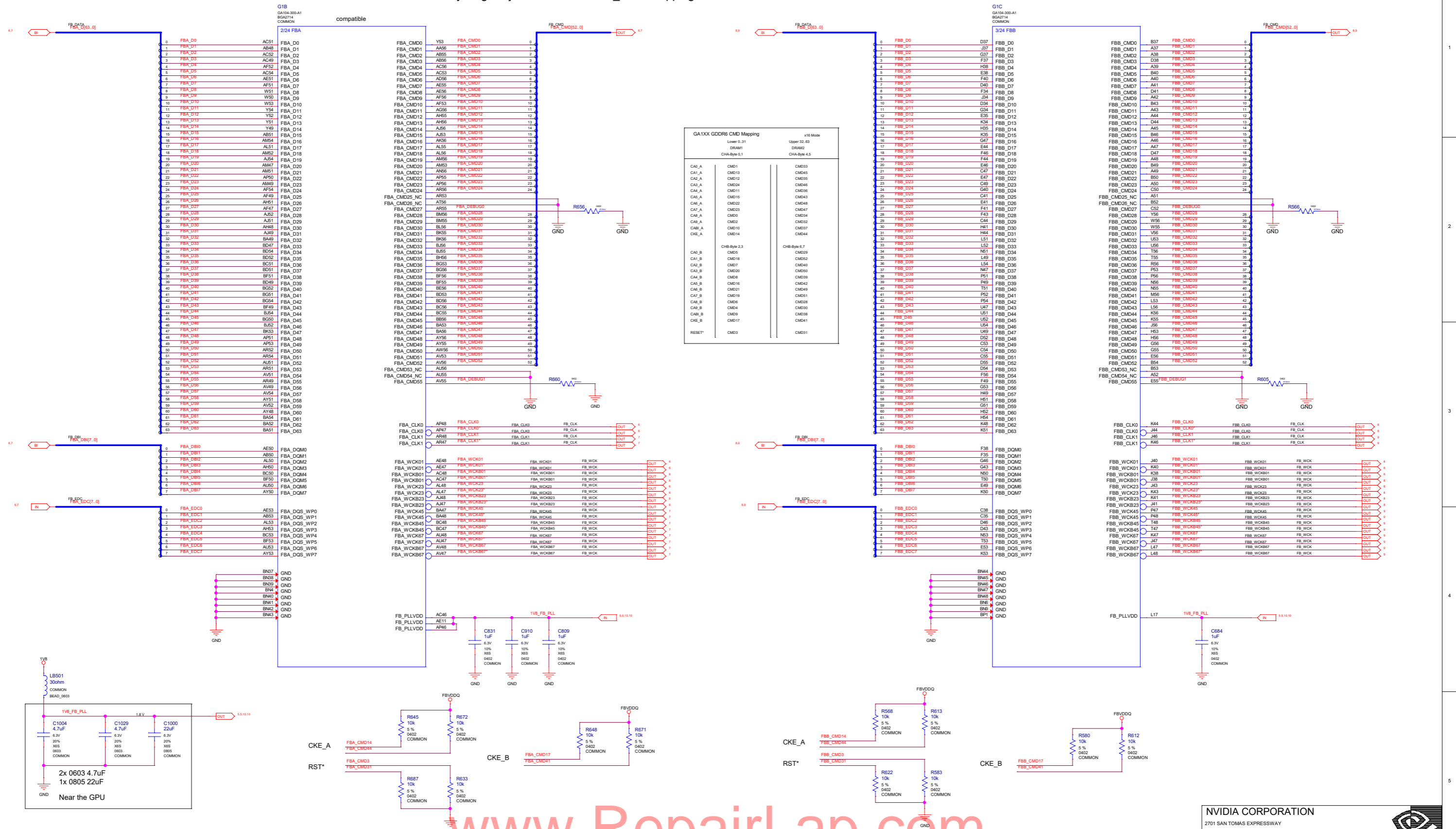


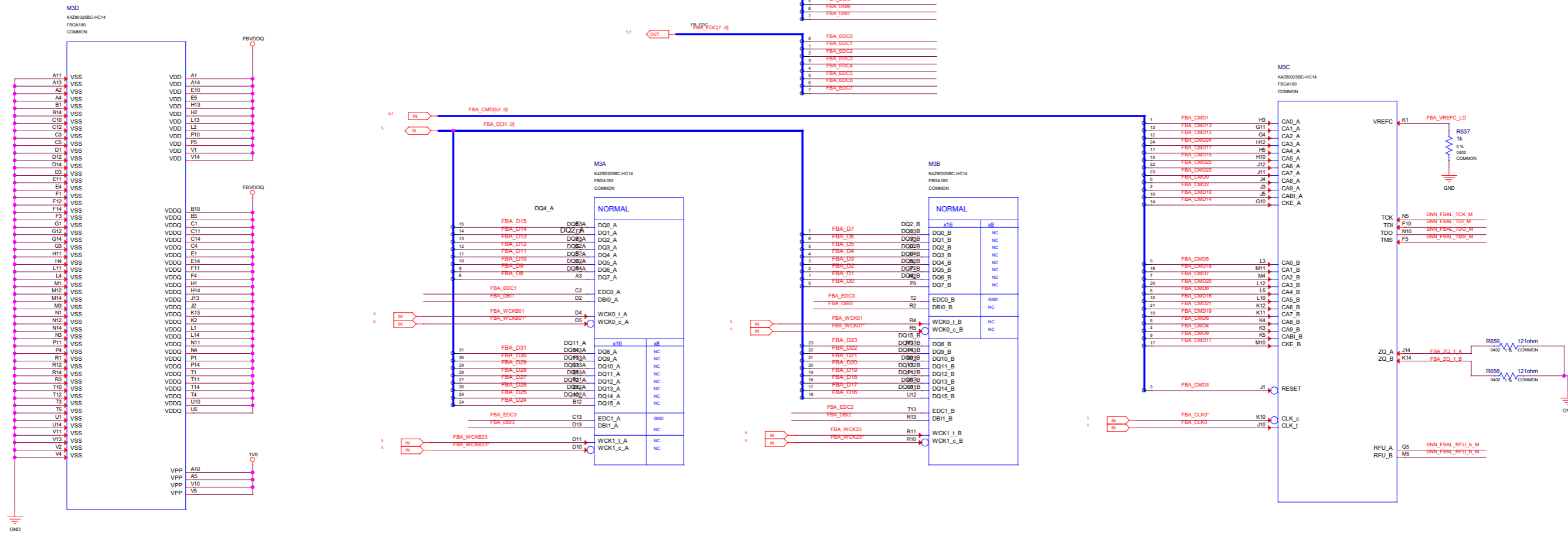
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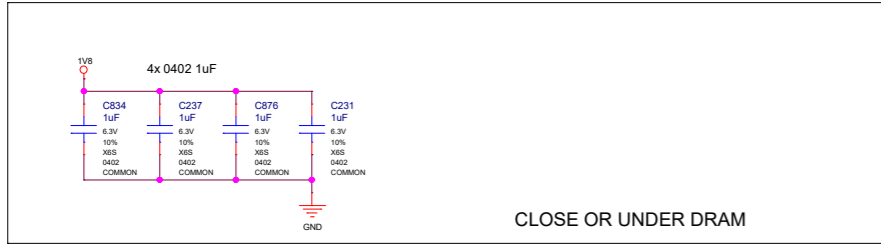
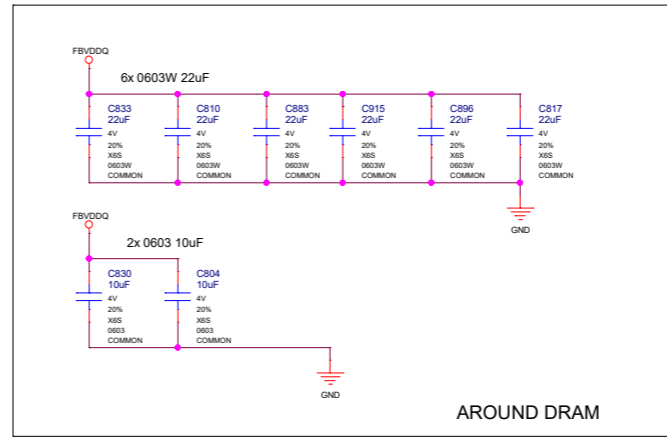
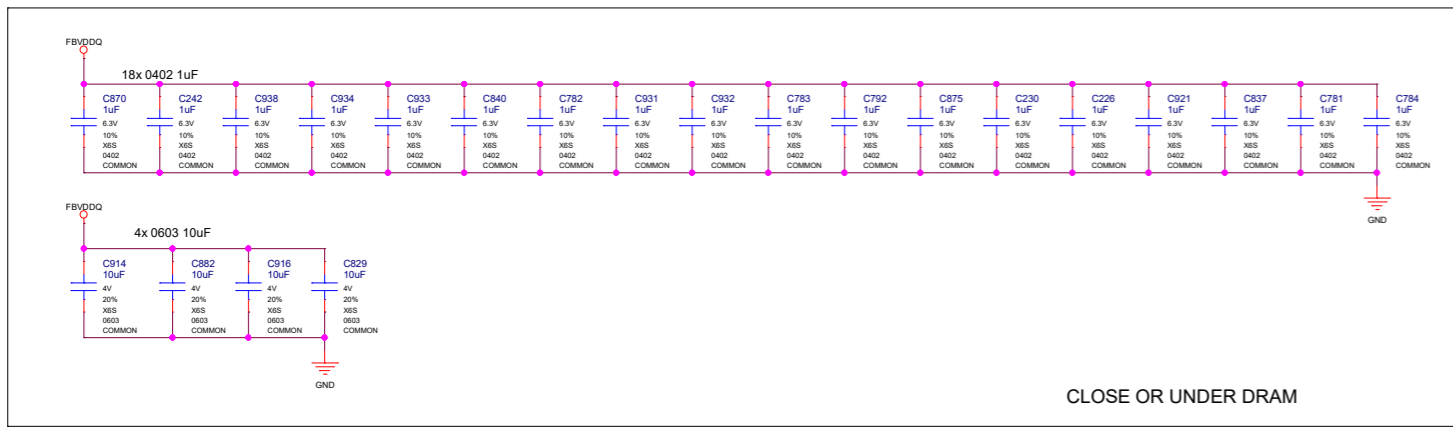
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//syseng/Projects/GA1xx/GA1XX\_CMD-Mapping.xls#





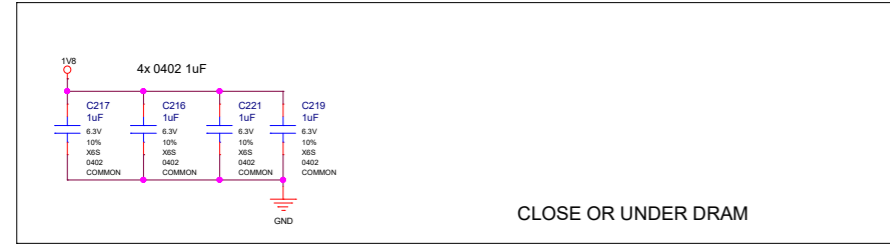
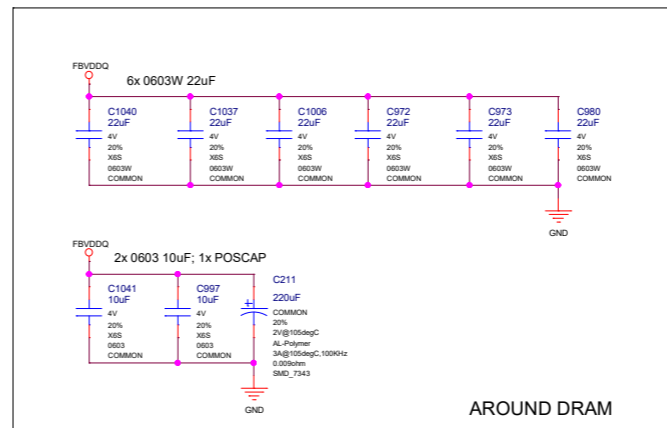
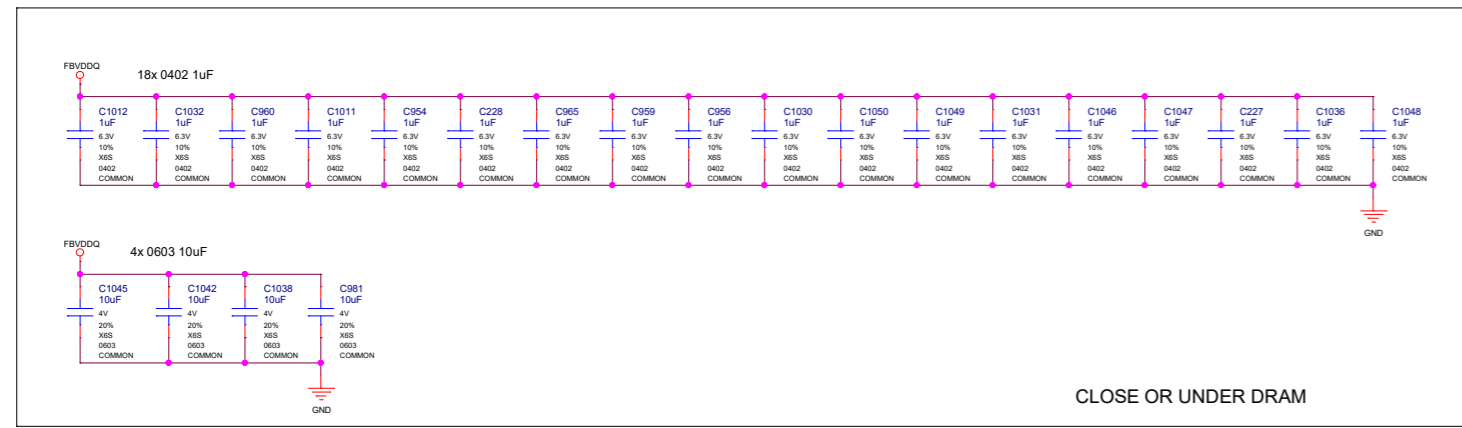
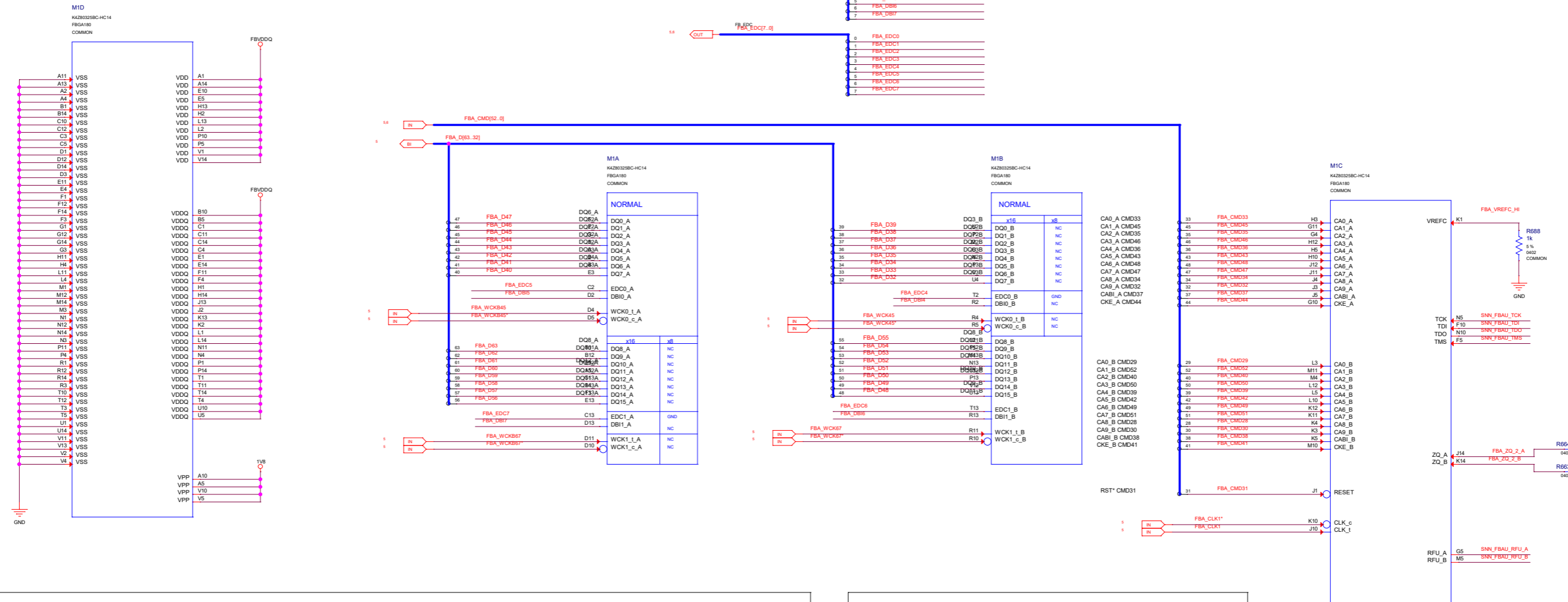
decap via : at least 2 gnd vias and 2 power vias for each cap



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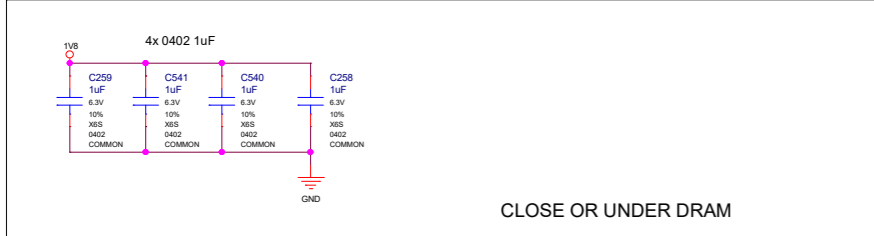
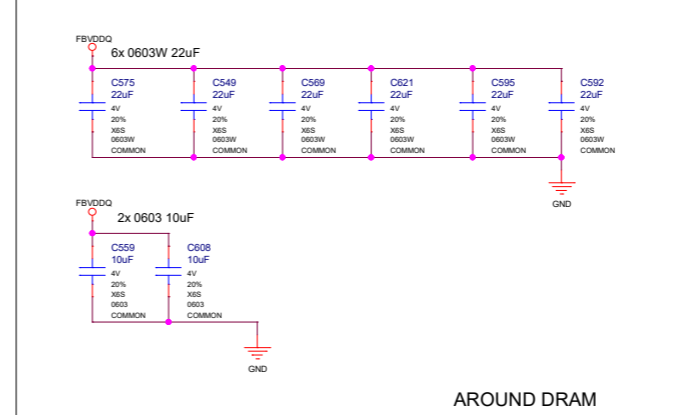
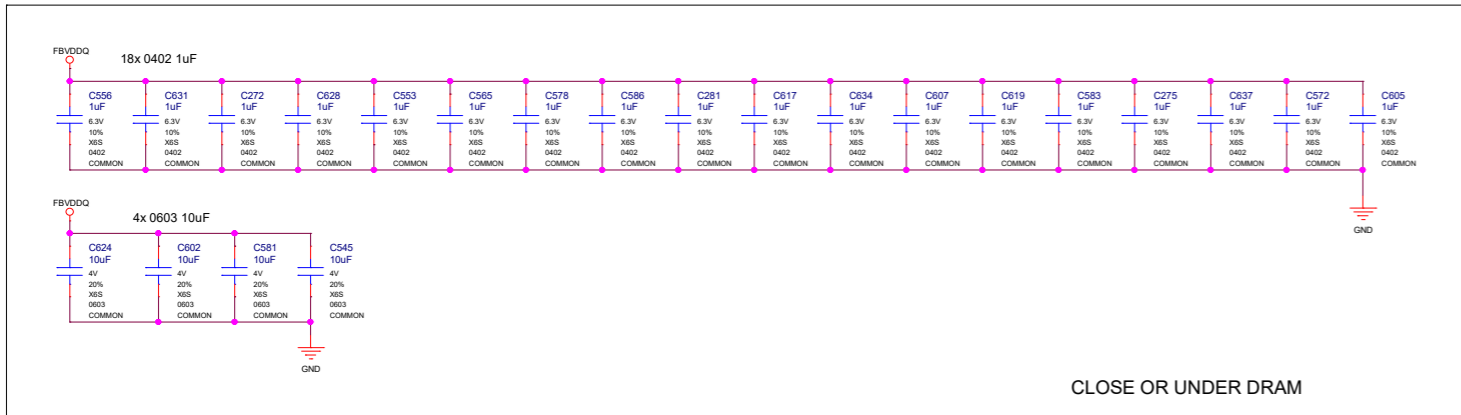
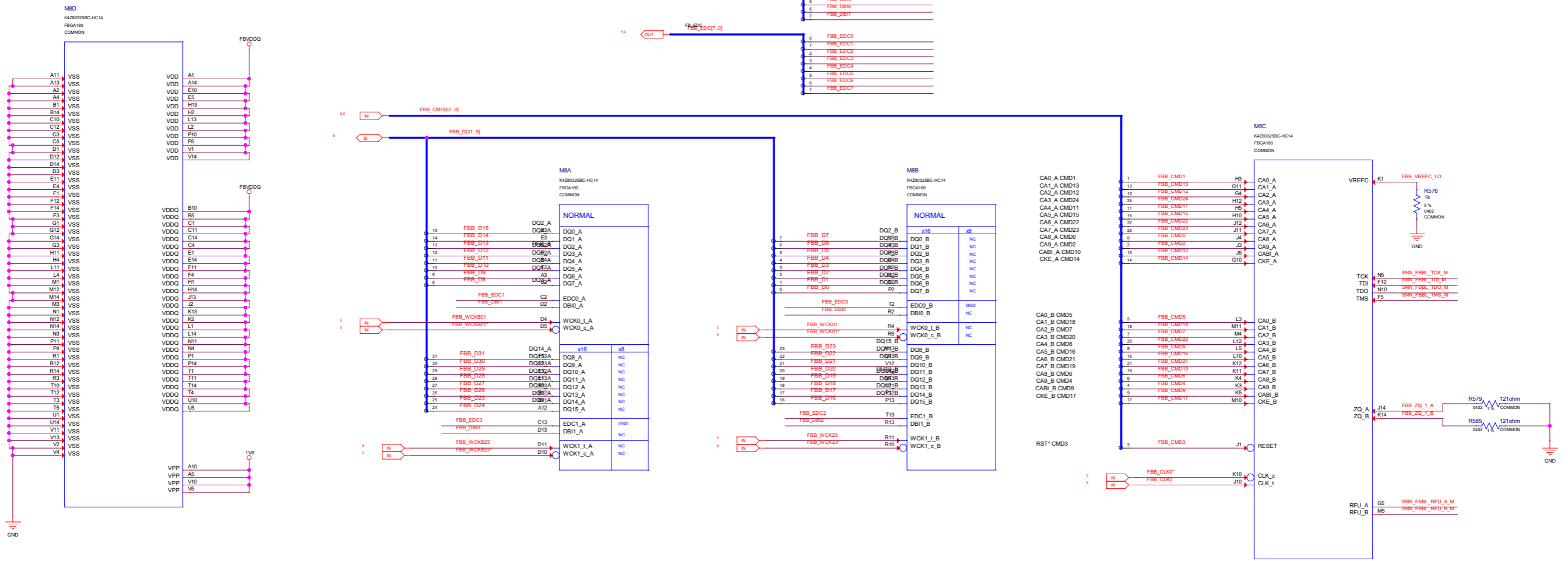
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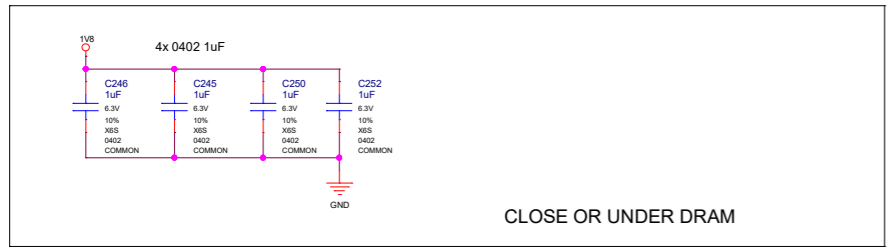
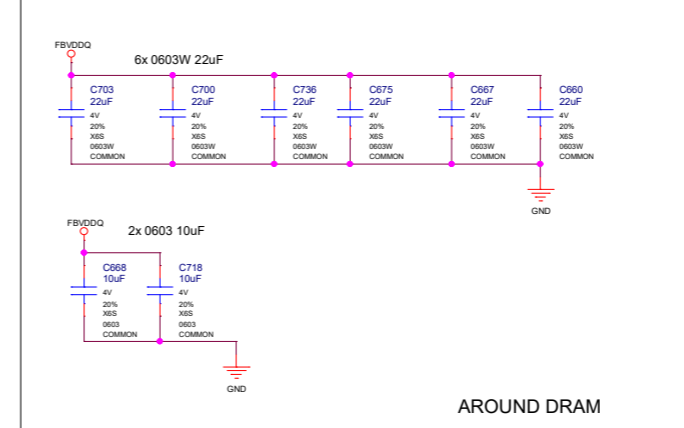
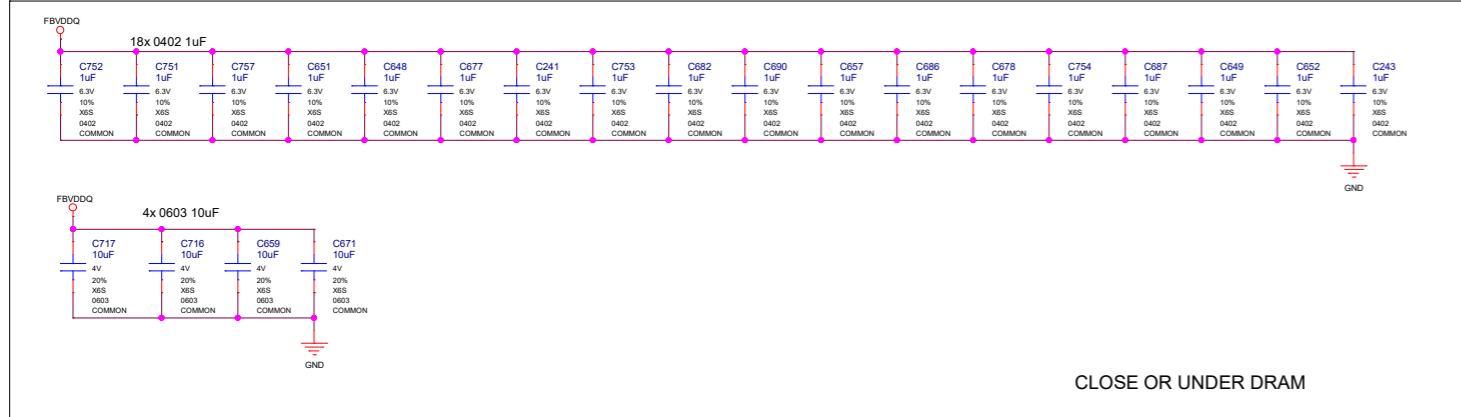
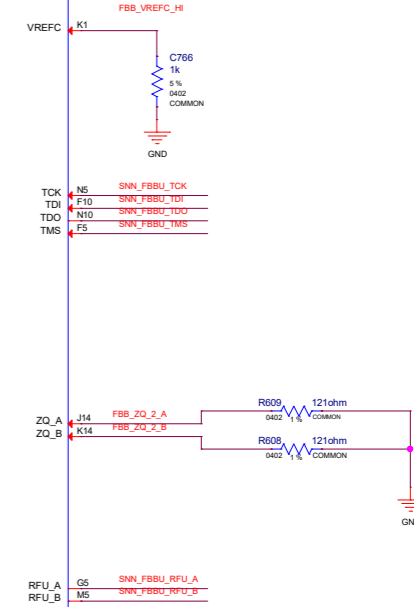
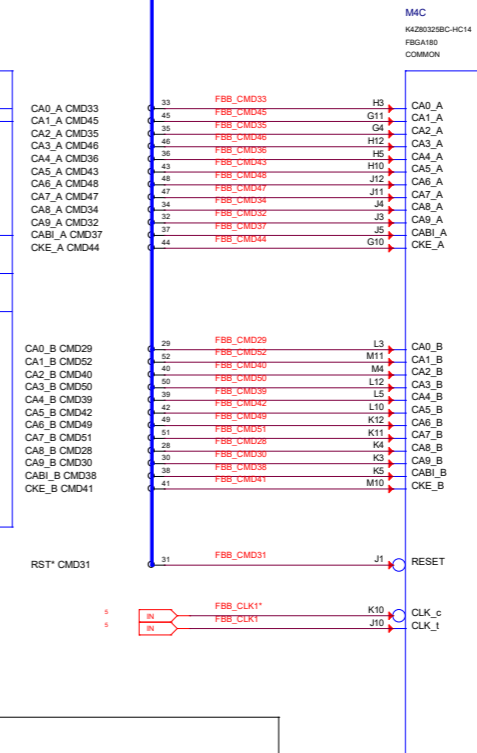
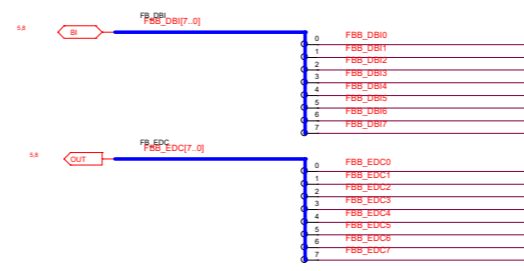
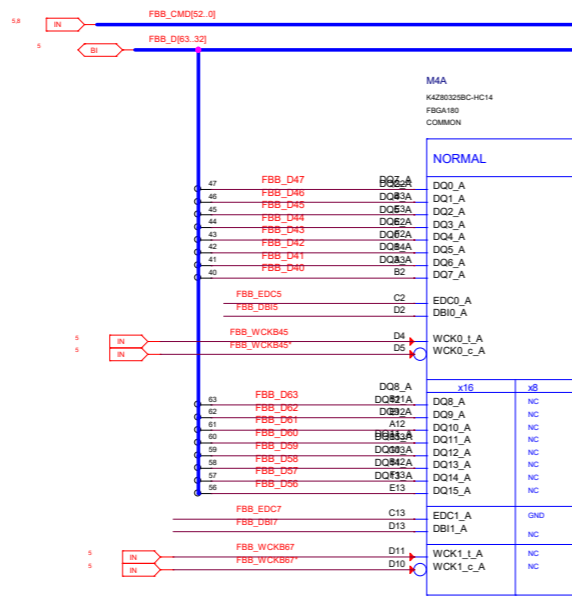
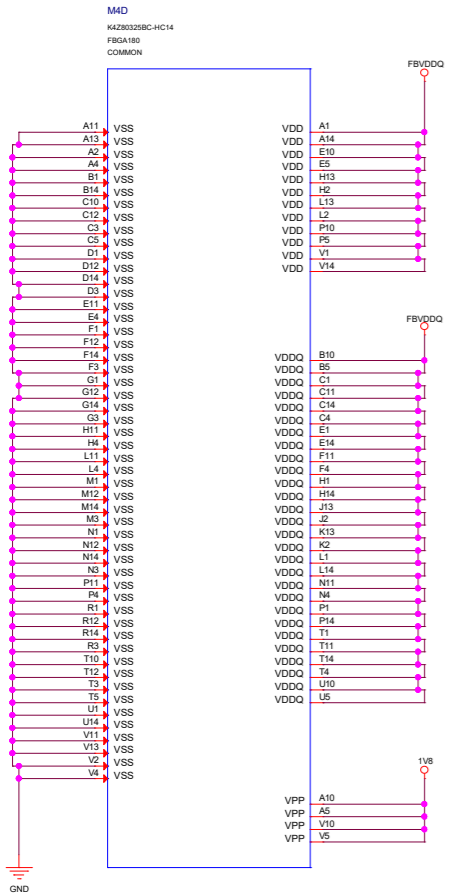
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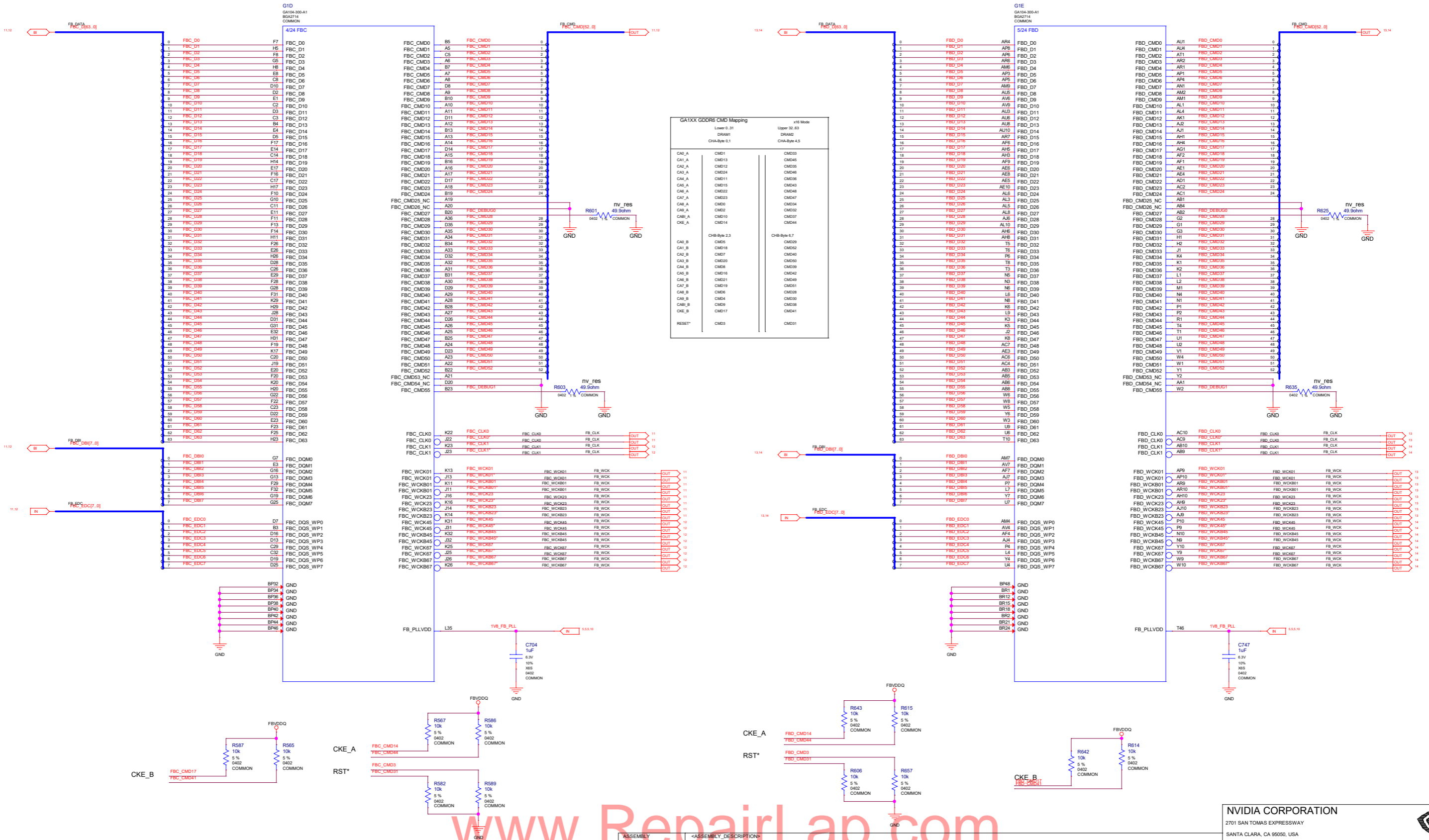
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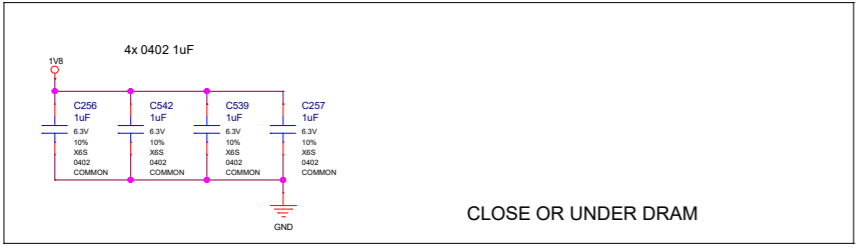
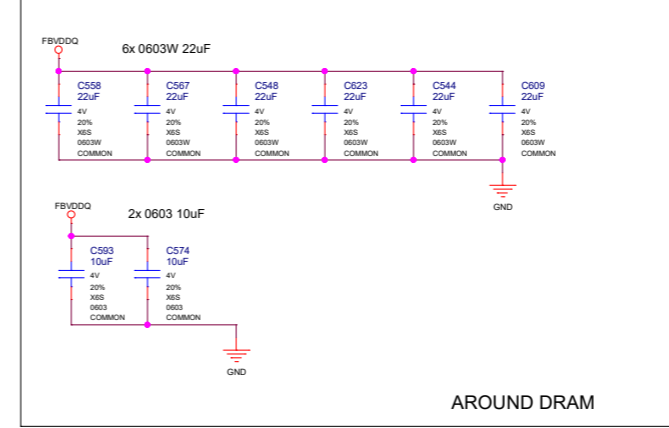
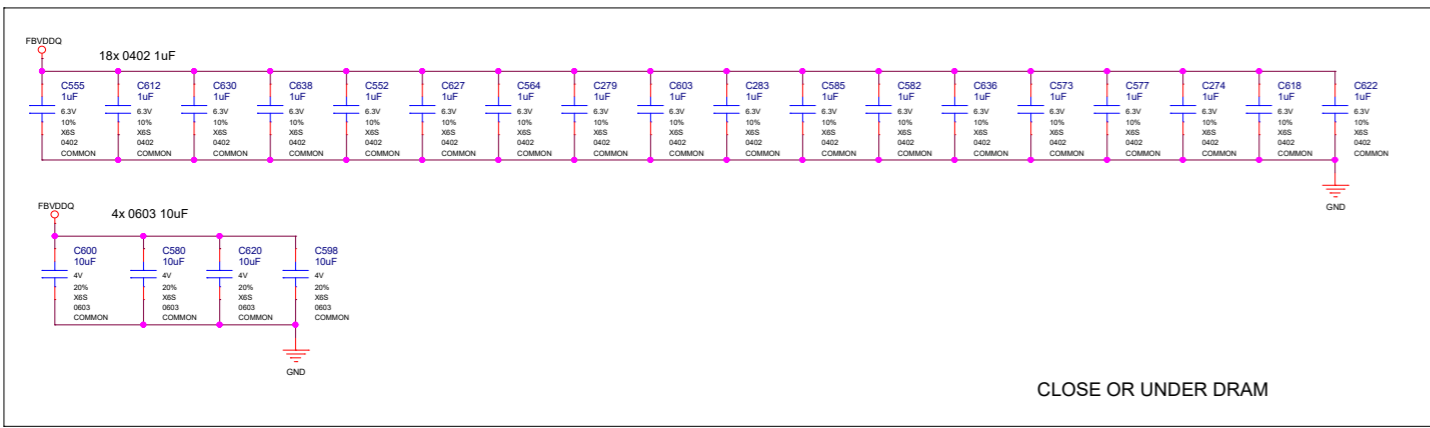
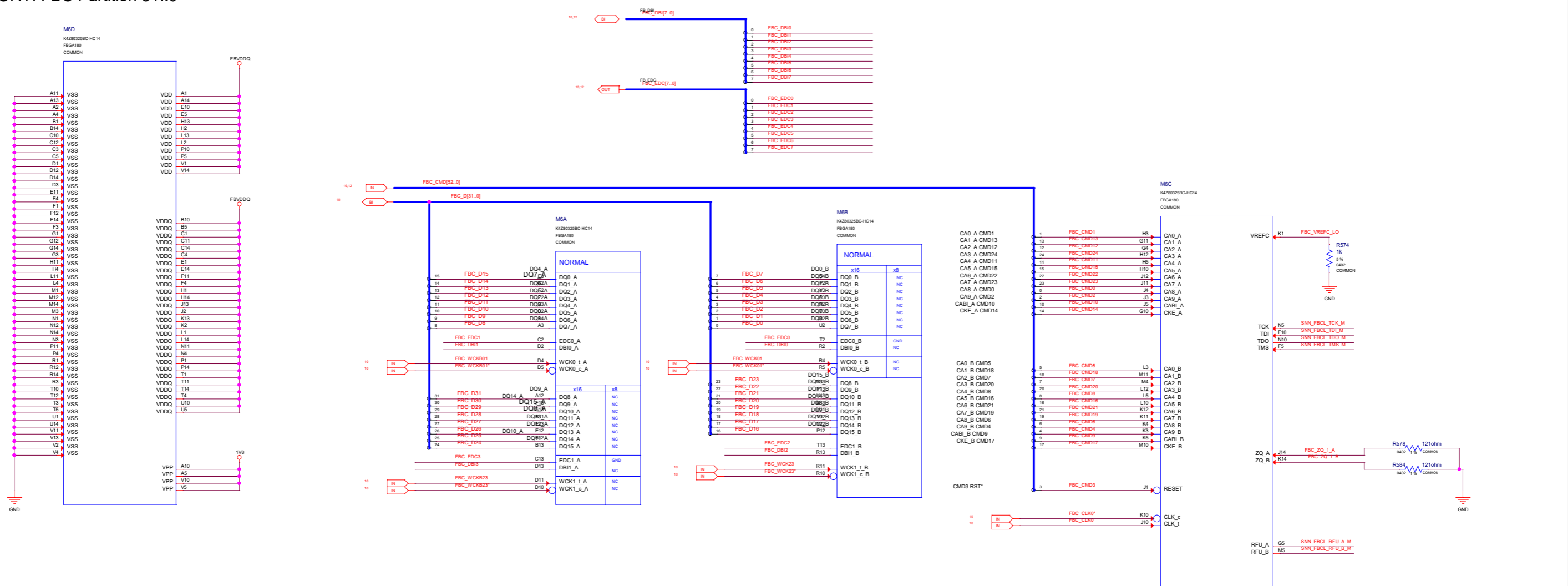


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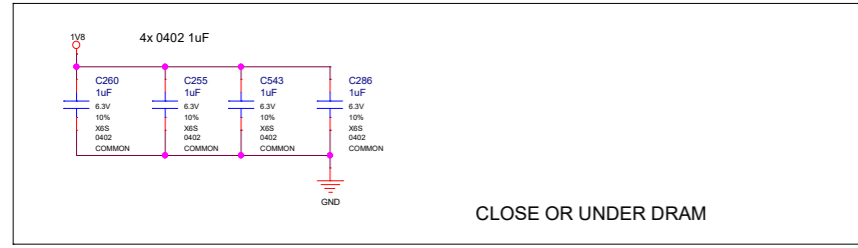
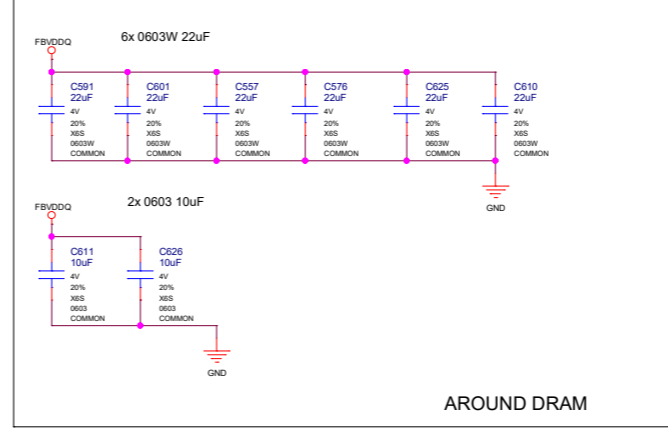
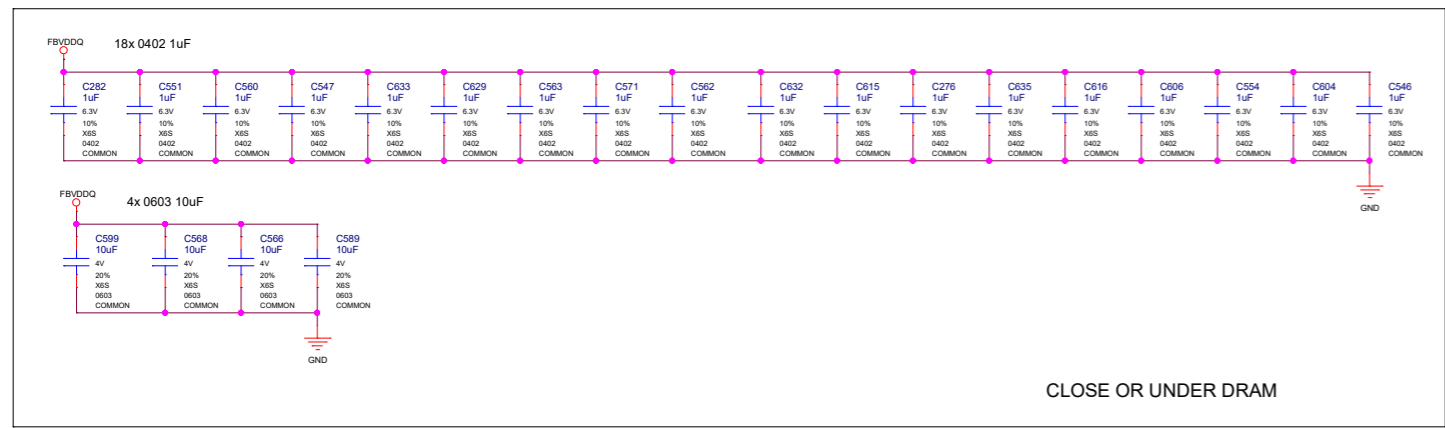
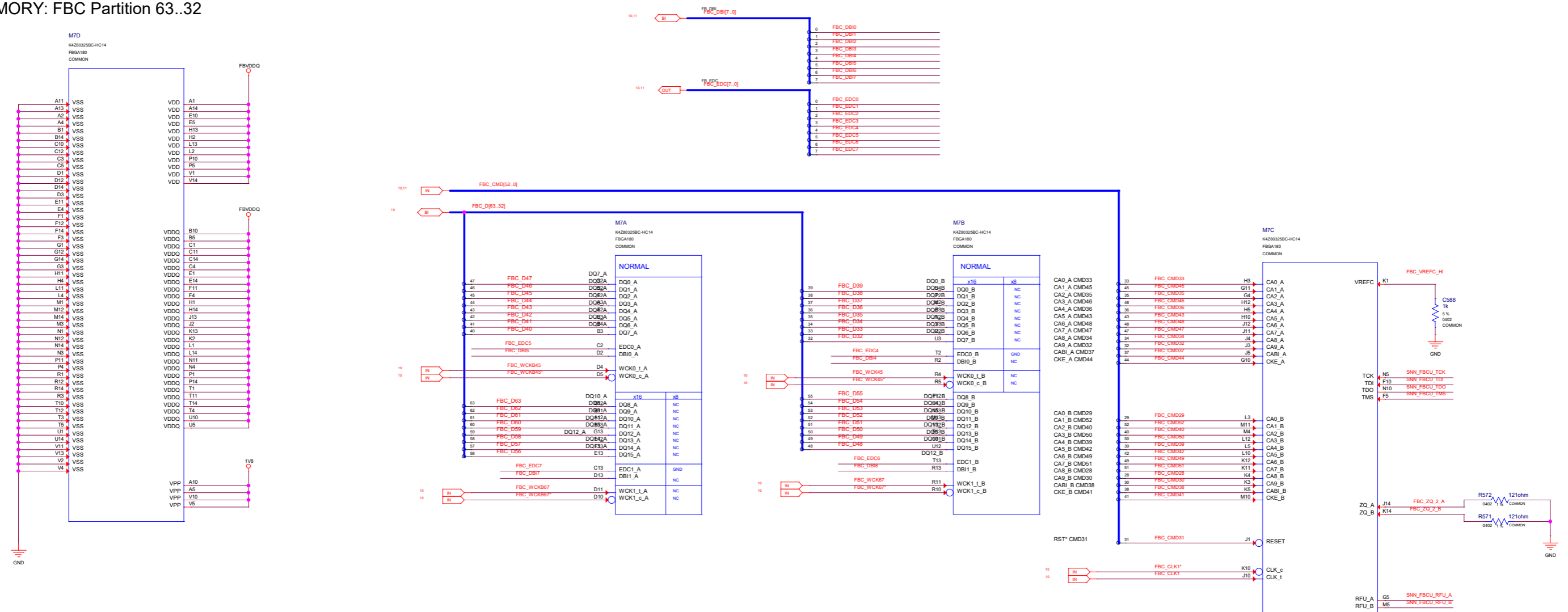
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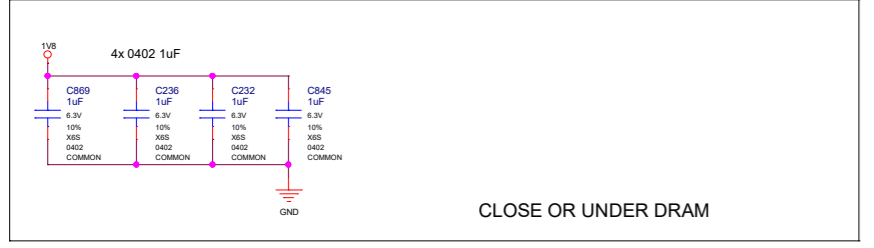
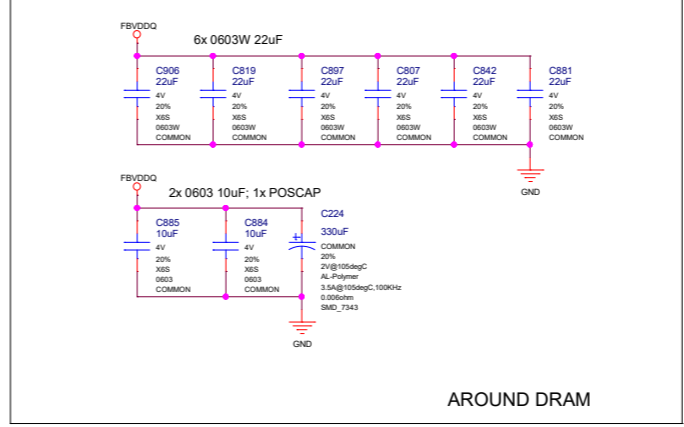
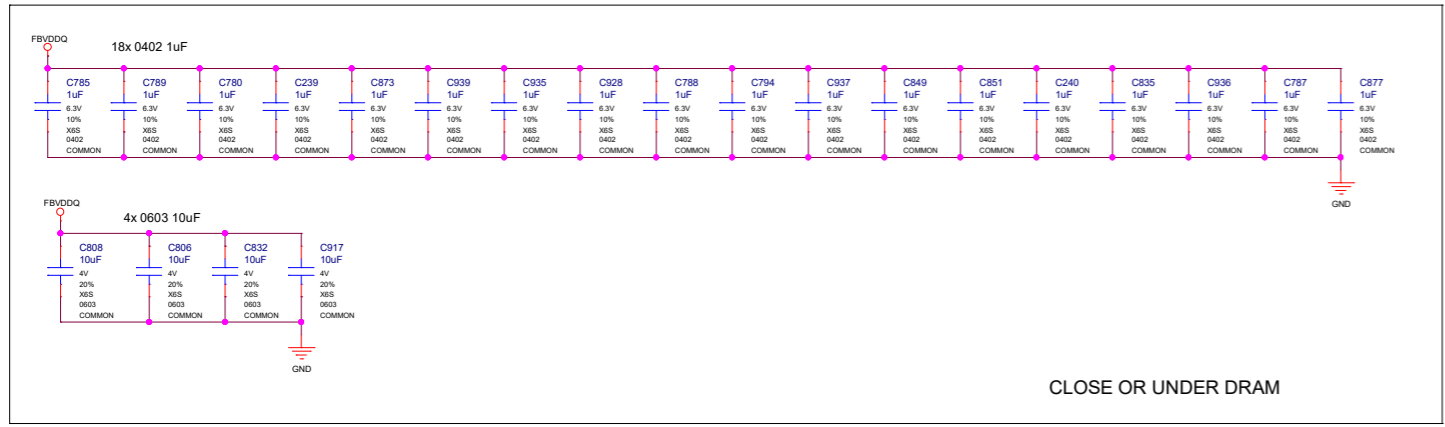
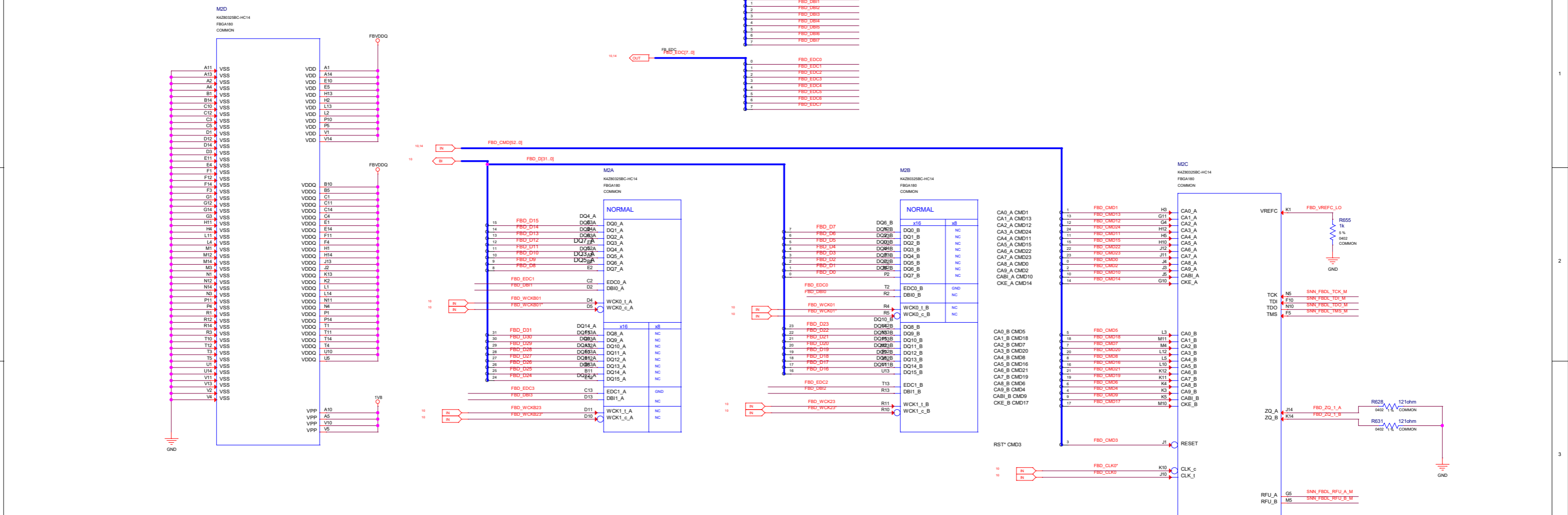
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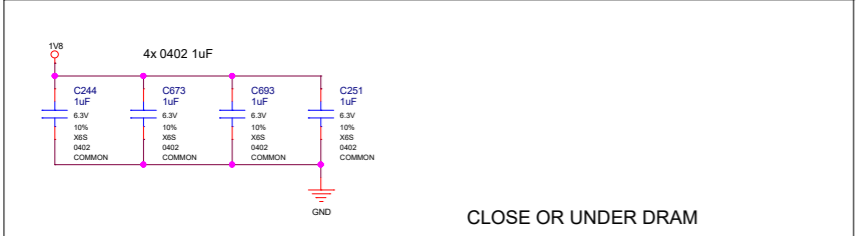
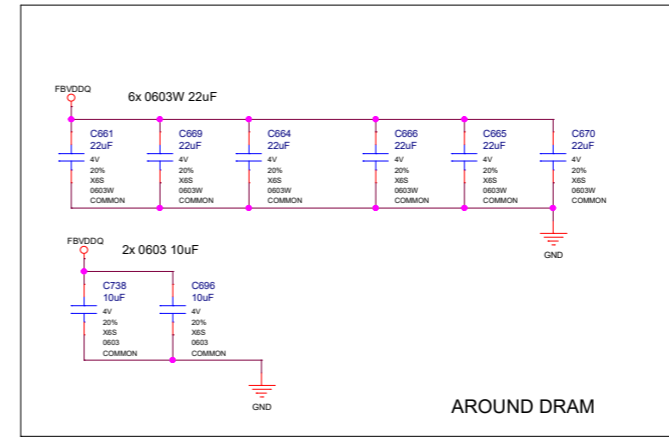
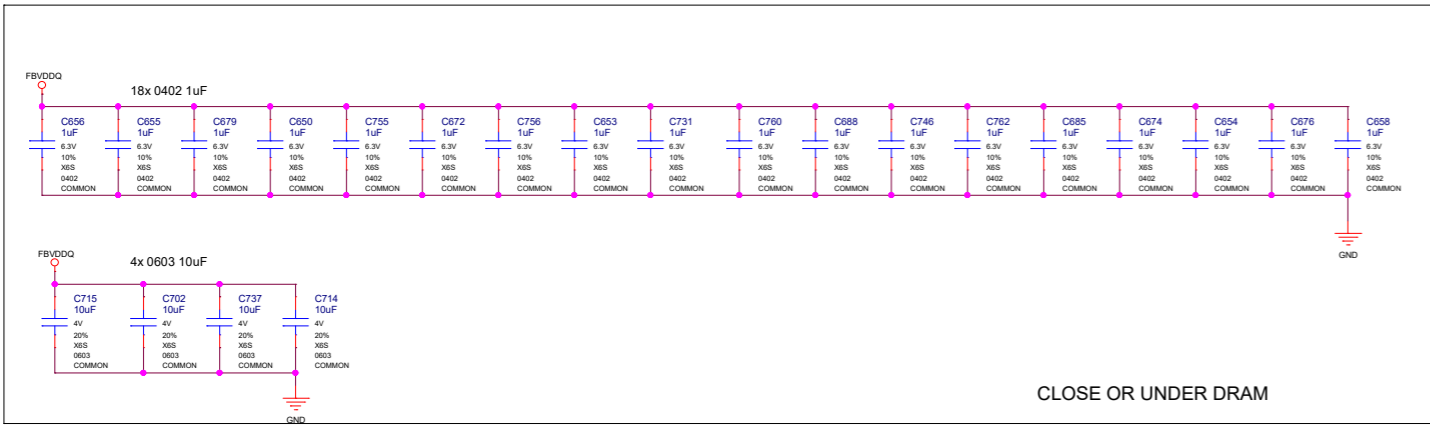
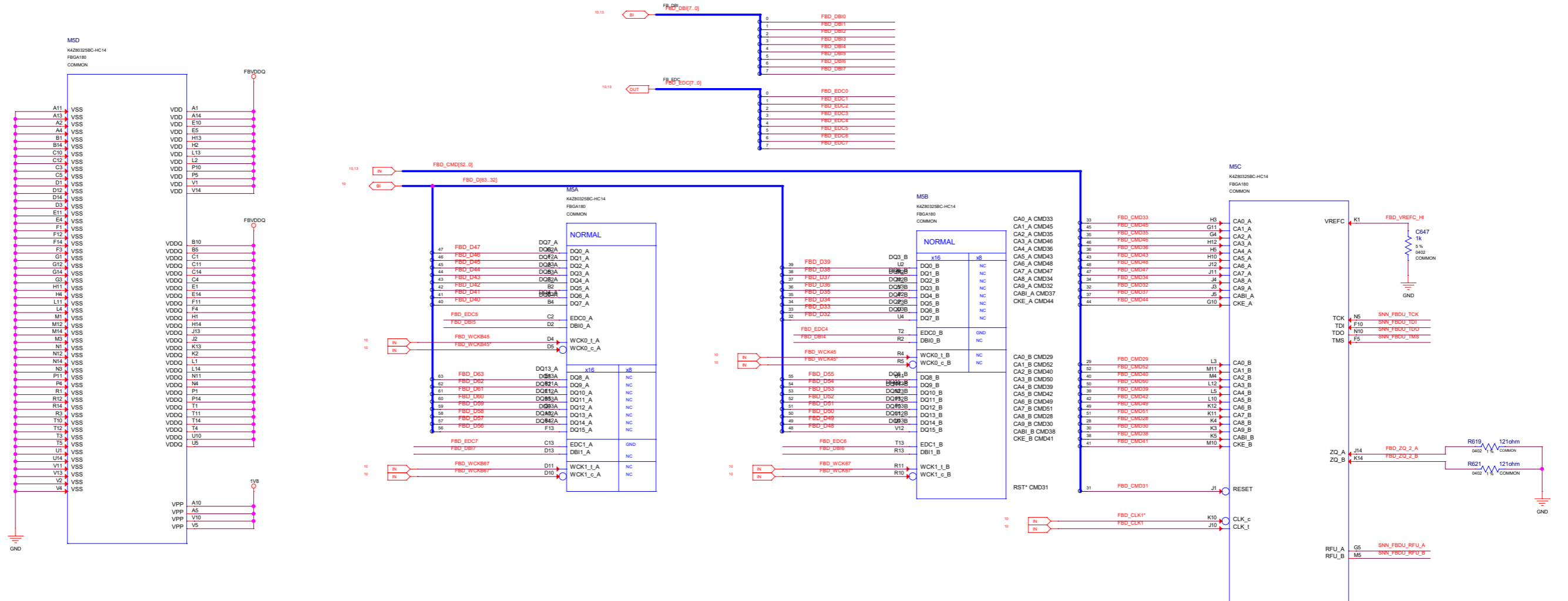
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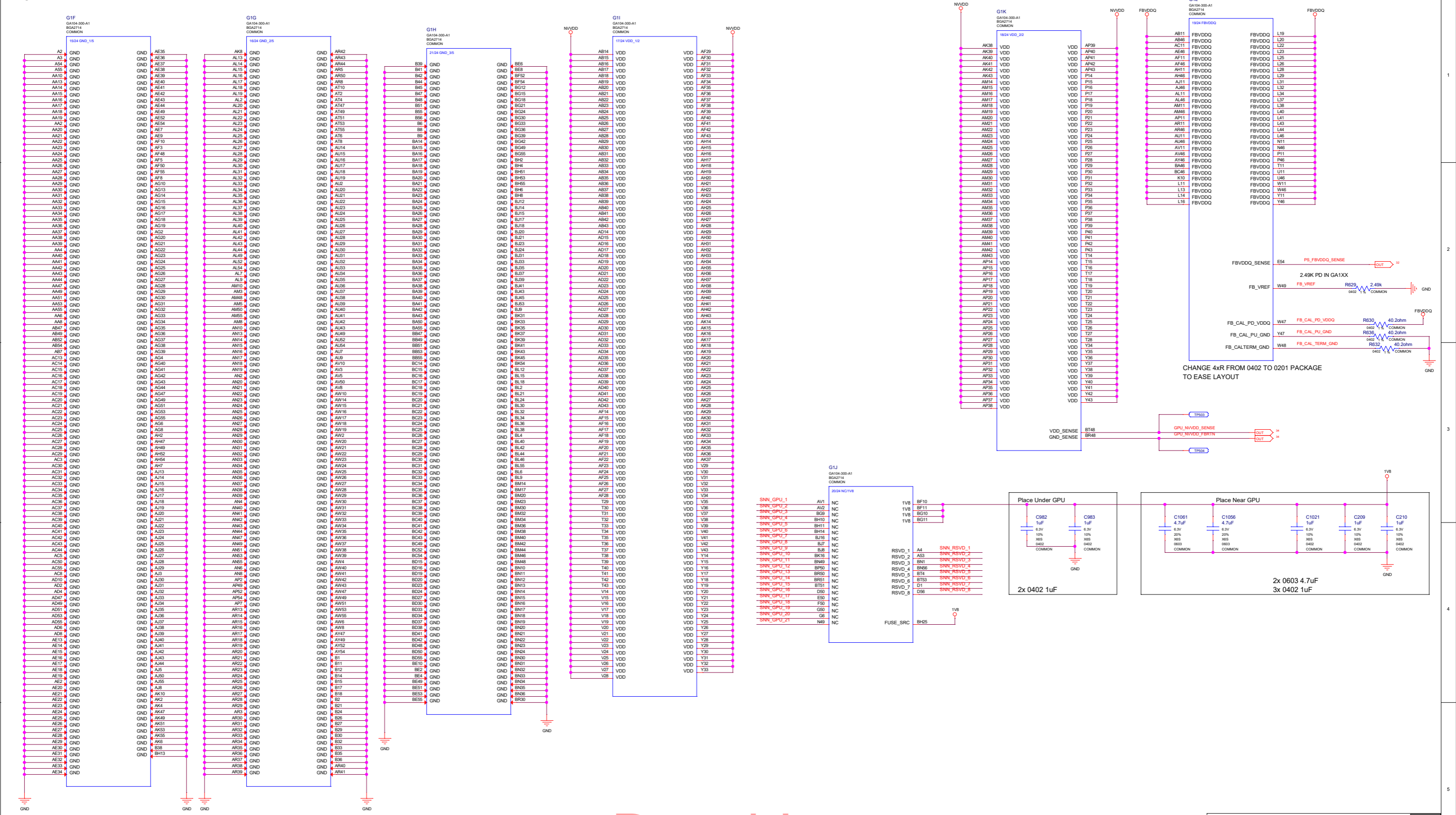
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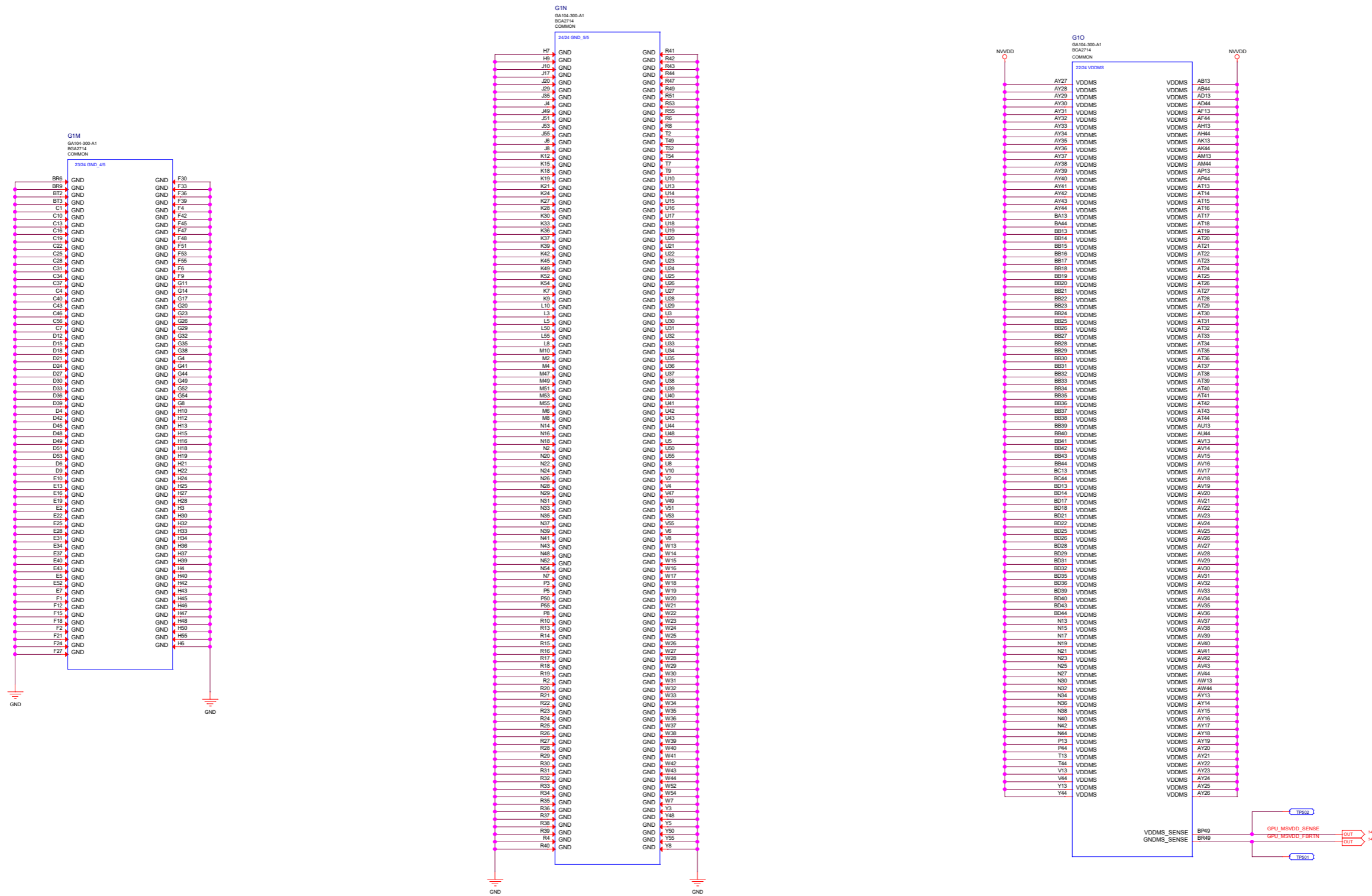


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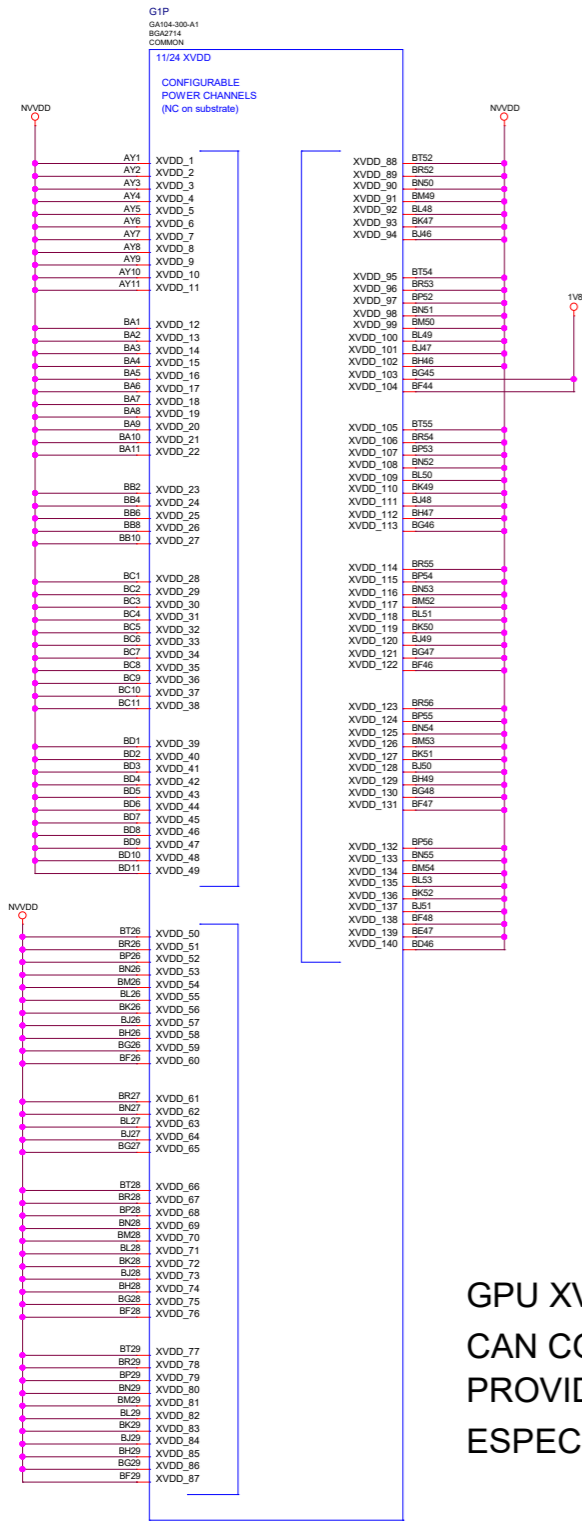
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ASSEMBLY PAGE DETAIL <ASSEMBLY DESCRIPTION> GPU PWR and GND 2



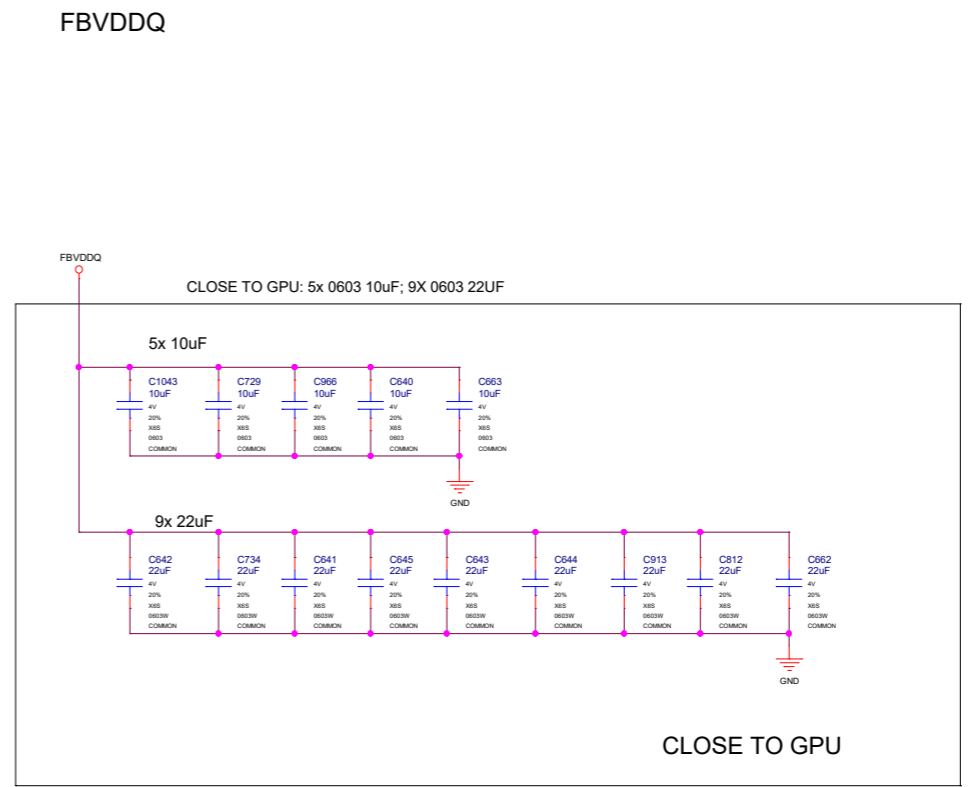
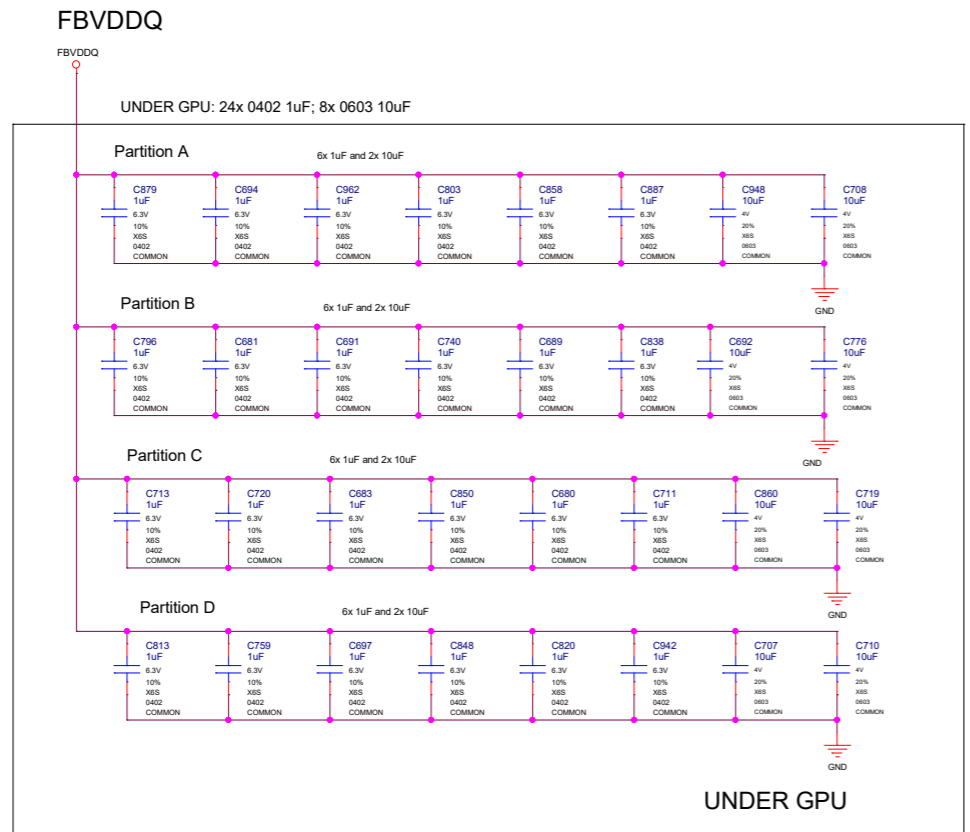


GPU XVDD BALLS (NC IN SUBSTRATE):  
 CAN CONNECT TO ANY POWER NET (NV/MS/1V8/PEX, etc.) ON SYSTEM BOARD,  
 PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,  
 ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.

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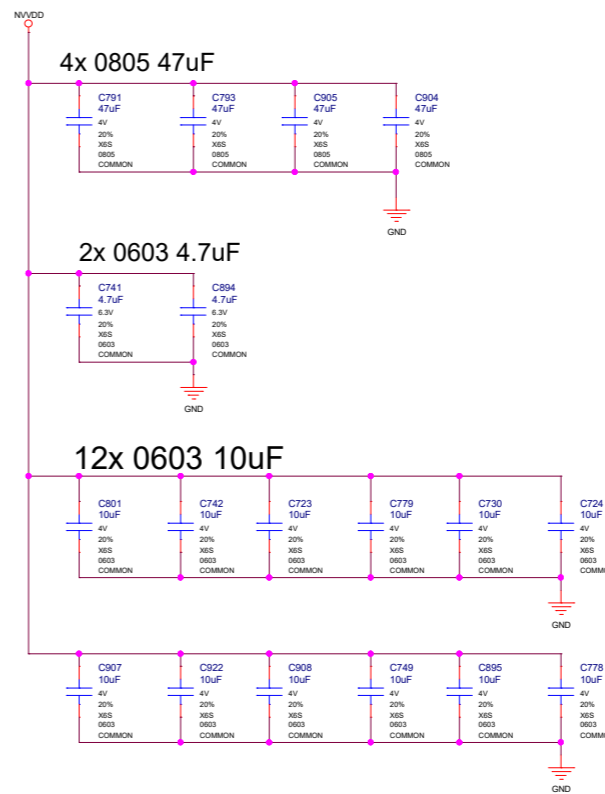
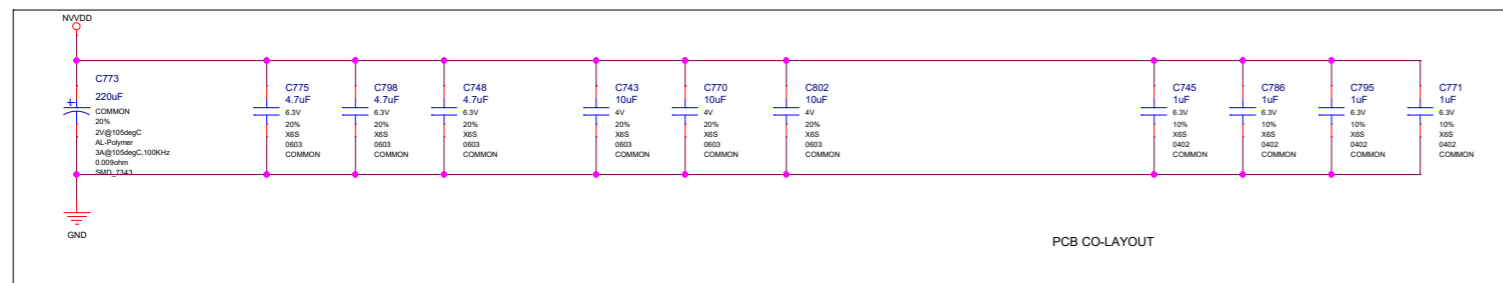
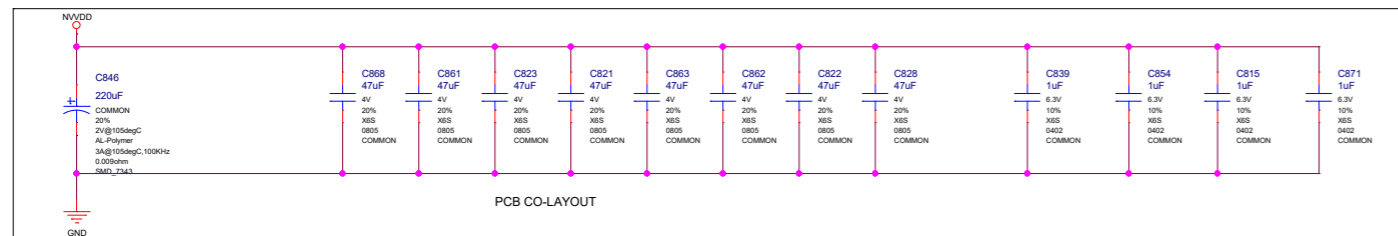
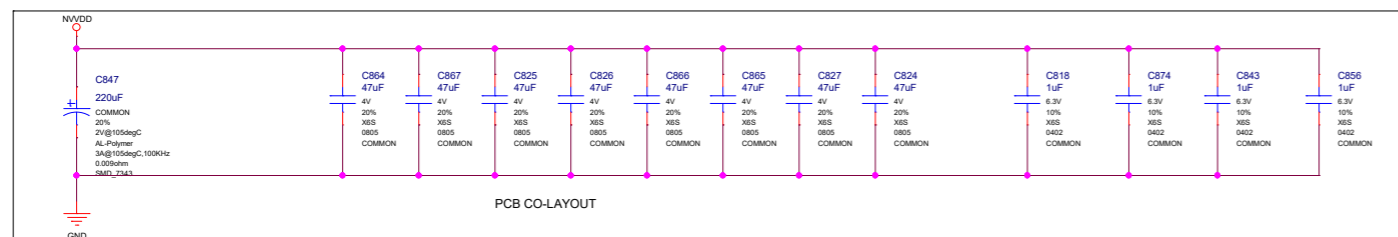
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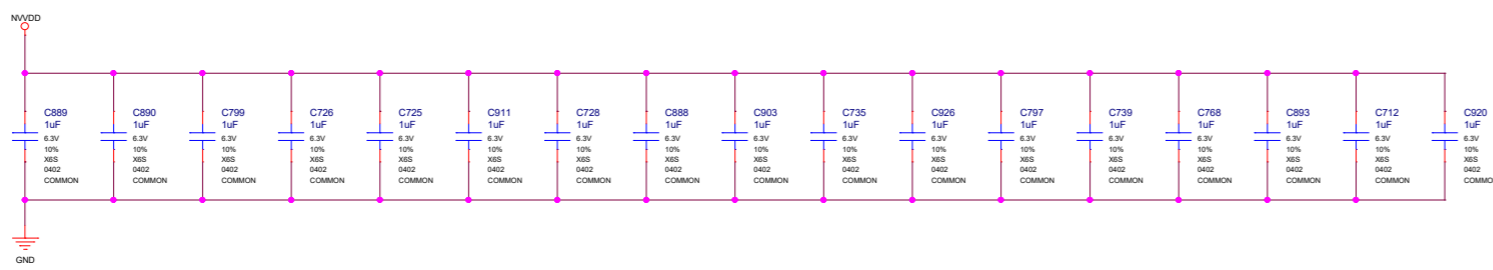
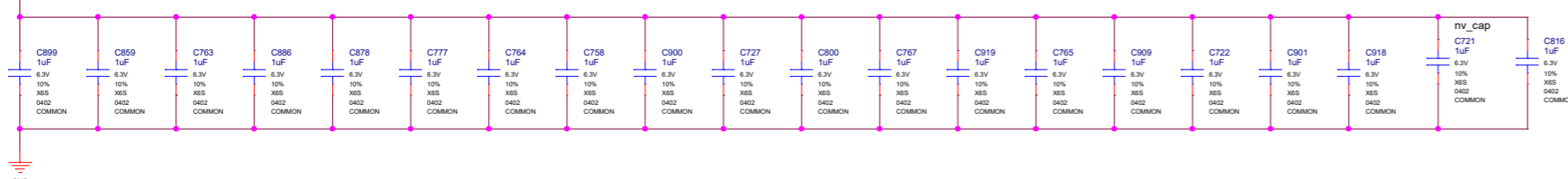
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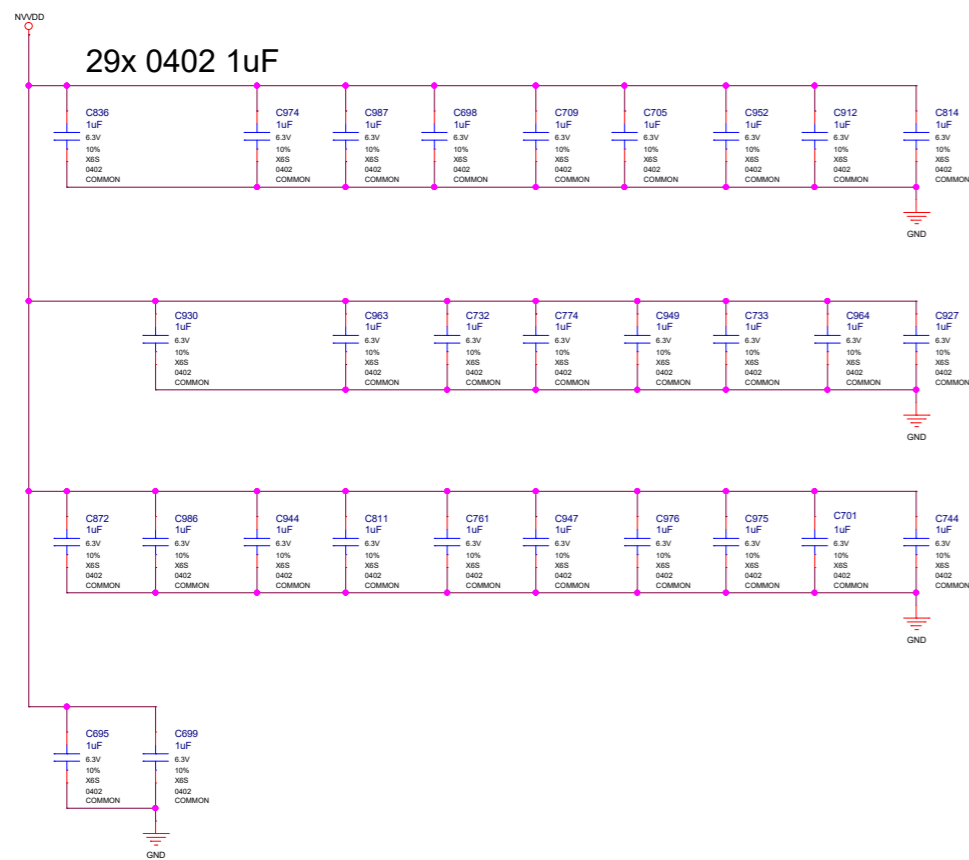
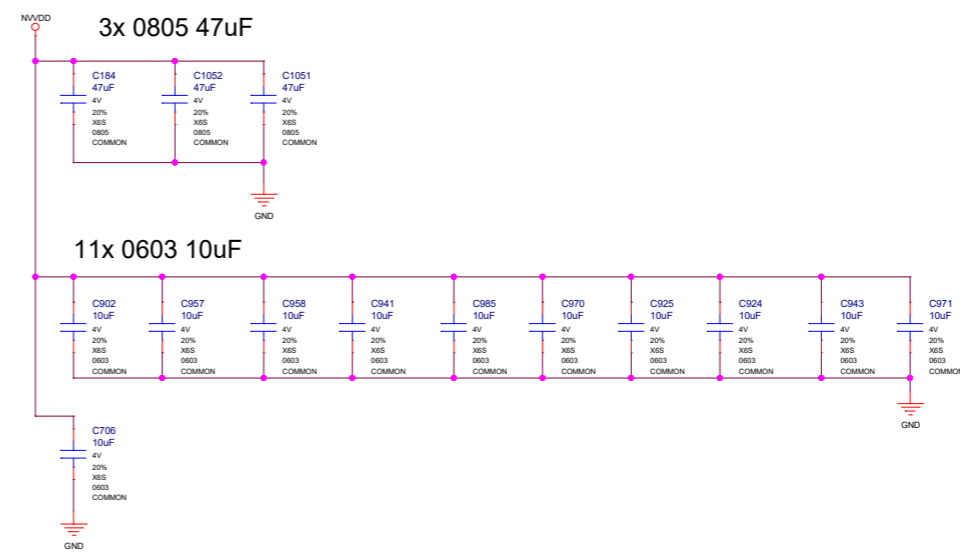
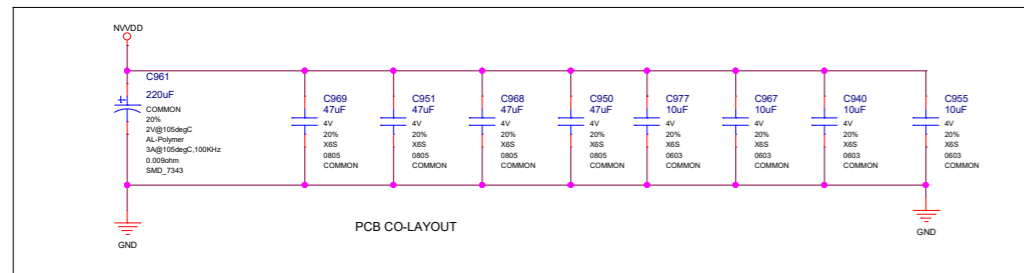


UNDER GPU

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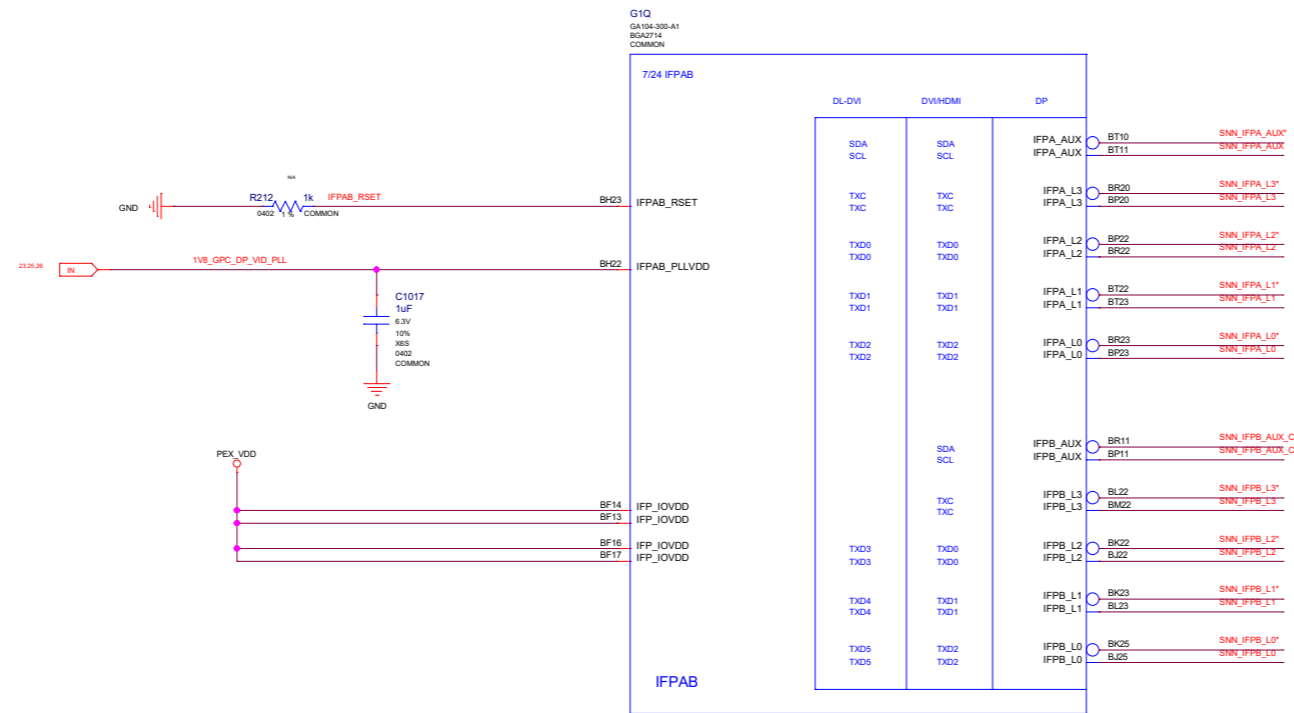


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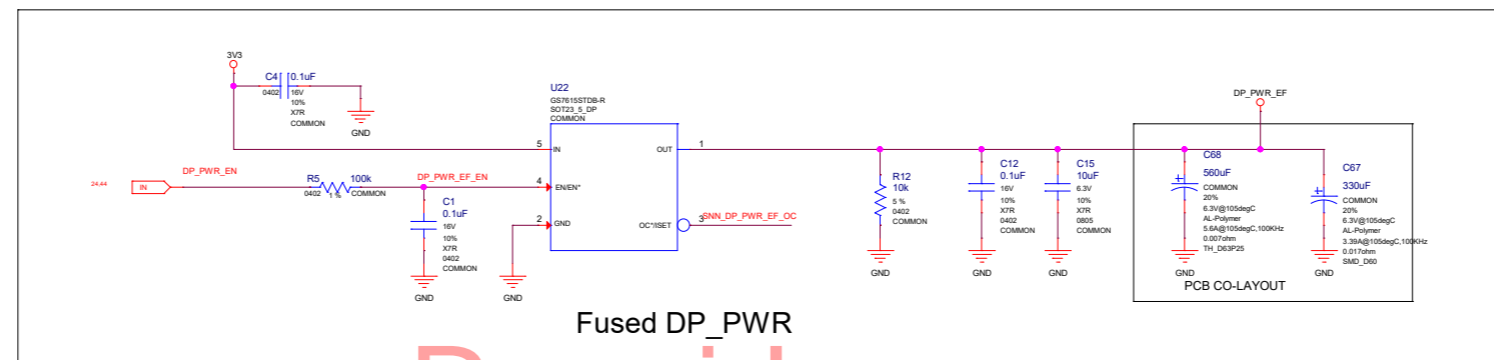
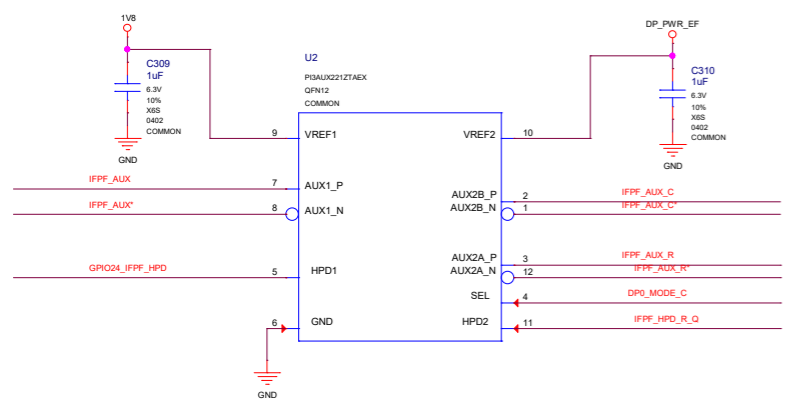
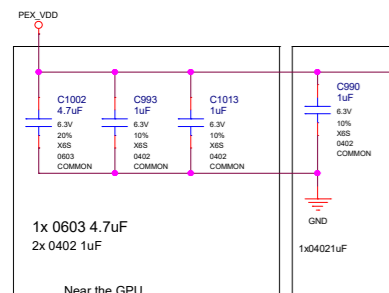
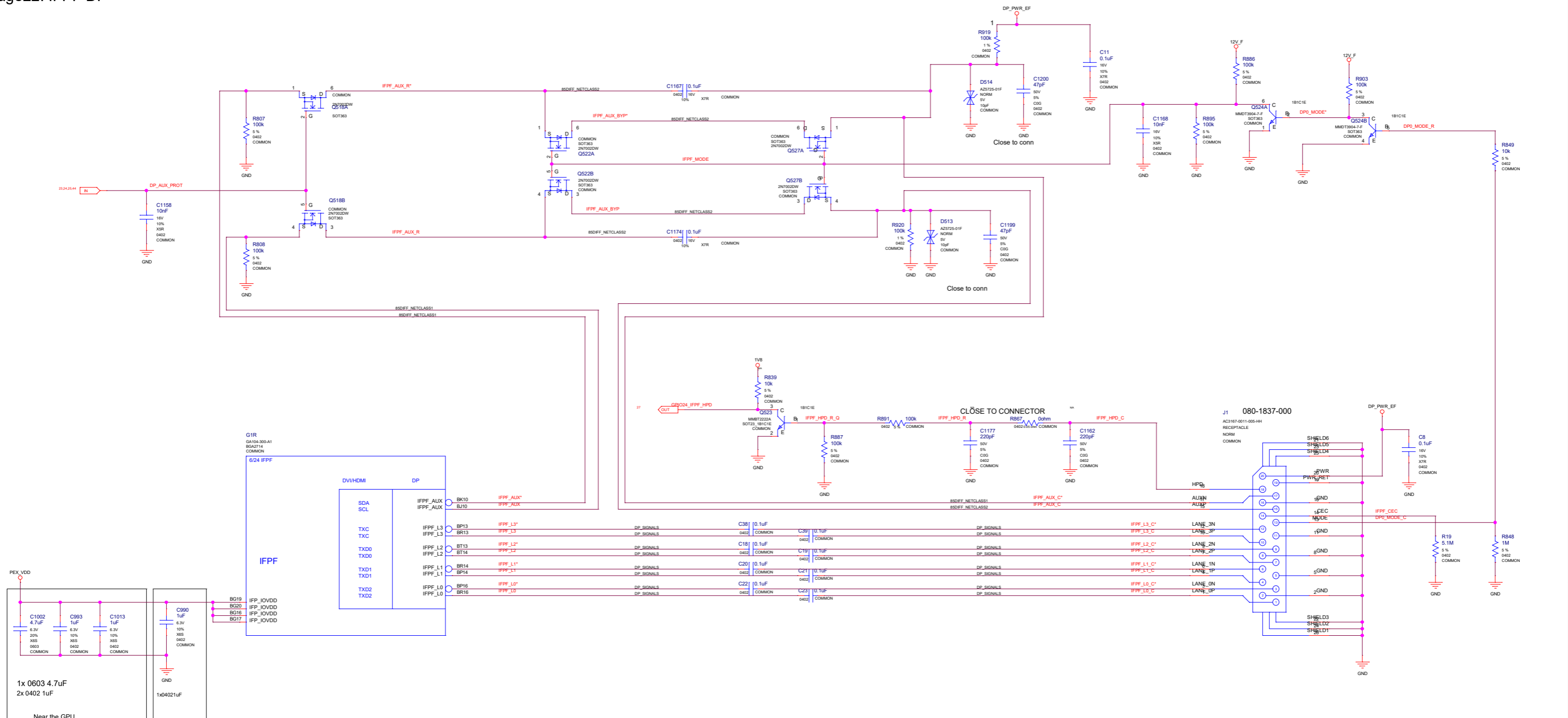
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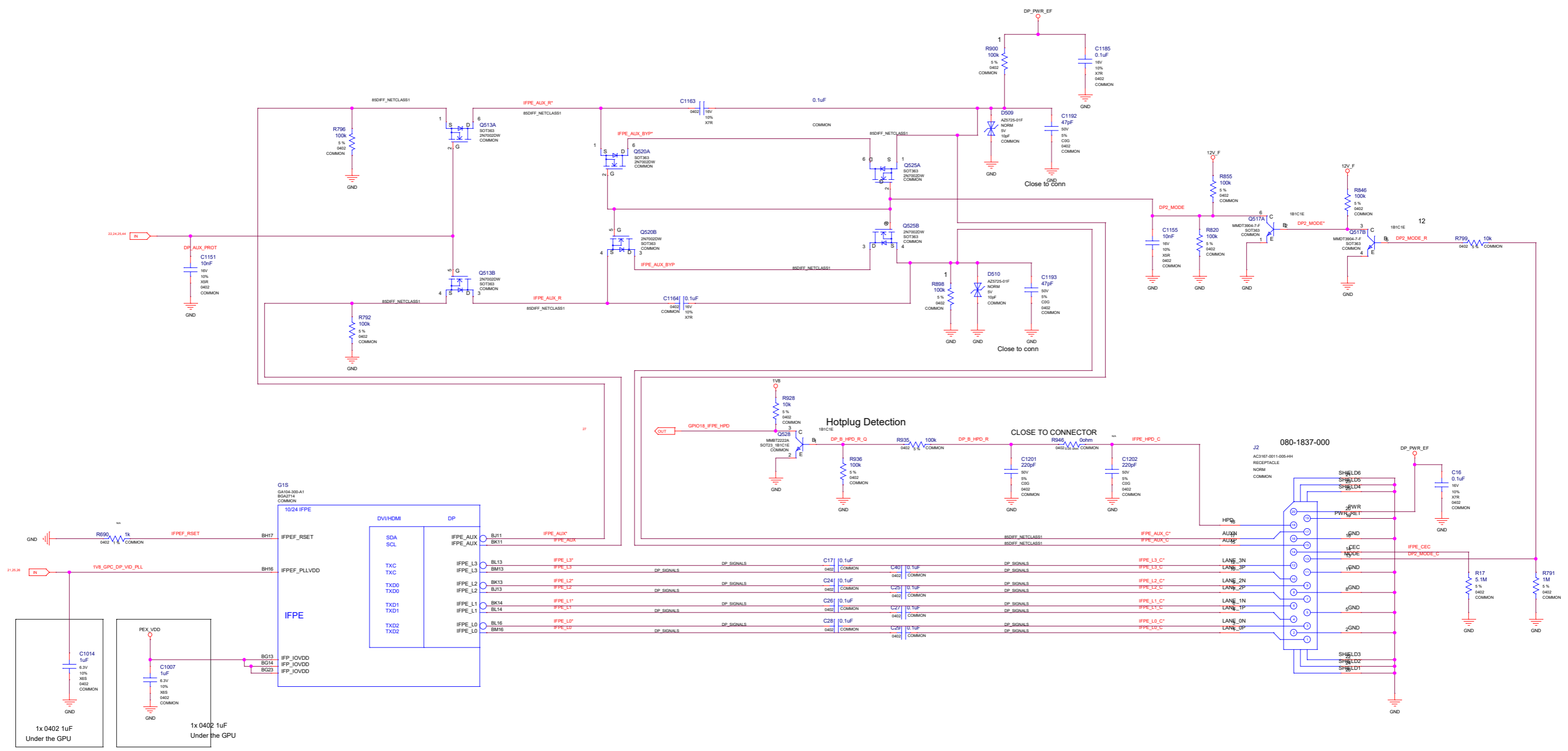


Fused DP\_PWR

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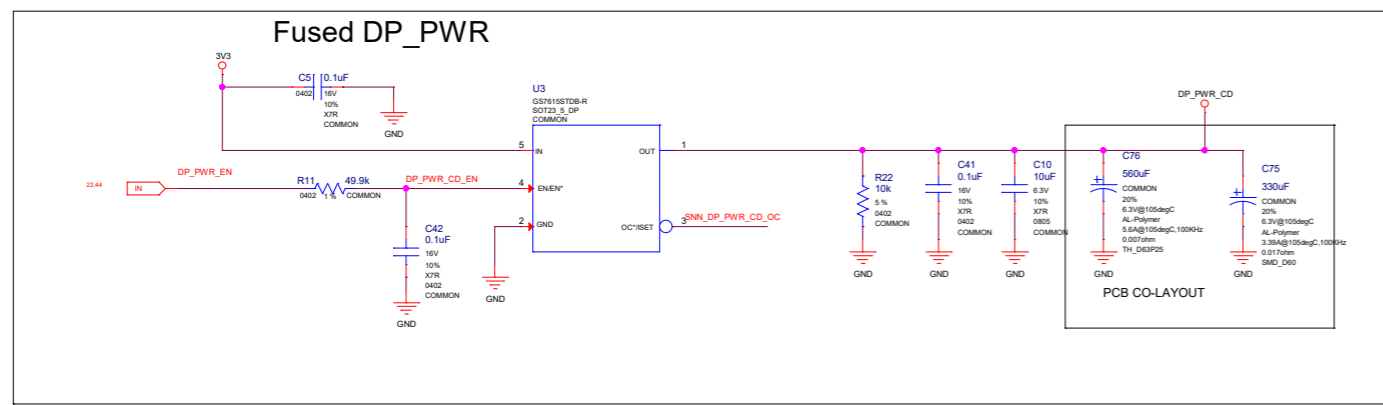
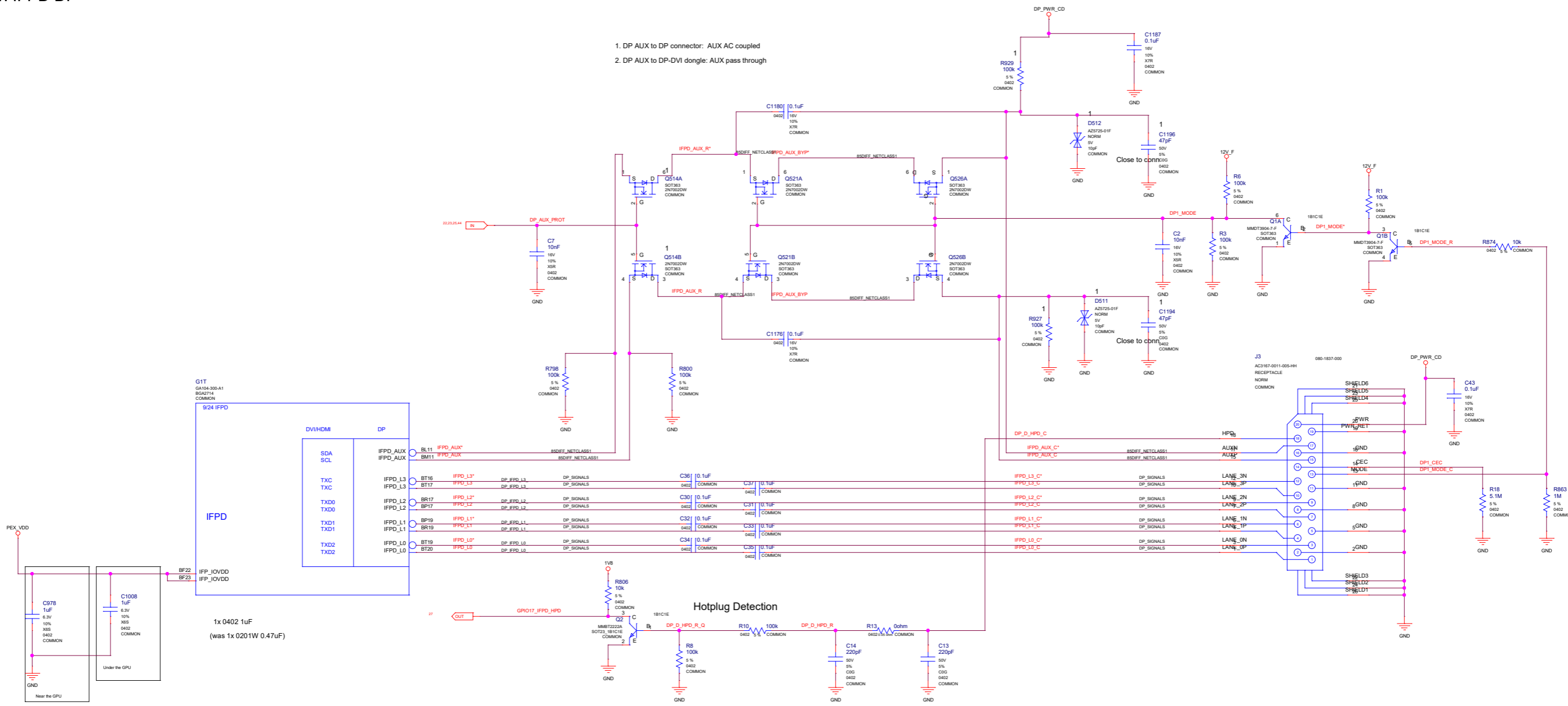
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

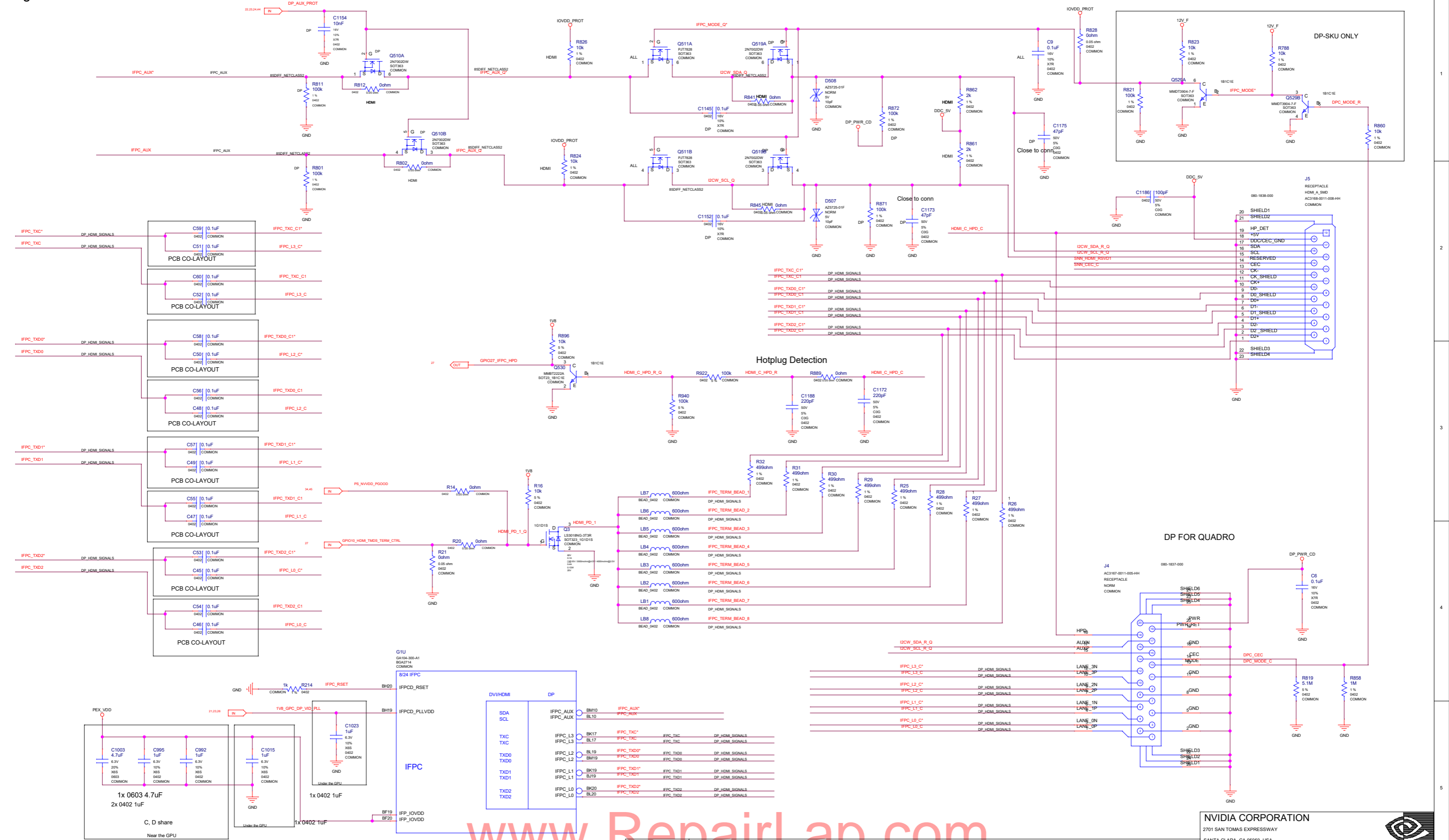


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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M

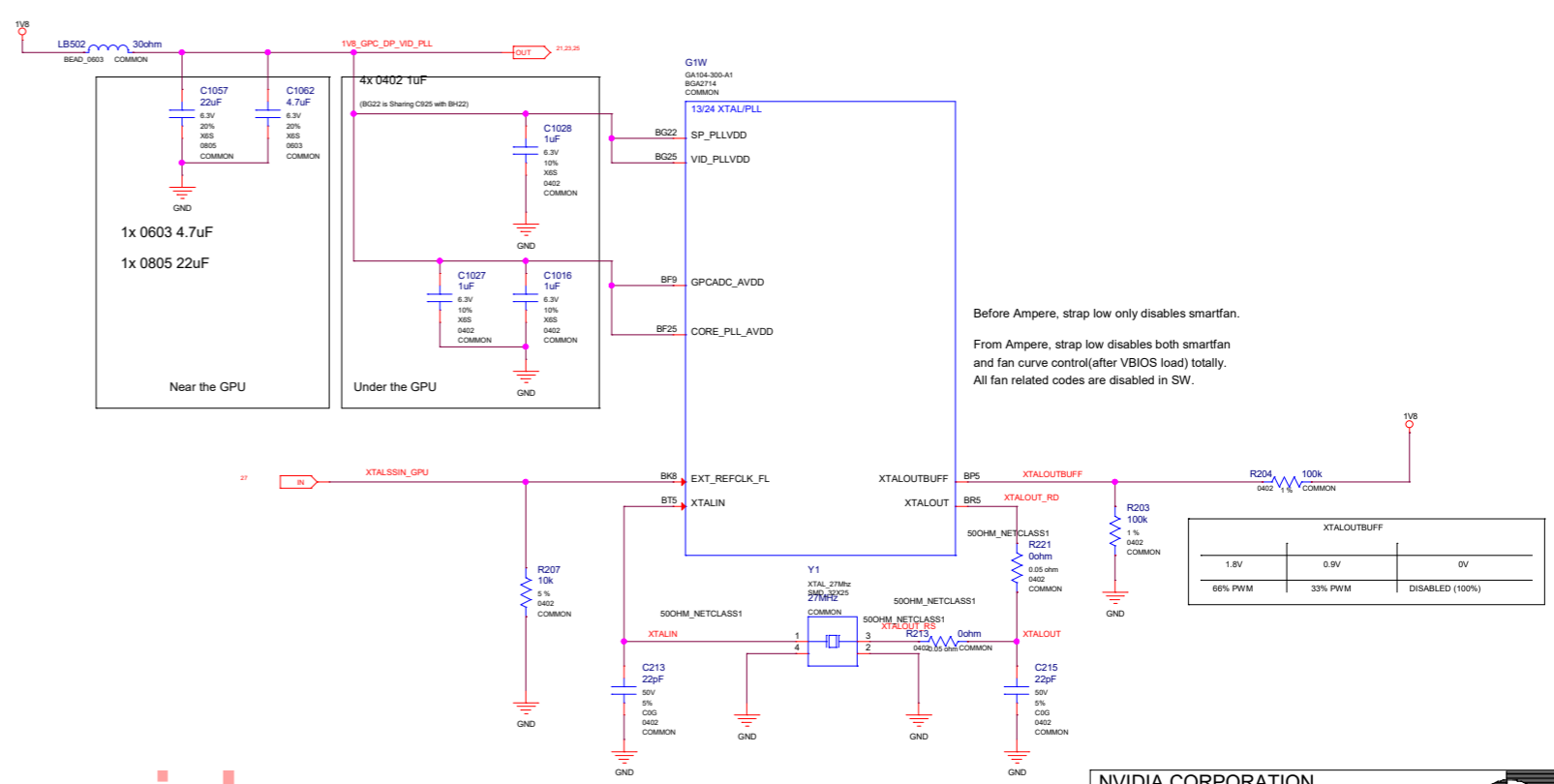
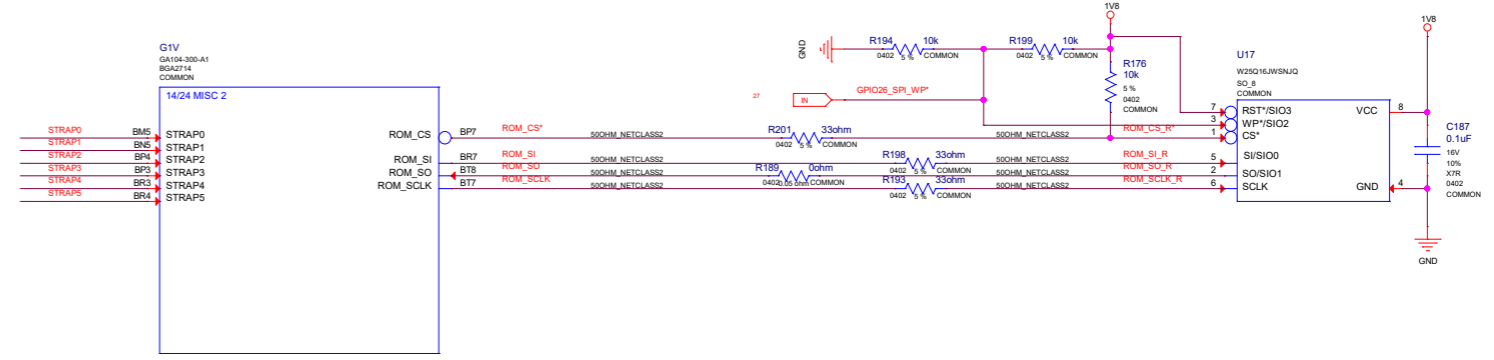
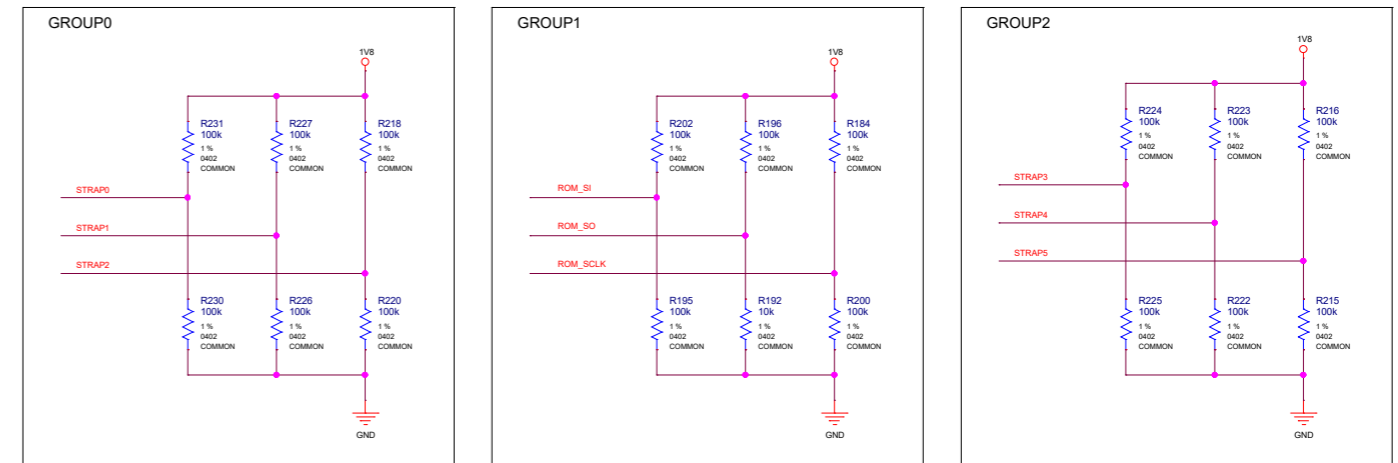
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	4'd7	FS_OVERT ENABLE
L	M	L	4'd9	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
L	L	L	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



Before Ampere, strap low only disables smartfan.  
From Ampere, strap low disables both smartfan and fan curve control(after VBIOS load) totally. All fan related codes are disabled in SW.

XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

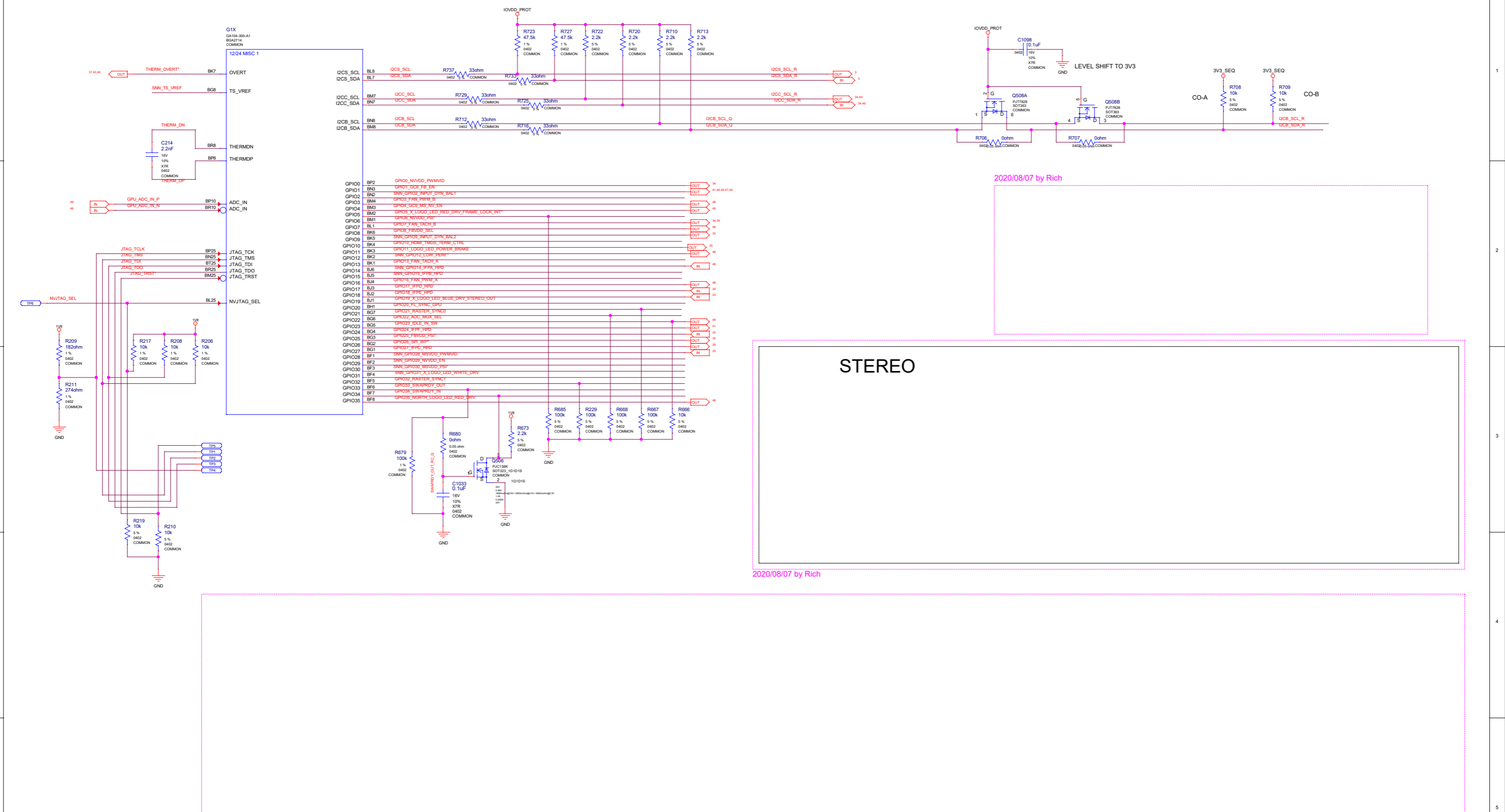
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A B C D E F G H

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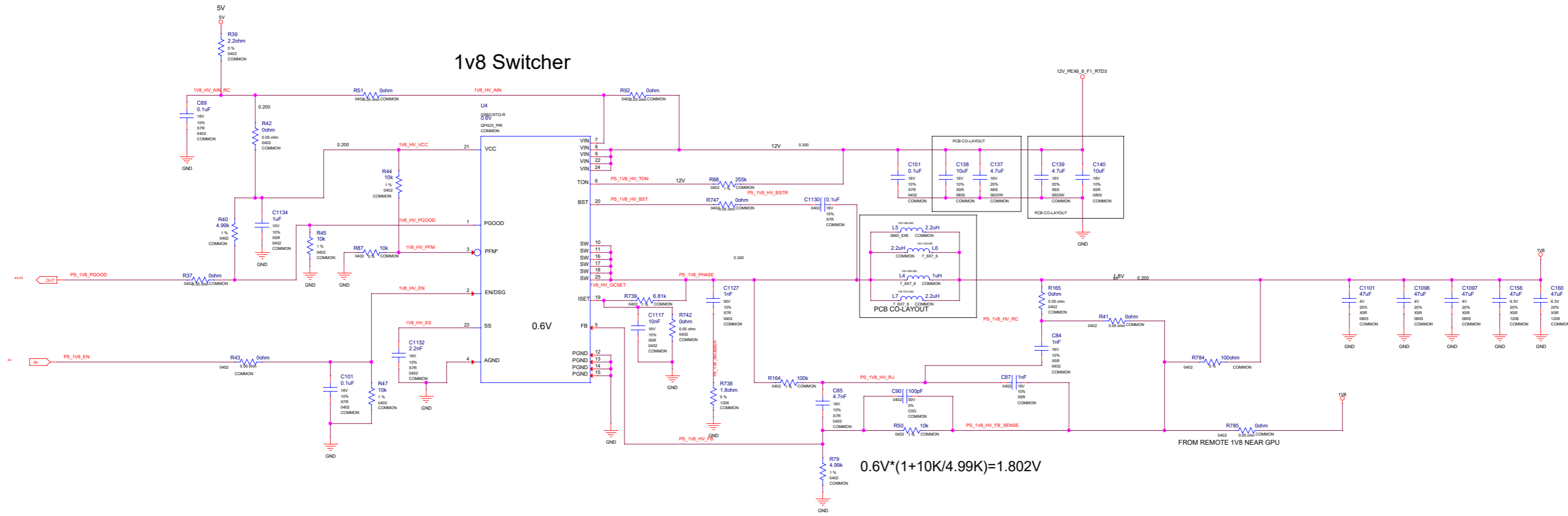
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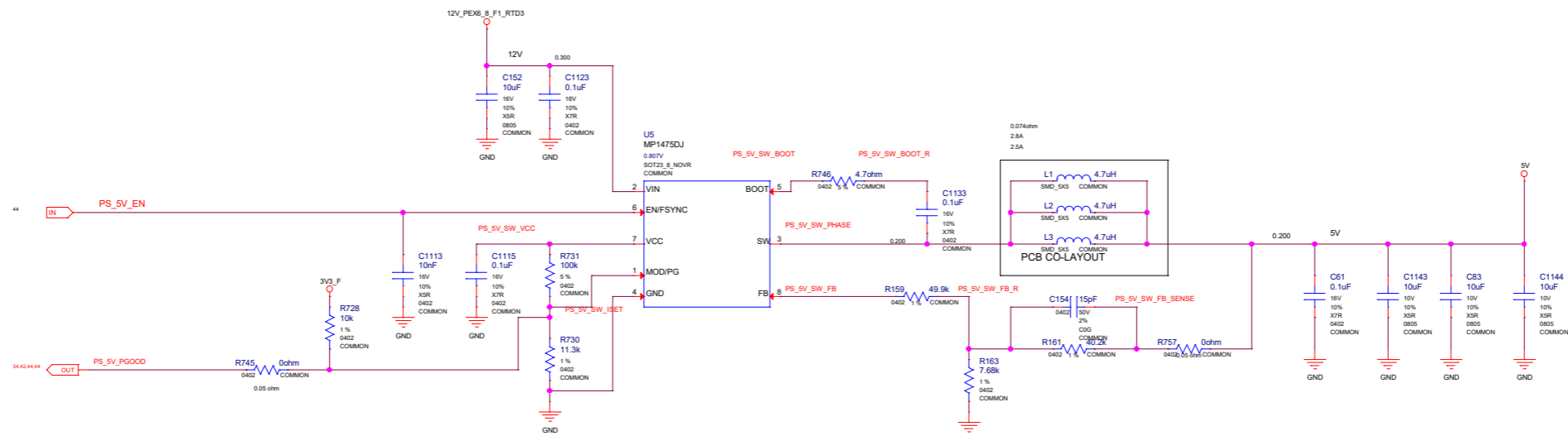
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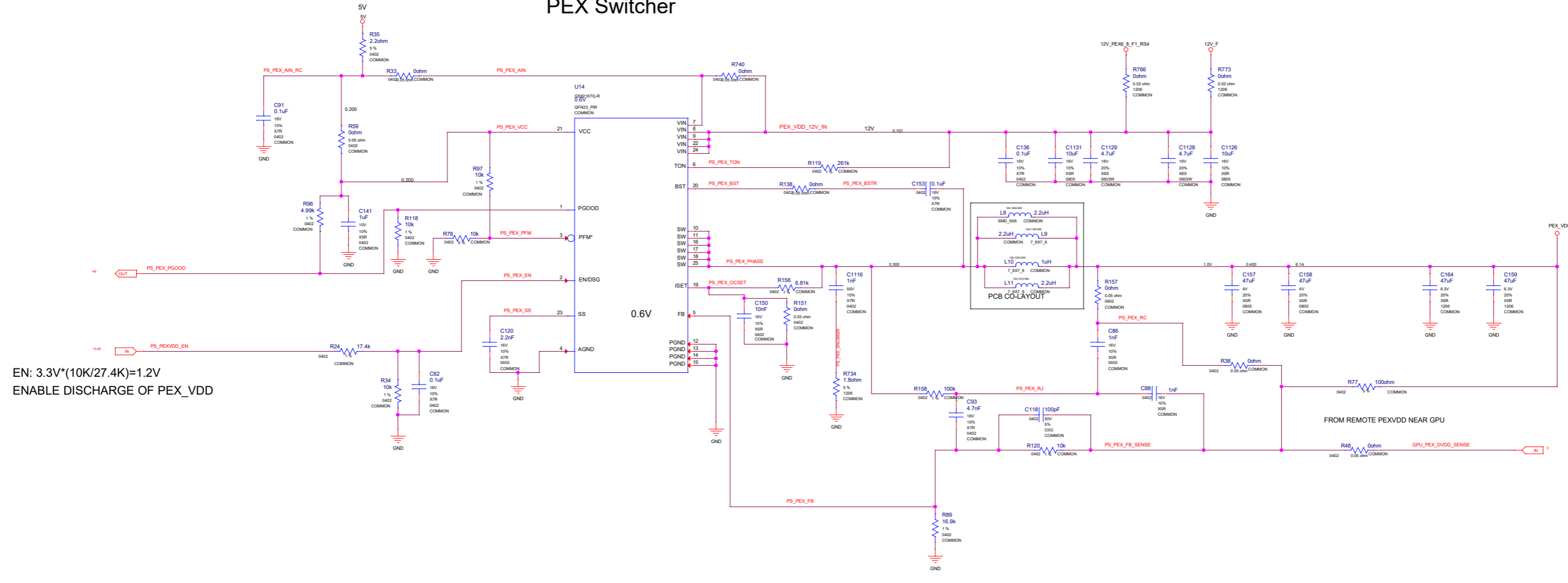
$$0.8V * (1 + 40.2K / 7.68K) = 4.9875V$$

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### PEX Switcher




EN:  $3.3V * (10K/27.4K) = 1.2V$   
 ENABLE DISCHARGE OF PEX\_VDD

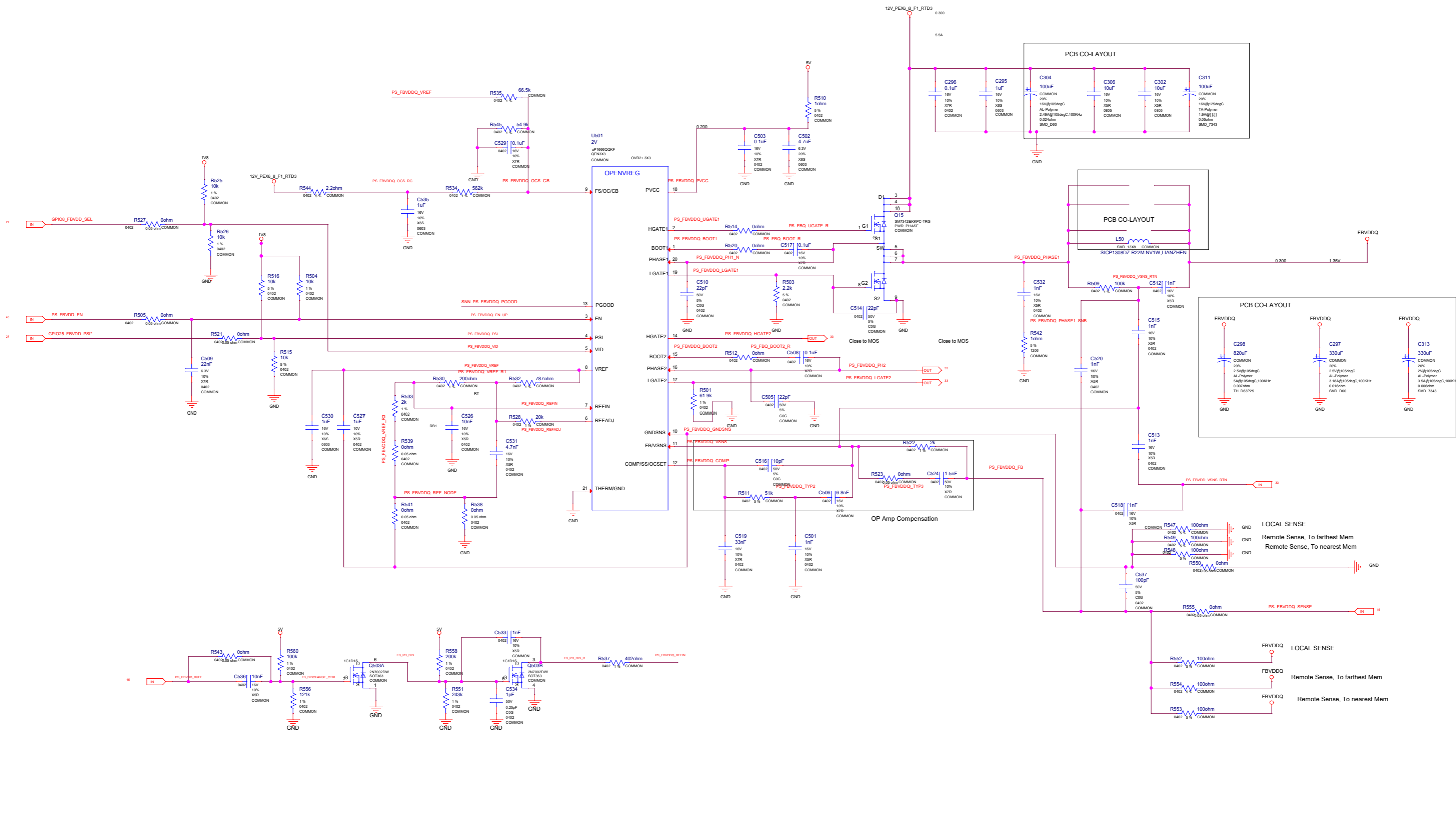
0.6V

$0.6V * (1 + 10K/16.9K) = 0.9550V$

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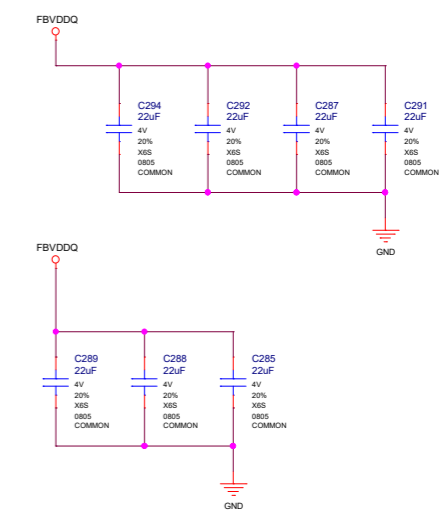
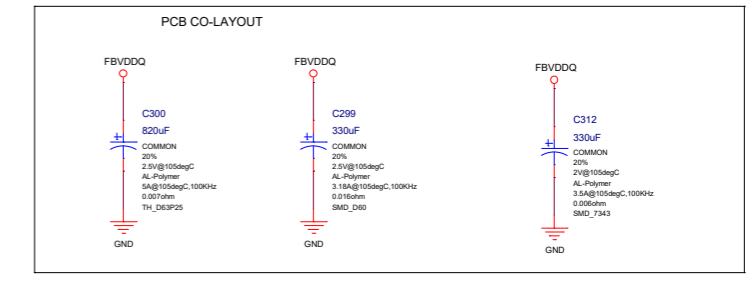
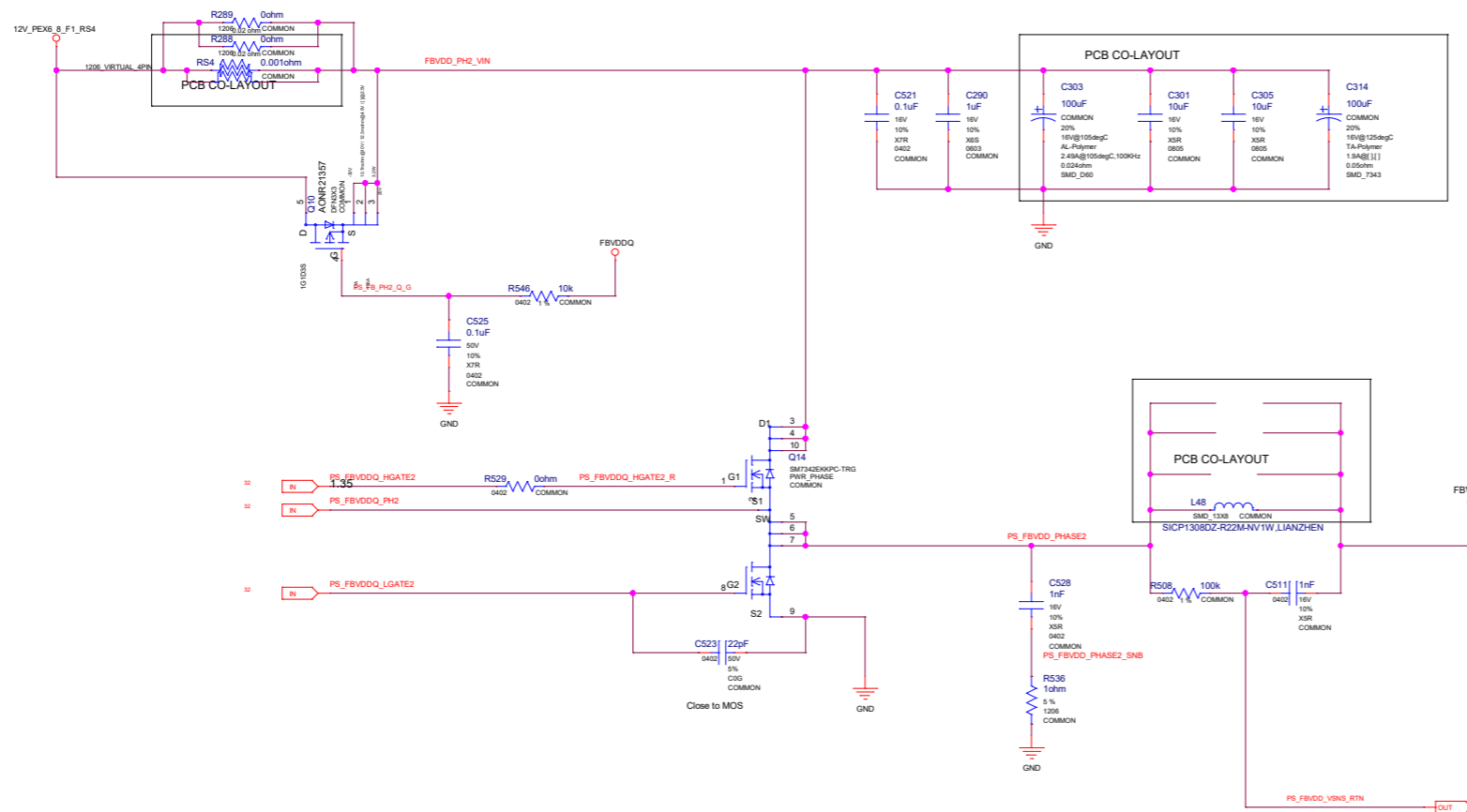
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FBVDD PH2 INPUT ANTI-BACKDRIVE

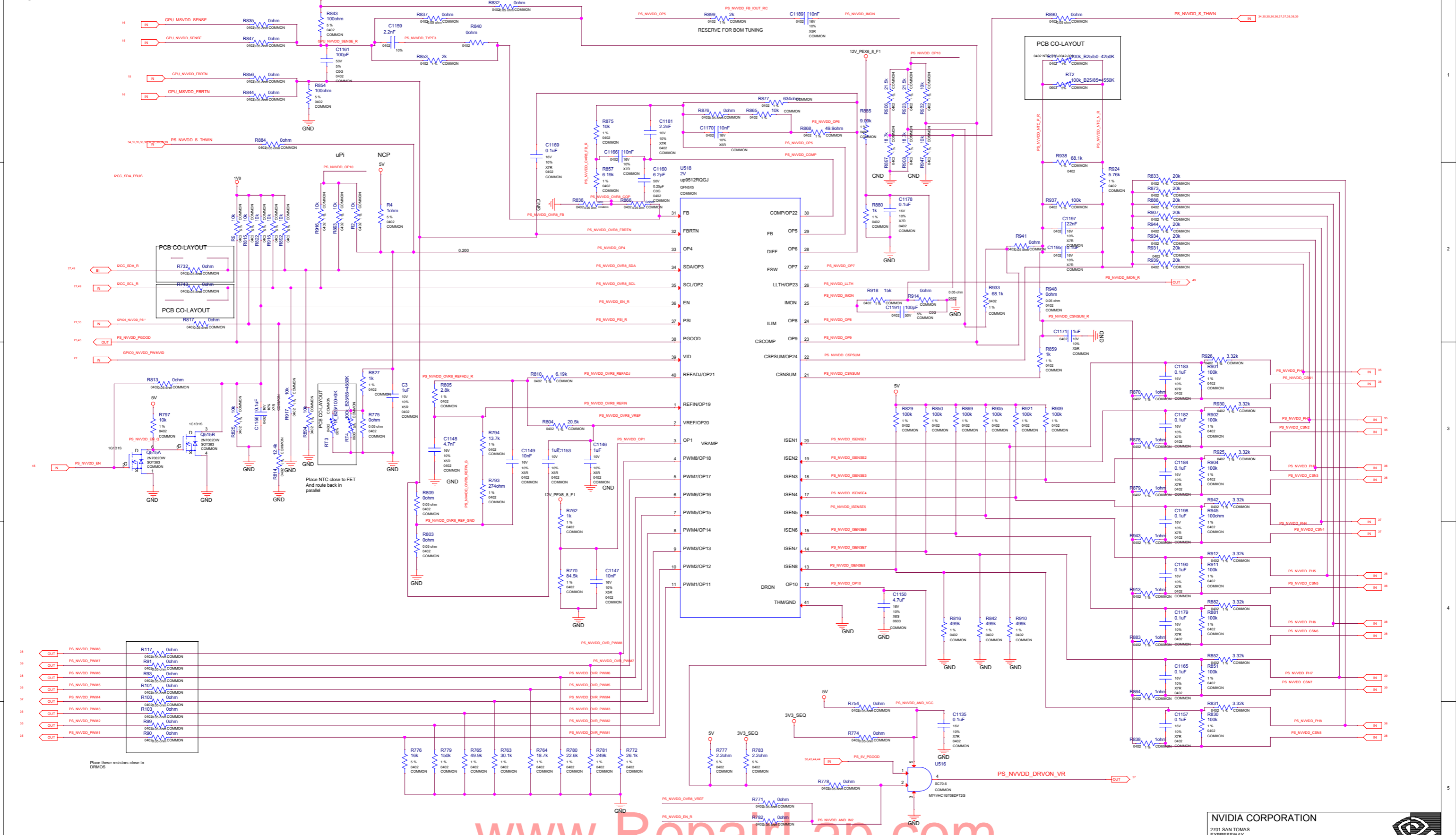


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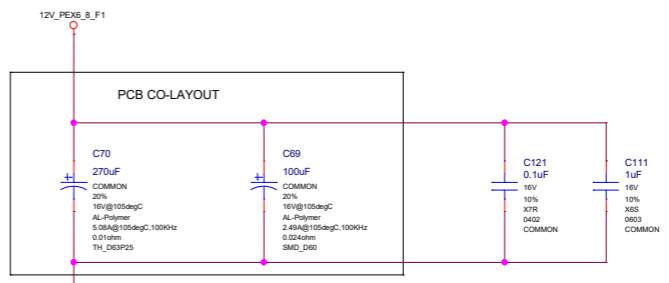
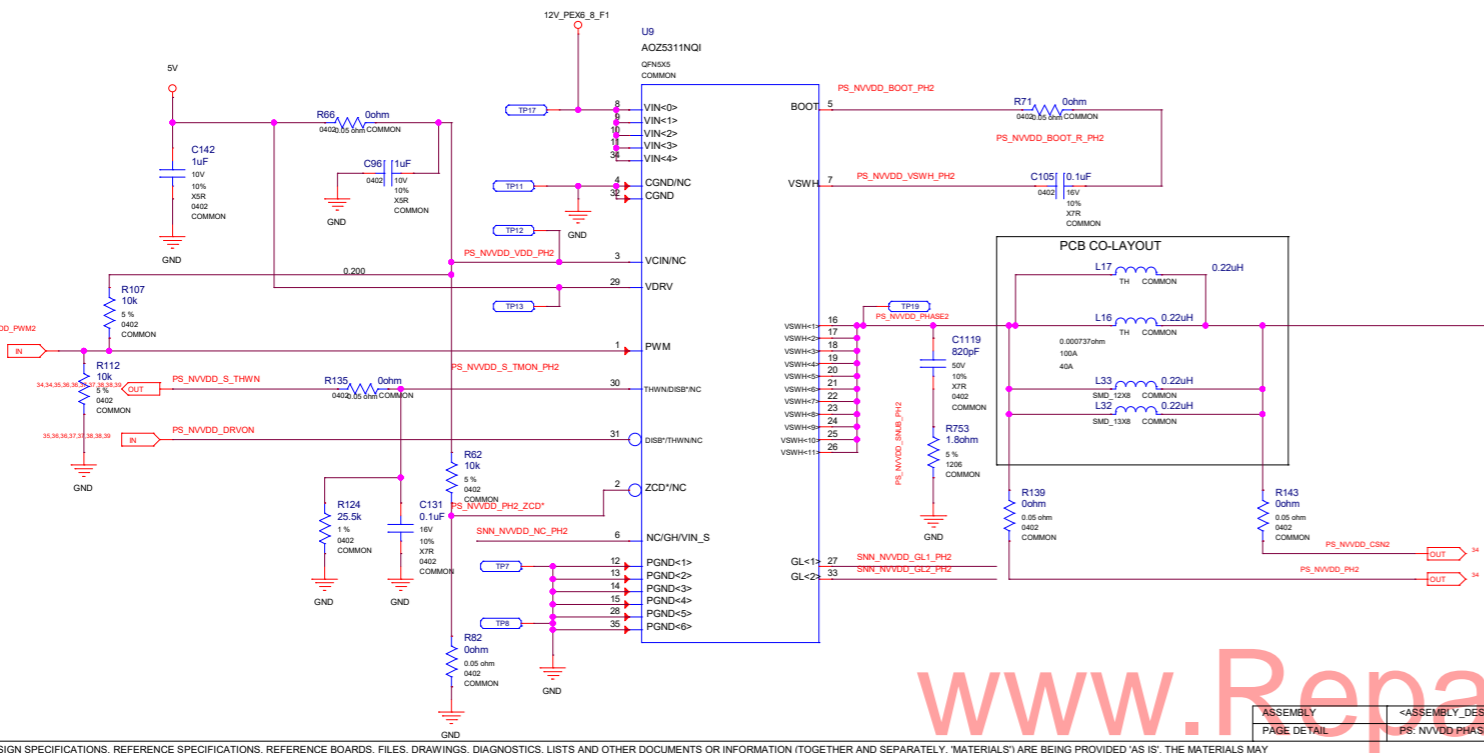
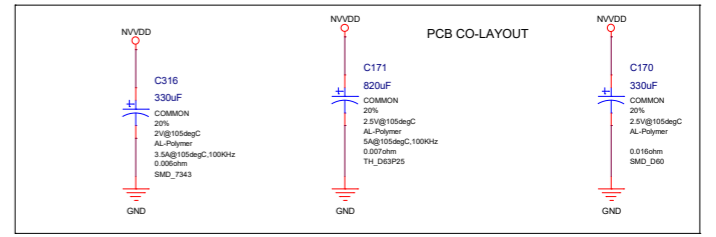
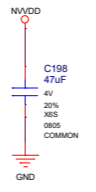
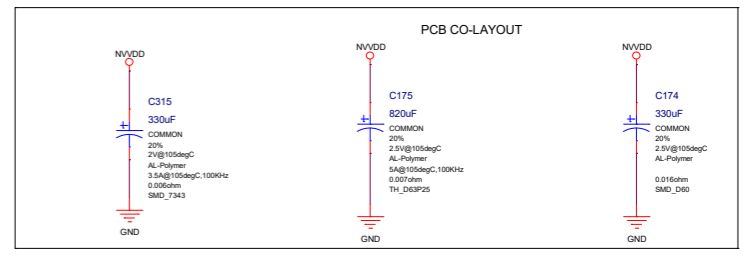
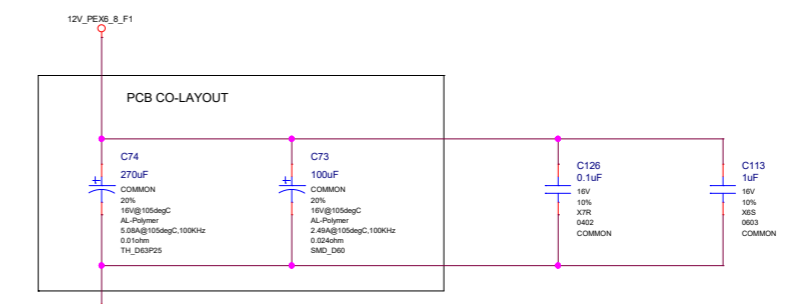
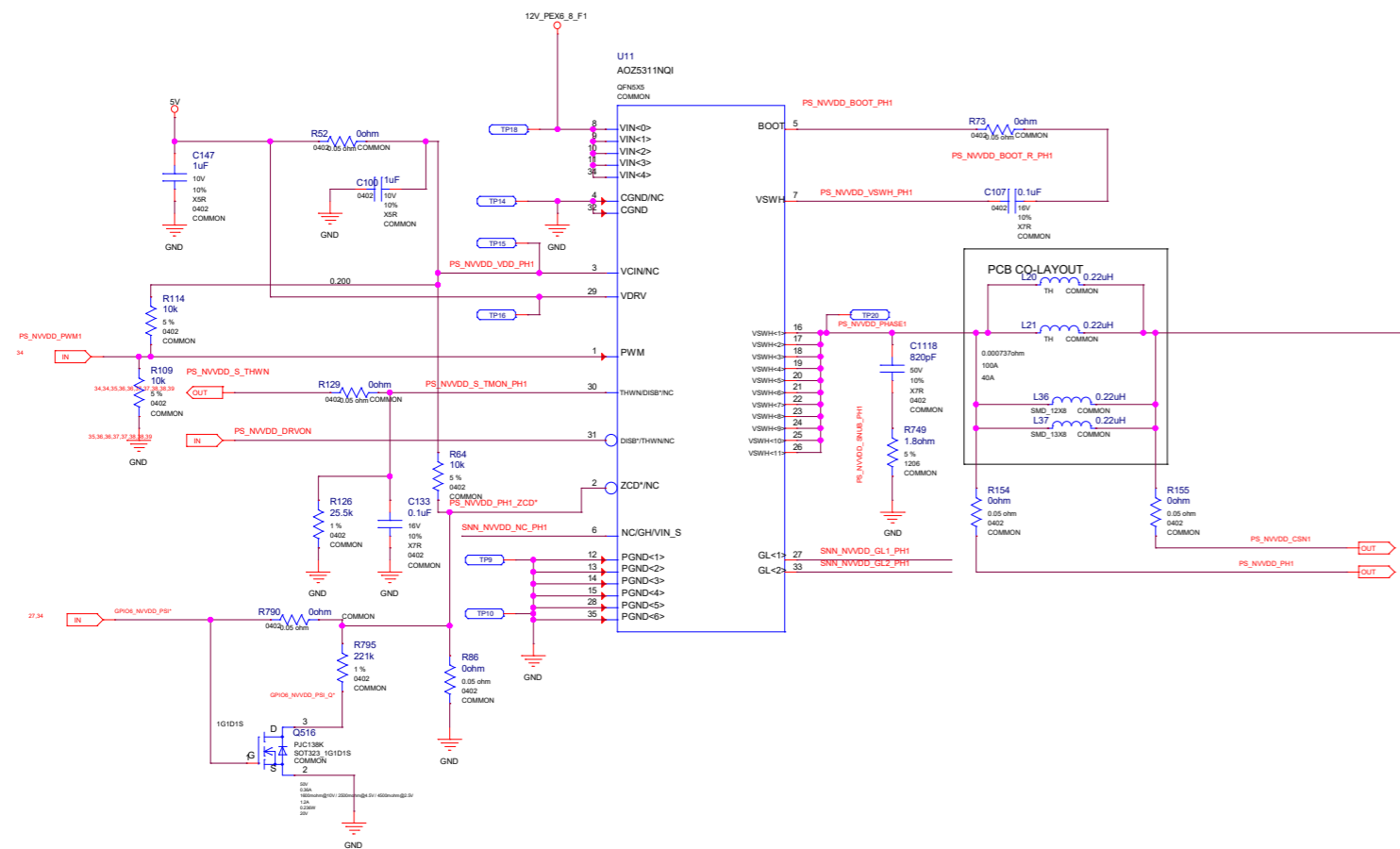
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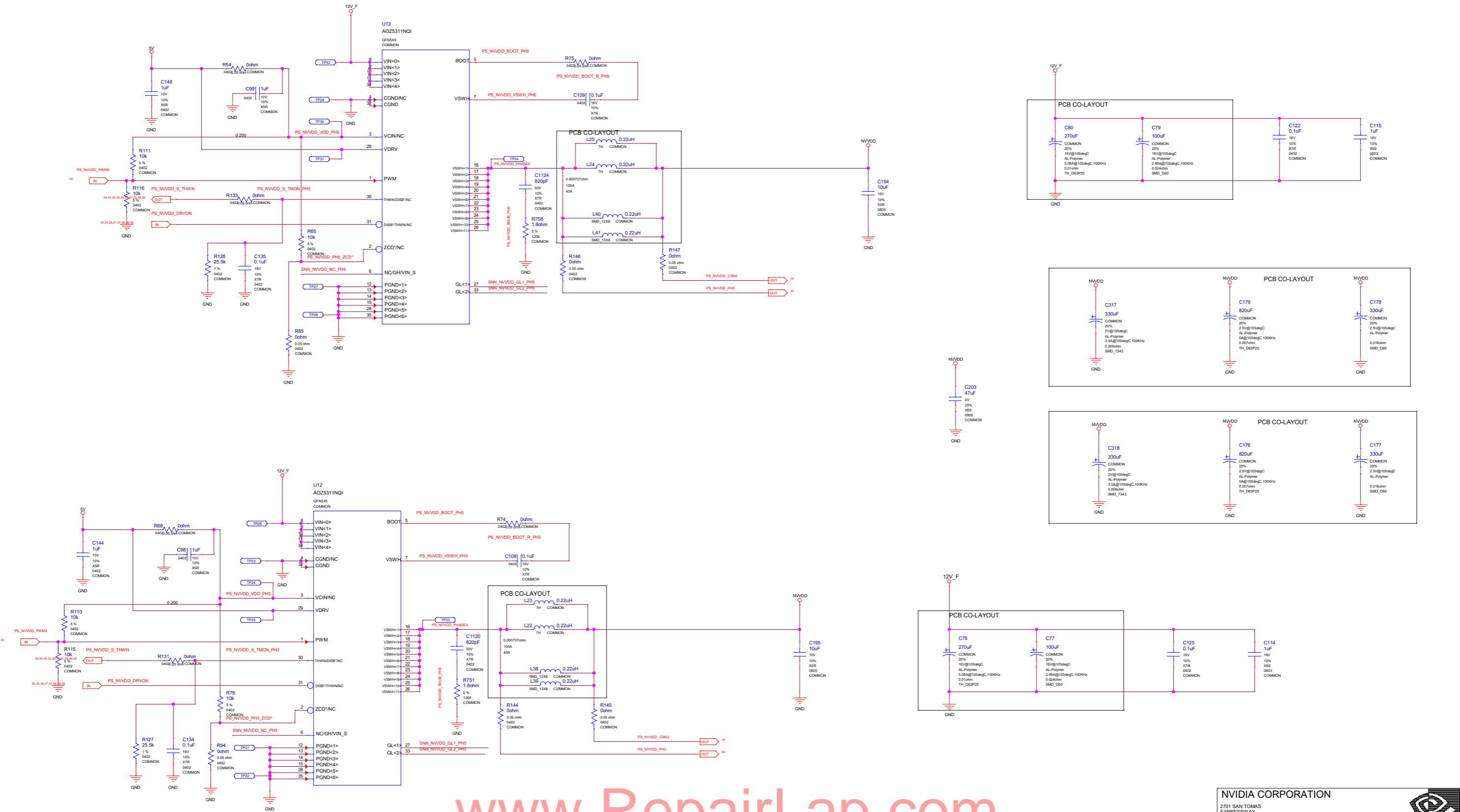
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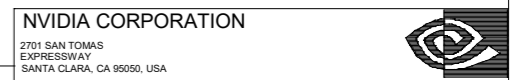
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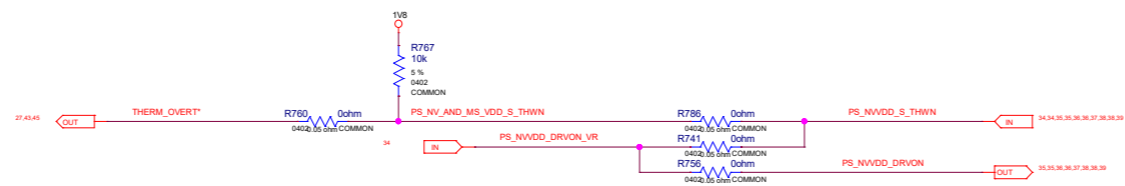
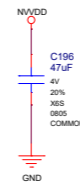
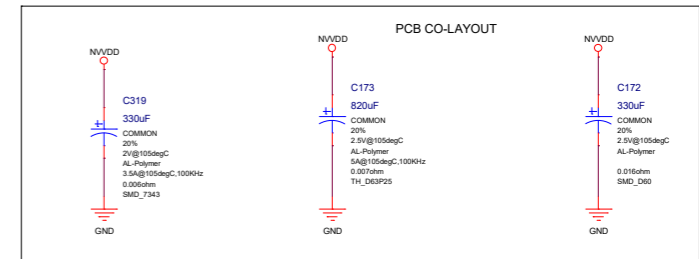
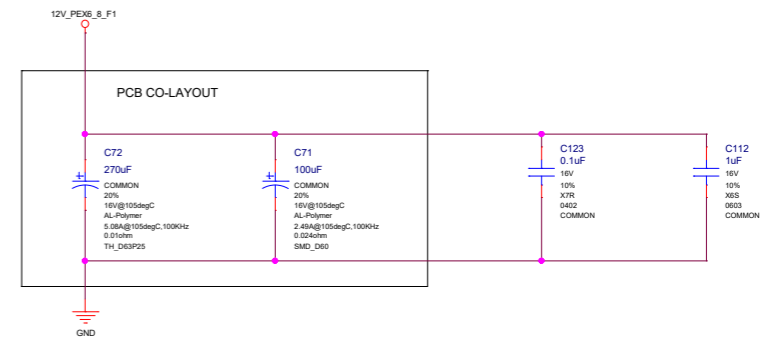
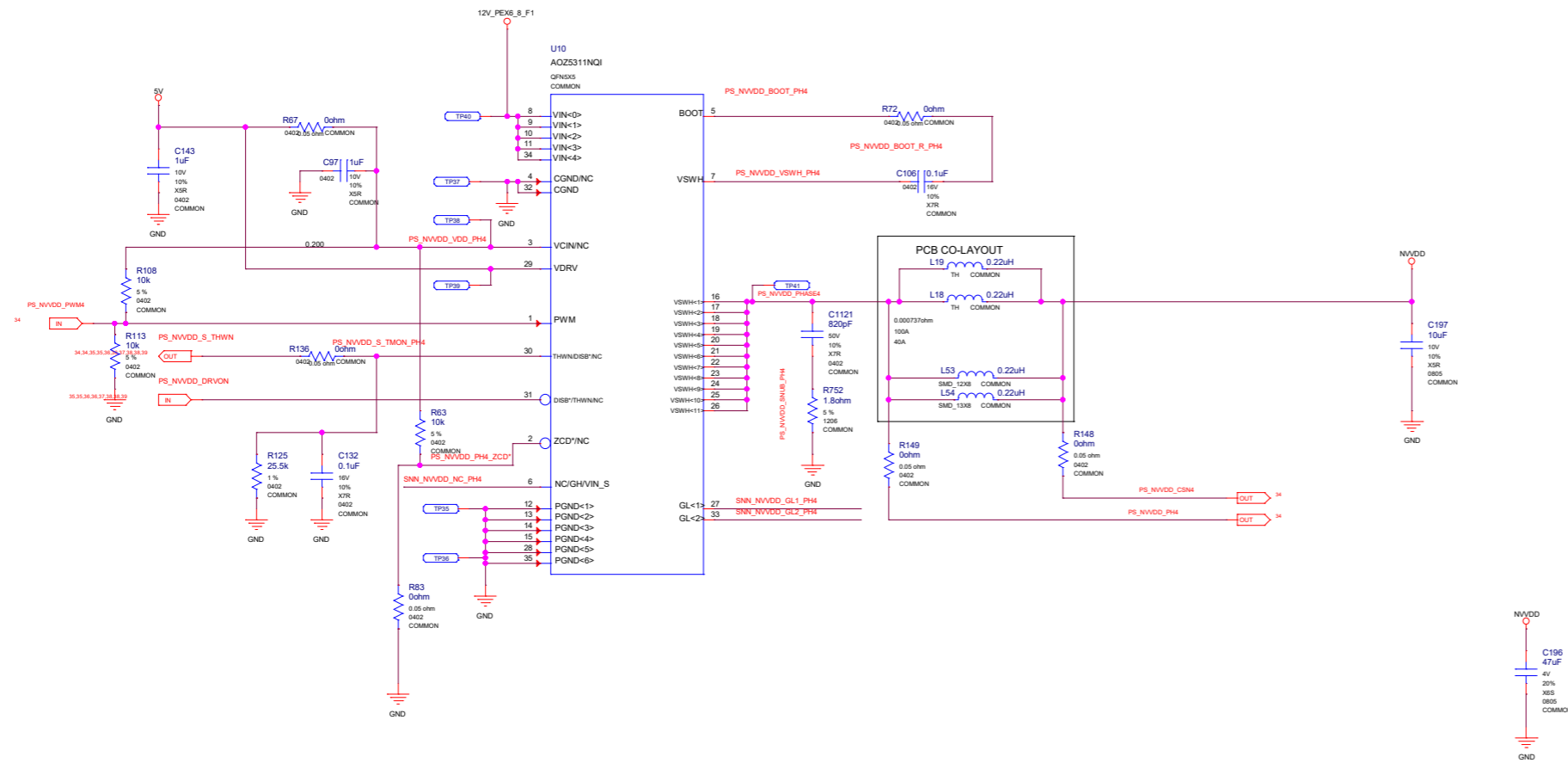
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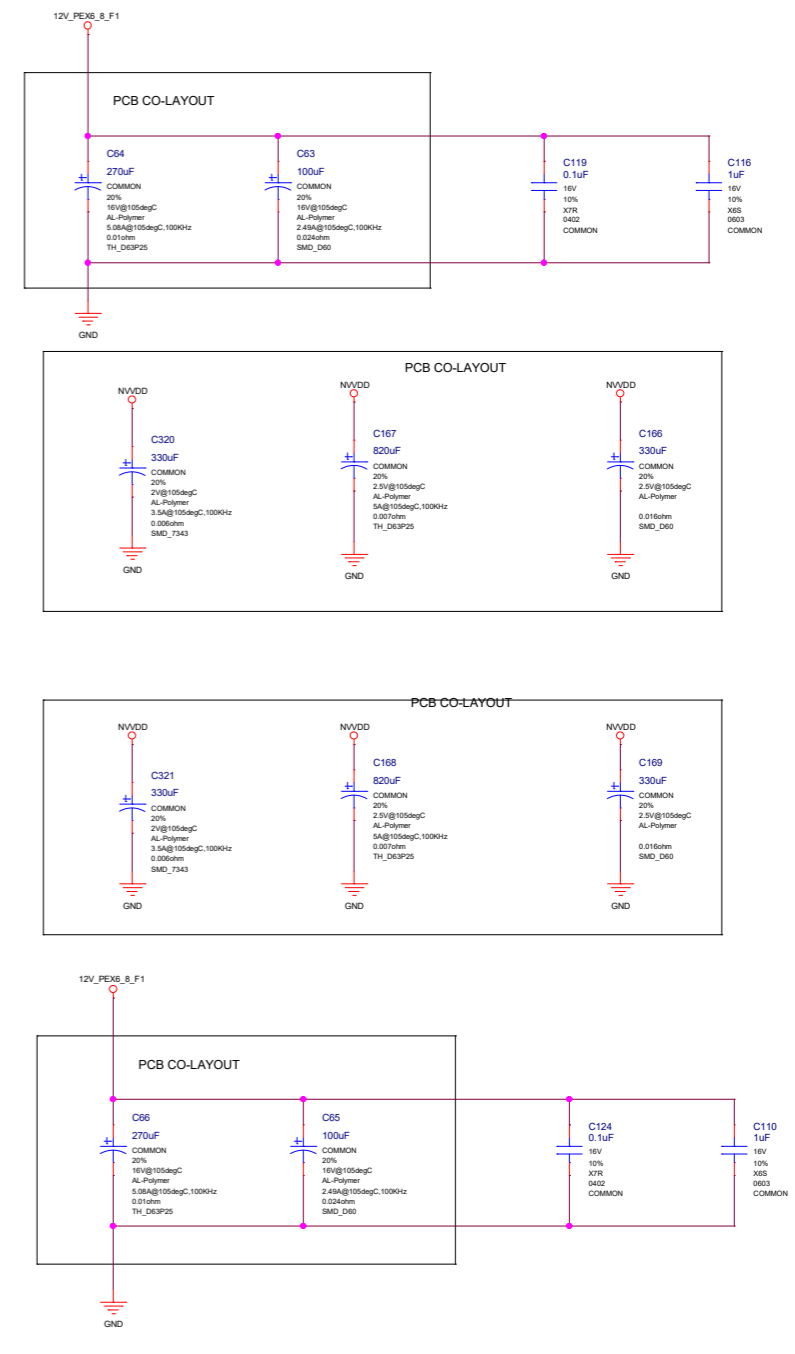
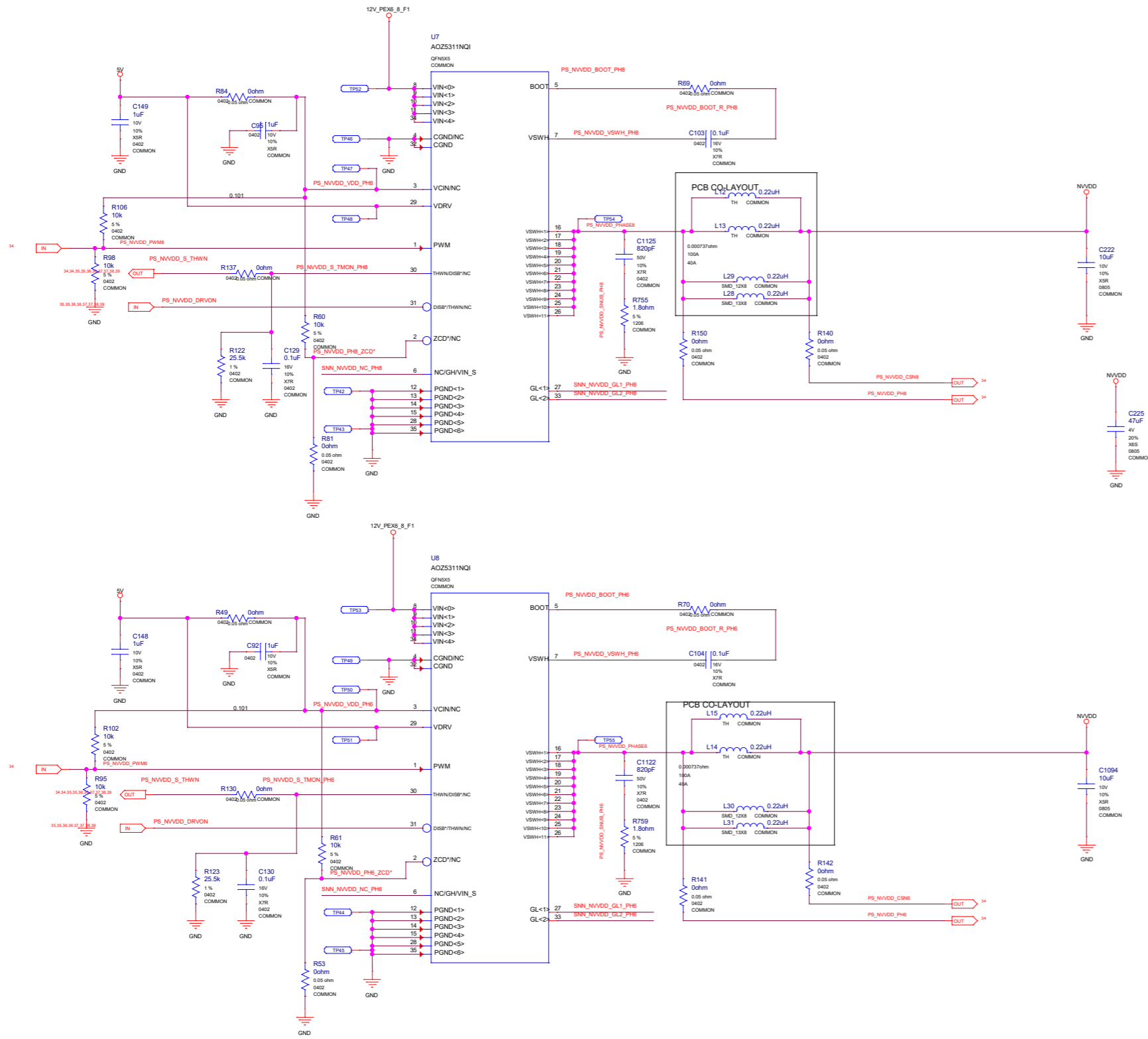
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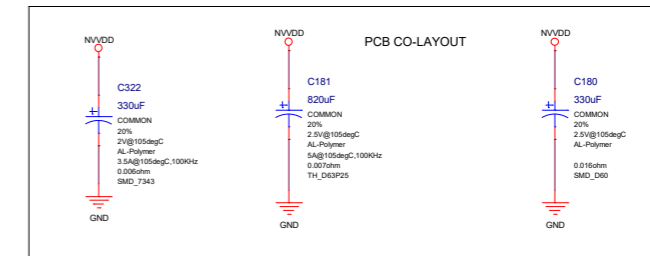
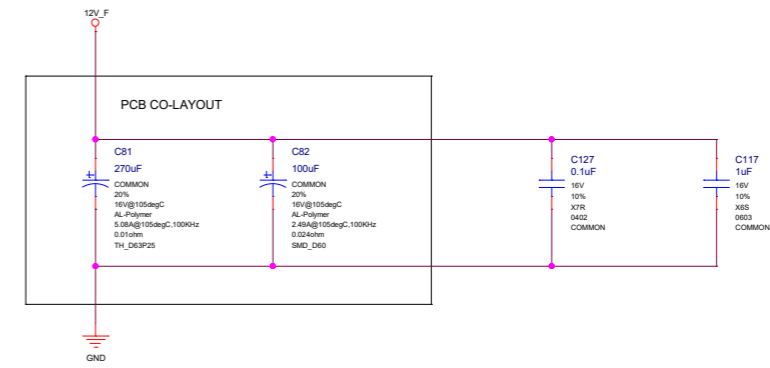
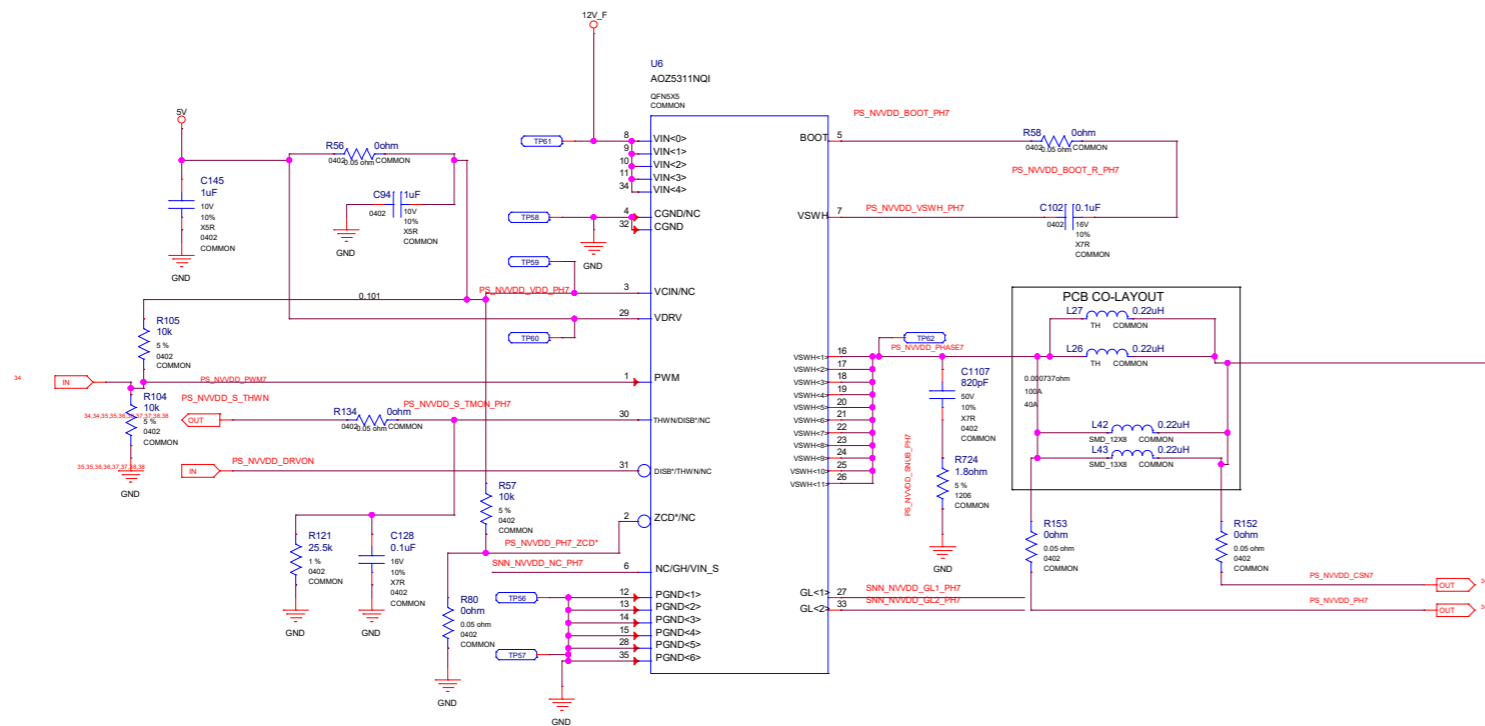
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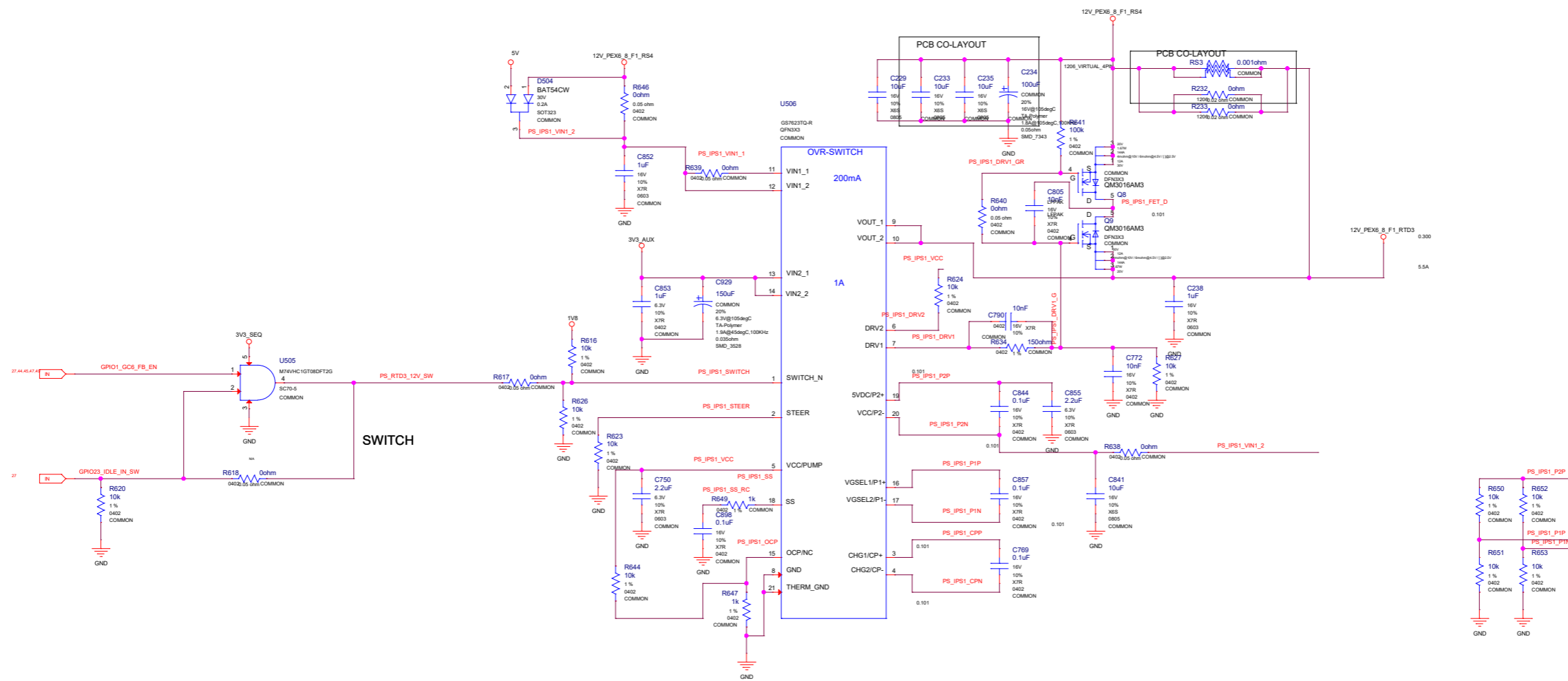


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A B C D E F G H



AND GATE LOGIC					
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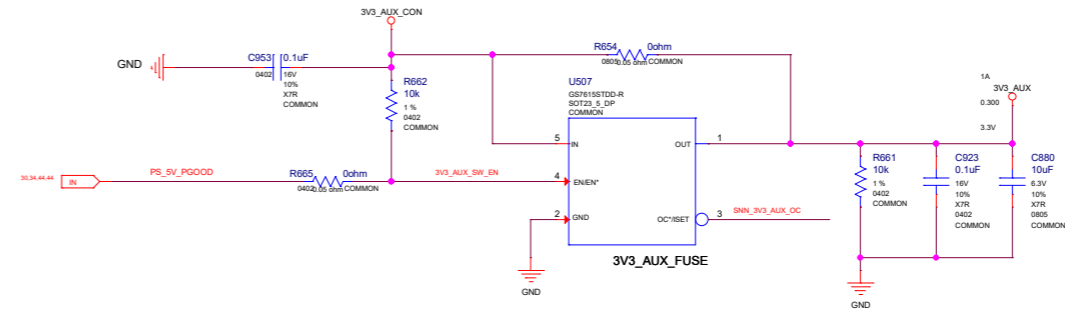
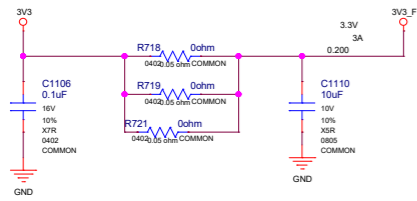


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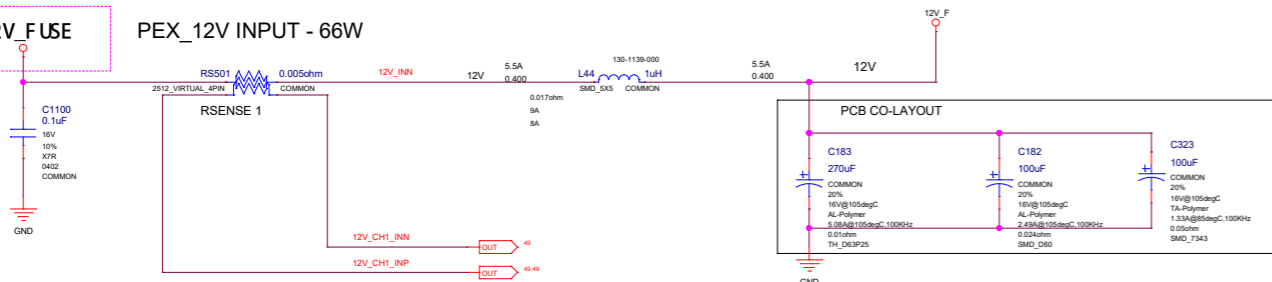
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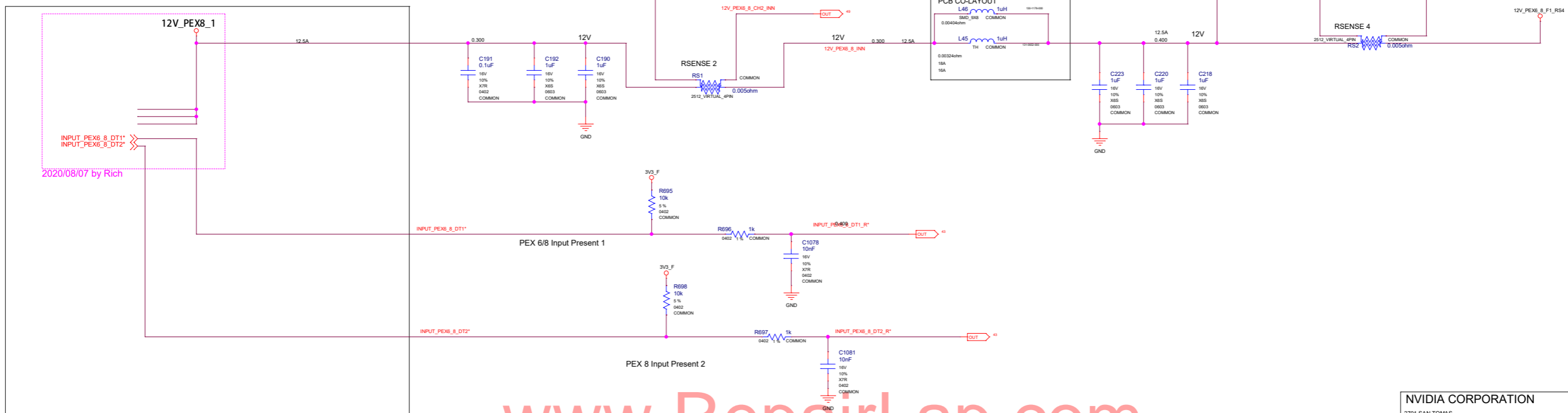
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2020/08/07 by Rich  
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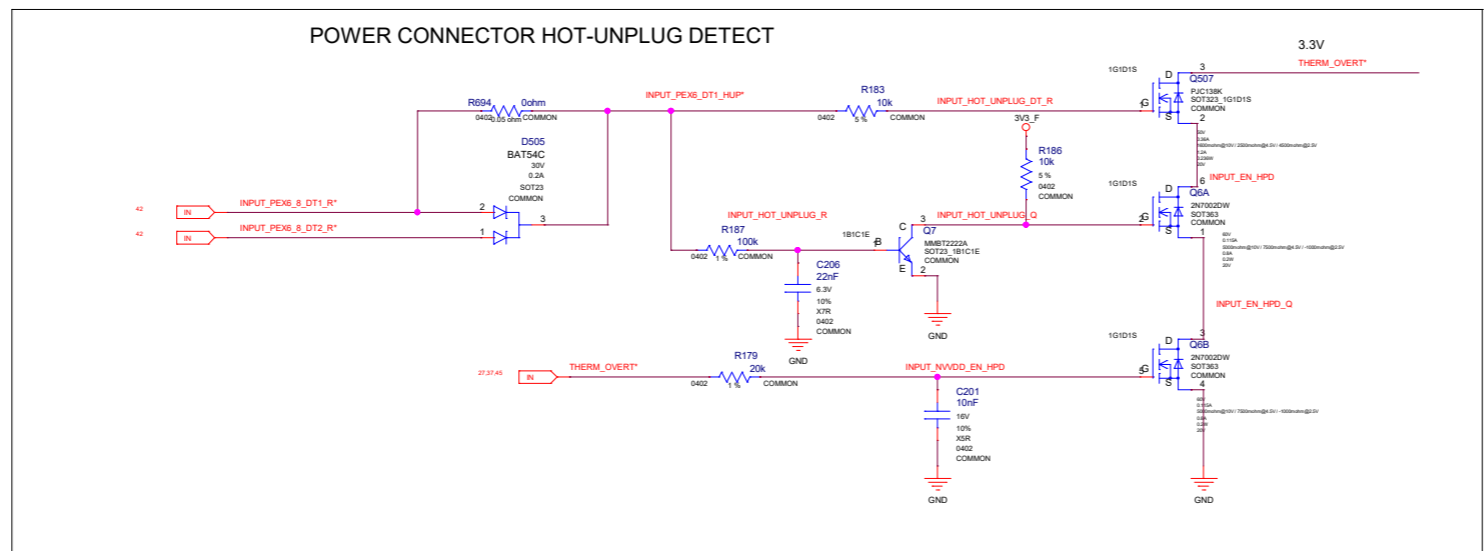
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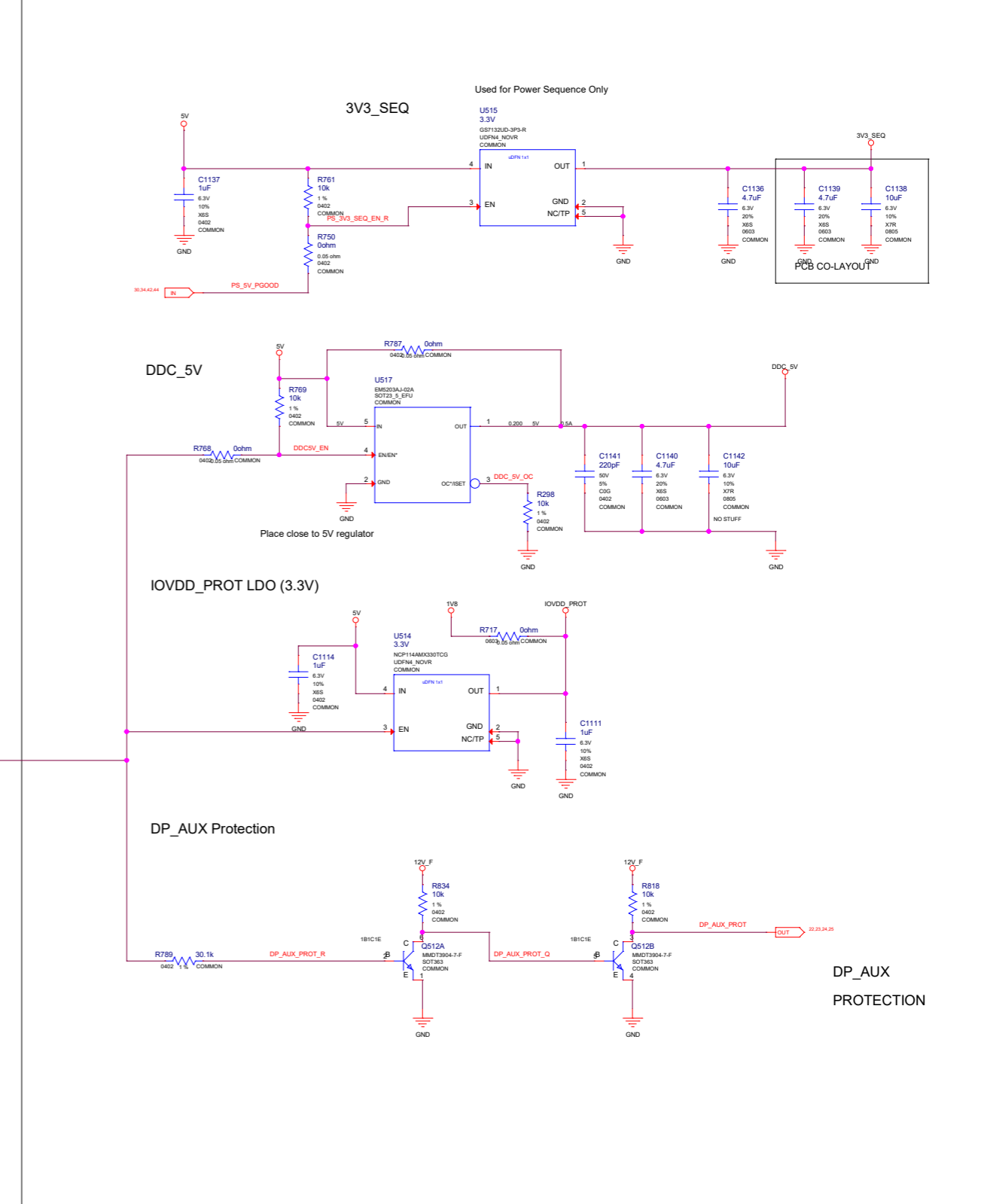
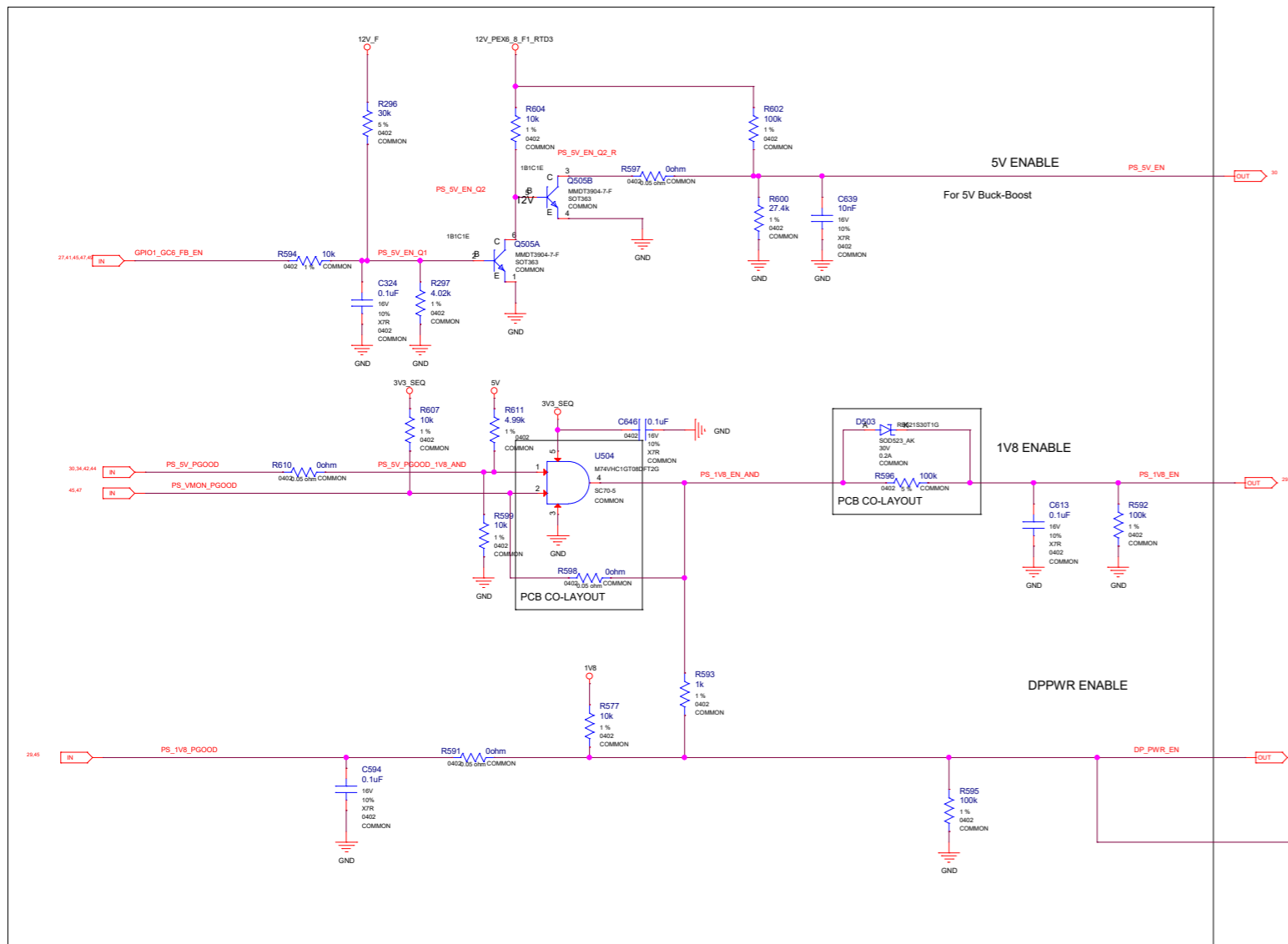


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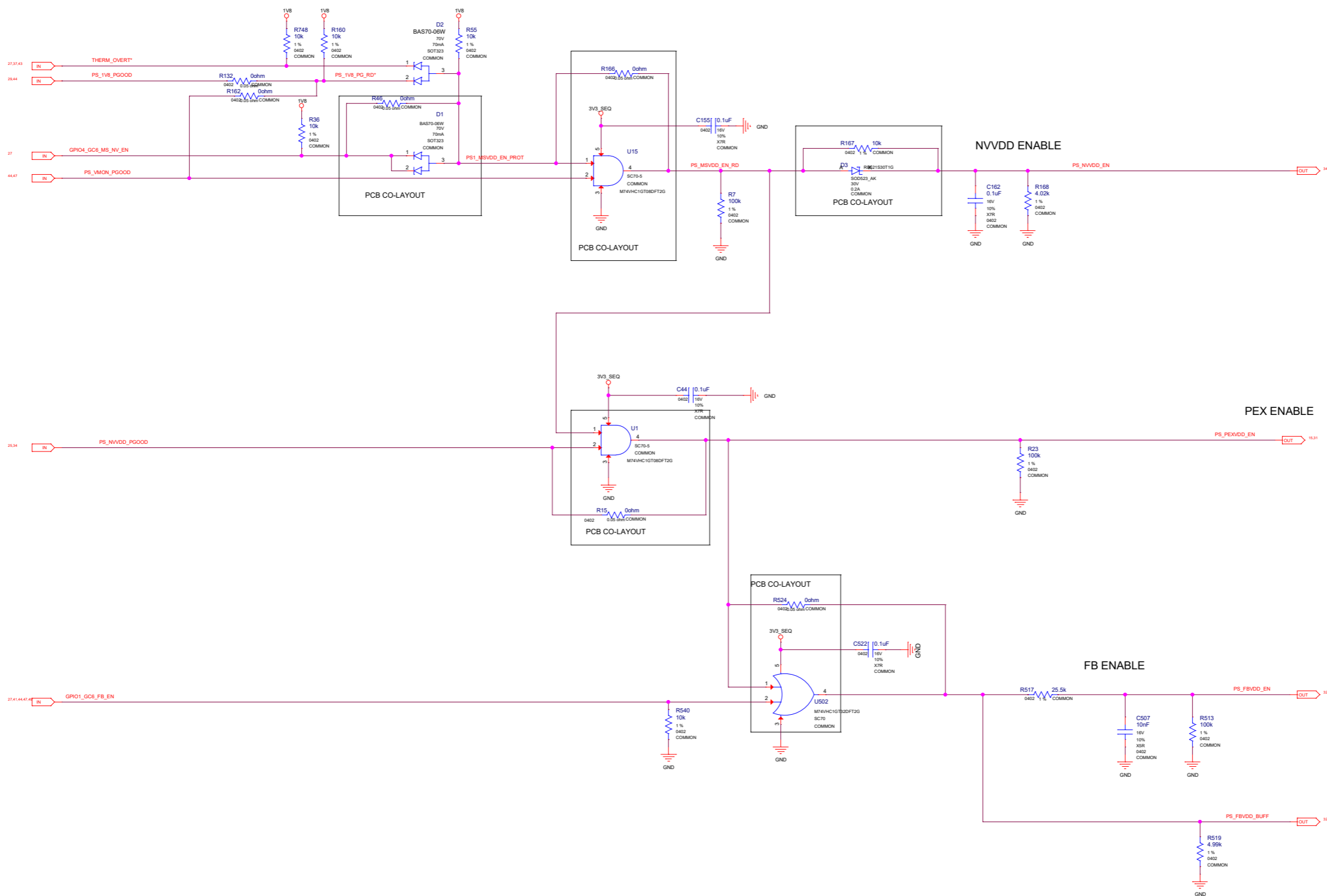


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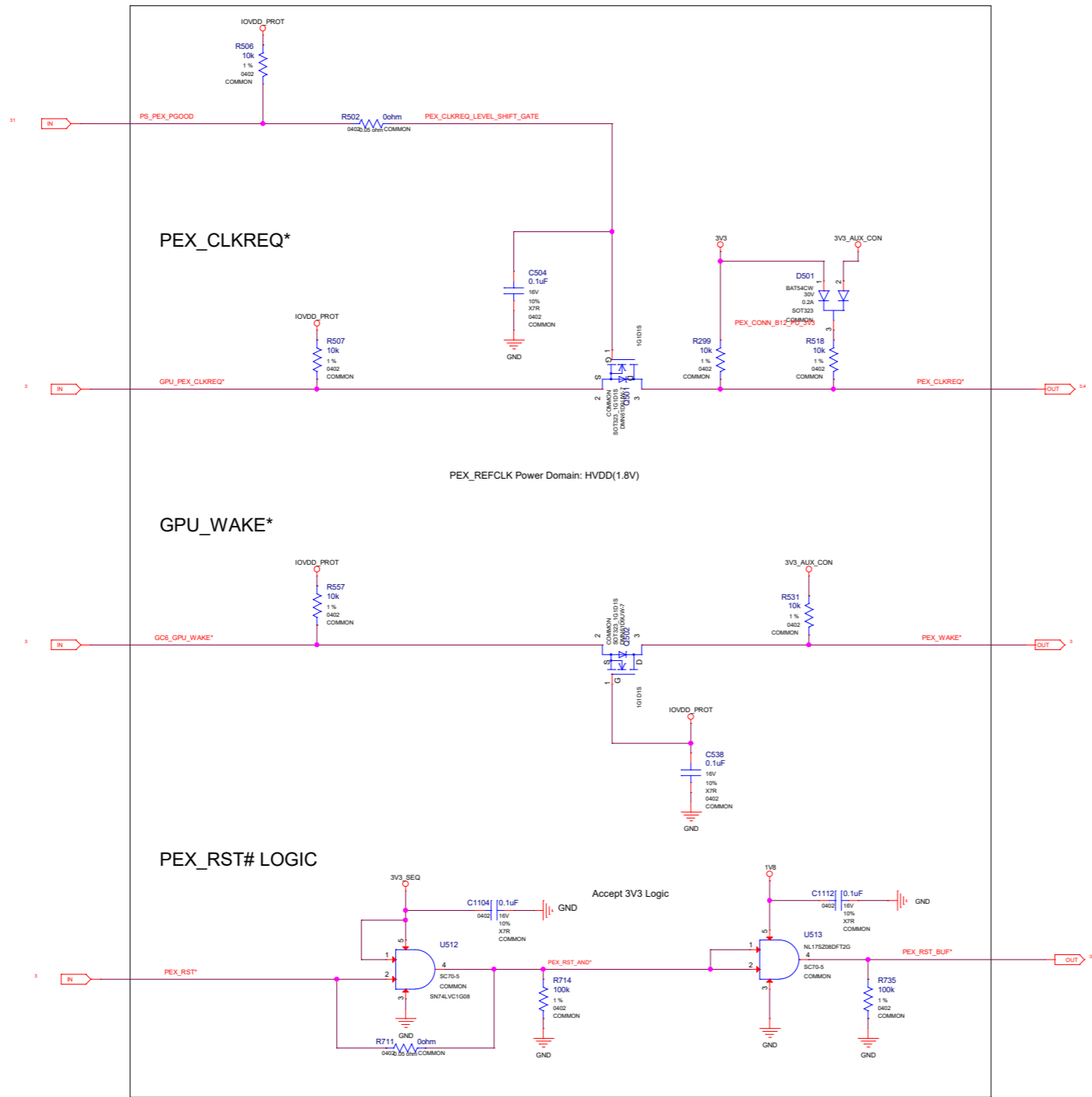


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 SEQ: NVVDD, PEXVDD AND FBVDDQ ENABLE



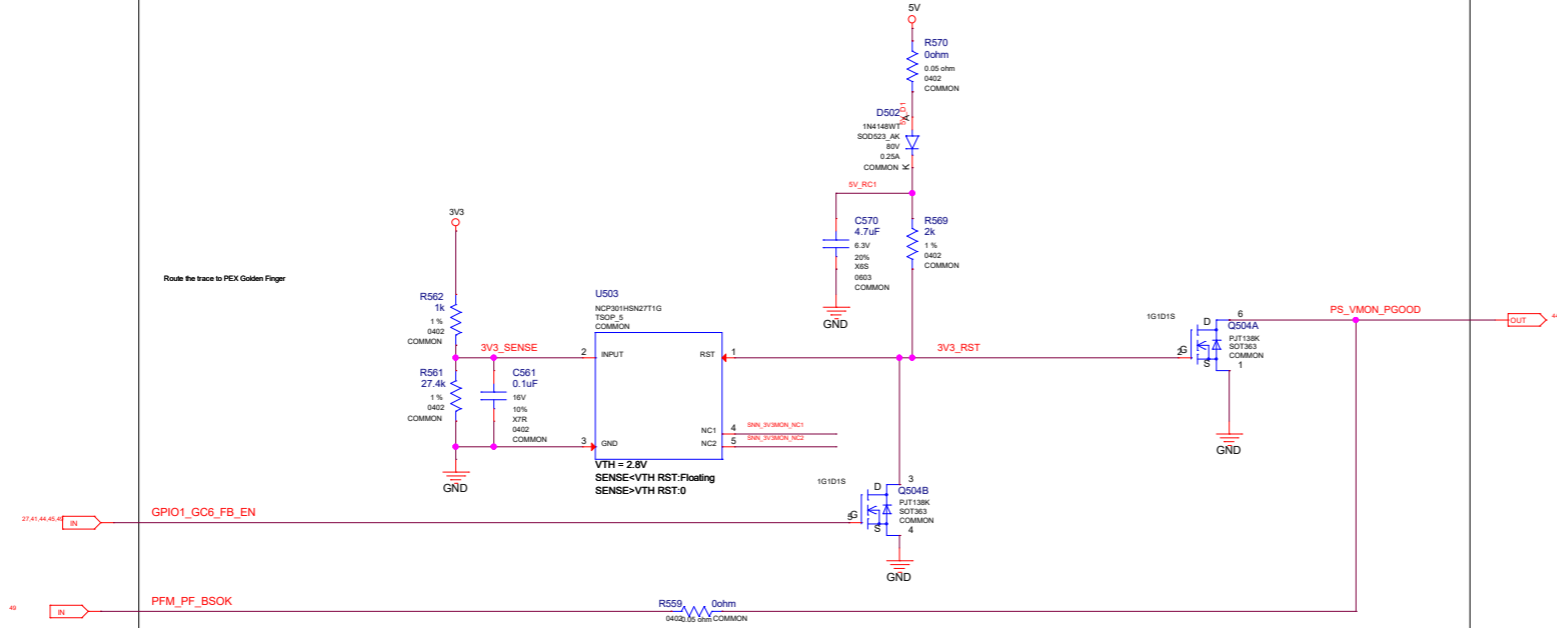
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ASSEMBLY PAGE DETAIL  
 <ASSEMBLY\_DESCRIPTION> SEQ: MISC

3V3PEX Voltage Monitor

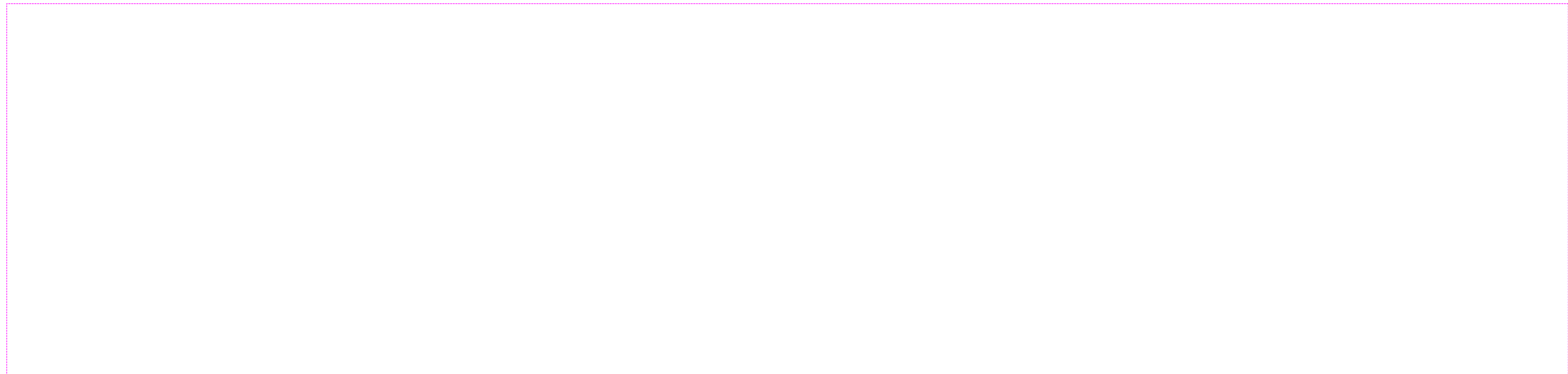


Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence, Use to Mask the VMON_PGOOD
PS_PF_BSOK	INPUT	From Pre-filter(BS_OK)

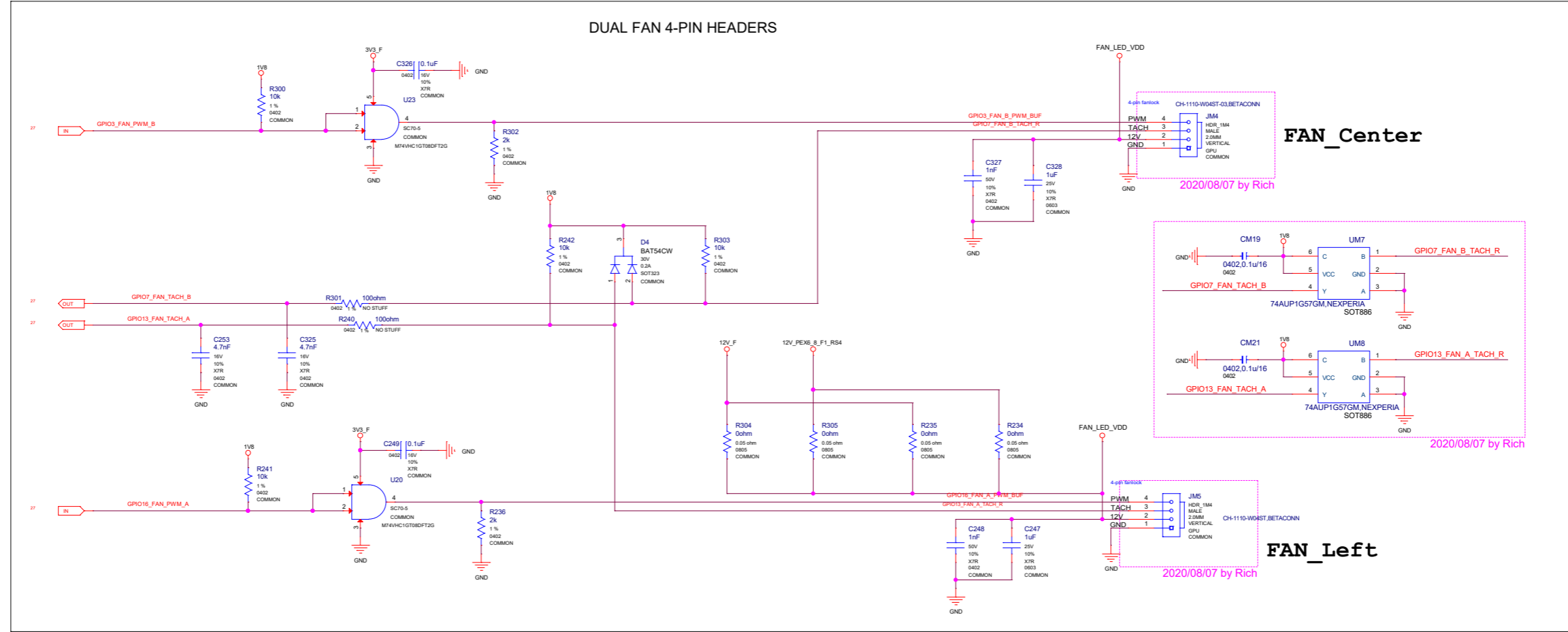
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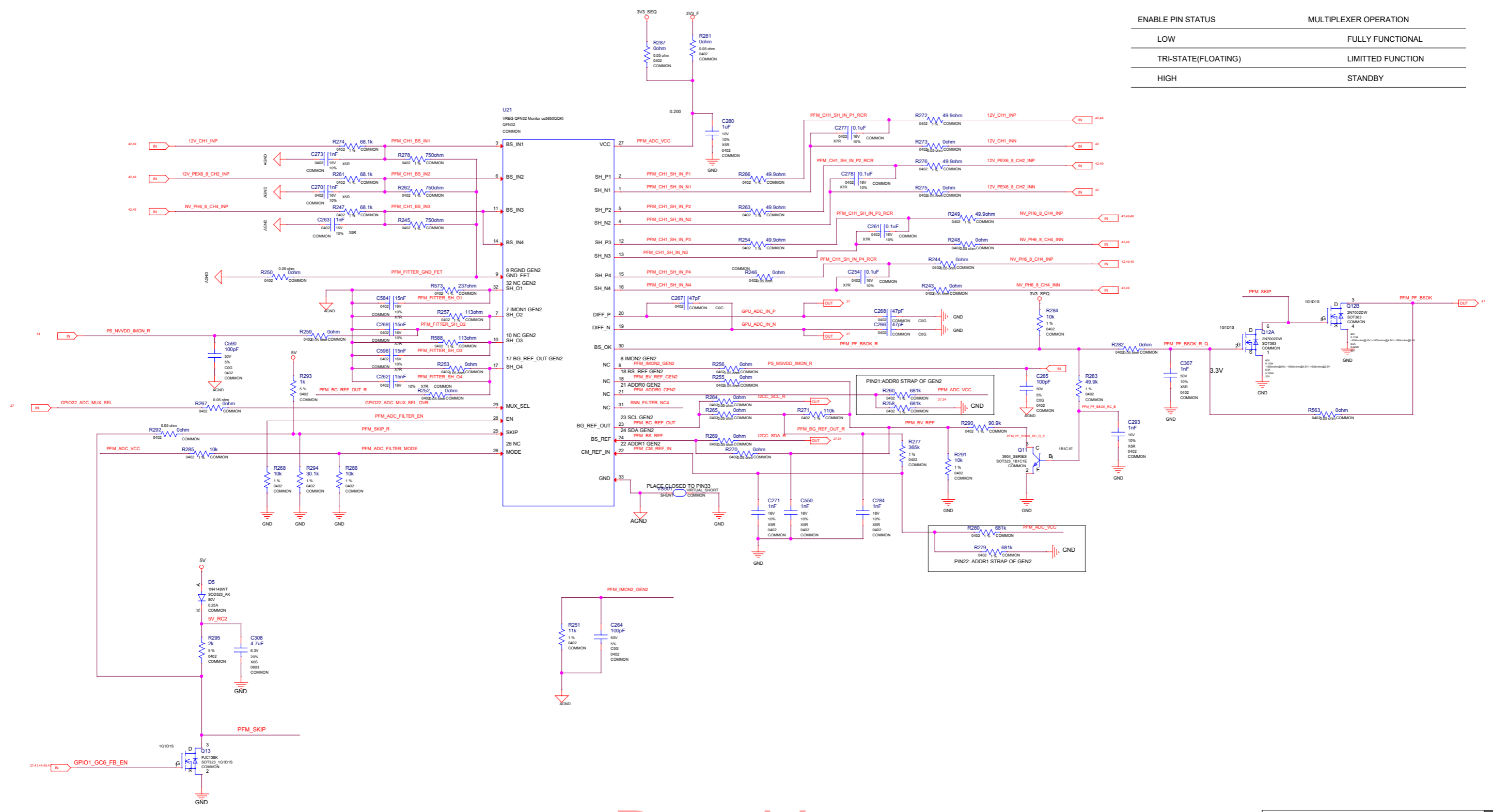
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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

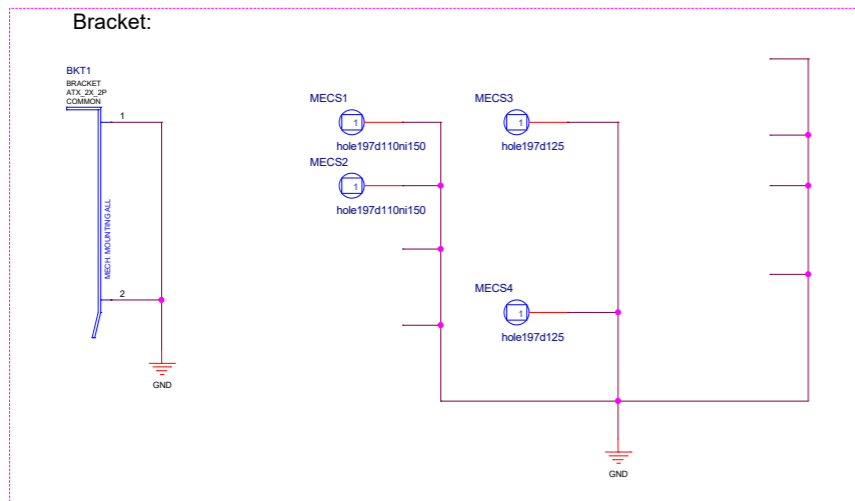
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



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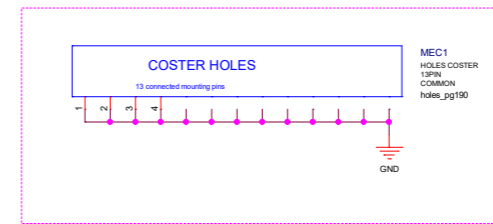
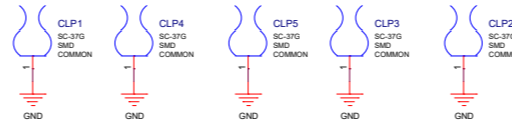
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EMI CLIPS:



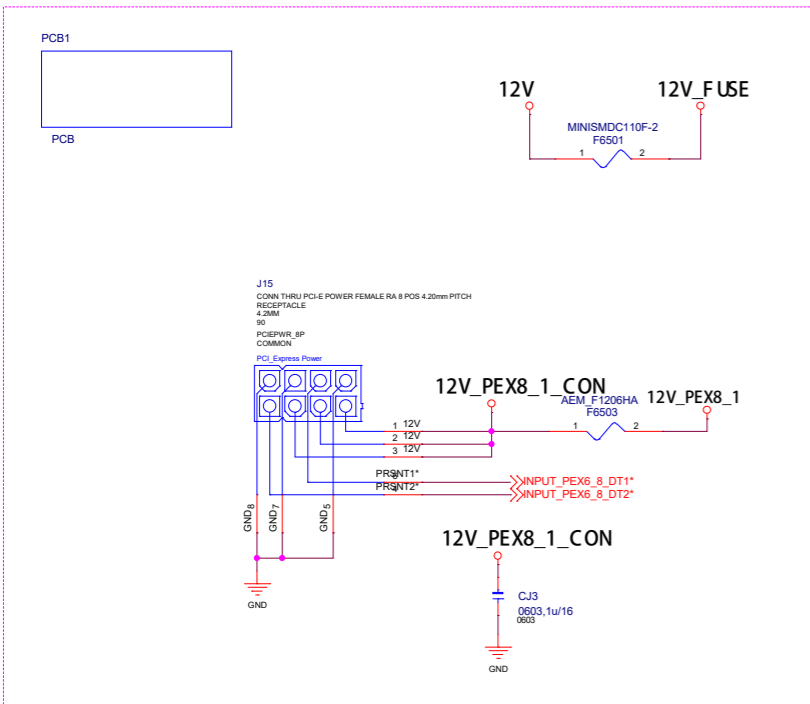
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	MECH

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R999: History

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**R0.0**

- Page.27:**
- 1. Remove NV STEREO Parts
  - 2. Remove NV J9 Parts
  - 3. Remove NV U19 Parts

- Page.42:**
- 1. Move J15 to Page.R009 and change netname to 12V\_PEX8\_1
  - 2. Change 12V netname to 12V\_FUSE
  - 3. Remove J8

- Page.48:**
- 1. Remove NV LED Parts
  - 2. Change Fan connector J10 => JM5, J11 => JM6
  - 3. Add filter IC UM7, UM8

- Page.50:**
- 1. Replace NV Bracket to EVGA
  - 2. Modify MEC1 Pin number
  - 3. Add hole

- Page.R009:**
- 1. Add fuse F6503 on PEX\_8Pin
  - 2. Add fuse F6501 on 12V

2020/08/21

- Page.32:**
- 1. Remove L34 / L35 / L49
  - 2. Change L50 footprint to SMD\_13X8

- Page.33:**
- 1. Remove L47 / L51 / L52
  - 2. Change L48 footprint to SMD\_13X8

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