

P75D V10

GP107 128b GDDR5, 75W  
DVI-D + HDMI + DP


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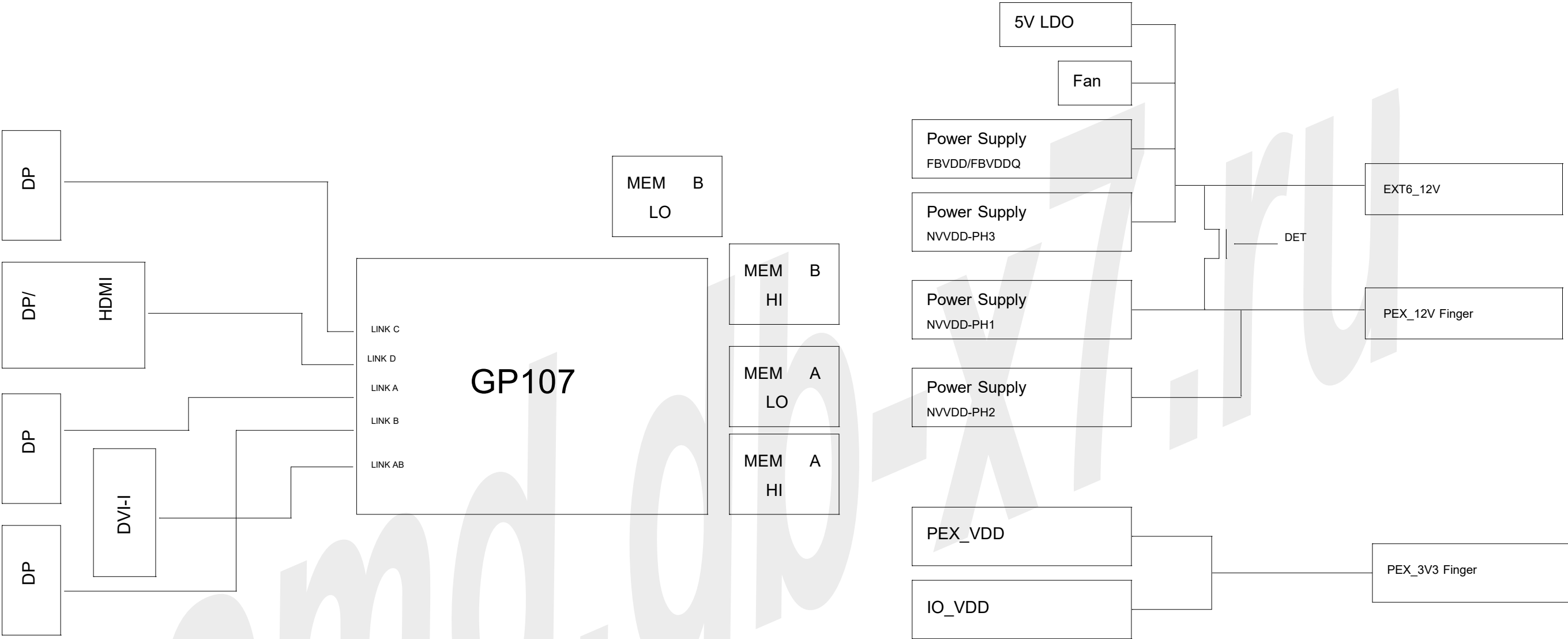
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Block Diagram



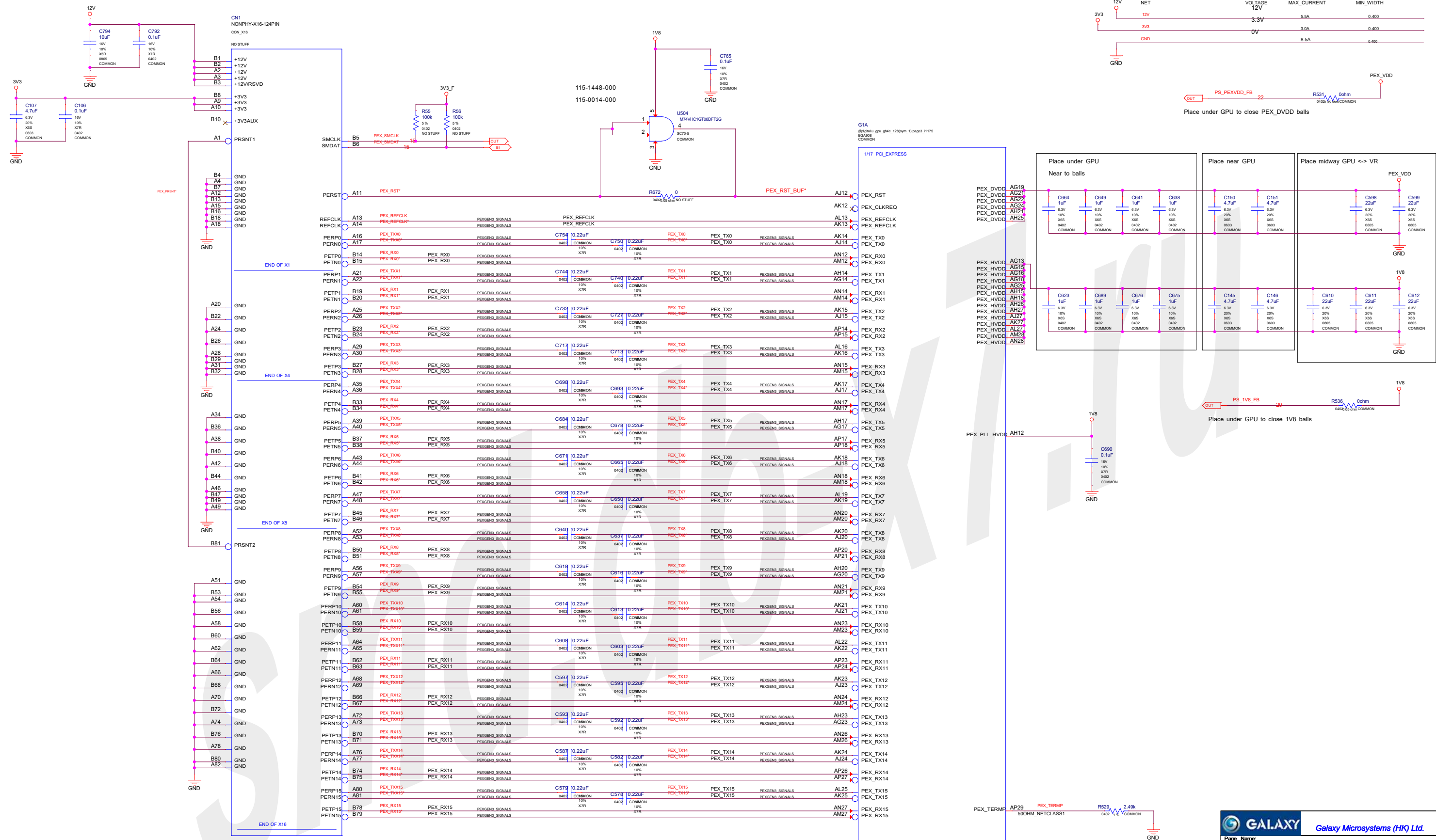
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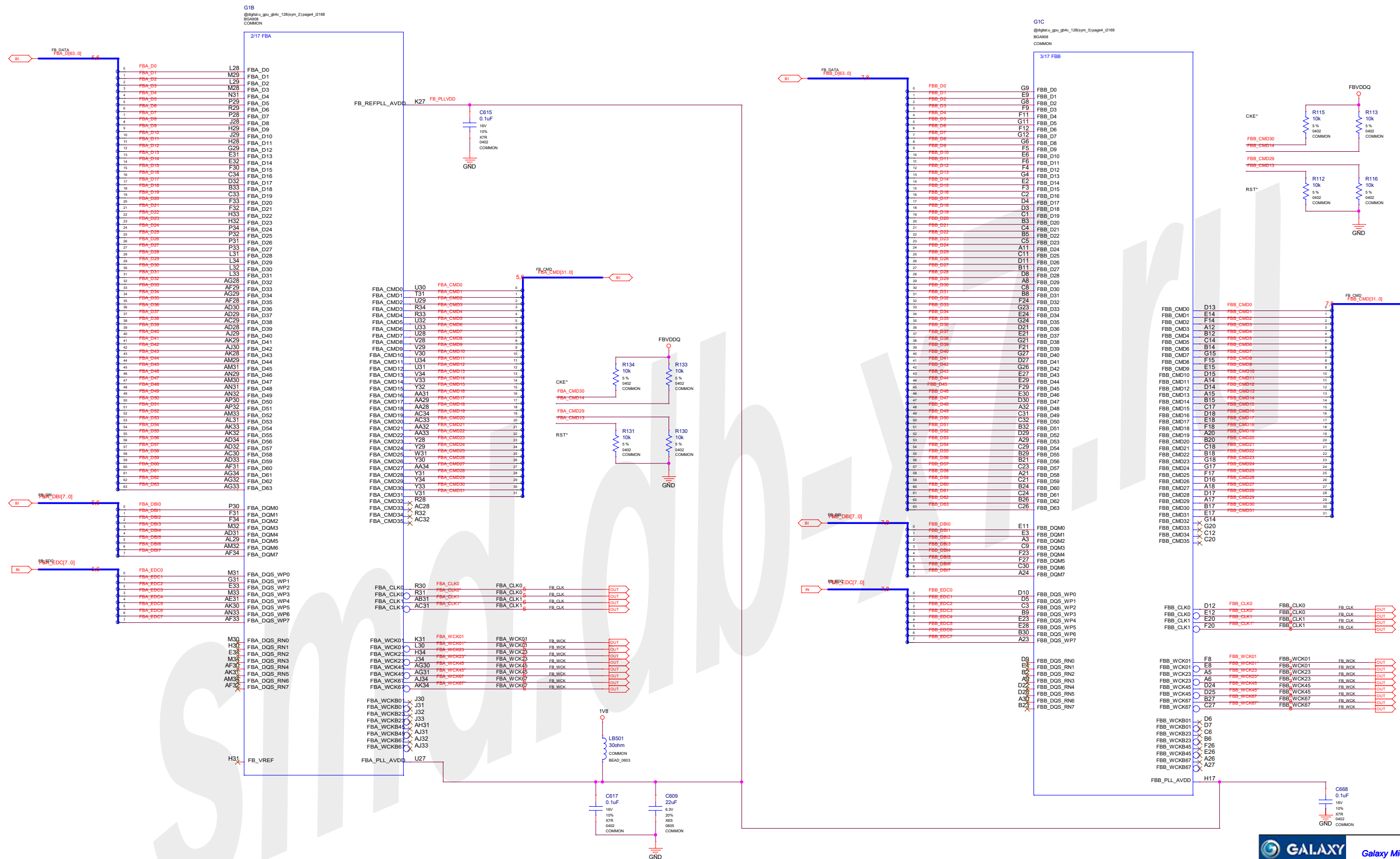
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## PCI Express

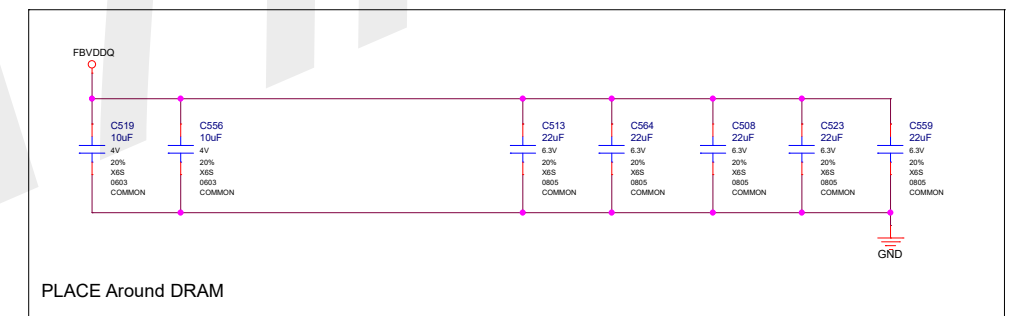
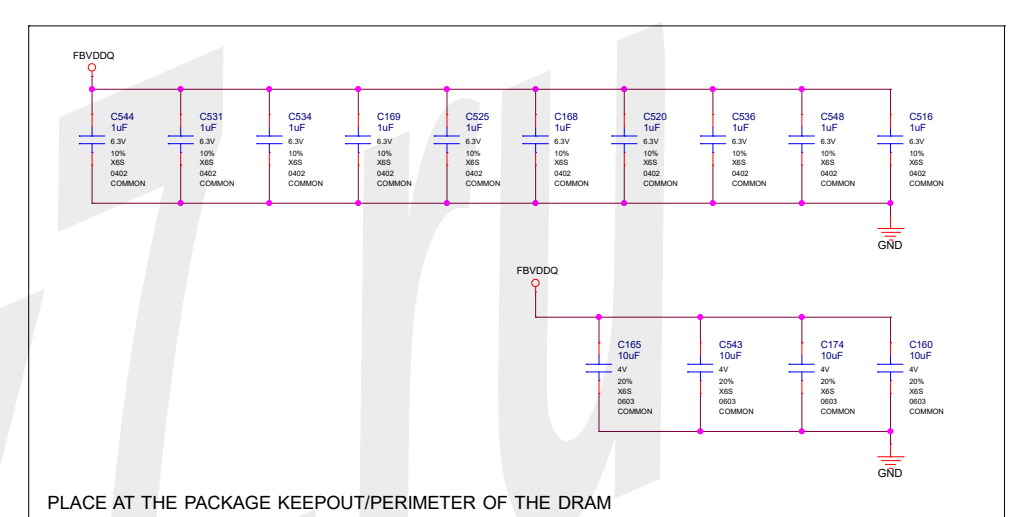
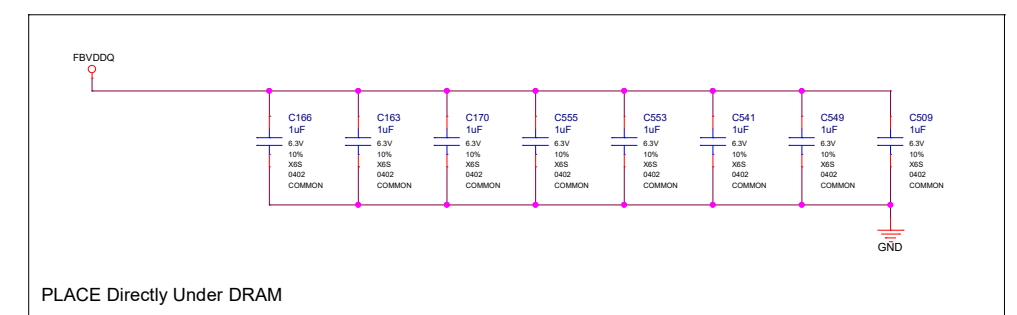
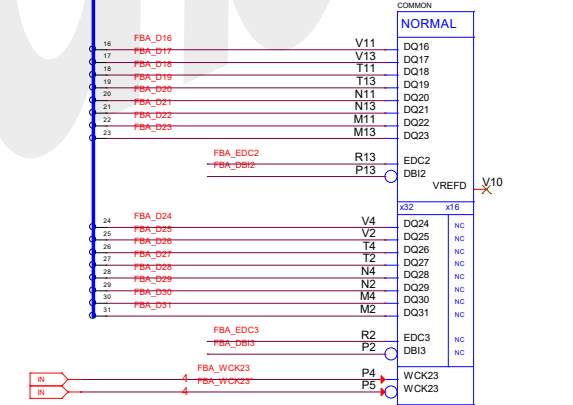
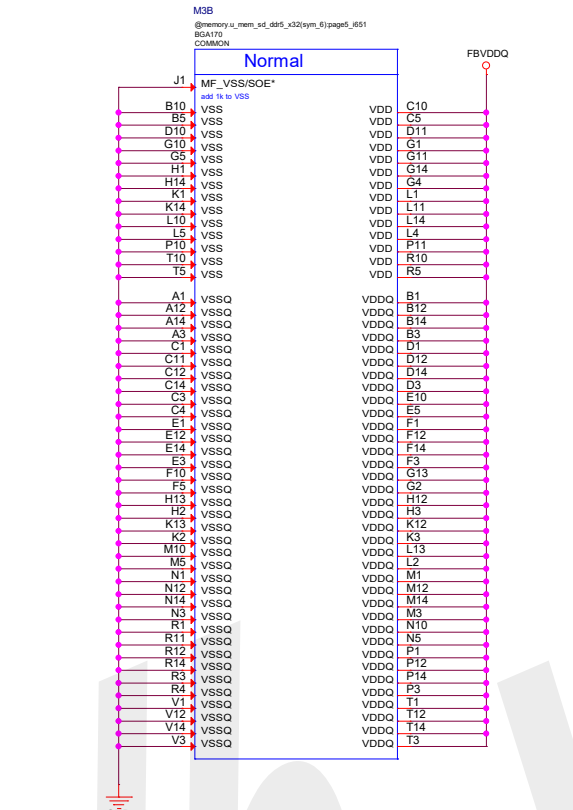
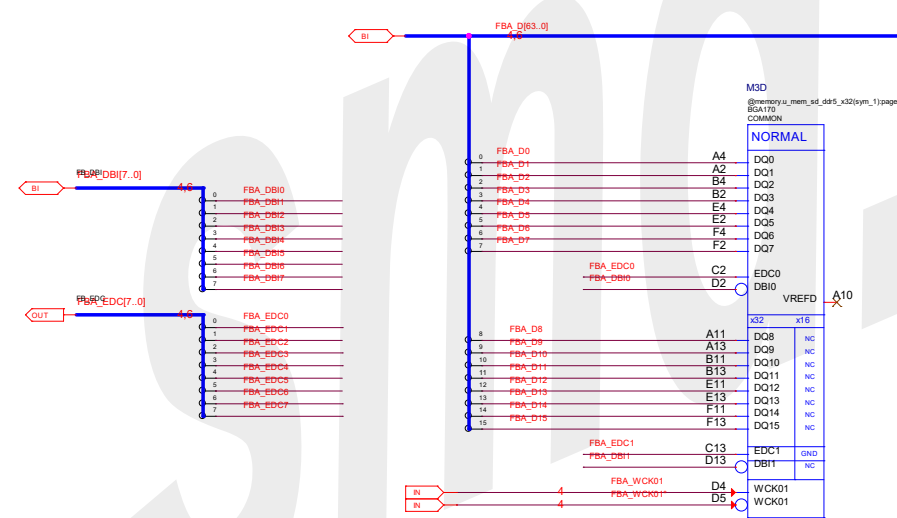
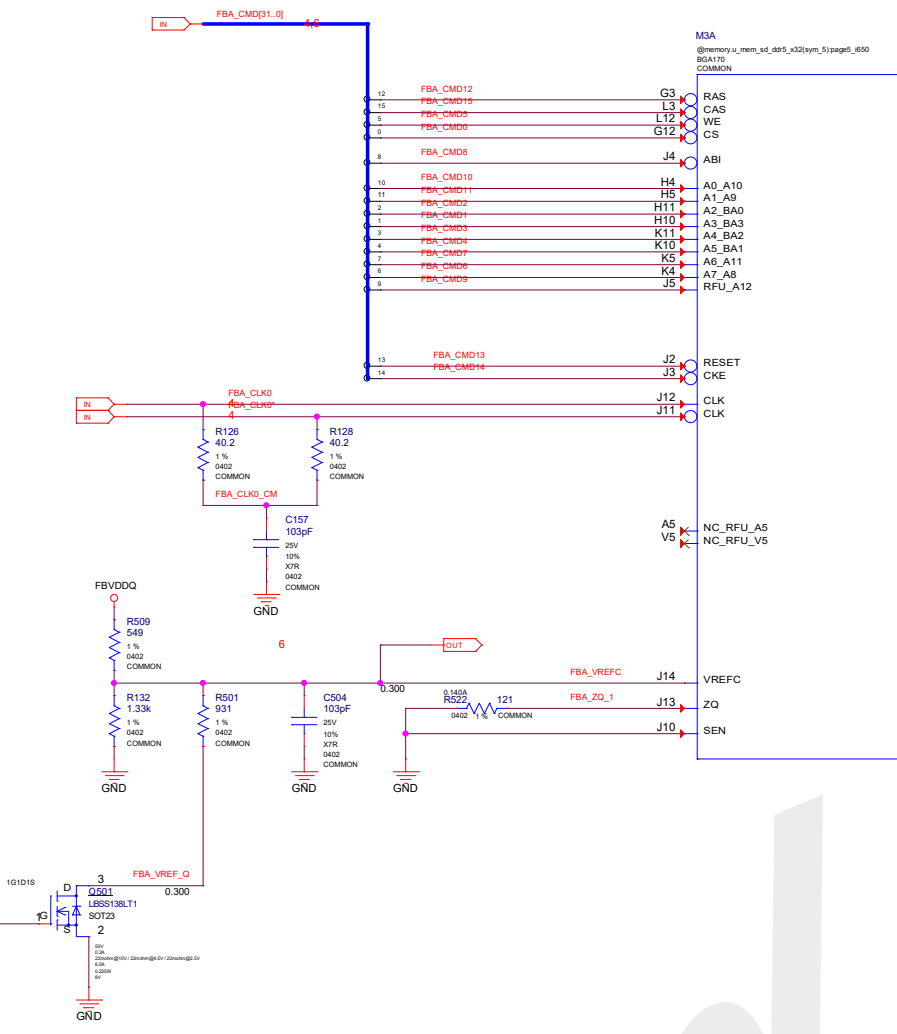


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MEMORY: GPU Partition A/B

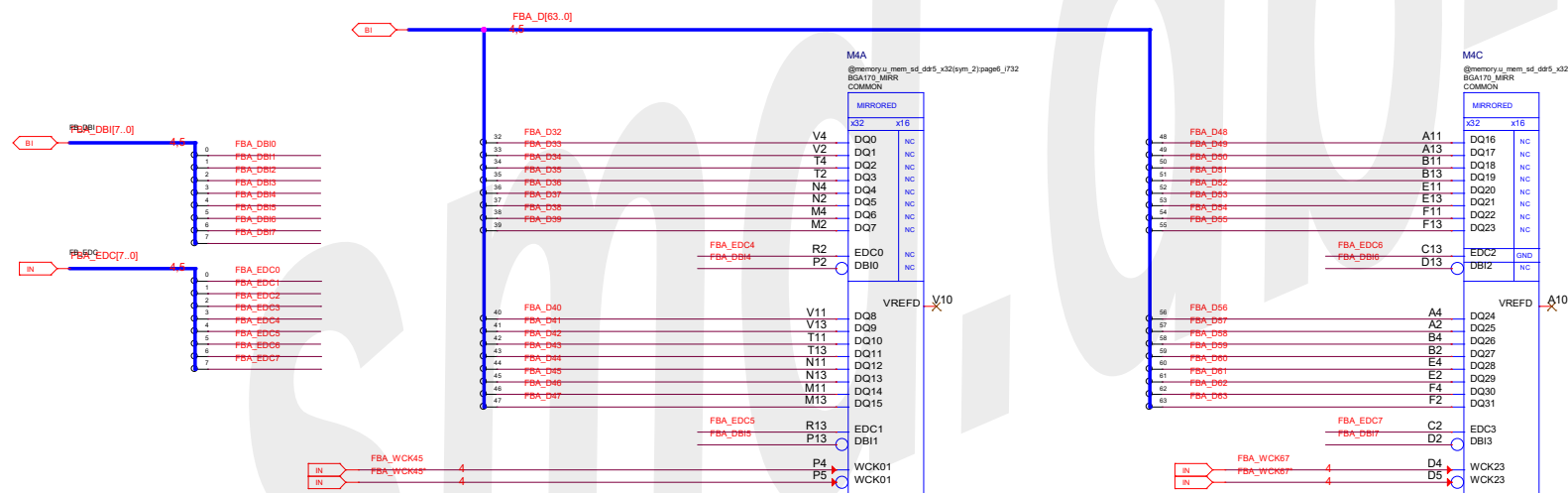
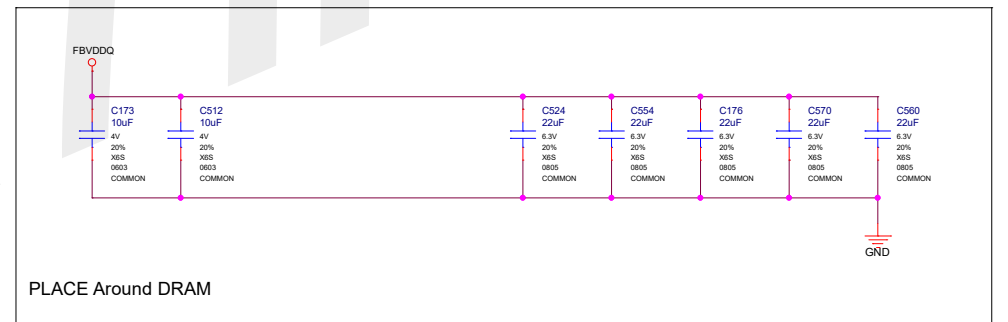
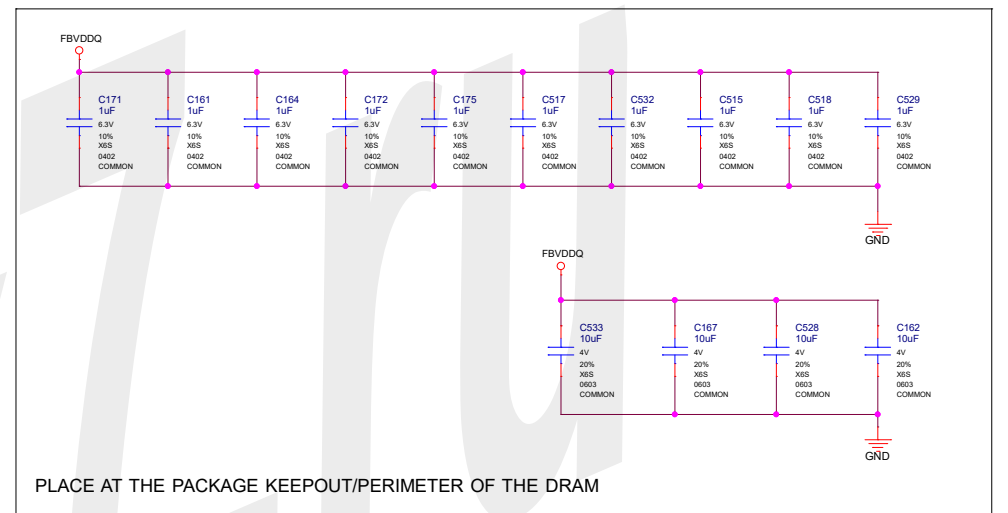
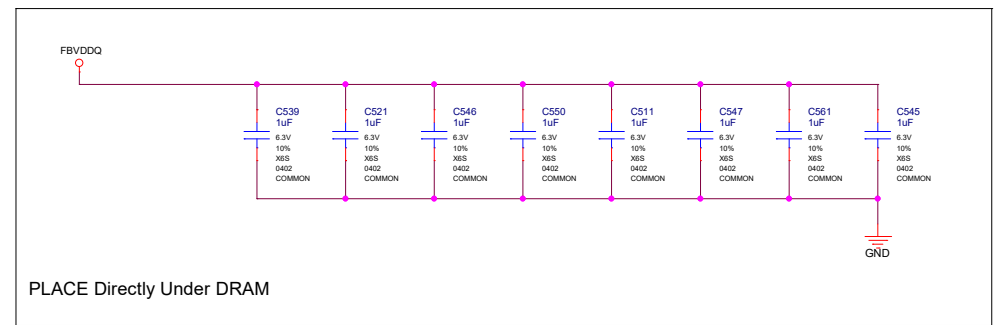
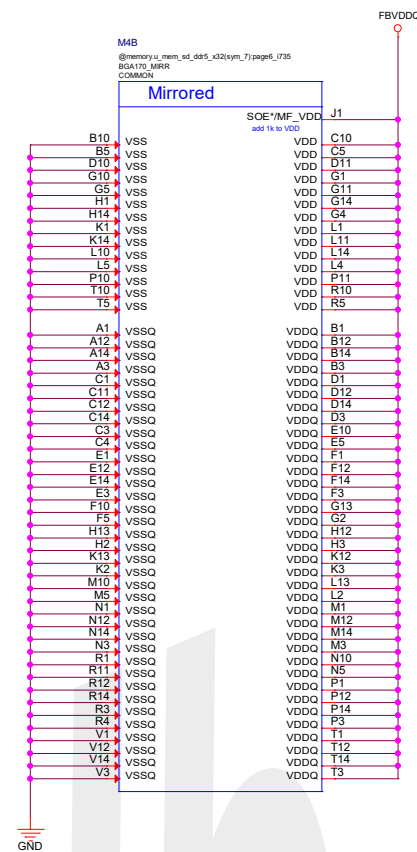
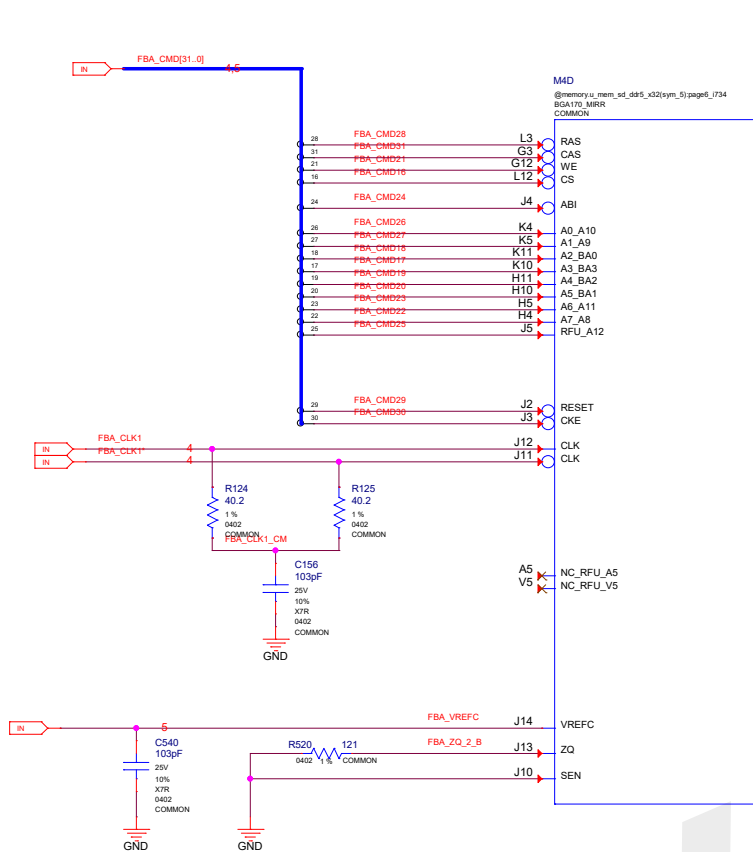


CMD	0..31	32..63
CMD0	CS*	
CMD1	A3, BA3	
CMD2	A2, BA0	
CMD3	A4, BA2	
CMD4	A5, BA1	
CMD5	WE*	
CMD6	A7, A8	
CMD7	A6, A11	
CMD8	ABI*	
CMD9	A12, RFU	
CMD10	A0, A0	
CMD11	A1, A9	
CMD12	RA5*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3, BA3
CMD18		A2, BA0
CMD19		A4, BA2
CMD20		A5, BA1
CMD21		WE*
CMD22		A7, A8
CMD23		A6, A11
CMD24		ABI*
CMD25		A12, RFU
CMD26		A0, A0
CMD27		A1, A9
CMD28		RA5*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



MEMORY: FBA Partition 63..32

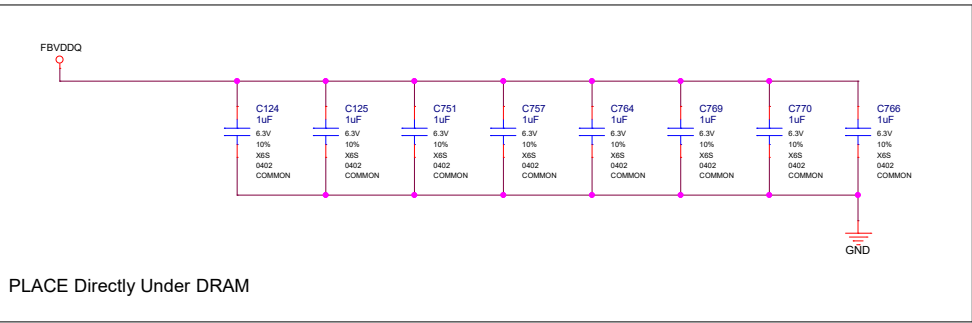
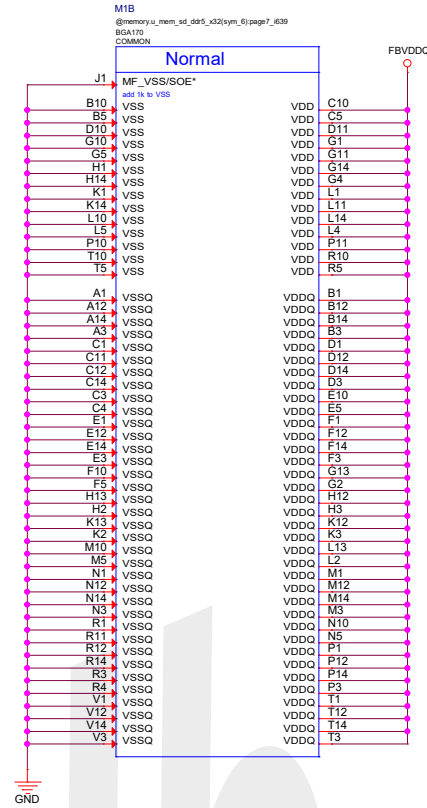
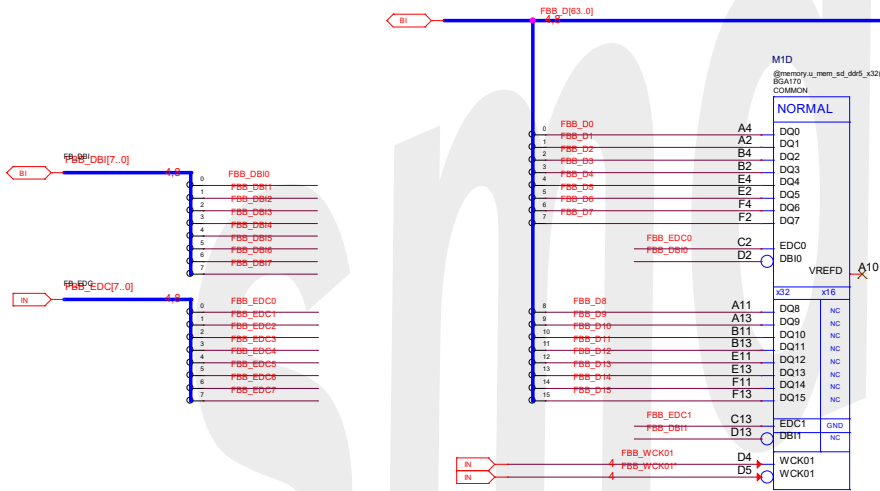
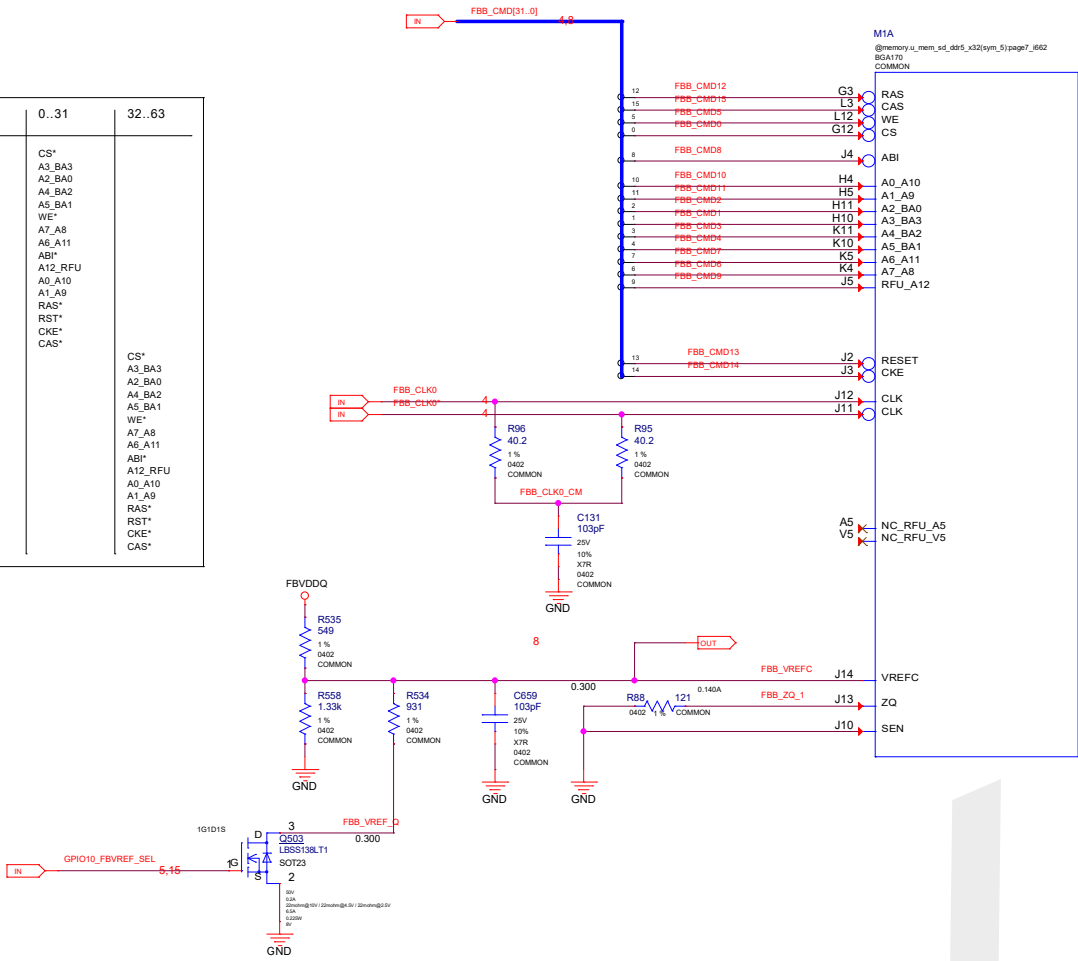
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CMD1	A3..BA3	
CMD2	A2..BA0	
CMD3	A4..BA2	
CMD4	A5..BA1	
CMD5	WE*	
CMD6	A7..A8	
CMD7	A6..A11	
CMD8	AB1*	
CMD9	A12..RFU	
CMD10	A0..A10	
CMD11	A1..A8	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3..BA3
CMD18		A2..BA0
CMD19		A4..BA2
CMD20		A5..BA1
CMD21		WE*
CMD22		A7..A8
CMD23		A6..A11
CMD24		AB1*
CMD25		A12..RFU
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CMD27		A1..A8
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



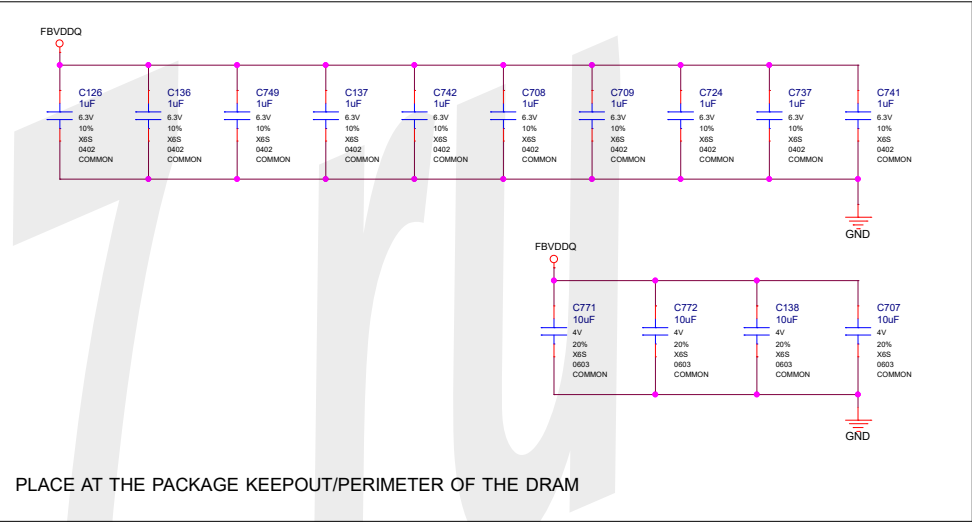


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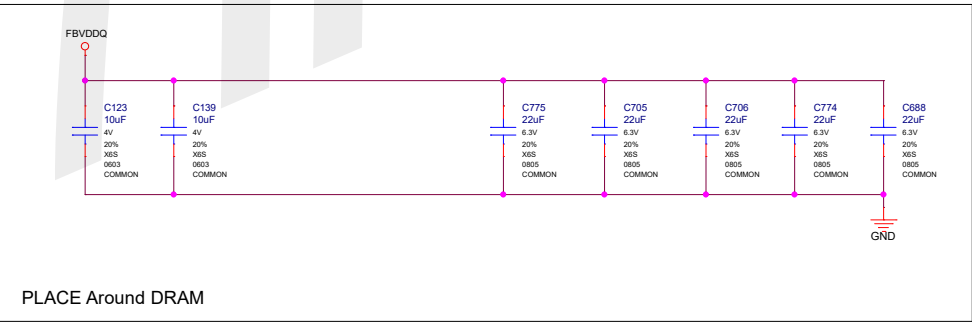
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CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB1*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM

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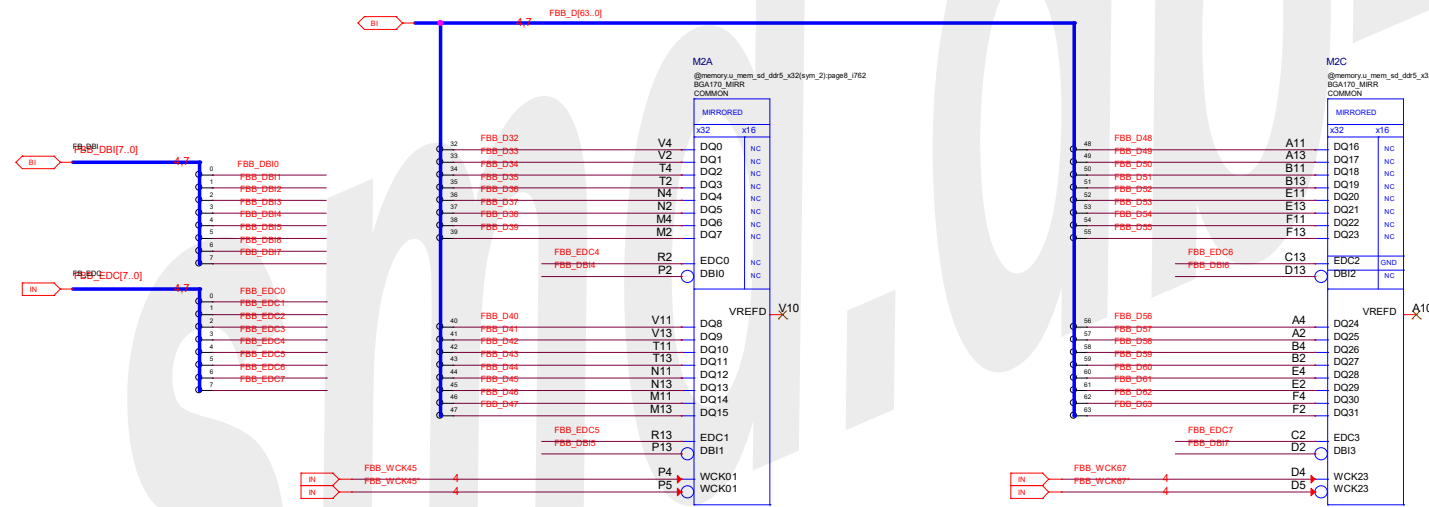
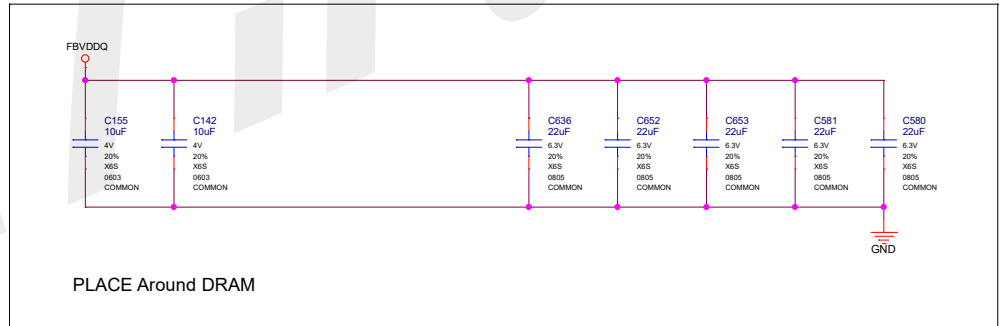
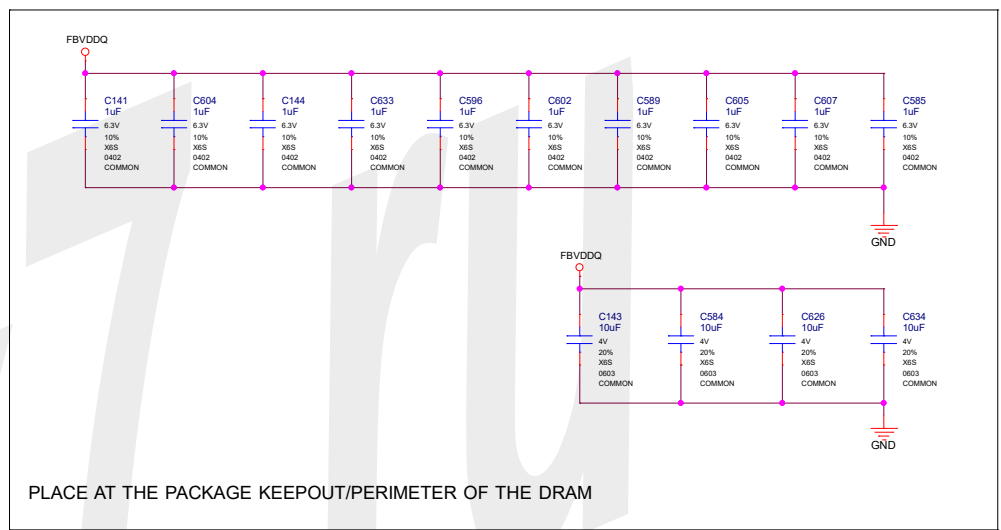
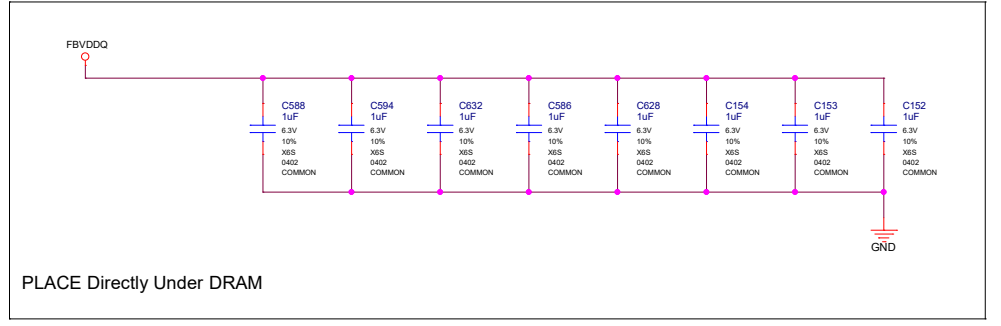
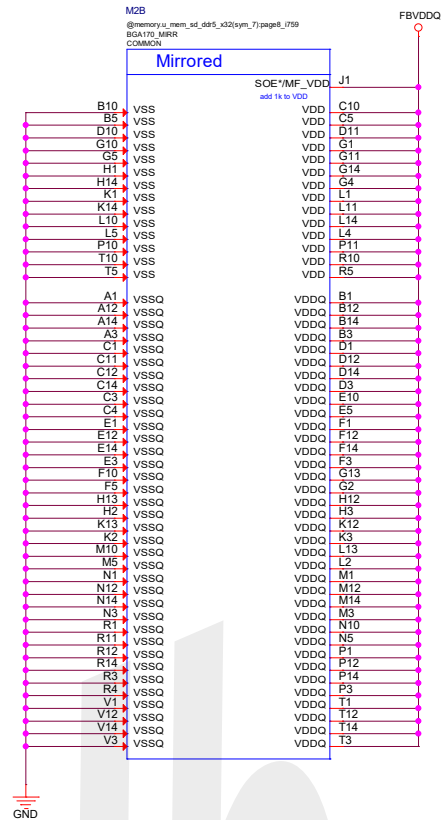
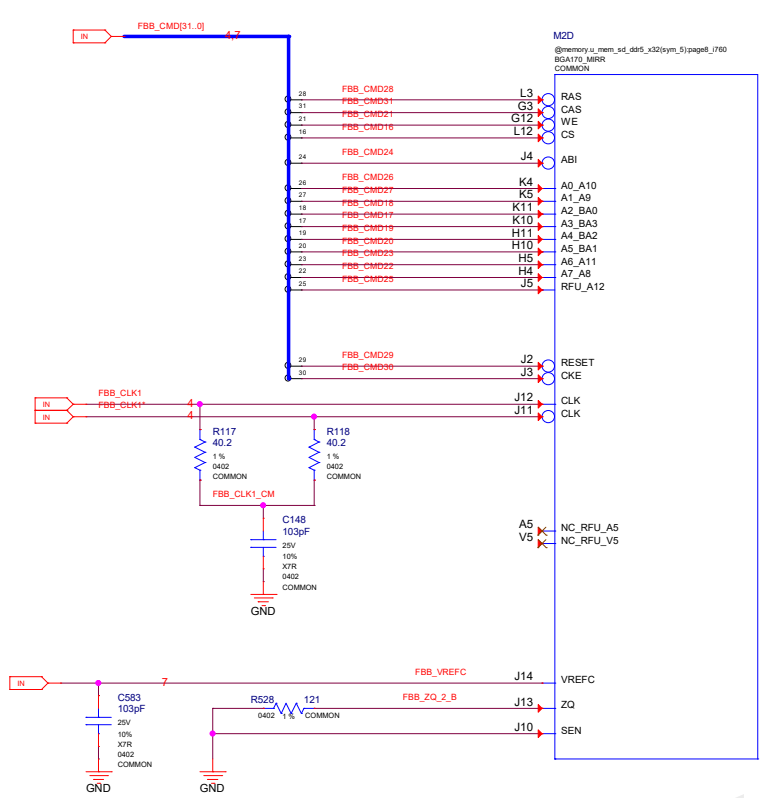
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MEMORY: FBB Partition 63..32

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CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



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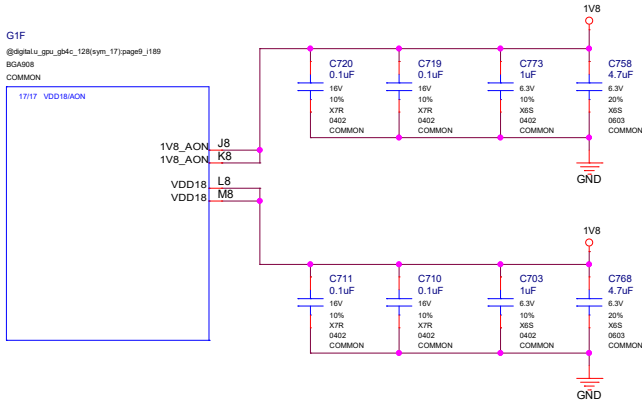
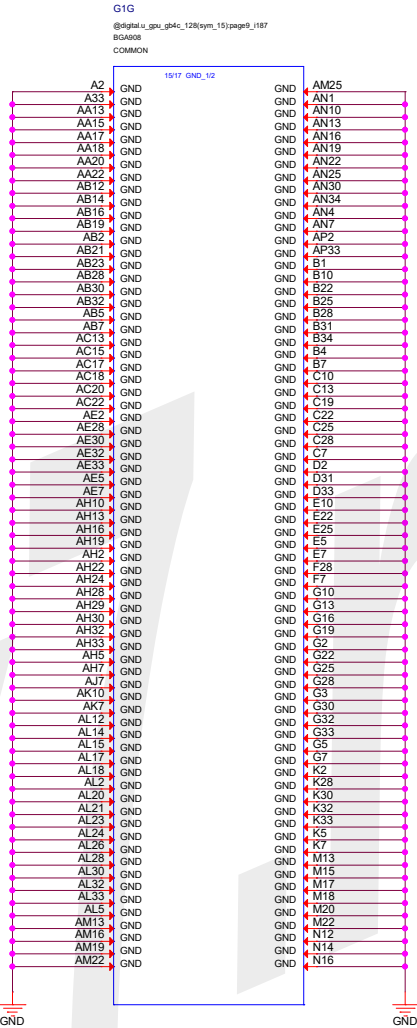
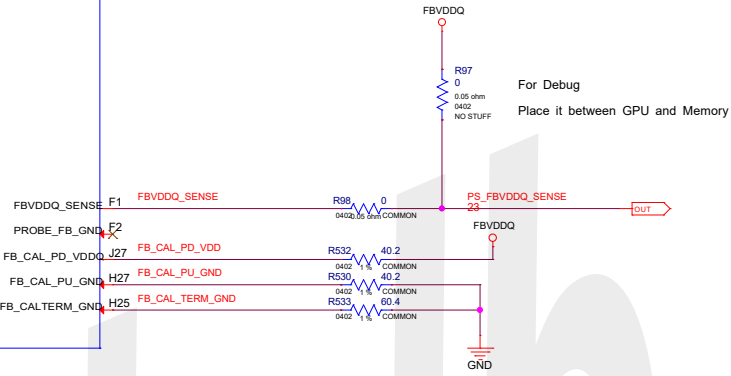
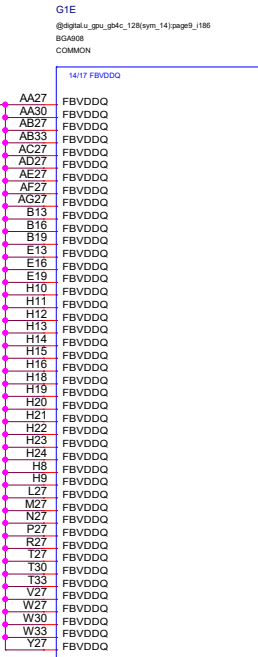
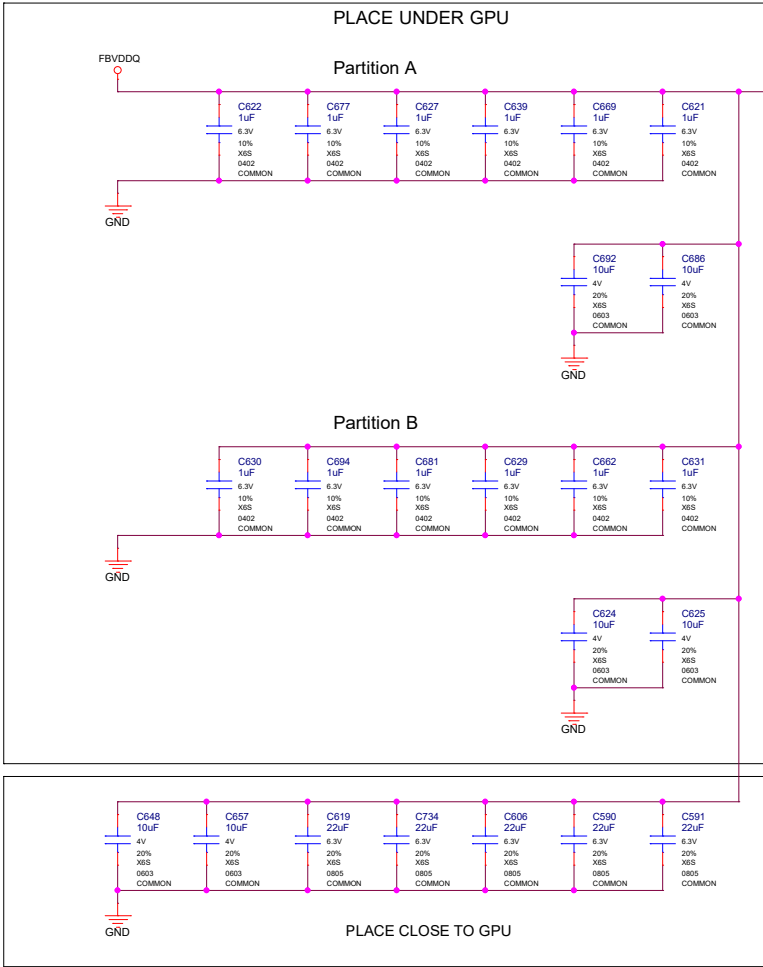
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GPU FBVDDQ & 1V8 Decoupling

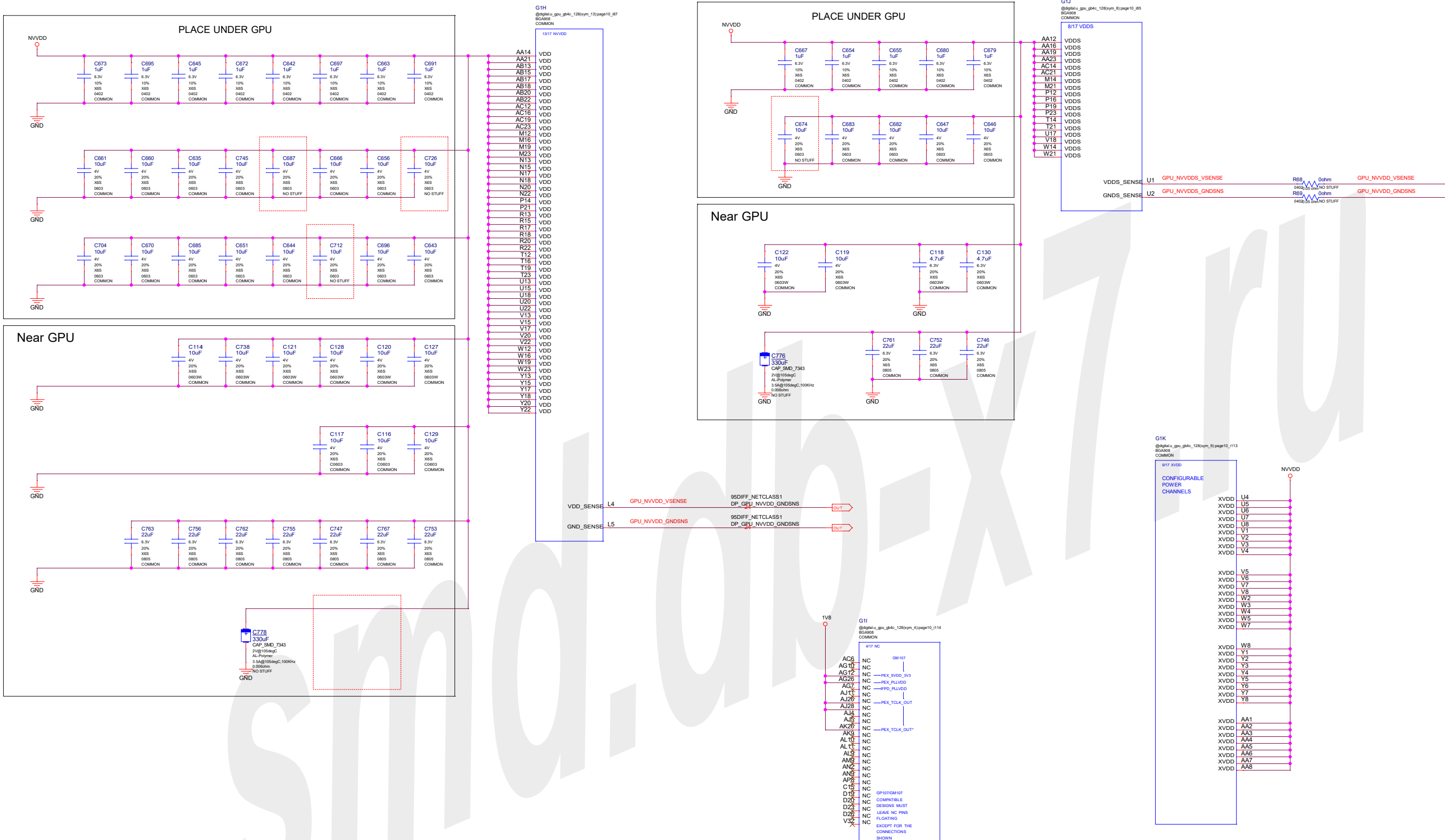


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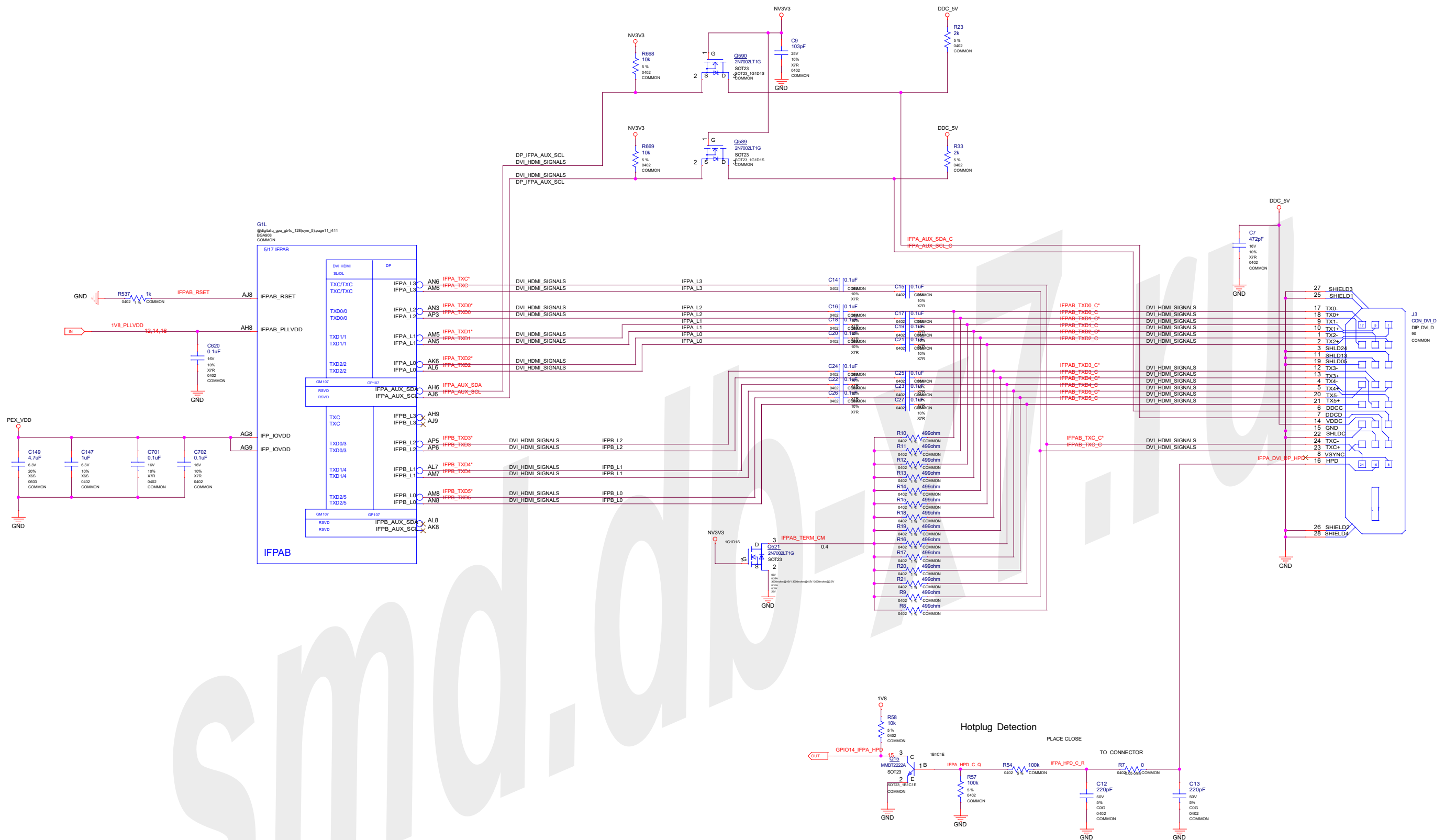
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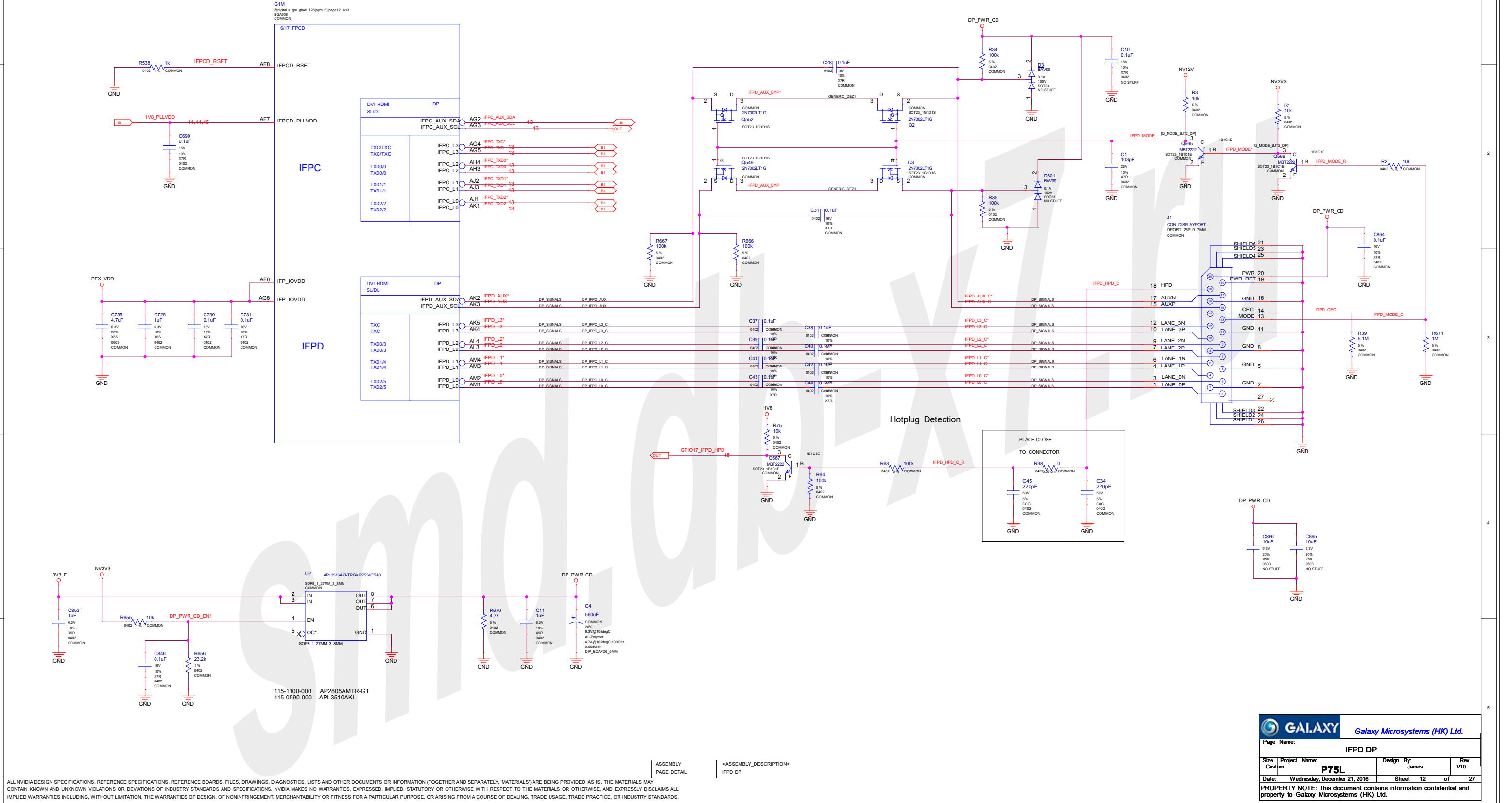
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IFPAB DVI-DL

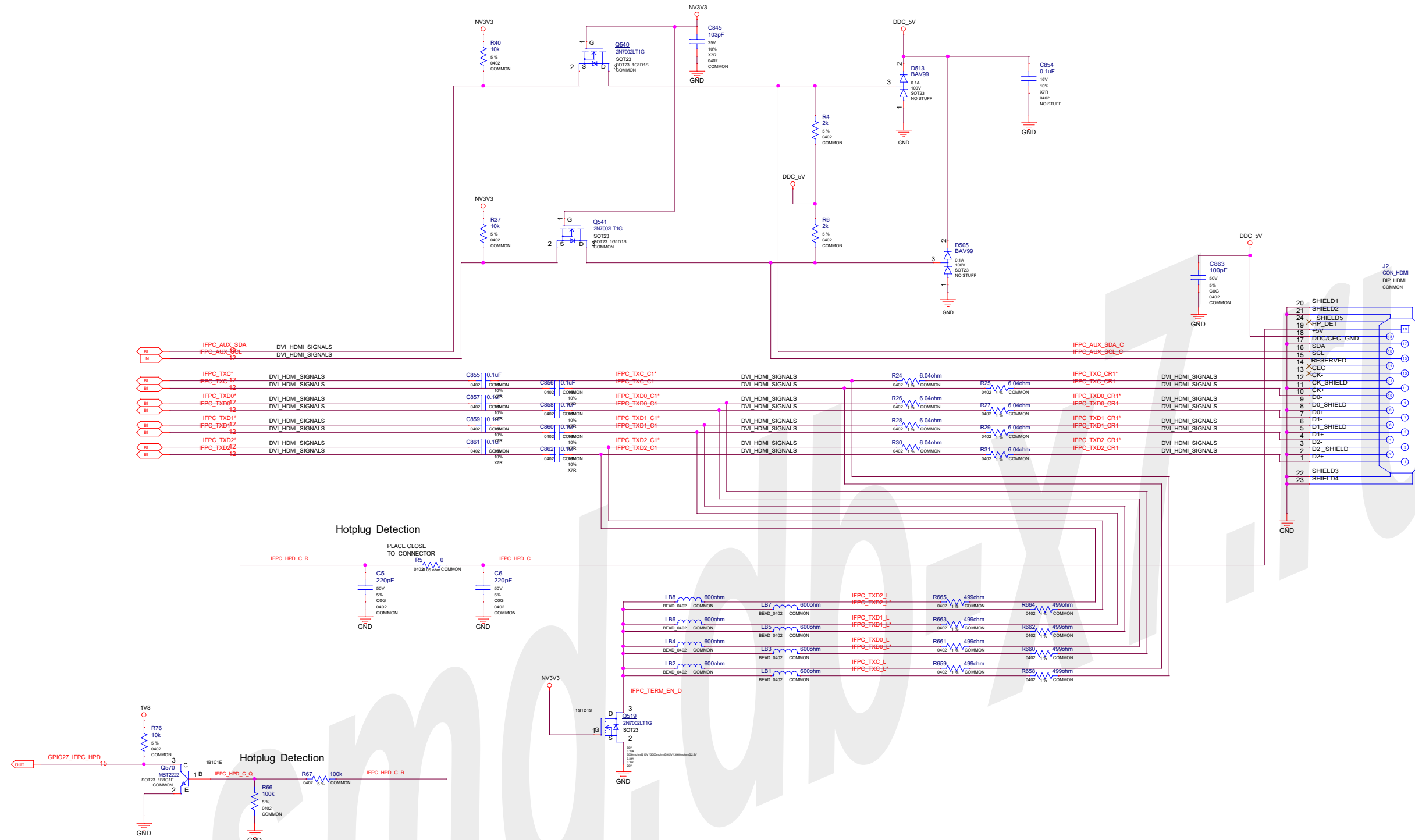


IFPD DP



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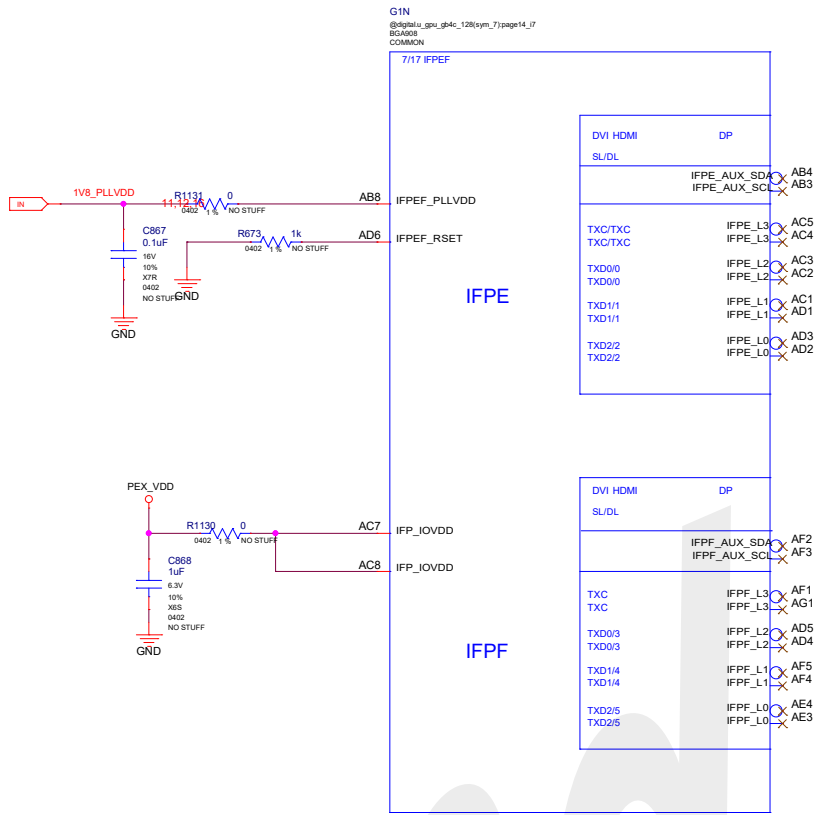
IFPC HDMI



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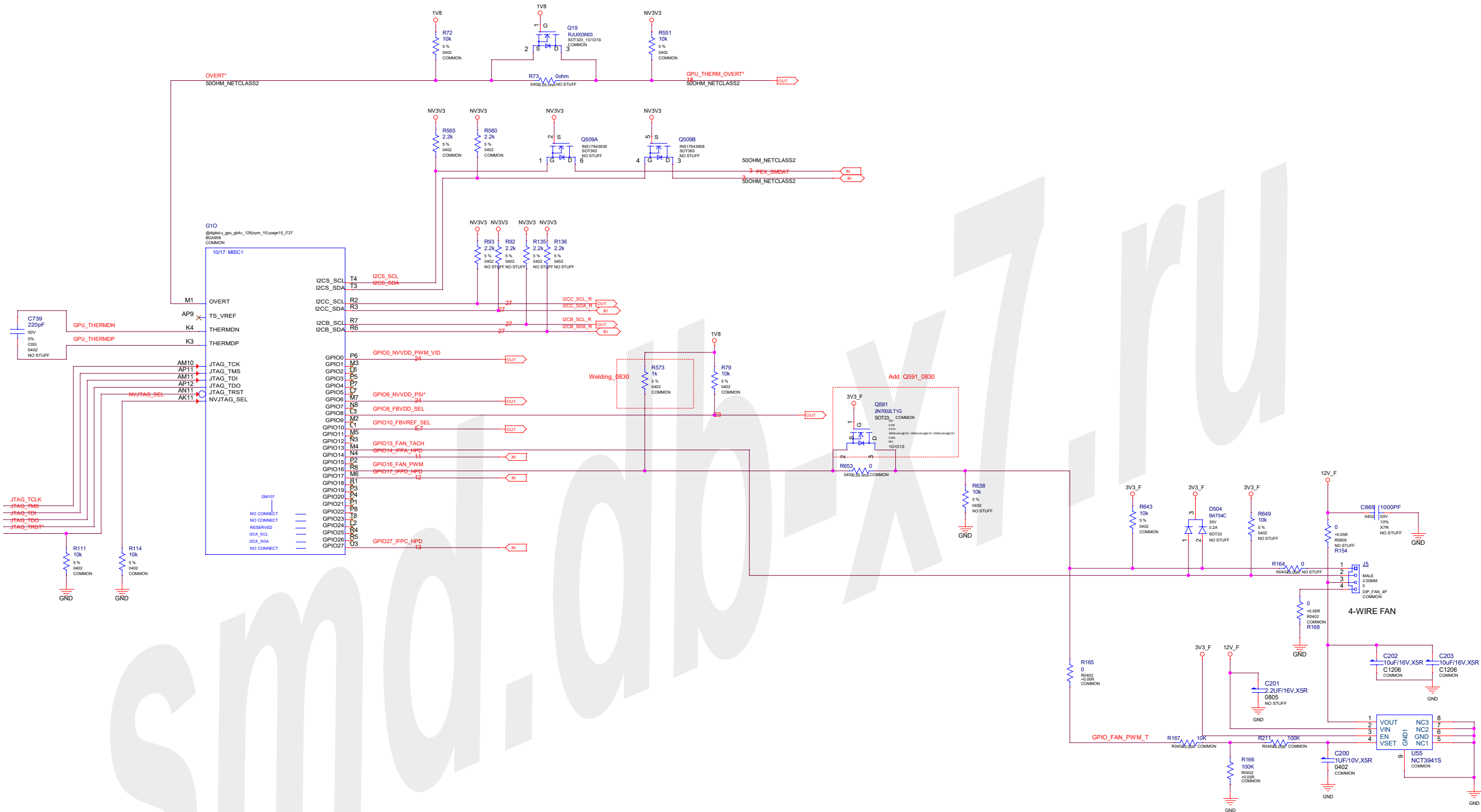
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MISC1: GPIO, Fan, Thermal, JTAG


PADS FOR DEBUGGING



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MISC1: Fan, Thermal, JTAG, GPIO

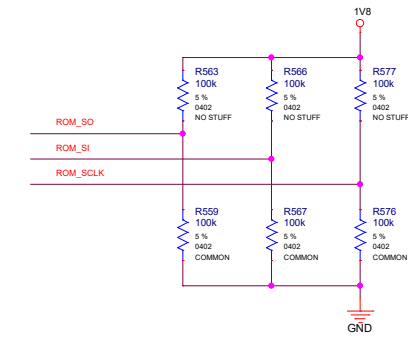
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MISC2: ROM, XTAL, Straps

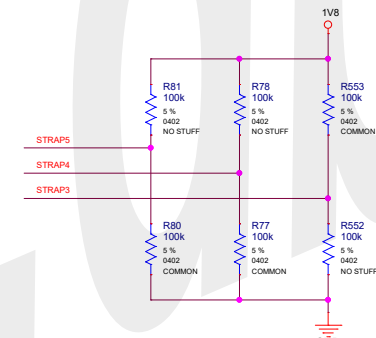
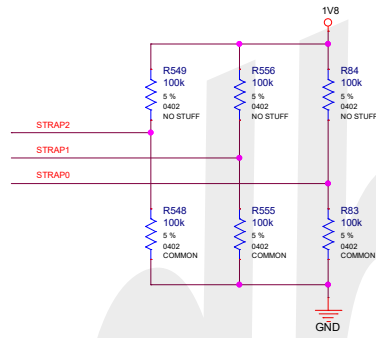
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L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

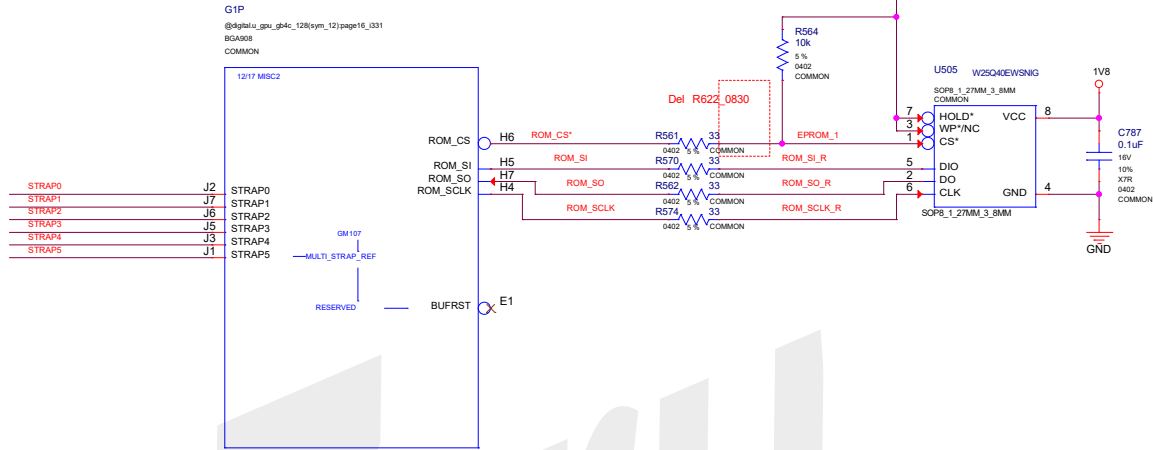


1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGNAL

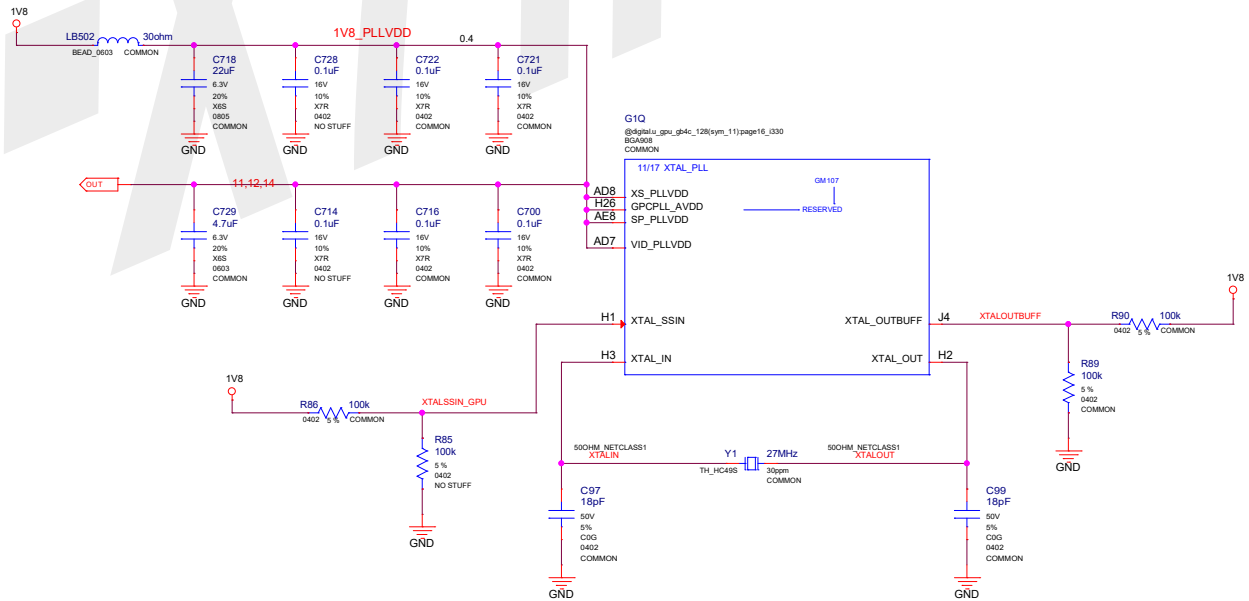
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



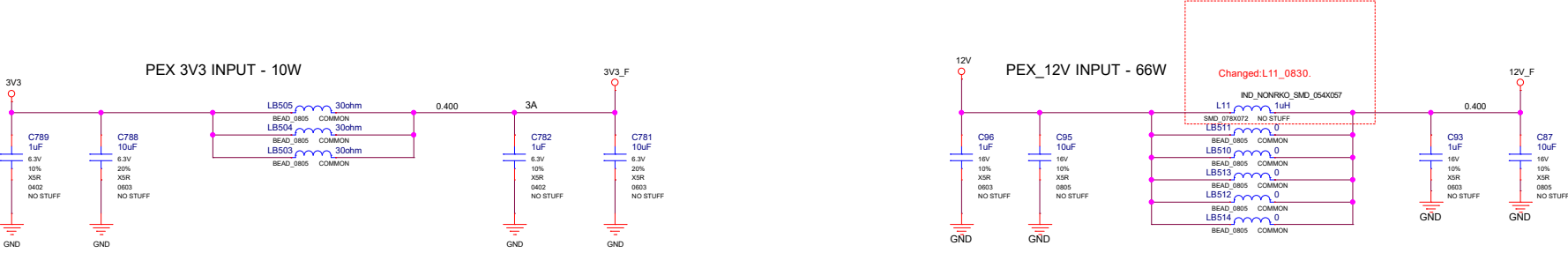
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Page Name: MISC2: ROM, XTAL, Straps

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Power Inputs and Filtering



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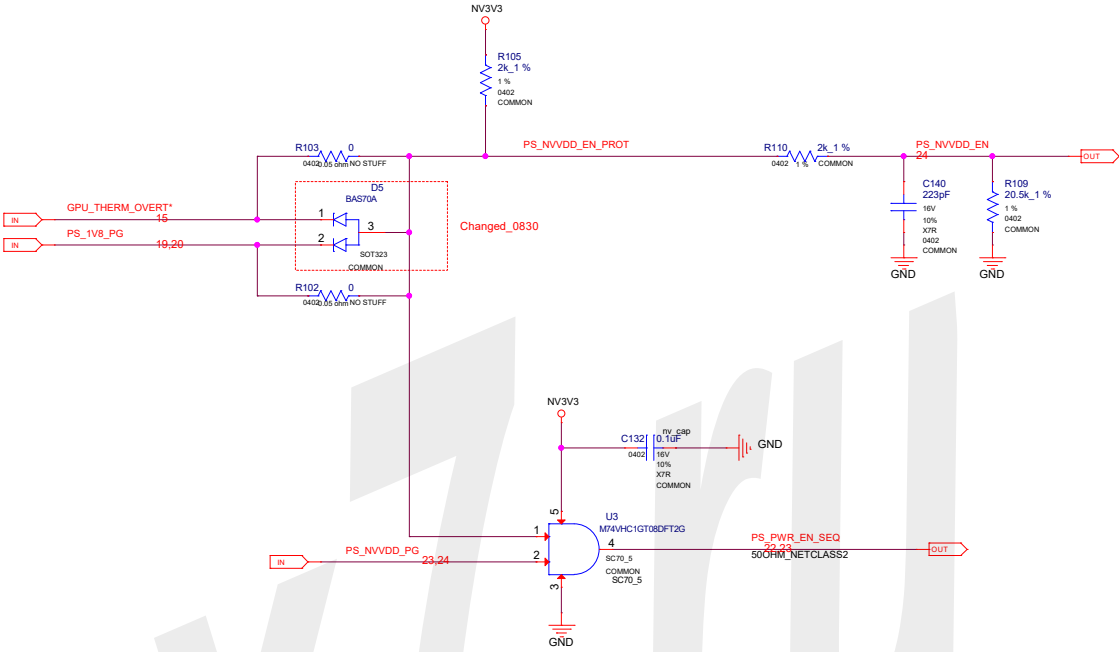
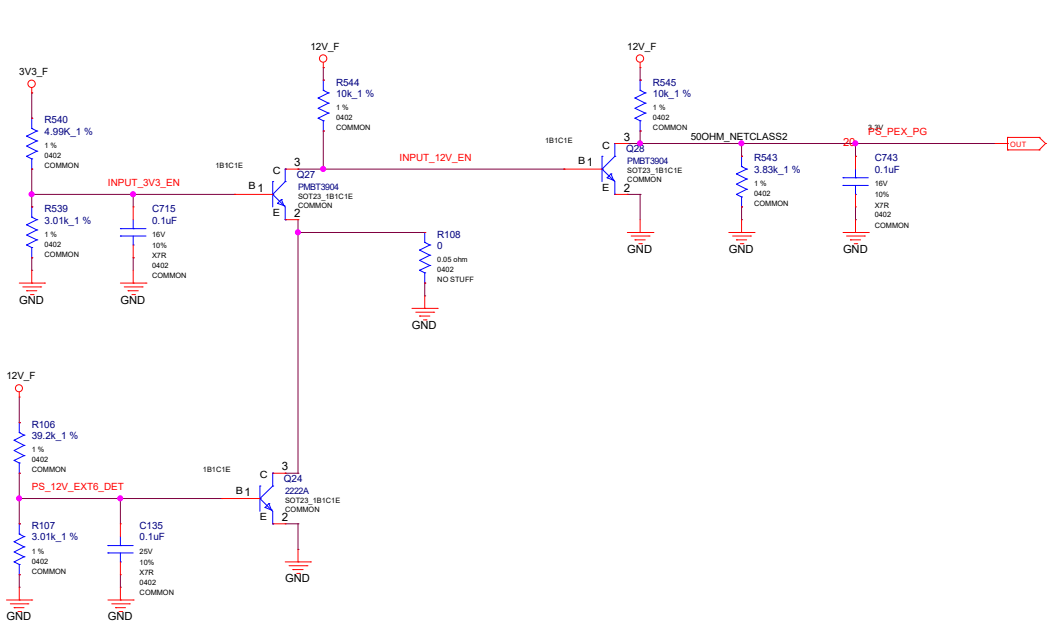
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Page Name: Power Inputs and Filtering

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Power sequence



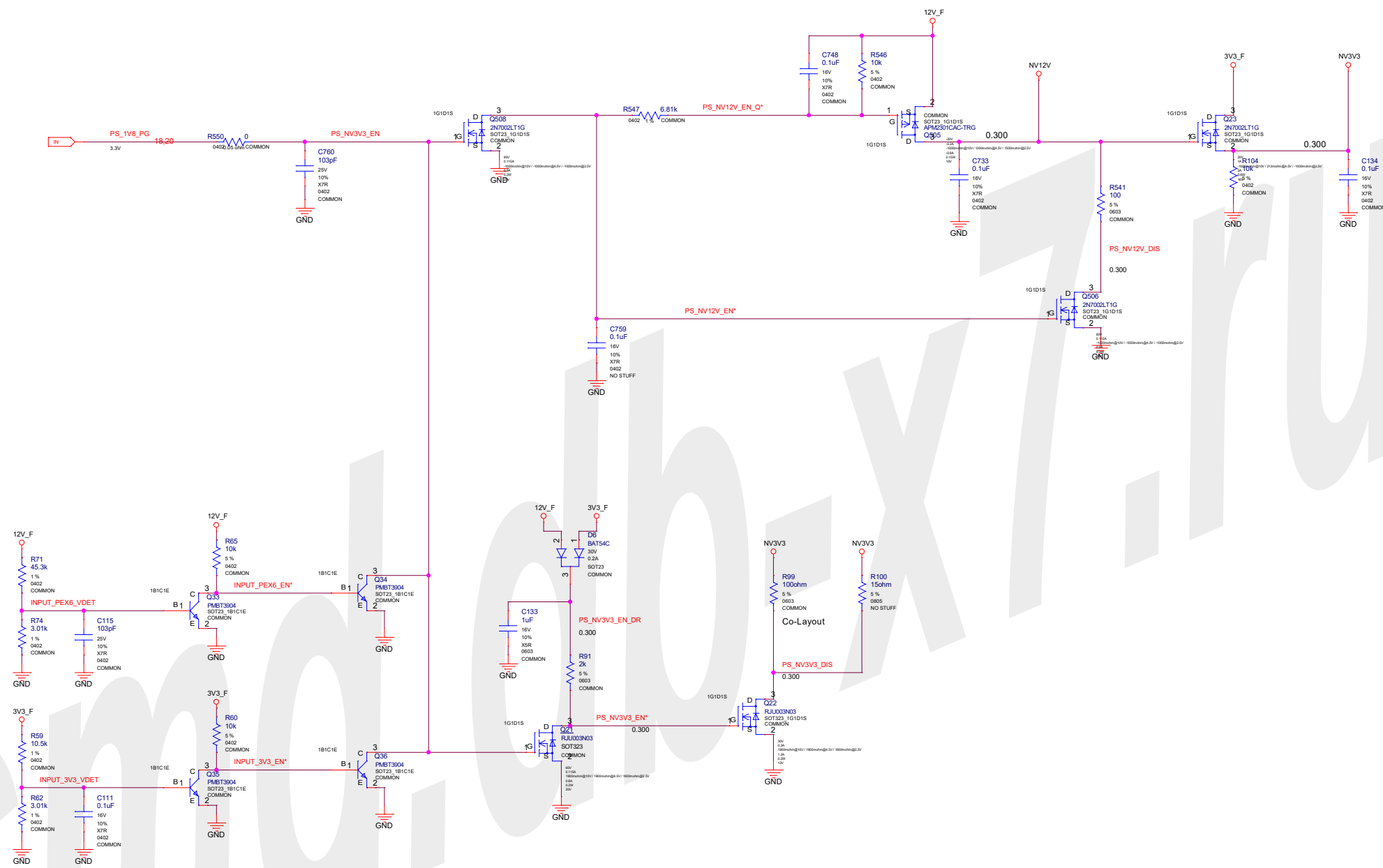
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PAGE DETAIL

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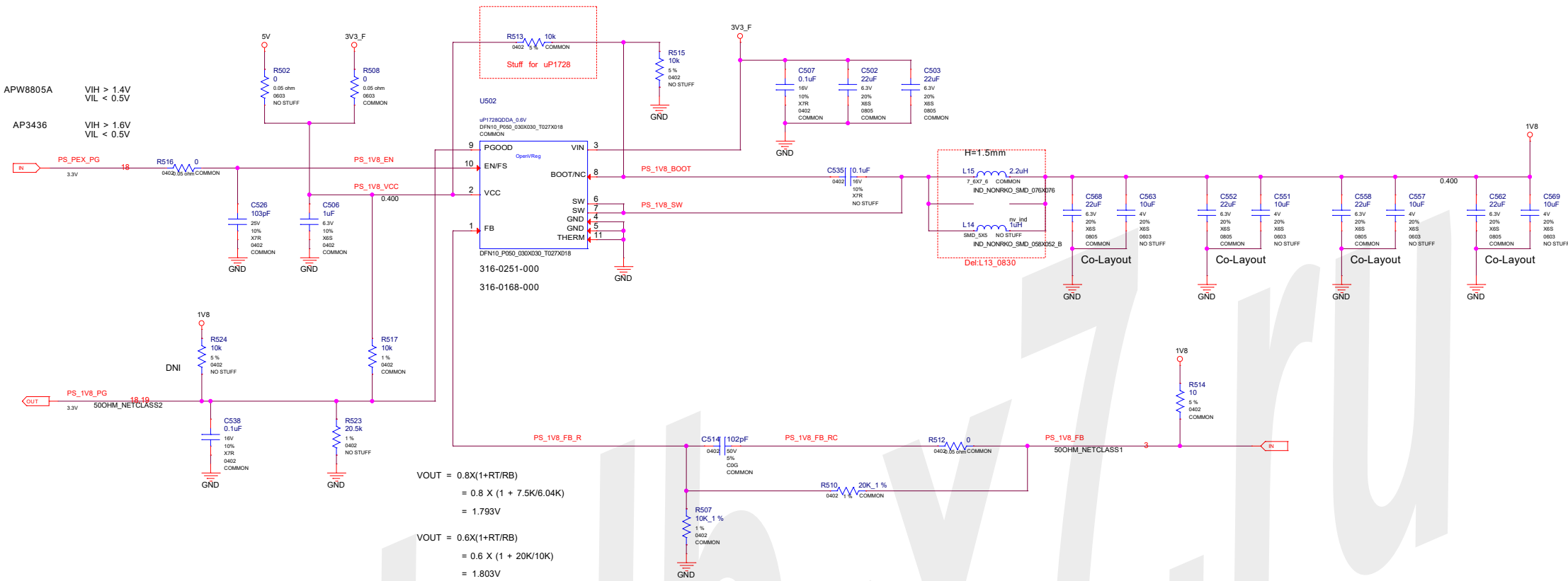
Page Name: Power sequence			
Size: Custom	Project Name: P75L	Design By: James	Rev: V10
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PS: NV3V3 & NV12V



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PAGE DETAIL	PS: NV3V3 & NV12V

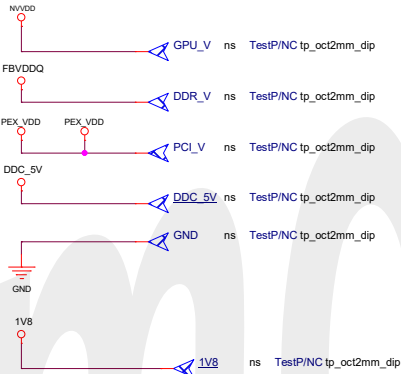
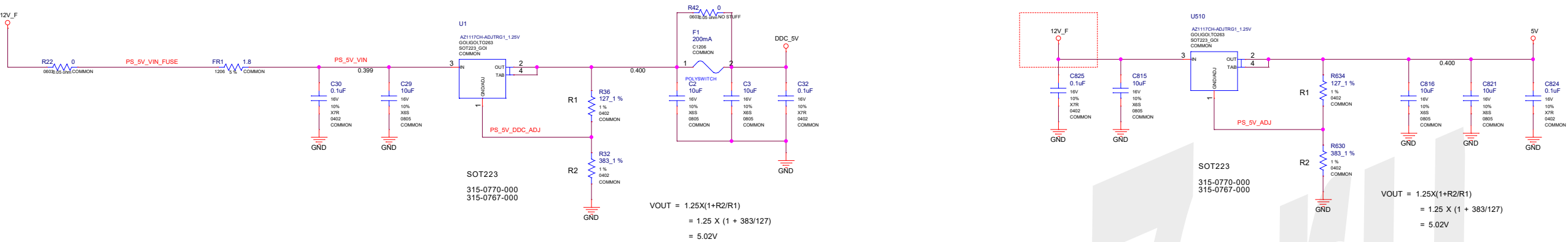


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Page Name: PS I: 1V8			
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PSII:5V



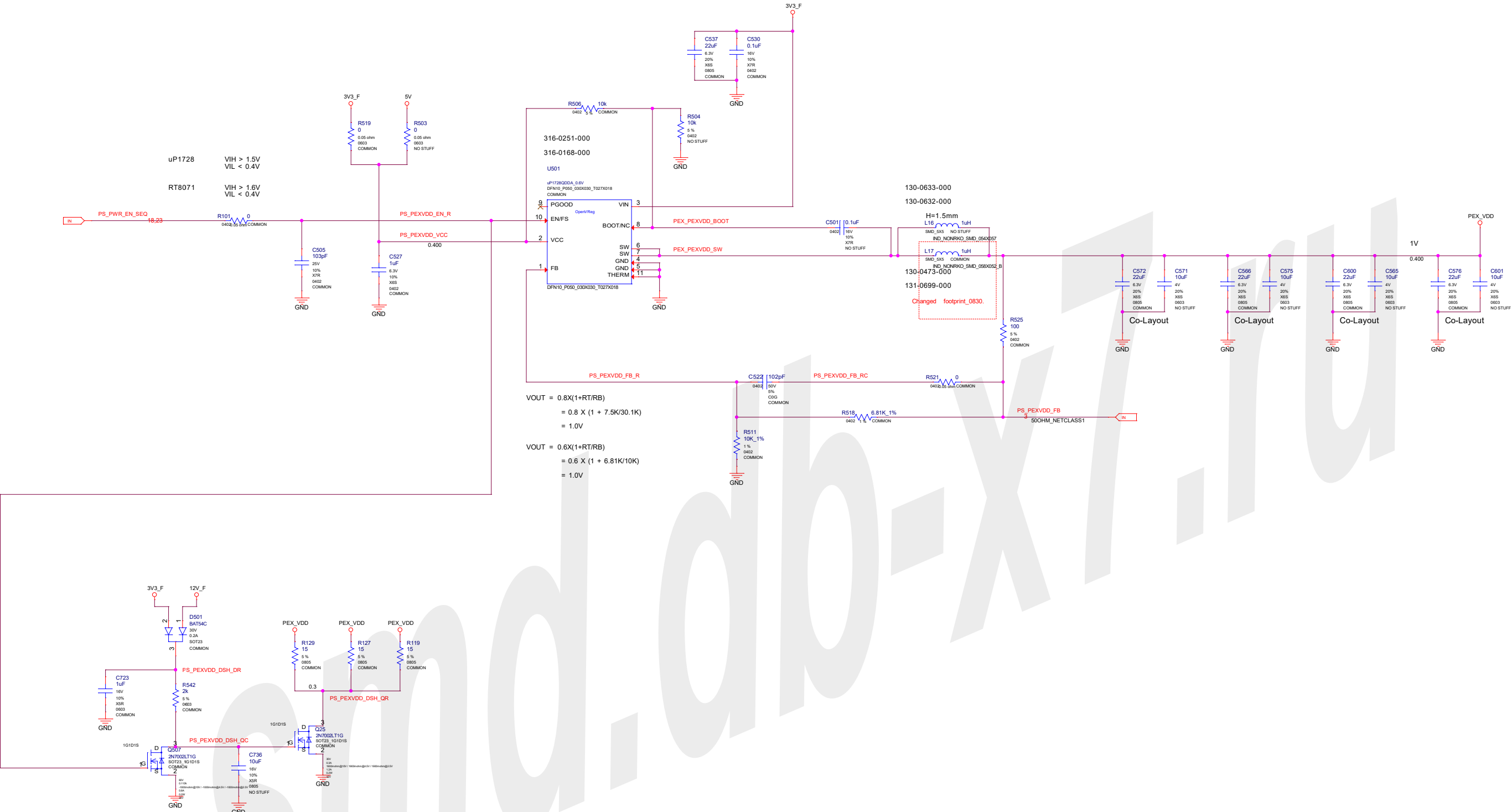
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ASSEMBLY  
PAGE DETAIL

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PSII: 5V & 12V\_FAN

GALAXY		Galaxy Microsystems (HK) Ltd.	
Page Name:		PSII:5V & 12V_FAN	
Size	Project Name:	Design By:	Rev
Custm	P75L	James	V10
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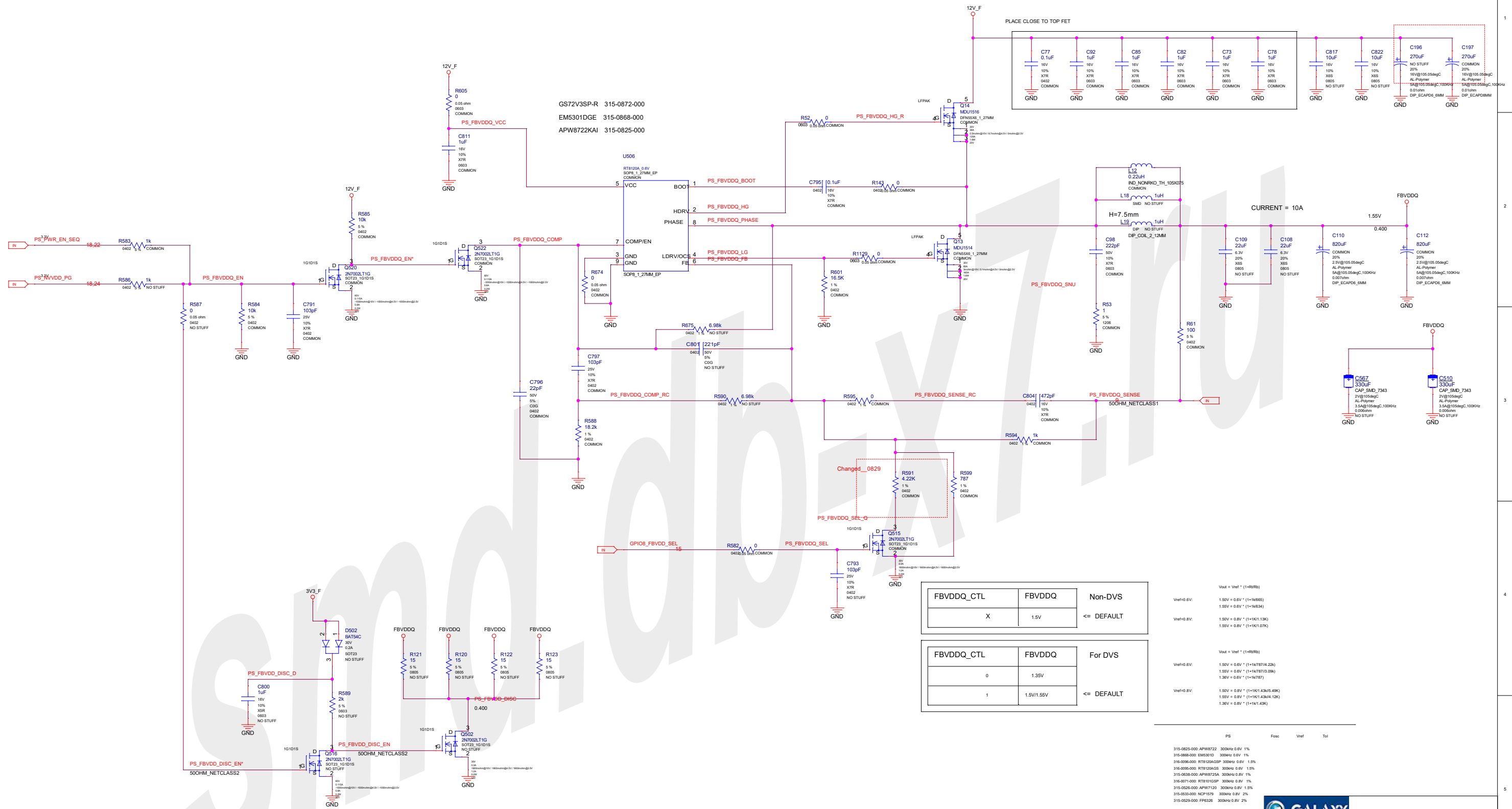
PS III: PEXVDD



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GALAXY		Galaxy Microsystems (HK) Ltd.	
Page Name:		PSII:5V & 12V_FAN	
Size	Project Name:	Design By:	Rev
Custom	P75L	James	V10
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## PS IV: FBVDDQ



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS IV: FBVDDQ


FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

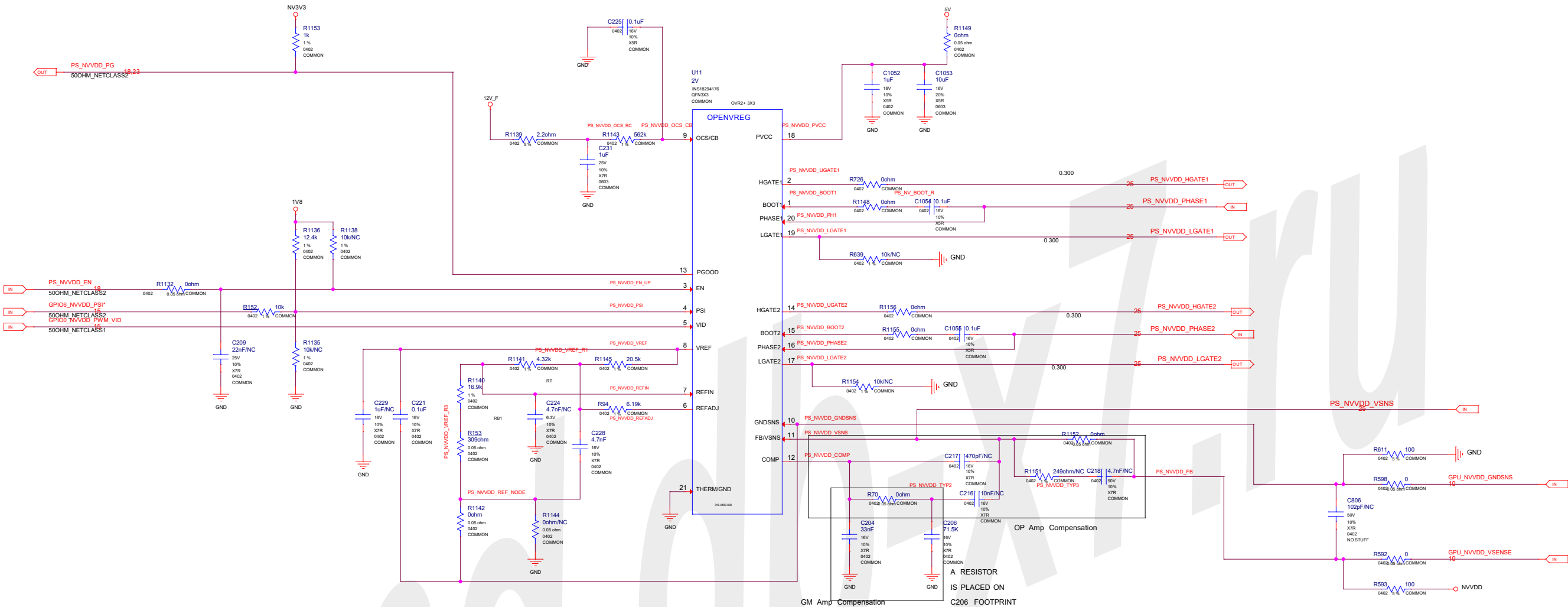
	$V_{out} = V_{ref} * (1+Rf/Rb)$
$V_{ref}=0.5V:$	$1.50V = 0.5V * (1+1K/66K)$ $1.55V = 0.5V * (1+1K/53K)$
$V_{ref}=0.8V:$	$1.50V = 0.8V * (1+1K/1K1)$ $1.55V = 0.8V * (1+1K/1K1)$
	$V_{out} = V_{ref} * (1+Rf/Rb)$
$V_{ref}=0.5V:$	$1.50V = 0.5V * (1+1K/78K)$ $1.55V = 0.5V * (1+1K/78K)$ $1.36V = 0.5V * (1+1K/78K)$
$V_{ref}=0.8V:$	$1.50V = 0.8V * (1+1K/1K1)$ $1.55V = 0.8V * (1+1K/1K1)$ $1.36V = 0.8V * (1+1K/1K1)$

PS	Fosc	Vref	Ta
----	------	------	----

315-0825-000: APW8722	300kHz 0.6V	1%
315-0868-000: EM5301D	300kHz 0.6V	1%
316-0096-000: RT8120A/GSP	300kHz 0.6V	1%
316-0095-000: RT8120A/GS	300kHz 0.6V	1%
315-0638-000: APW8725A	300kHz 0.8V	1%
316-0071-000: RT8101GSP	300kHz 0.8V	1%
315-0526-000: APW7120	300kHz 0.8V	1%
315-0533-000: NCP1579	300kHz 0.8V	2%
315-0529-000: FP6326	300kHz 0.8V	2%

 <b>GALAXY</b>		<i>Galaxy Microsystems (HK) Ltd.</i>	
Page Name: _____			
<b>PS IV: FBVDDQ</b>			
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Date: <u>Wednesday, December 21, 2016</u>		Sheet <u>23</u> of <u>27</u>	
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		DATE: _____	

PS V: NVVDD OVR2+1

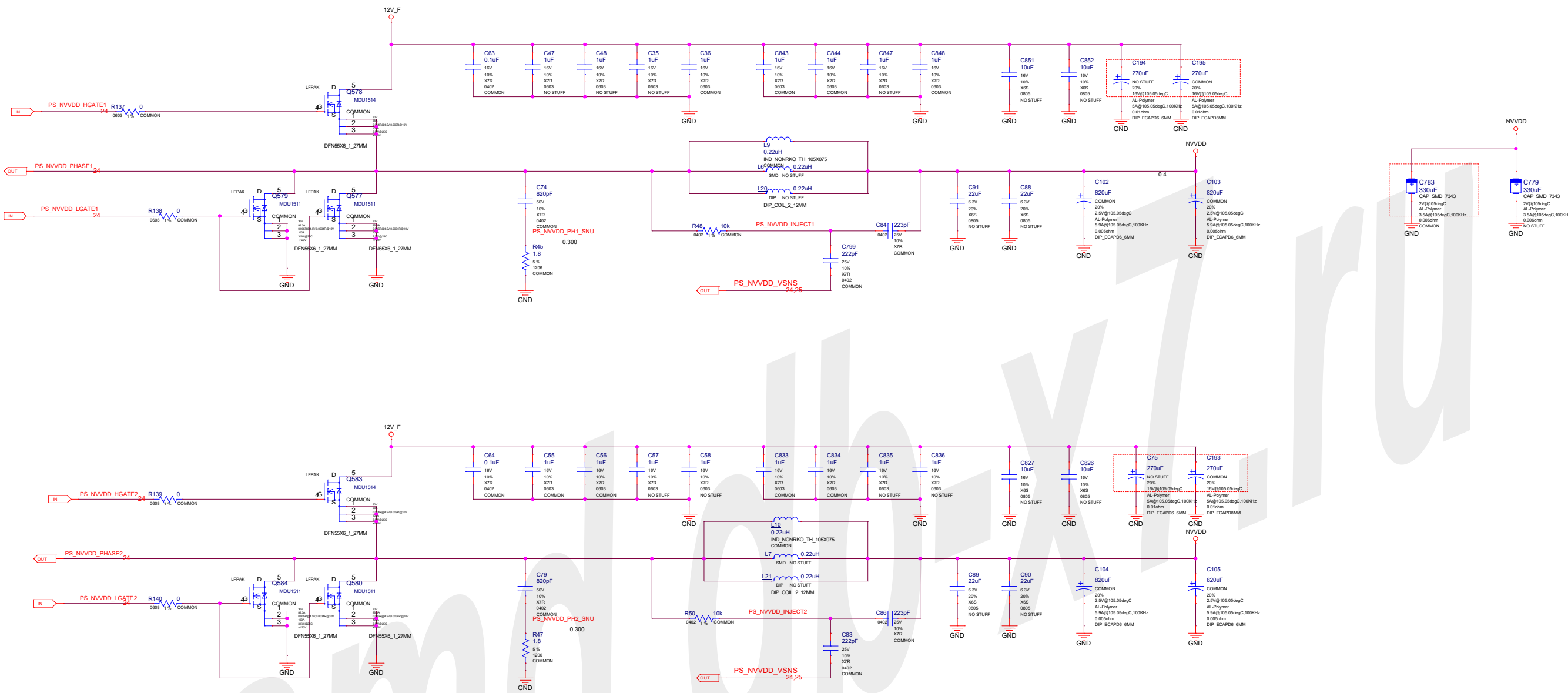


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ASSEMBLY PAGE DETAIL <ASSEMBLY\_DESCRIPTION> PS V: NVVDD OVR2+1

Page Name: PS V: NVVDD OVR2+1			
Size Custom	Project Name: P75L	Design By: James	Rev V10
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PS V: NVVDD Phase 1,2



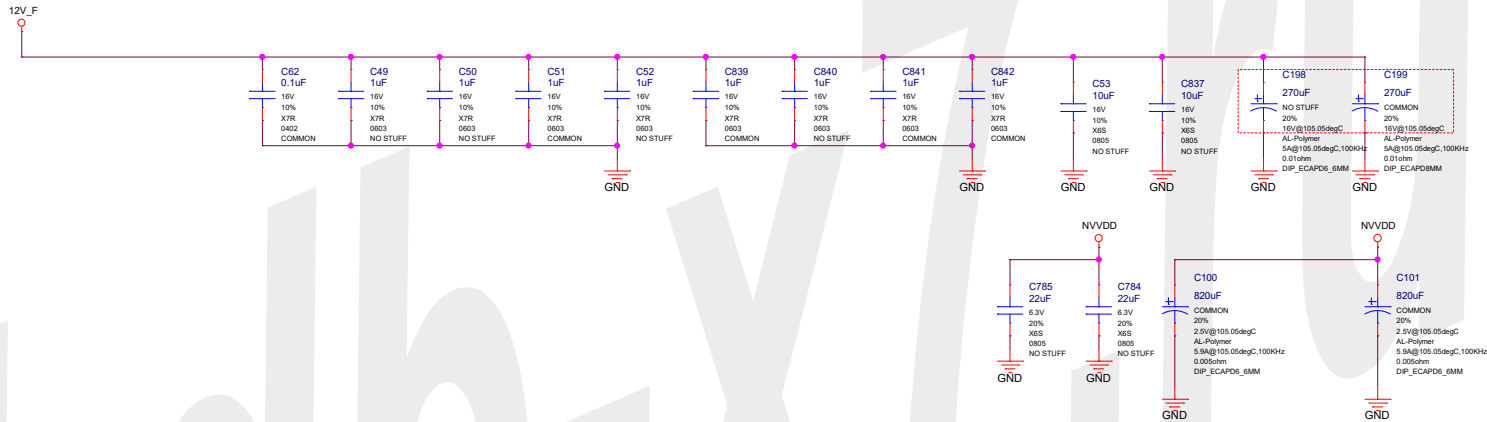
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PAGE DETAIL

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PS V: NVVDD Phase 1,2

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Page Name: PS V: NVVDD Phase 1,2			
Size: Custom	Project Name: P75L	Design By: James	Rev: V10
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PS V: NVVDD Phase 3



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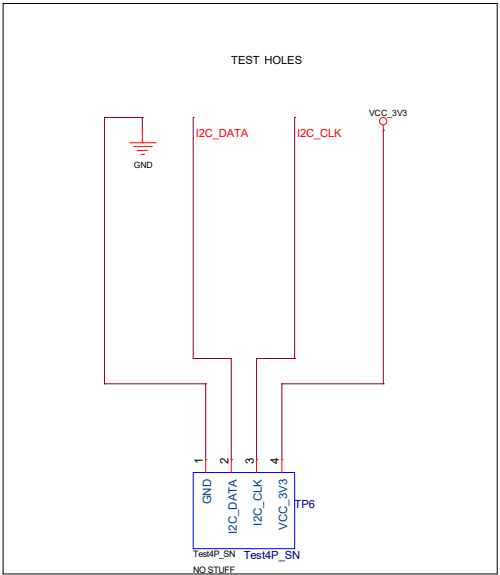
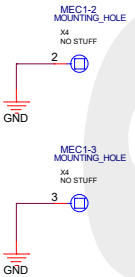
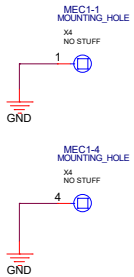
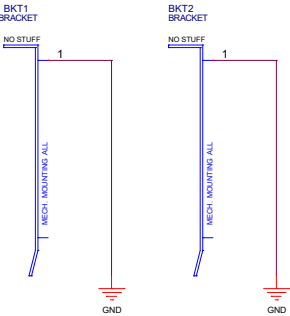
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Page Name:				PS V: NVVDD Phase 3			
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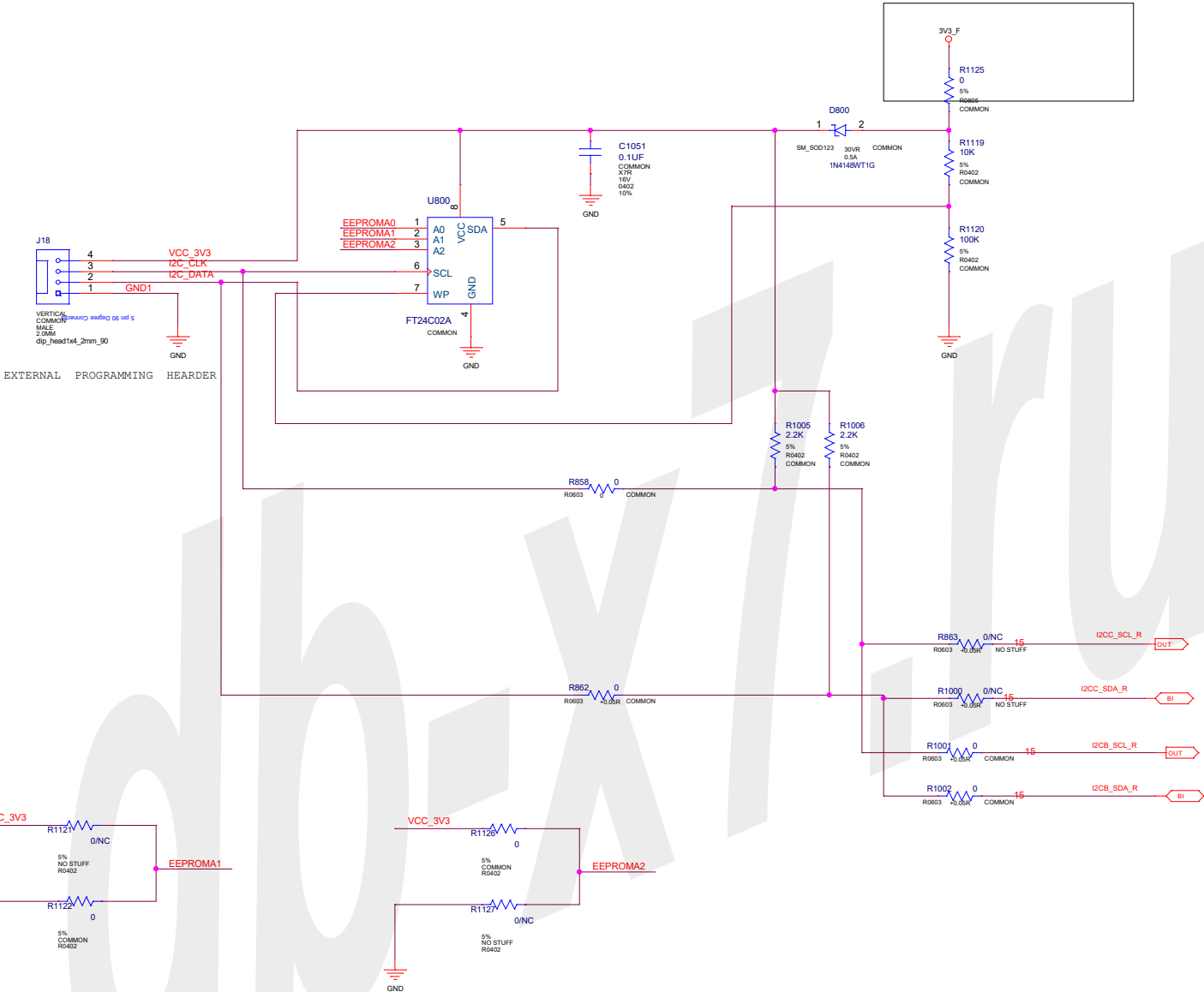


SN EPROM

Brackets:




PLACEMENT IN PCB : (TOP VIEW)  
FROM LEFT TO RIGHT : GND,I2C\_DATA,I2C\_CLK,VCC\_3V3



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ASSEMBLY  
PAGE DETAIL  
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MECH: Bracket/Thermal

		<i>Galaxy Microsystems (HK) Ltd.</i>		
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Size Custom	Project Name: <b>P75L</b>		Design By: James	Rev V10
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