

PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

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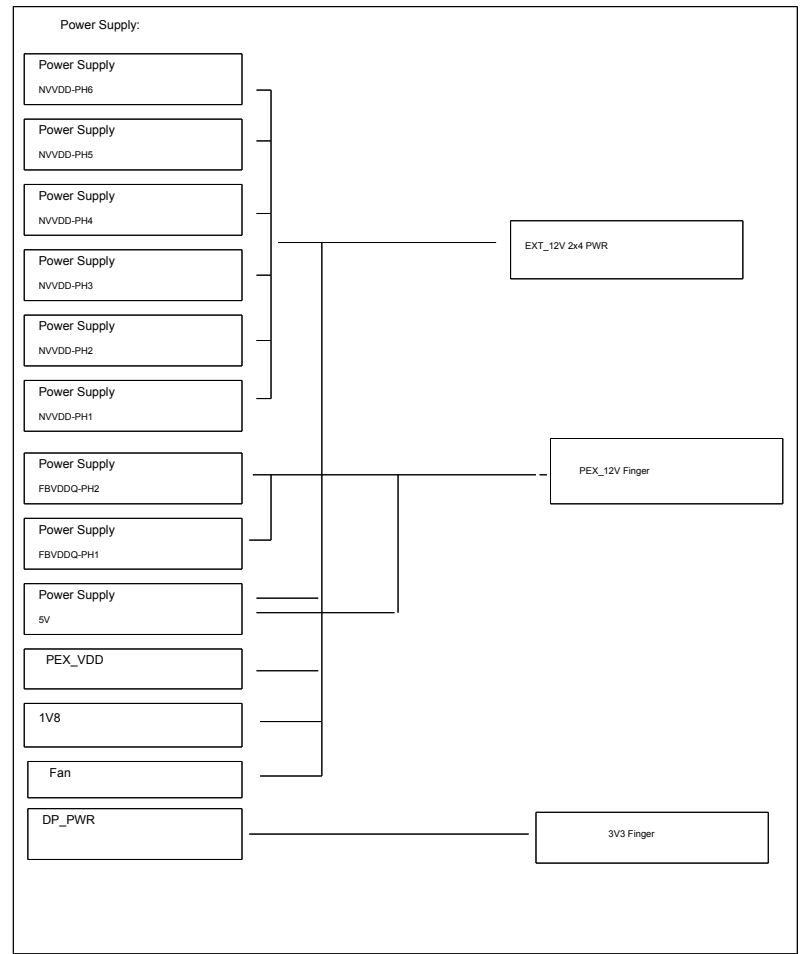
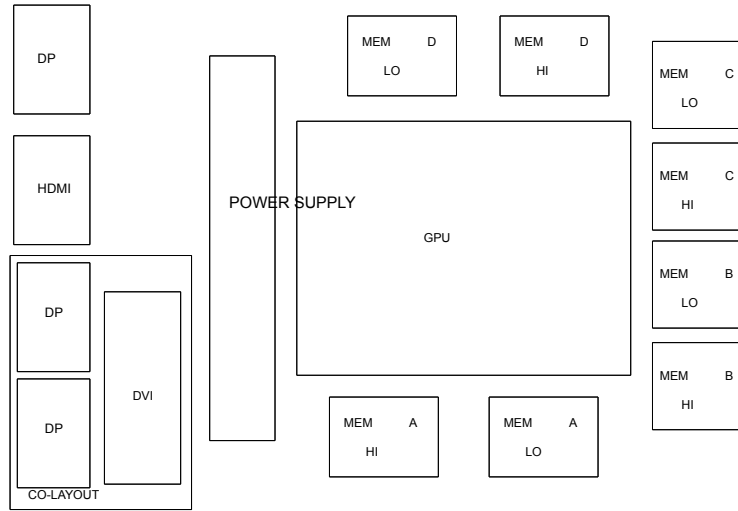
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NUMBER	DESCRIPTION
PG161-A00	TABLE OF CONTENTS

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10000 NVIDIA DRIVE AVENUE			
DALLAS, TEXAS 75243-1489			
			
MC-PN	800-1G161-BASE-000	REV	1.0F-01
FILE NO.	PG161-A00	DATE	21-04-2018
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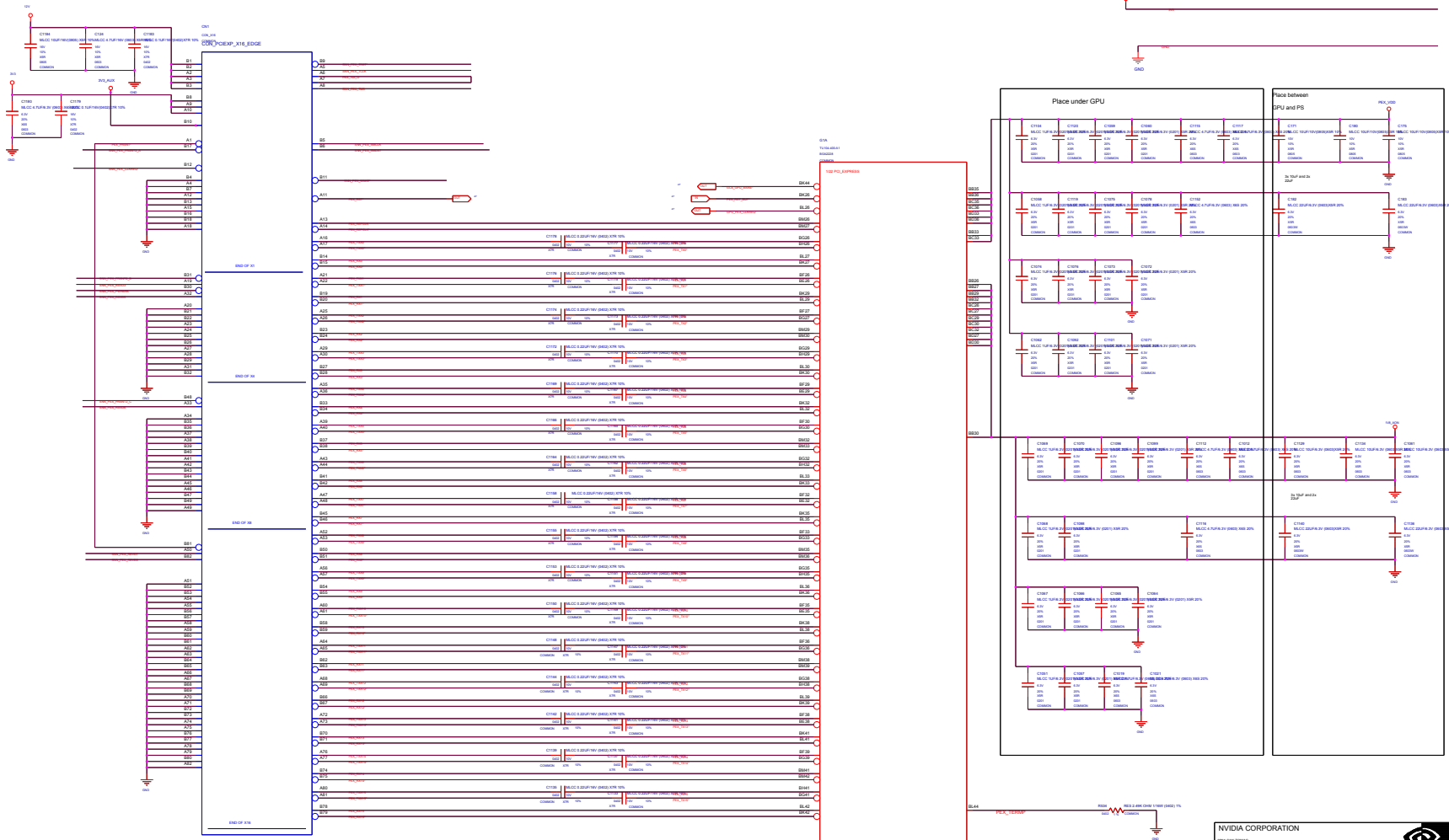


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Version	1.0
Date	01/20/2018

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SANTA CLARA, CA 95050, USA			
NV_PN	600-IG161-BASE-000	REV	1.0
REV	1.0	DATE	01/20/2018






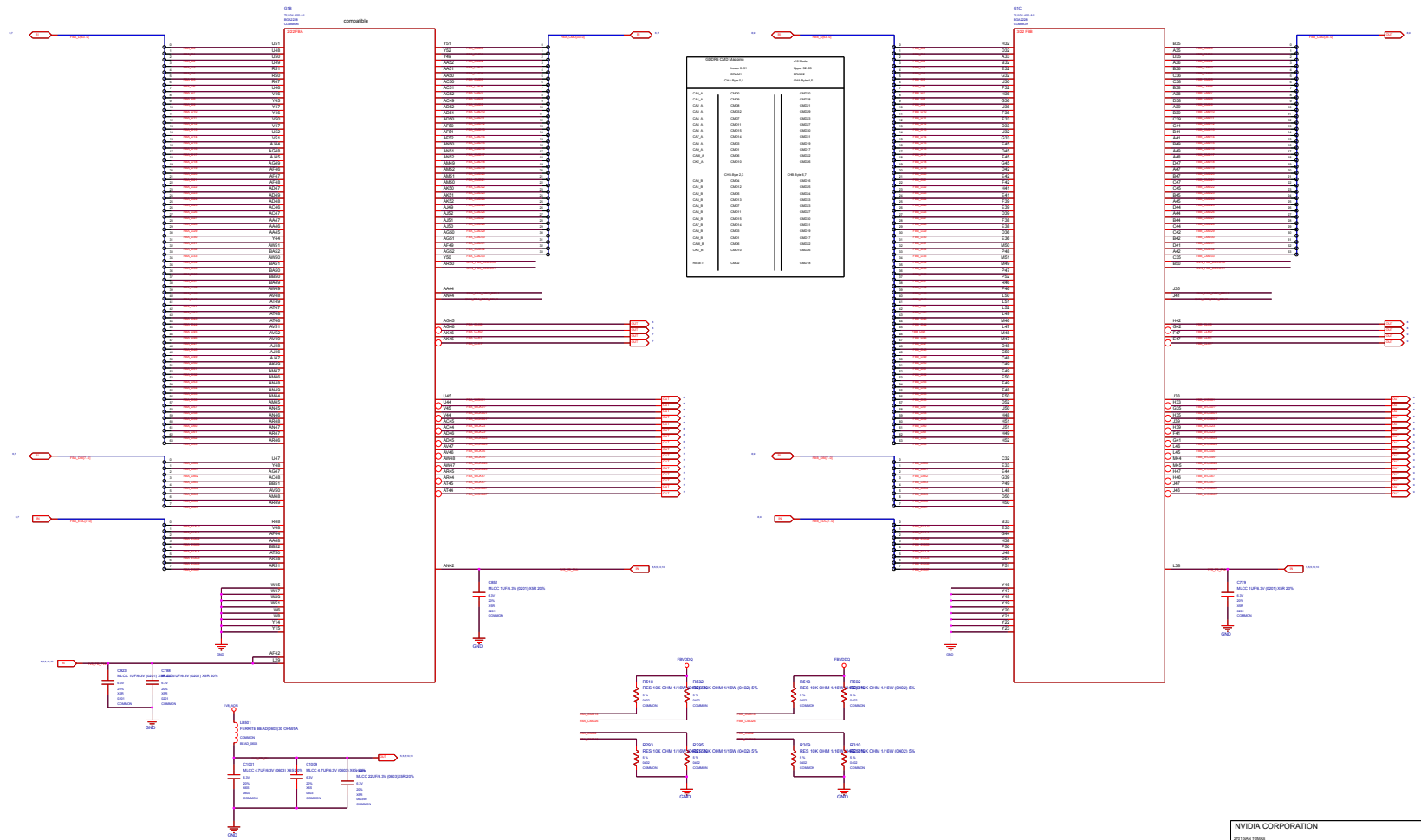
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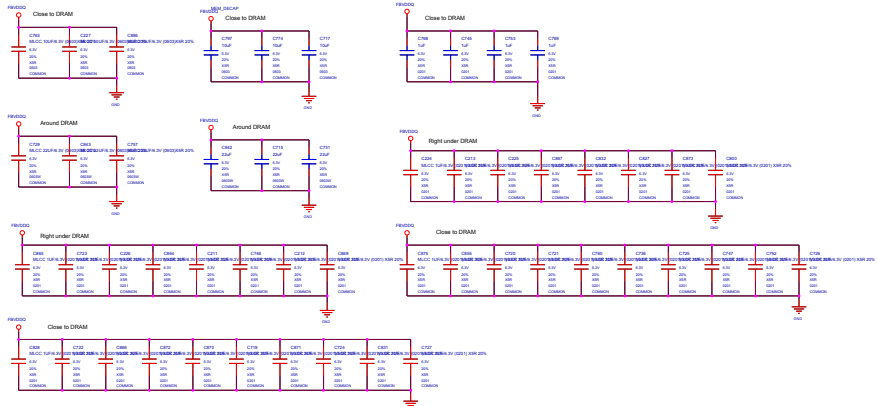
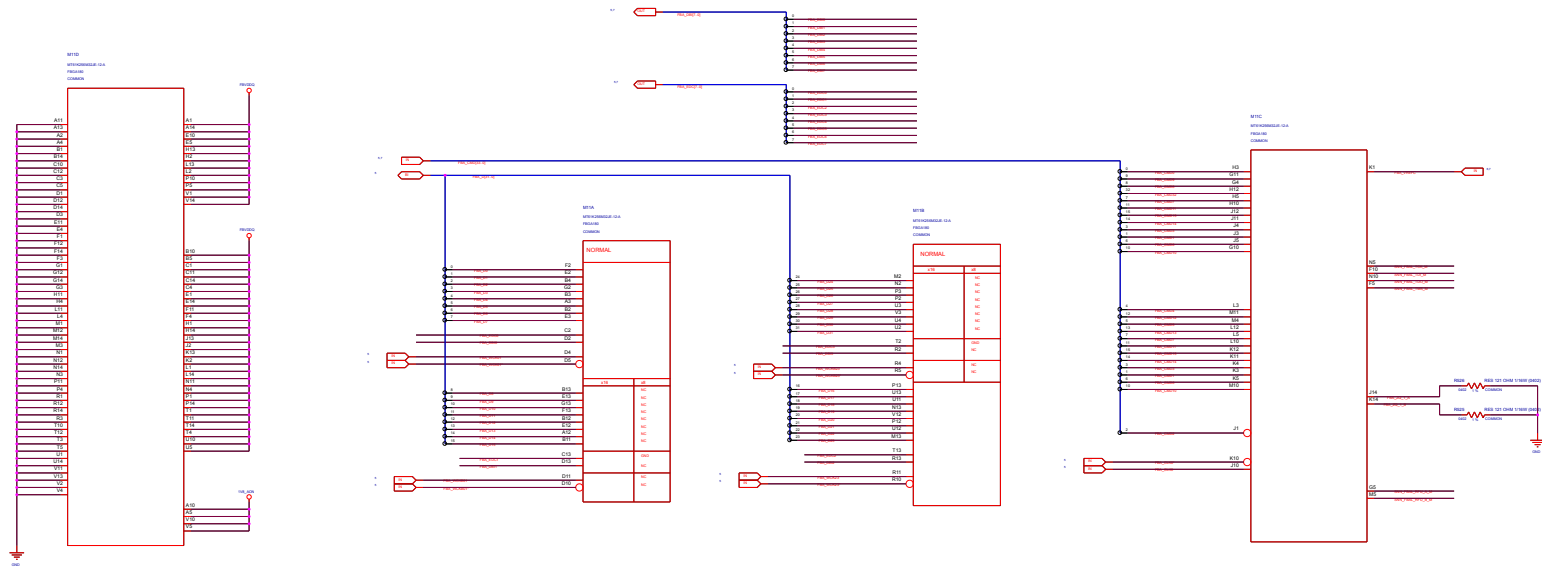
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DATE: 2018-07-10	REVISION: 001 (P1, P2)

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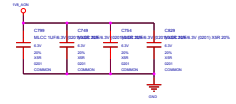
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NV_PN	800-IG161-BASE-000	DATE	8/2/18
PROJ	800-IG161	DESIGNER	SPR
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VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.2K
FOR R108



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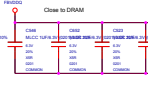
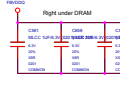
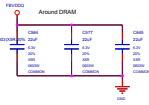
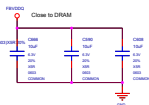
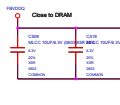
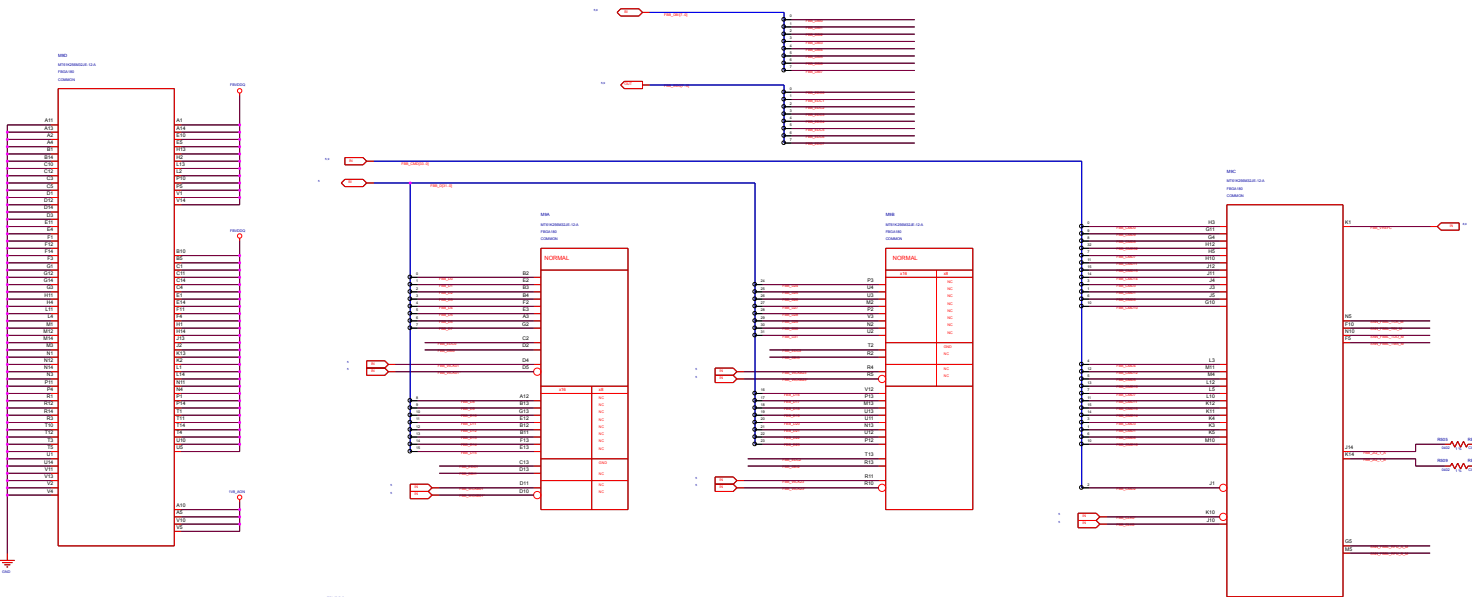
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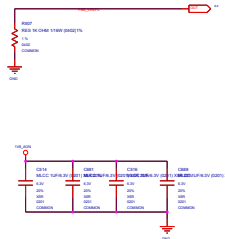
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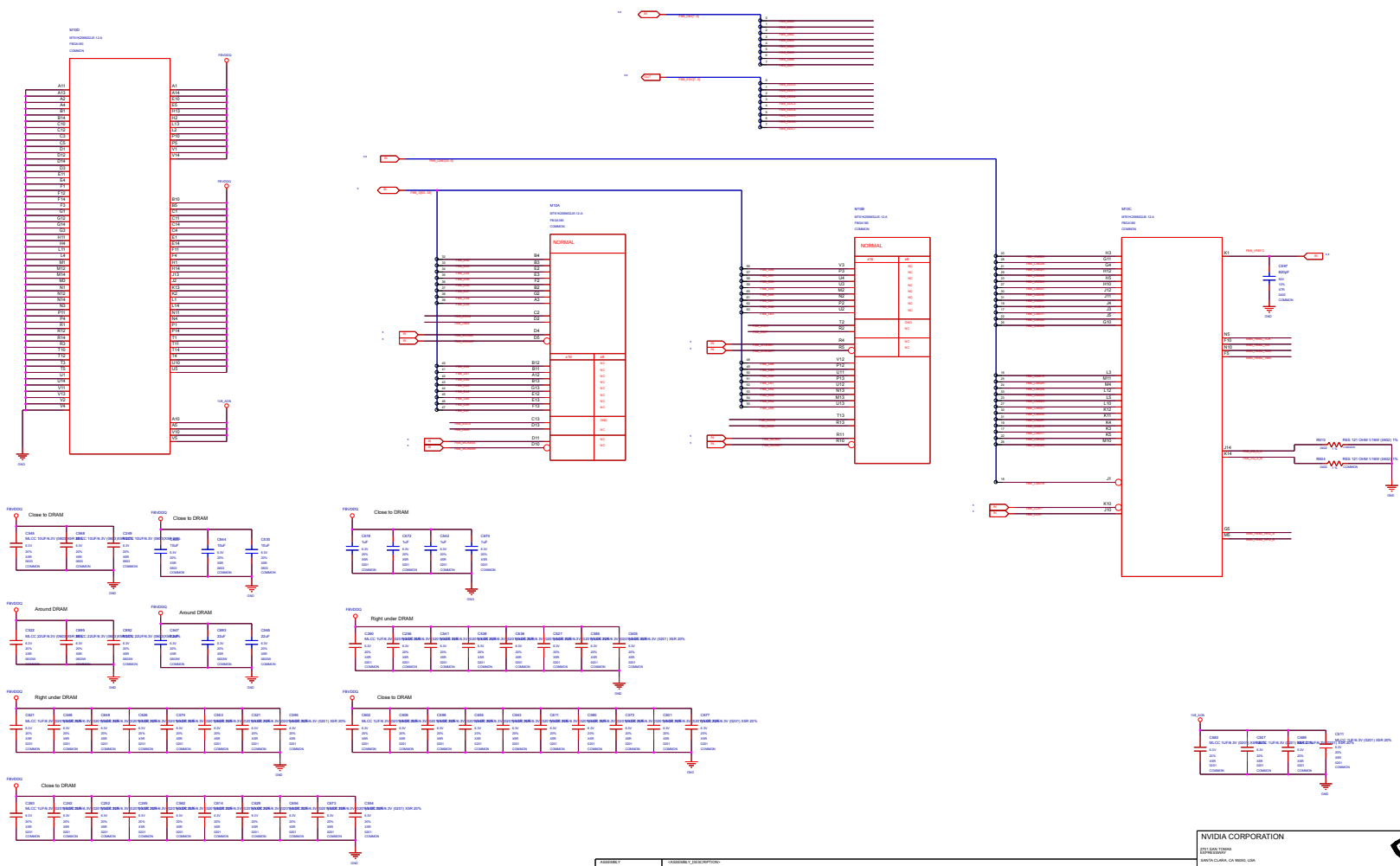
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VREFC IS NOT USED IN x16 CONFIGURATION. IN OHM PULL-DOWN IS IN PLACE OF THE 1.5KΩ FOR R104.





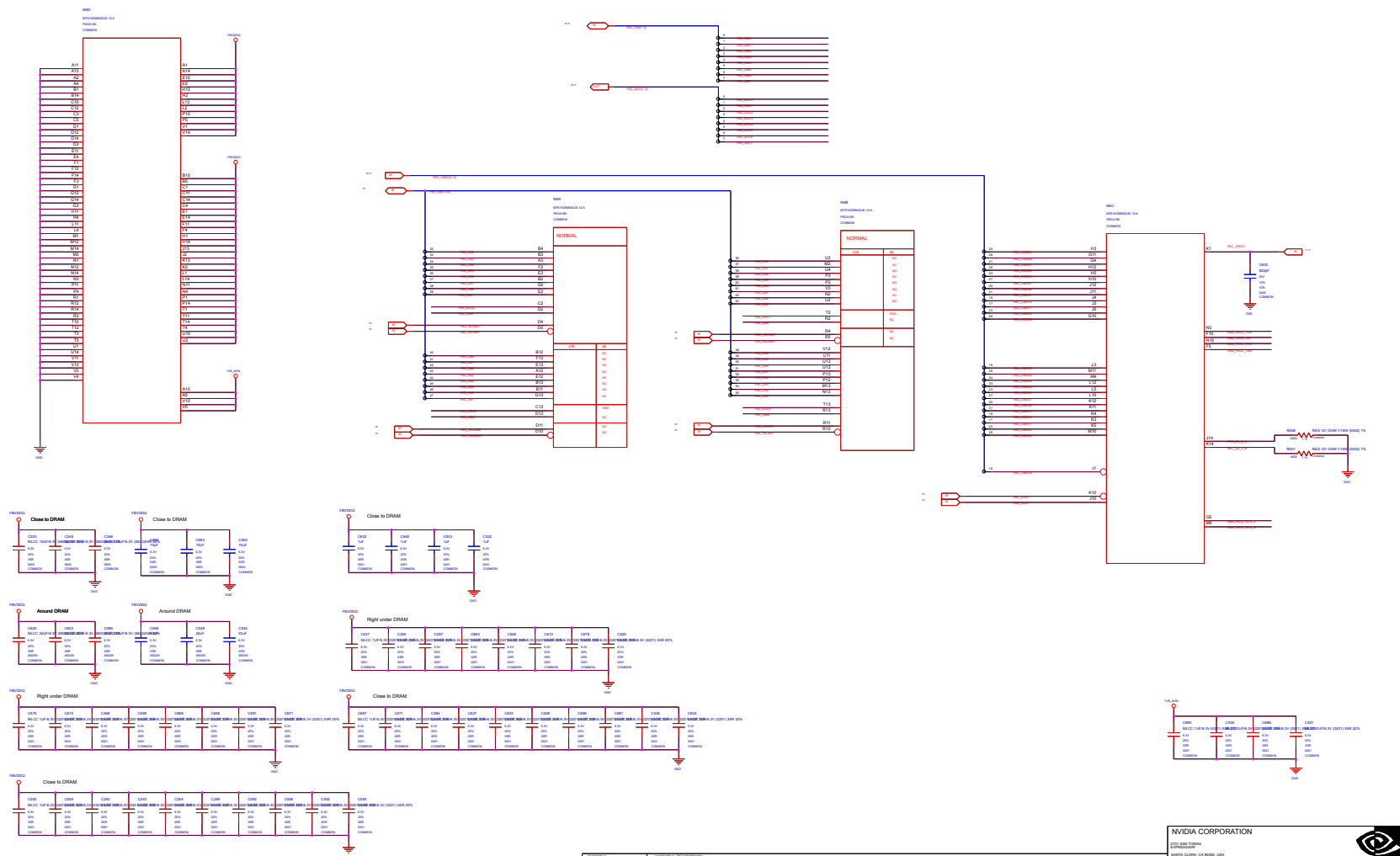
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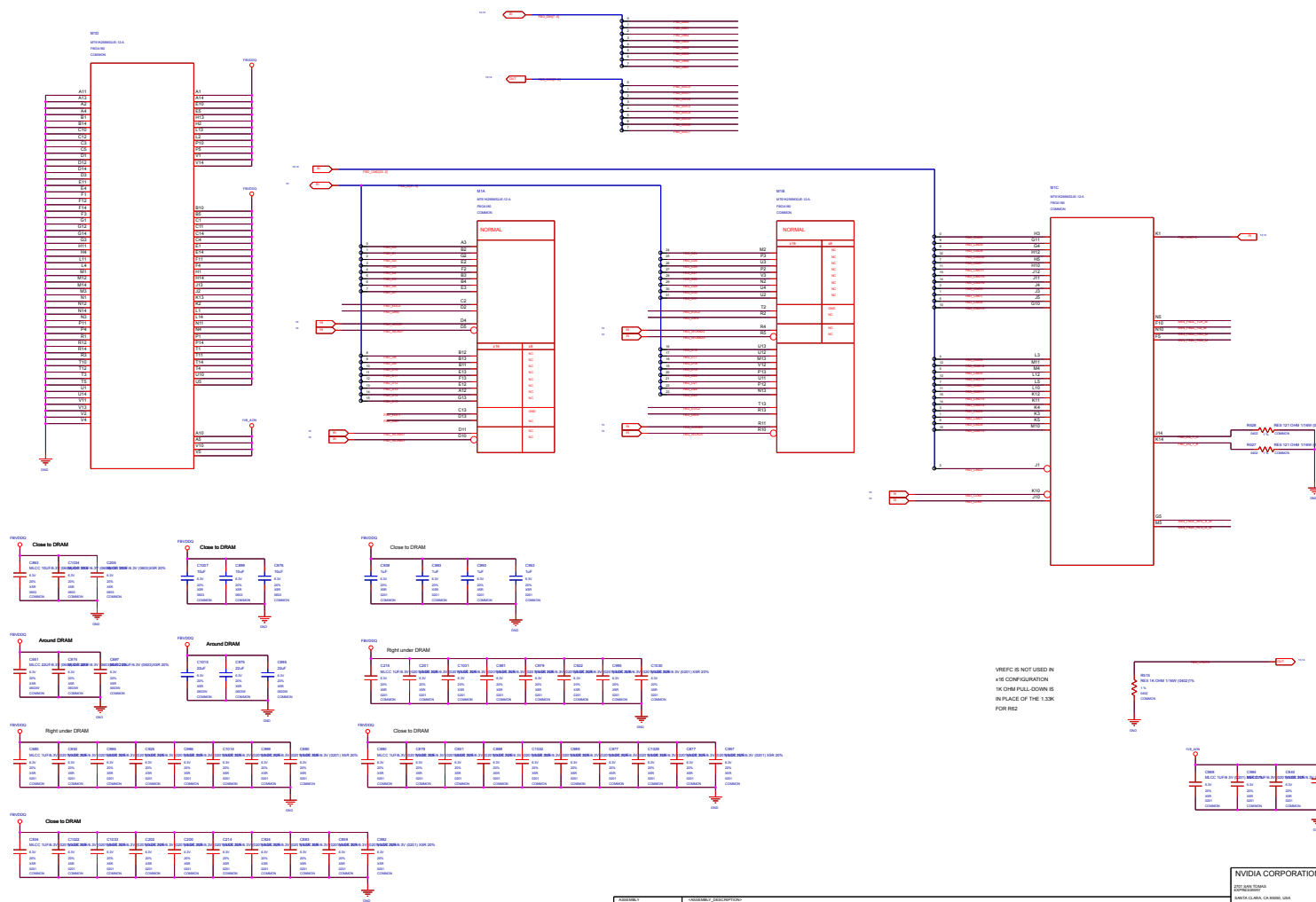
REVISION	DESCRIPTION / REVISION
1.0	INITIAL RELEASE

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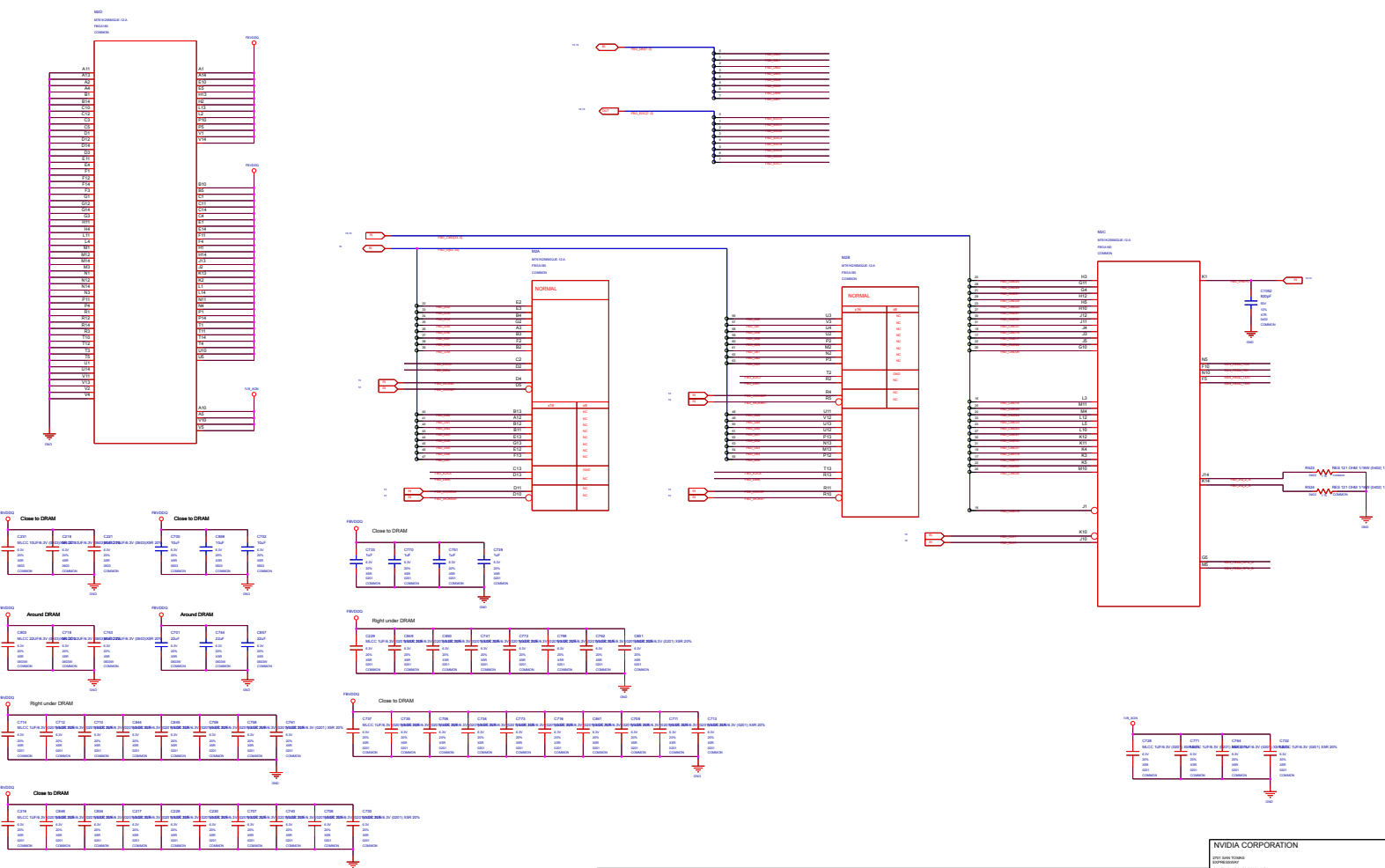
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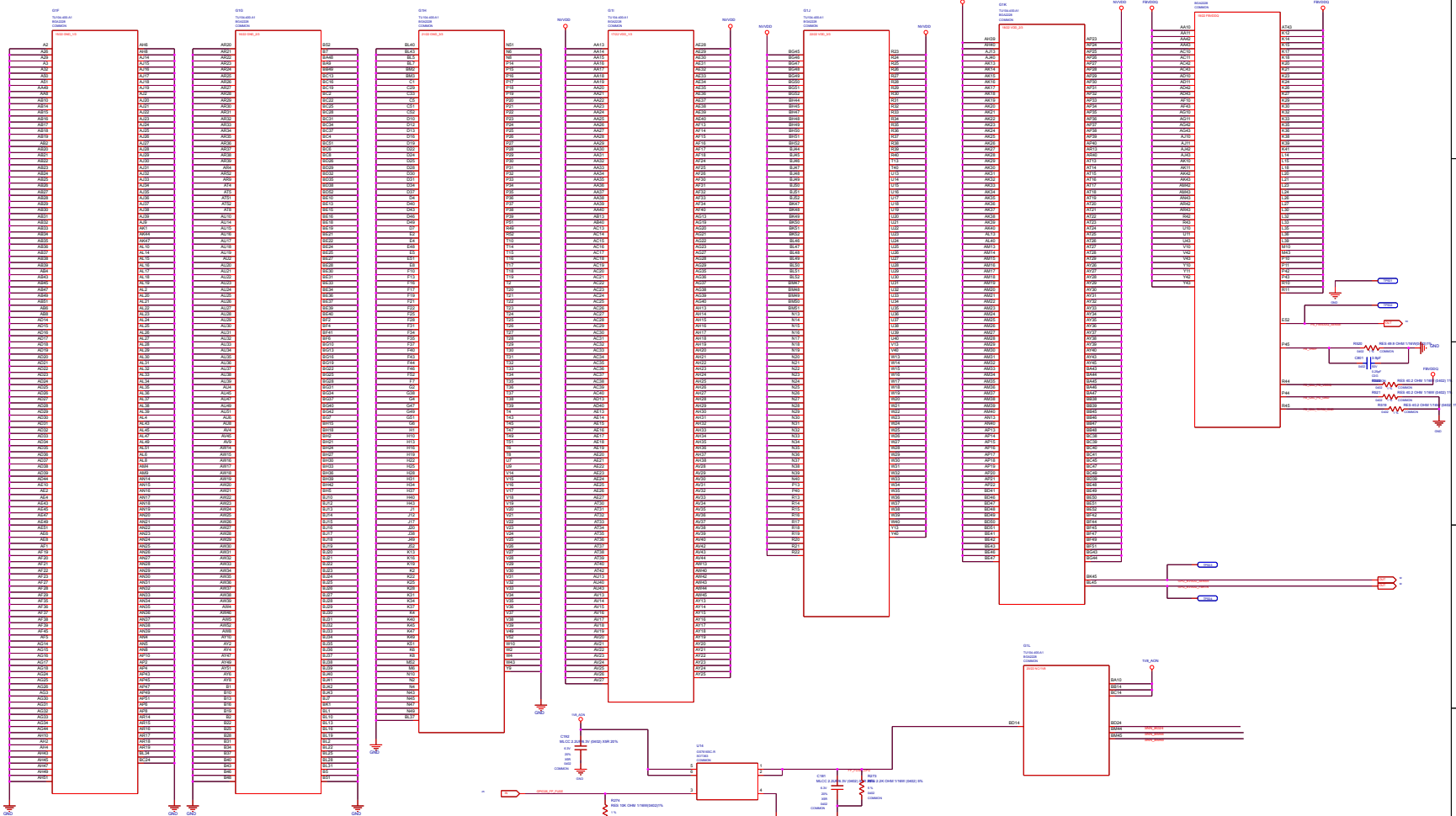
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REV	1.0
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REV	1.0



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REV. 0/0	600-1G161-BASE-000
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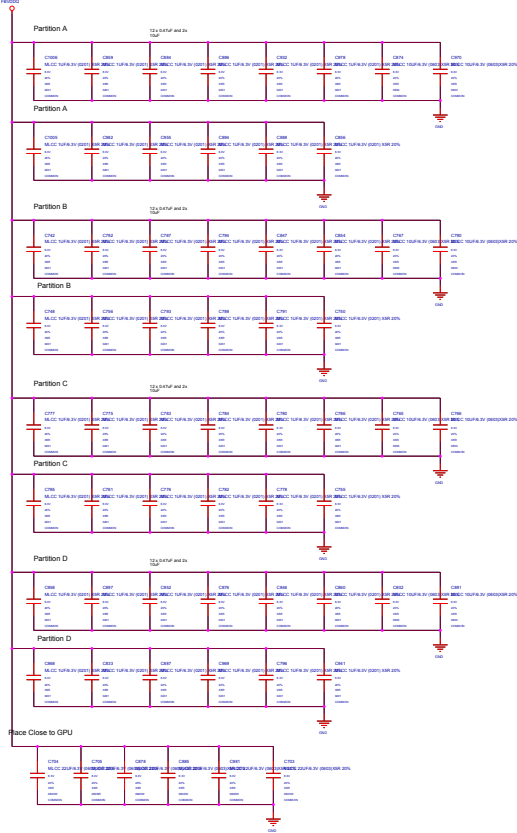


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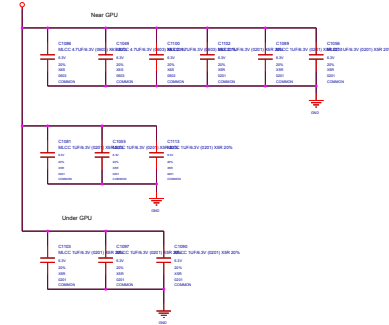
FBVDDQ



NVVDQ



1V8_AON



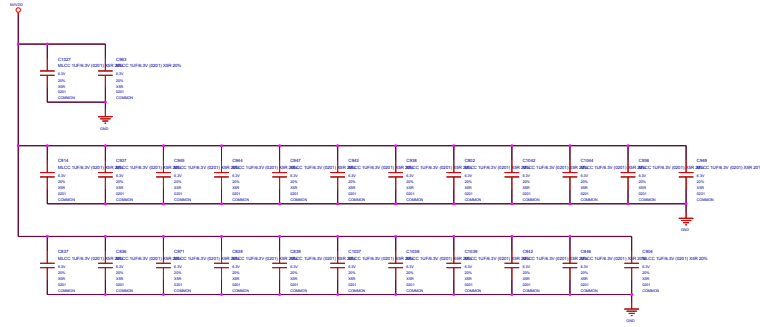
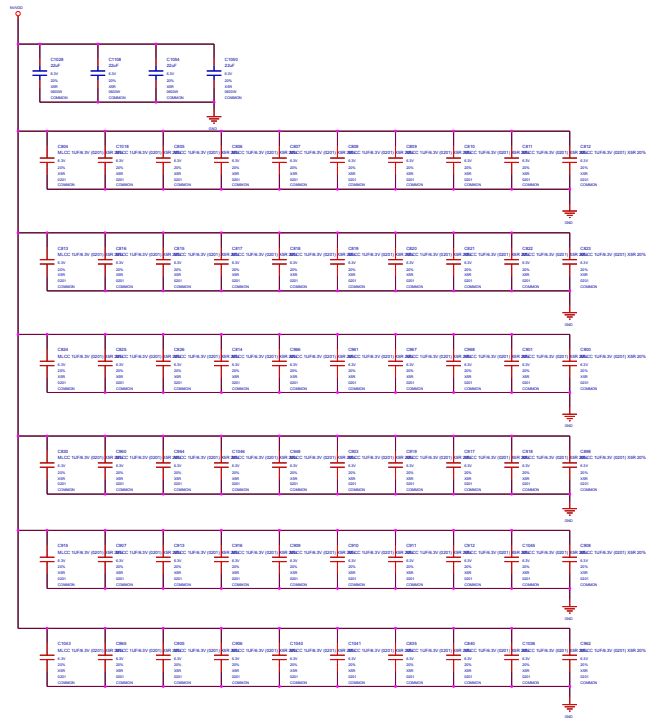
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DESIGN	GPU Decoupling

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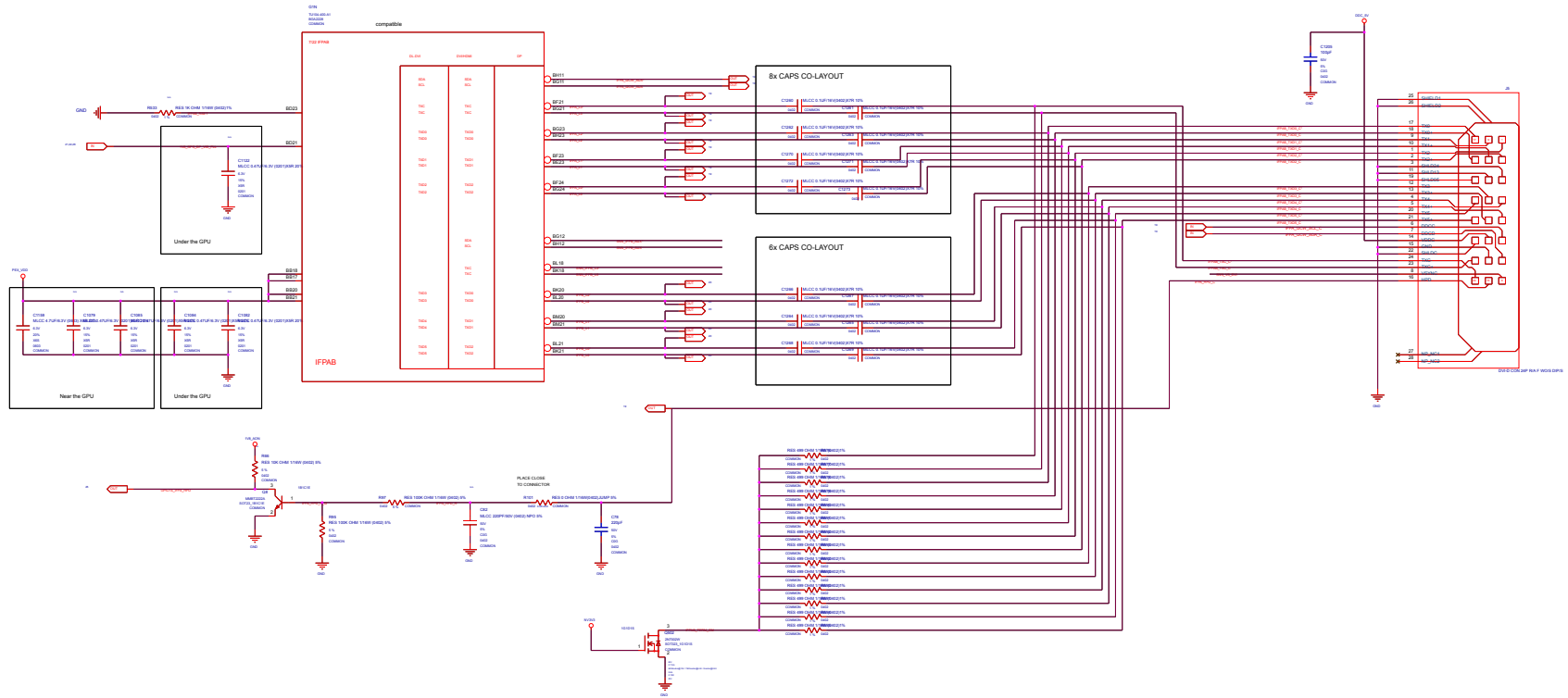
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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002	DESIGN CHANGES

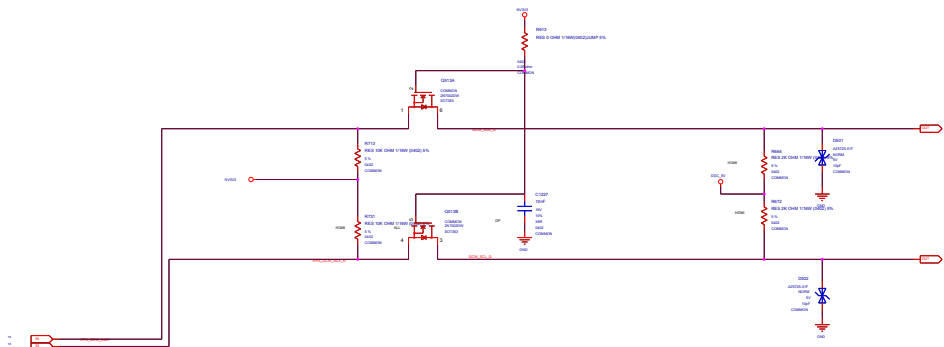
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1000 AVENUE OF THE SCIENCES
SANTA CLARA, CA 95051 USA

NY PIN: 600-1G161-BASE-000


Rev: 1.00
Date: 10/10/2011





IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

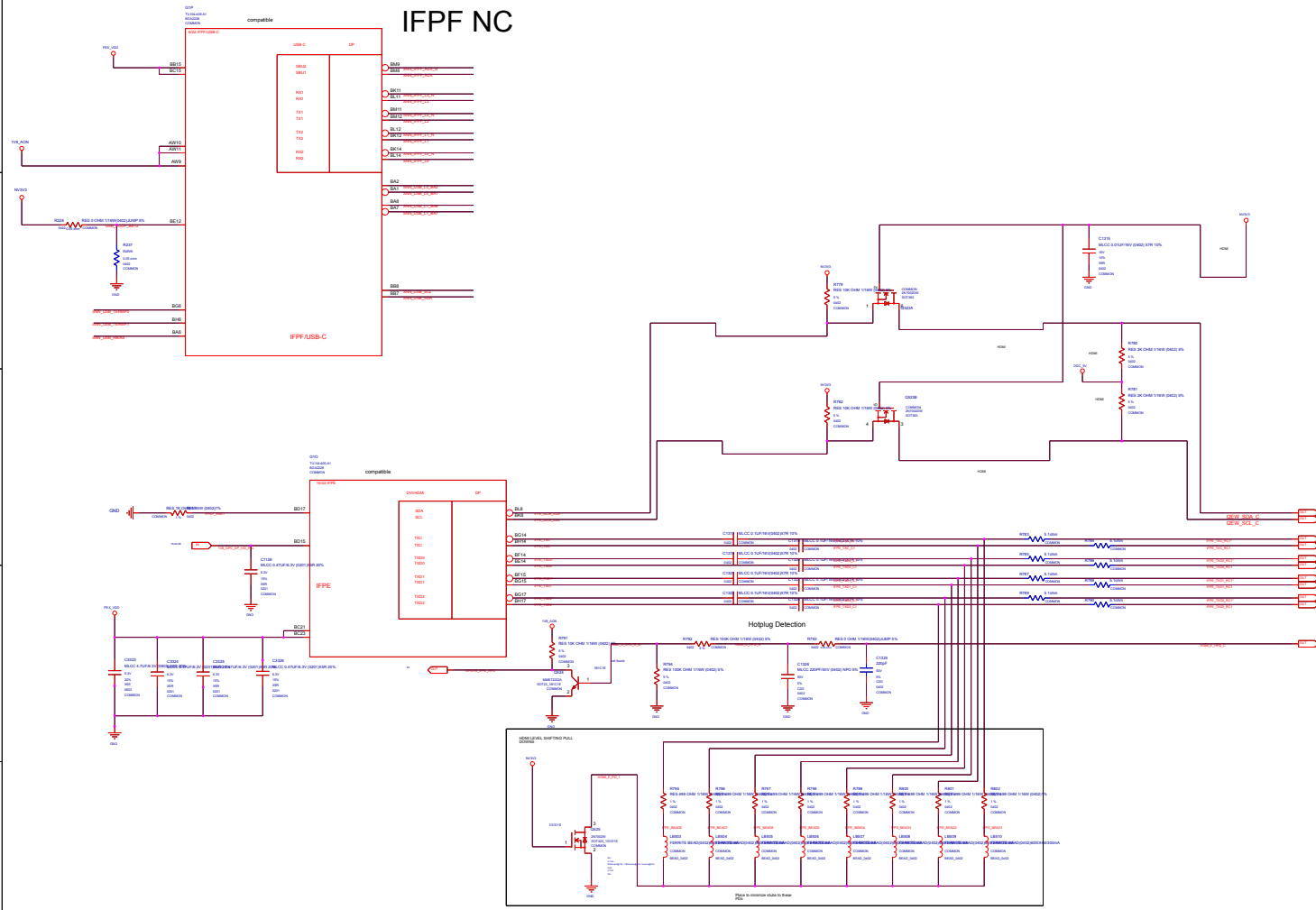
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2330 AVENUE OF THE CACTUSES SANTA CLARA, CA 95058, USA		
14C-774	800-1G161-BASE-000	REV. A
DATE	27 OCT 2018	REV. A




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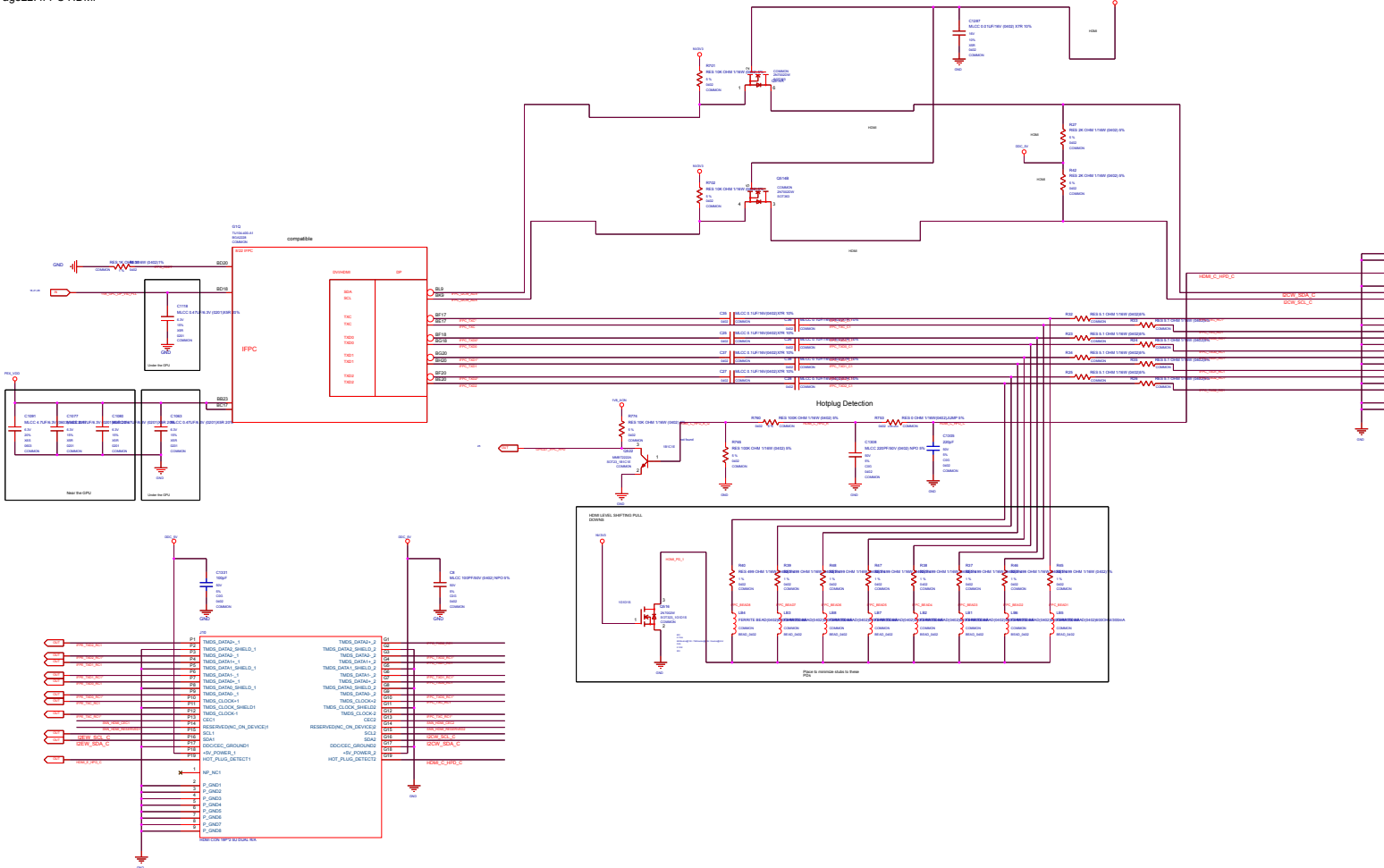
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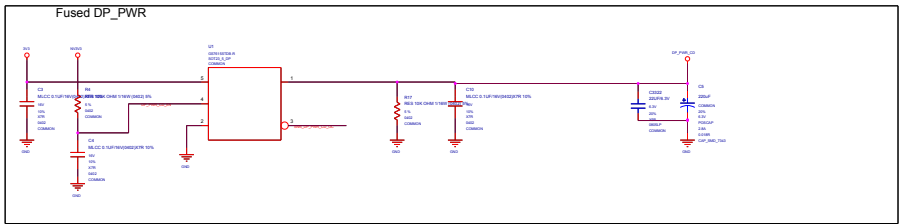
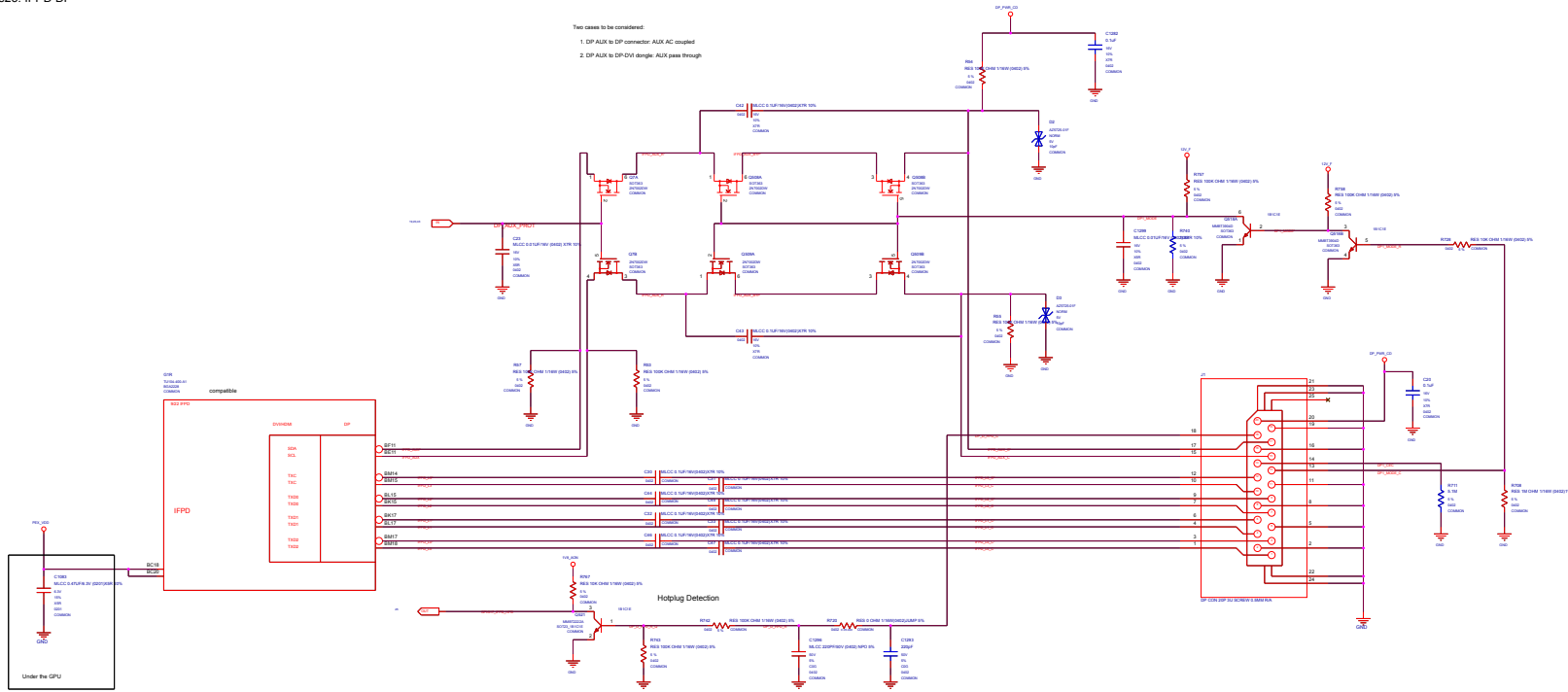
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REV D01	1	21 OF 31



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1.0	11/11/11	Initial Release

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Two cases to be considered:
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 2. DP AUX to DP-DVI adapter: AUX pass through

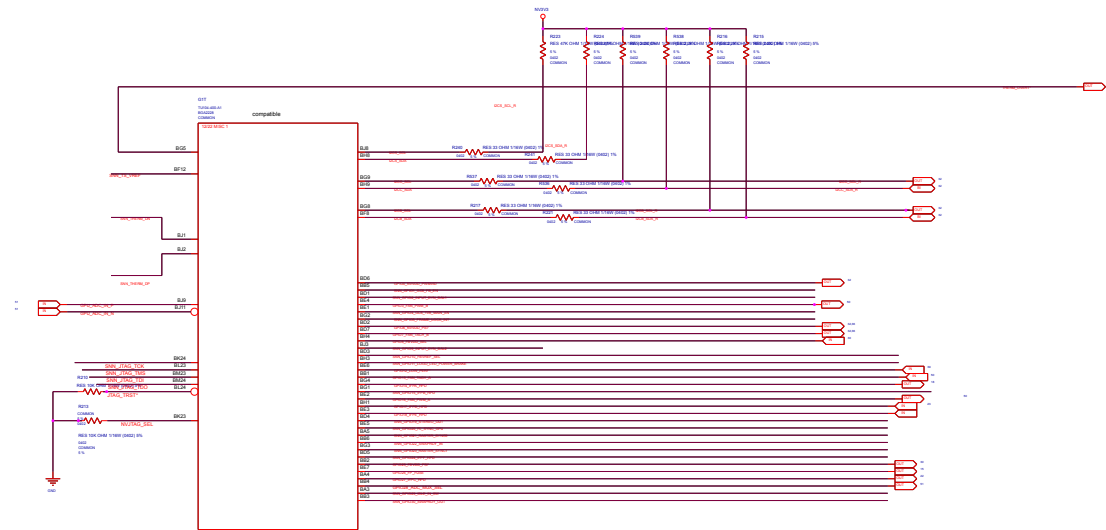


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Document ID	Document Description
600-1G161-000	DP-DVI Adapter

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2700 BAY FRONT ST			
SANTA CLARA, CA 95058, USA			
Doc ID	600-1G161-000	Rev	1.0
Doc Rev	1.0	Date	07/20/2014
Doc Type	PCB	Doc No	600-1G161-000






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FILE NAME	FILE DESCRIPTION
MISC1	MISC1

NVIDIA CORPORATION
 2700 RAVENSWOOD DRIVE
 SANTA CLARA, CA 95050-5005

800-IG161-BASE-000

REV: 1.0
 DATE: 11-01-2011



STRAP2	STRAP1	STRAP0	RAMCFQ[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00110
H	L	H	00111
L	L	M	01000

RAMCFQ[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256M	Samsung	C
00001	8Gb	256M	Micro	A
00010	8Gb	256M	Hynix	M
00011	8Gb	256M	Samsung	C
00100	8Gb	256M	Micro	A
00101	8Gb	256M	Hynix	M
00110	16Gb	256M	Samsung	M
00111				

ROM_S0	ROM_S1	ROM_SCLK	DUMMY[2:0]FS_OVERT	1ENABLE 0 DISABLE
L	L	L	XXXX1	FS_OVERT ENABLE
L	L	M	XXXX0	FS_OVERT DISABLE

STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_E_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

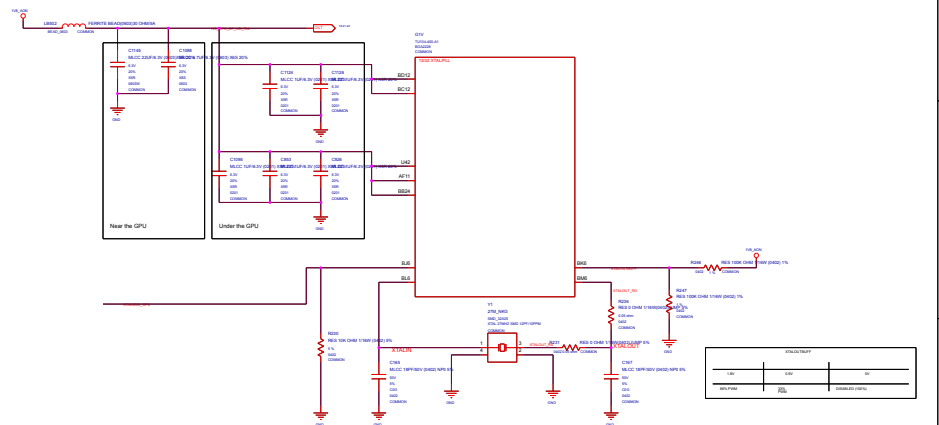
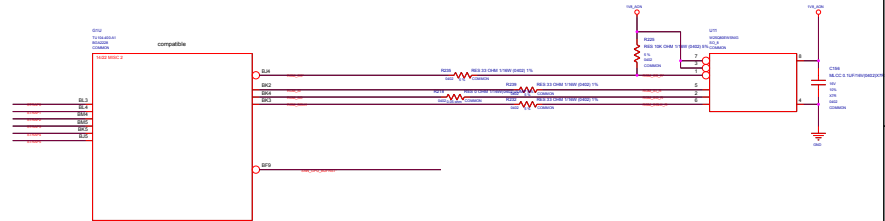
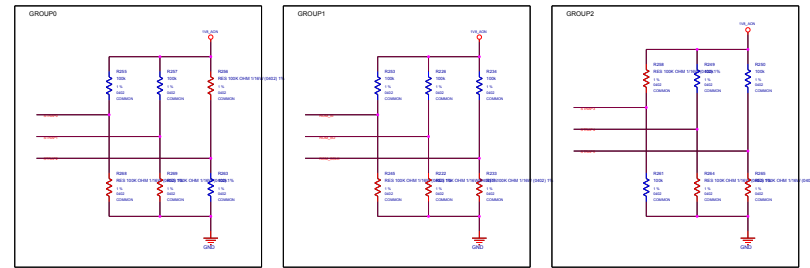
H=High -Tied to 1.8V
M=Medium -Tied to 0.9V
L=Low -Tied to 0V

1.SMB_ALT_ADDR ENABLE
0.SMB_ALT_ADDR DISABLE

1.DEVID_SEL REBRAND
0.DEVID_SEL ORIGINAL

1.PCI_E_CFG LOW POWER
0.PCI_E_CFG HIGH POWER

1.VGA_DEVICE ENABLE
0.VGA_DEVICE DISABLE



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SANTA CLARA, CA 95058, USA

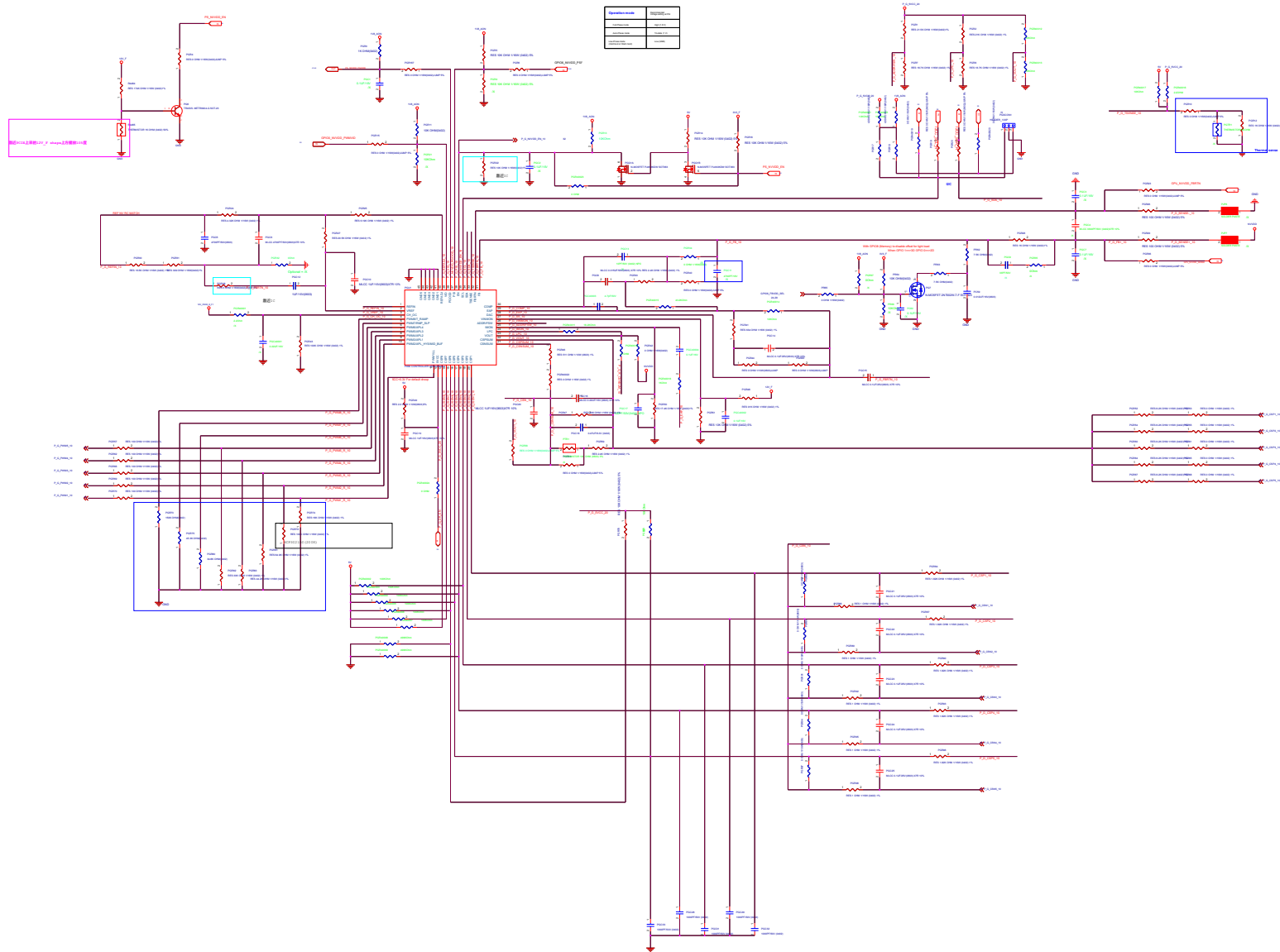
REV: 001

600-1G161-BASE-000

REV: 001

DATE: 08/07/10

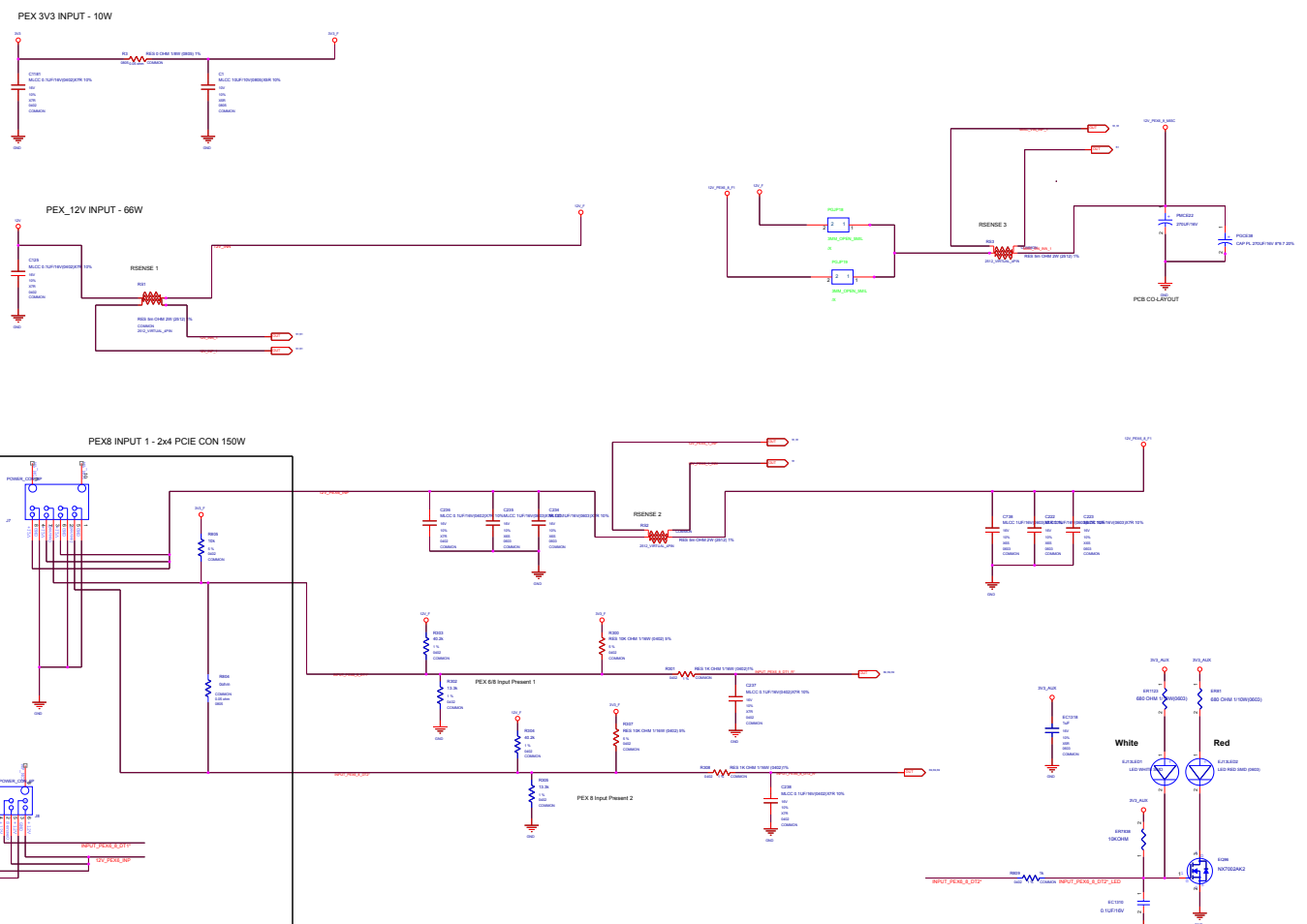
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Symbol	Value
[Resistor]	10k
[Capacitor]	100n
[Diode]	1N4148
[MOSFET]	IRF540
[IC]	ATmega328P

Microcontroller Pin Configuration

- Component List
- Part 1: Resistor
- Part 2: Capacitor
- Part 3: Diode
- Part 4: MOSFET
- Part 5: IC



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ASSEMBLY	ASSEMBLY DESCRIPTIONS
PCB CD LAYOUT	PCB CD LAYOUT AND CONNECTIONS

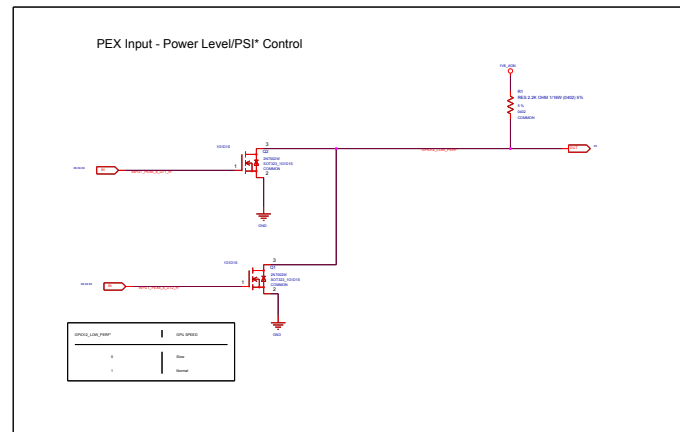
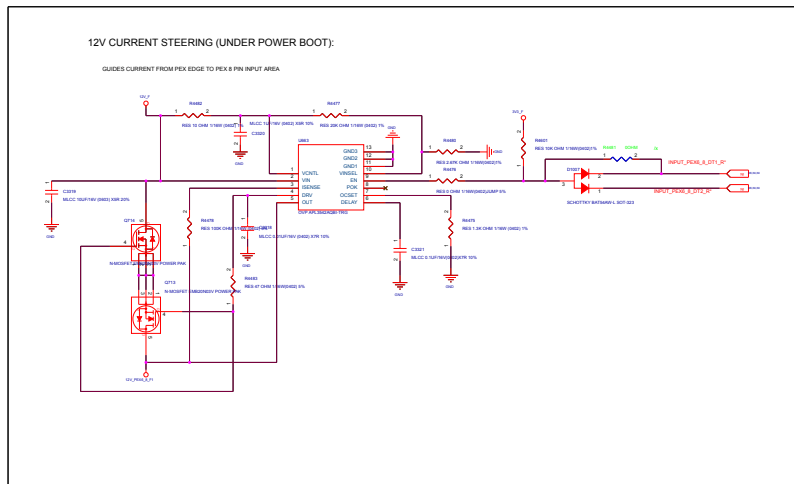
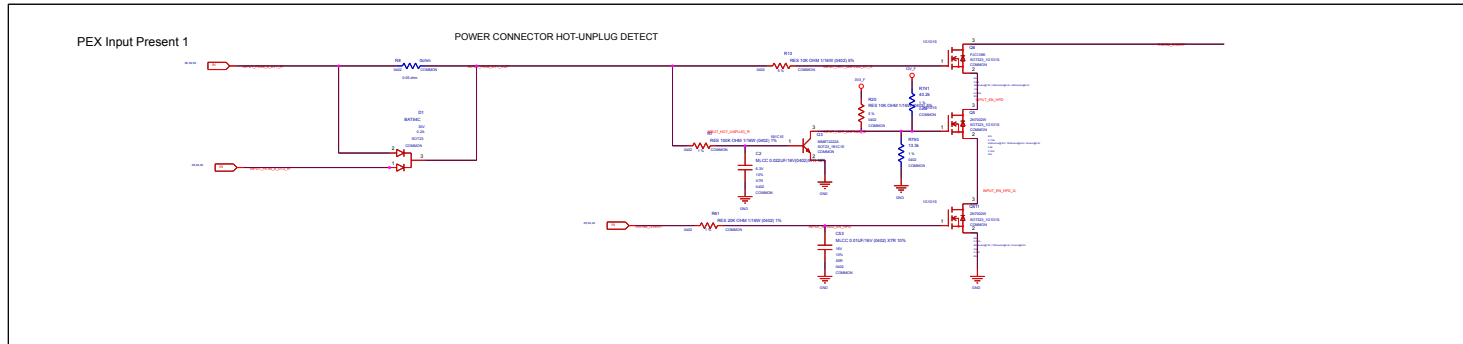
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REV	DATE	BY	CHKD BY
1.0	11/01/2016		

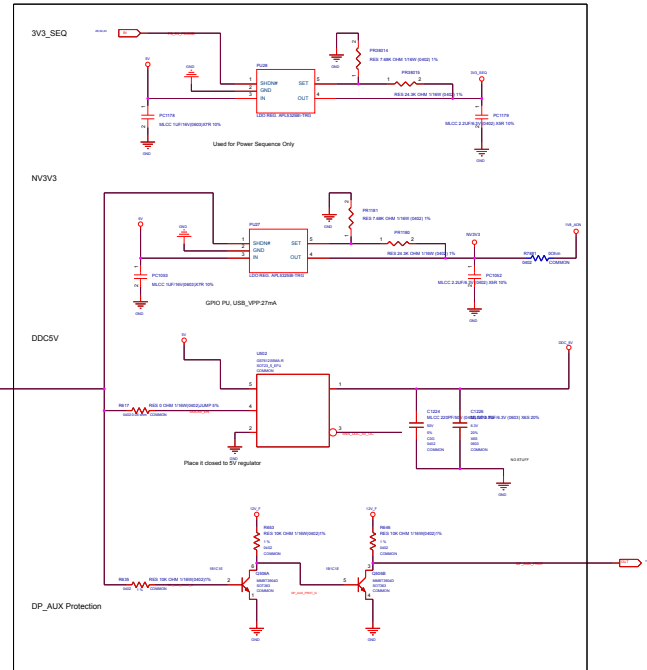
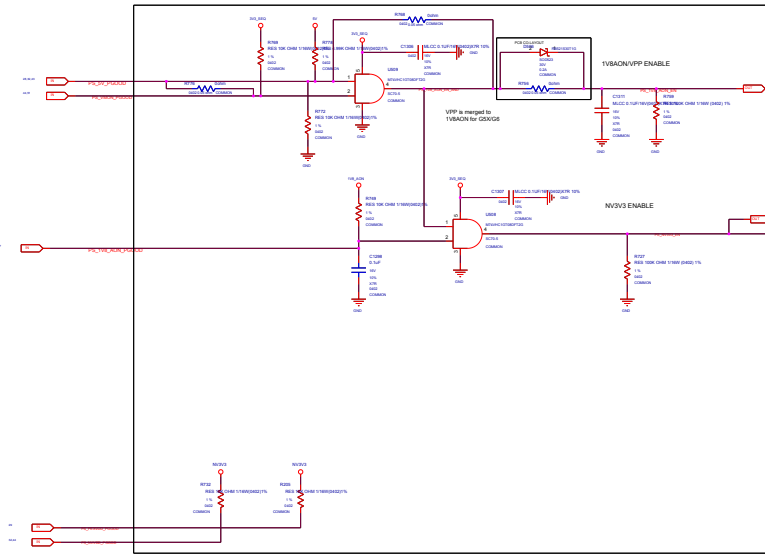




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REVISION	DESCRIPTION
1.0	INITIAL RELEASE

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6000 SHILOH ROAD			
SANTA CLARA, CA 95051 USA		NVIDIA PART NUMBER: 600-1G161-BASE-000	
REV. 1.0	1/15/2010	DATE	2/10/2010
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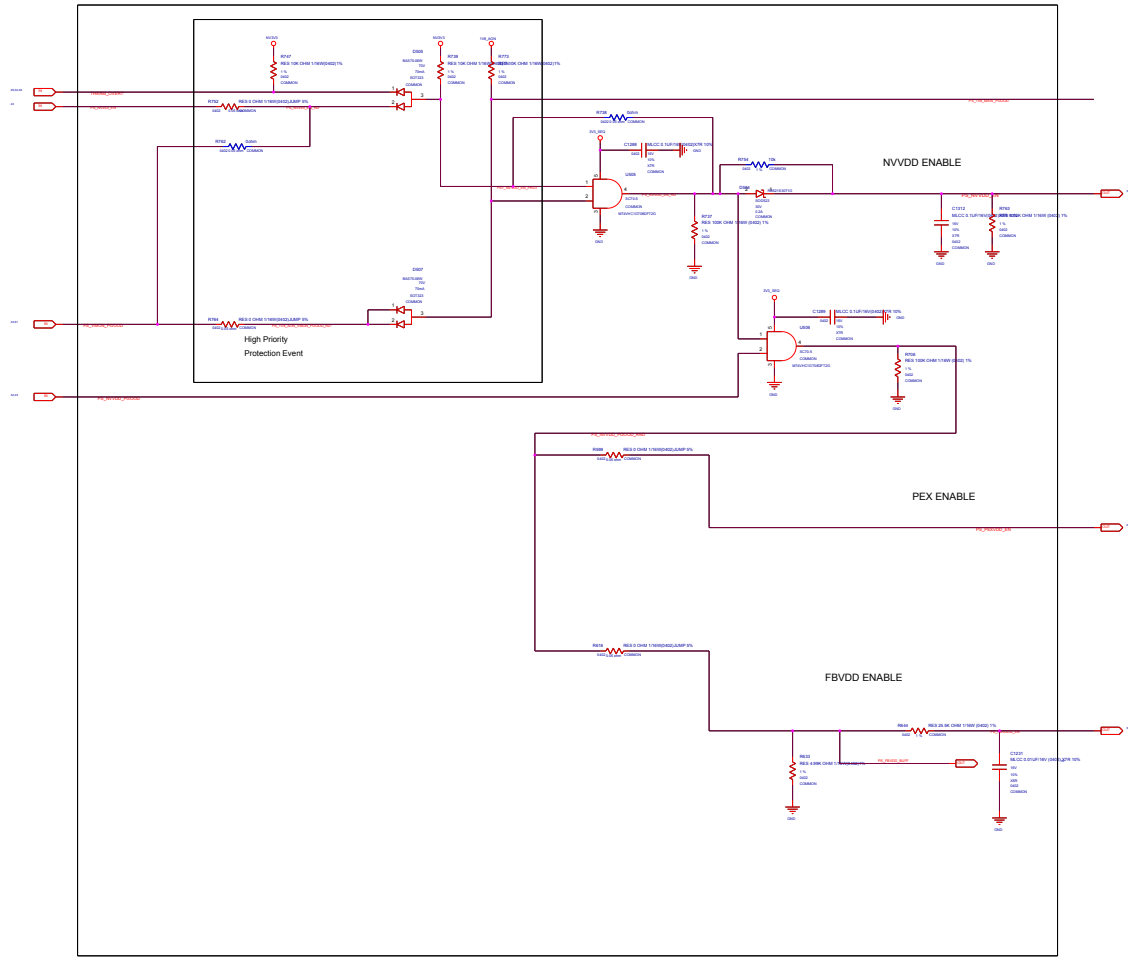


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NV_P/N	800-1G161-BASE-000	REV	42 OF 52
PCB REV	00000000000000000000	DATE	00000000000000000000
DOC REV	00000000000000000000	DATE	00000000000000000000





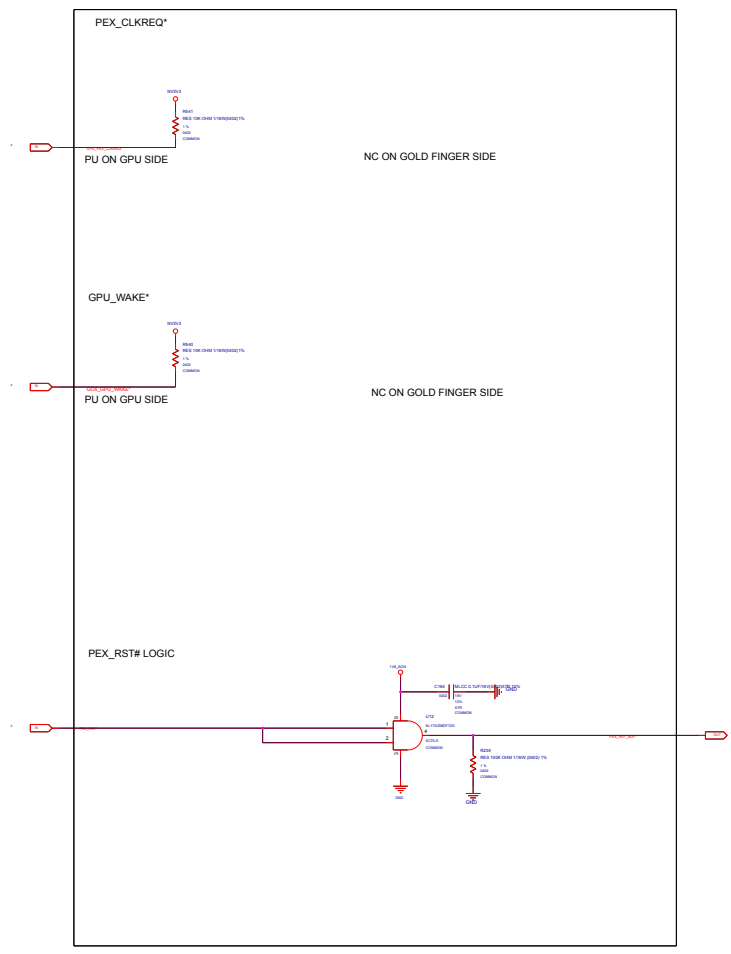
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ASSIGNMENT	ASSIGNMENT DESCRIPTION
FIGURE 44-1	SEQ NV PEX FB ENABLE

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001	21-OCT-2018		



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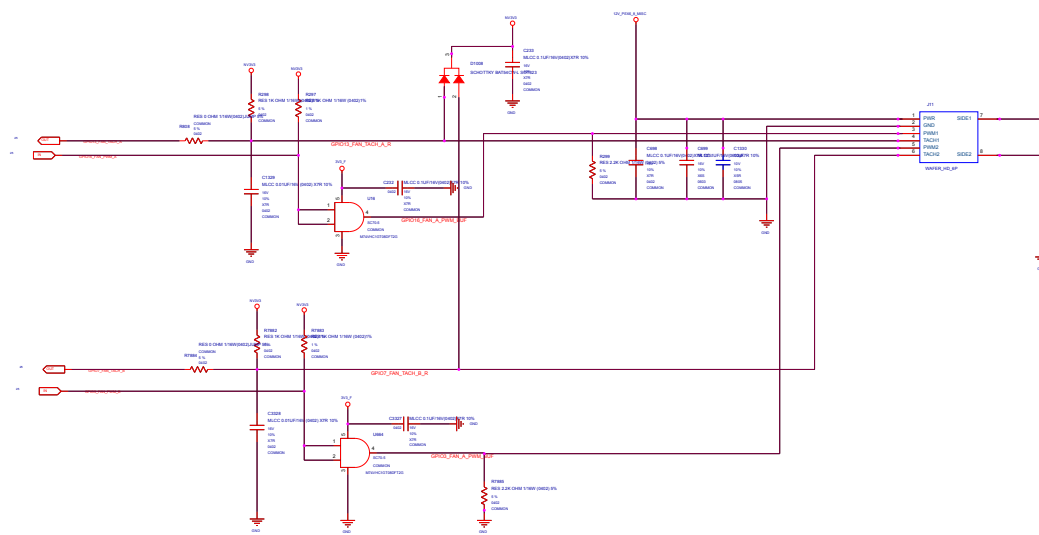
ASSEMBLY	DESCRIPTION
PEX SIGNAL	GPU SIDE

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1.0	01/14/14


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 PEX_PN: 600-1G161-BASE-000
 REV: 1.0
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ASSEMBLY	DESCRIPTION

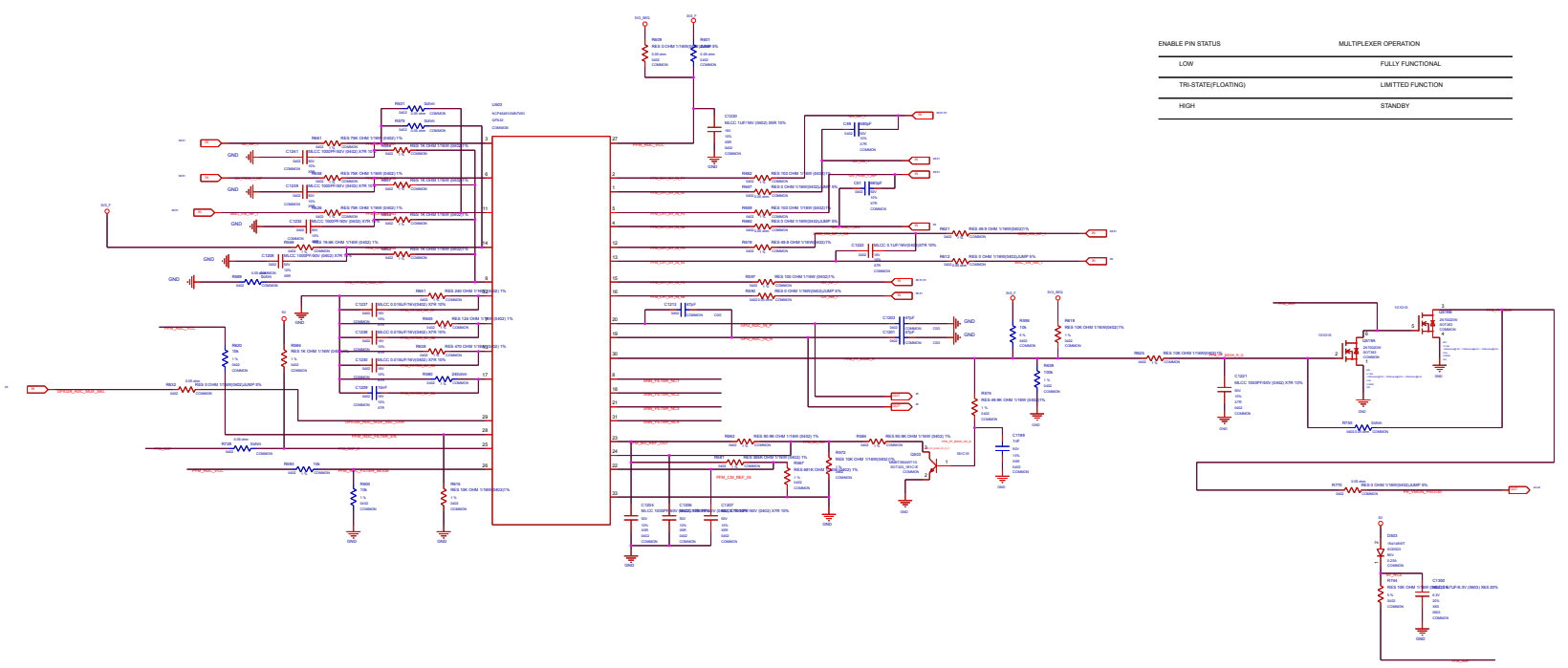
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NV_P/N	800-1G181-BASE-000	REV	REV 01
REV	1.0	DATE	07/01/2018


MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



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