

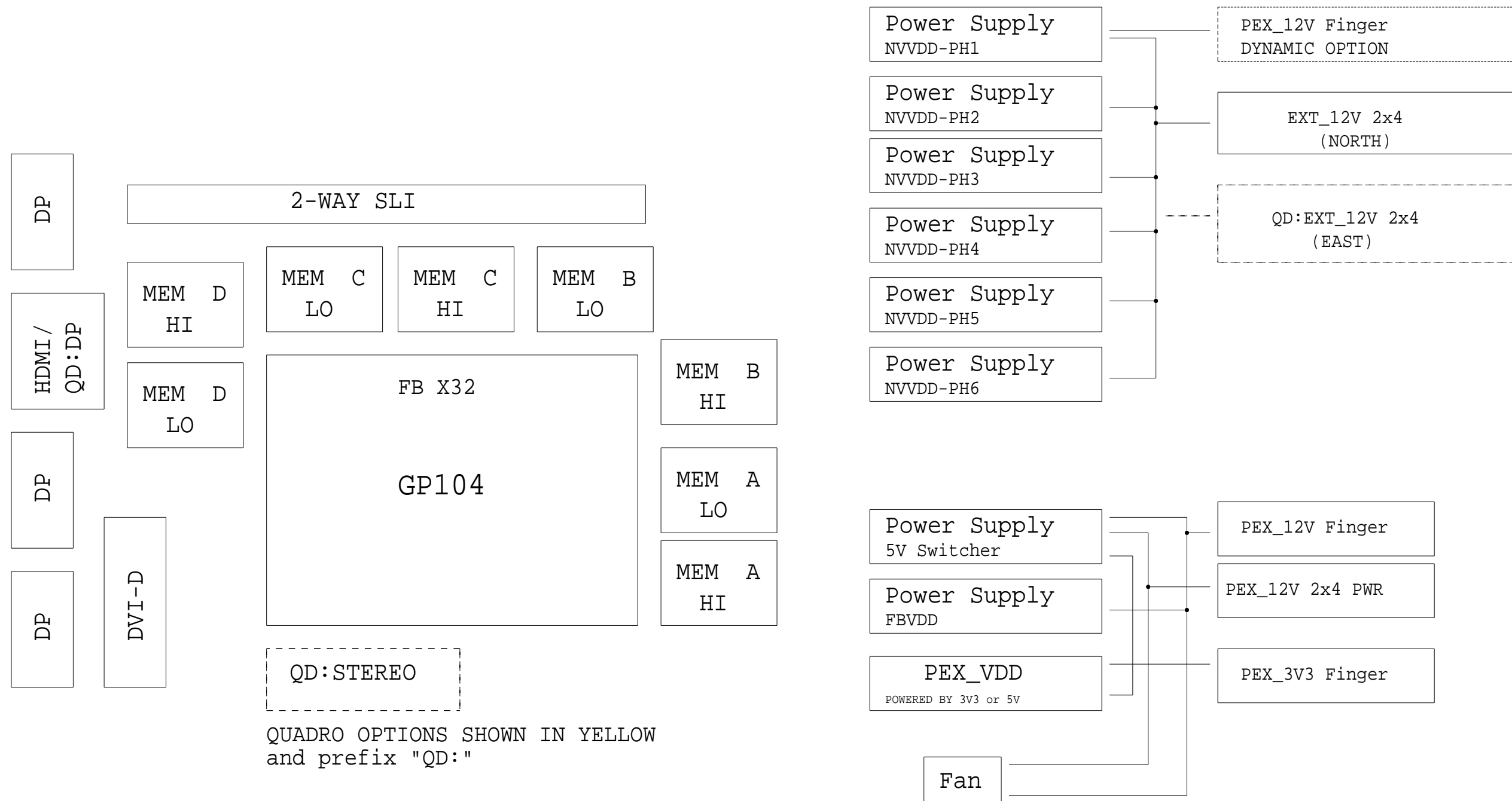
PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

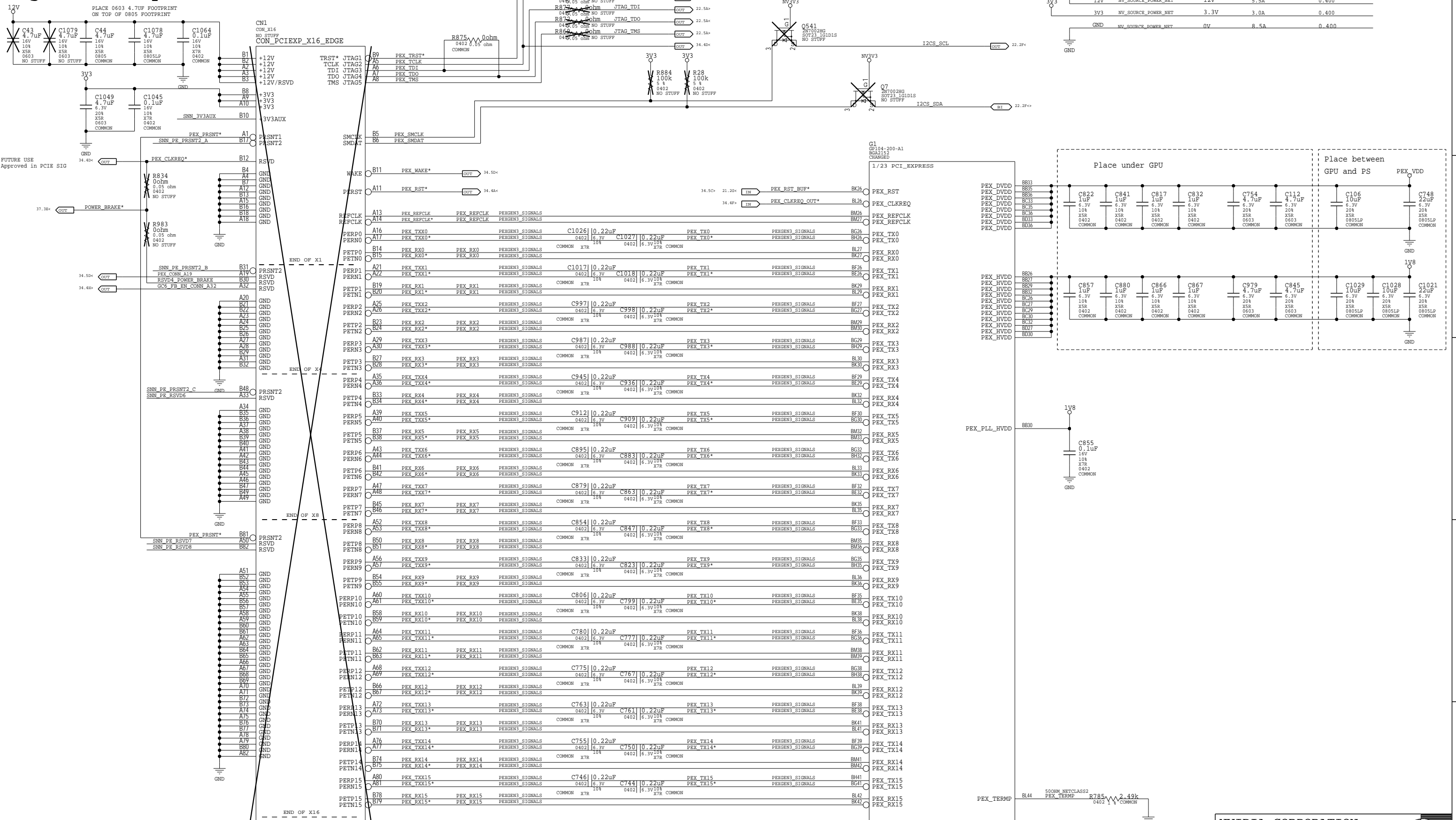
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QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

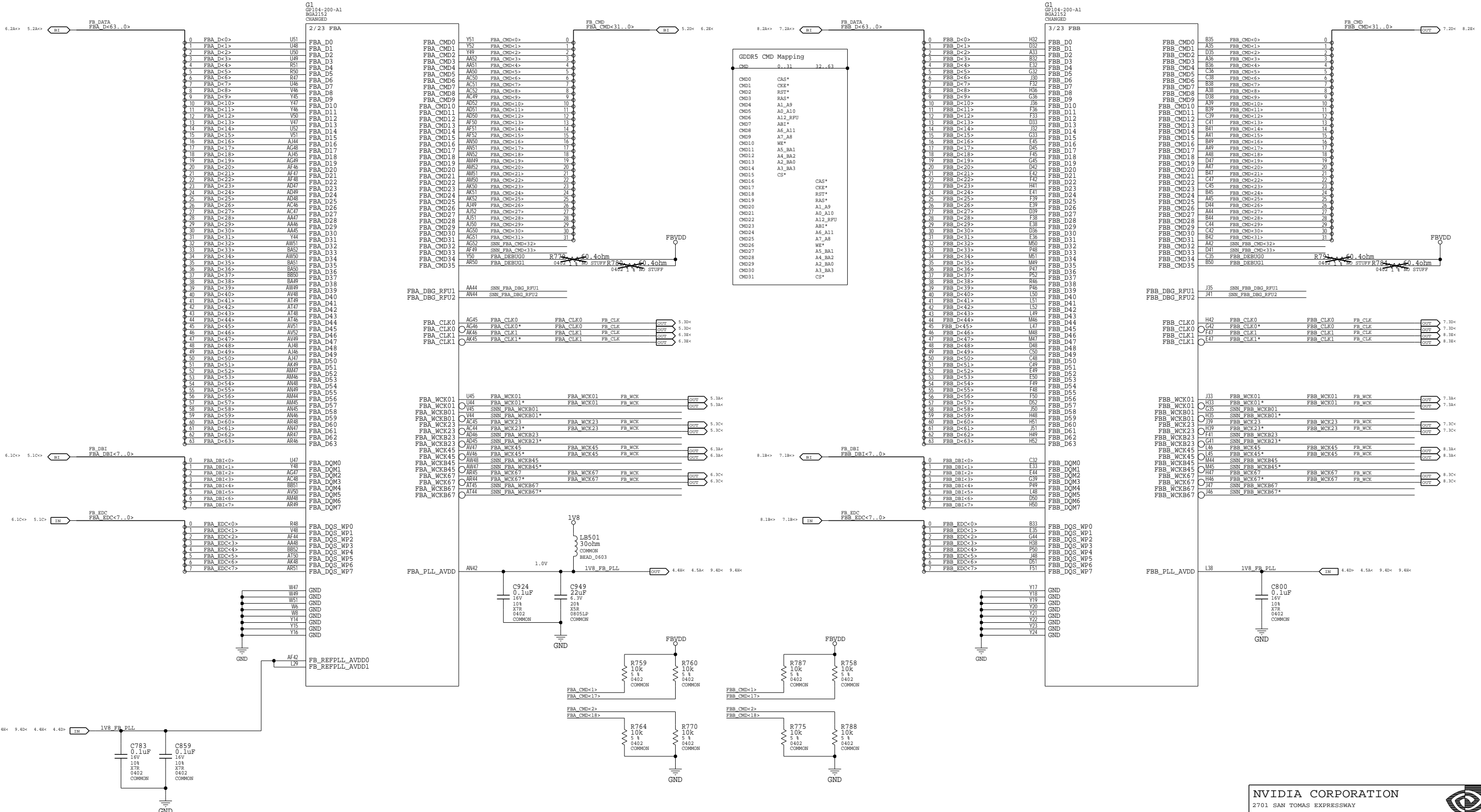


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ASSEMBLY SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL PCI Express

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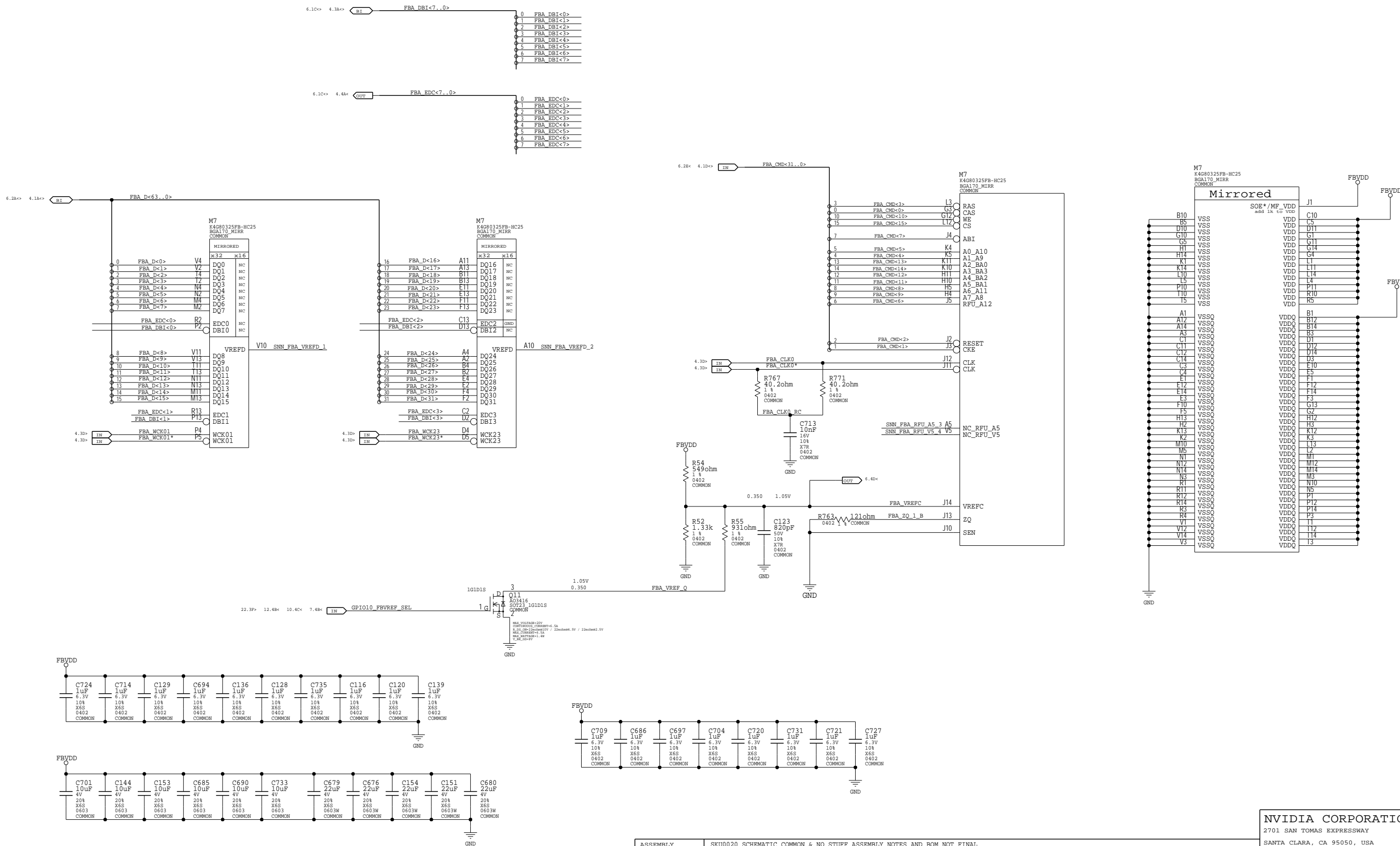


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ASSEMBLY: SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL: MEMORY: GPU Partition A/B

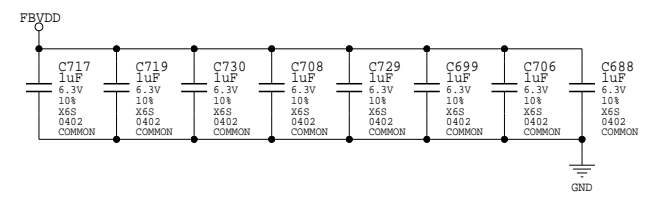
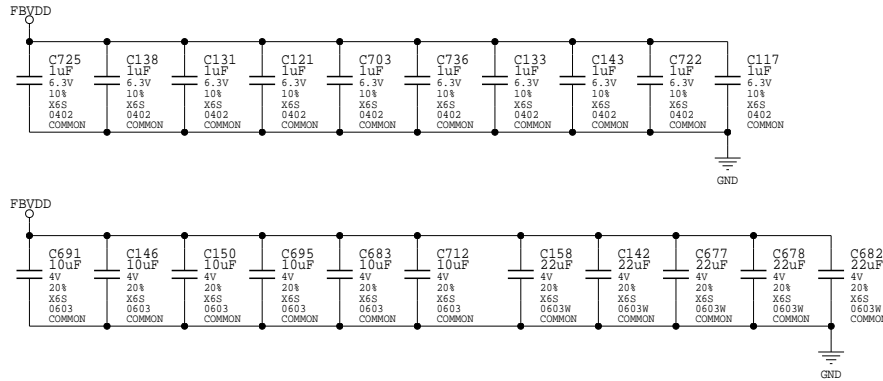
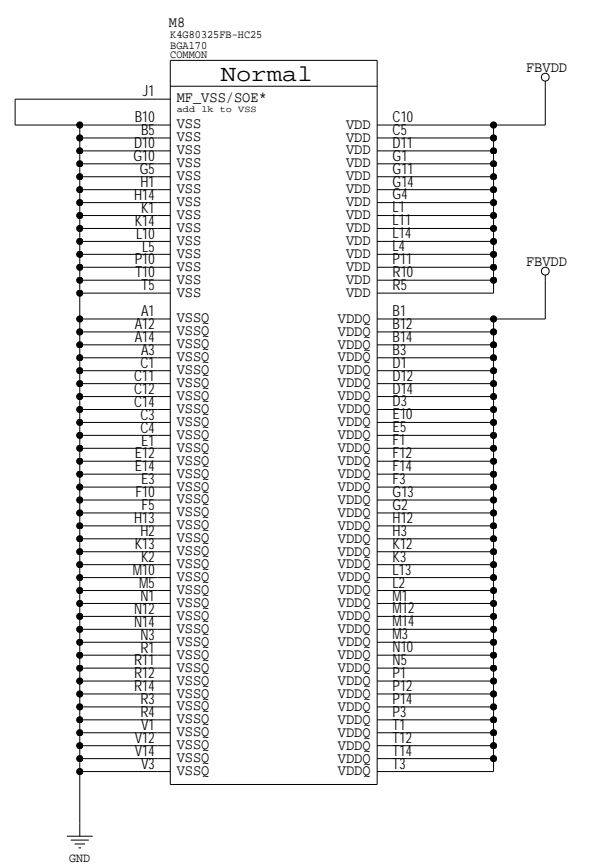
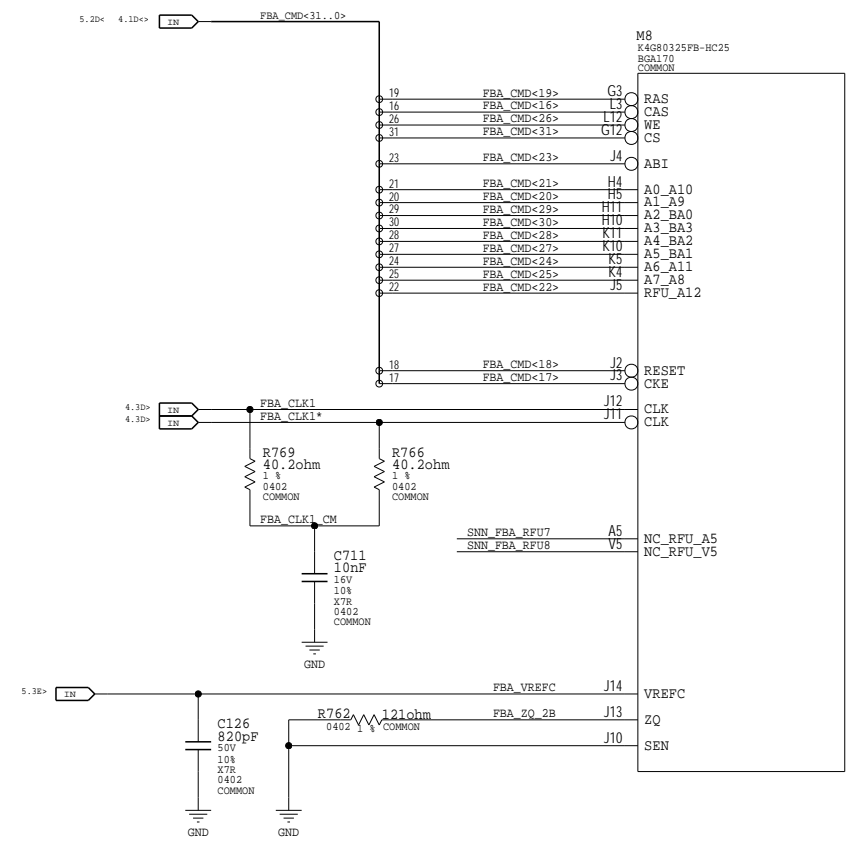
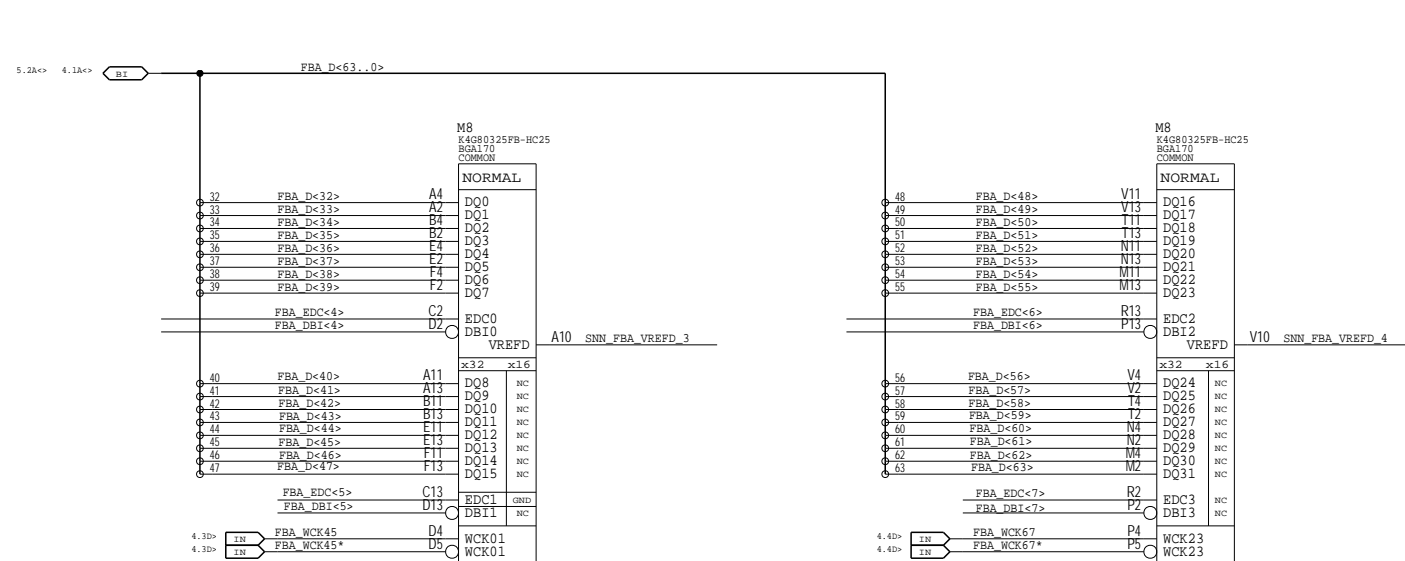
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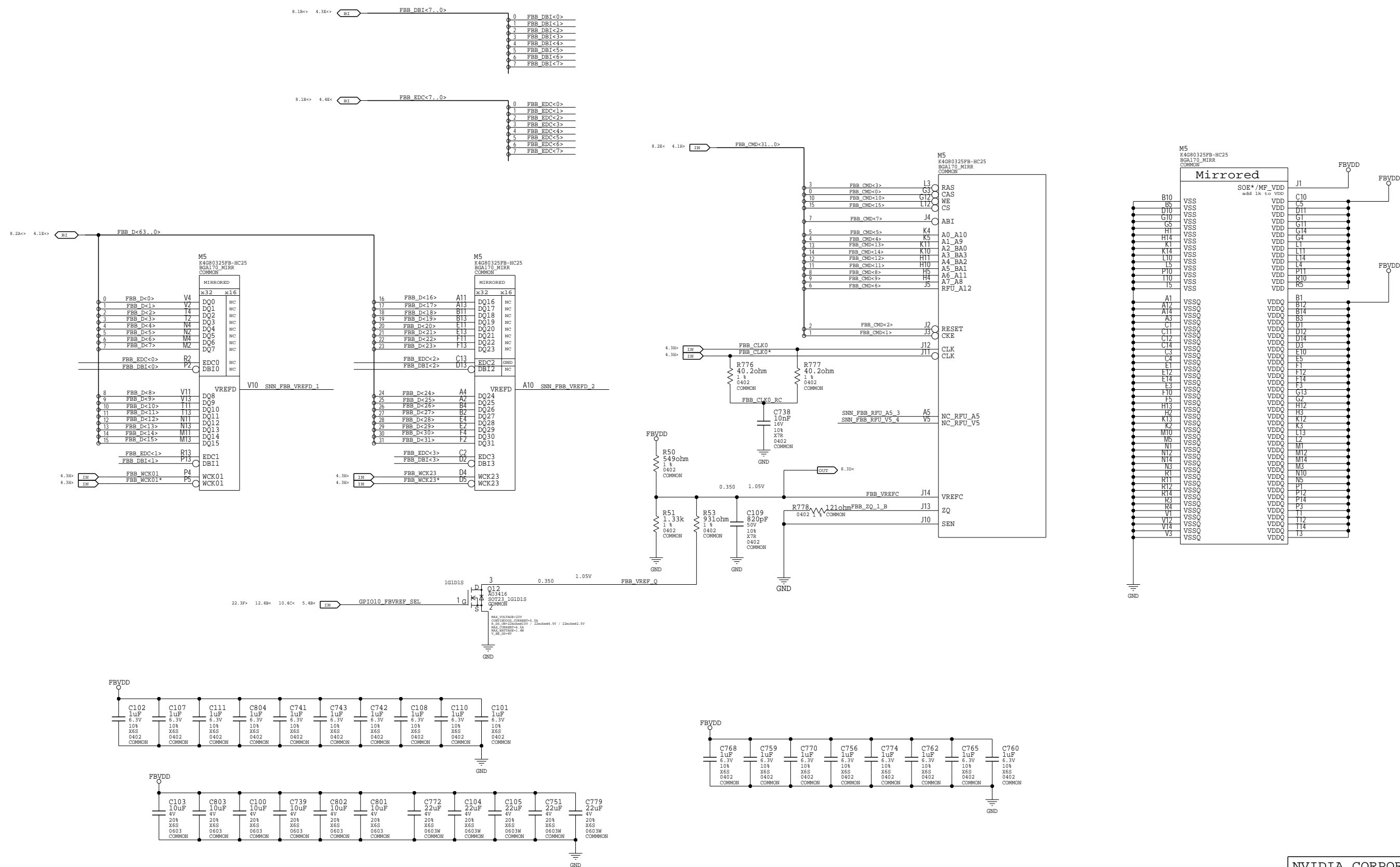
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 PAGE DETAIL MEMORY: FBA[31:0]



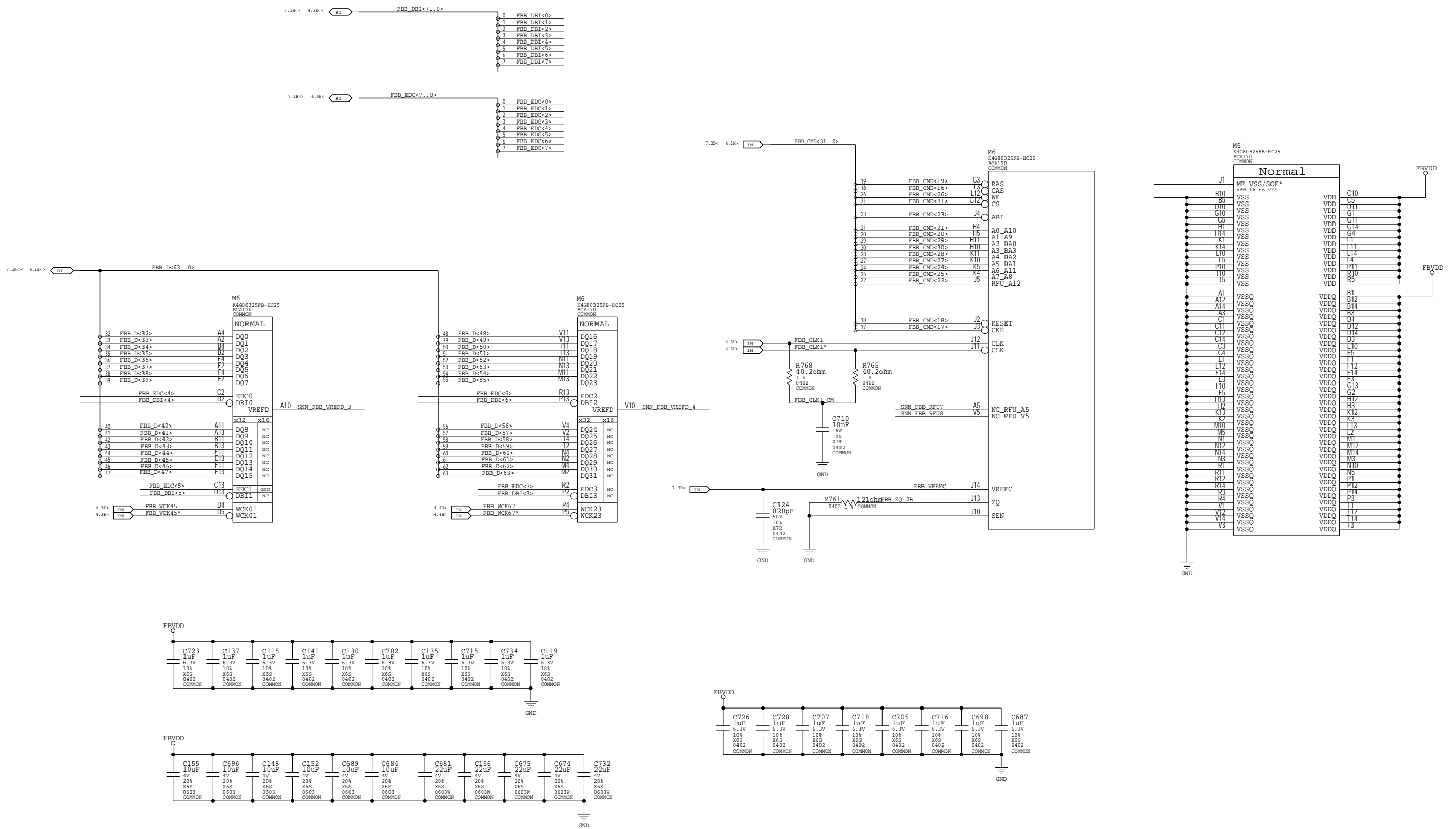


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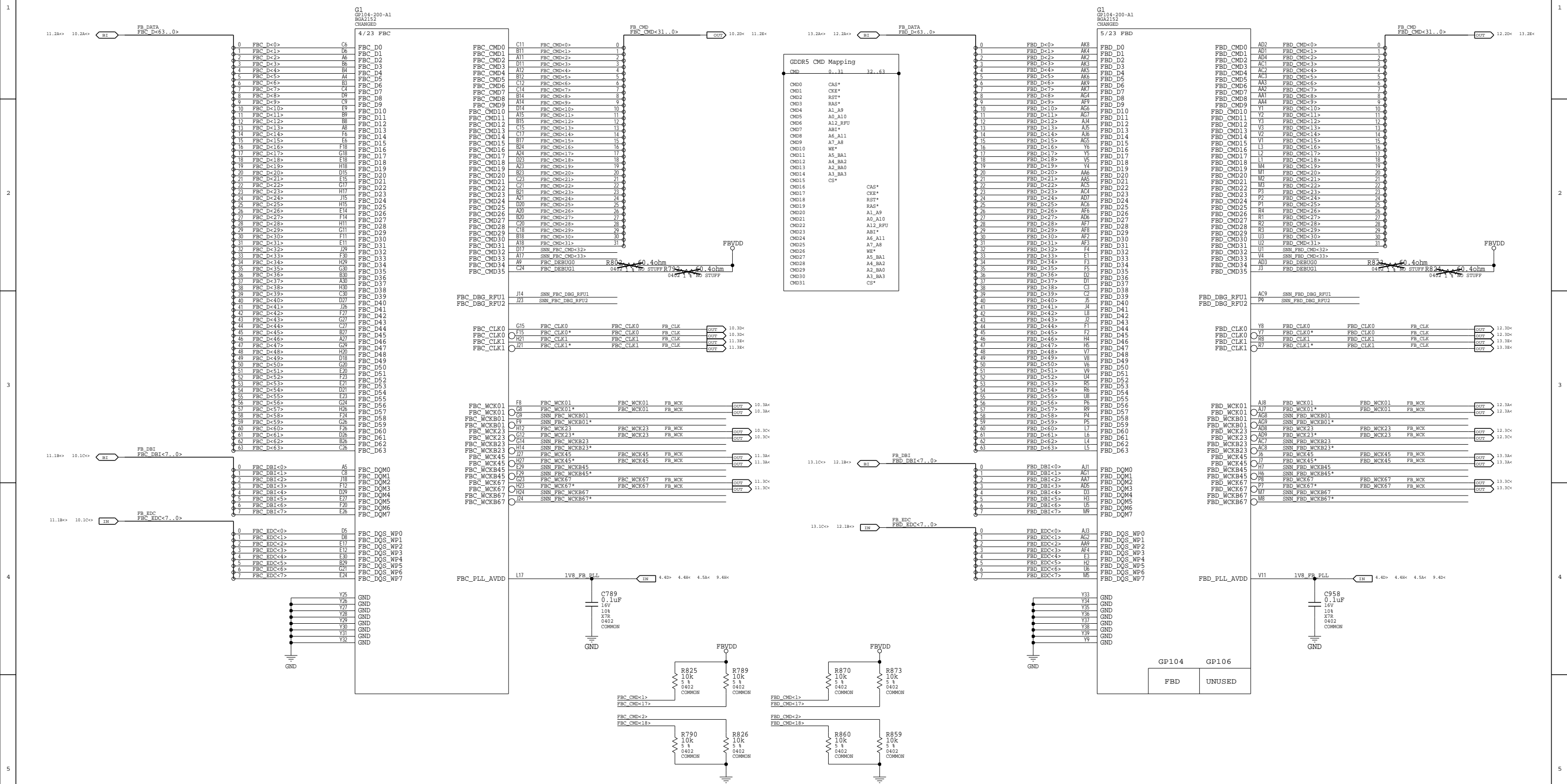
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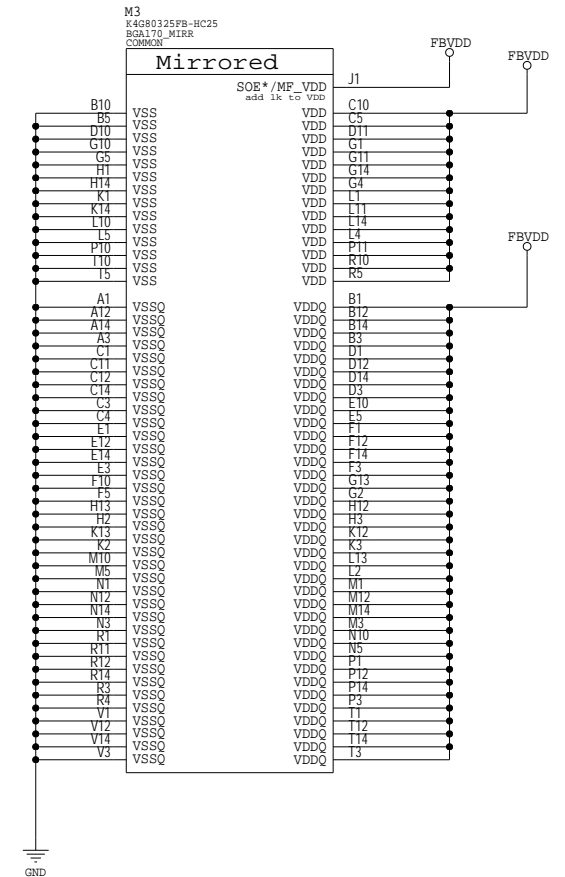
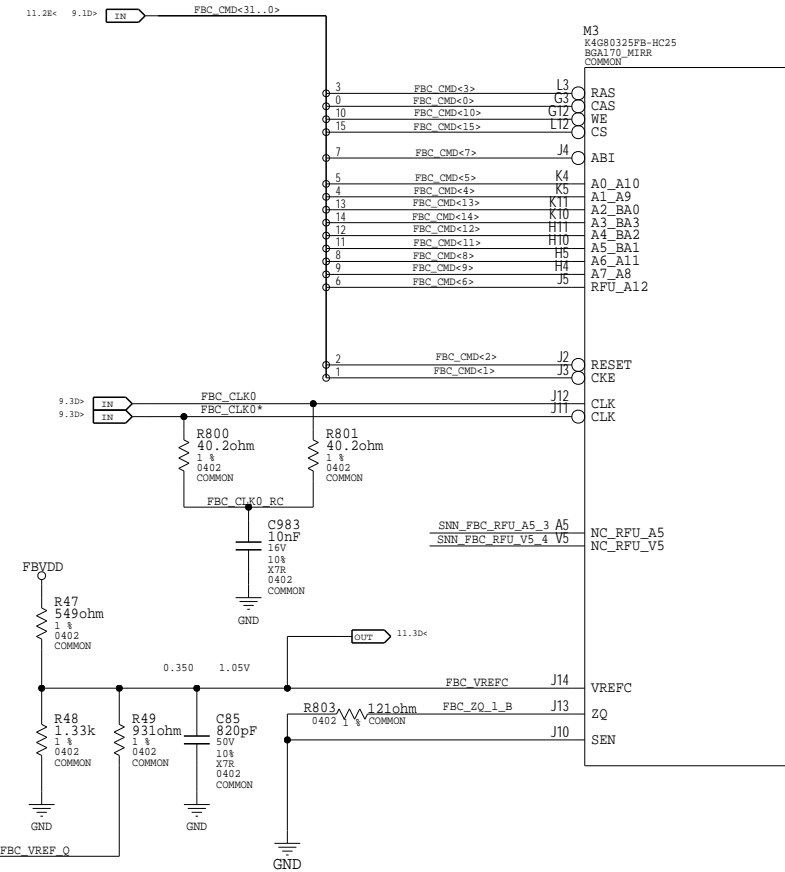
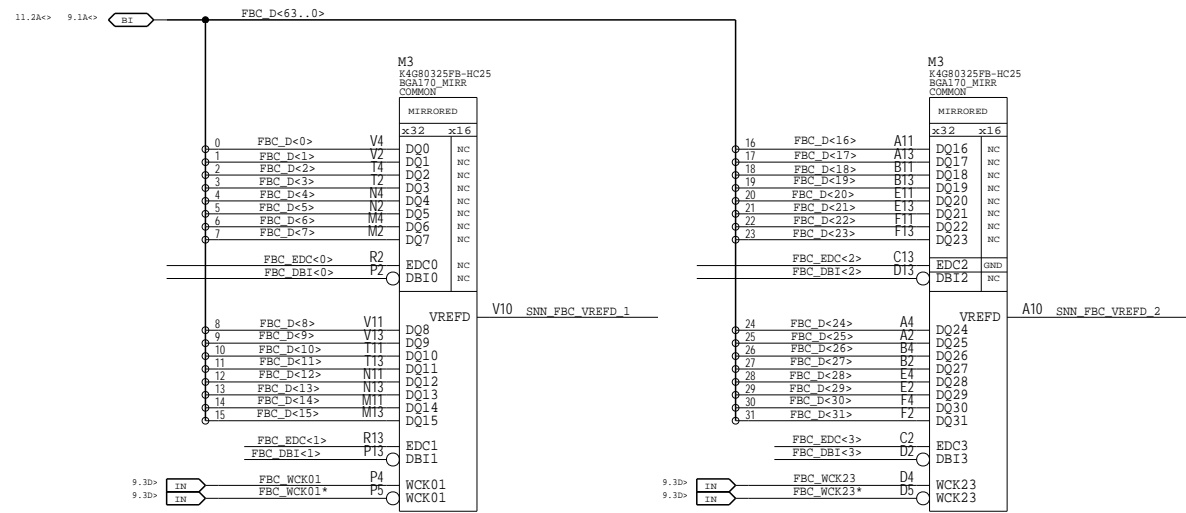
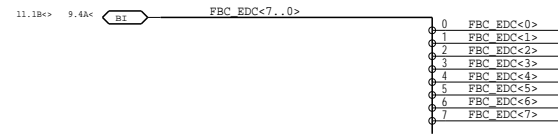
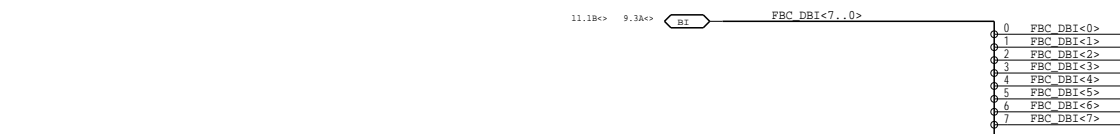
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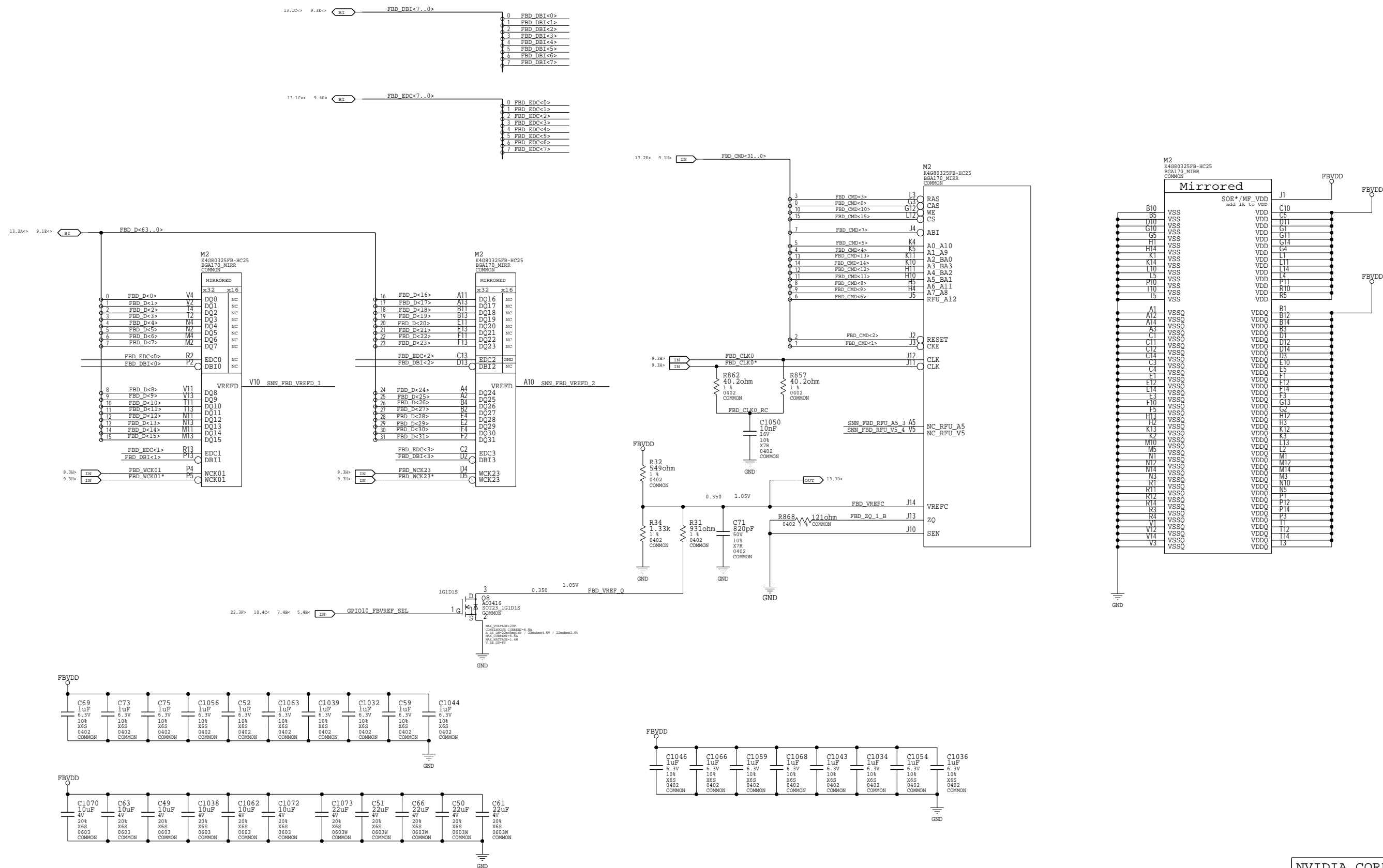
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 PCB REV: 1G411-A01
 BOM REV: B

ASSEMBLY: SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL: MEMORY: GPU Partition C/D

DATE: 30-JUN-2016

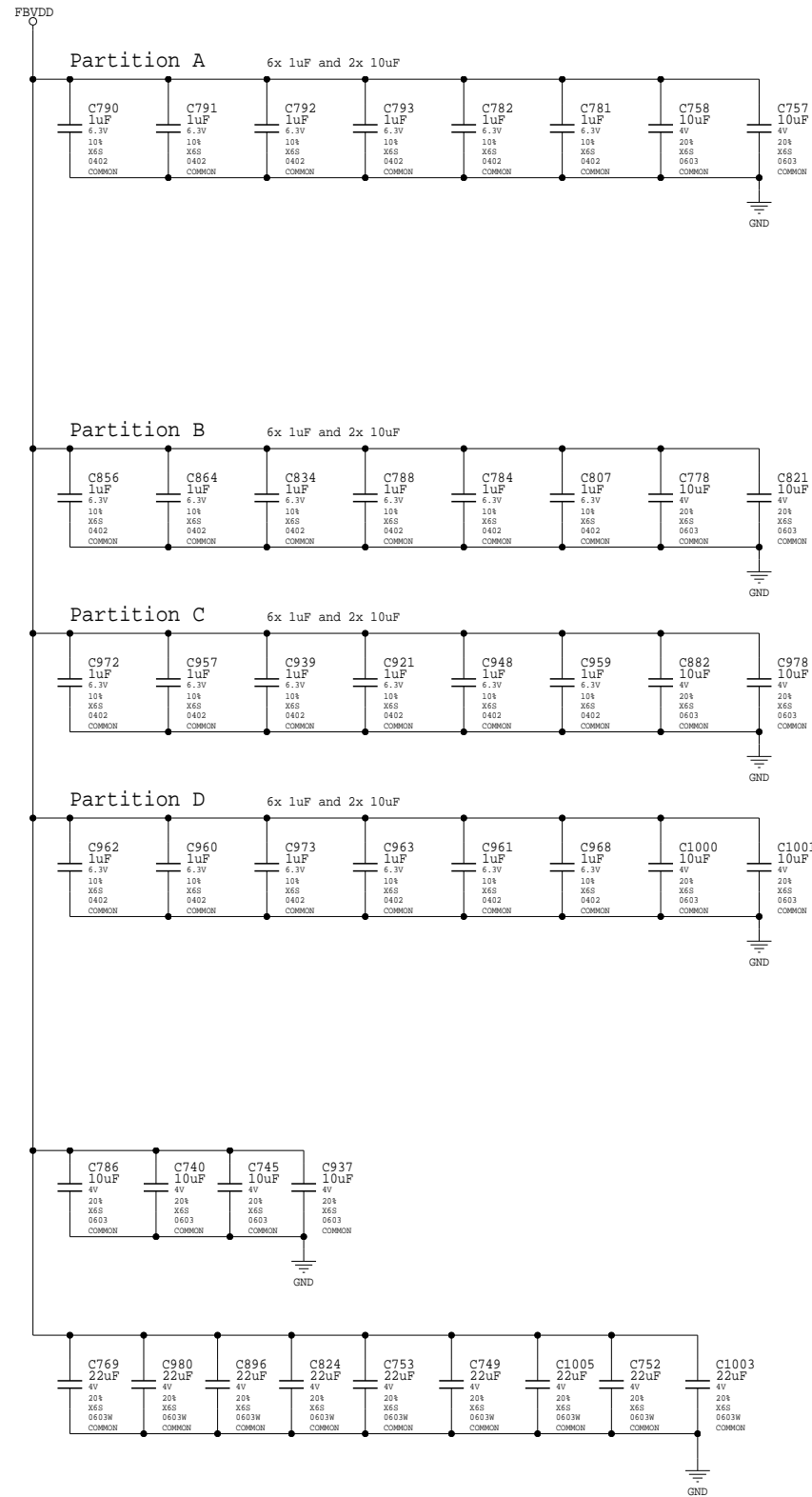
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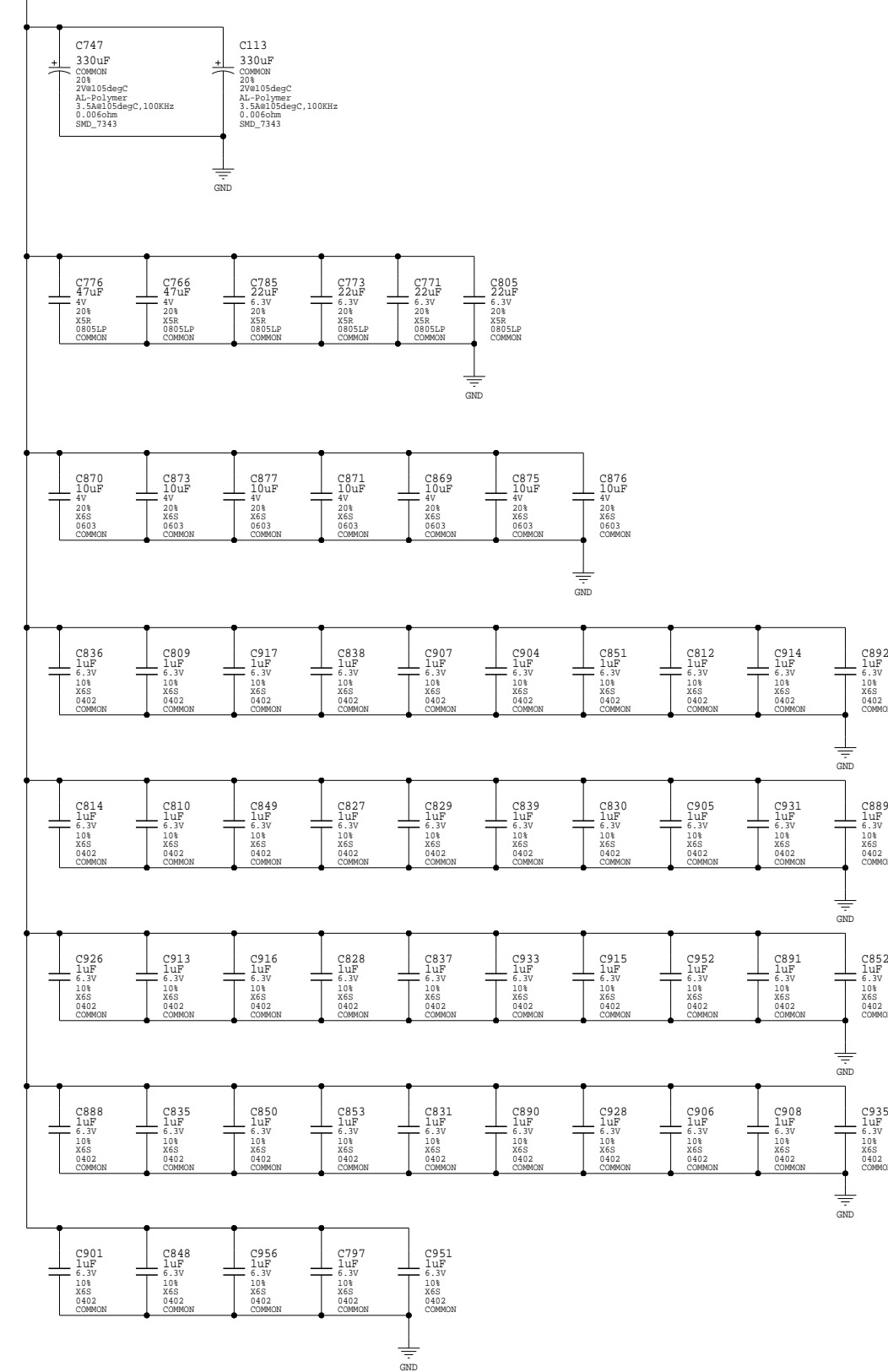


Page15: GPU Decoupling

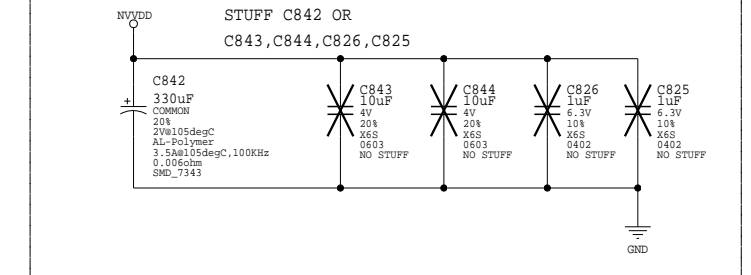
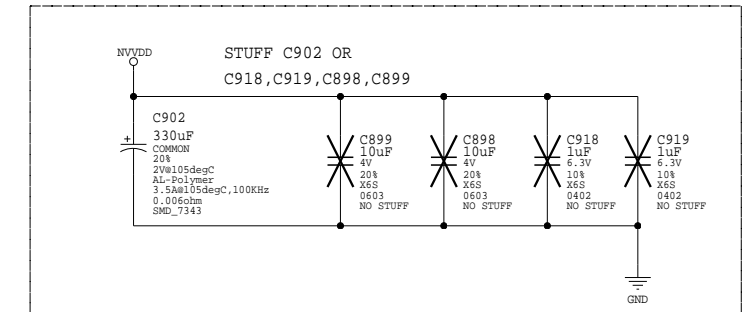
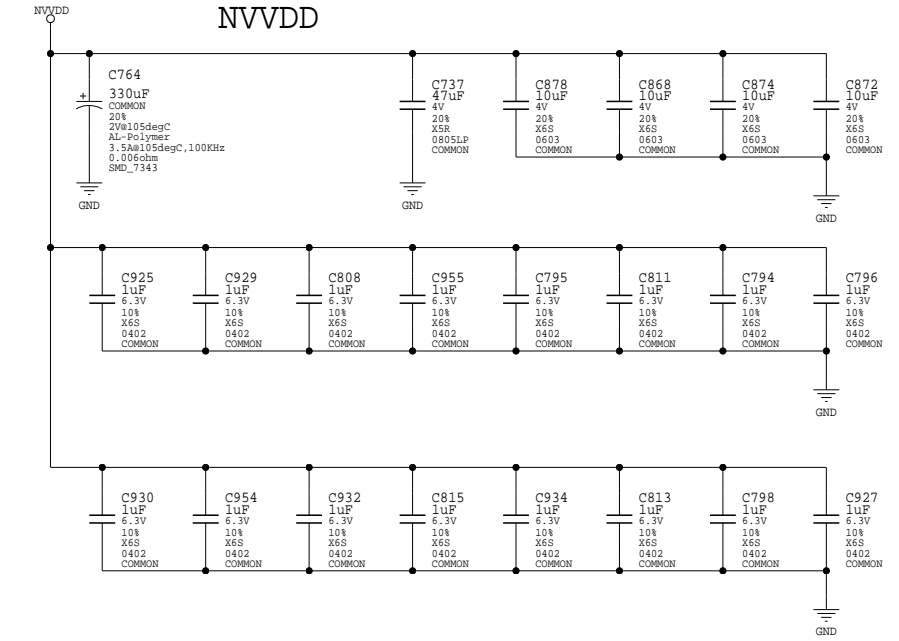
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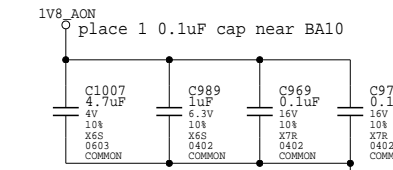
NVVDD



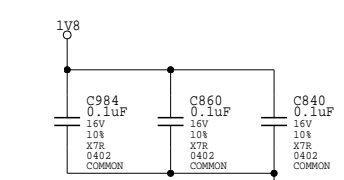
NVVDD



1V8_AON



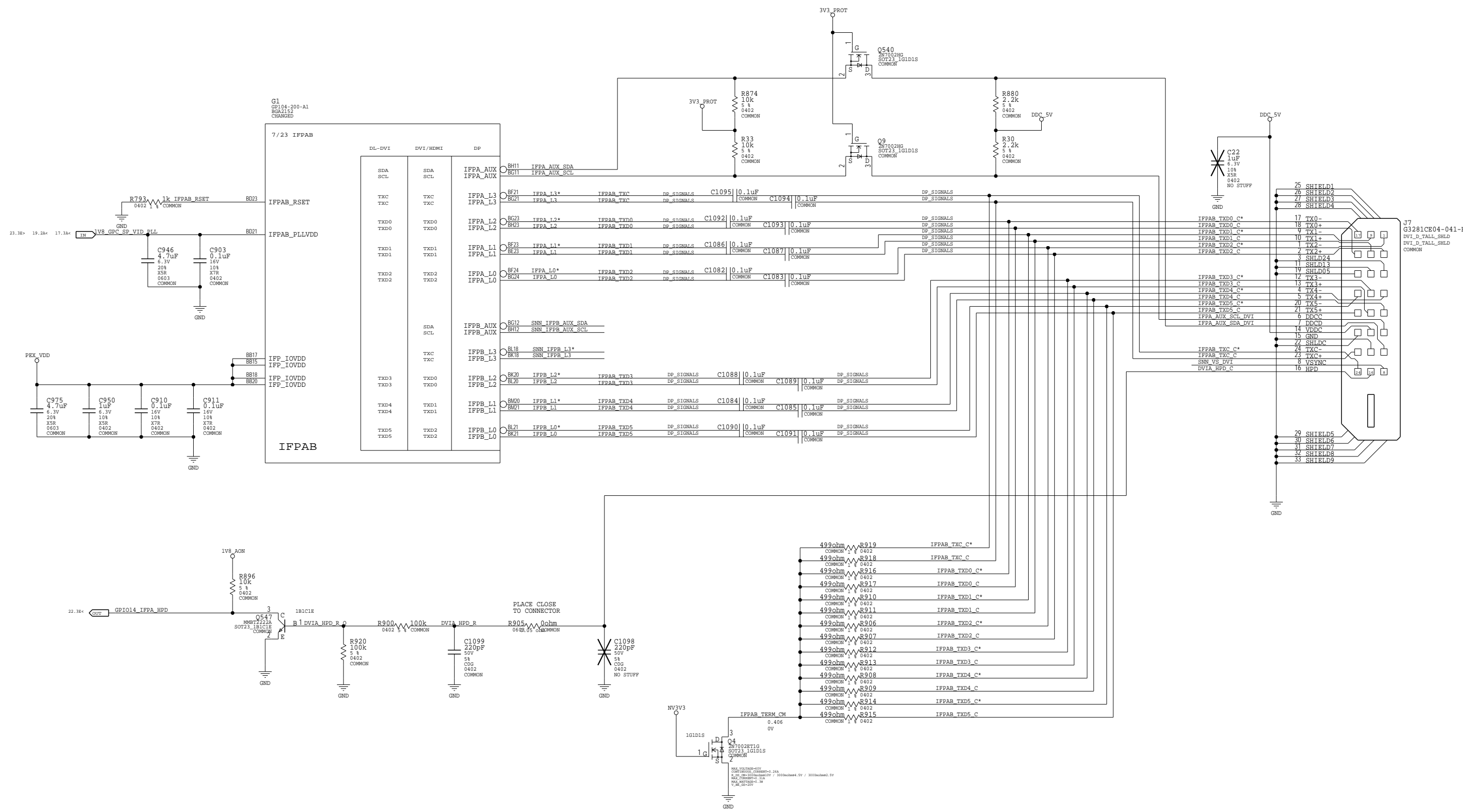
VDD18



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PAGE DETAIL GPU Decoupling

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NV_PN 600-1G411-0020-110 PCB REV 1G411-A01 BOM REV B			
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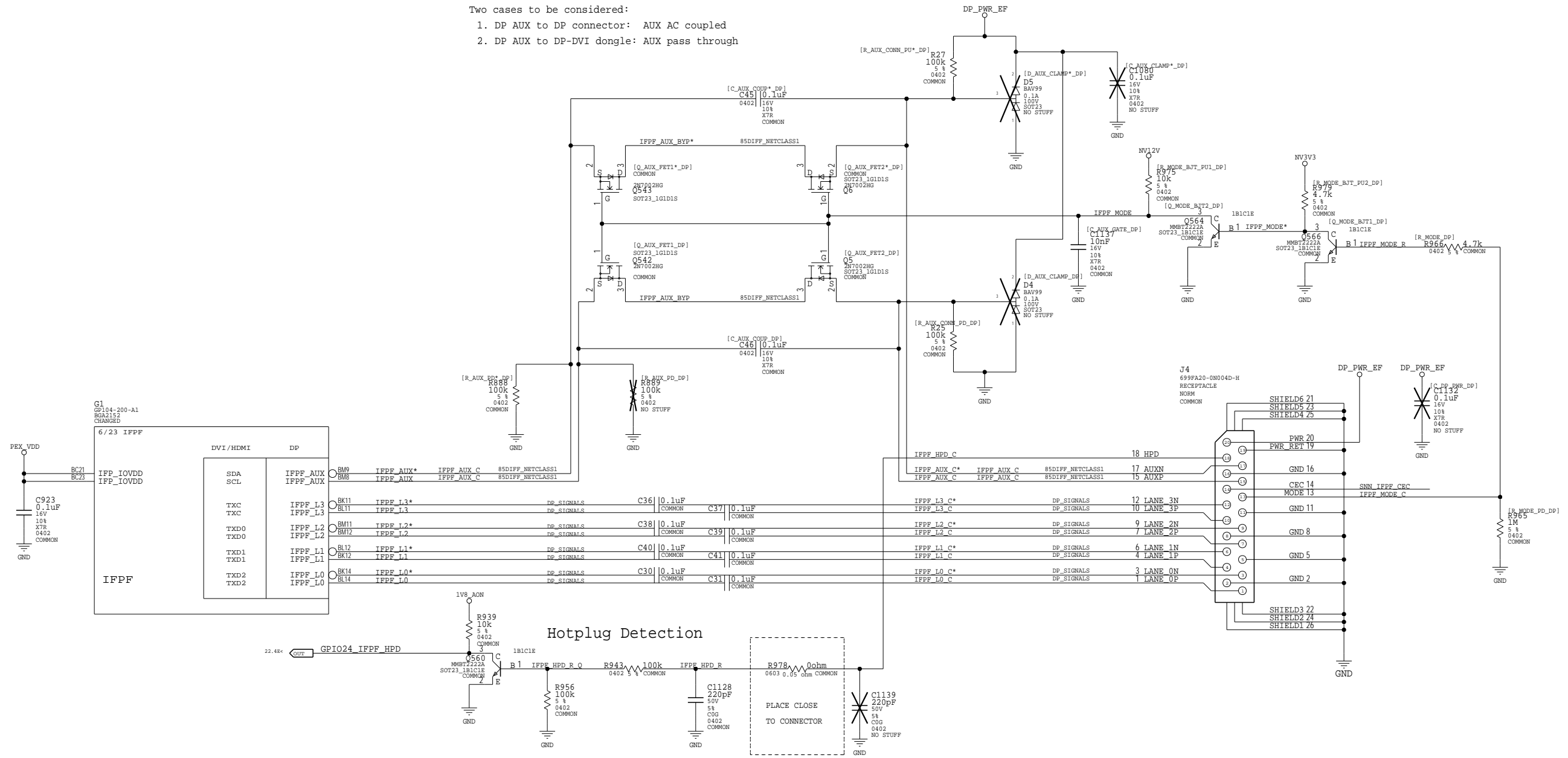
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PAGE DETAIL	IFPAB DVI-D-DL



- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

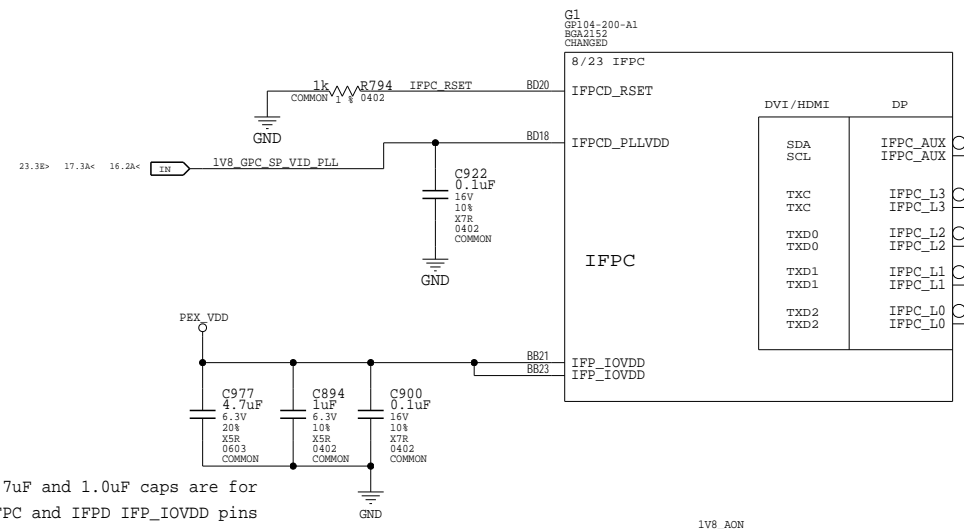
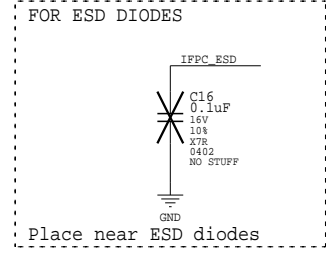


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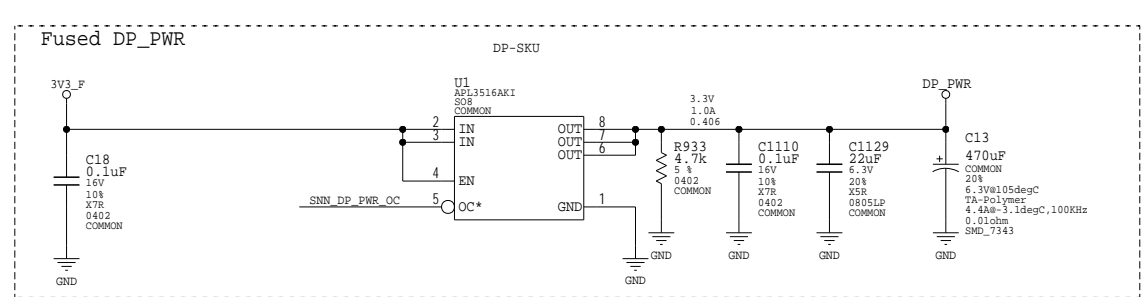
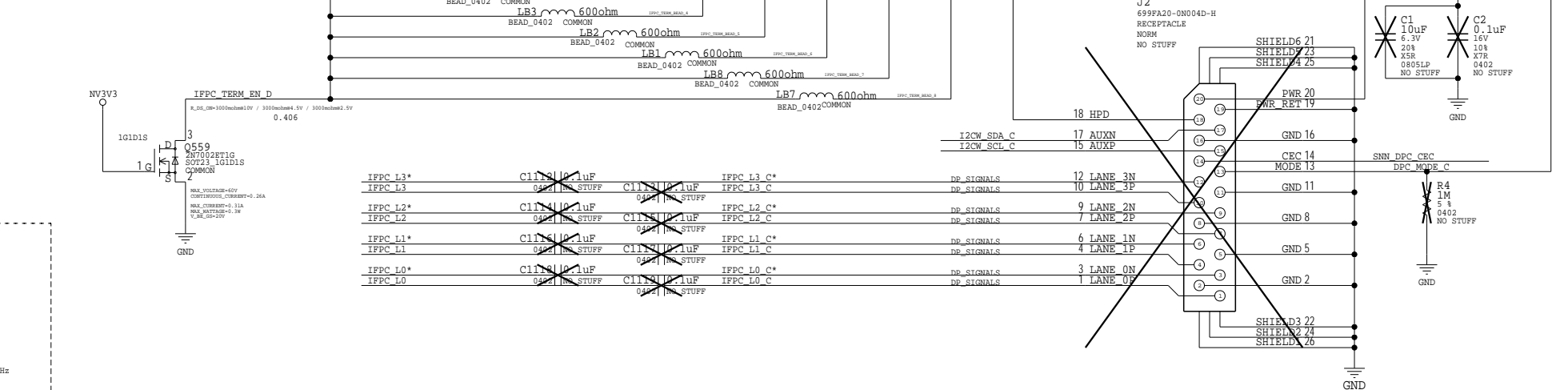
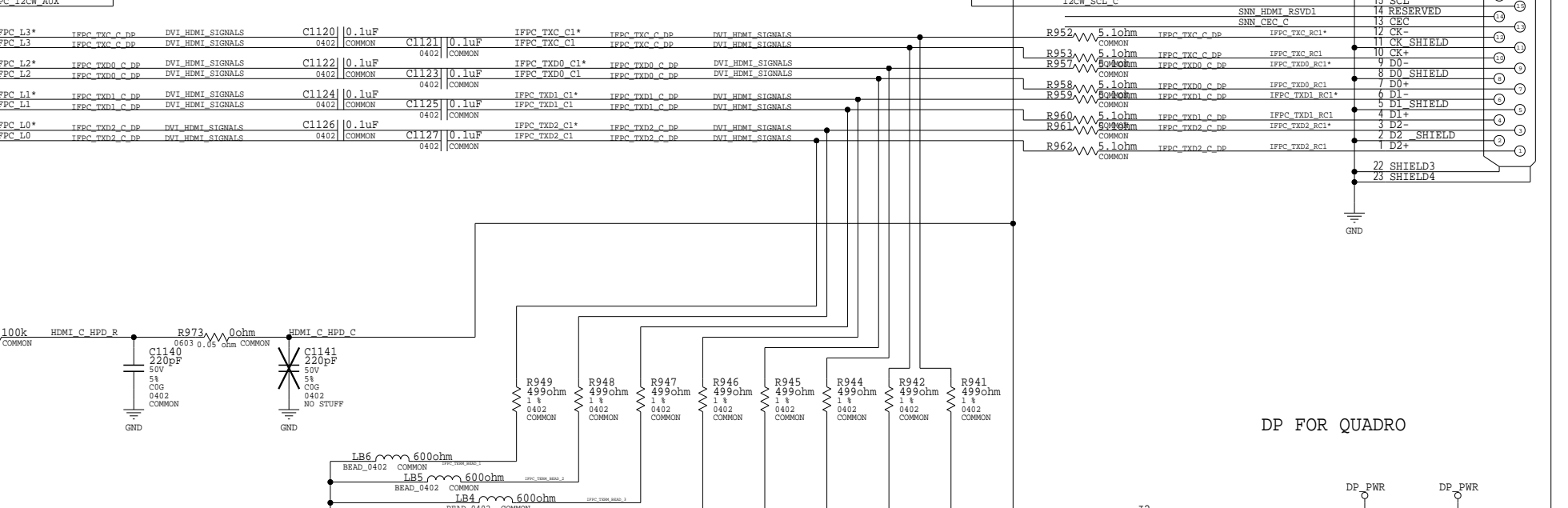
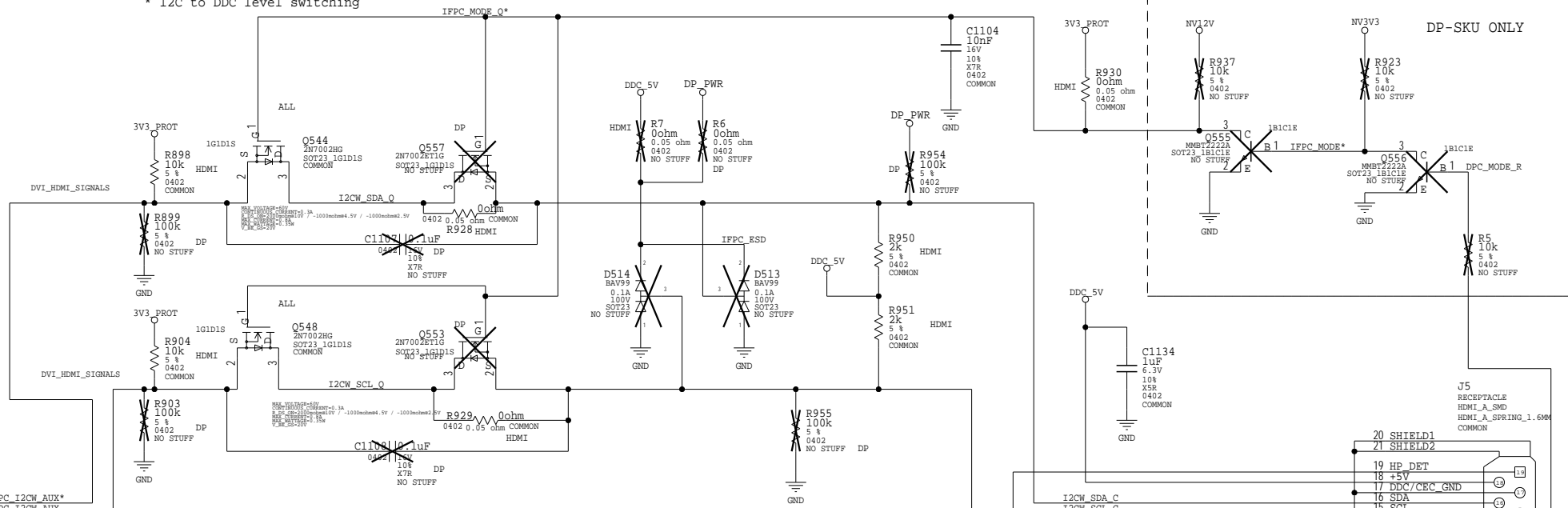
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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPF DP

* I2C to DDC level switching



4.7uF and 1.0uF caps are for IFPC and IFPD IFP_IOVDD pins

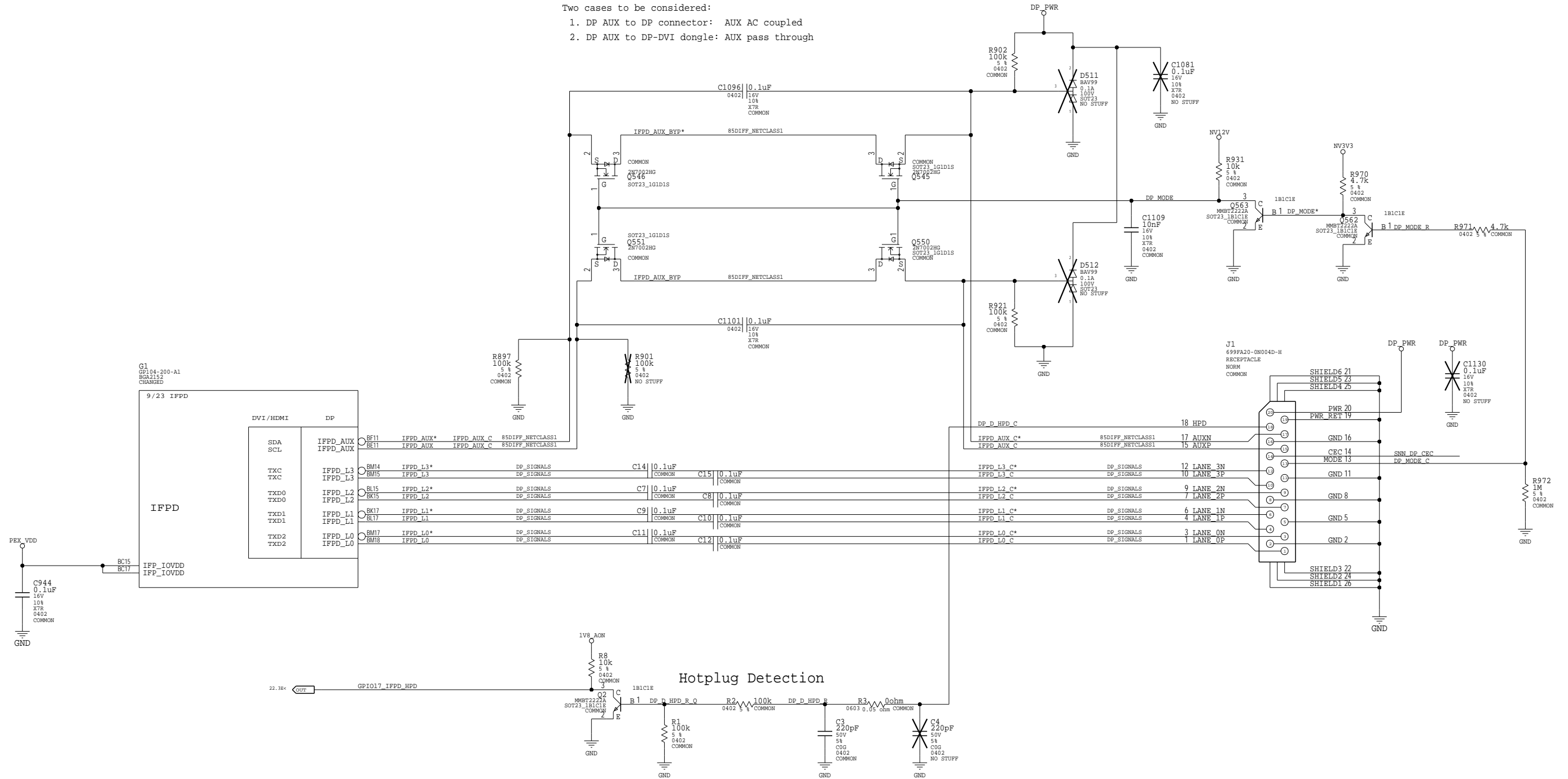


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PAGE DETAIL IFPC HDMI 2.0/DP

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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
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PAGE DETAIL		IFPD DP	
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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	CFG[2:0]
L	L	L	000
L	H	L	001
L	H	L	010
L	H	H	011
H	H	L	110
H	H	H	111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

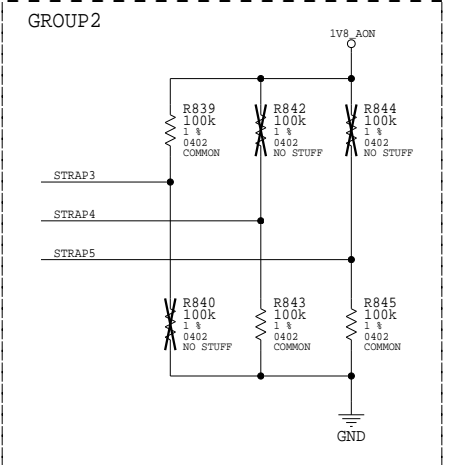
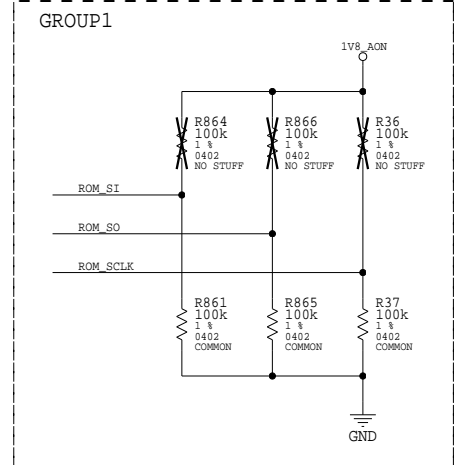
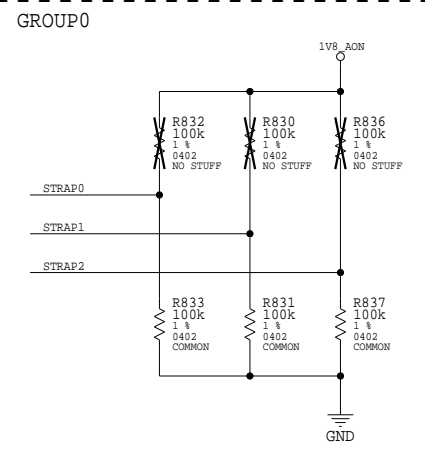
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

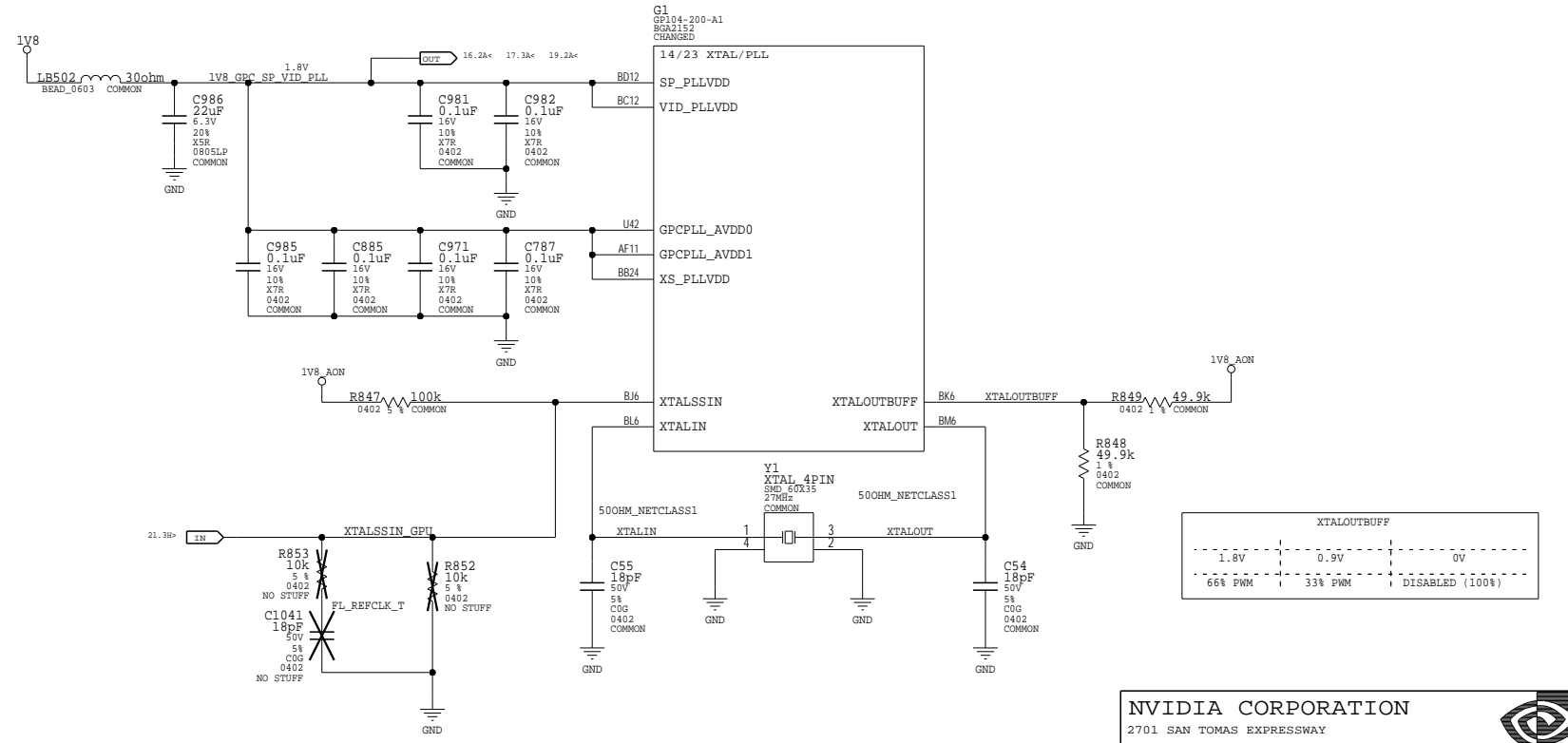
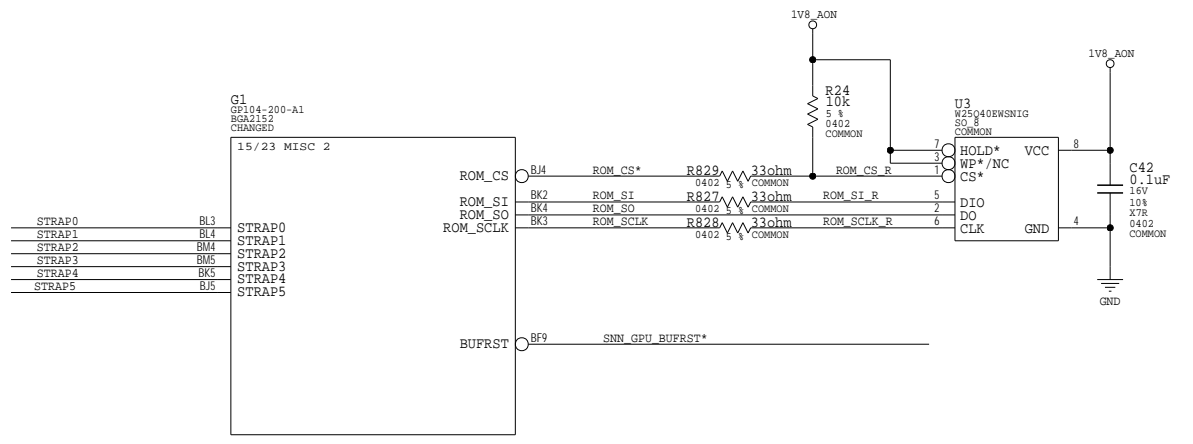
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[2:0]	Config	Width	Vendor
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001	256Mx32	256-bit	Micron
010	256Mx32	256-bit	Hynix
011	Reserved		
100	Reserved		
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111	Reserved		



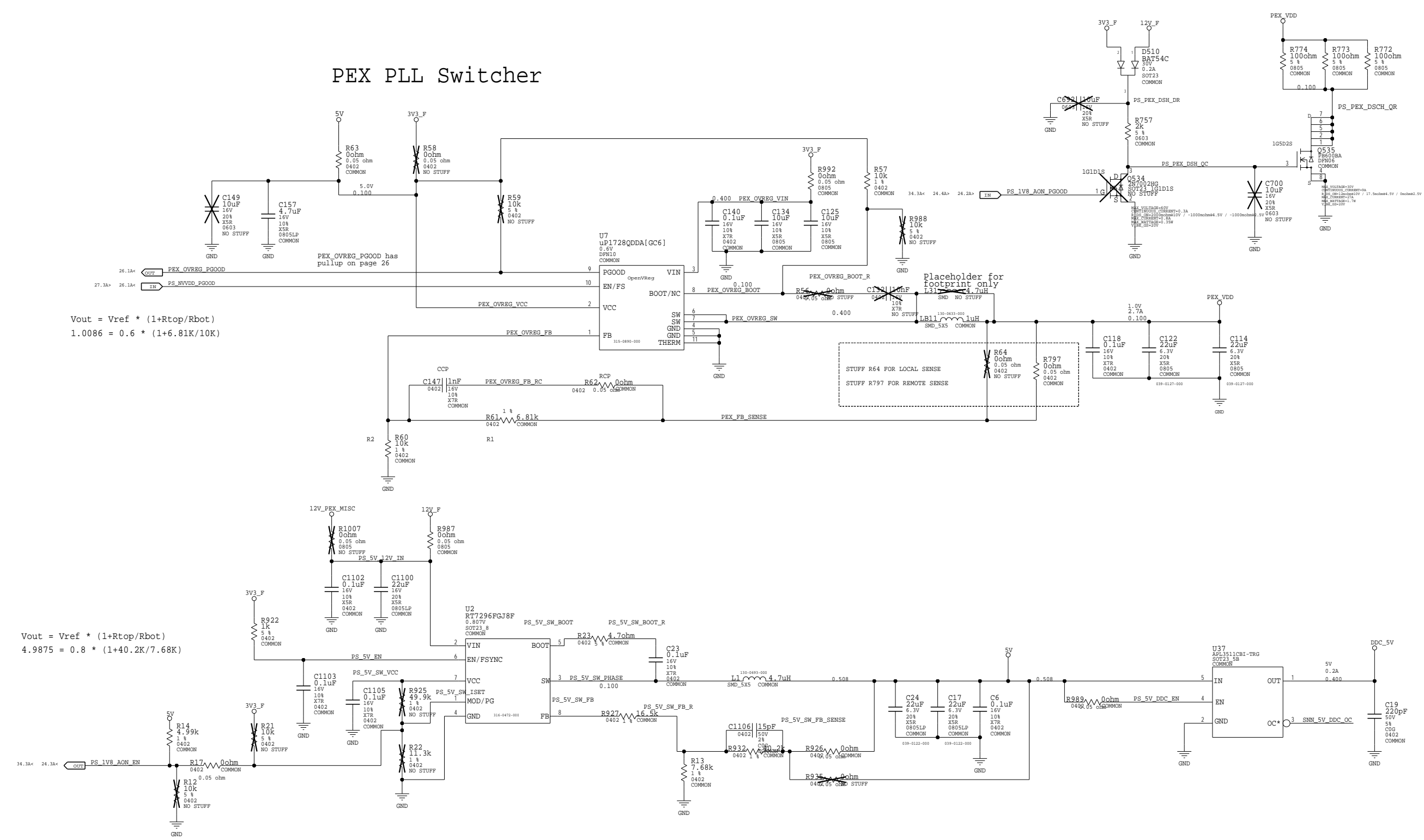
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NV_PN: 600-1G411-0020-110
PCB REV: 1G411-A01
BOM REV: B

DATE: 30-JUN-2016

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PEX PLL Switcher



$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $1.0086 = 0.6 * (1 + 6.81K/10K)$

$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $4.9875 = 0.8 * (1 + 40.2K/7.68K)$

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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: 5V, PEX_VDD

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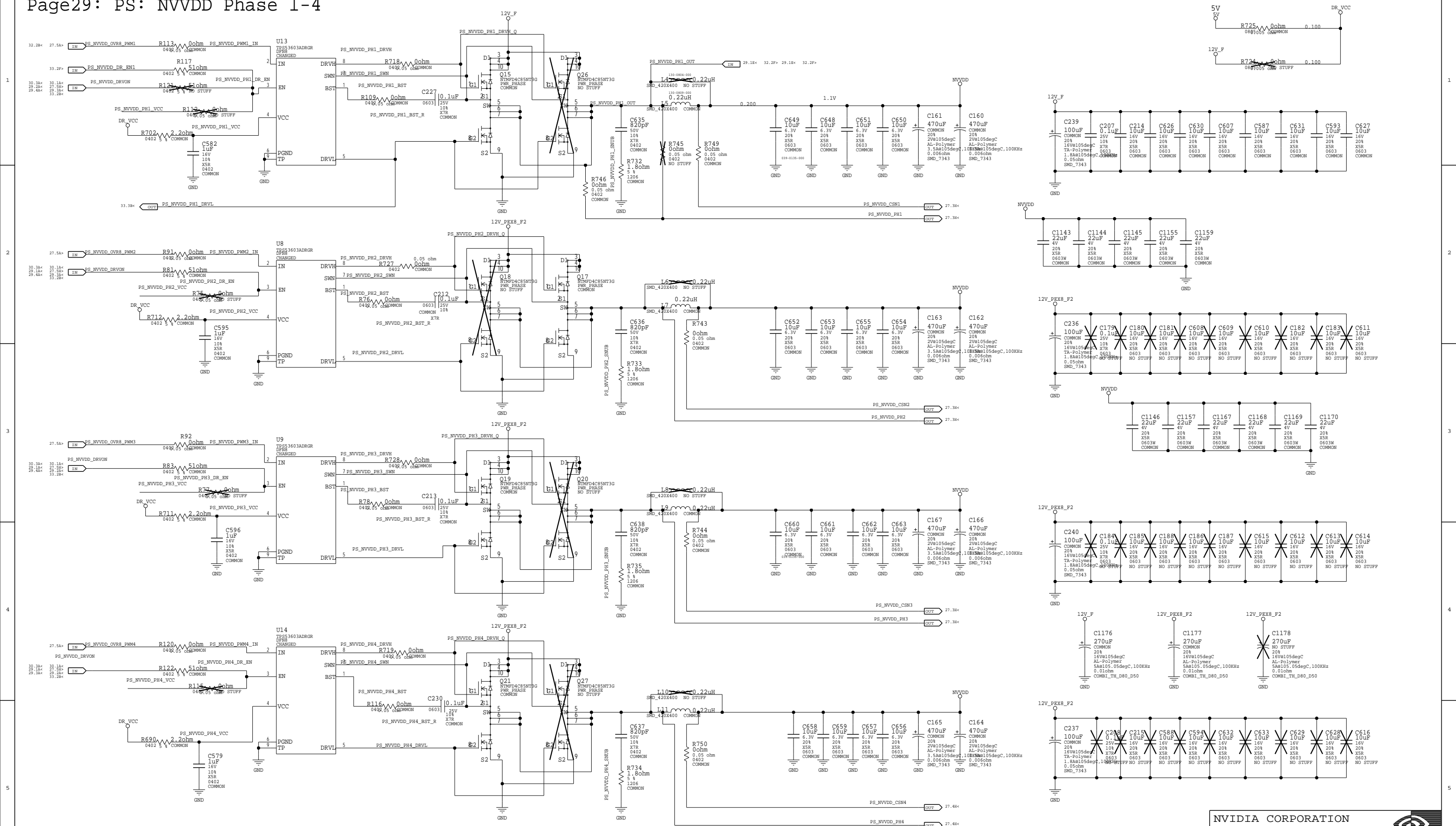
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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Blank Page

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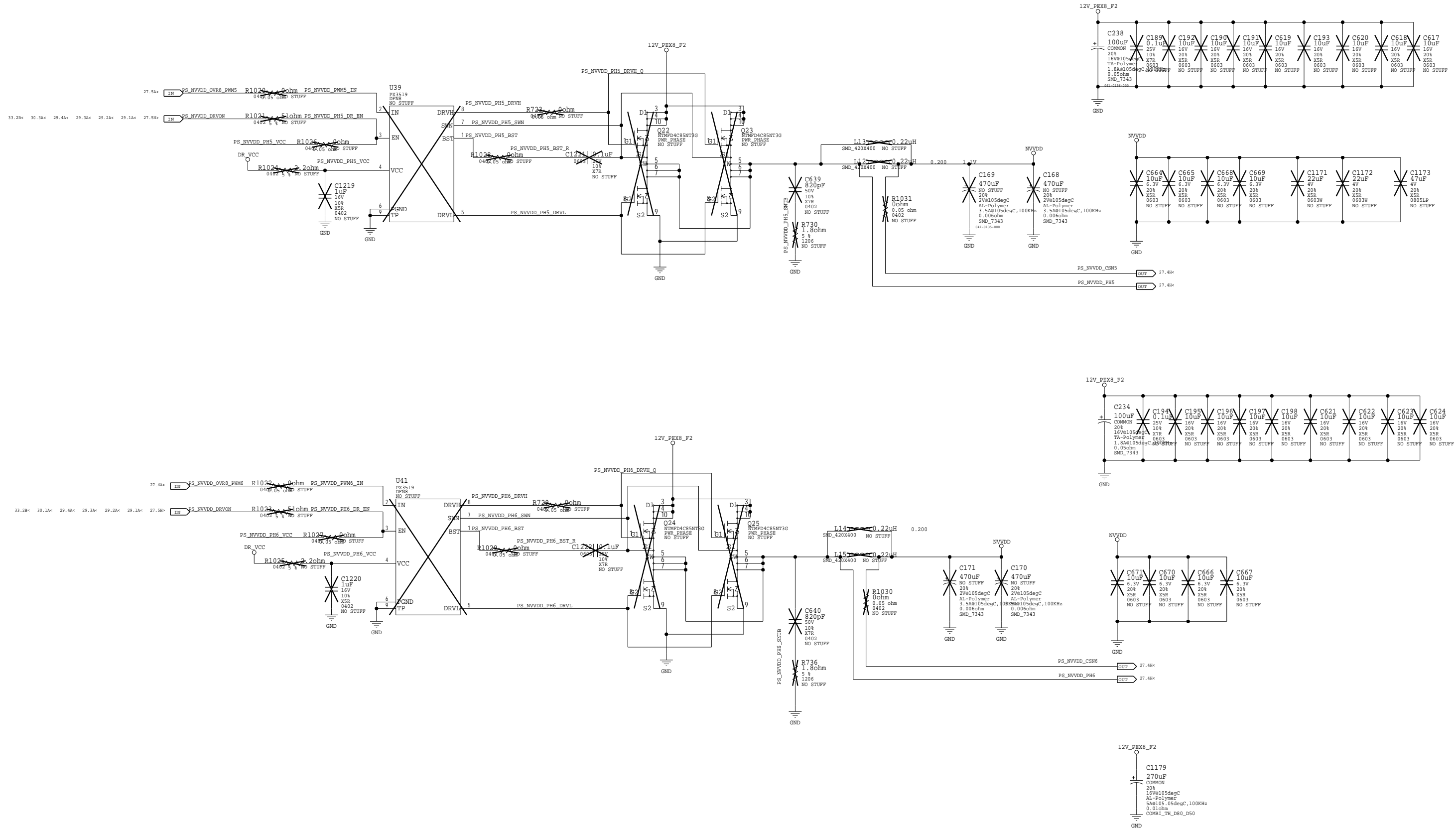
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ASSEMBLY SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
 PAGE DETAIL PS: NVVDD Phase 1-4

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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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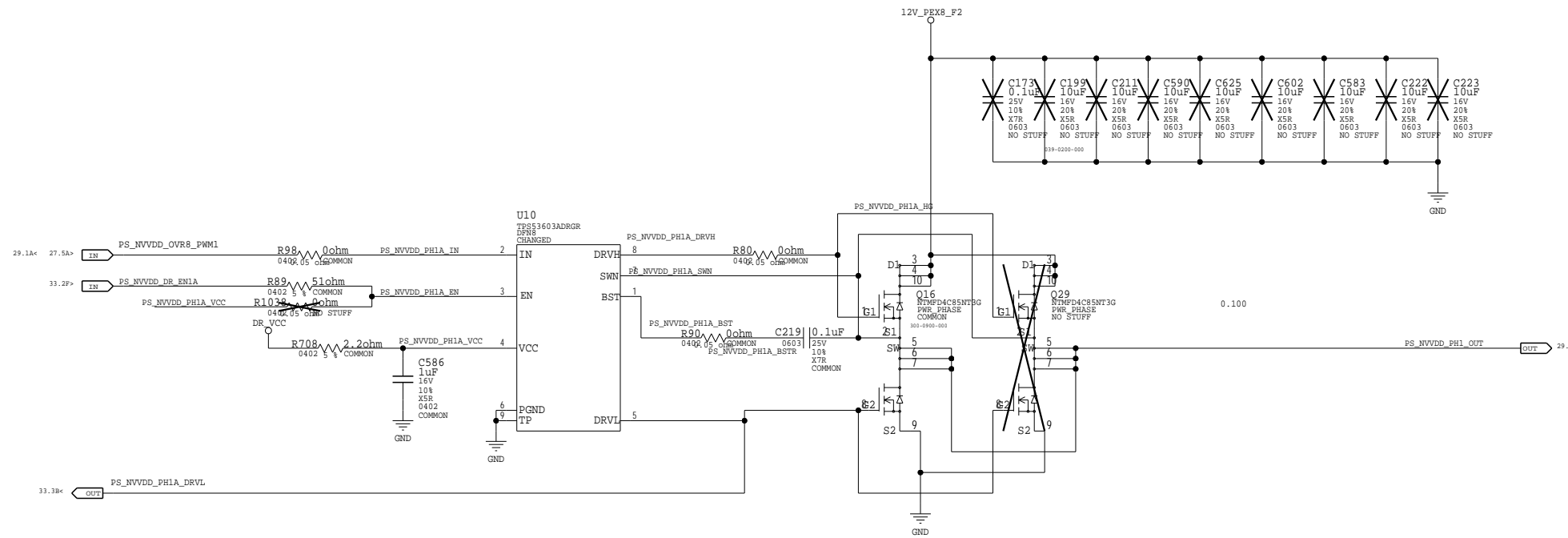
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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Blank Page

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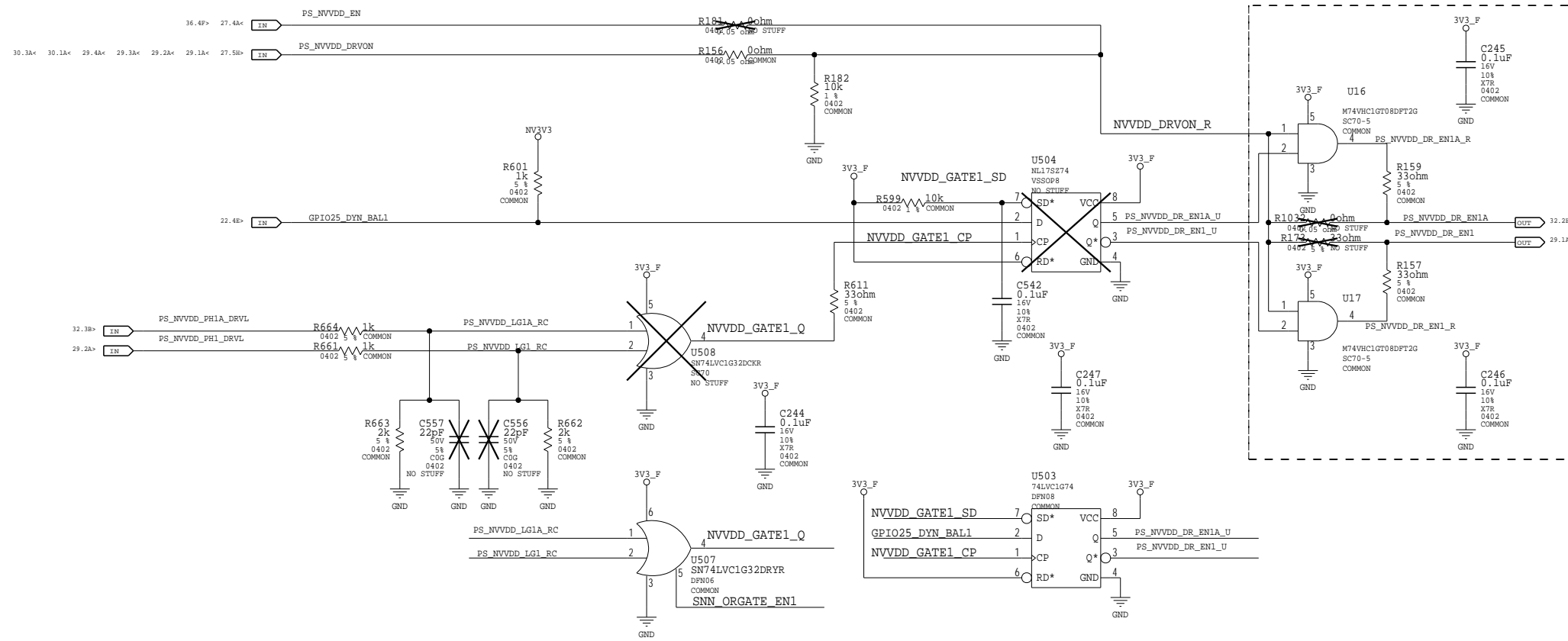
Page32: PS: Dynamic Power Balance Phases



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BOM REV	B		

ASSEMBLY: SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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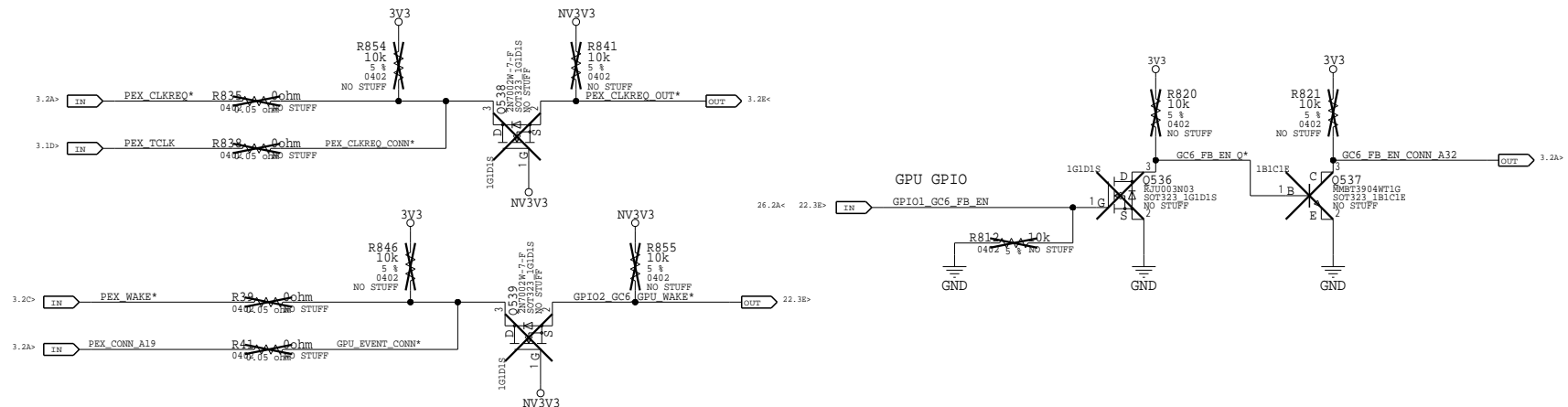
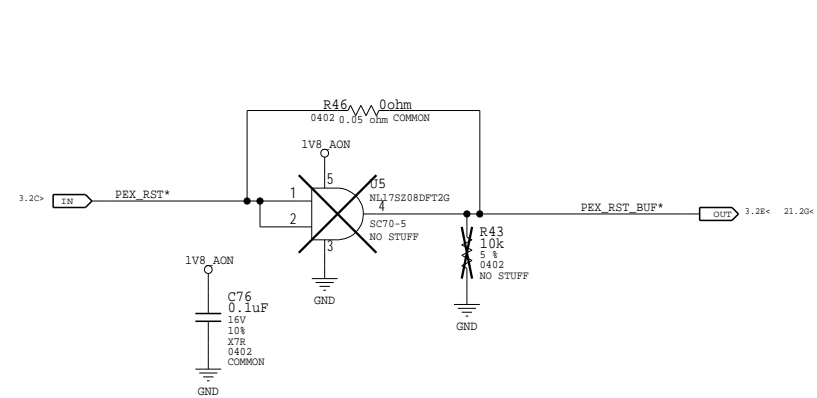
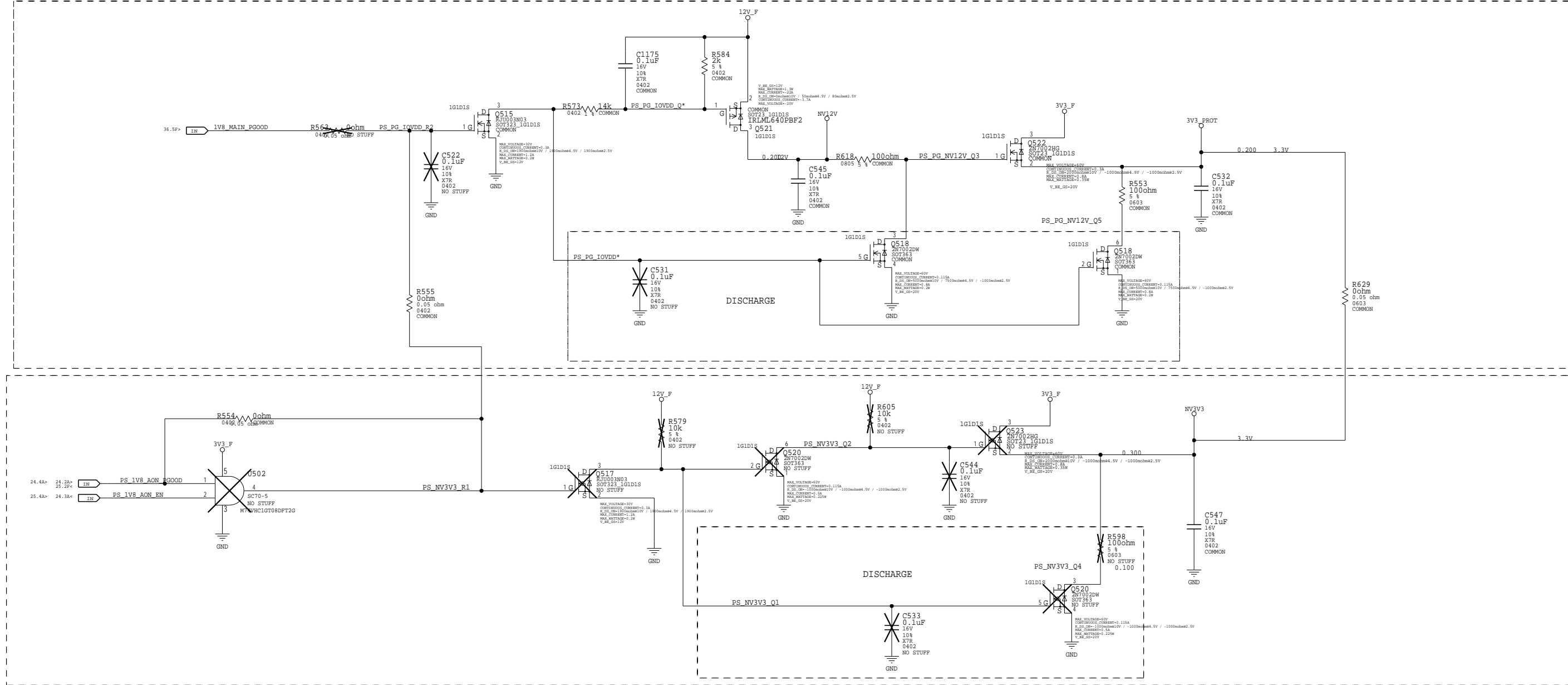
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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Dynamic Power Balance Logic

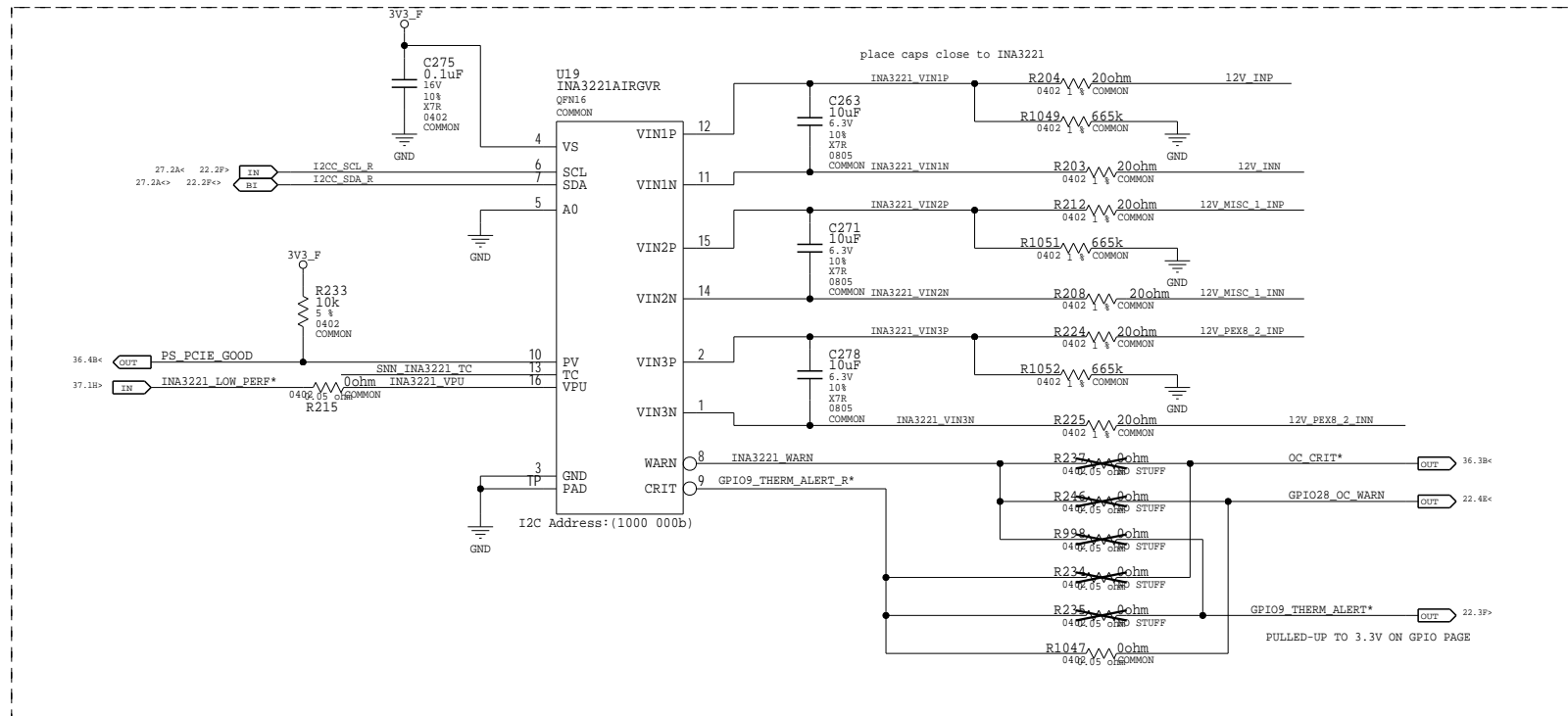
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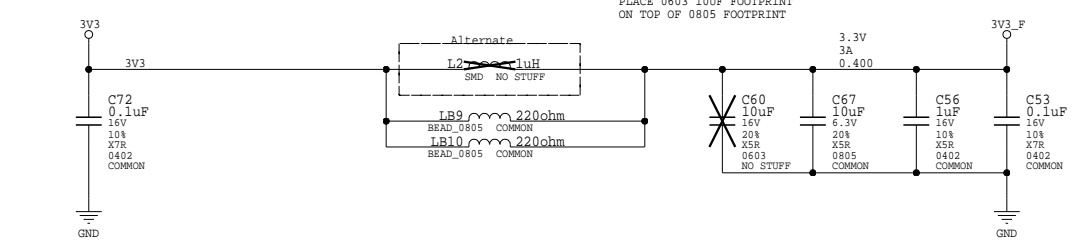
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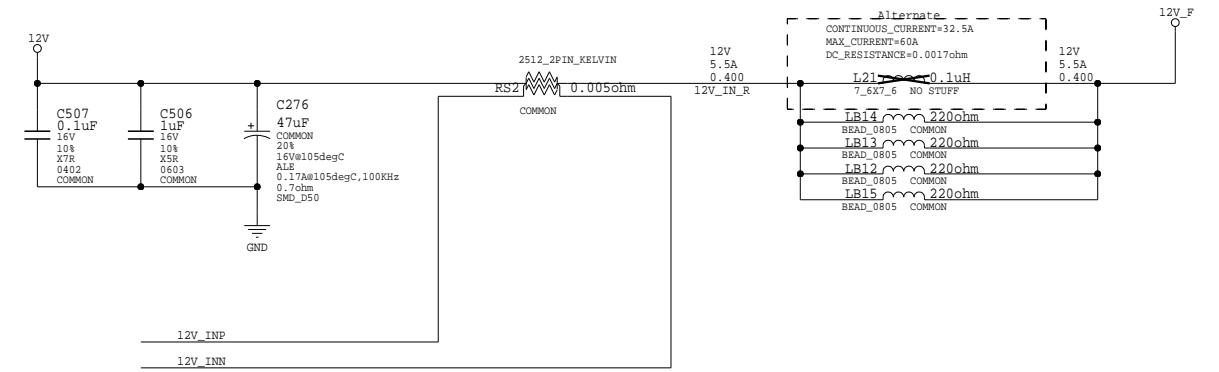
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 PAGE DETAIL PS: NV3V3, NV12V



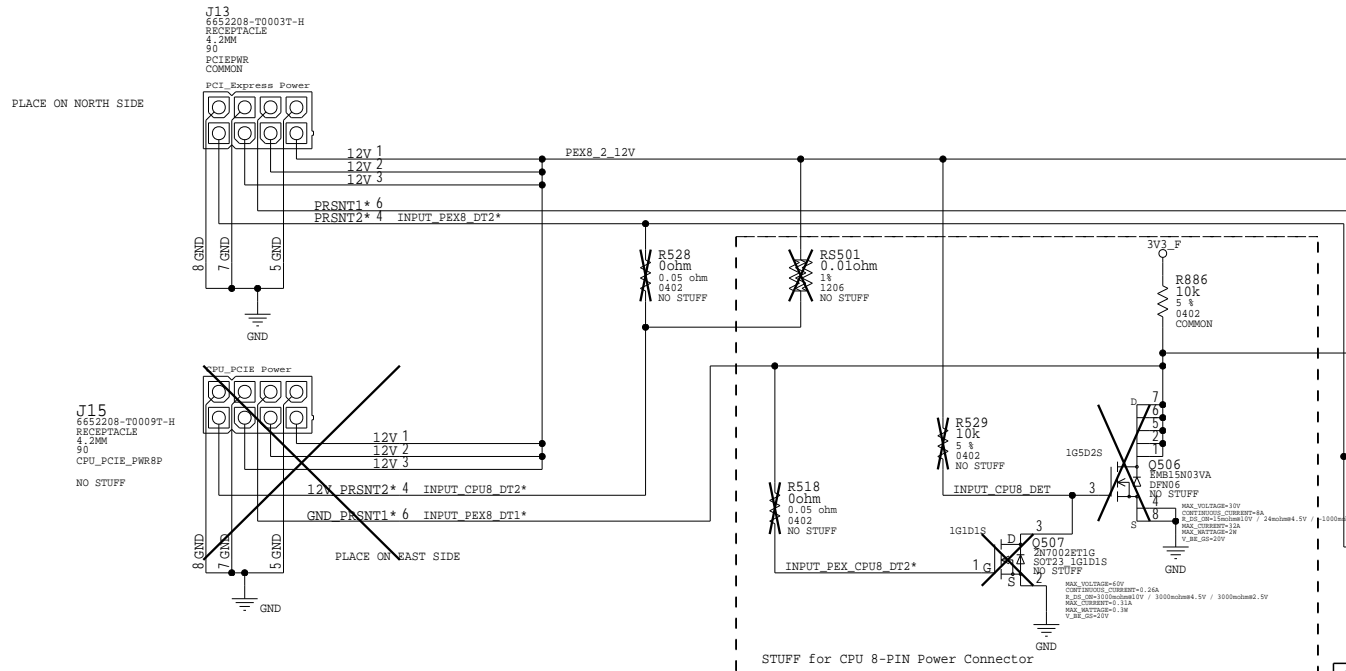
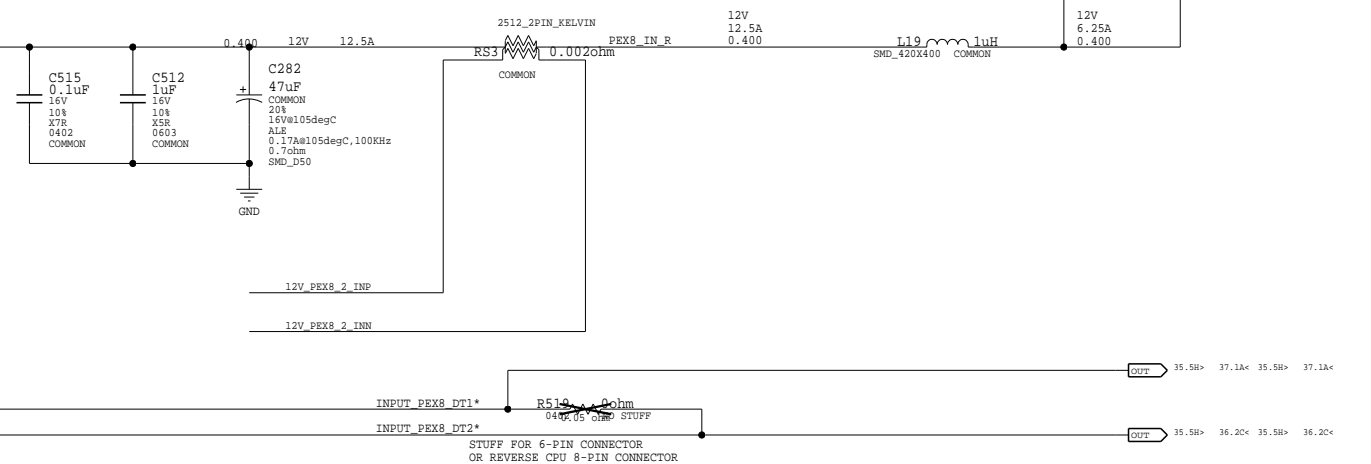
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



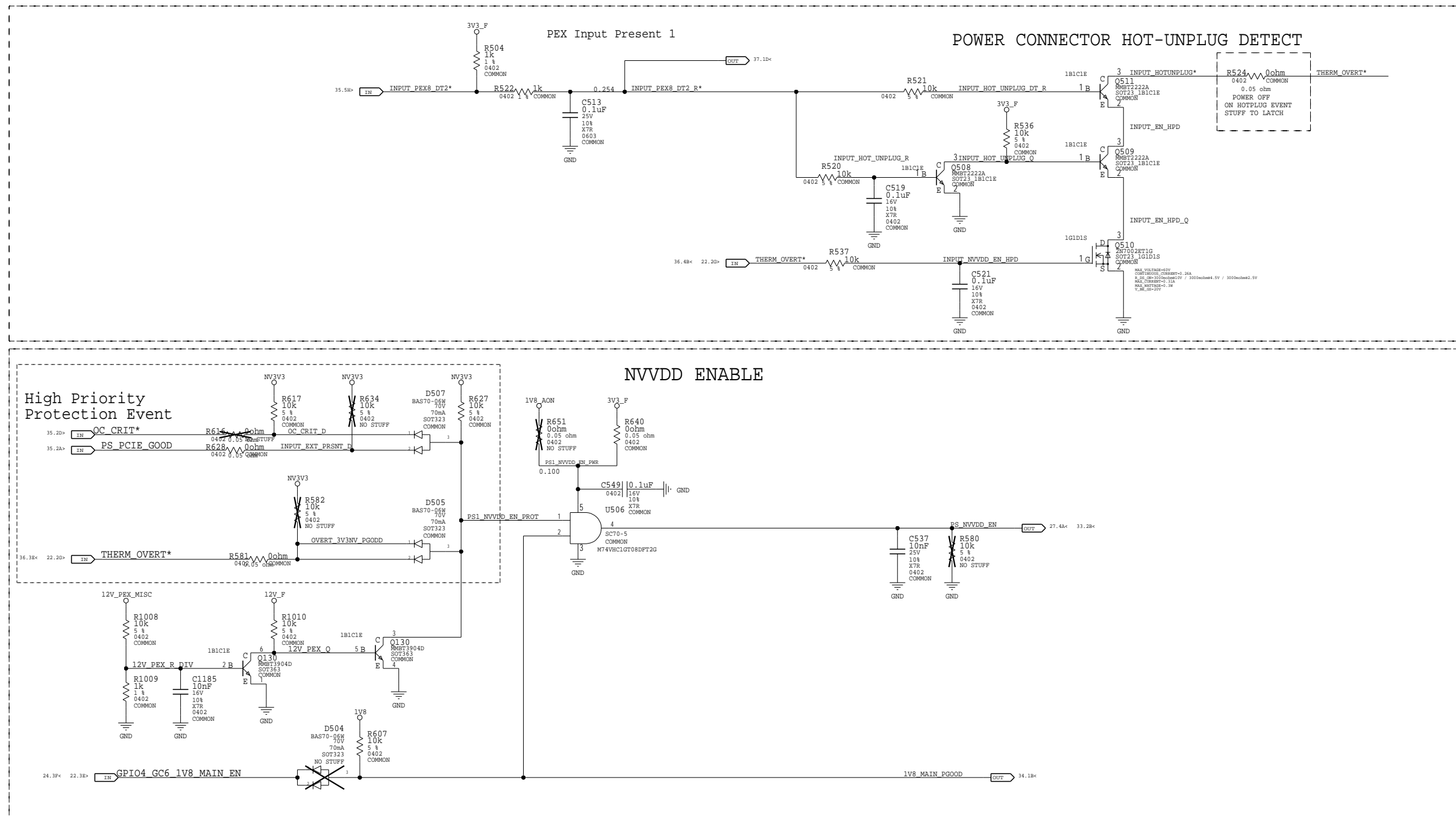
PEX8 INPUT 2 - 2x4 PCIE CON 150W



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ASSEMBLY SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL PS: Inputs, Filtering, and Monitoring

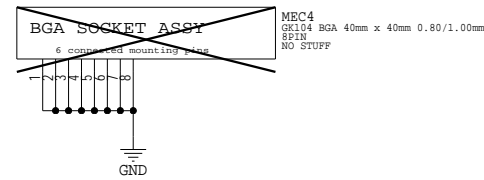
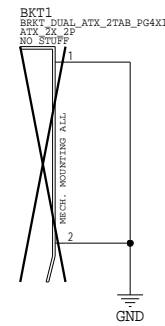


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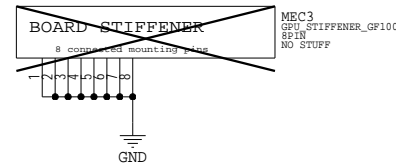
ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Shutdown and Sequencing

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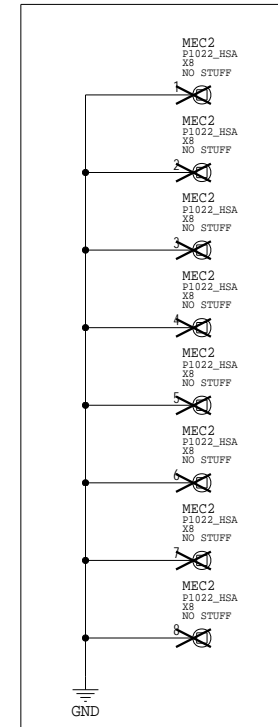
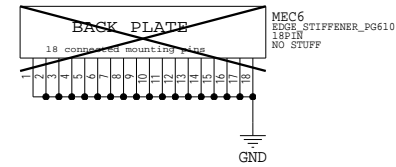
Brackets:



GPU Stiffner



Mechanical Holes Symbol



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