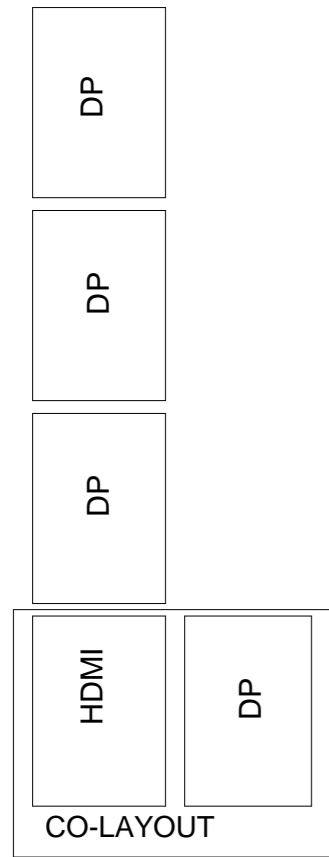


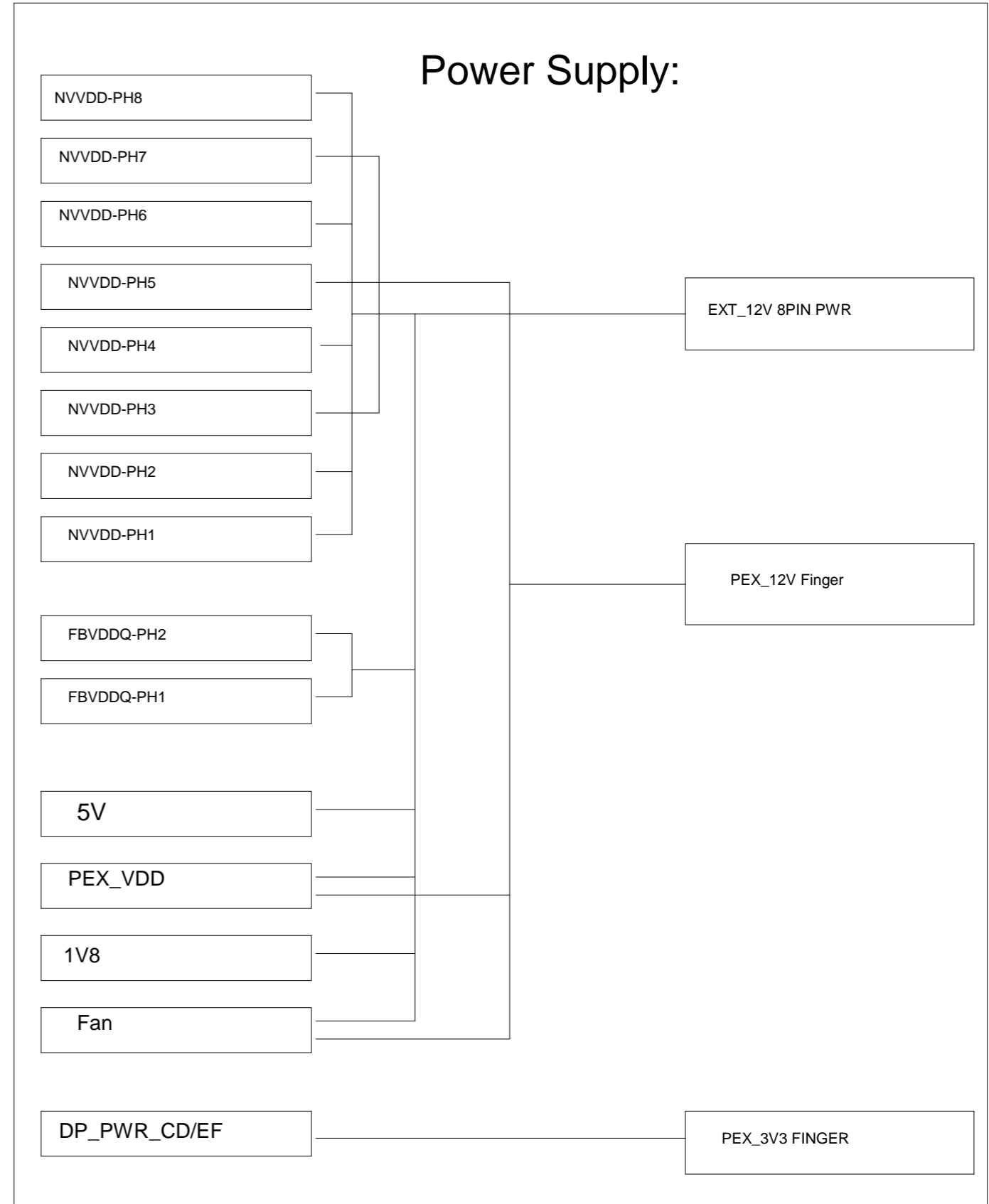
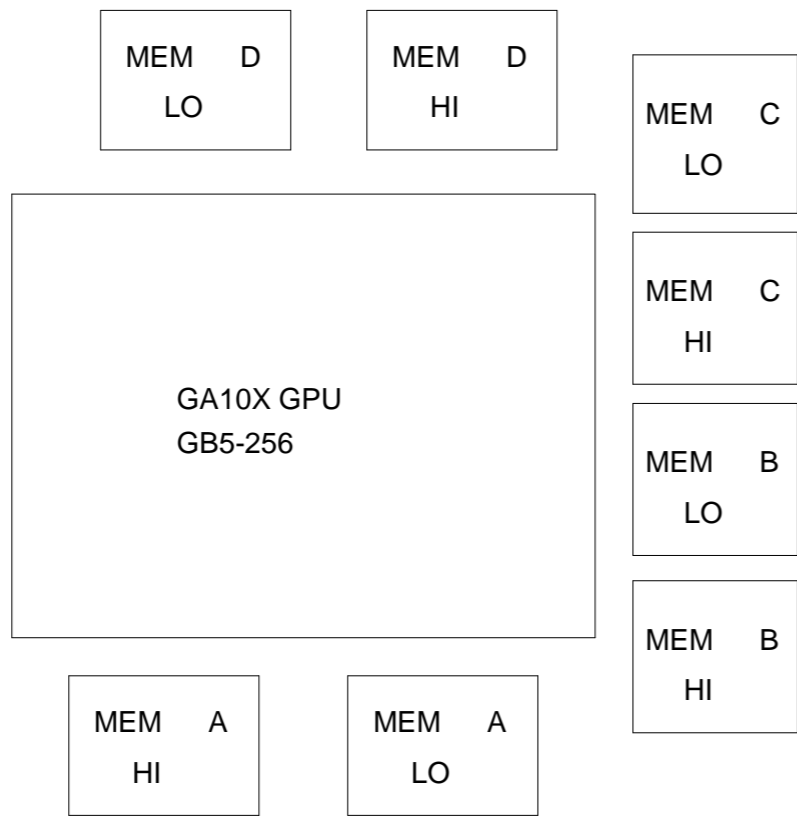
PG190-A02  
GA104/GA106 GB5256  
DP + DP + DP + HDMI/DP

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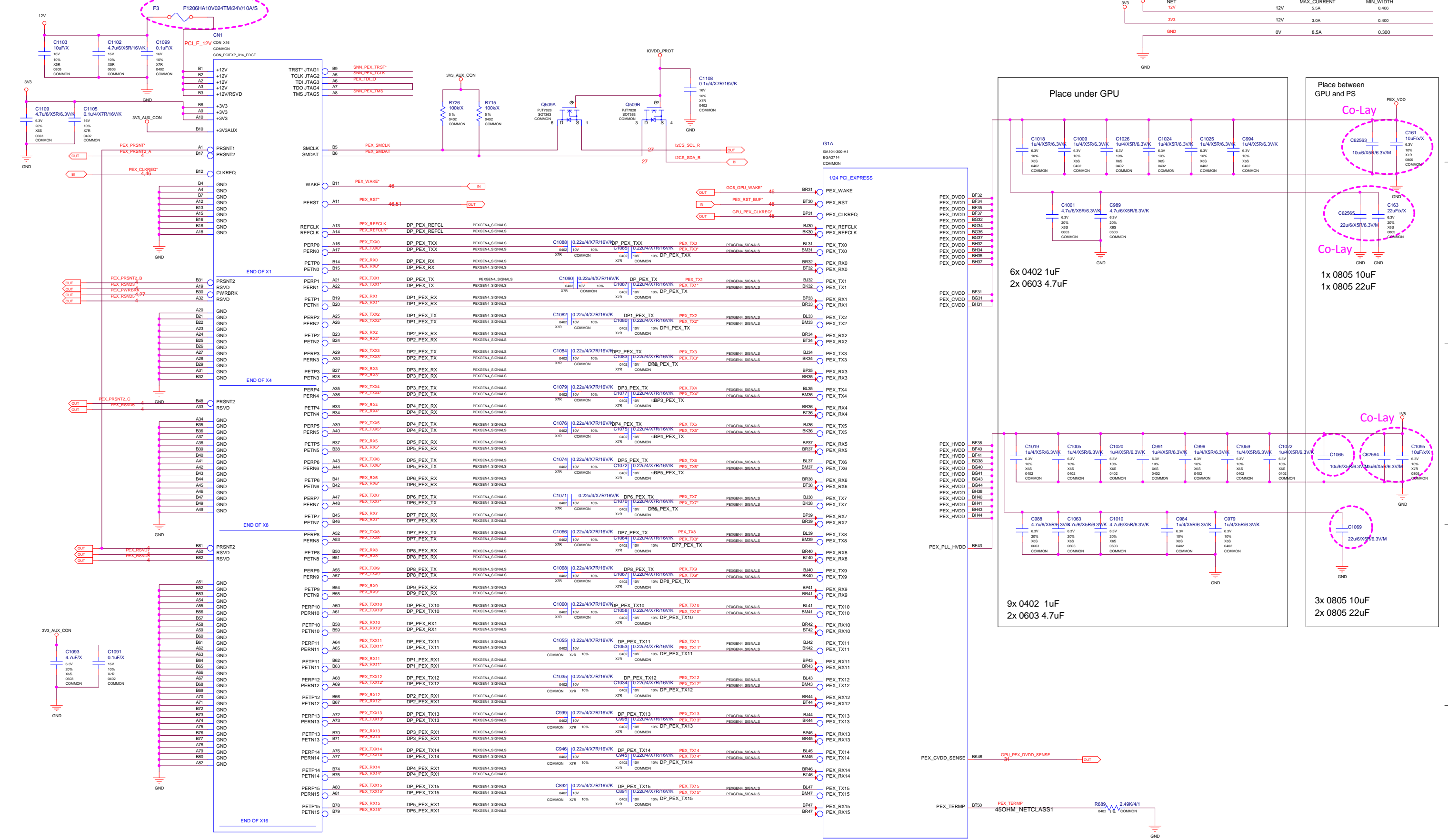
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POWER SUPPLY



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**GIGABYTE**

Title: **PCIE**

Size: **Custom**

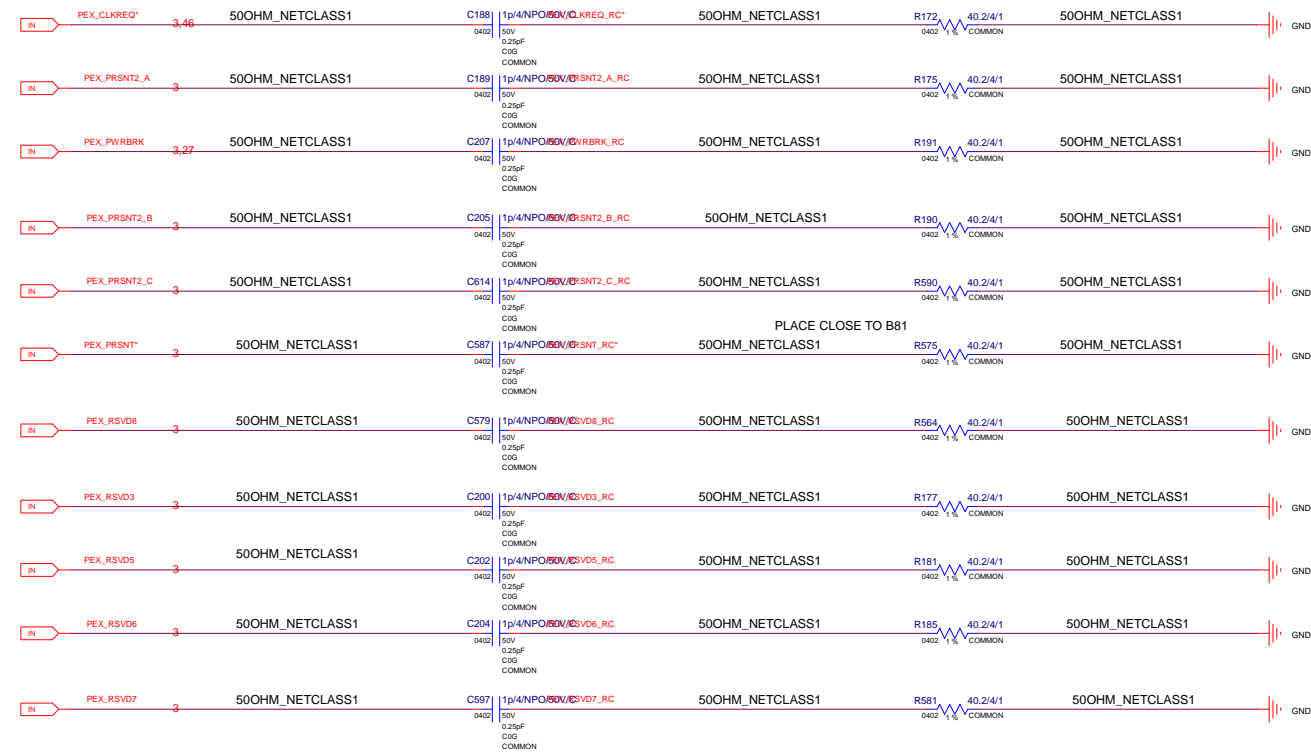
Document Number: **GV-N3060VISION OC-12GD**

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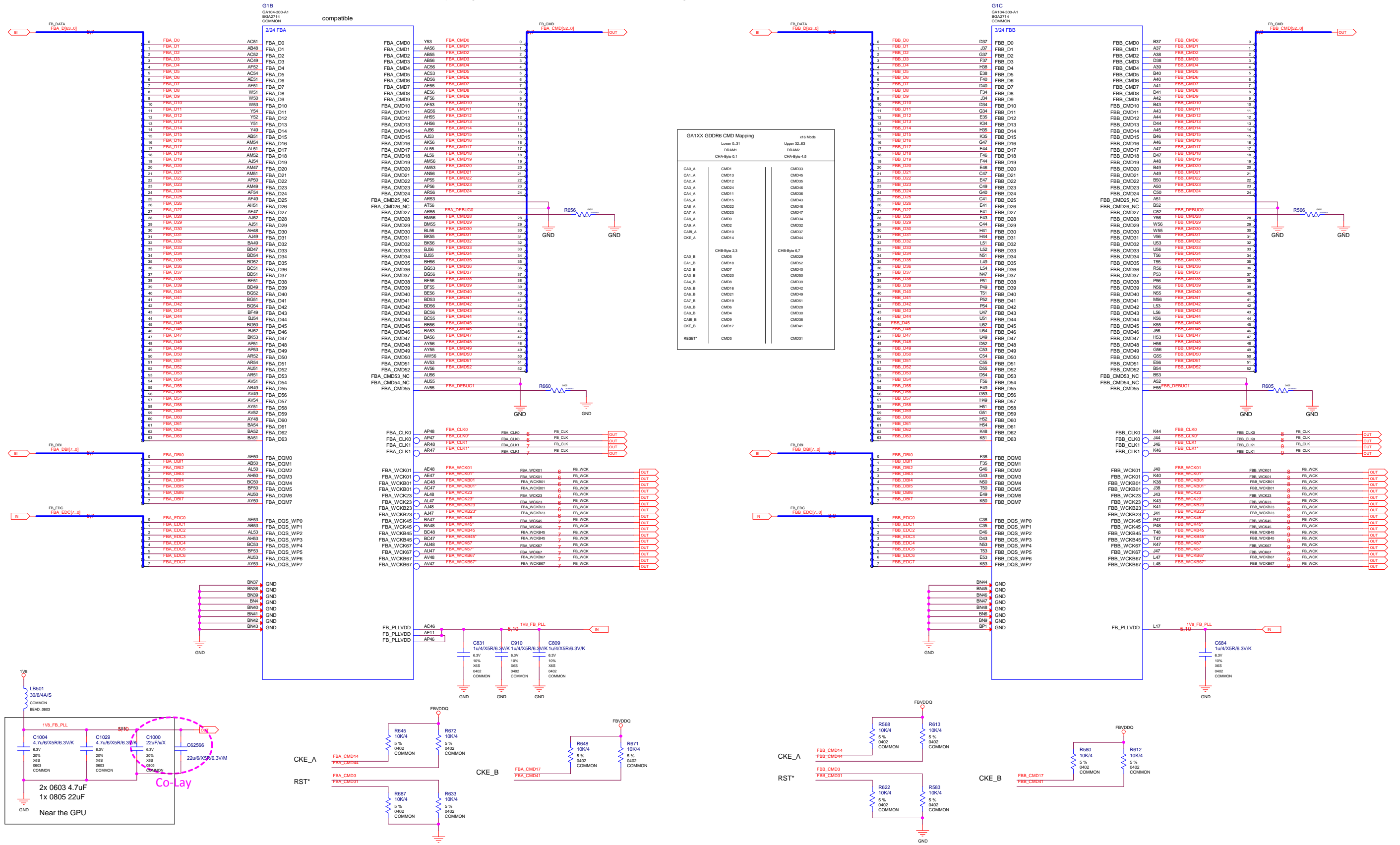


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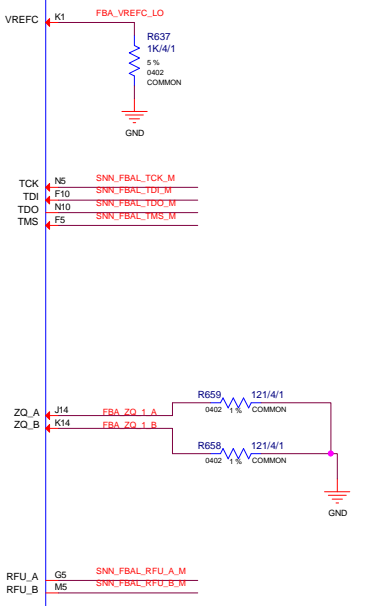
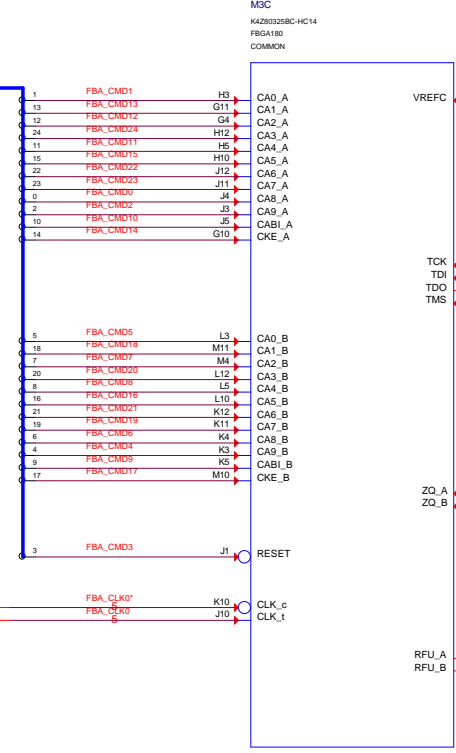
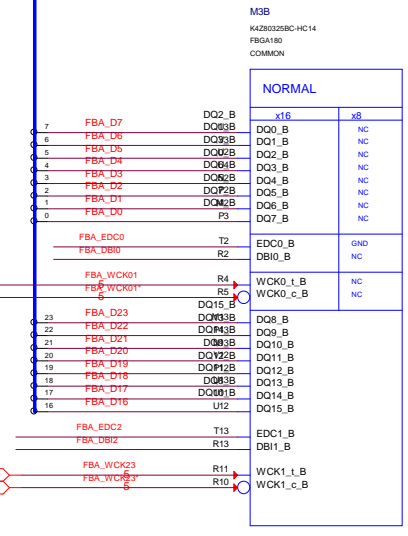
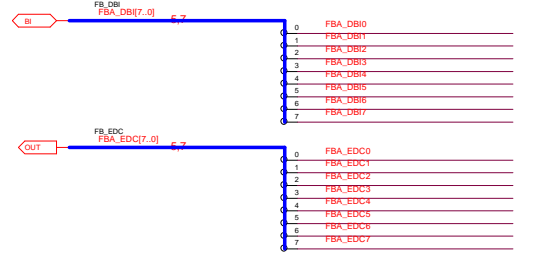
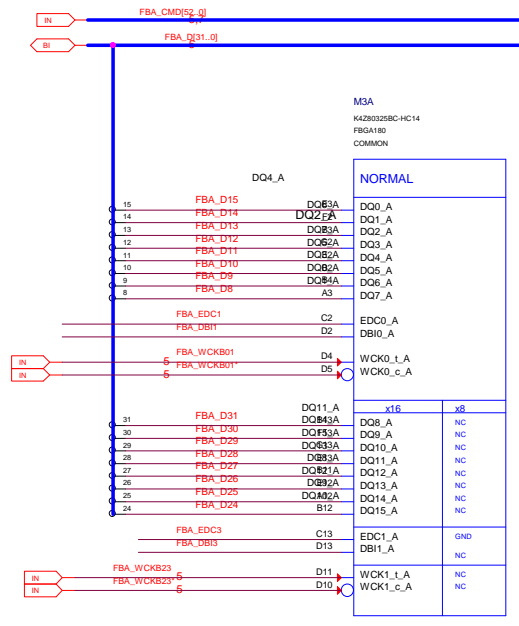
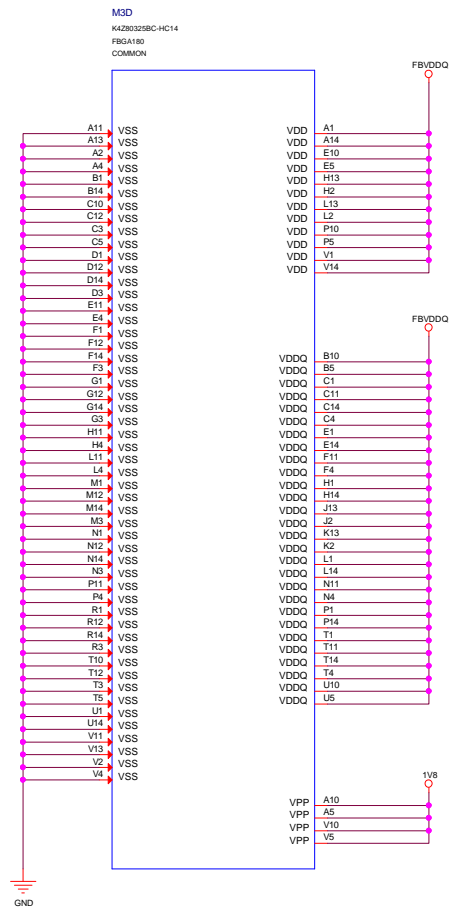
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<b>PCIE</b>			
Size	Document Number	Rev	Rev
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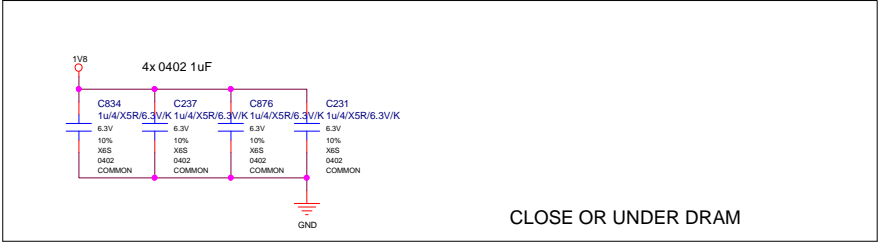
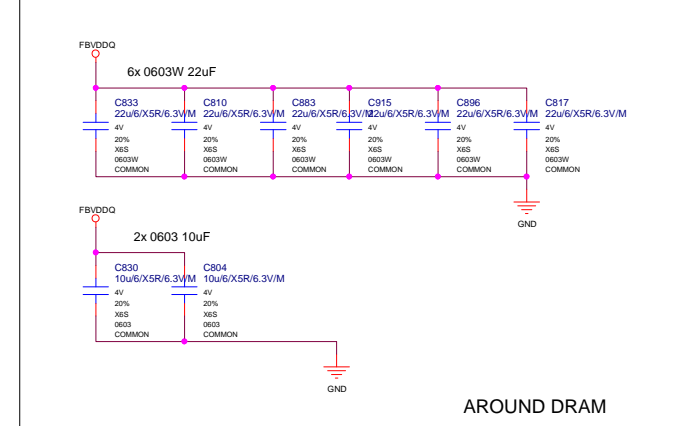
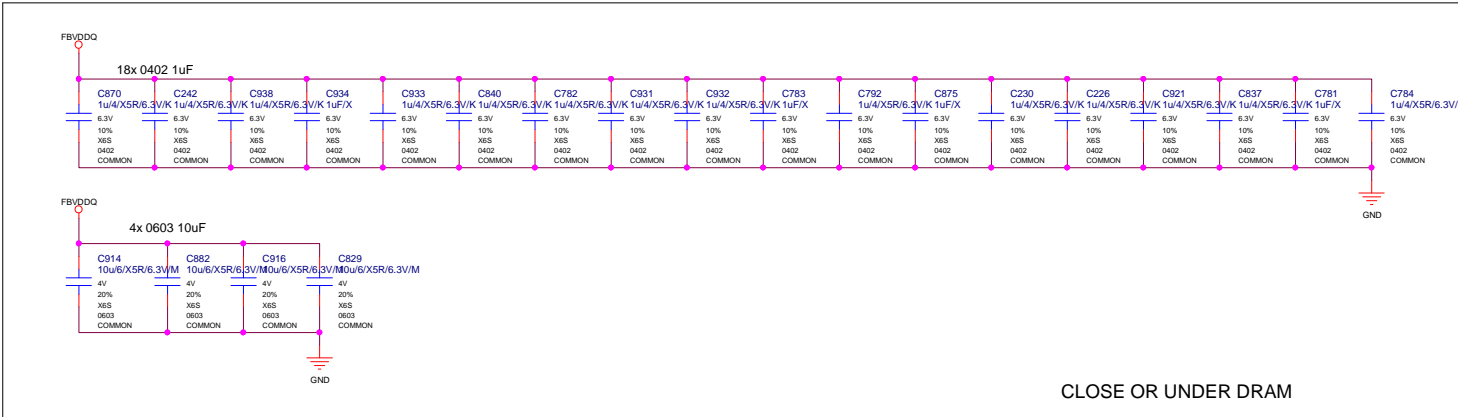
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Lower 0..31 DRAM1 CHA-Byte 0.1		Upper 32..63 DRAM2 CHA-Byte 4.5	
CA0.A	CMD1	CA0.A	CMD33
CA1.A	CMD13	CA1.A	CMD45
CA2.A	CMD10	CA2.A	CMD35
CA3.A	CMD24	CA3.A	CMD46
CA4.A	CMD11	CA4.A	CMD38
CA5.A	CMD15	CA5.A	CMD43
CA6.A	CMD22	CA6.A	CMD48
CA7.A	CMD23	CA7.A	CMD47
CA8.A	CMD0	CA8.A	CMD34
CA9.A	CMD12	CA9.A	CMD36
CAB.A	CMD10	CAB.A	CMD37
CAC.A	CMD14	CAC.A	CMD44
CA0.B	CMD5	CA0.B	CMD29
CA1.B	CMD13	CA1.B	CMD45
CA2.B	CMD7	CA2.B	CMD40
CA3.B	CMD20	CA3.B	CMD50
CA4.B	CMD8	CA4.B	CMD39
CA5.B	CMD16	CA5.B	CMD42
CA6.B	CMD21	CA6.B	CMD49
CA7.B	CMD9	CA7.B	CMD31
CA8.B	CMD6	CA8.B	CMD32
CA9.B	CMD18	CA9.B	CMD41
CAB.B	CMD4	CAB.B	CMD28
CAC.B	CMD9	CAC.B	CMD38
CAD.B	CMD17	CAD.B	CMD47
CCE.B	CMD17	CCE.B	CMD31
RESET*	CMD3	RESET*	CMD31



decap via : at least 2 gnd vias and 2 power vias for each cap

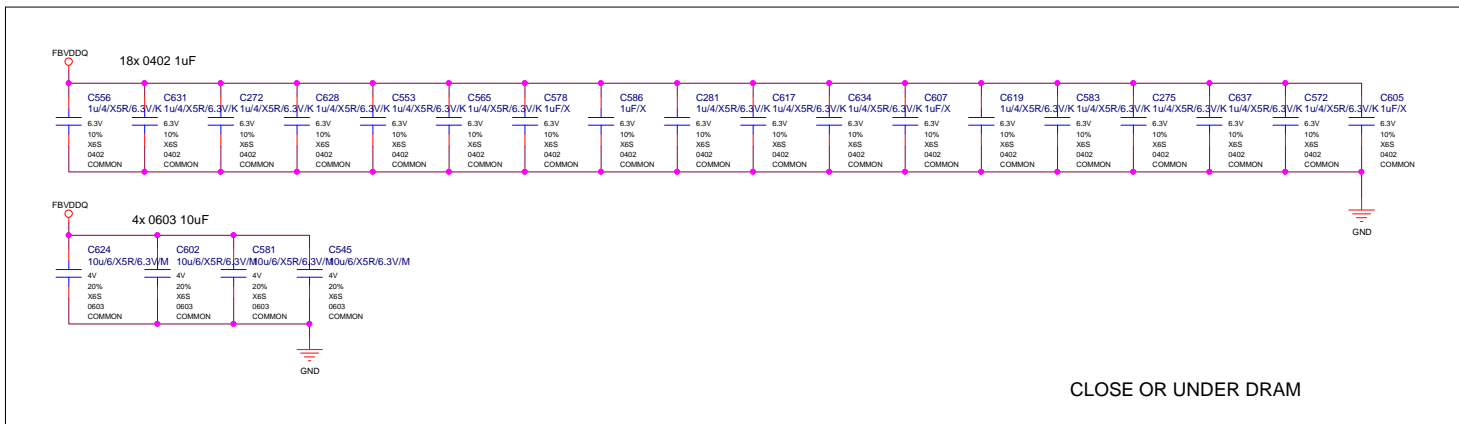
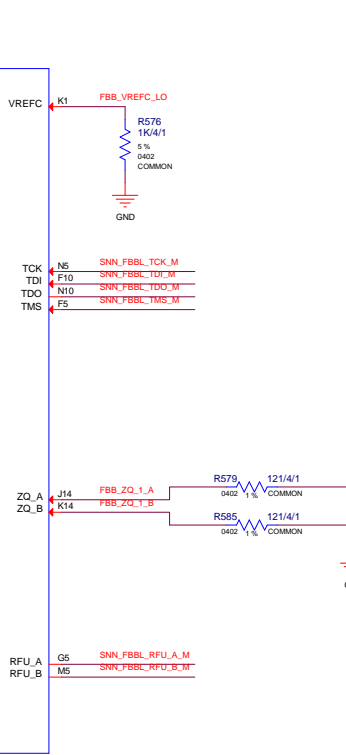
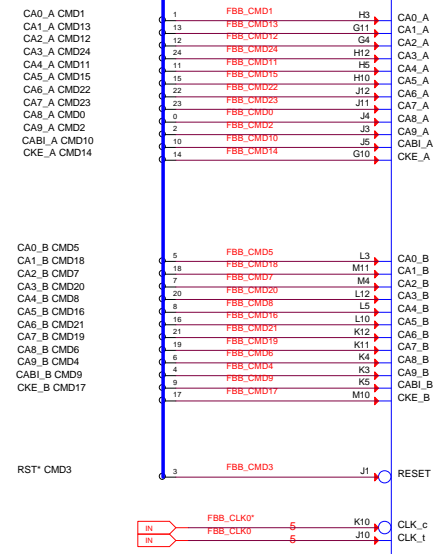
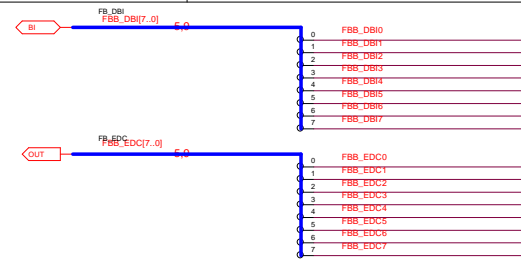
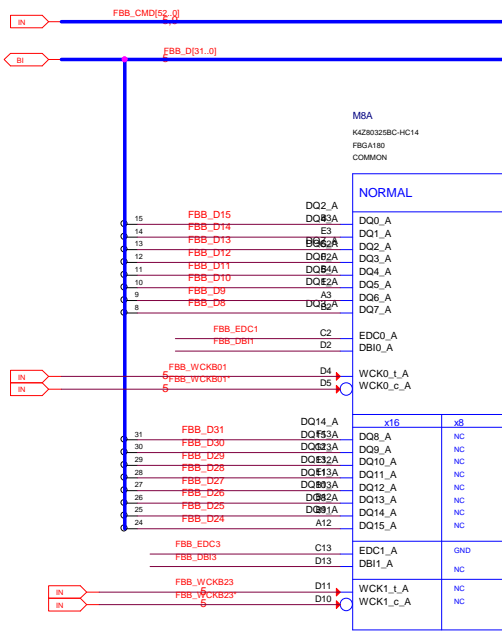
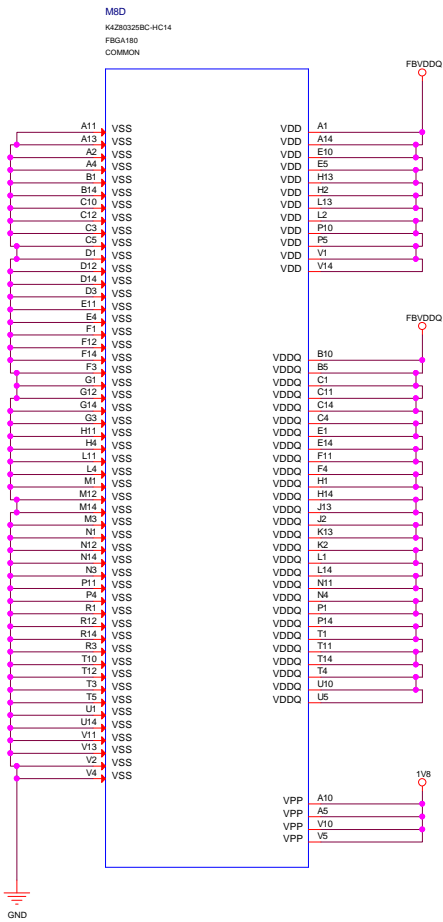


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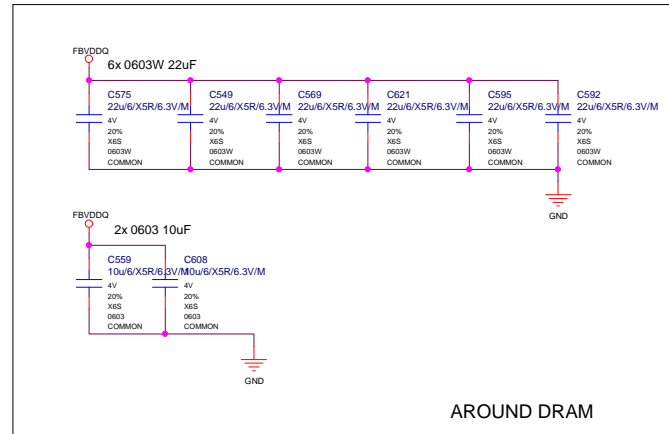
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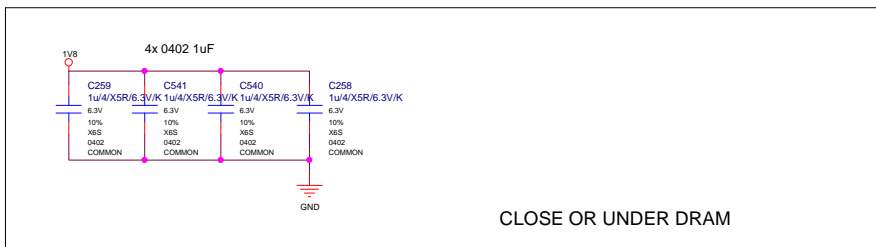




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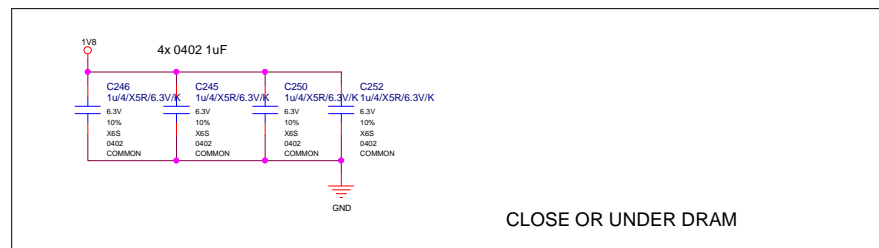
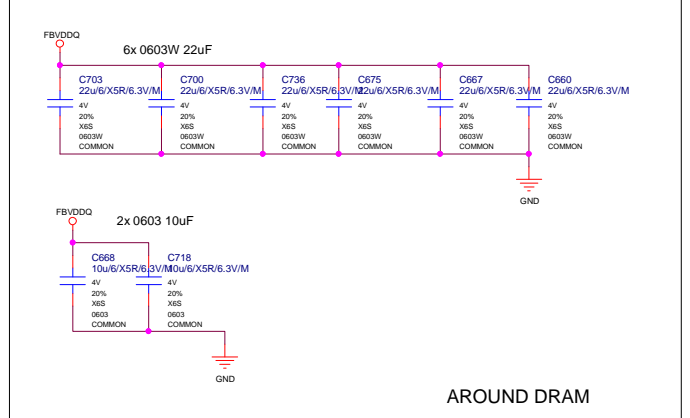
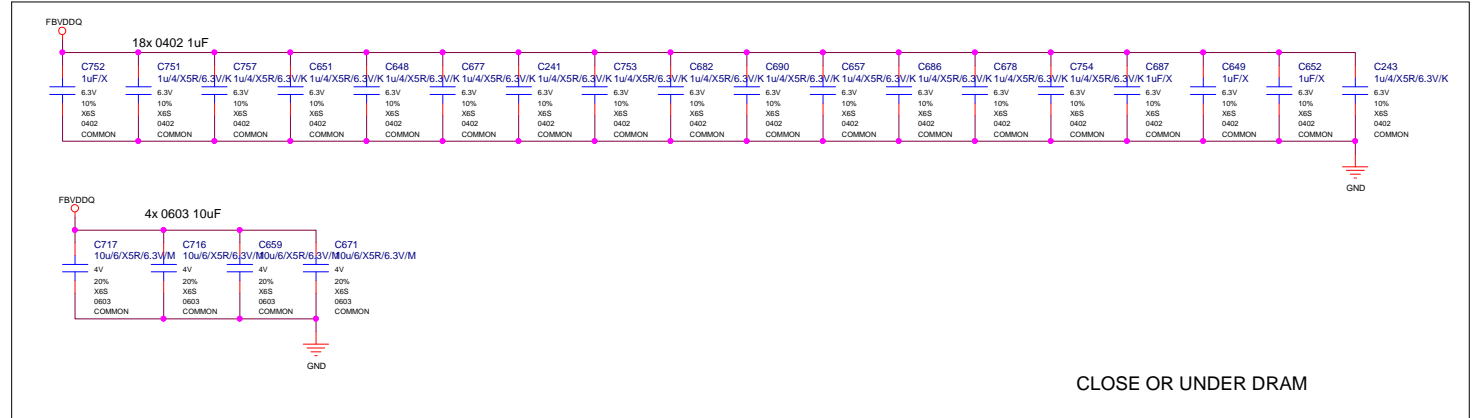
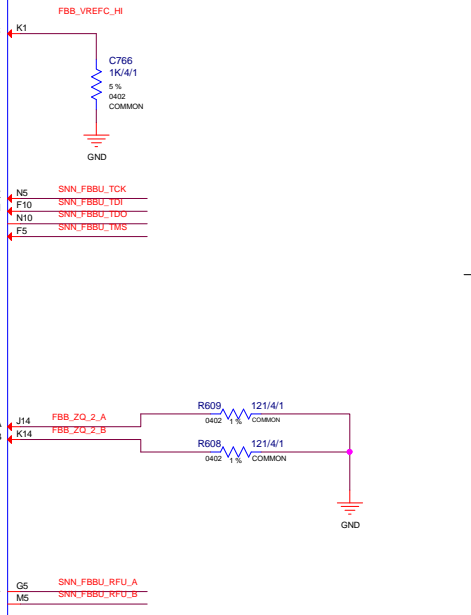
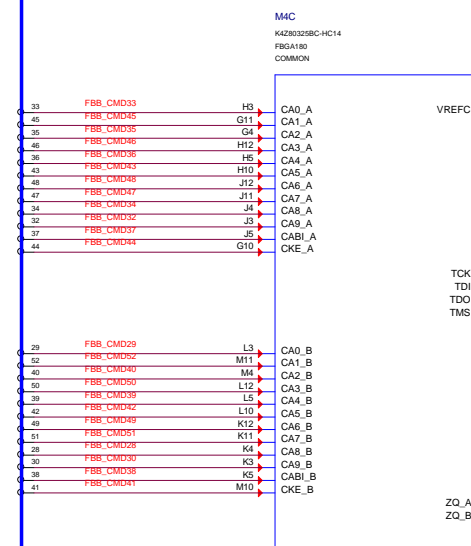
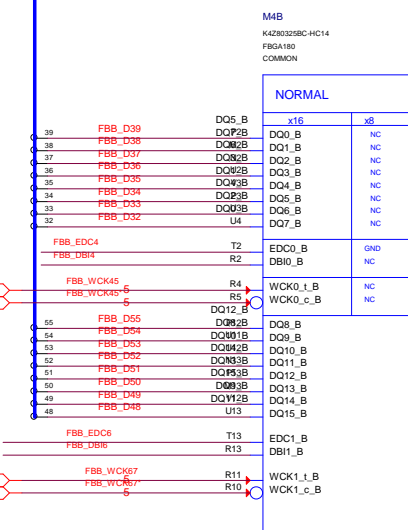
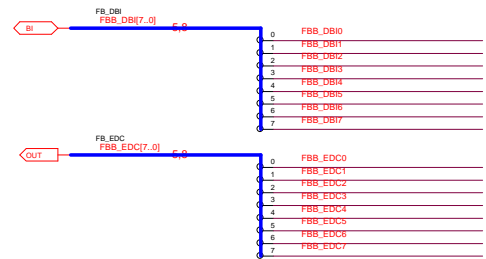
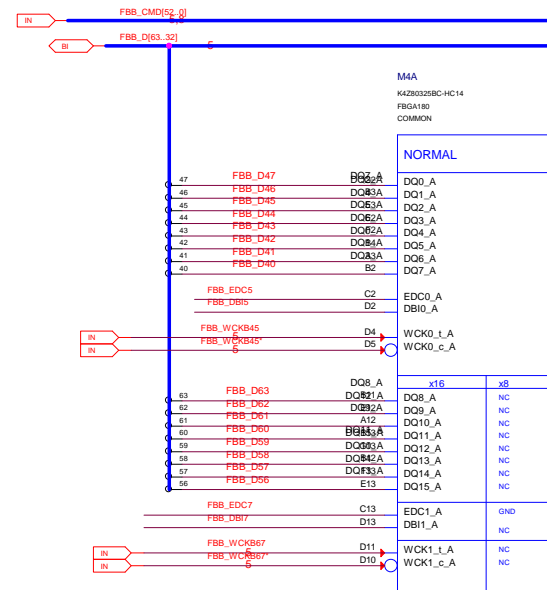
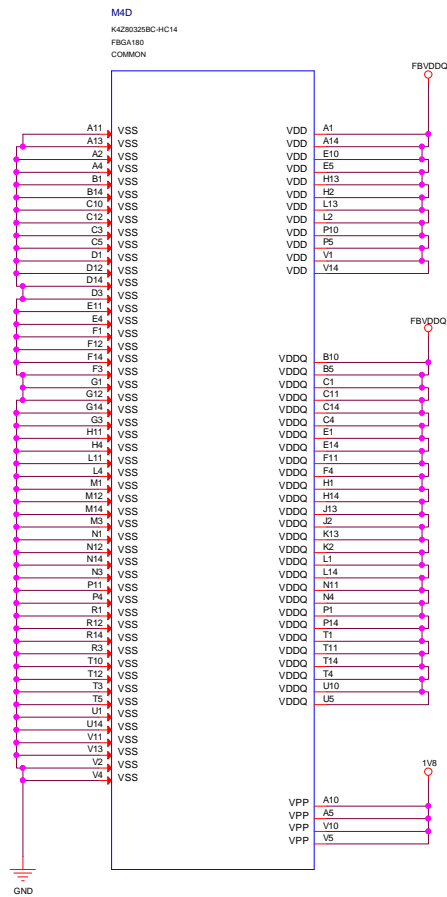
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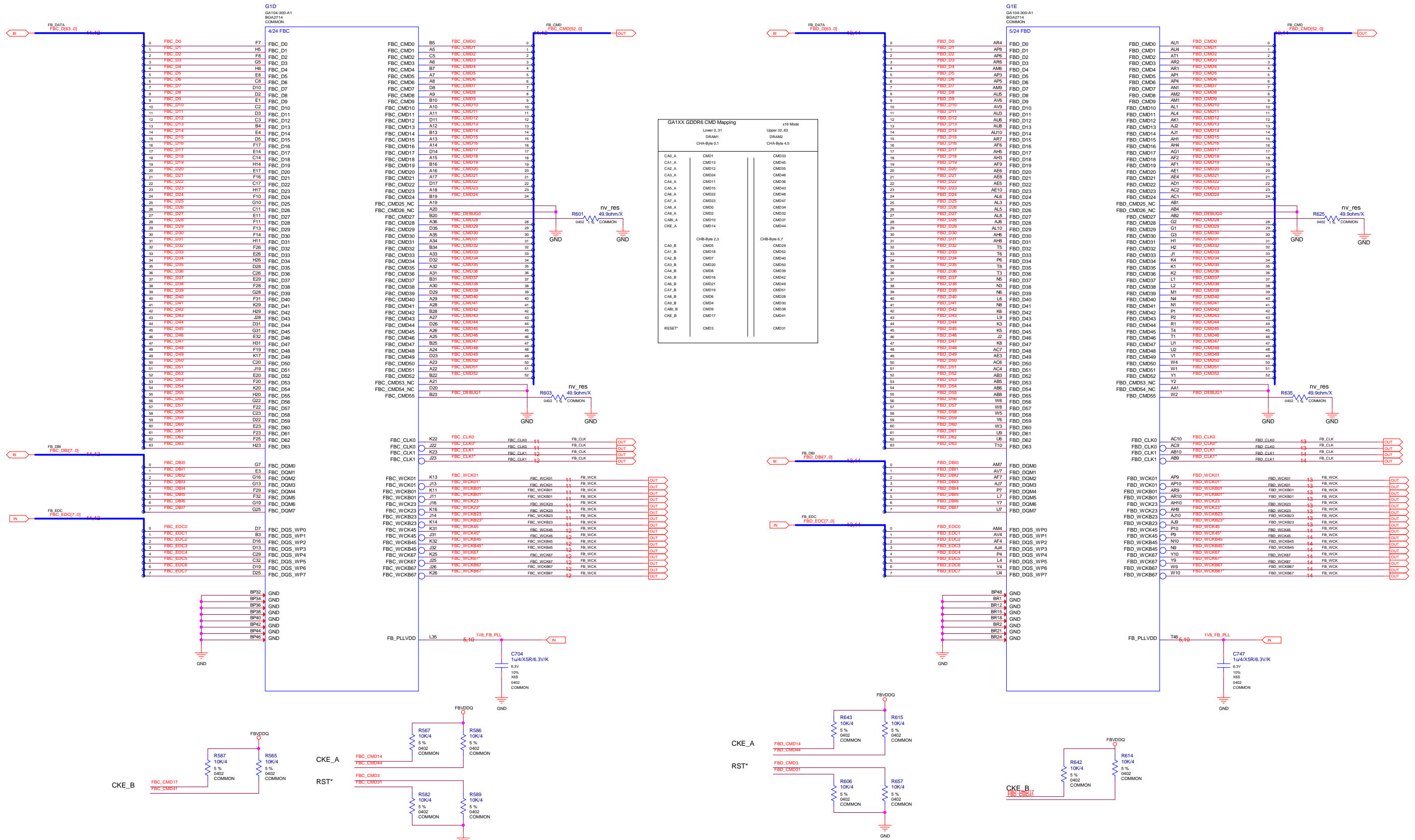
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**GIGABYTE**

Title: **PCIE**

Size: Custom Document Number: **GV-N3060VISION OC-12GD** Rev: 1.01

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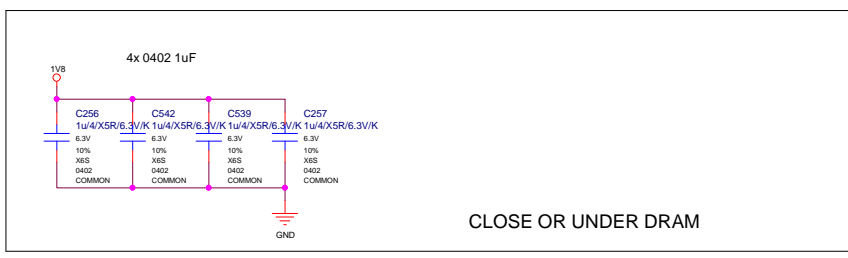
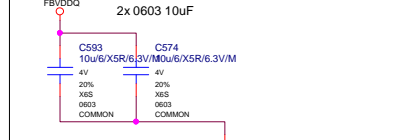
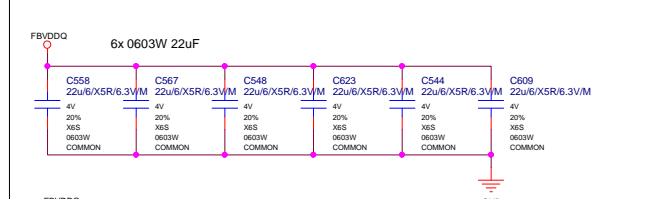
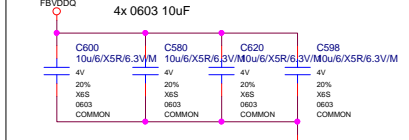
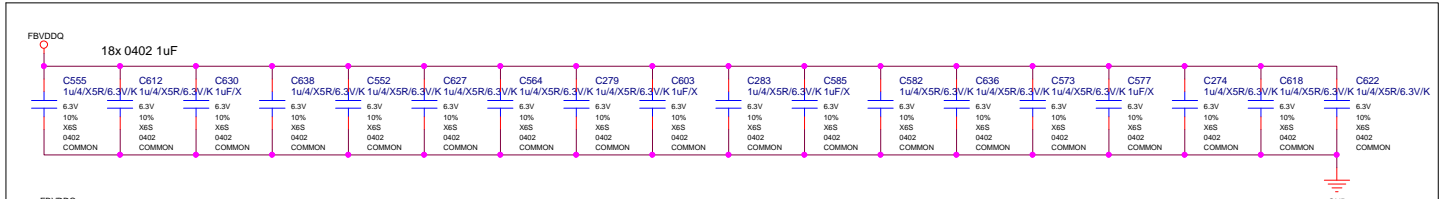
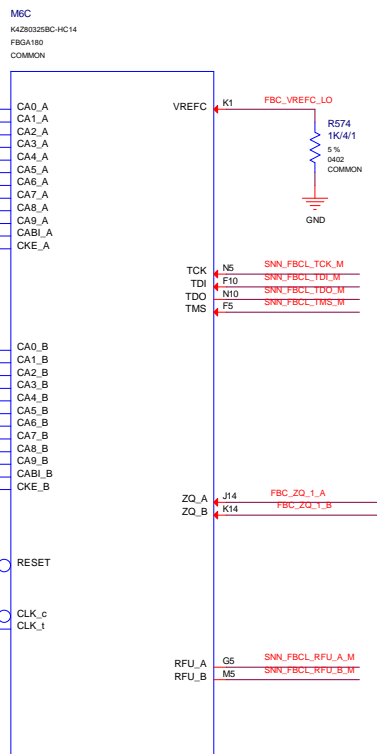
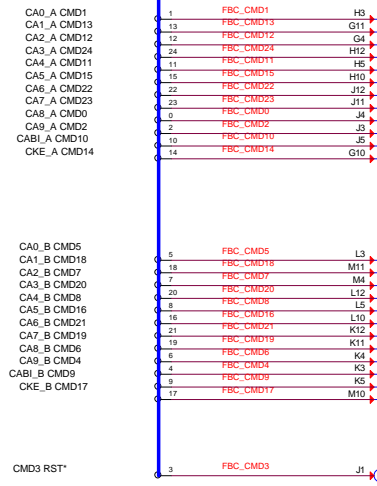
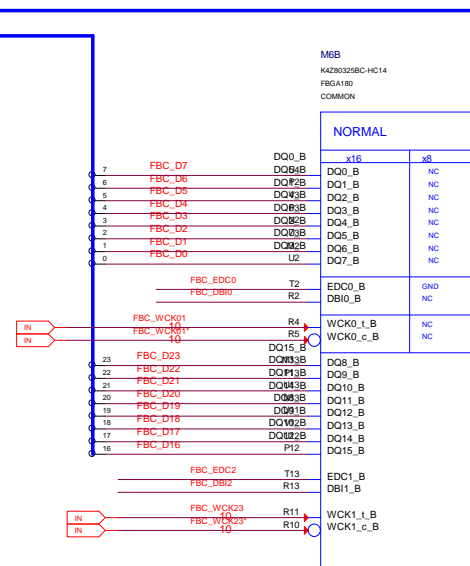
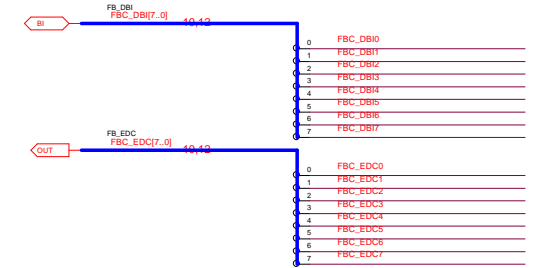
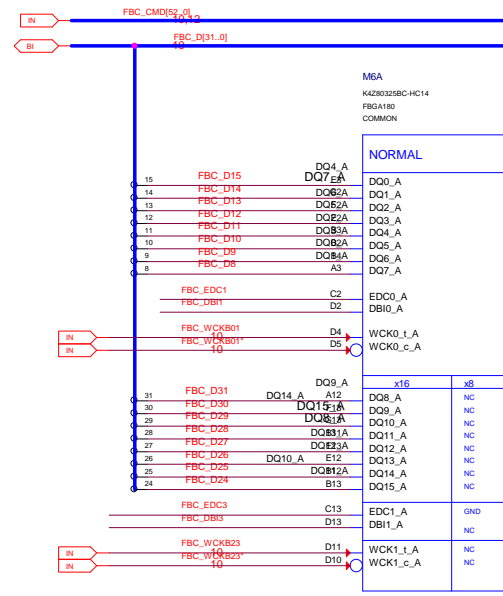
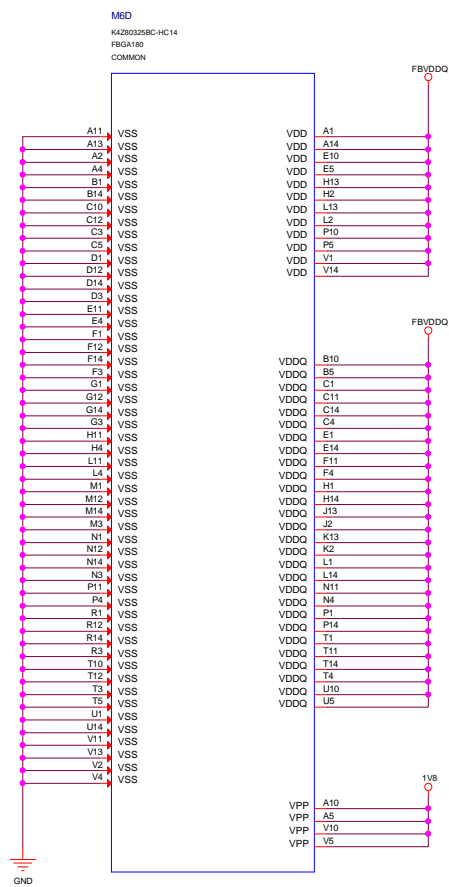
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**GIGABYTE**

Title: **PCIE**

Size: **Custom** | Document Number: **GV-N3060VISION OC-12GD** | Rev: **1.01**

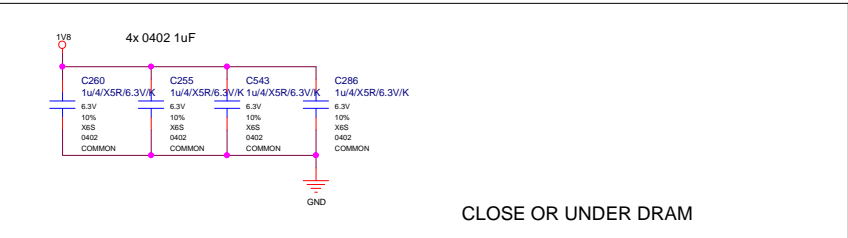
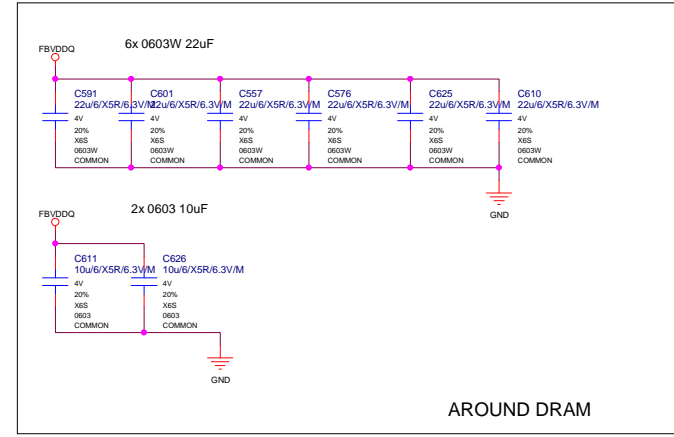
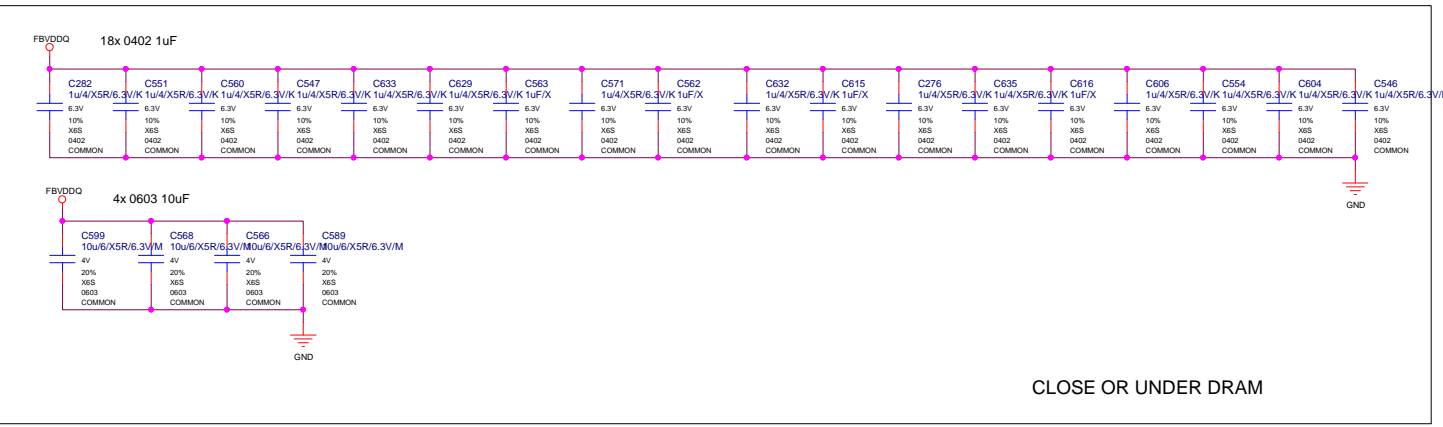
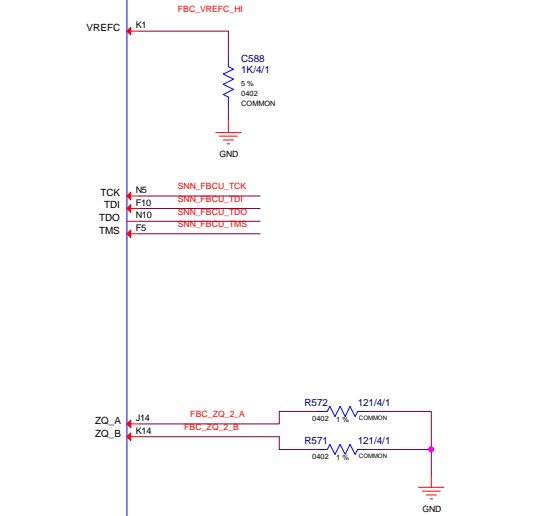
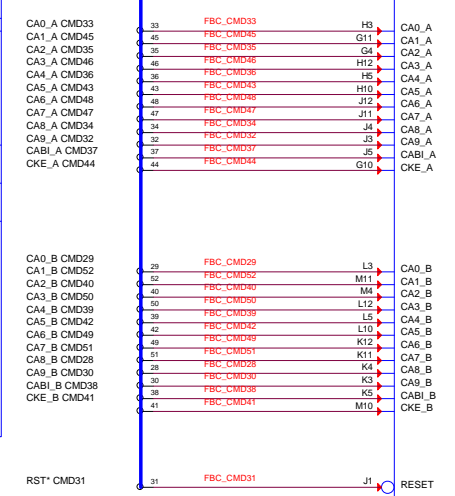
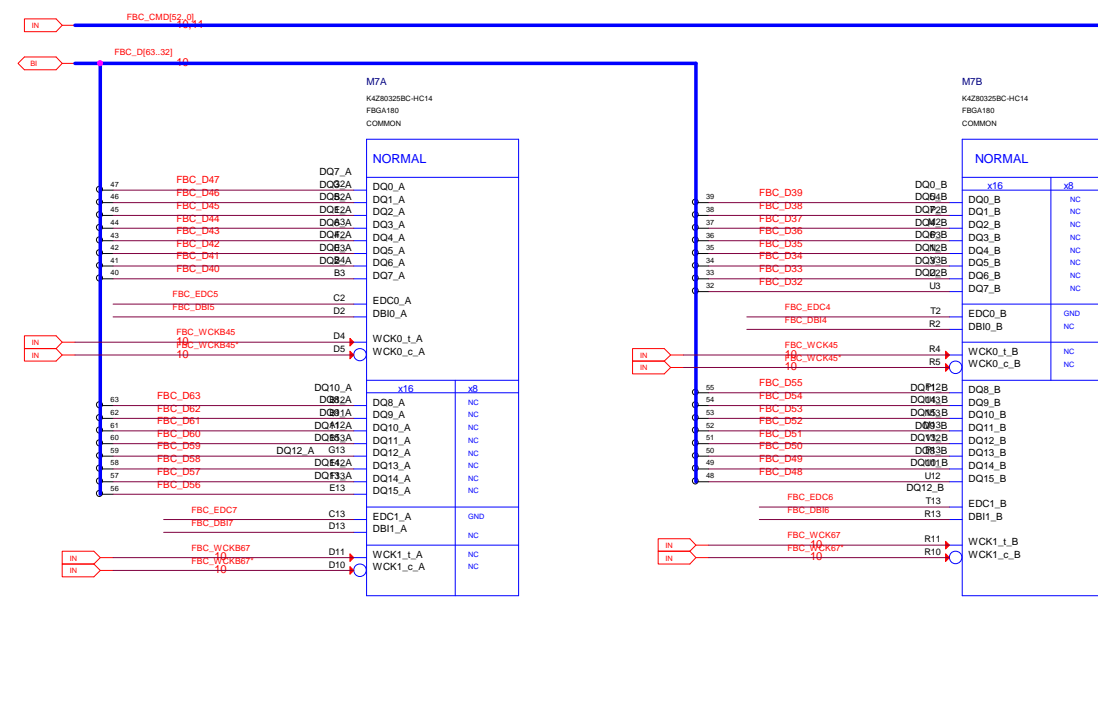
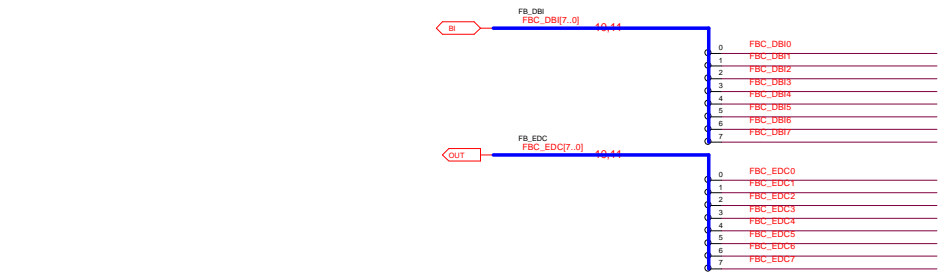
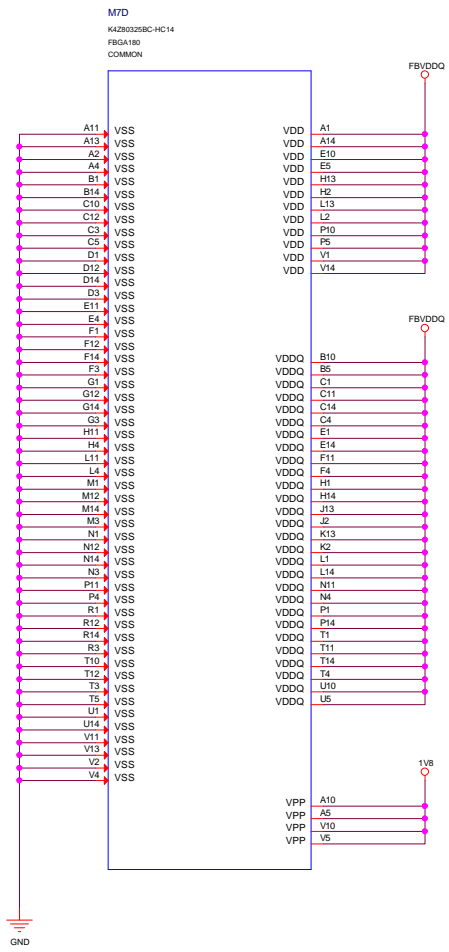
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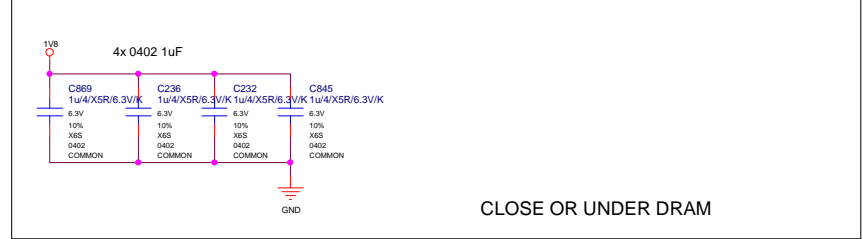
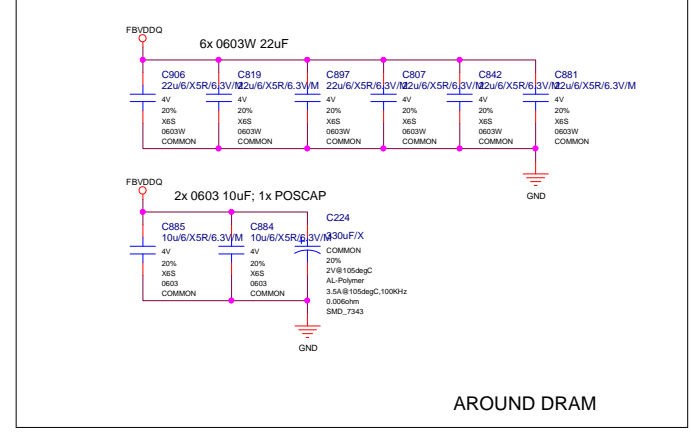
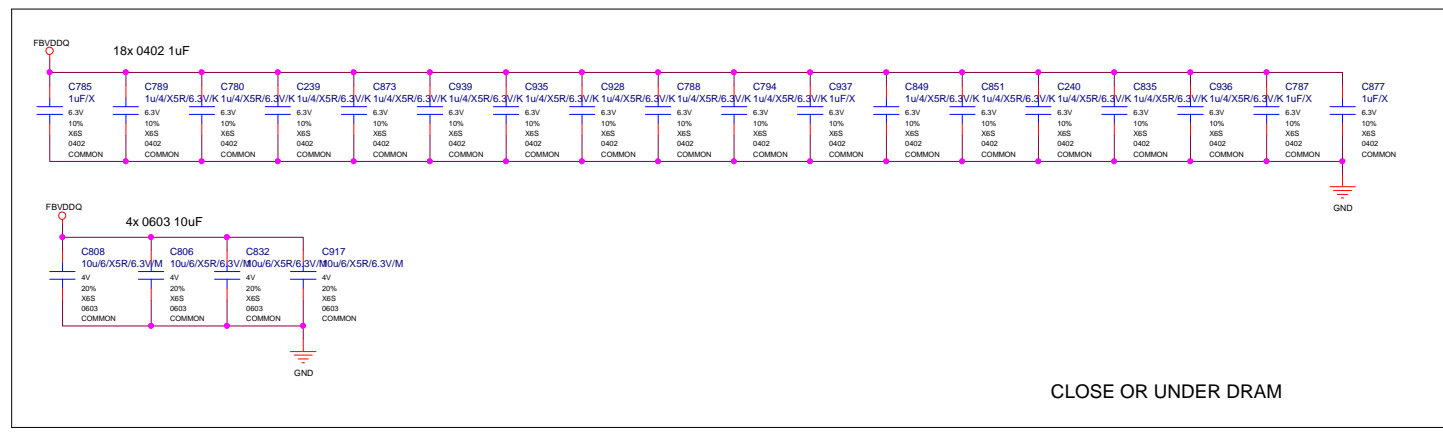
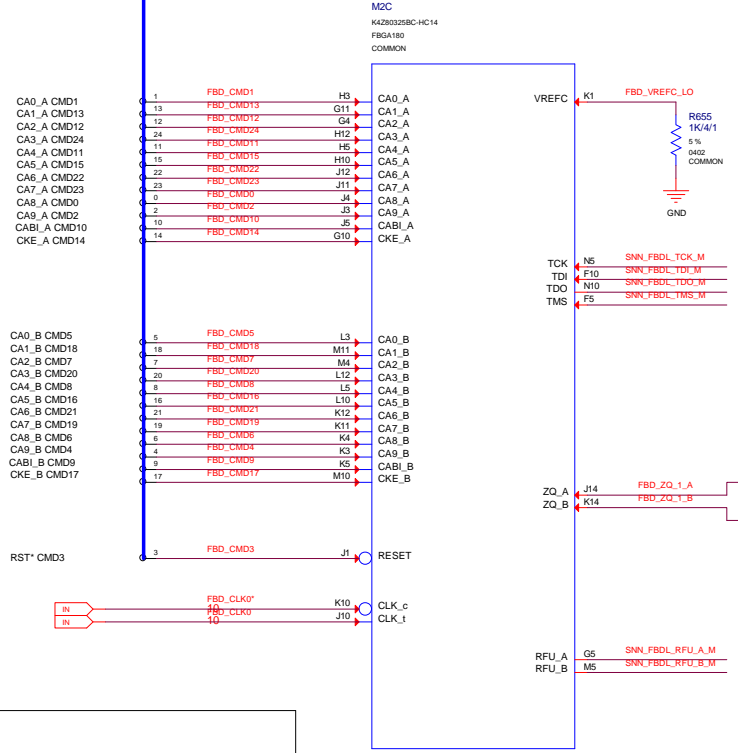
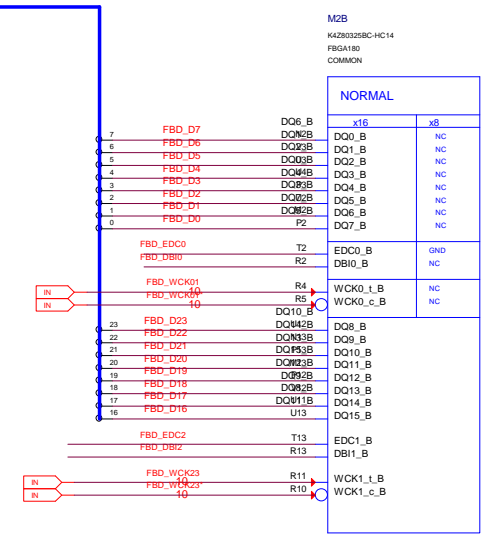
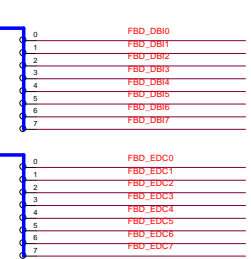
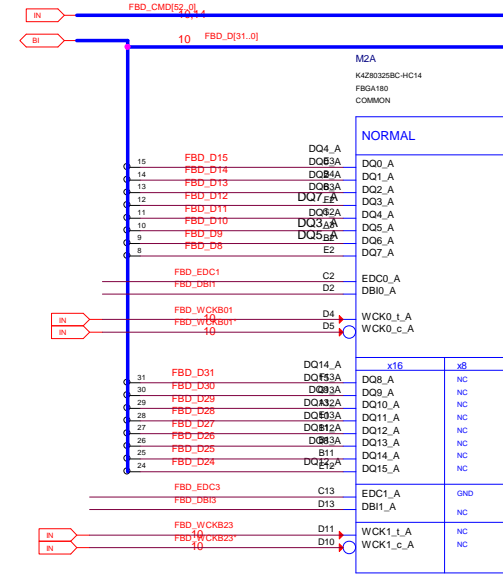
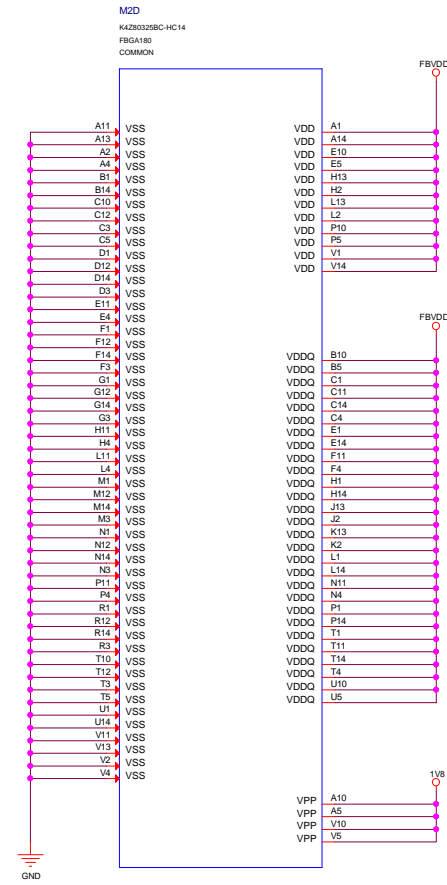


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AROUND DRAM

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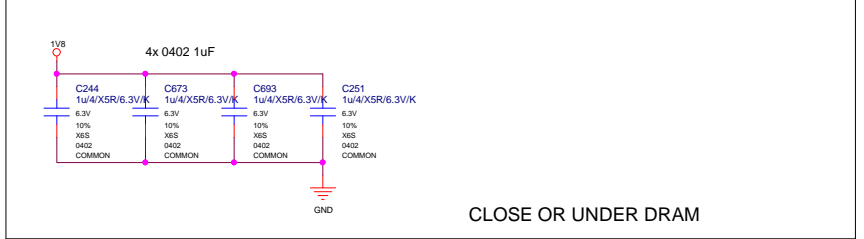
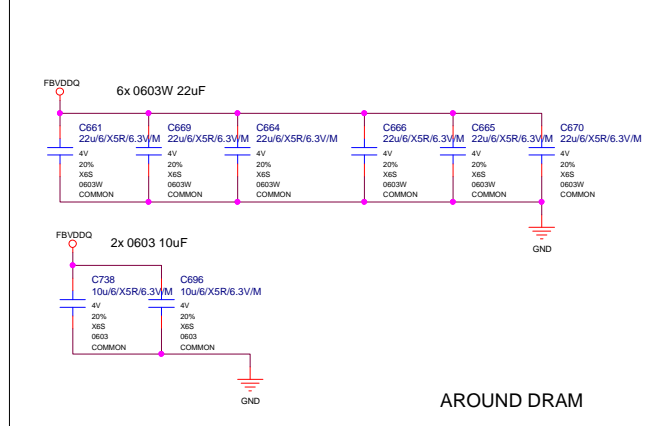
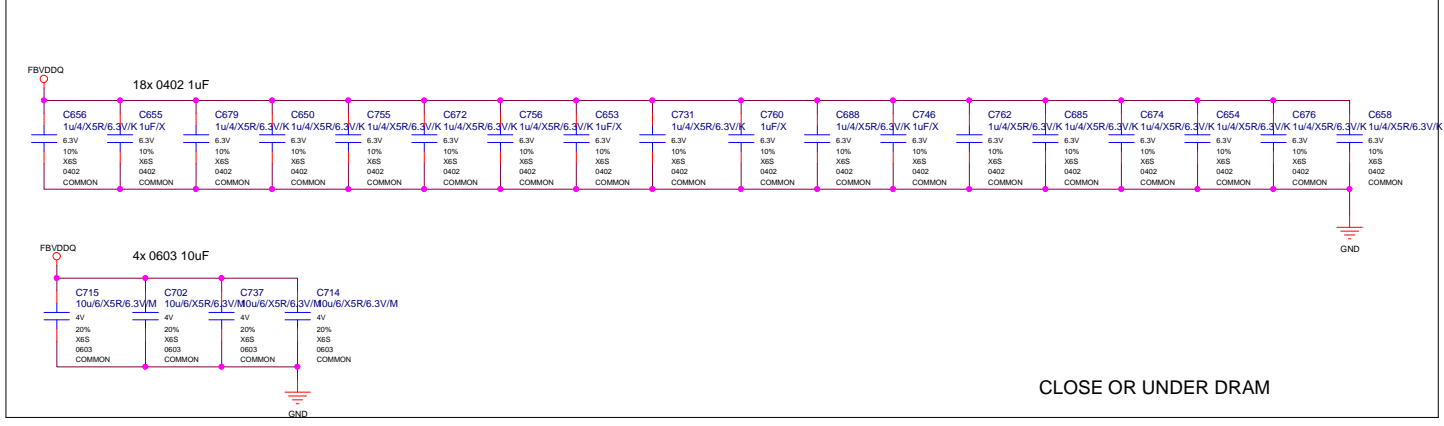
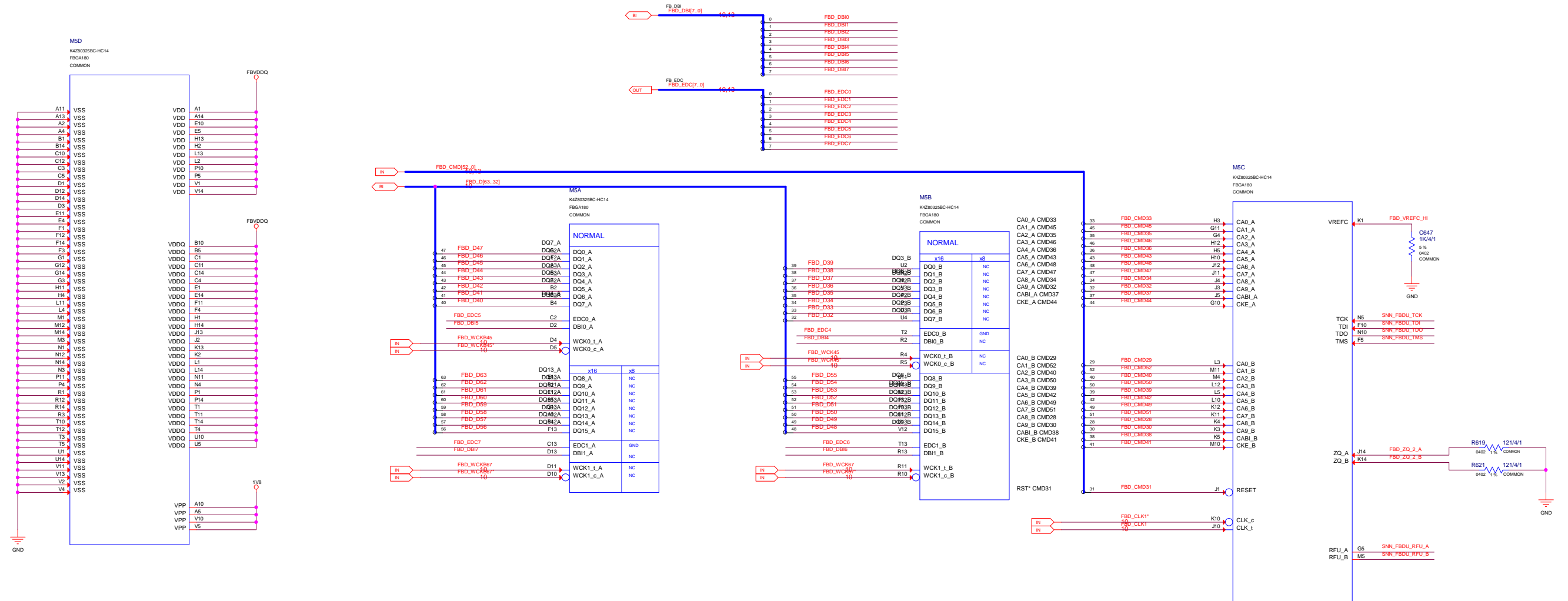


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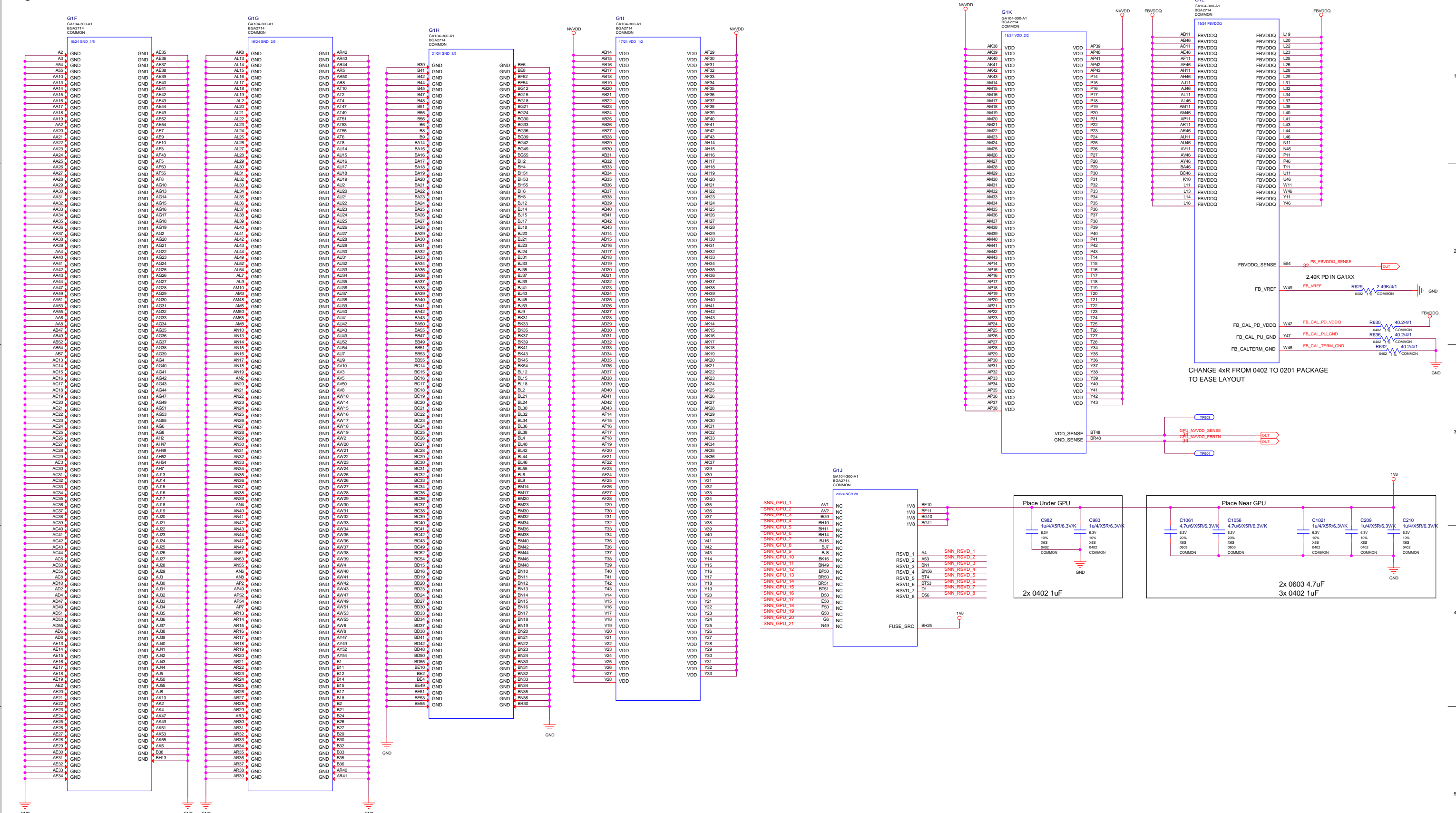
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**GIGABYTE**

Title: **PCIE**

Size: Custom Document Number: **GV-N3060VISION OC-12GD** Rev: 1.01

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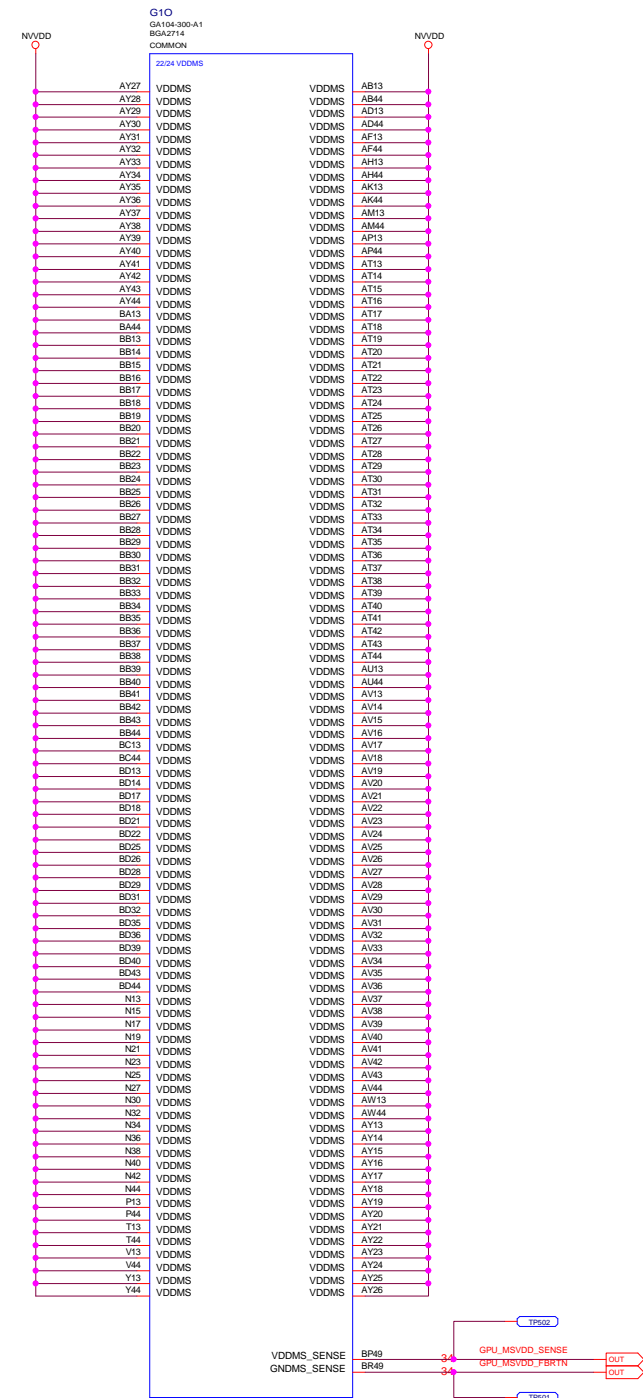
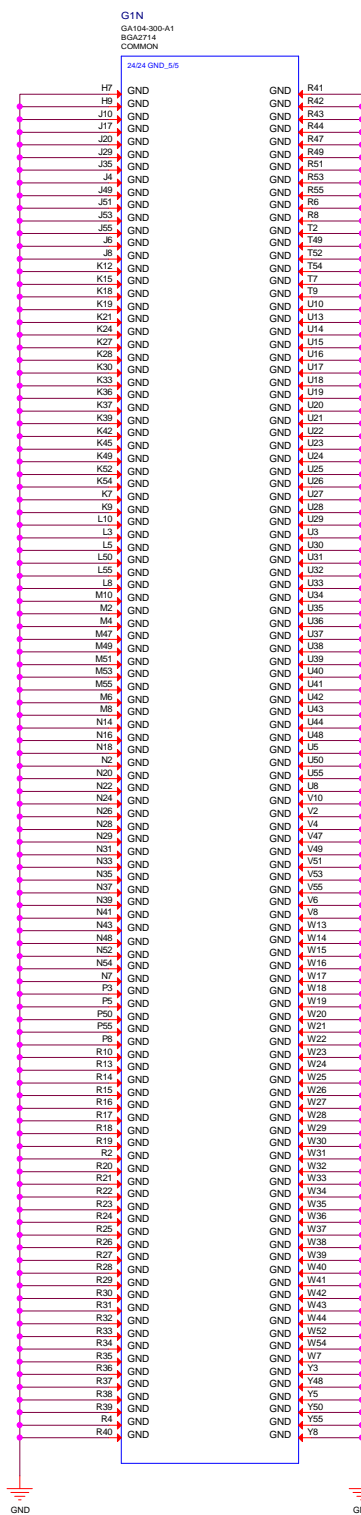
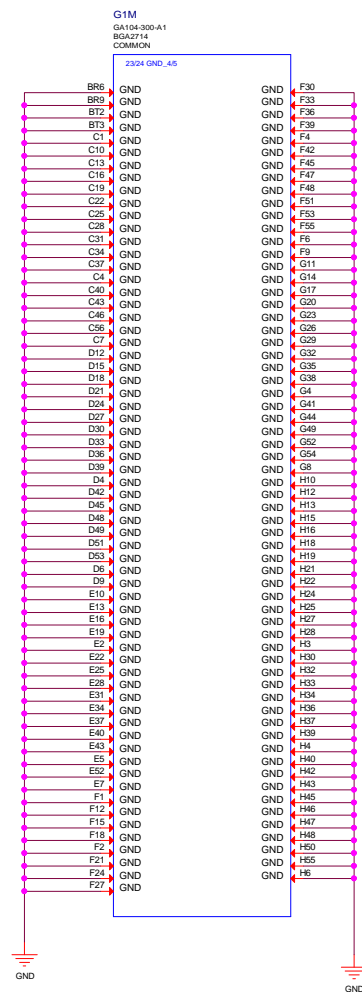
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ASSEMBLY PAGE DETAIL

<ASSEMBLY\_DESCRIPTION>  
GPU PWR and GND

GIGABYTE	
Title	PCIE
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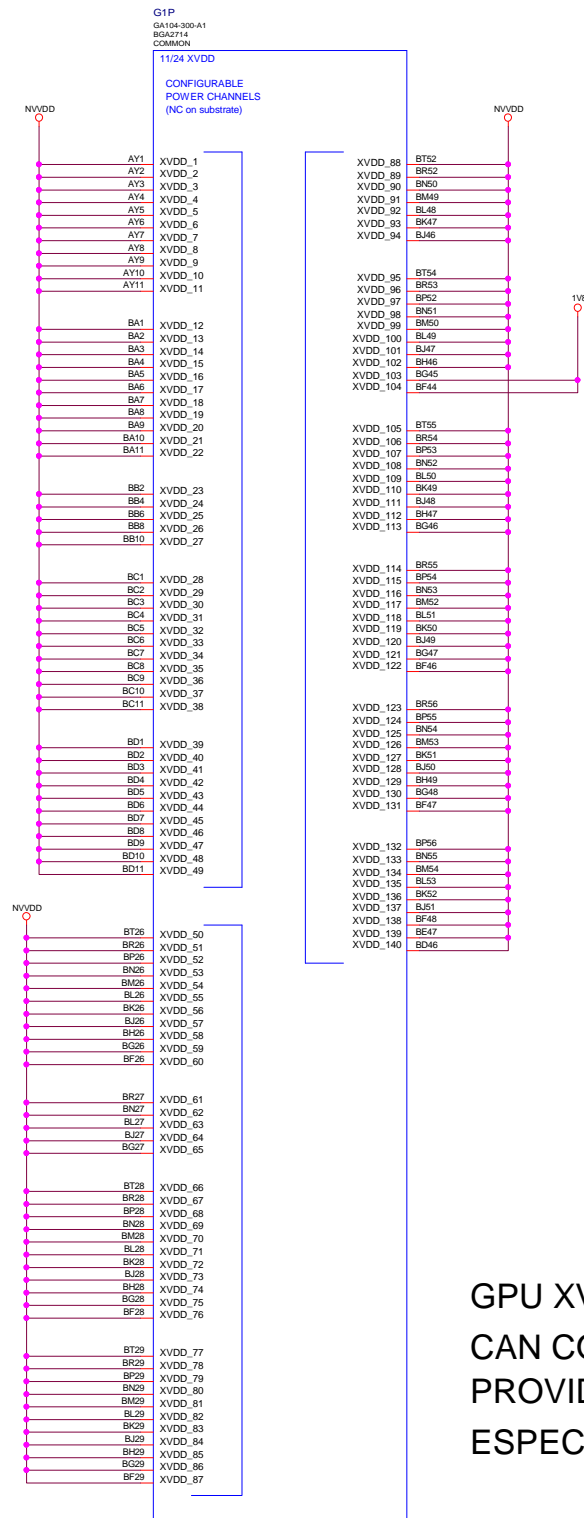


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ASSEMBLY PAGE DETAIL  
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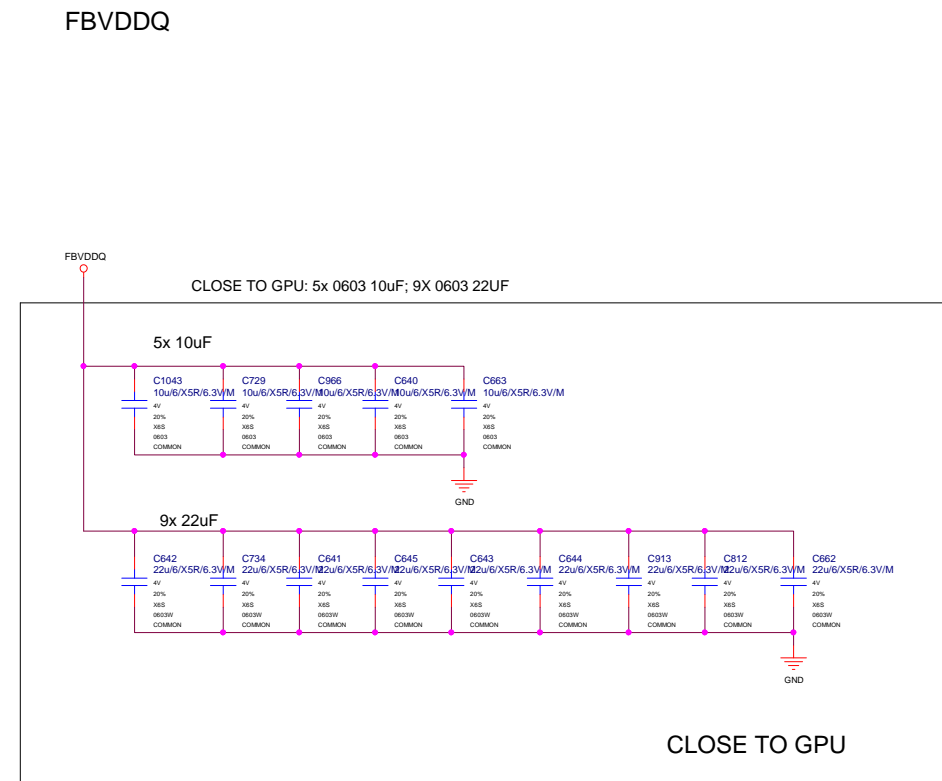
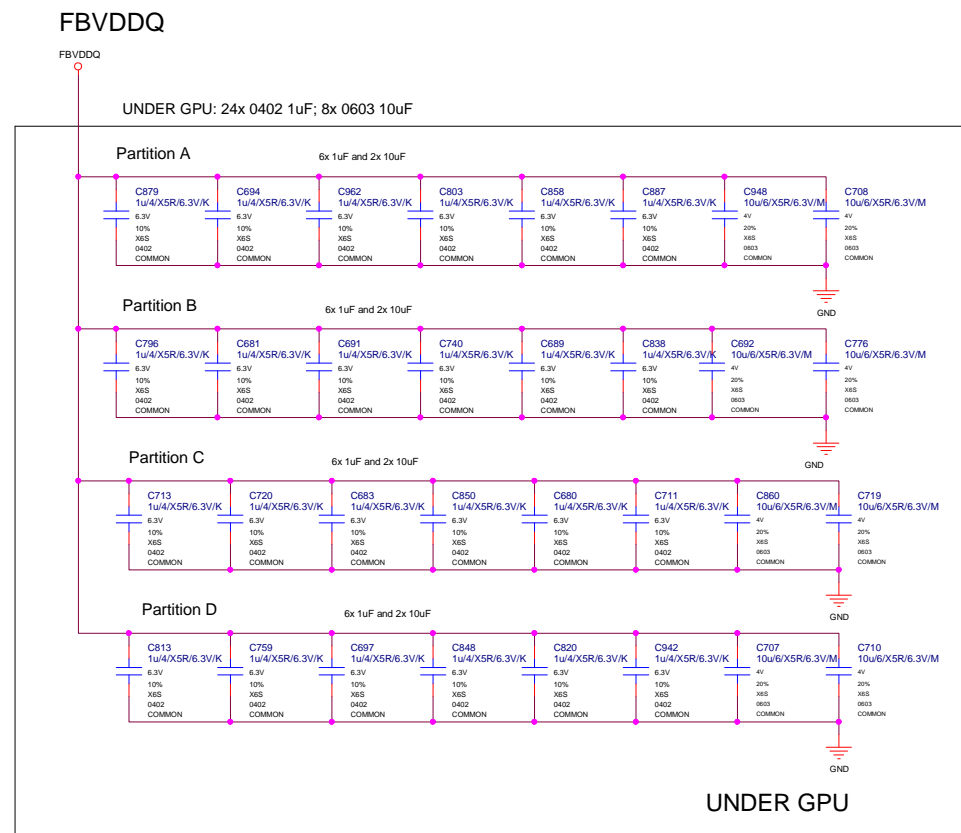
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**GPU XVDD BALLS (NC IN SUBSTRATE):**  
**CAN CONNECT TO ANY POWER NET (NV/MS/1V8/PEX, etc.) ON SYSTEM BOARD,**  
**PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,**  
**ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.**

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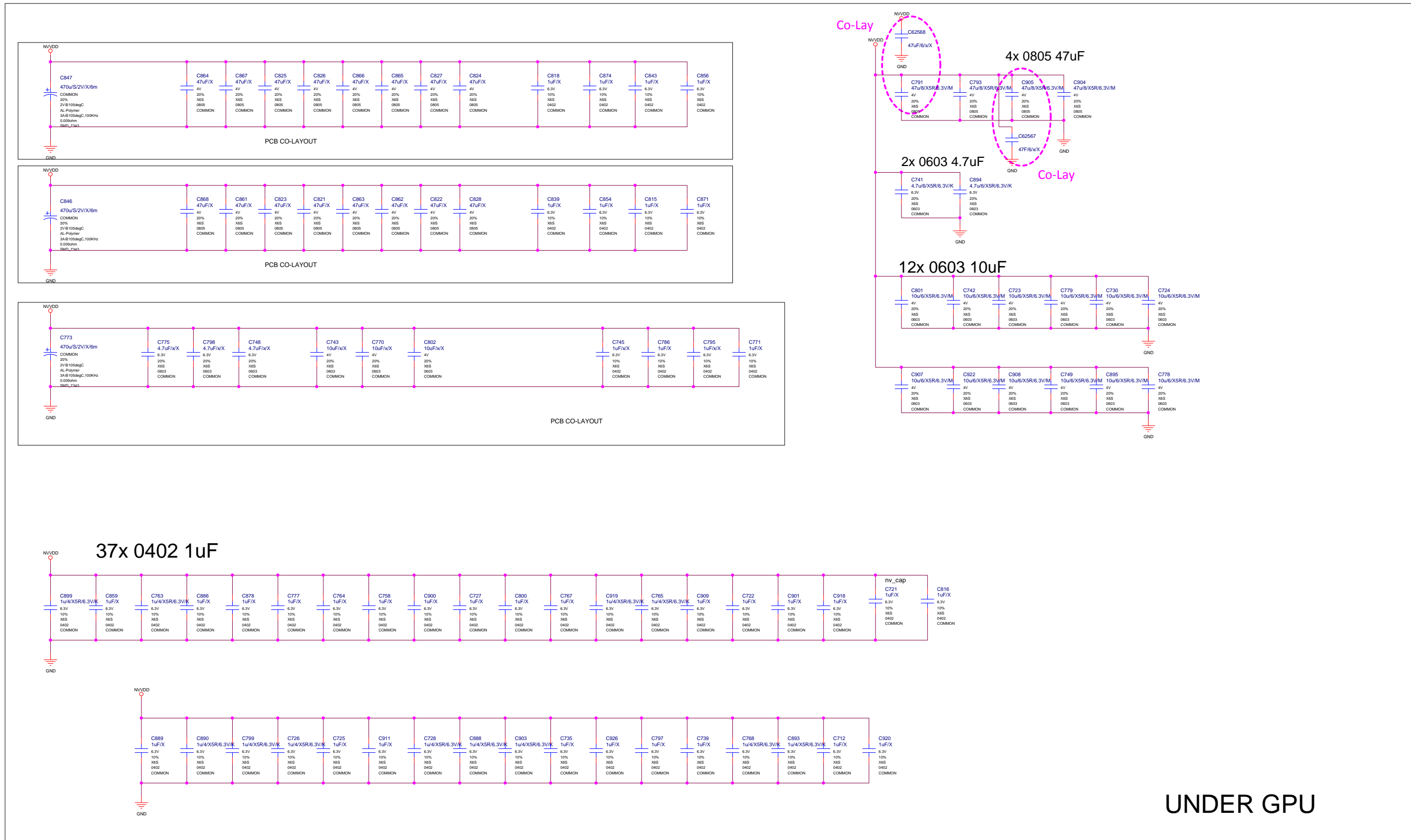


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<b>PCIE</b>			
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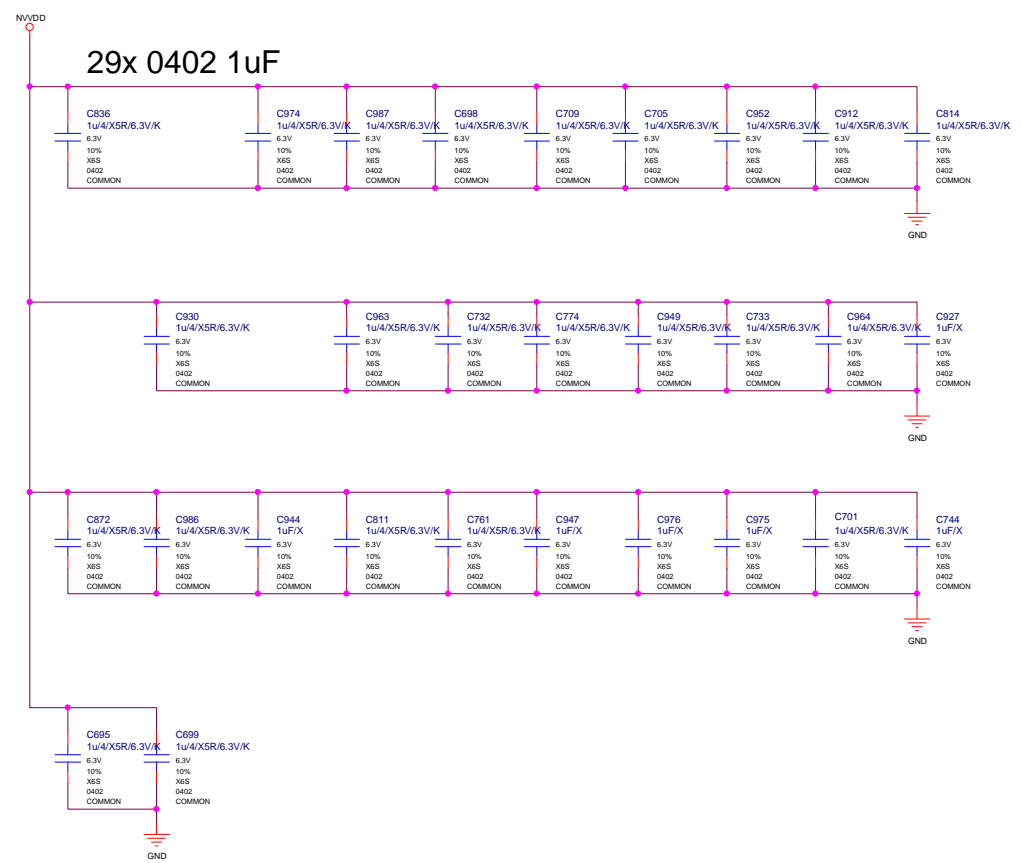
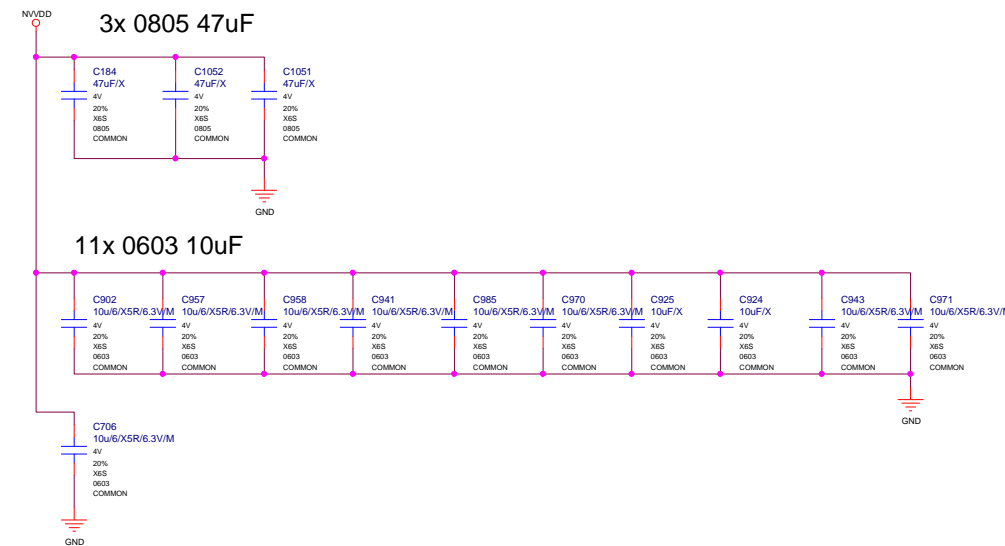
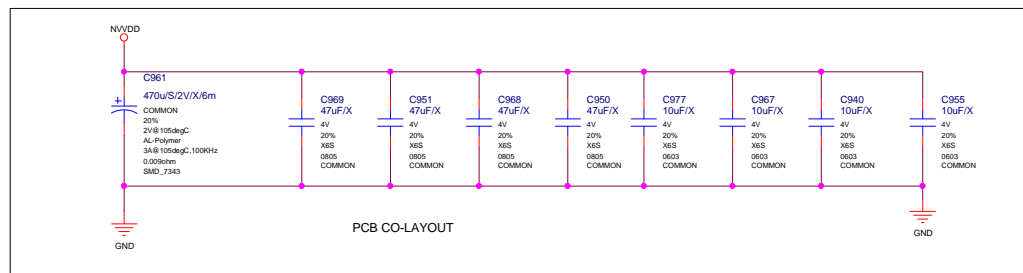


UNDER GPU

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<b>GIGABYTE</b>			
Title <b>PCIE</b>			
Size	Document Number		Rev
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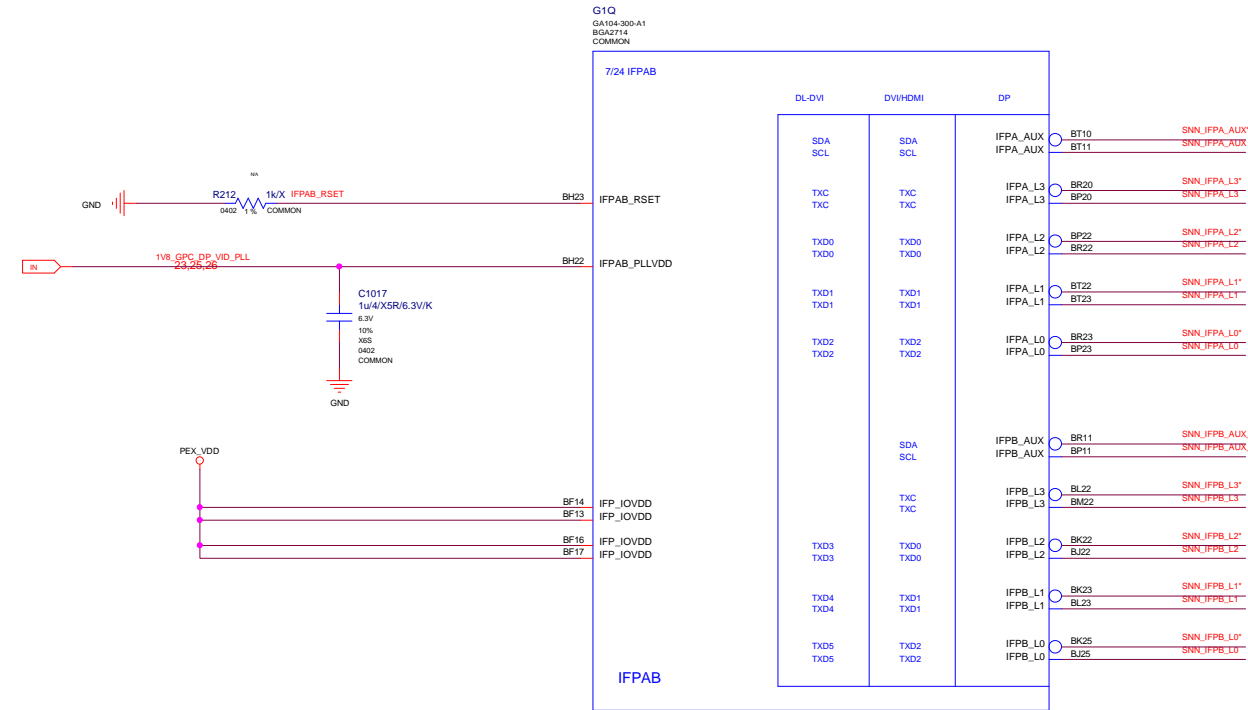


UNDER GPU

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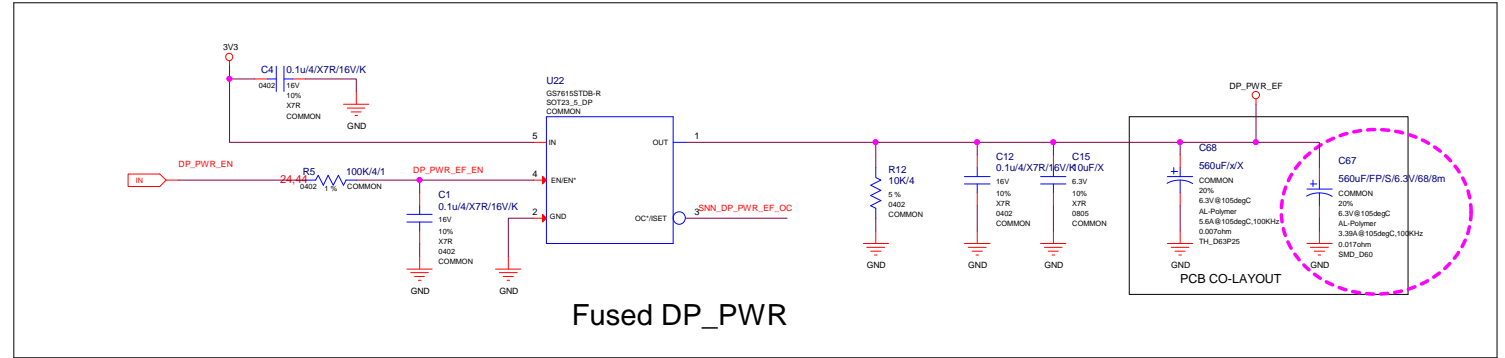
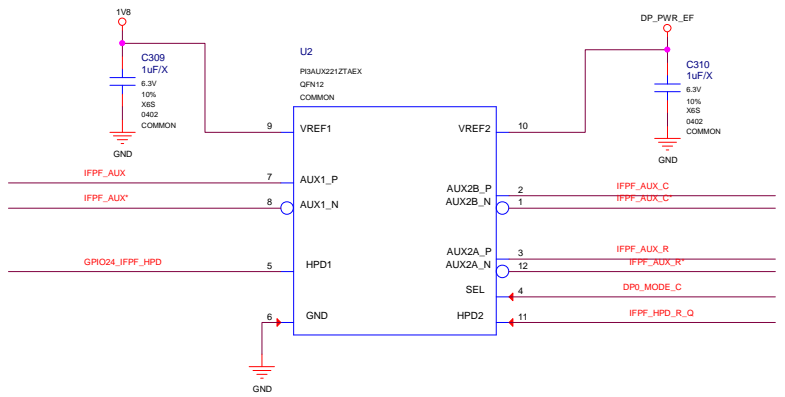
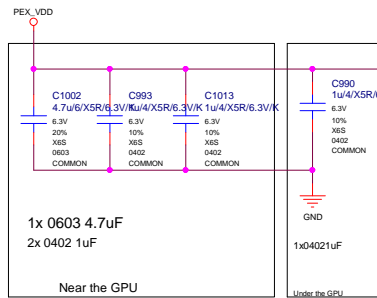
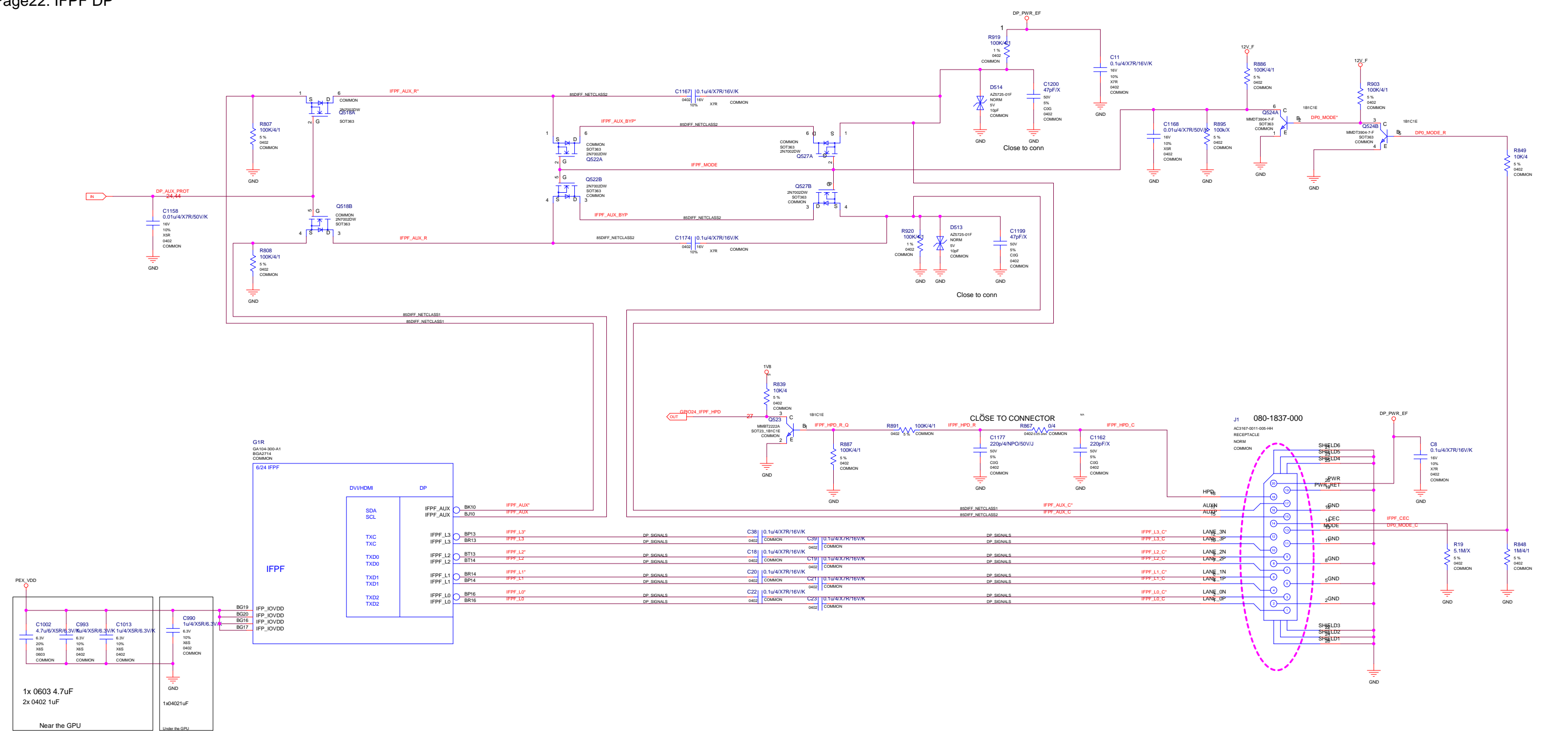
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Title <b>PCIE</b>		
Size Custom	Document Number <b>GV-N3060VISION OC-12GD</b>	Rev 1.01
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 IFPAB DVI-D-DL

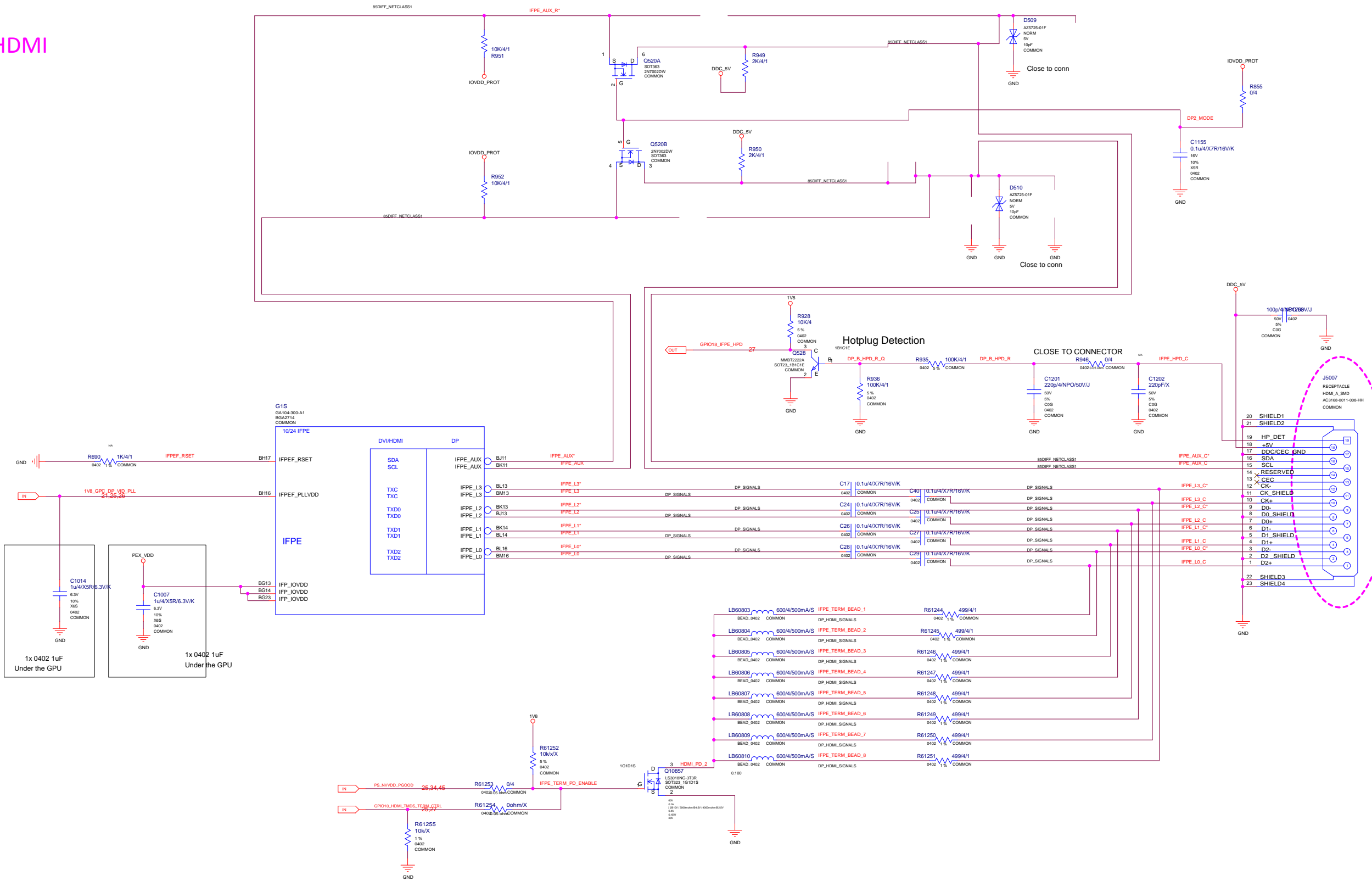
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<b>PCIE</b>			
Size	Document Number	Rev	
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<b>GIGABYTE</b>			
Title	PCIE		
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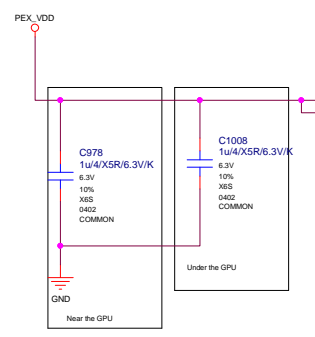
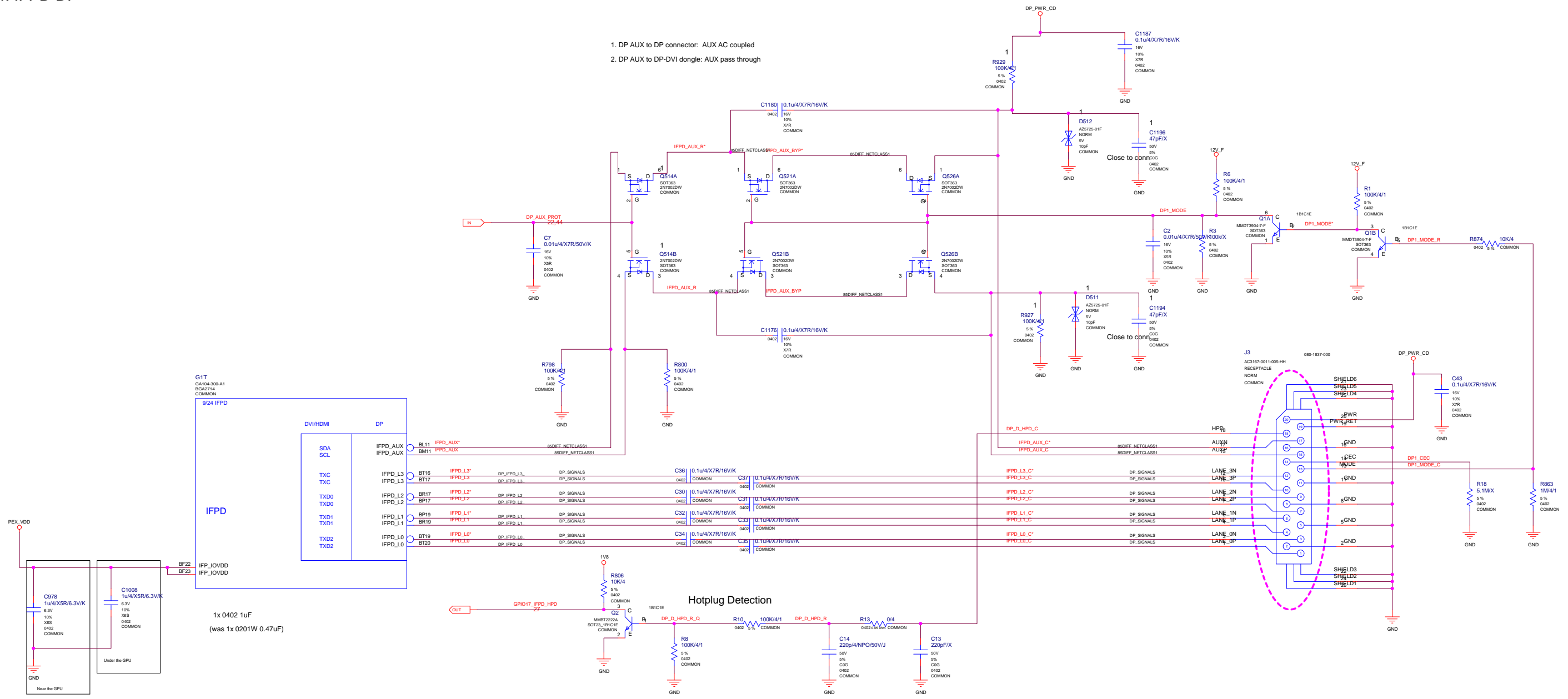
Change to HDMI



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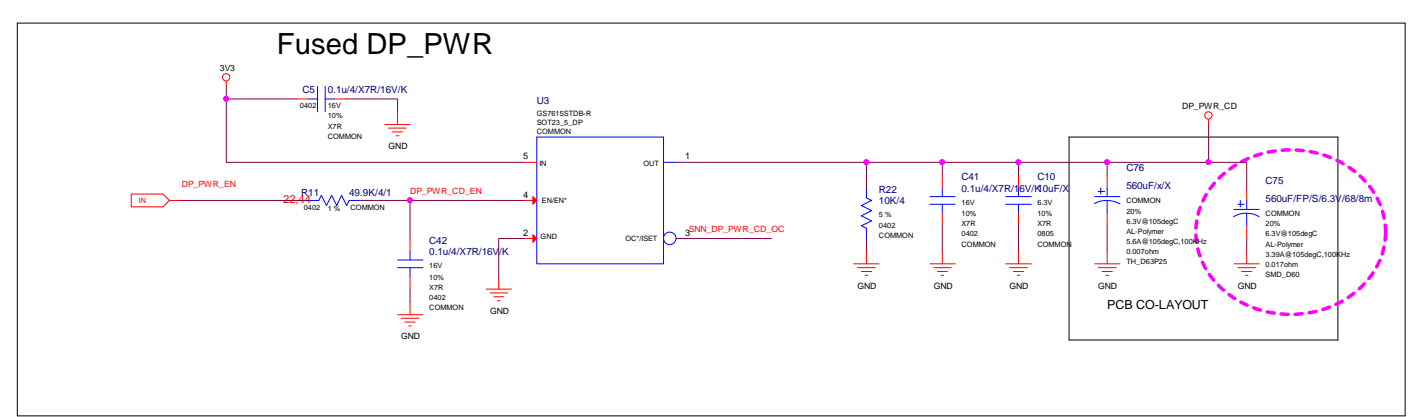
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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



1x 0402 1uF  
(was 1x 0201W 0.47uF)

### Hotplug Detection



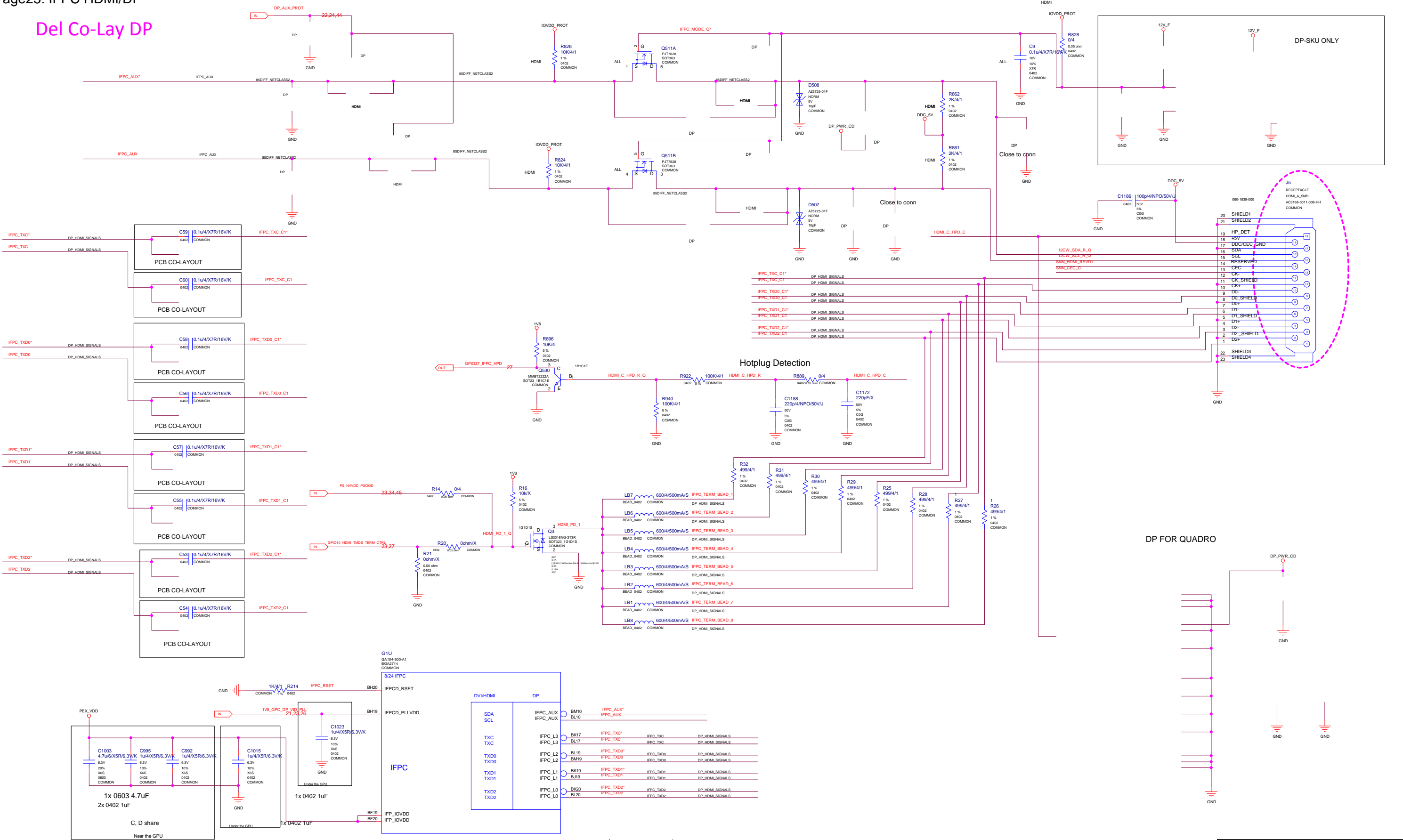
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<b>GIGABYTE</b>			
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Del Co-Lay DP



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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M

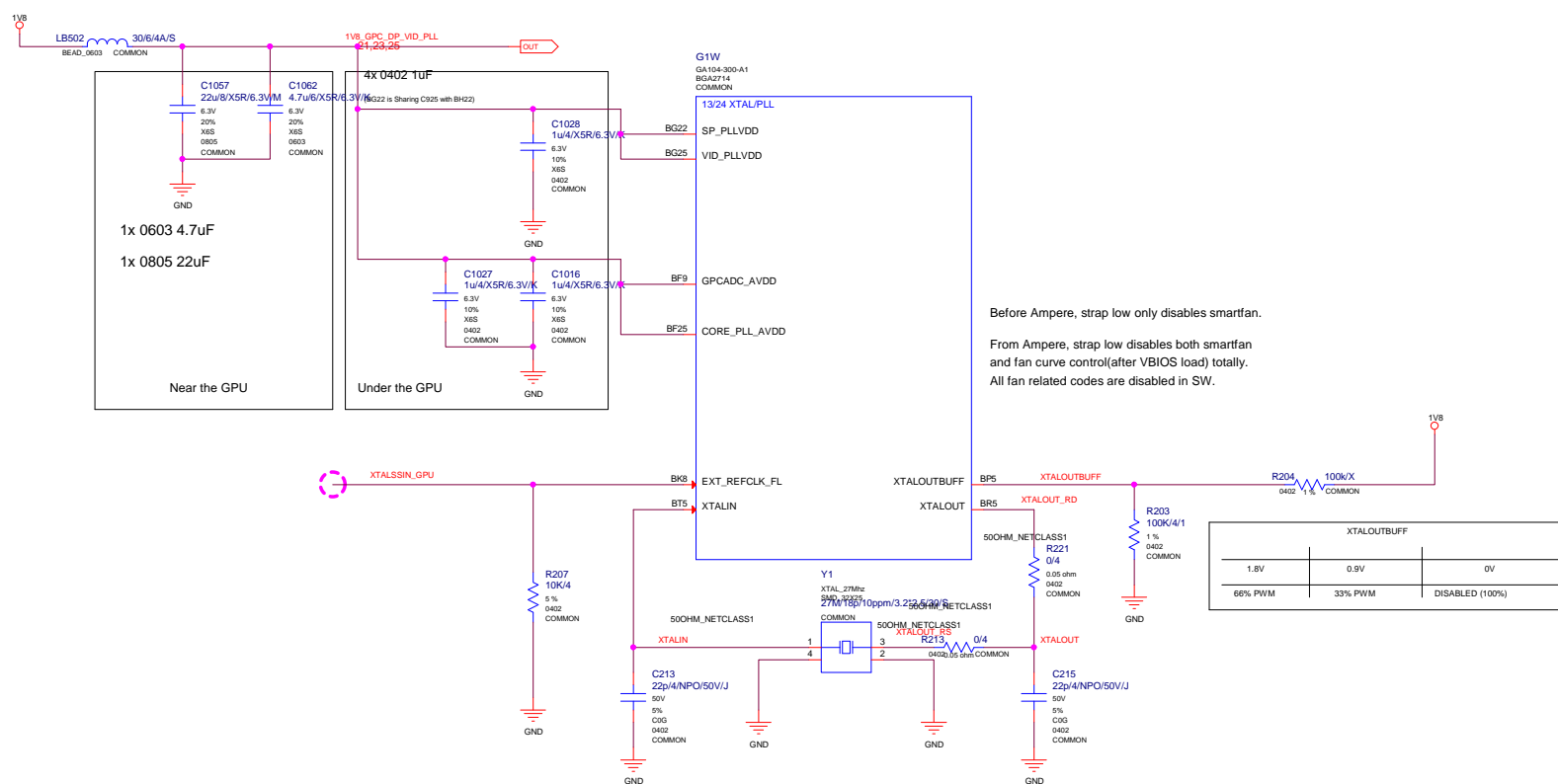
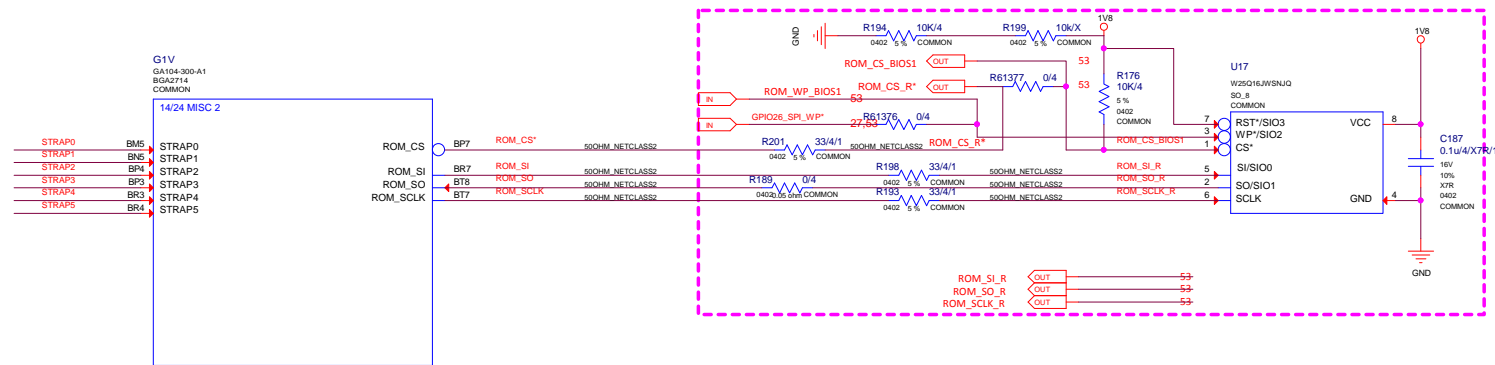
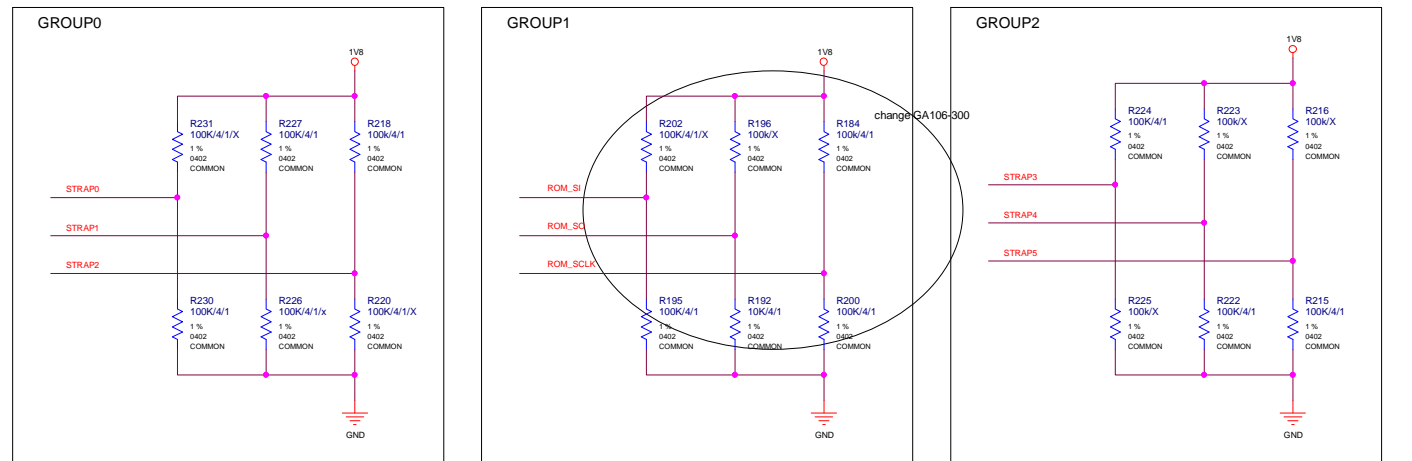
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	4'd7	FS_OVERT ENABLE
L	M	L	4'd9	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

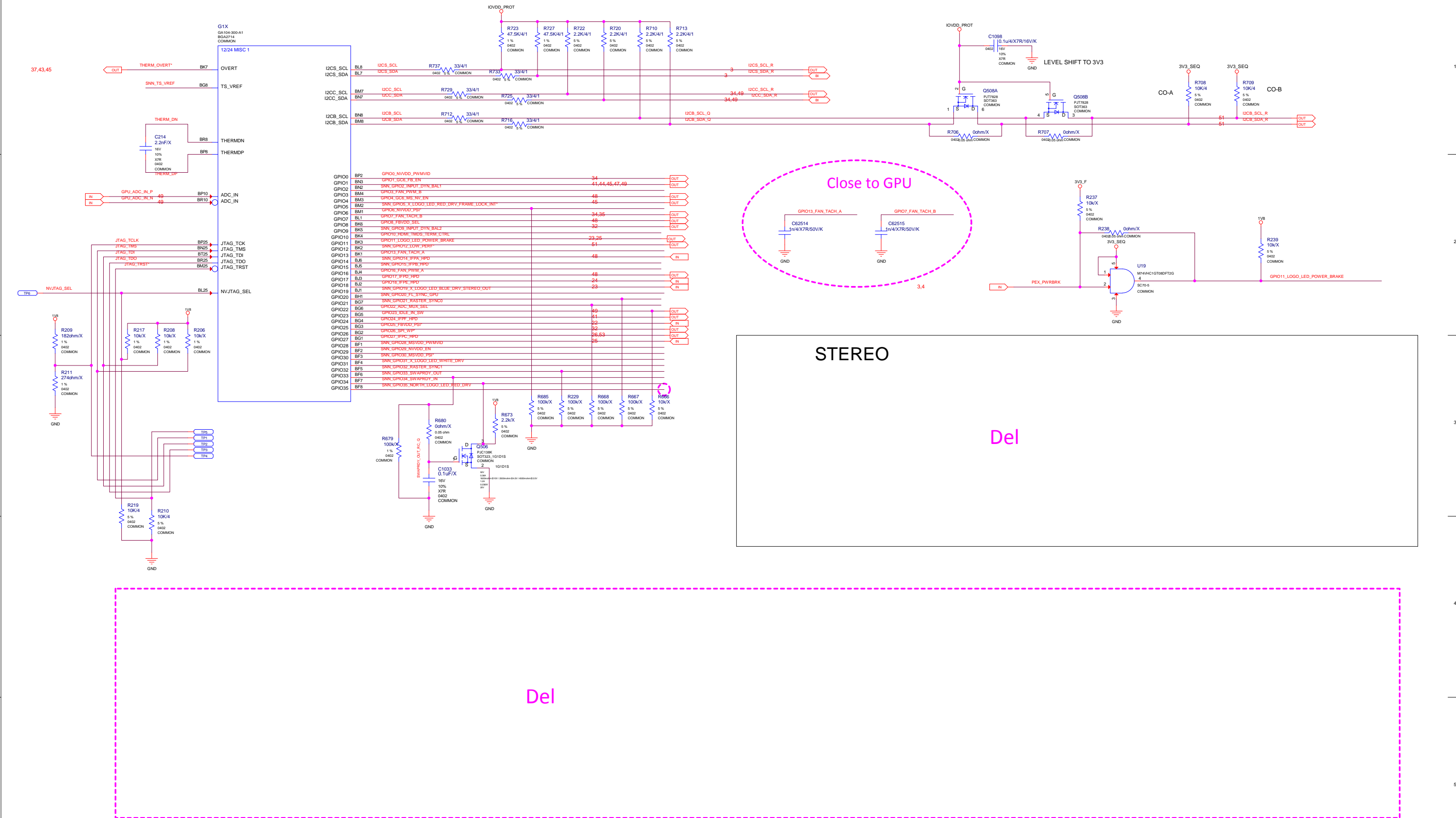
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



Before Ampere, strap low only disables smartfan.  
From Ampere, strap low disables both smartfan and fan curve control(after VBIOS load) totally.  
All fan related codes are disabled in SW.



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PAGE DETAIL

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Title <b>PCIE</b>		
Size	Document Number	Rev
Custom	<b>GV-N3060VISION OC-12GD</b>	1.01
Date:	Thursday, January 14, 2021	Sheet 28 of 54

A

B

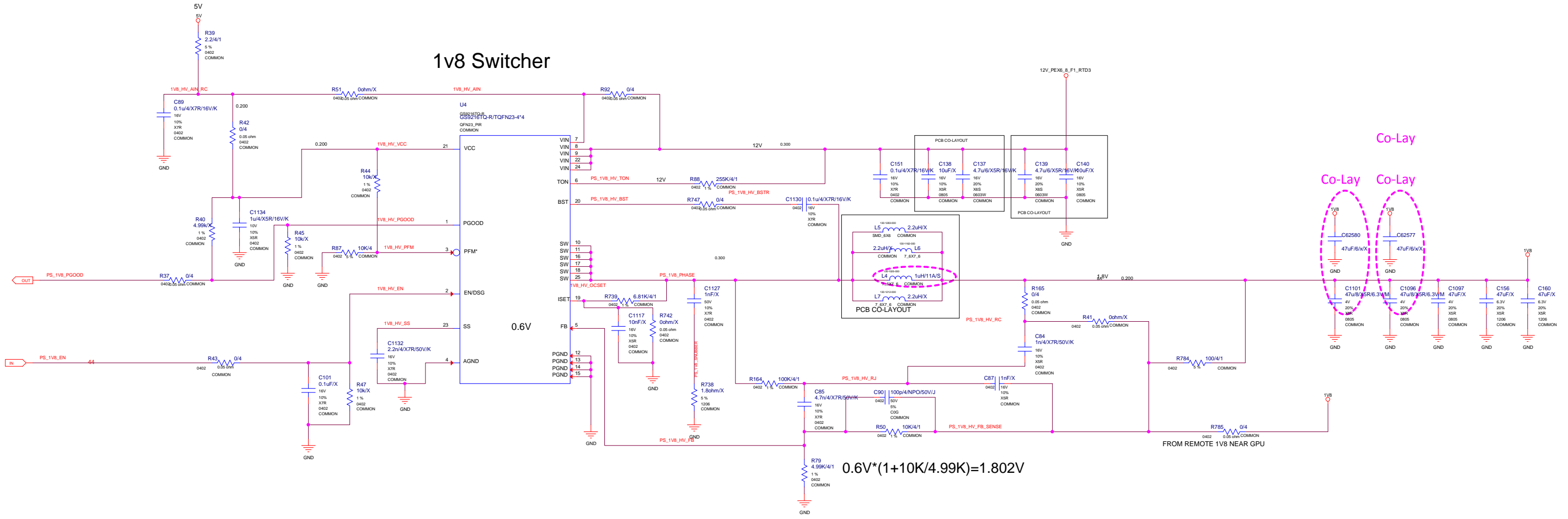
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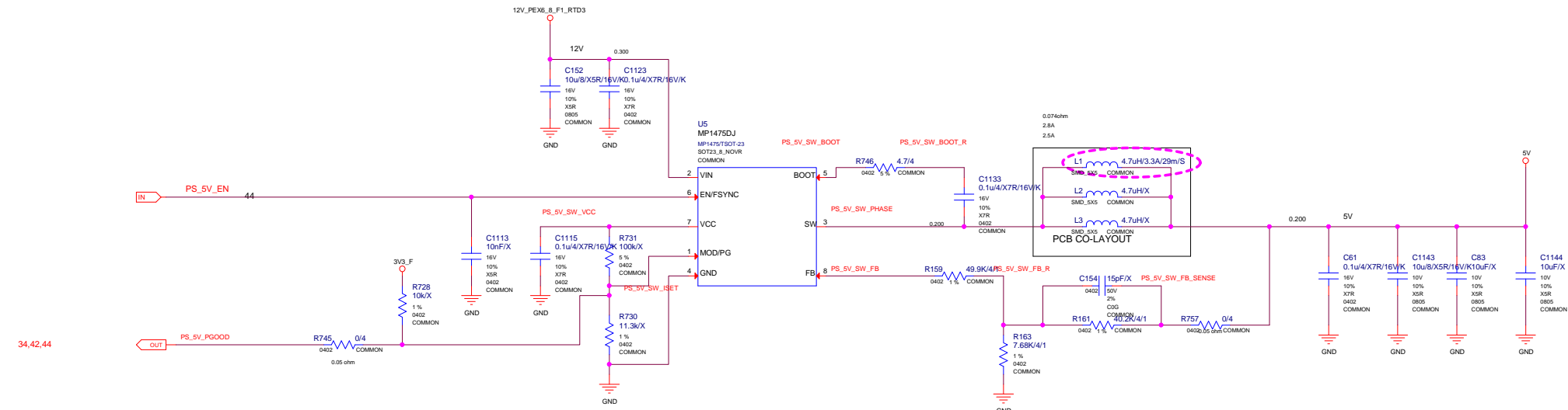
Co-Lay  
Co-Lay  
Co-Lay

$0.6V * (1 + 10K/4.99K) = 1.802V$

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<b>GIGABYTE</b>			
Title <b>PCIE</b>			
Size Custom	Document Number <b>GV-N3060VISION OC-12GD</b>		Rev 1.01
Date: Thursday, January 14, 2021	Sheet 29	of 54	



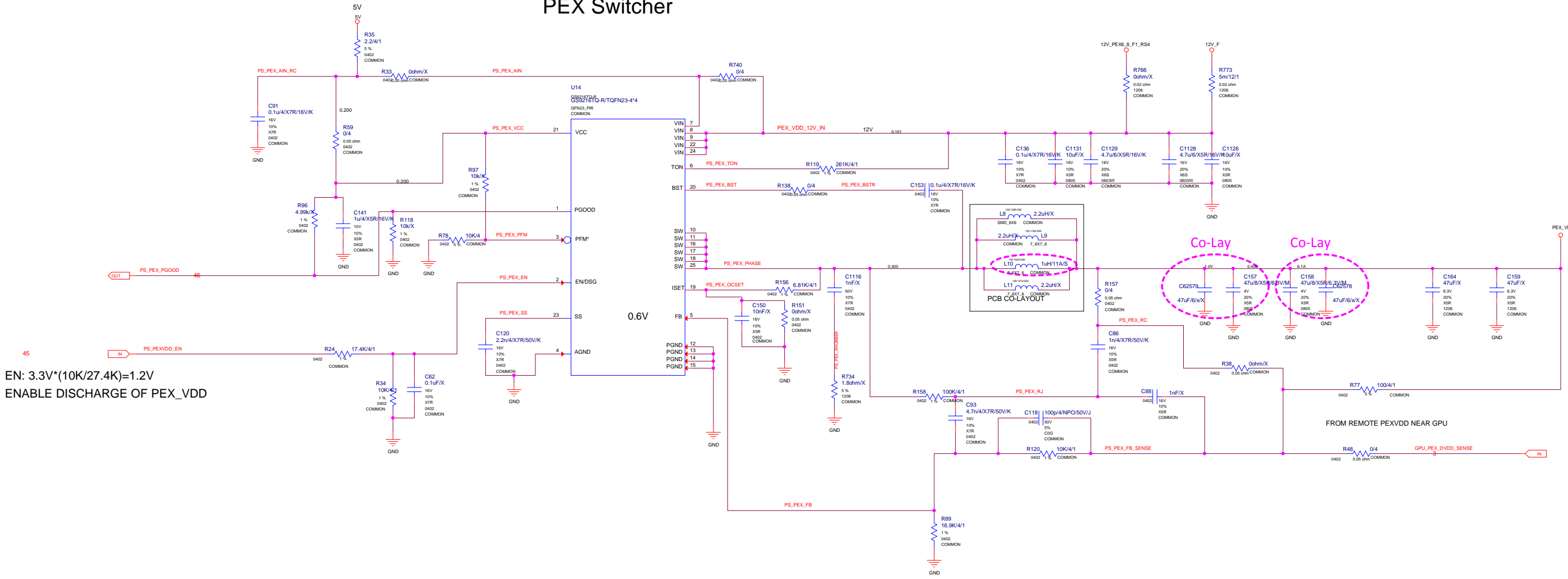
$$0.8V * (1 + 40.2K/7.68K) = 4.9875V$$

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Size	Document Number	Rev	1.01
Custom	GV-N3060VISION OC-12GD		
Date:	Thursday, January 14, 2021	Sheet	30 of 54

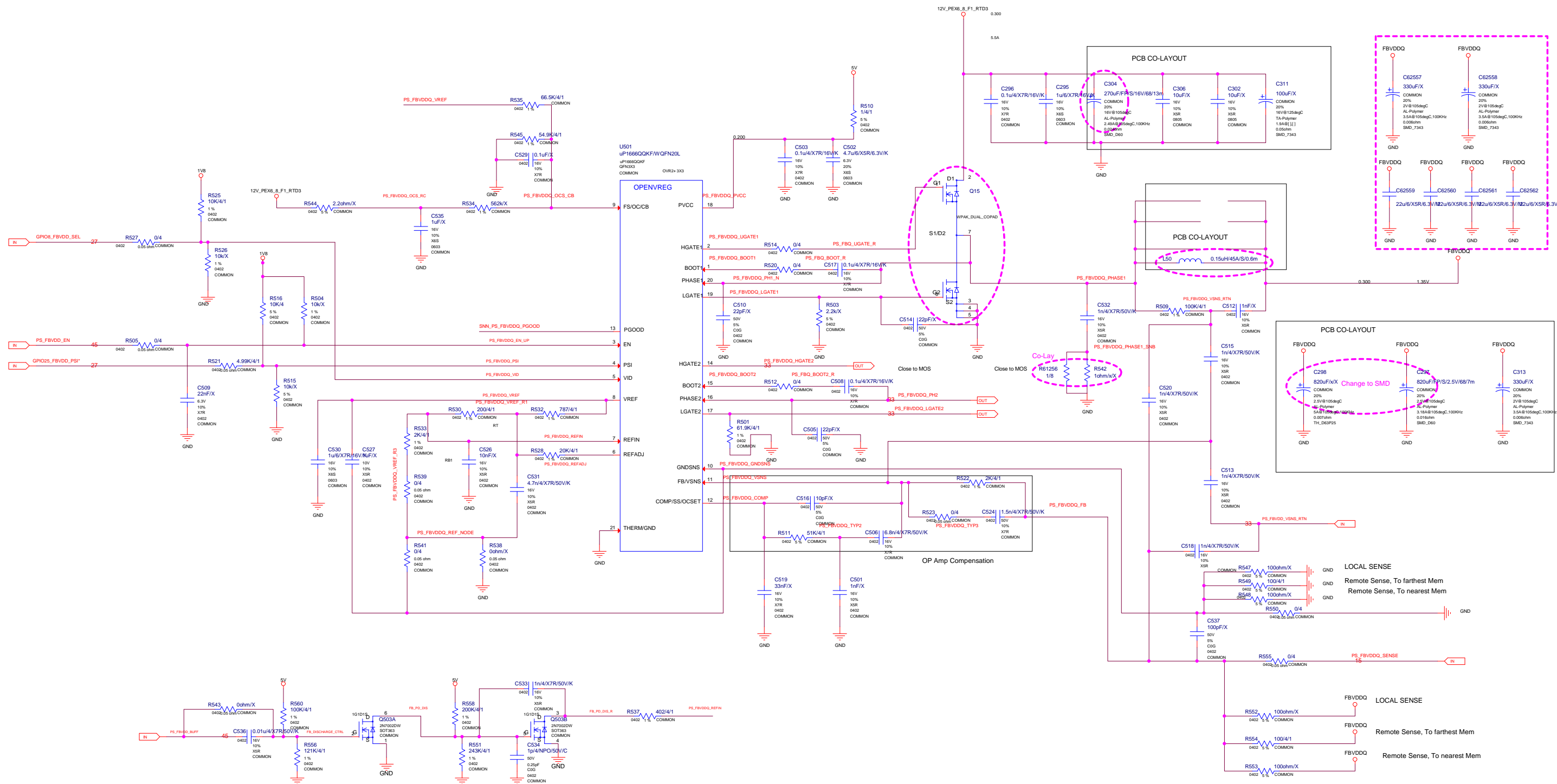
# PEX Switcher



EN:  $3.3V * (10K/27.4K) = 1.2V$   
 ENABLE DISCHARGE OF PEX\_VDD

$0.6V * (1 + 10K/16.9K) = 0.9550V$

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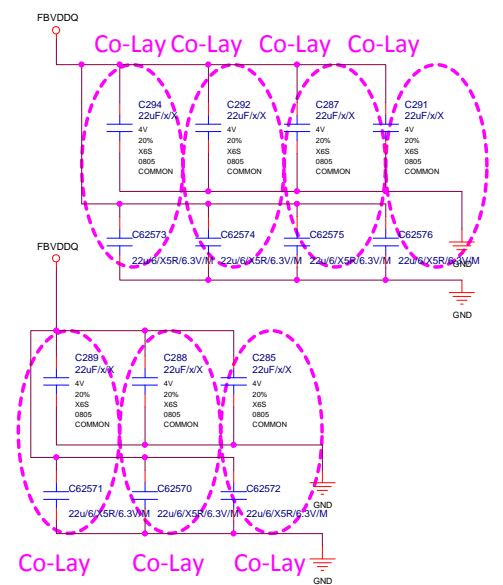
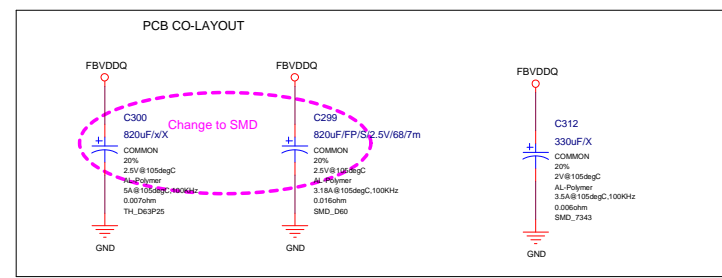
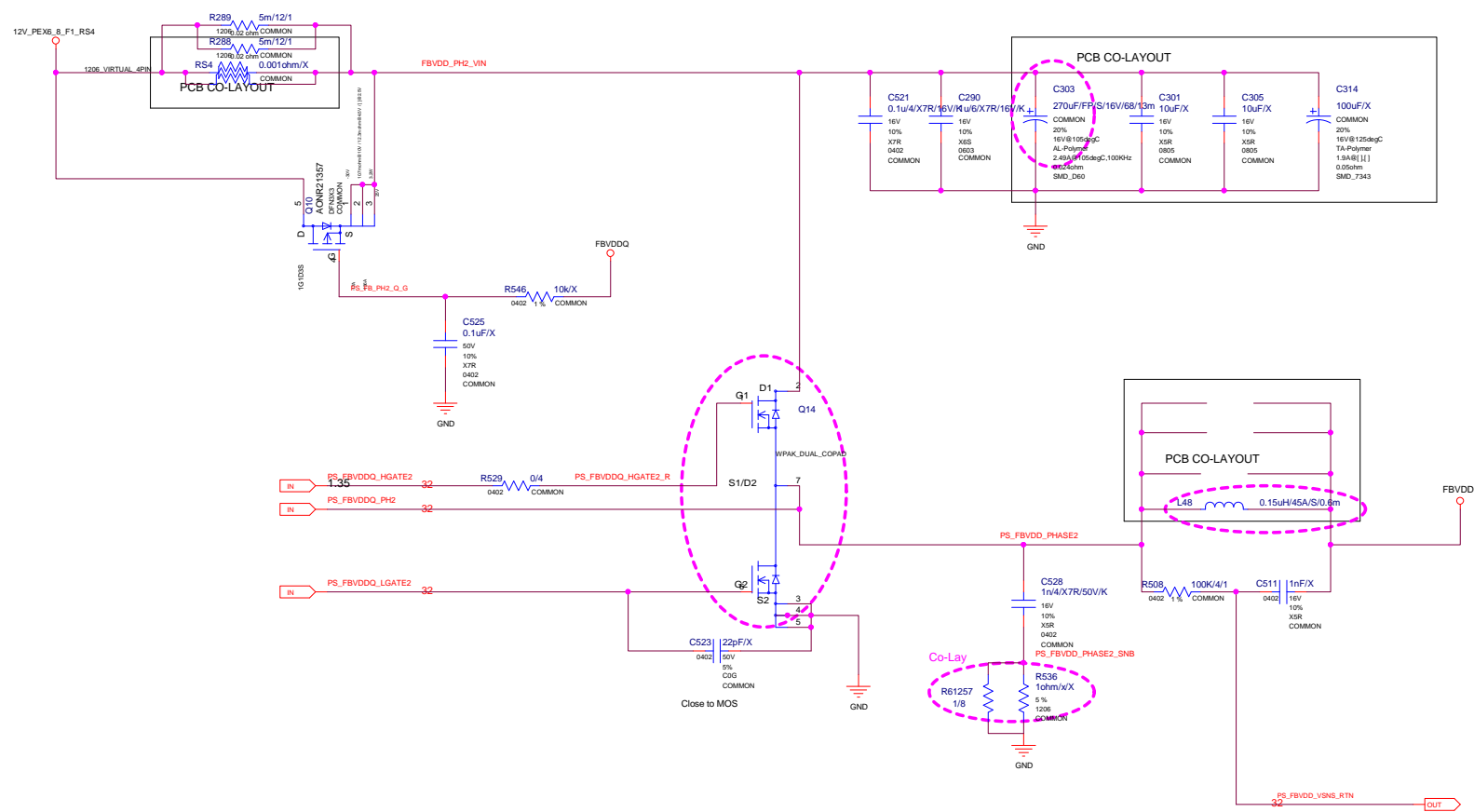
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ASSEMBLY PAGE DETAIL  
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<b>GIGABYTE</b>		
Title	PCIE	
Size	Document Number	Rev
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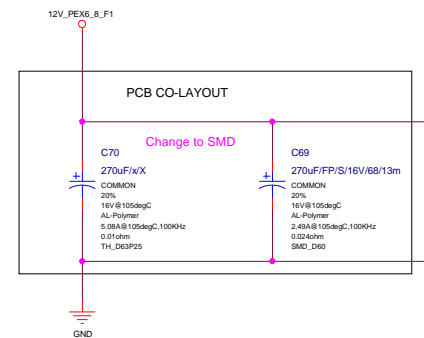
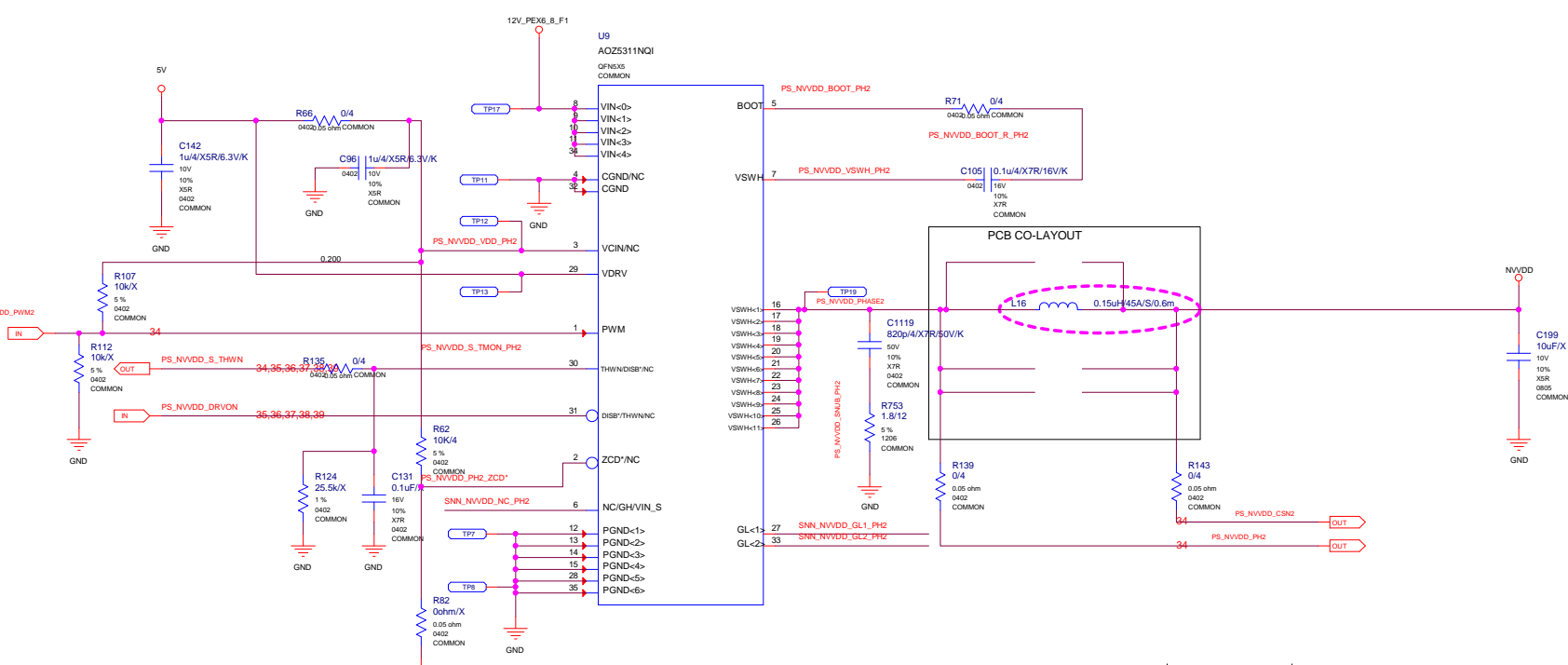
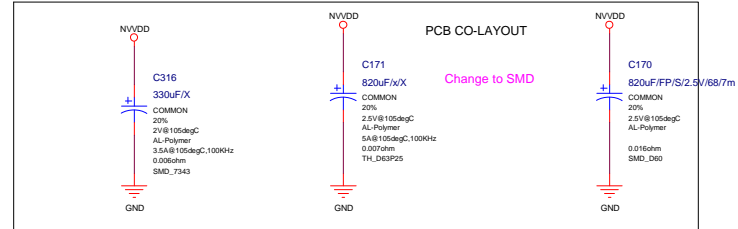
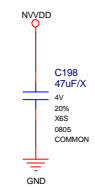
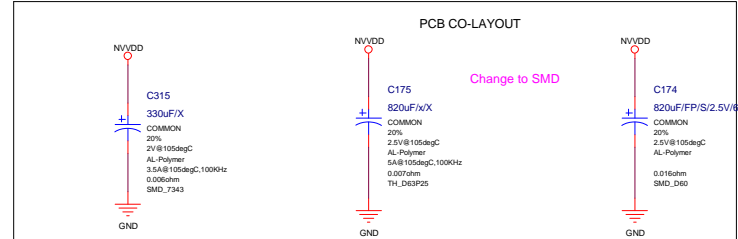
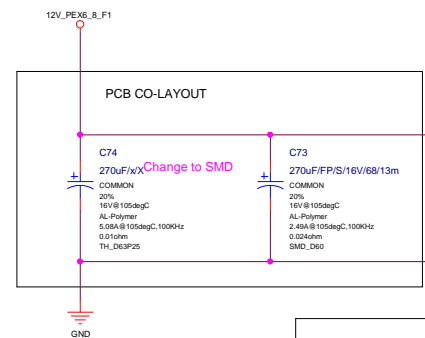
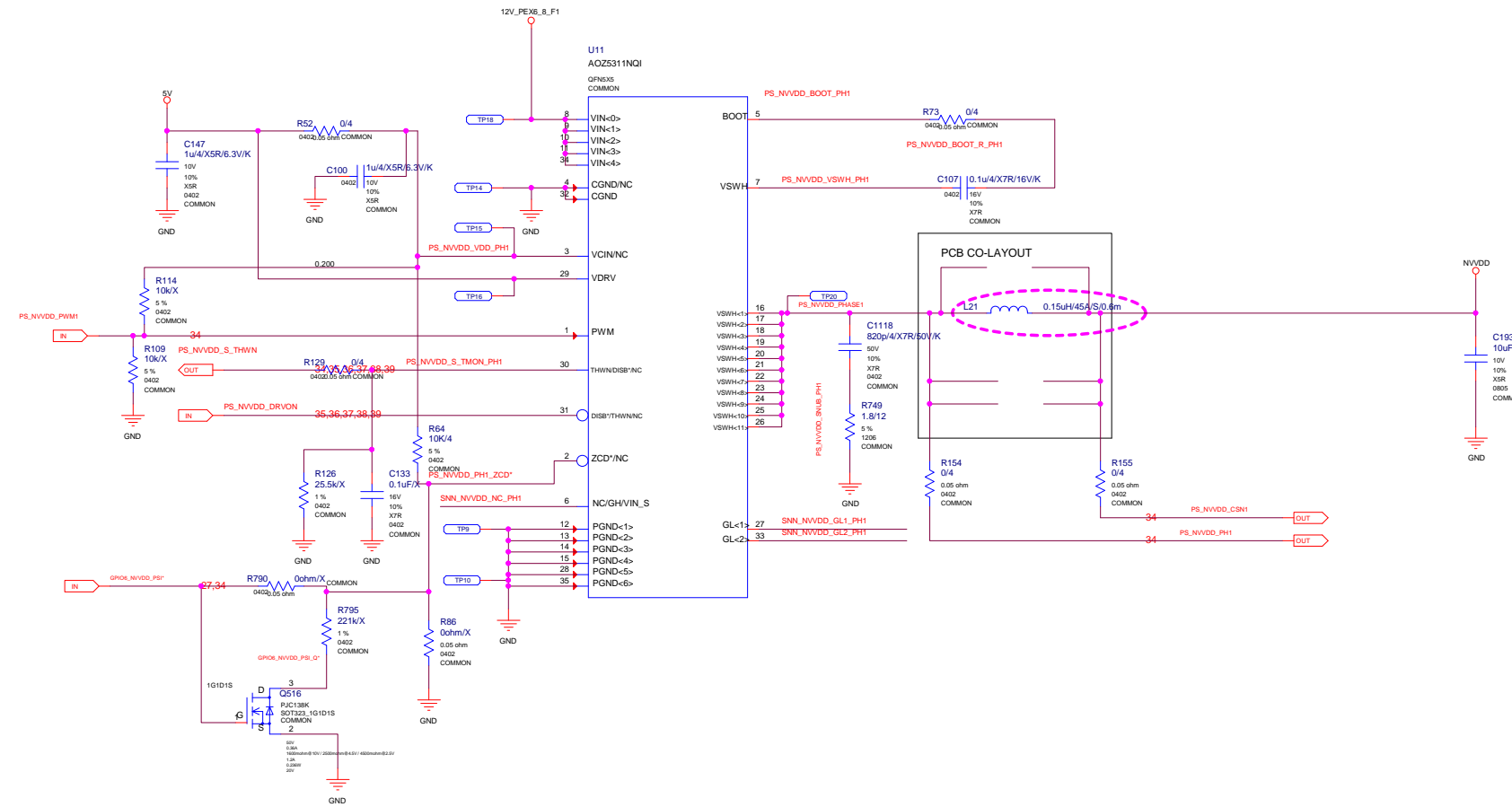
FBVDD PH2 INPUT ANTI-BACKDRIVE



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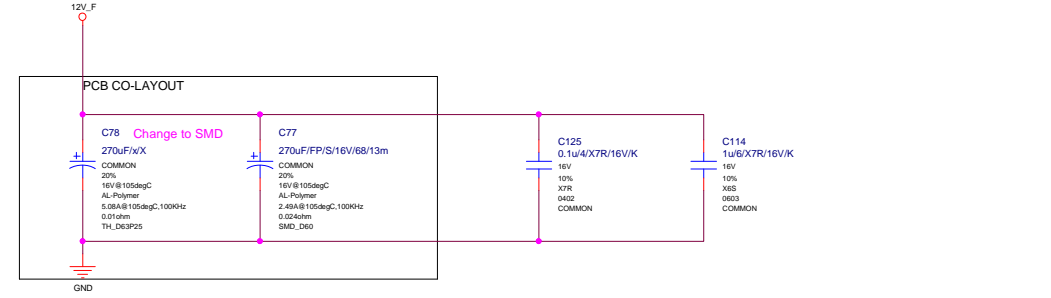
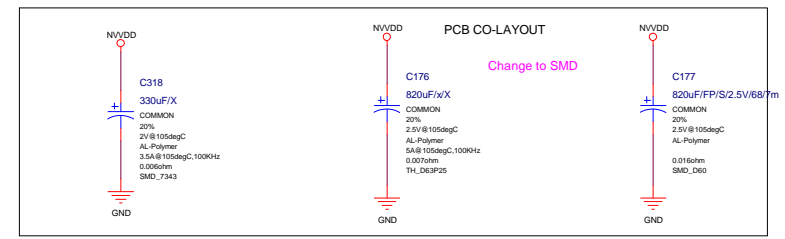
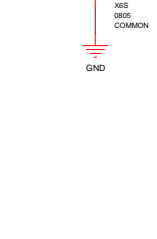
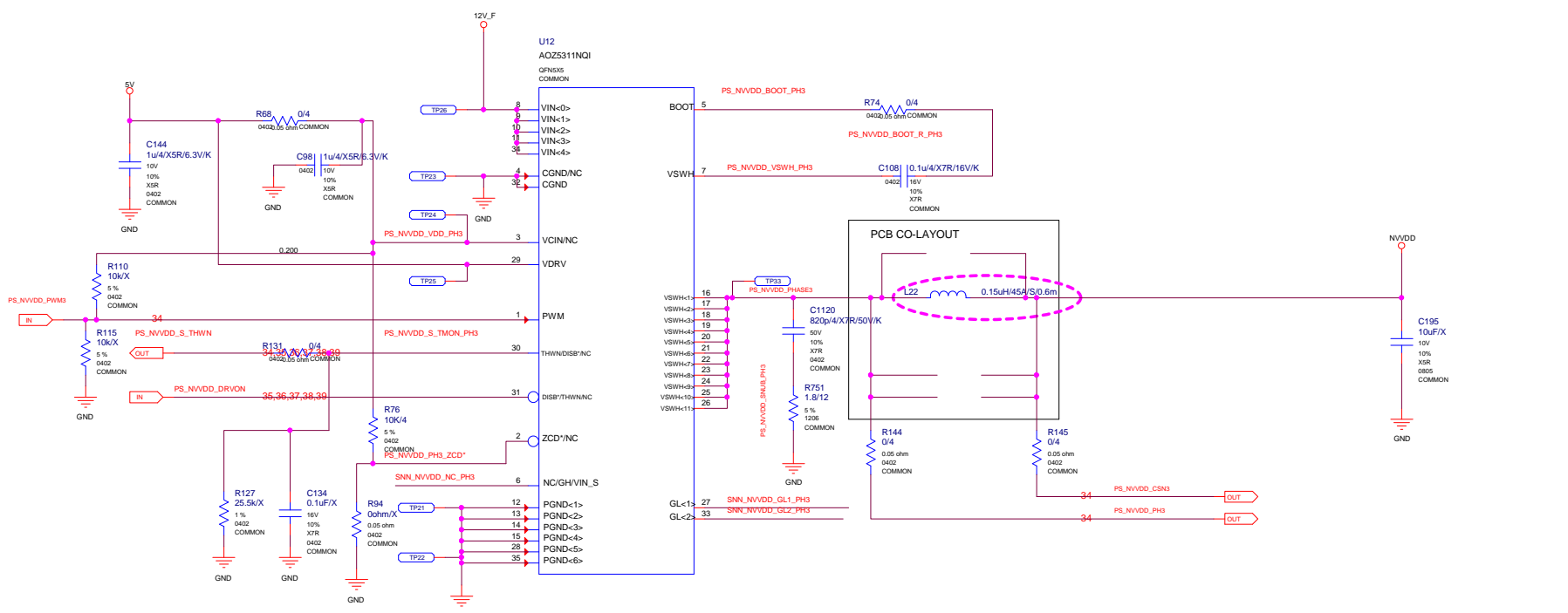
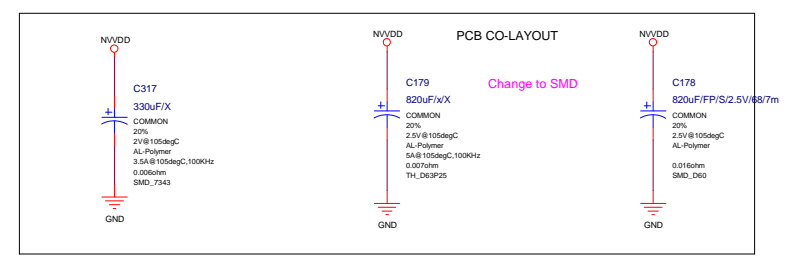
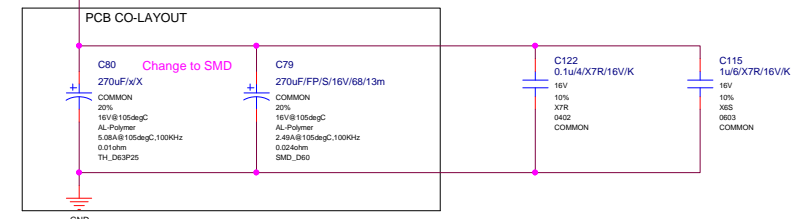
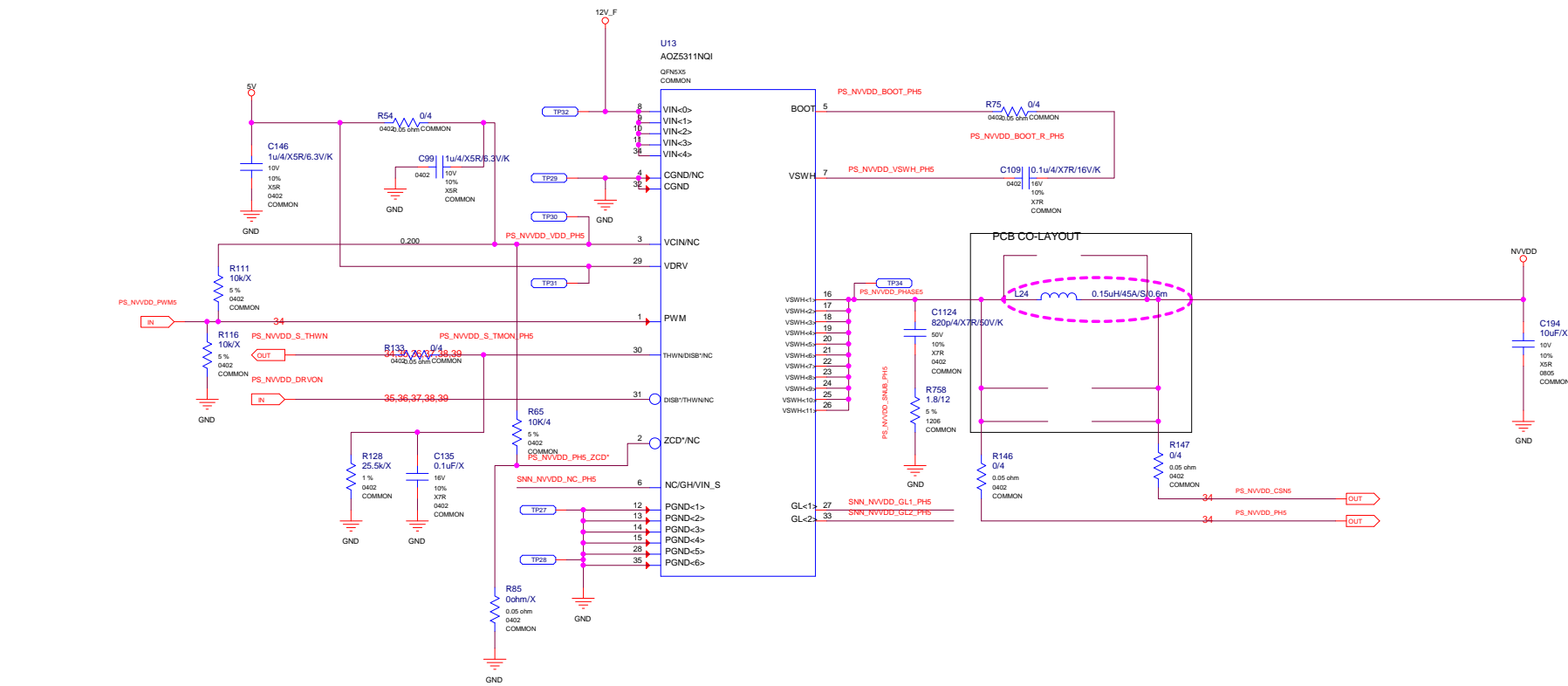
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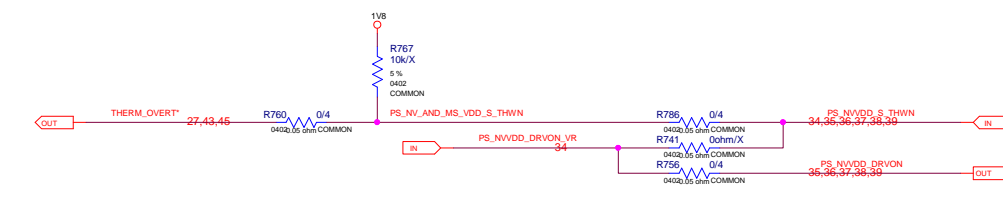
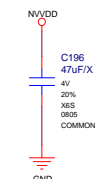
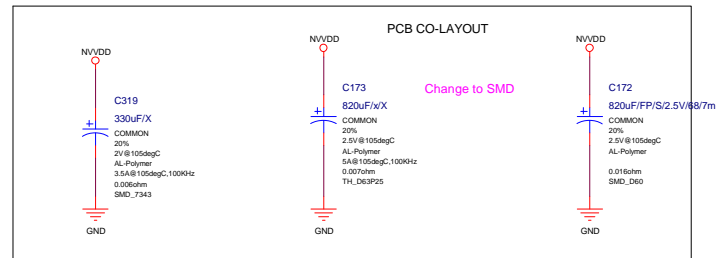
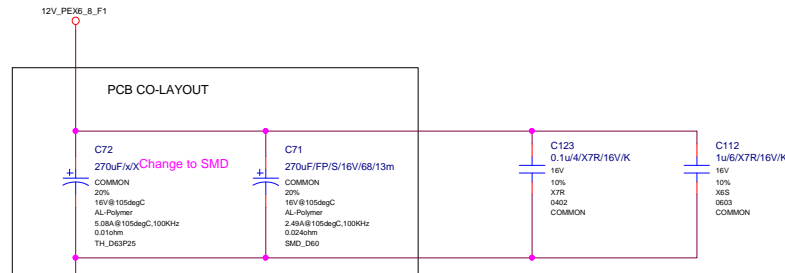
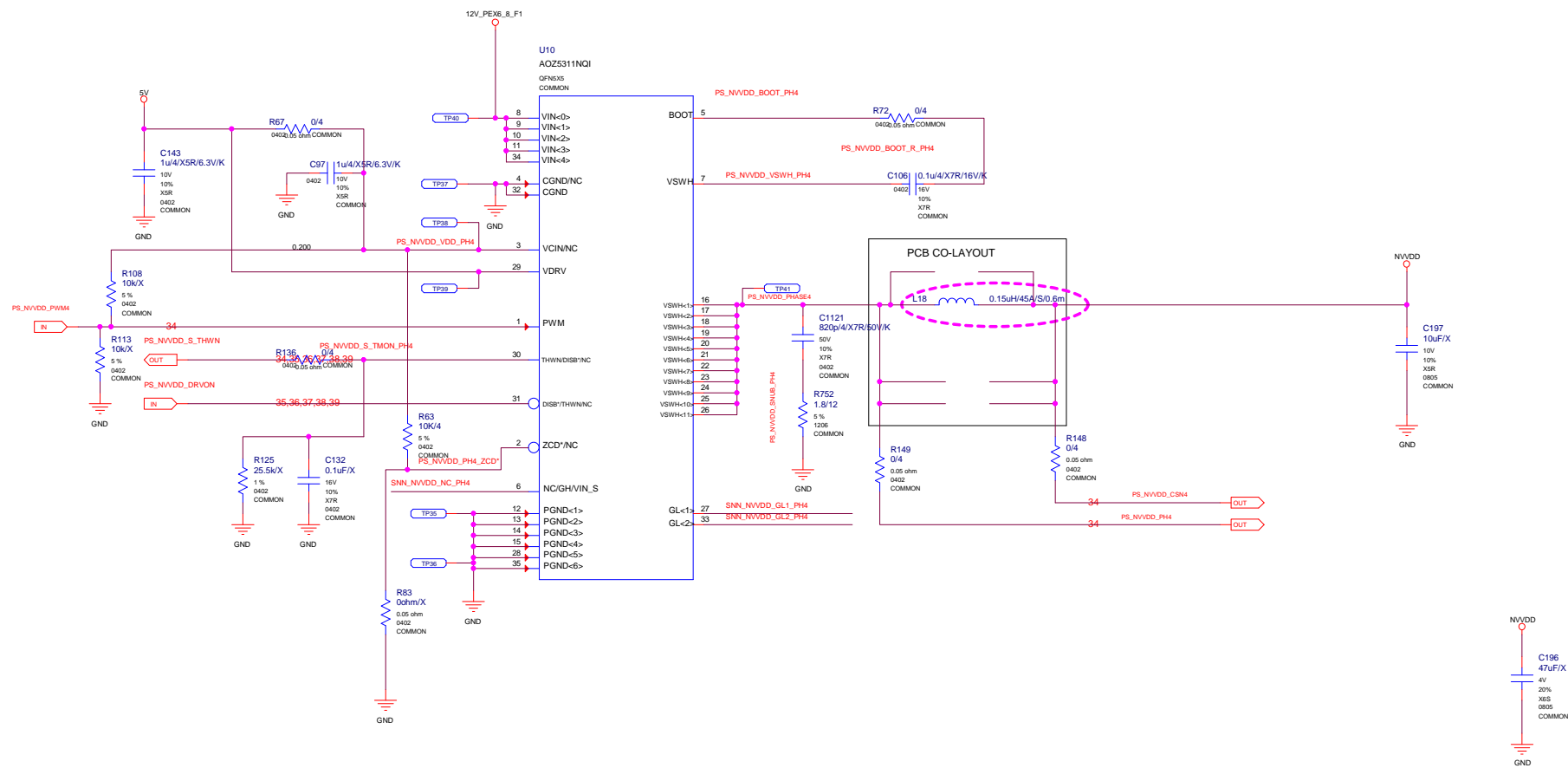
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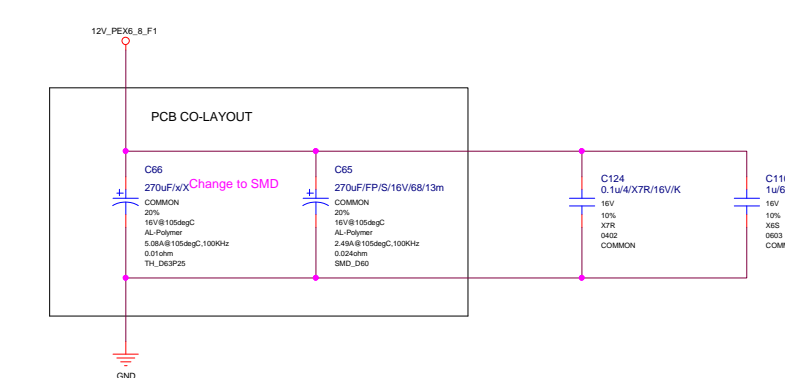
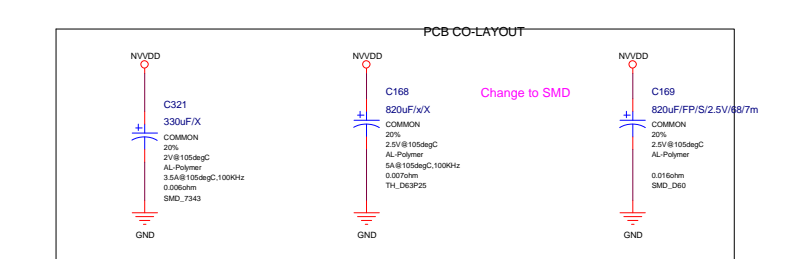
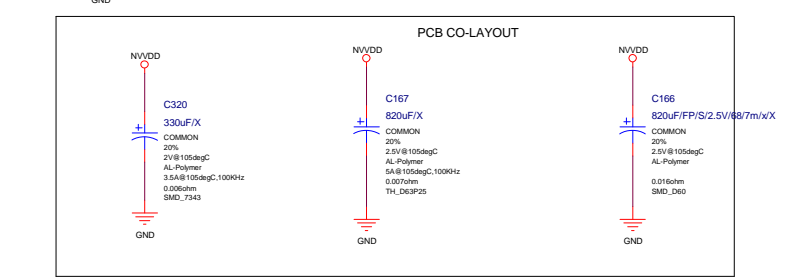
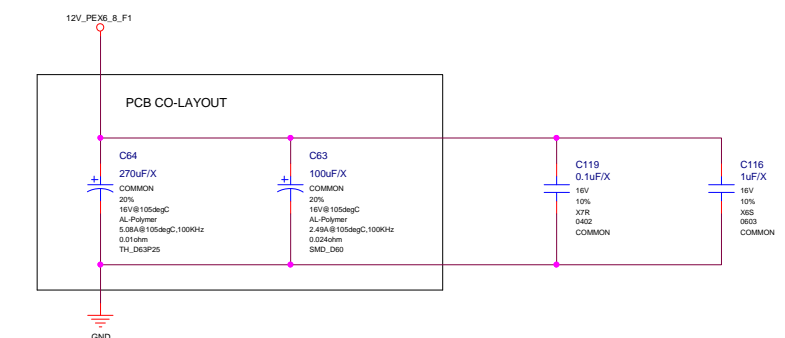
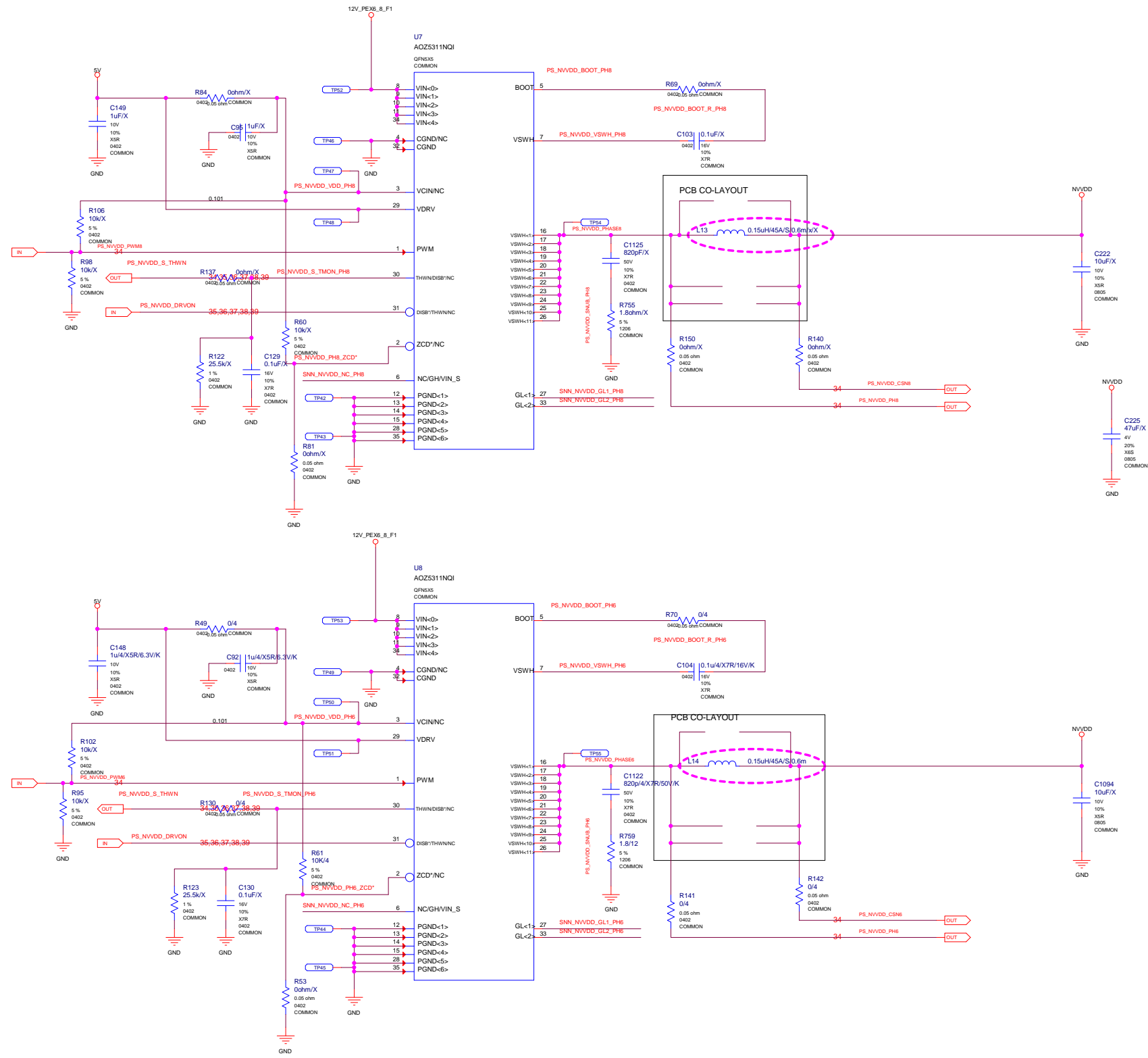
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Title		PCIE	
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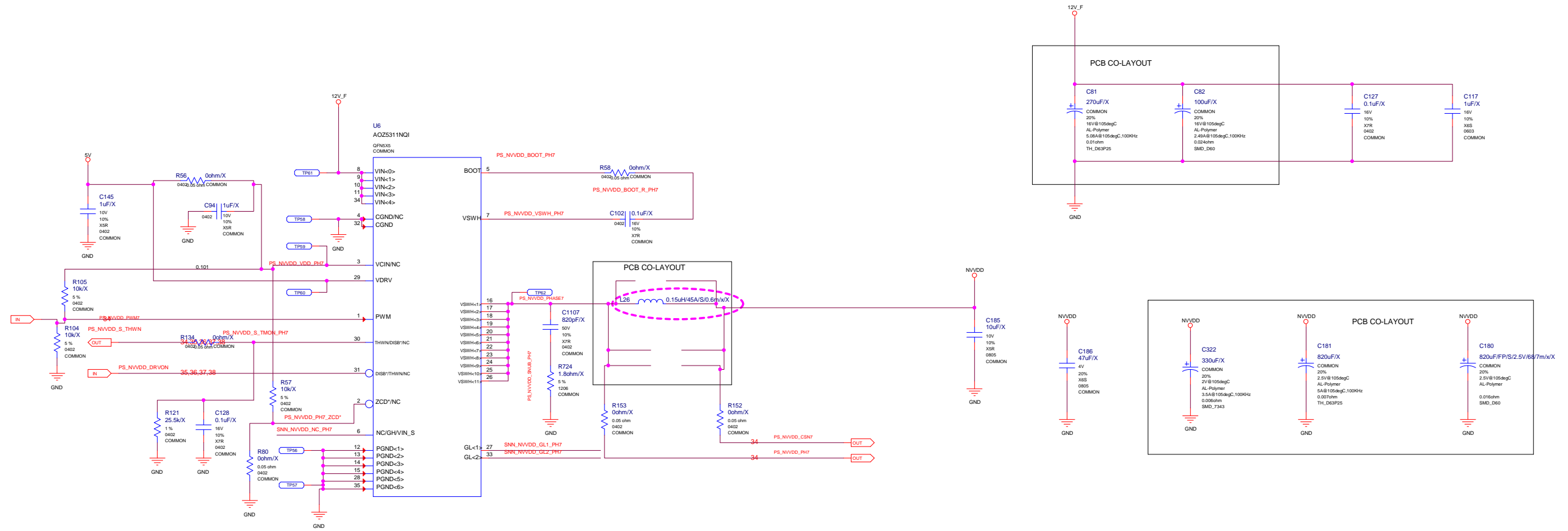
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Title <b>PCIE</b>			
Size	Document Number	Rev	
Custom	<b>GV-N3060VISION OC-12GD</b>	1.01	
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<b>GIGABYTE</b>			
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 PS: NVVDD PHASE 7

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Size <b>Custom</b>	Document Number <b>GV-N3060VISION OC-12GD</b>	Rev <b>1.01</b>
Date: <b>Thursday, January 14, 2021</b>	Sheet <b>39</b>	of <b>54</b>

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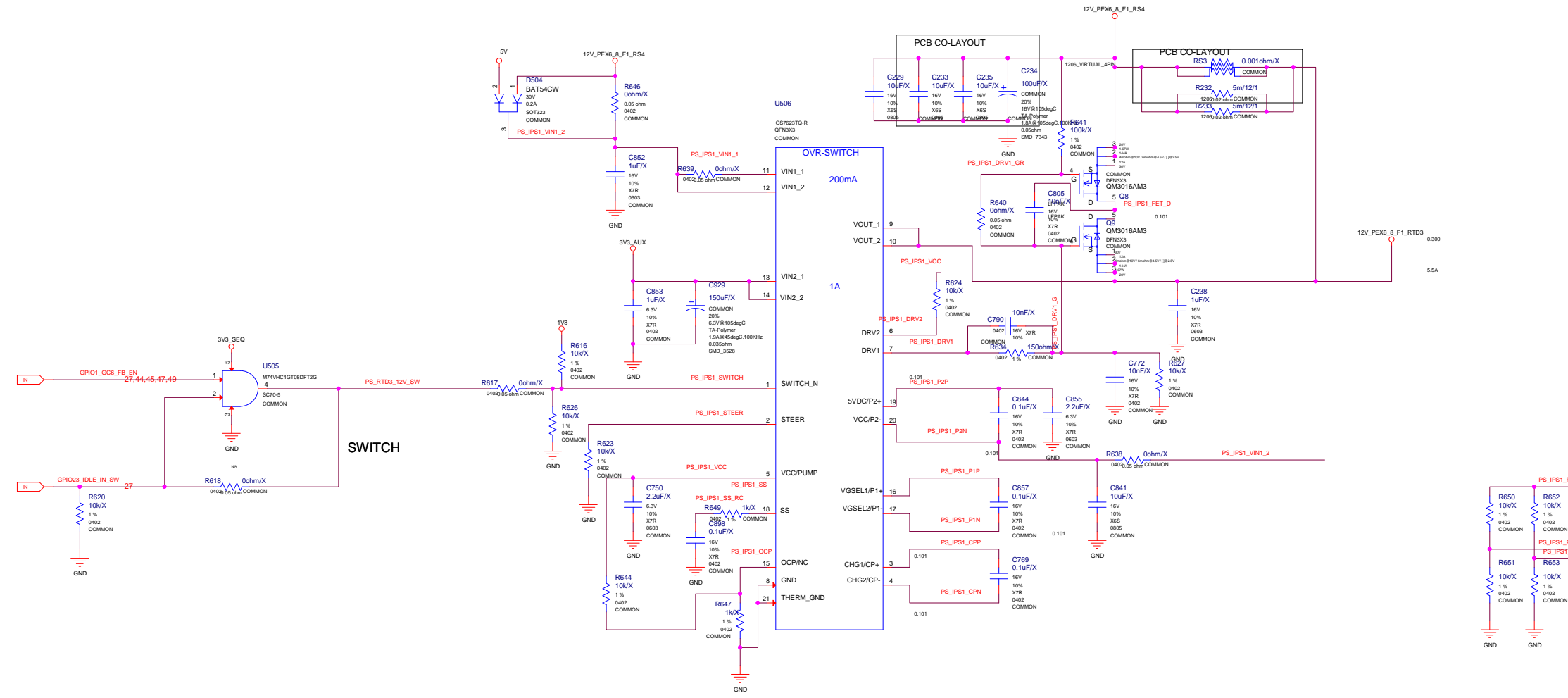
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Size Custom	Document Number <b>GV-N3060VISION OC-12GD</b>	Rev 1.01
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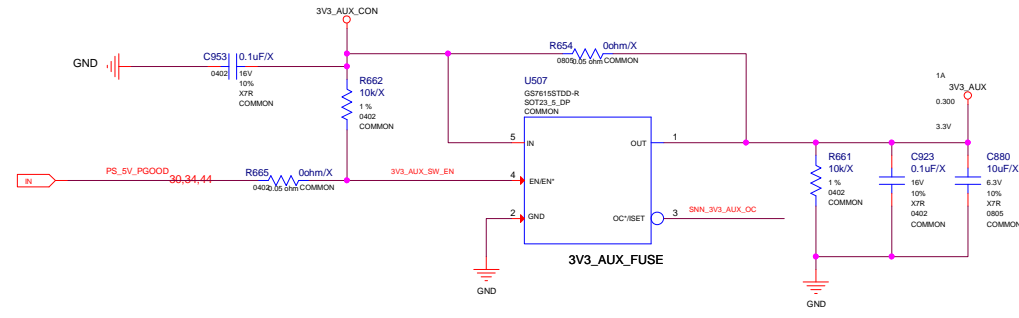
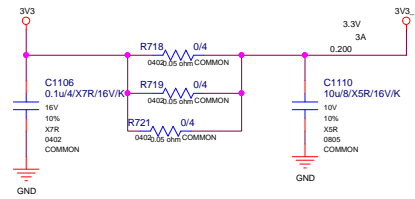
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0	1	0	12V	1	VOUT = VIN2
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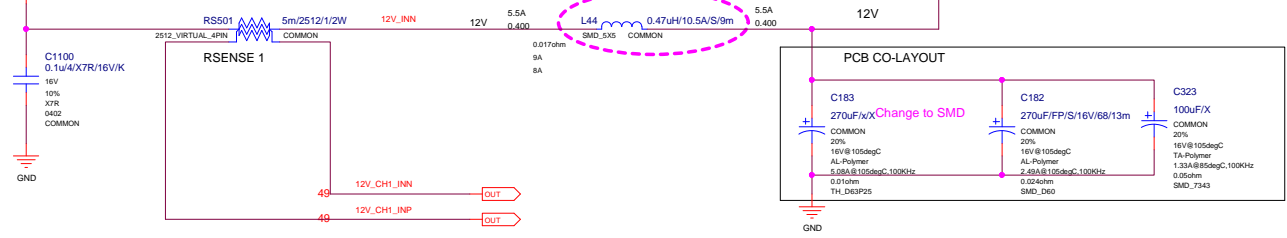
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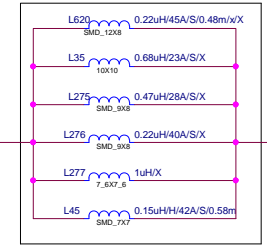
PEX 3V3 INPUT - 10W



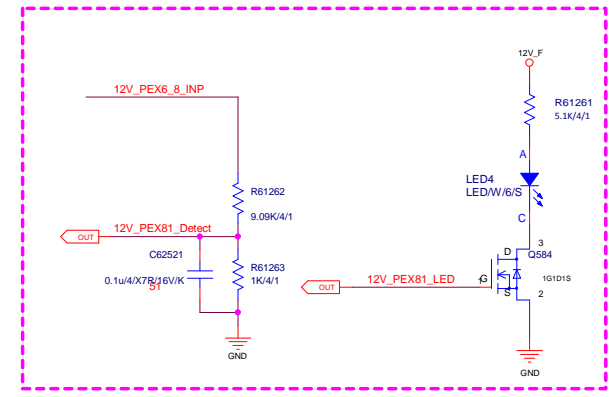
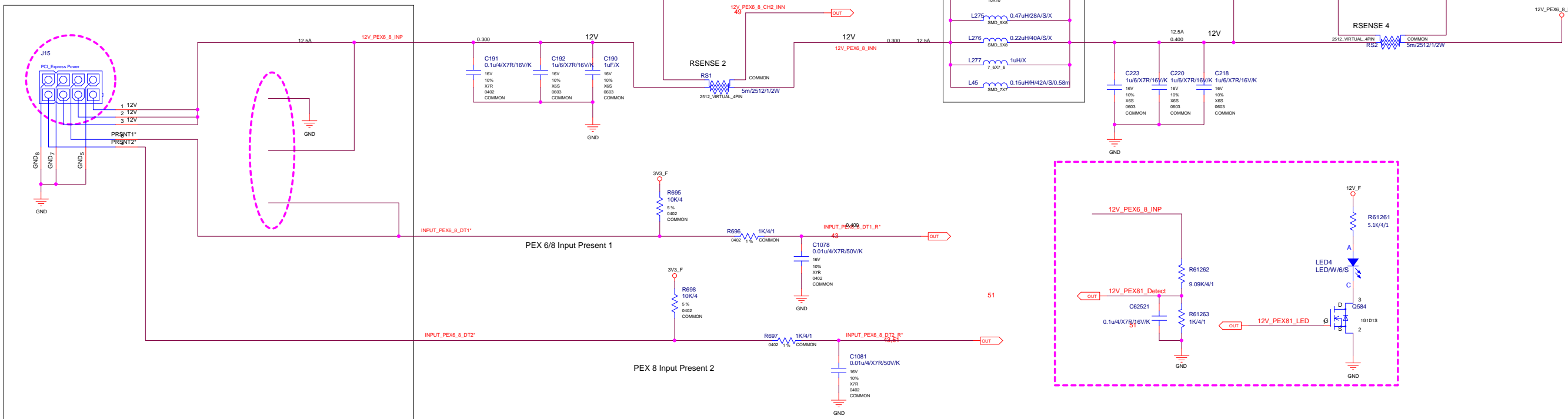
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PCB CO-LAYOUT

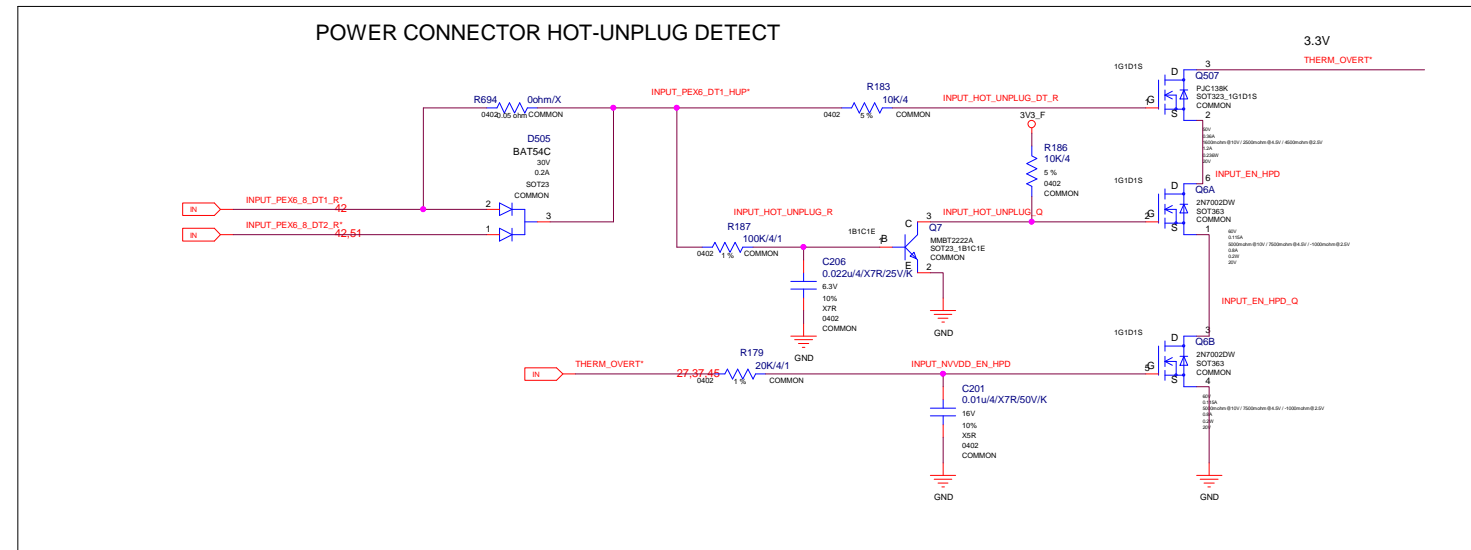


PEX8 INPUT 1 - 2x4 PCIE CON 150W



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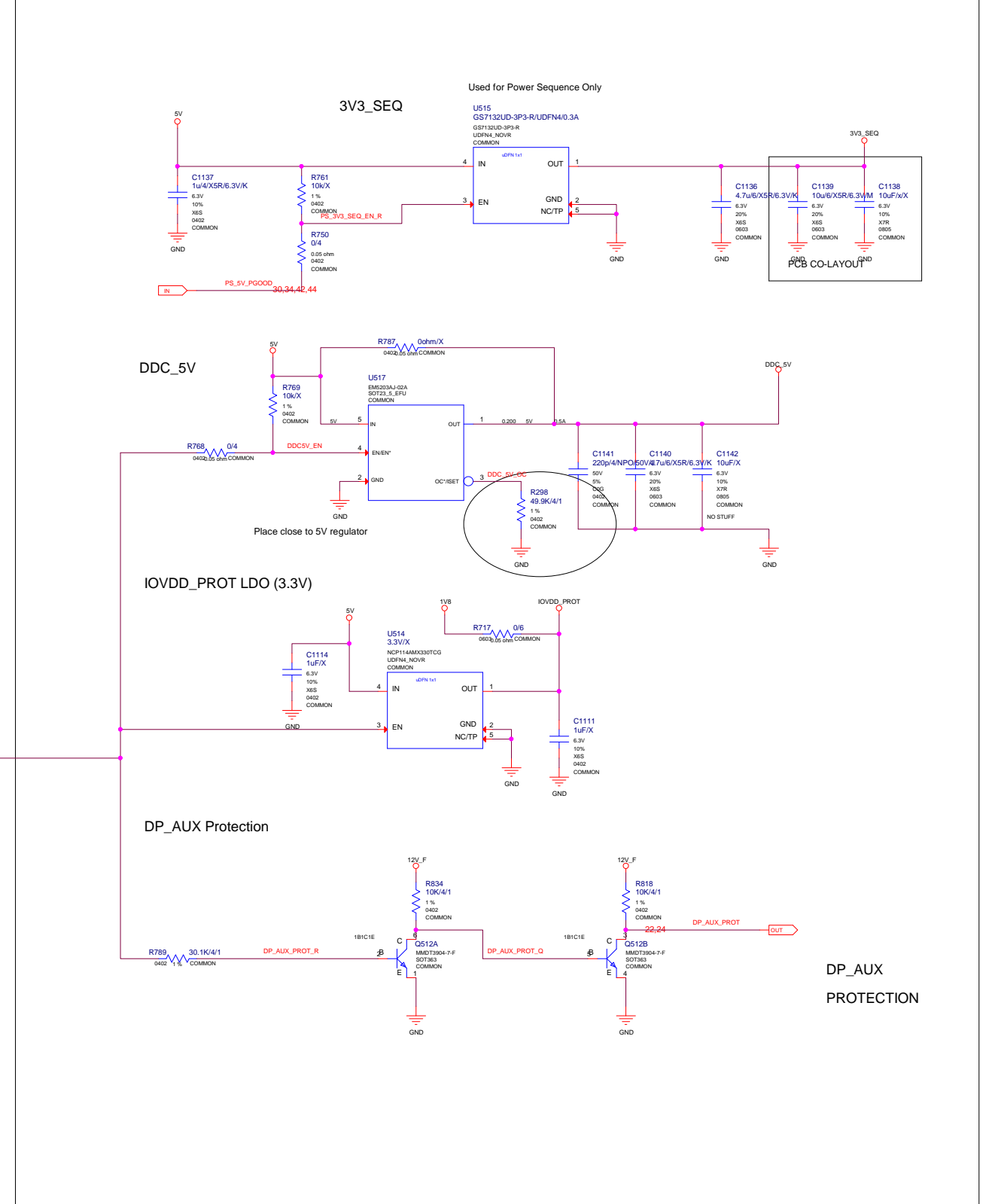
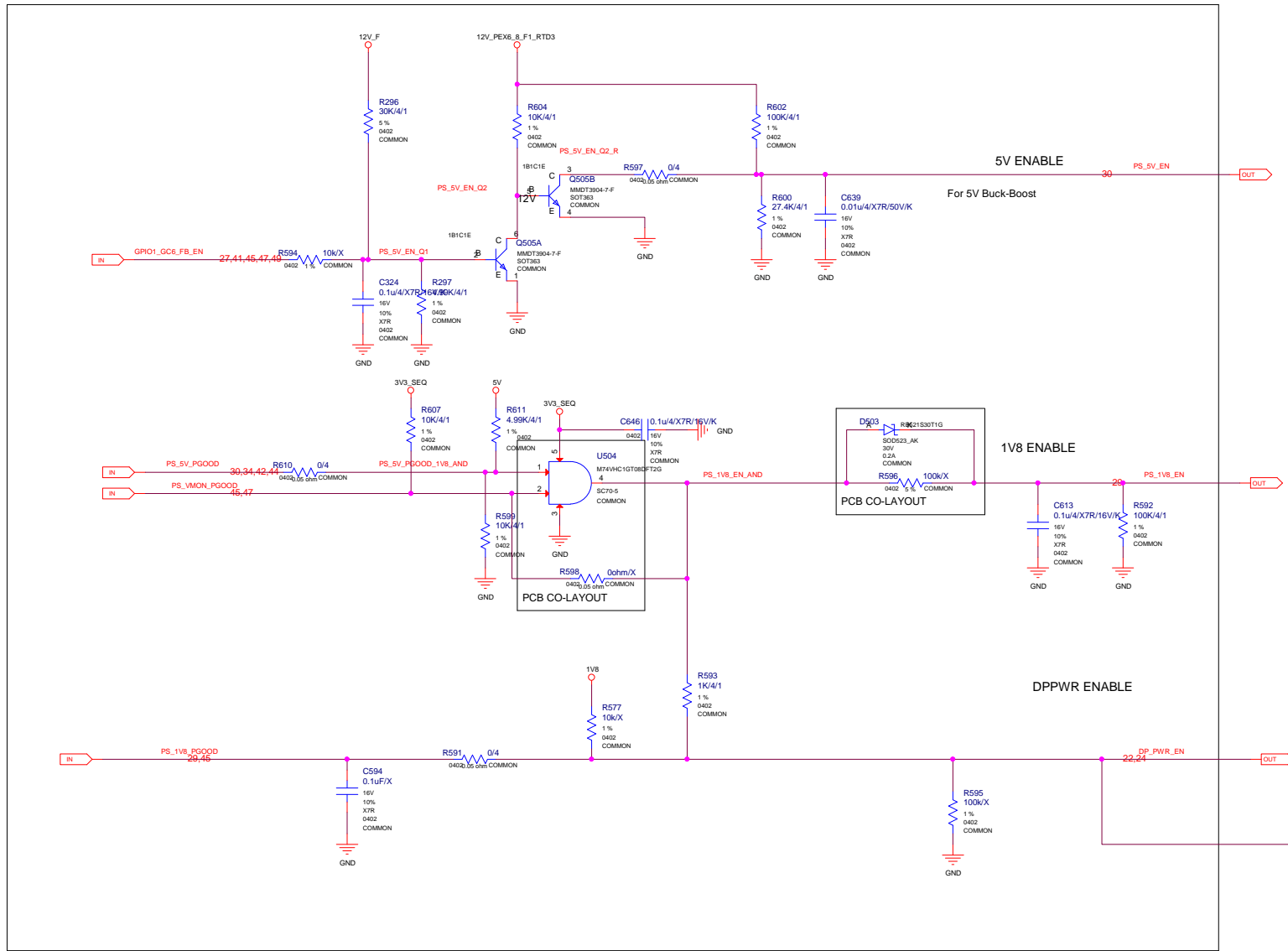
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 MISC: Hot Unplug

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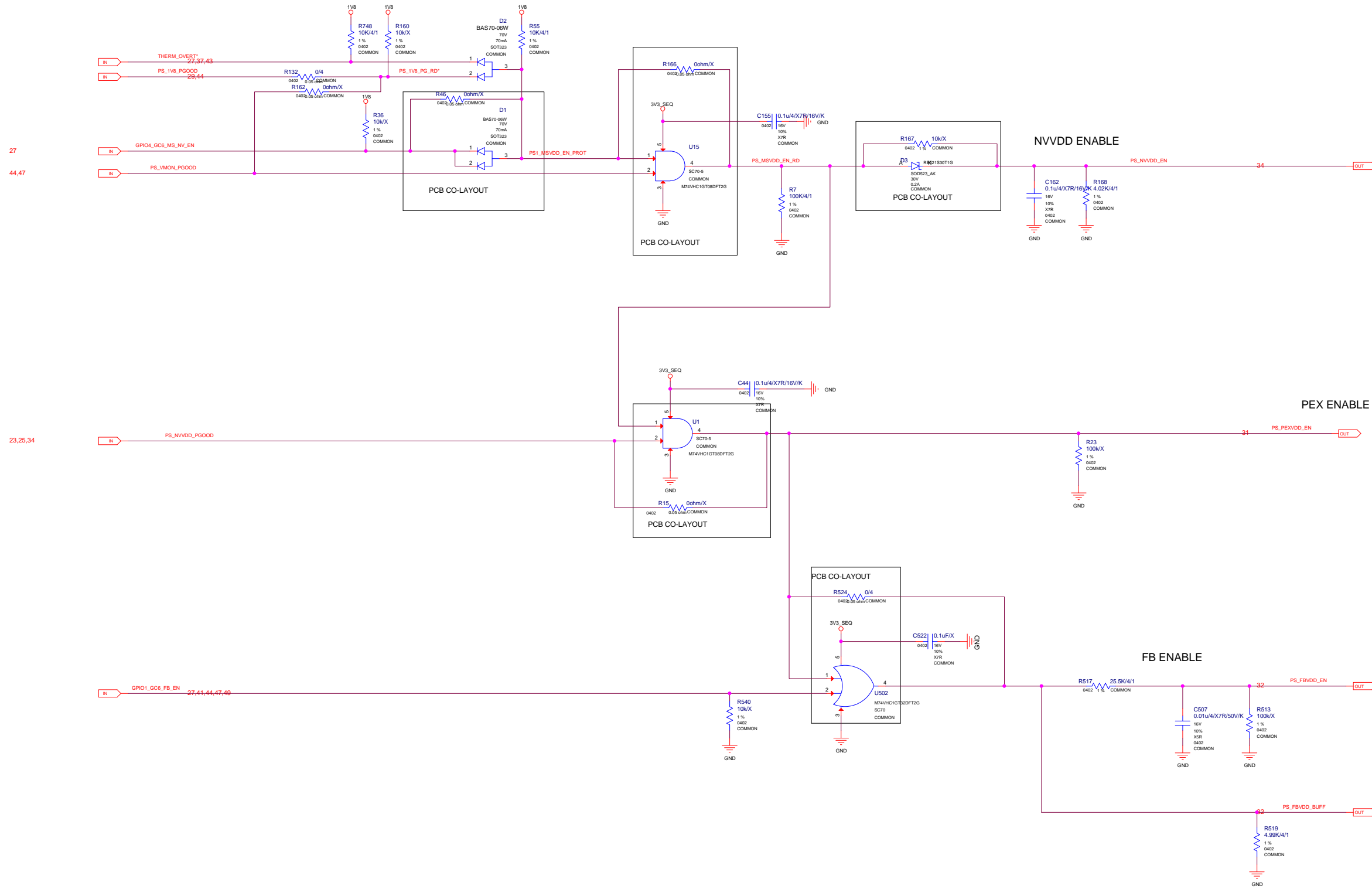
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Title <b>PCIE</b>			
Size	Document Number	Rev	
Custom	<b>GV-N3060VISION OC-12GD</b>	<b>1.01</b>	
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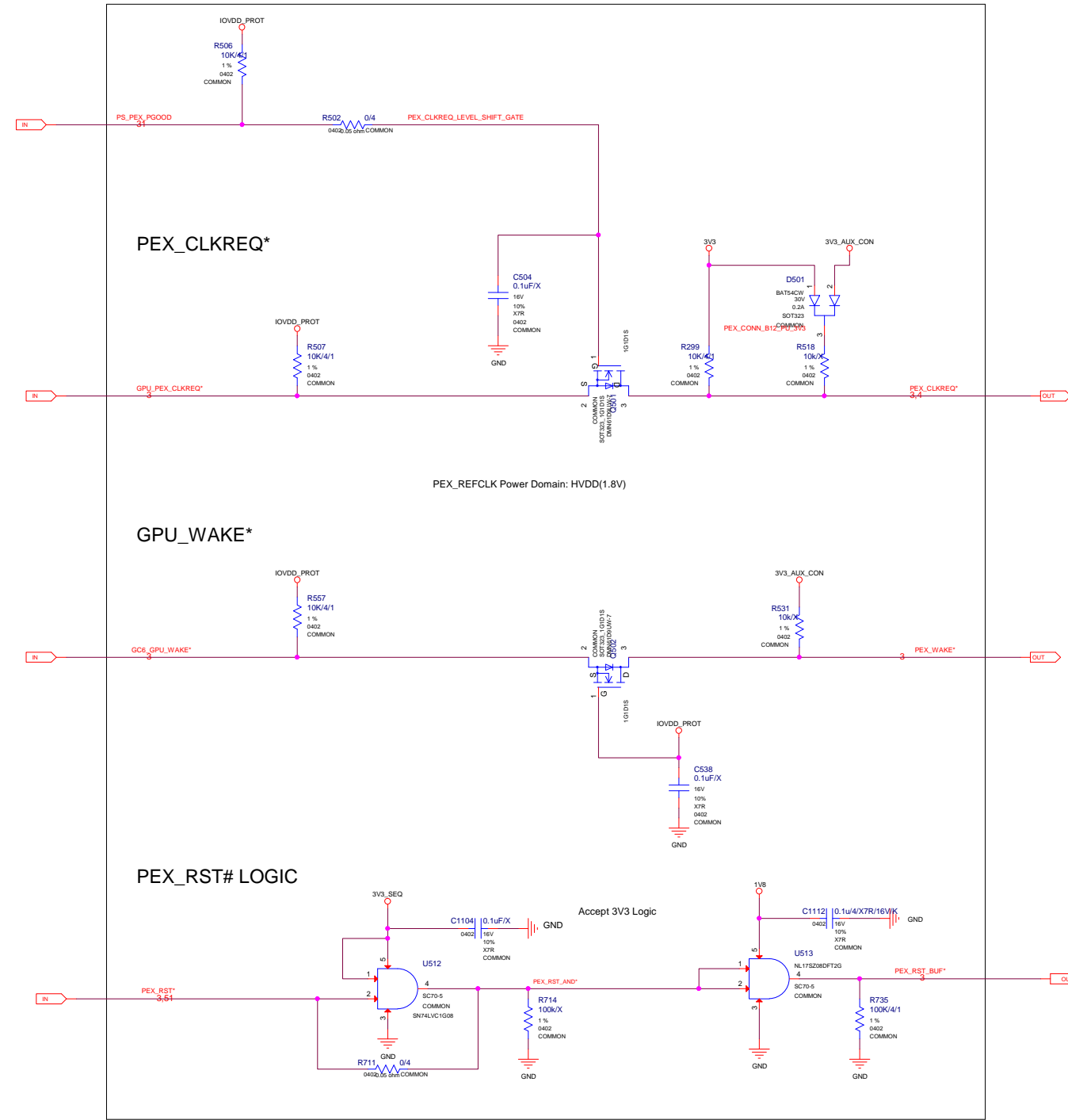
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<b>PCIE</b>			
Size	Document Number	Rev	
Custom	GV-N3060VISION OC-12GD	1.01	
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 SEQ: NVVDD, PEXVDD AND FBVDDQ ENABLE

<b>GIGABYTE</b>		
Title <b>PCIE</b>		
Size Custom	Document Number <b>GV-N3060VISION OC-12GD</b>	Rev 1.01
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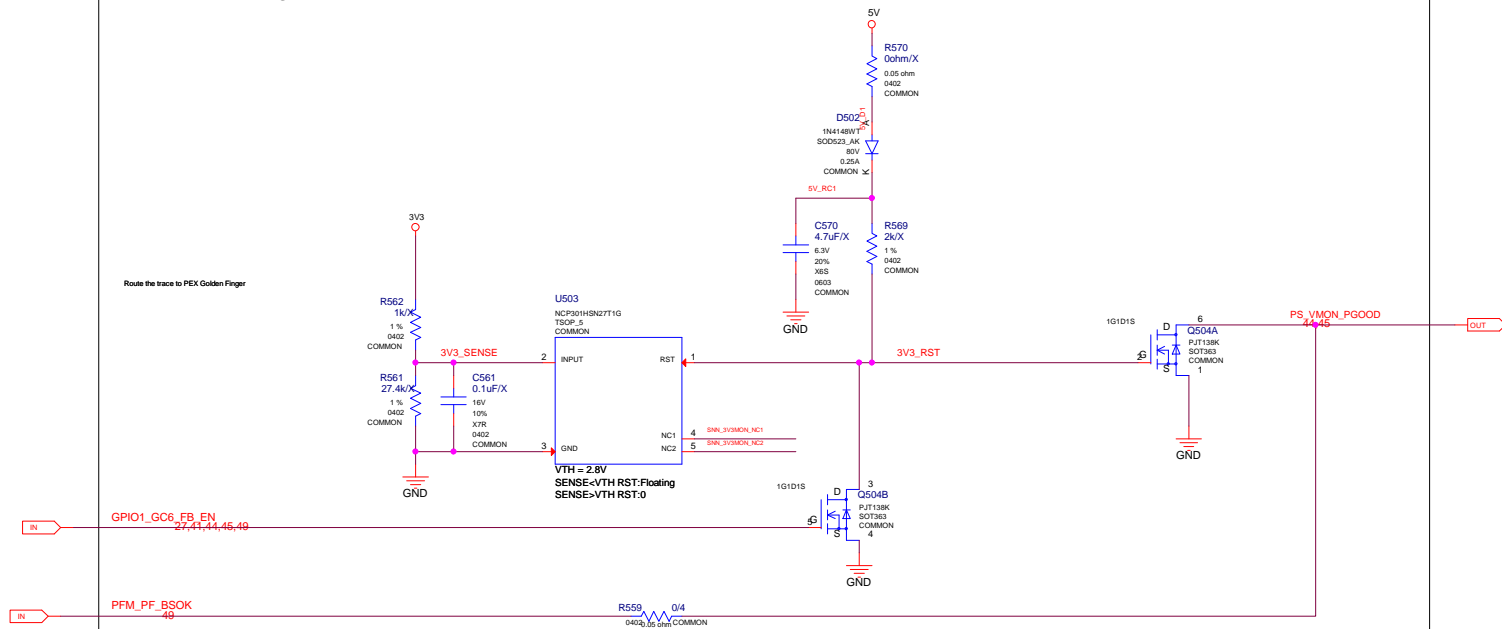


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<b>GIGABYTE</b>			
Title		PCIE	
Size	Document Number	GV-N3060VISION OC-12GD	
Date:	Thursday, January 14, 2021	Sheet	46 of 54
Rev	1.01		

### 3V3PEX Voltage Monitor

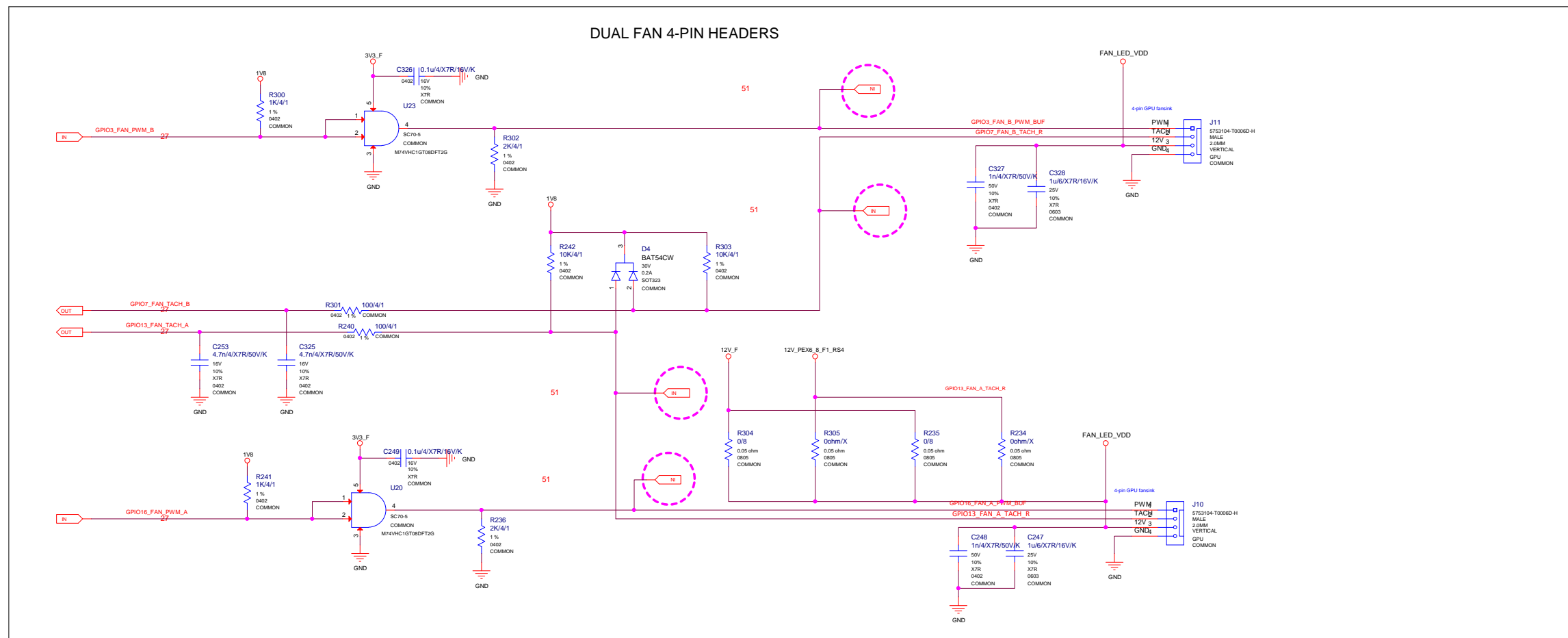
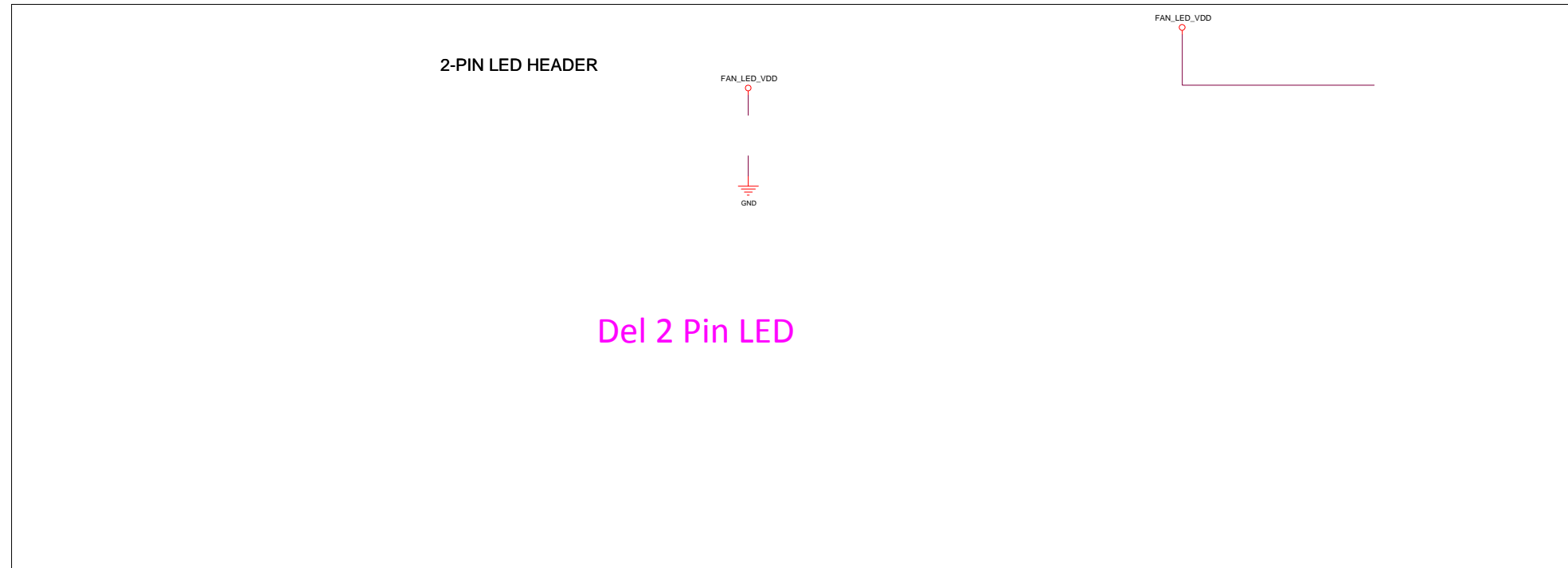


Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_BSOK	INPUT	From Pre-filter(BS_OK)

ASSEMBLY PAGE DETAIL <ASSEMBLY\_DESCRIPTION> SEQUENCE: VOLTAGE MONITOR

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<b>GIGABYTE</b>			
Title <b>PCIE</b>			
Size	Document Number	Rev	
Custom	<b>GV-N3060VISION OC-12GD</b>	1.01	
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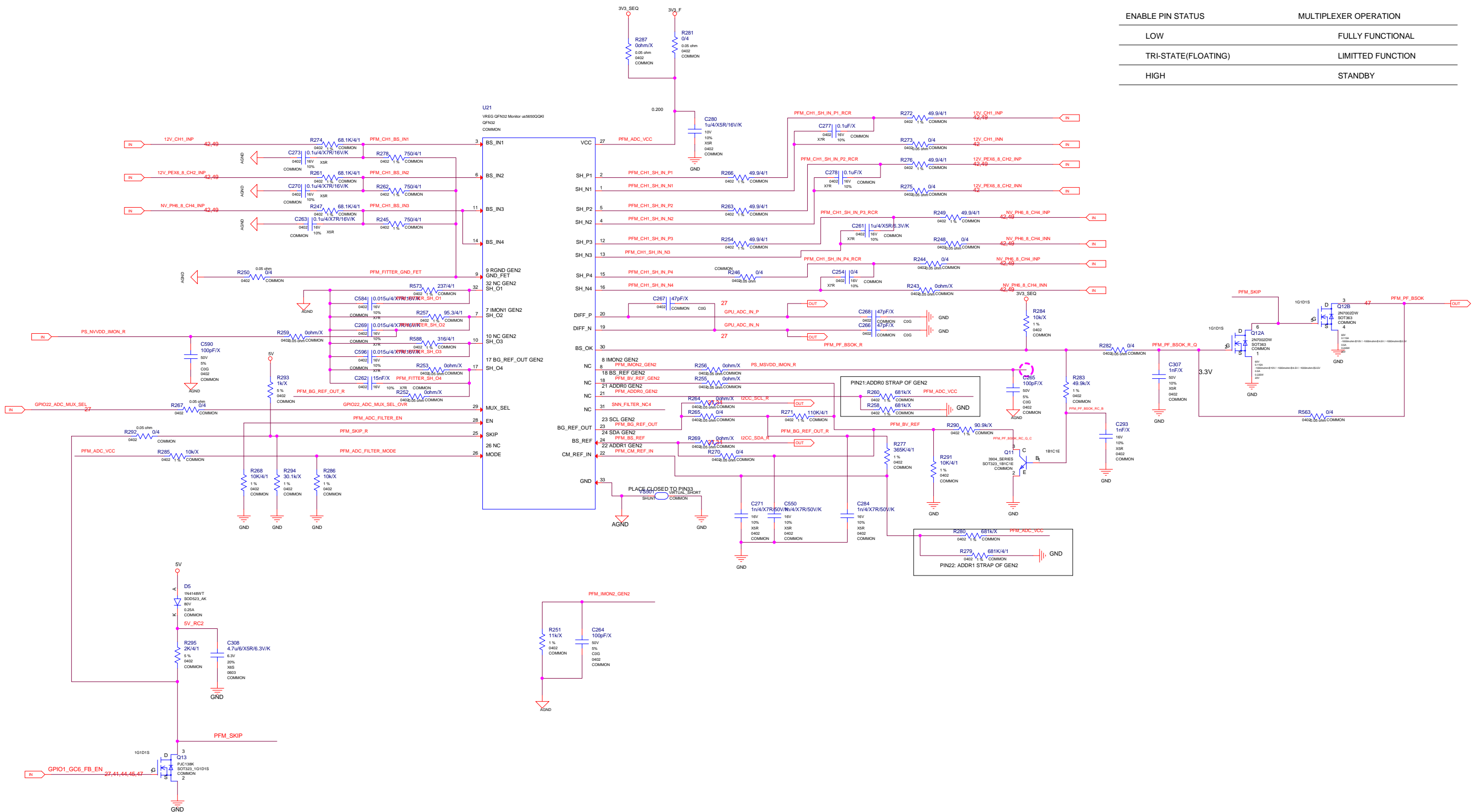


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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

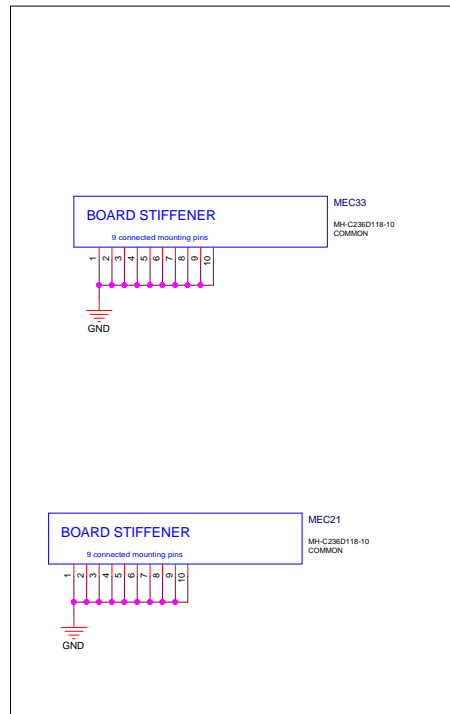


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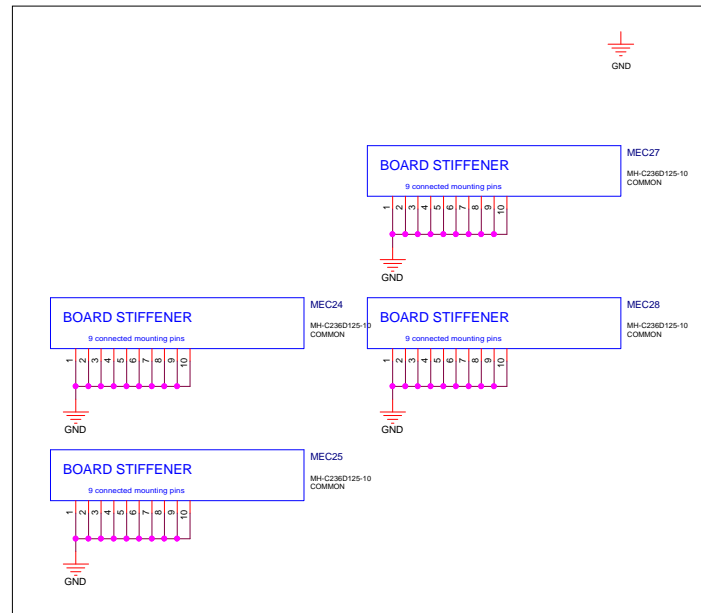
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<b>GIGABYTE</b>			
Title <b>PCIE</b>			
Size <b>Custom</b>	Document Number <b>GV-N3060VISION OC-12GD</b>		Rev <b>1.01</b>
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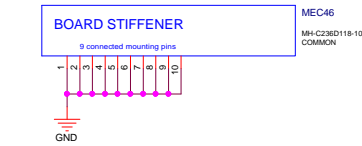
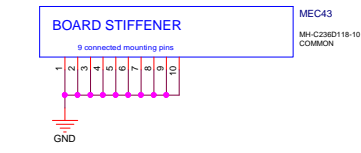
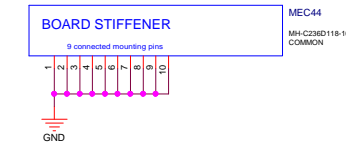
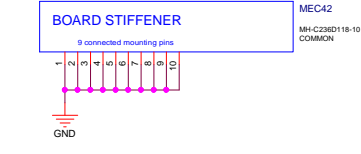
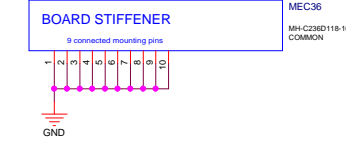
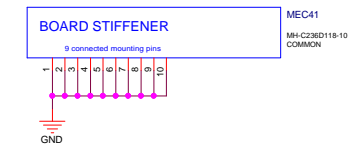
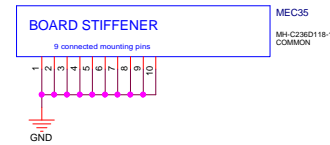
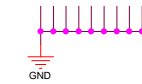
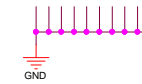
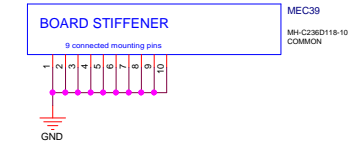
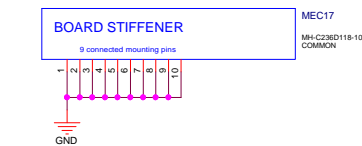
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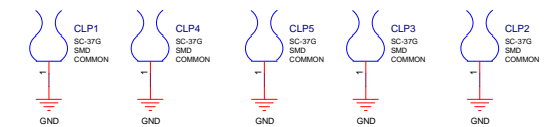
GPU SINK



MOS  
螺絲孔

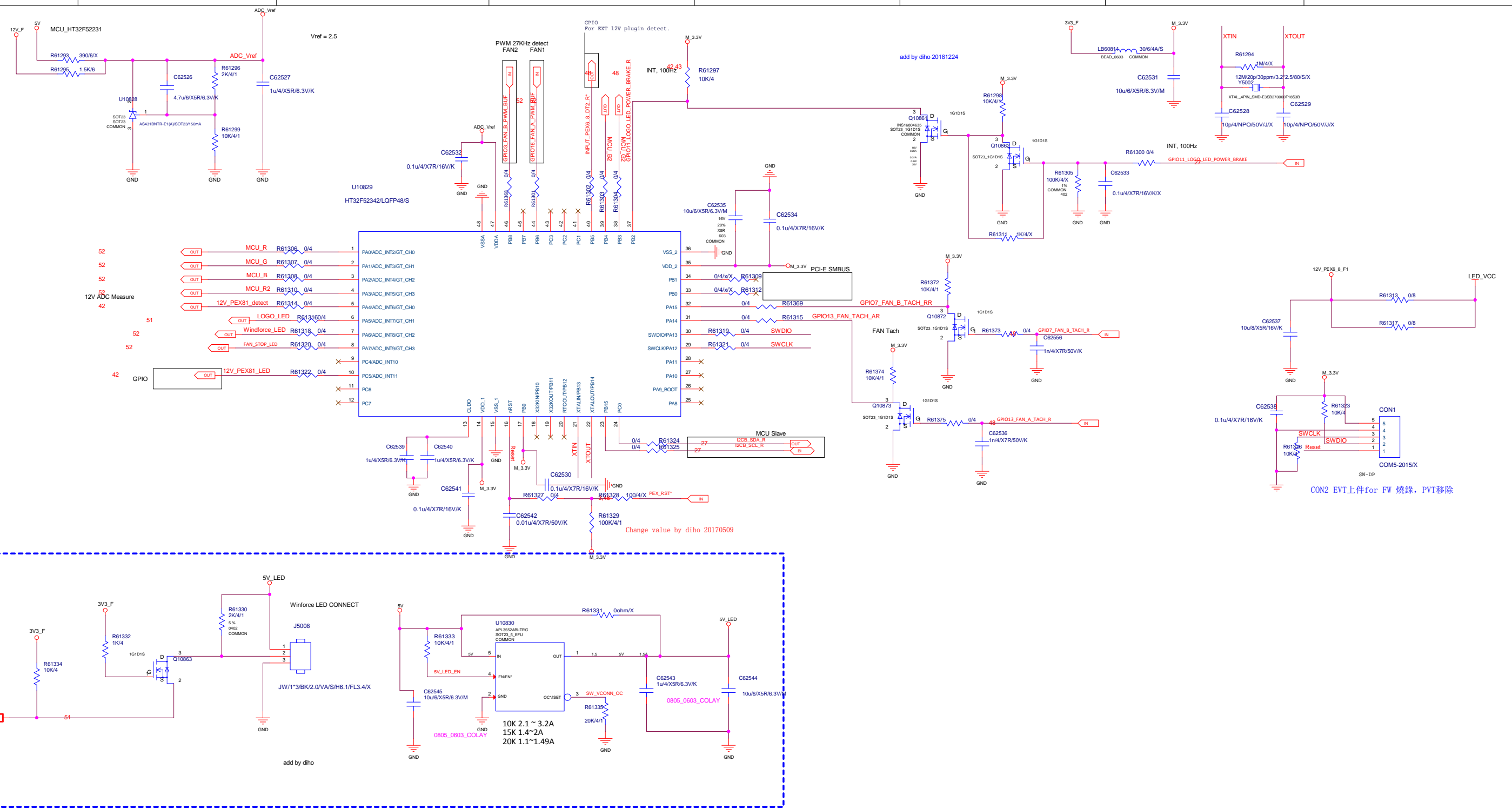


EMI CLIPS:

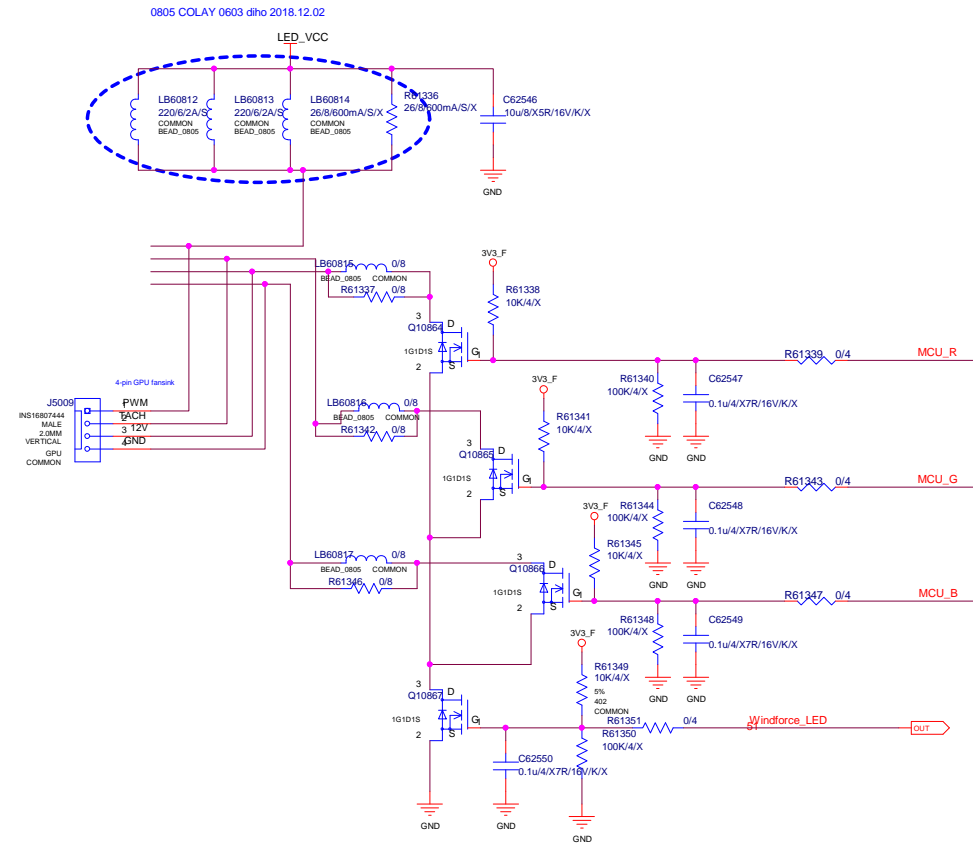


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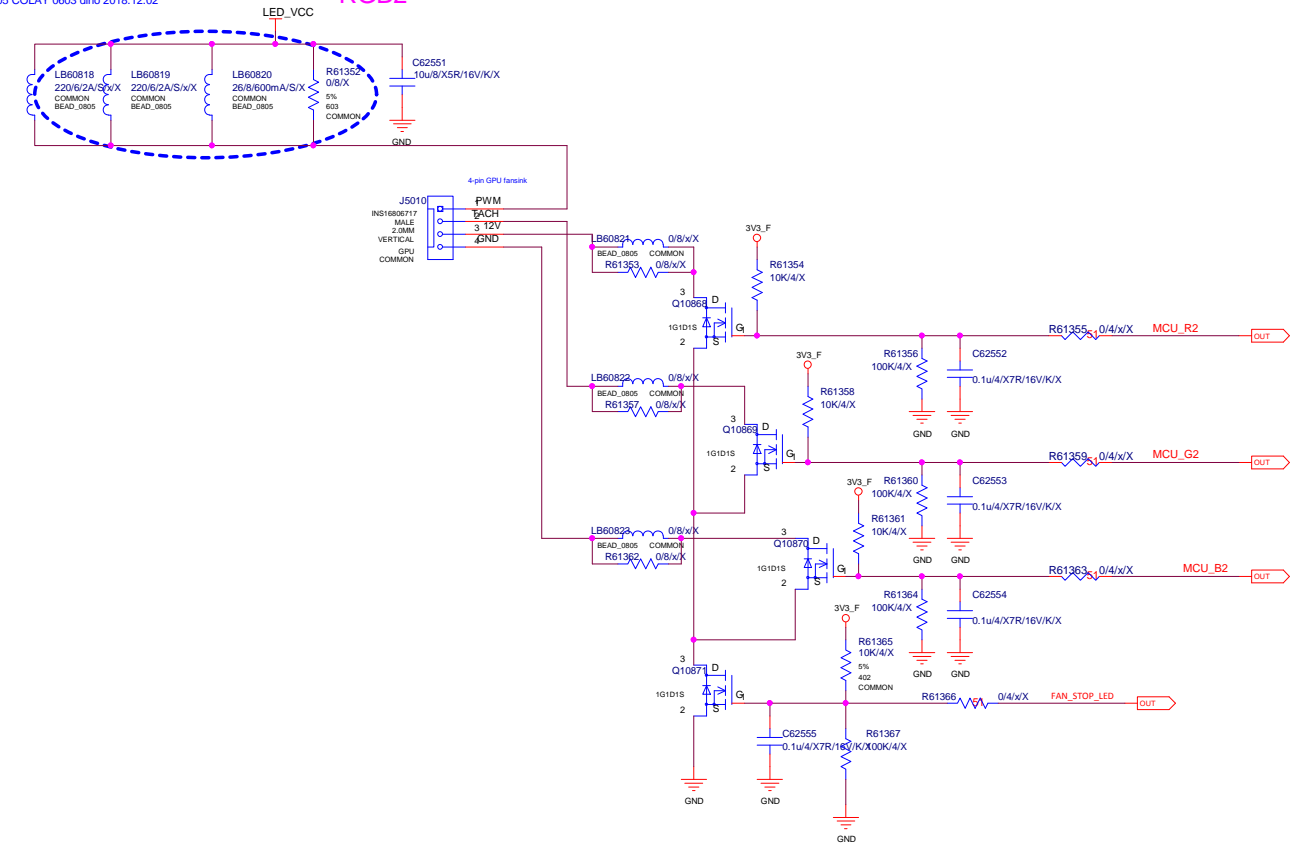
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51 OUT MCU\_R  
 51 OUT MCU\_G  
 51 OUT MCU\_B



0805 COLAY 0603 diho 2018.12.02



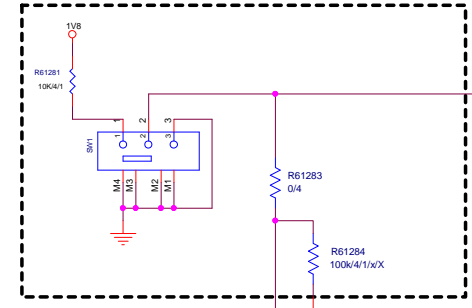
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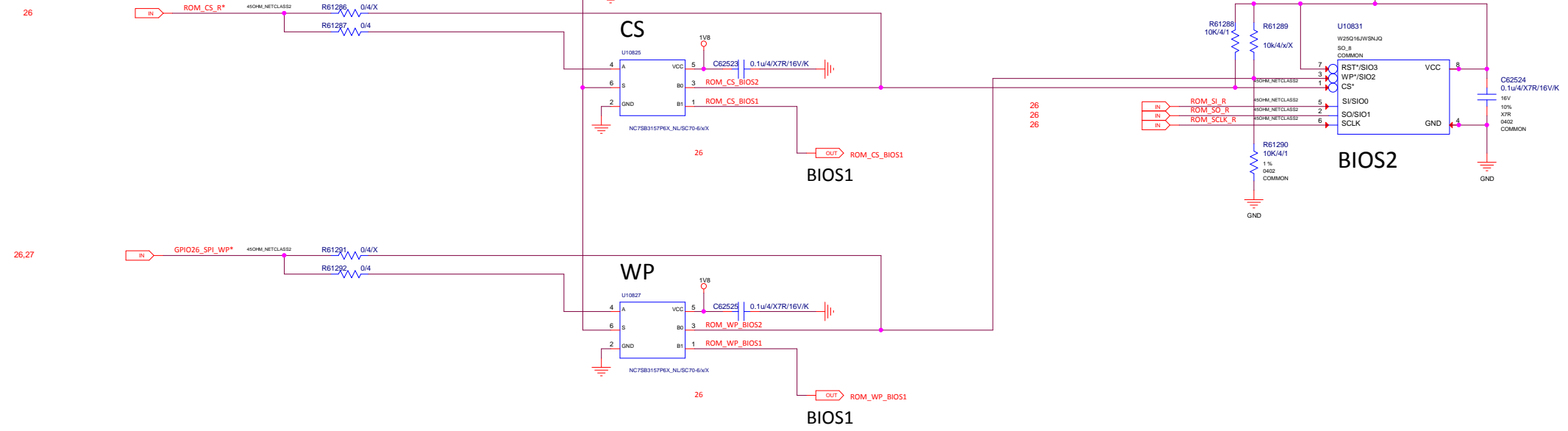
<b>GIGABYTE</b>			
Title		PCIE	
Size	Document Number	Rev	
Custom	GV-N3060VISION OC-12GD	1.01	
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# BIOS Switch

For Dual BIOS switch



S	Function
0	B0 to A = DP2
1	B1 to A = DP1



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ASSEMBLY PAGE DETAIL  
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 MCU ZERO POWER IDLE

<b>GIGABYTE</b>			
Title <b>PCIE</b>			
Size Custom	Document Number <b>GV-N3060VISION OC-12GD</b>		Rev 1.01
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### History

Date	Modify
2020.08.06	First version