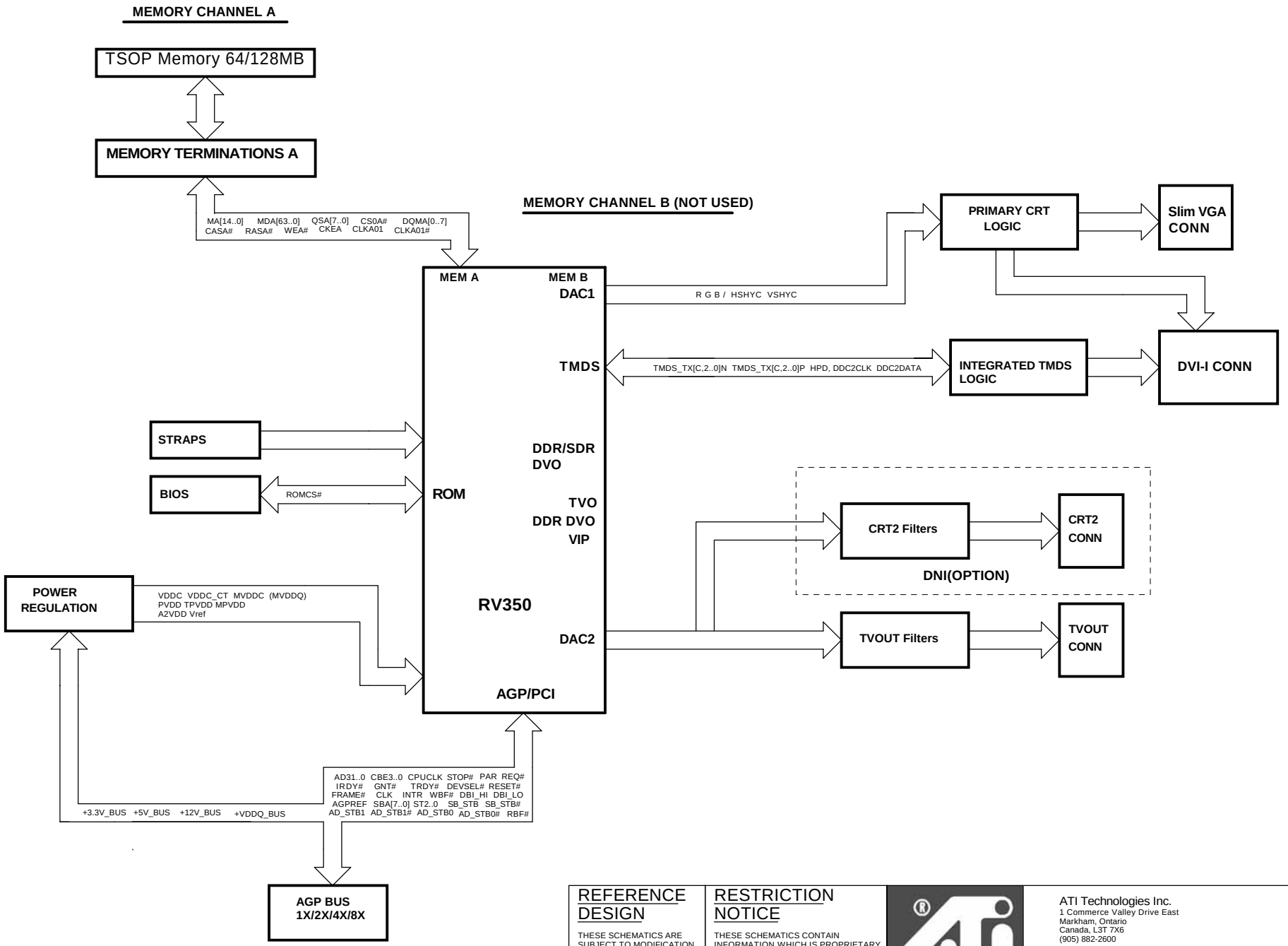

REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFOR-MATION CONTAINED HEREIN.

RESTRICTION NOTICE

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LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

+12V_BUS — C10 100uF_16V

+5V_BUS — C5 100uF_6.3V

+3.3V_BUS — C8 100uF_6.3V

+VDDQ_BUS — C2 100uF_6.3V >= 6.3V

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

Place C2 on left side of AGP connector

4X/8X AGP BUS

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

AGP_C/BE#[3..0] — AGP_AD[31..0] — AGP_SBA[7..0] — AGP_ST[2..0]

MAGP1

A1	12V	OVRCNT#	B1
A2	TYPEDET#	5.0V	B2
A3	GC_DET#/RESERVED	5.0V#B3	B3
A4	USB-	USB+	B4
A5	GND	GND#B5	B5
A6	INTA#	INTB#	B6
A7	RST#	CLK	B7
A8	GNT#	REQ#	B8
A9	VCC3.3	VCC3.3#B9	B9
A10	ST1	ST0	B10
A11	MB_DET#/RESERVED	ST2	B11
A12	DBI_HI/PIPE#	RBF#	B12
A13	GND#A13	GND#B13	B13
A14	WBF#	DBI_LO/RESERVED	B14
A15	SBA1	SBA0	B15
A16	VCC3.3#A16	VCC3.3#B16	B16
A17	SBA3	SBA2	B17
A18	SB_STB#	SB_STB	B18
A19	GND#A19	GND#B19	B19
A20	SBA5	SBA4	B20
A21	SBA7	SBA6	B21
A22	RESERVED	RESERVED#B22	B22
A23	GND#A23	GND#B23	B23
A24	RESERVED#A24	3.3VAUX	B24
A25	VCC3.3#A25	VCC3.3#B25	B25
A26	AD30	AD31	B26
A27	AD28	AD29	B27
A28	VCC3.3#A28	VCC3.3#B28	B28
A29	AD26	AD27	B29
A30	AD24	AD25	B30
A31	GND#A31	GND#B31	B31
A32	AD_STB1#	AD_STB1	B32
A33	C/BE3#	AD23	B33
A34	VDDQ1.5	VDDQ1.5#B34	B34
A35	AD22	AD21	B35
A36	AD20	AD19	B36
A37	GND#A37	GND#B37	B37
A38	AD18	AD17	B38
A39	AD16	C/BE2#	B39
A40	VDDQ1.5#A40	VDDQ1.5#B40	B40
A41	FRAME#	IRDY#	B41
A42	KEY	KEY#B42	B42
A43	KEY#A43	KEY#B43	B43
A44	KEY#A44	KEY#B44	B44
A45	KEY#A45	KEY#B45	B45
A46	TRDY#	DEVSEL#	B46
A47	STOP#	VDDQ1.5#B47	B47
A48	PME#	PERR#	B48
A49	GND#A49	GND#B49	B49
A50	PAR	SERR#	B50
A51	AD15	C/BE1#	B51
A52	VDDQ1.5#A52	VDDQ1.5#B52	B52
A53	AD13	AD14	B53
A54	AD11	AD12	B54
A55	GND#A55	GND#B55	B55
A56	AD9	AD10	B56
A57	C/BE0#	AD8	B57
A58	VDDQ1.5#A58	VDDQ1.5#B58	B58
A59	AD_STB0#	AD_STB0	B59
A60	AD6	AD7	B60
A61	GND#A61	GND#B61	B61
A62	AD4	AD5	B62
A63	AD2	AD3	B63
A64	VDDQ1.5#A64	VDDQ1.5#B64	B64
A65	AD0	AD1	B65
A66	VREFGC	VREFCG	B66

1.5V_AGP_BUS

AGP_TYPEDET# — AGP_GC_8X_DET# — AGP_INTR# — AGP_RESET# — AGP_GNT# — AGP_MB_8X_DET# — AGP_DBI_HI — AGP_WBF# — AGP_SBSTB# — AGP_ADSTB1# — AGP_FRAME# — AGP_TRDY# — AGP_STOP# — AGP_PAR — AGP_ADSTB0# — AGP_VREFGC

AGP_AGPCLK — AGP_REQ# — AGP_RBF# — AGP_DBI_LO — AGP_SBSTB — AGP_IRDY# — AGP_DEVSEL# — AGP_ADSTB1 — AGP_ADSTB0 — AGP_AGPREF

R1 0R — AGP_SBSTB_R — R2 0R

R5 0R — AGP_ADSTB1_R — R6 0R

R12 0R — AGP_ADSTB0_R — R13 0R

+12V_BUS — C4 100nF — +5V_BUS — C9 100nF — +3.3V_BUS — C15 100nF

Caps for EMI - install close to AGP connector

AGP_TYPEDET# — R19 0R

For retail, 1K ohm pull-down causes AMD system detects AGP2X only

+12V, TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET# — R60 0R

+12V_BUS — FAN1 — WAFER 2-PIN

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

May be placed far from connector

+3.3V_BUS — R17 47K

+12V_BUS — R3 DNI_20K

DNI

Q12 — DNI_BSN20

3 AGP_MB_8X_DET# — AGP_MB_8X_DET# — TEST

+VDDQ_BUS — Q1 2N7002E — R20 324R — R21 147R — AGP_VREFGC — R24 100R — C6 10nF — Close to ASIC

U7C — SN74ACT86D — R23 1K

UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF — +VDDQ_BUS

TEST — Q5 2N7002E

DNI — R66 324R — R64 DNI_0R

R67 147R — R65 100R — C7 10nF — Close to ASIC

AGP_AGPREFCG — AGP_AGPREFCG 3

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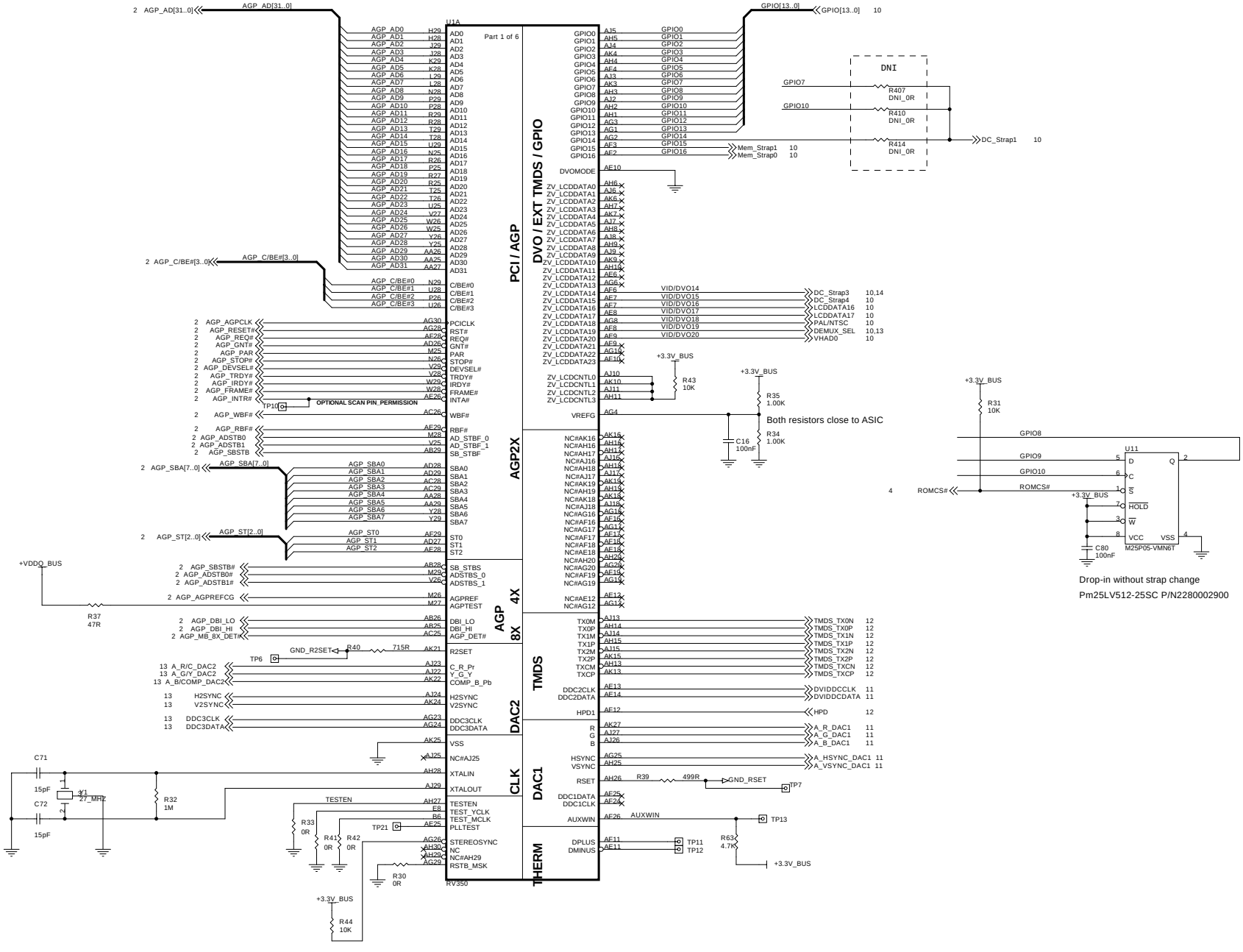

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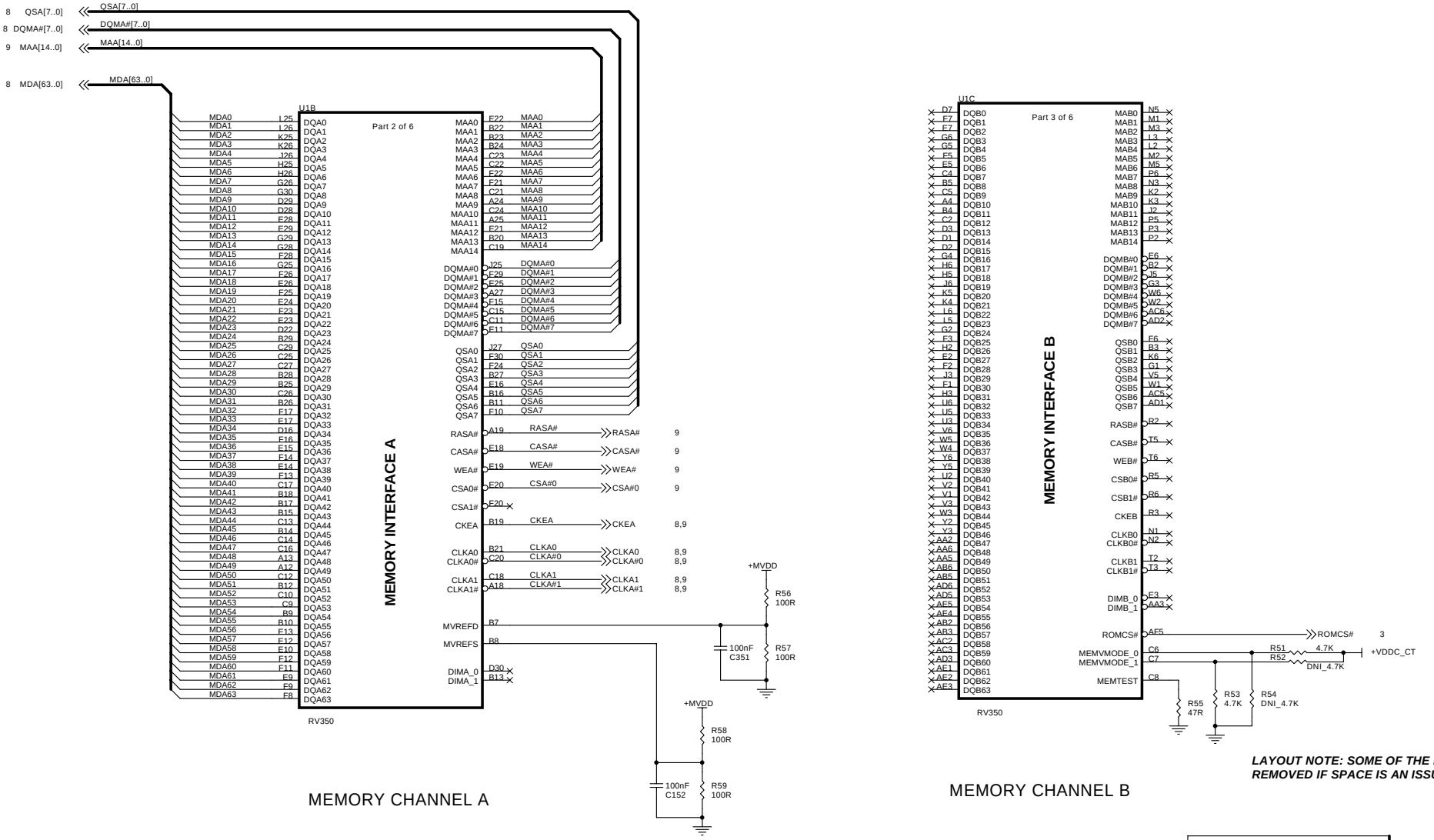

MEMORY CHANNEL A

PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL

MEMORY CHANNEL B

LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

FOR 2.5V VDDR1
MEMVMODE_0 = VDDC
MEMVMODE_1 = GND
FOR 1.8V VDDR1
MEMVMODE_0 = GND
MEMVMODE_1 = VDDC

(SEE DESIGN GUIDE)

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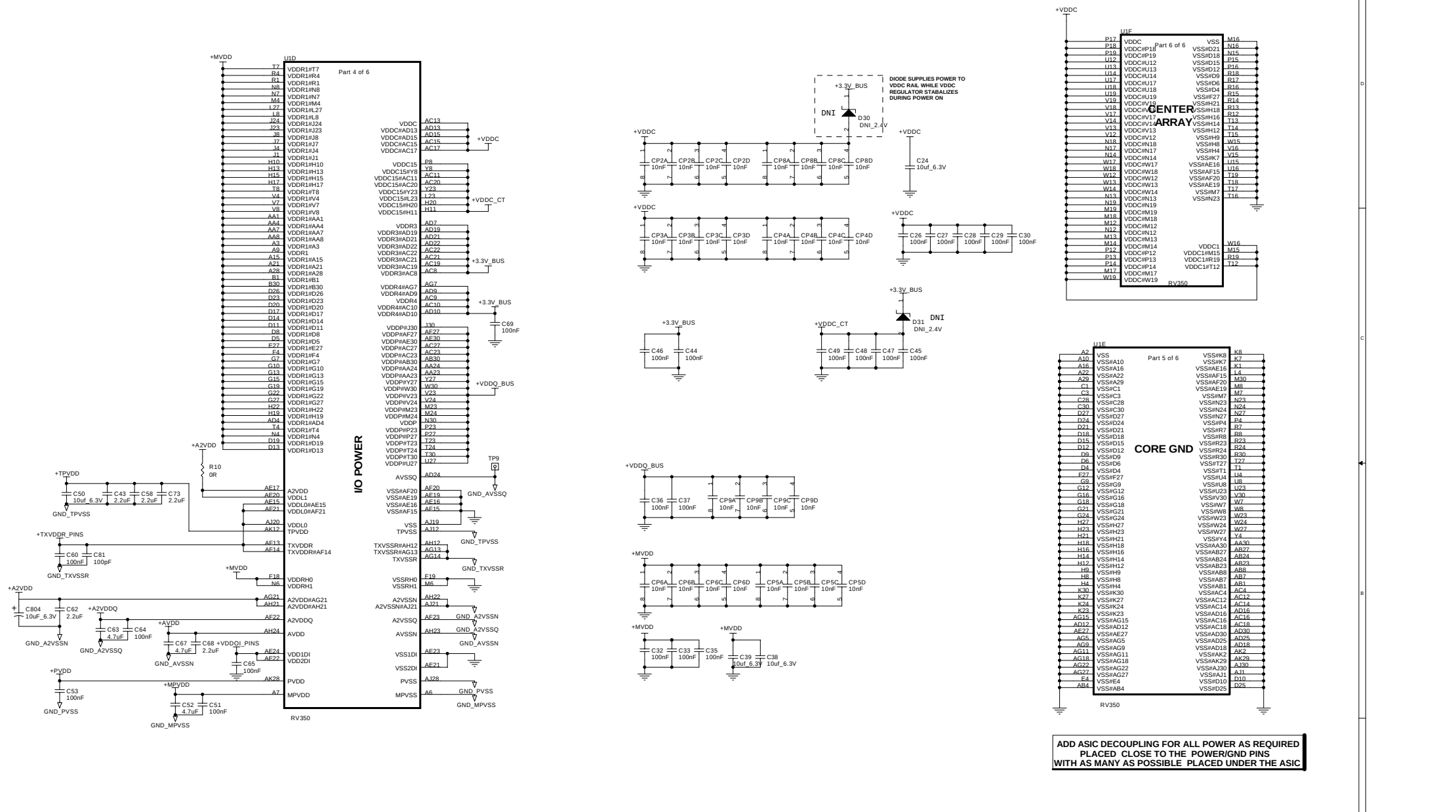

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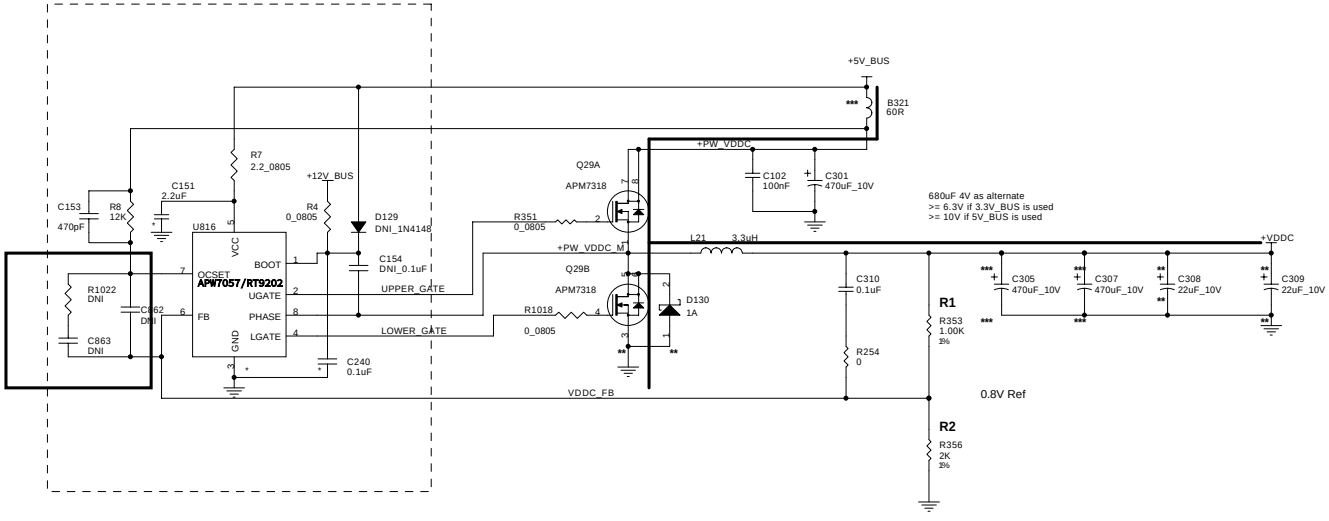
Regulator for VDDC (ASIC Core)

Vin = 5.0V AGP
Vout = 1.2V
Iout = Unknown (7A MAX at 350MHz) (load consumption)
Iout = 3A MAX (Power rail consumption)

***	Indicate number of via required for the connection

Part	Vout	R1	R2
APW7057 **RT9202** 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240110100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N
	1.62V	1.00K 1% ATI P/N 3240100100	976R 1% ATI P/N 3240976000
	2.5V	1.00K 1% ATI P/N 3240100100	475R 1% ATI P/N 3240475300
	3.3V TSOP Memory	1.00K 1% ATI P/N 3240100100	324R 1% ATI P/N 3240332000
	3.45V TSOP Memory	1.00K 1% ATI P/N 3240100100	301 1% ATI P/N 3240301000



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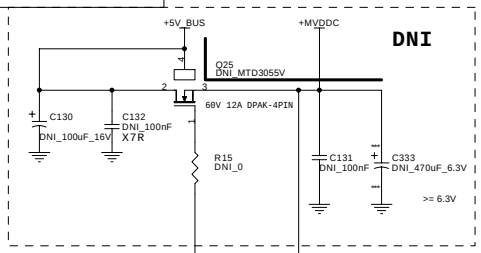
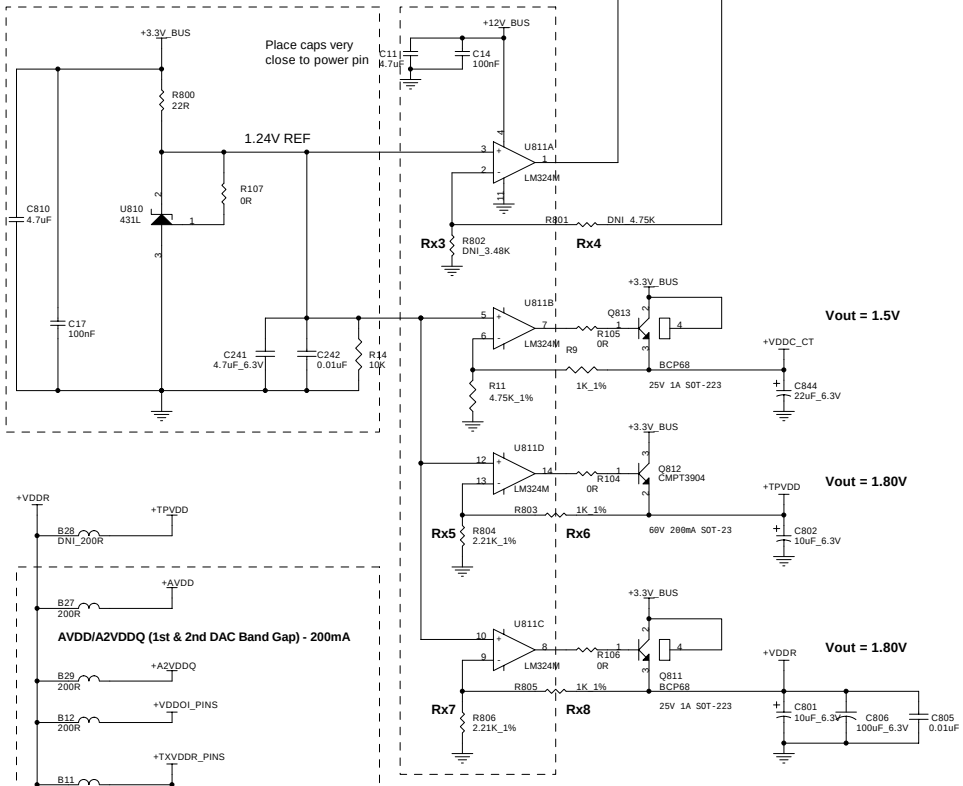
+MVDD	Rx3 / Rx9	Rx4 / Rx10	Memory
2.5V			Infineon,16Mx16, 200MHZ, Samsung,8Mx16, 250MHZ,
2.6V			Samsung, 16Mx16, 200MHZ

REF2	Rx1	Rx2
1.5V [-0.02V/+0.02V]		
+TPVDD / +VDDR		
1.800V		
1.847V		
1.855V		

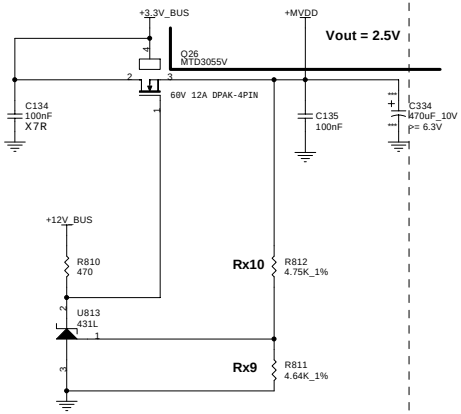
Regulator for :
+MVDD/+A2VDD
+VDDC_CT
+PVDD/+MPVDD
+VDDR4

Vout = 3.3V



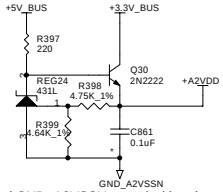


Regulator for +MVDD
Vin = +3.3V AGP
Vout = 2.5V



Regulator for +A2VDD (150mA)

Vin = +3.3V AGP
Vout = 2.5V

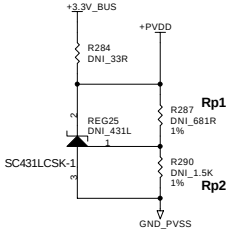


+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

DNI when use 2.5v Mem

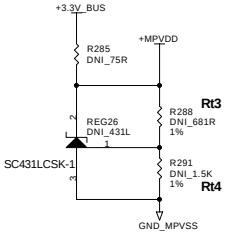
	Rp1 /Rt1/ Rt3	Rp2 /Rt2/ Rt4
1.61V +0.01V/-0.01V	432R 3240432000	1.5K 3230015200
1.69V +0.01V/-0.01V	432R 3240432000	1.21K 3240121100
1.718V +0.01V/-0.01V	562R 3240562000	1.5K 3230015200
1.8175V +0.01V/-0.01V	681R 3240681000	1.5K 3230015200

Regulator for +PVDD (30mA)
Vin = +3.3V AGP
Vout = 1.8V



DNI

Regulator for +MPVDD (10mA)
Vin = +3.3V AGP
Vout = 1.8V



DNI

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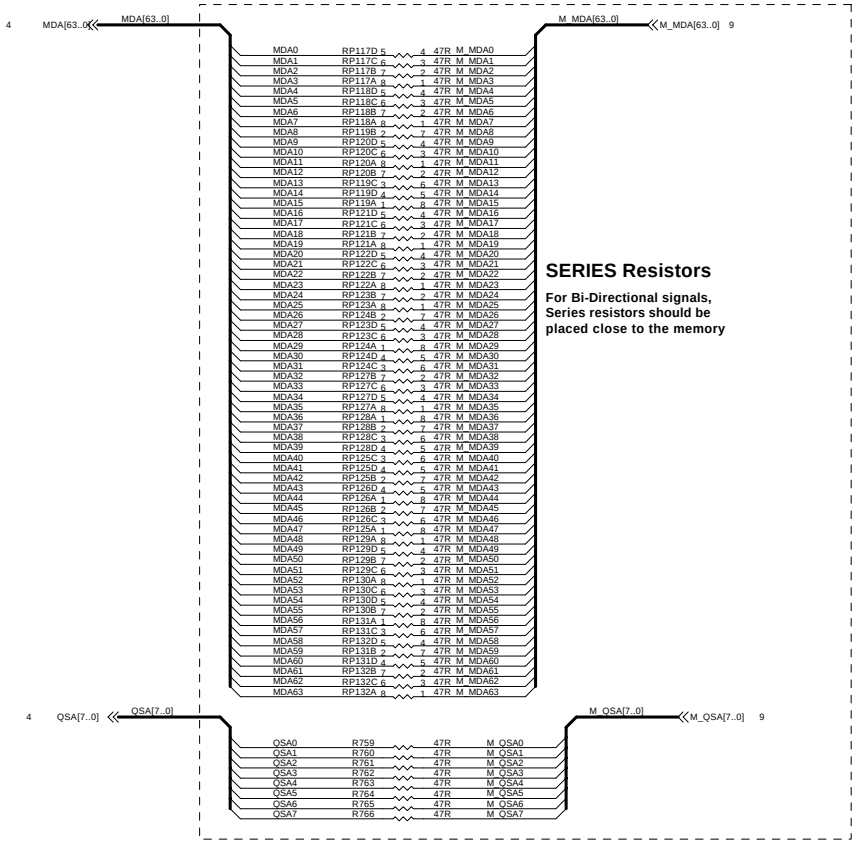
TERMINATION FOR MEMORY CHANNEL A



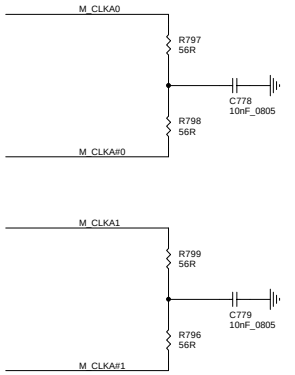
SERIES Resistors

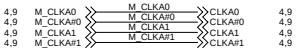
For Bi-Directional signals, Series resistors should be placed close to the memory

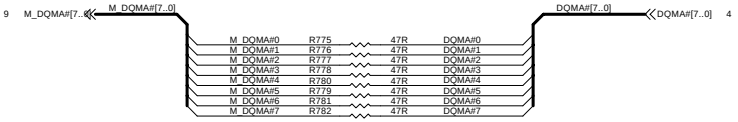
CLOCK terminations

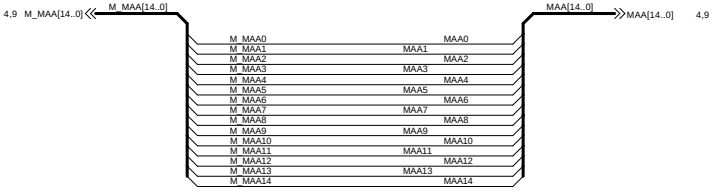
Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

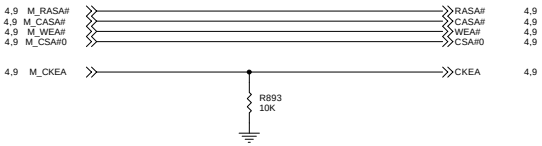
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory











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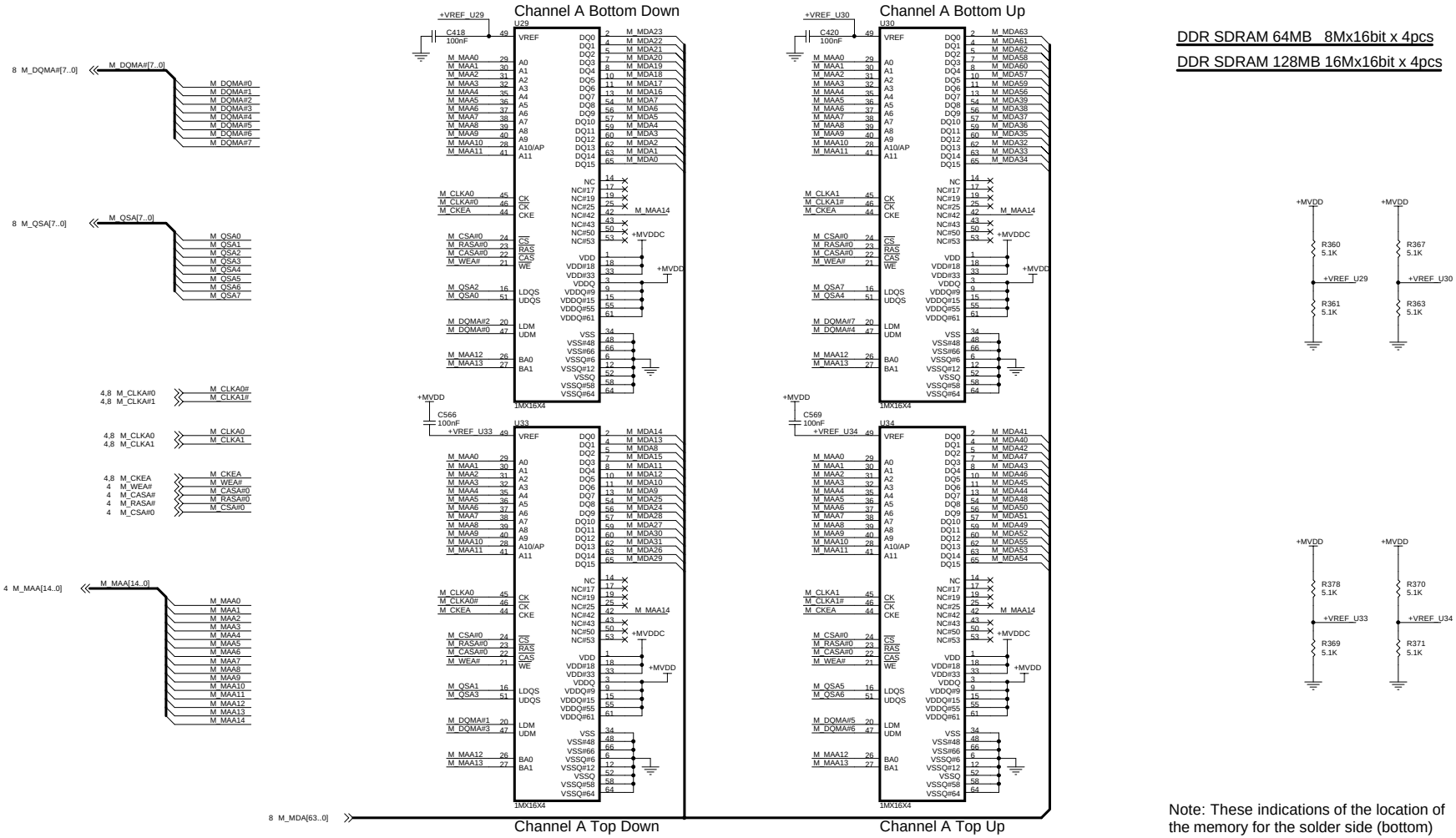
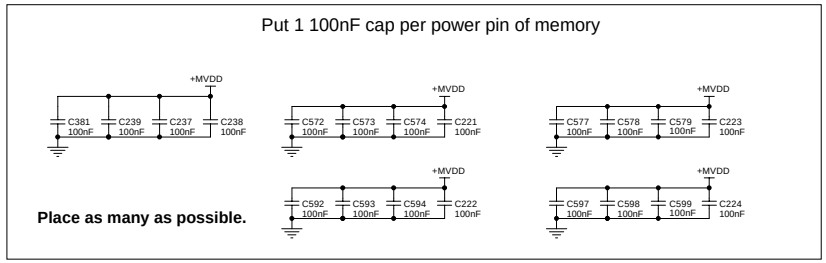
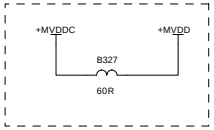


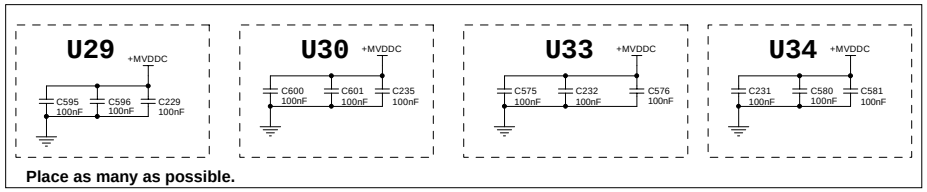
DDR SDRAM 64MB 8Mx16bit x 4pcs

DDR SDRAM 128MB 16Mx16bit x 4pcs

Note: These indications of the location of the memory for the solder side (bottom) are looking thru from the component side.







DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

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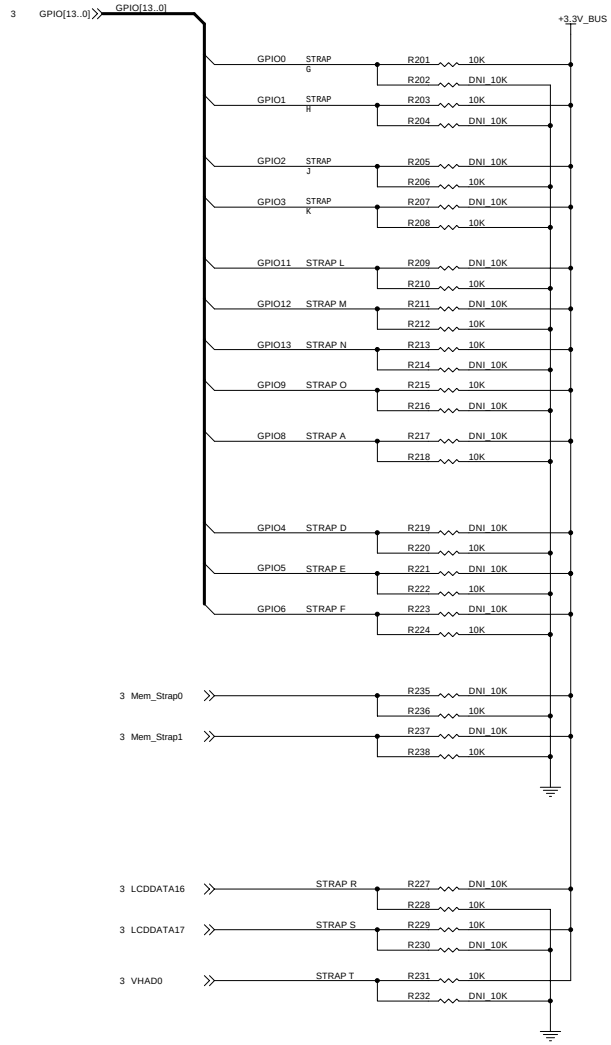
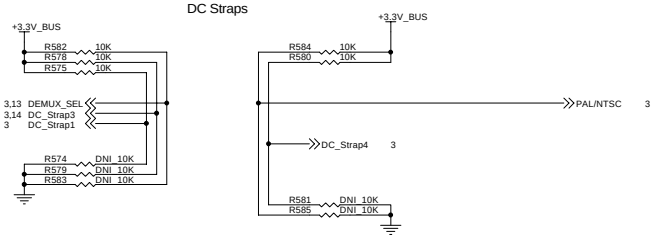
OPTION STRAPS



STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1001
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

DC Straps



STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled **0 - Disabled** 1 - Enabled THIS STRAP IS NOT PRESENT ON THIS CARD!
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19	DAC2 Configuration 0 0 DAC2 Off 0 1 DAC2 On as CRT 1 0 DAC2 On as TVOUT 1 1 DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)
DC_STRAP3	LCDDATA14	Connected to Component TV-Out Detect pin Normally high, pulled low by Component TVO dongle

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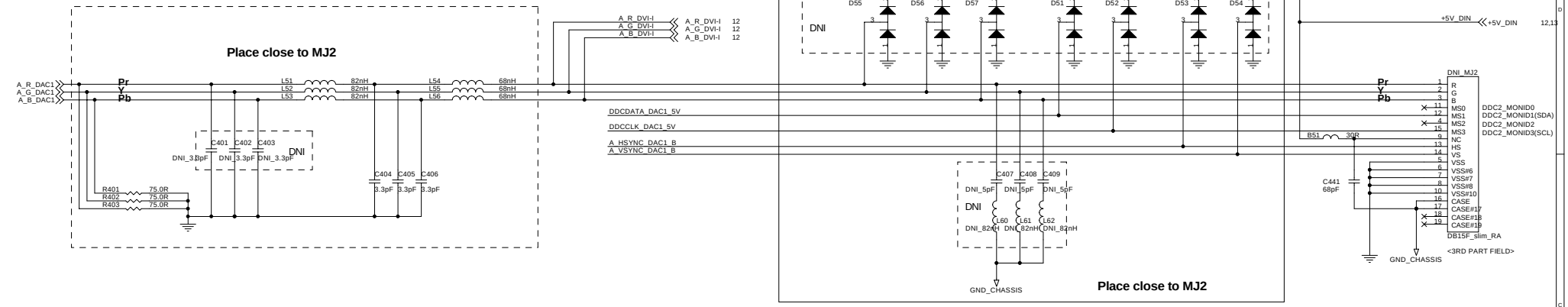
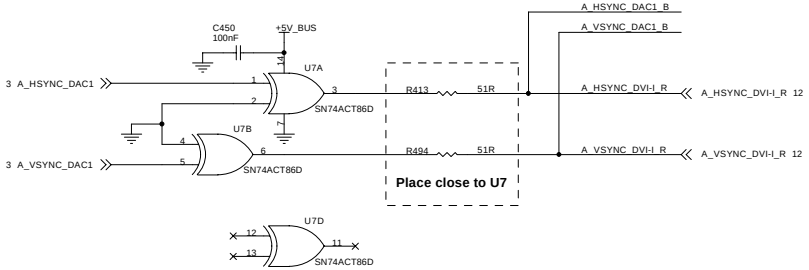
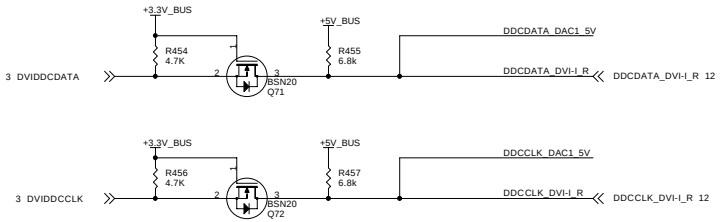
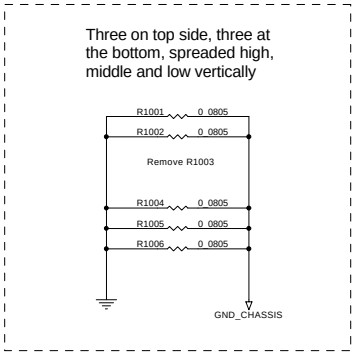
PRIMARY CRT

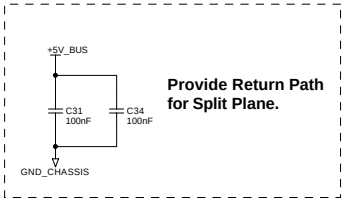


OPTIONAL ESD/HOTPLUG PROTECTION DIODES









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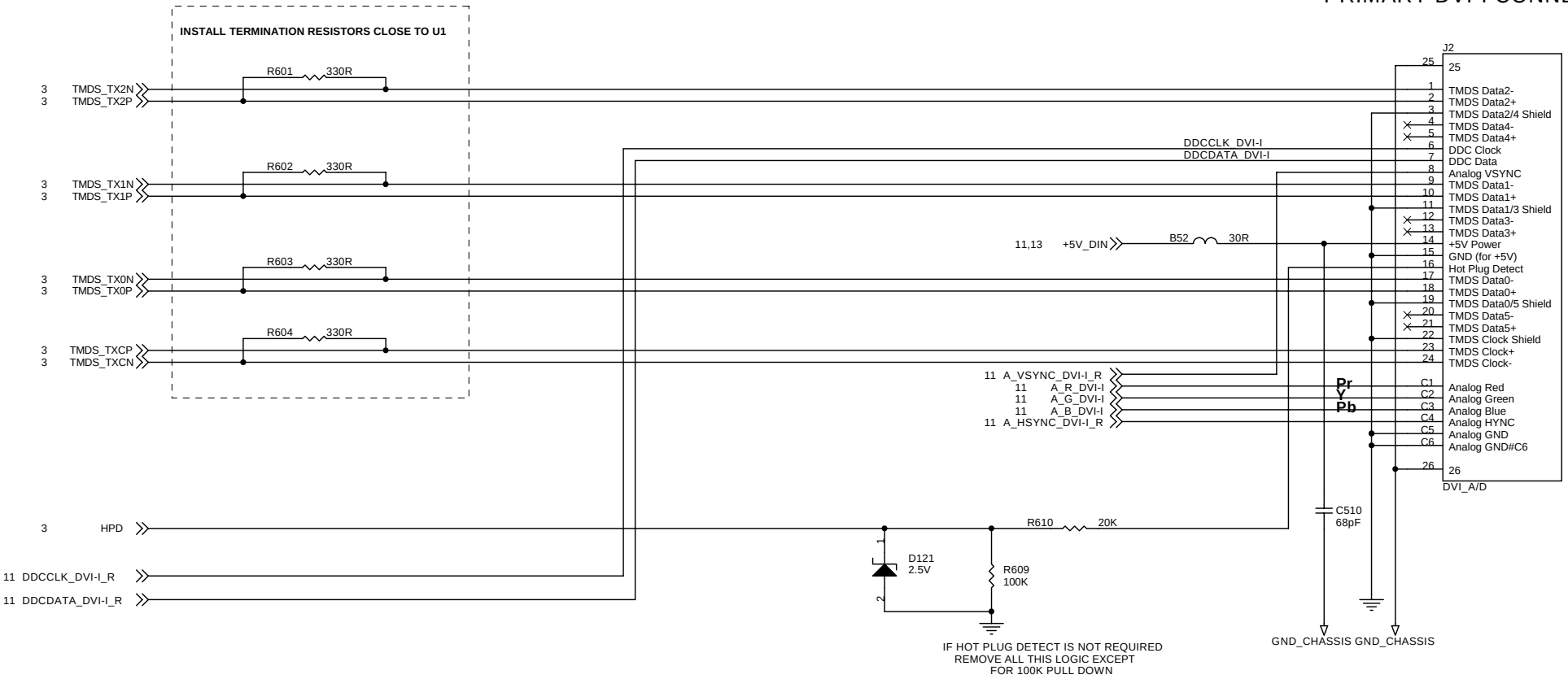
PRIMARY DVI-I CONNECTOR



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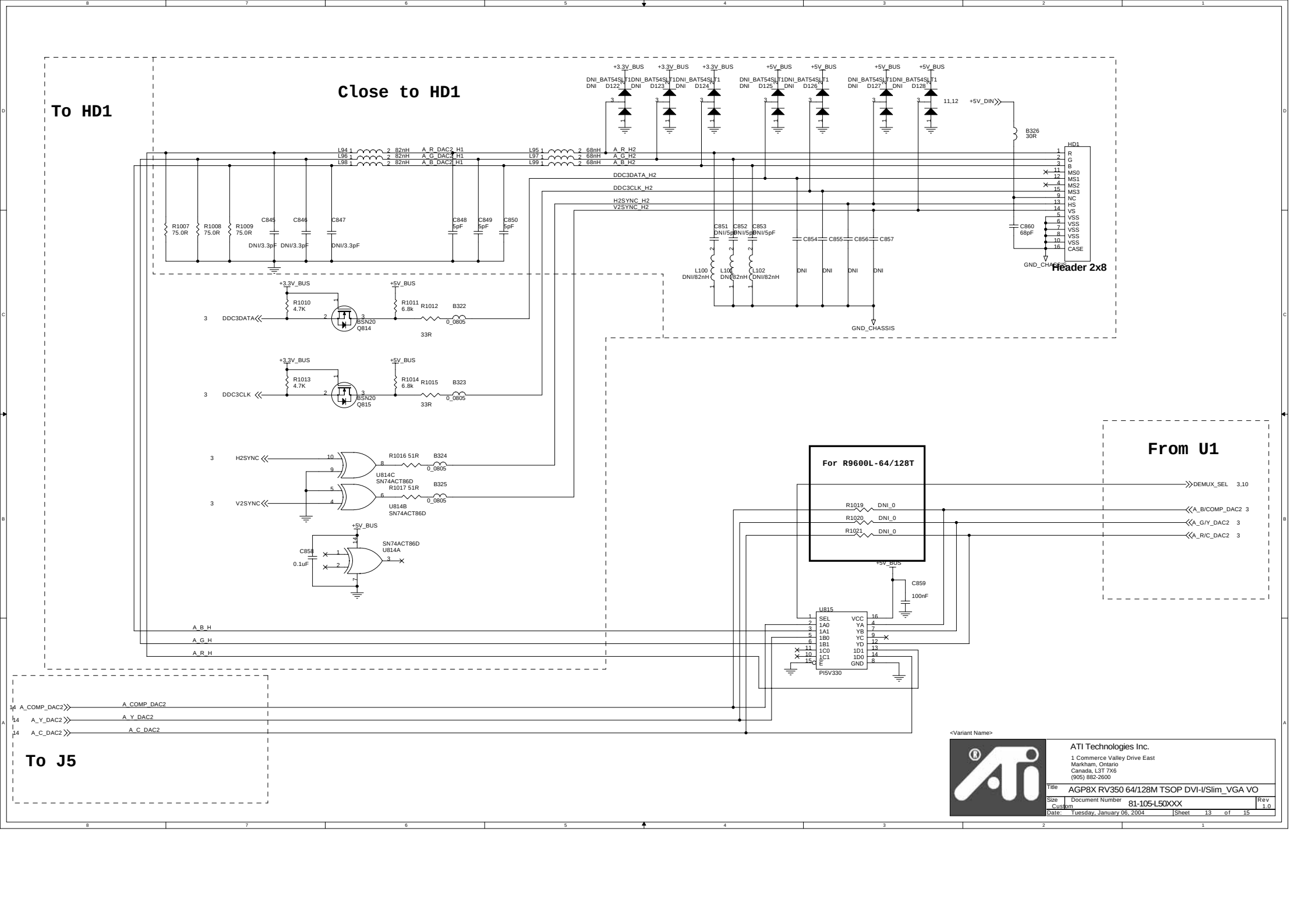
To HD1
Close to HD1
+3.3V_BUS
+5V_BUS
DNI_BAT54SLT1
D122
D123
D124
D125
D126
D127
D128
+5V_DIN
B326
30R
HD1
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
CASE
Header 2x8
L94 82nH A_R_DAC2_H1
L96 82nH A_G_DAC2_H1
L98 82nH A_B_DAC2_H1
L95 68nH A_R_H2
L97 68nH A_G_H2
L99 68nH A_B_H2
DDC3DATA_H2
DDC3CLK_H2
H2SYNC_H2
V2SYNC_H2
R1007 75.0R
R1008 75.0R
R1009 75.0R
C845
C846
C847
DNI/3.3pF
C848 5pF
C849 5pF
C850 5pF
C851 DNI/5pF
C852 DNI/5pF
C853 DNI/5pF
C854
C855
C856
C857
C860 68pF
L100 DNI/82nH
L101 DNI/82nH
L102 DNI/82nH
DNI
GND_CHASSIS
R1010 4.7K
R1011 6.8k
R1012
B322
0_0805
33R
BSN20
Q814
DDC3DATA
R1013 4.7K
R1014 6.8k
R1015
B323
Q815
DDC3CLK
H2SYNC
V2SYNC
R1016 51R
B324
R1017 51R
B325
U814C
SN74ACT86D
U814B
U814A
C858
0.1uF
For R9600L-64/128T
R1019 DNI_0
R1020 DNI_0
R1021 DNI_0
From U1
DEMUX_SEL 3,10
A_B/COMP_DAC2 3
A_G/Y_DAC2 3
A_R/C_DAC2 3
C859
100nF
U815
SEL
1A0
1A1
1B0
1B1
1C0
1C1
E
VCC
YA
YB
YC
YD
1D1
1D0
GND
PI5V330
A_B_H
A_G_H
A_R_H
A_COMP_DAC2
A_Y_DAC2
A_C_DAC2
To J5
<Variant Name>
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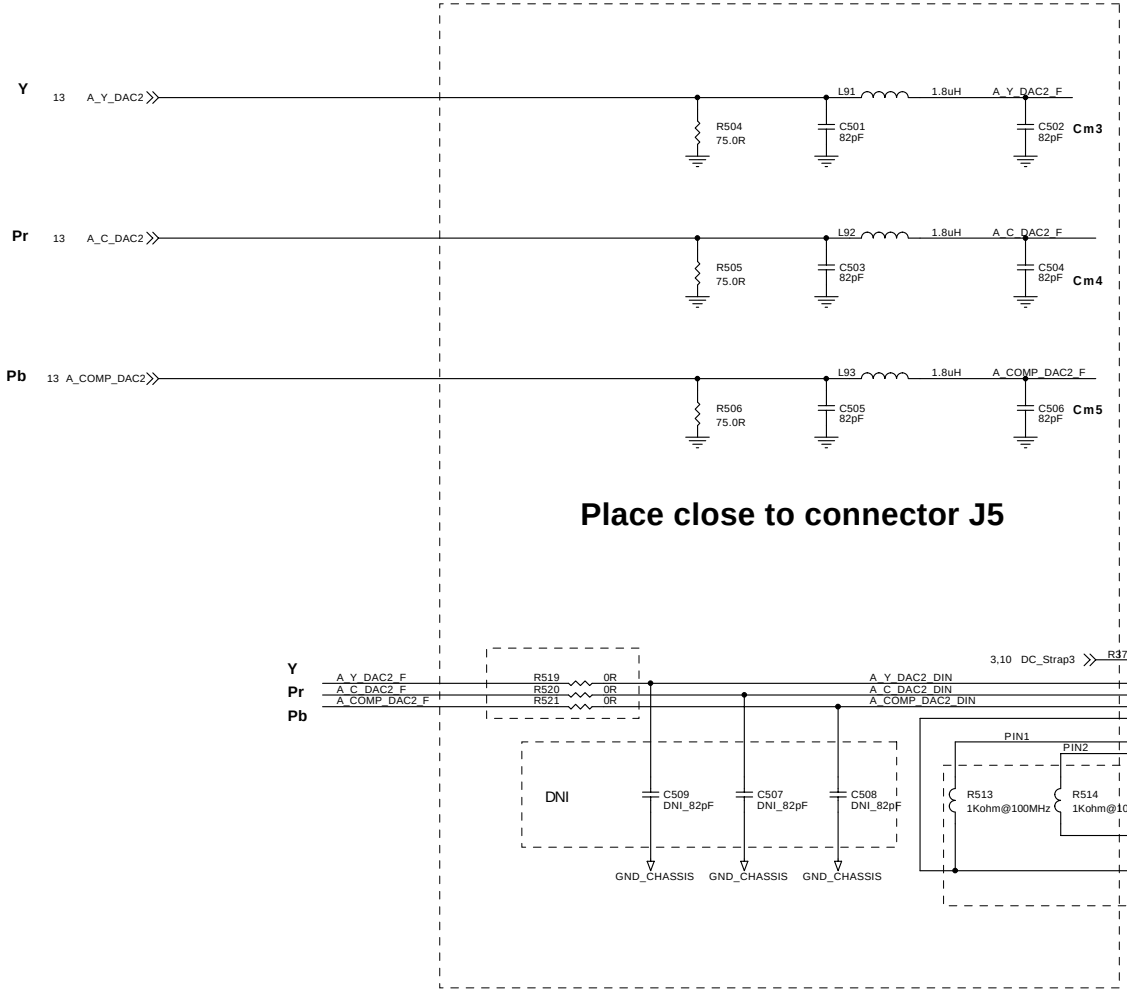

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PCB MOUNTING HOLE

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