1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB_BAFFIN,X363G

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0006897289	ENGINEERING RELEASED	2016-08-24

DRAWING
TITLE=MLB_BAFFIN
ABBREV=ABBREV
LAST_MODIFIED=Wed Aug 24 09:57:44 2016

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00647	1	SCHEM,MLB-BAFFIN,X363G	SCH	CRITICAL	
820-00281	1	PCBF,MLB-BAFFIN,X363G	PCB	CRITICAL	

LAST_MODIFICATION=Wed Aug 24 09:57:44 2016

This is the PVT design

DRAWING TITLE: SCHEM,MLB-BAFFIN,X363

Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
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SHEET: 1 OF 121

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00076	COMMON PARTS,MLB-BAFFIN,X363	X363_COMMON
985-00126	DEV,MLB-BAFFIN,X363	X363_DEVEL:PVT
985-00232	DEV,MLB-BAFFIN,PVT,X363	X363_DEVEL:PVT

639 BOMs have been moved to the end of the schematic

X363 BOM Groups

BOM GROUP	BOM OPTIONS
X363_COMMON	ALTERNATE,COMMON,X363_COMMON1,X363_COMMON2,X363_COMMON3,X363_COMMON4,X363_PROGPARTS
X363_COMMON1	SOC:HYNIX,SE:PROD,SKIP_5V3V3:AUDIBLE,DIPLEXER:MURATA,T208_PROG:REV5,BOARD_ID:17,VCCHDA:S0
X363_COMMON2	XDP:YES,SAMCONN,SOC_BOOT:SPI,DPMUX_XTAL:NO,GPUCLK:OSC,BAFFIN,AP_TEMP,VCCPLLOC:S3,WIFI_SAK:NO
X363_COMMON3	CPUTHRM:ALRT,TBTTHRM:ALRT,LOADRC:NO,OTHERRC:YES,DDRRC:YES,TBTRC:YES,TPADRC:YES,LID_FEATURE_ON
X363_COMMON4	EDP:YES,CPUPEG:X8X4X4,TBTTHRM_SNS,GPUTHRM_SNS,S3_STATE:YES,GPU_ROM:YES,SVID_PU:CORE
X363_PROGPARTS	BOOTROM_PROG:DVT,BT_PROG:DVT,WIFI_PROG:DVT,UPCROM_PROG:DVT,SMC_PROG:PVT,DPMUXMCU:PROG,PCC:NO
X363_DEVEL:ENG	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG,GPUROM:BLANK,PCC:YES
X363_DEVEL:DVT	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG
X363_DEVEL:PVT	ALTERNATE,XDP_CONN,USBC_DBG
ENGISNS	TBTISNS,LOADISNS,TPADISNS,DDRISNS,OTHERISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00227	1	CPU,SKY,SR2FT,R1,PRQ,4/2,2.9,BGA1440	U0500	CRITICAL	CPU_SKL:2.9
337S00228	1	CPU,SKY,SR2FU,R1,PRQ,4/2,2.7,BGA1440	U0500	CRITICAL	CPU_SKL:2.7
337S00229	1	CPU,SKY,SR2FQ,R1,PRQ,4/2,2.6,BGA1440	U0500	CRITICAL	CPU_SKL:2.6
998-04701	1	INTERPOSER,INTEL,BGA1440,MM940989	U0500	CRITICAL	CPU_SKL:SOCKET
337S00258	1	IC,SKL PCH-H,SFF,SR2NH,PRQ,D1,BGA939	U1100	CRITICAL	
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00254	2	IC,TBT,ALPINE RIDGE DP,QT5S,QS,C1,BGA337	U2800,UB000	CRITICAL	
353S01016	1	IC,ISL9239HIZ,PMU,TUBA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00221	1	IC,PMU,P650839,7X7MM.BGA168	U7800	CRITICAL	
338S00142	1	IC,CODEC,CLIFDEN,CS42L83A,B0,WLCSP49	U6300	CRITICAL	
337S00330	1	IC,GPU,BAFFIN,ULA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_ULA
337S00331	1	IC,GPU,BAFFIN,PROA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_PROA
337S00332	1	IC,GPU,BAFFIN,LEA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_LEA
998-04866	1	INTERPOSER,AMD,C989,BGA769,VDDCI/MVDD	UA000	CRITICAL	STARDUST:VDDCI_MVDD
998-04867	1	INTERPOSER,AMD,C988,BGA769,VDDC	UA000	CRITICAL	STARDUST:VDDC
677-04532	2	SUBASSY (T&R) PCBA, AMR, INTERPOSER, X363	J5250,J5260	CRITICAL	

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00076	1	COMMON PARTS,MLB-BAF,X363	BASE	CRITICAL	BASE_BOM
985-00126	1	DEV,MLB-BAF,X363	DEVEL	CRITICAL	DEVEL_BOM

WIFI/BT Diplexers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0979	3	FLTR,DIPLEXER,2.45/5.54GHZ,0805	U3810,U3820,U3830	CRITICAL	DIPLEXER:MURATA

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00227	08	CPU
337S00228	08	CPU
337S00229	08	CPU
333S00050	07	MAIN MEMORY
333S00070	07	MAIN MEMORY
335S00149	02	SSD NAND
335S00204	02	SSD NAND
335S00205	02	SSD NAND
335S00219	02	SSD NAND
339S00154	02	SSD CONTROLLER
339S00155	02	SSD CONTROLLER
338S00166	02	SSD PMIC
337S00225	08	GPU
337S00285	08	GPU
337S00286	08	GPU
333S00044	07	VIDEO MEMORY
333S00043	07	VIDEO MEMORY
333S00078	07	VIDEO MEMORY
333S00074	07	VIDEO MEMORY
333S00075	07	VIDEO MEMORY
343S00135	10	T208
343S00136	10	T208
343S00137	10	T208
338S00138	10	T208
338S00193	09	BERKELIUM
353S3978	02	MOJAVE
338S00097	02	SECURE ELEMENT
338S00254	08	ALPINE RIDGE
353S00961	09	ACE
338S00142	09	CLIFDEN
353S00604	07	AUDIO AMP
353S4316	08	BAYSIDE
338S00221	08	BANJO
353S00853	09	TUBA
339S00056	05	ICEBOCK
359S00006	08	GREEN CLOCK
353S00795	09	DEBUG MUX

GPU Options

BOM GROUP	BOM OPTIONS
2GB_MC_BAFFIN	FB_2GB_MICRON,VRAM:GRP1
2GB_HY_BAFFIN	FB_2GB_HYNIX,VRAM:GRP1
2GB_SM_BAFFIN	FB_2GB_SAMSUNG,VRAM:GRP2
4GB_SM_BAFFIN	FB_4GB_SAMSUNG,VRAM:GRP1
4GB_MC_BAFFIN	FB_4GB_MICRON,VRAM:GRP1

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00050	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_SAMSUNG_2133
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_MICRON_2133

FB VDRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00044	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_MICRON
333S00043	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_HYNIX
333S00078	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_SAMSUNG
333S00074	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_SAMSUNG
333S00075	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_MICRON

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_SAMSUNG_2133	16G_SAMSUNG_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG0:L
RAM_16G_MICRON_2133	16G_MICRON_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L

Sub-BOM DIPLEXER

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00085	DIPLEXERS,MURATA,X363G	DIPLEXER:MURATA

SYNC_MASTER=J80_MLB SYNC_DATE=07/07/2015

PAGE TITLE

BOM Configuration

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DRAWING NUMBER 051-00647 SIZE D

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Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC_PROG:BLANK	Blank
341S00701	1	IC,SMC-B1,EXT (v2.37F7) PVT,X363G	U5000	CRITICAL	SMC_PROG:PVT	TI
335S00013	1	IC,SPI SERIAL FLASH,64M BITS,3V,8P SOIC,QE=1	U6100	CRITICAL	BOOTROM_PROG:BLANK	Blank
341S00699	1	IC,EFI ROM (V0193), DVT, X363G	U6100	CRITICAL	BOOTROM_PROG:DVT	Macronix/Winbond
353S00926	2	IC,CD3215,ACE,B03,BLNK,BGA96	U2890,UB090	CRITICAL	UPCROM_PROG:BLANK	Blank
341S00707	1	T29,AR1 (V10.5) PVT, X363G	U2890	CRITICAL	UPCROM_PROG:DVT	Winbond
341S00708	1	T29,AR2 (V10.5) PVT, X363G	UB090	CRITICAL	UPCROM_PROG:DVT	Winbond
335S00024	1	IC,SERIAL-FLASH,2MBIT,4V,8-USON,2x3x,6MM	U3750	CRITICAL	BT_PROG:BLANK	Blank
341S00695	1	IC,BT ROM (V28), DVT, X362/X363	U3750	CRITICAL	BT_PROG:DVT	Macronix/Winbond
341S00709	1	WIFI ROM (P107) DVT,NEW,WW1,X362/X363	U3710	CRITICAL	WIFI_PROG:DVT	Rohm/On Semi
341S3565	1	IC, EDP MUX-95C, (RENESAS) V3.2.8,DVB,D2	U9800	CRITICAL	DPMUXMCU:PROG	
335S0724	1	IC,1Mbit SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	UA701	CRITICAL	GPUROM:BLANK	Blank

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
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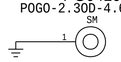
Pogo Pins

APN 870-01771

PG0410
POGO-2.30D-4.63H-SM



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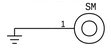
POGO-2.30D-4.63H-SM



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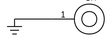

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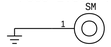

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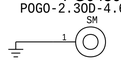

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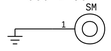
PG0470
POGO-2.30D-4.63H-SM

APN 870-01772

PG0400
POGO-2.30D-4.06H-SM



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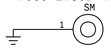

SMT Bosses

APN 860-00392

BS0400
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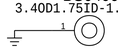

USB-C Left
BOT side - North

BS0410
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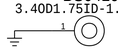

USB-C Right
BOT side - North

APN 806-06520

BS0420
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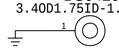

DFR Touch
BOT side

APN 806-06521

BS0430
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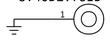

DFR Display
BOT side - Left

BS0440
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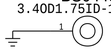

Keyboard
BOT side - Left

BS0450
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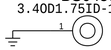

Trackpad
BOT side - Left

APN 860-00413

BS0460
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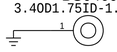
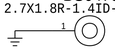


Lifeboat
BOT side - North

APN 860-00469

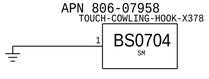
BS0470
2.7X1.8R-1.4ID-0.91H-SM



eDP
TOP side - Left

APN 806-07958
TOUCH-COWLING-HOOK-X378

BS0704
SM



DFR Touch - TOP side

BS0401
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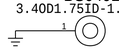
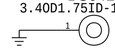


USB-C Left
BOT side - South

BS0411
3.40D1.75ID-1.12H-SM



USB-C Right
BOT side - South

APN 806-06600

BS0480
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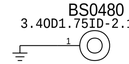

USB-C Right
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BS0431
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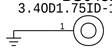
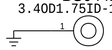


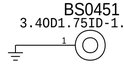
DFR Display
BOT side - Right

BS0441
3.40D1.75ID-1.9H-SM



Keyboard
BOT side - Right

BS0451
3.40D1.75ID-1.9H-SM



Trackpad
BOT side - Right

APN 860-00461

BS0461
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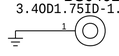
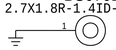


Lifeboat
BOT side - South

BS0701
2.7X1.8R-1.4ID-0.91H-SM



eDP
TOP side - Right

Rubber Mount Standoffs

APN 860-00452

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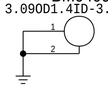

APN 860-00435

BM0401
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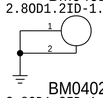
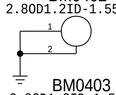


BM0402
2.8OD1.2ID-1.55H-SM



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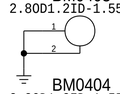

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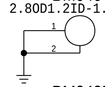

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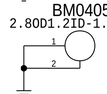

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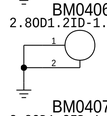

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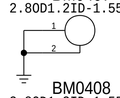

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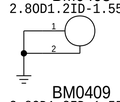

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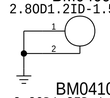

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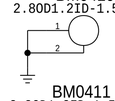

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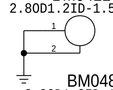

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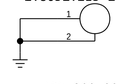
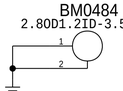


APN 860-00500

BM0484
2.8OD1.2ID-3.5H-SM



APN 860-00500

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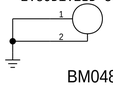

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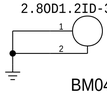

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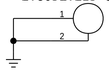
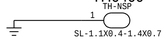


Shield Can TH

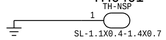
APN 998-2691

TH0400
TH-NSP



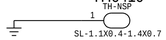
System Memory - BOT side - Left

TH0401
TH-NSP



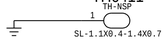
System Memory - BOT side - Right

TH0410
TH-NSP



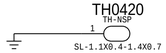
TBT Left - BOT side - North

TH0411
TH-NSP



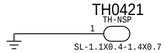
TBT Left - BOT side - South

TH0420
TH-NSP



TBT Right - BOT side - North

TH0421
TH-NSP



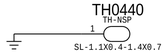
TBT Right - BOT side - South

T208 - TOP side - North

T208 through holes are non-plated... for now

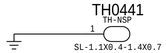
T208 - TOP side - South

TH0440
TH-NSP



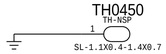
SSD - BOT side - North

TH0441
TH-NSP



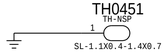
SSD - BOT side - South

TH0450
TH-NSP



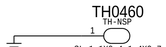
SSD - TOP side - North

TH0451
TH-NSP



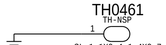
SSD - TOP side - South

TH0460
TH-NSP



Frame Buffer Memory - BOT side - Left

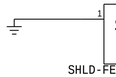
TH0461
TH-NSP



Frame Buffer Memory - BOT side - Right

Shield Can Fence

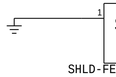
SH0400
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
DRAM - BOT side
APN 806-06590

SH0410
SM



SHLD-FENCE-MLB-M8-X379

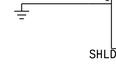
OMIT_TABLE
AR Right - BOT side
APN 806-06586

SH0420
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
AR Left - BOT side
APN 806-06588

SH0430
SM



SHLD-FENCE-M8-X379

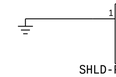
T208 - TOP side
APN 806-07814

SH0440
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
SSD - TOP side
APN 806-06584

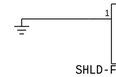
SH0450
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
SSD - BOT side
APN 806-06585

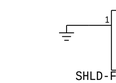
SH0460
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
Diplexer - BOT side
APN 806-06591

SH0470
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
VRAM - BOT side
APN 806-08026

Shield Can Omit Table

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08023	1	SHIELD,FENCE,DRAM,X378	SH0400	CRITICAL	
806-08019	1	SHIELD,FENCE,ALPINE RIDGE,RIGHT,X378	SH0410	CRITICAL	
806-08021	1	SHIELD,FENCE,ALPINE RIDGE,LEFT,X378	SH0420	CRITICAL	
806-07918	1	SHIELD,NAND,TOP,ALT,X363	SH0440	CRITICAL	
806-07917	1	SHIELD,NAND,BOTTOM,ALT,X363	SH0450	CRITICAL	
806-08024	1	SHIELD,DIPLEX,EG,X378	SH0460	CRITICAL	
806-08026	1	FENCE,VRAM,EG,X378	SH0470	CRITICAL	

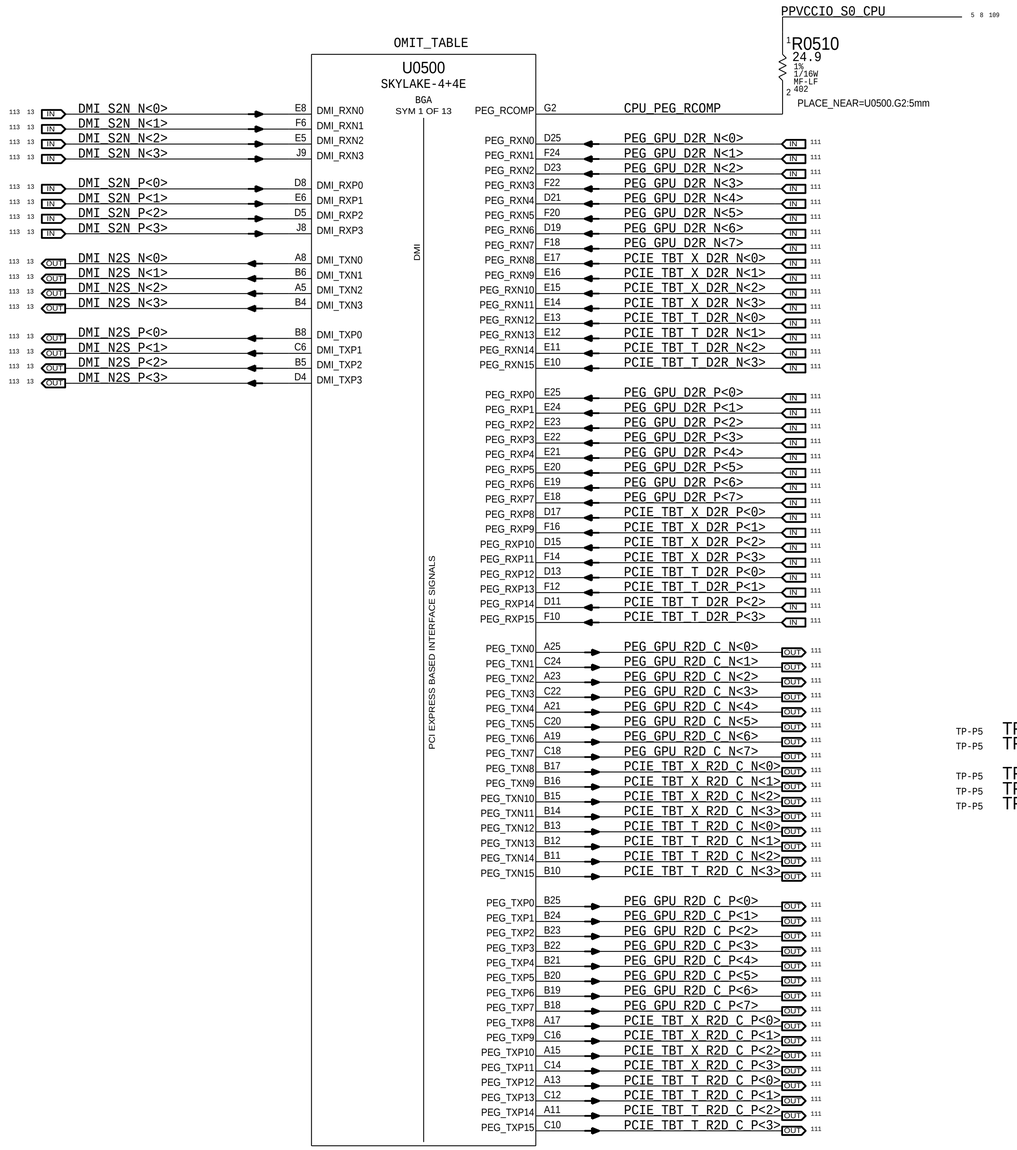
BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=J80_MLB SYNC_DATE=11/16/2015

PAGE TITLE
PD Parts

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 4 OF 145
SHEET 4 OF 121



PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

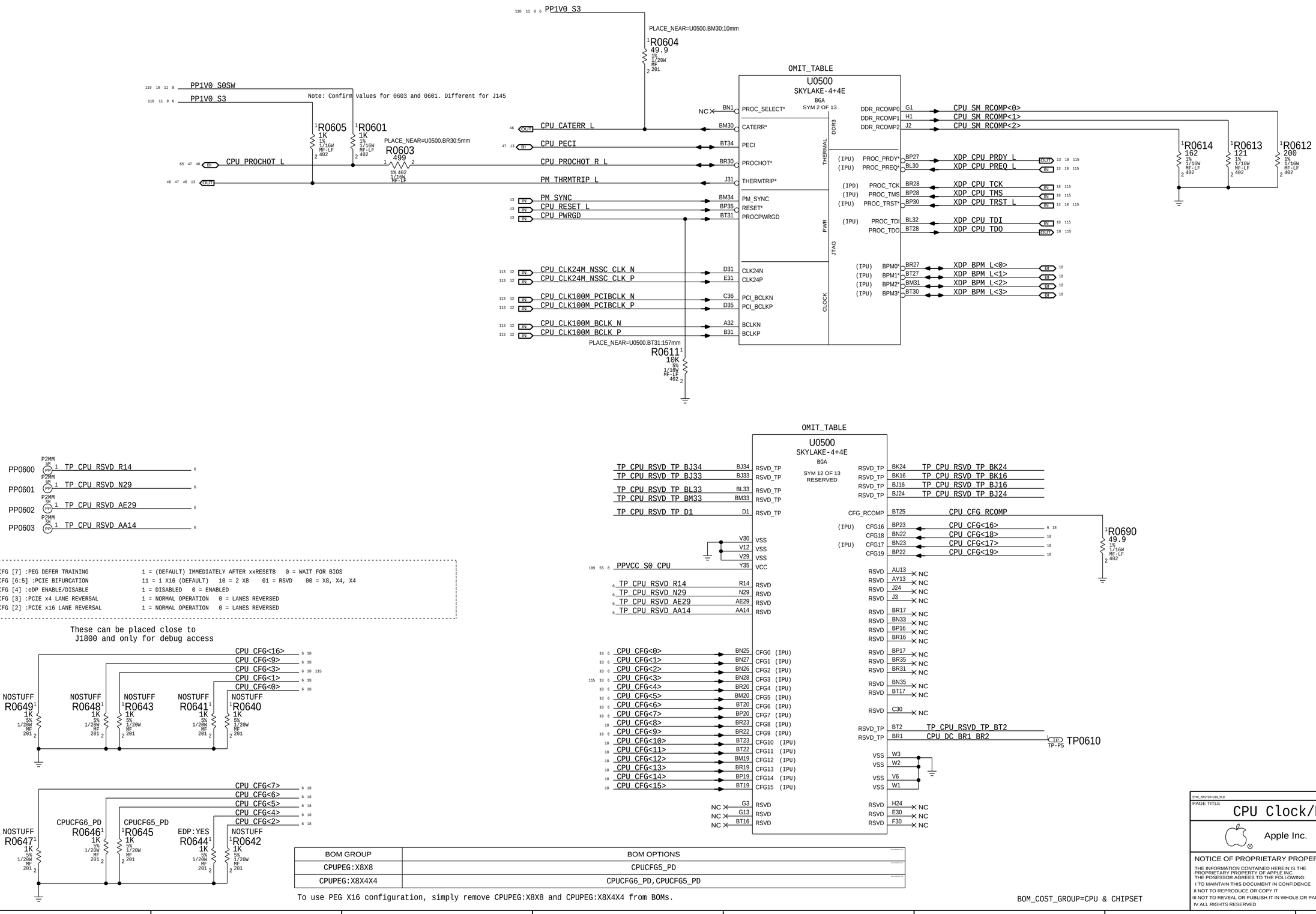
DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 5 OF 145

SHEET 5 OF 121



BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2016

PAGE TITLE

CPU Clock/Misc/JTAG/CFG

Apple Inc.

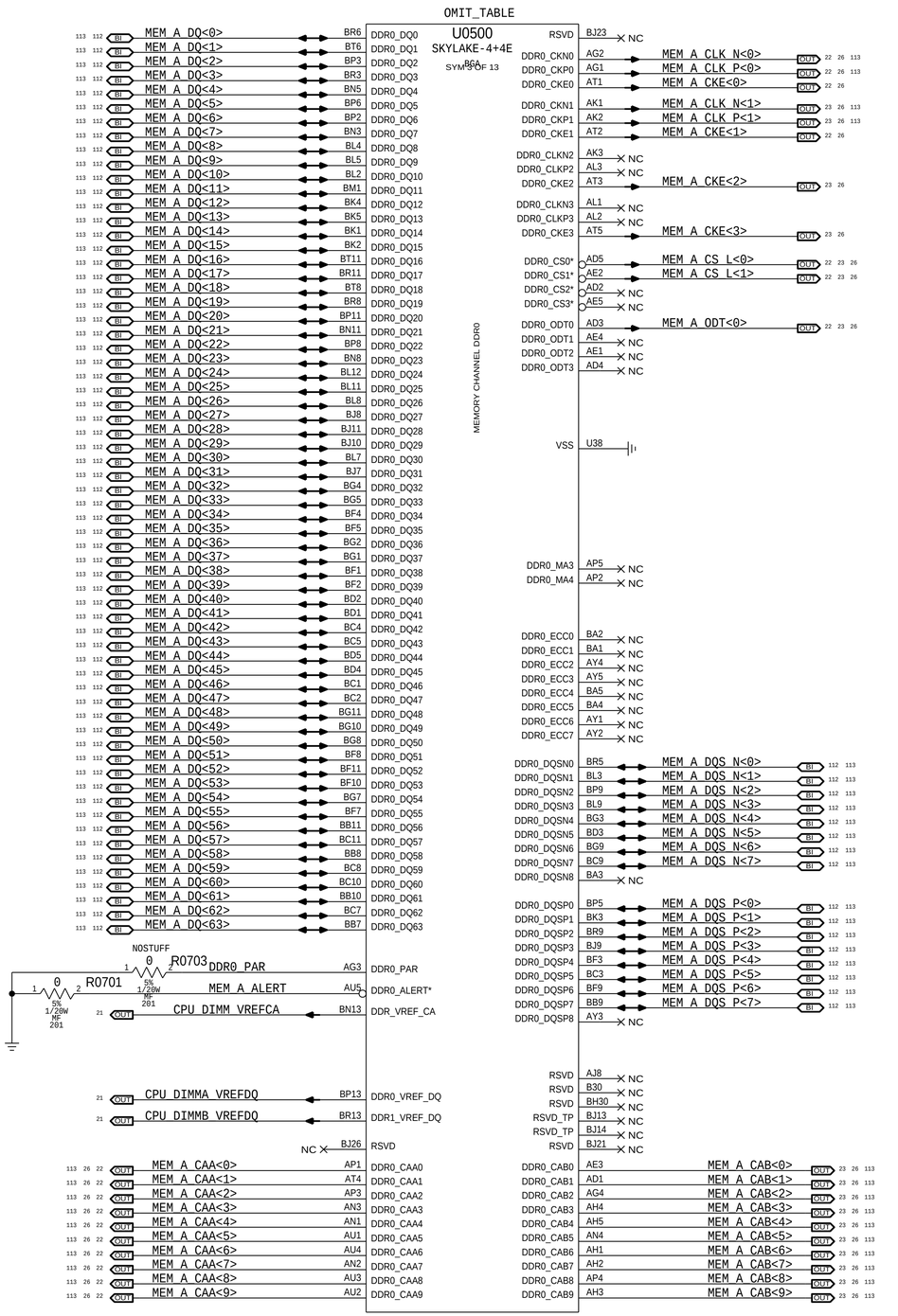
DRAWING NUMBER 051-00647 SIZE D

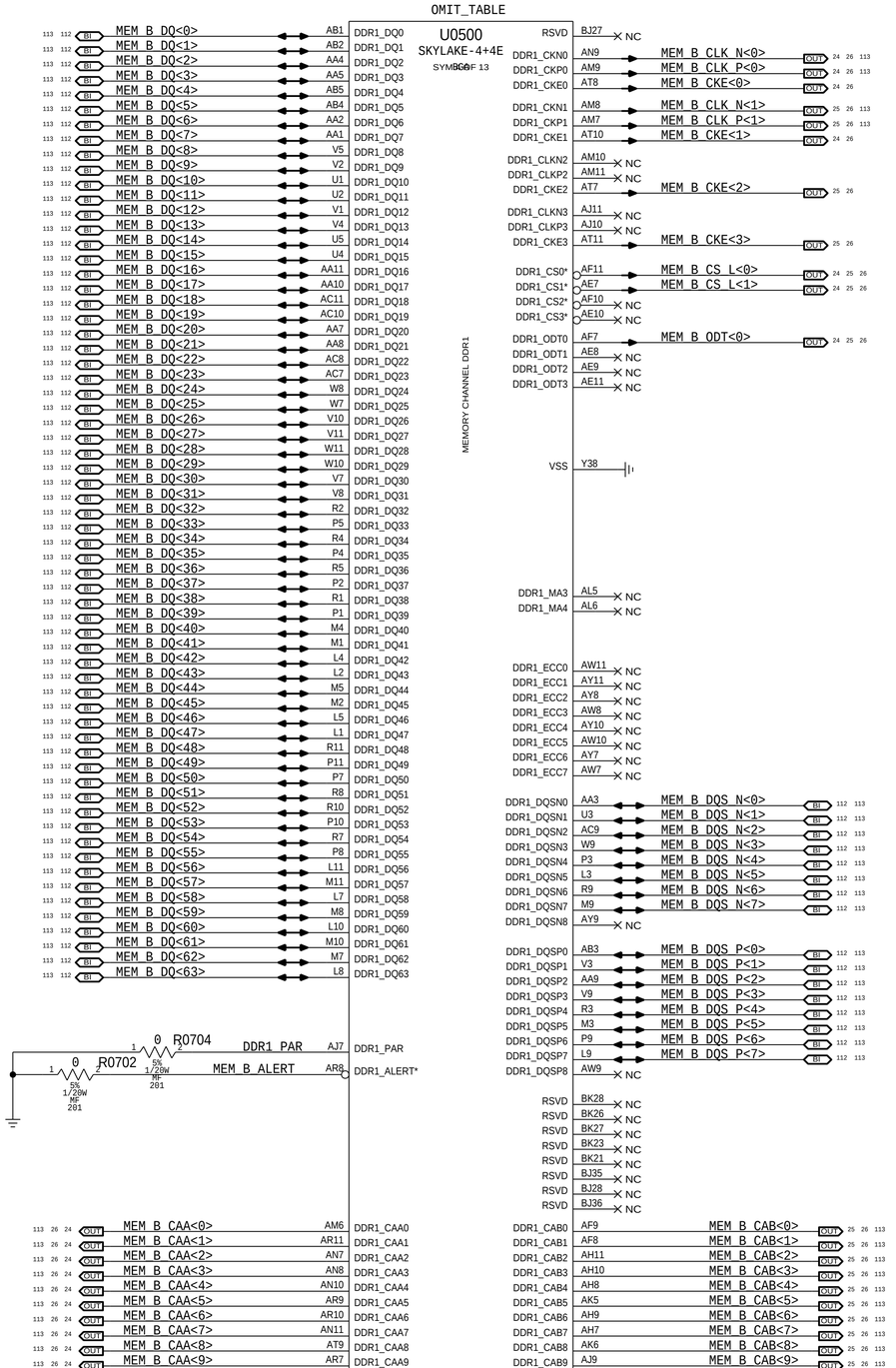
REVISION 10.0.0

BRANCH dvt-fab10

PAGE 6 OF 145

SHEET 6 OF 121





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

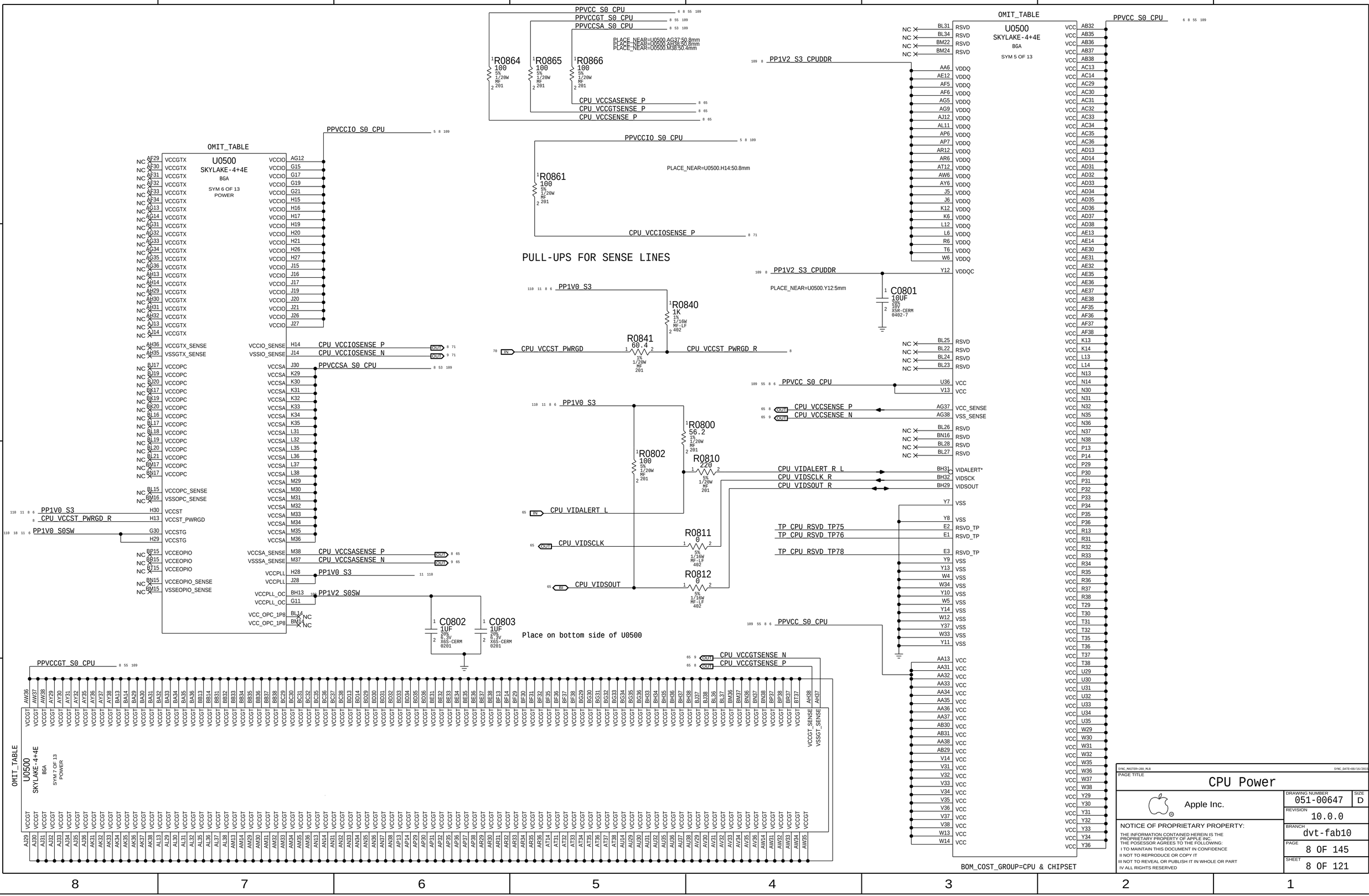
DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 7 OF 145

SHEET 7 OF 121



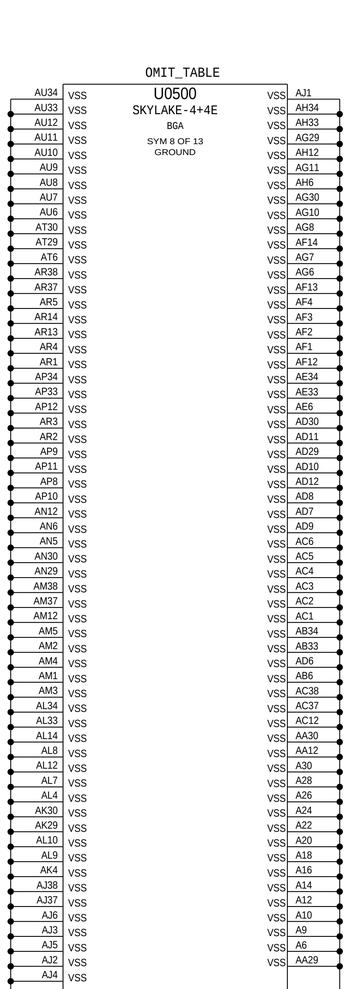
SYNC_MASTER=J80_MLB SYNC_DATE=08/16/2016

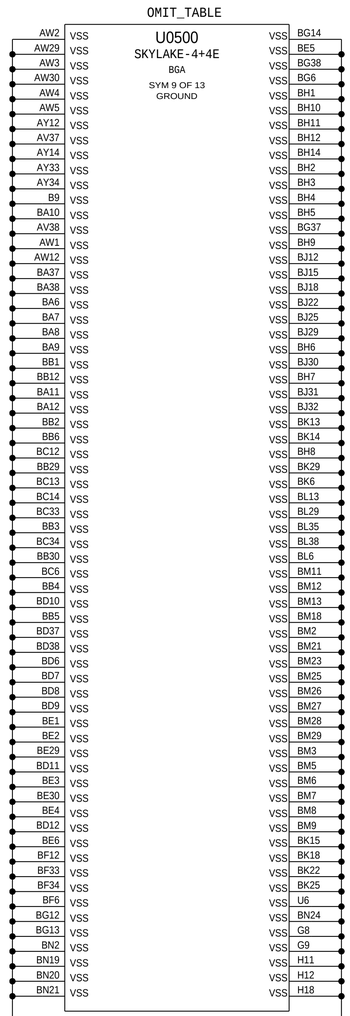
PAGE TITLE

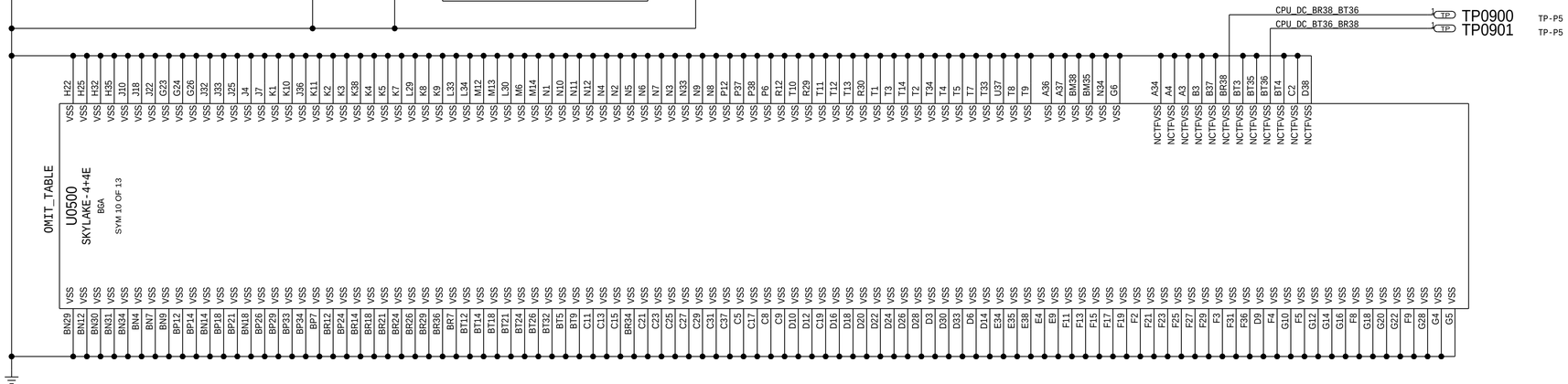
CPU Power

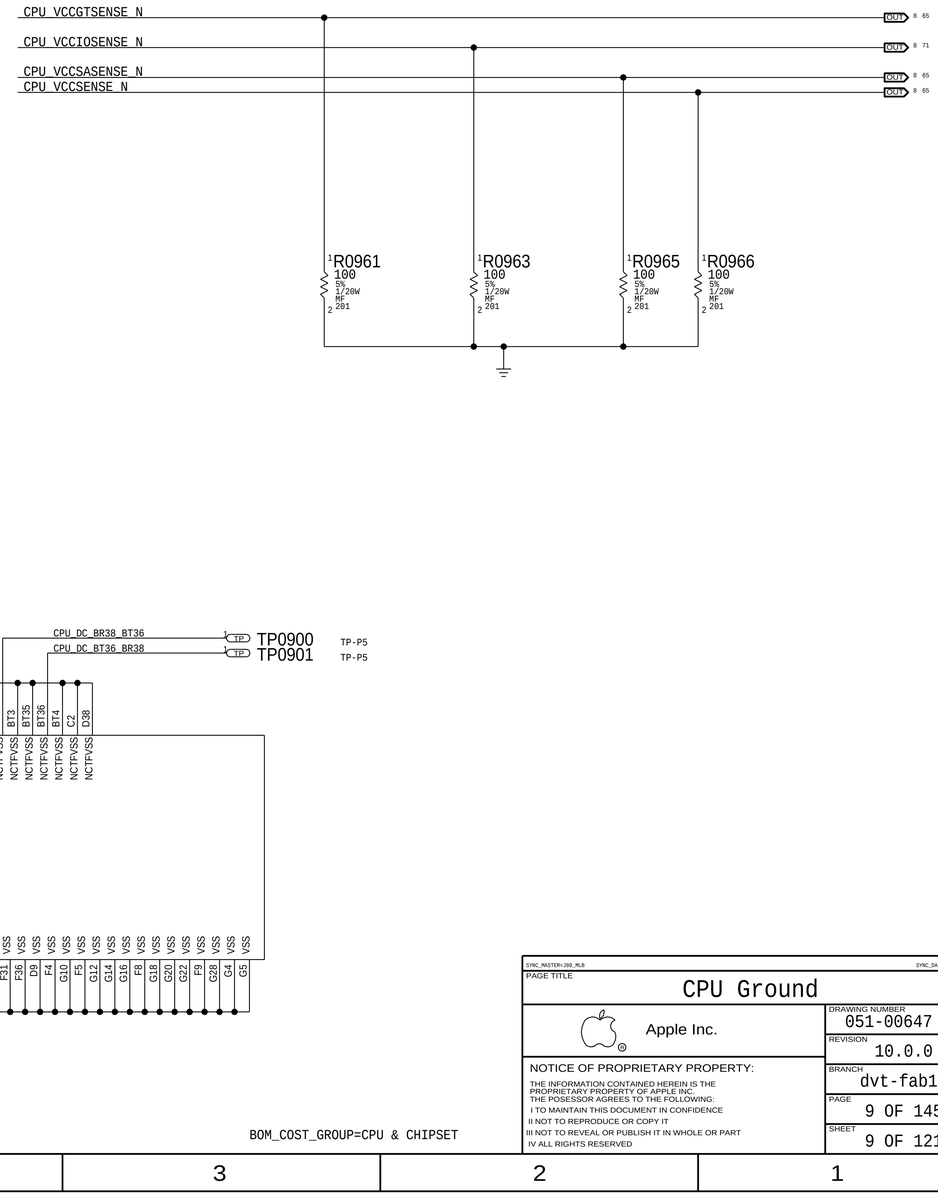
Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	8 OF 145
SHEET	8 OF 121









BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=08/17/2015

PAGE TITLE

CPU Ground

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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SHEET 9 OF 121

Vcc CPU Core Decoupling from 20140905 BOM

CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201   Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU Decoupling 1 [10]

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10

Vcc GT Slice Core Decoupling from 20140905 BOM

CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side

116 109 PPVCCGT_S0_CPU

Place on bottom side of U0500

C1100 1UF 20% 4V CERM-X6S 0201
C1101 1UF 20% 4V CERM-X6S 0201
C1102 1UF 20% 4V CERM-X6S 0201
C1103 1UF 20% 4V CERM-X6S 0201
C1104 1UF 20% 4V CERM-X6S 0201
C1105 1UF 20% 4V CERM-X6S 0201
C1106 1UF 20% 4V CERM-X6S 0201
C1107 1UF 20% 4V CERM-X6S 0201
C1108 1UF 20% 4V CERM-X6S 0201
C1109 1UF 20% 4V CERM-X6S 0201
C1110 1UF 20% 4V CERM-X6S 0201
C1111 1UF 20% 4V CERM-X6S 0201
C1112 1UF 20% 4V CERM-X6S 0201
C1113 1UF 20% 4V CERM-X6S 0201
C1114 1UF 20% 4V CERM-X6S 0201
C1115 1UF 20% 4V CERM-X6S 0201
C1116 1UF 20% 4V CERM-X6S 0201
C1117 1UF 20% 4V CERM-X6S 0201
C1118 1UF 20% 4V CERM-X6S 0201
C1119 1UF 20% 4V CERM-X6S 0201
C1120 1UF 20% 4V CERM-X6S 0201
C1121 1UF 20% 4V CERM-X6S 0201
C1122 1UF 20% 4V CERM-X6S 0201
C1123 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1124 1UF 20% 4V CERM-X6S 0201
C1125 1UF 20% 4V CERM-X6S 0201
C1126 1UF 20% 4V CERM-X6S 0201
C1127 1UF 20% 4V CERM-X6S 0201
C1128 1UF 20% 4V CERM-X6S 0201
C1129 1UF 20% 4V CERM-X6S 0201
C1130 1UF 20% 4V CERM-X6S 0201
C1131 1UF 20% 4V CERM-X6S 0201
C1132 1UF 20% 4V CERM-X6S 0201
C1133 1UF 20% 4V CERM-X6S 0201
C1134 1UF 20% 4V CERM-X6S 0201
C1135 1UF 20% 4V CERM-X6S 0201
C1136 1UF 20% 4V CERM-X6S 0201
C1137 1UF 20% 4V CERM-X6S 0201
C1138 1UF 20% 4V CERM-X6S 0201
C1139 1UF 20% 4V CERM-X6S 0201
C1140 1UF 20% 4V CERM-X6S 0201
C1141 1UF 20% 4V CERM-X6S 0201
C1142 1UF 20% 4V CERM-X6S 0201
C1143 1UF 20% 4V CERM-X6S 0201
C1144 1UF 20% 4V CERM-X6S 0201
C1145 1UF 20% 4V CERM-X6S 0201
C1146 1UF 20% 4V CERM-X6S 0201
C1147 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1148 1UF 20% 4V CERM-X6S 0201
C1149 1UF 20% 4V CERM-X6S 0201
C1150 1UF 20% 4V CERM-X6S 0201
C1151 1UF 20% 4V CERM-X6S 0201
C1152 1UF 20% 4V CERM-X6S 0201
C1153 1UF 20% 4V CERM-X6S 0201
C1154 1UF 20% 4V CERM-X6S 0201
C1155 1UF 20% 4V CERM-X6S 0201
C1156 1UF 20% 4V CERM-X6S 0201
C1157 1UF 20% 4V CERM-X6S 0201
C1158 1UF 20% 4V CERM-X6S 0201
C1159 1UF 20% 4V CERM-X6S 0201
C1160 1UF 20% 4V CERM-X6S 0201
C1161 1UF 20% 4V CERM-X6S 0201
C1162 1UF 20% 4V CERM-X6S 0201
C1163 1UF 20% 4V CERM-X6S 0201
C1164 1UF 20% 4V CERM-X6S 0201
C1165 1UF 20% 4V CERM-X6S 0201
C1166 1UF 20% 4V CERM-X6S 0201
C1167 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11A0 20UF 20% 2.5V X6S-CERM 0402-1
C11A1 20UF 20% 2.5V X6S-CERM 0402-1
C11A2 20UF 20% 2.5V X6S-CERM 0402-1
C11A3 20UF 20% 2.5V X6S-CERM 0402-1
C11A4 20UF 20% 2.5V X6S-CERM 0402-1
C11A5 20UF 20% 2.5V X6S-CERM 0402-1
C11A6 20UF 20% 2.5V X6S-CERM 0402-1
C11A7 20UF 20% 2.5V X6S-CERM 0402-1
C11A8 20UF 20% 2.5V X6S-CERM 0402-1
C11A9 20UF 20% 2.5V X6S-CERM 0402-1
C11B0 20UF 20% 2.5V X6S-CERM 0402-1
C11B1 20UF 20% 2.5V X6S-CERM 0402-1
C11B2 20UF 20% 2.5V X6S-CERM 0402-1
C11B3 20UF 20% 2.5V X6S-CERM 0402-1
C11B4 20UF 20% 2.5V X6S-CERM 0402-1
C11B5 20UF 20% 2.5V X6S-CERM 0402-1
C11B6 20UF 20% 2.5V X6S-CERM 0402-1
C11B7 20UF 20% 2.5V X6S-CERM 0402-1
C11B8 20UF 20% 2.5V X6S-CERM 0402-1
C11B9 20UF 20% 2.5V X6S-CERM 0402-1
C11C0 20UF 20% 2.5V X6S-CERM 0402-1
C11C1 20UF 20% 2.5V X6S-CERM 0402-1
C11C2 20UF 20% 2.5V X6S-CERM 0402-1
C11C3 20UF 20% 2.5V X6S-CERM 0402-1
C11C4 20UF 20% 2.5V X6S-CERM 0402-1
C11C5 20UF 20% 2.5V X6S-CERM 0402-1
C11C6 20UF 20% 2.5V X6S-CERM 0402-1
C11C7 20UF 20% 2.5V X6S-CERM 0402-1
C11C8 20UF 20% 2.5V X6S-CERM 0402-1
C11C9 20UF 20% 2.5V X6S-CERM 0402-1
C11D0 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11F0 20UF 20% 2.5V X6S-CERM 0402-1
C11F1 20UF 20% 2.5V X6S-CERM 0402-1
C11F2 20UF 20% 2.5V X6S-CERM 0402-1
C11F3 20UF 20% 2.5V X6S-CERM 0402-1
C11F4 20UF 20% 2.5V X6S-CERM 0402-1
C11F5 20UF 20% 2.5V X6S-CERM 0402-1
C11F6 20UF 20% 2.5V X6S-CERM 0402-1
C11F7 20UF 20% 2.5V X6S-CERM 0402-1
C11E0 20UF 20% 2.5V X6S-CERM 0402-1
C11E1 20UF 20% 2.5V X6S-CERM 0402-1
C11E2 20UF 20% 2.5V X6S-CERM 0402-1
C11E3 20UF 20% 2.5V X6S-CERM 0402-1
C11E4 20UF 20% 2.5V X6S-CERM 0402-1
C11E5 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11D4 20UF 20% 2.5V X6S-CERM 0402-1
C11D3 20UF 20% 2.5V X6S-CERM 0402-1
C11D2 20UF 20% 2.5V X6S-CERM 0402-1
C11D1 20UF 20% 2.5V X6S-CERM 0402-1

C1168 220UF 20% 2V ELEC SM-COMBO
C1169 220UF 20% 2V ELEC SM-COMBO
C1170 220UF 20% 2V ELEC SM-COMBO
C1171 220UF 20% 2V ELEC SM-COMBO
C1172 220UF 20% 2V ELEC SM-COMBO

CPU VCCSTG Decoupling

110 18 8 6 PP1V0_S0SW

Place near U0500 on bottom side

C11L1 1UF 20% 4V CERM-X6S 0201
C11L2 1UF 20% 4V CERM-X6S 0201

CPU VCCPLL and VCCST Decoupling

110 8 PP1V0_S3

110 8 6 PP1V0_S3

C11M1 1UF 20% 4V CERM-X6S 0201
C11M2 1UF 20% 4V CERM-X6S 0201

Place near U0500 on bottom side

109 PPVCCSA_S0_CPU

Place on bottom side of U0500

C11H0 1UF 20% 4V CERM-X6S 0201
C11H1 1UF 20% 4V CERM-X6S 0201
C11H2 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11I0 20UF 20% 2.5V X6S-CERM 0402-1
C11I1 20UF 20% 2.5V X6S-CERM 0402-1
C11I2 20UF 20% 2.5V X6S-CERM 0402-1
C11I3 20UF 20% 2.5V X6S-CERM 0402-1
C11I4 20UF 20% 2.5V X6S-CERM 0402-1
C11I5 20UF 20% 2.5V X6S-CERM 0402-1
C11I6 20UF 20% 2.5V X6S-CERM 0402-1
C11I7 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11J0 47UF 20% 6.3V POLY-TANT 0805
C11J1 47UF 20% 6.3V POLY-TANT 0805

C11K9 220UF 20% 2V ELEC SM-COMBO

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU Decoupling 2 [11]

Apple Inc.

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REVISION: 10.0.0
BRANCH: dvt-fab10
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OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 4 OF 12

SYSTEM POWER MANAGEMENT

48 IN	SMC_PCH_SUSACK_L	AL15	GPP_A15/SUSACK* (IPU)	DRAM_RESET*	AM11	NC_PCH_DRAM_RESET_L 20
115 46 18 12 IN	PM_SYSRST_L	AJ4	SYS_RESET*	(OD) DSW_PWROK	AF8	PM_DSW_PWRGD — IN 46
114 73 46 IN	PM_PCH_SYS_PWROK	AK3	SYS_PWROK	(IPD-DeepSx) WAKE*	AG12	PCIE_WAKE_L — IN 12 19
115 70 IN	PM_PCH_PWROK	AJ11	PCH_PWROK	GPP_A8/CLKRUN*	AK14	LPC_CLKRUN_L — BI 12 46
				GPP_A14/SUS_STAT*/ESPI_RESET*	AM15	LPC_PWRDWN_L — OUT 46
114 35 20 OUT	PLT_RST_L	AG23	GPP_B13/PLTRST*	(IPU-RSMRST#) GPD8/SUSCLK	AH12	PM_CLK32K_SUSCLK_R — OUT 47
115 73 46 18 IN	PM_RSMRST_L	AF12	RSMRST*	GPD10/SLP_S5*	AG10	PM_SLP_S5_L — OUT 12 20 46 73
48 OUT	SMC_PCH_SUSWARN_L	AJ16	GPP_A13/SUSWARN* /SUSPWRDNACK	GPD5/SLP_S4*	AK10	PM_SLP_S4_L — OUT 12 20 43 46 70 73
48 12 IN	PM_PWRBTN_L	AM10	GPD3/PWRBTN*	GPD4/SLP_S3*	AK9	PM_SLP_S3_L — OUT 12 20 27 46 70 73 76 89 101 114
12	SSD_SR_EN_L	AL12	GPD1/ACPRESENT	GPD6/SLP_A*	AG11	NC_PCH_SLP_A_L 20
103 46 29 12 IN	PM_BATLOW_L (IPU)	AM12	GPD0/BATLOW*	SLP_SUS*	AH13	PM_SLP_SUS_L — OUT 12 70 73
70 46 20 12 OUT	PM_SLP_S0_L	AM22	GPP_B12/SLP_S0*	SLP_LAN*	AK11	NC_PCH_SLP_LAN_L 20
111	NC_PCH_SLP_WLAN_L	AH10	GPD9/SLP_WLAN*	GPD2/LAN_WAKE*	AL9	SMC_WAKE_SCI_L — IN 12 46
20	NC_PCH_PME_L	AG16	GPP_A11/PME*	GPD11/LANPHYPC	AJ13	NC_PCH_LANPHYPC 20
59 12	AUD_PWR_EN	AG18	GPP_A12/BMBUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*	GPP_B2/VRALERT*	AH20	BT_LOW_PWR_L — OUT 12 35

NOSTUFF R1204 0 5% 1/20W MF 0201

R1205 100K 5% 1/20W MF 201

RTC / ESPI/LPC

20 IN	SYSCLK_CLK32K_PCH	AL8	RTCX1	GPP_A0/RCIN*/ESPI_ALERT1*	AM13	PCH_RCIN_L_PU 12
20 OUT	NC_PCH_CLK32K_RTCX2	AM8	RTCX2	GPP_A1/LAD0/ESPI_IO0	AK12	LPC_AD_R<0> R1440 33 — LPC_AD<0> BI 46 89
12	PCH_INTRUDER_L	AJ10	INTRUDER*	GPP_A2/LAD1/ESPI_IO1	AK13	LPC_AD_R<1> R1441 33 — LPC_AD<1> BI 46 89
12	PCH_SRTCRST_L	AJ8	SRTCRST*	GPP_A3/LAD2/ESPI_IO2	AG20	LPC_AD_R<2> R1442 33 — LPC_AD<2> BI 46 89
12	RTC_RESET_L	AH8	RTCRST*	GPP_A4/LAD3/ESPI_IO3	AM14	LPC_AD_R<3> R1443 33 — LPC_AD<3> BI 46 89
				GPP_A5/LFRAME*/ESPI_CS0*	AL14	LPC_FRAME_R_L R1444 33 — LPC_FRAME_L OUT 46 89
				GPP_A6/SERIRQ/ESPI_CS1*	AH14	LPC_SERIRQ — BI 12 46
				GPP_A7/PIRQA*/ESPI_ALERT0*	AJ18	SMC_RUNTIME_SCI_L — IN 12 46
				GPD7/RSVD	AL11	NC_PCH_GPD7 20

PLACE_NEAR=U1100.AL14:1.25mm

PP3V0_G3H 16 17 109

R1201 1M 5% 1/20W MF 201
R1202 20K 5% 1/20W MF 201
R1203 20K 5% 1/20W MF 201

PCH_SRTCRST_L 12
PCH_INTRUDER_L 12
RTC_RESET_L 12

C1202 1UF 10% 10V X5R 402-1
C1203 1UF 10% 10V X5R 402-1

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 2 OF 12

CLOCK SIGNALS

113 35 OUT	PCIE_CLK100M_AP_N	J5	CLKOUT_PCIE_N0	XTAL24_IN	B4	SYSCLK_CLK24M_PCH — IN 20
113 35 OUT	PCIE_CLK100M_AP_P	J6	CLKOUT_PCIE_P0	XTAL24_OUT	B3	NC_PCH_CLK24M_XTALOUT — OUT 20 113
111 OUT	NC_CLKOUT_PCIE_1_N	F2	CLKOUT_PCIE_N1			
111 OUT	NC_CLKOUT_PCIE_1_P	F1	CLKOUT_PCIE_P1			
111 OUT	NC_CLKOUT_PCIE_2_N	K6	CLKOUT_PCIE_N2			
111 OUT	NC_CLKOUT_PCIE_2_P	K5	CLKOUT_PCIE_P2			
27 OUT	PCIE_CLK100M_TBT_X_N	F3	CLKOUT_PCIE_N3			
27 OUT	PCIE_CLK100M_TBT_X_P	F4	CLKOUT_PCIE_P3			
101 OUT	PCIE_CLK100M_TBT_T_N	G2	CLKOUT_PCIE_N4			
101 OUT	PCIE_CLK100M_TBT_T_P	G3	CLKOUT_PCIE_P4			
113 87 OUT	PCIE_CLK100M_SSD_N	E2	CLKOUT_PCIE_N5			
113 87 OUT	PCIE_CLK100M_SSD_P	E1	CLKOUT_PCIE_P5			
111 OUT	NC_CLKOUT_PCIE_6_N	K2	CLKOUT_PCIE_N6			
111 OUT	NC_CLKOUT_PCIE_6_P	K3	CLKOUT_PCIE_P6			
111 OUT	EG_PEG_CLK100M_N	L1	CLKOUT_PCIE_N7			
111 OUT	EG_PEG_CLK100M_P	L2	CLKOUT_PCIE_P7			
111 OUT	NC_CLKOUT_PCIE_8_N	M3	CLKOUT_PCIE_N8			
111 OUT	NC_CLKOUT_PCIE_8_P	M4	CLKOUT_PCIE_P8			
111 OUT	NC_CLKOUT_PCIE_9_N	M2	CLKOUT_PCIE_N9			
111 OUT	NC_CLKOUT_PCIE_9_P	M1	CLKOUT_PCIE_P9			
111 OUT	NC_CLKOUT_PCIE_10_N	R6	CLKOUT_PCIE_N10			
111 OUT	NC_CLKOUT_PCIE_10_P	R7	CLKOUT_PCIE_P10			
111 OUT	NC_CLKOUT_PCIE_11_N	T6	CLKOUT_PCIE_N11			
111 OUT	NC_CLKOUT_PCIE_11_P	T5	CLKOUT_PCIE_P11			
111 OUT	NC_CLKOUT_PCIE_12_N	N3	CLKOUT_PCIE_N12			
111 OUT	NC_CLKOUT_PCIE_12_P	N2	CLKOUT_PCIE_P12			
20 OUT	NC_CLKOUT_PCIE_13_N	P5	CLKOUT_PCIE_N13			
20 OUT	NC_CLKOUT_PCIE_13_P	P6	CLKOUT_PCIE_P13			
111 OUT	NC_CLKOUT_PCIE_14_N	N5	CLKOUT_PCIE_N14			
111 OUT	NC_CLKOUT_PCIE_14_P	N6	CLKOUT_PCIE_P14			
111 OUT	NC_CLKOUT_PCIE_15_N	M6	CLKOUT_PCIE_N15			
111 OUT	NC_CLKOUT_PCIE_15_P	M7	CLKOUT_PCIE_P15			

XCLK_BIASREF E4 — PCH_DIFFCLK_BIASREF — R1234 2.7K 1% 1/20W MF 201 — PP1V0_SUS 110
PLACE_NEAR=U1100.E4:1.25mm

GPP_A9/CLKOUT_LPC0 /ESPI_CLK AJ14 — LPC_CLK24M_SMC_R — 22 — LPC_CLK24M_SMC BI 46
PLACE_NEAR=U1100.AJ14:1.4mm

GPP_A10/CLKOUT_LPC1 AH15 — LPC_CLK24M_DPMUX_UC_R 20

GPP_A16/CLKOUT_48 AL16 — CAMERA_PWR_EN 12

CLKOUT_ITPXDP_N	L6	NC_ITPXDP_CLK100MN	OUT	18 113 115
CLKOUT_ITPXDP_P	L5	NC_ITPXDP_CLK100MP	OUT	18 113 115
CLKOUT_CPUBCLK_N	J3	CPU_CLK100M_BCLK_N	OUT	6 113
CLKOUT_CPUBCLK_P	J4	CPU_CLK100M_BCLK_P	OUT	6 113
CLKOUT_CPUNSSC_N	H1	CPU_CLK24M_NSSC_CLK_N	OUT	6 113
CLKOUT_CPUNSSC_P	H2	CPU_CLK24M_NSSC_CLK_P	OUT	6 113
CLKOUT_CPUPCIBCLK_N	J1	CPU_CLK100M_PCIBCLK_N	OUT	6 113
CLKOUT_CPUPCIBCLK_P	J2	CPU_CLK100M_PCIBCLK_P	OUT	6 113

PCI EXPRESS CLOCKS & CONTROL

GPP_B5/SRCCLKREQ0*	AL20	AP_CLKREQ_L_R	BI	20
GPP_B6/SRCCLKREQ1*	AM19	ENETSD_CLKREQ_L	IN	20
GPP_B7/SRCCLKREQ2*	AK20	CAMERA_CLKREQ_L	IN	20
GPP_B8/SRCCLKREQ3*	AL19	TBT_X_CLKREQ_L_R	IN	20
GPP_B9/SRCCLKREQ4*	AH22	TBT_T_CLKREQ_L_R	IN	20
GPP_B10/SRCCLKREQ5*	AK22	SSD_CLKREQ_L_R	BI	20
GPP_H0/SRCCLKREQ6*	AM25	TBT_W_CLKREQ_L	IN	20
GPP_H1/SRCCLKREQ7*	AH26	EG_CLKREQ_OUT_L		111
GPP_H2/SRCCLKREQ8*	AL25	AP_S0IX_WAKE_SEL	OUT	12 19
GPP_H3/SRCCLKREQ9*	AF26	AP_S0IX_WAKE_L	IN	12 19
GPP_H4/SRCCLKREQ10*	AK26	TBT_X_CIO_PWR_EN	OUT	29
GPP_H5/SRCCLKREQ11*	AL26	TBT_T_CIO_PWR_EN	OUT	103
GPP_H6/SRCCLKREQ12*	AJ27	TBT_W_CIO_PWR_EN	OUT	20
GPP_H7/SRCCLKREQ13*	AH27	TBT_X_USB_PWR_EN	OUT	29
GPP_H8/SRCCLKREQ14*	AM26	TBT_T_USB_PWR_EN	OUT	103
GPP_H9/SRCCLKREQ15*	AK27	TBT_W_USB_PWR_EN	OUT	20

PP3V3_S0 14 20 73 110

R1238 47K 5% 1/20W MF 201
R1239 47K 5% 1/20W MF 201
R1240 47K 5% 1/20W MF 201
R1241 100K 5% 1/20W MF 201
R1242 100K 5% 1/20W MF 201
R1243 100K 5% 1/20W MF 201
R1244 100K 5% 1/20W MF 201
R1245 100K 5% 1/20W MF 201
R1246 100K 5% 1/20W MF 201

BOM_COST_GROUP=CPU & CHIPSET

PP3V3_S4 110
SSD_SR_EN_L 12 — R1211 100K 5% 1/20W MF 201

PP3V3_SUS 110 17 16 14
PM_SYSRST_L 115 46 18 12 — R1247 3.0K 5% 1/20W MF 201

PP3V3_SUS 110 17 16 15
PP3V3_S5 110 17 16

PCIE_WAKE_L 19 12	R1248	100K	5% 1/20W MF 201
SMC_WAKE_SCI_L 46 12	R1209	100K	5% 1/20W MF 201
PM_PWRBTN_L 48 12	R1210	1K	5% 1/20W MF 201
PM_BATLOW_L 103 46 29 12	R1212	10K	5% 1/20W MF 201
SMC_RUNTIME_SCI_L 46 12	R1207	100K	5% 1/20W MF 201
LPC_CLKRUN_L 46 12	R1208	10K	5% 1/20W MF 201
PCH_RCIN_L_PU 12	R1251	100K	5% 1/20W MF 201

PP3V3_S0 110 15 13 12

LPC_SERIRQ 46 12	R1206	10K	5% 1/20W MF 201
AUD_PWR_EN 59 12	R1214	100K	5% 1/20W MF 201
CAMERA_PWR_EN 12	R1215	100K	5% 1/20W MF 201
AP_S0IX_WAKE_L 19 12	R1216	100K	5% 1/20W MF 201
PM_SLP_S5_L 73 46 20 12	R1230	100K	5% 1/20W MF 201
PM_SLP_S4_L 73 70 46 43 20 12	R1231	100K	5% 1/20W MF 201
PM_SLP_S3_L 114 101 89 76 73 70 46 27 20 12	R1232	100K	5% 1/20W MF 201
PM_SLP_S0_L 70 46 20 12	R1233	100K	5% 1/20W MF 201
AP_S0IX_WAKE_SEL 19 12	R1236	100K	5% 1/20W MF 201
PM_SLP_SUS_L 73 70 12	R1237	100K	5% 1/20W MF 201

BT_LOW_PWR_L 35 12 — R1213 10K 5% 1/20W MF 201 — PP3V3_S0 110 15 13 12

PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK

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BRANCH dvt-fab10
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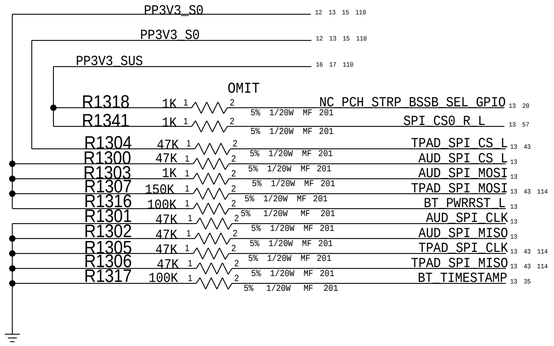

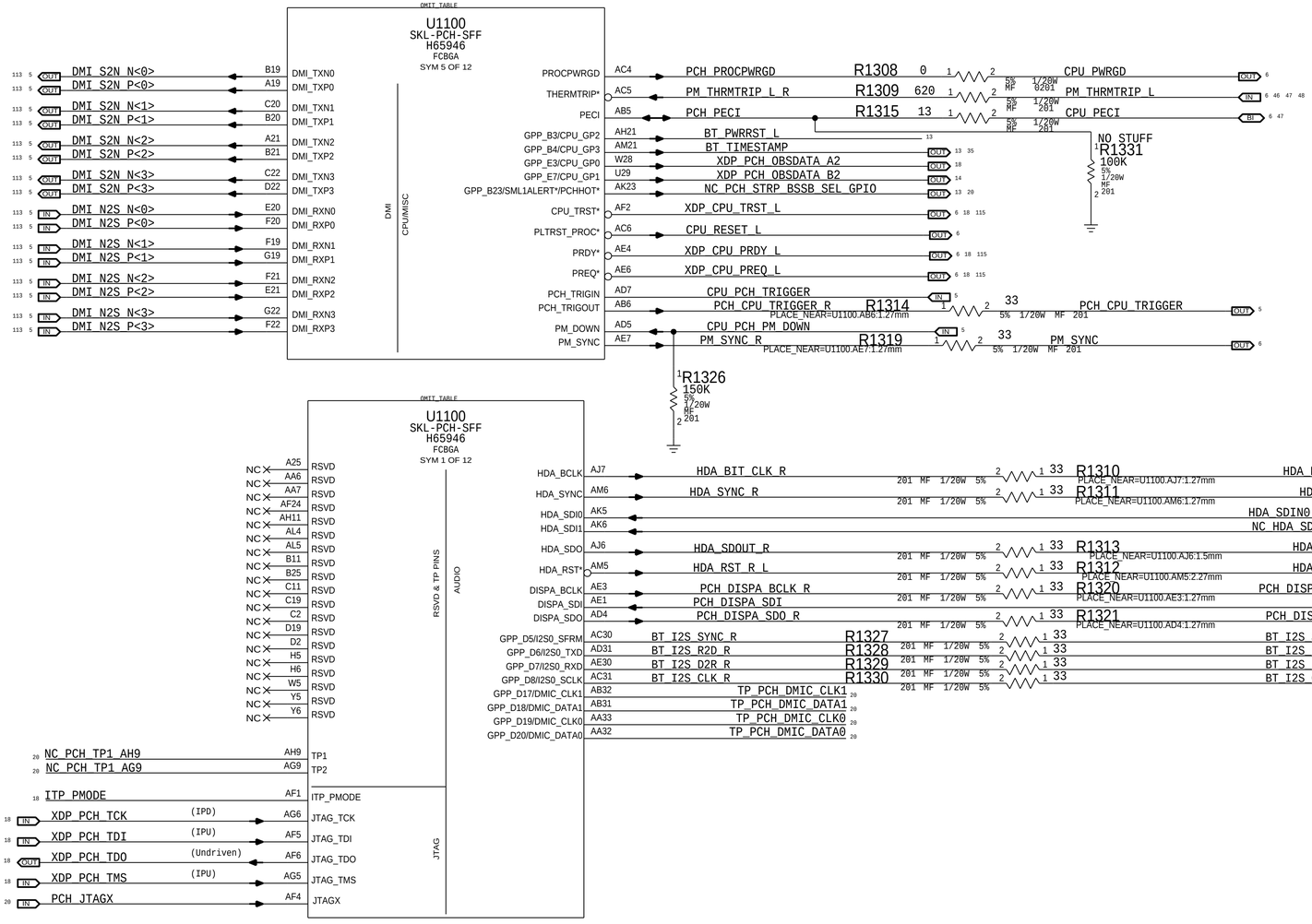

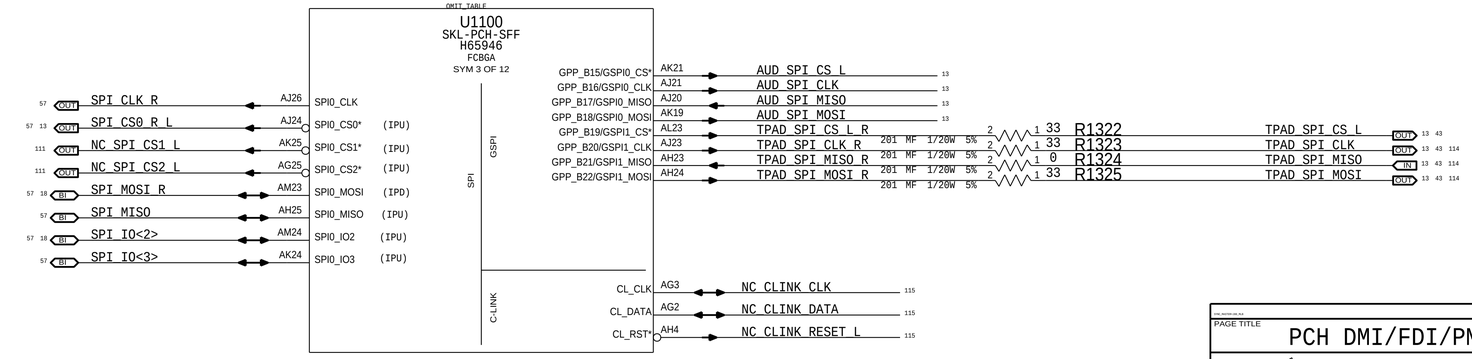

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

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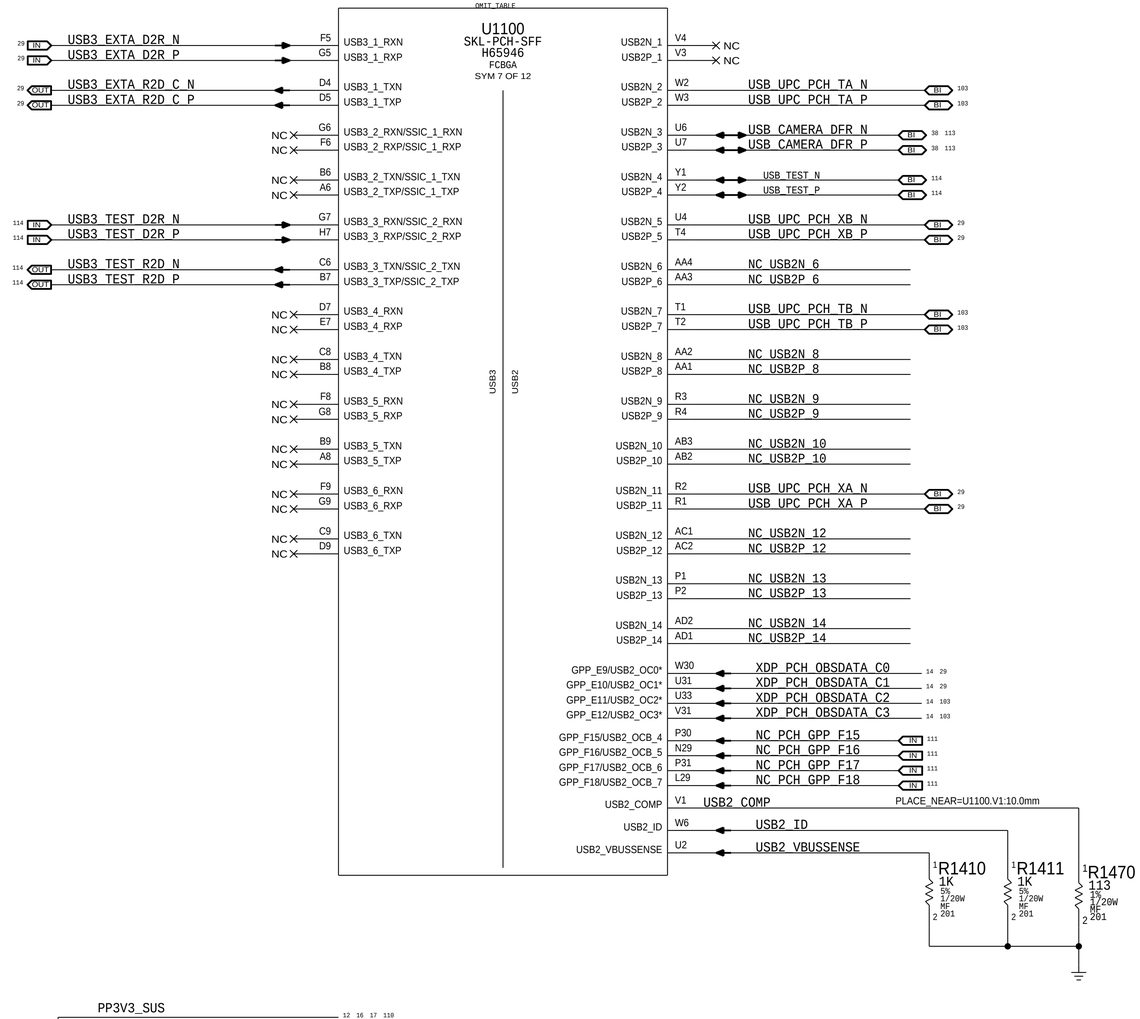

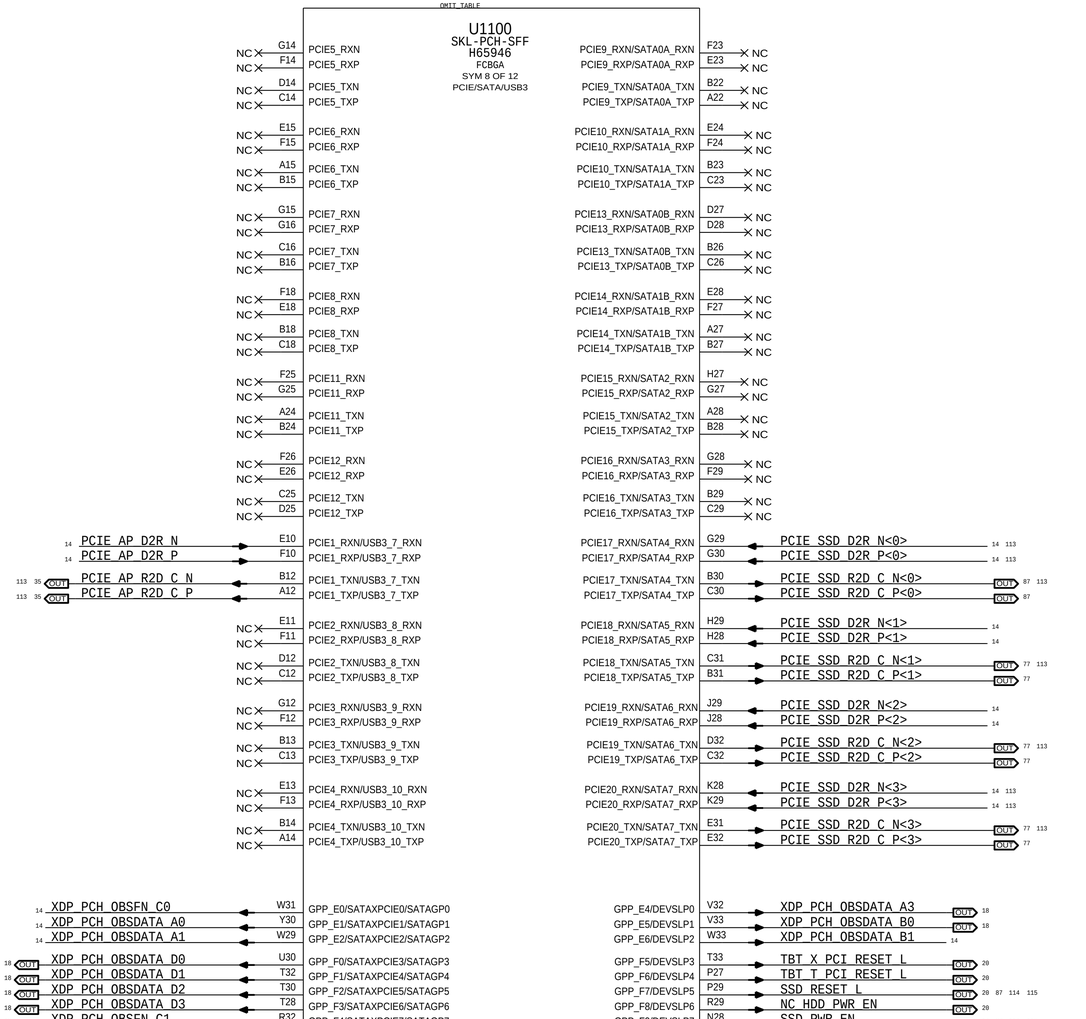

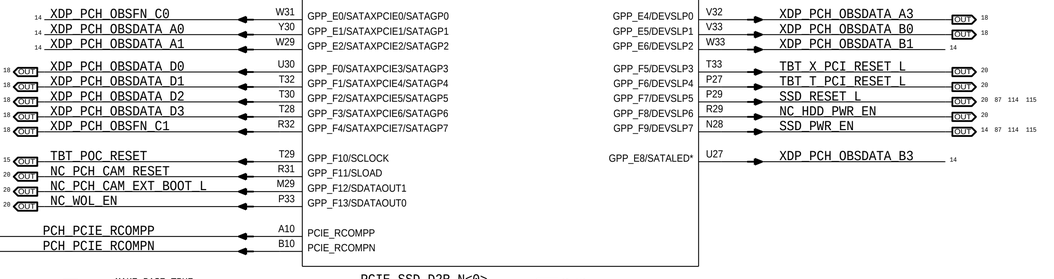

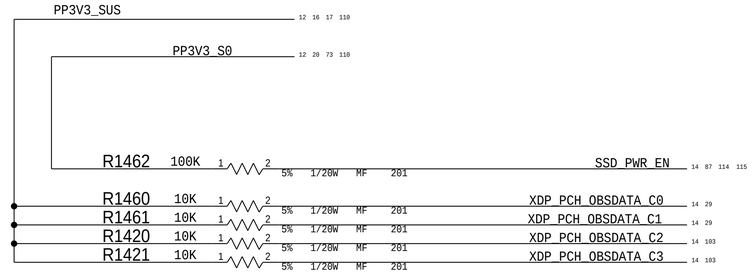

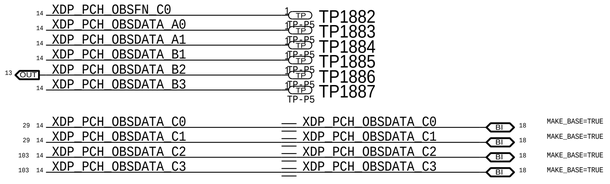

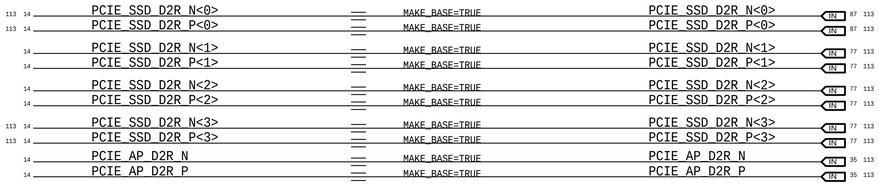

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER 051-00647
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BRANCH dvt-fab10
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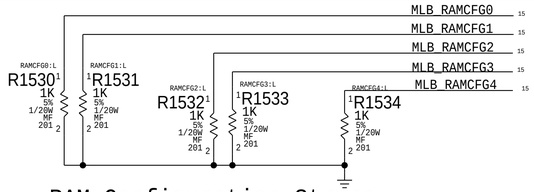
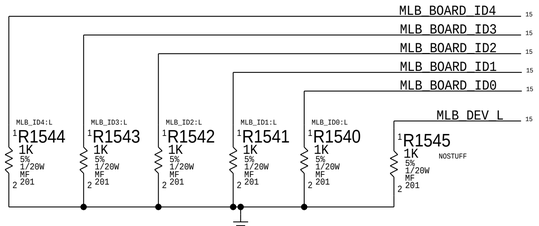


RAM Configuration Straps

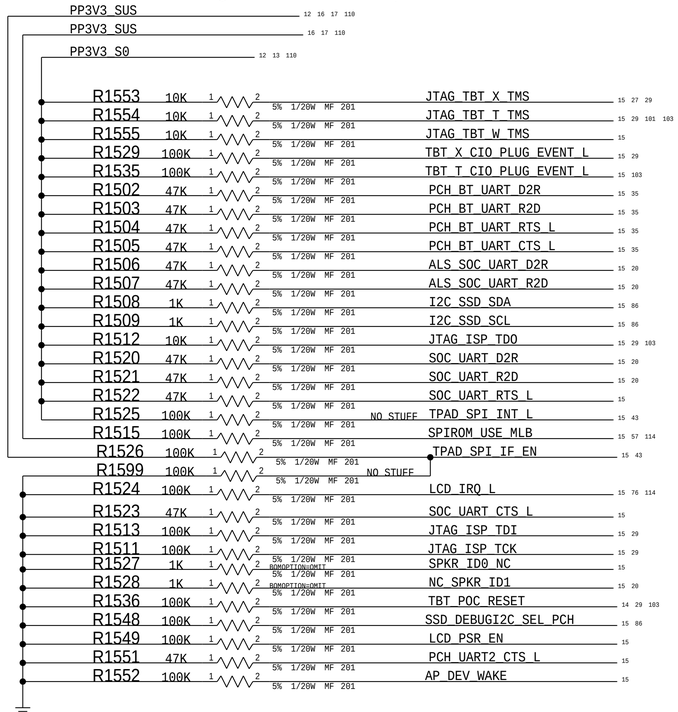
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L

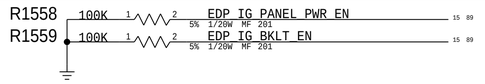
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	0	RES,MF,1/20W,1KOHM,5%,0201,SMD		BOARD_ID:1F
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1540	BOARD_ID:1E
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541	BOARD_ID:1D
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541,R1540	BOARD_ID:1C
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542	BOARD_ID:1B
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1540	BOARD_ID:1A
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541	BOARD_ID:19
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541,R1540	BOARD_ID:18
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543	BOARD_ID:17
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1540	BOARD_ID:16
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541	BOARD_ID:15
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541,R1540	BOARD_ID:14

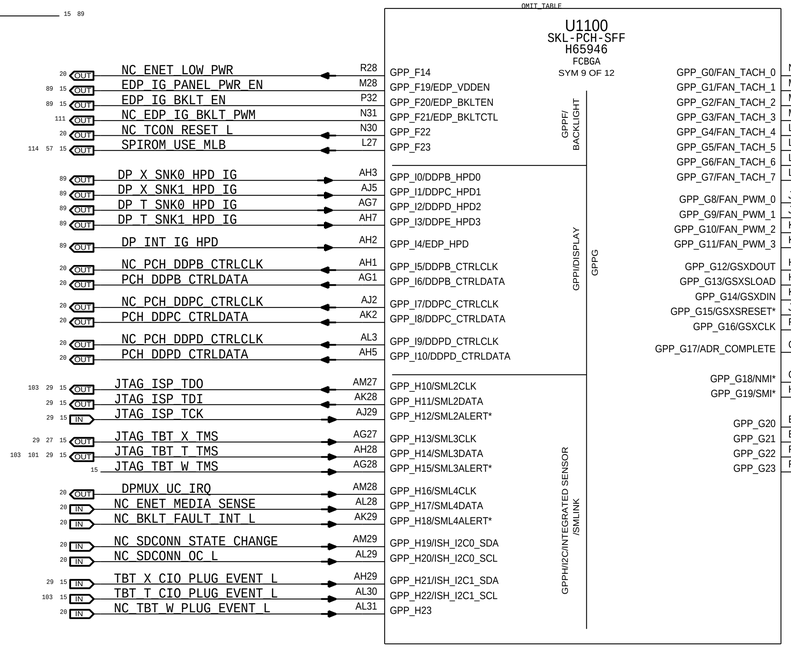
```
PROTO 0 = 0x1F = 1 1 1 1 1 (-01 PCB)
PROTO 0B = 0x1E = 1 1 1 1 0 (-02 PCB)
PROTO 1 = 0x1D = 1 1 1 0 1 (-03 PCB)
PROTO 2 = 0x1C = 1 1 1 0 0 (-04 & -05 PCB)
EVT1 = 0x1B = 1 1 0 1 1 (-06 PCB)
EVT2 = 0x1A = 1 1 0 1 0 (-07 PCB)
DVT = 0x19 = 1 1 0 0 1 (-08 PCB)
DVT1-1 = 0x18 = 1 1 0 0 0 (-09 PCB)
PVT = 0x17 = 1 0 1 1 1 (-10 PCB)
0x16 = 1 0 1 1 0
0x15 = 1 0 1 0 1
0x14 = 1 0 1 0 0
```

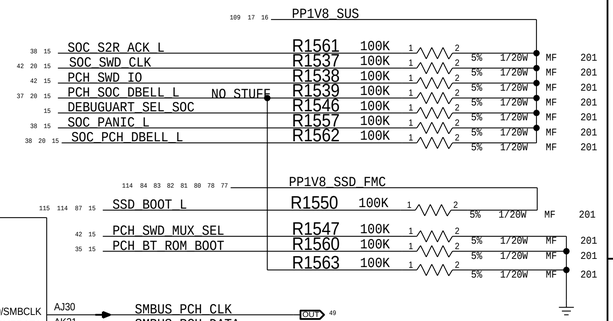


MLB BOARD ID Configuration Straps









BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
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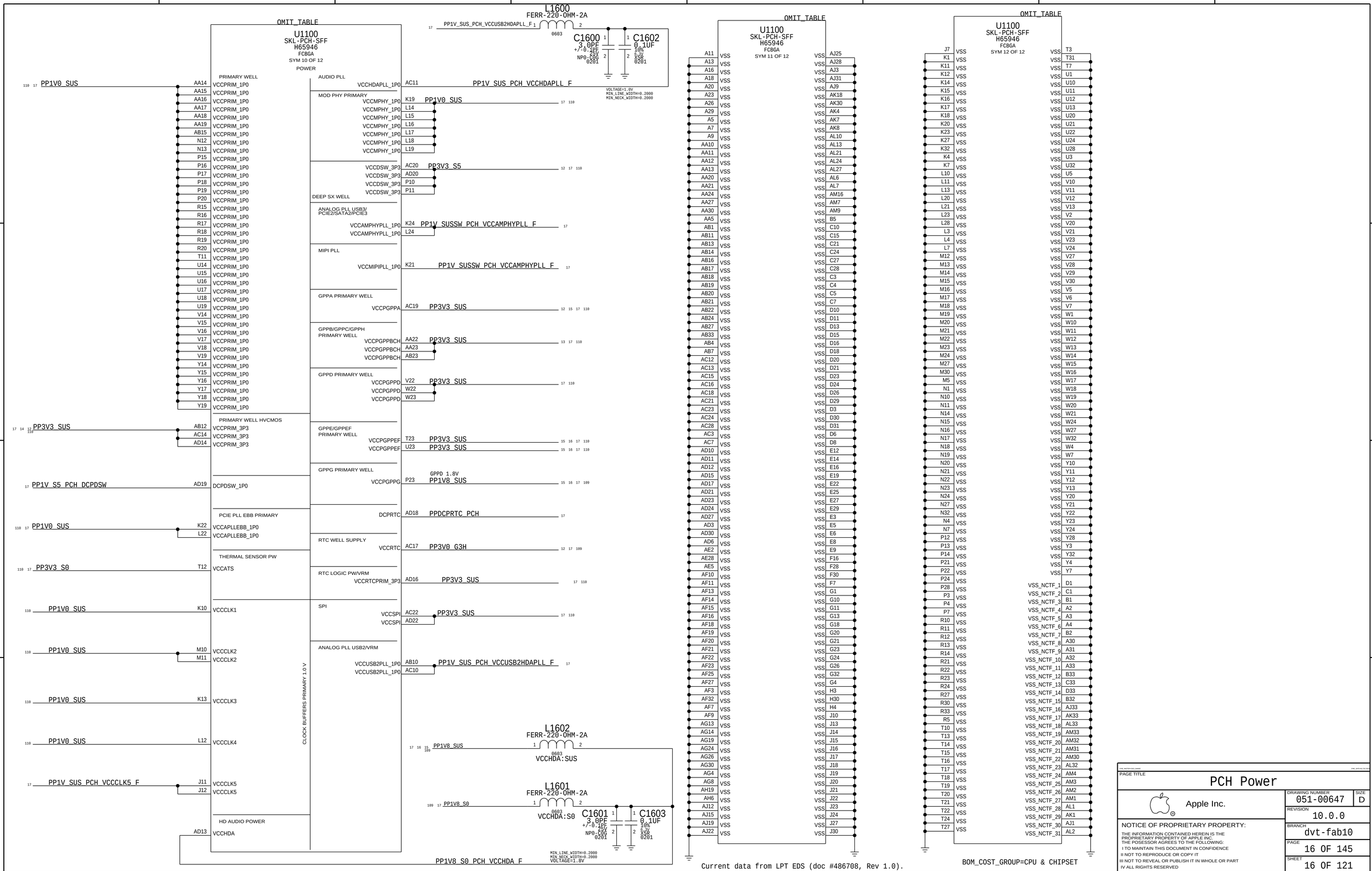
OMIT_TABLE
U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 10 OF 12
POWER
PRIMARY WELL
AUDIO PLL
MOD PHY PRIMARY
DEEP SX WELL
ANALOG PLL USB3/ PCIE2/SATA2/PCIE3
MIPI PLL
GPPA PRIMARY WELL
GPPB/GPPC/GPPH PRIMARY WELL
GPPD PRIMARY WELL
PRIMARY WELL HVCMOS
GPPE/GPPEF PRIMARY WELL
GPPG PRIMARY WELL
PCIE PLL EBB PRIMARY
RTC WELL SUPPLY
THERMAL SENSOR PW
RTC LOGIC PW/VRM
SPI
ANALOG PLL USB2/VRM
HD AUDIO POWER
CLOCK BUFFERS PRIMARY 1.0 V
PP1V0_SUS
PP3V3_SUS
PP1V_S5_PCH_DCPDSW
PP3V3_S0
PP1V_SUS_PCH_VCCCLK5_F
PP1V_SUS_PCH_VCCHDAPLL_F
PP1V0_SUS
PP1V_SUSSW_PCH_VCCAMPHYPLL_F
PP3V3_S5
PP3V3_SUS
PP1V8_SUS
PPDCPRTC_PCH
PP3V0_G3H
PP1V_SUS_PCH_VCCUSB2HDAPLL_F
PP1V8_S0_PCH_VCCHDA_F
L1600
FERR-220-OHM-2A
C1600
3.0PF
+/-0.1PF
25V
NP0-C0G
0201
C1602
0.1UF
10%
6.3V
X5R
0201
L1602
VCCHDA:SUS
L1601
VCCHDA:S0
C1601
C1603
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
OMIT_TABLE
U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 11 OF 12
OMIT_TABLE
U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 12 OF 12
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
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VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
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VSS_NCTF_21
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VSS_NCTF_29
VSS_NCTF_30
VSS_NCTF_31
Current data from LPT EDS (doc #486708, Rev 1.0).
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH Power
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
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10.0.0
BRANCH
dvt-fab10
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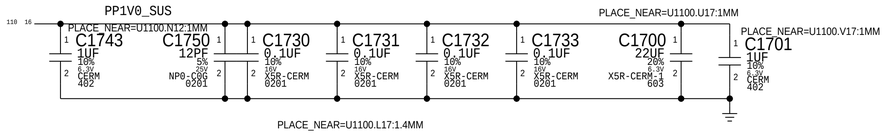
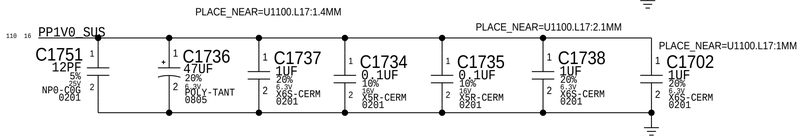
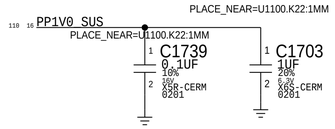
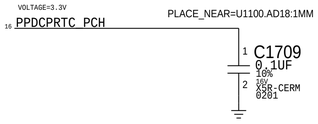
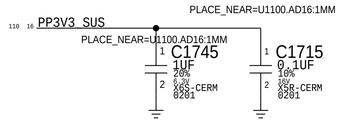
1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED

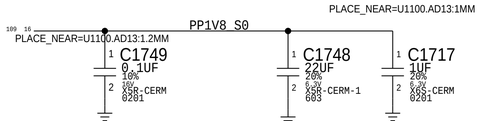


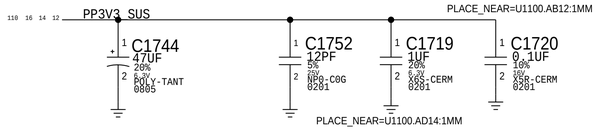


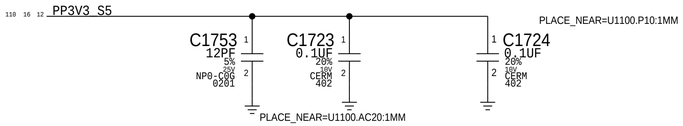


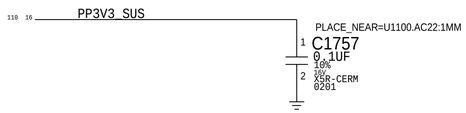


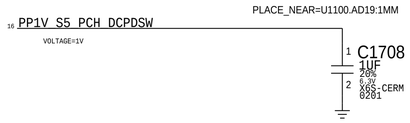


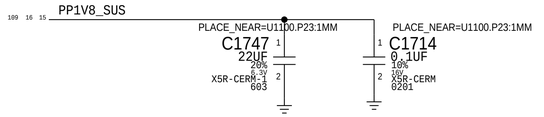


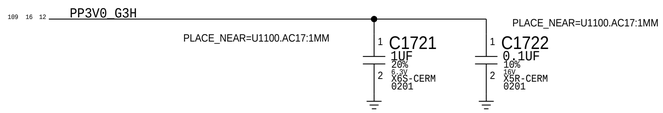


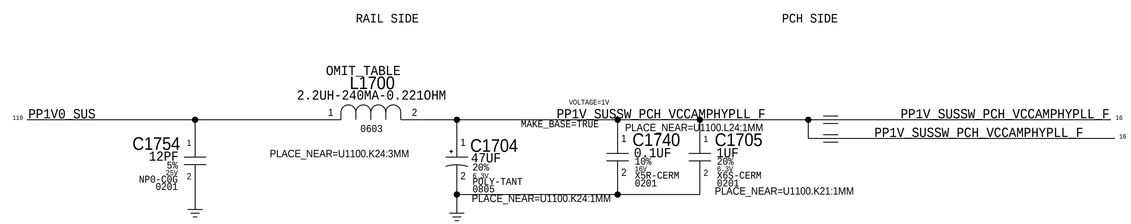


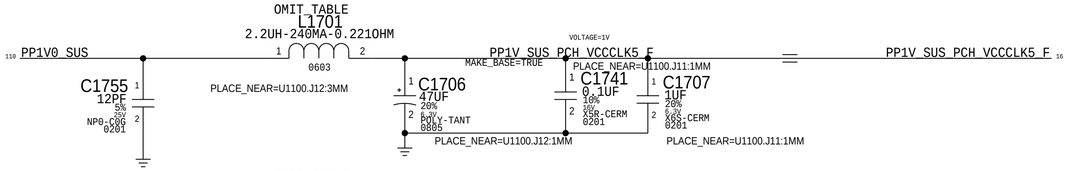


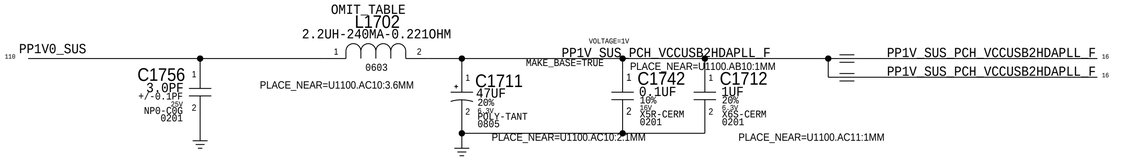












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	3	RES,MF,1A MAX,00HM,5%,0603	L1700,L1701,L1702		

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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Primary / Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<0> → TP1800
XDP_BPM_L<1> → TP1801
XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803

All: TP-P6

PULL CFG<3> LOW WHEN XDP PRESENT
PLACE_NEAR=U0500.BN28:2.54MM
XDP:YES R1801 1K 5% 1/20W MF 201
XDP_PRESENT_CPU → NO_XNET_CONNECTION

PP1V0_SUS

XDP_CONN J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CONN		
XDP_PIN_1		
OBSFN_A0	XDP_CPU_PREQ_L	
OBSFN_A1	XDP_CPU_PRDY_L	
OBSDATA_A0	CPU_CFG<0>	CPU_CFG<8>
OBSDATA_A1	CPU_CFG<1>	CPU_CFG<9>
OBSDATA_A2	CPU_CFG<2>	CPU_CFG<10>
OBSDATA_A3	CPU_CFG<3>	CPU_CFG<11>
OBSFN_B0	NC	CPU_CFG<19>
OBSFN_B1	NC	CPU_CFG<18>
OBSDATA_B0	CPU_CFG<4>	CPU_CFG<12>
OBSDATA_B1	CPU_CFG<5>	CPU_CFG<13>
OBSDATA_B2	CPU_CFG<6>	CPU_CFG<14>
OBSDATA_B3	CPU_CFG<7>	CPU_CFG<15>
HOOK0	XDP_PM_RSMRST_L	ITPCLK/HOOK4 — NC_ITPXDP_CLK100MP
HOOK1	XDP_CPU_PWRBTN_L	ITPCLK#/HOOK5 — NC_ITPXDP_CLK100MN
VCC_OBS_AB		VCC_OBS_CD
HOOK2	NC	RESET#/HOOK6 — ITP_PMODE
HOOK3	SPI_MOSI_R_CONN	DBR#/HOOK7 — XDP_DBRESET_L
SDA	NC	TDO
SCL	NC	TRSTn
TCK1	XDP_PCH_TCK	TDI
TCK0		TMS
		XDP_PRESENT#

518S0047

PP3V3_SUS
PLACE_NEAR=J1800.48:2.54MM
XDP:YES R1804 1K 5% 1/20W MF 201

PM_RSMRST_L → R1800 1K XDP:YES PLACE_NEAR=U1100.AF12:3.8MM
PM_PWRBTN_L → R1802 10 XDP:YES PLACE_NEAR=U1100.AM10:3MM
SPI_MOSI_R → R1803 1K XDP:YES PLACE_NEAR=U1100.AM23:2.54MM
XDP_CPU_TCK → PCH_JTAGX R1835 0 XDP:YES PLACE_NEAR=J1800.58:28MM

C1804 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.42:28MM
C1800 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.44:28MM
C1801 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.43:28MM
C1806 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.47:28MM

PP1V0_S0SW

XDP_PCH_TDO	R1890	51	XDP:YES PLACE_NEAR=U1100.AF6:28MM
XDP_PCH_TDI	R1891	51	XDP:YES PLACE_NEAR=U1100.AF5:28MM
XDP_PCH_TMS	R1892	51	XDP:YES PLACE_NEAR=U1100.AG5:28MM
XDP_CPU_TDO	R1810	51	XDP:YES PLACE_NEAR=U0500.BT28:28MM
XDP_CPU_TCK	R1813	51	XDP:YES PLACE_NEAR=U0500.BR28:28MM
XDP_PCH_TCK	R1897	51	NOSTUFF PLACE_NEAR=U1100.AG6:28MM
XDP_PCH_TRST_L	R1898	51	NOSTUFF PROPER WAY TO TERMINATE?

All: 5% 1/20W MF 201

R1830 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.EB:2.54MM

XDP:YES R1806 0 5% 1/20W MF 0201 — PM_SYSRST_L

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

R1821	0	XDP_CPU_TDO	PLACE_NEAR=J1800.51:2.54MM
R1822	0	XDP_CPU_TRST_L	PLACE_NEAR=J1800.53:2.54MM
R1823	0	XDP_CPU_TDI	PLACE_NEAR=J1800.55:2.54MM
R1824	0	XDP_CPU_TMS	PLACE_NEAR=J1800.57:2.54MM

All: XDP:YES 5% 1/20W MF 0201

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PP3V3_SUS
XDP:YES C1830 0.1UF 10% 10V X5R-CERM 0201
XDP:YES U1830 74AUP1G07GF SOT891 (VCC, GND, A, Y, (OD), NC)
PLACE_NEAR=U1830.4:7.54MM R1831 1.5K MF XDP:YES NO_XNET_CONNECTION — SPI_IO2_STRAP_L → SPI_IO<2> (STRAP TO PCH)
PLACE_NEAR=U1830.4:2.54MM R1832 49.9 MF NOSTUFF 1% 1/20W 201 NO_XNET_CONNECTION
XDP_PRESENT_L

PP3V3_SUS → XDP:YES R1850 100K 5% 1/20W MF 201

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals	Non-XDP Signals
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_C0	TP1873
XDP_PCH_OBSDATA_C1	TP1874
XDP_PCH_OBSDATA_C2	TP1875
XDP_PCH_OBSDATA_C3	TP1876
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C1	TP1881

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: 051-00647
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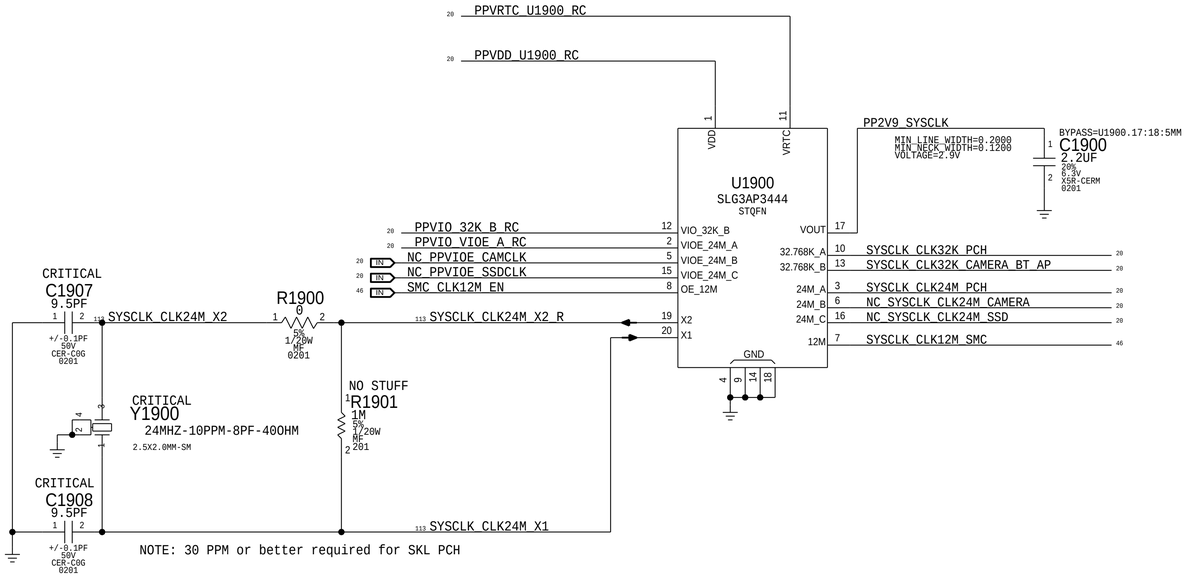
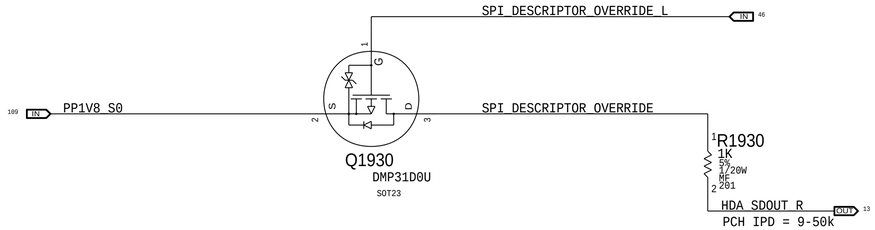
System 32kHz / 12MHz / 24MHz Clock Generator

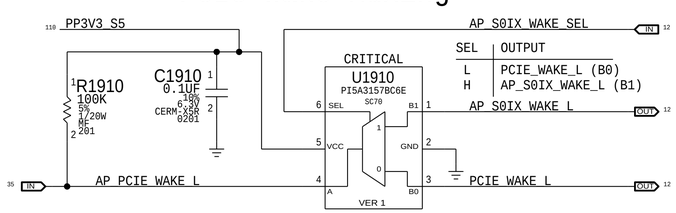


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing

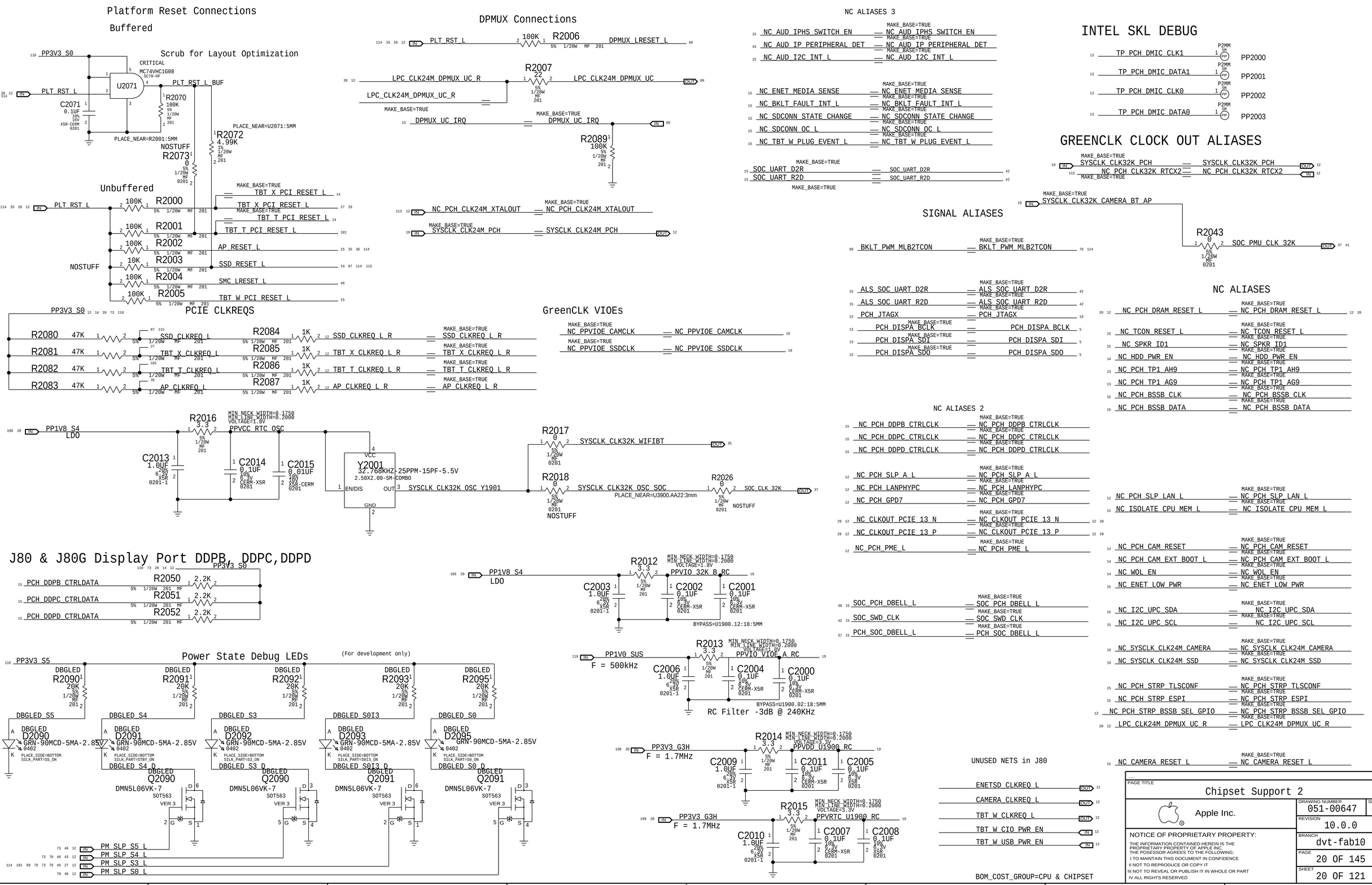


BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 1

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 19 OF 145
SHEET: 19 OF 121


Platform Reset Connections
Buffered
PP3V3_S0
Scrub for Layout Optimization
CRITICAL
U2071
MC74VHC1G08
SC70-HF
PLT_RST_L
PLT_RST_L_BUF
C2071
0.1UF
R2070
100K
PLACE_NEAR=R2001:5MM
PLACE_NEAR=U2071:5MM
R2072
4.99K
NOSTUFF
R2073
0
Unbuffered
R2000
R2001
R2002
R2003
R2004
R2005
TBT_X_PCI_RESET_L
TBT_T_PCI_RESET_L
AP_RESET_L
SSD_RESET_L
SMC_LRESET_L
TBT_W_PCI_RESET_L
DPMUX Connections
R2006
DPMUX_LRESET_L
R2007
22
LPC_CLK24M_DPMUX_UC_R
LPC_CLK24M_DPMUX_UC
R2089
DPMUX_UC_IRQ
NC_PCH_CLK24M_XTALOUT
SYSCLK_CLK24M_PCH
NC ALIASES 3
NC_AUD_IPHS_SWITCH_EN
NC_AUD_IP_PERIPHERAL_DET
NC_AUD_I2C_INT_L
NC_ENET_MEDIA_SENSE
NC_BKLT_FAULT_INT_L
NC_SDCONN_STATE_CHANGE
NC_SDCONN_OC_L
NC_TBT_W_PLUG_EVENT_L
SOC_UART_D2R
SOC_UART_R2D
INTEL SKL DEBUG
TP_PCH_DMIC_CLK1
TP_PCH_DMIC_DATA1
TP_PCH_DMIC_CLK0
TP_PCH_DMIC_DATA0
PP2000
PP2001
PP2002
PP2003
GREENCLK CLOCK OUT ALIASES
SYSCLK_CLK32K_PCH
NC_PCH_CLK32K_RTCX2
SIGNAL ALIASES
SYSCLK_CLK32K_CAMERA_BT_AP
R2043
SOC_PMU_CLK_32K
BKLT_PWM_MLB2TCON
ALS_SOC_UART_D2R
ALS_SOC_UART_R2D
PCH_JTAGX
PCH_DISPA_BCLK
PCH_DISPA_SDI
PCH_DISPA_SDO
NC ALIASES
NC_PCH_DRAM_RESET_L
NC_TCON_RESET_L
NC_SPKR_ID1
NC_HDD_PWR_EN
NC_PCH_TP1_AH9
NC_PCH_TP1_AG9
NC_PCH_BSSB_CLK
NC_PCH_BSSB_DATA
PCIE CLKREQS
PP3V3_S0
R2080
R2081
R2082
R2083
SSD_CLKREQ_L
TBT_X_CLKREQ_L
TBT_T_CLKREQ_L
AP_CLKREQ_L
R2084
R2085
R2086
R2087
SSD_CLKREQ_L_R
TBT_X_CLKREQ_L_R
TBT_T_CLKREQ_L_R
AP_CLKREQ_L_R
GreenCLK VIOEs
NC_PPVIOE_CAMCLK
NC_PPVIOE_SSDCLK
NC ALIASES 2
NC_PCH_DDPB_CTRLCLK
NC_PCH_DDPC_CTRLCLK
NC_PCH_DDPD_CTRLCLK
NC_PCH_SLP_A_L
NC_PCH_LANPHYPC
NC_PCH_GPD7
NC_CLKOUT_PCIE_13_N
NC_CLKOUT_PCIE_13_P
NC_PCH_PME_L
NC_PCH_SLP_LAN_L
NC_ISOLATE_CPU_MEM_L
NC_PCH_CAM_RESET
NC_PCH_CAM_EXT_BOOT_L
NC_WOL_EN
NC_ENET_LOW_PWR
NC_I2C_UPC_SDA
NC_I2C_UPC_SCL
NC_SYSCLK_CLK24M_CAMERA
NC_SYSCLK_CLK24M_SSD
NC_PCH_STRP_TLSCONF
NC_PCH_STRP_ESPI
NC_PCH_STRP_BSSB_SEL_GPIO
LPC_CLK24M_DPMUX_UC_R
NC_CAMERA_RESET_L
R2016
3.3
PPVCC_RTC_OSC
C2013
1.0UF
C2014
0.1UF
C2015
0.01UF
Y2001
32.768KHZ-25PPM-15PF-5.5V
2.50X2.00-SM-COMBO
SYSCLK_CLK32K_OSC_Y1901
R2017
SYSCLK_CLK32K_WIFIBT
R2018
SYSCLK_CLK32K_OSC_SOC
R2026
SOC_CLK_32K
NOSTUFF
J80 & J80G Display Port DDPB, DDPC,DDPD
PCH_DDPB_CTRLDATA
PCH_DDPC_CTRLDATA
PCH_DDPD_CTRLDATA
R2050
R2051
R2052
2.2K
Power State Debug LEDs
(For development only)
PP3V3_S5
DBGLED
D2090
D2091
D2092
D2093
D2095
GRN-90MCD-5MA-2.85V
DBGLED_S5
DBGLED_S4
DBGLED_S3
DBGLED_S0I3
DBGLED_S0
DBGLED_S4_D
DBGLED_S3_D
DBGLED_S0I3_D
DBGLED_S0_D
Q2090
Q2091
DMN5L06VK-7
SOT563
VER 3
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_S0_L
R2012
PPVIO_32K_B_RC
BYPASS=U1900.12:18:5MM
R2013
PPVIO_VIOE_A_RC
PP1V0_SUS
F = 500kHz
RC Filter -3dB @ 240KHz
R2014
PPVDD_U1900_RC
PP3V3_G3H
F = 1.7MHz
R2015
PPVRTC_U1900_RC
UNUSED NETS in J80
ENETSD_CLKREQ_L
CAMERA_CLKREQ_L
TBT_W_CLKREQ_L
TBT_W_CIO_PWR_EN
TBT_W_USB_PWR_EN
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
Chipset Support 2
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
PAGE
20 OF 145
SHEET
20 OF 121
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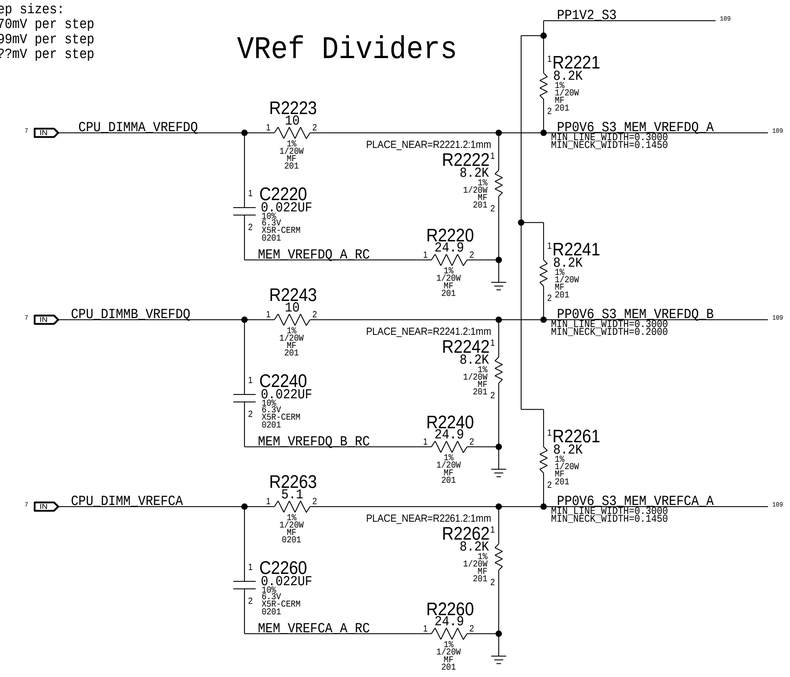
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



BOM_COST_GROUP=DRAM

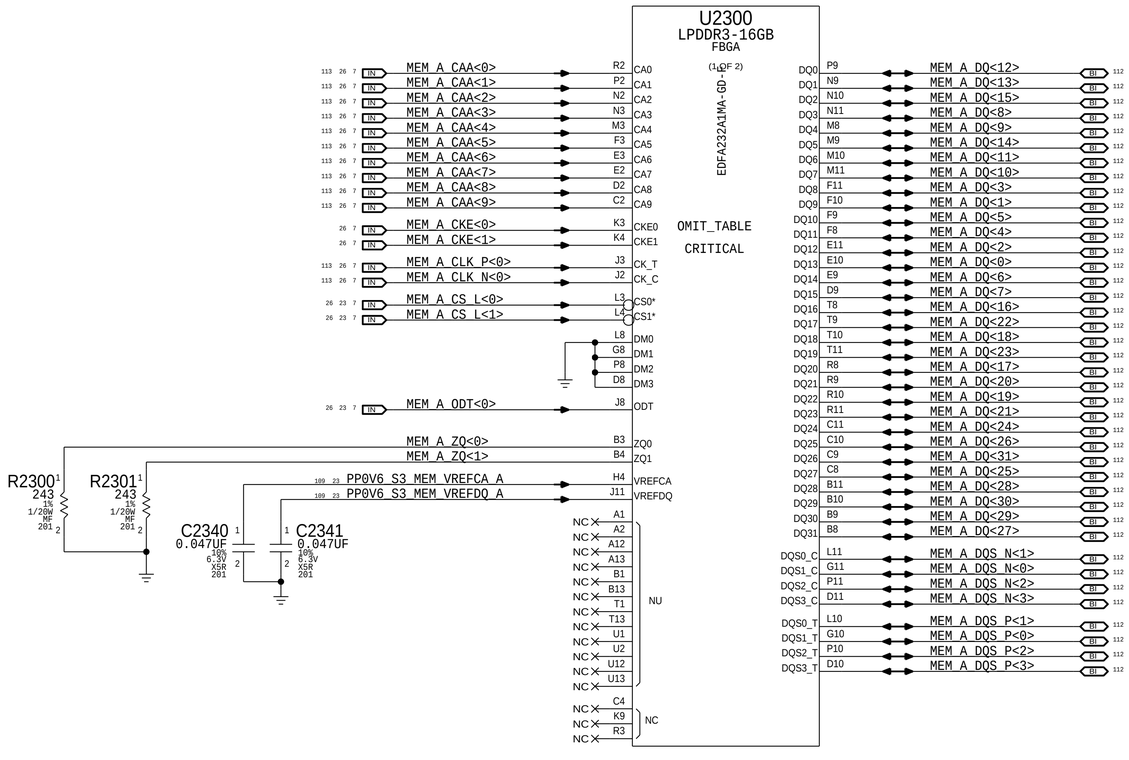
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

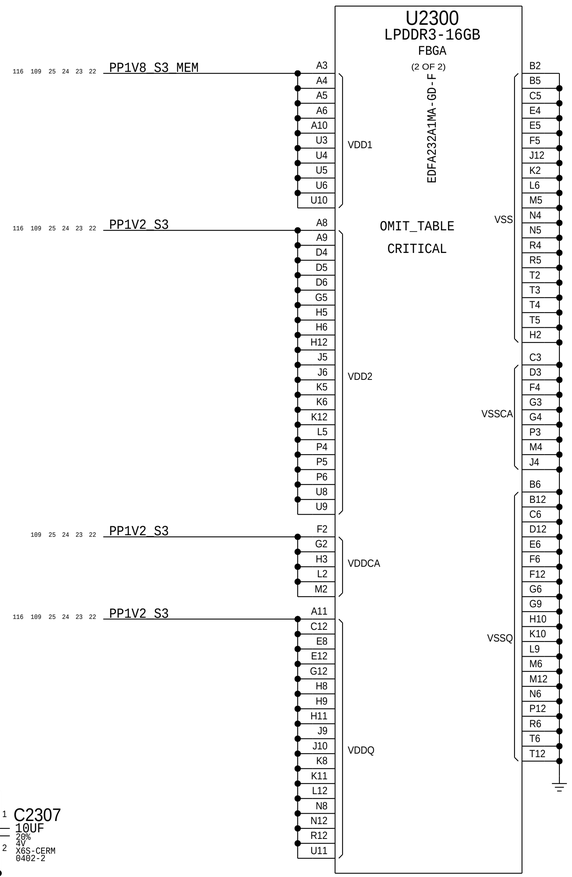
PAGE TITLE
LPDDR3 VREF MARGINING

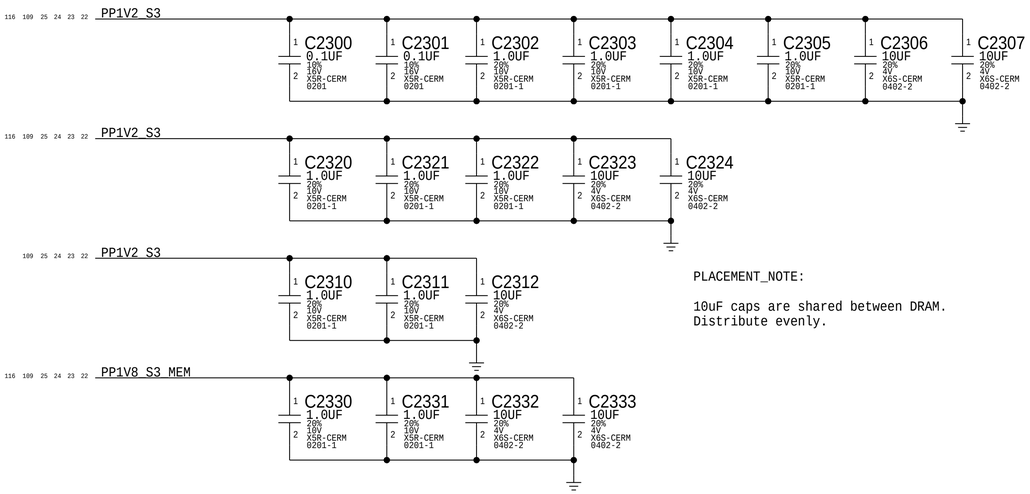
Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 22 OF 145
SHEET 21 OF 121

LPDDR3 CHANNEL A (0-31)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 23 OF 145
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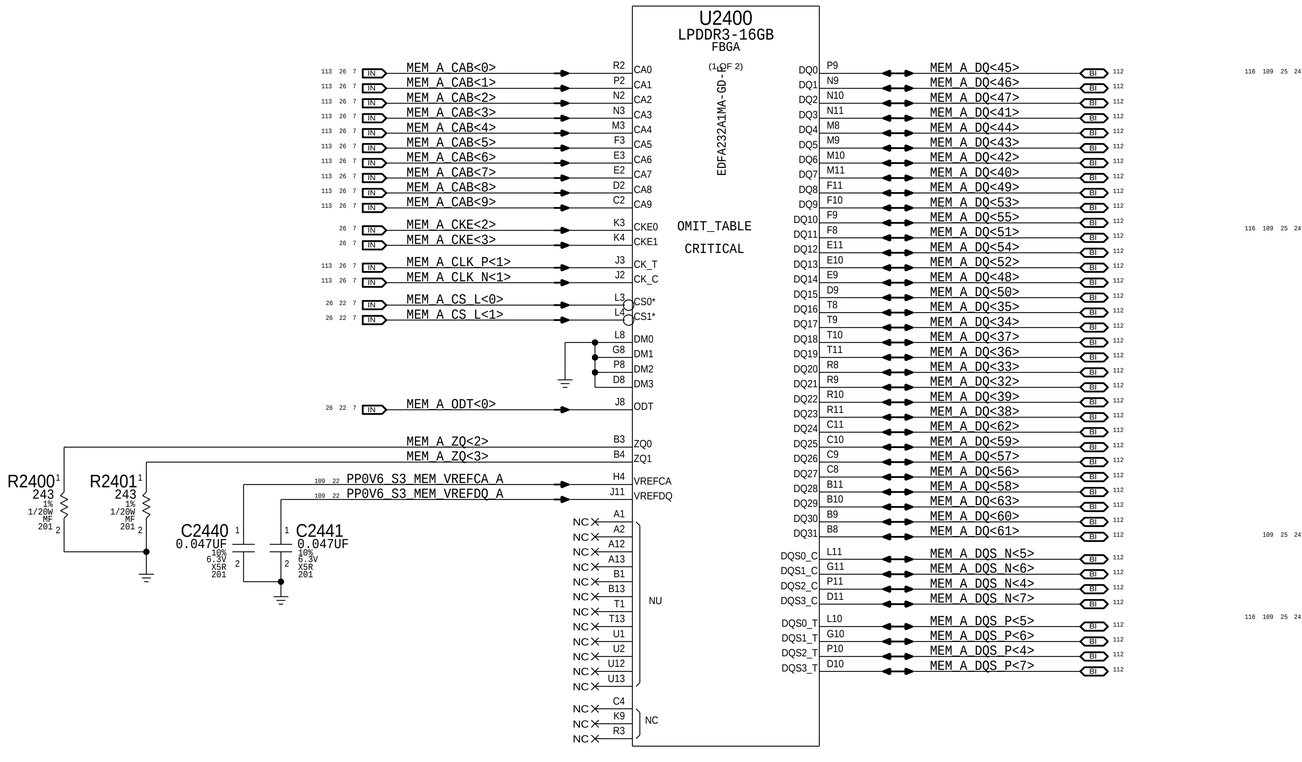
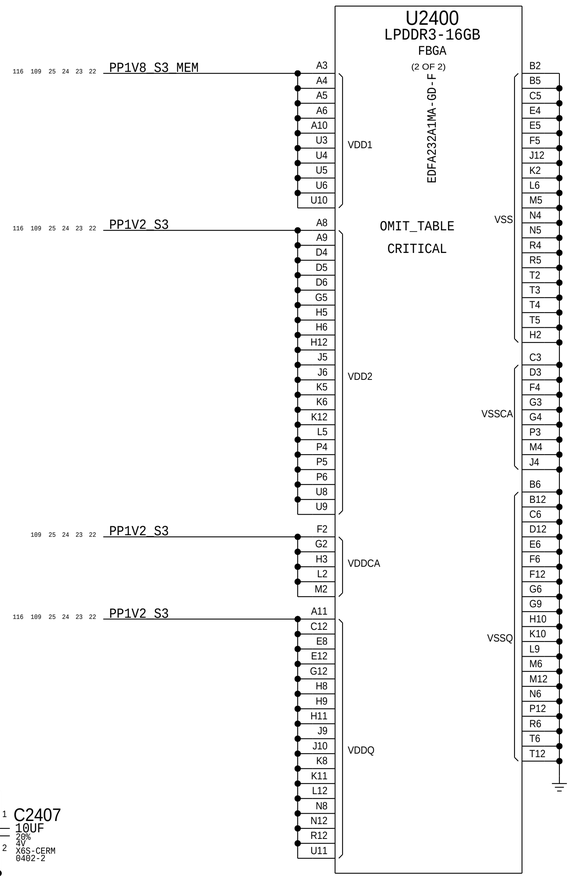
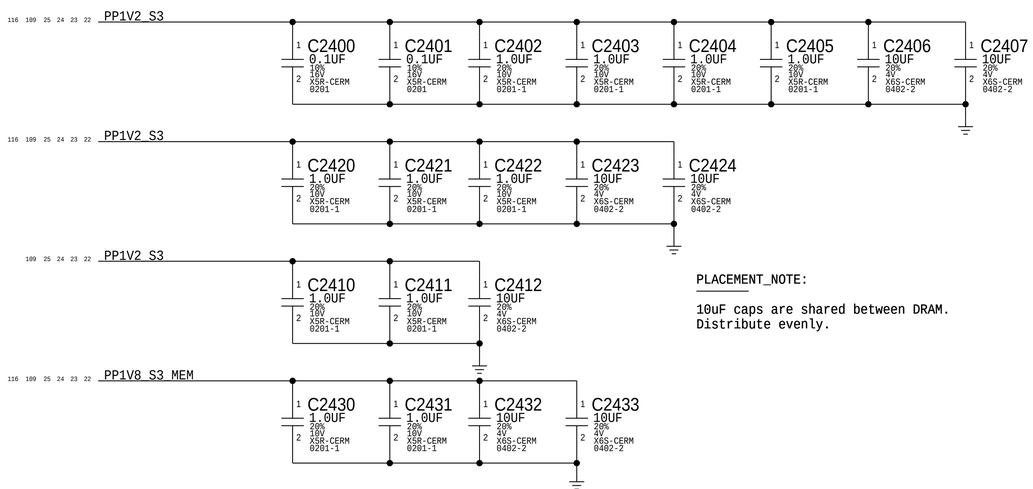
LPDDR3 CHANNEL A (32-63)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

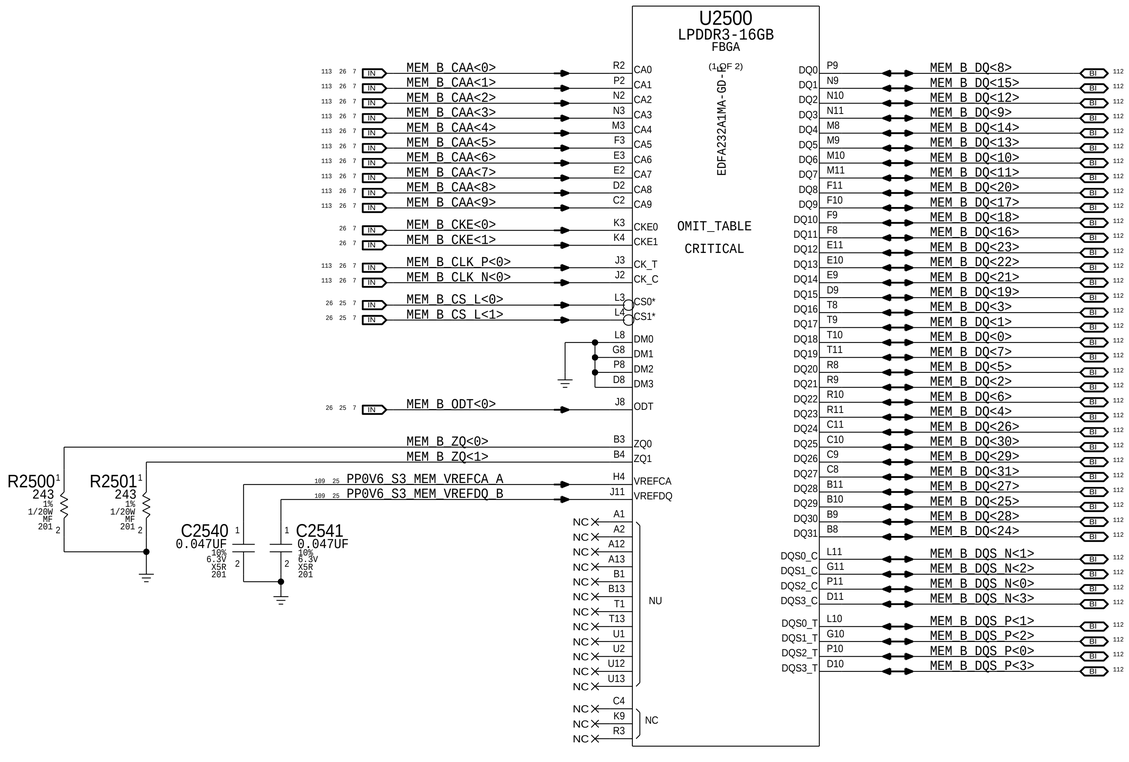
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

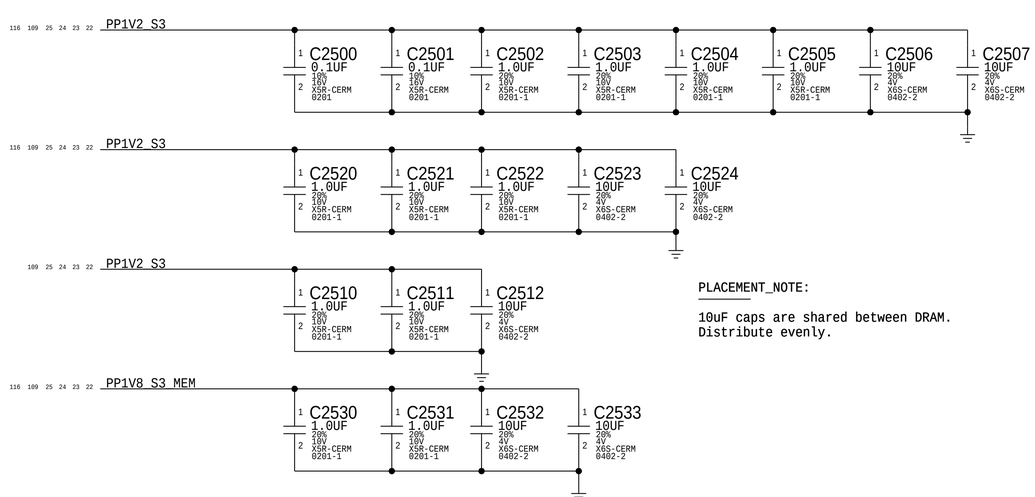
PAGE TITLE: LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 24 OF 145
SHEET: 23 OF 121

LPDDR3 CHANNEL B (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

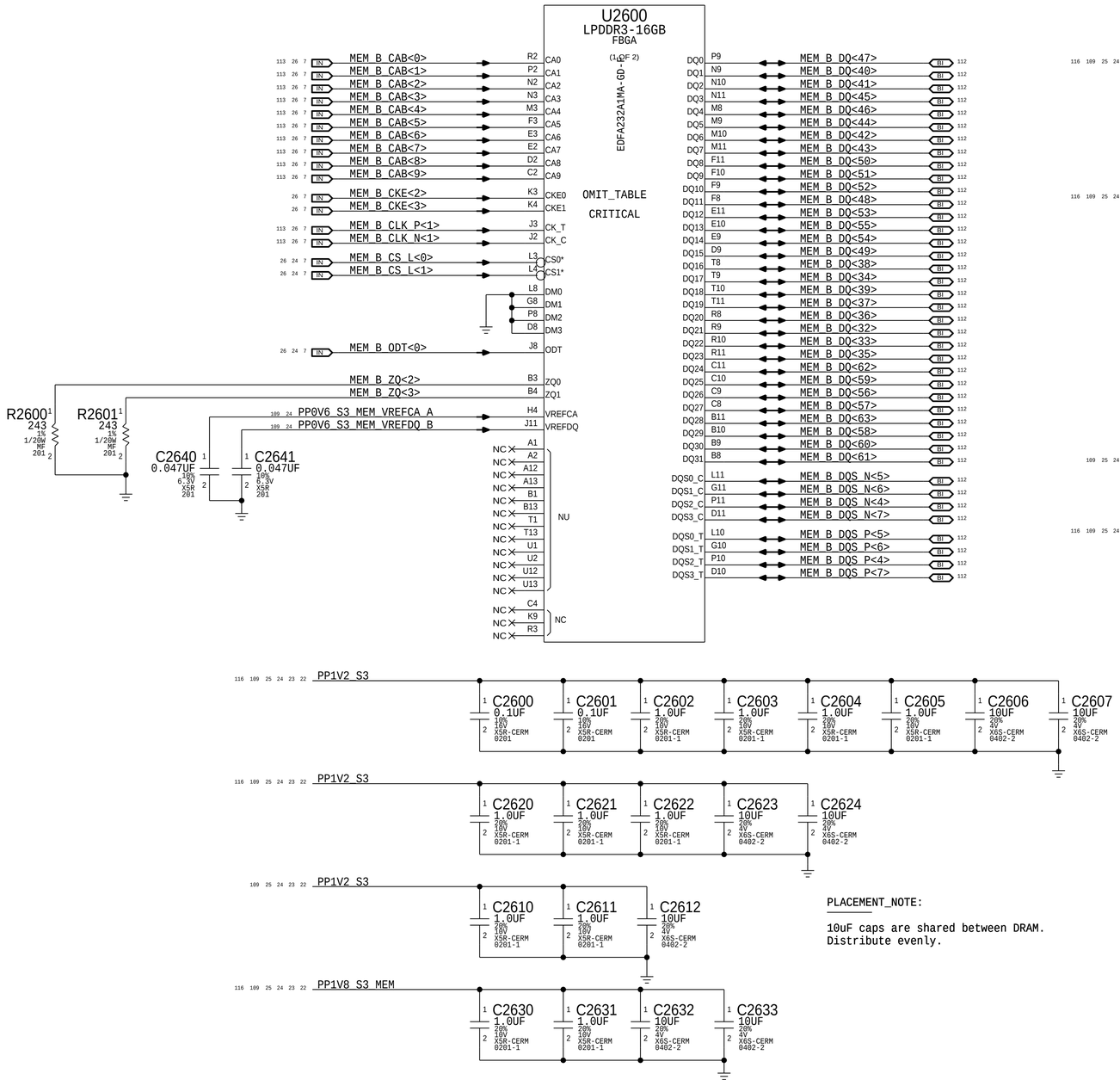
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 25 OF 145
SHEET: 24 OF 121

LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	LPDDR3 DRAM Channel B (32-63)
Apple Inc.	DRAWING NUMBER 051-00647
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	BRANCH dvt-fab10
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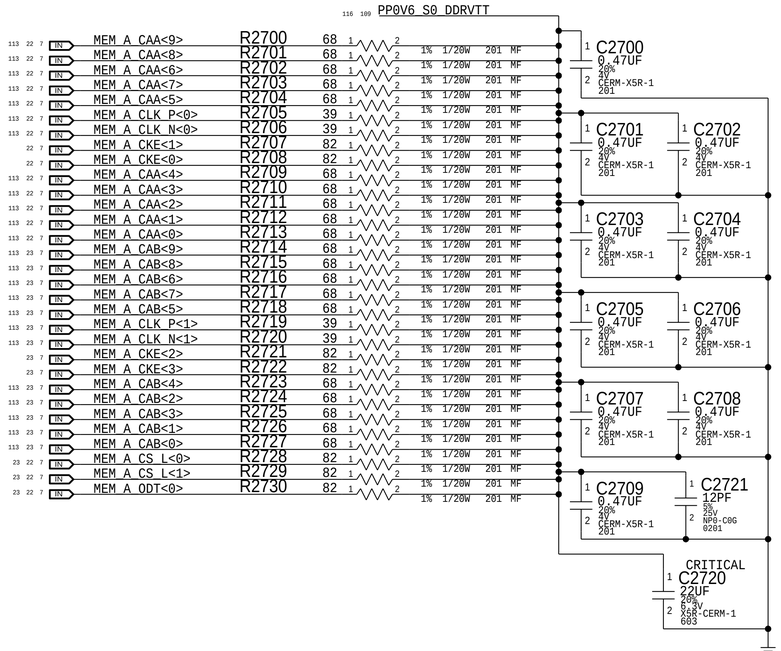
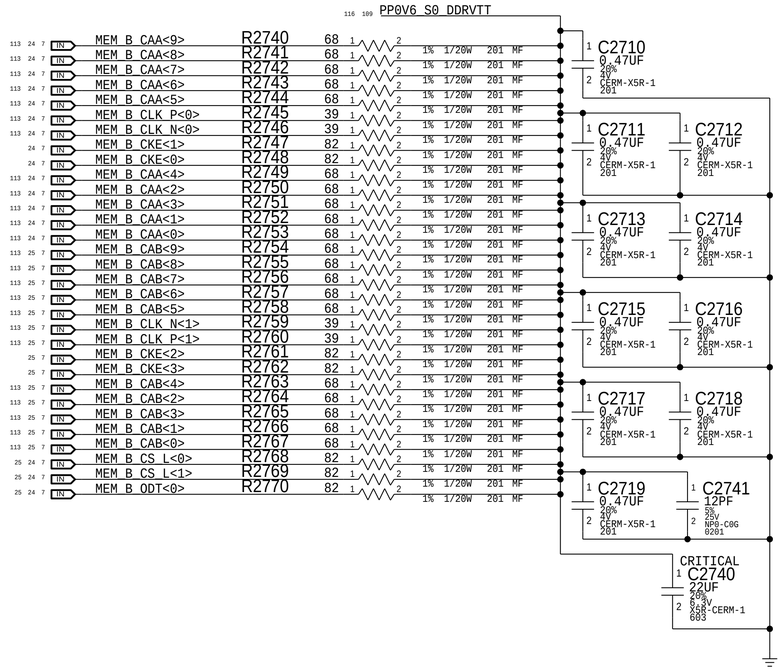
	SHEET 25 OF 121

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

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PP3V3_UPC_XB_LDO
R2890 3.3K
R2891 3.3K
R2893 3.3K
R2892 3.3K
C2890 1UF
U2890 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
U2800 TBT-AR-4C-CNTRL
SYM 1 OF 2
FCBGA
OMIT_TABLE
CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
LC GPIO
POC GPIO
MISC
PORT A
PORT B
TBT PORTS
DEBUG
PLACE_NEAR=U2800.N16:2MM
PLACE_NEAR=U2800.N6:2MM
PLACE_NEAR=U2800.Y18:2MM
PLACE_NEAR=U2800.H19:6MM
PLACE_NEAR=U2800.F19:5MM
PP3V3_S5_TBT_X_SW
PU at PCH
not used
To SPI Flash
USE NEAREST GND BALL (AC22) FOR THERM_D_N
GND_VOID=TRUE
BOM_COST_GROUP=TBT

DRAWING LAST_MODIFIED=Wed Aug 24 09:57:49 2016

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 1

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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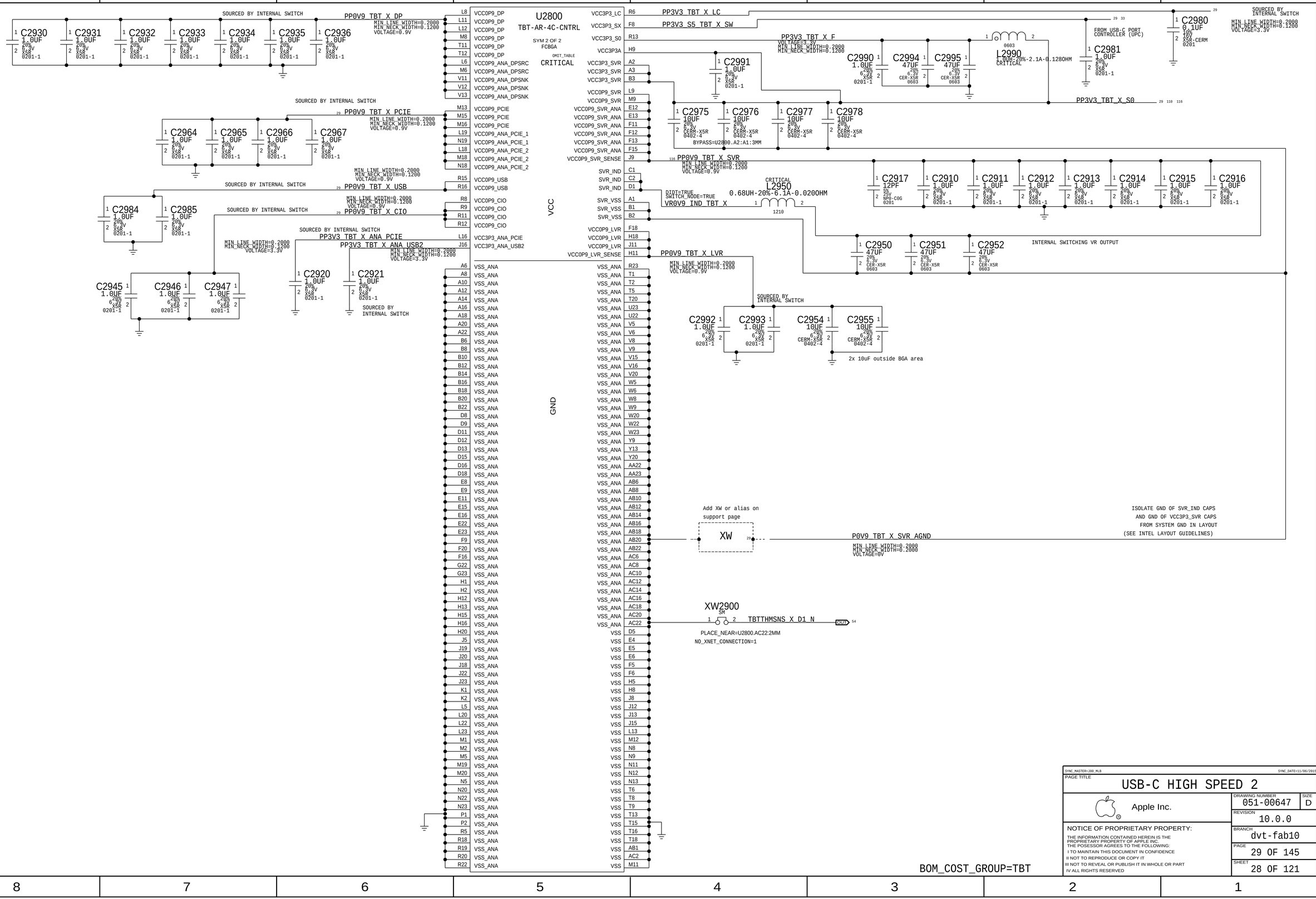

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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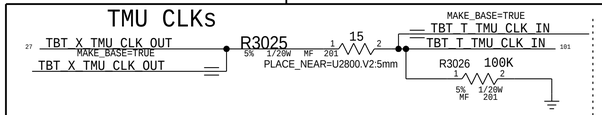
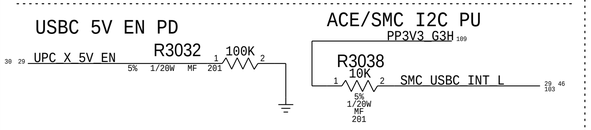
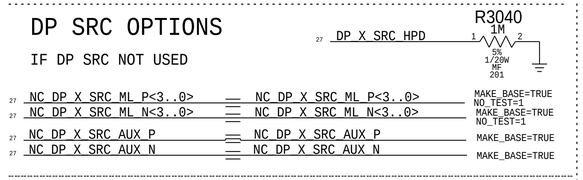
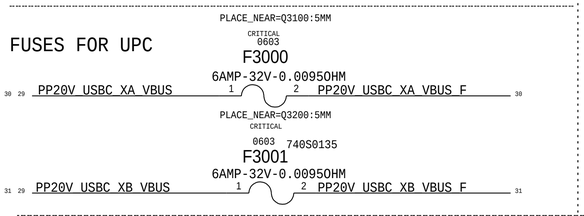
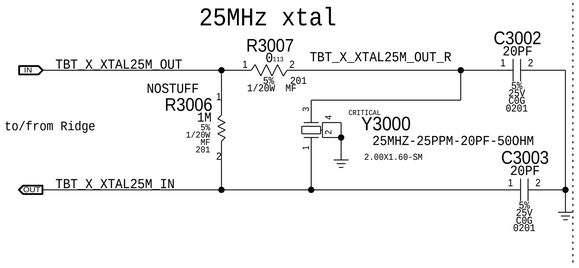
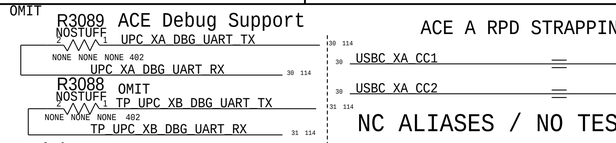


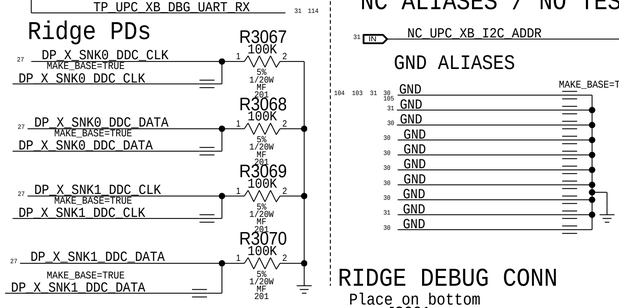


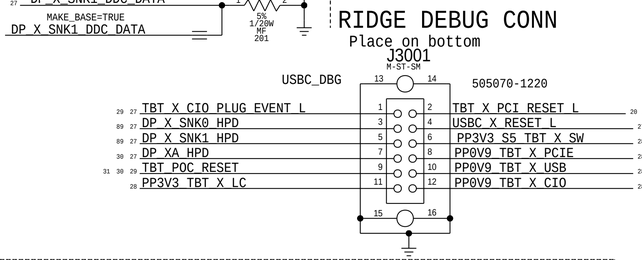


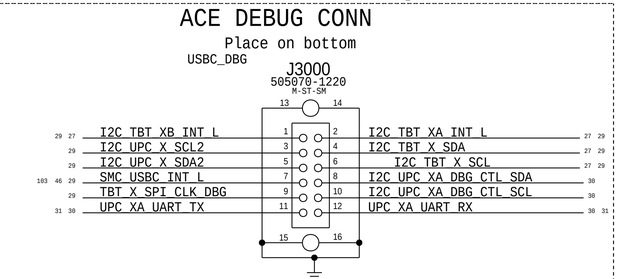


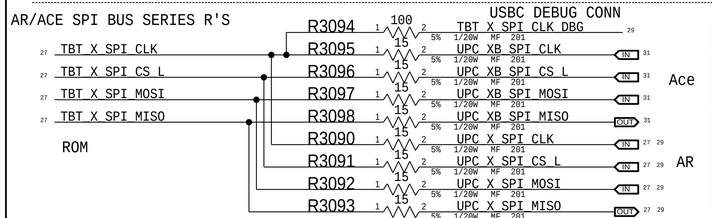


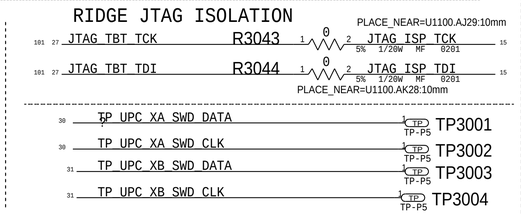


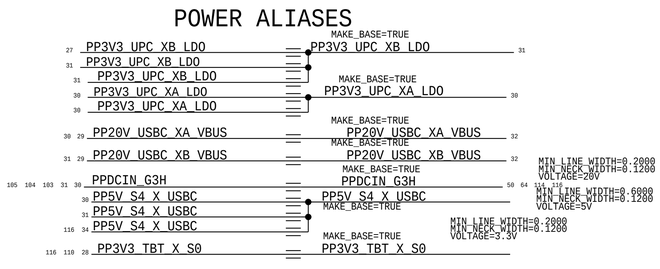


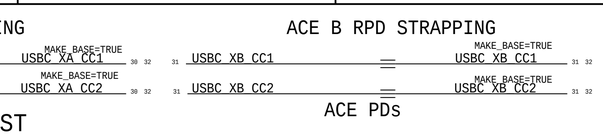


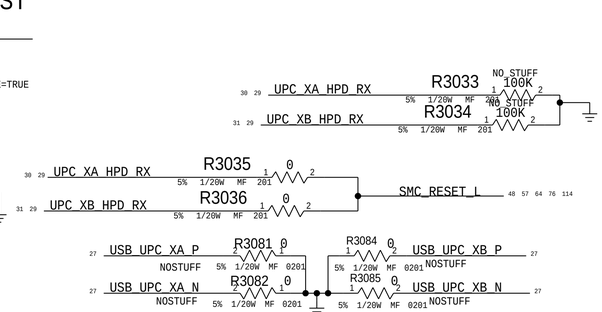


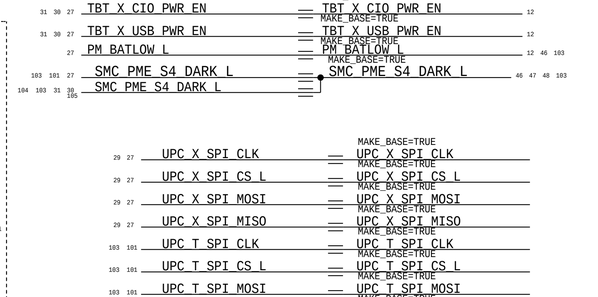


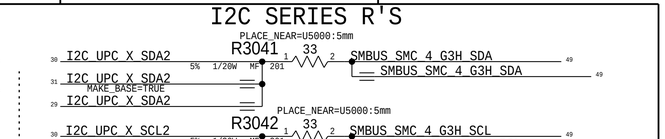


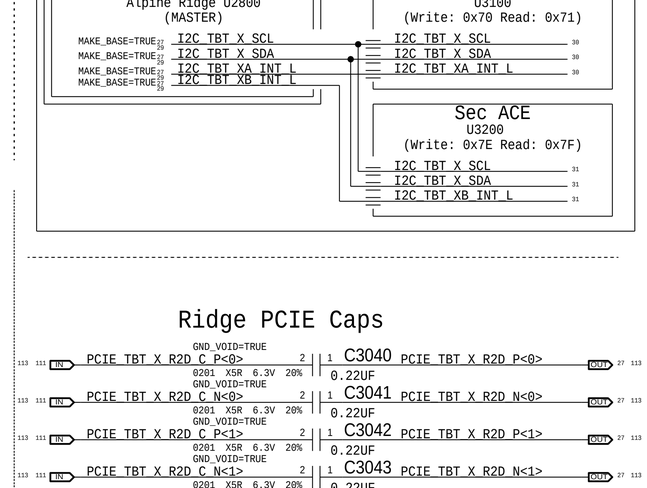


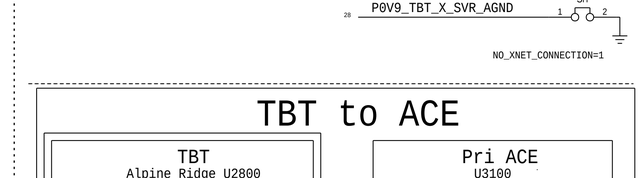


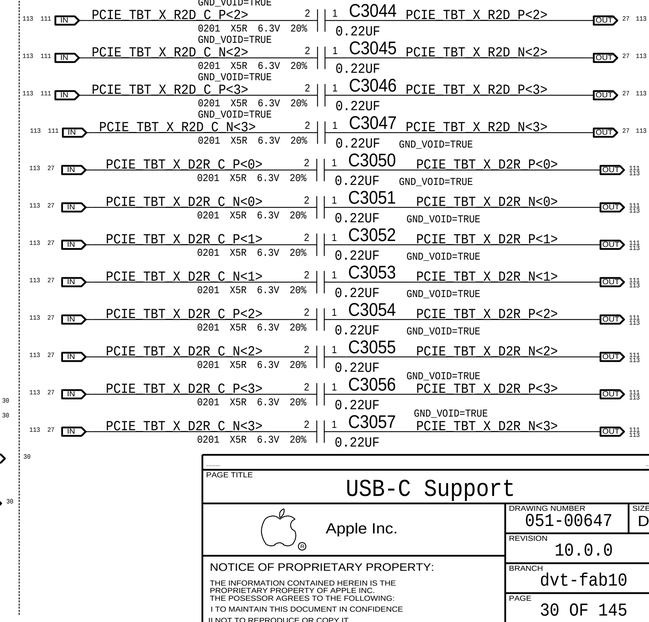












BOM_COST_GROUP=TBT

PAGE TITLE
USB-C Support

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 30 OF 145
SHEET 29 OF 121

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 31 OF 145
SHEET 30 OF 121

NOTICE OF PROPRIETARY PROPERTY:

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

CRITICAL
Q3200
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

29 PP20V_USBC_XB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

29 PP20V_USBC_XB_VBUS
C3201 1UF 10% 25V X5R 0402

PPDCIN_G3H 29 30 103 104 105
MAX 100uF TOTAL ON RAIL

UPC_XB_GATE1
TP_Q3200_DRAIN
UPC_XB_GATE2

29 PP3V3_UPC_XB_LDO
109 PP3V3_G3H
GND
29 PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE

C3200 10UF 20% 6.3V CERM-X5R 0402-1

PP3V3_UPC_XB_LDO 29
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V
P3V3_TBT_X_SX_EN_R 33
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_XB_LDOA
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V
PP1V8_UPC_XB_LDOD
PP1V1_UPC_XB_LDO_BMC
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.1V

C3205 1.0UF 20% 6.3V X5R 0201-1
C3208 10UF 20% 6.3V CERM-X5R 0402-1
C3204 2.2UF 20% 4V X5R-CERM 0201
C3206 0.47UF 10% 6.3V CERM-X5R 0201

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

U3200
CD3215A
BGA
CRITICAL
OMIT_TABLE

30 29 IN	TBT_POC_RESET	E11	MRESET
33 OUT	USBC_X_RESET_L_R	F11	RESET*
114 29	TP_UPC_XB_DBG_UART_TX	B2	GPIO0
114 29	TP_UPC_XB_DBG_UART_RX	C2	GPIO1
30 29 27 BI	TBT_X_CIO_PWR_EN	D10	GPIO2
30 29 27 BI	TBT_X_USB_PWR_EN	G11	GPIO3
27 OUT	DP_XB_HPD	C10	GPIO4
29	UPC_XB_HPD_RX	E10	GPIO5
29 OUT	UPC_X_5V_EN	G10	GPIO6
105 104 103 30 29 OUT	SMC_PME_S4_DARK_L	D7	GPIO7
29 OUT	UPC_XB_FAULT_L	H6	GPIO8
29 IN	GND	F10	BUSPOWERZ
29	NC_UPC_XB_I2C_ADDR	F1	I2C_ADDR
	UPC_XB_R_OSC	G2	R_OSC
31	I2C_UPC_XB_DBG_CTL_SCL	E4	DEBUG_CTL1
31	I2C_UPC_XB_DBG_CTL_SDA	D5	DEBUG_CTL2
29 BI	I2C_TBT_X_SDA	D1	I2C_SDA1
29 BI	I2C_TBT_X_SCL	D2	I2C_SCL1
29 OUT	I2C_TBT_XB_INT_L	C1	I2C_IRQ1*
29 BI	I2C_UPC_X_SDA2	A5	I2C_SDA2
29 BI	I2C_UPC_X_SCL2	B5	I2C_SCL2
29 OUT	SMC_USBC_INT_L	B6	I2C_IRQ2*
29 OUT	UPC_XB_SPI_CLK	A3	SPI_CLK
29 OUT	UPC_XB_SPI_MOSI	B4	SPI_MOSI
29 IN	UPC_XB_SPI_MISO	A4	SPI_MISO
29 OUT	UPC_XB_SPI_CS_L	B3	SPI_SSZ
29	TP_UPC_XB_SWD_DATA	F4	SWD_DATA
29	TP_UPC_XB_SWD_CLK	G4	SWD_CLK
31 30 29	UPC_XA_UART_TX	F2	UART_RX
30 29 OUT	UPC_XA_UART_RX	E2	UART_TX
27 IN	TBT_XB_LSTX	L4	LSX_R2P
27 OUT	TBT_XB_LSRX	K4	LSX_P2R
	USB_UPC_XB_F_P	L5	USB_RP_P
	USB_UPC_XB_F_N	K5	USB_RP_N
	DP_XB_AUXCH_P	J1	AUX_P
	DP_XB_AUXCH_N	J2	AUX_N
42 BI	SOC_SWCLK_DBG	L2	DEBUG1
42 BI	SOC_SWDIO_DBG	K2	DEBUG2
29 BI	SMC_DEBUGPRT_TX_L	L3	DEBUG3
29 BI	SMC_DEBUGPRT_RX_L	K3	DEBUG4

PULL R3209 AND R3208 UP TO ACE's LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XB_LDO 29
R3209 1M 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SCL 31
R3208 1M 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SDA 31

CRITICAL
R3203 15K 0.1% 1/20W TF-LF 0201 — NEED 0.1%

R3205 1M 5% 1/20W MF 201 — UPC_XA_UART_TX 29 30 31

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

L3200 90-OHM-0.1A EXCX4CE SYM_VER_1
USB2_UPC_XB_P 29 BI — 1 — 4 — PLACE_NEAR=U3200.L5:5mm
USB2_UPC_XB_N 29 BI — 2 — 3 — PLACE_NEAR=U3200.K5:5mm

29 PP3V3_S4
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
R3210 100K 5% 1/20W MF 201
113 27 BI
113 27 BI
R3211 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS	H7	UPC_XB_SS
SENSEP	B10	
SENSEN	A10	
HV_GATE1	B9	
HV_GATE2	A9	

C3209 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1	L9	USBC_XB_CC1
C_CC2	L10	USBC_XB_CC2
RPD_G1	K9	USBC_XB_CC1
RPD_G2	K10	USBC_XB_CC2
C_USB_TP	K6	USBC_XB_USB_TOP_P
C_USB_TN	L6	USBC_XB_USB_TOP_N
C_USB_BP	K7	USBC_XB_USB_BOT_P
C_USB_BN	L7	USBC_XB_USB_BOT_N
C_SBU1	K8	USBC_XB_SBU1
C_SBU2	L8	USBC_XB_SBU2
NC	L11	GROUND

BI 29 32 — BI 29 32
BI 29 — BI 29
BI 32 — BI 32
BI 32 — BI 32
BI 32 115 — BI 32 115

C3214 220PF 10% 16V CER-X7R 0201
C3213 220PF 10% 16V CER-X7R 0201

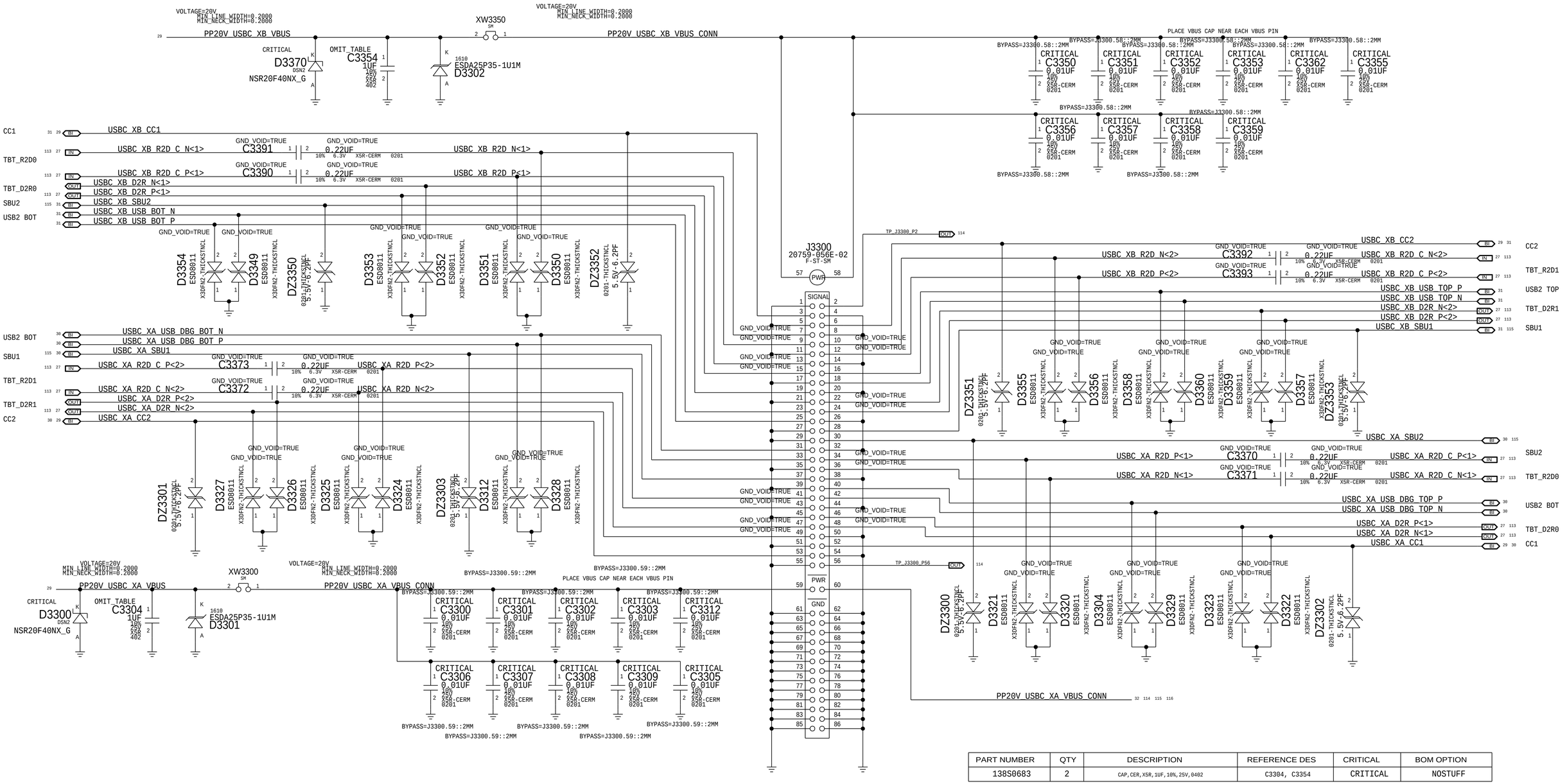
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

NC or GND to dissipate heat

GND 29
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015
PAGE TITLE: USB-C PORT CONTROLLER B
Apple Inc.
DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 32 OF 145
SHEET: 31 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D

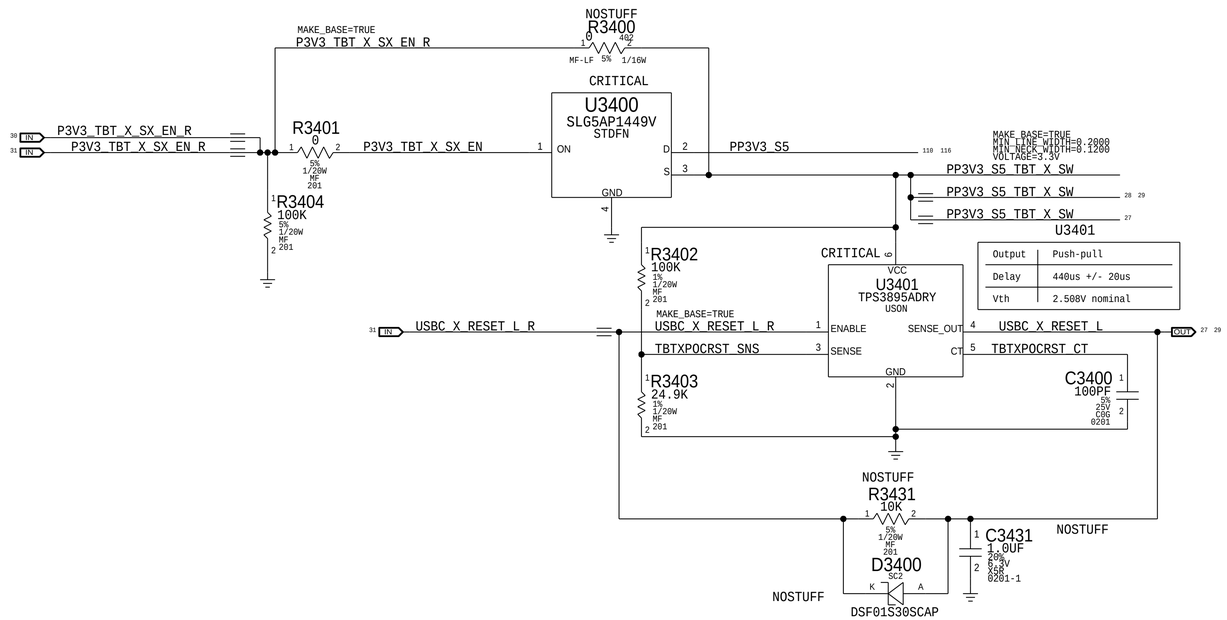
REVISION: 10.0.0

BRANCH: dvt-fab10

PAGE: 33 OF 145

SHEET: 32 OF 121

TBT X "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

SYNC_MASTER=X502_MLB SYNC_DATE=03/29/2016

PAGE TITLE

USB-C CONNECTOR B

Apple Inc.

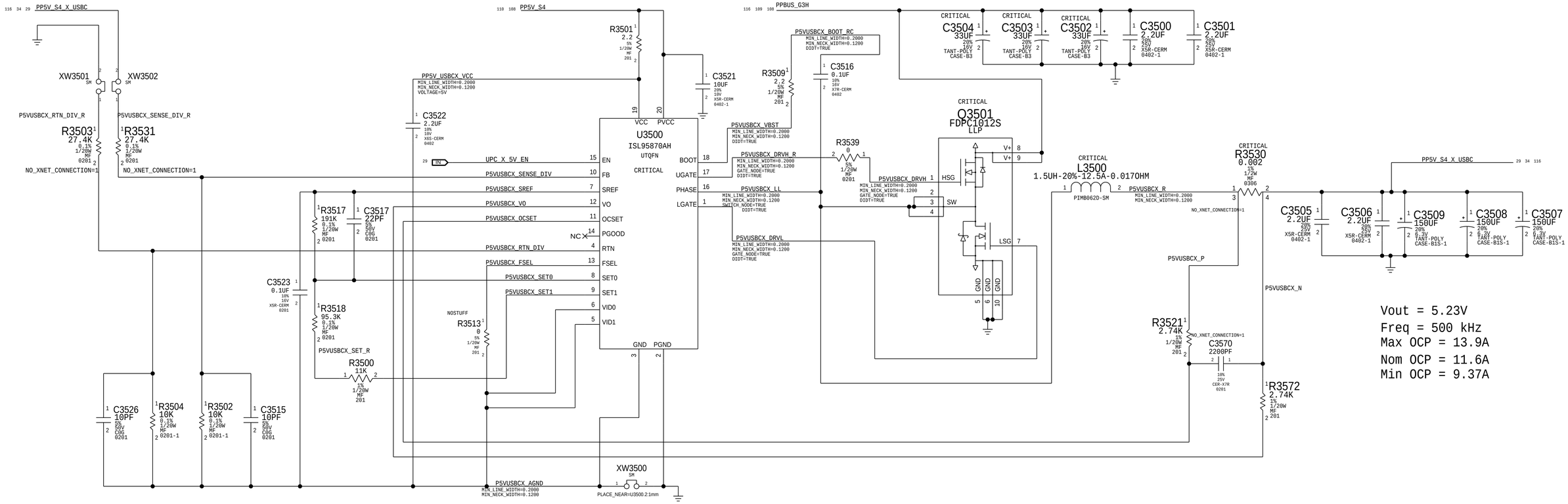
DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 34 OF 145

SHEET 33 OF 121



BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=12/04/2015

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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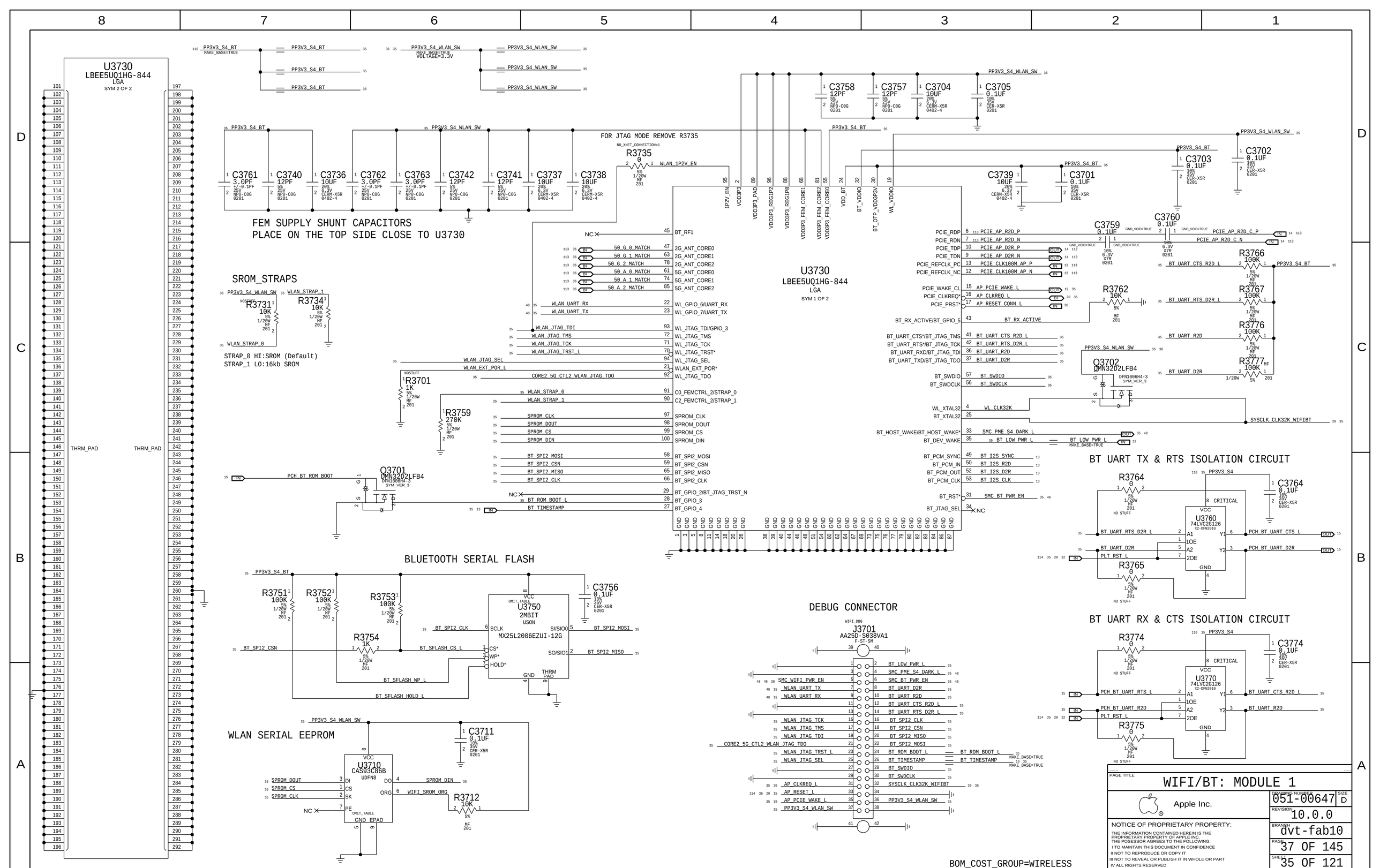
U3730
LBEE5UQ1HG-844
LGA
SYM 2 OF 2
THRM_PAD
THRM_PAD
PP3V3_S4_BT
MAKE_BASE=TRUE
PP3V3_S4_WLAN_SW
MAKE_BASE=TRUE
VOLTAGE=3.3V
C3761 3.0PF
C3740 12PF
C3736 10UF
C3762 3.0PF
C3763 3.0PF
C3742 12PF
C3741 12PF
C3737 10UF
C3738 10UF
FEM SUPPLY SHUNT CAPACITORS
PLACE ON THE TOP SIDE CLOSE TO U3730
FOR JTAG MODE REMOVE R3735
NO_XNET_CONNECTION=1
R3735 0
WLAN_1P2V_EN
C3758 12PF
C3757 12PF
C3704 10UF
C3705 0.1UF
C3739 10UF
C3701 0.1UF
C3703 0.1UF
C3702 0.1UF
C3759 0.1UF
C3760 0.1UF
SROM_STRAPS
R3731 10K
R3734 10K
WLAN_STRAP_1
WLAN_STRAP_0
STRAP_0 HI:SROM (Default)
STRAP_1 LO:16kb SROM
R3701 1K
R3759 270K
Q3701 DMN32D2LFB4
PCH_BT_ROM_BOOT
BT_TIMESTAMP
BLUETOOTH SERIAL FLASH
R3751 100K
R3752 100K
R3753 100K
R3754 1K
U3750 2MBIT USON
MX25L2006EZUI-12G
C3756 0.1UF
BT_SFLASH_WP_L
BT_SFLASH_HOLD_L
WLAN SERIAL EEPROM
U3710 CAT93C86B UDFN8
C3711 0.1UF
R3712 10K
WIFI_SROM_ORG
U3730
LBEE5UQ1HG-844
LGA
SYM 1 OF 2
PCIE_RDP
PCIE_RDN
PCIE_TDP
PCIE_TDN
PCIE_REFCLK_PC
PCIE_REFCLK_NC
PCIE_WAKE_CL
PCIE_CLKREQ*
PCIE_PRST*
BT_RX_ACTIVE/BT_GPIO_5
BT_UART_CTS*/BT_JTAG_TMS
BT_UART_RTS*/BT_JTAG_TCK
BT_UART_RXD/BT_JTAG_TDI
BT_UART_TXD/BT_JTAG_TDO
BT_SWDIO
BT_SWDCLK
WL_XTAL32
BT_XTAL32
BT_HOST_WAKE/BT_HOST_WAKE*
BT_DEV_WAKE
BT_PCM_SYNC
BT_PCM_IN
BT_PCM_OUT
BT_PCM_CLK
BT_RST*
BT_JTAG_SEL
R3762 10K
Q3702 DMN32D2LFB4
SYSCLK CLK32K WIFIBT
BT UART TX & RTS ISOLATION CIRCUIT
R3764 0
R3765 0
U3760 74LVC2G126
C3764 0.1UF
DEBUG CONNECTOR
J3701 AA25D-S038VA1
F-ST-SM
BT UART RX & CTS ISOLATION CIRCUIT
R3774 0
R3775 0
U3770 74LVC2G126
C3774 0.1UF
BOM_COST_GROUP=WIRELESS
PAGE TITLE
WIFI/BT: MODULE 1
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 37 OF 145
SHEET 35 OF 121
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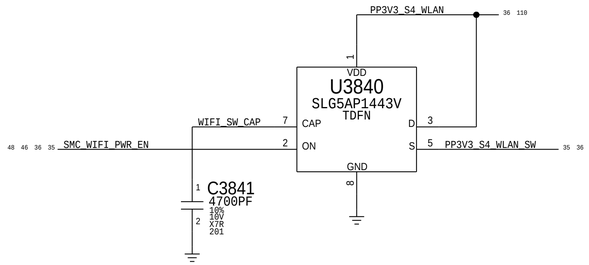
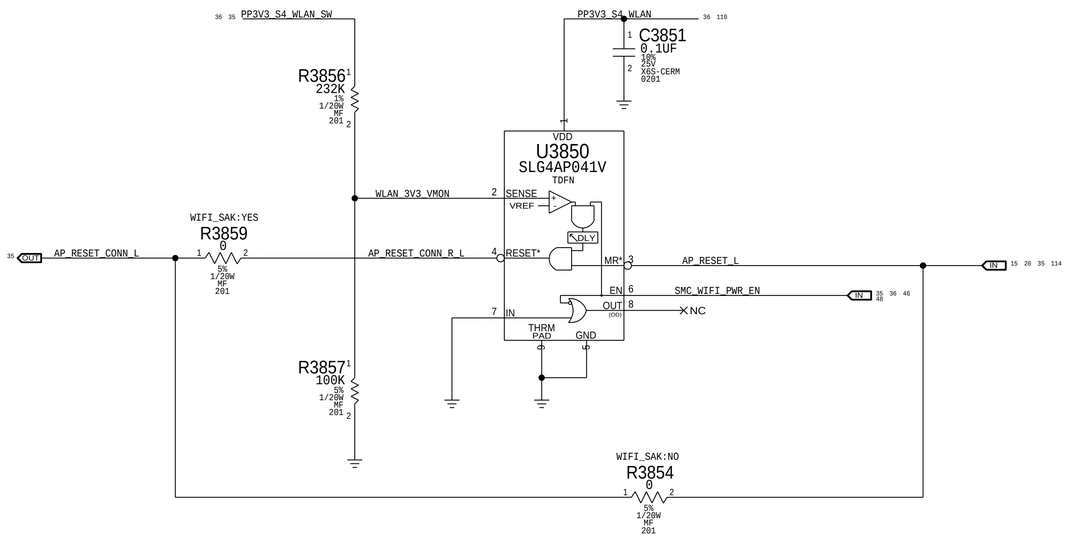
WLAN Power Switch

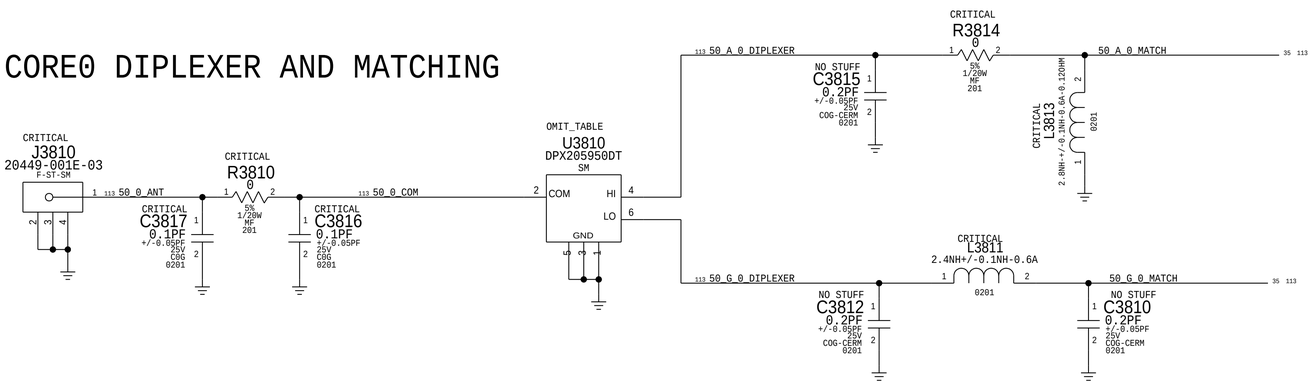


Supervisor & CLKREQ# Isolation

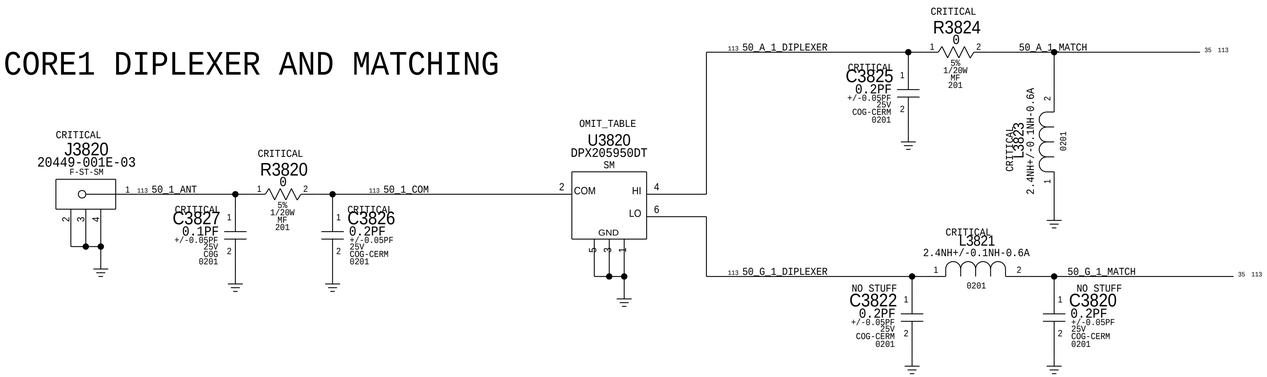
Delay = 130ms +/- 20%



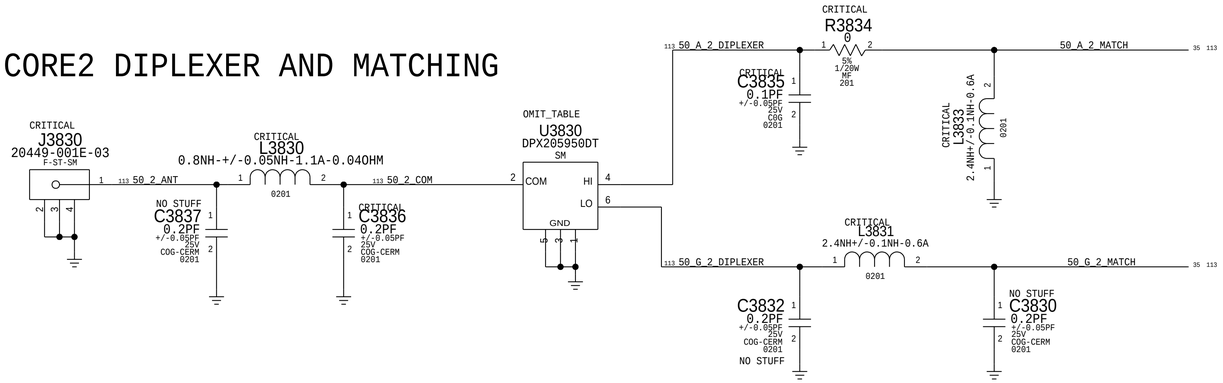
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

WIFI/BT: MODULE 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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SHEET 36 OF 121

T208

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00136	1	IC,M8+512MB 20NM DDR,A12,S,SCK,BGA780	U3900	CRITICAL	SOC:HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338S00097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD

SEP ROM

PP1V8_AWAKE_SW3C
C3903 0.1UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=U3901.8:2mm
U3901 MZ4128 EEPROM MLP
VCC E2 E1 E0 WC* SCL SDA VSS THM_P
R3970 10K 5% 1/20W MF 201
SEP_ROM_WC
SEP_I2C_SCL
SEP_I2C_SDA

L3900

L3900 120-OHM-0.1A-1.5-OHM 0201
PP1V1_SLEEP1_SW2
PP1V1_SLEEP1_PLL_DDR_FILT
VOLTAGE=1.1V
C3900 0.22UF 10% 6.3V X5R-CERM 0201
PP1V1_SLEEP3_BUCK2
VDDIO11_RET_DDR (N25)
VDDIO11_PLL_DDR (U21)

unstuff R3951 and stuff R3952 to enable boundary scan

PP1V8_SLEEP2_SW3A
R3952 NOSTUFF 1K 5% 1/20W MF 201
SOC_JTAG_SEL
R3951 10K 5% 1/20W MF 201
M7 needed stronger PU but should be fixed on M8
PP1V8_AWAKE_SW3C
R3953 NOSTUFF 1K 5% 1/20W MF 201
SOC_SWDIO

PP1V8_SLEEP2_SW3A
R3973 10K 5% 1/20W MF 201
PMU_TO_SOC_RESET_L
C3960 100PF 5% 25V C0G 0201

32K CLK OPTION

PLACE_NEAR=U3900.AA22:3mm
R3990 0 5% 1/20W MF 0201
SOC_PMU_CLK_32K
GREENCLK
SOC_CLK_32K
SOC
R3925 0 5% 1/20W MF 0201 NOSTUFF
PMU_TO_SOC_CLK_32K
SOC PMU
PLACE_NEAR=U3900.AA22:3mm

PP1V1_SLEEP1_SW2
R3901 240 1% 1/20W MF 201
R3902 240 1% 1/20W MF 201
SOC_PAD_ZQ_A
SOC_DDR_RREF
PMU_TO_SOC_SLEEP1_PWRGD
PMU_TO_SOC_SYS_ALIVE

U3900 M8-LPDDR4-H-A-FUSE

OMIT_TABLE
UFBGA
(1 OF 7)

DDR0_CA_0	L25	NC
DDR0_CA_1	L26	NC
DDR0_CA_2	N26	NC
DDR0_CA_3	N27	NC
DDR0_CA_4	P26	NC
DDR0_CA_5	P25	NC
DDR0_CK_P	M26	NC
DDR0_CK_N	M27	NC
DDR0_CKE	M25	NC
DDR0_CS	L27	NC
DDR0_DMI_0	J26	NC
DDR0_DMI_1	V27	NC
DDR0_DQ_0	E26	NC
DDR0_DQ_1	F26	NC
DDR0_DQ_2	G26	NC
DDR0_DQ_3	H26	NC
DDR0_DQ_4	G27	NC
DDR0_DQ_5	K25	NC
DDR0_DQ_6	H27	NC
DDR0_DQ_7	K26	NC
DDR0_DQ_8	AA25	NC
DDR0_DQ_9	Y25	NC
DDR0_DQ_10	W25	NC
DDR0_DQ_11	Y26	NC
DDR0_DQ_12	V26	NC
DDR0_DQ_13	U26	NC
DDR0_DQ_14	T26	NC
DDR0_DQ_15	T27	NC
DDR0_DQS_P_0	E27	NC
DDR0_DQS_N_0	F27	NC
DDR0_DQS_P_1	W26	NC
DDR0_DQS_N_1	W27	NC
PAD_ZQ_A	R26	
DDR0_RESET_N	M24	NC
DDR0_RREF	N24	
DDR0_RET_N	L24	
DDR0_SYS_ALIVE	P24	

DDR0

AOP_DETECT_0	AD26	DFR_TOUCH_RESET_L (OUT)
AOP_DETECT_1	AD27	NC
AOP_PDM_CLK	AA10	NC
AOP_PDM_DAT	AB10	NC
AOP_PLED_0	AC10	NC
AOP_PLED_1	Y10	NC
AOP_PLED_2	AC14	NC
AOP_PLED_3	AA13	NC
AOP_PLED_4	AD12	NC
AOP_PLED_5	AD13	TP_SOC_CLKOUT
AOP_PLED_6	AC15	NC
AOP_PLED_7	AB14	NC
AOP_PSENSE_CTRL_4	AA24	NC
AOP_PSENSE_CTRL_5	W24	NC
AOP_PSENSE_CTRL_6	AA21	NC
AOP_PSENSE_CTRL_7	Y24	NC
AOP_PSPI_CS_TRIG_3	AD22	DFR_TOUCH_SPI_CS_L (OUT)
AOP_PSPI_CS_TRIG_4	AD23	NC
AOP_PSPI_MISO	AD24	DFR_TOUCH_SPI_MISO (IN)
AOP_PSPI_MOSI	Y20	DFR_TOUCH_SPI_MOSI (OUT)
AOP_PSPI_SCLK	AB21	DFR_TOUCH_SPI_CLK (OUT)
AOP_SPI0_MISO	AC22	NC
AOP_SPI0_MOSI	AC23	NC
AOP_SPI0_SCLK	AD21	NC
AOP_MON_0	AE13	SOC_TO_STOCKHOLM_DWLD_REQ
AOP_MON_1	AE14	NC
AOP_MON_2	AB15	PCH_SOC_DBELL_L (IN)
AOP_MON_3	Y14	NC
AOP_MON_4	AE15	PMU_TO_SOC_IRQ_L (IN)
AOP_MON_5	AD15	NC
AOP_MON_6	AA14	NC
AOP_MON_7	AC16	NC
AOP_I2S0_MCK	AA9	NC
AOP_I2S1_MCK	AB9	NC
AOP_SWD_TCK_OUT	AE16	NC
AOP_SWD_TMS0	AD16	NC
AOP_SWD_TMS1	AB16	NC
AOP_I2C0_SCL	AB20	MESA_I2C_SCL (OUT)
AOP_I2C0_SDA	AE26	MESA_I2C_SDA (BI)
AOP_I2C1_SCL	AE27	ALS_SCL_I2C_1V8 (OUT)
AOP_I2C1_SDA	AA19	ALS_SDA_I2C_1V8 (BI)

SOC_JTAG_SEL	AB12	JTAG_SEL
TP_SOC_JTAG_TRST_L	AB11	JTAG_TRSTN
SOC_SWDIO	AC13	JTAG_TMS
SOC_SWCLK	AD10	JTAG_TCK
TP_SOC_JTAG_TDI	AD9	JTAG_TDI
TP_SOC_JTAG_TDO	AA11	JTAG_TDO
PMU_TO_SOC_RESET_L (IN)	AE10	CFSB_AOP
PMU_TO_SOC_SLEEP1_PWRGD (IN)	Y12	AOP_DDR_PWRGOOD
SOC_SLEEP1_REQ (OUT)	AB13	AOP_DDR_REQ
SOC_WDOG_RST	AE11	WDOG
SOC_VDD_HI_LO (OUT)	AE12	SOC_VDD_HI_LO
	AC11	AOP_DOCK_ATTENTION
	AC12	AOP_DOCK_CONNECT
SOC_CLK_32K	AA22	RT_CLK32768
PMU_TO_SOC_AWAKE_PWRGD (IN)	AB24	AWAKE_PWRGOOD
SOC_AWAKE_REQ (OUT)	AD11	AWAKE_REQ
PMU_TO_SOC_RESET_L (IN)	AA12	COLD_RESETN

U3900 M8-LPDDR4-H-A-FUSE

OMIT_TABLE
UFBGA
(2 OF 7)

VDD18_LPPLL
PP1V8_SLEEP2_LPPLL_FILT
VOLTAGE=1.8V
C3902 0.47UF 10% 6.3V CERM-X5R 0201
R3900 499 1% 1/20W MF 201
PP1V8_SLEEP2_SW3A

AOP_LSPI_MISO	AA20	NC
AOP_LSPI_MOSI	AB22	NC
AOP_LSPI_SCLK	AD25	NC
AOP_SPI_CS_TRIG_0	AE20	NC
AOP_SPI_CS_TRIG_1	AB17	MESA_PWR_EN (OUT)
AOP_SPI_CS_TRIG_2	AB18	SOC_TO_STOCKHOLM_DEV_WAKE
AOP_SPI_CS_TRIG_3	AE21	SOC_SPI_BOOT_STATUS
AOP_SPI_CS_TRIG_4	AD19	NC
AOP_SPI_CS_TRIG_5	AA17	NC
AOP_SPI_CS_TRIG_6	AC19	NC
AOP_SPI_CS_TRIG_7	AE22	NC
AOP_SPI_CS_TRIG_8	AE23	NC
AOP_SPI_CS_TRIG_9	AB19	NC
AOP_SPI_CS_TRIG_10	AA18	NC
AOP_SPI_CS_TRIG_11	AE24	NC
AOP_SPI_CS_TRIG_12	AD20	NC
AOP_SPI_CS_TRIG_13	AC21	NC
AOP_SPI_CS_TRIG_14	Y18	NC
AOP_SPI_CS_TRIG_15	AE25	NC
AOP_UART0_CTSN	AC17	NC
AOP_UART0_RTSN	AE18	NC
AOP_UART0_RXD	AE17	NC
AOP_UART0_TXD	AA15	NC
AOP_UART1_CTSN	AA16	NC
AOP_UART1_RTSN	AE19	NC
AOP_UART1_RXD	AD17	NC
AOP_UART1_TXD	AC18	NC
AOP_UART2_RXD	AD18	NC
AOP_UART2_TXD	Y16	NC

R3943 78.7K 1% 1/20W MF 201
PPSVDD_STOCKHOLM

UART_SOC_TO_STOCKHOLM_TXD (IN)	C1	RX
UART_STOCKHOLM_TO_SOC_TXD (OUT)	B1	TX
UART_SOC_TO_STOCKHOLM_RTS_L (IN)	D2	CTS
UART_STOCKHOLM_TO_SOC_RTS_L (OUT)	A1	RTS
SOC_TO_STOCKHOLM_EN (IN)	E1	VEN

STOCKHOLM

PP_STOCKHOLM_TVDD
PP3V3_S0_LEFT
C3919 4.7UF 20% 6.3V X5R 402
C3925 1.0UF 20% 6.3V X5R 0201-1
PPVDD_STOCKHOLM
C3916 0.1UF 10% 6.3V CERM-X5R 0201
C3917 1.0UF 20% 6.3V X5R 0201-1
PP1V8_AWAKE_SW3C
C3918 1.0UF 20% 6.3V X5R 0201-1
PPSVDD_STOCKHOLM
C3915 0.1UF 10% 6.3V CERM-X5R 0201

OMIT_TABLE
U3905
PN66VEU3-A101D004
UFLGA

IRQ	D1	NC
SVDD_REQ	A5	NC
DWL	B2	SOC_TO_STOCKHOLM_DWLD_REQ
CLK_REQ	A2	NC
NFC_CLK_XTAL1	A3	NC
RX	C1	UART_SOC_TO_STOCKHOLM_TXD
TX	B1	UART_STOCKHOLM_TO_SOC_TXD
CTS	D2	UART_SOC_TO_STOCKHOLM_RTS_L
RTS	A1	UART_STOCKHOLM_TO_SOC_RTS_L
VEN	E1	SOC_TO_STOCKHOLM_EN
SMX_RST*	E3	PPSVDD_STOCKHOLM
SMX_CLK	E4	NC
ESE_IO1	F4	NC
SPIM_MOSI	B3	NC
SPIM_MISO	B4	NC
SPIM_SCK	E6	NC
XTAL2	C3	NC
SPIM_IRQ	F1	NC
SIM_SWIO	A4	NC
GPIO0	A7	NC
SPIM_NSS	A6	NC
TX_PWR_REQ	D5	NC
ESE_DWPM_DBG	G7	NC
ESE_DWPS_DBG	G6	NC
RXP	F6	NC
RXN	F5	NC
TX1	G3	NC
TX2	G5	NC
WKUP_REQ	E5	SOC_TO_STOCKHOLM_DEV_WAKE
VMID	F7	PP_STOCKHOLM_VMID
SE2_PWR_REQ	F2	NC
SE2_SVDD_IN	G1	NC

VSS E2 AVSS D4 AVSS D6 AVSS F3 DVSS B6 DVSS C4 TVSS G4 PVSS C2
C3926 0.1UF 10% 6.3V CERM-X5R 0201

4MB SPI ROM

PP1V8_AWAKE_SW3C
C3920 0.1UF 10% 6.3V CERM-X5R 0201
R3941 10K 5% 1/20W MF 201
R3942 10K 5% 1/20W MF 201
U3906 4MX8-1.8V UFDFPN N25Q032A11E
SOC_ROM_SPI_CLK_R
SOC_ROM_SPI_CS_L
SOC_ROM_SPI_WP_L
SOC_ROM_SPI_RST_L
SOC_ROM_SPI_MOSI_R
SOC_ROM_SPI_MISO_R

I2C Pullups

PP1V8_AWAKE_SW3C
R3904 2.2K 5% 1/20W MF 201
R3905 2.2K 5% 1/20W MF 201
SEP_I2C_SCL
SEP_I2C_SDA
PP1V8_AWAKE_SW3C
R3911 2.2K 5% 1/20W MF 201
R3912 2.2K 5% 1/20W MF 201
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
PP1V8_S0SW_DFR
R3915 2.2K 5% 1/20W MF 201
R3916 2.2K 5% 1/20W MF 201
DFR_TOUCH_ROM_I2C_SCL
DFR_TOUCH_ROM_I2C_SDA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SERIAL,SPI,4MX8,4X3MM,DFN8	U3906		

T208 DFU_STATUS Isolation

DFU_STATUS can be driven high outside of S0
U3910 creates version that is only high in S0
PP1V8_S0
R3981 0 5% 1/20W MF 0201
DFU_STATUS
DFU_SPI_STATUS
U3910 74LVC2G08GT/S505 SOT833
PCH_SOC_DFU_STATUS
R3980 0 5% 1/20W MF 0201 NOSTUFF
SOC_SPI_BOOT_STATUS

T208 WDOG Isolation

SOC_WDOG_RESET can be driven high outside of S0
U3910 creates version that is only high in S0
PP1V8_S0
C3950 0.1UF 10% 6.3V CERM-X5R 0201
U3910 74LVC2G08GT/S505 SOT833
SOC_WDOG_RST
PCH_SOC_WDOG
R3972 300K 5% 1/20W MF 201
R3971 100K 5% 1/20W MF 201

PP1V8_S0
R3960 3.0K 5% 1/20W MF 201
R3961 3.0K 5% 1/20W MF 201
ALS_SCL_I2C_1V8
ALS_SDA_I2C_1V8

PP1V8_S0
R3906 1K 5% 1/20W MF 201
R3907 1K 5% 1/20W MF 201
I2C_CAM_SCL
I2C_CAM_SDA
PP1V8_S0SW_DFR
R3917 4.7K 5% 1/20W MF 201
R3918 4.7K 5% 1/20W MF 201
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA

SOC_TO_STOCKHOLM_DWLD_REQ
R3940 100K 5% 1/20W MF 201 NOSTUFF

BOM_COST_GROUP=T151

PAGE TITLE: Camera/DFR 1

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
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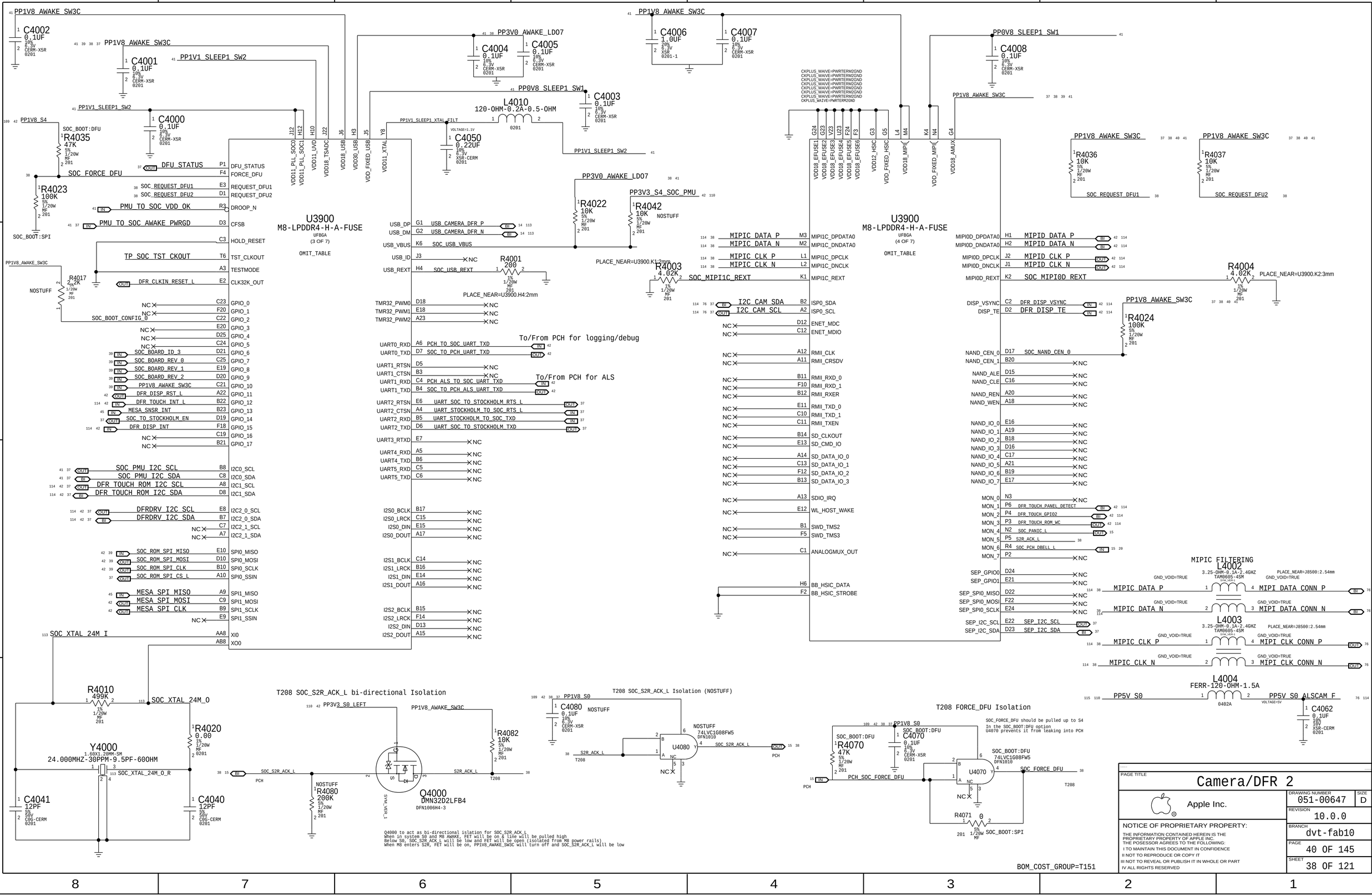
PP1V8_AWAKE_SW3C
C4002 0.1UF
PP1V8_AWAKE_SW3C
C4001 0.1UF
PP1V1_SLEEP1_SW2
C4000 0.1UF
PP1V8_S4
R4035 47K
SOC_BOOT:DFU
SOC_BOOT:SPI
SOC FORCE DFU
R4023 100K
PMU TO SOC VDD OK
PMU TO SOC AWAKE PWRGD
TP SOC TST CKOUT
R4017 2.2K
NOSTUFF
DFR CLKIN RESET L
SOC_BOARD_ID_3
SOC_BOARD_REV_0
SOC_BOARD_REV_1
SOC_BOARD_REV_2
PP1V8_AWAKE_SW3C
DFR_DISP_RST_L
DFR_TOUCH_INT_L
MESA_SNSR_INT
SOC_TO_STOCKHOLM_EN
DFR_DISP_INT
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
DFR TOUCH ROM I2C SCL
DFR TOUCH ROM I2C SDA
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA
SOC_ROM_SPI_MISO
SOC_ROM_SPI_MOSI
SOC_ROM_SPI_CLK
SOC_ROM_SPI_CS_L
MESA_SPI_MISO
MESA_SPI_MOSI
MESA_SPI_CLK
SOC_XTAL_24M_I
U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(3 OF 7)
OMIT_TABLE
DFU_STATUS
SOC_REQUEST_DFU1
SOC_REQUEST_DFU2
PMU_TO_SOC_VDD_OK
PMU_TO_SOC_AWAKE_PWRGD
TP_SOC_TST_CKOUT
DFR_CLKIN_RESET_L
SOC_BOOT_CONFIG_0
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
DFR_TOUCH_ROM_I2C_SCL
DFR_TOUCH_ROM_I2C_SDA
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA
SOC_ROM_SPI_MISO
SOC_ROM_SPI_MOSI
SOC_ROM_SPI_CLK
SOC_ROM_SPI_CS_L
MESA_SPI_MISO
MESA_SPI_MOSI
MESA_SPI_CLK
SOC_XTAL_24M_I
PP3V0_AWAKE_LDO7
C4004 0.1UF
C4005 0.1UF
PP0V8_SLEEP1_SW1
C4003 0.1UF
L4010
120-OHM-0.2A-0.5-OHM
PP1V1_SLEEP1_XTAL_FILT
C4050 0.22UF
PP1V1_SLEEP1_SW2
PP3V0_AWAKE_LDO7
R4022 10K
PP3V3_S4_SOC_PMU
R4042 10K
NOSTUFF
PLACE_NEAR=U3900.K1:2mm
R4003 4.02K
SOC_MIPI1C_REXT
R4001 200
PLACE_NEAR=U3900.H4:2mm
USB_CAMERA_DFR_P
USB_CAMERA_DFR_N
SOC_USB_VBUS
SOC_USB_REXT
To/From PCH for logging/debug
PCH_TO_SOC_UART_TXD
SOC_TO_PCH_UART_TXD
To/From PCH for ALS
PCH_ALS_TO_SOC_UART_TXD
SOC_TO_PCH_ALS_UART_TXD
UART_SOC_TO_STOCKHOLM_RTS_L
UART_STOCKHOLM_TO_SOC_RTS_L
UART_STOCKHOLM_TO_SOC_TXD
UART_SOC_TO_STOCKHOLM_TXD
I2S0_BCLK
I2S0_LRCK
I2S0_DIN
I2S0_DOUT
I2S1_BCLK
I2S1_LRCK
I2S1_DIN
I2S1_DOUT
I2S2_BCLK
I2S2_LRCK
I2S2_DIN
I2S2_DOUT
PP1V8_AWAKE_SW3C
C4006 1.0UF
C4007 0.1UF
MIPIC_DATA_P
MIPIC_DATA_N
MIPIC_CLK_P
MIPIC_CLK_N
SOC_MIPI1C_REXT
I2C_CAM_SDA
I2C_CAM_SCL
ENET_MDC
ENET_MDIO
RMII_CLK
RMII_CRSDV
RMII_RXD_0
RMII_RXD_1
RMII_RXER
RMII_TXD_0
RMII_TXD_1
RMII_TXEN
SD_CLKOUT
SD_CMD_IO
SD_DATA_IO_0
SD_DATA_IO_1
SD_DATA_IO_2
SD_DATA_IO_3
SDIO_IRQ
WL_HOST_WAKE
SWD_TMS2
SWD_TMS3
ANALOGMUX_OUT
BB_HSIC_DATA
BB_HSIC_STROBE
CKPLUS_WAIVE=PWRTERM2GND
CKPLUS_WAIVE=PWRTERMD0ND
PP0V8_SLEEP1_SW1
C4008 0.1UF
PP1V8_AWAKE_SW3C
R4036 10K
R4037 10K
SOC_REQUEST_DFU1
SOC_REQUEST_DFU2
MIPID_DATA_P
MIPID_DATA_N
MIPID_CLK_P
MIPID_CLK_N
SOC_MIPI0D_REXT
R4004 4.02K
PLACE_NEAR=U3900.K2:3mm
DISP_VSYNC
DISP_TE
DFR_DISP_VSYNC
DFR_DISP_TE
PP1V8_AWAKE_SW3C
R4024 100K
NAND_CEN_0
NAND_CEN_1
NAND_ALE
NAND_CLE
NAND_REN
NAND_WEN
NAND_IO_0
NAND_IO_1
NAND_IO_2
NAND_IO_3
NAND_IO_4
NAND_IO_5
NAND_IO_6
NAND_IO_7
SOC_NAND_CEN_0
MON_0
MON_1
MON_2
MON_3
MON_4
MON_5
MON_6
MON_7
DFR_TOUCH_PANEL_DETECT
DFR_TOUCH_GPIO2
DFR_TOUCH_ROM_WC
SOC_PANIC_L
S2R_ACK_L
SOC_PCH_DBELL_L
SEP_GPIO0
SEP_GPIO1
SEP_SPI0_MISO
SEP_SPI0_MOSI
SEP_SPI0_SCLK
SEP_I2C_SCL
SEP_I2C_SDA
MIPIC FILTERING
L4002
3.25-OHM-0.1A-2.4GHZ
TAM0605-4SM
MIPIC_DATA_P
MIPI_DATA_CONN_P
L4003
MIPIC_DATA_N
MIPI_DATA_CONN_N
MIPIC_CLK_P
MIPI_CLK_CONN_P
MIPIC_CLK_N
MIPI_CLK_CONN_N
L4004
FERR-120-OHM-1.5A
PP5V_S0
PP5V_S0_ALSCAM_F
C4062 0.1UF
R4010 499K
SOC_XTAL_24M_O
Y4000
1.60X1.20MM-SM
24.000MHZ-30PPM-9.5PF-600HM
SOC_XTAL_24M_O_R
C4041 12PF
C4040 12PF
R4020 0.00
T208 SOC_S2R_ACK_L bi-directional Isolation
PP3V3_S0_LEFT
PP1V8_AWAKE_SW3C
R4082 10K
R4080 200K
NOSTUFF
Q4000
DMN32D2LFB4
DFN1006H4-3
SOC_S2R_ACK_L
S2R_ACK_L
T208 SOC_S2R_ACK_L Isolation (NOSTUFF)
PP1V8_S0
C4080 0.1UF
NOSTUFF
U4080
74LVC1G08FW5
DFN1010
T208 FORCE_DFU Isolation
SOC_FORCE_DFU should be pulled up to S4
In the SOC_BOOT:DFU option
U4070 prevents it from leaking into PCH
R4070 47K
C4070 0.1UF
U4070
SOC_FORCE_DFU
PCH_SOC_FORCE_DFU
R4071 0
SOC_BOOT:SPI
Q4000 to act as bi-directional islation for SOC_S2R_ACK_L
When in system S0 and M8 AWAKE, FET will be on & line will be pulled high
Below S0, SOC_S2R_ACK_L will be low and FET will be open (isolated from M8 power rails)
When M8 enters S2R, FET will be on, PP1V8_AWAKE_SW3C will turn off and SOC_S2R_ACK_L will be low
BOM_COST_GROUP=T151
PAGE TITLE
Camera/DFR 2
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
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38 OF 121
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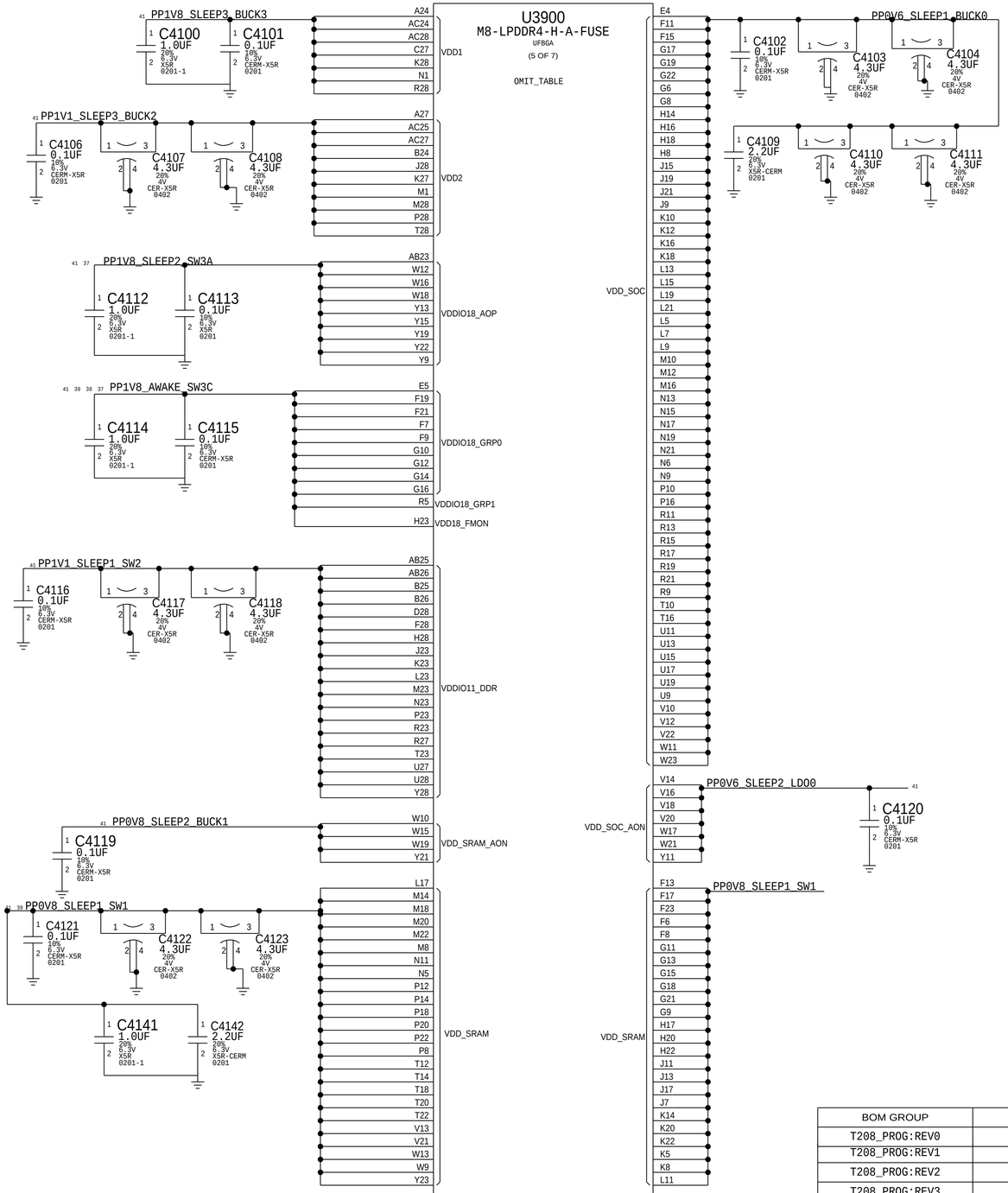
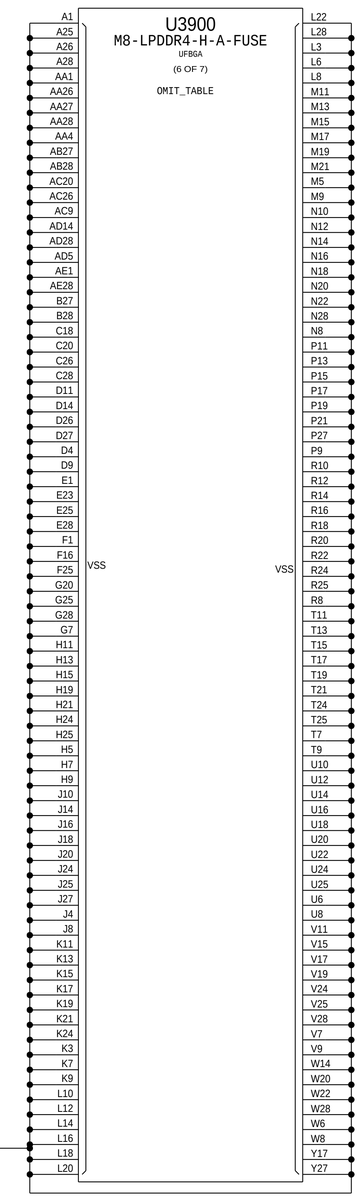
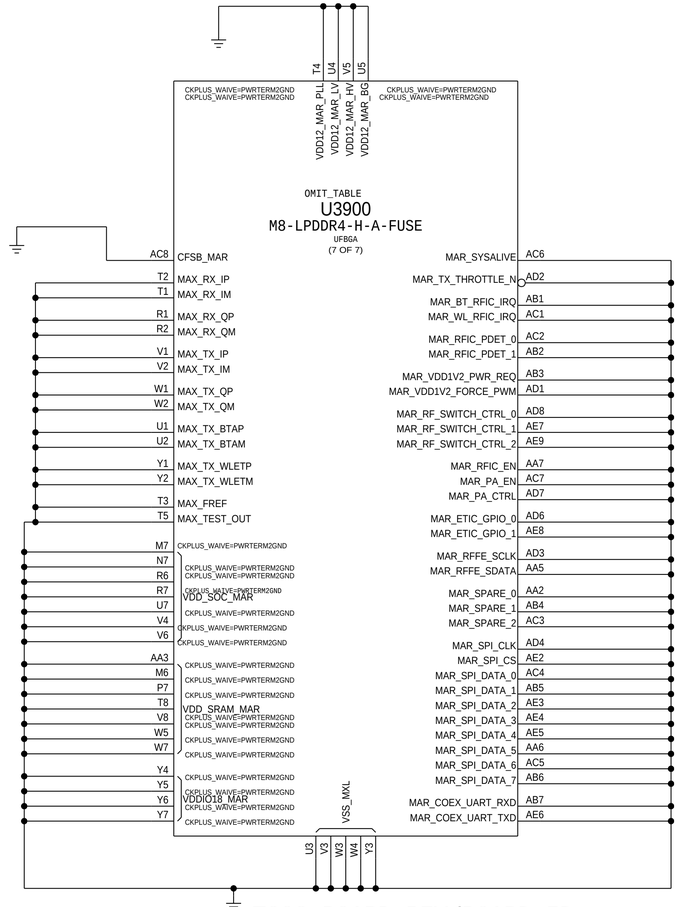


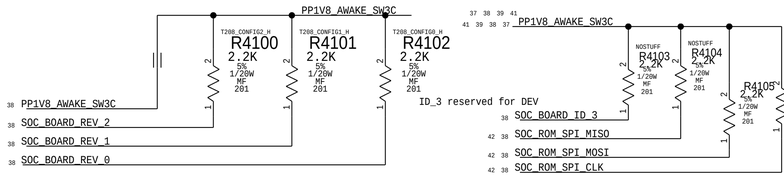




T208 BOARD REV/BOARD ID

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



BOARD REV[3:0]	MODE
1111	T208_Rev0 (X362 P0)
1110	T208_Rev1 (X363 P0)
1101	T208_Rev2 (X362 P1)
1100	T208_Rev3 (X362 P2)
1011	T208_Rev4 (X363 P2/X362 localEVT)
1010	T208_Rev5 (X363 EVT/X362 EVT1)

BOARD ID[3:0]	MODE
1XXX	T202 DEV
0010	T208

BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

BOM_COST_GROUP=T151

PAGE TITLE: Camera/DFR 3

Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 41 OF 145
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Berkelium

FB for Bucks

R4200 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK0_FB — PP0V6_SLEEP1_BUCK0

R4201 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK1_FB — PP0V8_SLEEP1_SW1

R4202 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK2_FB — PP1V1_SLEEP3_BUCK2

R4203 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK3_FB — PP1V8_SLEEP3_BUCK3

Q4201

CSD58892Q2
SON2X2
PP0V8_SLEEP2_BUCK1
SW1_EXT_ON
PP0V8_SLEEP1_SW1

U4200

D2346A1-OTP-CE
WLCSP
SYM 1 OF 2

PP3V3_S4_SOC_PMU
PLACE_NEAR=U4200.K11:2mm
PLACE_NEAR=U4200.D1:2mm
PLACE_NEAR=U4200.F12:2mm
PLACE_NEAR=U4200.A7:2mm
PLACE_NEAR=U4200.A2:2mm
PLACE_NEAR=U4200.E1:3mm
PLACE_NEAR=U4200.M4:2mm
PLACE_NEAR=U4200.L8:2mm

CRITICAL C4203 15UF 20% 6.3V CERM 0402
CRITICAL C4202 15UF 20% 6.3V CERM 0402
CRITICAL C4204 15UF 20% 6.3V CERM 0402
CRITICAL C4205 15UF 20% 6.3V CERM 0402
CRITICAL C4206 15UF 20% 6.3V CERM 0402
CRITICAL C4207 15UF 20% 6.3V CERM 0402
C4219 2.2UF 20% 6.3V X5R-CERM 0201
C4218 2.2UF 20% 6.3V X5R-CERM 0201
C4220 2.2UF 20% 6.3V X5R-CERM 0201
C4227 0.22UF 10% 6.3V CERM-X5R 0201
C4226 0.022UF 10% 6.3V X5R-CERM 0201
C4228 2.2UF 20% 6.3V X5R-CERM 0201

A7	VDD_MAIN_BUCK0	
A8	VDD_MAIN_BUCK1	
A2	VDD_MAIN_BUCK2	
F12	VDD_MAIN_BUCK3	
G12	VDD_MAIN_BUCK4	
D1	VDD_MAIN_BB	
K11	VDD_MAIN_CHG	
L11	VDD_MAIN_CHG	
M11	VDD_MAIN_CHG	
J1	VDD_MAIN_BBCORE	
K3	ACT_DIODE	NC
L2	VDD_MAIN_SW4	
K12	VBAT	NC
L12	VBAT	NC
M12	VBAT	NC
K10	VBAT_S	NC
C6	SW0_EXT	
D7	SW1_EXT	NC SW1_EXT_ON
E1	BB_LX1	
G1	BB_LX2	
J3	BB_FB	
H1	BB_OUT	
M4	VDD_HVLDO_237	
N2	VDD_HVLDO_45	
L8	VDD_HVLDO_RTC	
L3	VDD_HVLDO_SW6	
M5	LDO2_OUT	NC
N4	LDO3_OUT	NC
M1	LDO4_OUT	NC
N3	LDO5_OUT	NC
N5	LDO7_OUT	PP3V0_AWAKE_LDO7
M2	SW4_OUT	NC
M10	VDD_MAIN_LDO_16	
M6	VDD_MAIN_LDO_8	
M9	VDD_MAIN_LDO_9	PP3V3_S4_SOC_PMU
N7	VDD_MAIN_LDO_AUX	CAP150_AWAKE_PWRTERM2GND
N10	LDO1_OUT	NC
N9	LDO6_OUT	NC
N6	LDO8_OUT	NC
M8	LDO9_OUT	VOLTAGE=1.8V PP1V8_ALWAYS_LDO9
N8	AUX_PWR_OUT	NC
B10	SW1_IN	PP0V8_SLEEP2_BUCK1
A11	SW1_OUT	PP0V8_SLEEP1_SW1
C10	LDO0_OUT	PP0V6_SLEEP2_LDO0
B1	SW2_IN	PP1V1_SLEEP3_BUCK2
C1	SW2_OUT	PP1V1_SLEEP1_SW2
B12	SW3_IN	PP1V8_SLEEP3_BUCK3
B11	SW3A_OUT	PP1V8_SLEEP2_SW3A
C11	SW3B_OUT	NC
C12	SW3C_OUT	PP1V8_AWAKE_SW3C
K1	SW5_IN	
L1	SW5_OUT	NC
K2	SW6_OUT	NC

VSS_BB F1
VSS_BUCK0 A5
VSS_BUCK1 A10
VSS_BUCK2 A4
VSS_BUCK3 D12
VSS_BUCK4 J12

VSS1 B2, VSS2 B9, VSS3 C4, VSS3 C5, VSS3 E5, VSS4 E6, VSS4 H5, VSS4 H6, VSS4 F5, VSS4 F6, VSS4 G5, VSS4 G6, VSS6 M3, VSS7 M7, VSS8 G8, VSS8 H7, VSS8 H8, VSS8 E7, VSS8 F7, VSS8 F8, VSS8 G7, VSS8 A1, VSS9 A12, VSS9 N1, VSS9 N12

L4202 — VDD_SOC

1.0UH-1.82A-0.203OHM
MCFK2012-SM
BUCK0_LX A6 SOC_PMU_BUCK0_LX
BUCK0_FB C9 SOC_PMU_BUCK0_FB
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
DIDT=TRUE
SWITCH_NODE=TRUE

CRITICAL C4208 15UF 20% 6.3V CERM 0402
CRITICAL C4209 15UF 20% 6.3V CERM 0402
CRITICAL C4210 2.2UF 20% 6.3V X5R-CERM 0201
PP0V6_SLEEP1_BUCK0
Mirror Capacitors in Layout

501MA MAX

L4203 — VDD_SRAM_AON, VDD_SRAM, VDD_SOC_AON

1.0UH-1.3A-0.326OHM
MCFK1608T1R0M NA
BUCK1_LX A9 SOC_PMU_BUCK1_LX
BUCK1_FB D9 SOC_PMU_BUCK1_FB
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
DIDT=TRUE
SWITCH_NODE=TRUE

CRITICAL C4211 4.2UF 10% 10V X5R-CERM 0402-1
CRITICAL C4231 4.2UF 10% 10V X5R-CERM 0402-1
CRITICAL C4233 4.7UF 20% 6.3V CER-X5R 0402
CRITICAL C4232 4.7UF 20% 6.3V CER-X5R 0402
PP0V8_SLEEP2_BUCK1
Mirror Capacitors in Layout

VDD_FIXED_MIPI
VDD_FIXED_USB
300MA MAX

L4204 — VDD2, VDDQ, VDD11_XTAL

1.0UH-1.3A-0.326OHM
MCFK1608T1R0M NA
BUCK2_LX A3 SOC_PMU_BUCK2_LX
BUCK2_FB C2 SOC_PMU_BUCK2_FB
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
DIDT=TRUE
SWITCH_NODE=TRUE

CRITICAL C4238 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C4239 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C4240 4.7UF 20% 6.3V CER-X5R 0402
CRITICAL C4241 4.7UF 20% 6.3V CER-X5R 0402
PP1V1_SLEEP3_BUCK2
Mirror Capacitors in Layout

460MA MAX

L4205 — VDD1, VDD18_USB, VDDIO18_GRP0

1.0UH-1.3A-0.326OHM
MCFK1608T1R0M NA
BUCK3_LX E12 SOC_PMU_BUCK3_LX
BUCK3_FB D10 SOC_PMU_BUCK3_FB
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
DIDT=TRUE
SWITCH_NODE=TRUE

CRITICAL C4234 4.7UF 20% 6.3V CER-X5R 0402
CRITICAL C4235 4.7UF 20% 6.3V CER-X5R 0402
CRITICAL C4236 4.7UF 20% 6.3V CER-X5R 0402
CRITICAL C4237 4.7UF 20% 6.3V CER-X5R 0402
PP1V8_SLEEP3_BUCK3
Mirror Capacitors in Layout

100MA MAX

BUCK4_LX H12 NC
BUCK4_FB J10 NC
Not using Buck4

BOM_COST_GROUP=T151

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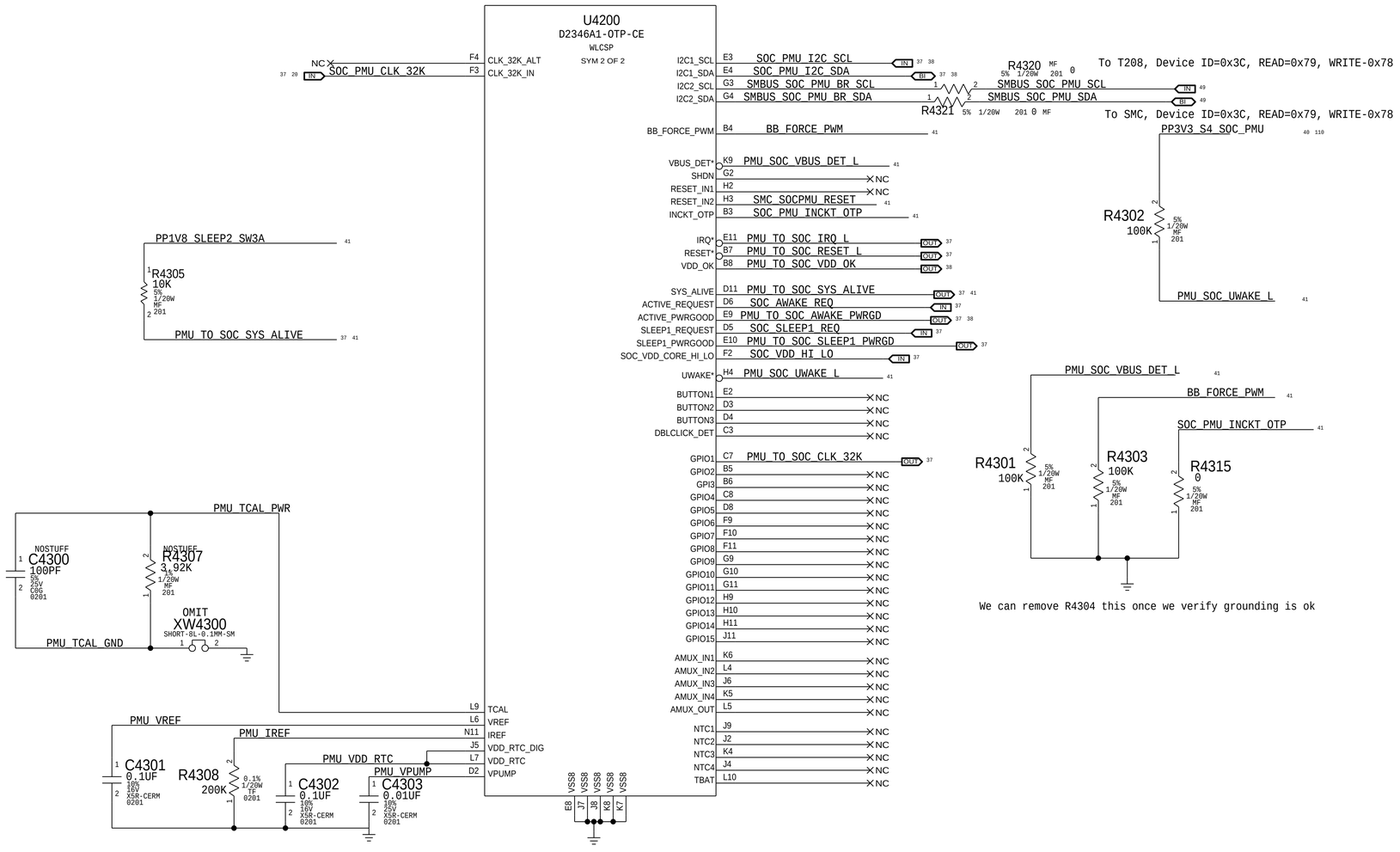
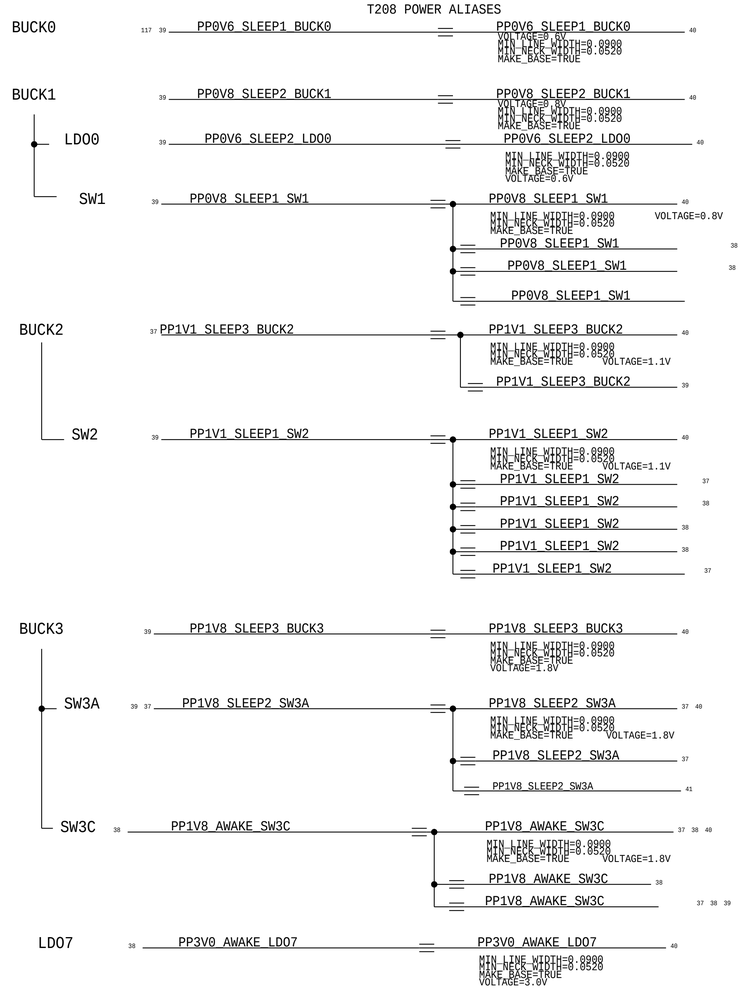
Berkelium - 2





Signal Aliases

SMC_SOCPMU_RESET = SMC_SOCPMU_RESET (MAKE_BASE=TRUE)

BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 2
	Apple Inc.
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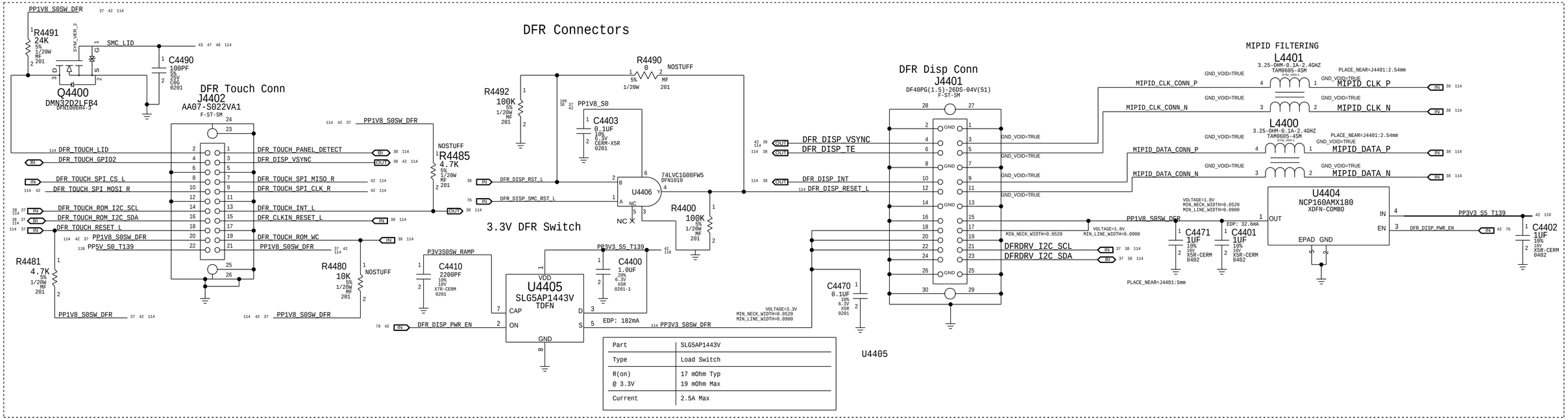
T208 Support

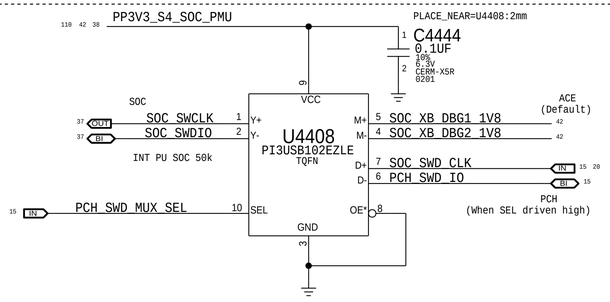
DFR Connectors



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 3.3V	17 mOhm Typ 19 mOhm Max
Current	2.5A Max

U4405

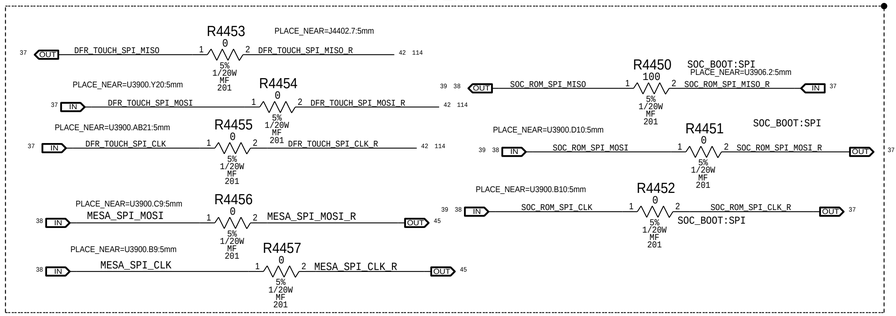
SWD DEBUG MUX



T208 I2C Mapping

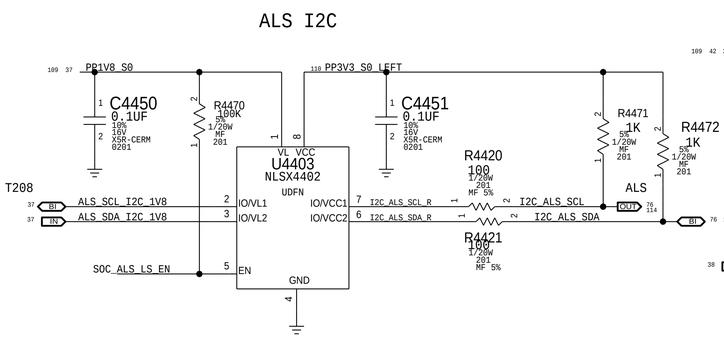
Bus	Device	7-bit Address	8-bit Address Read	8-bit Address Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2

SPI TERM

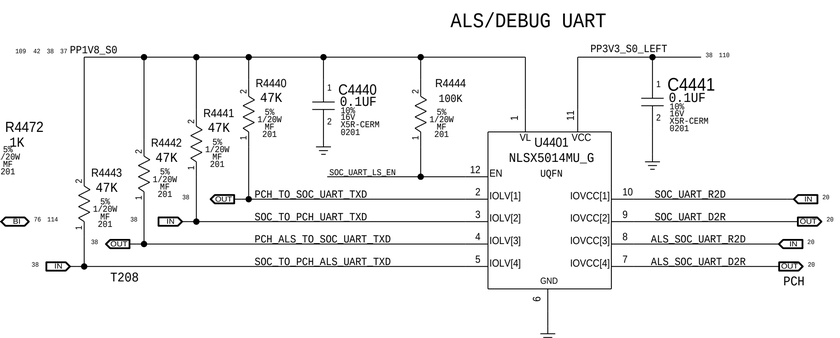


T208 LEVEL SHIFTING

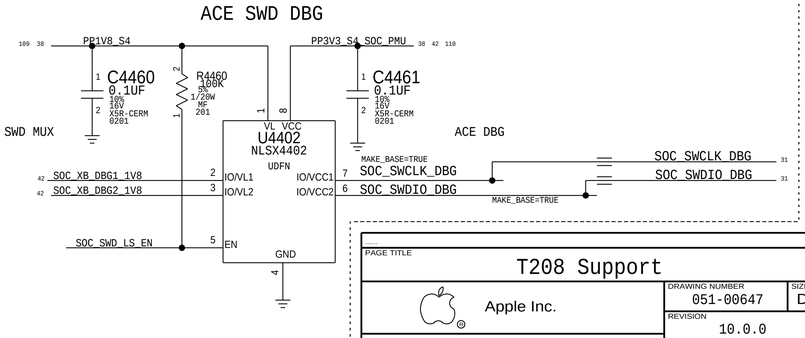
ALS I2C



ALS/DEBUG UART



ACE SWD DBG



BOM_COST_GROUP=T151

PAGE TITLE: T208 Support

Apple Inc.

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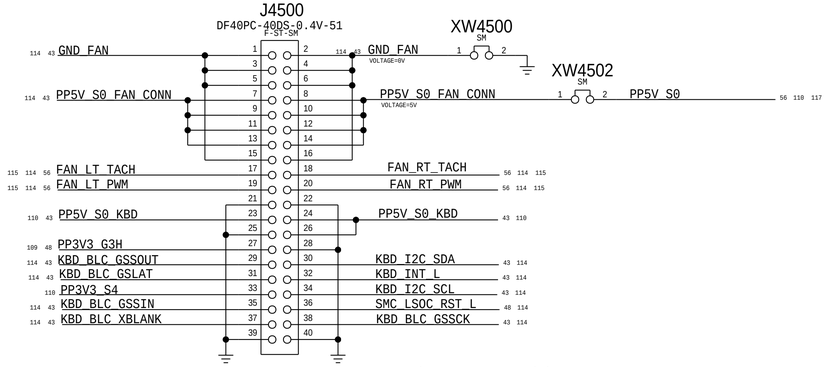
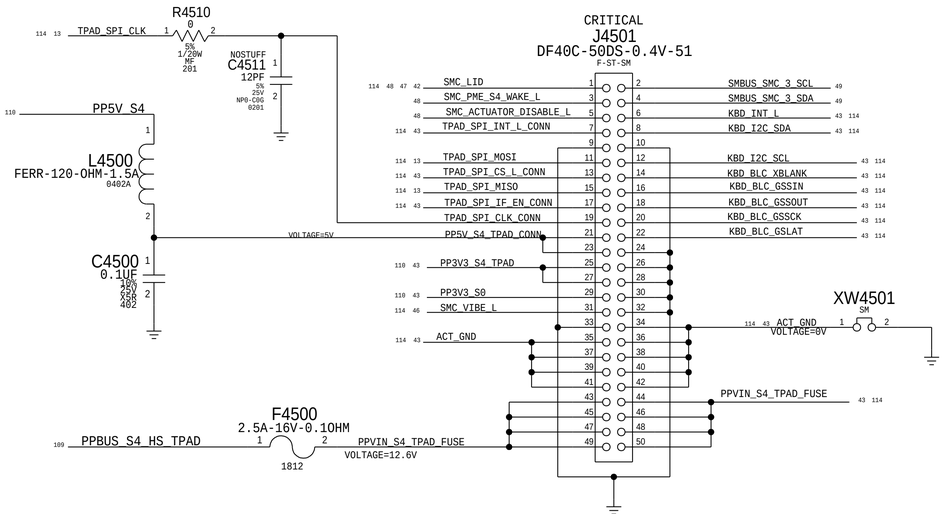
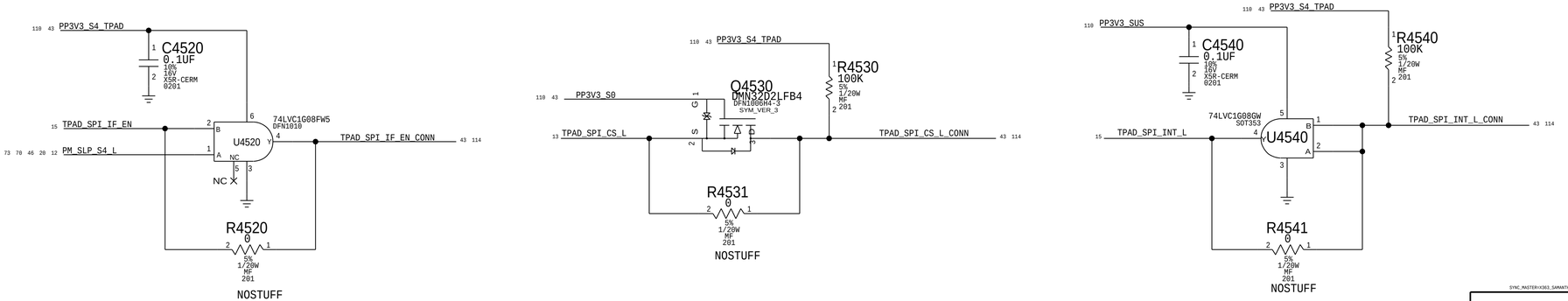
KBD CONNECTOR



TPAD CONNECTOR



TRACKPAD ISOLATION GATES/FET



BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=X383_SAMANTHA SYNC_DATE=01/08/2018

PAGE TITLE: Connectors&ESD

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
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Debug Stuff Was Here

BOM_COST_GROUP=DEBUG

SYNC_MASTER=J68_MLB SYNC_DATE=08/26/2015

PAGE TITLE

External A USB3 Connector

Apple Inc.

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REVISION 10.0.0

BRANCH dvt-fab10

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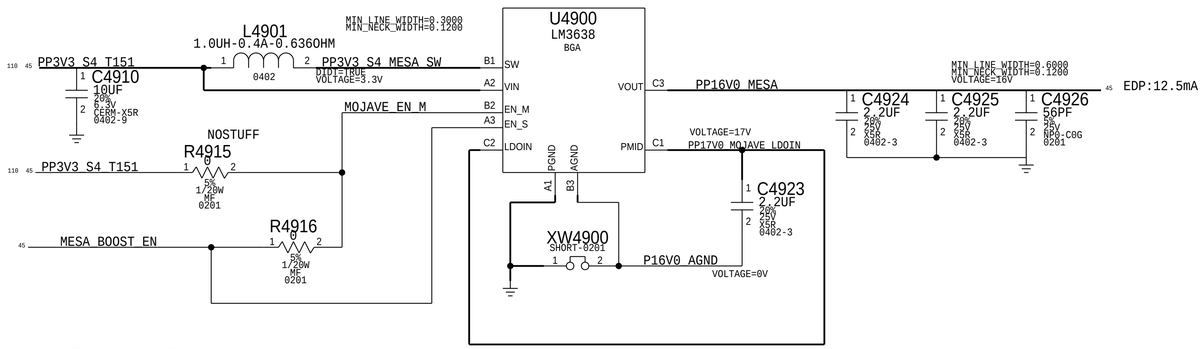
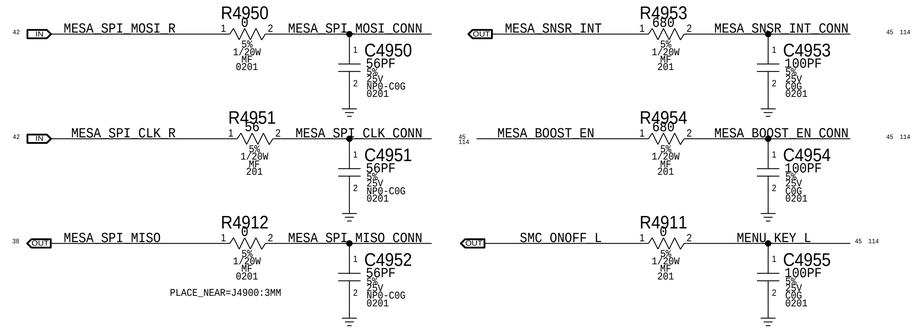
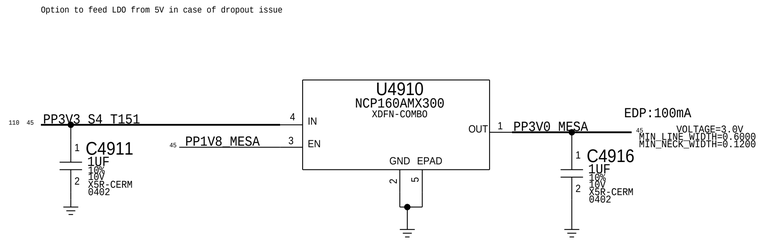
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

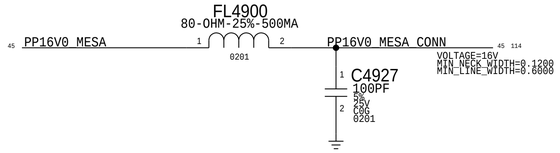
MOJAVE 16V BOOST





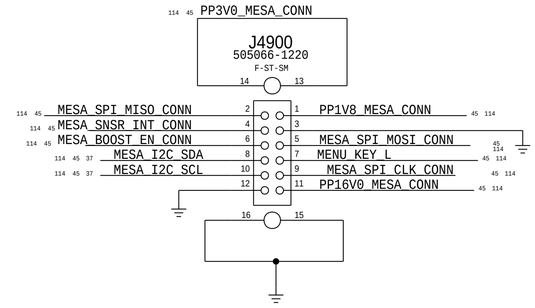
3.0V MESA

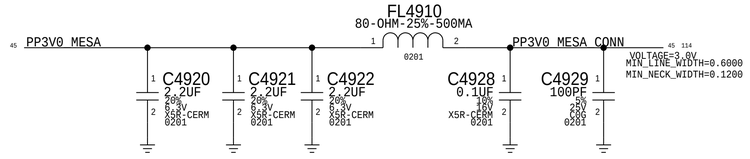




MESA FLEX CONNECTOR

Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB

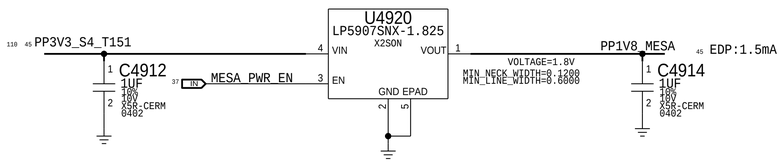


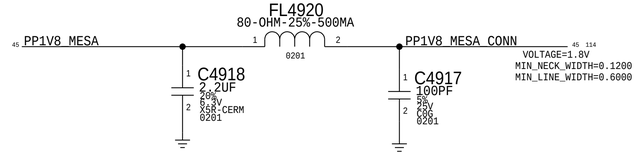


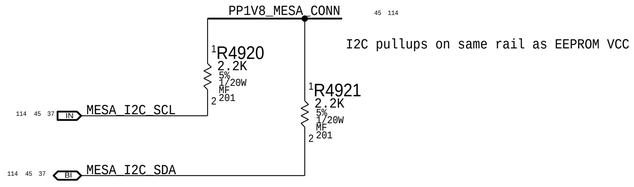
Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

1.8V MESA







BOM_COST_GROUP=T151

PAGE TITLE: MESA

Apple Inc.

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BRANCH: dvt-fab10
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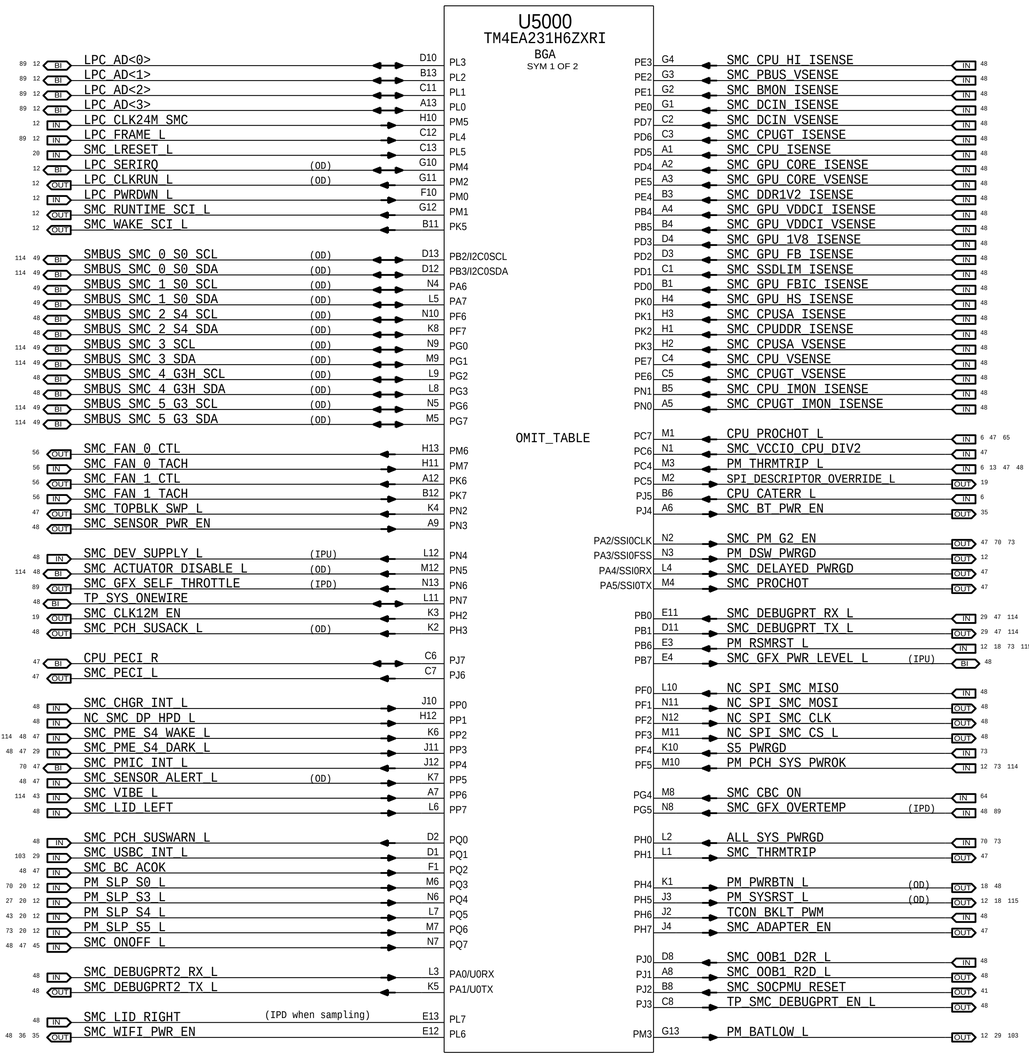

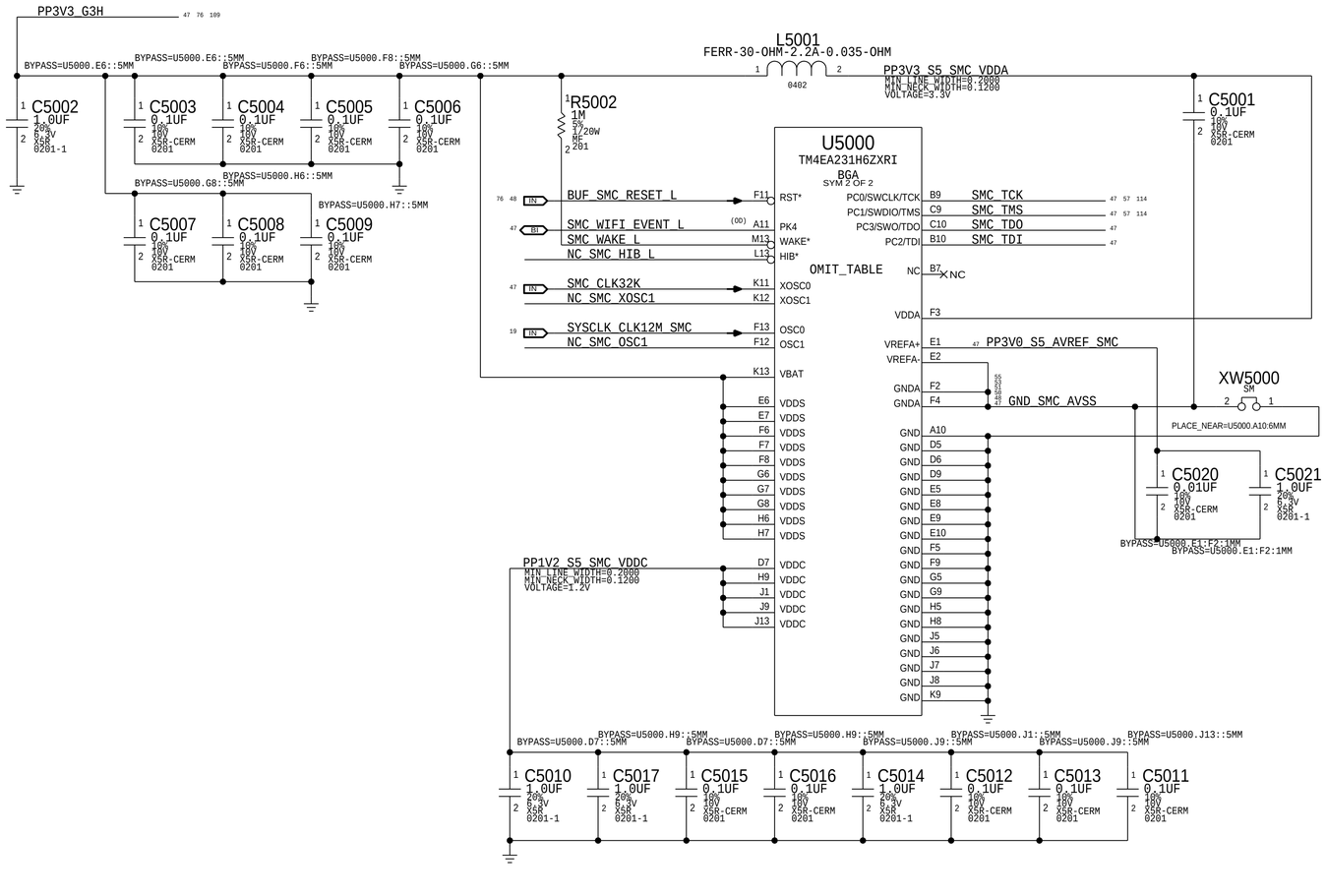

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

BOM_COST_GROUP=SMC

PAGE TITLE
SMC

Apple Inc.

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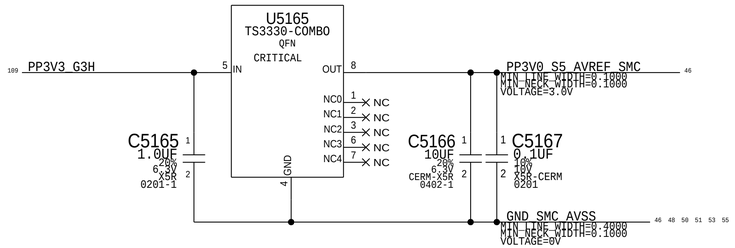
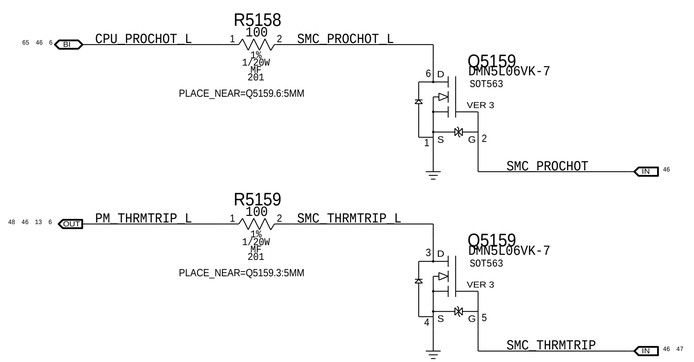
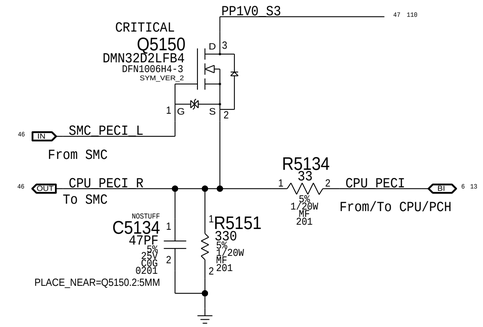
SMC AVREF Supply



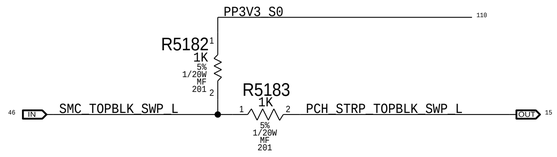
PROCHOT/THRMTRIP Support

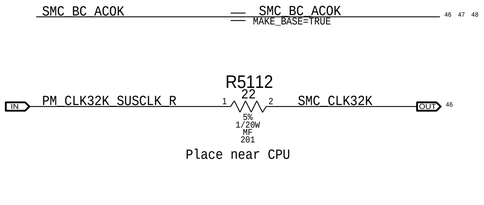


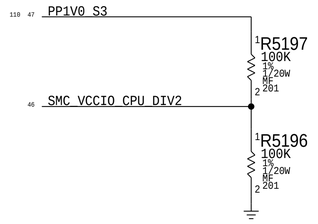
PECI Support

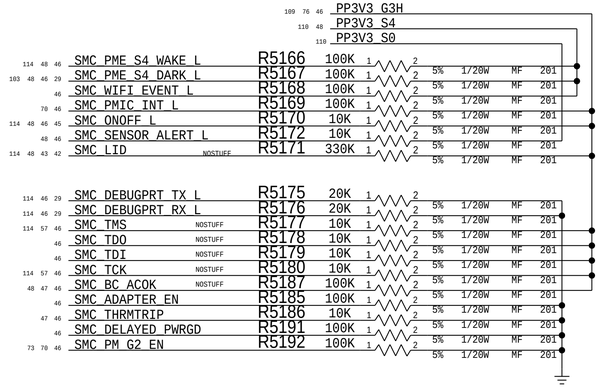


Top-Block Swap









BOM_COST_GROUP=SMC

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=11/19/2015

PAGE TITLE: SMC Shared Support

Apple Inc.

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SMC12 ADC Assignments

46	SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE		50
46	SMC_PBUS_VSENSE	SMC_PBUS_VSENSE		50
46	SMC_BMON_ISENSE	SMC_BMON_ISENSE		50
46	SMC_DCIN_ISENSE	SMC_DCIN_ISENSE		50
46	SMC_DCIN_VSENSE	SMC_DCIN_VSENSE		50
46	SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE		53
46	SMC_CPU_ISENSE	SMC_CPU_ISENSE		51
46	SMC_GPU_CORE_ISENSE	SMC_GPU_CORE_ISENSE		55
46	SMC_GPU_CORE_VSENSE	SMC_GPU_CORE_VSENSE		55
46	SMC_DDR1V2_ISENSE	SMC_DDR1V2_ISENSE		51
46	SMC_GPU_VDDCI_ISENSE	SMC_GPU_VDDCI_ISENSE		55
46	SMC_GPU_VDDCI_VSENSE	SMC_GPU_VDDCI_VSENSE		55
46	SMC_GPU_1V8_ISENSE	SMC_GPU_1V8_ISENSE		55
46	SMC_GPU_FB_ISENSE	SMC_GPU_FB_ISENSE		55
46	SMC_SSDLIM_ISENSE	SMC_SSDLIM_ISENSE		53
46	SMC_GPU_FBIC_ISENSE	SMC_GPU_FBIC_ISENSE		55
46	SMC_GPU_HS_ISENSE	SMC_GPU_HS_ISENSE		55
46	SMC_CPUSA_ISENSE	SMC_CPUSA_ISENSE		53
46	SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE		51
46	SMC_CPUSA_VSENSE	SMC_CPUSA_VSENSE		53
46	SMC_CPU_VSENSE	SMC_CPU_VSENSE		55
46	SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE		55
46	SMC_CPU_IMON_ISENSE	SMC_CPU_IMON_ISENSE		51 55
46	SMC_CPUGT_IMON_ISENSE	SMC_CPUGT_IMON_ISENSE		53 55

SMC12 Pin Assignments

46	SMC_GFX_PWR_LEVEL_L	SMC_GFX_PWR_LEVEL_L	89
46	TP_SYS_ONEWIRE	TP_SYS_ONEWIRE	
46	TP_SMC_DEBUGPRT_EN_L	TP_SMC_DEBUGPRT_EN_L	
46	NC_SMC_DP_HPD_L	NC_SMC_DP_HPD_L	

47 46 13 6 PM_THRMTRIP_L

CRITICAL
O5290
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

SMC_GFX_OVERTEMP — IN 46 89

46	NC_SPI_SMC_MISO	NC_SPI_SMC_MISO	115 TRUE
46	NC_SPI_SMC_MOSI	NC_SPI_SMC_MOSI	115 TRUE
46	NC_SPI_SMC_CLK	NC_SPI_SMC_CLK	115 TRUE
46	NC_SPI_SMC_CS_L	NC_SPI_SMC_CS_L	115 TRUE

46 OUT	SMC_PCH_SUSWARN_L	SMC_PCH_SUSWARN_L	IN 12
46 IN	SMC_PCH_SUSACK_L	SMC_PCH_SUSACK_L	OUT 12

48 46	SMC_SENSOR_PWR_EN	SMC_SENSOR_PWR_EN	74
		SMC_SENSOR_PWR_EN	50

46 18	PM_PWRBTN_L	PM_PWRBTN_L	12
		SMC_BC_ACOK	64
47 46	SMC_BC_ACOK	SMC_BC_ACOK	50
49	SMBUS_SMC_4_G3H_SCL	SMBUS_SMC_4_G3H_SCL	46
49	SMBUS_SMC_4_G3H_SDA	SMBUS_SMC_4_G3H_SDA	46
49	SMBUS_SMC_2_S4_SCL	SMBUS_SMC_2_S4_SCL	46
49	SMBUS_SMC_2_S4_SDA	SMBUS_SMC_2_S4_SDA	46
46	SMC_OOB1_D2R_L	SMC_OOB1_D2R_L	77 80 114
46	SMC_OOB1_R2D_L	SMC_OOB1_R2D_L	77 80 114

114 46	SMC_ACTUATOR_DISABLE_L	SMC_ACTUATOR_DISABLE_L	43
46	SMC_CHGR_INT_L	SMC_CHGR_INT_L	64

Debug Power "Buttons"

PLACE_SIDE=TOP
SILK_PART=PWR_BTN
R5226
RES
0603-NSP
BOMOPTION=OMIT

SMC_ONOFF_L — OUT 45 46 47 48 114

SW5200
EVQPUA02K
BOMOPTION=DBG_BTN
SILK_PART=PWR_BTN
PLACE_SIDE=BOTTOM

Debug RESET "Buttons"

BOMOPTION=DBG_BTN
PLACE_SIDE=BOTTOM
SILK_PART=RESET_BTN
CRITICAL
SW5227
SOX-152HNT
SM

SMC_RESET_L — OUT 29 57 64 76 114

Thermal Alerts

NOSTUFF

51 IN	SMC_CPUHI_COMP_ALERT_L	R5217 100	
54 IN	CPUTHMSNS_THM_L	R5216 100	CPUTHRM_THRM:SMC
54 IN	CPUTHMSNS_ALERT_L	R5214 100	CPUTHRM_ALRT:SMC
54 IN	TBTTHMSNS_X_THM_L	R5220 100	TBTTHRM_THRM:SMC
54 IN	TBTTHMSNS_T_THM_L	R5221 100	TBTTHRM_THRM:SMC
54 IN	TBTTHMSNS_X_ALERT_L	R5210 100	TBTTHRM_ALRT:SMC
54 IN	TBTTHMSNS_T_ALERT_L	R5211 100	TBTTHRM_ALRT:SMC

All: 5% 1/20W MF 201

SMC_SENSOR_ALERT_L — OUT 46 47

S4 SMC Wake Sources

43 IN	SMC_PME_S4_WAKE_L	SMC_PME_S4_WAKE_L	OUT 46 47 114
35 IN	SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L	29 46 47 103

MAKE_BASE=TRUE

BYPASS=U5256.5::5MM
PP3V3_G3H — 43 109

R5256 100K 5% 1/20W MF 201
C5256 0.1UF 10% 10V X5R-CERM 0201

SMC_LSOC_RST_L — IN 114 43
SMC_ONOFF_L — IN 114 48 47 46 45

U5256
SN74LVC1G02
SOT553-5
CRITICAL

SMC_4FINGERS_RST — OUT 64

R5258 0 5% 1/20W MF 201
PP3V3_G3H — 109 48
LID_FEATURE_ON
SMC_LID_LEFT — OUT 46

BYPASS=U5255.6::5MM
C5255 0.1UF 10% 10V X5R-CERM 0201

R5257 0 5% 1/20W MF 201
LID_FEATURE_OFF

SMC_LID_LEFT_R — 48
SMC_LID_RIGHT — 48 46

U5255
74LVC1G32
SOT891
CRITICAL

R5255 10K 5% 1/20W MF 201
SMC_LID_R
SMC_LID — OUT 42 43 47 114

NC

R5259 0 5% 1/20W MF 201
SMC_DEV_SUPPLY_L — 46
SMC_DEV_SUPPLY_R_L — 114

R5260 10 5% 1/20W MF 201
TCON_BKLT_PWM — 46
BKLT_PWM_TCON2MLB — 76 114

C5257 3300PF 10% 16V X7R-CERM 0201
NOSTUFF

Hall Effect Pads - Left

J5250
AMR-MLB-X502
SM
OMIT_TABLE

HALL_SENSOR_LEFT
PP3V3_G3H — 48 109

C5250 1000PF 10% 16V X7R-1 0201
NOSTUFF

R5252 10K 5% 1/20W MF 201
SMC_LID_LEFT_R — 48

Hall Effect Pads - Right

J5260
AMR-MLB-X502
SM
OMIT_TABLE

HALL_SENSOR_RIGHT
PP3V3_G3H — 48 109

C5260 1000PF 10% 16V X7R-1 0201
NOSTUFF

R5253 10K 5% 1/20W MF 201
SMC_LID_RIGHT — OUT 46 48

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC
CPUTHRM:ALRT	CPUTHRM_ALRT:SMC

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

110 47 PP3V3_S4

R5274 100K 5% 1/20W MF 201
PLACE_SIDE=BOTTOM
NOSTUFF
R5273 10K 5% 1/20W MF 201

R5275 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_TX_L — 46
WLAN_UART_RX — 35

PLACE_SIDE=BOTTOM
NOSTUFF
R5276 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_RX_L — 46
WLAN_UART_TX — 35

PP3V3_G3H — 109

R5280 100K 5% 1/20W MF 201
PLACE_SIDE=BOTTOM
R5281 10K 5% 1/20W MF 201

R5277 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_R_TX

R5278 0 5% 1/20W MF 0201
PLACE_SIDE=BOTTOM
SMC_DEBUGPRT2_R_RX

TP-P6 A TP5200
TP-P6 A TP5201

46 36 35 SMC_WIFI_PWR_EN — R5295 10K 5% 1/20W MF 201 NOSTUFF
48 46 SMC_SENSOR_PWR_EN — R5294 10K 5% 1/20W MF 201 NOSTUFF

BUF_SMC_RESET_L — 46 76

NOSTUFF
C5270 1000PF 10% 16V X7R-CERM 0201

GND_SMC_AVSS — 46 47 50 51 53 55

BOM_COST_GROUP=SMC

PAGE TITLE: SMC Project Support

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REVISION: 10.0.0
BRANCH: dvt-fab10
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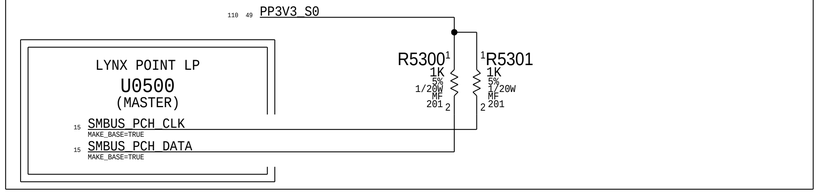
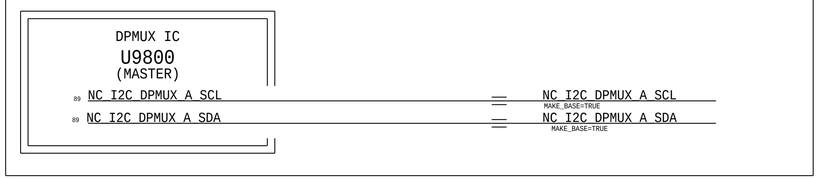
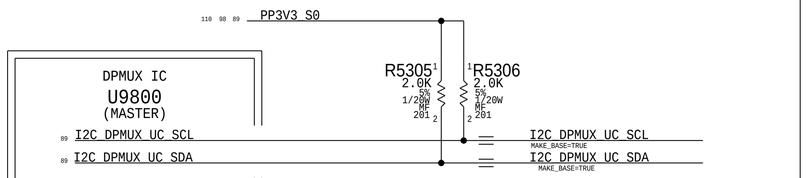
LYNX POINT LP S0 "SMBus 0" Connections



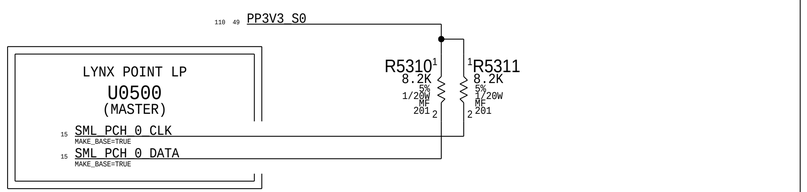
DPMUX Connections



DPMUX Connections



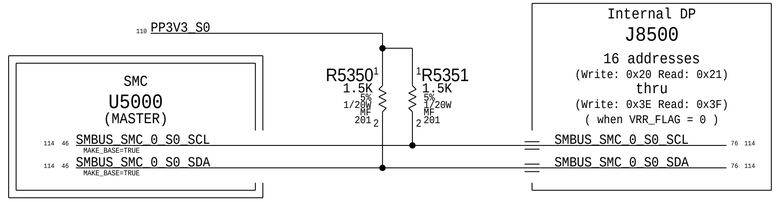
LYNX POINT LP S0 "SMLink 0" Connections



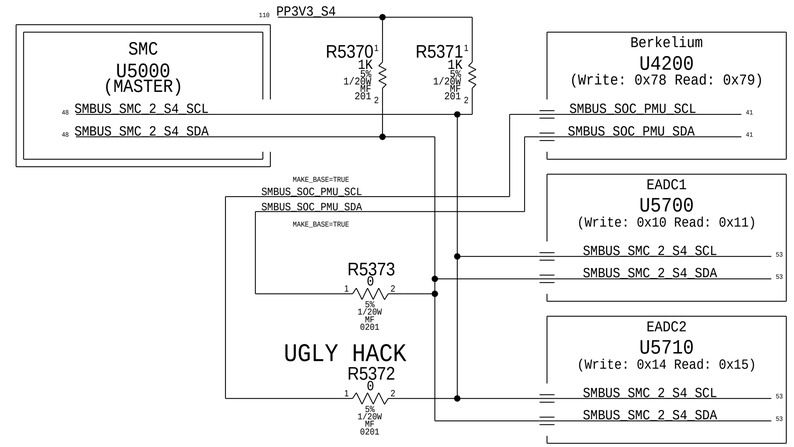
LYNX POINT LP S0 "SMLink 1" Connections

SMLink 1 is slave port to
access PCH.

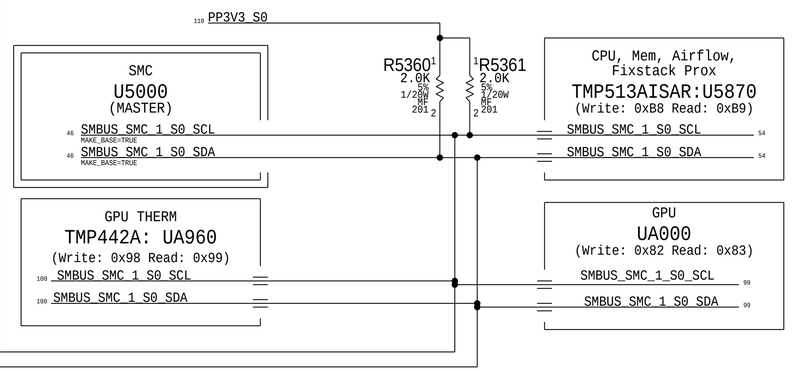
SMC SMBus "0" S0 Connections



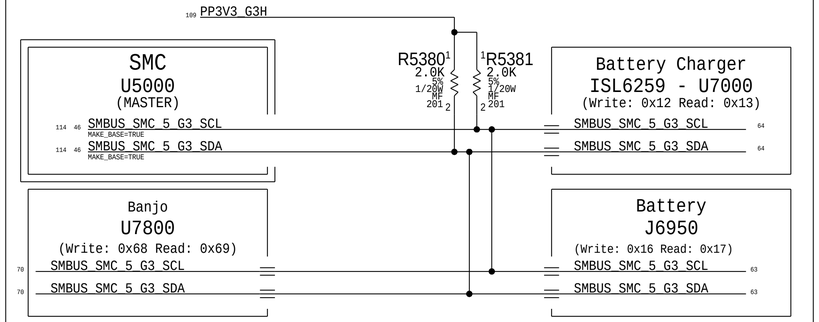
SMC SMBus "2" S4 Connections



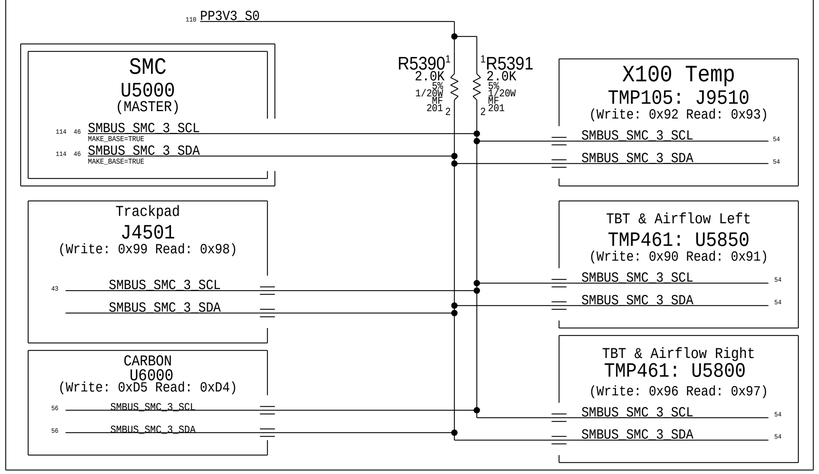
SMC SMBus "1" S0 Connections



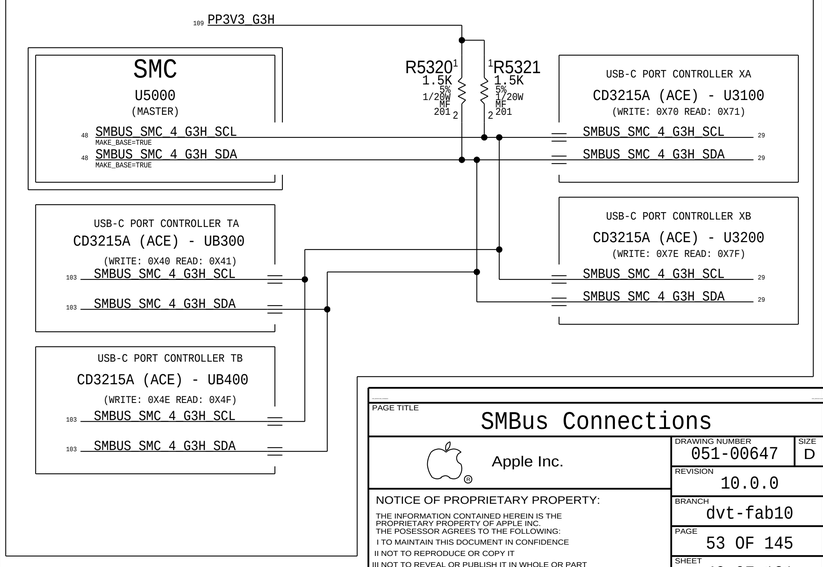
SMC SMBus "5" G3H Connections



SMC SMBus "3" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



BOM_COST_GROUP=SMC

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER	051-00647
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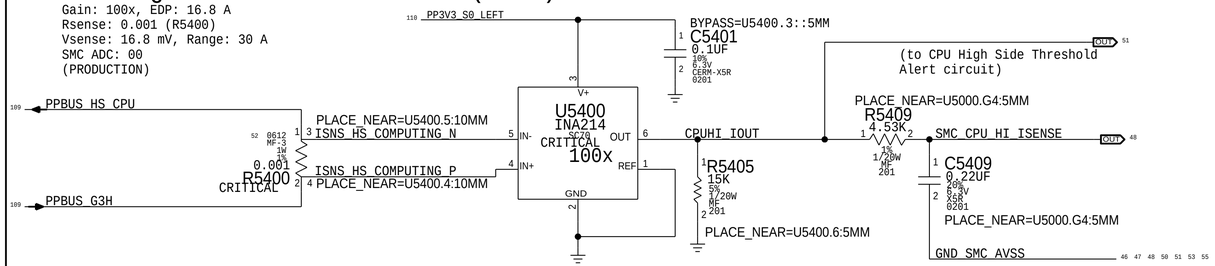
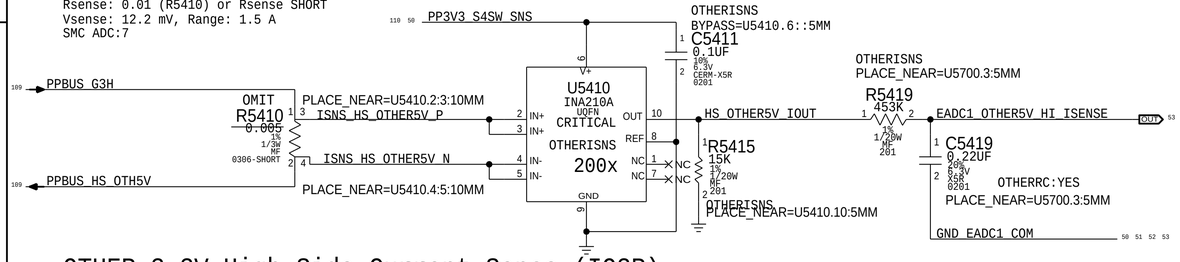
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 16.8 A
Rsense: 0.001 (R5400)
Vsense: 16.8 mV, Range: 30 A
SMC ADC: 00
(PRODUCTION)



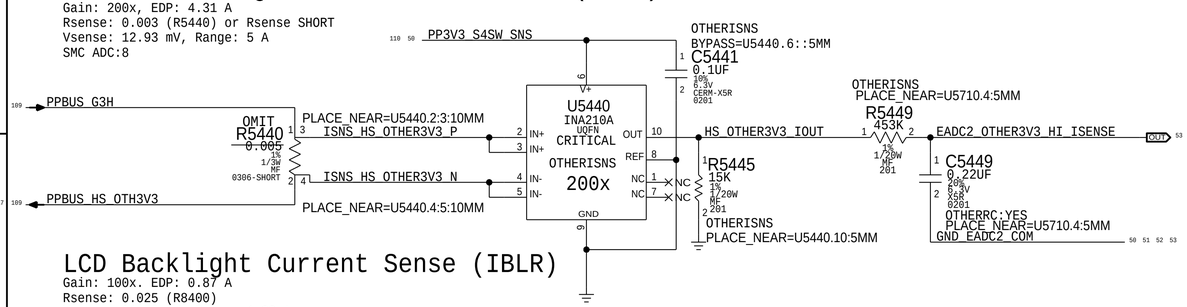
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
Rsense: 0.01 (R5410) or Rsense SHORT
Vsense: 12.2 mV, Range: 1.5 A
SMC ADC:7



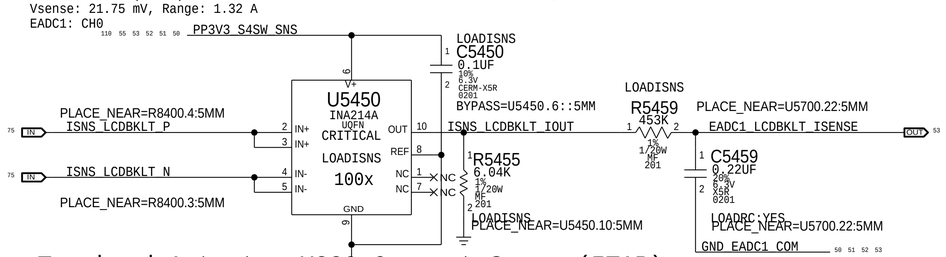
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12.93 mV, Range: 5 A
SMC ADC:8



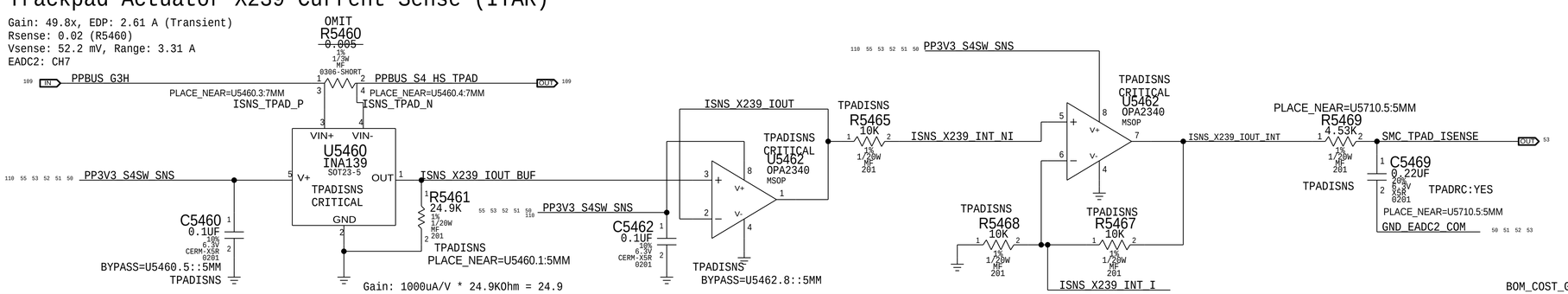
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 0.87 A
Rsense: 0.025 (R8400)
Vsense: 21.75 mV, Range: 1.32 A
EADC1: CH0



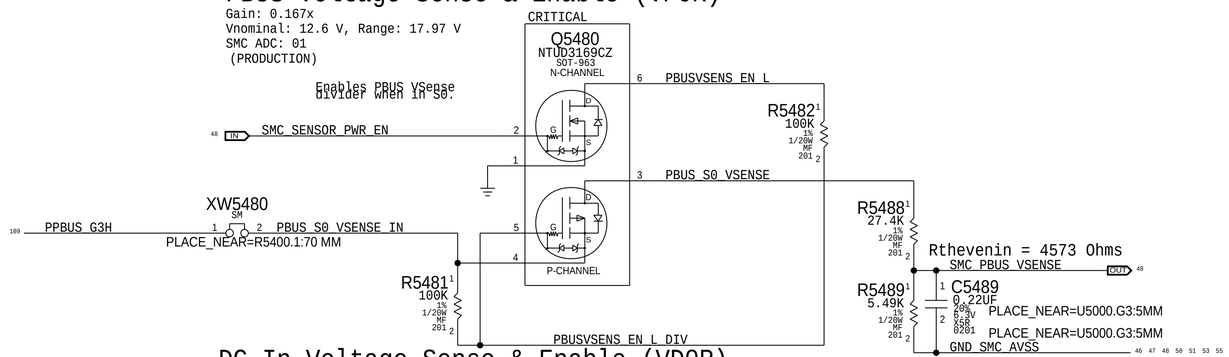
Trackpad Actuator X239 Current Sense (ITAR)

Gain: 49.8x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 52.2 mV, Range: 3.31 A
EADC2: CH7



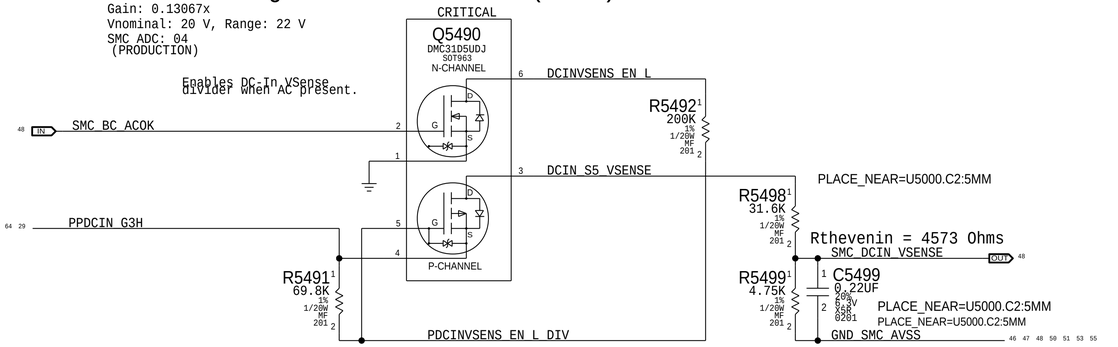
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 17.97 V
SMC ADC: 01
(PRODUCTION)



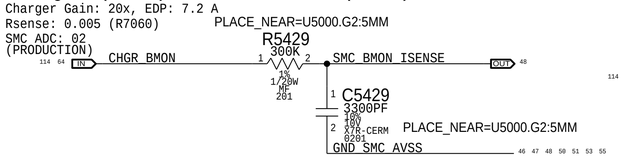
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13067x
Vnominal: 20 V, Range: 22 V
SMC ADC: 04
(PRODUCTION)



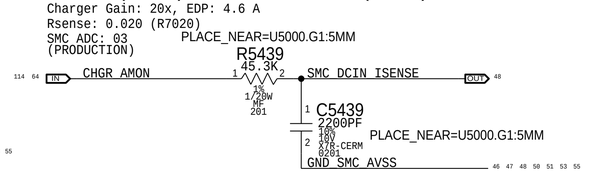
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
Rsense: 0.005 (R7060)
SMC ADC: 02
(PRODUCTION)



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 03
(PRODUCTION)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: High Side

Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
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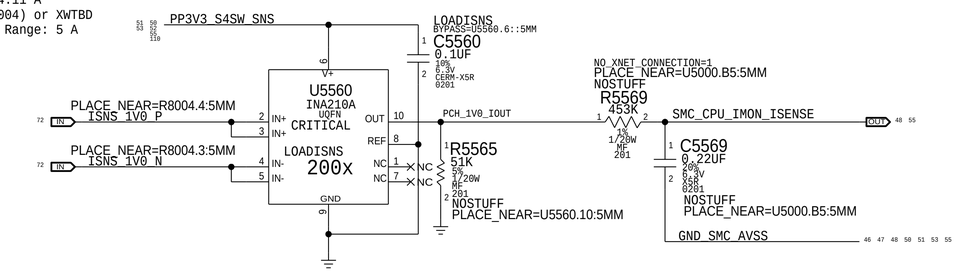
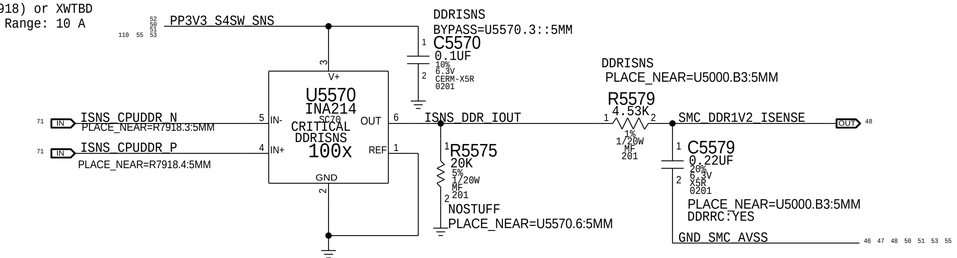
PCH 1.0V Current Sense (ISCC)

Gain: 200x, EDP: 4.11 A
Rsense: 0.003 (R8004) or XWTBD
Vsense: 11.33 mV, Range: 5 A
SMC ADC: 22



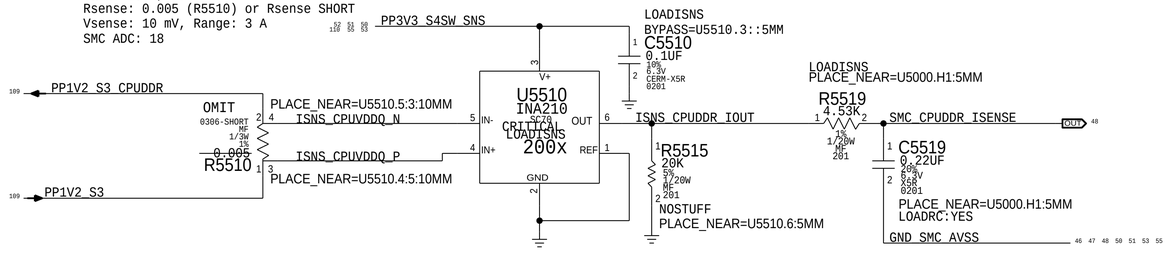
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9.01 A
Rsense: 0.003 (R7918) or XWTBD
Vsense: 27.03 mV, Range: 10 A
SMC ADC: 09



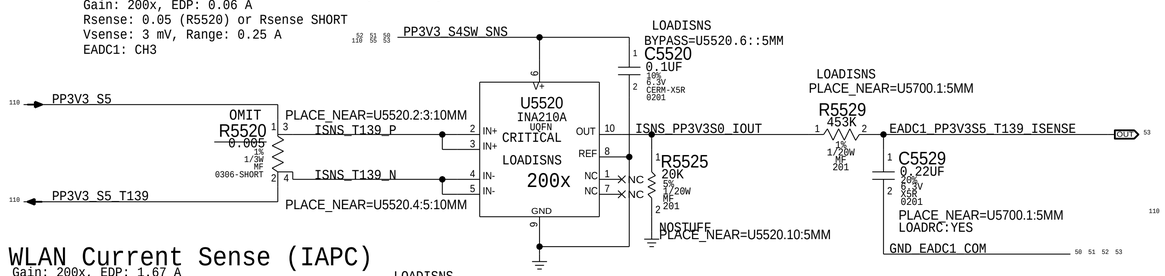
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 10 mV, Range: 3 A
SMC ADC: 18



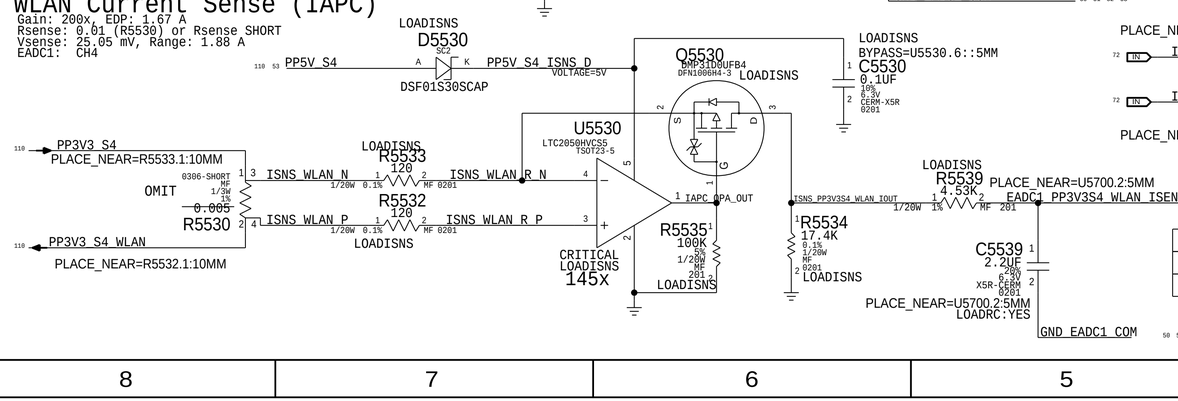
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC1: CH3



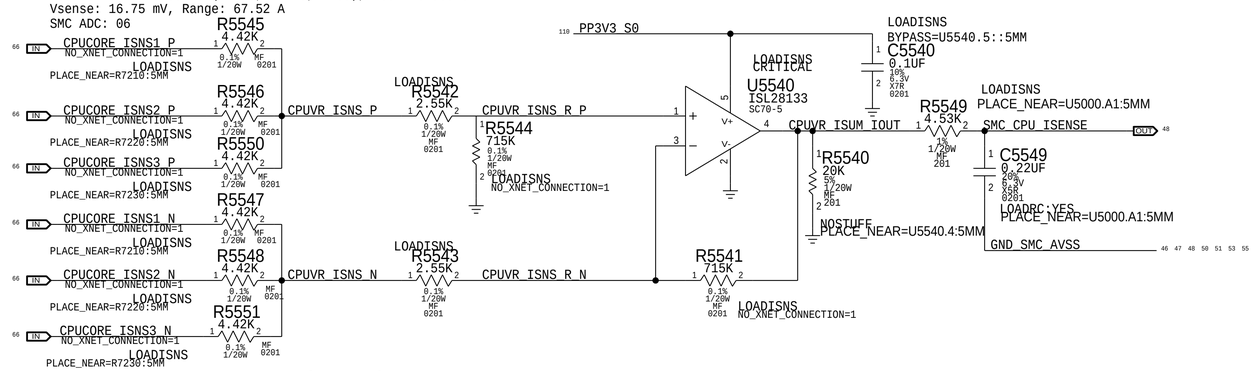
WLAN Current Sense (IAPC)

Gain: 200x, EDP: 1.67 A
Rsense: 0.01 (R5530) or Rsense SHORT
Vsense: 25.05 mV, Range: 1.88 A
EADC1: CH4



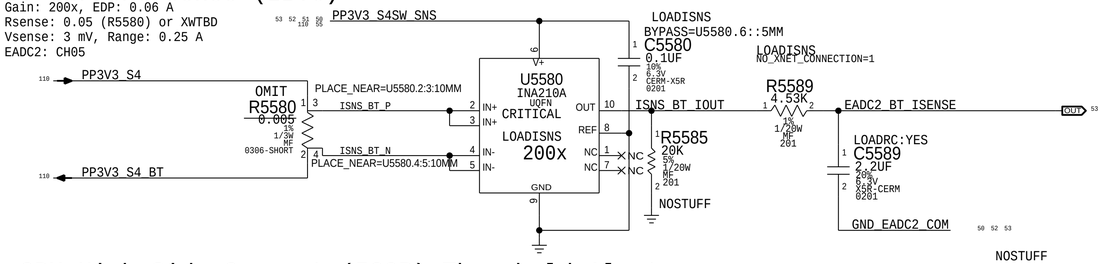
CPU Fixed Current Sense (ICAC)

Gain: 177.71x, EDP: 67 A
Rsense: 3x of 0.00075 (R7210, R7220,R7230), Rsum: 0.00025
Vsense: 16.75 mV, Range: 67.52 A
SMC ADC: 06



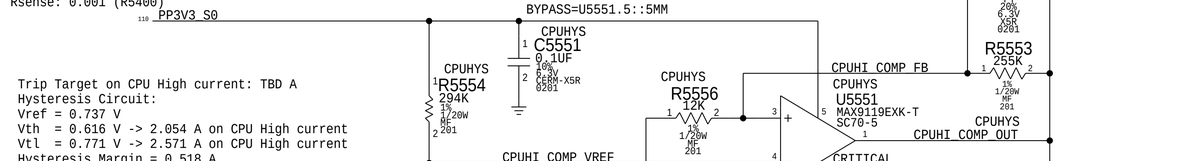
BT Current Sense (IBTC)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5580) or XWTBD
Vsense: 3 mV, Range: 0.25 A
EADC2: CH05



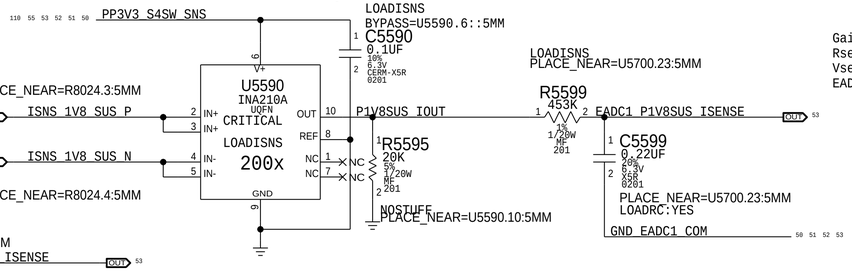
CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.001 (R5400)



Trip Target on CPU High current: TBD A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A

1.8V Current Sense (I18C)



Gain: 200x, EDP: 0.7 A
Rsense: 0.025 (R8024) or Rsense SHORT
Vsense: 17.5 mV, Range: 0.6 A
EADC1: CH1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	6	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5519,C5529,C5539,C5549,C5589,C5599		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Load Side

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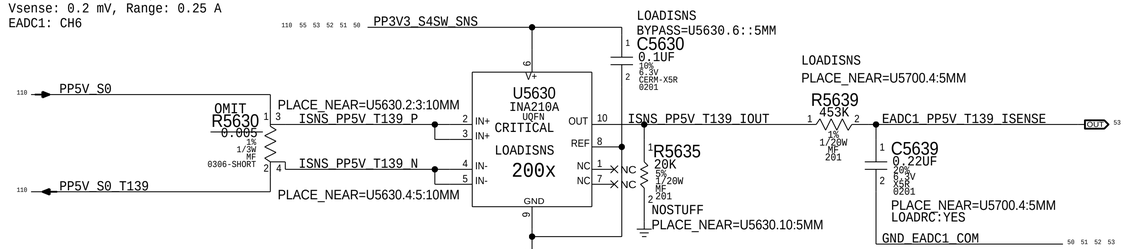
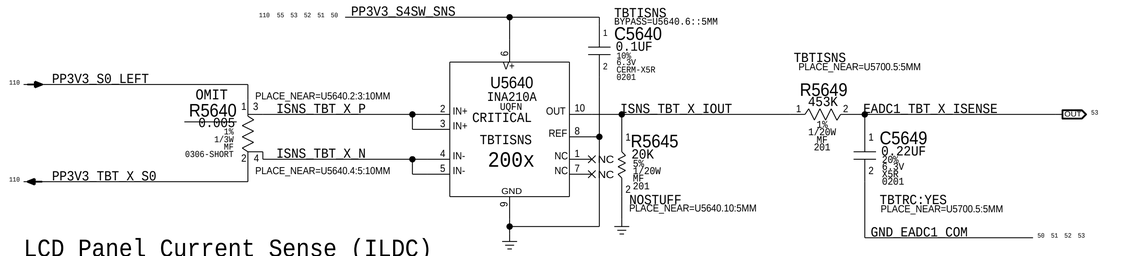
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



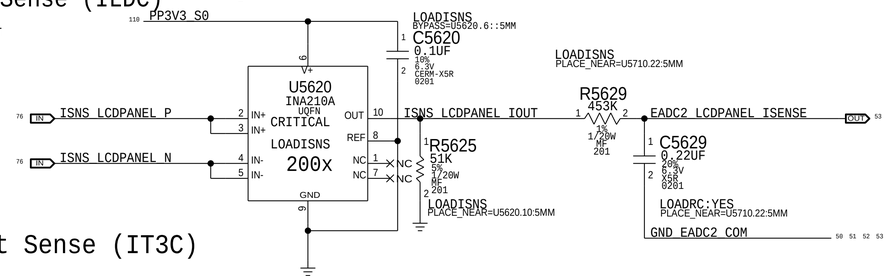
Thunderbolt TBT LEFT Current Sense (IULC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



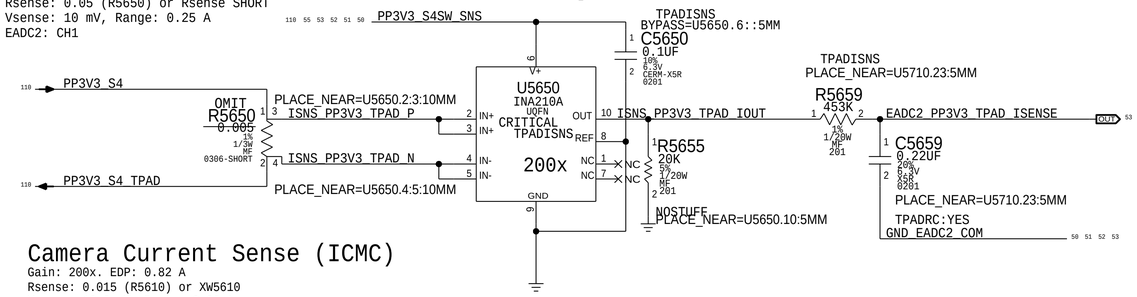
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



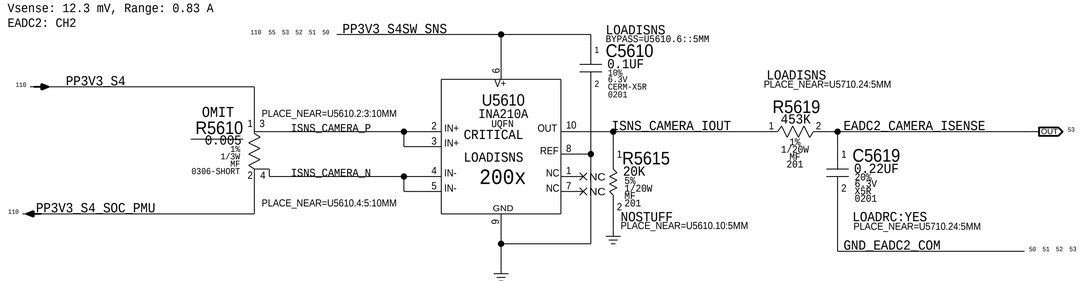
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

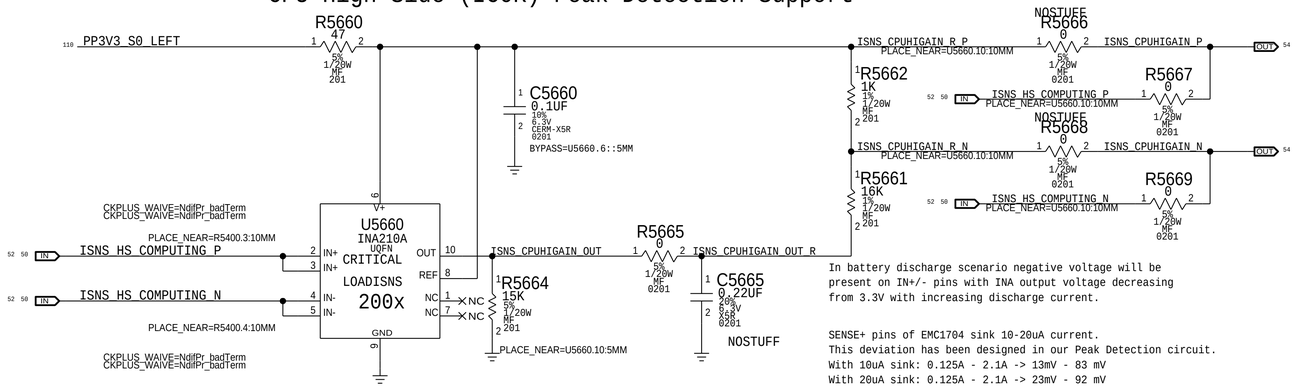


Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

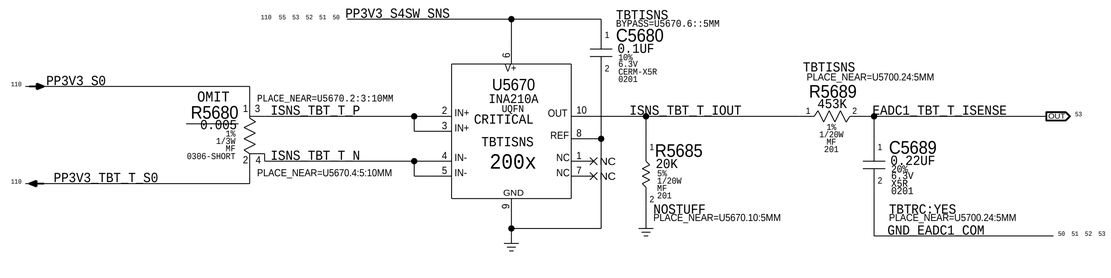


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

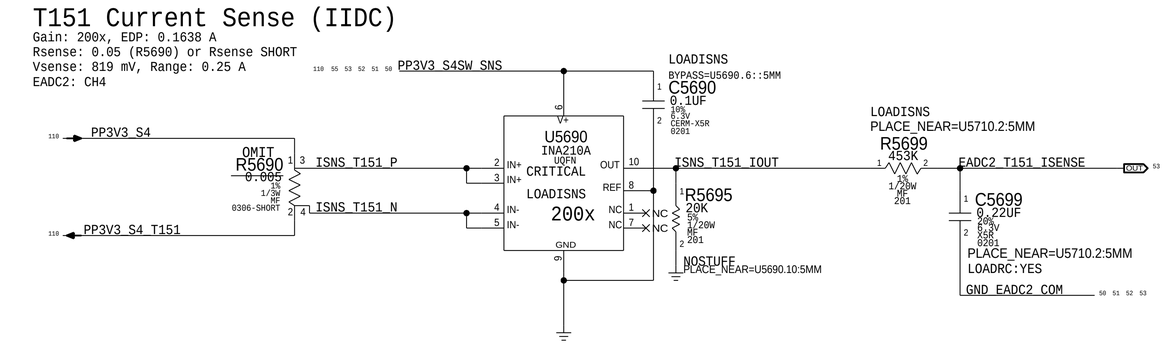
Thunderbolt TBT RIGHT Current Sense (IURC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5680) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



T151 Current Sense (IIDC)

Gain: 200x, EDP: 0.1638 A
Rsense: 0.05 (R5690) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5639,C5699		LOADRC:NO
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649,C5689		TBTRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5659		TPADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended

Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
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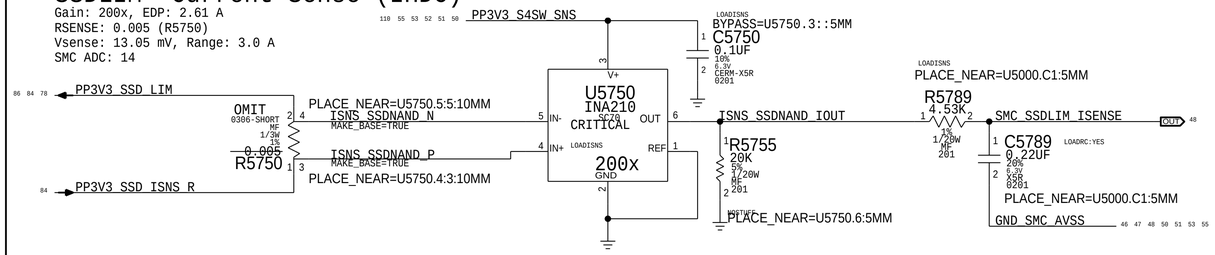
SHEET: 52 OF 121

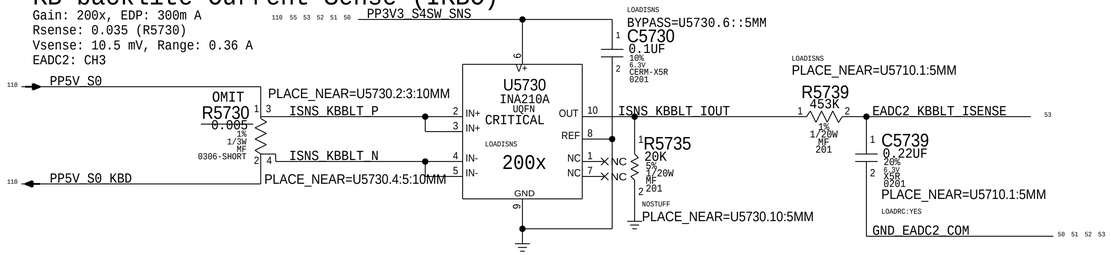
SSDLIM Current Sense (IHDC)

Gain: 200x, EDP: 2.61 A
RSENSE: 0.005 (R5750)
Vsense: 13.05 mV, Range: 3.0 A
SMC ADC: 14



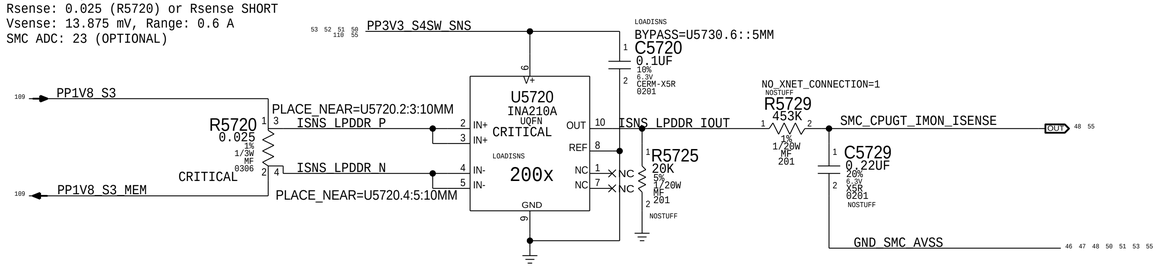
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



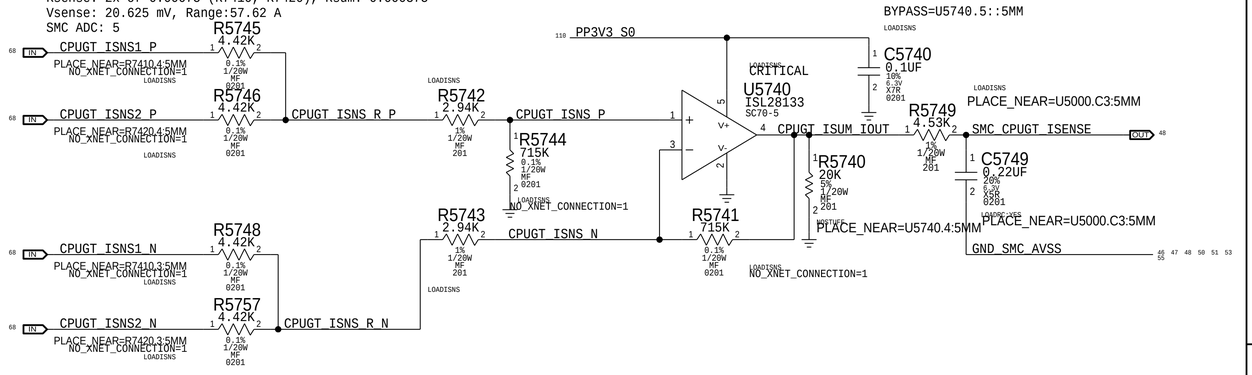
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 23 (OPTIONAL)



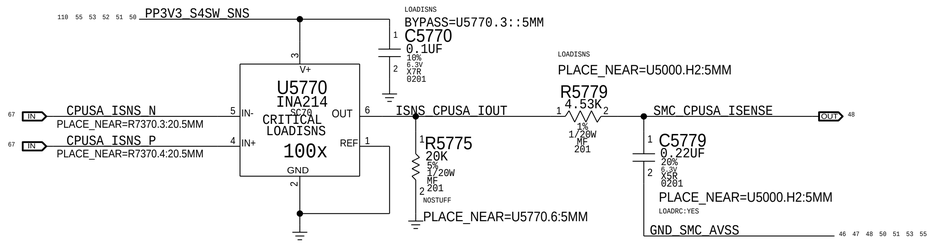
CPU GT Current Sense (ICTC)

Gain: 202.93x, EDP: 55 A
Rsense: 2x of 0.00075 (R7410, R7420), Rsum: 0.000375
Vsense: 20.625 mV, Range:57.62 A
SMC ADC: 5



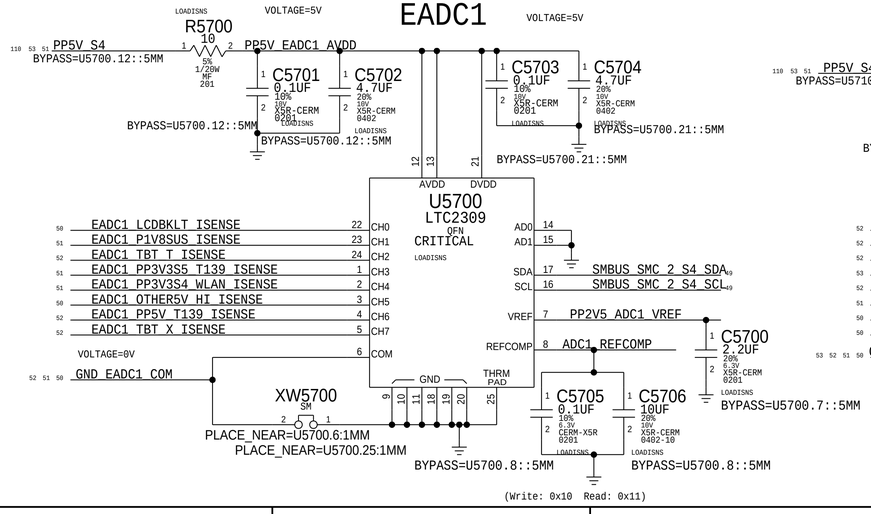
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 8 A
Rsense: 0.002 (R7570)
Vsense: 16 mV, Range: 7.5 A
SMC ADC: 17



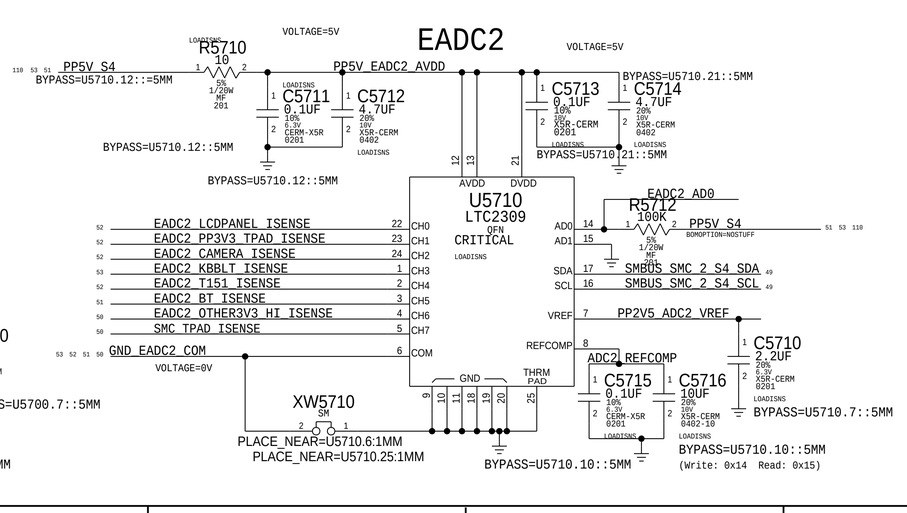
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5739,C5749,C5779,C5789		LOADRC:NO

EADC1



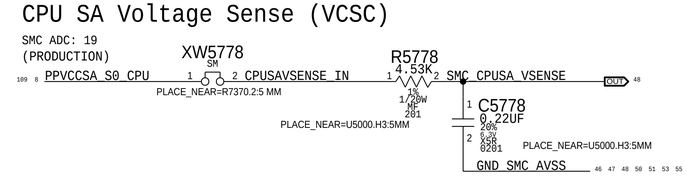
(Write: 0x10 Read: 0x11)

EADC2



(Write: 0x14 Read: 0x15)

CPU SA Voltage Sense (VCSC)



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended 2

Apple Inc.

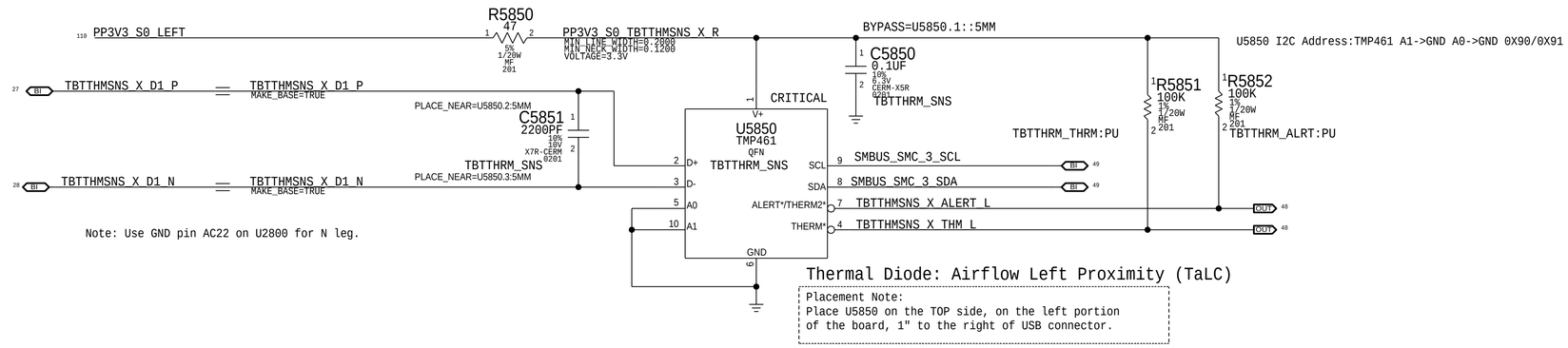
DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 57 OF 145
SHEET: 53 OF 121

Thermal Sensor A:
Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Left Proximity (TaLC)

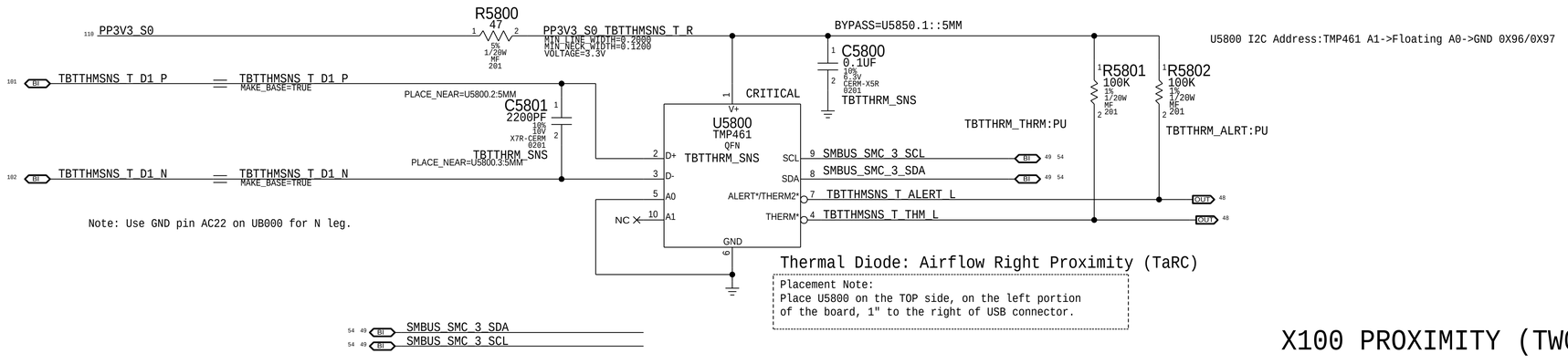
Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor C:
Thunderbolt Die, Air Flow Right

I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: TBT Die (TTRD)

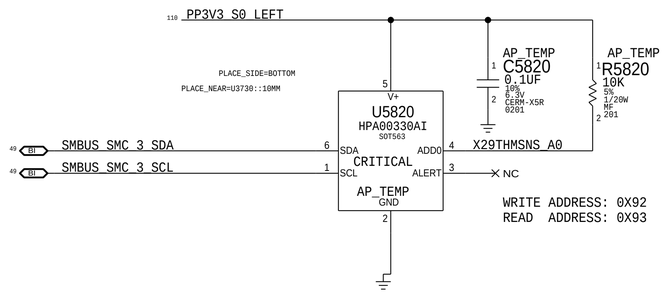
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

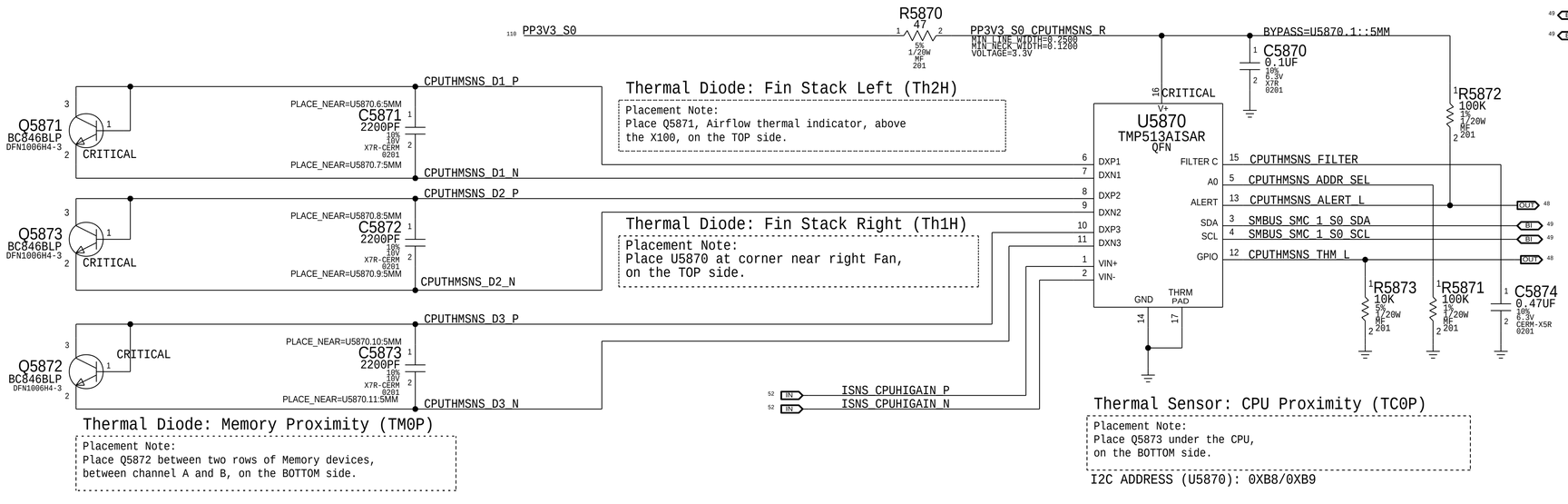
X100 PROXIMITY (TW0P)



Placement note:
PLACE U5820 ON BOTTOM NEAR X100

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0x98, I2C Read: 0x99



BOM_COST_GROUP=SENSORS

PAGE TITLE	Thermal Sensors
Apple Inc.	
DRAWING NUMBER	051-00647
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BRANCH	dvt-fab10
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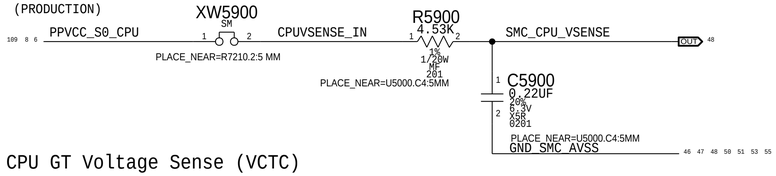
SENSORS: EXTENDER 3

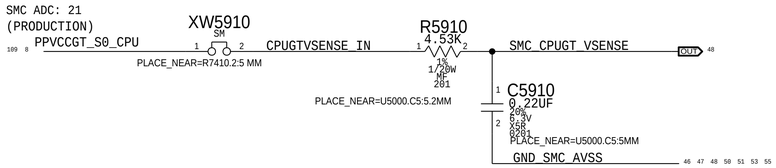
CPU Core Voltage Sense (VCAC)

SMC ADC: 20
(PRODUCTION)



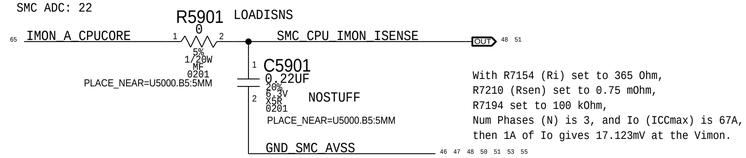
CPU GT Voltage Sense (VCTC)

SMC ADC: 21
(PRODUCTION)



CPU Core IMON Current Sense (ICAM)

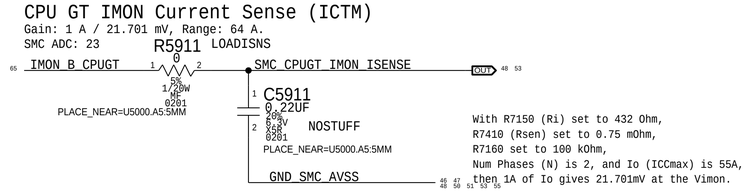
Gain: 1 A / 17.123 mV, Range: 67 A.
SMC ADC: 22



With R7154 (Ri) set to 365 Ohm,
R7210 (Rsen) set to 0.75 mOhm,
R7194 set to 100 kOhm,
Num Phases (N) is 3, and Io (ICCmax) is 67A,
then 1A of Io gives 17.123mV at the Vimon.

CPU GT IMON Current Sense (ICTM)

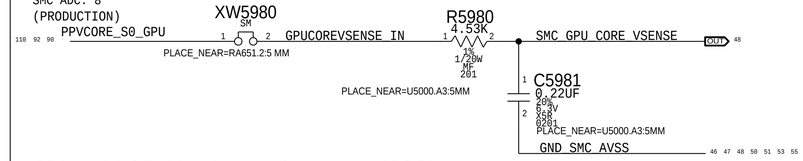
Gain: 1 A / 21.701 mV, Range: 64 A.
SMC ADC: 23



With R7150 (Ri) set to 432 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7160 set to 100 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 55A,
then 1A of Io gives 21.701mV at the Vimon.

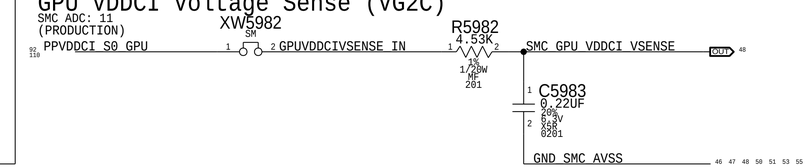
GPU CORE Voltage Sense (VG0C)

SMC ADC: 8
(PRODUCTION)



GPU VDDCI Voltage Sense (VG2C)

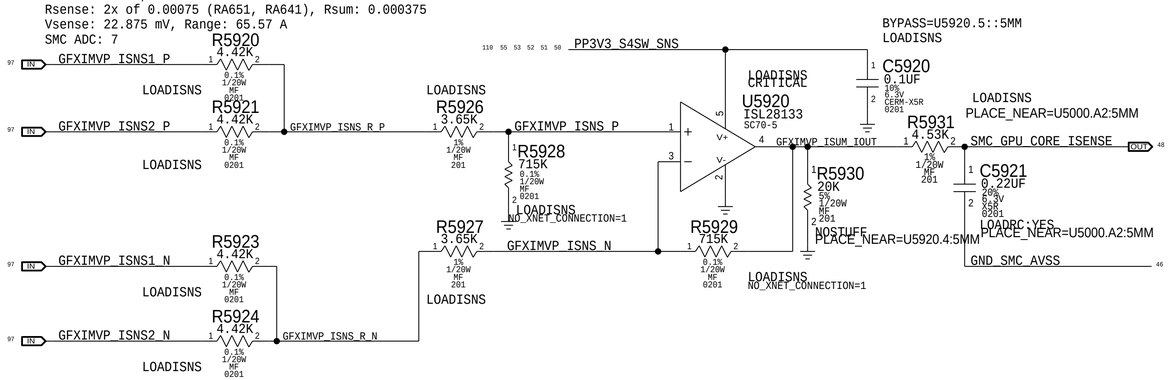
SMC ADC: 11
(PRODUCTION)



GPU SENSORS

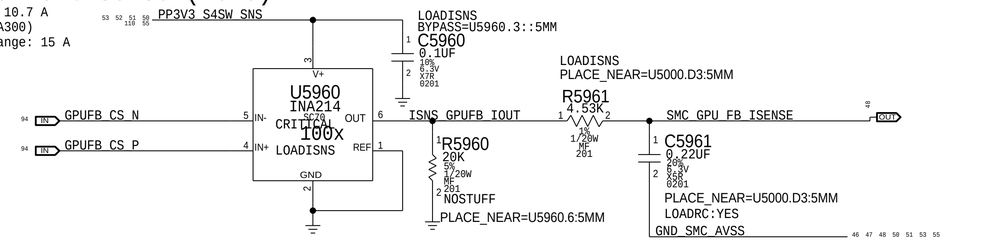
GPU CORE Current Sense (IG0C)

Gain: 122.01x, EDP: 64.2 A
Rsense: 2x of 0.00075 (RA651, RA641), Rsum: 0.000375
Vsense: 22.875 mV, Range: 65.57 A
SMC ADC: 7



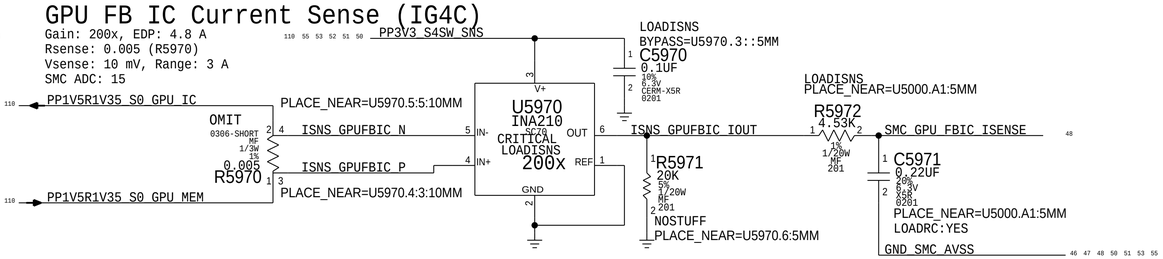
GPU FB Current Sense (IG1C)

Gain: 100x, EDP: 10.7 A
Rsense: 0.002 (RA300)
Vsense: 16 mV, Range: 15 A
SMC ADC: 13



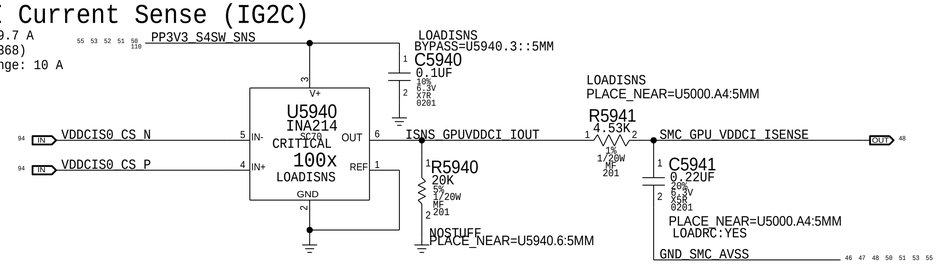
GPU FB IC Current Sense (IG4C)

Gain: 200x, EDP: 4.8 A
Rsense: 0.005 (R5970)
Vsense: 10 mV, Range: 3 A
SMC ADC: 15



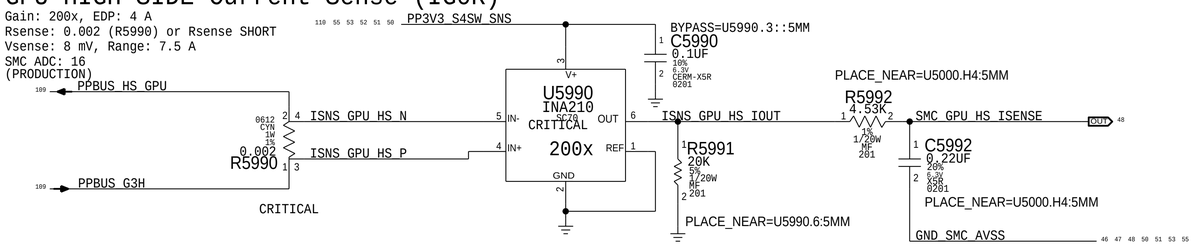
GPU VDDCI Current Sense (IG2C)

Gain: 100x, EDP: 9.7 A
Rsense: 0.003 (RA368)
Vsense: 24 mV, Range: 10 A
SMC ADC: 10



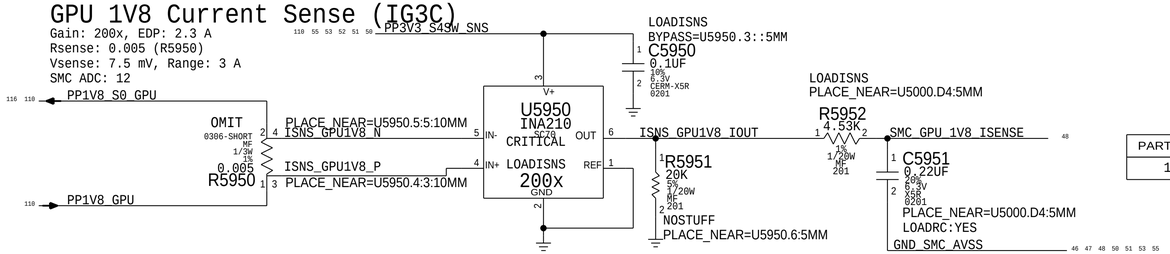
GPU HIGH SIDE Current Sense (IG0R)

Gain: 200x, EDP: 4 A
Rsense: 0.002 (R5990) or Rsense SHORT
Vsense: 8 mV, Range: 7.5 A
SMC ADC: 16
(PRODUCTION)



GPU 1V8 Current Sense (IG3C)

Gain: 200x, EDP: 2.3 A
Rsense: 0.005 (R5950)
Vsense: 7.5 mV, Range: 3 A
SMC ADC: 12



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5921,C5941,C5951,C5961,C5971		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE
Sensor Extended 3

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
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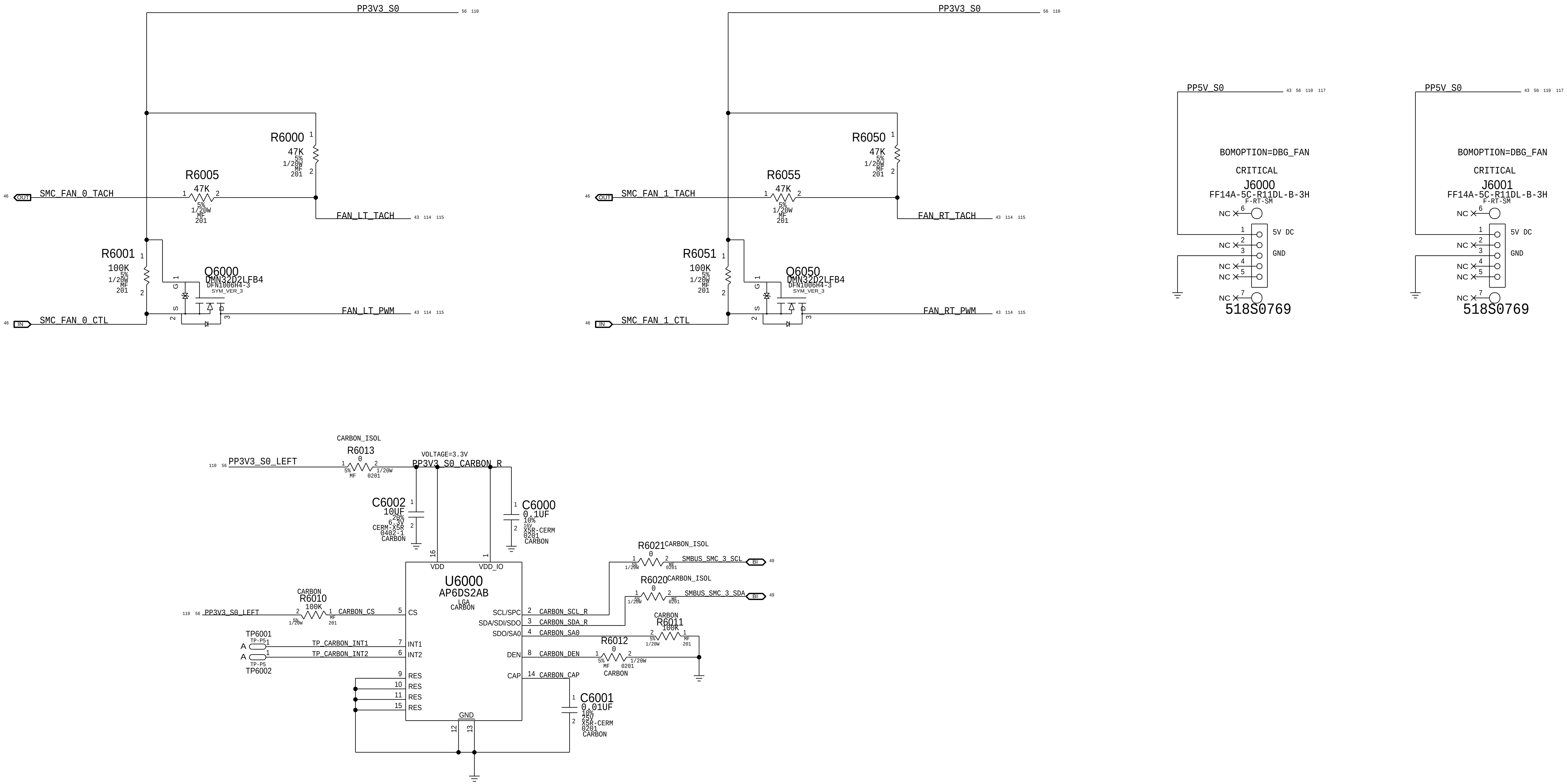
FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



BOM_COST_GROUP=FAN

PAGE TITLE: Fans

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

BRANCH: dvt-fab10

PAGE: 60 OF 145

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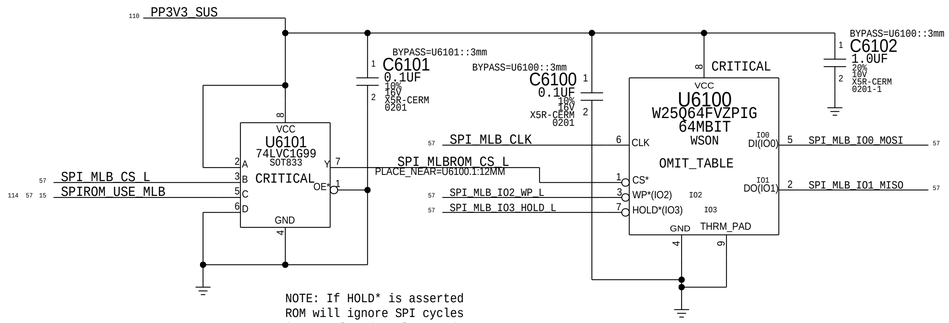
SPI ROM

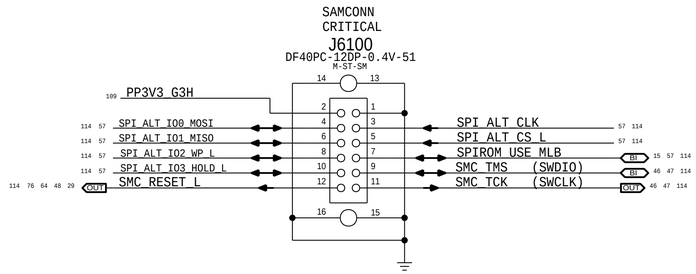
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

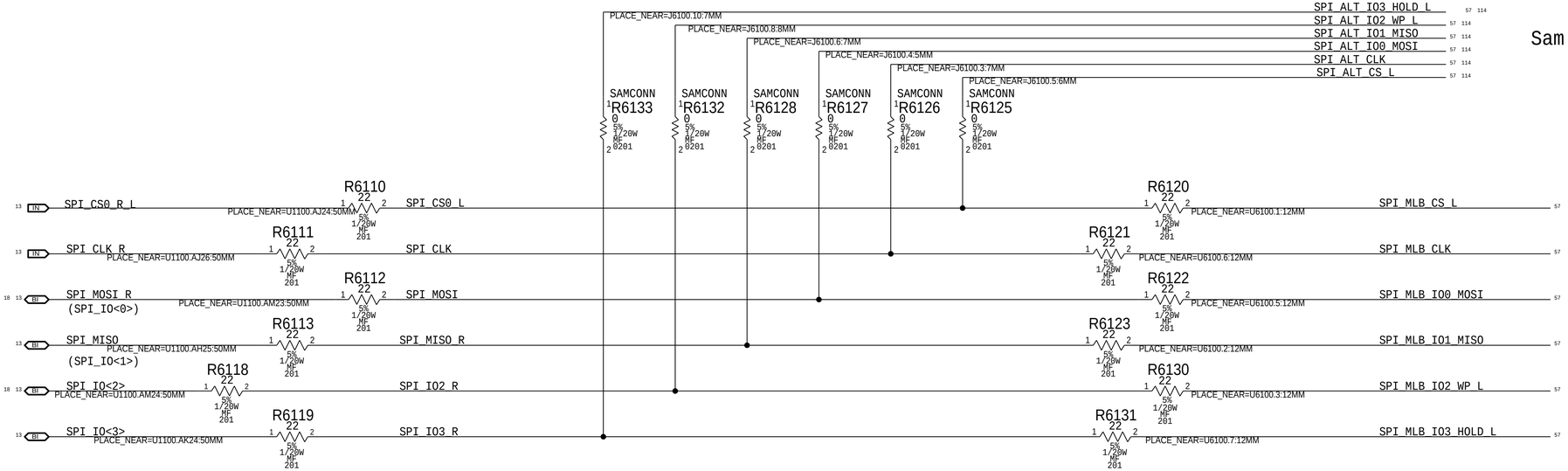
Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)

CPU Master



Sam Card ROM Slave

SPI ROM Slave

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE
SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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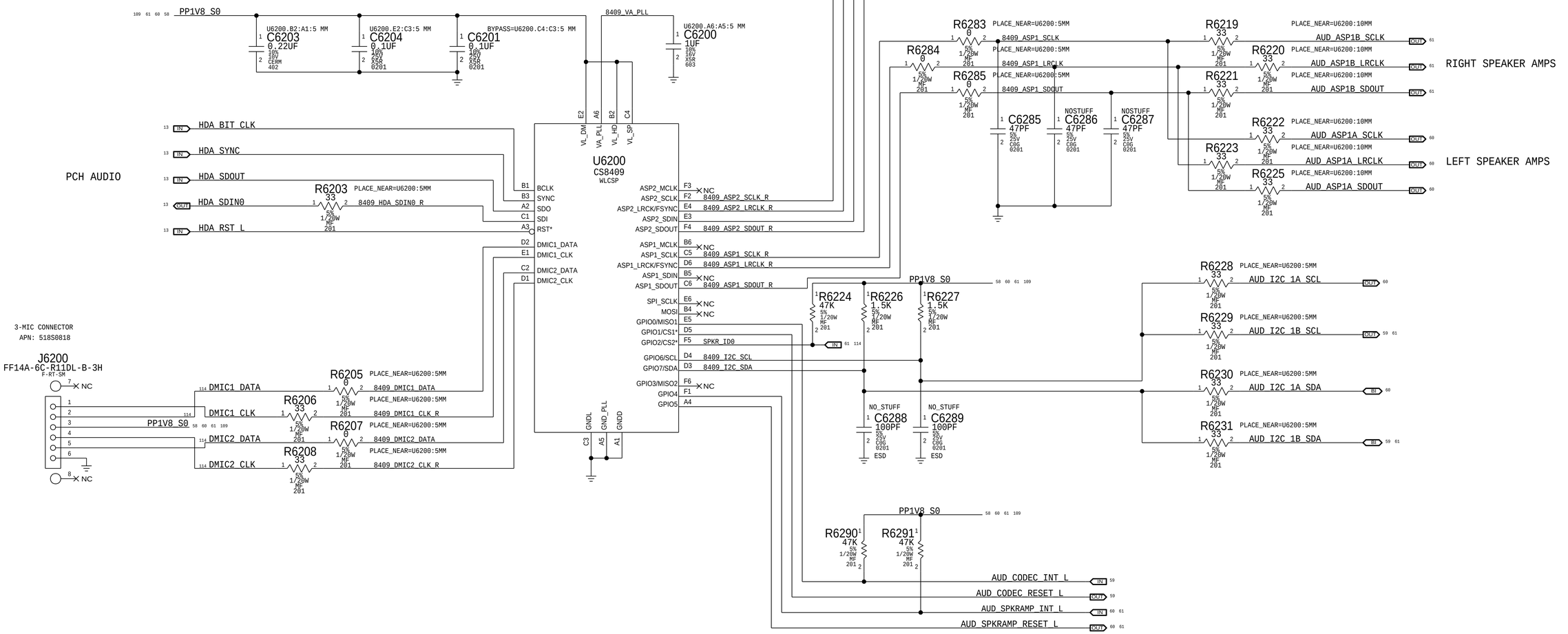


PAGE TITLE	HDA Bridge
	Apple Inc.
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	62 OF 145
SHEET	58 OF 121

AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B

L6361 FERR-470-OHM 0201
AUD_PWR_EN (12) → L83_LDO_EN

L6360 FERR-22-OHM-1A-0.055OHM 0201
PP3V3_S0 (59,110) → PP3V3_S0_AUD_F

U6360 NCP160AMX180 XDFN-COMBO
IN ← PP3V3_S0_AUD_F
EN ← L83_LDO_EN
OUT → PP1V8_S0_LDO_AUD (59)
GND EPAD

VOLTAGE=1.8V

CRITICAL C6360 1.0UF 20% 10V X5R-CERM 0201-1
BYPASS=U6360.A1:B2:3 MM

NOSTUFF R6360 100K 5% 1/20W MF 201

CRITICAL C6361 1.0UF 20% 10V X5R-CERM 0201-1
BYPASS=U6360.A2:B2:3 MM

XW6300 SHORT-8L-0.25MM-SM
GND_AUDIO_CODEC (59,117)

PP1V8_S0_LDO_AUD (59) → CRITICAL C6301 2.2UF 10% 10V X5R-CERM 0402 → GND_AUDIO_CODEC (59,117)
BYPASS=U6300.B1:C2:5 MM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200

L6300 FERR-22-OHM-1A-0.055OHM 0201
L83_VCP MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.0850

L6301 FERR-22-OHM-1A-0.055OHM 0201
PP1V8_S0_LDO_AUD (59) → L83_VL MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
CRITICAL C6303 0.1UF 10% 50V X7R 603-1
BYPASS=U6300.A3:B3:5 MM

L6302 FERR-22-OHM-1A-0.055OHM 0201
PP3V3_S0 (59,110) → L83_VP MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1800
CRITICAL C6304 10UF 20% 10V X5R-CERM 0402-7
BYPASS=U6300.D7:C7:5 MM

C6302 2.2UF 10% 10V X5R-CERM 0402
CRITICAL
BYPASS=U6300.D6:F6:5 MM
XW6301 SHORT-8L-0.25MM-SM
GND_VCP

OMIT_TABLE C6305 4.7UF 10% 10V X5R 0402
BYPASS=U6300.E6:F6:5 MM
L83_VCP_FILTP MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

OMIT_TABLE C6306 4.7UF 10% 10V X5R 0402
BYPASS=U6300.G6:F6:5 MM
L83_VCP_FILTN MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

AUD_HP_PORT_L (62 OUT) → NO_XNET_CONNECTION=1 → R6300 1K 5% 1/20W MF 201 → GND_AUDIO_CODEC (59,117)
NO_XNET_CONNECTION=1 → R6301 1K 5% 1/20W MF 201
AUD_HP_PORT_R (62 OUT)

AUD_HP_SENSE_L (62 IN)
AUD_HP_SENSE_R (62 IN)
AUD_HP_PORT_CH_GND (62 BI) → C6321 470PF 10% 16V X5R-X7R 201 NOSTUFF; C6322 470PF 10% 16V X5R-X7R 201 NOSTUFF; C6320 560PF 5% 25V C0G 0201 NOSTUFF
PLACE_NEAR=U6300:10mm
AUD_HP_PORT_US_GND (62 BI)
HS_MIC_P
HS_MIC_N
AUD_HS_MIC_P (62 IN)
AUD_HS_MIC_N (62 IN)

R6351 2.2K 1% 1/20W MF 201
R6352 2.2K 1% 1/20W MF 201
CRITICAL C6352 27PF 5% 25V C0G 0201
CRITICAL C6351 3300PF 10% 16V X7R-CERM 0201
R6350 100K 5% 1/20W MF 201
R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

AUD_RING_SENSE
AUD_TIP_SENSE (62 IN)
R6310 0 5% 1/20W MF 201
PLACE_NEAR=U6300:10mm
CRITICAL C6309 4.7UF 20% 6.3V X5R 402
BYPASS=U6300.F3:E3:5 MM
L83_HSBIAS_FILT MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
L83_HSBIAS_FILT_REF MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

CRITICAL U6300 CS42L83A WLCSP-SKT
APN:338S00142

D7	VP	+VCP_FILT	E6
A3	VL	-VCP_FILT	G6
A7	VD_FILT	GNDCP	F6
XNC		VL_SEL	C4
B1	VA	DIGLDO_PDN*	D4
D6	VCP	INT*	B7
D5	HPSENSA	WAKE*	C6
E5	HPOUTA	RESET*	C5
F5	HPSENSB	SPDIF_TX	A6
G5	HPOUTB	SWIRE_SEL	D3
F1	HS4	ASP_LRCK/FSYNC	B5
E2	HS_CLAMP2	SWIRE_SD/ASP_SDIN	A5
E1	HSIN+	ASP_SDOUT	A4
G2	HS3	SWIRE_CLK/ASP_SCLK	B4
F2	HS_CLAMP1	AD0	C3
D1	HSIN-	AD1	B2
F4	HS4_REF	SDA	A1
G4	HS3_REF	SCL	A2
G3	RING_SENSE	FLYP	E7
E4	TIP_SENSE	FLYC	F7
F3	HSBIAS_FILT	FLYN	G7
E3	HSBIAS_FILT_REF	FILT_P	C1
B3	GNDL		
B6	GNDD		
C7			
G1	GNDHS		
C2	GNDA		
D2			

AUD_CODEC_INT_L (58 OUT)
AUD_CODEC_WAKE_L <RDAR://PROBLEM/22033298>
AUD_CODEC_RESET_L (58 IN)
AUD_ASP2_LRCLK (58 IN)
AUD_ASP2_SDOUT (58 IN)
AUD_ASP2_SDIN (58 OUT)
AUD_ASP2_SCLK (58 IN)
L83_SDOUT_R → R6304 0 5% 1/20W MF 201 PLACE_NEAR=U6300:5mm → L83_SDOUT → R6306 33 5% 1/20W MF 201 PLACE_NEAR=U6300:10MM
AUD_I2C_1B_SDA (58 61 BI)
AUD_I2C_1B_SCL (58 61 IN)
L83_FLYP
L83_FLYC
L83_FLYN
L83_FILTP

R6302 47K 5% 1/20W MF 201 ← PP3V3_S0 (59,110)
R6303 100K 5% 1/20W MF 201

CRITICAL C6307 2.2UF 10% 10V X5R-CERM 0402
BYPASS=U6300.E7:F7:5 MM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

NOSTUFF C6380 47PF 5% 25V C0G 0201

CRITICAL C6308 2.2UF 10% 10V X5R-CERM 0402
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
BYPASS=U6300.G7:F7:5 MM

CRITICAL C6310 10UF 20% 10V X5R 0603
BYPASS=U6300.C1:C2:5 MM
GND_AUDIO_CODEC (59,117)
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

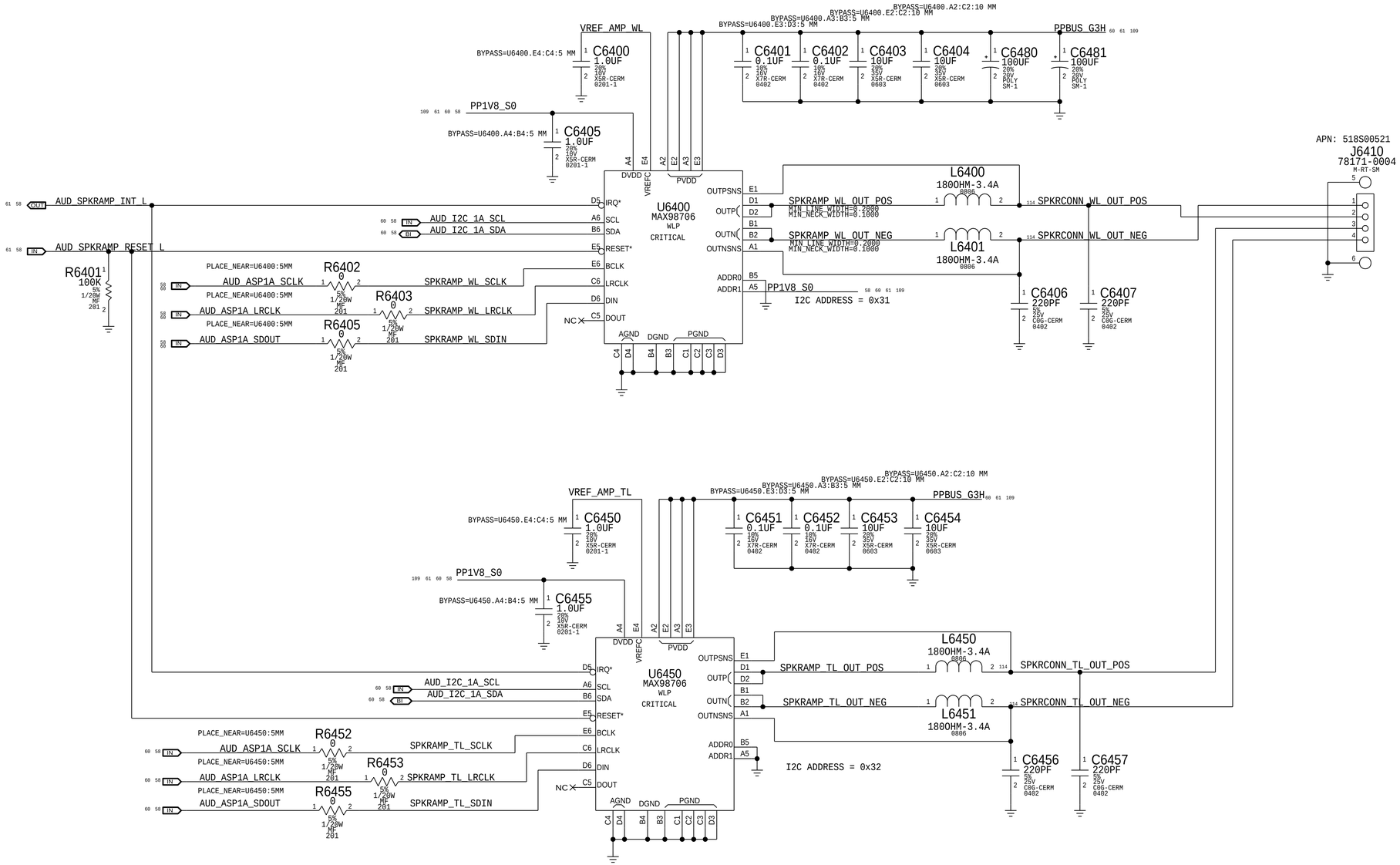
BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 63 OF 145
SHEET 59 OF 121

2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK



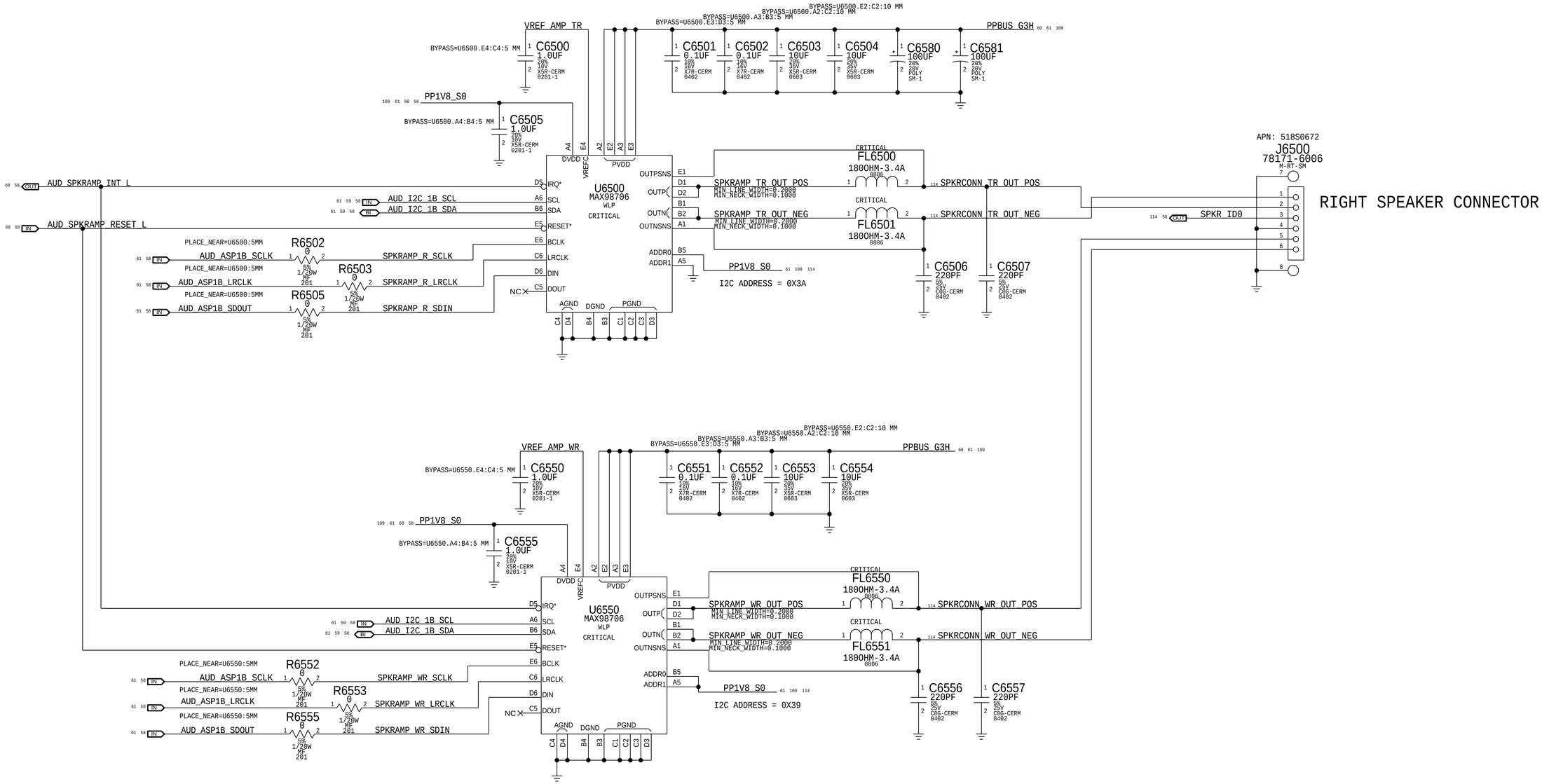
BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 64 OF 145
SHEET 60 OF 121

2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK

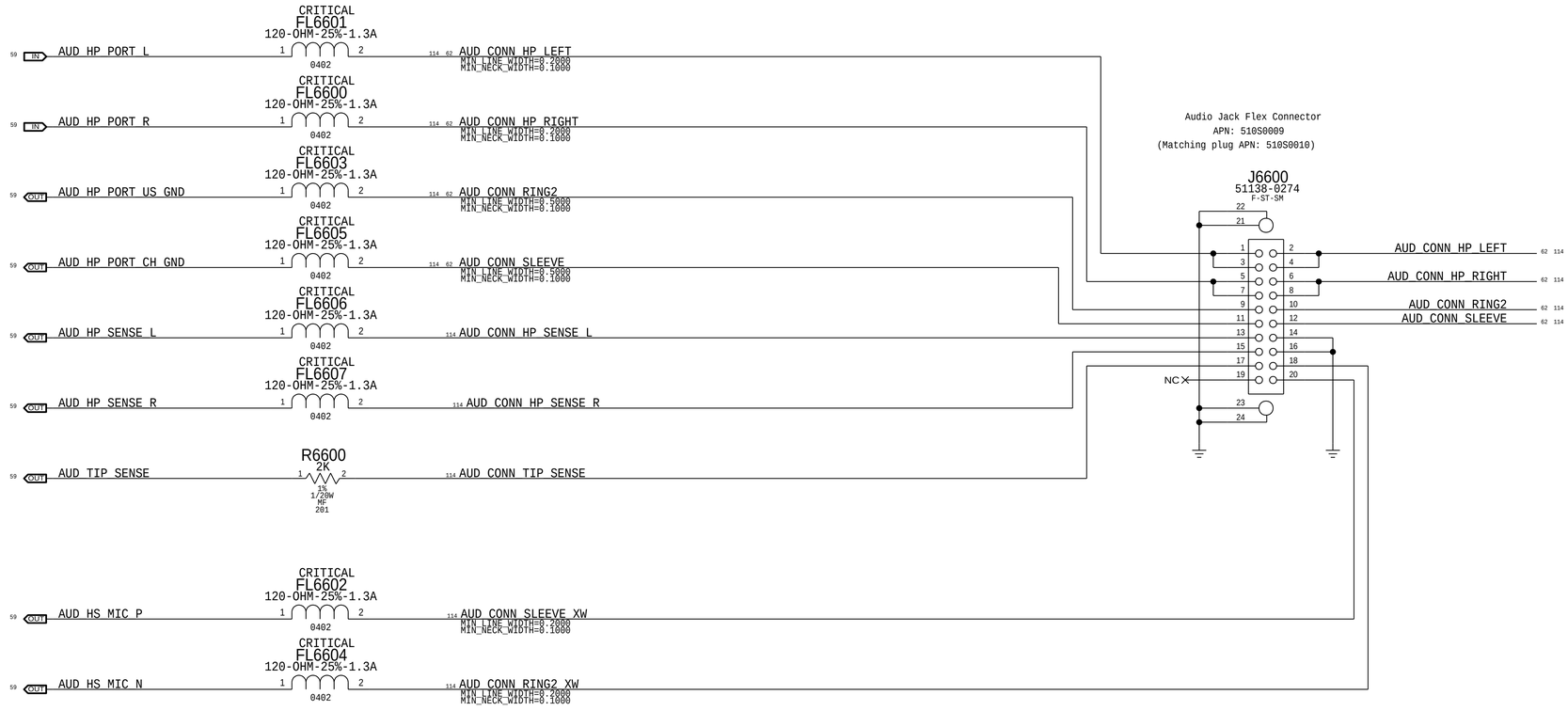


BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 65 OF 145
SHEET 61 OF 121



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

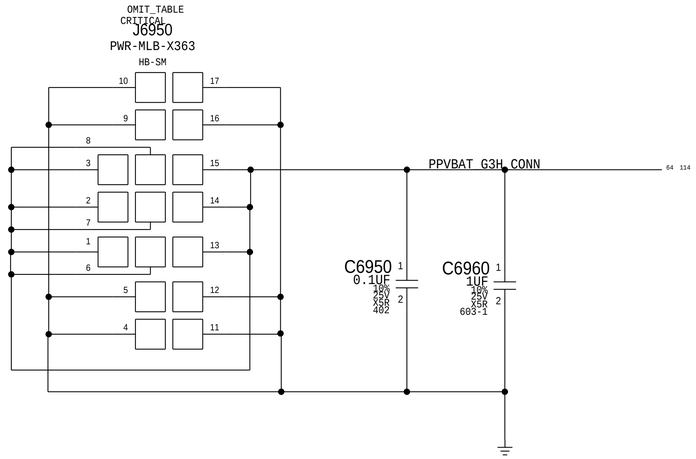
BRANCH dvt-fab10

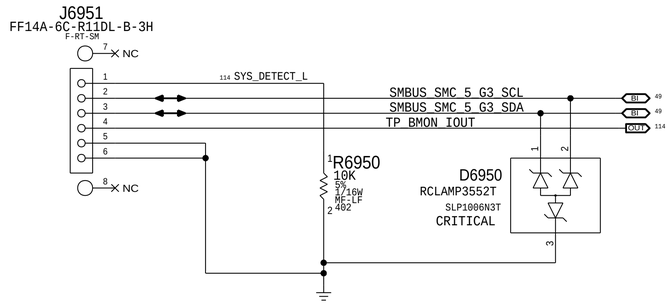
PAGE 66 OF 145

SHEET 62 OF 121

J80 Battery Hotbar Flex Pads 998-03902
Flex Pad TO MLB 998-03780.

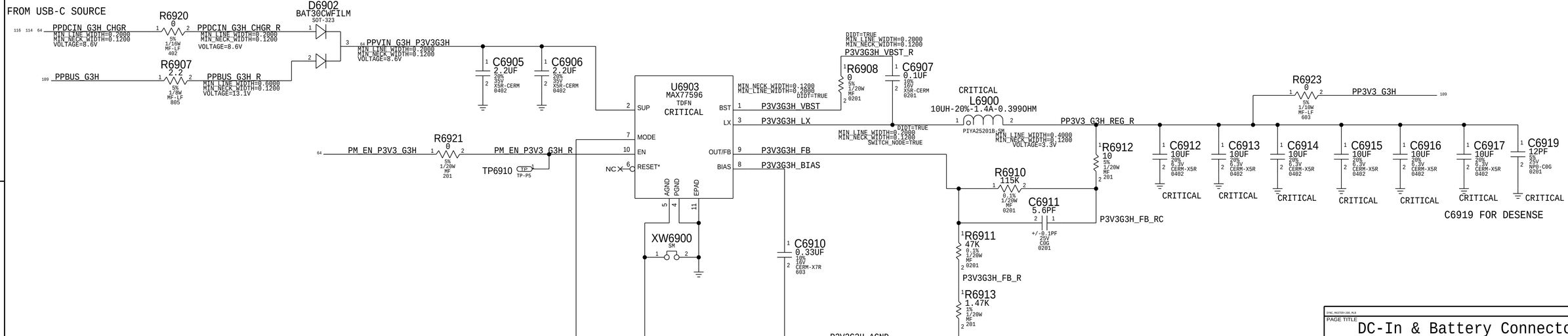
APN:518S0818





BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00862	1	PCBA,FLEX,BMU PWR,X363	J6950	CRITICAL	

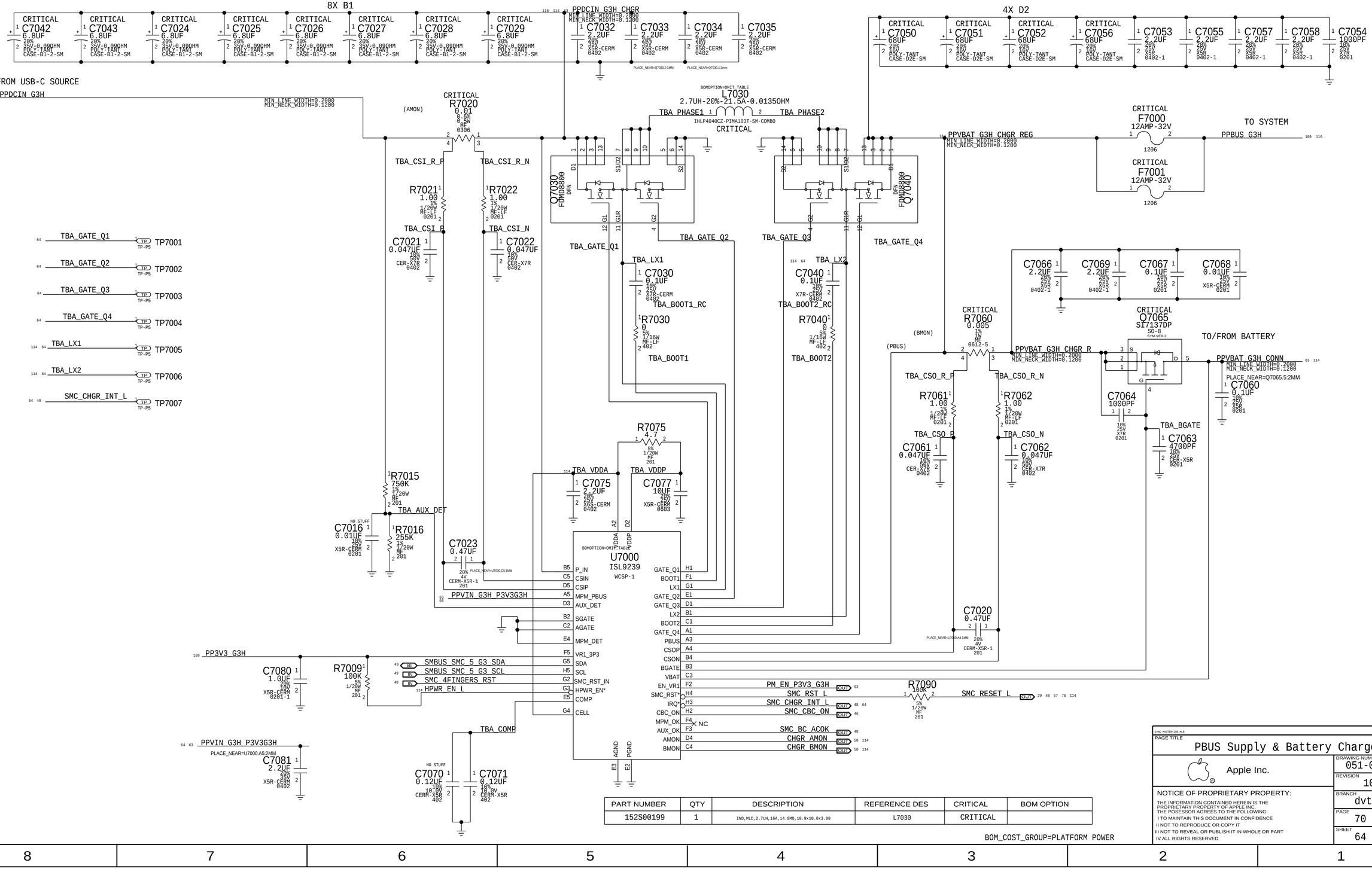


BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 69 OF 145
SHEET 63 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00199	1	IND,MLD,2.7UH,16A,14.8MO,10.9x10.0x3.00	L7030	CRITICAL	

SYNC_MASTER=J80_MLB — SYNC_DATE=11/06/2015

PAGE TITLE

PBUS Supply & Battery Charger

Apple Inc.

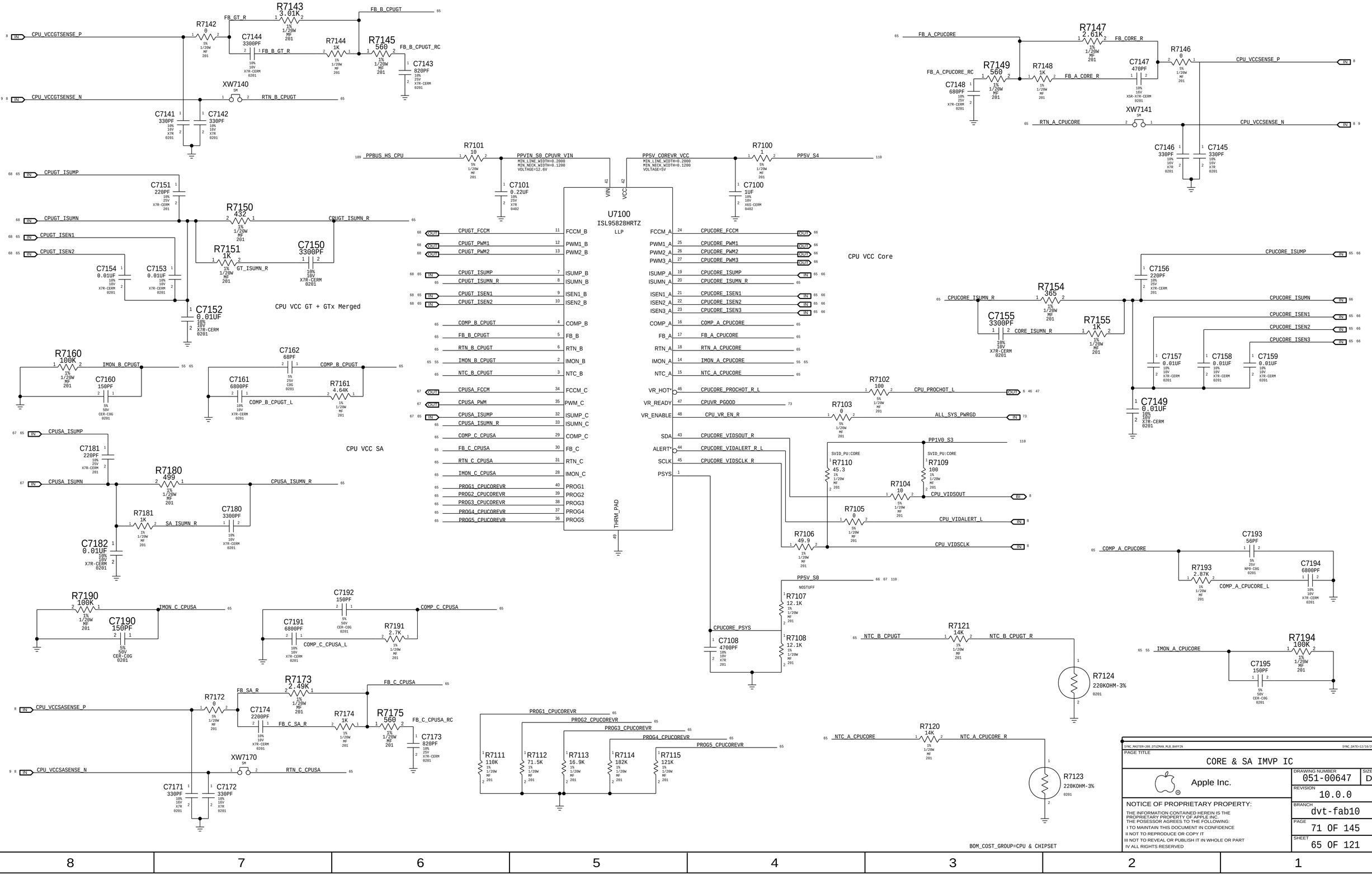
DRAWING NUMBER 051-00647 — SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 70 OF 145

SHEET 64 OF 121


CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
R7142 0
R7143 3.01K
R7144 1K
R7145 560
C7144 3300PF
C7143 820PF
FB_GT_R
FB_B_CPUGT
FB_B_CPUGT_RC
RTN_B_CPUGT
XW7140
C7141 330PF
C7142 330PF
CPUGT_ISUMP
CPUGT_ISUMN
CPUGT_ISEN1
CPUGT_ISEN2
C7151 220PF
R7150 432
R7151 1K
C7150 3300PF
C7154 0.01UF
C7153 0.01UF
C7152 0.01UF
CPUGT_ISUMN_R
GT_ISUMN_R
CPU VCC GT + GTx Merged
R7160 100K
C7160 150PF
IMON_B_CPUGT
C7162 68PF
C7161 6800PF
R7161 4.64K
COMP_B_CPUGT
COMP_B_CPUGT_L
CPUSA_ISUMP
CPUSA_ISUMN
C7181 220PF
R7180 499
R7181 1K
C7180 3300PF
C7182 0.01UF
CPUSA_ISUMN_R
SA_ISUMN_R
CPU VCC SA
R7190 100K
C7190 150PF
IMON_C_CPUSA
C7192 150PF
C7191 6800PF
R7191 2.7K
COMP_C_CPUSA
COMP_C_CPUSA_L
R7101 10
C7101 0.22UF
PPBUS_HS_CPU
PPVIN_S0_CPUVR_VIN
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
R7100 1
C7100 1UF
PP5V_COREVR_VCC
PP5V_S4
U7100
ISL95828HRTZ
LLP
VIN
VCC
THRM_PAD
FCCM_B
PWM1_B
PWM2_B
ISUMP_B
ISUMN_B
ISEN1_B
ISEN2_B
COMP_B
FB_B
RTN_B
IMON_B
NTC_B
FCCM_C
PWM_C
ISUMP_C
ISUMN_C
COMP_C
FB_C
RTN_C
IMON_C
PROG1
PROG2
PROG3
PROG4
PROG5
FCCM_A
PWM1_A
PWM2_A
PWM3_A
ISUMP_A
ISUMN_A
ISEN1_A
ISEN2_A
ISEN3_A
COMP_A
FB_A
RTN_A
IMON_A
NTC_A
VR_HOT*
VR_READY
VR_ENABLE
SDA
ALERT*
SCLK
PSYS
CPUCORE_FCCM
CPUCORE_PWM1
CPUCORE_PWM2
CPUCORE_PWM3
CPUCORE_ISUMP
CPUCORE_ISUMN_R
CPUCORE_ISEN1
CPUCORE_ISEN2
CPUCORE_ISEN3
COMP_A_CPUCORE
FB_A_CPUCORE
RTN_A_CPUCORE
IMON_A_CPUCORE
NTC_A_CPUCORE
CPUCORE_PROCHOT_R_L
CPU_VR_EN_R
CPUCORE_VIDSOUT_R
CPUCORE_VIDALERT_R_L
CPUCORE_VIDSCLK_R
CPU VCC Core
R7102 100
R7103 0
CPU_PROCHOT_L
ALL_SYS_PWRGD
PP1V0_S3
R7110 45.3
R7109 100
R7104 10
R7105 0
R7106 49.9
CPU_VIDSOUT
CPU_VIDALERT_L
CPU_VIDSCLK
SVID_PU:CORE
PP5V_S0
NOSTUFF
R7107 12.1K
R7108 12.1K
C7108 4700PF
CPUCORE_PSYS
R7147 2.61K
R7148 1K
R7149 560
C7147 470PF
C7148 680PF
FB_A_CPUCORE
FB_A_CPUCORE_RC
FB_CORE_R
FB_A_CORE_R
R7146 0
C7146 330PF
C7145 330PF
CPU_VCCSENSE_P
CPU_VCCSENSE_N
RTN_A_CPUCORE
XW7141
R7121 14K
R7124 220KOHM-3%
NTC_B_CPUGT
NTC_B_CPUGT_R
R7120 14K
R7123 220KOHM-3%
NTC_A_CPUCORE
NTC_A_CPUCORE_R
C7193 56PF
R7193 2.87K
C7194 6800PF
COMP_A_CPUCORE_L
R7194 100K
C7195 150PF
R7154 365
C7155 3300PF
R7155 1K
CORE_ISUMN_R
C7156 220PF
C7157 0.01UF
C7158 0.01UF
C7159 0.01UF
C7149 0.01UF
CPUCORE_ISUMP
CPUCORE_ISUMN
CPUCORE_ISEN1
CPUCORE_ISEN2
CPUCORE_ISEN3
R7111 110K
R7112 71.5K
R7113 16.9K
R7114 182K
R7115 121K
PROG1_CPUCOREVR
PROG2_CPUCOREVR
PROG3_CPUCOREVR
PROG4_CPUCOREVR
PROG5_CPUCOREVR
R7172 0
C7174 2200PF
R7174 1K
R7175 560
C7173 820PF
R7173 2.49K
FB_SA_R
FB_C_CPUSA
FB_C_CPUSA_RC
FB_C_SA_R
XW7170
C7171 330PF
C7172 330PF
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
RTN_C_CPUSA
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=J80_DTU2MAR_MLB_BAFFIN
SYNC_DATE=12/10/2015
PAGE TITLE
CORE & SA IMVP IC
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 71 OF 145
SHEET 65 OF 121
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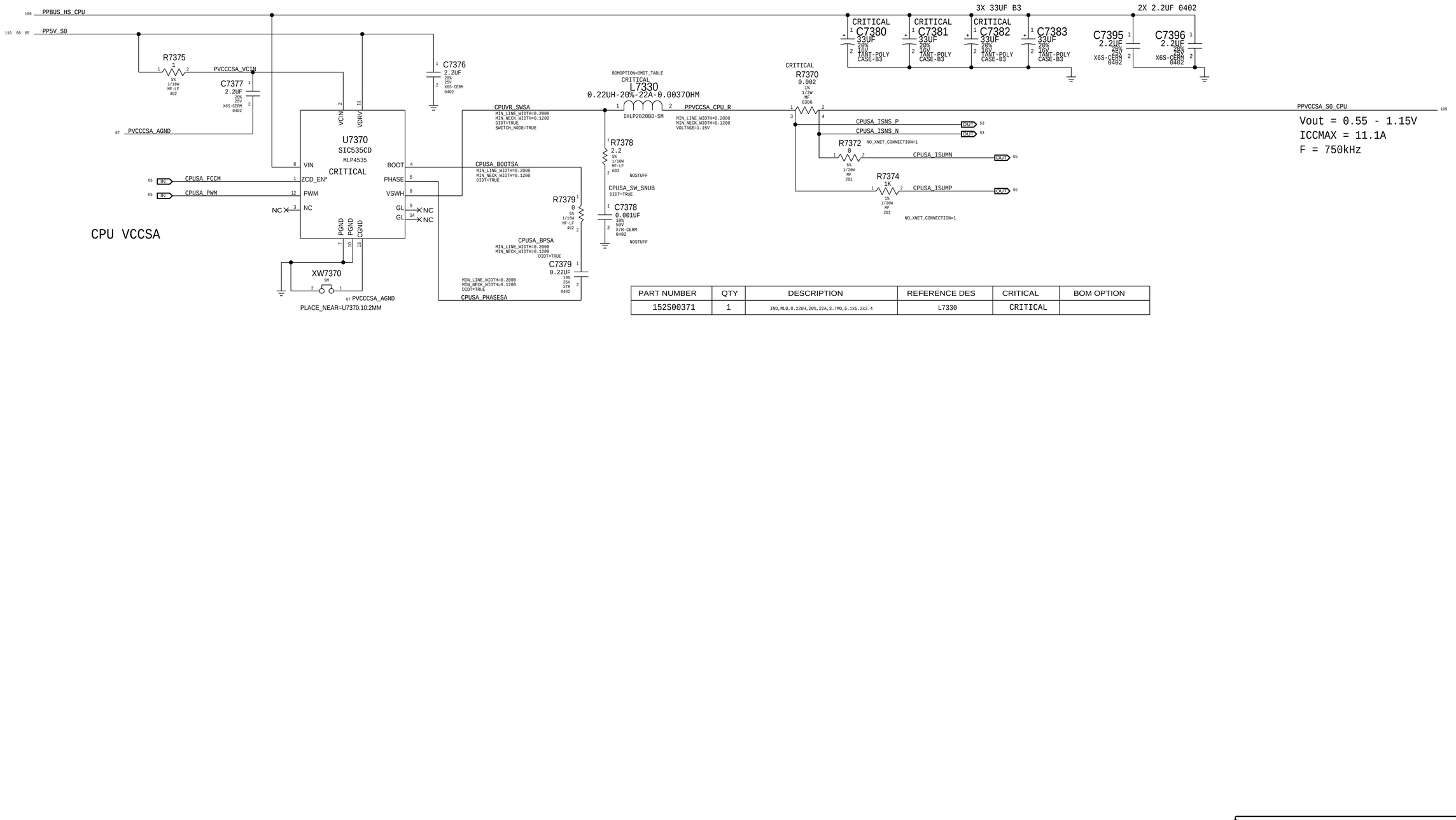
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7230	CRITICAL	

SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN
SYNC_DATE=09/03/2015

PAGE TITLE
CORE IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 72 OF 145
SHEET 66 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00371	1	IND,MLD,0.22UH,20%,22A,3.7MO,5.1x5.2x2.4	L7330	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN SYNC_DATE=11/18/2015

PAGE TITLE

SA IMVP IC

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

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BRANCH dvt-fab10

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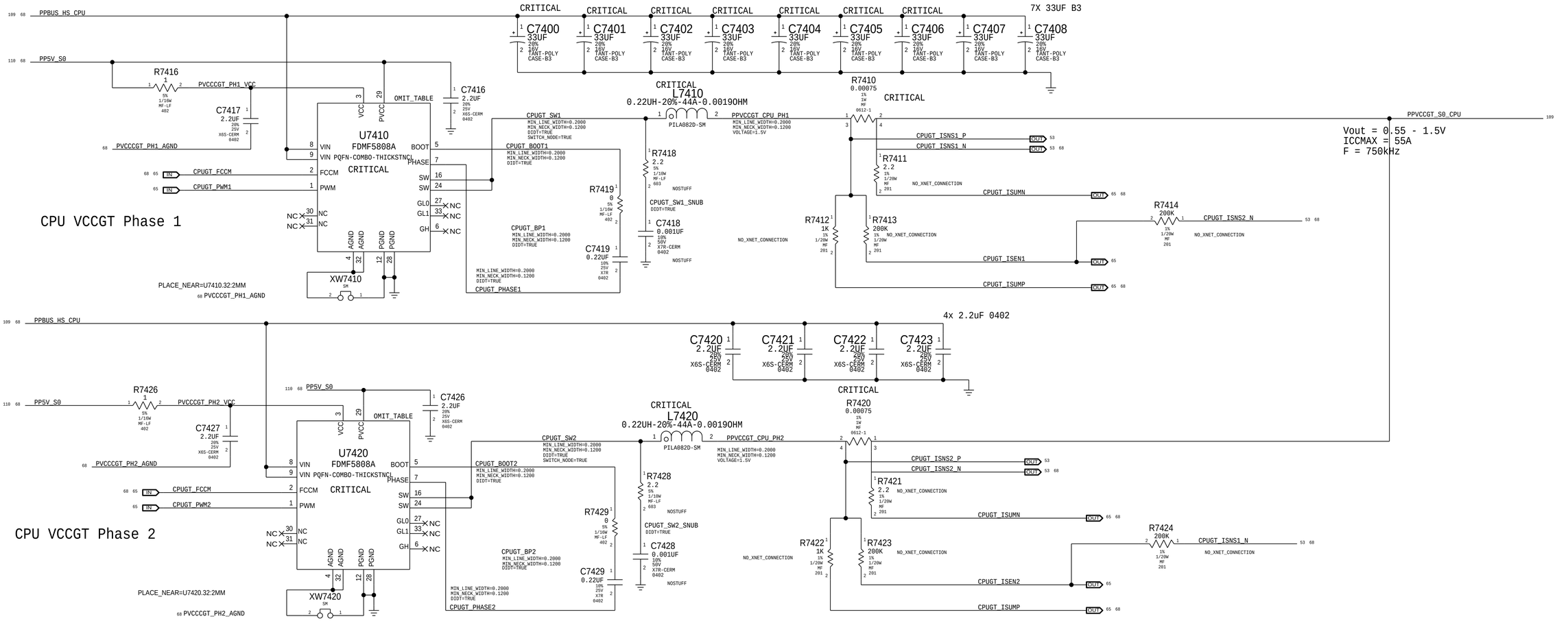
SHEET 67 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7410,U7420	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTU2MAN_MLB_BAFFIN SYNC_DATE=09/03/2015

PAGE TITLE

GT & GTX IMVP POWER BLOCK

Apple Inc.

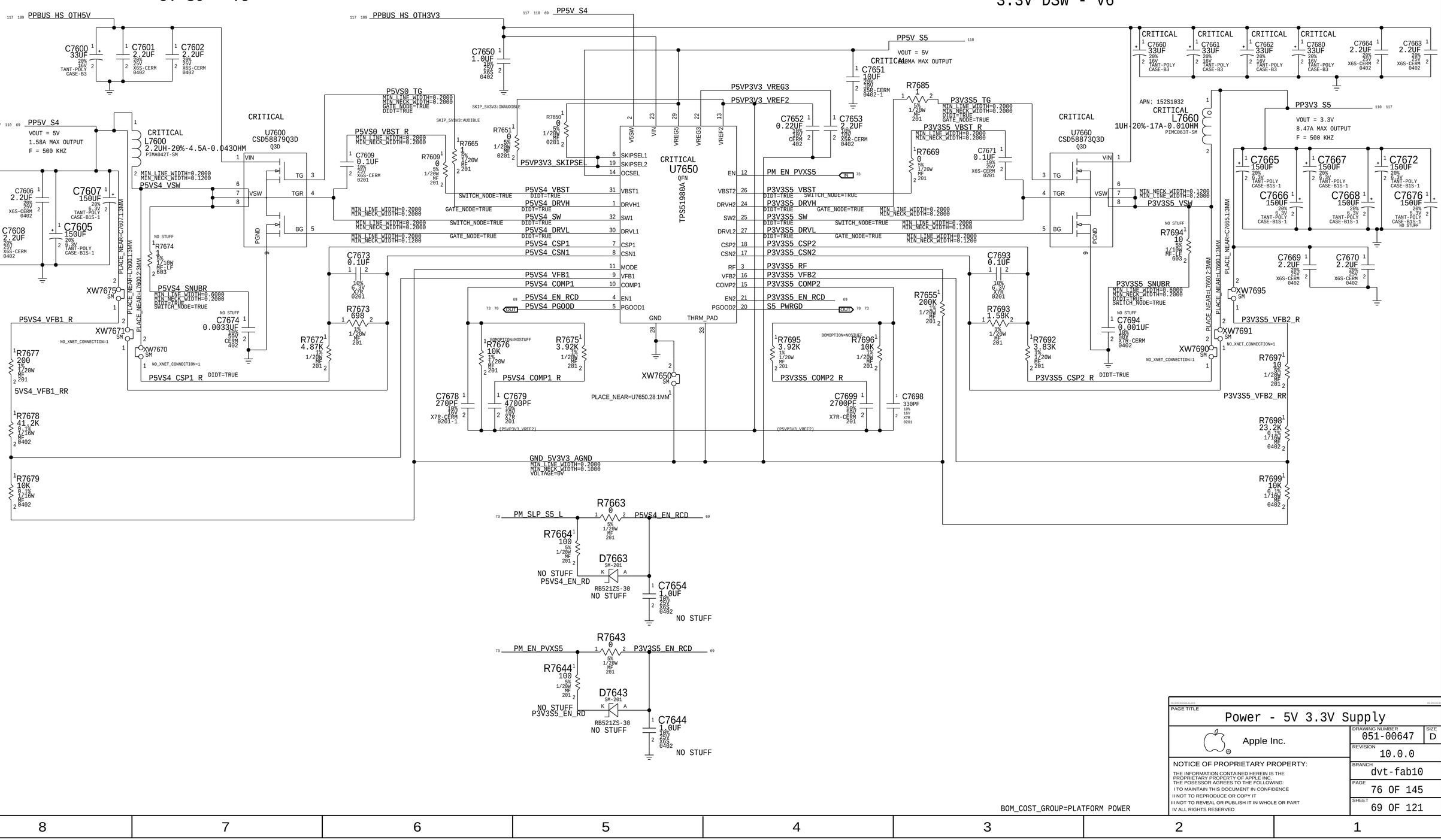
DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 74 OF 145

SHEET 68 OF 121



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PAGE TITLE	Power - 5V 3.3V Supply
	Apple Inc.
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	76 OF 145
SHEET	69 OF 121

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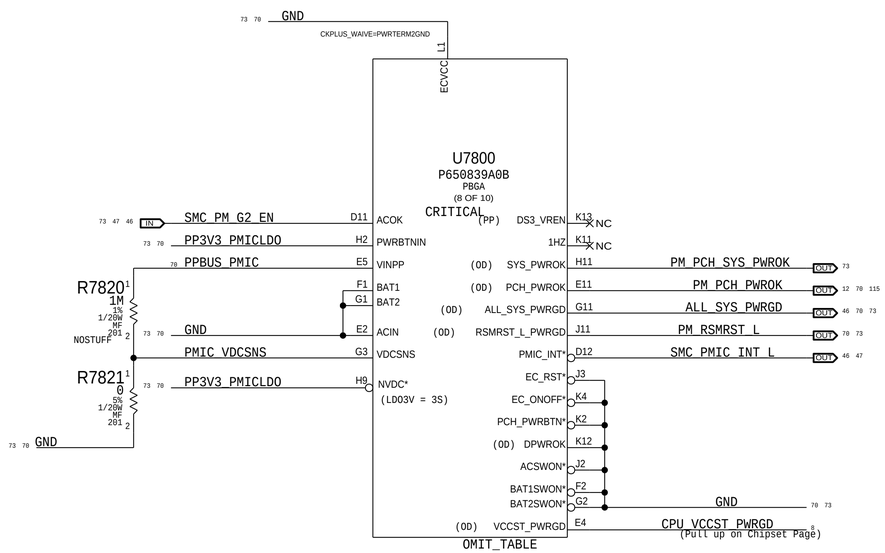
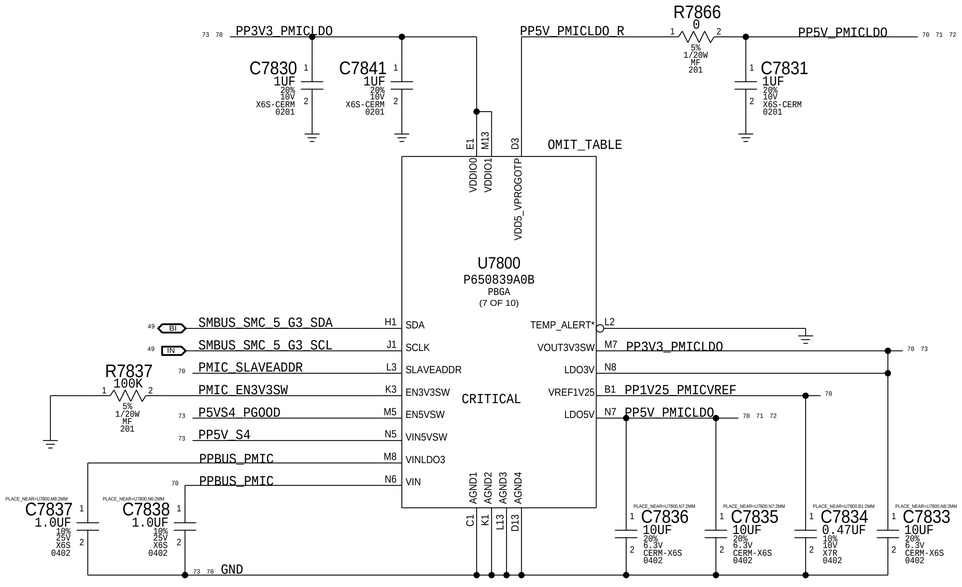
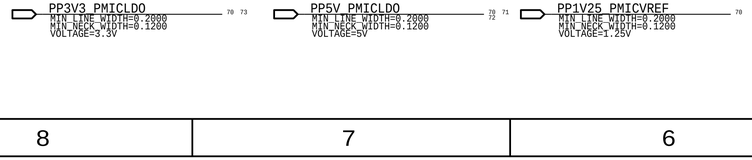
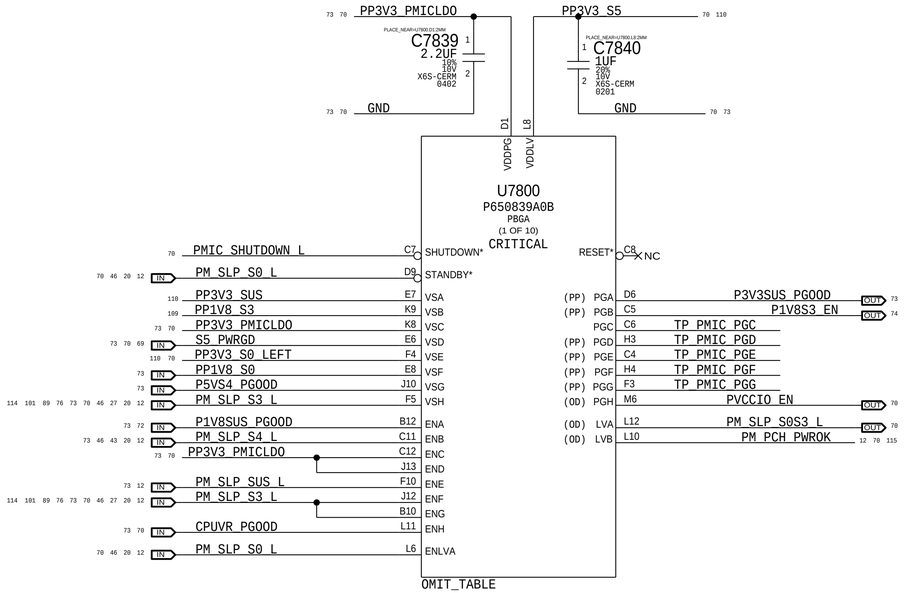
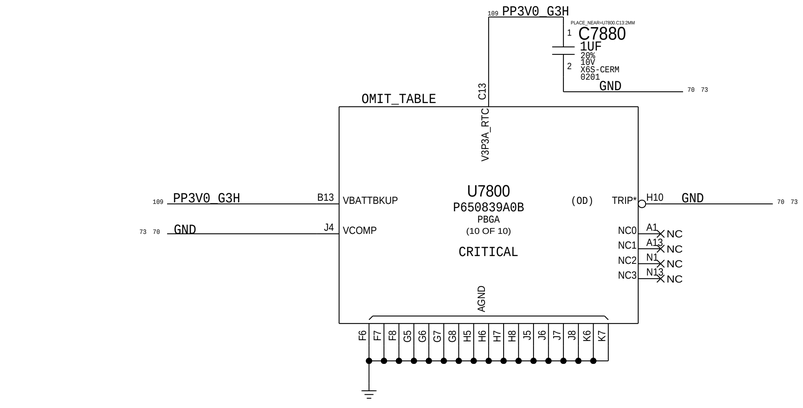
BANJO - PMIC Control

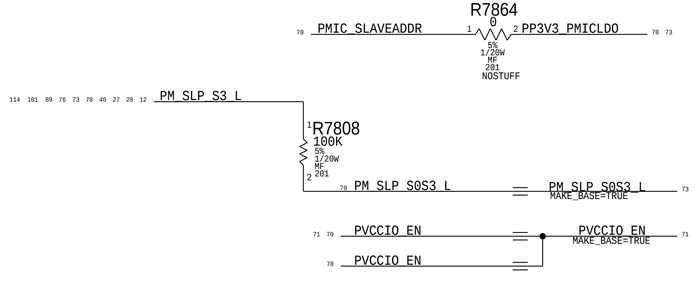


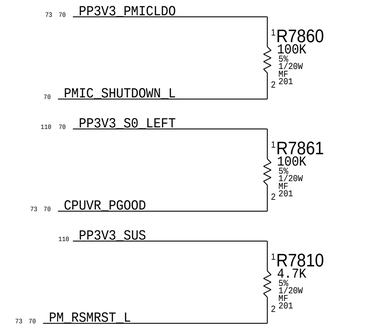


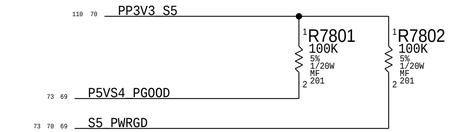


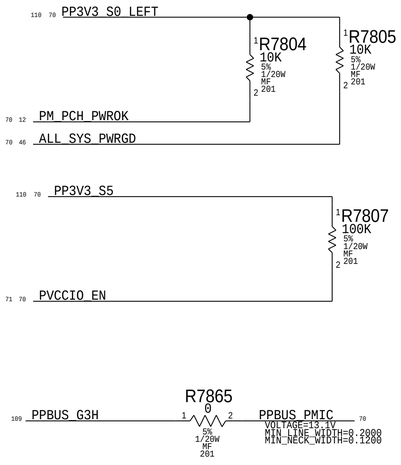












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SYNC_MASTER=J08_MLB SYNC_DATE=12/08/2010

PAGE TITLE

PMIC-1 & Power Control

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

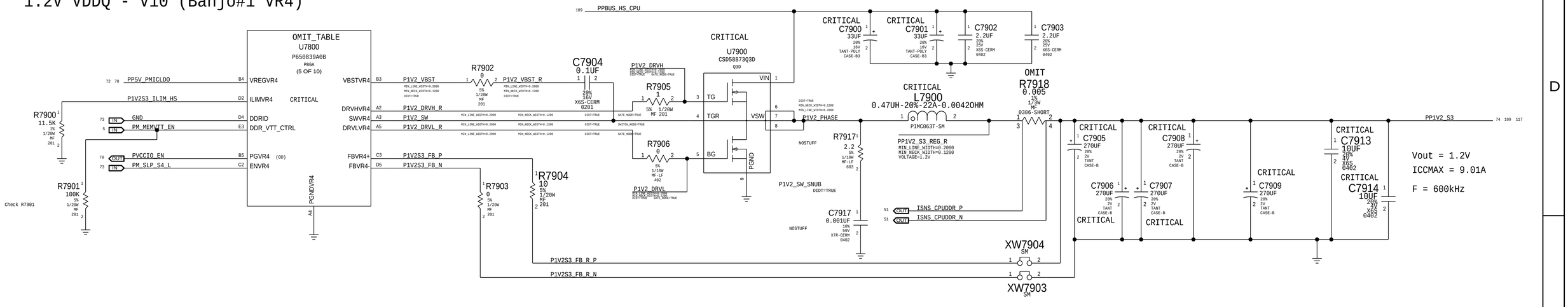
REVISION 10.0.0

BRANCH dvt-fab10

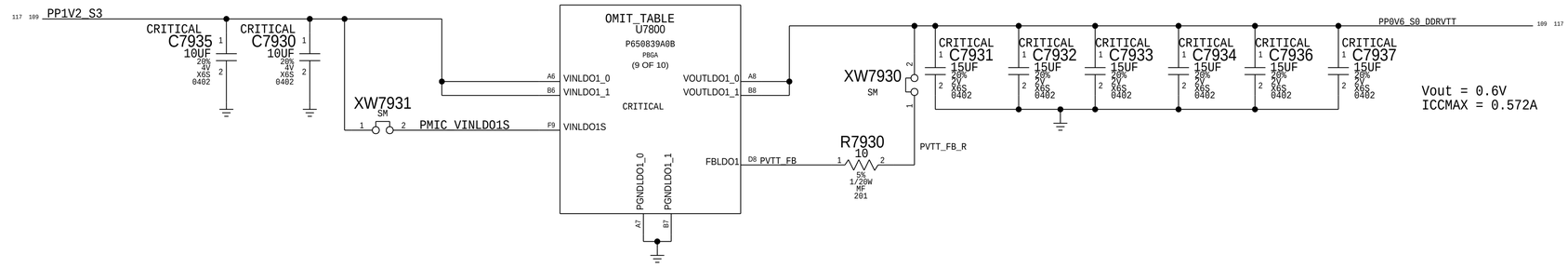
PAGE 78 OF 145

SHEET 70 OF 121

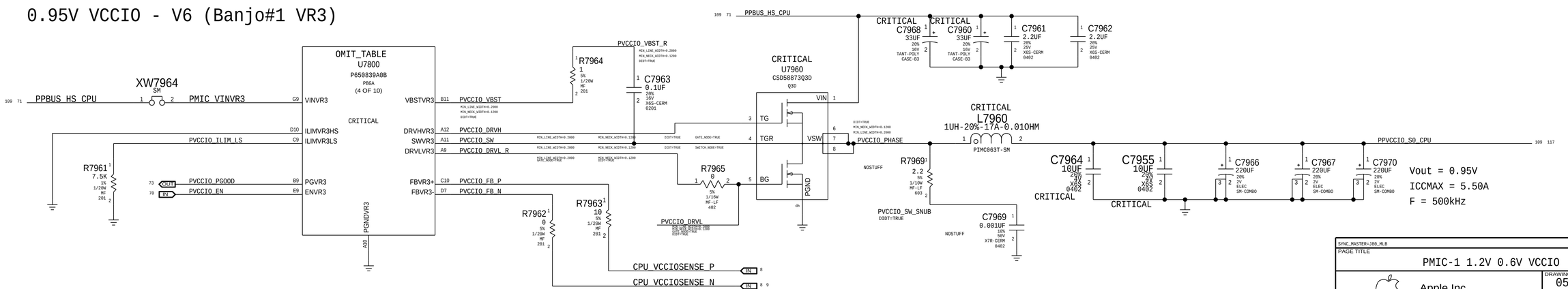
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LDO1)



0.95V VCCIO - V6 (Banjo#1 VR3)



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

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BRANCH dvt-fab10

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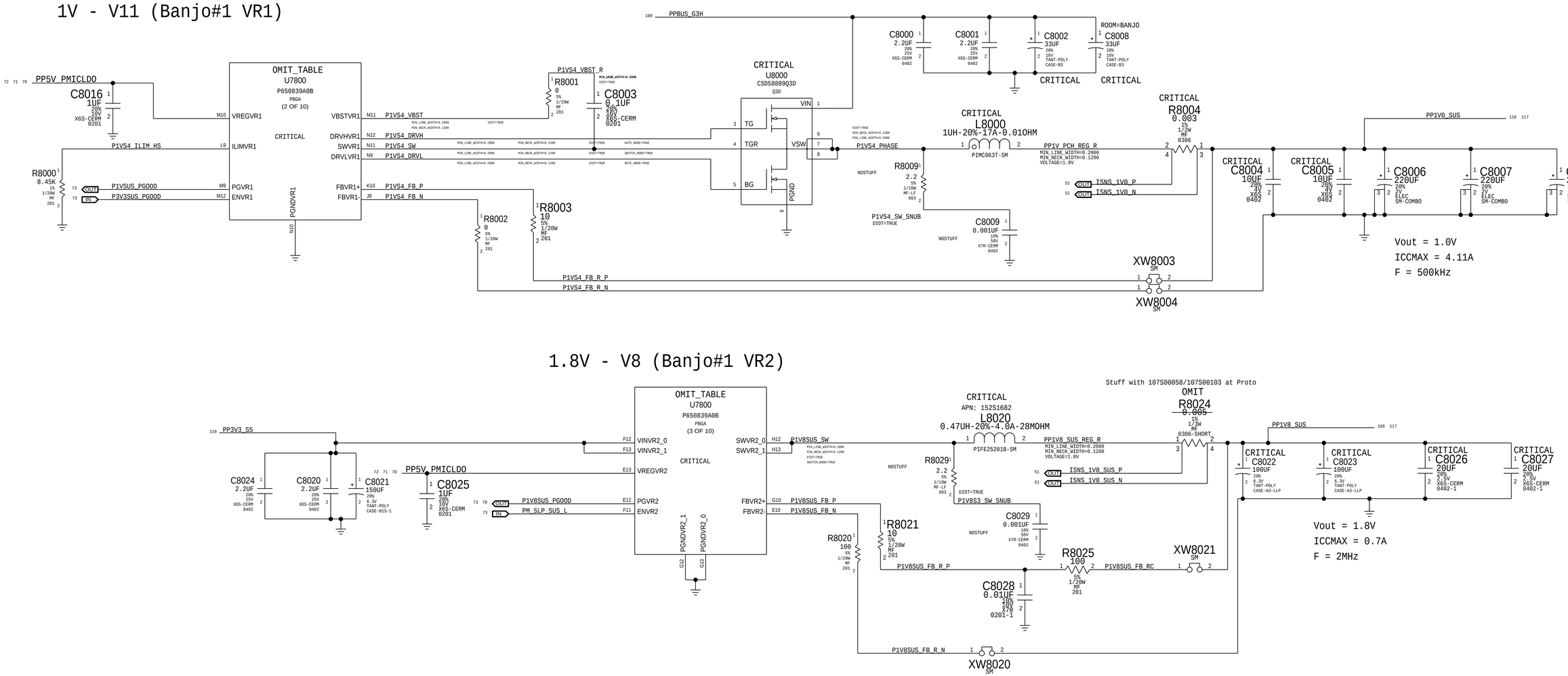
SHEET 71 OF 121



PAGE TITLE

PMIC-1 1V 1.8V VCCPCH

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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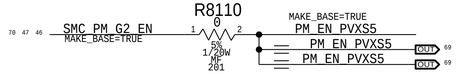
BOM_COST_GROUP=PLATFORM POWER

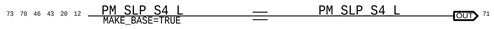
S5 Enables



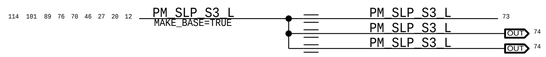
SUS Enables

S4 Enables

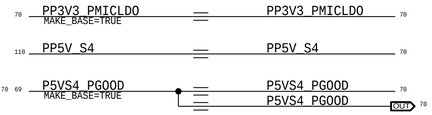
S3 Enables

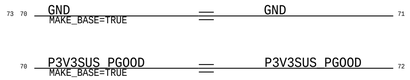


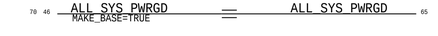
S0 Enables

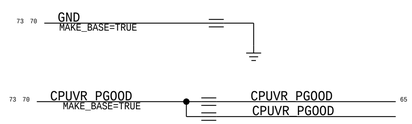


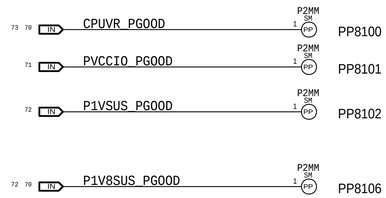
S0i Enables



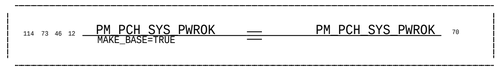


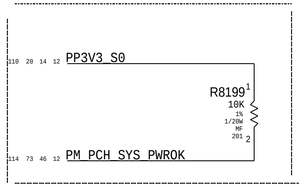




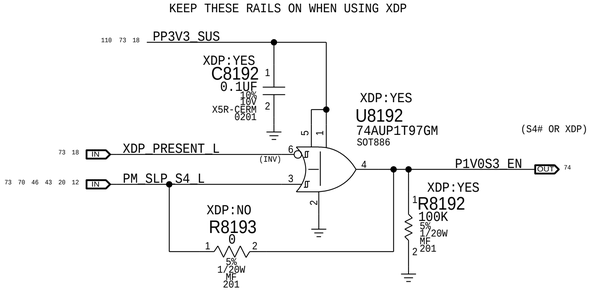


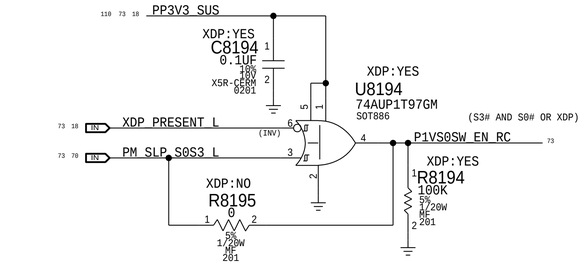
J80G specific

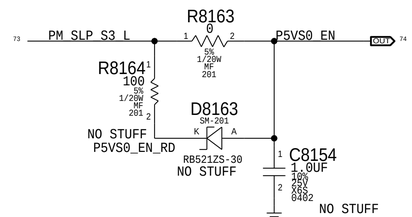




KEEP THESE RAILS ON WHEN USING XDP







BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

PMIC-1 Aliases & TPs

Apple Inc.

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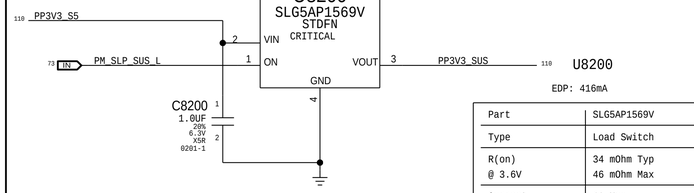
3.3V SUS Switch

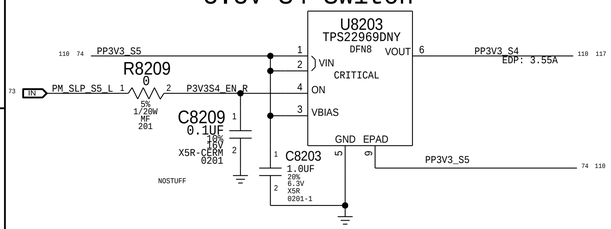


U8200

EDP: 416mA

Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

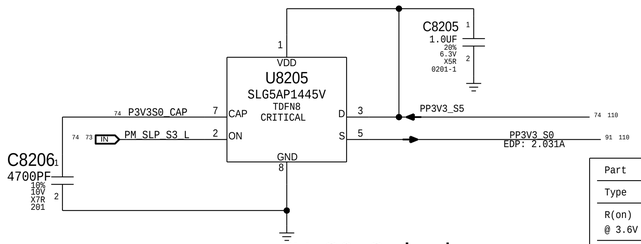
3.3V S4 Switch



U8203

Part	TPS22969
Type	Load Switch
R(on) @ 3.6V	4.4 MOHM TYP 6.6 MOHM MAX
Current	6A MAX

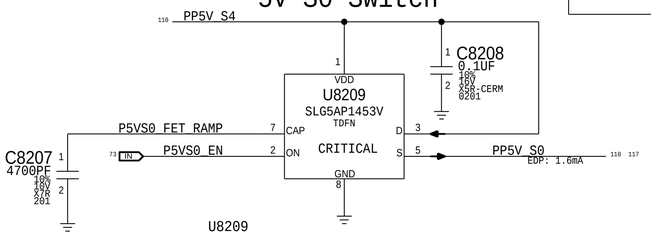
3.3V S0 Switch



U8205

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

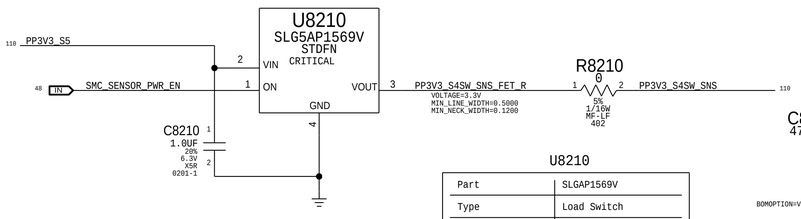
5V S0 Switch



U8209

Part	SLG5AP1453V
Type	Load Switch
R(on)	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A

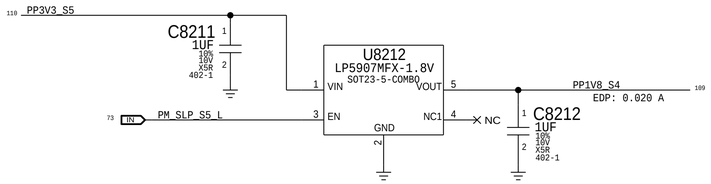
3.3V Sensor Switch



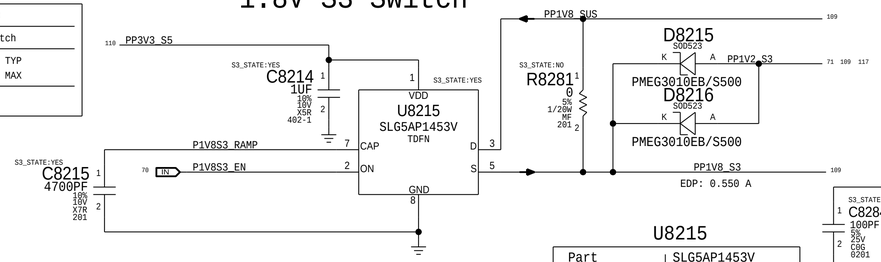
U8210

Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

1.8V S4 LDO



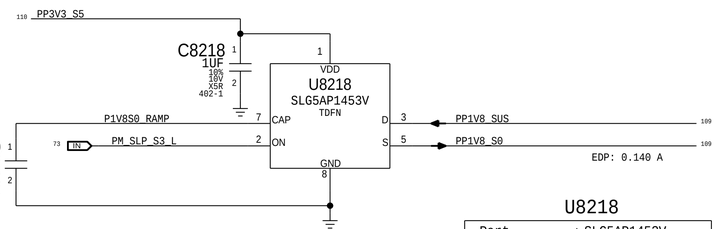
1.8V S3 Switch



U8215

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

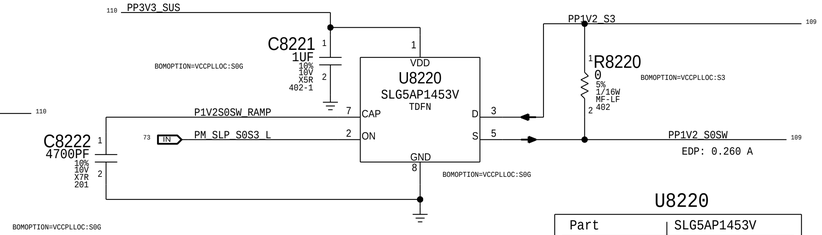
1.8V S0 Switch



U8218

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

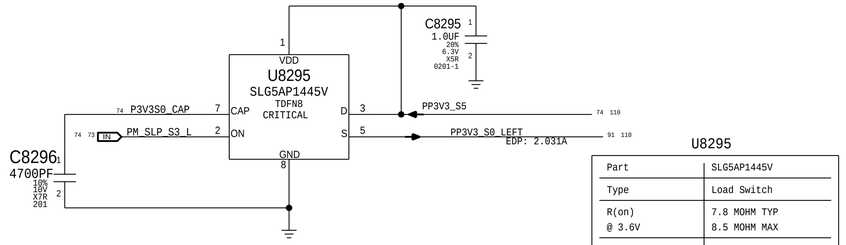
1.2V S0 SW Switch



U8220

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

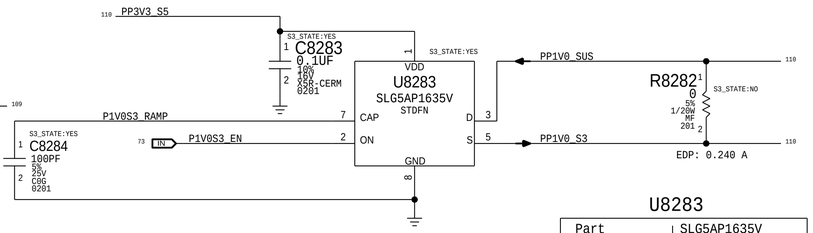
3.3V S0 Switch LEFT



U8295

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

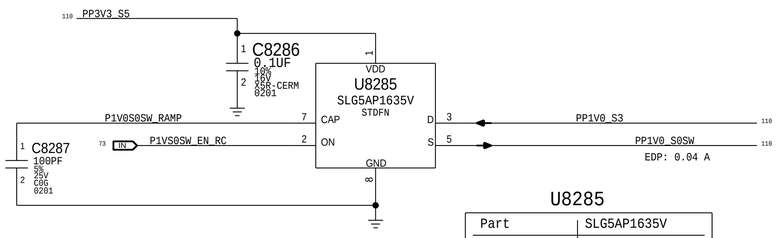
1.0V S3 Switch



U8283

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

1.0V S0 SW Switch



U8285

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

Power FETs

Apple Inc.

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Page Notes

Power aliases required by this page:

- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)

PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

I2C ID DEDICATED.ONLY CONNECTS TO JERRY

VOUT = 52V TYP, 59V MAX
IOUT = 0.135A TYP, 0.15A MAX
FS = 625KHZ TYP (+/- 7%)

PBUS LINE WIDTHS

PP5V_S0_BKLT_A: MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V
PP5V_S0_BKLT_D: MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V
PPVIN_S0SW_LCDBKLT_FET: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=12.6V
PPVIN_S0SW_LCDBKLT_R: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=12.6V
PPVIN_S0SW_LCDBKLT_FET: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200
PPVIN_S0SW_LCDBKLT: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=12.6V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV_R: MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE
PPVIN_SW_LCDBKLT_SW: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=59V, SWITCH_NODE=TRUE, DIDT=TRUE
PPVOUT_S0_LCDBKLT: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=59V

BOM_COST_GROUP=DISPLAY

PAGE TITLE	LCD Backlight Driver
	Apple Inc.
DRAWING NUMBER	051-00647
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LCD PANEL INTERFACE (eDP) + Camera (MIPI)

U8510 BYPASS

NO STUFF
R8590 0 5% 1/20W MF 0201
EDP_PANEL_PWR_EN (89 76) → PANEL_FET_EN_DLY (76)

NO STUFF
R8591 0 5% 1/20W MF 0201
EDP_PANEL_PWR_EN → BUF_EDP_PANEL_PWR_EN (76 114)

NO STUFF
R8592 0 5% 1/20W MF 0201
SMC_RESET_L (IN, 76 64 57 48 29 114) → BUF_SMC_RESET_L (OUT, 46 48 76)

LCD Panel HPD, FSS & AUX strapping

PP3V3_S0 (116)

NO_XNET_CONNECTION=1
NO_STUFF
R8503 1M 5% 1/20W MF 201 → EDP_AUXCH_C_N (114 76)

R8505 0 5% 1/20W MF 0201
DP_INT_HPD (OUT, 114 89) → DP_INT_HPD_R (76)

EDP_AUXCH_C_P (114 76)

LCD_FSS (114 76 89)

R8504 100K 5% 1/20W MF 201

R8501 100K 5% 1/20W MF 201

NO_XNET_CONNECTION=1
NO_STUFF
R8502 1M 5% 1/20W MF 201

R8517 330 5% 1/20W MF 201
PANEL_P5V_EN_D → D8517 DSF01S30SCAP (SC2)

R8515 150K 5% 1/20W MF 201
PANEL_P5V_EN

PP5V_S0 (110)
CRITICAL
U8500 SLG5AP1443V TDFN
VDD, CAP, ON, GND, D, S
LCD_PWR_SLEW

C8515 0.1UF 10% 16V X5R-CERM 0201
C8509 2200PF 10% 10V X7R-CERM 0201
C8511 0.1UF 10% 16V X5R-CERM 0201
C8512 10UF 20% 6.3V X5R-CERM 0402-7

VOLTAGE=5V
PP5V_S0SW_LCD (76 114)

R8516 200K 1% 1/20W MF 201
PANEL_P3V3_EN

R8518 330 5% 1/20W MF 201
PANEL_P3V3_EN_D → D8518 DSF01S30SCAP (SC2)

C8516 0.47UF 10% 6.3V CERM-X5R 0201

PP3V3_S5 (110)
CRITICAL
U8501 SLG5AP1443V TDFN
VDD, CAP, ON, GND, D, S
LCD_PWR_SLEW_3V3

C8513 2200PF 10% 10V X7R-CERM 0201

C8510 1.0UF 20% 6.3V X5R 0201-1

VOLTAGE=3.3V
PP3V3_S0SW_LCD_R

Stuff with 107S0276/107S0020 at Proto
0MIT
R8520 0.005 1% 1/2W MF 0306-SHORT
NO_XNET_CONNECTION=1
PP3V3_S0SW_LCD (76 114)
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

ISNS_LCDPANEL_P (52)
ISNS_LCDPANEL_N (52)

PPVOUT_S0_LCDBKLT (75 76 114 116)
C8500 1000PF 10% 100V X7R-CERM 0603

76 PANEL_FET_EN_DLY

109 47 46 PP3V3_G3H

CRITICAL
U8510 SLG4AP4998 STQFN
VDD, EDP_PANEL_PWR_EN, PM_SLP_S3_L, SMC_RESET_INPUT_L, PANEL_FET_EN_DLY, PANEL_PWR_EN_CONN, SMC_RESET_OUTPUT_L, X604_DISP_PWR_EN, X604_DISP_SMC_RST_L, NC0, NC1, GND

EDP_PANEL_PWR_EN (IN, 89 76)
PM_SLP_S3_L (IN, 114 101 89 73 70 46 27 20 12)
SMC_RESET_L (IN, 114 76 64 57 48 29)

BUF_SMC_RESET_L (OUT, 46 48 76)
DFR_DISP_PWR_EN (OUT, 42)
DFR_DISP_SMC_RST_L (OUT, 42)
BUF_EDP_PANEL_PWR_EN (76 114)

NC_U8510_5
NC_U8510_11

J8500 20759-042E-02 F-ST-SM
NO_XNET_CONNECTION=1

PPVOUT_S0_LCDBKLT (116 114 76 75)	43 PWR	44	PP3V3_S0SW_LCD (76 114)
EDP_AUXCH_C_N (114 76)	1 SIGNAL	2	
EDP_AUXCH_C_P (114 76)	3	4	BUF_EDP_PANEL_PWR_EN (76 114)
	5	6	DP_INT_HPD_R (76)
EDP_INT_ML_N<0> (76)	7	8	LCD_FSS (76 89 114)
EDP_INT_ML_P<0> (76)	9	10	LCD_IRQ_L (OUT, 15 114)
EDP_INT_ML_N<1> (76)	11	12	
EDP_INT_ML_P<1> (76)	13	14	BKLT_PWM_TCON2MLB (OUT, 48 114)
	15	16	BKLT_PWM_MLB2TCON (IN, 20 114)
EDP_INT_ML_N<2> (76)	17	18	
EDP_INT_ML_P<2> (76)	19	20	
	21	22	
EDP_INT_ML_N<3> (76)	23	24	I2C_BKLT_SDA (BI, 111 114)
EDP_INT_ML_P<3> (76)	25	26	I2C_BKLT_SCL (IN, 111 114)
	27	28	SMBUS_SMC_0_S0_SDA (BI, 49 114)
	29	30	SMBUS_SMC_0_S0_SCL (IN, 49 114)
MIPI_DATA_CONN_N (38 BI)	31	32	
MIPI_DATA_CONN_P (38 BI)	33	34	I2C_ALS_SDA (BI, 42 114)
	35	36	I2C_ALS_SCL (IN, 42 114)
MIPI_CLK_CONN_N (38 IN)	37	38	I2C_CAM_SCL (IN, 37 38 114)
MIPI_CLK_CONN_P (38 IN)	39	40	I2C_CAM_SDA (BI, 37 38 114)
	41	42	
	PWR		
PP5V_S0SW_LCD (114 76)	45	46	PP5V_S0_ALSCAM_F (38 114)
	GND		
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	

EDP_INT_ML_P<0> (IN, 114 111)	=	EDP_INT_ML_P<0> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<0> (IN, 114 111)	=	EDP_INT_ML_N<0> (76) MAKE_BASE=TRUE
EDP_INT_ML_P<1> (IN, 114 111)	=	EDP_INT_ML_P<1> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<1> (IN, 114 111)	=	EDP_INT_ML_N<1> (76) MAKE_BASE=TRUE
EDP_INT_ML_P<2> (IN, 114 111)	=	EDP_INT_ML_P<2> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<2> (IN, 114 111)	=	EDP_INT_ML_N<2> (76) MAKE_BASE=TRUE
EDP_INT_ML_P<3> (IN, 114 111)	=	EDP_INT_ML_P<3> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<3> (IN, 114 111)	=	EDP_INT_ML_N<3> (76) MAKE_BASE=TRUE
EDP_AUXCH_C_P (BI, 113 111)	=	EDP_AUXCH_C_P (76 114) MAKE_BASE=TRUE
EDP_AUXCH_C_N (BI, 113 111)	=	EDP_AUXCH_C_N (76 114) MAKE_BASE=TRUE

BOM_COST_GROUP=DISPLAY

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: 051-00647
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REVISION: 10.0.0
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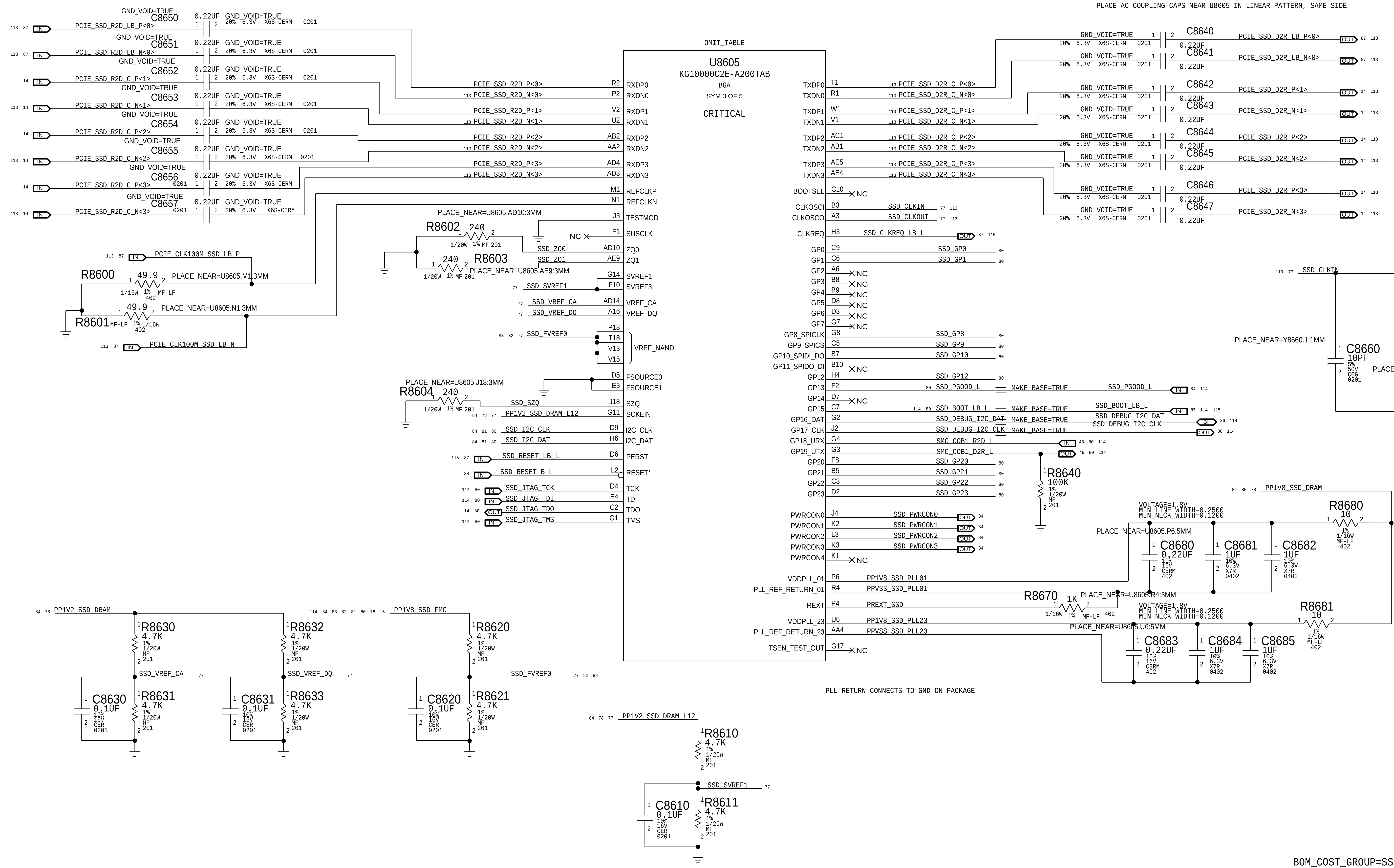

PLACE AC COUPLING CAPS NEAR U8605 IN LINEAR PATTERN, SAME SIDE
U8605
KG10000C2E-A200TAB
BGA
SYM 3 OF 5
CRITICAL
OMIT_TABLE
PCIE_SSD_R2D_LB_P<0>
PCIE_SSD_R2D_LB_N<0>
PCIE_SSD_R2D_C_P<1>
PCIE_SSD_R2D_C_N<1>
PCIE_SSD_R2D_C_P<2>
PCIE_SSD_R2D_C_N<2>
PCIE_SSD_R2D_C_P<3>
PCIE_SSD_R2D_C_N<3>
C8650 C8651 C8652 C8653 C8654 C8655 C8656 C8657
0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PCIE_SSD_D2R_LB_P<0>
PCIE_SSD_D2R_LB_N<0>
PCIE_SSD_D2R_P<1>
PCIE_SSD_D2R_N<1>
PCIE_SSD_D2R_P<2>
PCIE_SSD_D2R_N<2>
PCIE_SSD_D2R_P<3>
PCIE_SSD_D2R_N<3>
C8640 C8641 C8642 C8643 C8644 C8645 C8646 C8647
PCIE_CLK100M_SSD_LB_P
PCIE_CLK100M_SSD_LB_N
R8600 49.9 PLACE_NEAR=U8605.M1:3MM
R8601 49.9 PLACE_NEAR=U8605.N1:3MM
R8602 240 PLACE_NEAR=U8605.AD10:3MM
R8603 240 PLACE_NEAR=U8605.AE9:3MM
R8604 240 PLACE_NEAR=U8605.J18:3MM
SSD_ZQ0 SSD_ZQ1 SSD_SVREF1 SSD_VREF_CA SSD_VREF_DQ SSD_FVREF0 SSD_SZQ
PP1V2_SSD_DRAM_L12
SSD_I2C_CLK SSD_I2C_DAT SSD_RESET_LB_L SSD_RESET_B_L
SSD_JTAG_TCK SSD_JTAG_TDI SSD_JTAG_TDO SSD_JTAG_TMS
VREF_NAND
SSD_CLKIN SSD_CLKOUT SSD_CLKREQ_LB_L
SSD_GP0 SSD_GP1 SSD_GP8 SSD_GP9 SSD_GP10 SSD_GP12
SSD_PGOOD_L SSD_BOOT_LB_L SSD_DEBUG_I2C_DAT SSD_DEBUG_I2C_CLK
MAKE_BASE=TRUE
SMC_OOB1_R2D_L SMC_OOB1_D2R_L
SSD_GP20 SSD_GP21 SSD_GP22 SSD_GP23
R8640 100K
SSD_PWRCON0 SSD_PWRCON1 SSD_PWRCON2 SSD_PWRCON3
PP1V8_SSD_PLL01 PPVSS_SSD_PLL01 PREXT_SSD PP1V8_SSD_PLL23 PPVSS_SSD_PLL23
R8670 1K PLACE_NEAR=U8605.R4:3MM
PP1V8_SSD_DRAM
R8680 10
R8681 10
VOLTAGE=1.8V MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.1200
PLACE_NEAR=U8605.P6:5MM
PLACE_NEAR=U8605.U6:5MM
C8680 0.22UF C8681 1UF C8682 1UF
C8683 0.22UF C8684 1UF C8685 1UF
PLL RETURN CONNECTS TO GND ON PACKAGE
R8660 1M
R8661 240
Y8660 2.00X1.60-SM 25MHZ-30PPM-6PF-120OHM
C8660 10PF C8661 10PF
SSD_CLKOUT_R
PLACE_NEAR=Y8660.1:1MM
PLACE_NEAR=U8605.B3:4MM
PLACE_NEAR=U8605.A3:4MM
PLACE_NEAR=Y8660.3:1MM
PP1V2_SSD_DRAM
PP1V8_SSD_FMC
R8630 4.7K R8631 4.7K C8630 0.1UF SSD_VREF_CA
R8632 4.7K R8633 4.7K C8631 0.1UF SSD_VREF_DQ
R8620 4.7K R8621 4.7K C8620 0.1UF SSD_FVREF0
R8610 4.7K R8611 4.7K C8610 0.1UF SSD_SVREF1

BOM_COST_GROUP=SSD

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POLARIS_CONTROLLER

Apple Inc.

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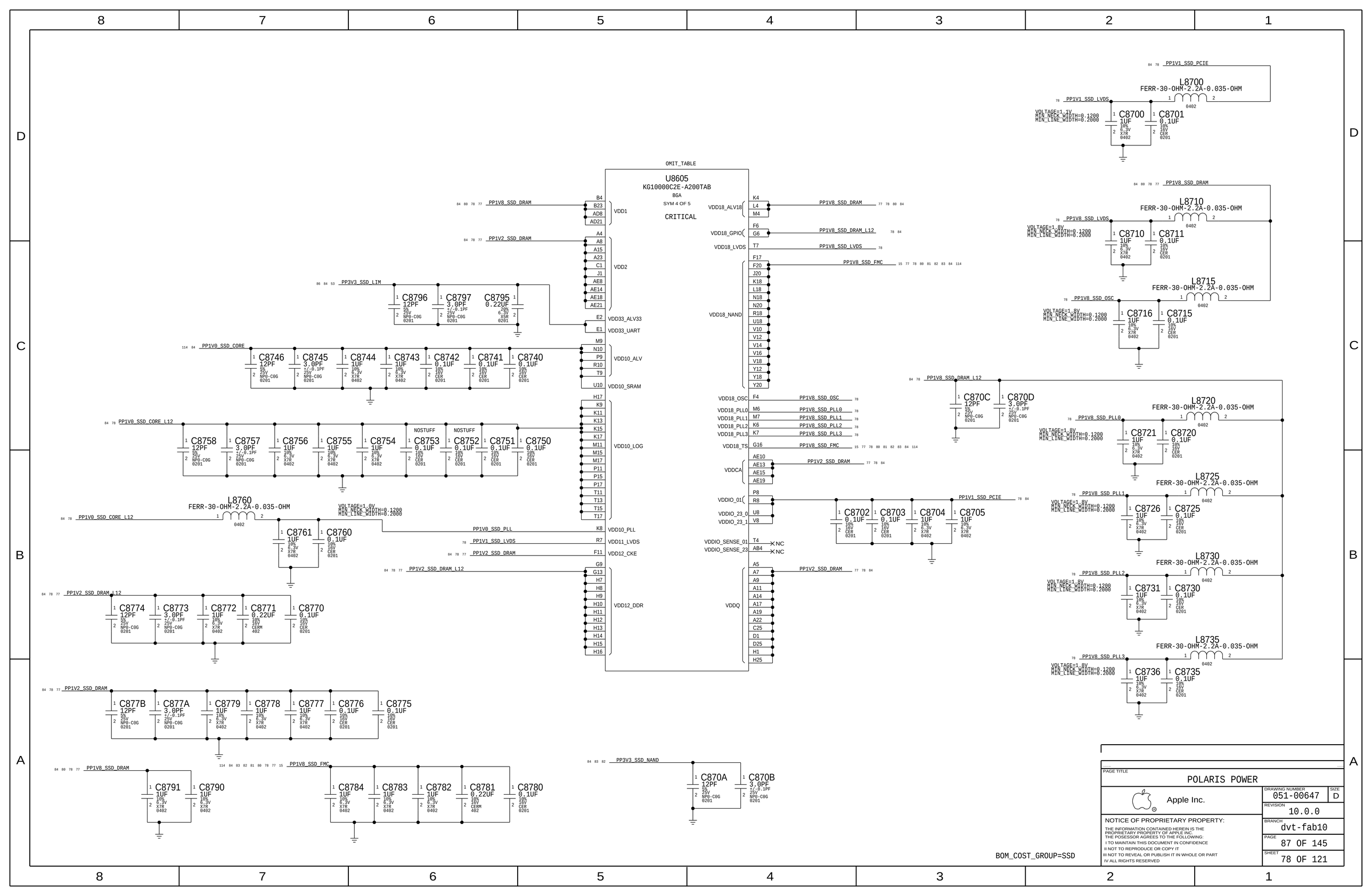

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OMIT_TABLE

U8605

KG10000C2E-A200TAB

BGA

SYM 5 OF 5

CRITICAL

A1		L1	
A2		M2	
A10		N2	
A24		N3	
A25		N4	
B1		N6	
B2		N7	
B6		N8	
B12		P1	
B14		P3	
B21		R3	
B24		R6	
B25		T2	
C4		T3	
C8		T6	
C14		T8	
C16		U1	
C18		U3	
C20		U4	
D10		U7	
D12		V3	
D15		V4	VSSIO
D23		V6	
E25		W2	
F7		W3	
F9		W4	
F14		W8	
G10		Y1	
G15		Y2	
G19		Y3	
G22		Y4	
G24		AA1	
H2		AA3	
J6		AB3	
J7		AB5	
J8		AC2	
J10		AC3	
J12		AC4	
J14		AC5	
J16		AD1	
K19		AD2	
K23		AD5	
K25		AD6	
L6		AE1	
L7		AE2	
L8	VSSI	AE3	
L10		AE6	
L12		AE7	
L14			
L16			
M3		F3	VSS18_OSC
M8		P7	
M18		V7	VSS_LVDS
N16			
N23			
N25			
R12			
R14			
R16			
R19			
R24			
U12			
U14			
U16			
U23			
V9			
V11			
V19			
V25			
W10			
W14			
W17			
Y23			
AA25			
AB16			
AB20			
AB23			
AC9			
AC13			
AD11			
AD17			
AD22			
AD24			
AD25			
AE24			
AE25			

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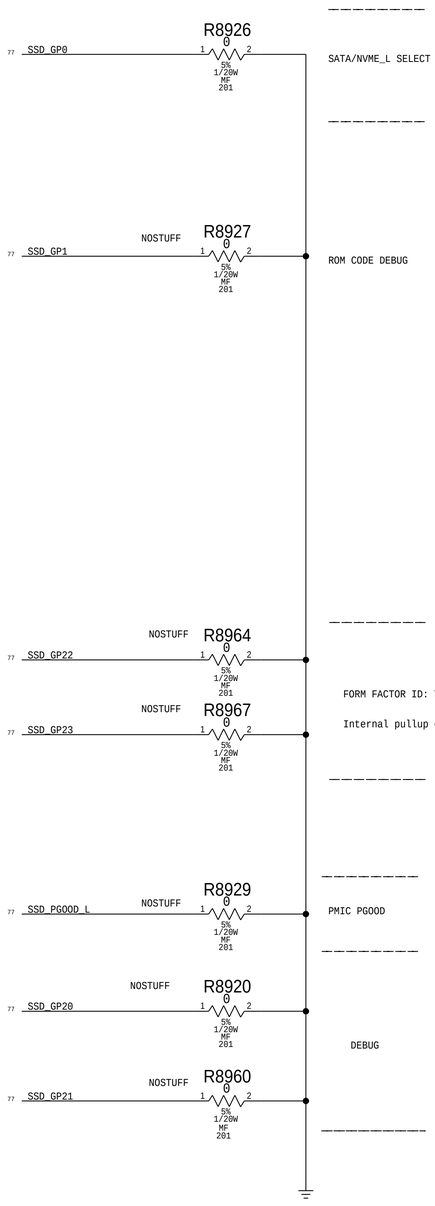

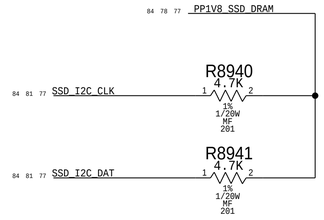

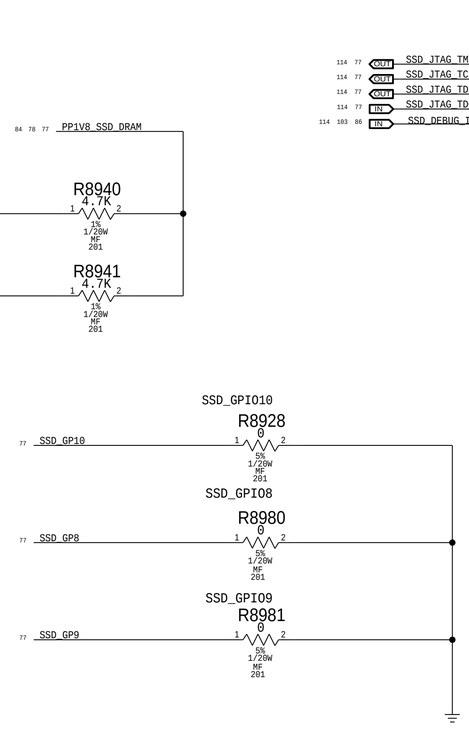

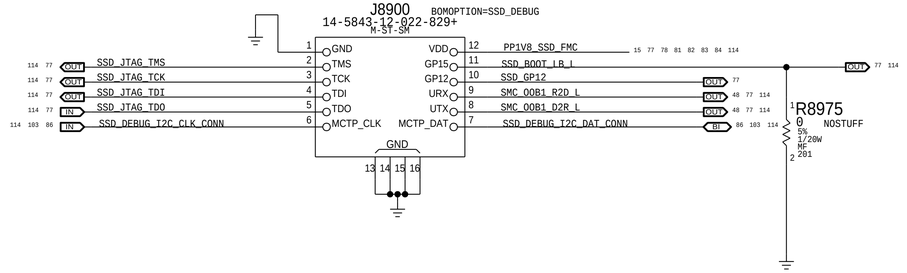

SSD RELATED BOM Groups

BOM GROUP	BOM OPTIONS
SSD_CONFIG:256GB	SSD_GPIO9,NAND_TYPE:256GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:512GB	SSD_GPIO8,NAND_TYPE:512GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:1TB	NAND_TYPE:1TB,SSD_CTRL_TYPE:8GBIT
SSD_CONFIG:2TB	SSD_GPIO10,NAND_TYPE:2TB,SSD_CTRL_TYPE:8GBIT

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00149	4	NAND,1Z,64GBM,TOGG DDR2,64G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:256GB
335S00204	4	NAND,V3,128GBM,TOGG DDR2,256G,SSBGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:512GB
335S00205	4	NAND,V3,256GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:1TB
335S00219	4	NAND,V3,512GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:2TB

SSD Controller Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00154	1	POP,POLARIS+4GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:4GBIT
339S00155	1	POP,POLARIS+8GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:8GBIT

SSD DENSITY

SSD CONFIGURATIONS

CAPACITY	NAND APN	CONTROLLER APN	R8980/GPIO8	R8981/GPIO9	R8928/GPIO10
128 GB	-	-	STUFF-0	STUFF-0	STUFF-0
256 GB	335S00149	339S00154 (A2 4GB DRAM)	NOSTUFF-1	STUFF-0	NOSTUFF-1
512 GB	335S00204	339S00154 (A2 4GB DRAM)	STUFF-0	NOSTUFF-1	NOSTUFF-1
1 TB	335S00205	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	NOSTUFF-1
2 TB	335S00219	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	STUFF-0

BOM_COST_GROUP=SSD

PAGE TITLE: Connector

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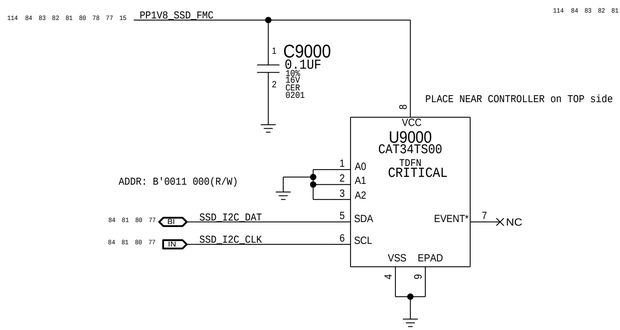

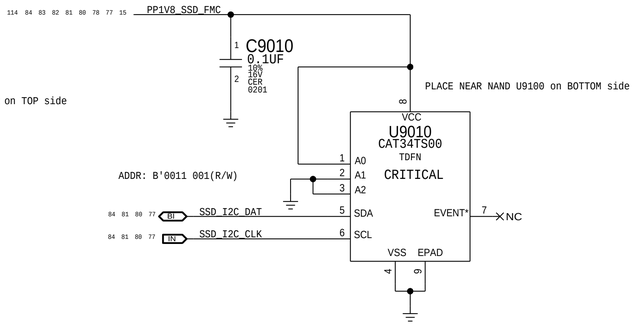

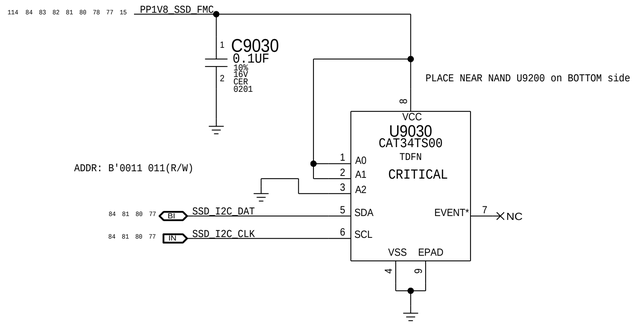

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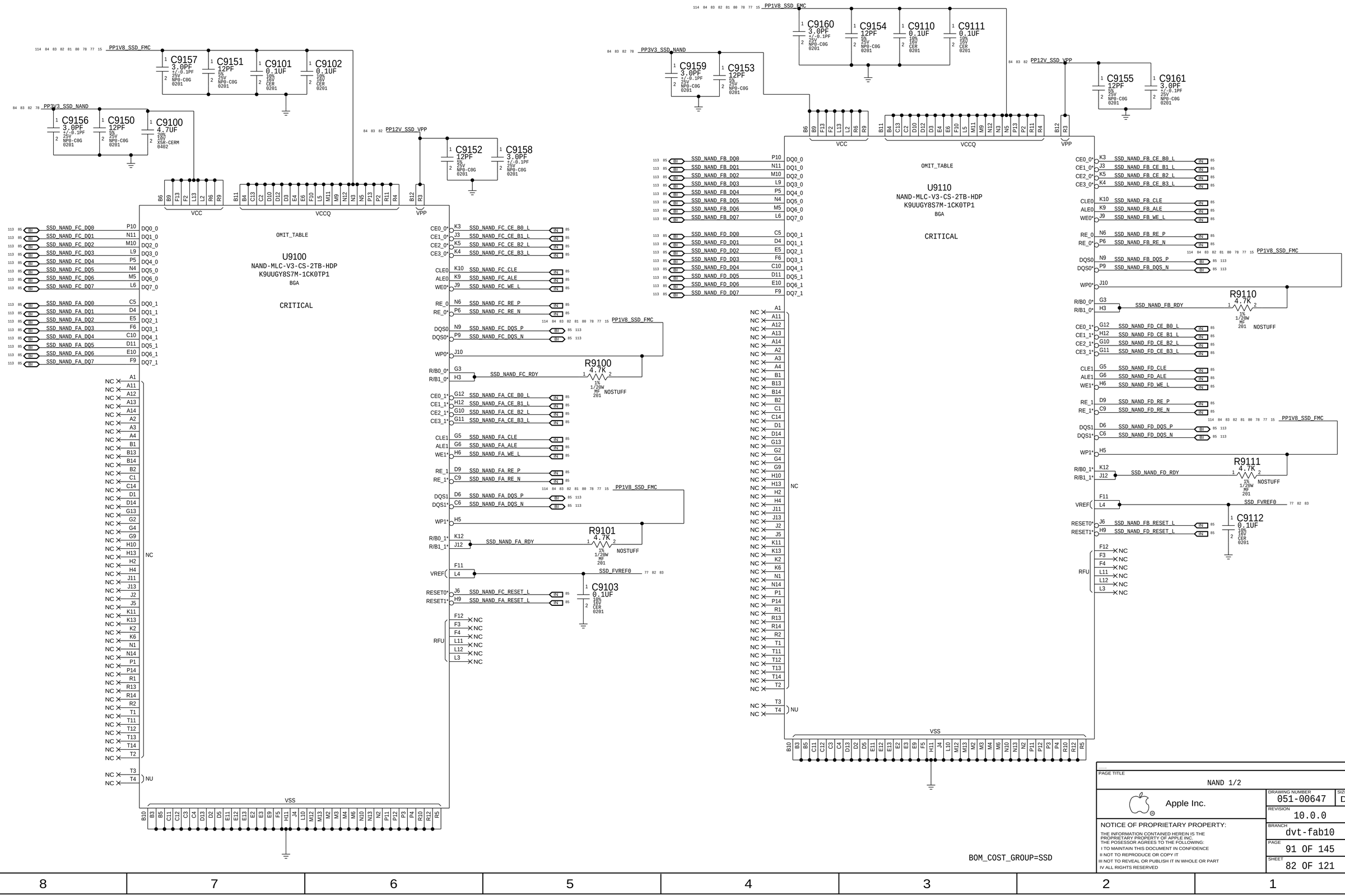
PP1V8_SSD_FMC
C9157 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9151 12PF 5% 25V NP0-C0G 0201
C9101 0.1UF 10% 16V CER 0201
C9102 0.1UF 10% 16V CER 0201
PP3V3_SSD_NAND
C9156 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9150 12PF 5% 25V NP0-C0G 0201
C9100 4.7UF 20% 10V X5R-CERM 0402
PP12V_SSD_VPP
C9152 12PF 5% 25V NP0-C0G 0201
C9158 3.0PF +/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9100
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FC_DQ0
SSD_NAND_FC_DQ1
SSD_NAND_FC_DQ2
SSD_NAND_FC_DQ3
SSD_NAND_FC_DQ4
SSD_NAND_FC_DQ5
SSD_NAND_FC_DQ6
SSD_NAND_FC_DQ7
SSD_NAND_FA_DQ0
SSD_NAND_FA_DQ1
SSD_NAND_FA_DQ2
SSD_NAND_FA_DQ3
SSD_NAND_FA_DQ4
SSD_NAND_FA_DQ5
SSD_NAND_FA_DQ6
SSD_NAND_FA_DQ7
NC
NU
VSS
SSD_NAND_FC_CE_B0_L
SSD_NAND_FC_CE_B1_L
SSD_NAND_FC_CE_B2_L
SSD_NAND_FC_CE_B3_L
SSD_NAND_FC_CLE
SSD_NAND_FC_ALE
SSD_NAND_FC_WE_L
SSD_NAND_FC_RE_P
SSD_NAND_FC_RE_N
SSD_NAND_FC_DQS_P
SSD_NAND_FC_DQS_N
SSD_NAND_FC_RDY
R9100 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FA_CE_B0_L
SSD_NAND_FA_CE_B1_L
SSD_NAND_FA_CE_B2_L
SSD_NAND_FA_CE_B3_L
SSD_NAND_FA_CLE
SSD_NAND_FA_ALE
SSD_NAND_FA_WE_L
SSD_NAND_FA_RE_P
SSD_NAND_FA_RE_N
SSD_NAND_FA_DQS_P
SSD_NAND_FA_DQS_N
SSD_NAND_FA_RDY
R9101 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
C9103 0.1UF 10% 16V CER 0201
SSD_NAND_FC_RESET_L
SSD_NAND_FA_RESET_L
RFU
PP1V8_SSD_FMC
PP3V3_SSD_NAND
C9160 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9154 12PF 5% 25V NP0-C0G 0201
C9110 0.1UF 10% 16V CER 0201
C9111 0.1UF 10% 16V CER 0201
C9159 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9153 12PF 5% 25V NP0-C0G 0201
PP12V_SSD_VPP
C9155 12PF 5% 25V NP0-C0G 0201
C9161 3.0PF +/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9110
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FB_DQ0
SSD_NAND_FB_DQ1
SSD_NAND_FB_DQ2
SSD_NAND_FB_DQ3
SSD_NAND_FB_DQ4
SSD_NAND_FB_DQ5
SSD_NAND_FB_DQ6
SSD_NAND_FB_DQ7
SSD_NAND_FD_DQ0
SSD_NAND_FD_DQ1
SSD_NAND_FD_DQ2
SSD_NAND_FD_DQ3
SSD_NAND_FD_DQ4
SSD_NAND_FD_DQ5
SSD_NAND_FD_DQ6
SSD_NAND_FD_DQ7
NC
NU
VSS
SSD_NAND_FB_CE_B0_L
SSD_NAND_FB_CE_B1_L
SSD_NAND_FB_CE_B2_L
SSD_NAND_FB_CE_B3_L
SSD_NAND_FB_CLE
SSD_NAND_FB_ALE
SSD_NAND_FB_WE_L
SSD_NAND_FB_RE_P
SSD_NAND_FB_RE_N
SSD_NAND_FB_DQS_P
SSD_NAND_FB_DQS_N
SSD_NAND_FB_RDY
R9110 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FD_CE_B0_L
SSD_NAND_FD_CE_B1_L
SSD_NAND_FD_CE_B2_L
SSD_NAND_FD_CE_B3_L
SSD_NAND_FD_CLE
SSD_NAND_FD_ALE
SSD_NAND_FD_WE_L
SSD_NAND_FD_RE_P
SSD_NAND_FD_RE_N
SSD_NAND_FD_DQS_P
SSD_NAND_FD_DQS_N
SSD_NAND_FD_RDY
R9111 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
C9112 0.1UF 10% 16V CER 0201
SSD_NAND_FB_RESET_L
SSD_NAND_FD_RESET_L
RFU
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PAGE TITLE
NAND 1/2
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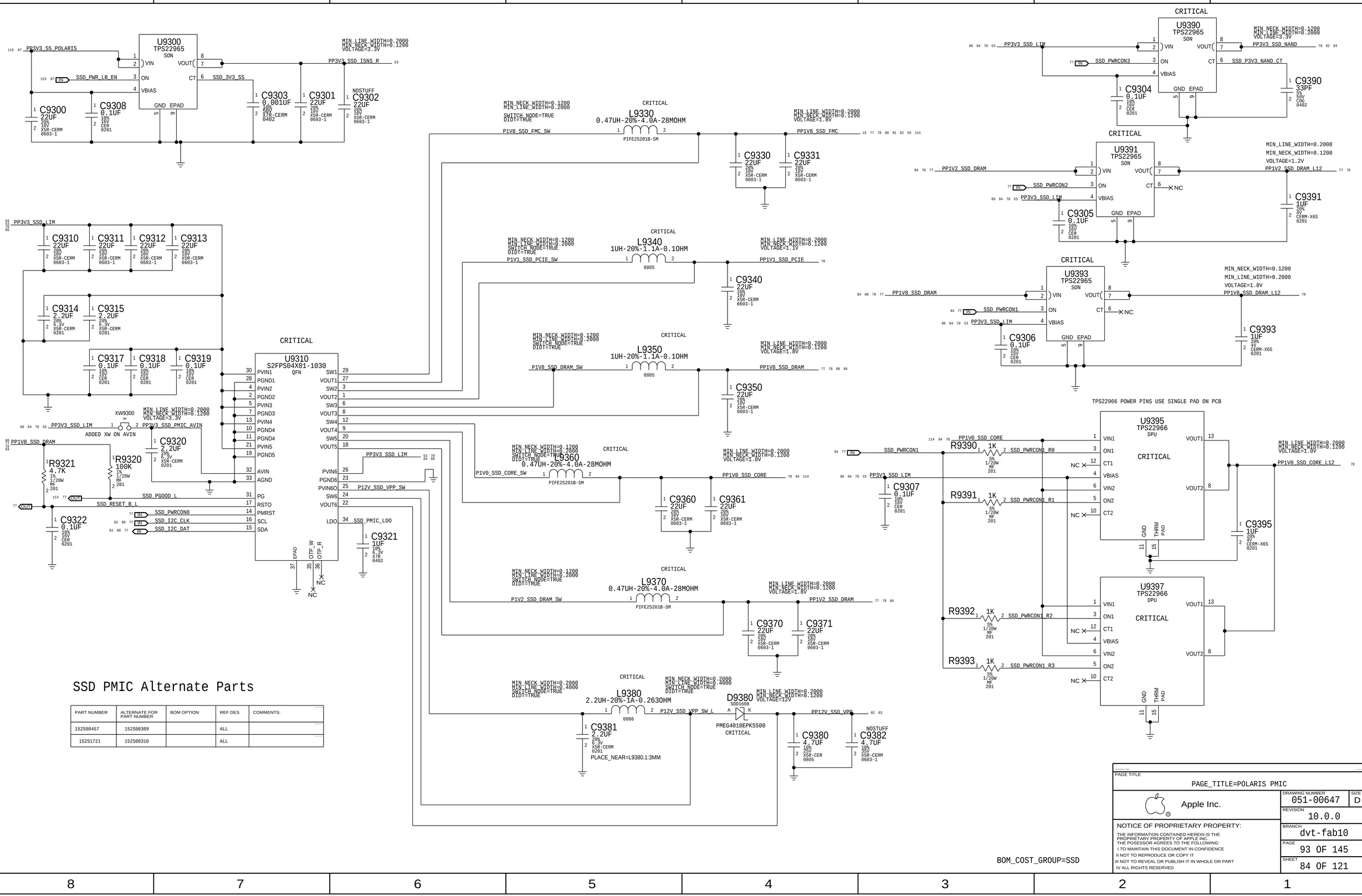

SSD PMIC Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00457	152S00309		ALL	
152S1721	152S00310		ALL	

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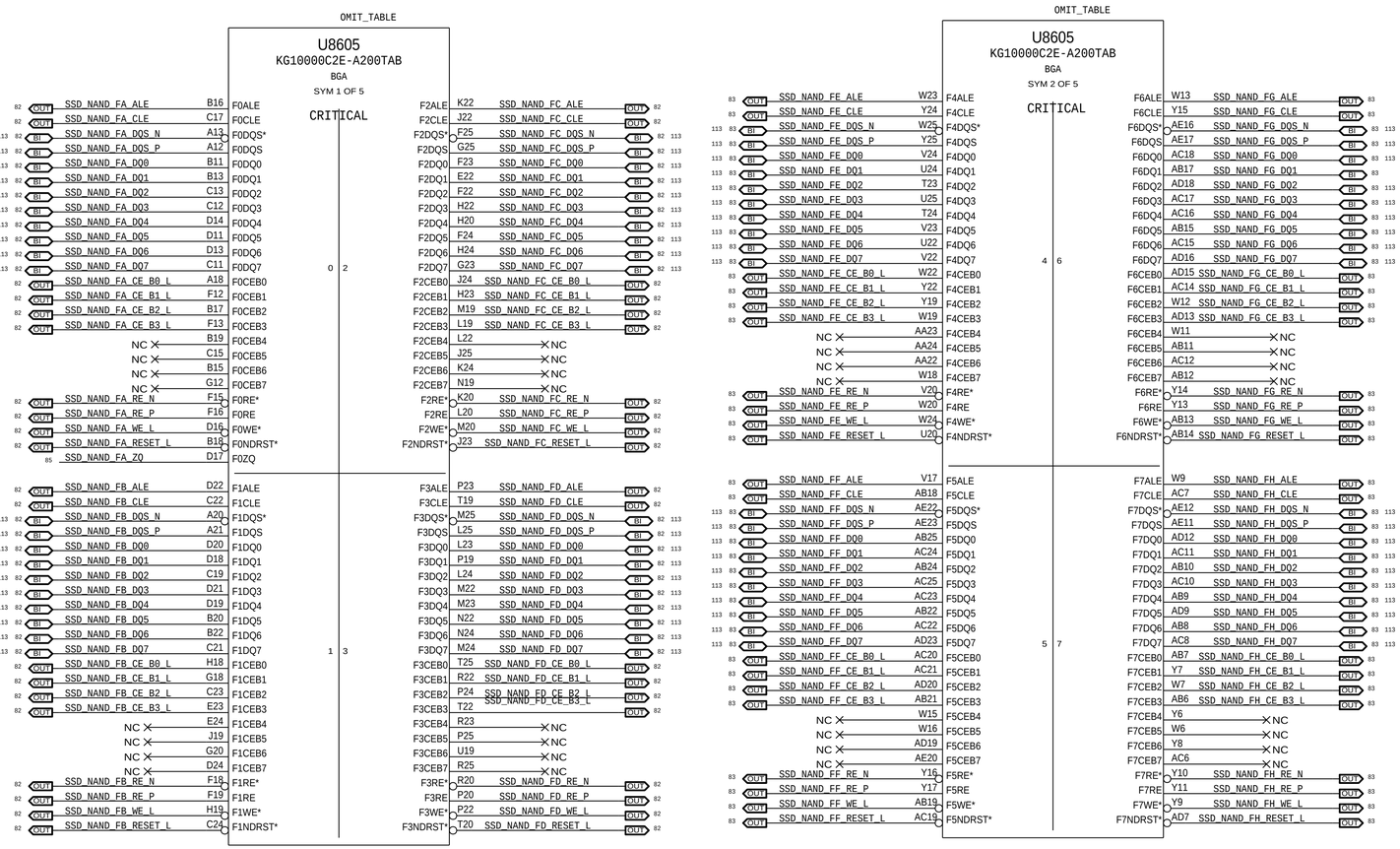

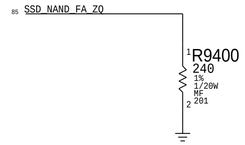

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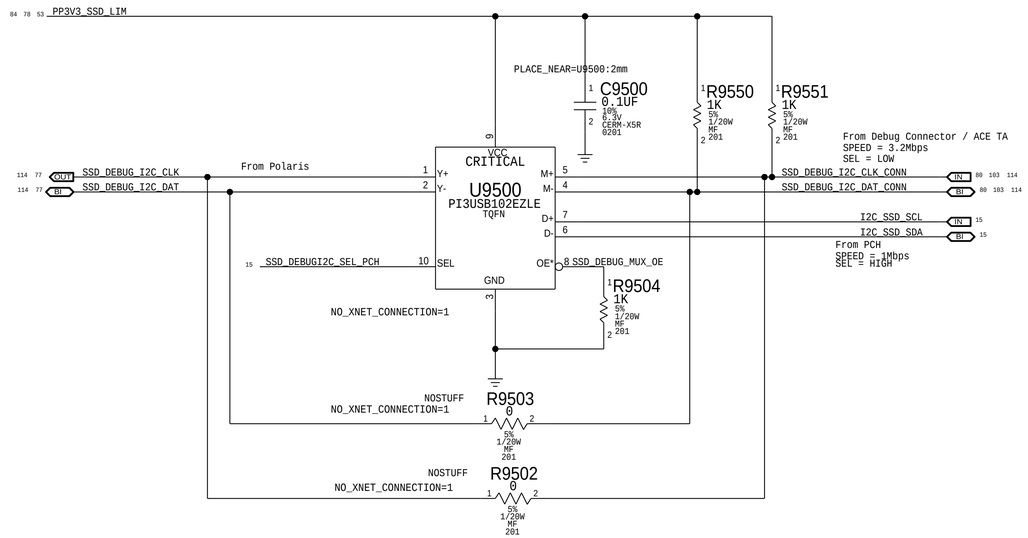

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SSD SUPPORT

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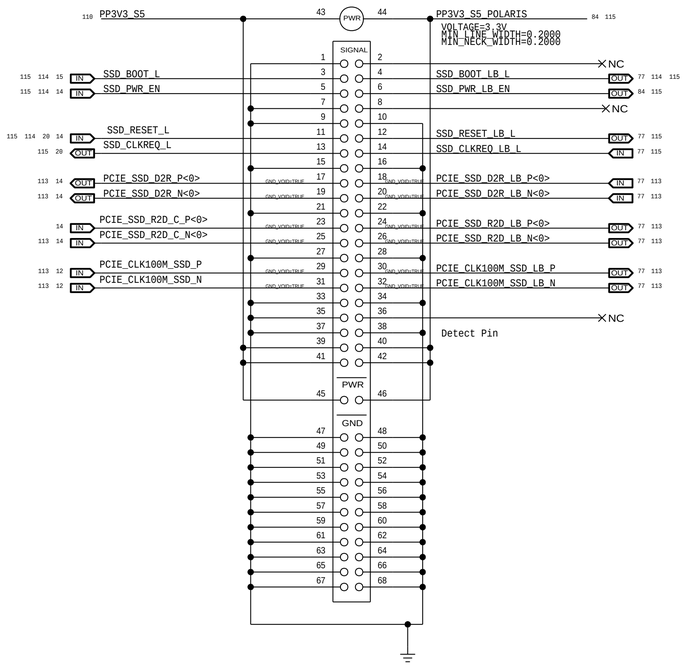
LIFEBOAT

J9600
20759-042E-02
F-ST-SM

PCH Side

SSD Side



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Lifeboat

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OMIT_TABLE

TP_DPMUX_UC_P10	B12	P10/WUE0*	
TP_DPMUX_UC_P11	A13	P11/WUE1*	
TP_DPMUX_UC_P12	A12	P12/WUE2*	
TP_DPMUX_UC_P13	B13	P13/WUE3*	
TP_DPMUX_UC_P14	D11	P14/WUE4*	
TP_DPMUX_UC_P15	C13	P15/WUE5*	
TP_DPMUX_UC_P16	C12	P16/WUE6*	
TP_DPMUX_UC_P17	D10	P17/WUE7*	
EG_RAIL1_EN	D13	P20	
EG_RAIL2_EN	E11	P21	
EG_RAIL3_EN	D12	P22	
EG_RAIL4_EN	F11	P23	
EG_RAIL5_EN	E13	P24	
EG_CLKREQ_SEL_L	E12	P25	
EG_RESET_L	F13	P26	
TP_FB_CLAMP	E10	P27	
LPC_AD<0>	A9	P30/LAD0	
LPC_AD<1>	D9	P31/LAD1	
LPC_AD<2>	C8	P32/LAD2	
LPC_AD<3>	B7	P33/LAD3	
LPC_FRAME_L	A8	P34/LFRAM*	
DPMUX_LRESET_L	D8	P35/LRESET*	
LPC_CLK24M_DPMUX_UC	D7	P36/LCLK	was 33MHz now 24MHz!!!
TP_DPMUX_UC_P37	D6	P37/SERIRQ	
TP_DPMUX_UC_P40	D4	P40/TMI0/TCMCYI0	
TP_DPMUX_UC_P41	A5	P41/TMO0/TCMCKI0/TCMMCI0	
TP_DPMUX_UC_P42	B4	P42/TCMCYI1	
LCD_FSS	A1	P43/TMI1/TCMCKI1/TCMMCI1	
LCD_MUX_SEL	C2	P44/TMO1/PWMU2B/TCMCYI2	
TP_DPMUX_UC_P45	B2	P45/PWMU3B/TCMCKI2/TCMMCI2	
TP_DPMUX_UC_P46	C1	P46/PWMU4B	
TP_DPMUX_UC_P47	C3	P47/PWMU5B	
DPMUX_UC_TX	G2	P50/FTXD	
DPMUX_UC_RX	F3	P51/FRXD	
TP_DPMUX_UC_P52	E4	P52/SCL0	
TP_DPMUX_UC_P60	L13	P60/KIN0*	
TP_DPMUX_UC_P61	K12	P61/KIN1*	
TP_DPMUX_UC_P62	K11	P62/KIN2*	
GMUX_SLP_S3_BUF_L	J12	P63/KIN3*	
TP_DPMUX_UC_P64	K13	P64/KIN4*	
TP_DPMUX_UC_P65	J10	P65/KIN5*	
TP_DPMUX_UC_P66	J11	P66/KIN6*	
TP_DPMUX_UC_P67	H12	P67/IRQ7*/KIN7*	
	N10	P70/AN0	NC
	M11	P71/AN1	NC
	L10	P72/AN2	NC
	N11	P73/AN3	NC
	N12	P74/AN4	NC
	M13	P75/AN5	NC
	N13	P76/AN6	NC
	L12	P77/AN7	NC
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TP_DPMUX_UC_P81	B6	P81/GA20	
TP_DPMUX_UC_P82	C7	P82/CLKRUN*	
TP_DPMUX_UC_P83	D5	P83/LPCPD*	
DPMUX_UC_TX	A6	P84/IRQ3*/TXD1	
DPMUX_UC_RX	B5	P85/IRQ4*/RXD1	
TP_LCD_IRQ	C6	P86/IRQ5*/SCK1	
GPU_GFX_OVERTEMP	J4	P90/IRQ2*	
DP_X_SNK0_HPD	G3	P91/IRQ1*	
DP_X_SNK1_HPD	H2	P92/IRQ0*	
DP_T_SNK0_HPD	G1	P93/IRQ12*	
DP_T_SNK1_HPD	H4	P94/IRQ13*	
SMC_GFX_PWR_LEVEL_L	G4	P95/IRQ14*	
GFX_SELF_THROTTLE	F4	P96/EXCL	
TP_DPMUX_UC_P97	F1	P97/SDA0/IRQ15*	

U9800 R4F2113NLG TLP-145V SYM 2 OF 3

OMIT_TABLE

I2C_DPMUX_UC_SDA	N3	PA0/KIN8*/SDA1	
I2C_DPMUX_UC_SCL	N1	PA1/KIN9*/SCL1	
DPMUX_UC_IRQ	M3	PA2/KIN10*/PS2AC	
	M2	PA3/KIN11*/PS2AD	NC
	N2	PA4/KIN12*/PS2BC	NC
	L1	PA5/KIN13*/PS2BD	NC
SMC_GFX_OVERTEMP	K3	PA6/KIN14*/PS2CC	
TP_FB_CLAMP_TOGGLE_REQ_L	L2	PA7/KIN15*/PS2CD	
TP_DPA_EG_HPD	B8	PB0/LSMI*	
DP_X_SNK0_HPD_EG	C9	PB1/LSCI	
DP_X_SNK1_HPD_EG	B9	PB2/RI*/PWMU0B	
DP_T_SNK0_HPD_EG	A10	PB3/DCD*/PWMU1B	
DP_T_SNK1_HPD_EG	C10	PB4/DSR*/FSIDO	
GPU_GFX_PWR_LEVEL_L	B10	PB5/DTR*/FSIDI	
SMC_GFX_SELF_THROTTLE	C11	PB6/CTS*/FSICK	
DP_INT_EG_HPD	A11	PB7/RTS*/FSISS	
EDP_PANEL_PWR_EN	G11	PC0/TIOCA0/WUE8*	
EDP_BKLT_EN	G13	PC1/TIOCB0/WUE9*	
TP_DPMUX_UC_PC2	F12	PC2/TIOCC0/TCLKA/WUE10*	
TP_DPMUX_UC_PC3	H13	PC3/TIOCD0/TCLKB/WUE11*	
LCD_MUX_EN	G10	PC4/TIOCA1/WUE12*	
TP_LCD_MUX_REQ	G12	PC5/TIOCB1/TCLKC/WUE13*	
BKLT_PWM_MLB2TCON	H11	PC6/TIOCA2/WUE14*	
TP_DPMUX_UC_PC7	J13	PC7/TIOCB2/TCLKD/WUE15*	
TP_DPA_IG_HPD	M10	PD0/AN8	
DP_X_SNK0_HPD_IG	N9	PD1/AN9	
DP_X_SNK1_HPD_IG	K10	PD2/AN10	
DP_T_SNK0_HPD_IG	L8	PD3/AN11	
DP_T_SNK1_HPD_IG	M9	PD4/SSO	
TP_DPMUX_UC_PD5	N8	PD5/SSI	
TP_DPMUX_UC_PD6	K9	PD6/SSCK	
DP_INT_IG_HPD	L7	PD7/SCS	
DPMUX_UC_CLK32K	K1	PE0/EXEXCL	
DPMUX_UC_TCK	J3	PE1/ETCK	
DPMUX_UC_TDI	K2	PE2/ETDI	
DPMUX_UC_TDO	J1	PE3/ETDO	
DPMUX_UC_TMS	K4	PE4/ETMS	
DPMUX_UC_TRST_L	H3	PE5/ETRST*	
EG_LCD_PWR_EN	K5	PF0/IRQ8*/PWMU0A	
EG_BKLT_EN	N5	PF1/IRQ9*/PWMU1A	
PM_ALL_GPU_PGOOD	M6	PF2/IRQ10*/TMOY	
P5_S0GPU_PGOOD	L5	PF3/IRQ11*/TMOX	
GPUVCORE_PGOOD	M5	PF4/PWMU2A/EXDSR	
PVDDCI_PGOOD	N4	PF5/PWMU3A/EXDTR	
P1V8GPU_PGOOD	L4	PF6/PWMU4A/EXCTS	
P3V3_S0GPU_PGOOD	M4	PF7/PWMU5A/EXRTS	
NC_I2C_DPMUX_A_SDA	M8	PG0/EXIRQ8*/TMIX/SDAA	
NC_I2C_DPMUX_A_SCL	N7	PG1/EXIRQ9*/TMIY/SCLA	
	K8	PG2/EXIRQ10*/SDAB	NC
	K7	PG3/EXIRQ11*/SCLB	NC
	K6	PG4/EXIRQ12*/SDAC	NC
DPMUX_LRESET_L	N6	PG5/EXIRQ13*/SCLC	
TP_DPMUX_UC_PG6	M7	PG6/EXIRQ14*/SDAD	
DP_INT_HPD	L6	PG7/EXIRQ15*/SCLD	
EDP_IG_PANEL_PWR_EN	E2	PH0/IRQ6*	
EDP_IG_BKLT_EN	F2	PH1/EXIRQ7*	
DPMUX_UC_PECI	A4	PECI	
DPMUX_UC_PEVREF	B3	PEVREF	

CONNECT I2C TO LCD BKLT IC

DPMUX UC DEBUG HEADER

J9800 1909782 M-RT-SM

PP3V3_S0_DPMUX_UC_R	1
DPMUX_UC_TX	2
DPMUX_UC_RX	3
DPMUX_UC_RESET_L	4
	5
DPMUX_UC_MD1	6
	7
	8

DPMUX_DEBUG

R9890 10K 5% 1/20W MF 201 — DPMUX_XTAL:YES — PP3V3_S0 — DPMUX_UC_MDCKN

R9891 10K 5% 1/20W MF 201 — DPMUX_XTAL:NO

R9892 0 5% 1/20W MF 201 — DPMUX_XTAL:YES

Y9800 1.60X1.20MM-SM 24.000MHZ-38PPM-9.5PF-600HM — DBG_XTAL — DPMUX_UC_XTAL_R — DPMUX_UC_EXTAL_R

C9890 12PF 5% 50V C0G-CERM 0201 — DBG_XTAL

C9891 12PF 5% 50V C0G-CERM 0201 — DBG_XTAL

R9893 0 5% 1/20W MF 201 — DPMUX_XTAL:YES — DPMUX_UC_XTAL — DPMUX_UC_EXTAL

R9894

0 5% 1/20W MF 201 — DPMUX_UC_MD2_R — DPMUX_UC_MD2

Q9890 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 — DPMUX_UC_MD1

R9801

0 5% 1/16W MF-LF 402 — PP3V3_S4 — PP3V3_S3_DPMUX_UC_R MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V

R9800

0 5% 1/16W MF-LF 402 — PP3V3_S0 — PP3V3_S0_DPMUX_UC_R MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V

C9800 0.1UF 20% 10V X7R-CERM 0402

C9801 0.1UF 20% 10V X7R-CERM 0402

C9802 0.1UF 20% 10V X7R-CERM 0402

C9803 0.1UF 20% 10V X7R-CERM 0402

C9804 0.1UF 20% 10V X7R-CERM 0402

DPMUX_UC_VCL

C9805 0.47UF 10% 6.3V X6S-CERM 0402

DPMUX_UC_RESET_L — NOSTUFF R9802 0 5% 1/16W MF-LF 402 — DPMUX_LRESET_L

U9800 R4F2113NLG TLP-145V SYM 3 OF 3

OMIT_TABLE

AVCC	M12		
VCC	B1		
VCC	M1		
VCC	H10		
VCL	E1		
AVREF	L11		
VBAT	J2		
RES*	D3		
XTAL	A3	DPMUX_UC_XTAL	
EXTAL	A2	DPMUX_UC_EXTAL	
MDCKN	C4	DPMUX_UC_MDCKN	
MD1	D1	DPMUX_UC_MD1	
MD2	H1	DPMUX_UC_MD2	
NMI	E3	DPMUX_UC_NMI	
NC	E5	NC	
VSS	D2		
VSS	L3		
VSS	F10		
VSS	C5		
VSS	B11		
AVSS	L9		

R9850 10K 5% 1/20W MF 201 — DPMUX_XTAL:NO

DPMUX UC PULL-UPS

DPMUX_UC_NMI	R9810	10K	PP3V3_S0
DPMUX_UC_TRST_L	R9811	10K	
DPMUX_UC_MD1	R9812	10K	
DPMUX_UC_MD2	R9813	10K	
DPMUX_UC_CLK32K	R9814	10K	
DPMUX_UC_TCK	R9815	10K	
DPMUX_UC_TDI	R9816	10K	
DPMUX_UC_TDO	R9817	10K	
DPMUX_UC_TMS	R9818	10K	
EG_CLKREQ_SEL_L	R9819	100K	
SMC_GFX_PWR_LEVEL_L	R9842	100K	
LCD_MUX_EN	R9855	10K	
LCD_MUX_SEL	R9856	10K	NOSTUFF
DPMUX_UC_RESET_L	R9840	100K	NOSTUFF
	R9841	0	GMUX_SLP_S3_BUF_L

U9870 74LVC1G07GF SOT891

PP3V3_S5 — C9870 0.1UF 10% 6.3V X7R 0201

PP3V3_S0 — R9870 4.7K 5% 1/20W MF 201

PM_SLP_S3_L — A — Y — GMUX_SLP_S3_BUF_L — GMUX_SLP_S3_BUF_L

NC — 1 — NC — 5 — NC — GND — 3

NOSTUFF R9871 470K 5% 1/20W MF 201

MAKE_BASE=TRUE

DP 2:1 ANALOG MUX

PP3V3_S0 — C9850 0.1UF 20% 10V X7R-CERM 0402 — C9851 0.1UF 20% 10V X7R-CERM 0402

U9850 CBTL06142EEE TFBGA

CRITICAL

VDD	A2		
VDD	J4		
DP_INT_IG_ML_P<0>	B4	DIN1_0+	
DP_INT_IG_ML_N<0>	A4	DIN1_0-	
DP_INT_IG_ML_P<1>	B5	DIN1_1+	
DP_INT_IG_ML_N<1>	A5	DIN1_1-	
DP_INT_IG_ML_P<2>	B6	DIN1_2+	
DP_INT_IG_ML_N<2>	A6	DIN1_2-	
DP_INT_IG_ML_P<3>	A8	DIN1_3+	
DP_INT_IG_ML_N<3>	A9	DIN1_3-	
DP_INT_IG_AUX_P	H9	DAUX1+	
DP_INT_IG_AUX_N	J9	DAUX1-	
	H8	DDC_CLK1	NC
	J8	DDC_DAT1	NC
	J2	HPD_1	NC
DP_INT_EG_ML_P<0>	B8	DIN2_0+	
DP_INT_EG_ML_N<0>	B9	DIN2_0-	
DP_INT_EG_ML_P<1>	D8	DIN2_1+	
DP_INT_EG_ML_N<1>	D9	DIN2_1-	
DP_INT_EG_ML_P<2>	E8	DIN2_2+	
DP_INT_EG_ML_N<2>	E9	DIN2_2-	
DP_INT_EG_ML_P<3>	F8	DIN2_3+	
DP_INT_EG_ML_N<3>	F9	DIN2_3-	
DP_INT_EG_AUX_P	H6	DAUX2+	
DP_INT_EG_AUX_N	J6	DAUX2-	
	H5	DDC_CLK2	NC
	J5	DDC_DAT2	NC
	H3	HPD_2	NC
LCD_MUX_SEL	A1	GPU_SEL	
LCD_MUX_EN	B7	XSD*	
	C2	DDC_AUX_SEL	
GND	B3		
GND	C8		
GND	G8		
GND	H4		
GND	H7		
GND	C2		

DOUT_0+	B2	EDP_INT_ML_P<0>	OUT
DOUT_0-	B1	EDP_INT_ML_N<0>	OUT
DOUT_1+	D2	EDP_INT_ML_P<1>	OUT
DOUT_1-	D1	EDP_INT_ML_N<1>	OUT
DOUT_2+	E2	EDP_INT_ML_P<2>	OUT
DOUT_2-	E1	EDP_INT_ML_N<2>	OUT
DOUT_3+	F2	EDP_INT_ML_P<3>	OUT
DOUT_3-	F1	EDP_INT_ML_N<3>	OUT
AUX+	H2	EDP_AUXCH_C_P	BI
AUX-	H1	EDP_AUXCH_C_N	BI
HPDIN	J1	DPMUX_HPD_PD	

R9862 100K 1% 1/20W MF 201

DPMUX UC PULL-DOWNS

DPMUX_UC_RESET_L	R9820	10K	NOSTUFF
EG_RAIL1_EN	R9821	10K	
EG_RAIL2_EN	R9822	10K	
EG_RAIL3_EN	R9823	10K	
EG_RAIL4_EN	R9824	10K	
EG_RAIL5_EN	R9825	10K	
EDP_PANEL_PWR_EN	R9826	10K	
EDP_BKLT_EN	R9827	10K	
BKLT_PWM_MLB2TCON	R9828	10K	
DPMUX_UC_NMI	R9829	10K	NOSTUFF
DPMUX_UC_MD1	R9830	10K	NOSTUFF
DPMUX_UC_MD2	R9831	10K	NOSTUFF
DPMUX_UC_PECI	R9832	10K	
DPMUX_UC_PEVREF	R9833	10K	
EG_RESET_L	R9835	100K	
DP_X_SNK0_HPD_IG	R9836	100K	
DP_X_SNK0_HPD_EG	R9837	100K	
DP_X_SNK1_HPD_IG	R9838	100K	
DP_X_SNK1_HPD_EG	R9839	100K	
DP_INT_IG_HPD	R9845	100K	
DP_INT_EG_HPD	R9846	100K	
GPU_GFX_OVERTEMP	R9847	100K	
GFX_SELF_THROTTLE	R9848	100K	
SMC_GFX_OVERTEMP	R9849	100K	
SMC_GFX_SELF_THROTTLE	R9852	100K	
LCD_MUX_SEL	R9853	100K	
LCD_MUX_EN	R9854	100K	NOSTUFF

DP_T_SNK0_HPD_IG	R9872	100K	
DP_T_SNK0_HPD_EG	R9873	100K	
DP_T_SNK1_HPD_IG	R9874	100K	
DP_T_SNK1_HPD_EG	R9875	100K	

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SYNC_MASTER=dpmux SYNC_DATE=08/22/2015

PAGE TITLE: eDP Mux

Apple Inc.

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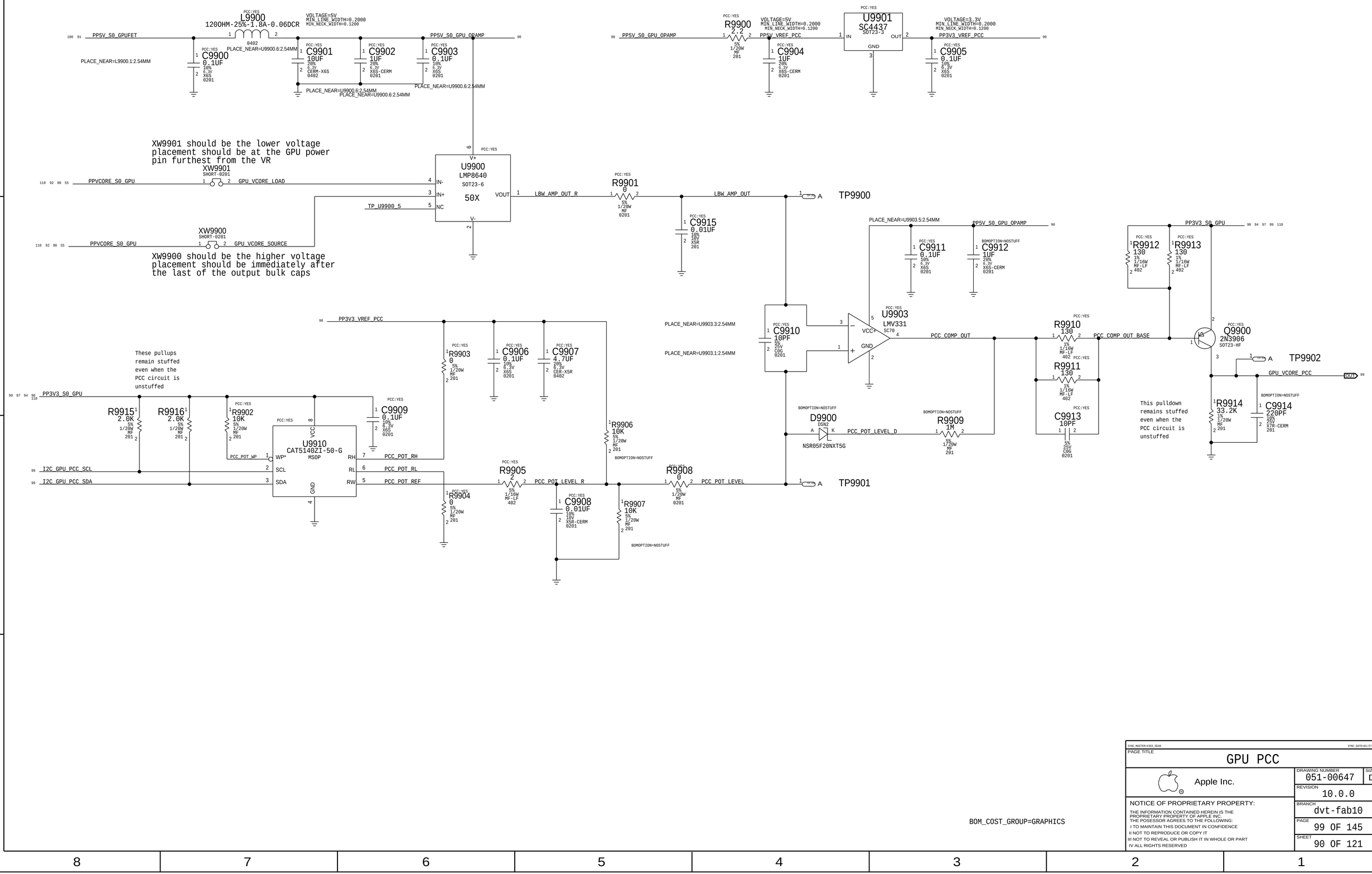
SHEET 89 OF 121



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PAGE TITLE	GPU PCC
Apple Inc.	DRAWING NUMBER 051-00647 SIZE D
	REVISION 10.0.0
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	PAGE 99 OF 145
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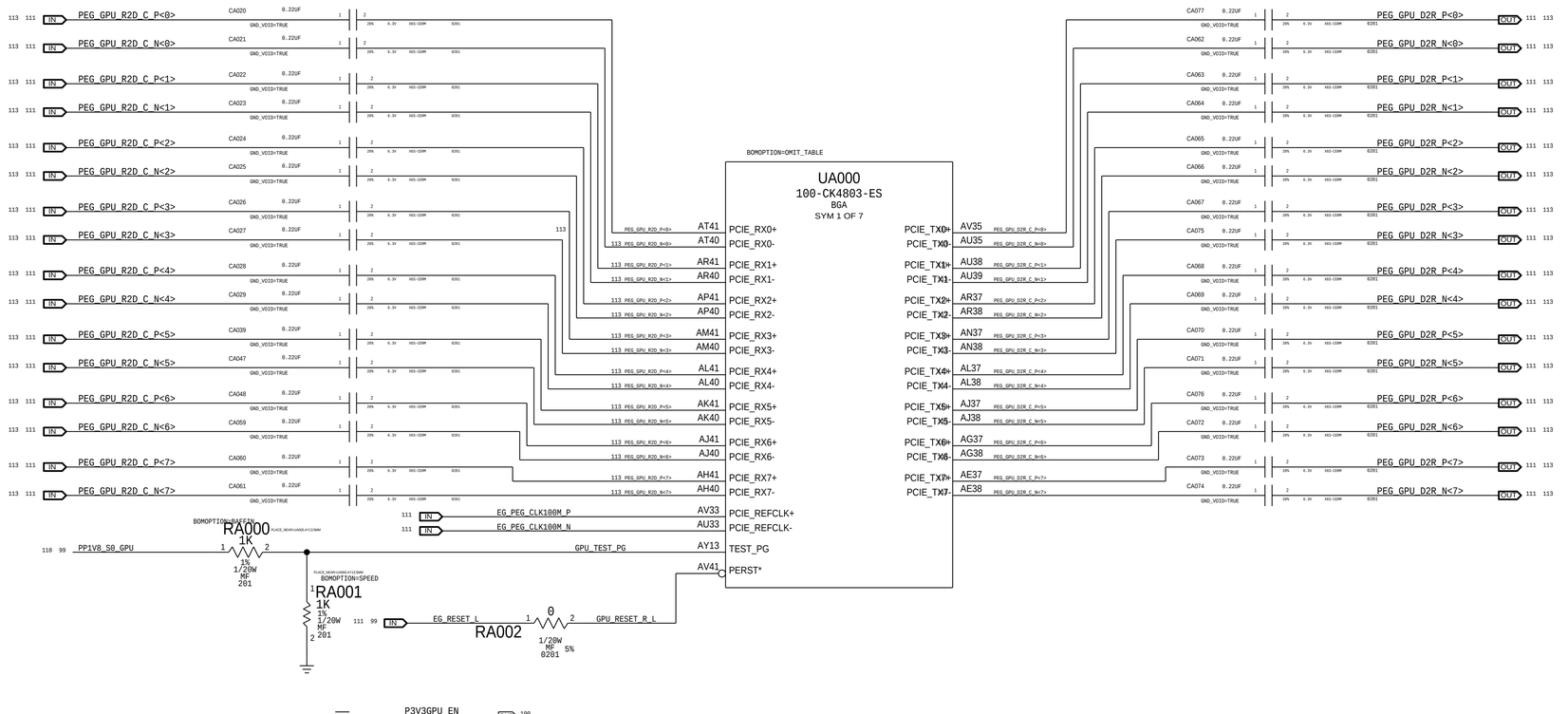

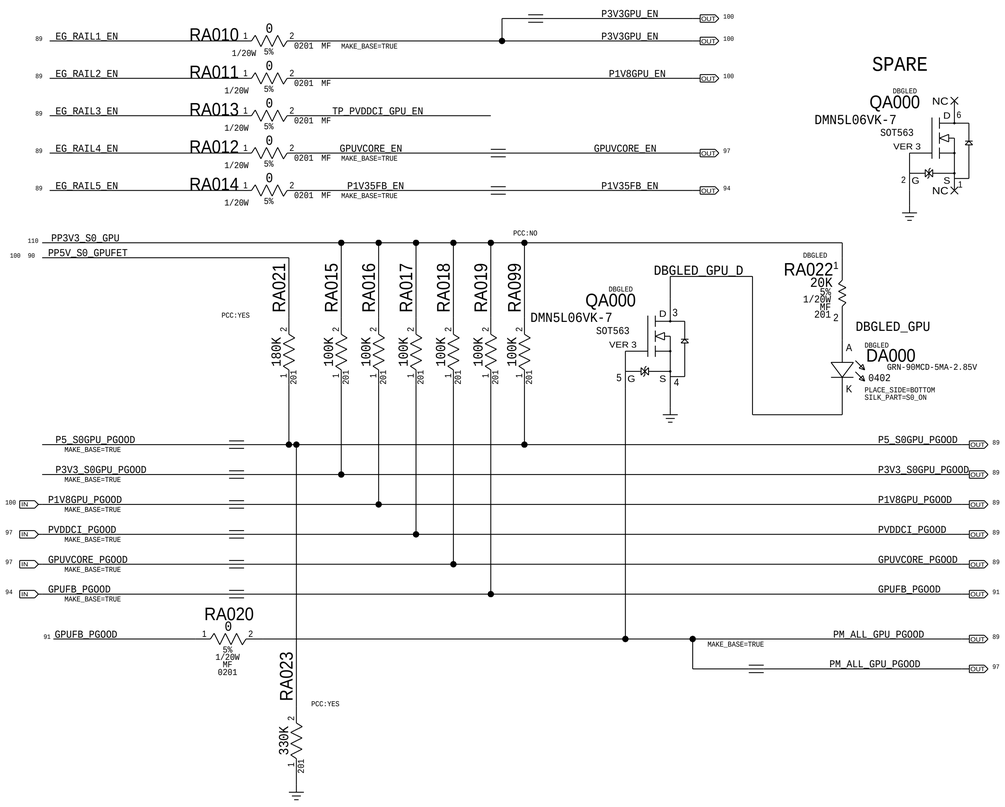

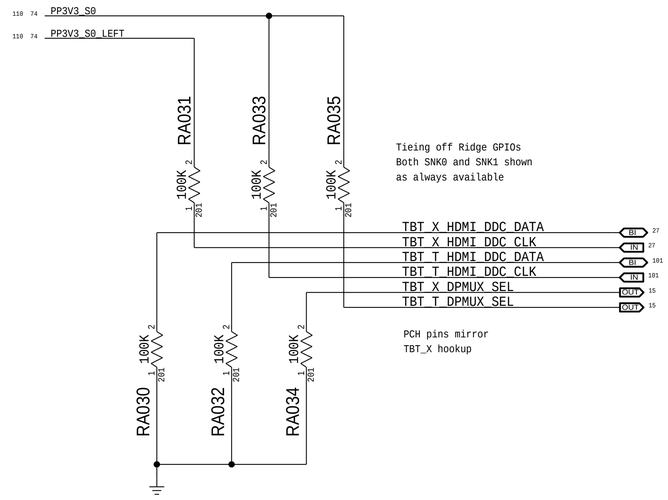

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	REVISION 10.0.0
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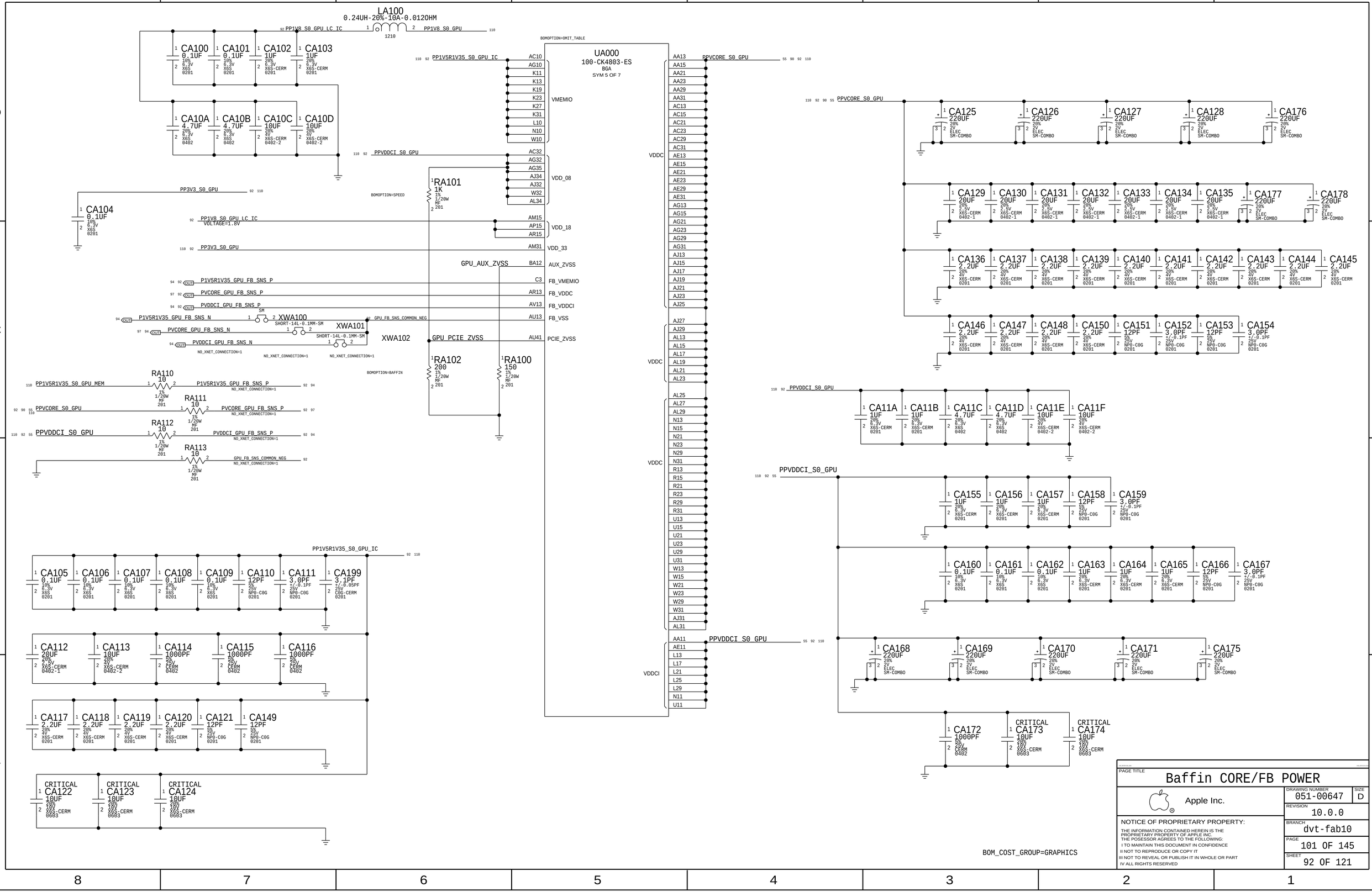
LA100
0.24UH-20%-10A-0.0120HM
1210
PP1V8_S0_GPU_LC_IC
PP1V8_S0_GPU
CA100 0.1UF 10% 6.3V X6S 0201
CA101 0.1UF 10% 6.3V X6S 0201
CA102 1UF 20% 6.3V X6S-CERM 0201
CA103 1UF 20% 6.3V X6S-CERM 0201
CA10A 4.7UF 20% 6.3V X6S 0402
CA10B 4.7UF 20% 6.3V X6S 0402
CA10C 10UF 20% 4V X6S-CERM 0402-2
CA10D 10UF 20% 4V X6S-CERM 0402-2
CA104 0.1UF 10% 6.3V X6S 0201
PP3V3_S0_GPU
PP1V8_S0_GPU_LC_IC
VOLTAGE=1.8V
PP3V3_S0_GPU
P1V5R1V35_GPU_FB_SNS_P
PVCORE_GPU_FB_SNS_P
PVDDCI_GPU_FB_SNS_P
P1V5R1V35_GPU_FB_SNS_N
PVCORE_GPU_FB_SNS_N
PVDDCI_GPU_FB_SNS_N
XWA100
SHORT-14L-0.1MM-SM
XWA101
XWA102
GPU_FB_SNS_COMMON_NEG
NO_XNET_CONNECTION=1
BOMOPTION=SPEED
RA101 1K 1% 1/20W MF 201
BOMOPTION=BAFFIN
RA102 200 1% 1/20W MF 201
RA100 150 1% 1/20W MF 201
RA110 10 1% 1/20W MF 201
RA111 10 1% 1/20W MF 201
RA112 10 1% 1/20W MF 201
RA113 10 1% 1/20W MF 201
PP1V5R1V35_S0_GPU_MEM
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
BOMOPTION=OMIT_TABLE
UA000
100-CK4803-ES
BGA
SYM 5 OF 7
PP1V5R1V35_S0_GPU_IC
PPVDDCI_S0_GPU
GPU_AUX_ZVSS
GPU_PCIE_ZVSS
VMEMIO
VDD_08
VDD_18
VDD_33
AUX_ZVSS
FB_VMEMIO
FB_VDDC
FB_VDDCI
FB_VSS
PCIE_ZVSS
VDDC
VDDCI
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
CA105 0.1UF 10% 6.3V X6S 0201
CA106 0.1UF 10% 6.3V X6S 0201
CA107 0.1UF 10% 6.3V X6S 0201
CA108 0.1UF 10% 6.3V X6S 0201
CA109 0.1UF 10% 6.3V X6S 0201
CA110 12PF 5% 25V NP0-C0G 0201
CA111 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA199 3.1PF +/-0.05PF 25V C0G-CERM 0201
CA112 20UF 20% 4V X6S-CERM 0402-1
CA113 10UF 20% 4V X6S-CERM 0402-2
CA114 1000PF 5% 25V CERM 0402
CA115 1000PF 5% 25V CERM 0402
CA116 1000PF 5% 25V CERM 0402
CA117 2.2UF 20% 4V X6S-CERM 0201
CA118 2.2UF 20% 4V X6S-CERM 0201
CA119 2.2UF 20% 4V X6S-CERM 0201
CA120 2.2UF 20% 4V X6S-CERM 0201
CA121 12PF 5% 25V NP0-C0G 0201
CA149 12PF 5% 25V NP0-C0G 0201
CRITICAL CA122 10UF 20% 10V X6S-CERM 0603
CRITICAL CA123 10UF 20% 10V X6S-CERM 0603
CRITICAL CA124 10UF 20% 10V X6S-CERM 0603
CA125 220UF 20% 2V ELEC SM-COMBO
CA126 220UF 20% 2V ELEC SM-COMBO
CA127 220UF 20% 2V ELEC SM-COMBO
CA128 220UF 20% 2V ELEC SM-COMBO
CA176 220UF 20% 2V ELEC SM-COMBO
CA129 20UF 20% 2.5V X6S-CERM 0402-1
CA130 20UF 20% 2.5V X6S-CERM 0402-1
CA131 20UF 20% 2.5V X6S-CERM 0402-1
CA132 20UF 20% 2.5V X6S-CERM 0402-1
CA133 20UF 20% 2.5V X6S-CERM 0402-1
CA134 20UF 20% 2.5V X6S-CERM 0402-1
CA135 20UF 20% 2.5V X6S-CERM 0402-1
CA177 220UF 20% 2V ELEC SM-COMBO
CA178 220UF 20% 2V ELEC SM-COMBO
CA136 2.2UF 20% 4V X6S-CERM 0201
CA137 2.2UF 20% 4V X6S-CERM 0201
CA138 2.2UF 20% 4V X6S-CERM 0201
CA139 2.2UF 20% 4V X6S-CERM 0201
CA140 2.2UF 20% 4V X6S-CERM 0201
CA141 2.2UF 20% 4V X6S-CERM 0201
CA142 2.2UF 20% 4V X6S-CERM 0201
CA143 2.2UF 20% 4V X6S-CERM 0201
CA144 2.2UF 20% 4V X6S-CERM 0201
CA145 2.2UF 20% 4V X6S-CERM 0201
CA146 2.2UF 20% 4V X6S-CERM 0201
CA147 2.2UF 20% 4V X6S-CERM 0201
CA148 2.2UF 20% 4V X6S-CERM 0201
CA150 2.2UF 20% 4V X6S-CERM 0201
CA151 12PF 5% 25V NP0-C0G 0201
CA152 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA153 12PF 5% 25V NP0-C0G 0201
CA154 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA11A 1UF 20% 6.3V X6S-CERM 0201
CA11B 1UF 20% 6.3V X6S-CERM 0201
CA11C 4.7UF 20% 6.3V X6S 0402
CA11D 4.7UF 20% 6.3V X6S 0402
CA11E 10UF 20% 4V X6S-CERM 0402-2
CA11F 10UF 20% 4V X6S-CERM 0402-2
CA155 1UF 20% 6.3V X6S-CERM 0201
CA156 1UF 20% 6.3V X6S-CERM 0201
CA157 1UF 20% 6.3V X6S-CERM 0201
CA158 12PF 5% 25V NP0-C0G 0201
CA159 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA160 0.1UF 10% 6.3V X6S 0201
CA161 0.1UF 10% 6.3V X6S 0201
CA162 0.1UF 10% 6.3V X6S 0201
CA163 1UF 20% 6.3V X6S-CERM 0201
CA164 1UF 20% 6.3V X6S-CERM 0201
CA165 1UF 20% 6.3V X6S-CERM 0201
CA166 12PF 5% 25V NP0-C0G 0201
CA167 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA168 220UF 20% 2V ELEC SM-COMBO
CA169 220UF 20% 2V ELEC SM-COMBO
CA170 220UF 20% 2V ELEC SM-COMBO
CA171 220UF 20% 2V ELEC SM-COMBO
CA175 220UF 20% 2V ELEC SM-COMBO
CA172 1000PF 5% 25V CERM 0402
CRITICAL CA173 10UF 20% 10V X6S-CERM 0603
CRITICAL CA174 10UF 20% 10V X6S-CERM 0603
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin CORE/FB POWER
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
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SHEET 92 OF 121
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PAGE TITLE

Baffin FRAME BUFFER I/F

Apple Inc.

DRAWING NUMBER	051-00647
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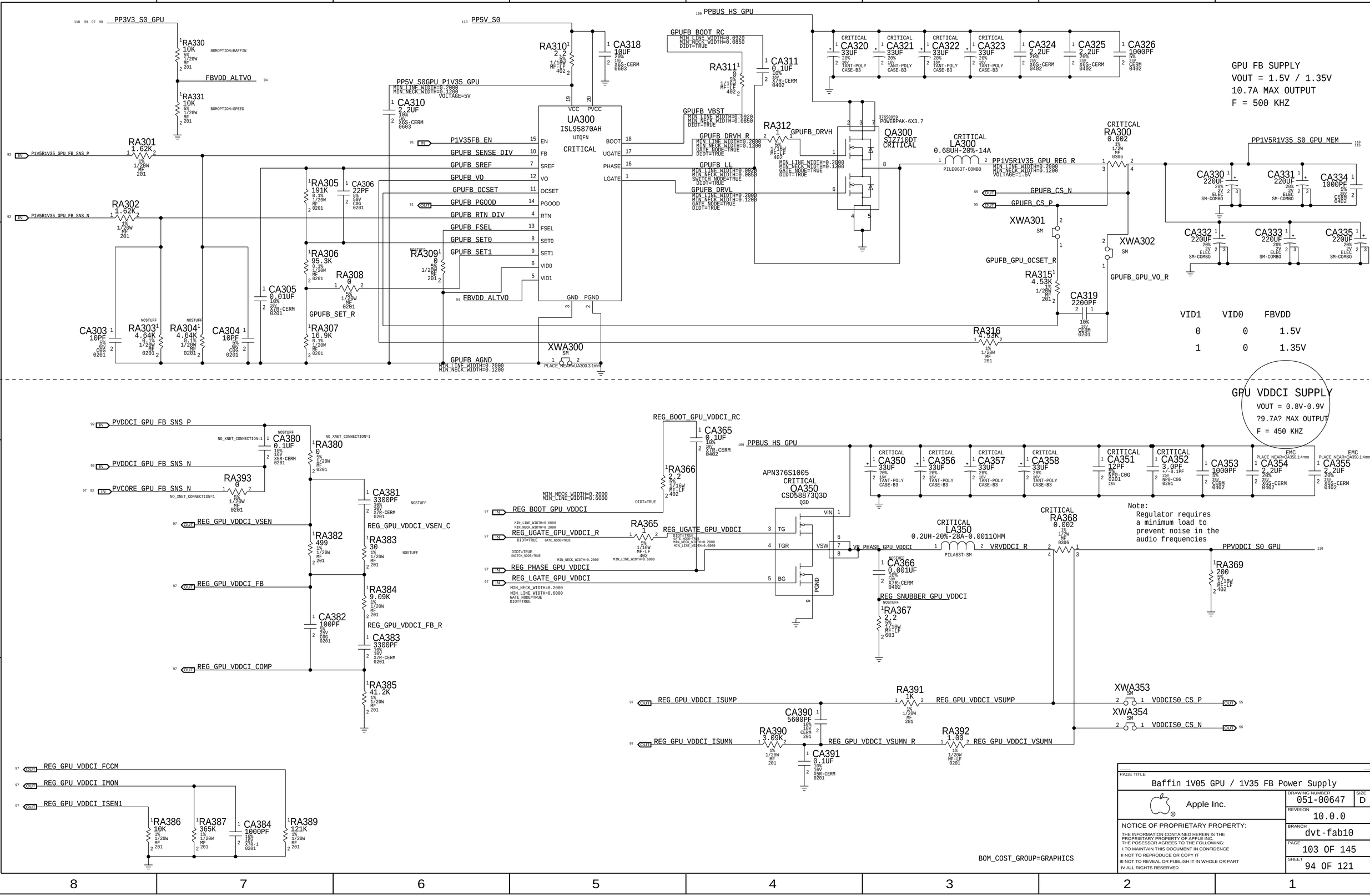
PP3V3_S0_GPU
RA330 10K 5% 1/20W MF 201 BOMOPTION=BAFFIN
FBVDD_ALTVO
RA331 10K 5% 1/20W MF 201 BOMOPTION=SPEED
PP5V_S0
RA310 2.2 5% 1/16W MF-LF 402
CA318 10UF 20% 10V X5S-CERM 0603
PP5V_S0GPU_P1V35_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
CA310 2.2UF 10% 10V X5S-CERM 0603
PPBUS_HS_GPU
GPUFB_BOOT_RC
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
DIDT=TRUE
RA311 0 5% 1/16W MF-LF 402
CA311 0.1UF 10% 16V X7R-CERM 0402
GPUFB_VBST
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
DIDT=TRUE
CRITICAL CA320 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA321 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA322 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA323 33UF 20% 16V TANT-POLY CASE-B3
CA324 2.2UF 20% 25V X5S-CERM 0402
CA325 2.2UF 20% 25V X5S-CERM 0402
CA326 1000PF 5% 25V C0G-CERM 0402
GPU FB SUPPLY
VOUT = 1.5V / 1.35V
10.7A MAX OUTPUT
F = 500 KHZ
UA300
ISL95870AH
UTQFN
CRITICAL
VCC PVCC BOOT UGATE PHASE LGATE
EN FB SREF VO OCSET PGOOD RTN FSEL SET0 SET1 VID0 VID1
GND PGND
P1V35FB_EN
GPUFB_SENSE_DIV
GPUFB_SREF
GPUFB_VO
GPUFB_OCSET
GPUFB_PGOOD
GPUFB_RTN_DIV
GPUFB_FSEL
GPUFB_SET0
GPUFB_SET1
FBVDD_ALTVO
GPUFB_AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
XWA300 SM PLACE_NEAR=UA300.3:1mm
RA312 1 5% 1/16W MF-LF 402
GPUFB_DRVH
GPUFB_DRVH_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
GATE_NODE=TRUE
DIDT=TRUE
GPUFB_LL
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
SWITCH_NODE=TRUE
DIDT=TRUE
GPUFB_DRVL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
GATE_NODE=TRUE
DIDT=TRUE
QA300 SIZ710DT CRITICAL 376S0959 POWERPAK-6X3.7
CRITICAL LA300 0.68UH-20%-14A PILE063T-COMBO
PP1V5R1V35_GPU_REG_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.5V
CRITICAL RA300 0.002 1% 1/2W MF 0306
PP1V5R1V35_S0_GPU_MEM
CA330 220UF 20% 2V ELEC SM-COMBO
CA331 220UF 20% 2V ELEC SM-COMBO
CA334 1000PF 5% 25V C0G 0402
CA332 220UF 20% 2V ELEC SM-COMBO
CA333 220UF 20% 2V ELEC SM-COMBO
CA335 220UF 20% 2V ELEC SM-COMBO
GPUFB_CS_N
GPUFB_CS_P
XWA301 SM
XWA302 SM
GPUFB_GPU_OCSET_R
GPUFB_GPU_VO_R
RA315 4.53K 1% 1/20W MF 201
CA319 2200PF 10% 16V CERM 0201
RA316 4.53K 1% 1/20W MF 201
VID1 VID0 FBVDD
0 0 1.5V
1 0 1.35V
PP1V5R1V35_GPU_FB_SNS_P
PP1V5R1V35_GPU_FB_SNS_N
RA301 1.62K 1% 1/20W MF 201
RA302 1.62K 1% 1/20W MF 201
RA305 191K 0.1% 1/20W MF 0201
CA306 22PF 5% 50V C0G 0201
RA306 95.3K 0.1% 1/20W MF 0201
RA307 16.9K 0.1% 1/20W MF 0201
RA308 0 5% 1/20W MF 0201
RA309 0 5% 1/20W MF 201 NOSTUFF
CA305 0.01UF 10% 16V X7R-CERM 0201
CA303 10PF 5% 50V C0G 0201
RA303 4.64K 0.1% 1/20W MF 0201 NOSTUFF
RA304 4.64K 0.1% 1/20W MF 0201 NOSTUFF
CA304 10PF 5% 50V C0G 0201
GPUFB_SET_R
GPU VDDCI SUPPLY
VOUT = 0.8V-0.9V
?9.7A? MAX OUTPUT
F = 450 KHZ
PVDDCI_GPU_FB_SNS_P
PVDDCI_GPU_FB_SNS_N
PVCORE_GPU_FB_SNS_N
CA380 0.1UF 10% 16V X5R-CERM 0201 NOSTUFF NO_XNET_CONNECTION=1
RA380 0 5% 1/20W MF 0201 NO_XNET_CONNECTION=1
RA393 0 5% 1/20W MF 0201 NO_XNET_CONNECTION=1
CA381 3300PF 10% 10V X7R-CERM 0201 NOSTUFF
REG_GPU_VDDCI_VSEN
REG_GPU_VDDCI_VSEN_C
RA382 499 1% 1/20W MF 201
RA383 30 1% 1/20W MF 201 NOSTUFF
REG_GPU_VDDCI_FB
REG_GPU_VDDCI_FB_R
RA384 9.09K 1% 1/20W MF 201
CA382 100PF 5% 25V C0G 0201
CA383 3300PF 10% 10V X7R-CERM 0201
REG_GPU_VDDCI_COMP
RA385 41.2K 1% 1/20W MF 201
REG_BOOT_GPU_VDDCI_RC
CA365 0.1UF 10% 16V X7R-CERM 0402
RA366 2.2 5% 1/16W MF-LF 402
PPBUS_HS_GPU
APN376S1005
CRITICAL
QA350
CSD58873Q3D
Q3D
CRITICAL CA350 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA356 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA357 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA358 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA351 12PF 5% NP0-C0G 0201 25V
CRITICAL CA352 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA353 1000PF 5% 25V C0G 0402
EMC CA354 2.2UF 20% 25V X5S-CERM 0402 PLACE_NEAR=QA350.1:4mm
EMC CA355 2.2UF 20% 25V X5S-CERM 0402 PLACE_NEAR=QA350.1:4mm
REG_BOOT_GPU_VDDCI
REG_UGATE_GPU_VDDCI_R
RA365 1 5% 1/16W MF-LF 402
REG_UGATE_GPU_VDDCI
REG_PHASE_GPU_VDDCI
REG_LGATE_GPU_VDDCI
VIN TG TGR VSW BG PGND
VR_PHASE_GPU_VDDCI
CRITICAL LA350 0.2UH-20%-28A-0.00110HM PILA63T-SM
VRVDDCI_R
CRITICAL RA368 0.002 1% 1/2W MF 0306
PPVDDCI_S0_GPU
RA369 200 5% 1/16W MF-LF 402
Note:
Regulator requires a minimum load to prevent noise in the audio frequencies
CA366 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
REG_SNUBBER_GPU_VDDCI
RA367 2.2 5% 1/10W MF-LF 603 NOSTUFF
REG_GPU_VDDCI_ISUMP
REG_GPU_VDDCI_ISUMN
RA391 1K 1% 1/20W MF 201
RA390 3.09K 1% 1/20W MF 201
CA390 5600PF 10% 16V CERM 201
CA391 0.1UF 10% 16V X5R-CERM 0201
REG_GPU_VDDCI_VSUMP
REG_GPU_VDDCI_VSUMN_R
RA392 1.00 1% 1/20W MF-LF 0201
REG_GPU_VDDCI_VSUMN
XWA353 SM VDDCIS0_CS_P
XWA354 SM VDDCIS0_CS_N
REG_GPU_VDDCI_FCCM
REG_GPU_VDDCI_IMON
REG_GPU_VDDCI_ISEN1
RA386 10K 1% 1/20W MF 201
RA387 365K 1% 1/20W MF 201
CA384 1000PF 10% 16V X7R-1 0201
RA389 121K 1% 1/20W MF 201
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin 1V05 GPU / 1V35 FB Power Supply
Apple Inc.
DRAWING NUMBER 051-00647
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REVISION 10.0.0
BRANCH dvt-fab10
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SYNC_MASTER=J80_SEAN SYNC_DATE=04/29/2015

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GDDR5 Frame Buffer A

DRAWING NUMBER 051-00647 SIZE D

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REVISION 10.0.0

BRANCH dvt-fab10

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8 7 6 5 4 3 2 1

D C B A

UA500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

UA550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

UA500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

UA550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

PP1V5R1V35_S0_GPU_MEM
CK TERMINATION - B0
RA501 60.4 1% 1/20W MF 201
RA502 60.4 1% 1/20W MF 201
FB_B0_CLK_P
FB_B0_CLK_N
PLACE_NEAR=UA500.J12:0.4MM
PLACE_NEAR=UA500.J11:0.4MM

PP1V5R1V35_S0_GPU_MEM
CK TERMINATION - B1
RA551 60.4 1% 1/20W MF 201
RA552 60.4 1% 1/20W MF 201
FB_B1_CLK_P
FB_B1_CLK_N
PLACE_NEAR=UA550.J12:0.4MM
PLACE_NEAR=UA550.J11:0.4MM

RA500 120 1% 1/20W MF 201
RA504 120 1% 1/20W MF 201
RA503 120 1% 1/20W MF 201
RA550 120 1% 1/20W MF 201
RA554 120 1% 1/20W MF 201
RA553 120 1% 1/20W MF 201

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FB_B0_A<7> FB_B0_A<1> FB_B0_A<0> FB_B0_A<6> FB_B0_CKE_L
FB_B0_CLK_P FB_B0_CLK_N FB_B0_CS_L FB_B0_WE_L FB_B0_CAS_L FB_B0_RAS_L
FB_B0_ZQ FB_B0_MF FB_B0_SEN FB_B_RESET_L FB_B0_ABI_L
FB_B0_EDC<0> FB_B0_EDC<1> FB_B0_EDC<2> FB_B0_EDC<3>
FB_B0_WCLK_P<0> FB_B0_WCLK_N<0> FB_B0_WCLK_P<1> FB_B0_WCLK_N<1>
FB_B0_DBI_L<0> FB_B0_DBI_L<1> FB_B0_DBI_L<2> FB_B0_DBI_L<3>
FB_B0_DQ<0> FB_B0_DQ<1> FB_B0_DQ<2> FB_B0_DQ<3> FB_B0_DQ<4> FB_B0_DQ<5> FB_B0_DQ<6> FB_B0_DQ<7> FB_B0_DQ<8> FB_B0_DQ<9> FB_B0_DQ<10> FB_B0_DQ<11> FB_B0_DQ<12> FB_B0_DQ<13> FB_B0_DQ<14> FB_B0_DQ<15> FB_B0_DQ<16> FB_B0_DQ<17> FB_B0_DQ<18> FB_B0_DQ<19> FB_B0_DQ<20> FB_B0_DQ<21> FB_B0_DQ<22> FB_B0_DQ<23> FB_B0_DQ<24> FB_B0_DQ<25> FB_B0_DQ<26> FB_B0_DQ<27> FB_B0_DQ<28> FB_B0_DQ<29> FB_B0_DQ<30> FB_B0_DQ<31>
FB_B0_A<8>

FB_B1_A<2> FB_B1_A<5> FB_B1_A<4> FB_B1_A<3>
FB_B1_A<7> FB_B1_A<1> FB_B1_A<0> FB_B1_A<6> FB_B1_CKE_L
FB_B1_CLK_P FB_B1_CLK_N FB_B1_CS_L FB_B1_WE_L FB_B1_CAS_L FB_B1_RAS_L
FB_B1_ZQ FB_B1_MF FB_B1_SEN FB_B_RESET_L FB_B1_ABI_L
FB_B1_EDC<0> FB_B1_EDC<1> FB_B1_EDC<2> FB_B1_EDC<3>
FB_B1_WCLK_P<0> FB_B1_WCLK_N<0> FB_B1_WCLK_P<1> FB_B1_WCLK_N<1>
FB_B1_DBI_L<0> FB_B1_DBI_L<1> FB_B1_DBI_L<2> FB_B1_DBI_L<3>
FB_B1_DQ<0> FB_B1_DQ<1> FB_B1_DQ<2> FB_B1_DQ<3> FB_B1_DQ<4> FB_B1_DQ<5> FB_B1_DQ<6> FB_B1_DQ<7> FB_B1_DQ<8> FB_B1_DQ<9> FB_B1_DQ<10> FB_B1_DQ<11> FB_B1_DQ<12> FB_B1_DQ<13> FB_B1_DQ<14> FB_B1_DQ<15> FB_B1_DQ<16> FB_B1_DQ<17> FB_B1_DQ<18> FB_B1_DQ<19> FB_B1_DQ<20> FB_B1_DQ<21> FB_B1_DQ<22> FB_B1_DQ<23> FB_B1_DQ<24> FB_B1_DQ<25> FB_B1_DQ<26> FB_B1_DQ<27> FB_B1_DQ<28> FB_B1_DQ<29> FB_B1_DQ<30> FB_B1_DQ<31>
FB_B1_A<8>

CA500 CA501 CA502 4.7UF 20% 6.3V X6S 0402
NOSTUFF CA498 12PF 5% 25V NP0-C0G 0201
CA503 CA504 CA505 4.7UF 20% 6.3V X6S 0402
CA499 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA506 CA507 CA508 CA509 1UF 20% 4V CERM-X6S 0201
CA510 CA511 CA512 CA513 1UF 20% 4V CERM-X6S 0201
CA514 CA515 CA516 CA517 1UF 20% 4V CERM-X6S 0201
CA518 CA519 CA530 CA521 0.1UF 10% 6.3V X6S 0201
CA522 CA523 CA524 CA525 0.1UF 10% 6.3V X6S 0201

CA550 CA551 CA552 4.7UF 20% 6.3V X6S 0402
CA553 CA554 CA555 4.7UF 20% 6.3V X6S 0402
CA556 CA557 CA558 CA559 1UF 20% 4V CERM-X6S 0201
CA560 CA561 CA562 CA563 1UF 20% 4V CERM-X6S 0201
CA564 CA565 CA566 0.1UF 10% 6.3V X6S 0201
CA567 0.1UF 10% 6.3V X6S 0201
CA568 CA569 CA570 0.1UF 10% 6.3V X6S 0201
CA571 0.1UF 10% 6.3V X6S 0201
CA572 CA573 CA574 0.1UF 10% 6.3V X6S 0201
CA575 0.1UF 10% 6.3V X6S 0201

RA530 549 1% 1/20W MF 201
CA531 820PF 10% 25V X7R-CERM 0201
RA531 1.33K 1% 1/20W MF 201
RA534 931 1% 1/20W MF 201
PLACE CLOSE TO U9000

RA580 549 1% 1/20W MF 201
CA581 820PF 10% 25V X7R-CERM 0201
RA581 1.33K 1% 1/20W MF 201
RA584 931 1% 1/20W MF 201
PLACE CLOSE TO U9050

NOSTUFF RA532 549 1% 1/20W MF 201
NOSTUFF CA532 CA533 820PF 10% 25V X7R-CERM 0201
NOSTUFF RA533 1.33K 1% 1/20W MF 201
NOSTUFF RA535 931 1% 1/20W MF 201

NOSTUFF RA582 549 1% 1/20W MF 201
NOSTUFF CA582 CA583 820PF 10% 25V X7R-CERM 0201
NOSTUFF RA583 1.33K 1% 1/20W MF 201
NOSTUFF RA585 931 1% 1/20W MF 201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0850

VDD VSS VDDQ VSSQ VREFC VREFD

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=J80_SEAN SYNC_DATE=04/29/2015

PAGE TITLE
GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER 051-00647
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00174	2	MOSFET,CTRL+SYNC,25V,4.1/1.4MO,QFN32,6x6	QA640,QA650	CRITICAL	

GPU CORE SUPPLY

VOUT = 0.75-1.00V

64.2A MAX OUTPUT

F = 450 KHZ

PP1V8_S0_GPU

PP5V_S0 — RA601 0 — VOLTAGE=5V — PP5V_S0_GFXIMVP_VDD — CA637 1.0UF

PP5V_S0_GFXIMVP_VDDP — CA638 1.0UF

PPBUS_HS_GPU — RA603 0 — VOLTAGE=12.6V — PPVIN_S0_GFXIMVP_VIN — CA639 0.22UF

VDDIO = 1.14V - 1.95V

UA600 ISL6277AHRZ QFN CRITICAL

VIN	35	
VDDP	30	
VDDIO	7	
VDD	29	
VSEN_NB	45	REG_GPU_VDDCI_VSEN
COMP_NB	43	REG_GPU_VDDCI_COMP
FB_NB	44	REG_GPU_VDDCI_FB
ISUMP_NB	47	REG_GPU_VDDCI_ISUMP
ISUMN_NB	46	REG_GPU_VDDCI_ISUMN
ISEN1_NB	48	REG_GPU_VDDCI_ISEN1
ISEN2_NB	1	PP5V_S0
NTC_NB	2	NC
NTC 27-33uA	12	GPUVCORE_NTC
VR_HOT 11Rdwn,1uA-leak	5	GPUVCORE_VR_HOT_L
ENABLE Vil<1V,Vih>1.6V 1leak<35UA	9	GPUVCORE_EN
PWROK thres=750mV, 1uA-leak	10	PM_ALL_GPU_PGOOD
SVC Vih>0.7*VDDIO	4	GPUVCORE_SVC
SVD Vil<0.3*VDDIO	6	GPUVCORE_SVD
SVT 50R	8	GPUVCORE_SVT_R
COMP Vol<0.4V@4mA 10n|<10uA	22	GPUVCORE_COMP
VSEN	18	GPUVCORE_SENSE_P
RTN	19	GPUVCORE_SENSE_N
FB	21	GPUVCORE_FB
FB2	20	GPUVCORE_FB2
ISUMP	16	GFXIMVP_ISUMP
ISUMN	17	GFXIMVP_ISUMN
THRM PAD	49	
IMON	11	
IMON_NB	3	REG_GPU_VDDCI_IMON
PWM2_NB	40	NC
PGOOD_NB	42	PVDDCI_PGOOD
BOOTX	36	REG_BOOT_GPU_VDDCI
UGATEX	37	REG_UGATE_GPU_VDDCI_R
PHASEX	38	REG_PHASE_GPU_VDDCI
LGATEX	39	REG_LGATE_GPU_VDDCI
PWM_Y	28	NC
BOOT2	34	GFXIMVP_BOOT2
UGATE2	33	GFXIMVP_UGATE2
PHASE2	32	GFXIMVP_Q1S2
LGATE2	31	GFXIMVP_LGATE2
BOOT1	24	GFXIMVP_BOOT1
UGATE1	25	GFXIMVP_UGATE1
PHASE1	26	GFXIMVP_Q1S1
LGATE1	27	GFXIMVP_LGATE1
PGOOD	23	GPUVCORE_PGOOD
FCCM_NB	41	REG_GPU_VDDCI_FCCM
ISEN3	13	PP5V_S0
ISEN2	14	GFXIMVP_ISEN2
ISEN1	15	GFXIMVP_ISEN1

TP_GPUVCORE_IMON — RA660 127K — CA660 1000PF

Line Width & DIDT on all DIDT nets

CA640 0.22UF — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE — GFXIMVP_BOOT2_R — RA640 0

RA650 0 — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE — GFXIMVP_BOOT1_R — CA650 0.22UF

PPBUS_HS_GPU — CA600 33UF, CA601 33UF, CA602 33UF, CA603 33UF, CA604 33UF, CA605 33UF, CA606 33UF, CRITICAL CA607 12PF, CRITICAL CA608 3.0PF

PPBUS_HS_GPU — CA609 2.2UF, CA610 2.2UF, CA611 2.2UF, CA612 2.2UF

PPBUS_HS_GPU — CA690 12PF, CA691 3.0PF, CA692 12PF, CA693 3.0PF, CA694 12PF, CA695 3.0PF, CA696 12PF, CA697 3.0PF

OMIT_TABLE

QA640 IRF3575 PQFN CRITICAL — 376S1136

VIN	18, 20, 21, 22, 23
GATEH	25
SW	6, 7
Q1S	26
GATEL	5, 32
PGND	4, 16, 28, 31
NC	1, 2, 3, 24, 27, 29, 30

GFXIMVP_PHASE2 — SWITCH_NODE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE

QA650 IRF3575 PQFN CRITICAL — 376S1136

PPBUS_HS_GPU — OMIT_TABLE

VIN	18, 20, 21, 22, 23
GATEH	25
SW	6, 7
Q1S	26
GATEL	5, 32
PGND	4, 16, 28, 31
NC	1, 2, 3, 24, 27, 29, 30

GFXIMVP_PHASE1 — SWITCH_NODE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE

CRITICAL LA640 0.2UH-20%-28A-0.0011OHM PILA63T-SM — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 — PPVCORE_S0_GFX_PH2 — VOLTAGE=1.1V — CRITICAL RA641 0.00075 — PPVCORE_S0_GPU

GFXIMVP_ISNS2_P — GFXIMVP_ISNS2_N

NO_XNET_CONNECTION — RA642 10K, RA643 1K, RA644 1.00

GFXIMVP_ISEN2 — GFXIMVP_ISUMN — GFXIMVP_ISUMP

CA641 0.22UF

RA645 10K — GFXIMVP_ISNS1_N

CRITICAL LA650 0.2UH-20%-28A-0.0011OHM PILA63T-SM — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 — PPVCORE_S0_GFX_PH1 — VOLTAGE=1.1V — CRITICAL RA651 0.00075

GFXIMVP_ISNS1_P — GFXIMVP_ISNS1_N

NO_XNET_CONNECTION — RA652 10K, RA653 1K, RA654 1.00

GFXIMVP_ISEN1 — GFXIMVP_ISUMN — GFXIMVP_ISUMP

CA651 0.22UF

RA655 10K — GFXIMVP_ISNS2_N

GPUVCORE_COMP_C: CA661 220PF, RA662 10K, CA663 10PF, CA664 2.0PF

GPUVCORE_FB_R: RA663 100 NOSTUFF, CA662 220PF, RA664 806

CA666 5600PF — GFXIMVP_ISUMP_C: CA665 1000PF NOSTUFF, RA665 10 — RA666 634 — GFXIMVP_ISUMN_R

CA667 0.1UF

GPUVCORE_SVC_R — RA680 22 — GPUVCORE_SVC

GPUVCORE_SVD_R — RA681 22 — GPUVCORE_SVD

GPUVCORE_SVT — RA682 22 — GPUVCORE_SVT_R

PP1V8_S0_GPU — RA684 47K NOSTUFF — GPUVCORE_PGOOD; RA685 47K — GPUVCORE_SVC; RA686 10K NOSTUFF, RA687 47K NOSTUFF — GPUVCORE_SVD; RA688 10K

PP3V3_S0_GPU — RA683 10K — GPUVCORE_VR_HOT_L; RA690 100K — GPUVCORE_NTC

PVCORE_GPU_FB_SNS_P — RA667 0 — GPUVCORE_SENSE_P

PVCORE_GPU_FB_SNS_N — RA668 0 — GPUVCORE_SENSE_N

CA668 2.0PF NOSTUFF, CA669 0.01UF — NO_XNET_CONNECTION=1

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

ISL6277A datasheet (December 19,2012)

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: GFX IMVP VCore Regulator [106]

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	106 OF 145
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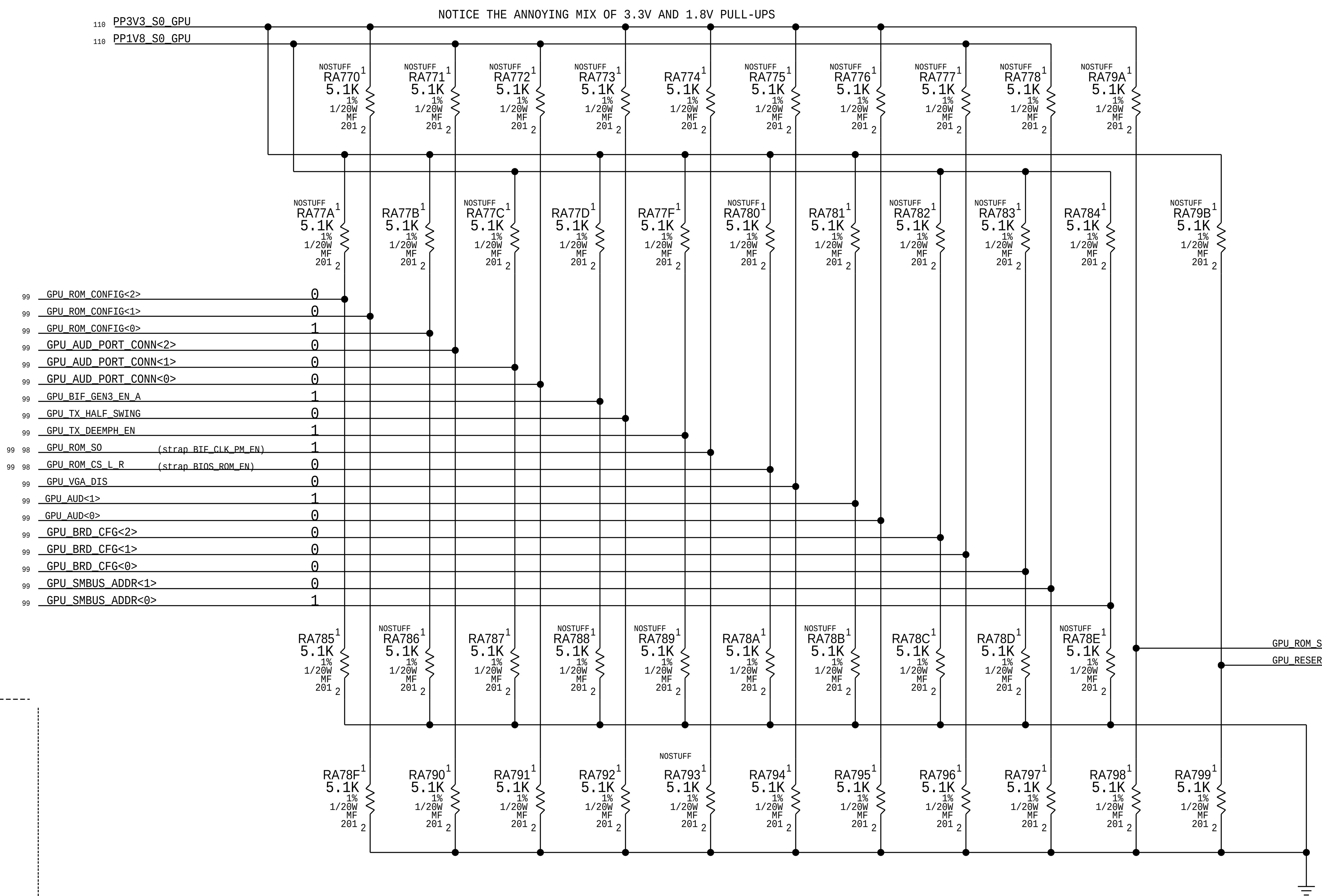
former site of the SPEED MLPS STRAPS

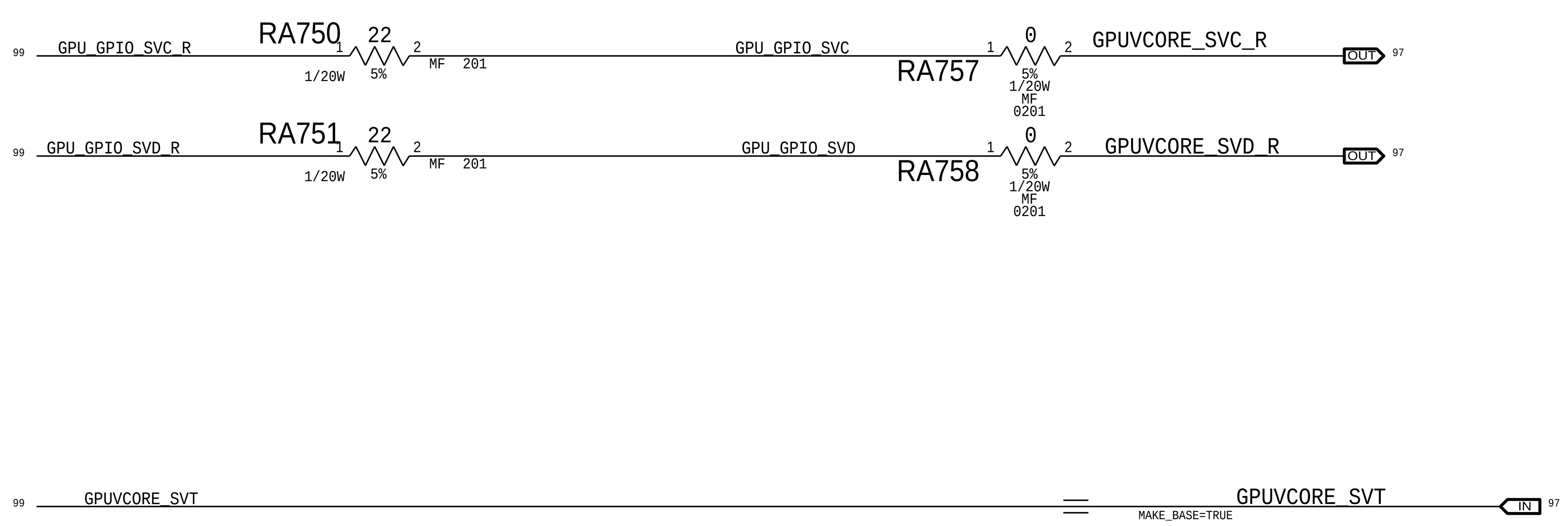
PCIe Gen3 enabled, Half-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled
All power audio-capable display output
256MB FB Aperture Size
PS_0: 01001 82nF 8.45k 2k
PS_1: 10001 10nF 8.45k 2k
PS_2: 10000 10nF NC 4.75k
PS_3: 00000 680nF NC 4.75k



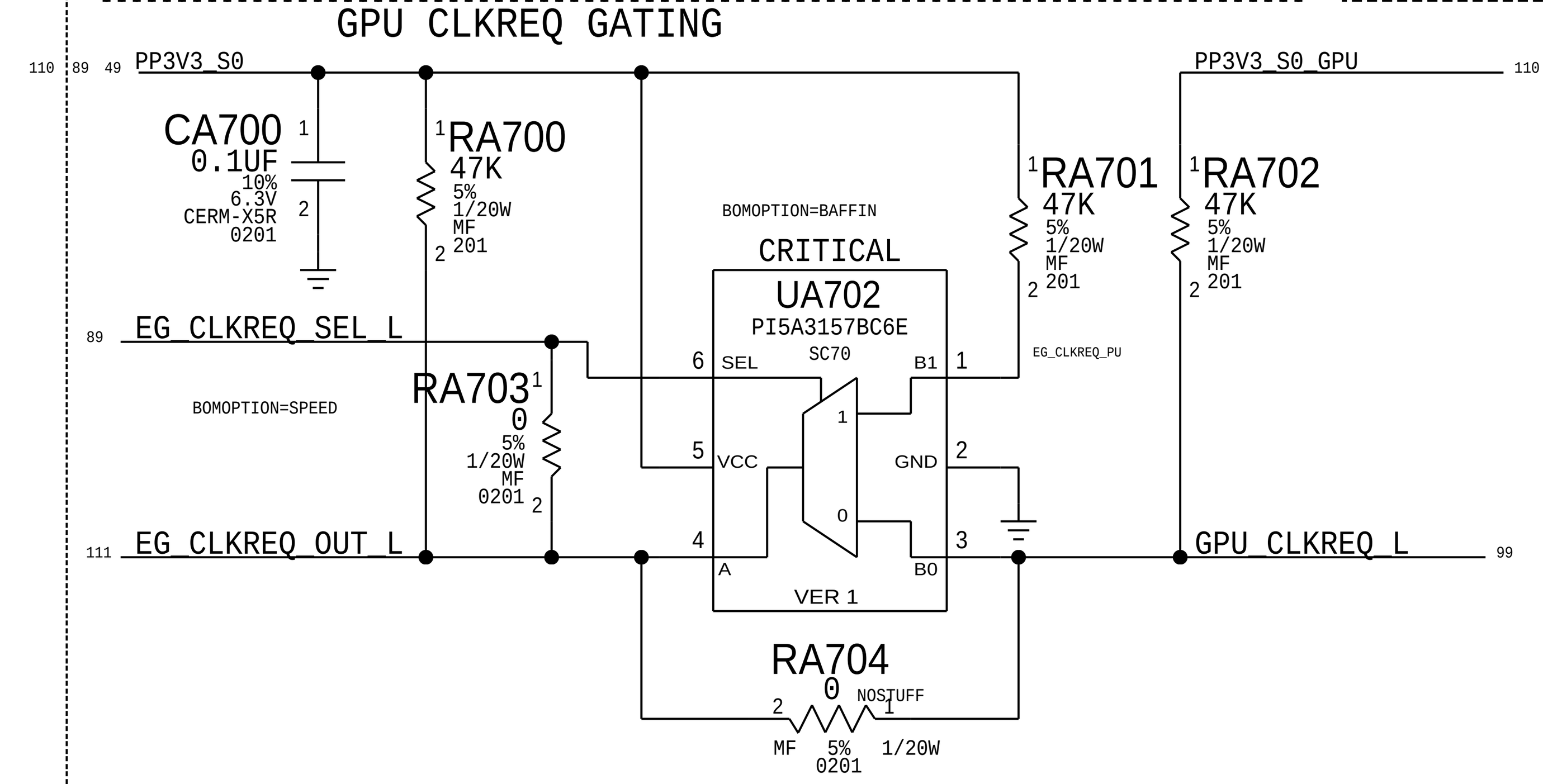
BAFFIN STRAPS

PCIe Gen3 enabled, FULL-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled, CLKREQ_L enabled
All power audio-capable display output
Audio for DP or HDMI dongle
256MB FB Aperture Size
SMBUS address 41

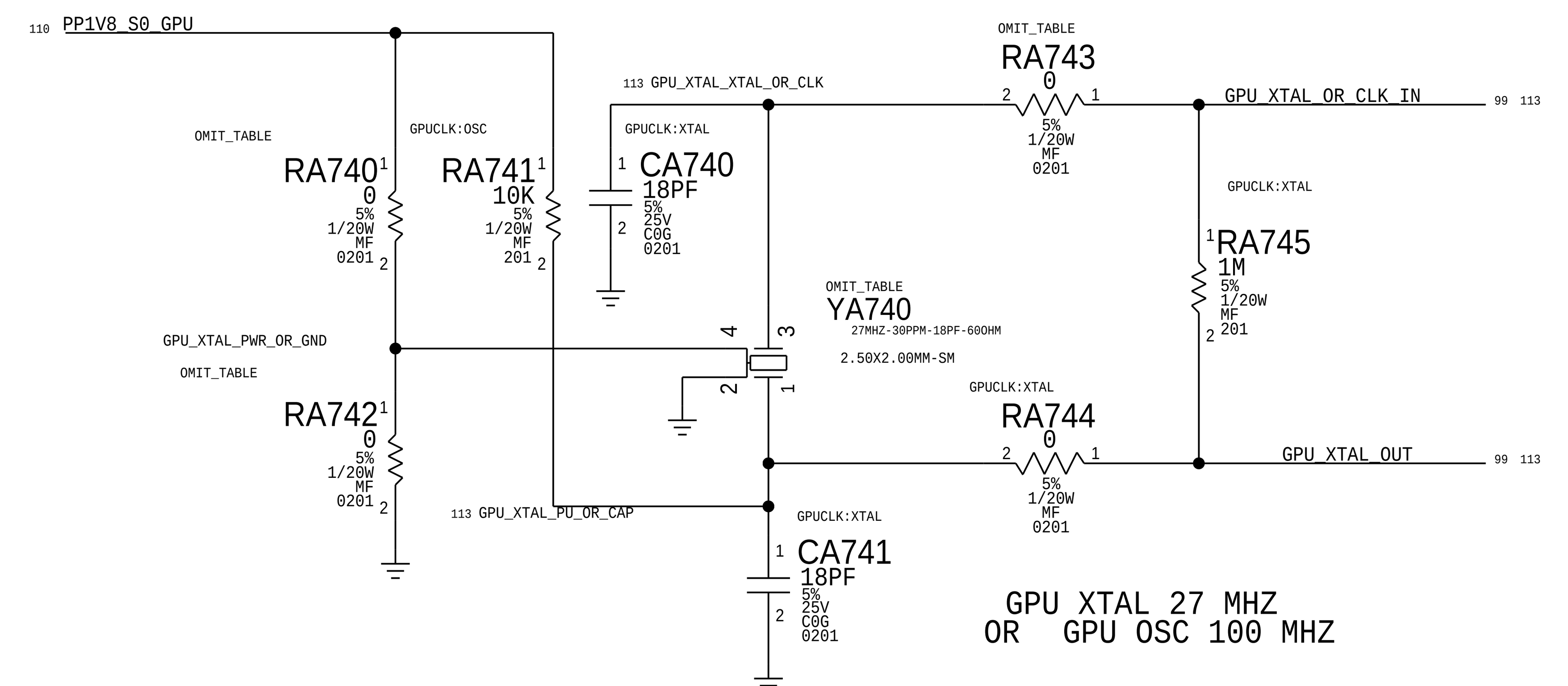
Former site of the GPU SVI2 VOLTAGE TRANSLATION SPEED ONLY



GPU CLKREQ GATING



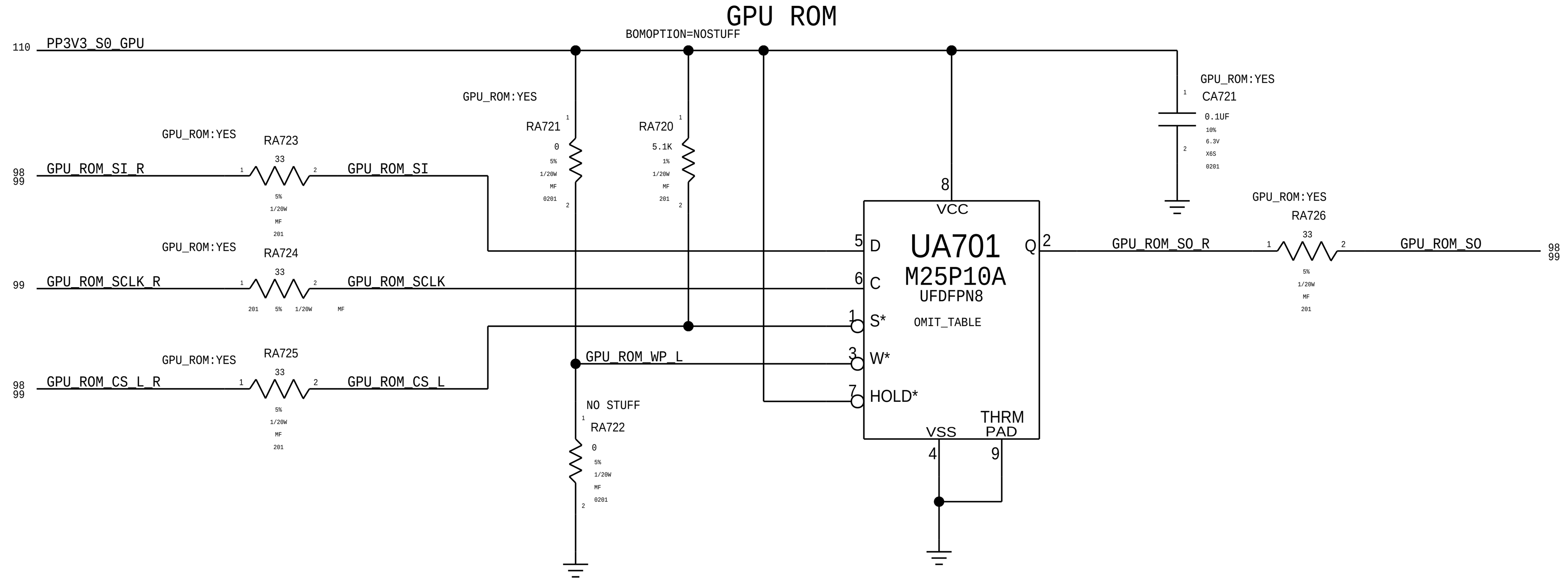
SEL = 0 : PCH CLKREQ CONNECTED TO GPU
SEL = 1 : PCH CLKREQ TIED TO PULLUP



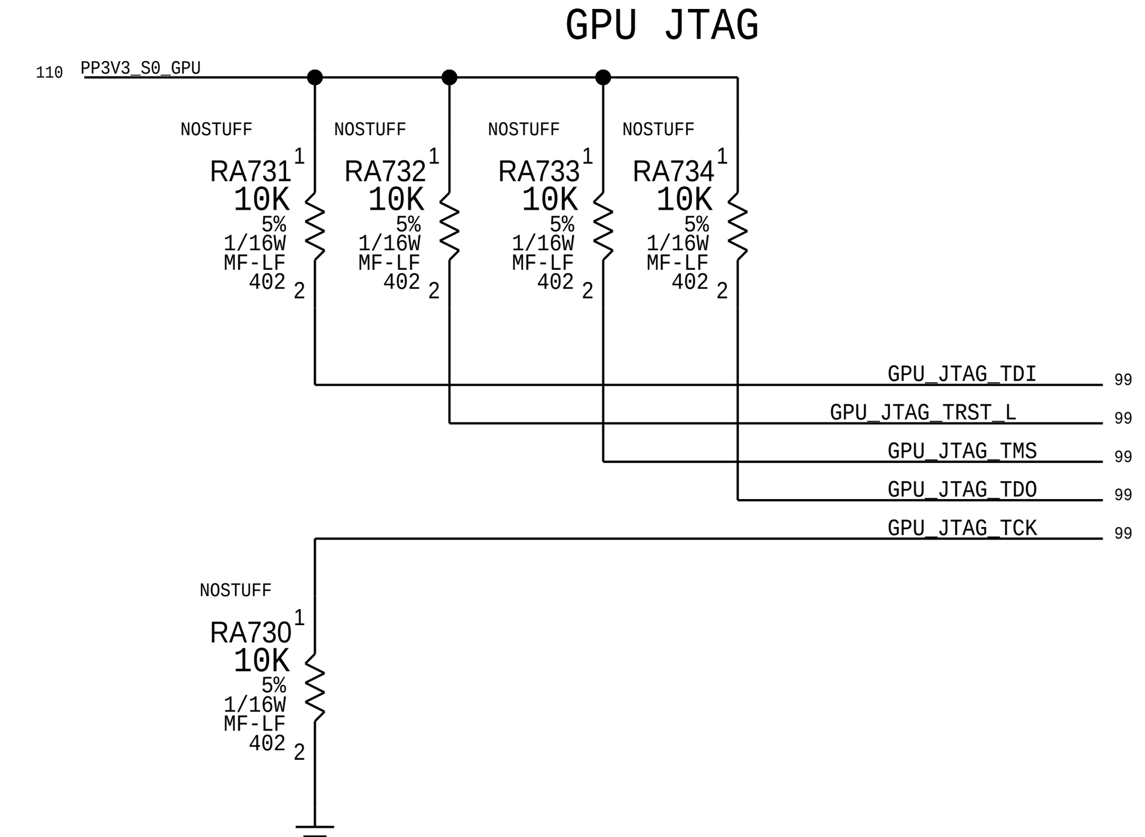
GPU XTAL 27 MHZ
OR GPU OSC 100 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0499	1	XTAL,27.000MHZ,30PPM,12PF,2.5x2.0MM	YA740	CRITICAL	GPUCLK:XTAL
197S00056	1	OSC,MEMS,100MHZ,+/-20PPM,1.8V,2520	YA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA743	CRITICAL	GPUCLK:XTAL
117S0080	1	RES,33 OHM,5%,0201	RA743	CRITICAL	GPUCLK:OSC
155S0387	1	FERRITE BEAD, 470OHM,0.1A,1.5MOHM DCR,060	RA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA742	CRITICAL	GPUCLK:XTAL
132S0444	1	CAP,CER,X5R,0.1UF,10%,6.3V,0201	RA742	CRITICAL	GPUCLK:OSC

GPU ROM



GPU JTAG

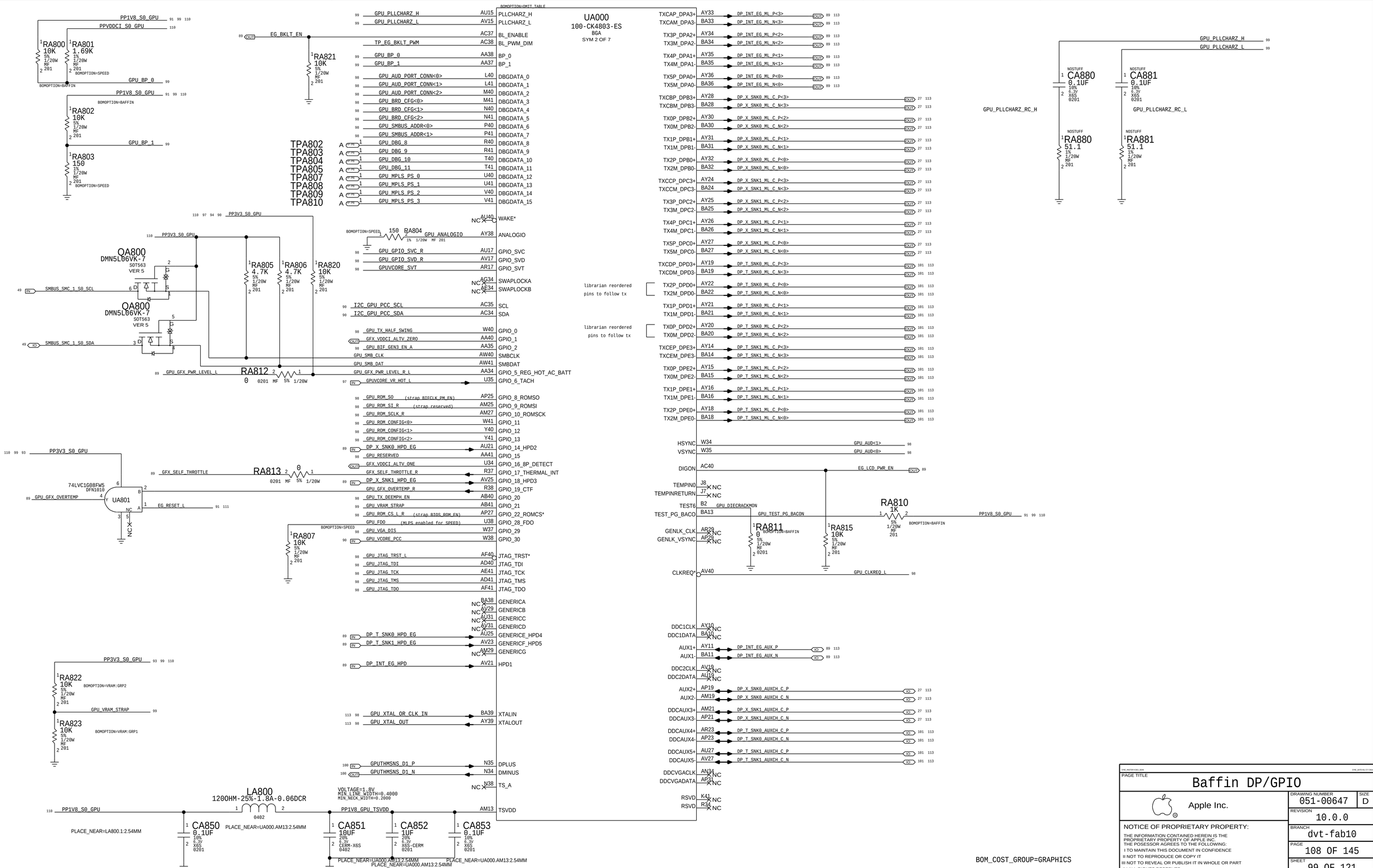


BOM_COST_GROUP=GRAPHICS

PAGE TITLE: Baffin GPIOs,CLK & Straps

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 107 OF 145
SHEET: 98 OF 121



PAGE TITLE

Baffin DP/GPIO

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	108 OF 145
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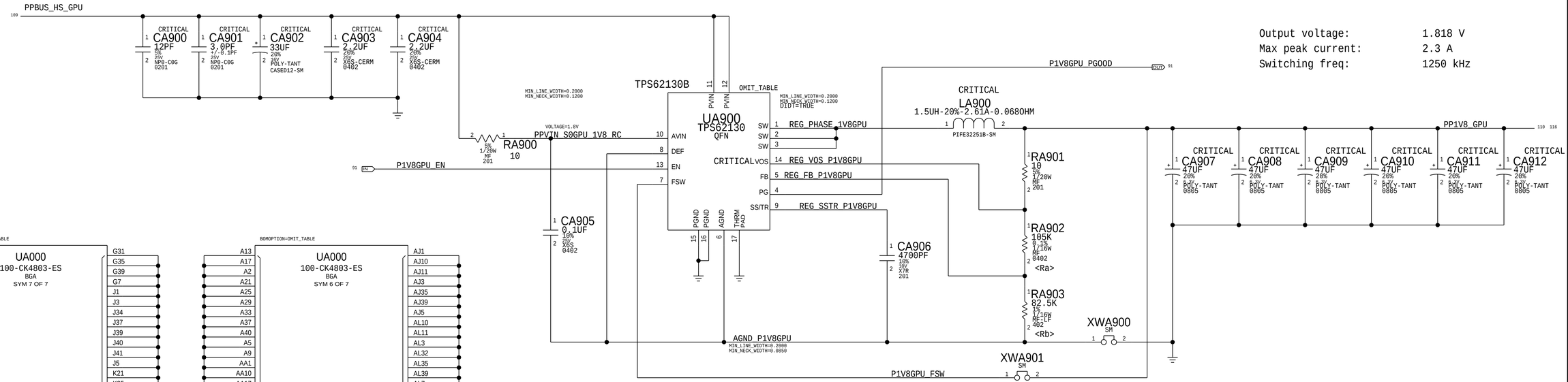
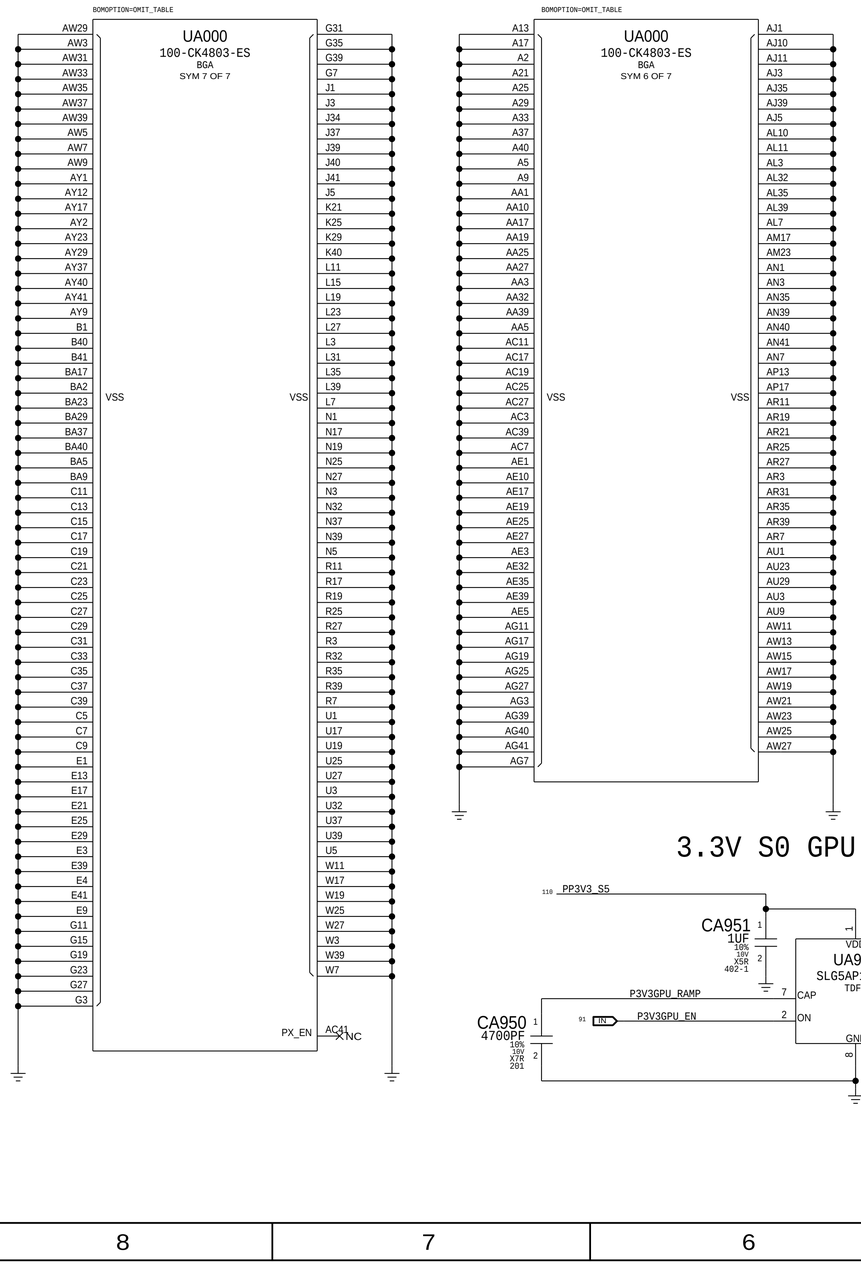


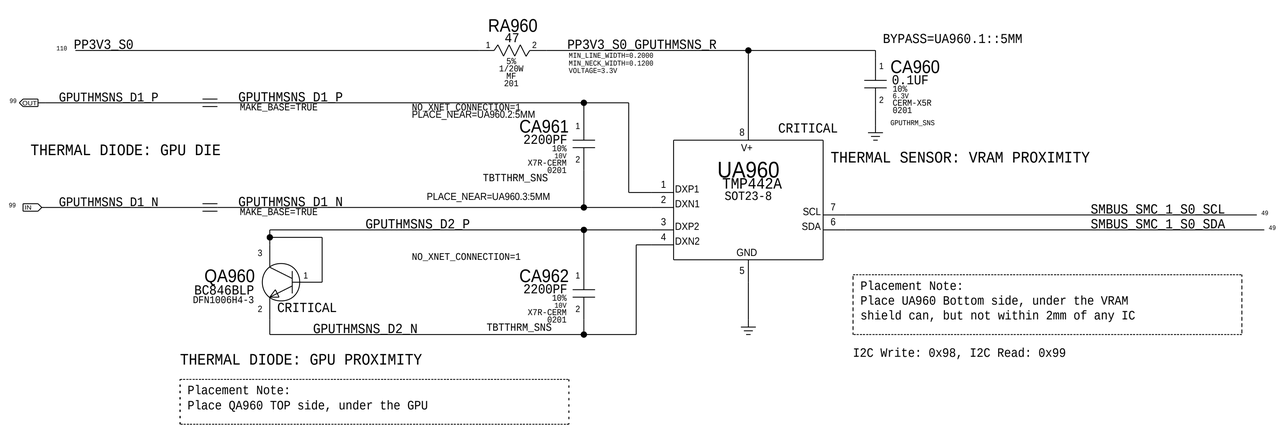
Output voltage: 1.818 V
Max peak current: 2.3 A
Switching freq: 1250 kHz

Vout = 0.8V * (Ra + Rb) / Rb

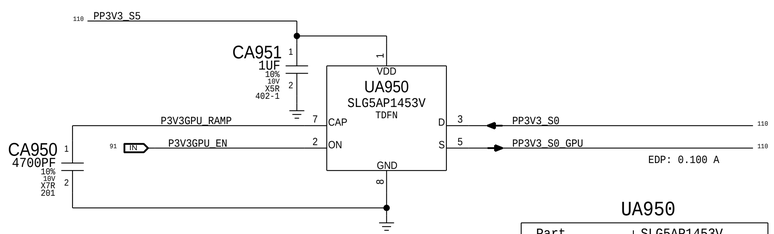
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00897	1	IC,TPS62130B-S,3A BUCK CNVTRT,QFN16,3X3M	UA900	CRITICAL	



GPU THERMAL



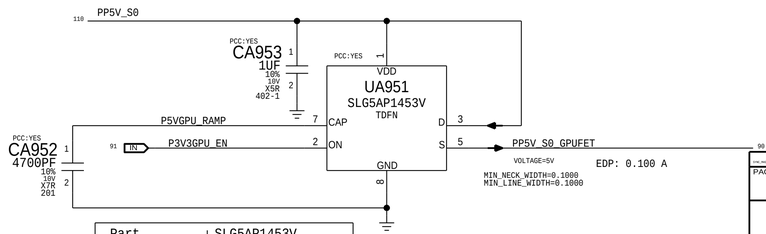
3.3V S0 GPU Switch



UA950

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

5V S0 GPU Switch



UA951

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: Baffin VSS & MISC

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 109 OF 145
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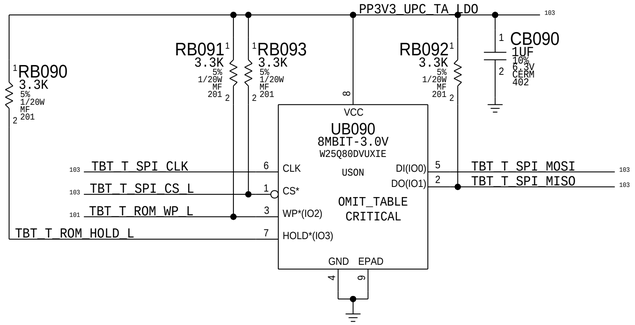


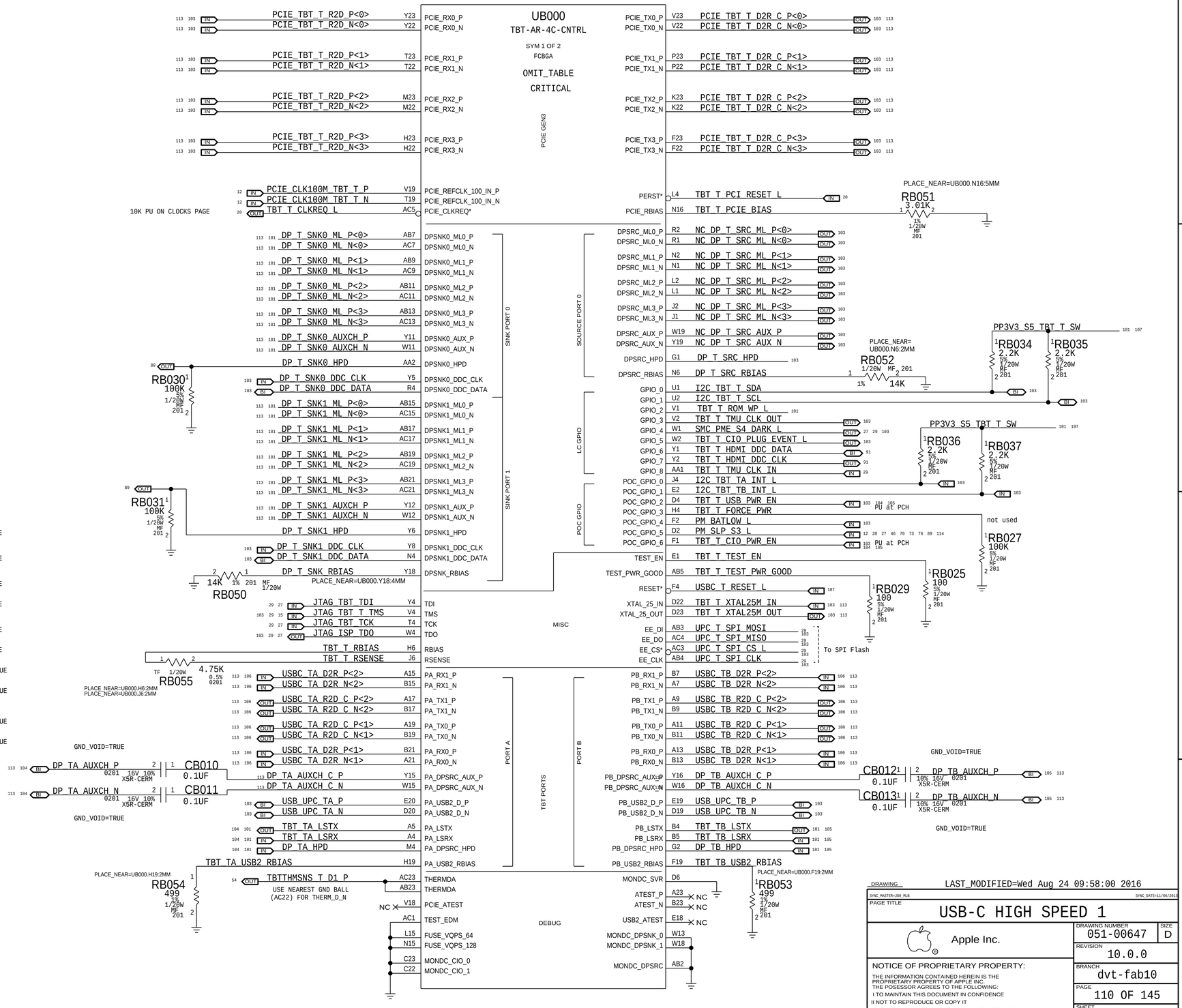
SNK0 AC Coupling

DP_T_SNK0_ML_C_P<0>	CB020 0.1UF	DP_T_SNK0_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<0>	CB021 0.1UF	DP_T_SNK0_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<1>	CB022 0.1UF	DP_T_SNK0_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<1>	CB023 0.1UF	DP_T_SNK0_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<2>	CB024 0.1UF	DP_T_SNK0_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<2>	CB025 0.1UF	DP_T_SNK0_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<3>	CB026 0.1UF	DP_T_SNK0_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<3>	CB027 0.1UF	DP_T_SNK0_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_P	CB028 0.1UF	DP_T_SNK0_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_N	CB029 0.1UF	DP_T_SNK0_AUXCH_N	GND_VOID=TRUE	

SNK1 AC Coupling

DP_T_SNK1_ML_C_P<0>	CB030 0.1UF	DP_T_SNK1_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<0>	CB031 0.1UF	DP_T_SNK1_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<1>	CB032 0.1UF	DP_T_SNK1_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<1>	CB033 0.1UF	DP_T_SNK1_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<2>	CB034 0.1UF	DP_T_SNK1_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<2>	CB035 0.1UF	DP_T_SNK1_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<3>	CB036 0.1UF	DP_T_SNK1_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<3>	CB037 0.1UF	DP_T_SNK1_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_P	CB038 0.1UF	DP_T_SNK1_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_N	CB039 0.1UF	DP_T_SNK1_AUXCH_N	GND_VOID=TRUE	

RB062 100K 5% 1/20W MF 201	DP_TA_HPD	
RB072 100K 5% 1/20W MF 201	DP_TB_HPD	
RB060 1M 5% 1/20W MF 201	TBT_TA_LSTX	
RB061 1M 5% 1/20W MF 201	TBT_TA_LSRX	
RB070 1M 5% 1/20W MF 201	TBT_TB_LSTX	
RB071 1M 5% 1/20W MF 201	TBT_TB_LSRX	



DRAWING	LAST_MODIFIED=Wed Aug 24 09:58:00 2016
SYNC_MASTER=J89_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	USB-C HIGH SPEED 1
Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
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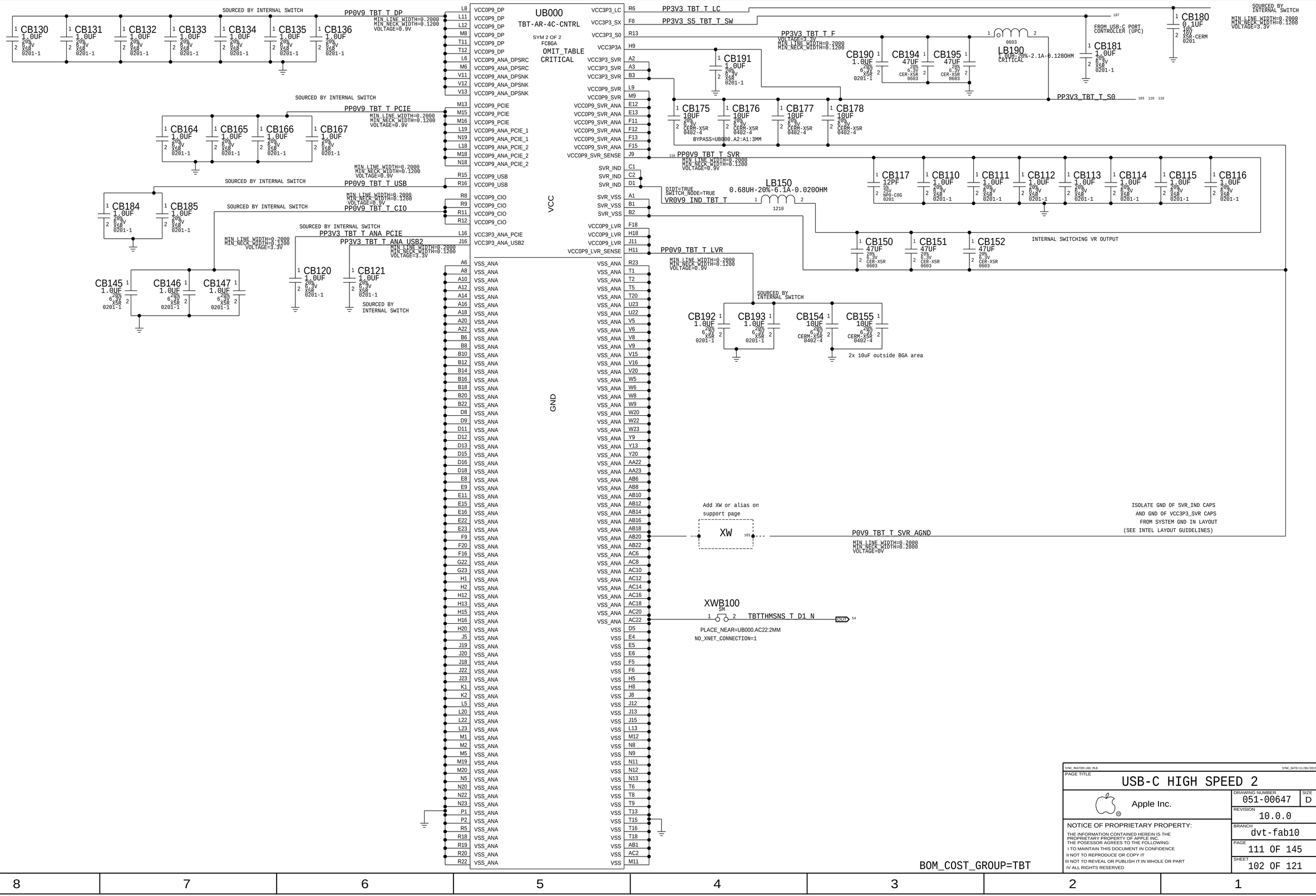

SYNC_MASTER=J89_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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TMU CLKs

TBT_T_TMU_CLK_OUT — MAKE_BASE=TRUE — TBT_T_TMU_CLK_OUT
RB225 15 5% 1/20W MF 201 — PLACE_NEAR=UB000.V2:5mm
TBT_X_TMU_CLK_IN — MAKE_BASE=TRUE
TBT_X_TMU_CLK_IN
RB226 100K 5% 1/20W MF 201

DP SRC OPTIONS

IF DP SRC NOT USED

RB240 1M 5% 1/20W MF 201 — DP_T_SRC_HPD

NC_DP_T_SRC_ML_P<3..0>	NC_DP_T_SRC_ML_P<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_T_SRC_ML_N<3..0>	NC_DP_T_SRC_ML_N<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P	MAKE_BASE=TRUE
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N	MAKE_BASE=TRUE

FUSES FOR UPC

PP20V_USBC_TA_VBUS — FB200 (PLACE_NEAR=QB300:5MM, CRITICAL, 0603, 6AMP-32V-0.0095OHM) — PP20V_USBC_TA_VBUS_F
PP20V_USBC_TB_VBUS — FB201 (PLACE_NEAR=QB400:5MM, CRITICAL, 0603, 740S0135, 6AMP-32V-0.0095OHM) — PP20V_USBC_TB_VBUS_F

25MHz xtal

TBT_T_XTALIN25M_OUT — RB207 0 5% 1/20W MF 201 — TBT_T_XTAL25M_OUT_R
NOSTUFF RB206 1M 5% 1/20W MF 201 — to/from Ridge
CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CB202 20PF 5% 25V C0G 0201
CB203 20PF 5% 25V C0G 0201
TBT_T_XTAL25M_IN

AR/ACE SPI BUS SERIES R'S

ROM: TBT_T_SPI_CLK, TBT_T_SPI_CS_L, TBT_T_SPI_MOSI, TBT_T_SPI_MISO

RB290 100	TBT_T_SPI_CLK_DBG		
RB280 15	UPC_TA_SPI_CLK	IN	Ace
RB281 15	UPC_TA_SPI_CS_L	IN	Ace
RB282 15	UPC_TA_SPI_MOSI	IN	Ace
RB283 15	UPC_TA_SPI_MISO	OUT	Ace
RB284 15	UPC_T_SPI_CLK	IN	AR
RB285 15	UPC_T_SPI_CS_L	IN	AR
RB286 15	UPC_T_SPI_MOSI	IN	AR
RB287 15	UPC_T_SPI_MISO	OUT	AR

(5% 1/20W MF 201)

TP PADS

TP_UPC_TA_SWD_DATA — TPB201
TP_UPC_TA_SWD_CLK — TPB202
TP_UPC_TB_SWD_DATA — TPB203
TP_UPC_TB_SWD_CLK — TPB204
(TP-P5)

ACE Debug Support

OMIT RB289 NOSTUFF NONE 402 — TP_UPC_TA_DBG_UART_TX — TP_UPC_TA_DBG_UART_RX
OMIT RB288 NOSTUFF NONE 402 — TP_UPC_TB_DBG_UART_TX — TP_UPC_TB_DBG_UART_RX

USBC 5V EN PD

UPC_T_5V_EN — RB232 100K 5% 1/20W MF 201

ACE A/B RPD STRAPPING

USBC_TA_CC1	USBC_TA_CC1	MAKE_BASE=TRUE
USBC_TB_CC1	USBC_TB_CC1	MAKE_BASE=TRUE
USBC_TA_CC2	USBC_TA_CC2	MAKE_BASE=TRUE
USBC_TB_CC2	USBC_TB_CC2	MAKE_BASE=TRUE

Ridge PDs

DP_T_SNK0_DDC_CLK (MAKE_BASE=TRUE)	RB267 100K	DP_T_SNK0_DDC_CLK
DP_T_SNK0_DDC_DATA (MAKE_BASE=TRUE)	RB268 100K	DP_T_SNK0_DDC_DATA
DP_T_SNK1_DDC_CLK (MAKE_BASE=TRUE)	RB269 100K	DP_T_SNK1_DDC_CLK
DP_T_SNK1_DDC_DATA (MAKE_BASE=TRUE)	RB270 100K	DP_T_SNK1_DDC_DATA

(5% 1/20W MF 201)

ACE PDs

UPC_TA_DBG3	RB260 100K	
UPC_TA_DBG4	RB261 100K	
UPC_TB_DBG3	RB262 100K	
UPC_TB_DBG4	RB263 100K	
UPC_TA_DBG1	RB264 100K	
UPC_TA_DBG2	RB265 100K	
UPC_TA_HPD_RX	RB233 100K	
UPC_TB_HPD_RX	RB234 100K	

(5% 1/20W MF 201)

ACE FET DCIN Bypass Caps

PPDCIN_G3H
CB211 0.1UF 10% 35V CER-X5R 0201
CB212 0.1UF 10% 35V CER-X5R 0201
CB213 0.1UF 10% 35V CER-X5R 0201
CB214 0.1UF 10% 35V CER-X5R 0201

RIDGE 0.9V SVR XW

XWB200 SM — P0V9_TBT_T_SVR_AGND — NO_XNET_CONNECTION=1

I2C SERIES R'S

I2C_UPC_T_SDA2 — RB241 33 (PLACE_NEAR=U5000:5MM) — SMBUS_SMC_4_G3H_SDA
I2C_UPC_T_SCL2 — RB242 33 (PLACE_NEAR=U5000:5MM) — SMBUS_SMC_4_G3H_SCL
(5% 1/20W MF 201)

ACE DEBUG CONN

Place on bottom

USBC_DBG JB200 505070-1220 M-ST-SM

I2C_TBT_TB_INT_L	1	2	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	3	4	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	5	6	I2C_TBT_T_SCL
SMC_USBC_INT_L	7	8	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	9	10	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	11	12	UPC_TA_UART_RX
	15	16	

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)
Pri ACE — U3100 (Write: 0x70 Read: 0x71)
Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

	TBT	Pri ACE	Sec ACE
I2C_TBT_T_SCL	MAKE_BASE=TRUE	104	105
I2C_TBT_T_SDA	MAKE_BASE=TRUE	104	105
I2C_TBT_TA_INT_L	MAKE_BASE=TRUE	104	
I2C_TBT_TB_INT_L	MAKE_BASE=TRUE		105

SIGNAL ALIASES

USB2_UPC_TB_P	RB252 0	USB_UPC_PCH_TB_P
USB2_UPC_TB_N	RB253 0	USB_UPC_PCH_TB_N
USB2_UPC_TA_P	RB256 0	USB_UPC_PCH_TA_P
USB2_UPC_TA_N	RB257 0	USB_UPC_PCH_TA_N
TBT_T_CIO_PWR_EN		TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN		TBT_T_USB_PWR_EN
PM_BATLOW_L		PM_BATLOW_L
SMC_PME_S4_DARK_L		SMC_PME_S4_DARK_L
UPC_T_5V_EN		UPC_T_5V_EN
JTAG_ISP_TDO		JTAG_ISP_TDO
SMC_USBC_INT_L		SMC_USBC_INT_L
SMC_USBC_INT_L		SMC_USBC_INT_L
SSD_DEBUG_I2C_CLK_CONN		SSD_DEBUG_I2C_CLK_CONN
SSD_DEBUG_I2C_DAT_CONN		SSD_DEBUG_I2C_DAT_CONN
TBT_T_CIO_PLUG_EVENT_L		TBT_T_CIO_PLUG_EVENT_L
UPC_TA_FAULT_L	RB258 0	XDP_PCH_OBSDATA_C2
UPC_TB_FAULT_L	RB259 0	XDP_PCH_OBSDATA_C3
JTAG_TBT_T_TMS		JTAG_TBT_T_TMS
PP3V3_S4		PP3V3_S4
PP3V3_S4		
TP_USBC_TB_RESET_L		TP_USBC_TB_RESET_L
TBT_POC_RESET		TBT_POC_RESET

(5% 1/20W MF 0201)

Ridge PCIE Caps

R2D

PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF	PCIE_TBT_T_R2D_P<0>
PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF	PCIE_TBT_T_R2D_N<0>
PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF	PCIE_TBT_T_R2D_P<1>
PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF	PCIE_TBT_T_R2D_N<1>
PCIE_TBT_T_R2D_C_P<2>	CB244 0.22UF	PCIE_TBT_T_R2D_P<2>
PCIE_TBT_T_R2D_C_N<2>	CB245 0.22UF	PCIE_TBT_T_R2D_N<2>
PCIE_TBT_T_R2D_C_P<3>	CB246 0.22UF	PCIE_TBT_T_R2D_P<3>
PCIE_TBT_T_R2D_C_N<3>	CB247 0.22UF	PCIE_TBT_T_R2D_N<3>

(GND_VOID=TRUE; 0201 X5R 6.3V 20%)

D2R

PCIE_TBT_T_D2R_C_P<0>	CB250 0.22UF	PCIE_TBT_T_D2R_P<0>
PCIE_TBT_T_D2R_C_N<0>	CB251 0.22UF	PCIE_TBT_T_D2R_N<0>
PCIE_TBT_T_D2R_C_P<1>	CB252 0.22UF	PCIE_TBT_T_D2R_P<1>
PCIE_TBT_T_D2R_C_N<1>	CB253 0.22UF	PCIE_TBT_T_D2R_N<1>
PCIE_TBT_T_D2R_C_P<2>	CB254 0.22UF	PCIE_TBT_T_D2R_P<2>
PCIE_TBT_T_D2R_C_N<2>	CB255 0.22UF	PCIE_TBT_T_D2R_N<2>
PCIE_TBT_T_D2R_C_P<3>	CB256 0.22UF	PCIE_TBT_T_D2R_P<3>
PCIE_TBT_T_D2R_C_N<3>	CB257 0.22UF	PCIE_TBT_T_D2R_N<3>

(GND_VOID=TRUE; 0201 X5R 6.3V 20%)

USB_UPC_TB_P / USB_UPC_TB_N / USB_UPC_TA_P / USB_UPC_TA_N

RB250 0 USB_UPC_TB_P NOSTUFF
RB251 0 USB_UPC_TB_N NOSTUFF
RB354 0 USB_UPC_TA_P NOSTUFF
RB255 0 USB_UPC_TA_N NOSTUFF
(5% 1/20W MF 0201)

POWER ALIASES

PP3V3_UPC_TA_LDO	PP3V3_UPC_TA_LDO	MAKE_BASE=TRUE
PP20V_USBC_TA_VBUS	PP20V_USBC_TA_VBUS	MAKE_BASE=TRUE
PP20V_USBC_TB_VBUS	PP20V_USBC_TB_VBUS	MAKE_BASE=TRUE
PP3V3_UPC_TB_LDO	PP3V3_UPC_TB_LDO	MAKE_BASE=TRUE
PP5V_S4_T_USBC	PP5V_S4_T_USBC	MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V
PP3V3_TBT_T_S0	PP3V3_TBT_T_S0	MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V

NO TEST

NC_UPC_TB_I2C_ADDR

GND ALIASES

GND — MAKE_BASE=TRUE — BOM_COST_GROUP=TBT

USB-C Support

Apple Inc.

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PRIMARY ACE USB-C PORT CONTROLLER (UPC)

QB300
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

PP20V_USBC_TA_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

PP20V_USBC_TA_VBUS
CB301 1UF 100 35V X5R 0402

PPDCIN_G3H
MAX 100uF TOTAL ON RAIL

UPC_TA_GATE1
TP_QB300_DRAIN
UPC_TA_GATE2

PP3V3_UPC_TA_LDO
PP3V3_G3H
GND
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB300 10UF 20% 6.3V X5R-CERM-X5R 0402-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V

PP3V3_UPC_TA_LDO
P3V3_TBT_T_SX_EN_R
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED

PP1V8_UPC_TA_LDOA
PP1V8_UPC_TA_LDOD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V

PP1V1_UPC_TA_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V

CB305 1.0UF 20% 6.3V X5R 0201-1
CB308 10UF 20% 6.3V X5R-CERM-X5R 0402-1
CB304 2.2UF 20% 6.3V X5R-CERM 0201
CB306 0.47UF 10% 6.3V CERM-X5R 0201

PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

GND
RB309 1M 5% 1/20W MF 201 — I2C_UPC_TA_DBG_CTL_SCL
RB308 1M 5% 1/20W MF 201 — I2C_UPC_TA_DBG_CTL_SDA

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

UB300
CD3215A
BGA

TBT_POC_RESET	E11	MRESET	PRIMARY ONLY
USBC_T_RESET_L_R	F11	RESET*	PRIMARY ONLY
TP_UPC_TA_DBG_UART_TX	B2	GPIO0	
TP_UPC_TA_DBG_UART_RX	C2	GPIO1	
TBT_T_CIO_PWR_EN	D10	GPIO2	
TBT_T_USB_PWR_EN	G11	GPIO3	
DP_TA_HPD	C10	GPIO4	
UPC_TA_HPD_RX	E10	GPIO5	
UPC_T_5V_EN	G10	GPIO6	
SMC_PME_S4_DARK_L	D7	GPIO7	
UPC_TA_FAULT_L	H6	GPIO8	
GND	F10	BUSPOWERZ	
UPC_TA_I2C_ADDR	F1	I2C_ADDR	
UPC_TA_R_OSC	G2	R_OSC	
I2C_UPC_TA_DBG_CTL_SCL	E4	DEBUG_CTL1	
I2C_UPC_TA_DBG_CTL_SDA	D5	DEBUG_CTL2	
I2C_TBT_T_SDA	D1	I2C_SDA1	
I2C_TBT_T_SCL	D2	I2C_SCL1	
I2C_TBT_TA_INT_L	C1	I2C_IRQ1*	
I2C_UPC_T_SDA2	A5	I2C_SDA2	
I2C_UPC_T_SCL2	B5	I2C_SCL2	
SMC_USBC_INT_L	B6	I2C_IRQ2*	
UPC_TA_SPI_CLK	A3	SPI_CLK	
UPC_TA_SPI_MOSI	B4	SPI_MOSI	
UPC_TA_SPI_MISO	A4	SPI_MISO	
UPC_TA_SPI_CS_L	B3	SPI_SSZ	
TP_UPC_TA_SWD_DATA	F4	SWD_DATA	
TP_UPC_TA_SWD_CLK	G4	SWD_CLK	
UPC_TA_UART_RX	F2	UART_RX	
UPC_TA_UART_TX	E2	UART_TX	
TBT_TA_LSTX	L4	LSX_R2P	
TBT_TA_LSRX	K4	LSX_P2R	
USB_UPC_TA_F_P	L5	USB_RP_P	
USB_UPC_TA_F_N	K5	USB_RP_N	
DP_TA_AUXCH_P	J1	AUX_P	
DP_TA_AUXCH_N	J2	AUX_N	
UPC_TA_DBG1	L2	DEBUG1	
UPC_TA_DBG2	K2	DEBUG2	
UPC_TA_DBG3	L3	DEBUG3	
UPC_TA_DBG4	K3	DEBUG4	

CRITICAL
OMIT_TABLE

PP_5V0 A11 B11 C11 D11
PP_HV A6 A7 A8 B7
PP_CABLE H10
VBUS H11 J10 J11 K11
VIN_3V3 H1
VDDIO B1
LDO_3V3 G1
VOUT_3V3 H2
LDO_1V8A K1
LDO_1V8D A2
LDO_BMC E1

HV FET/SENSE
SS H7 — UPC_TA_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9

CB309 0.47UF 10% 6.3V CERM-X5R 0201

DIGITAL CORE I/O AND CONTROL
TYPE-C
C_CC1 L9 — USBC_TA_CC1
C_CC2 L10 — USBC_TA_CC2
RPD_G1 K9 — USBC_TA_CC1
RPD_G2 K10 — USBC_TA_CC2
C_USB_TP K6 — USBC_TA_USB_TOP_P
C_USB_TN L6 — USBC_TA_USB_TOP_N
C_USB_BP K7 — USBC_TA_USB_BOT_P
C_USB_BN L7 — USBC_TA_USB_BOT_N
C_SBU1 K8 — USBC_TA_SBU1
C_SBU2 L8 — USBC_TA_SBU2

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

CB314 220PF 10% 16V C0G 0201
CB313 220PF 10% 16V C0G 0201

NC L11 — GROUND
NC or GND to dissipate heat

GND_I2C_ADDR
PRIMARY ONLY
RB302 0 5% 1/20W MF 201

CRITICAL
RB303 15K 0.1% 1/20W TF-LF 0201
NEED 0.1%

UPC_TA_UART_RX
RB305 1M 5% 1/20W MF 201

TO SMC

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

PORT MUX

LB300
90-OHM-0.1A
EXCX4CE

USB2_UPC_TA_P — PLACE_NEAR=UB300.L5:5mm
USB2_UPC_TA_N — PLACE_NEAR=UB300.K5:5mm

PP3V3_S4
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
RB310 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

RB311 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

GND pins: A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7 — GND

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

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SECONDARY ACE USB-C PORT CONTROLLER (UPC)

PULL R3209 AND R3208 UP TO ACE5 LDO5 FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

GND
1M RB409 I2C_UPC_TB_DBG_CTL_SCL 105
1M RB408 I2C_UPC_TB_DBG_CTL_SDA 105
5% 1/20W MF 201

1M RB405 UPC_TA_UART_TX 103 104 105

QB400
FDPC4044
PWR-CLIP-33
S2 G2 G1 S1

FUSE
Add on support page

103 PP20V_USBC_TB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

NC

103 PP20V_USBC_TB_VBUS
CB401 1UF 10% 25V X5R 0402

UPC_TB_GATE1
TP_QB400_DRAIN
UPC_TB_GATE2

PPDCIN_G3H 29 30 31 103 104
MAX 100uF TOTAL ON RAIL

103 PP3V3_UPC_TB_LDO
109 PP3V3_G3H
104 103 31 30 29 GND
103 PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB400 10UF 20% 6.3V CERM-X5R 0402-1

PP3V3_UPC_TB_LDO 103
P3V3_TBT_T_SX_EN_R 107
PP1V8_UPC_TB_LDOA
PP1V8_UPC_TB_LDOD
PP1V1_UPC_TB_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V

CB405 1.0UF 20% 6.3V X5R 0201-1
CB408 10UF 20% 6.3V CERM-X5R 0402-1
CB404 2.2UF 20% 4V X5R-CERM 0201
CB406 0.47UF 10% 6.3V CERM-X5R 0201

PP_5V0 A11 B11 C11 D11
PP_HV A6 A7 A8 B7
PP_HV H10
VBUS H11 J10 J11 K11
VIN_3V3 H1
VDDIO B1
LDO_3V3 G1
VOUT_3V3 H2 K1
LDO_1V8A A2
LDO_1V8D E1
LDO_BMC

CRITICAL
OMIT_TABLE

UB400
CD3215A
BGA

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

104 103 IN	TBT_POC_RESET	E11	MRESET
103 OUT	TP_USBC_TB_RESET_L	F11	RESET*
114 103	TP_UPC_TB_DBG_UART_TX	B2	GPIO0
103 114	TP_UPC_TB_DBG_UART_RX	C2	GPIO1
104 103 101 BI	TBT_T_CIO_PWR_EN	D10	GPIO2
104 103 101 BI	TBT_T_USB_PWR_EN	G11	GPIO3
101 OUT	DP_TB_HPD	C10	GPIO4
103	UPC_TB_HPD_RX	E10	GPIO5
103 OUT	UPC_T_5V_EN	G10	GPIO6
104 103 31 30 29 OUT	SMC_PME_S4_DARK_L	D7	GPIO7
103 OUT	UPC_TB_FAULT_L	H6	GPIO8
103 IN	GND	F10	BUSPOWERZ
103	NC_UPC_TB_I2C_ADDR	F1	I2C_ADDR
	UPC_TB_R_OSC	G2	R_OSC
105	I2C_UPC_TB_DBG_CTL_SCL	E4	DEBUG_CTL1
105	I2C_UPC_TB_DBG_CTL_SDA	D5	DEBUG_CTL2
103 BI	I2C_TBT_T_SDA	D1	I2C_SDA1
103 BI	I2C_TBT_T_SCL	D2	I2C_SCL1
103 OUT	I2C_TBT_TB_INT_L	C1	I2C_IRQ1*
103 BI	I2C_UPC_T_SDA2	A5	I2C_SDA2
103 BI	I2C_UPC_T_SCL2	B5	I2C_SCL2
103 OUT	SMC_USBC_INT_L	B6	I2C_IRQ2*
103 OUT	GND	A3	SPI_CLK
103 OUT	GND	B4	SPI_MOSI
103 IN	GND	A4	SPI_MISO
103 OUT	GND	B3	SPI_SSZ
103	TP_UPC_TB_SWD_DATA	F4	SWD_DATA
103	TP_UPC_TB_SWD_CLK	G4	SWD_CLK
105 104 103	UPC_TA_UART_TX	F2	UART_RX
104 103 OUT	UPC_TA_UART_RX	E2	UART_TX
101 IN	TBT_TB_LSTX	L4	LSX_R2P
101 OUT	TBT_TB_LSRX	K4	LSX_P2R
	USB_UPC_TB_F_P	L5	USB_RP_P
	USB_UPC_TB_F_N	K5	USB_RP_N
	DP_TB_AUXCH_P	J1	AUX_P
	DP_TB_AUXCH_N	J2	AUX_N
103 BI	SSD_DEBUG_I2C_CLK_CONN	L2	DEBUG1
103 BI	SSD_DEBUG_I2C_DAT_CONN	K2	DEBUG2
103 BI	UPC_TB_DBG3	L3	DEBUG3
103 BI	UPC_TB_DBG4	K3	DEBUG4

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

CRITICAL
RB403 15K 0.1% 1/20W TF-LF 0201 NEED 0.1%

TO SMC

LB400
90-OHM-0.1A
EXCX4CE
SYM_VER_1
103 BI USB2_UPC_TB_P 1 4 PLACE_NEAR=UB400.L5:5mm
103 BI USB2_UPC_TB_N 2 3 PLACE_NEAR=UB400.K5:5mm

103 PP3V3_S4
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
RB410 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1
113 101 BI
113 101 BI
RB411 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS H7 UPC_TB_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9
CB409 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 L9 USBC_TB_CC1 BI 103 106
C_CC2 L10 USBC_TB_CC2 BI 103 106
RPD_G1 K9 USBC_TB_CC1 BI 103
RPD_G2 K10 USBC_TB_CC2 BI 103
C_USB_TP K6 USBC_TB_USB_TOP_P BI 106
C_USB_TN L6 USBC_TB_USB_TOP_N BI 106
C_USB_BP K7 USBC_TB_USB_BOT_P BI 106
C_USB_BN L7 USBC_TB_USB_BOT_N BI 106
C_SBU1 K8 USBC_TB_SBU1 BI 106 115
C_SBU2 L8 USBC_TB_SBU2 BI 106 115
NC L11 GROUND
NC or GND to dissipate heat

CB414 220PF 10% 16V CER-X7R 0201
CB413 220PF 10% 16V CER-X7R 0201
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

GND A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7
GND 103
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=J30_MLB SYNC_DATE=11/08/2021
PAGE TITLE
USB-C PORT CONTROLLER B

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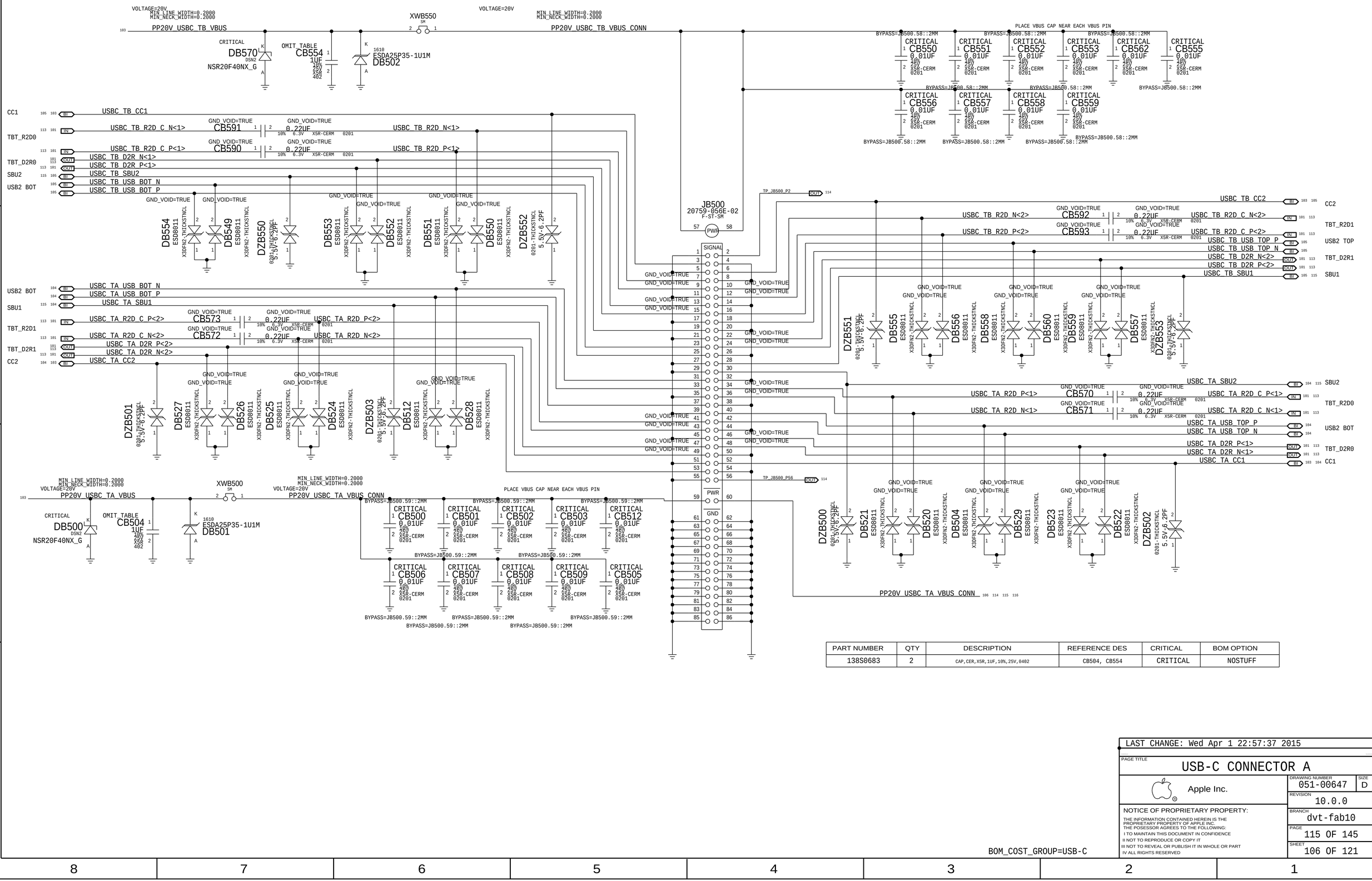

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	CB504, CB554	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A

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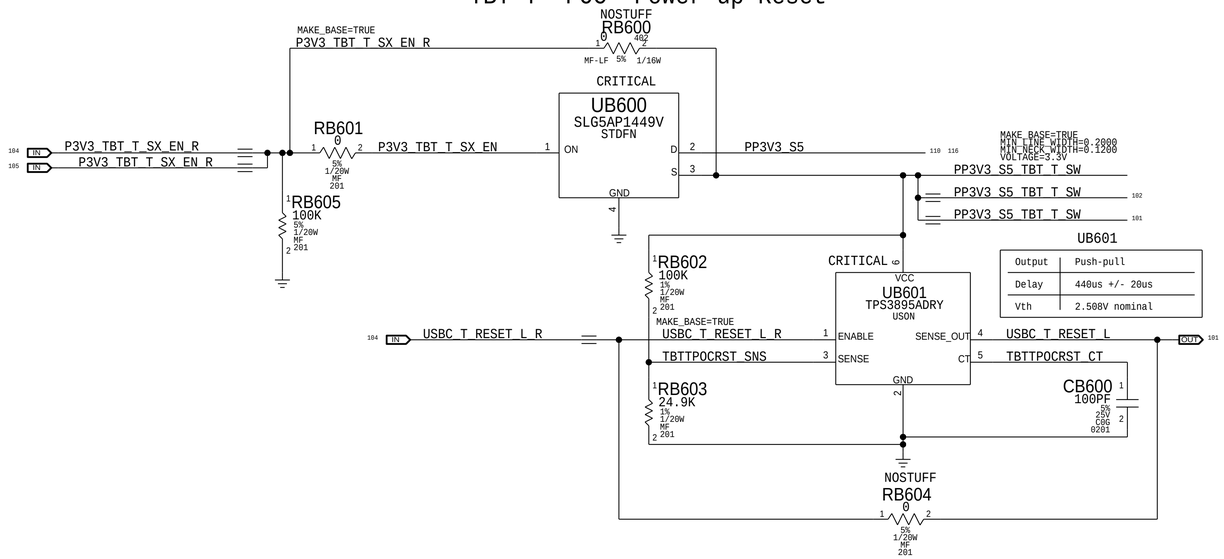
TBT T "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: j130/dev_mlb_u
LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

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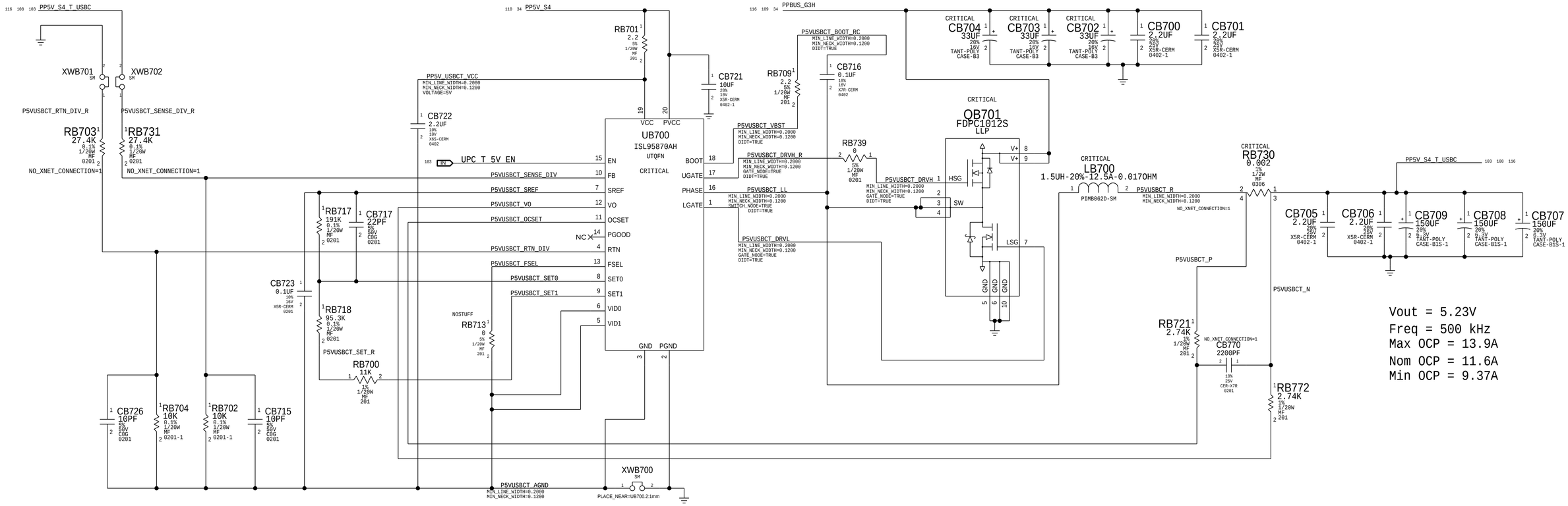

BOM_COST_GROUP=USB-C

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

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PAGE TITLE
Power Aliases - 1

Apple Inc.

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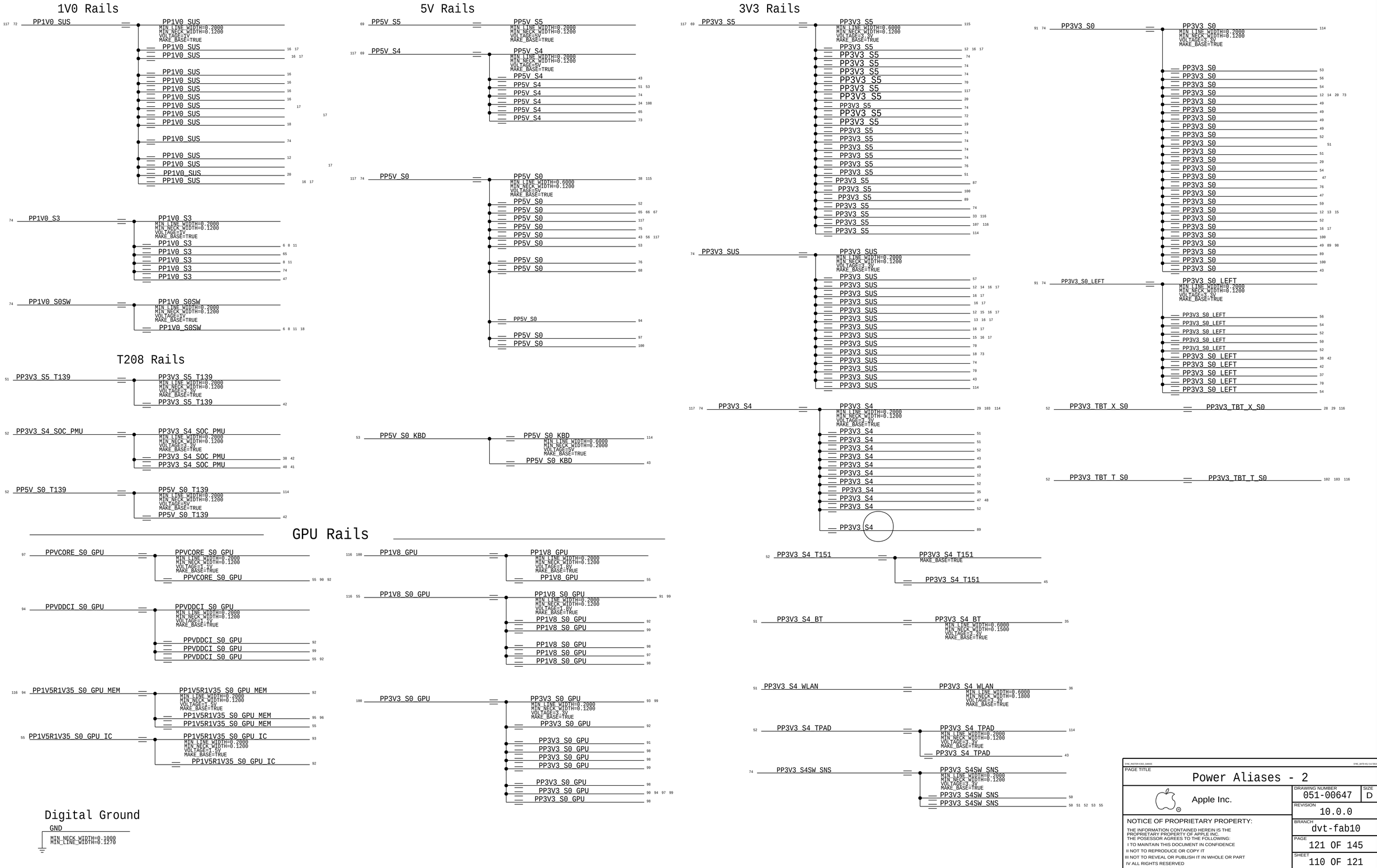
1V0 Rails
PP1V0_SUS
PP1V0_S3
PP1V0_S0SW
T208 Rails
PP3V3_S5_T139
PP3V3_S4_SOC_PMU
PP5V_S0_T139
5V Rails
PP5V_S5
PP5V_S4
PP5V_S0
PP5V_S0_KBD
GPU Rails
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
PP1V5R1V35_S0_GPU_MEM
PP1V5R1V35_S0_GPU_IC
PP1V8_GPU
PP1V8_S0_GPU
PP3V3_S0_GPU
Digital Ground
GND
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.1270
3V3 Rails
PP3V3_S5
PP3V3_SUS
PP3V3_S4
PP3V3_S4_T151
PP3V3_S4_BT
PP3V3_S4_WLAN
PP3V3_S4_TPAD
PP3V3_S4SW_SNS
PP3V3_S0
PP3V3_S0_LEFT
PP3V3_TBT_X_S0
PP3V3_TBT_T_S0
PAGE TITLE
Power Aliases - 2
Apple Inc.
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SIGNAL ALIAS

NC ALIASES 2

111 12	NC_CLKOUT_PCIE_1_N	NC_CLKOUT_PCIE_1_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_1_P	NC_CLKOUT_PCIE_1_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_2_N	NC_CLKOUT_PCIE_2_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_2_P	NC_CLKOUT_PCIE_2_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_6_N	NC_CLKOUT_PCIE_6_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_6_P	NC_CLKOUT_PCIE_6_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_8_N	NC_CLKOUT_PCIE_8_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_8_P	NC_CLKOUT_PCIE_8_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_9_N	NC_CLKOUT_PCIE_9_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_9_P	NC_CLKOUT_PCIE_9_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_10_N	NC_CLKOUT_PCIE_10_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_10_P	NC_CLKOUT_PCIE_10_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_11_N	NC_CLKOUT_PCIE_11_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_11_P	NC_CLKOUT_PCIE_11_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_12_N	NC_CLKOUT_PCIE_12_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_12_P	NC_CLKOUT_PCIE_12_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_14_N	NC_CLKOUT_PCIE_14_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_14_P	NC_CLKOUT_PCIE_14_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_15_N	NC_CLKOUT_PCIE_15_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_15_P	NC_CLKOUT_PCIE_15_P	12 111	MAKE_BASE=TRUE

15	NC_TP_PCH_GPP_G1	NC_TP_PCH_GPP_G1	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G2	NC_TP_PCH_GPP_G2	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G3	NC_TP_PCH_GPP_G3	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G4	NC_TP_PCH_GPP_G4	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G5	NC_TP_PCH_GPP_G5	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G6	NC_TP_PCH_GPP_G6	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G7	NC_TP_PCH_GPP_G7	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G8	NC_TP_PCH_GPP_G8	15	MAKE_BASE=TRUE

14	NC_PCH_GPP_F15	NC_PCH_GPP_F15	14	MAKE_BASE=TRUE
14	NC_PCH_GPP_F16	NC_PCH_GPP_F16	14	MAKE_BASE=TRUE
14	NC_PCH_GPP_F17	NC_PCH_GPP_F17	14	MAKE_BASE=TRUE
14	NC_PCH_GPP_F18	NC_PCH_GPP_F18	14	MAKE_BASE=TRUE

GPU PEG Lanes

113 91	IN PEG_GPU_D2R_P<7..0>	=PEG_D2R_P<7..0>	OUT 5	MAKE_BASE=TRUE
113 91	IN PEG_GPU_D2R_N<7..0>	=PEG_D2R_N<7..0>	OUT 5	MAKE_BASE=TRUE
113 91	OUT PEG_GPU_R2D_C_P<7..0>	=PEG_R2D_C_P<7..0>	IN 5	MAKE_BASE=TRUE
113 91	OUT PEG_GPU_R2D_C_N<7..0>	=PEG_R2D_C_N<7..0>	IN 5	MAKE_BASE=TRUE

Thunderbolt Signals Through PEG

113 29	IN PCIE_TBT_X_D2R_P<3..0>	=PEG_D2R_P<11..8>	OUT 5	MAKE_BASE=TRUE
113 29	IN PCIE_TBT_X_D2R_N<3..0>	=PEG_D2R_N<11..8>	OUT 5	MAKE_BASE=TRUE
113 29	OUT PCIE_TBT_X_R2D_C_P<3..0>	=PEG_R2D_C_P<11..8>	IN 5	MAKE_BASE=TRUE
113 29	OUT PCIE_TBT_X_R2D_C_N<3..0>	=PEG_R2D_C_N<11..8>	IN 5	MAKE_BASE=TRUE
113 103	IN PCIE_TBT_T_D2R_P<3..0>	=PEG_D2R_P<15..12>	OUT 5	MAKE_BASE=TRUE
113 103	IN PCIE_TBT_T_D2R_N<3..0>	=PEG_D2R_N<15..12>	OUT 5	MAKE_BASE=TRUE
113 103	OUT PCIE_TBT_T_R2D_C_P<3..0>	=PEG_R2D_C_P<15..12>	IN 5	MAKE_BASE=TRUE
113 103	OUT PCIE_TBT_T_R2D_C_N<3..0>	=PEG_R2D_C_N<15..12>	IN 5	MAKE_BASE=TRUE

GPU ALIAS

12	EG_CLKREQ_OUT_L	EG_CLKREQ_OUT_L	98	MAKE_BASE=TRUE
12	EG_PEG_CLK100M_N	EG_PEG_CLK100M_N	91	MAKE_BASE=TRUE
12	EG_PEG_CLK100M_P	EG_PEG_CLK100M_P	91	MAKE_BASE=TRUE
89	EG_RESET_L	EG_RESET_L	91 99	MAKE_BASE=TRUE

CPU Display Aliases

eDP conn		DPMUX	
114 76	EDP_INT_ML_P<3..0>	EDP_INT_ML_P<3..0>	89 MAKE_BASE=TRUE
114 76	EDP_INT_ML_N<3..0>	EDP_INT_ML_N<3..0>	89 MAKE_BASE=TRUE
113 76	EDP_AUXCH_C_P	EDP_AUXCH_C_P	89 MAKE_BASE=TRUE
113 76	EDP_AUXCH_C_N	EDP_AUXCH_C_N	89 MAKE_BASE=TRUE

NC_DDI1_ML_C_P<3..0>	NC_DDI1_ML_C_P<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
NC_DDI1_ML_C_N<3..0>	NC_DDI1_ML_C_N<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
NC_DDI1_AUXCH_C_P	NC_DDI1_AUXCH_C_P	5	MAKE_BASE=TRUE
NC_DDI1_AUXCH_C_N	NC_DDI1_AUXCH_C_N	5	MAKE_BASE=TRUE
NC_DDI2_ML_C_P<3..0>	NC_DDI2_ML_C_P<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
NC_DDI2_ML_C_N<3..0>	NC_DDI2_ML_C_N<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
NC_DDI2_AUXCH_C_P	NC_DDI2_AUXCH_C_P	5	MAKE_BASE=TRUE
NC_DDI2_AUXCH_C_N	NC_DDI2_AUXCH_C_N	5	MAKE_BASE=TRUE
NC_DDI3_ML_P<3..0>	NC_DDI3_ML_P<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
NC_DDI3_ML_N<3..0>	NC_DDI3_ML_N<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
NC_DDI3_AUXCH_P	NC_DDI3_AUXCH_P	5	MAKE_BASE=TRUE
NC_DDI3_AUXCH_N	NC_DDI3_AUXCH_N	5	MAKE_BASE=TRUE

89 DPMUX_UC_RX	DPMUX_UC_RX	89	
89 DPMUX_UC_TX	DPMUX_UC_TX	89	MAKE_BASE=TRUE MAKE_BASE=TRUE
15 NC_EDP_IG_BKLT_PWM	NC_EDP_IG_BKLT_PWM		MAKE_BASE=TRUE

EPD PANEL

75	I2C_BKLT_SCL	I2C_BKLT_SCL	76 114	MAKE_BASE TRUE
75	I2C_BKLT_SDA	I2C_BKLT_SDA	76 114	TRUE

UNUSED SIGNALS

12	NC_PCH_SLP_WLAN_L	NC_PCH_SLP_WLAN_L		MAKE_BASE=TRUE
13	NC_SPI_CS1_L	NC_SPI_CS1_L		MAKE_BASE=TRUE
13	NC_SPI_CS2_L	NC_SPI_CS2_L		MAKE_BASE=TRUE

SYNC_MASTER=X363_SAMXOC SYNC_DATE=01/13/2016

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

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LPDDR3 COMMAND/ADDRESS

Memory Bit/Byte Swizzle

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_A_DQ<0>	MEM_A_DQ<0>
MEM_A_DQ<1>	MEM_A_DQ<1>
MEM_A_DQ<2>	MEM_A_DQ<2>
MEM_A_DQ<3>	MEM_A_DQ<3>
MEM_A_DQ<4>	MEM_A_DQ<4>
MEM_A_DQ<5>	MEM_A_DQ<5>
MEM_A_DQ<6>	MEM_A_DQ<6>
MEM_A_DQ<7>	MEM_A_DQ<7>
MEM_A_DQ<8>	MEM_A_DQ<8>
MEM_A_DQ<9>	MEM_A_DQ<9>
MEM_A_DQ<10>	MEM_A_DQ<10>
MEM_A_DQ<11>	MEM_A_DQ<11>
MEM_A_DQ<12>	MEM_A_DQ<12>
MEM_A_DQ<13>	MEM_A_DQ<13>
MEM_A_DQ<14>	MEM_A_DQ<14>
MEM_A_DQ<15>	MEM_A_DQ<15>
MEM_A_DQ<16>	MEM_A_DQ<16>
MEM_A_DQ<17>	MEM_A_DQ<17>
MEM_A_DQ<18>	MEM_A_DQ<18>
MEM_A_DQ<19>	MEM_A_DQ<19>
MEM_A_DQ<20>	MEM_A_DQ<20>
MEM_A_DQ<21>	MEM_A_DQ<21>
MEM_A_DQ<22>	MEM_A_DQ<22>
MEM_A_DQ<23>	MEM_A_DQ<23>
MEM_A_DQ<24>	MEM_A_DQ<24>
MEM_A_DQ<25>	MEM_A_DQ<25>
MEM_A_DQ<26>	MEM_A_DQ<26>
MEM_A_DQ<27>	MEM_A_DQ<27>
MEM_A_DQ<28>	MEM_A_DQ<28>
MEM_A_DQ<29>	MEM_A_DQ<29>
MEM_A_DQ<30>	MEM_A_DQ<30>
MEM_A_DQ<31>	MEM_A_DQ<31>
MEM_A_DQ<32>	MEM_A_DQ<32>
MEM_A_DQ<33>	MEM_A_DQ<33>
MEM_A_DQ<34>	MEM_A_DQ<34>
MEM_A_DQ<35>	MEM_A_DQ<35>
MEM_A_DQ<36>	MEM_A_DQ<36>
MEM_A_DQ<37>	MEM_A_DQ<37>
MEM_A_DQ<38>	MEM_A_DQ<38>
MEM_A_DQ<39>	MEM_A_DQ<39>
MEM_A_DQ<40>	MEM_A_DQ<40>
MEM_A_DQ<41>	MEM_A_DQ<41>
MEM_A_DQ<42>	MEM_A_DQ<42>
MEM_A_DQ<43>	MEM_A_DQ<43>
MEM_A_DQ<44>	MEM_A_DQ<44>
MEM_A_DQ<45>	MEM_A_DQ<45>
MEM_A_DQ<46>	MEM_A_DQ<46>
MEM_A_DQ<47>	MEM_A_DQ<47>
MEM_A_DQ<48>	MEM_A_DQ<48>
MEM_A_DQ<49>	MEM_A_DQ<49>
MEM_A_DQ<50>	MEM_A_DQ<50>
MEM_A_DQ<51>	MEM_A_DQ<51>
MEM_A_DQ<52>	MEM_A_DQ<52>
MEM_A_DQ<53>	MEM_A_DQ<53>
MEM_A_DQ<54>	MEM_A_DQ<54>
MEM_A_DQ<55>	MEM_A_DQ<55>
MEM_A_DQ<56>	MEM_A_DQ<56>
MEM_A_DQ<57>	MEM_A_DQ<57>
MEM_A_DQ<58>	MEM_A_DQ<58>
MEM_A_DQ<59>	MEM_A_DQ<59>
MEM_A_DQ<60>	MEM_A_DQ<60>
MEM_A_DQ<61>	MEM_A_DQ<61>
MEM_A_DQ<62>	MEM_A_DQ<62>
MEM_A_DQ<63>	MEM_A_DQ<63>

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_B_DQ<0>	MEM_B_DQ<0>
MEM_B_DQ<1>	MEM_B_DQ<1>
MEM_B_DQ<2>	MEM_B_DQ<2>
MEM_B_DQ<3>	MEM_B_DQ<3>
MEM_B_DQ<4>	MEM_B_DQ<4>
MEM_B_DQ<5>	MEM_B_DQ<5>
MEM_B_DQ<6>	MEM_B_DQ<6>
MEM_B_DQ<7>	MEM_B_DQ<7>
MEM_B_DQ<8>	MEM_B_DQ<8>
MEM_B_DQ<9>	MEM_B_DQ<9>
MEM_B_DQ<10>	MEM_B_DQ<10>
MEM_B_DQ<11>	MEM_B_DQ<11>
MEM_B_DQ<12>	MEM_B_DQ<12>
MEM_B_DQ<13>	MEM_B_DQ<13>
MEM_B_DQ<14>	MEM_B_DQ<14>
MEM_B_DQ<15>	MEM_B_DQ<15>
MEM_B_DQ<16>	MEM_B_DQ<16>
MEM_B_DQ<17>	MEM_B_DQ<17>
MEM_B_DQ<18>	MEM_B_DQ<18>
MEM_B_DQ<19>	MEM_B_DQ<19>
MEM_B_DQ<20>	MEM_B_DQ<20>
MEM_B_DQ<21>	MEM_B_DQ<21>
MEM_B_DQ<22>	MEM_B_DQ<22>
MEM_B_DQ<23>	MEM_B_DQ<23>
MEM_B_DQ<24>	MEM_B_DQ<24>
MEM_B_DQ<25>	MEM_B_DQ<25>
MEM_B_DQ<26>	MEM_B_DQ<26>
MEM_B_DQ<27>	MEM_B_DQ<27>
MEM_B_DQ<28>	MEM_B_DQ<28>
MEM_B_DQ<29>	MEM_B_DQ<29>
MEM_B_DQ<30>	MEM_B_DQ<30>
MEM_B_DQ<31>	MEM_B_DQ<31>
MEM_B_DQ<32>	MEM_B_DQ<32>
MEM_B_DQ<33>	MEM_B_DQ<33>
MEM_B_DQ<34>	MEM_B_DQ<34>
MEM_B_DQ<35>	MEM_B_DQ<35>
MEM_B_DQ<36>	MEM_B_DQ<36>
MEM_B_DQ<37>	MEM_B_DQ<37>
MEM_B_DQ<38>	MEM_B_DQ<38>
MEM_B_DQ<39>	MEM_B_DQ<39>
MEM_B_DQ<40>	MEM_B_DQ<40>
MEM_B_DQ<41>	MEM_B_DQ<41>
MEM_B_DQ<42>	MEM_B_DQ<42>
MEM_B_DQ<43>	MEM_B_DQ<43>
MEM_B_DQ<44>	MEM_B_DQ<44>
MEM_B_DQ<45>	MEM_B_DQ<45>
MEM_B_DQ<46>	MEM_B_DQ<46>
MEM_B_DQ<47>	MEM_B_DQ<47>
MEM_B_DQ<48>	MEM_B_DQ<48>
MEM_B_DQ<49>	MEM_B_DQ<49>
MEM_B_DQ<50>	MEM_B_DQ<50>
MEM_B_DQ<51>	MEM_B_DQ<51>
MEM_B_DQ<52>	MEM_B_DQ<52>
MEM_B_DQ<53>	MEM_B_DQ<53>
MEM_B_DQ<54>	MEM_B_DQ<54>
MEM_B_DQ<55>	MEM_B_DQ<55>
MEM_B_DQ<56>	MEM_B_DQ<56>
MEM_B_DQ<57>	MEM_B_DQ<57>
MEM_B_DQ<58>	MEM_B_DQ<58>
MEM_B_DQ<59>	MEM_B_DQ<59>
MEM_B_DQ<60>	MEM_B_DQ<60>
MEM_B_DQ<61>	MEM_B_DQ<61>
MEM_B_DQ<62>	MEM_B_DQ<62>
MEM_B_DQ<63>	MEM_B_DQ<63>

MAKE_BASE		
TRUE	MEM_A_DQS_P<0>	MEM_A_DQS_P<0>
TRUE	MEM_A_DQS_N<0>	MEM_A_DQS_N<0>
TRUE	MEM_A_DQS_P<1>	MEM_A_DQS_P<1>
TRUE	MEM_A_DQS_N<1>	MEM_A_DQS_N<1>
TRUE	MEM_A_DQS_P<2>	MEM_A_DQS_P<2>
TRUE	MEM_A_DQS_N<2>	MEM_A_DQS_N<2>
TRUE	MEM_A_DQS_P<3>	MEM_A_DQS_P<3>
TRUE	MEM_A_DQS_N<3>	MEM_A_DQS_N<3>
TRUE	MEM_A_DQS_P<4>	MEM_A_DQS_P<4>
TRUE	MEM_A_DQS_N<4>	MEM_A_DQS_N<4>
TRUE	MEM_A_DQS_P<5>	MEM_A_DQS_P<5>
TRUE	MEM_A_DQS_N<5>	MEM_A_DQS_N<5>
TRUE	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>
TRUE	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>
TRUE	MEM_A_DQS_P<7>	MEM_A_DQS_P<7>
TRUE	MEM_A_DQS_N<7>	MEM_A_DQS_N<7>

MAKE_BASE		
TRUE	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>
TRUE	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>
TRUE	MEM_B_DQS_P<1>	MEM_B_DQS_P<1>
TRUE	MEM_B_DQS_N<1>	MEM_B_DQS_N<1>
TRUE	MEM_B_DQS_P<2>	MEM_B_DQS_P<2>
TRUE	MEM_B_DQS_N<2>	MEM_B_DQS_N<2>
TRUE	MEM_B_DQS_P<3>	MEM_B_DQS_P<3>
TRUE	MEM_B_DQS_N<3>	MEM_B_DQS_N<3>
TRUE	MEM_B_DQS_P<4>	MEM_B_DQS_P<4>
TRUE	MEM_B_DQS_N<4>	MEM_B_DQS_N<4>
TRUE	MEM_B_DQS_P<5>	MEM_B_DQS_P<5>
TRUE	MEM_B_DQS_N<5>	MEM_B_DQS_N<5>
TRUE	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>
TRUE	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>
TRUE	MEM_B_DQS_P<7>	MEM_B_DQS_P<7>
TRUE	MEM_B_DQS_N<7>	MEM_B_DQS_N<7>

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: Memory Bit/Byte Swizzle

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

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High Speed NO_TEST

DMI

- IN DMI_S2N_P<3..0> NO_TEST=1
- IN DMI_S2N_N<3..0> NO_TEST=1
- IN DMI_N2S_P<3..0> NO_TEST=1
- IN DMI_N2S_N<3..0> NO_TEST=1

DP - CPU/ACE

- IN DP_X_SNK0_ML_C_N<3..0> NO_TEST=1
- IN DP_X_SNK0_ML_C_P<3..0> NO_TEST=1
- IN DP_X_SNK0_ML_N<3..0> NO_TEST=1
- IN DP_X_SNK0_ML_P<3..0> NO_TEST=1
- IN DP_X_SNK1_ML_C_N<3..0> NO_TEST=1
- IN DP_X_SNK1_ML_C_P<3..0> NO_TEST=1
- IN DP_X_SNK1_ML_N<3..0> NO_TEST=1
- IN DP_X_SNK1_ML_P<3..0> NO_TEST=1
- IN DP_T_SNK0_ML_C_N<3..0> NO_TEST=1
- IN DP_T_SNK0_ML_C_P<3..0> NO_TEST=1
- IN DP_T_SNK0_ML_N<3..0> NO_TEST=1
- IN DP_T_SNK0_ML_P<3..0> NO_TEST=1
- IN DP_T_SNK1_ML_C_N<3..0> NO_TEST=1
- IN DP_T_SNK1_ML_C_P<3..0> NO_TEST=1
- IN DP_T_SNK1_ML_N<3..0> NO_TEST=1
- IN DP_T_SNK1_ML_P<3..0> NO_TEST=1
- IN DP_X_SNK0_AUXCH_C_P NO_TEST=1
- IN DP_X_SNK0_AUXCH_C_N NO_TEST=1
- IN DP_T_SNK0_AUXCH_C_P NO_TEST=1
- IN DP_T_SNK0_AUXCH_C_N NO_TEST=1
- IN DP_X_SNK0_AUXCH_P NO_TEST=1
- IN DP_X_SNK0_AUXCH_N NO_TEST=1
- IN DP_T_SNK0_AUXCH_P NO_TEST=1
- IN DP_T_SNK0_AUXCH_N NO_TEST=1
- IN DP_X_SNK1_AUXCH_C_P NO_TEST=1
- IN DP_X_SNK1_AUXCH_C_N NO_TEST=1
- IN DP_T_SNK1_AUXCH_C_P NO_TEST=1
- IN DP_T_SNK1_AUXCH_C_N NO_TEST=1
- IN DP_X_SNK1_AUXCH_P NO_TEST=1
- IN DP_X_SNK1_AUXCH_N NO_TEST=1
- IN DP_T_SNK1_AUXCH_P NO_TEST=1
- IN DP_T_SNK1_AUXCH_N NO_TEST=1

CPU/EDP

- IN EDP_AUXCH_C_N
- IN EDP_AUXCH_C_P

PCH/AR

- IN PCIE_AP_D2R_P NO_TEST=1
- IN PCIE_AP_D2R_N NO_TEST=1
- IN PCIE_AP_R2D_P NO_TEST=1
- IN PCIE_AP_R2D_N NO_TEST=1

- IN PCIE_AP_R2D_C_P NO_TEST=1
- IN PCIE_AP_R2D_C_N NO_TEST=1

PCH/SSD

- IN PCIE_SSD_D2R_N<3..0> NO_TEST=1
- IN PCIE_SSD_D2R_P<3..0> NO_TEST=1
- IN PCIE_SSD_R2D_N<3..0> NO_TEST=1
- IN PCIE_SSD_R2D_N<3..0> NO_TEST=1
- IN PCIE_SSD_D2R_C_N<3..0> NO_TEST=1
- IN PCIE_SSD_R2D_C_N<3..0> NO_TEST=1
- IN PCIE_SSD_D2R_N<0> NO_TEST=1
- IN PCIE_SSD_D2R_P<0> NO_TEST=1
- IN PCIE_SSD_D2R_C_P<3..0> NO_TEST=1
- IN PCIE_SSD_R2D_C_N<3..0> NO_TEST=1
- IN PCIE_SSD_D2R_LB_P<0>
- IN PCIE_SSD_R2D_LB_N<0>
- IN PCIE_SSD_D2R_P<3> NO_TEST=1
- IN PCIE_SSD_D2R_LB_N<0>
- IN PCIE_SSD_D2R_N<3> NO_TEST=1
- IN PCIE_SSD_R2D_LB_P<0>

USB-C X

- IN USBC_XB_D2R_N<2..1> NO_TEST=1
- IN USBC_XB_D2R_P<2..1> NO_TEST=1
- IN USBC_XA_D2R_P<2..1> NO_TEST=1
- IN USBC_XB_R2D_C_P<2..1> NO_TEST=1
- IN DP_XA_AUXCH_P NO_TEST=1
- IN USBC_XA_D2R_N<2..1> NO_TEST=1
- IN USBC_XB_R2D_C_N<2..1> NO_TEST=1
- IN USBC_XA_R2D_C_P<2..1> NO_TEST=1
- IN DP_XB_AUXCH_P NO_TEST=1
- IN USBC_XA_R2D_C_N<2..1> NO_TEST=1
- IN DP_XB_AUXCH_N NO_TEST=1
- IN DP_XA_AUXCH_N NO_TEST=1
- IN DP_XA_AUXCH_C_N NO_TEST=1
- IN DP_XA_AUXCH_C_P NO_TEST=1
- IN DP_XB_AUXCH_C_P NO_TEST=1
- IN DP_XB_AUXCH_C_N NO_TEST=1

PEG

- IN PEG_GPU_D2R_N<7..0> NO_TEST=1
- IN PEG_GPU_D2R_P<7..0> NO_TEST=1
- IN PEG_GPU_R2D_C_N<7..0> NO_TEST=1
- IN PEG_GPU_R2D_C_P<7..0> NO_TEST=1
- IN PCIE_TBT_X_D2R_P<3..0> NO_TEST=1
- IN PCIE_TBT_X_D2R_N<3..0> NO_TEST=1
- IN PCIE_TBT_X_R2D_C_P<3..0> NO_TEST=1
- IN PCIE_TBT_X_R2D_C_N<3..0> NO_TEST=1
- IN PCIE_TBT_T_D2R_P<3..0> NO_TEST=1
- IN PCIE_TBT_T_D2R_N<3..0> NO_TEST=1
- IN PCIE_TBT_T_D2R_C_P<3..0> NO_TEST=1
- IN PCIE_TBT_T_D2R_C_N<3..0> NO_TEST=1
- IN PCIE_TBT_X_D2R_C_P<3..0> NO_TEST=1
- IN PCIE_TBT_X_D2R_C_N<3..0> NO_TEST=1
- IN PCIE_TBT_X_R2D_P<3..0> NO_TEST=1
- IN PCIE_TBT_X_R2D_N<3..0> NO_TEST=1
- IN PCIE_TBT_T_R2D_P<3..0> NO_TEST=1
- IN PCIE_TBT_T_R2D_N<3..0> NO_TEST=1
- IN PCIE_TBT_T_R2D_C_P<3..0> NO_TEST=1
- IN PCIE_TBT_T_R2D_C_N<3..0> NO_TEST=1
- IN PEG_GPU_D2R_C_N<7..0> NO_TEST=1
- IN PEG_GPU_D2R_C_P<7..0> NO_TEST=1
- IN PEG_GPU_R2D_N<7..0> NO_TEST=1
- IN PEG_GPU_R2D_P<7..0> NO_TEST=1

PCH/DFR

- IN USB_CAMERA_DFR_N
- IN USB_CAMERA_DFR_P

BAFFIN FRAME BUFFER

- IN FB_A1_CS_L NO_TEST=1
- IN FB_A0_CKE_L NO_TEST=1
- IN FB_A1_CKE_L NO_TEST=1
- IN FB_A0_WE_L NO_TEST=1
- IN FB_A1_WE_L NO_TEST=1
- IN FB_B1_CS_L NO_TEST=1
- IN FB_B0_CKE_L NO_TEST=1
- IN FB_B1_CKE_L NO_TEST=1
- IN FB_B0_WE_L NO_TEST=1
- IN FB_B0_WE_L NO_TEST=1
- IN FB_B0_CLK_P NO_TEST=1
- IN FB_B1_CLK_N NO_TEST=1
- IN FB_B1_CLK_P NO_TEST=1
- IN FB_B0_RAS_L NO_TEST=1
- IN FB_B1_RAS_L NO_TEST=1
- IN FB_B0_CAS_L NO_TEST=1
- IN FB_B1_CAS_L NO_TEST=1
- IN FB_B0_CS_L NO_TEST=1
- IN FB_A0_DQ<31..0> NO_TEST=1
- IN FB_A1_DQ<31..0> NO_TEST=1
- IN FB_A0_A<8..0> NO_TEST=1
- IN FB_A1_A<8..0> NO_TEST=1
- IN FB_A0_WCLK_N<1..0> NO_TEST=1
- IN FB_A0_WCLK_P<1..0> NO_TEST=1
- IN FB_A1_WCLK_N<1..0> NO_TEST=1
- IN FB_A1_WCLK_P<1..0> NO_TEST=1
- IN FB_A0_EDC<3..0> NO_TEST=1
- IN FB_A1_EDC<3..0> NO_TEST=1
- IN FB_A0_DBI_L<3..0> NO_TEST=1
- IN FB_A1_DBI_L<3..0> NO_TEST=1
- IN FB_A0_ABI_L NO_TEST=1
- IN FB_A1_ABI_L NO_TEST=1
- IN FB_A0_CLK_N NO_TEST=1
- IN FB_A0_CLK_P NO_TEST=1
- IN FB_A1_CLK_N NO_TEST=1
- IN FB_A1_CLK_P NO_TEST=1
- IN FB_A0_RAS_L NO_TEST=1
- IN FB_A1_RAS_L NO_TEST=1
- IN FB_A0_CAS_L NO_TEST=1
- IN FB_A1_CAS_L NO_TEST=1
- IN FB_A0_CS_L NO_TEST=1
- IN FB_B0_CLK_N NO_TEST=1
- IN FB_B0_DQ<31..0> NO_TEST=1
- IN FB_B1_DQ<31..0> NO_TEST=1
- IN FB_B0_A<8..0> NO_TEST=1
- IN FB_B1_A<8..0> NO_TEST=1
- IN FB_B0_WCLK_N<1..0> NO_TEST=1
- IN FB_B0_WCLK_P<1..0> NO_TEST=1
- IN FB_B1_WCLK_N<1..0> NO_TEST=1
- IN FB_B1_WCLK_P<1..0> NO_TEST=1
- IN FB_B0_EDC<3..0> NO_TEST=1
- IN FB_B1_EDC<3..0> NO_TEST=1
- IN FB_B0_DBI_L<3..0> NO_TEST=1
- IN FB_B1_DBI_L<3..0> NO_TEST=1
- IN FB_B0_ABI_L NO_TEST=1
- IN FB_B1_ABI_L NO_TEST=1

CPU/PCH CLK

- IN CPU_CLK24M_NSSC_CLK_N NO_TEST=1
- IN CPU_CLK24M_NSSC_CLK_P NO_TEST=1
- IN CPU_CLK100M_PCIBCLK_N NO_TEST=1
- IN CPU_CLK100M_PCIBCLK_P NO_TEST=1
- IN CPU_CLK100M_BCLK_N NO_TEST=1
- IN CPU_CLK100M_BCLK_P NO_TEST=1
- IN PCIE_CLK100M_SSD_N NO_TEST=1
- IN PCIE_CLK100M_SSD_P NO_TEST=1
- IN PCIE_CLK100M_SSD_LB_N NO_TEST=1
- IN PCIE_CLK100M_SSD_LB_P NO_TEST=1
- IN NC_ITPXDP_CLK100MN NO_TEST=1
- IN NC_ITPXDP_CLK100MP NO_TEST=1
- IN PCIE_CLK100M_AP_P NO_TEST=1
- IN PCIE_CLK100M_AP_N NO_TEST=1

MUX

- IN DP_INT_IG_ML_N<3..0> NO_TEST=1
- IN DP_INT_IG_ML_P<3..0> NO_TEST=1
- IN DP_INT_IG_AUX_N NO_TEST=1
- IN DP_INT_IG_AUX_P NO_TEST=1
- IN DP_INT_EG_ML_N<3..0> NO_TEST=1
- IN DP_INT_EG_ML_P<3..0> NO_TEST=1
- IN DP_INT_EG_AUX_N NO_TEST=1
- IN DP_INT_EG_AUX_P NO_TEST=1

DP MUX CRYSTAL

- IN DPMUX_UC_XTAL NO_TEST=1
- IN DPMUX_UC_EXTAL NO_TEST=1
- IN DPMUX_UC_EXTAL_R NO_TEST=1
- IN DPMUX_UC_XTAL_R NO_TEST=1

XTAL

- IN GPU_XTAL_PU_OR_CAP NO_TEST=1
- IN NC_PCH_CLK24M_XTALOUT NO_TEST=1
- IN SYSCLK_CLK24M_X2 NO_TEST=1
- IN SYSCLK_CLK24M_X2_R NO_TEST=1
- IN SYSCLK_CLK24M_X1 NO_TEST=1

- IN TBT_X_XTAL25M_OUT NO_TEST=1
- IN TBT_X_XTAL25M_OUT_R NO_TEST=1
- IN TBT_X_XTAL25M_IN NO_TEST=1
- IN TBT_T_XTAL25M_OUT NO_TEST=1
- IN TBT_T_XTAL25M_OUT_R NO_TEST=1
- IN SOC_XTAL_24M_O NO_TEST=1
- IN TBT_T_XTAL25M_IN NO_TEST=1
- IN SOC_XTAL_24M_I NO_TEST=1
- IN SOC_XTAL_24M_O_R NO_TEST=1
- IN SSD_CLKIN NO_TEST=1
- IN SSD_CLKOUT NO_TEST=1
- IN SSD_CLKOUT_R NO_TEST=1
- IN GPU_XTAL_OUT NO_TEST=1
- IN GPU_XTAL_OR_CLK_IN NO_TEST=1
- IN GPU_XTAL_XTAL_OR_CLK NO_TEST=1

MEM

- IN MEM_A_CAA<9..0> NO_TEST=1
- IN MEM_A_CLK_P<1..0> NO_TEST=1
- IN MEM_A_CLK_N<1..0> NO_TEST=1
- IN MEM_A_DQ<63..0> NO_TEST=1
- IN MEM_B_DQ<63..0> NO_TEST=1
- IN MEM_A_DQS_P<7..0> NO_TEST=1
- IN MEM_A_DQS_N<7..0> NO_TEST=1
- IN MEM_B_DQS_P<7..0> NO_TEST=1
- IN MEM_B_DQS_N<7..0> NO_TEST=1
- IN MEM_A_CAB<9..0> NO_TEST=1
- IN MEM_B_CAA<9..0> NO_TEST=1
- IN MEM_B_CAB<9..0> NO_TEST=1
- IN MEM_B_CLK_P<1..0> NO_TEST=1
- IN MEM_B_CLK_N<1..0> NO_TEST=1

WIFI

- IN 50_0_ANT NO_TEST=1
- IN 50_1_ANT NO_TEST=1
- IN 50_2_ANT NO_TEST=1
- IN 50_0_COM NO_TEST=1
- IN 50_1_COM NO_TEST=1
- IN 50_2_COM NO_TEST=1
- IN 50_A_0_DIPLEXER NO_TEST=1
- IN 50_A_0_MATCH NO_TEST=1
- IN 50_G_0_DIPLEXER NO_TEST=1
- IN 50_G_0_MATCH NO_TEST=1
- IN 50_A_1_DIPLEXER NO_TEST=1
- IN 50_A_1_MATCH NO_TEST=1
- IN 50_G_1_DIPLEXER NO_TEST=1
- IN 50_G_1_MATCH NO_TEST=1
- IN 50_A_2_DIPLEXER NO_TEST=1
- IN 50_A_2_MATCH NO_TEST=1
- IN 50_G_2_DIPLEXER NO_TEST=1
- IN 50_G_2_MATCH NO_TEST=1

USB-C T

- IN USBC_TA_D2R_P<2..1> NO_TEST=1
- IN USBC_TA_D2R_N<2..1> NO_TEST=1
- IN USBC_TA_R2D_C_P<2..1> NO_TEST=1
- IN USBC_TA_R2D_C_N<2..1> NO_TEST=1
- IN DP_TA_AUXCH_P NO_TEST=1
- IN DP_TA_AUXCH_N NO_TEST=1
- IN DP_TA_AUXCH_C_P NO_TEST=1
- IN DP_TA_AUXCH_C_N NO_TEST=1
- IN USBC_TB_D2R_P<2..1> NO_TEST=1
- IN USBC_TB_D2R_N<2..1> NO_TEST=1
- IN USBC_TB_R2D_C_P<2..1> NO_TEST=1
- IN USBC_TB_R2D_C_N<2..1> NO_TEST=1
- IN DP_TB_AUXCH_P NO_TEST=1
- IN DP_TB_AUXCH_N NO_TEST=1
- IN DP_TB_AUXCH_C_P NO_TEST=1
- IN DP_TB_AUXCH_C_N NO_TEST=1
- IN SSD_NAND_FH_DQ4 NO_TEST=1
- IN SSD_NAND_FH_DQ0 NO_TEST=1
- IN SSD_NAND_FH_DQS_P NO_TEST=1
- IN SSD_NAND_FH_DQ5 NO_TEST=1
- IN SSD_NAND_FH_DQ6 NO_TEST=1
- IN SSD_NAND_FH_DQ7 NO_TEST=1
- IN SSD_NAND_FH_DQS_N NO_TEST=1

NAND

- IN SSD_NAND_FA_DQ0 NO_TEST=1
- IN SSD_NAND_FA_DQ1 NO_TEST=1
- IN SSD_NAND_FA_DQ2 NO_TEST=1
- IN SSD_NAND_FA_DQ3 NO_TEST=1
- IN SSD_NAND_FA_DQ4 NO_TEST=1
- IN SSD_NAND_FA_DQ5 NO_TEST=1
- IN SSD_NAND_FA_DQ6 NO_TEST=1
- IN SSD_NAND_FA_DQ7 NO_TEST=1
- IN SSD_NAND_FA_DQS_N NO_TEST=1
- IN SSD_NAND_FA_DQS_P NO_TEST=1
- IN SSD_NAND_FB_DQ0 NO_TEST=1
- IN SSD_NAND_FB_DQ1 NO_TEST=1
- IN SSD_NAND_FB_DQ2 NO_TEST=1
- IN SSD_NAND_FB_DQ3 NO_TEST=1
- IN SSD_NAND_FB_DQ4 NO_TEST=1
- IN SSD_NAND_FB_DQ5 NO_TEST=1
- IN SSD_NAND_FB_DQ6 NO_TEST=1
- IN SSD_NAND_FB_DQ7 NO_TEST=1
- IN SSD_NAND_FB_DQS_N NO_TEST=1
- IN SSD_NAND_FB_DQS_P NO_TEST=1
- IN SSD_NAND_FC_DQ0 NO_TEST=1
- IN SSD_NAND_FC_DQ1 NO_TEST=1
- IN SSD_NAND_FC_DQ2 NO_TEST=1
- IN SSD_NAND_FC_DQ3 NO_TEST=1
- IN SSD_NAND_FC_DQ4 NO_TEST=1
- IN SSD_NAND_FC_DQ5 NO_TEST=1
- IN SSD_NAND_FC_DQ6 NO_TEST=1
- IN SSD_NAND_FC_DQ7 NO_TEST=1
- IN SSD_NAND_FC_DQS_N NO_TEST=1
- IN SSD_NAND_FC_DQS_P NO_TEST=1
- IN SSD_NAND_FD_DQ0 NO_TEST=1
- IN SSD_NAND_FD_DQ1 NO_TEST=1
- IN SSD_NAND_FD_DQ2 NO_TEST=1
- IN SSD_NAND_FD_DQ3 NO_TEST=1
- IN SSD_NAND_FD_DQ4 NO_TEST=1
- IN SSD_NAND_FD_DQ5 NO_TEST=1
- IN SSD_NAND_FD_DQ6 NO_TEST=1
- IN SSD_NAND_FD_DQ7 NO_TEST=1
- IN SSD_NAND_FD_DQS_N NO_TEST=1
- IN SSD_NAND_FD_DQS_P NO_TEST=1
- IN SSD_NAND_FE_DQ0 NO_TEST=1
- IN SSD_NAND_FE_DQ1 NO_TEST=1
- IN SSD_NAND_FE_DQ2 NO_TEST=1
- IN SSD_NAND_FE_DQ3 NO_TEST=1
- IN SSD_NAND_FE_DQ4 NO_TEST=1
- IN SSD_NAND_FE_DQ5 NO_TEST=1
- IN SSD_NAND_FE_DQ6 NO_TEST=1
- IN SSD_NAND_FE_DQ7 NO_TEST=1
- IN SSD_NAND_FE_DQS_N NO_TEST=1
- IN SSD_NAND_FE_DQS_P NO_TEST=1
- IN SSD_NAND_FF_DQ0 NO_TEST=1
- IN SSD_NAND_FF_DQ1 NO_TEST=1
- IN SSD_NAND_FF_DQ2 NO_TEST=1
- IN SSD_NAND_FF_DQ3 NO_TEST=1
- IN SSD_NAND_FF_DQ4 NO_TEST=1
- IN SSD_NAND_FF_DQ5 NO_TEST=1
- IN SSD_NAND_FF_DQ6 NO_TEST=1
- IN SSD_NAND_FF_DQ7 NO_TEST=1
- IN SSD_NAND_FF_DQS_N NO_TEST=1
- IN SSD_NAND_FF_DQS_P NO_TEST=1
- IN SSD_NAND_FG_DQ0 NO_TEST=1
- IN SSD_NAND_FG_DQ2 NO_TEST=1
- IN SSD_NAND_FG_DQ3 NO_TEST=1
- IN SSD_NAND_FG_DQ4 NO_TEST=1
- IN SSD_NAND_FG_DQ5 NO_TEST=1
- IN SSD_NAND_FG_DQ6 NO_TEST=1
- IN SSD_NAND_FG_DQ7 NO_TEST=1
- IN SSD_NAND_FG_DQS_N NO_TEST=1
- IN SSD_NAND_FG_DQS_P NO_TEST=1
- IN SSD_NAND_FH_DQ1 NO_TEST=1
- IN SSD_NAND_FH_DQ2 NO_TEST=1
- IN SSD_NAND_FH_DQ3 NO_TEST=1

SYNC_MASTER=X363_SAKKOC SYNC_DATE=04/14/2016

PAGE TITLE

ICT & FCT 1

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

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MESA CONNECTOR

45	IN	PP3V0_MESA_CONN	FUNC_TEST=TRUE
45	IN	MESA_SPI_MISO_CONN	FUNC_TEST=TRUE
45	IN	MESA_SNSR_INT_CONN	FUNC_TEST=TRUE
45	IN	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE
45 37	IN	MESA_I2C_SDA	FUNC_TEST=TRUE
45 37	IN	MESA_I2C_SCL	FUNC_TEST=TRUE
45	IN	PP1V8_MESA_CONN	FUNC_TEST=TRUE
45	IN	MESA_SPI_MOSI_CONN	FUNC_TEST=TRUE
45	IN	MENU_KEY_L	FUNC_TEST=TRUE
45	IN	MESA_SPI_CLK_CONN	FUNC_TEST=TRUE
45	IN	PP16V0_MESA_CONN	FUNC_TEST=TRUE
		GND	

SPI ROM

114 109	IN	PP3V3_G3H	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO0_MOSI	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO1_MISO	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO2_WP_L	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO3_HOLD_L	FUNC_TEST=TRUE
76 64 57 48 29 114	IN	SMC_RESET_L	FUNC_TEST=TRUE
57	IN	SPI_ALT_CLK	FUNC_TEST=TRUE
57	IN	SPI_ALT_CS_L	FUNC_TEST=TRUE
57 15	IN	SPIROM_USE_MLB	FUNC_TEST=TRUE
57 47 46	IN	SMC_TMS	FUNC_TEST=TRUE
57 47 46	IN	SMC_TCK	FUNC_TEST=TRUE
		GND	

AUDIO AMP

61	IN	SPKRCONN_TR_OUT_POS	FUNC_TEST=TRUE
61	IN	SPKRCONN_TR_OUT_NEG	FUNC_TEST=TRUE
61	IN	SPKRCONN_WR_OUT_POS	FUNC_TEST=TRUE
61	IN	SPKRCONN_WR_OUT_NEG	FUNC_TEST=TRUE
60	IN	SPKRCONN_TL_OUT_POS	FUNC_TEST=TRUE
60	IN	SPKRCONN_TL_OUT_NEG	FUNC_TEST=TRUE
60	IN	SPKRCONN_WL_OUT_POS	FUNC_TEST=TRUE
60	IN	SPKRCONN_WL_OUT_NEG	FUNC_TEST=TRUE
61 58	IN	SPKR_ID0	FUNC_TEST=TRUE
		GND	FUNC_TEST=

DFR Touch Conn

42	IN	DFR_TOUCH_LID	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_GPIO2	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_SPI_CS_L	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MOSI_R	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SDA	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_RESET_L	FUNC_TEST=TRUE
114 42 37	IN	PP1V8_S0SW_DFR	X2 FUNC_TEST=TRUE
110	IN	PP5V_S0_T139	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE
114 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MISO_R	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_CLK_R	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_INT_L	FUNC_TEST=TRUE
42 38	IN	DFR_CLKIN_RESET_L	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_ROM_WC	FUNC_TEST=TRUE
		GND	X4

DFR Disp Conn

114 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_TE	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_INT	FUNC_TEST=TRUE
42	IN	DFR_DISP_RESET_L	FUNC_TEST=TRUE
42	IN	PP3V3_S0SW_DFR	X3 FUNC_TEST=TRUE
42 38	IN	MIPID_CLK_P	FUNC_TEST=TRUE
42 38	IN	MIPID_CLK_N	FUNC_TEST=TRUE
42 38	IN	MIPID_DATA_P	FUNC_TEST=TRUE
42 38	IN	MIPID_DATA_N	FUNC_TEST=TRUE
114 42 37	IN	PP1V8_S0SW_DFR	X2 FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SDA	FUNC_TEST=TRUE
		GND	X6

KBD CONNECTOR

43	IN	GND_FAN	X2 FUNC_TEST=TRUE
43	IN	PP5V_S0_FAN_CONN	X2 FUNC_TEST=TRUE
115 56 43	IN	FAN_LT_TACH	FUNC_TEST=TRUE
115 56 43	IN	FAN_LT_PWM	FUNC_TEST=TRUE
110	IN	PP5V_S0_KBD	X2 FUNC_TEST=TRUE
114 109	IN	PP3V3_G3H	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
110 103 29	IN	PP3V3_S4	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
43	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
115 56 43	IN	FAN_RT_TACH	FUNC_TEST=TRUE
115 56 43	IN	FAN_RT_PWM	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
114 43	IN	KBD_INT_L	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
114 48 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
		GND	X5

TPAD CONNECTOR

114 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
114 43	IN	KBD_INT_L	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_3_SDA	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_3_SCL	FUNC_TEST=TRUE
110	IN	PP3V3_S4_TPAD	FUNC_TEST=TRUE
43	IN	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
43	IN	ACT_GND	X4 FUNC_TEST=TRUE
43	IN	PPVIN_S4_TPAD_FUSE	X4 FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_CLK	FUNC_TEST=TRUE
43	IN	TPAD_SPI_IF_EN_CONN	FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_MISO	FUNC_TEST=TRUE
43	IN	TPAD_SPI_CS_L_CONN	FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_MOSI	FUNC_TEST=TRUE
43	IN	TPAD_SPI_INT_L_CONN	FUNC_TEST=TRUE
48 46	IN	SMC_ACTUATOR_DISABLE_L	FUNC_TEST=TRUE
48 47 46	IN	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
48 47 43 42	IN	SMC_LID	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
46 43	IN	SMC_VIBE_L	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
		GND	X3

eDP

116 76 75	IN	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
76	IN	PP3V3_S0SW_LCD	X2 FUNC_TEST=TRUE
76	IN	EDP_AUXCH_C_N	FUNC_TEST=TRUE
76	IN	EDP_AUXCH_C_P	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<0>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<0>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<1>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<1>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<2>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<2>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<3>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<3>	FUNC_TEST=TRUE
38	IN	MIPIC_CLK_N	FUNC_TEST=TRUE
38	IN	MIPIC_CLK_P	FUNC_TEST=TRUE
76	IN	PP5V_S0SW_LCD	FUNC_TEST=TRUE
76 38	IN	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
76 42	IN	I2C_ALS_SDA	FUNC_TEST=TRUE
76 42	IN	I2C_ALS_SCL	FUNC_TEST=TRUE
76 38 37	IN	I2C_CAM_SCL	FUNC_TEST=TRUE
76 38 37	IN	I2C_CAM_SDA	FUNC_TEST=TRUE
111 76	IN	I2C_BKLT_SDA	FUNC_TEST=TRUE
111 76	IN	I2C_BKLT_SCL	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
76 48	IN	BKLT_PWM_TCON2MLB	FUNC_TEST=TRUE
76 20	IN	BKLT_PWM_MLB2TCON	FUNC_TEST=TRUE
89 76	IN	LCD_FSS	FUNC_TEST=TRUE
76 15	IN	LCD_IRQ_L	FUNC_TEST=TRUE
76	IN	BUF_EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
89 76	IN	DP_INT_HPD	FUNC_TEST=TRUE
		GND	X3
76 49	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
76 49	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
38	IN	MIPIC_DATA_P	FUNC_TEST=TRUE
38	IN	MIPIC_DATA_N	FUNC_TEST=TRUE

AUDIO JACK

62	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
62	IN	AUD_CONN_RING2	FUNC_TEST=TRUE
62	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
62	IN	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
62	IN	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
62	IN	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
		GND	X2

BATTERY TUBA

64 63	IN	PPVBAT_G3H_CONN	X7 FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_5_G3_SCL	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_5_G3_SDA	FUNC_TEST=TRUE
63	IN	TP_BMON_IOUT	FUNC_TEST=TRUE
64 56	IN	CHGR_AMON	FUNC_TEST=TRUE
64 56	IN	CHGR_BMON	FUNC_TEST=TRUE
63	IN	SYS_DETECT_L	FUNC_TEST=TRUE
		GND	X5
114 48 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
64	IN	TBA_COMP	FUNC_TEST=TRUE
64	IN	TBA_VDDA	FUNC_TEST=TRUE
64	IN	TBA_LX1	FUNC_TEST=TRUE
64	IN	TBA_LX2	FUNC_TEST=TRUE
		GND	X2
64	IN	PPVBAT_G3H_CHGR_REG	X5 FUNC_TEST=TRUE
116 64 63	IN	PPDCIN_G3H_CHGR	X5 FUNC_TEST=TRUE

USB_C

TP_UPC_XA_SWD_DATA	---------->	TP3001
TP_UPC_XA_SWD_CLK	---------->	TP3002
TP_UPC_XB_SWD_DATA	---------->	TP3003
TP_UPC_XB_SWD_CLK	---------->	TP3004

104 103	IN	TP_UPC_TA_DBG_UART_TX	FUNC_TEST=TRUE
104 103	IN	TP_UPC_TA_DBG_UART_RX	FUNC_TEST=TRUE
105 103	IN	TP_UPC_TB_DBG_UART_TX	FUNC_TEST=TRUE
105 103	IN	TP_UPC_TB_DBG_UART_RX	FUNC_TEST=TRUE
30 29	IN	UPC_XA_DBG_UART_TX	FUNC_TEST=TRUE
30 29	IN	UPC_XA_DBG_UART_RX	FUNC_TEST=TRUE
31 29	IN	TP_UPC_XB_DBG_UART_TX	FUNC_TEST=TRUE
31 29	IN	TP_UPC_XB_DBG_UART_RX	FUNC_TEST=TRUE
116 115 106	IN	PP20V_USBC_TB_VBUS_CONN	X5 FUNC_TEST=TRUE
116 115 106	IN	PP20V_USBC_TA_VBUS_CONN	X5 FUNC_TEST=TRUE
		GND	X5
116 115 32	IN	PP20V_USBC_XB_VBUS_CONN	X4 FUNC_TEST=TRUE
116 115 32	IN	PP20V_USBC_XA_VBUS_CONN	X5 FUNC_TEST=TRUE
		GND	X5

SSD DEBUG CONNECTOR

115 87 77	IN	SSD_BOOT_LB_L	FUNC_TEST=TRUE
80 77	IN	SSD_BOOT_LB_L	FUNC_TEST=TRUE
103 86 80	IN	SSD_DEBUG_I2C_CLK_CONN	FUNC_TEST=TRUE
103 86 80	IN	SSD_DEBUG_I2C_DAT_CONN	FUNC_TEST=TRUE
80 77 48	IN	SMC_OOB1_R2D_L	FUNC_TEST=TRUE
80 77 48	IN	SMC_OOB1_D2R_L	FUNC_TEST=TRUE
83 82 81 80 78 77 85	IN	PP1V8_SSD_FMC	
		GND	

MIC

58	IN	DMIC1_CLK	FUNC_TEST=TRUE
58	IN	DMIC1_DATA	FUNC_TEST=TRUE
58	IN	DMIC2_CLK	FUNC_TEST=TRUE
58	IN	DMIC2_DATA	FUNC_TEST=TRUE
109 61	IN	PP1V8_S0	FUNC_TEST=TRUE
		GND	

USB-C PROBE BLOCK TESTING

32	IN	TP_J3300_P2	FUNC_TEST=TRUE	TPAC580
32	IN	TP_J3300_P56	FUNC_TEST=TRUE	TPAC581
106	IN	TP_JB500_P2	FUNC_TEST=TRUE	TPAC582
106	IN	TP_JB500_P56	FUNC_TEST=TRUE	TPAC583

ADDITIONAL TPs

110	IN	PP3V3_S5	FUNC_TEST=TRUE	TPAC584
110	IN	PP3V3_SUS	FUNC_TEST=TRUE	TPAC585

Wifi & SSD fixture Test Points
(row,col)=(4,2) Diameter=0.6mm Pitch=1mm

Right Side - Top Layer

			TPAC528
80 77	SSD_JTAG_TMS		TPAC519
80 77	SSD_JTAG_TCK		TPAC520
80 77	SSD_JTAG_TDI		TPAC521
80 77	SSD_JTAG_TDO		TPAC522
86 77	SSD_DEBUG_I2C_CLK		TPAC523
86 77	SSD_DEBUG_I2C_DAT		TPAC524
84 77	SSD_PGOOD_L		TPAC535

(row,col)=(2,6) Diameter=0.6mm Pitch=1mm

Left Side - Top Layer

50 114	PPDCIN_G3H		TPAC500
50 114	PPDCIN_G3H		TPAC501
50 114	PPDCIN_G3H		TPAC502
50 114	PPDCIN_G3H		TPAC503
			TPAC504
			TPAC505
			TPAC506
			TPAC507
	GND	TRUE	TPAC529
64	HPWR_EN_L		TPAC512
110	PP3V3_S0		TPAC536
114 109	PP3V3_G3H		TPAC518

(row,col)=(5,5) Diameter=0.6mm Pitch=1mm

Middle - Top Layer

46 48 45 47	SMC_ONOFF_L		TPAC517
			TPAC538
28 20 114	SMC_RESET_L		TPAC539
			TPAC527
14	USB3_TEST_D2R_N		TPAC510
14	USB3_TEST_D2R_P		TPAC511
			TPAC595
			TPAC596
84 78	PP1V0_SSD_CORE		TPAC598
109	PPVCC_S0_CPU		TPAC597
109	PPBUS_G3H		TPAC599
14	USB3_TEST_R2D_N		TPAC525
14	USB3_TEST_R2D_P		TPAC526
29 35	AP_RESET_L		TPAC537
14	USB_TEST_P		TPAC530
14	USB_TEST_N		TPAC531
29 115	SSD_RESET_L		TPAC532
46 12 75	PM_PCH_SYS_PWROK		TPAC533
87 14 115	SSD_PWR_EN		TPAC534
46 29 47	SMC_DEBUGPRT_TX_L		TPAC508
46 29 47	SMC_DEBUGPRT_RX_L		TPAC509
87 15 115 101	SSD_BOOT_L		TPAC513
73 72 17 49 89 76	PM_SLP_S3_L		TPAC514
48	SMC_DEV_SUPPLY_R_L		TPAC515
20 32 35	PLT_RST_L		TPAC516

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OTHER TEST POINTS / NC

NC with No Testpoint Property

13	NC_CLINK_CLK	1	TRUE		NC_CLINK_CLK
13	NC_CLINK_DATA	1	TRUE		NC_CLINK_DATA
13	NC_CLINK_RESET_L	1	TRUE		NC_CLINK_RESET_L
113 18 12	NC_ITPXDP_CLK100MN	1	TRUE		NC_ITPXDP_CLK100MN
113 18 12	NC_ITPXDP_CLK100MP	1	TRUE		NC_ITPXDP_CLK100MP
13	NC_HDA_SDIN1	1	TRUE		NC_HDA_SDIN1
11	NC_SPI_SMC_MOSI	1			48
12	NC_SPI_SMC_MISO	1			48
14	NC_SPI_SMC_CS_L	1			48
13	NC_SPI_SMC_CLK	1			48
17	NC_PCH_CLK32K_RTCX2				20

FAN Test Points

123	TRUE	FAN_LT_PWM	43 56 114
124	TRUE	FAN_LT_TACH	43 56 114
127	TRUE	PP5V_S0	38 110 115
128	TRUE	FAN_RT_PWM	43 56 114
129	TRUE	FAN_RT_TACH	43 56 114
130	TRUE	PP5V_S0	38 110 115

XDP Test-Points

152	TRUE	XDP_CPU_TCK	6 18
153	TRUE	XDP_PCH_TCK	13 18
157	TRUE	XDP_CPU_TDI	6 18
156	TRUE	XDP_CPU_TDO	6 18
155	TRUE	XDP_CPU_TRST_L	6 13 18
154	TRUE	XDP_CPU_TMS	6 18
158	TRUE	XDP_PCH_TMS	13 18
162	TRUE	XDP_PCH_TDI	13 18
161	TRUE	XDP_PCH_TDO	13 18
160	TRUE	XDP_CPU_PREQ_L	6 13 18
159	TRUE	XDP_CPU_PRDY_L	6 13 18
163	TRUE	PM_RSMRST_L	12 18 46 73
164	TRUE	PM_PCH_PWROK	12 70
165	TRUE	PM_SYSRST_L	12 18 46
166	TRUE	CPU_CFG<3>	6 18

CPU (Refer to CPU pages)

CPU_DC_B2_C1	TP0501
CPU_DC_B38_C38	TP0502
CPU_DC_BR2_BR1	TP0503
CPU_DC_C1_B2	TP0504
CPU_DC_C38_B38	TP0505
CPU_DC_BR1_BR2	TP0610
CPU_DC_BR38_BT36	TP0900
CPU_DC_BT36_BR38	TP0901

PCH (Refer to PCH pages)

XDP_PCH_OBSDATA_A0	TP1883
XDP_PCH_OBSDATA_A1	TP1884
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_B1	TP1885
XDP_PCH_OBSDATA_B2	TP1886
XDP_PCH_OBSDATA_B3	TP1887
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C0	TP1882
XDP_BPM_L<0>	TP1800
XDP_BPM_L<1>	TP1801
XDP_BPM_L<2>	TP1802
XDP_BPM_L<3>	TP1803
NC_USB_EXTA_OC_L	TP1873
NC_USB_EXTB_OC_L	TP1874
NC_USB_EXTC_OC_L	TP1875
NC_USB_EXTD_OC_L	TP1876

TPs on BOTTOM to check USB-C Instalation

175	USBC_XA_SBU1	FUNC_TEST=TRUE	30 32
176	USBC_XB_SBU1	FUNC_TEST=TRUE	31 32
177	USBC_XA_SBU2	FUNC_TEST=TRUE	30 32
178	USBC_XB_SBU2	FUNC_TEST=TRUE	31 32
179	USBC_TA_SBU1	FUNC_TEST=TRUE	104 106
180	USBC_TB_SBU1	FUNC_TEST=TRUE	105 106
181	USBC_TA_SBU2	FUNC_TEST=TRUE	104 106
182	USBC_TB_SBU2	FUNC_TEST=TRUE	105 106
***	PP20V_USBC_XA_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
183	PP20V_USBC_XB_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
185	PP20V_USBC_TA_VBUS_CONN	FUNC_TEST=TRUE	106 114 116
184	PP20V_USBC_TB_VBUS_CONN	FUNC_TEST=TRUE	106 114 116

TPs to check LifeBoat Instalation

186	PP3V3_S5_POLARIS	FUNC_TEST=TRUE	84 87
187	PP3V3_S5	FUNC_TEST=TRUE	110
192	SSD_PWR_EN	FUNC_TEST=TRUE	14 87 114
189	SSD_PWR_LB_EN	FUNC_TEST=TRUE	84 87
191	SSD_BOOT_L	FUNC_TEST=TRUE	15 87 114
197	SSD_BOOT_LB_L	FUNC_TEST=TRUE	77 87 114
193	SSD_RESET_L	FUNC_TEST=TRUE	14 20 87 114
195	SSD_RESET_LB_L	FUNC_TEST=TRUE	77 87
194	SSD_CLKREQ_L	FUNC_TEST=TRUE	20 87
196	SSD_CLKREQ_LB_L	FUNC_TEST=TRUE	77 87

SYNC_MASTER=K363_BBABADI SYNC_DATE=01/26/2016

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00041	6	CAP,CER,12PF,5%,100V,C0G,0402	CC784,CC785,CC786,CC787,CC788	CRITICAL	

PAGE TITLE

Desense Caps

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BOM_COST_GROUP=WIRELESS

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Project Specific Constraints

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BOM Variants

44 ULA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02212	MLB,2.6G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02120	MLB,2.6G,MC-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02591	MLB,2.6G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02214	MLB,2.6G,MC-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02587	MLB,2.6G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02116	MLB,2.6G,SM-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02589	MLB,2.6G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02586	MLB,2.6G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01615	MLB,2.7G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02592	MLB,2.7G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01614	MLB,2.7G,MC-16,ULA-MC,SSD-512,X36G3	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01603	MLB,2.7G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02594	MLB,2.7G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01602	MLB,2.7G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01639	MLB,2.9G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01637	MLB,2.9G,MC-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02596	MLB,2.9G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01638	MLB,2.9G,MC-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01627	MLB,2.9G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01625	MLB,2.9G,SM-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02598	MLB,2.9G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01626	MLB,2.9G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02154	MLB,2.6G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02119	MLB,2.6G,MC-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02590	MLB,2.6G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02213	MLB,2.6G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02211	MLB,2.6G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02115	MLB,2.6G,SM-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02588	MLB,2.6G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02585	MLB,2.6G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01612	MLB,2.7G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02593	MLB,2.7G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01611	MLB,2.7G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01600	MLB,2.7G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02595	MLB,2.7G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01599	MLB,2.7G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01636	MLB,2.9G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01634	MLB,2.9G,MC-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02597	MLB,2.9G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01635	MLB,2.9G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01624	MLB,2.9G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01622	MLB,2.9G,SM-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02599	MLB,2.9G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01623	MLB,2.9G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB

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BOM NUMBER	BOM NAME	BOM OPTIONS
639-02655	MLB,2.7G,MC-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02656	MLB,2.7G,MC-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02654	MLB,2.7G,MC-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02664	MLB,2.7G,SM-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02665	MLB,2.7G,SM-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02663	MLB,2.7G,SM-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02673	MLB,2.9G,MC-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02674	MLB,2.9G,MC-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02672	MLB,2.9G,MC-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02682	MLB,2.9G,SM-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02683	MLB,2.9G,SM-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02681	MLB,2.9G,SM-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02652	MLB,2.7G,MC-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02653	MLB,2.7G,MC-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02651	MLB,2.7G,MC-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02661	MLB,2.7G,SM-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02662	MLB,2.7G,SM-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02660	MLB,2.7G,SM-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02670	MLB,2.9G,MC-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02671	MLB,2.9G,MC-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02669	MLB,2.9G,MC-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02679	MLB,2.9G,SM-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02680	MLB,2.9G,SM-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02678	MLB,2.9G,SM-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02649	MLB,2.7G,MC-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02650	MLB,2.7G,MC-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02648	MLB,2.7G,MC-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02658	MLB,2.7G,SM-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02659	MLB,2.7G,SM-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02657	MLB,2.7G,SM-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02667	MLB,2.9G,MC-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02668	MLB,2.9G,MC-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02666	MLB,2.9G,MC-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02676	MLB,2.9G,SM-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02677	MLB,2.9G,SM-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02675	MLB,2.9G,SM-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB

BOM Variants, Power/Socket Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01966	PCBA,MLB,NONE,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01967	PCBA,MLB,SKT,VDDC,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01968	PCBA,MLB,SKT,MVDD,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC?_MVDD,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01969	PCBA,MLB,SKT,CPU,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,CPU_SKL:SOCKET,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB

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BOM Variants

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BOM NUMBER	BOM NAME	BOM OPTIONS
639-02621	MLB,2.6G,MC-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02618	MLB,2.6G,MC-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02622	MLB,2.6G,MC-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02620	MLB,2.6G,MC-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02608	MLB,2.6G,SM-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02602	MLB,2.6G,SM-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02611	MLB,2.6G,SM-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02605	MLB,2.6G,SM-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02645	MLB,2.9G,MC-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02643	MLB,2.9G,MC-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02646	MLB,2.9G,MC-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02644	MLB,2.9G,MC-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02633	MLB,2.9G,SM-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02631	MLB,2.9G,SM-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02634	MLB,2.9G,SM-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02632	MLB,2.9G,SM-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02647	MLB,2.6G,MC-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02616	MLB,2.6G,MC-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02619	MLB,2.6G,MC-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02617	MLB,2.6G,MC-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02607	MLB,2.6G,SM-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02601	MLB,2.6G,SM-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02610	MLB,2.6G,SM-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02604	MLB,2.6G,SM-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02641	MLB,2.9G,MC-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02639	MLB,2.9G,MC-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02642	MLB,2.9G,MC-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02640	MLB,2.9G,MC-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02629	MLB,2.9G,SM-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02627	MLB,2.9G,SM-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02630	MLB,2.9G,SM-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02628	MLB,2.9G,SM-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02614	MLB,2.6G,MC-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02612	MLB,2.6G,MC-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02615	MLB,2.6G,MC-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02613	MLB,2.6G,MC-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02606	MLB,2.6G,SM-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02600	MLB,2.6G,SM-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02609	MLB,2.6G,SM-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02603	MLB,2.6G,SM-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02637	MLB,2.9G,MC-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02635	MLB,2.9G,MC-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02638	MLB,2.9G,MC-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02636	MLB,2.9G,MC-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02625	MLB,2.9G,SM-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02623	MLB,2.9G,SM-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02626	MLB,2.9G,SM-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02624	MLB,2.9G,SM-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB

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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
740S0144	740S0118		ALL		
740S00003	740S0135		ALL		
376S1089	376S1128		ALL		
376S1080	376S0820		ALL		
376S00086	376S0761		ALL		
376S00074	376S0855		ALL		
376S00014	376S0761		ALL		
372S0186	372S0185		ALL		
371S0713	371S0558		ALL		
311S00060	311S0273		ALL		
311S00004	311S0370		ALL		
155S0914	155S0897		ALL		
155S0694	155S0387		ALL		
155S0660	155S0513		ALL		
155S00154	155S0398		ALL		
155S00007	155S0667		ALL		
138S0863	138S0853		ALL		
138S0775	138S0860		ALL		<rdar://problem/23155097> for IG <rdar://problem/23564467> for EG
138S0703	138S0648		ALL		<rdar://problem/23118084> for IG <rdar://problem/> for EG
132S00064	132S0409		ALL		
128S0325	128S0397		ALL		
128S00029	128S00007		ALL		
128S00026	128S00011		ALL		
128S00070	128S00007		ALL		<rdar://problem/25329164>
128S00009	128S00007		ALL		
107S0249	107S0251		ALL		
107S00071	107S00053		ALL		
107S00070	107S0085		ALL		
107S00033	107S00034		ALL		BLC
107S00015	107S00011		ALL		
376S1106	376S0678		ALL	Fairchild alt to Vishay	BLC
138S0738	138S1101		ALL	Samsung alt to Murata	
138S0846	138S0811		ALL	Samsung alt to Murata	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
152S00359	152S00253		ALL	Chillisin alt to Cyntec	
740S00027	740S0159		ALL	Bourns alt to Little Fuse	
371S0704	371S00077		ALL	NXP alt to Diodes	
138S00032	138S0831		ALL		
138S00049	138S0831		ALL		
998-04070	998-04071		OFF	Hynix alt to SS	220uF 2.0V D-case, 128S00044 DQ - T208
128S00010	128S00011		ALL		
128S00031	128S00011		ALL		
138S00084	138S0060		ALL		<rdar://problem/23118634> for IG <rdar://problem/23527737> for EG
155S00155	155S0441		OFF		(Stale; delete later after page sync)
155S00190	155S0897		ALL		
353S00107	353S3239		ALL		
353S00525	353S4471		ALL		
376S1193	376S0037		OFF		
740S00028	740S0118		ALL		
152S00369	152S00268		ALL	Cyntec w/ NEC	<rdar://problem/23405116> for IG <rdar://problem/23542193> for EG
128S0296	128S0487		ALL	NEC w/ pana	<rdar://problem/23422212> for IG <rdar://problem/23527282> for EG
128S00012	128S0487		ALL	NEC w/ Rohm	
155S00188	155S0275		ALL	Murata w/ Taiyo	<rdar://problem/23446936> for IG <rdar://problem/23542939> for EG
155S00018	155S0664		ALL	Murata w/ Taiyo	<rdar://problem/23447549> for IG <rdar://problem/23543068> for EG
152S00388	152S00182		ALL		<rdar://problem/23542023>
107S0240	107S0255		ALL		<rdar://problem/23520324>
128S00062	128S00067		ALL	NEC for Panasonic	150uF 6.3V B12
138S0660	138S0684		ALL		<rdar://problem/24316249>
155S00204	155S0731		ALL		<rdar://problem/24310837>

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197S00046	197S00036		ALL	Epson w/ TXC	<rdar://problem/23117749> for IG <rdar://problem/23543146> for EG
197S00047	197S00036		ALL	Kyocera w/ TXC	
197S00048	197S00036		ALL	Murata w/ TXC	
197S00053	197S00050		ALL	Kyocera w/ TXC	<rdar://problem/23117849> for IG <rdar://problem/23543858> for EG
197S00054	197S00050		ALL	NDK w/ TXC	
197S00055	197S00050		ALL	Murata w/ TXC	
311S0596	311S0593		ALL	NXP w/ Diodes	<rdar://problem/23118093> for IG <rdar://problem/23544824> for EG
107S0276	107S00020		ALL	Cyntec w/ TFT	<rdar://problem/23117951> for IG <rdar://problem/23542980> for EG
107S00021	107S0284		ALL	TFT w/ Yageo	<rdar://problem/23129685> for IG <rdar://problem/23519943> for EG
132S00012	132S0401		ALL	Taiyo w/ Murata&TDK	<rdar://problem/23118402> for IG <rdar://problem/23527525> for EG
152S00343	152S1682		ALL	NXP w/ Diodes	<rdar://problem/23541694> for IG <rdar://problem/23541871> for EG
107S00087	107S00029		ALL	TFT w/ Yageo	<rdar://problem/23121290> for IG <rdar://problem/23520039> for EG
128S00057	128S00018		ALL	NEC w/ Vishay	<rdar://problem/23363718> for IG <rdar://problem/23526361> for EG
128S00058	128S00018		ALL	NEC w/ Rohm	
128S0364	128S0264		ALL	Kemet w/ Panasonic	<rdar://problem/23366105> for IG <rdar://problem/23527232> for EG
138S0641	138S0700		ALL	Murata w/ SS&Taiyo	<rdar://problem/23118759> for IG <rdar://problem/23528188> for EG
138S0739	138S0706		ALL	NEC w/ Vishay	<rdar://problem/23118915> for IG <rdar://problem/23528364 for EG
138S0945	138S0706		ALL	NEC w/ Rohm	
152S00358	152S00208		ALL	Murata w/ Chillisin	<rdar://problem/23119390> for IG <rdar://problem/23542869> for EG
152S00389	152S00241		OFF	Cyntec w/ Vishay	<rdar://problem/23342644> for IG <rdar://problem/> for EG
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152S00400	152S1872		ALL	Murata w/ Cyntec	
152S1872	152S00361		ALL	Murata w/ Cyntec	<rdar://problem/23132240> for IG <rdar://problem/23542412> for EG
155S00034	155S0706		ALL	Taiyo w/ Murata	<rdar://problem/23118020> for IG <rdar://problem/23543015> for EG
371S00082	371S00046		ALL	On-Semi w/ Diodes	<rdar://problem/23341512> for IG <rdar://problem/23545301> for EG
376S00146	376S1061		ALL	NXP w/ Diodes	<rdar://problem/23341674> for IG <rdar://problem/23545469> for EG
353S00711	353S2073		ALL	On Semi w/ TI	<rdar://problem/23605939> for IG <rdar://problem/23605957> for EG
740S00019	740S00007		ALL	Bourns w/ Polytronics	<rdar://problem/23137505> for IG <rdar://problem/23545479> for EG
155S00189	155S0342		ALL	Murata w/ Taiyo	<rdar://problem/23117986> for IG <rdar://problem/23543015> for EG
132S0438	132S0428		ALL	Murata w/ Taiyo&TDK	<rdar://problem/23118548> for IG <rdar://problem/23527609> for EG
138S0714	138S0713		ALL	Murata w/ Samsung	<rdar://problem/23118842> for IG <rdar://problem/23528300> for EG
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138S0786	138S0705		ALL	Murata w/ Samsung	<rdar://problem/23129934> for IG <rdar://problem/23528216> for EG
155S0382	155S0659		ALL	Murata w/ TDK	<rdar://problem/23132624> for IG <rdar://problem/23543045> for EG
152S2052	152S1954		ALL	Taiyo w/ Cyntec	<rdar://problem/23135833> for IG <rdar://problem/23542478> for EG
152S2015	152S1958		ALL	Taiyo w/ Cyntec	<rdar://problem/23137154> for IG <rdar://problem/23542579> for EG
128S00055	128S00002		ALL	Kemet w/ Panasonic	<rdar://problem/23148659> for IG <rdar://problem/23526236> for EG
138S0748	138S0751		ALL	Murata w/ SS	<rdar://problem/23155052> for IG <rdar://problem/23528417> for EG
138S00102	138S0773		ALL	Murata w/ Taiyo	<rdar://problem/23155089> for IG <rdar://problem/23529046> for EG
138S0789	138S0941		ALL	Murata w/ SS	<rdar://problem/23155132> for IG <rdar://problem/23529142> for EG
107S00101	107S00005		ALL	Cyntec w/ Yageo	<rdar://problem/23193801> for IG <rdar://problem/23519872> for EG
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107S00103	107S00058		ALL	Cyntec w/ Yageo	<rdar://problem/23228523> for IG <rdar://problem/23520163> for EG
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107S00105	107S00062		ALL	Cyntec w/ Yageo	<rdar://problem/23230371> for IG <rdar://problem/23520241> for EG
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353S00852	353S4262		ALL	TI w/ OnSemi	<rdar://problem/23341158> for IG <rdar://problem/23542282> for EG
138S00104	138S0978		ALL		<rdar://problem/23583487>
128S00069	128S00067		ALL	Rohm for Panasonic	150uF 6.3V B12 <rdar://problem/23527054>
138S0759	138S0762		ALL		<rdar://problem/23582324>
377S0077	377S0183		ALL		<rdar://problem/23640745>
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311S00007	311S0426		ALL		<rdar://problem/23597412>
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353S00991	353S00920		ALL		
131S00134	131S00041		ALL		<rdar://problem/24316117>

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