

Compal Confidential

2014 S-series(400series) Rolo/Reeses/Raisinet

INTEL Sharkbay & Crescent bay ULT –U processor with DDR3L

www.laptoprepairsecrets.com

Date : 2014/02/18

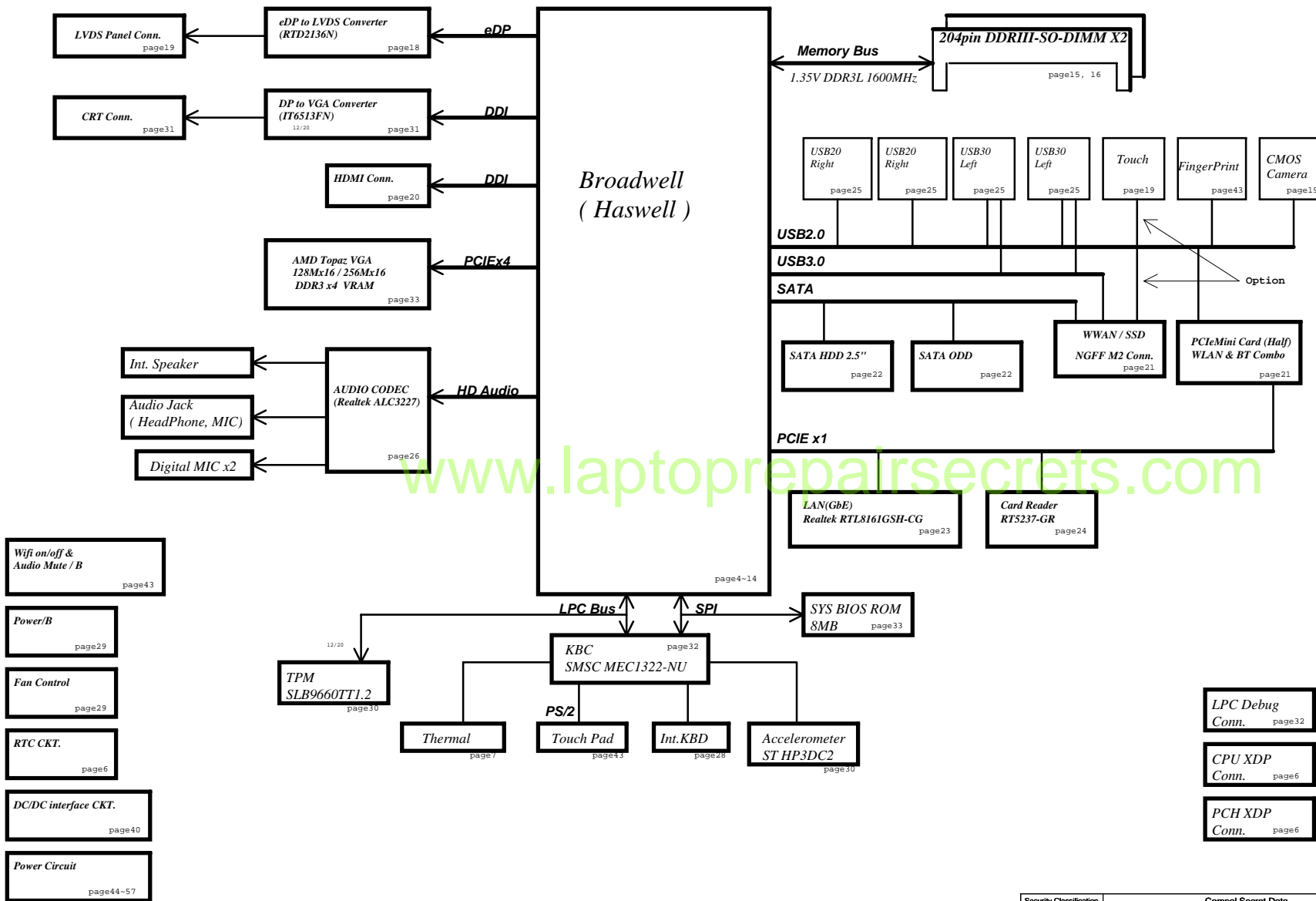
Version 0.5

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Cover Page
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B181P	0.5
				Date: Tuesday, March 25, 2014	Sheet 1 of 62

Model Name :

Intel Broadwell U / Haswell Block Diagram

Project Name :

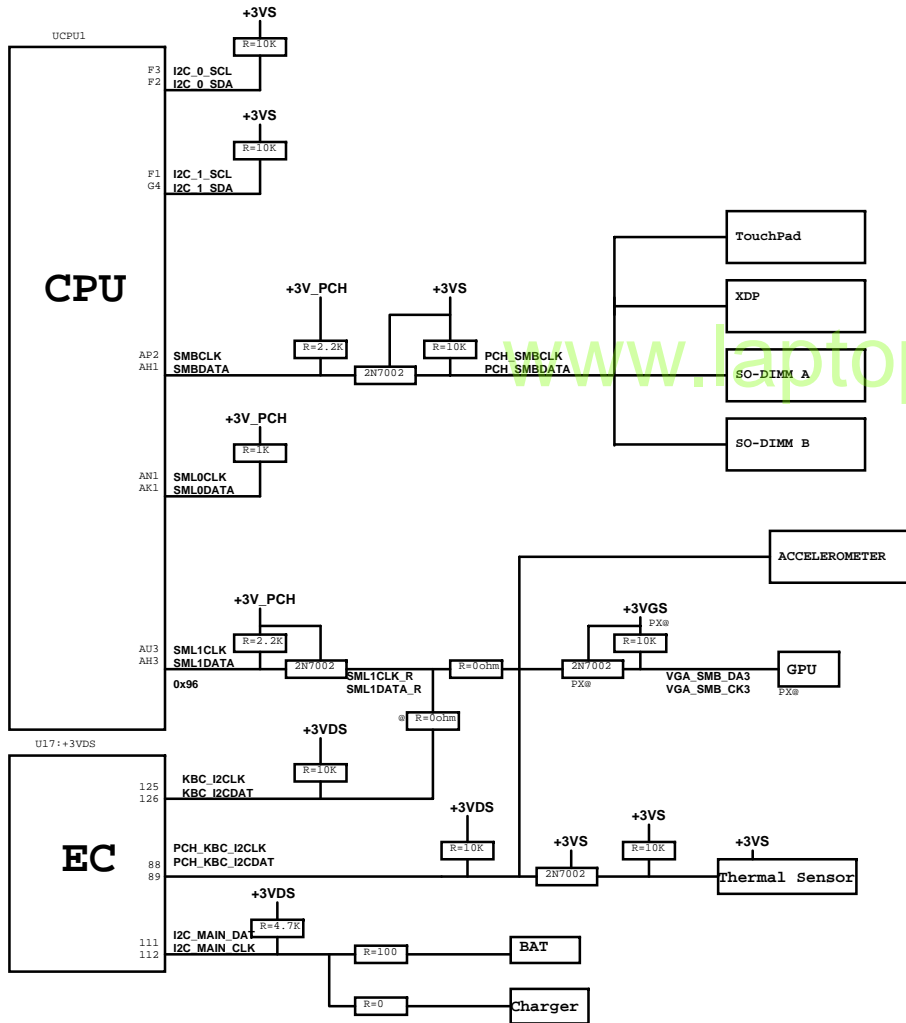


www.laptoprepairsecrets.com

CPU DC/DC	
TPS51622ARSMR	50~51
INPUTS	OUTPUTS
B+	VCC_VORE
SYSTEM DC/DC	
RT8243AZQW	47
INPUTS	OUTPUTS
B+	3VDS/5VDS
SYSTEM DC/DC	
RT8207MZQW	48
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS
SYSTEM DC/DC	
SY8206DQNC	49
INPUTS	OUTPUTS
B+	1.05VS
SYSTEM DC/DC	
SY8003DFC	52
INPUTS	OUTPUTS
B+	1.5VS
SYSTEM DC/DC	
RT8880BGQW	54~55
INPUTS	OUTPUTS
B+	+VGA_CORE
SYSTEM DC/DC	
SY8003DFC	56
INPUTS	OUTPUTS
B+	+1.8VS_VGA
SYSTEM DC/DC	
SY8003DFC	57
INPUTS	OUTPUTS
B+	+0.95VS_VGA

@ is NO SMT part (empty)
short@ : short pad , don't pop.
@EMI@, @ESD@, @RF@ : Reserve , don't pop.
RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel. WWAN@ : For WWAN function. PX@ : GPU BOM config.
eDP@ : Support eDP panel.



<USB2.0 port>

USB2.0 port	DESTINATION
0	CS
1	USB 2.0(Right side)
2	USB 2.0(Left side)
3	WLAN/BT
4	Finger Print
5	WWAN Touch (Option)
6	Camera
7	USB 2.0(Left side)

<PCI-E,SATA,USB3.0>

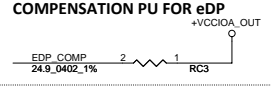
Lane#	PCI-E	SATA	USB3.0	DESTINATION
1			0	CS
2			1	USB3.0
3	1		2	WWAN (M.2)
4	2		3	Card reader(PCI-E)
5	3			10/100/1000 LAN
6	4			WLAN (M.2)
7				GPU(DIS only)
8				GPU(DIS only)
9				GPU(DIS only)
10				GPU(DIS only)
11	L3	3		2.5"HDD
12	L2	2		ODD
13	L1	1		
14	L0	0		SSD(NGFF)

CC97-CC102 must closed to connector not CPU

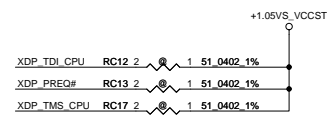
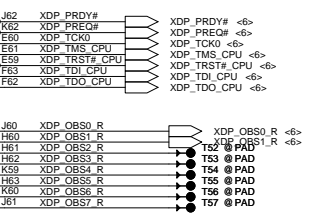
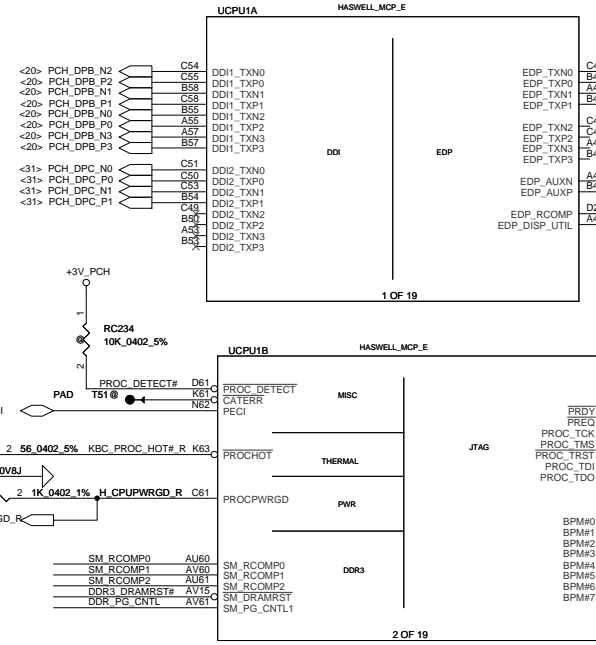
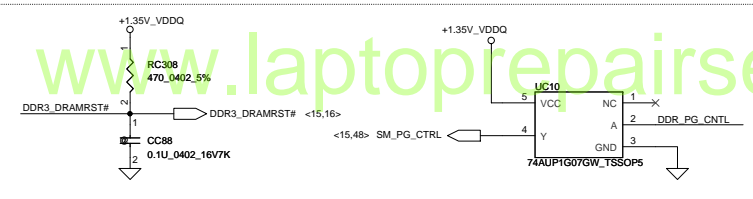
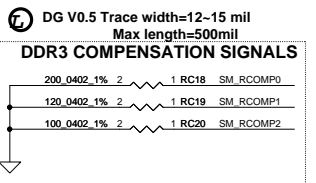
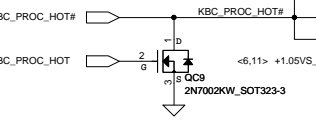
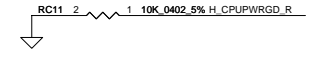
<HDMI>

<eDP>

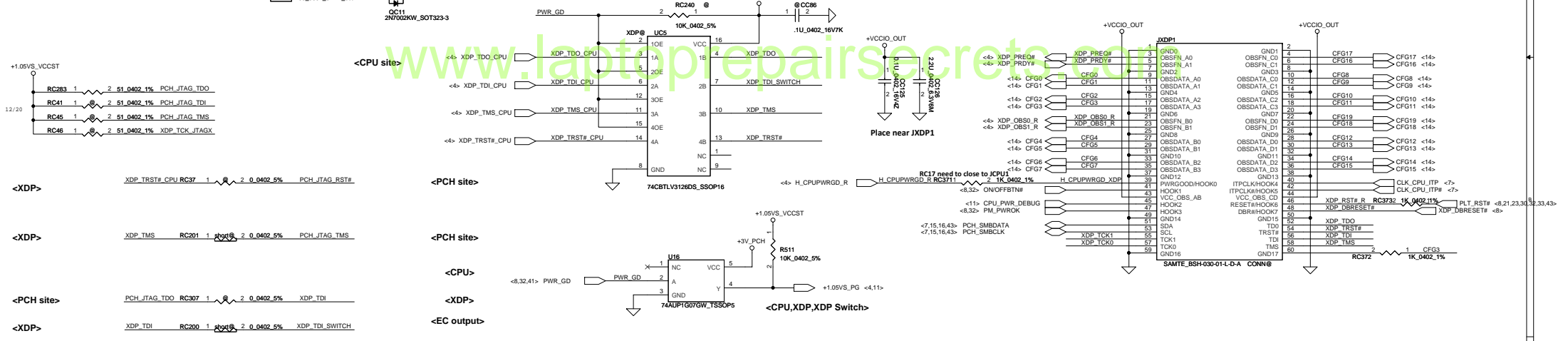
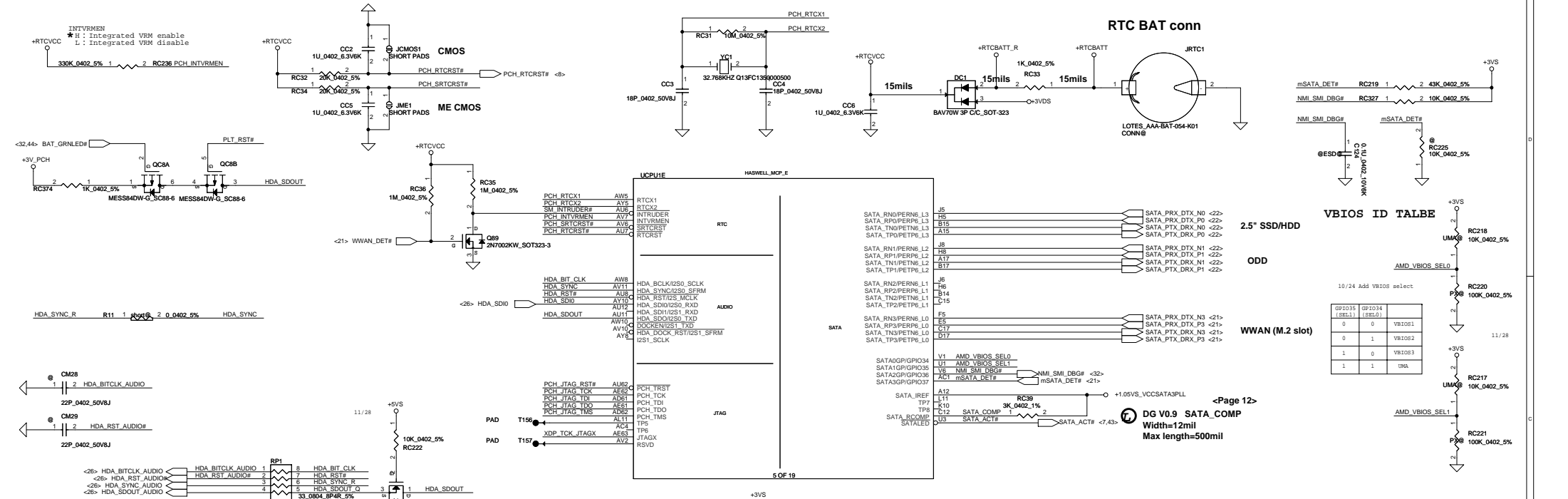
<eDP>



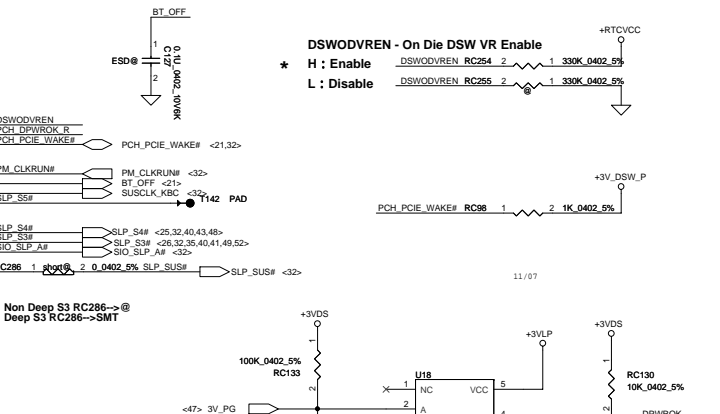
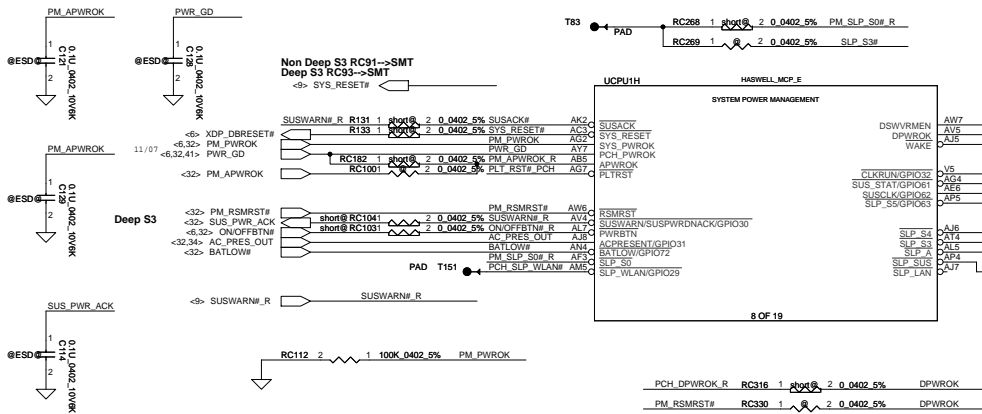
DG V0.9 PEG_COMP
 Trace width=20mil and spacing=25mil
 Max length=100mil



Security Classification	Compal Secret Data		Title
Issued Date	2011/06/29	Deciphered Date	2011/06/29
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Document Number LA-B181P Date: Tuesday, March 25, 2014
			Rev 0.5
			Sheet 4 of 62

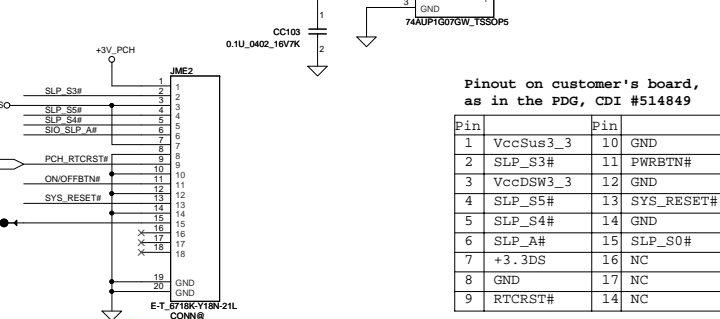


Topology	Description	Best Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other document)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6, R7,R8,R9
Single TCK scan chain (also known as "Common JTAG" in other document)	In this topology, PCH TDI-TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	- Boundary Scan/ - Manufacturing test	J1s, J2s, J3s** R2, R4, R5, R5s**	R1d, R3d, J1d, J2d J3d**, J4d, R6, R7, R8, R9



Intel ME-EC Interaction Signal List with and without M3 support

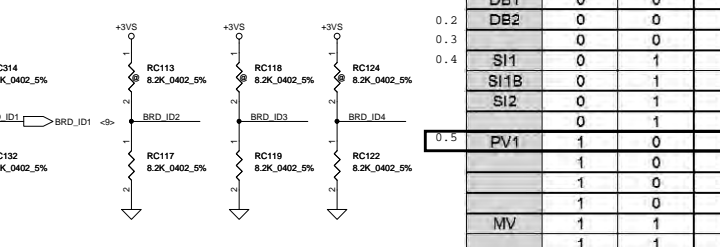
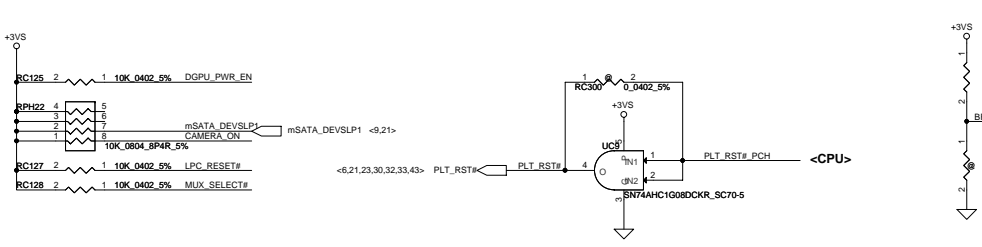
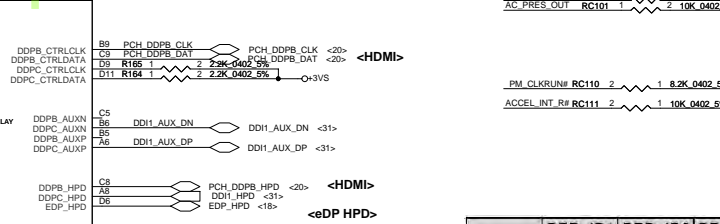
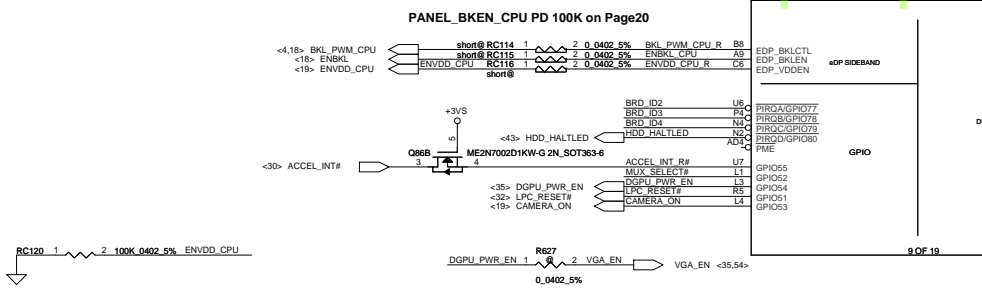
Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSWRDNACK (GPIO39)	Required	Required
ACPRESENT (GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from FCH to EC, then SLP_A# becomes required from Intel ME-EC perspective.



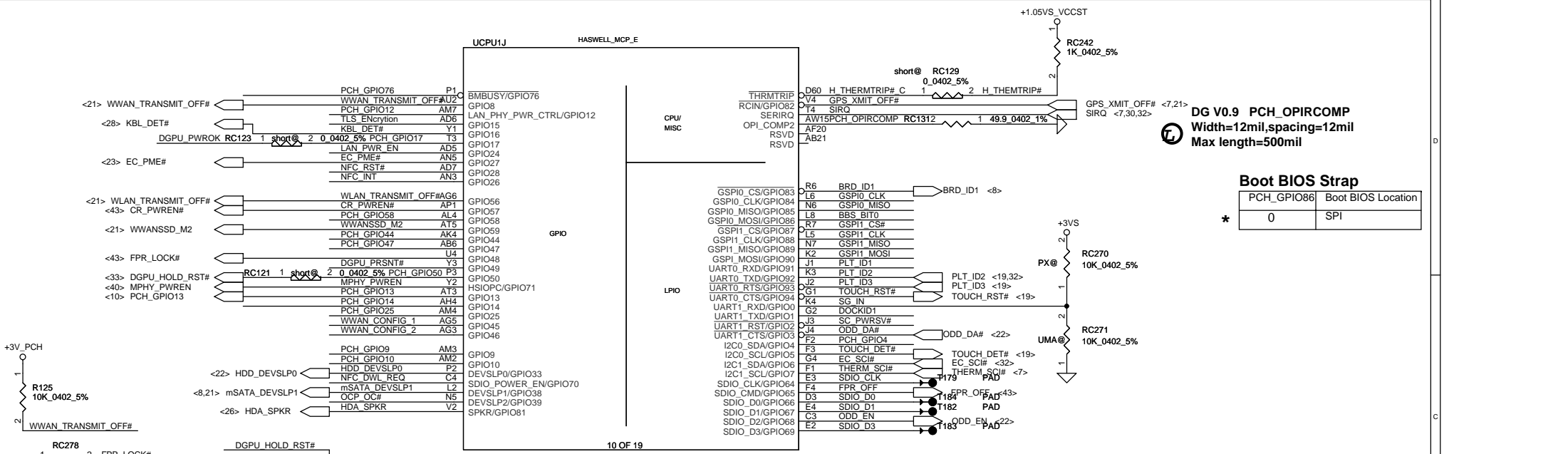
Pinout on customer's board, as in the PDG, CDI #514849

Pin	Pin
1	VccSus_3_3
2	SLP_S3#
3	VccDSW3_3
4	SLP_S5#
5	SLP_S4#
6	SLP_A#
7	+3.3DS
8	GND
9	RTORST#
10	GND
11	PWRBTN#
12	GND
13	SYS_RESET#
14	GND
15	SLP_S0#
16	NC
17	NC
18	NC

www.laptoprepairsecrets.com



Board	BRD ID1	BRD ID2	BRD ID3	BRD ID4
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
S10	0	0	1	1
S1B	0	1	0	1
S12	0	1	1	0
PV1	1	0	0	0
MV	1	1	0	0
	1	0	1	0
	1	0	1	1
	1	1	1	0
	1	1	1	1



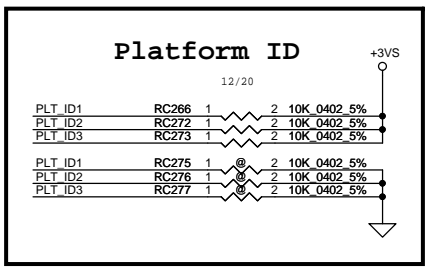
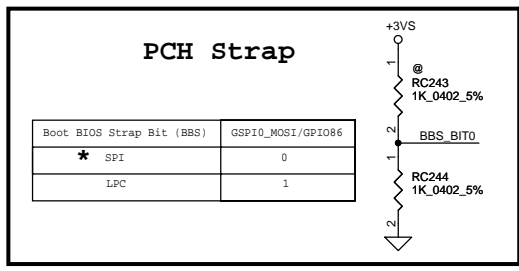
DG V0.9 PCH_OPIRCOMP
 Width=12mil,spacing=12mil
 Max length=500mil

Boot BIOS Strap

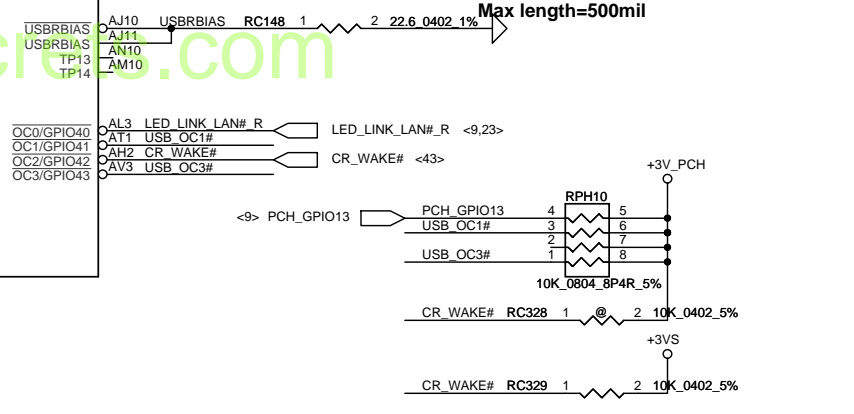
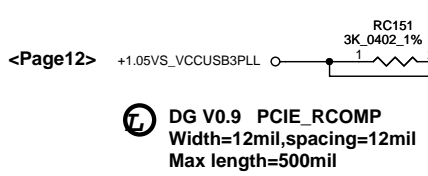
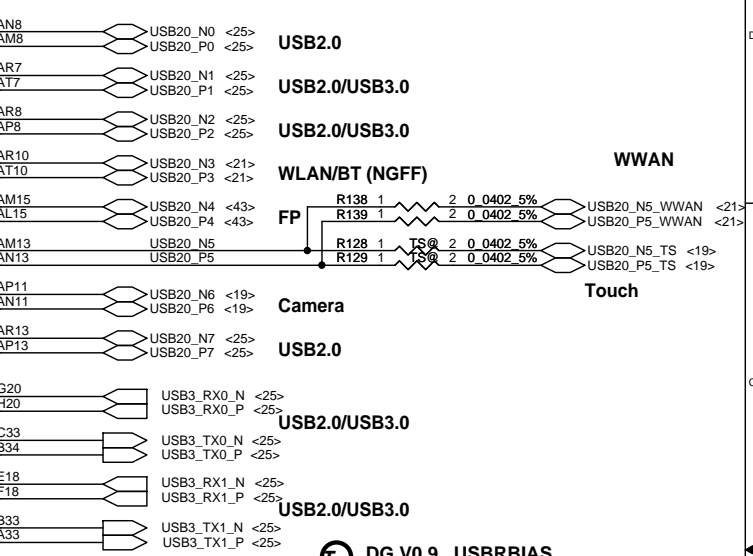
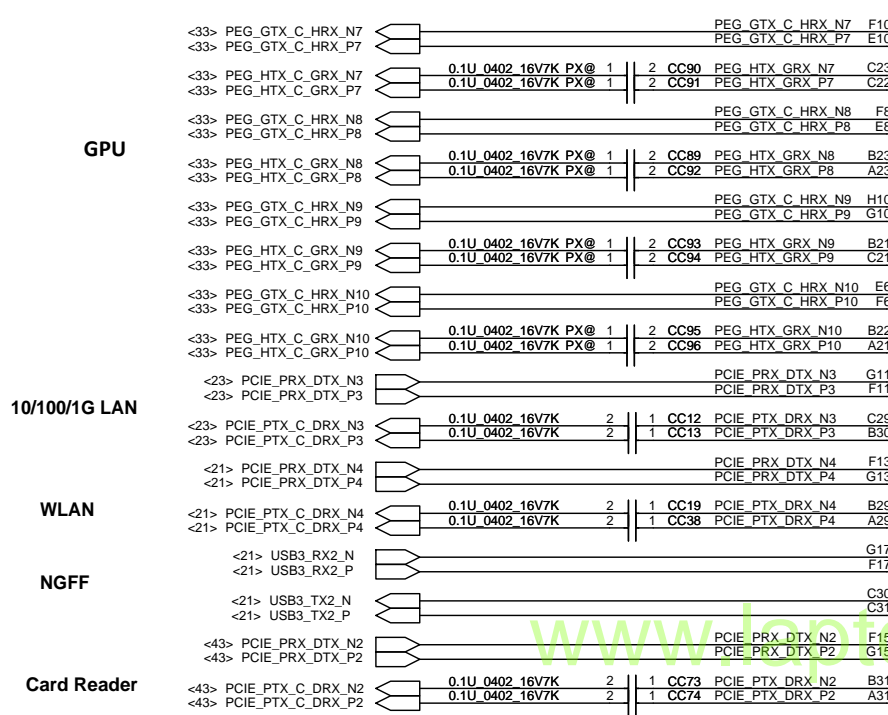
PCH_GPIO86	Boot BIOS Location
0	SPI

www.laptoprepairscrets.com

TOUCH_RST#	RC274	1	2	10K 0402 5%
DOCKID1	RC284	1	2	10K 0402 5%
SC_PWRSV#	RC287	1	2	10K 0402 5%
ODD_DA#	RC289	1	2	10K 0402 5%
PCH_GPIO4	RC290	1	2	10K 0402 5%
TOUCH_DET#	RC291	1	2	10K 0402 5%
EC_SCI#	RC292	1	2	10K 0402 5%
SDIO_CLK	RC293	1	2	10K 0402 5%
FPR_OFF	RC305	1	2	10K 0402 5%
SDIO D1	RC308	1	2	10K 0402 5%
SDIO D3	RC312	1	2	10K 0402 5%
PCH_GPIO7E	RC315	1	2	10K 0402 5%
GSPI0_CLK	RC317	1	2	10K 0402 5%
GSPI0_MISO	RC318	1	2	10K 0402 5%
GSPI1_CLK	RC319	1	2	10K 0402 5%
GSPI1_MISO	RC320	1	2	10K 0402 5%
GSPI1_MOSI	RC321	1	2	10K 0402 5%



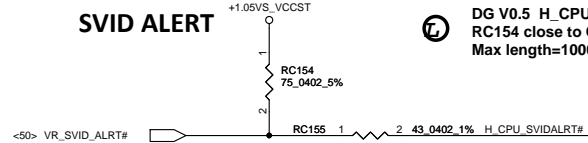
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	GPIO, UART, I2C	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-B181P
Date:	Tuesday, March 25, 2014	Sheet	9	of	62
				Rev	0.5



Security Classification	Compal Secret Data			Title	PCIE, USB
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Document Number	LA-B181P
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 0.5
Date:	Tuesday, March 25, 2014	Sheet	10	of	62

+VCC_CORE@1000mA

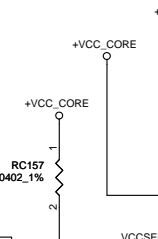
SVID ALERT



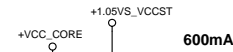
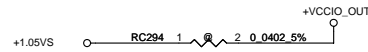
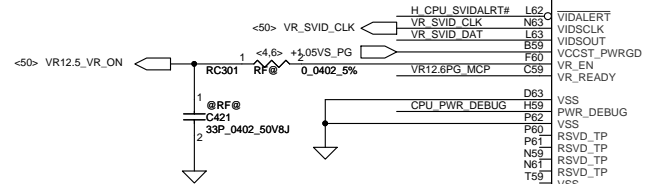
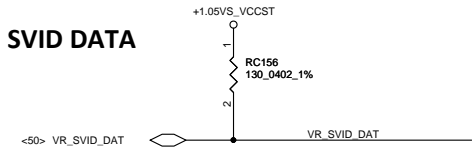
DG V0.5 H_CPU_SVIDALRT#
 RC154 close to CPU-300mil
 Max length=1000-2000mil

VCC_SENSE

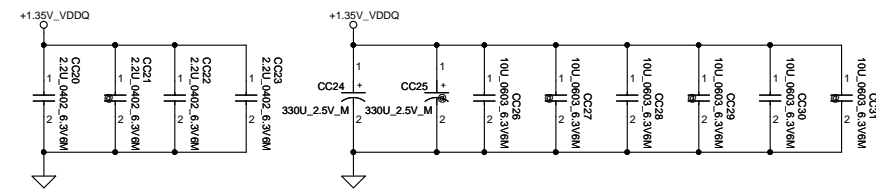
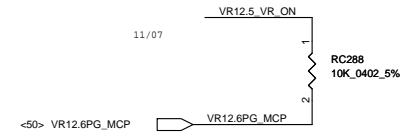
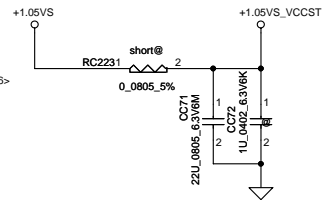
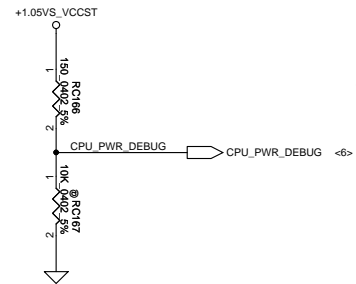
<50> VCCSENSE



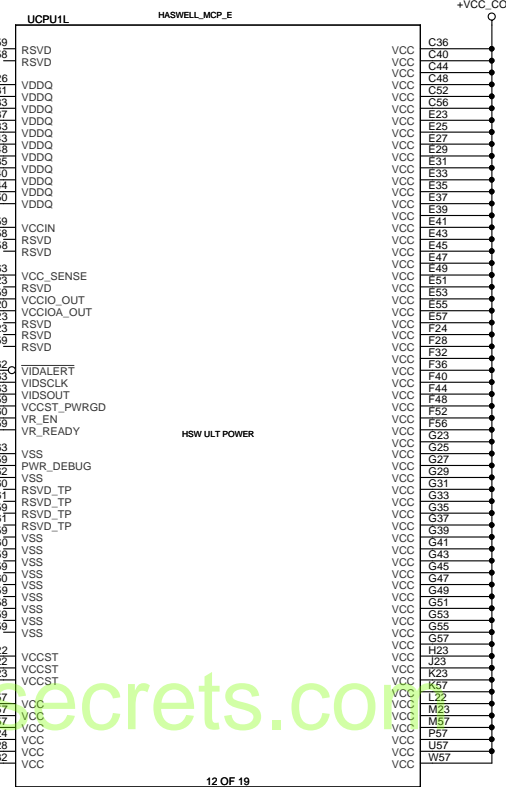
SVID DATA



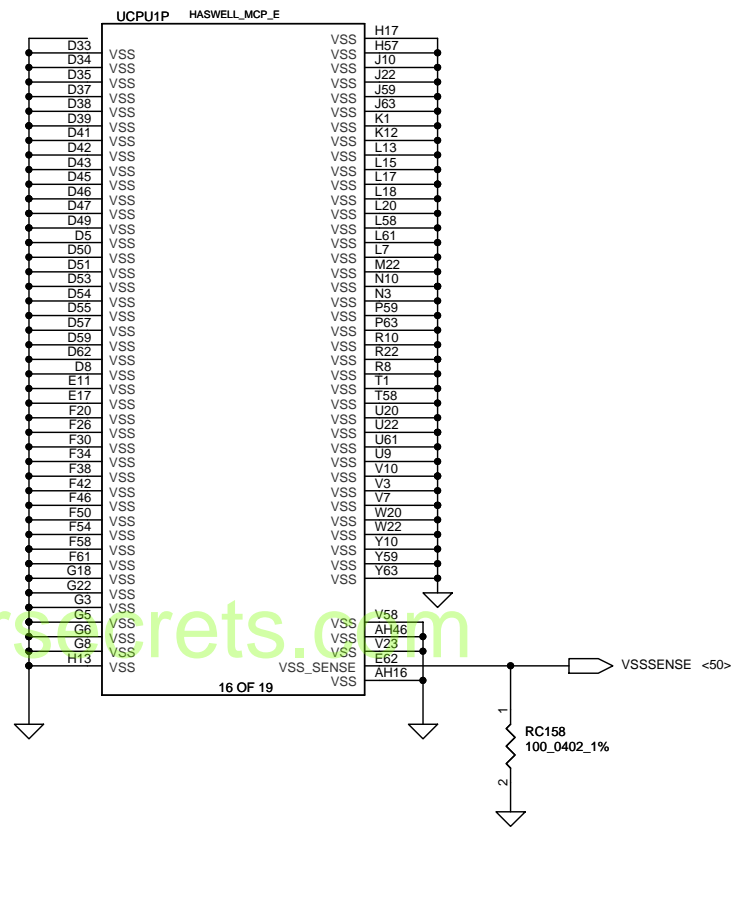
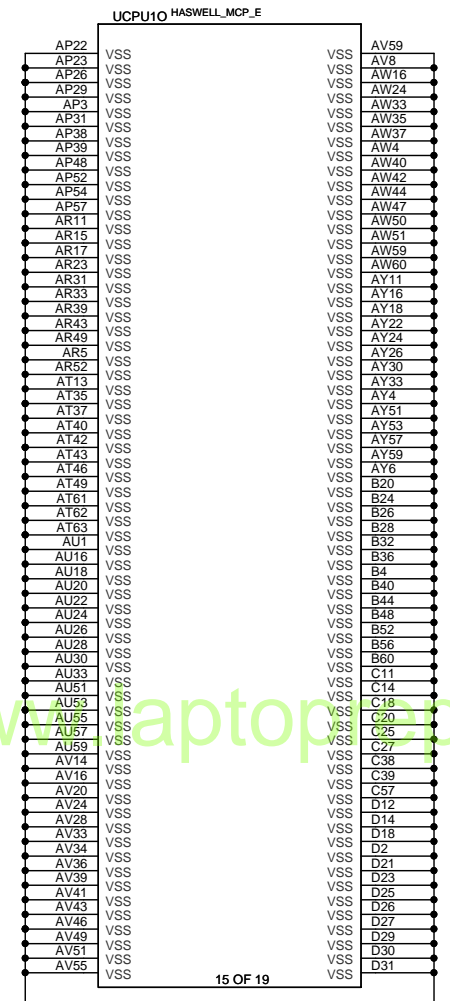
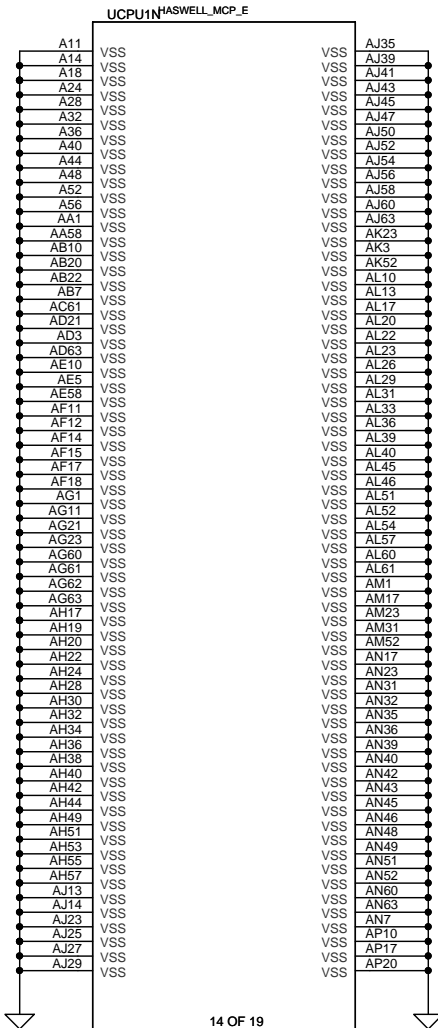
DG V0.5 VIDSOUT
 RC156 close to CPU-500mil
 Max length=1000-2000mil





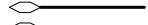

www.laptoprepairsecrets.com

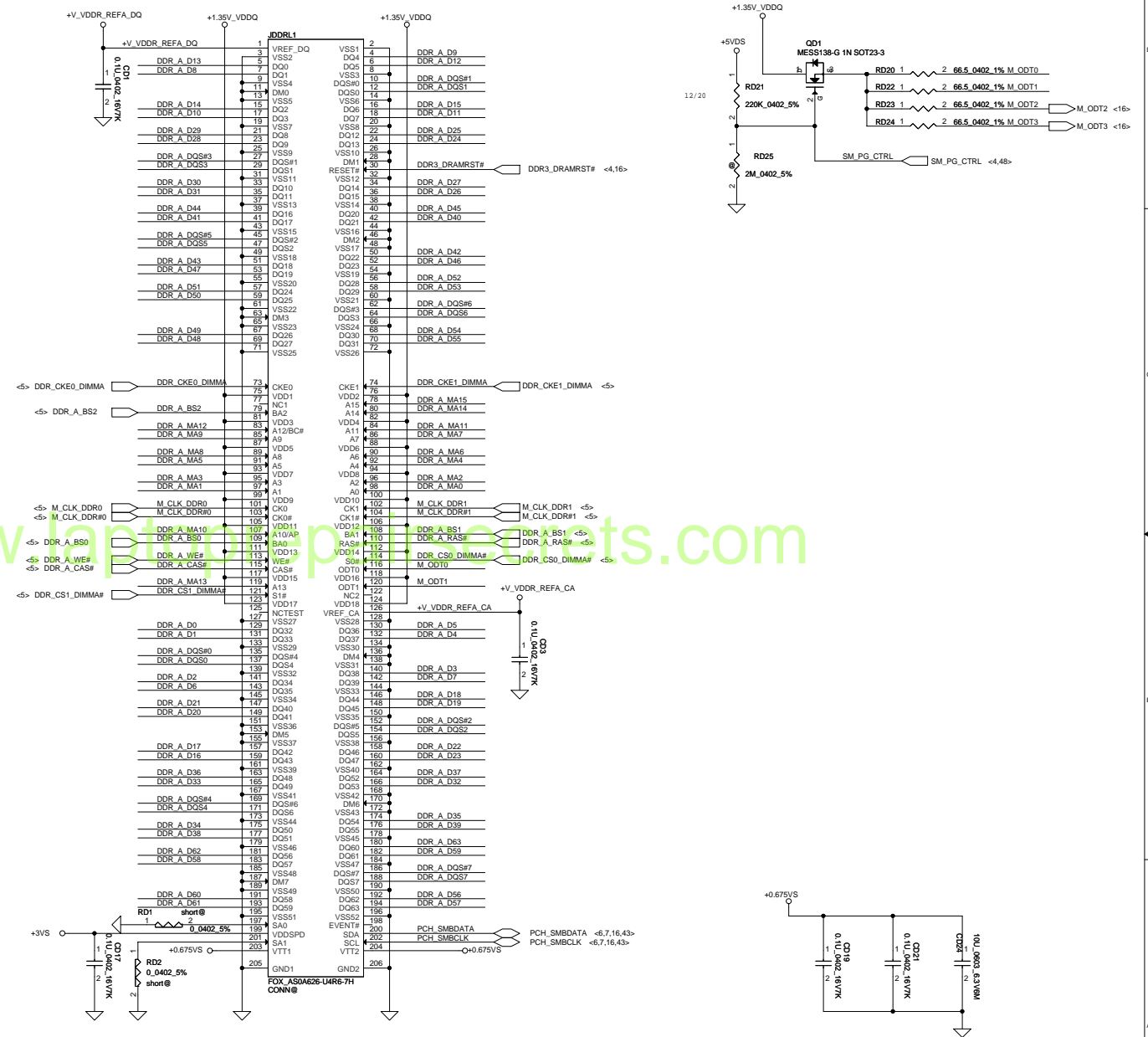


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Power
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	LA-B181P
				Date	Tuesday, March 25, 2014
				Sheet	11 of 62
				Rev	0.5



Security Classification	Compal Secret Data			Compal Electronics, Inc. Title: GND/VSSSEN	
Issued Date	2010/05/27	Deciphered Date	2011/05/11		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LA-B181P	Rev 0.5
				Date:	Tuesday, March 25, 2014

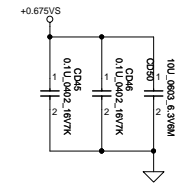
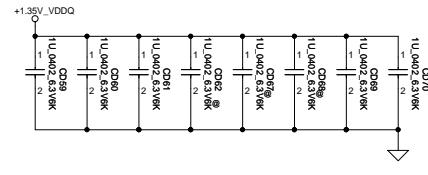
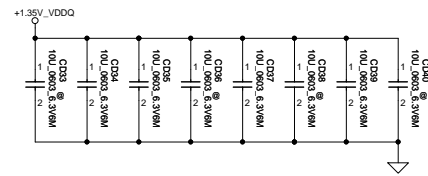
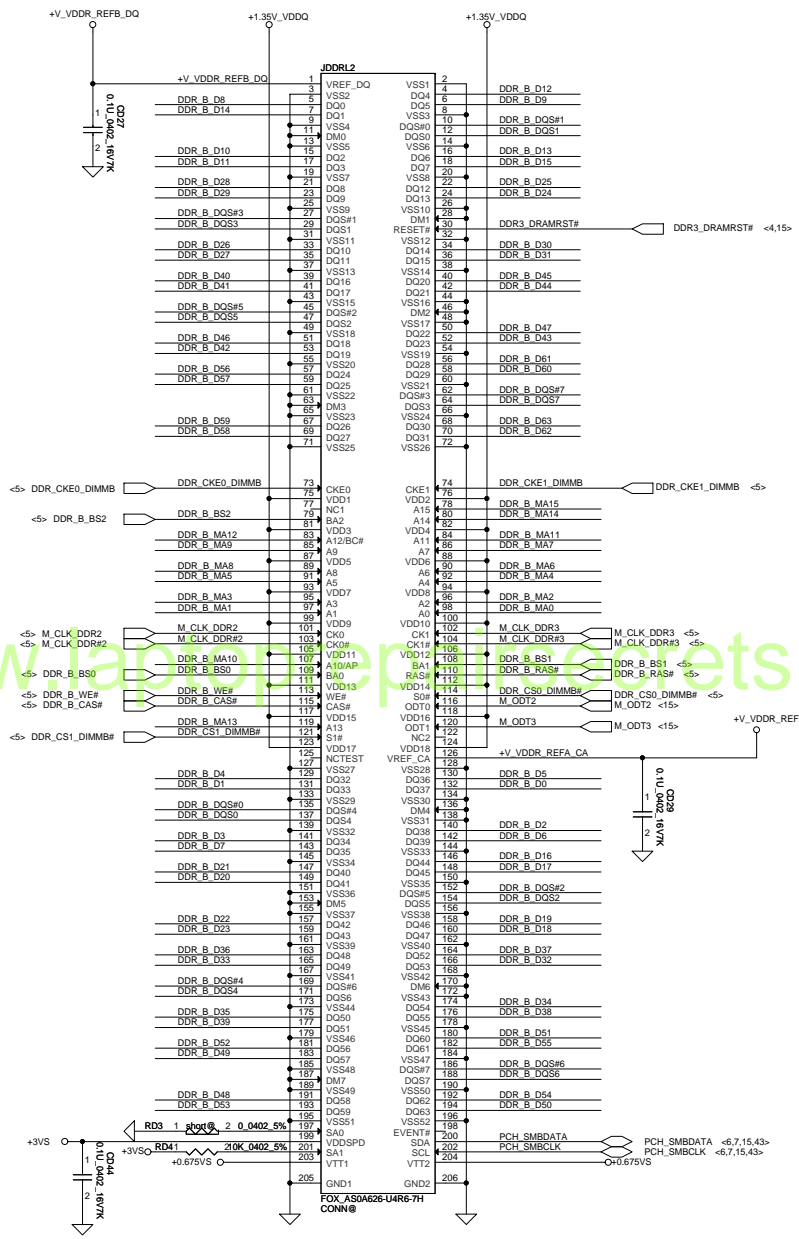
<S> DDR_A_D[0..63] 
 <S> DDR_A_DQS[0..7] 
 <S> DDR_A_DQS# [0..7] 
 <S> DDR_A_MA[0..15] 



www.laptopsparts.com

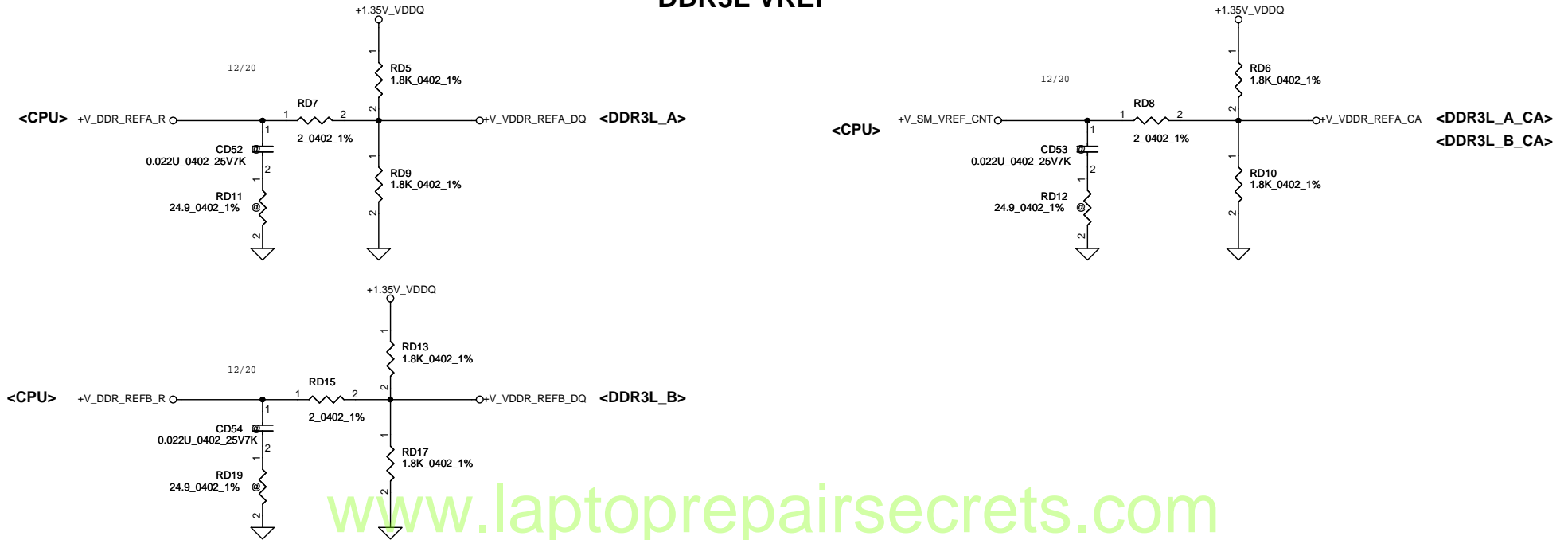
Security Classification	Compal Secret Data		Title
Issued Date	2011/06/29	Deciphered Date	2011/06/29
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Document Number LA-B181P Date: Tuesday, March 25, 2014
Sheet 15 of 62			Rev 0.5

- <-> DDR_B_D[0..63]
- <-> DDR_B_DQS[0..7]
- <-> DDR_B_DQS#[0..7]
- <-> DDR_B_MA[0..15]



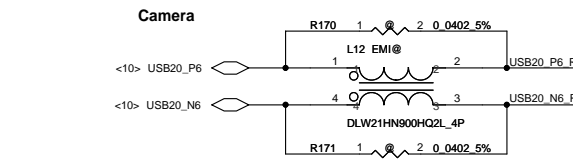
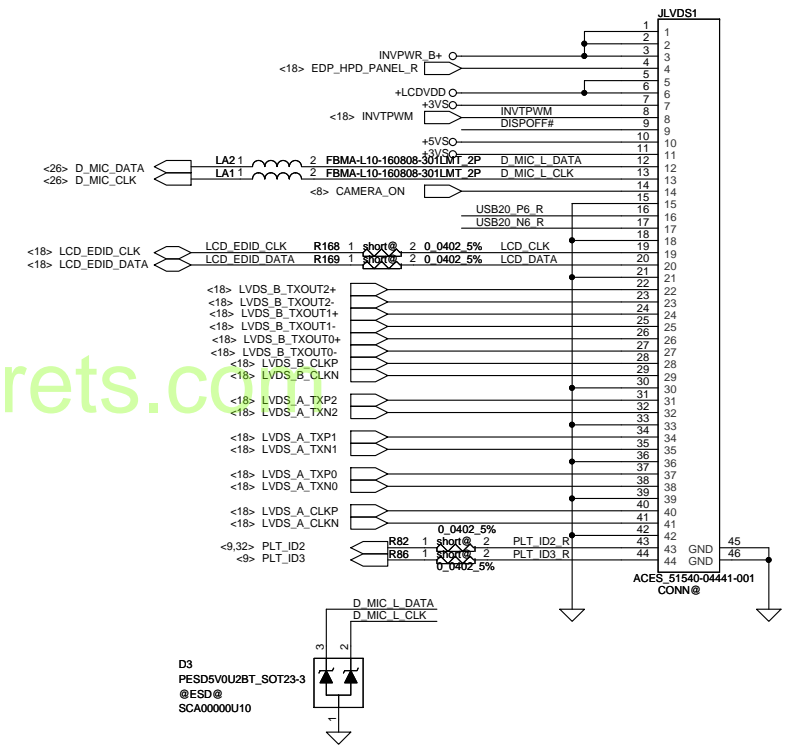
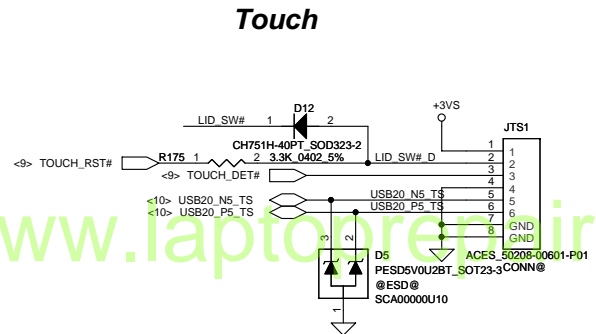
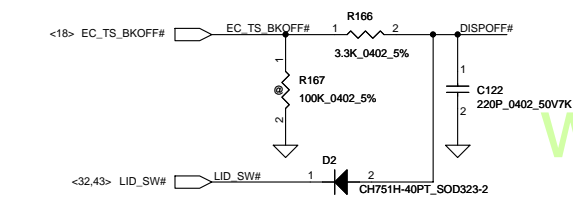
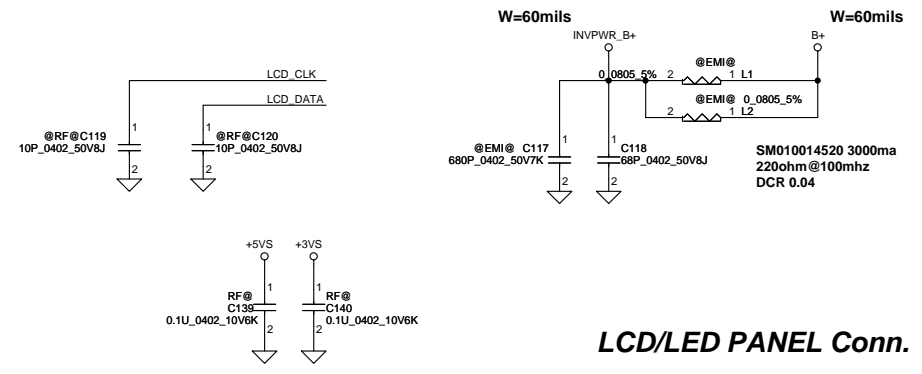
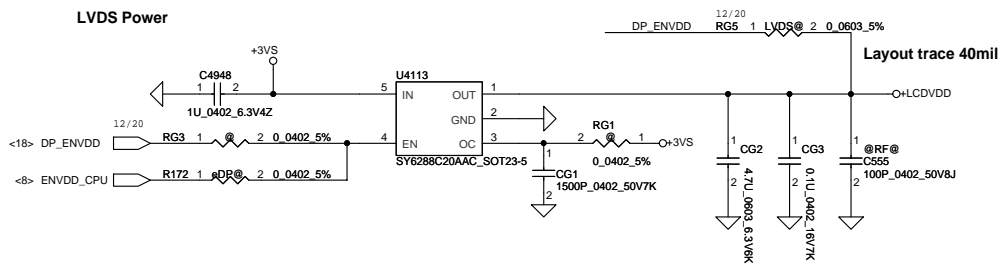
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/05/27	Deciphered Date	2011/05/11	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				LA-B181P
				Rev 0.5
				Date: Tuesday, March 25, 2014
				Sheet 16 of 62

DDR3L VREF



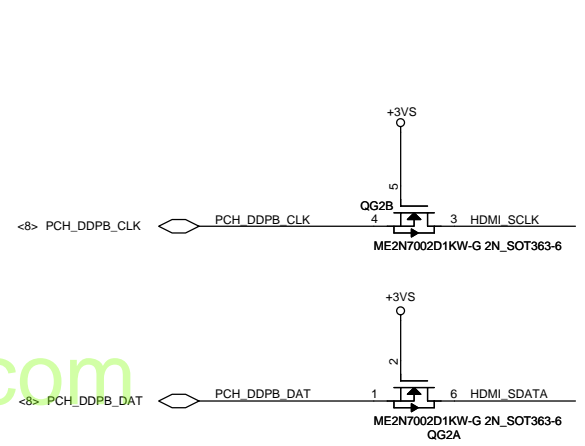
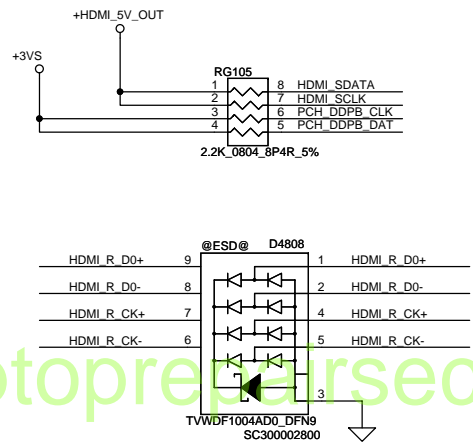
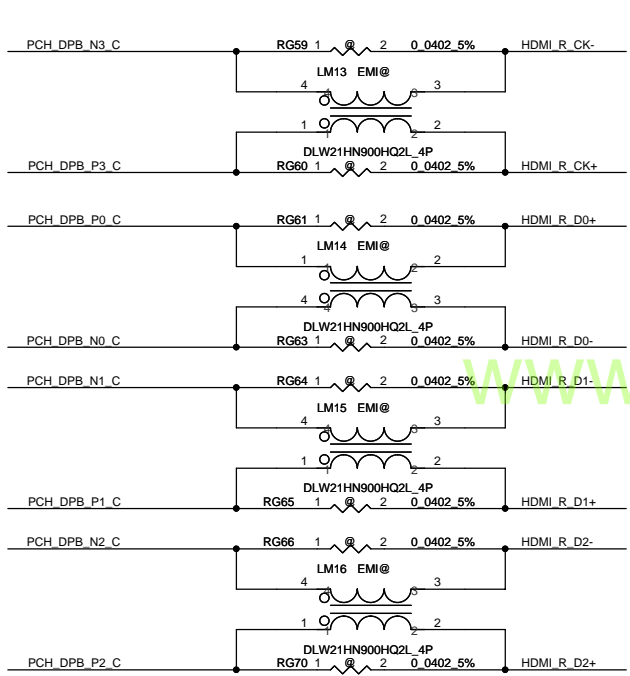
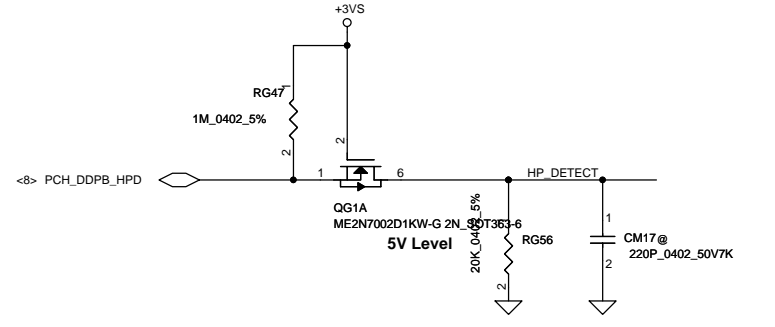
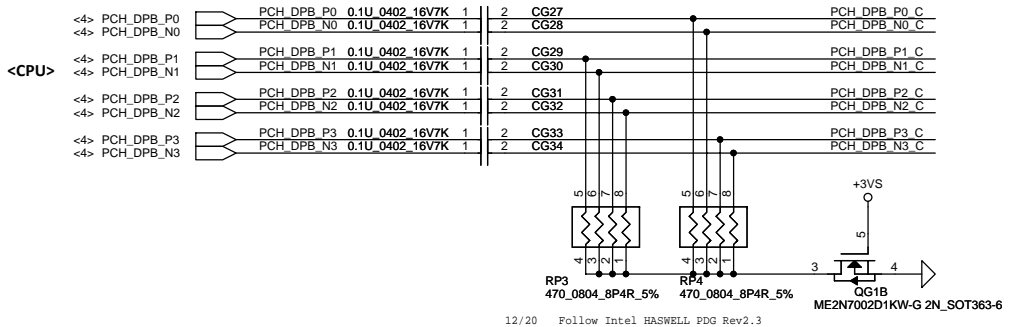
www.laptoprepairsecrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	DDR3L VREF
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B181P
				Date:	Tuesday, March 25, 2014

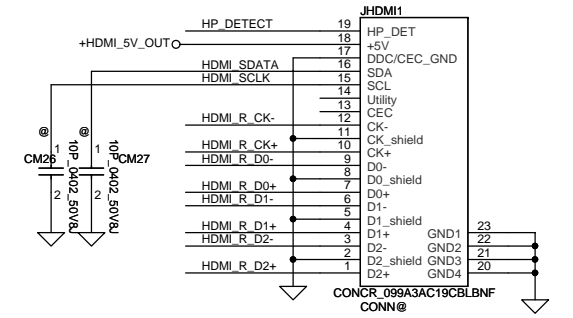
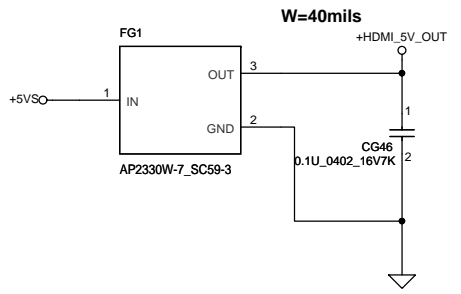
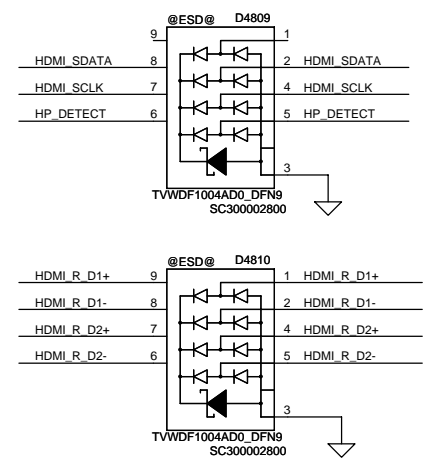


	GPIO92 PLT_ID2	GPIO93 PLT_ID3
Rolo 14"	0	1
Reeses 15"	1	0
Raisinnet 17"	1	1

Security Classification	Compal Secret Data		Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev
				LA-B181P
Date: Tuesday, March 25, 2014				Sheet 19 of 62

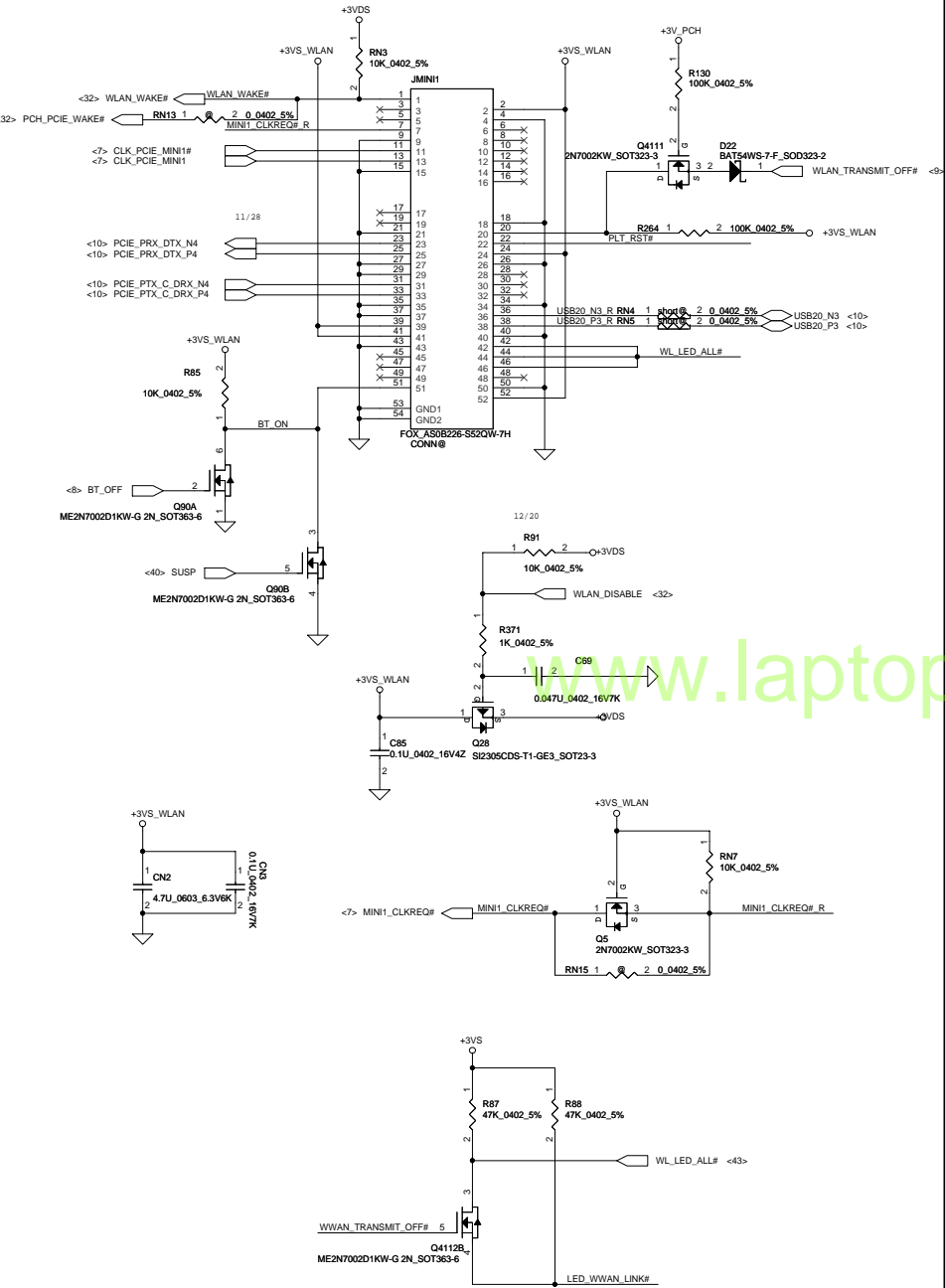


5V PULL UP IN CONNECTER SIDE

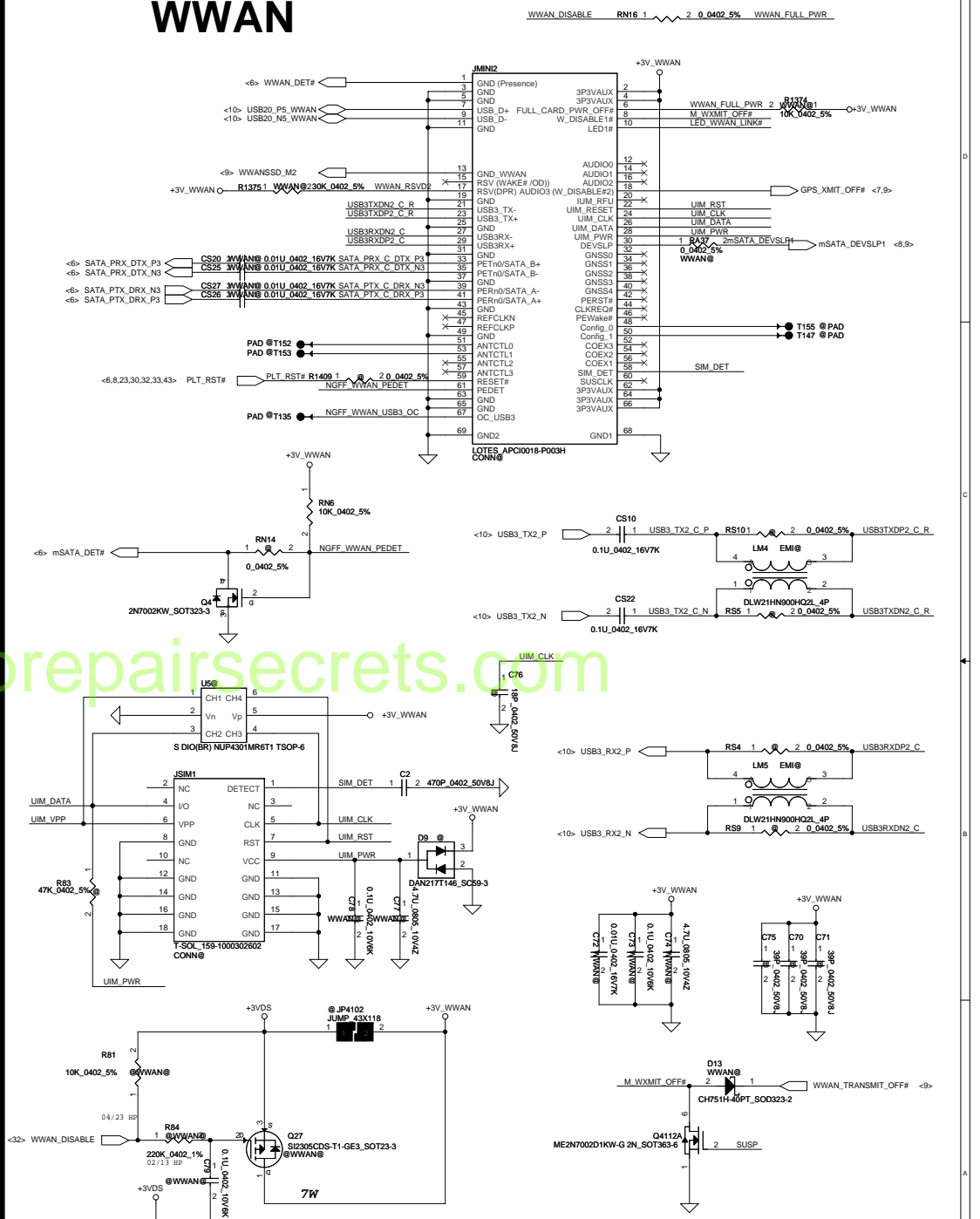


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	HDMI Conn/Level shift	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-B181P	Rev 0.5
Date: Tuesday, March 25, 2014		Sheet 20 of 62			

WLAN



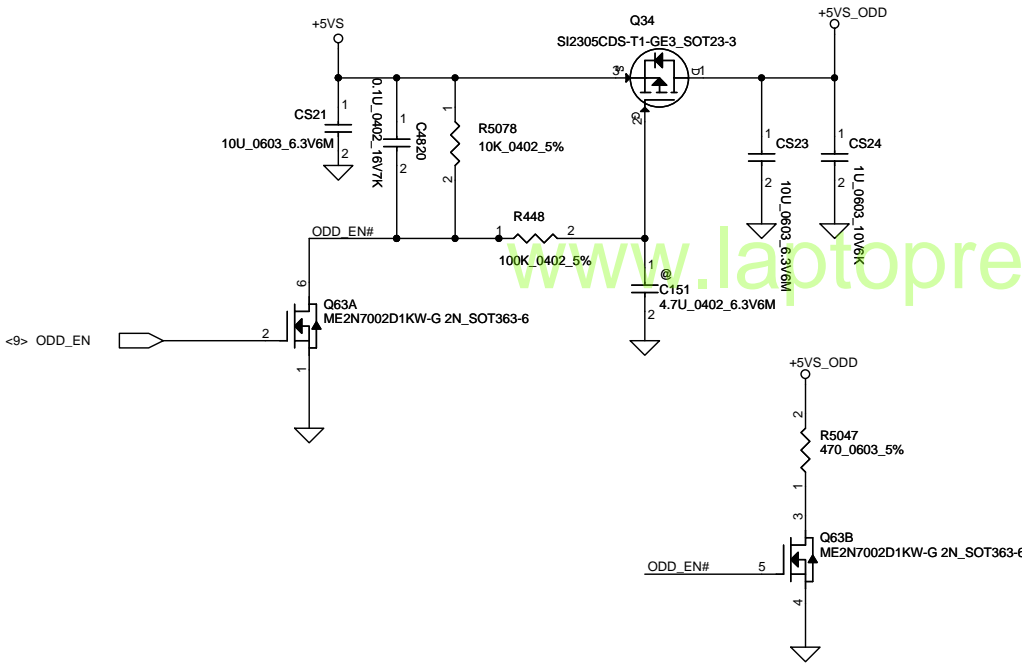
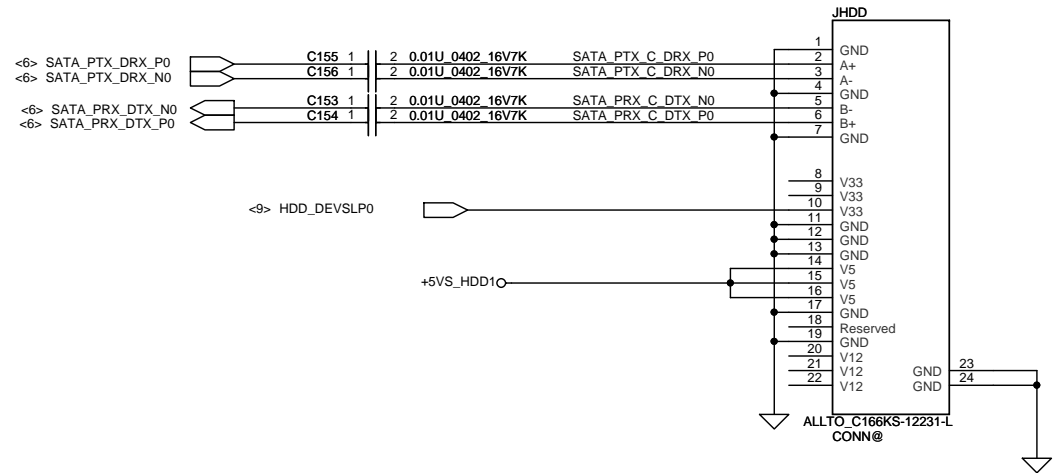
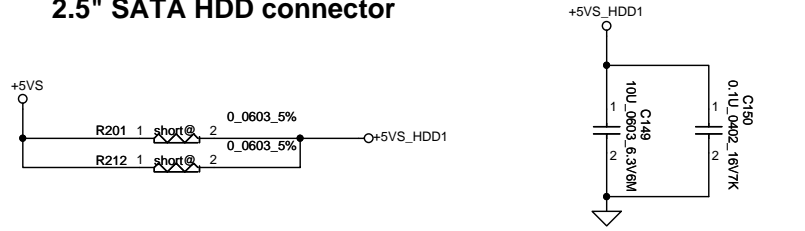
WWAN



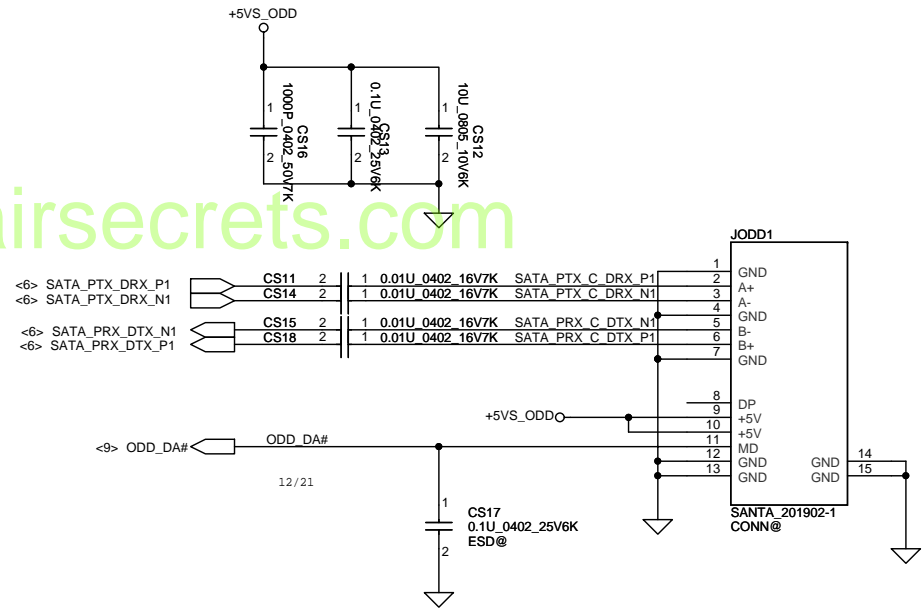
www.laptoprepairsecrets.com

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Size	WLAN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Document Number	LA-B181P	Rev 0.5
			Date:	Tuesday, March 25, 2014	ISheet 21 of 62

2.5" SATA HDD connector

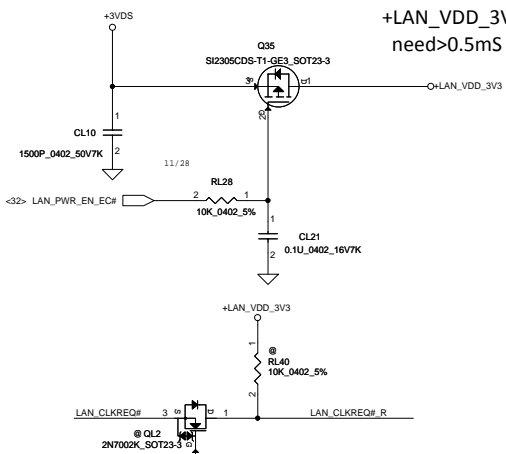


Place near ODD Connector

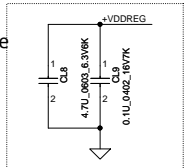


12/20 Customer change GPIO table

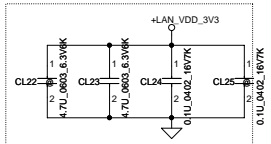
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B181P	0.5
Date: Tuesday, March 25, 2014				Sheet	22 of 62



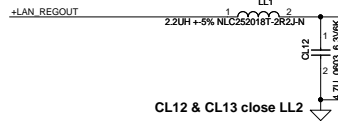
+LAN_VDD_3V3 Rising time
need>0.5ms and <100ms



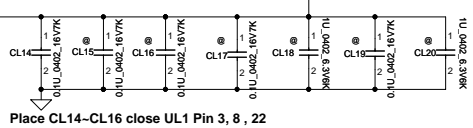
CL8 & CL9 close to UL1: Pin 23



CL22 & CL23 close to UL1: Pin 11,32
CL24 close to UL1: Pin 32
CL25 close to UL1: Pin 11

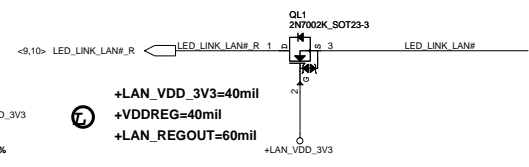


CL12 & CL13 close LL2

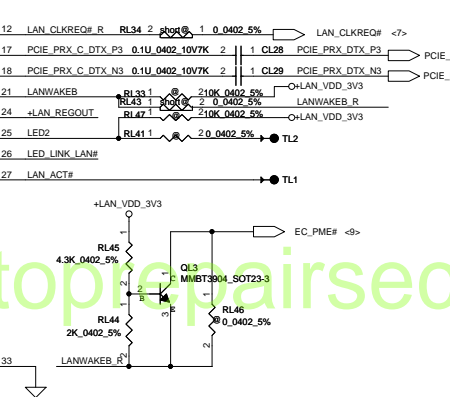
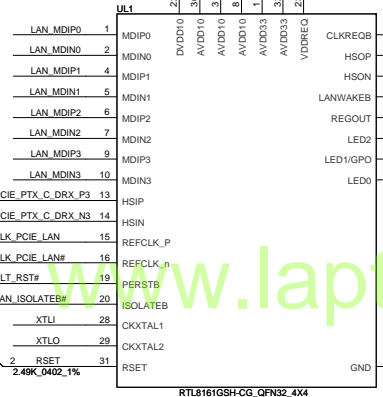
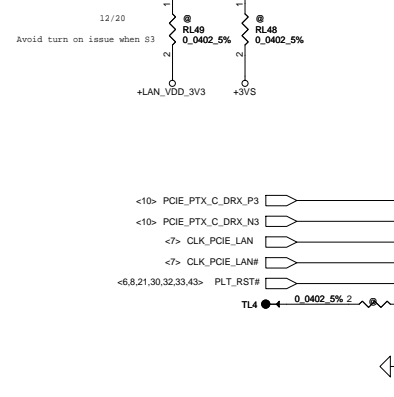
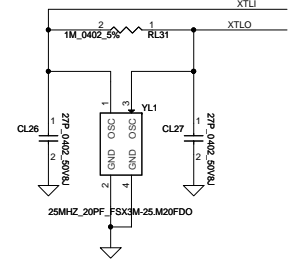


Place CL14-CL16 close UL1 Pin 3, 8, 22

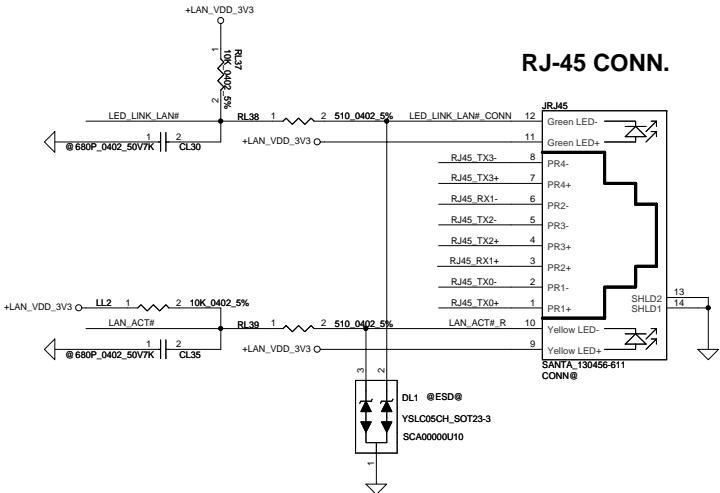
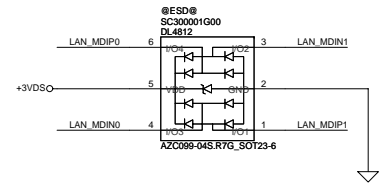
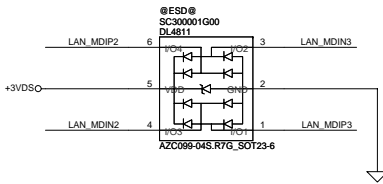
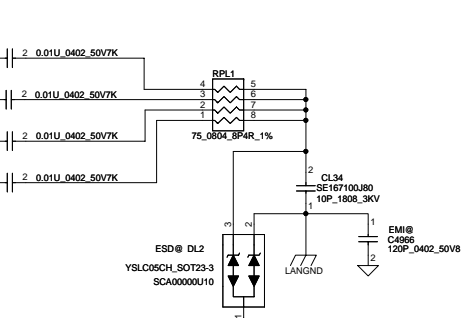
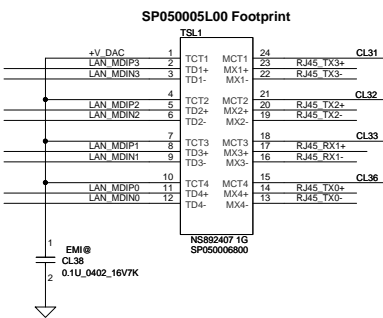
CL17 & CL18 close UL1 Pin22
CL19 & CL20 close UL1 Pin30



+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



www.laptoprepairsecrets.com



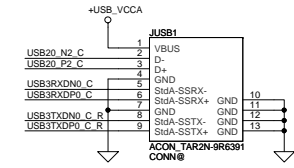
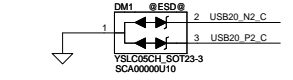
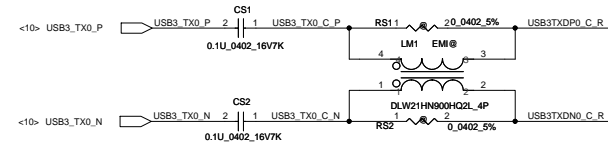
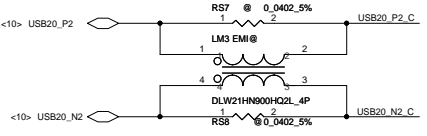
RJ-45 CONN.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2011/06/29
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title LAN RTL8161GSH Document Number LA-B181P Date: Tuesday, March 25, 2014 Sheet 23 of 62

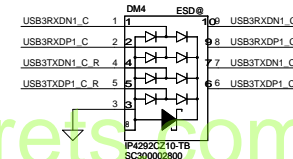
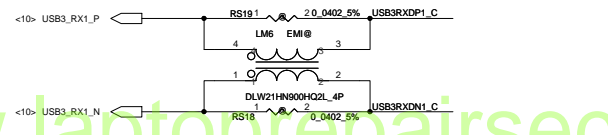
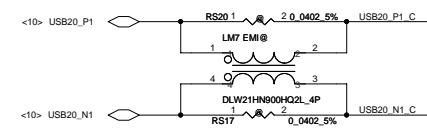
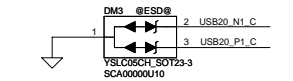
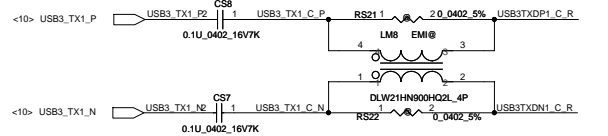
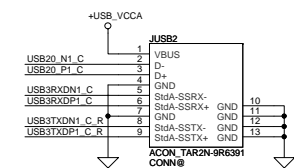
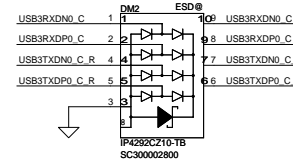
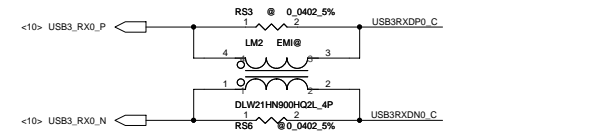
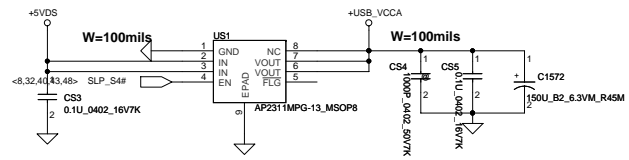
www.laptoprepairsecrets.com

Security Classification	Compal Secret Data			Title
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Card Reader RTS5237
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-B181P
Date: Tuesday, March 25, 2014			Sheet 24 of 62	Rev 0.5

USB3.0

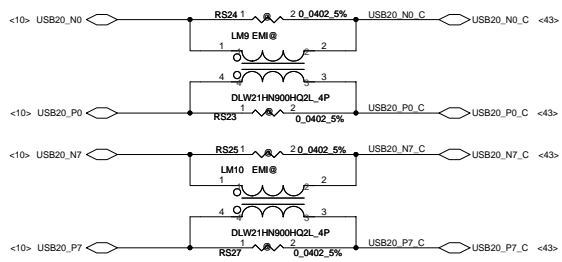


USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

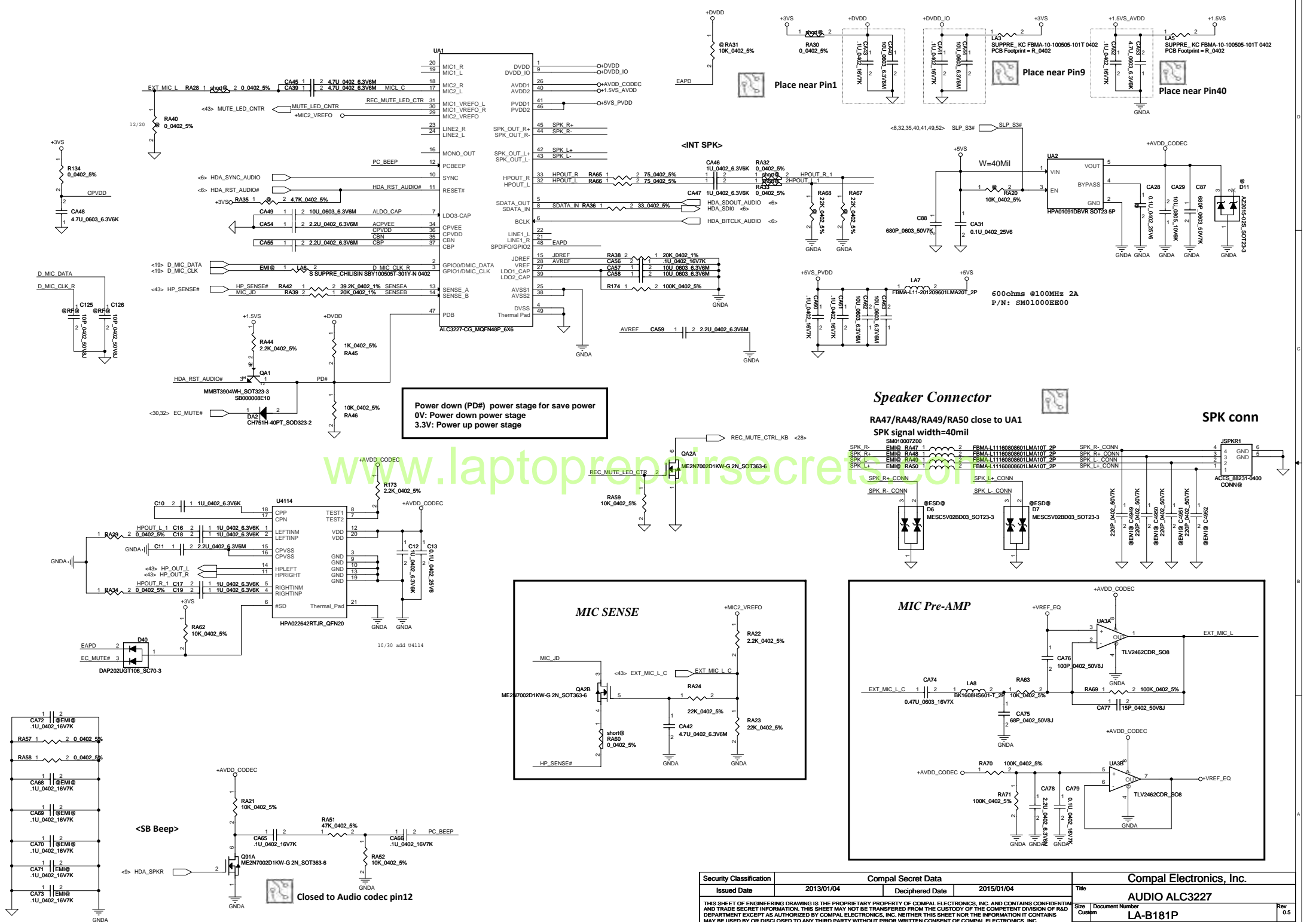


www.laptoprepairsecrets.com

USB2.0



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB 3.0 Document Number LA-B181P Date: Tuesday, March 25, 2014 Sheet 25 of 62
Rev	0.5			



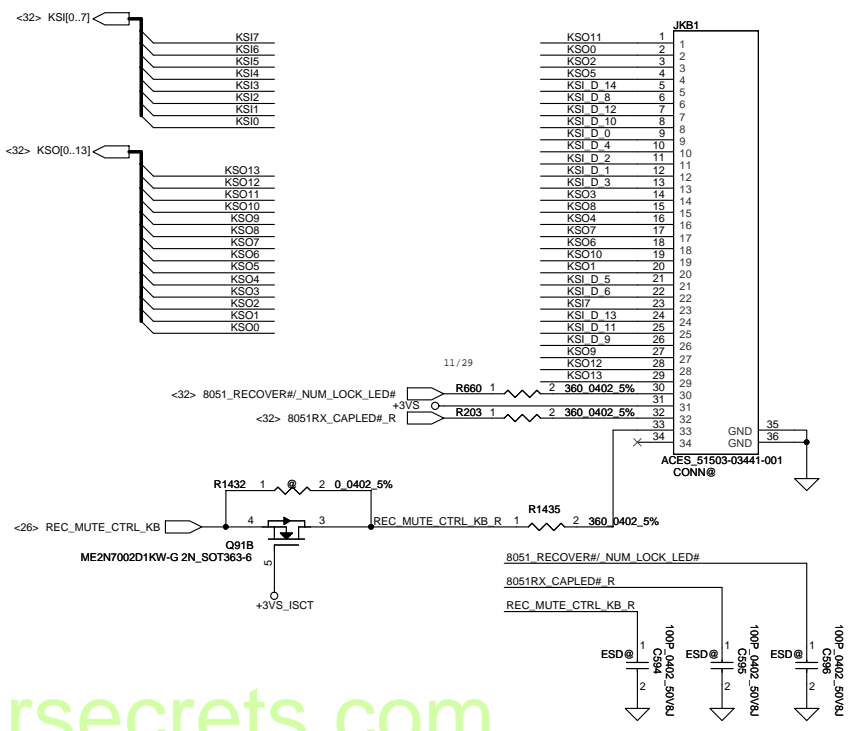
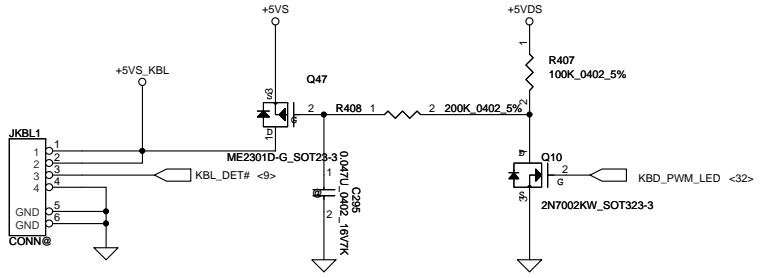
Security Classification	Compal Secret Data		Title	
Issued Date	2013/01/04	Deciphered Date	2015/01/04	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Document Number			Rev	
LA-B181P			0.5	
Date:	Tuesday, March 25, 2014	Sheet	26 of 82	

www.laptoprepairsecrets.com

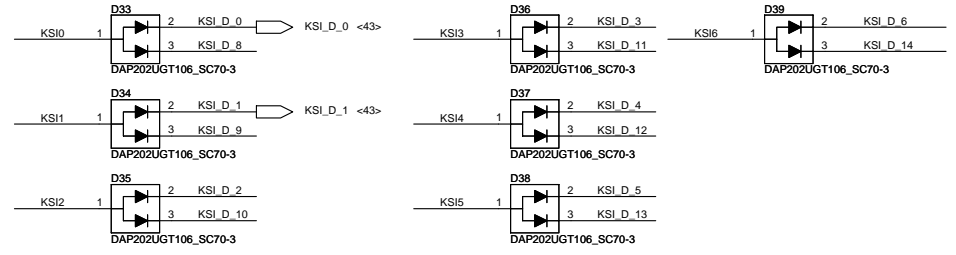
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/03/23	Deciphered Date	2012/10/21	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Audio SPK Conn/Jack/MIC
Size	Document Number	Rev		
C	LA-B181P	0.5		
Date:	Tuesday, March 25, 2014	Sheet	27	of 62

Keyboard conn

KB backlight Conn

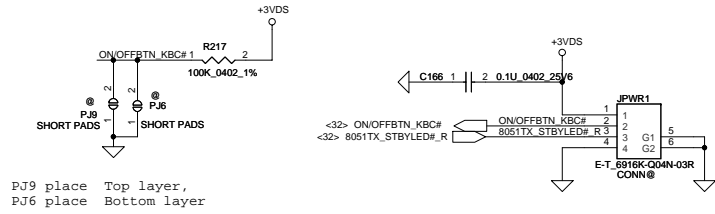


www.laptoprepairsecrets.com

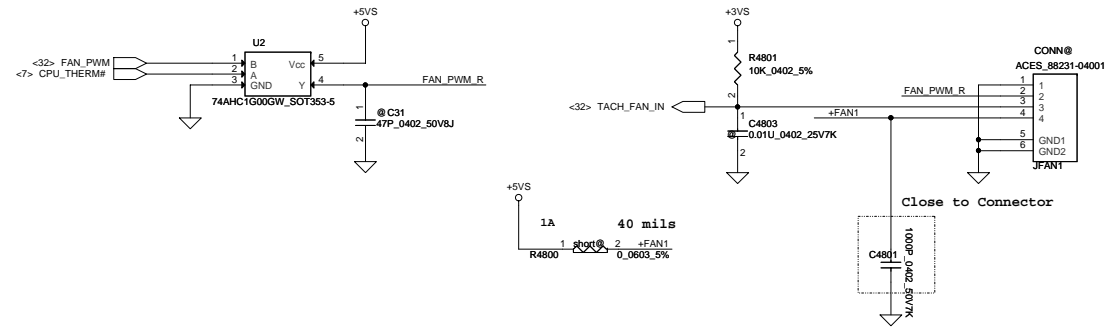


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	KB/TP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B181P	
				Date	Tuesday, March 25, 2014	Rev
				Sheet	28	of 62

Power Button Connector

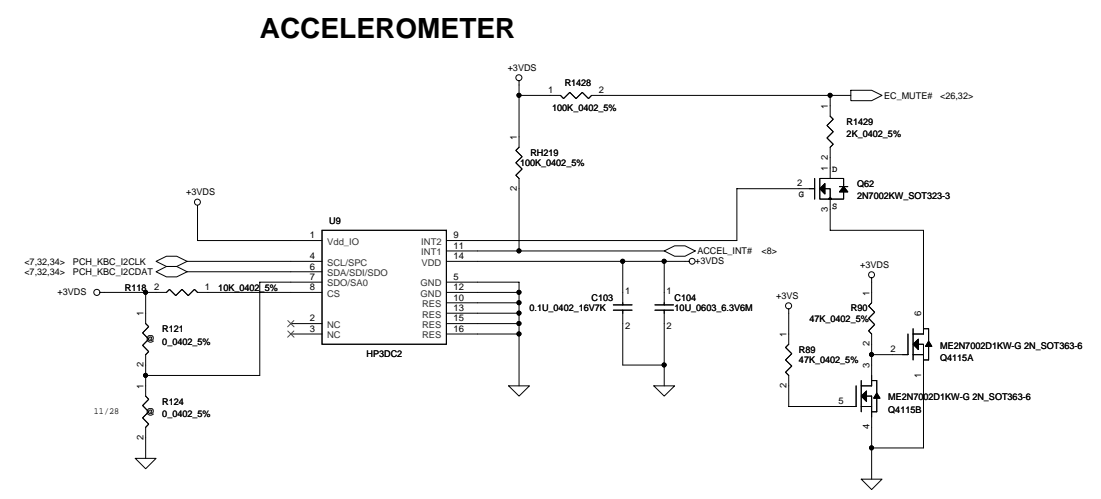
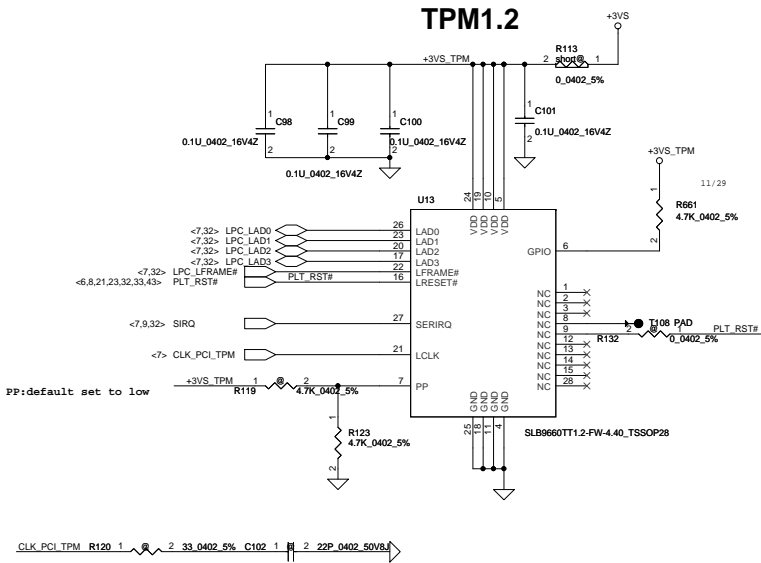


Fan Control Circuit

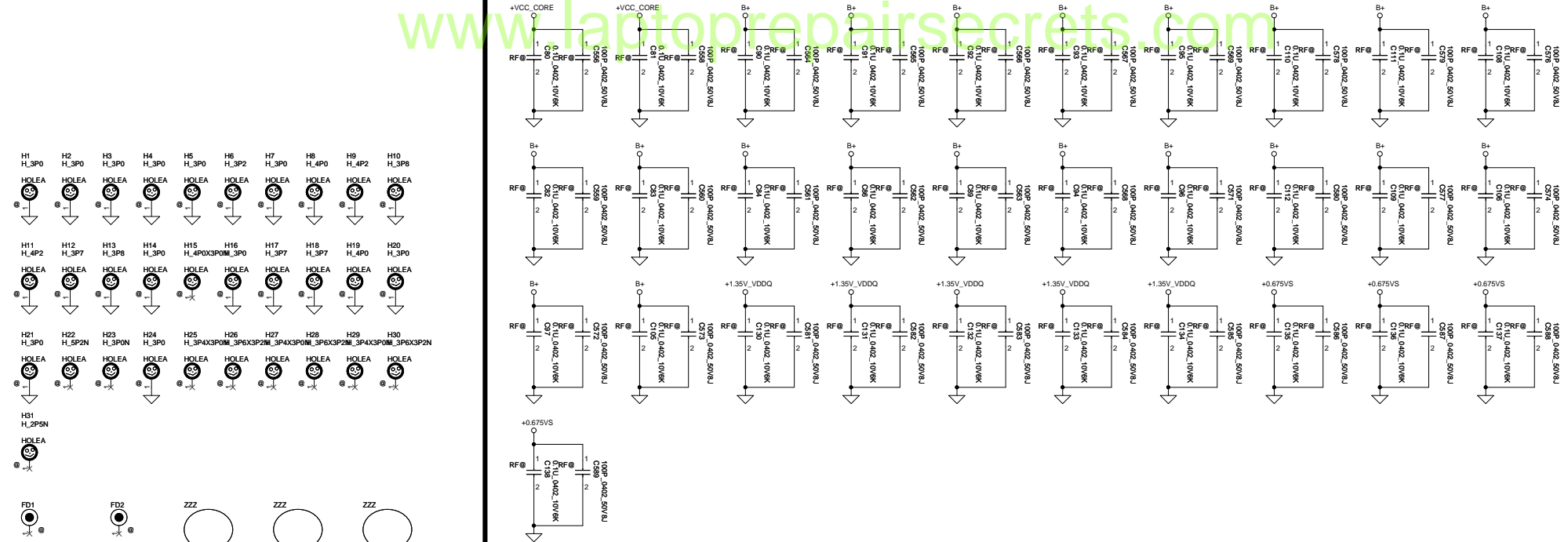


www.laptoprepairsecrets.com

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title PWRBTN/FAN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-B181P Rev 0.5
Date: Tuesday, March 25, 2014				Sheet 29 of 62

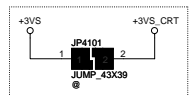


RF CAP

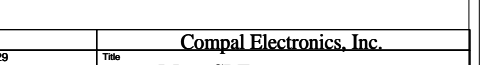
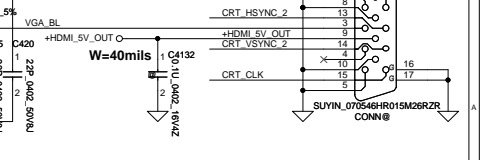
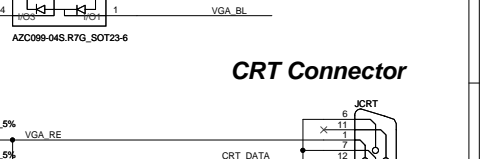
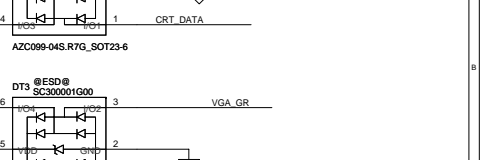
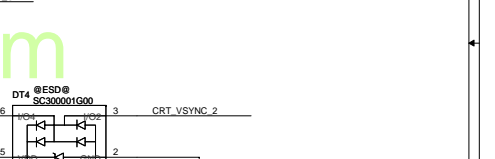
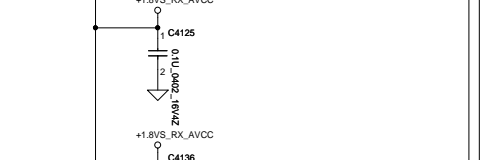
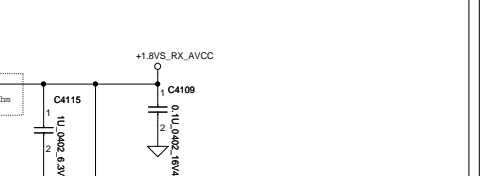
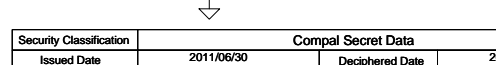
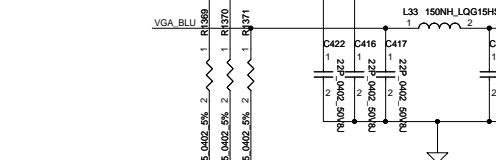
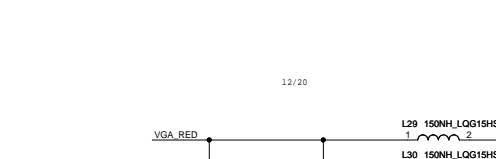
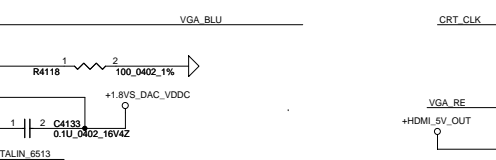
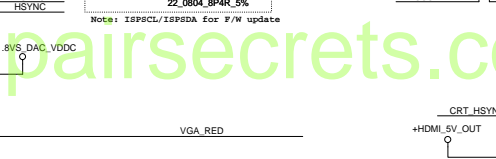
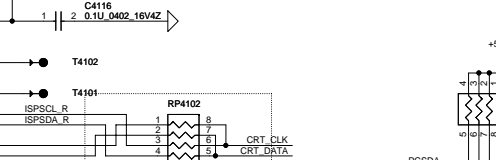
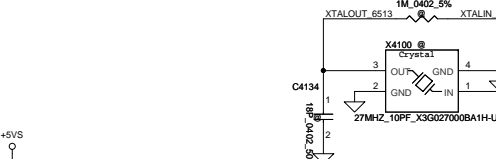
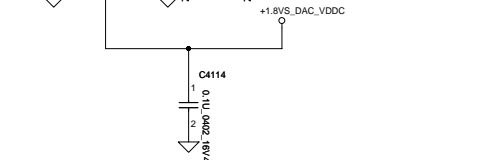
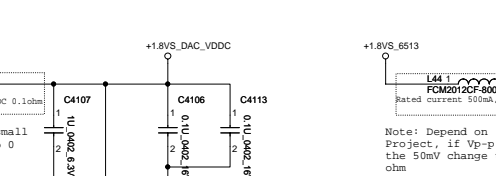
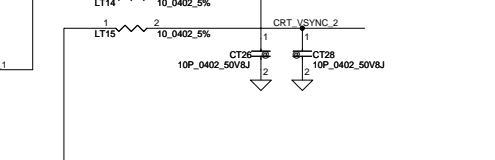
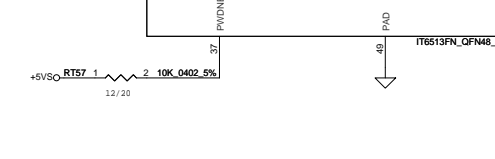
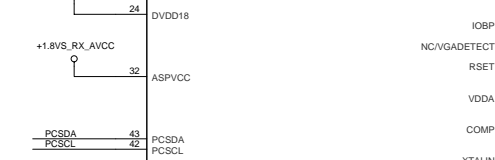
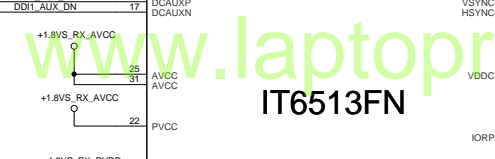
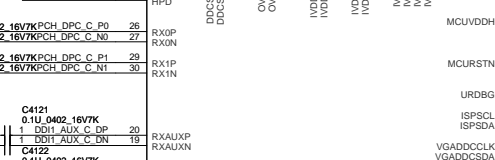
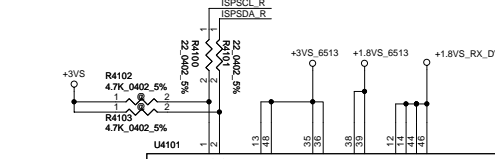
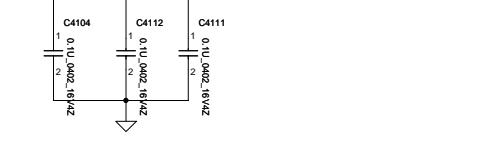
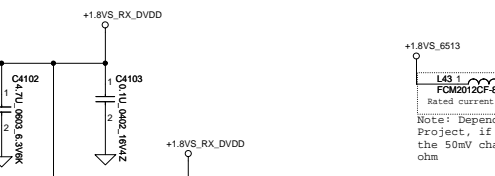
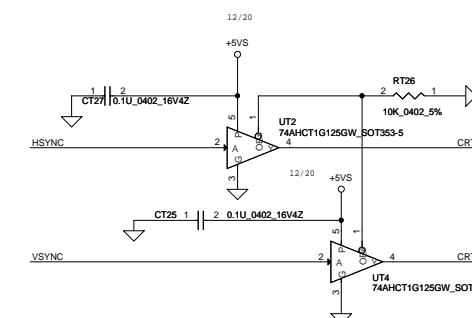
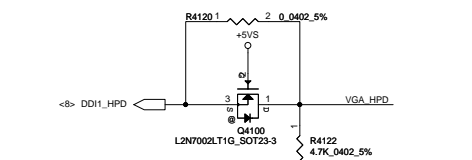
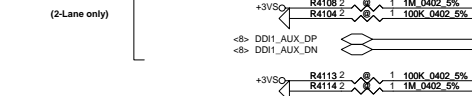
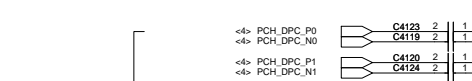


Security Classification	Compal Secret Data		Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	LED/Screw hole
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 0.5
Document Number			LA-B181P	Size
Date			Tuesday, March 25, 2014	Sheet 30 of 62

For Power consumption Measurement

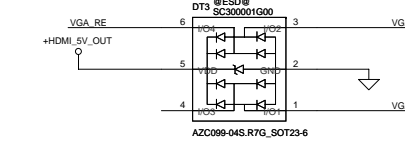
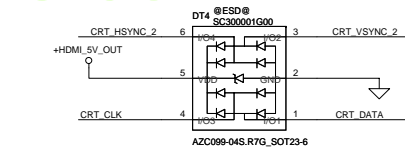
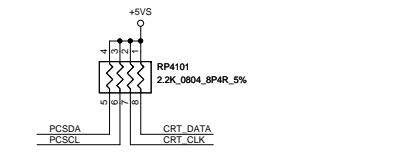
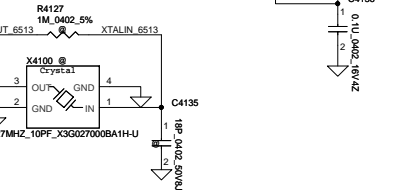
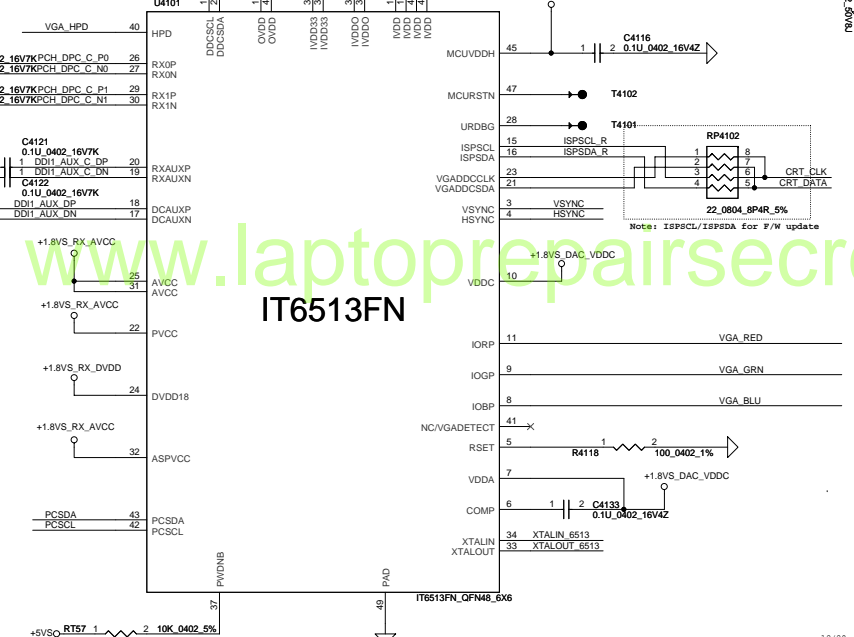


+3VS TO +3VS_6513

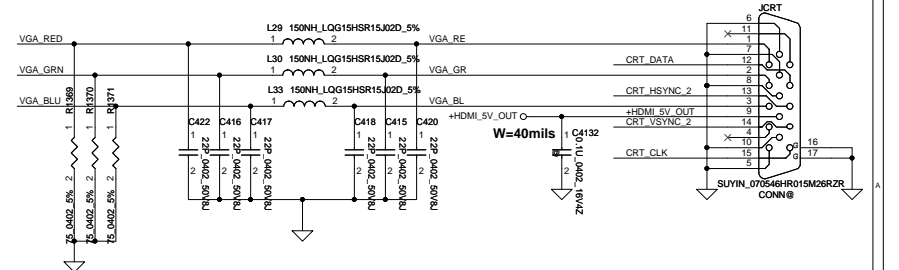


www.laptoprepairsecrets.com

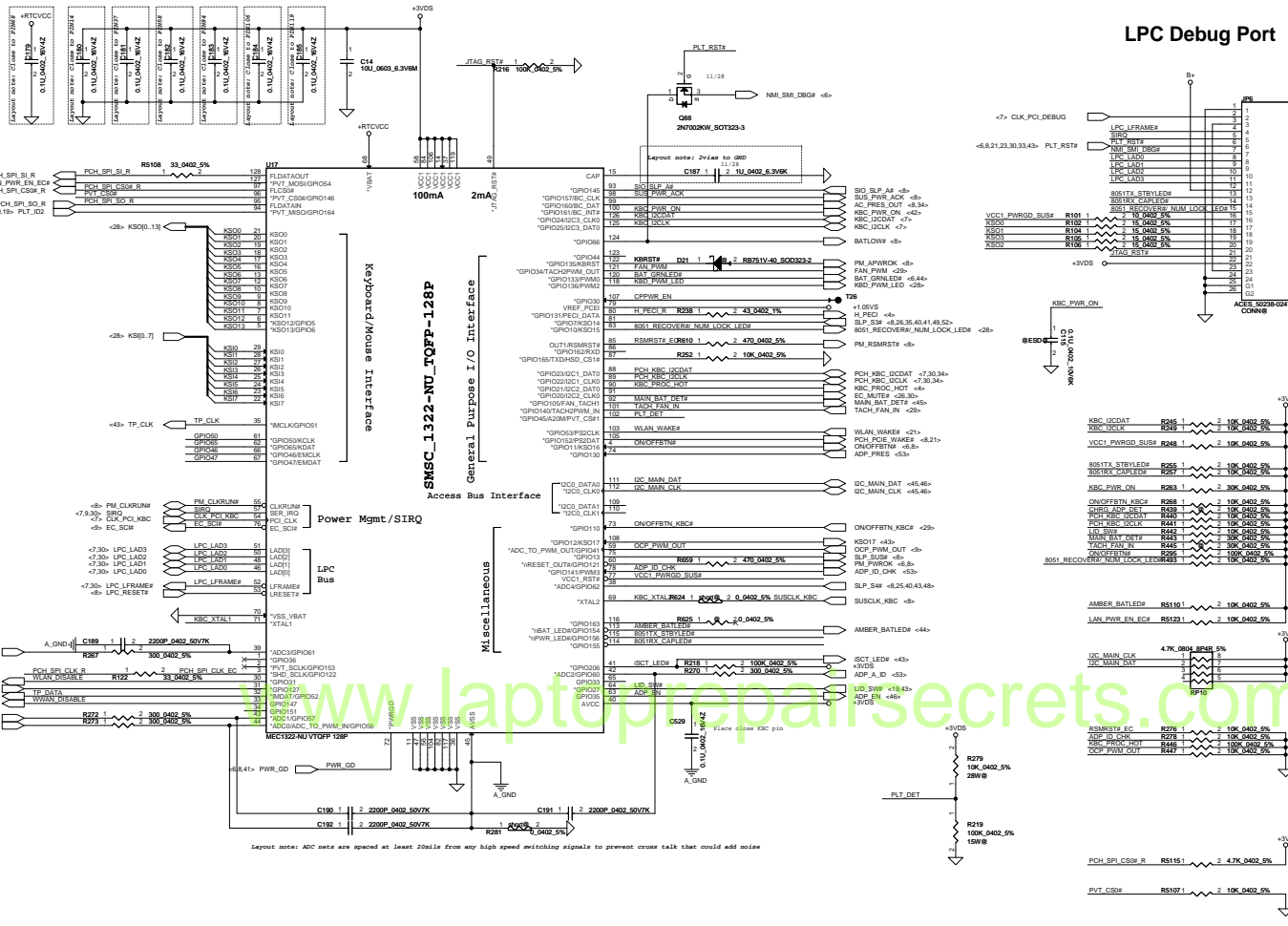
IT6513FN



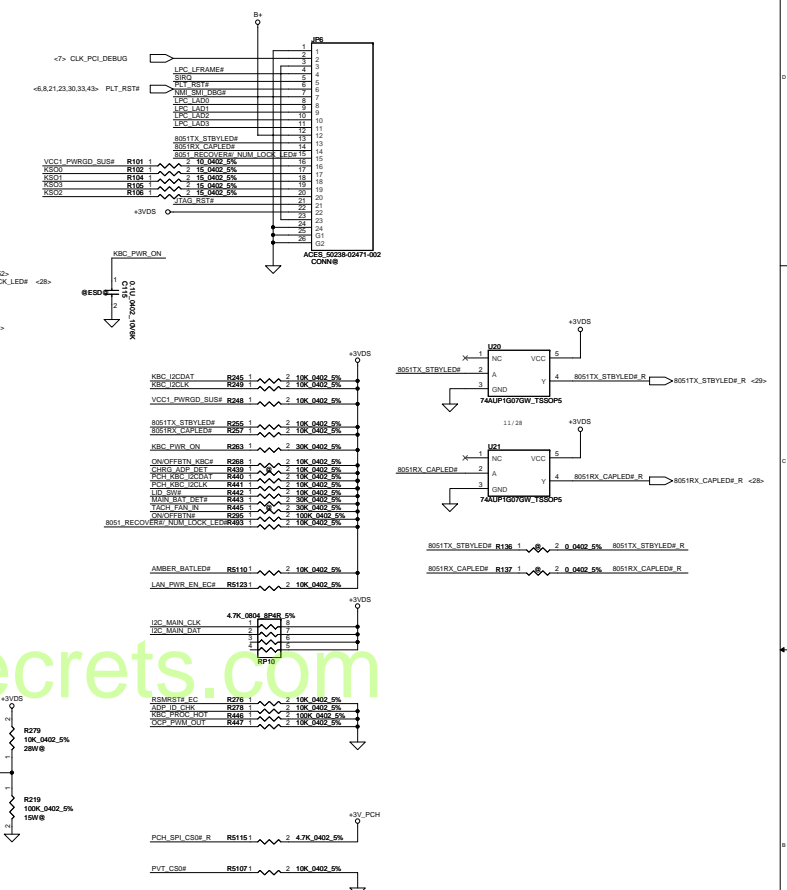
CRT Connector



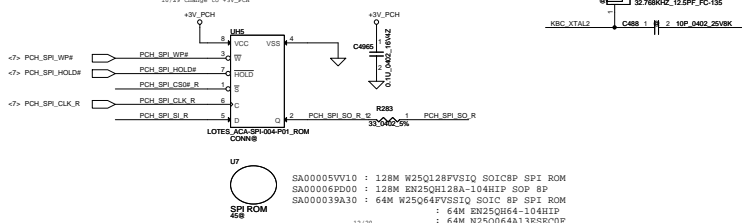
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2011/06/29	Title
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Document Number
				LA-B181P
				Rev 0.5
				Date: Tuesday, March 25, 2014
				Sheet 31 of 62



LPC Debug Port



SPI ROM (8MByte)



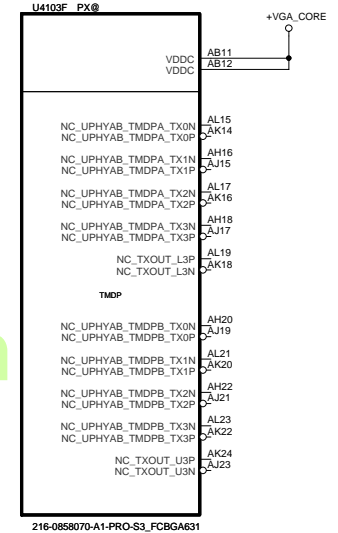
SA00005V10 : 128M N250128PVS1Q SOIC8P SPI ROM
 SA00006P00 : 128M N2508128A-104H1P SOP 8P
 SA000039A30 : 64M N25Q64PVS1Q SOIC 8P SPI ROM
 : 64M N2520864-104H1P
 : 64M N25Q64A13BSC00P

Security Classification	2011/06/29		Compal Secret Data	2011/06/29		Doc Number	EC SMC KB1322
Issued Date	2011/06/29		Deciphered Date	2011/06/29		Doc Number	LA-B181P
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPARTMENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.							
Date	Issued	Revised	By	Checked	By	By	By

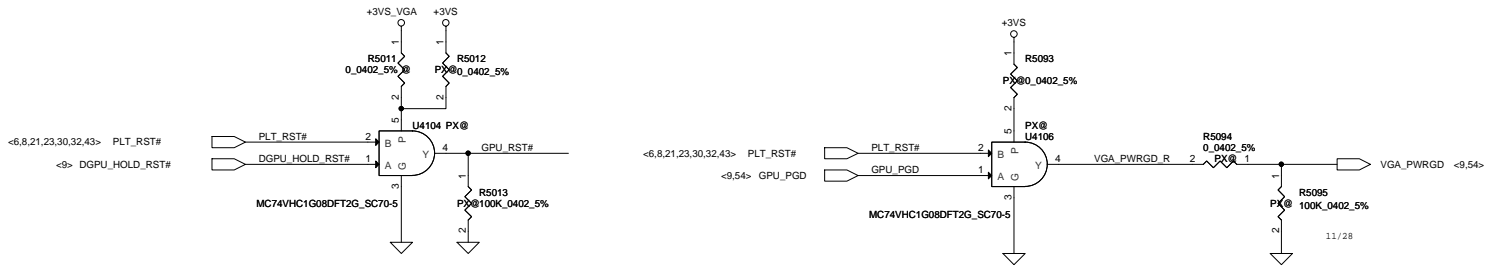


AC Coupling Capacitor
 PCIe Gen3: Recommended value is 220 nF
 PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No Use GPU Display Port output

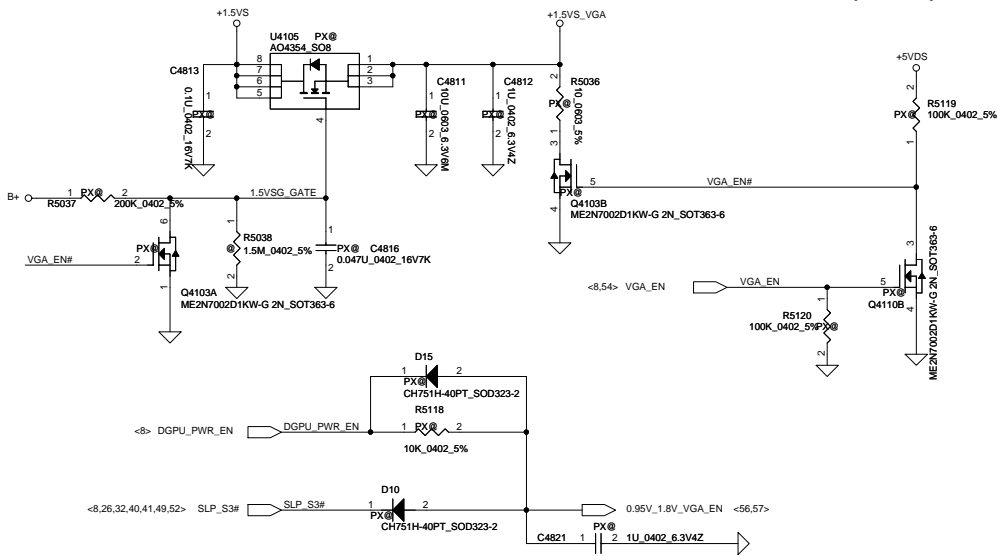


www.laptoprepairsecrets.com

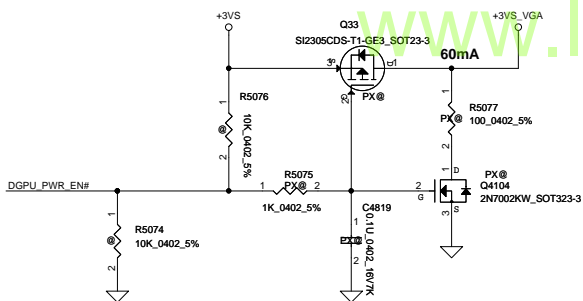


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	Topaz PCIe/DP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Custom	Document Number	LA-B181P	Rev	0.5
Date:	Tuesday, March 25, 2014	Sheet	33	of	62

+1.5VS to +1.5VS_VGA (2.096A)

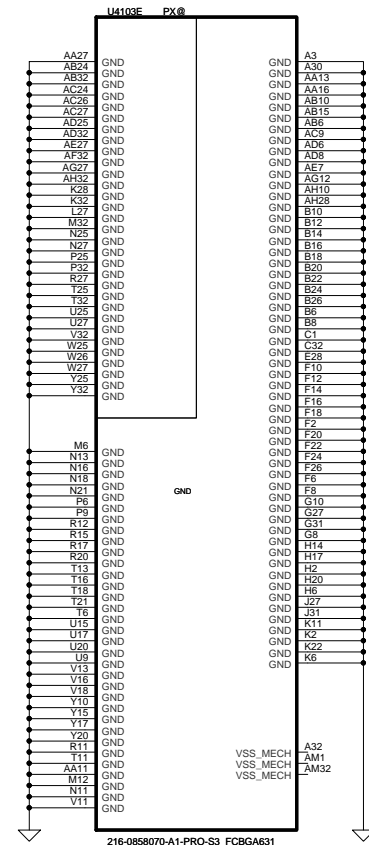
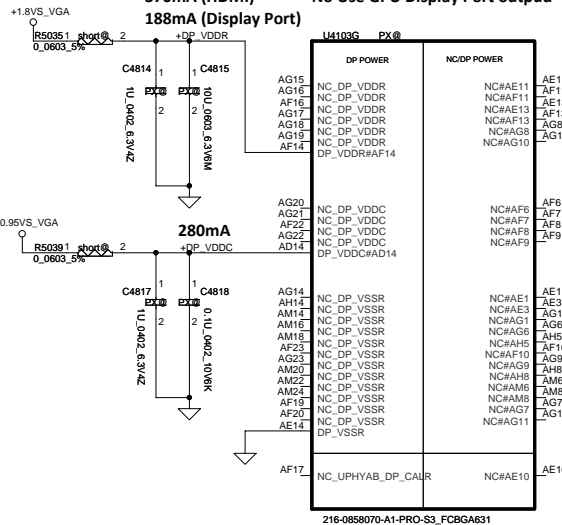


+3VS to +3VS_VGA (25mA)

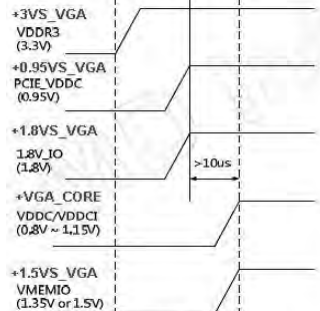


**370mA (HDMI)
188mA (Display Port)**

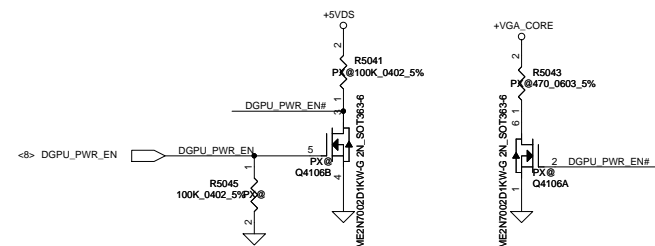
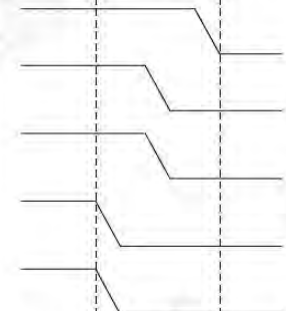
No Use GPU Display Port output



POWER UP



POWER DOWN



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	Topaz Power/GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Custom	Document Number	LA-B181P	Rev	0.5
Date:	Tuesday, March 25, 2014	Sheet	35	of	62

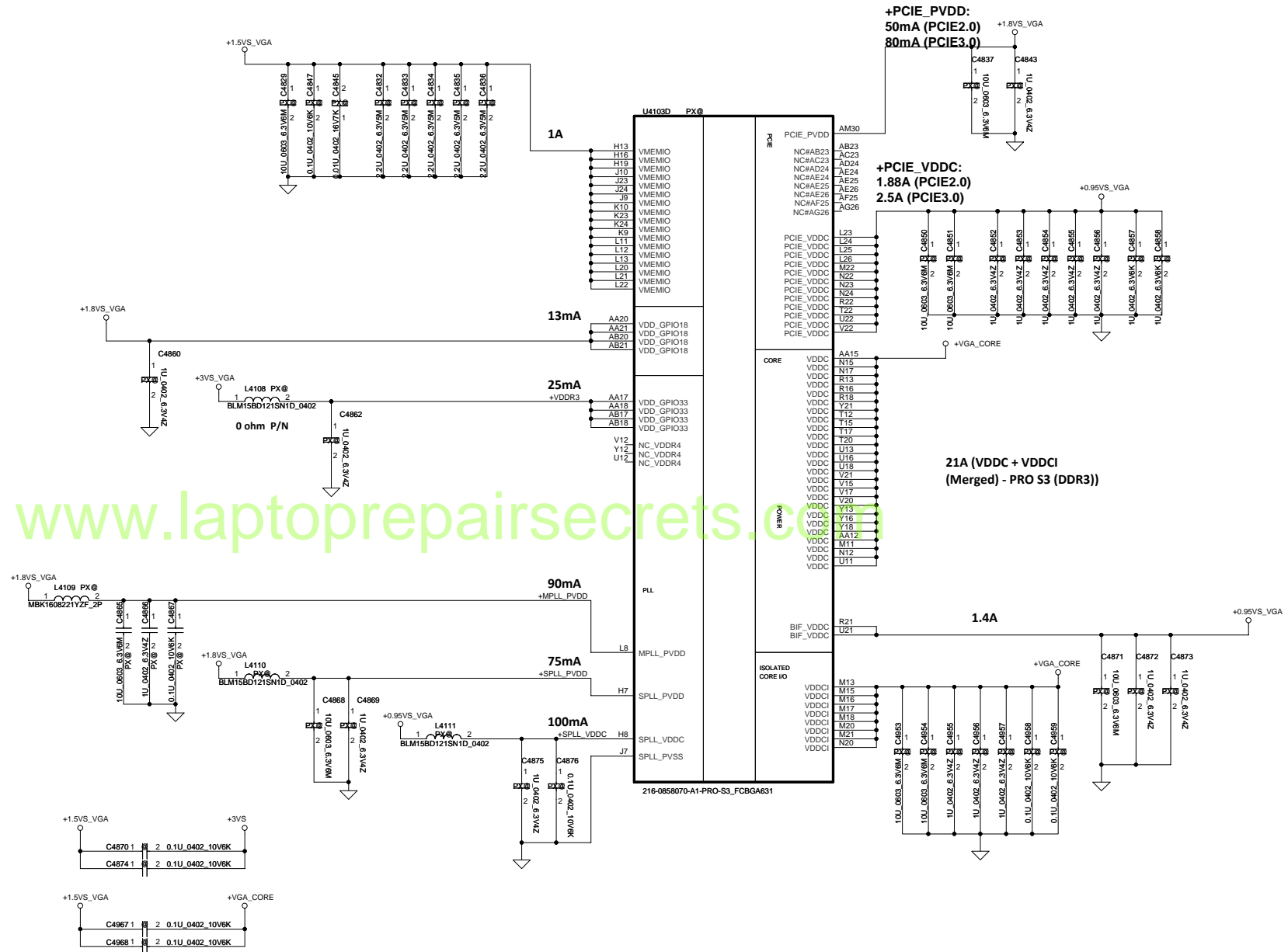
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

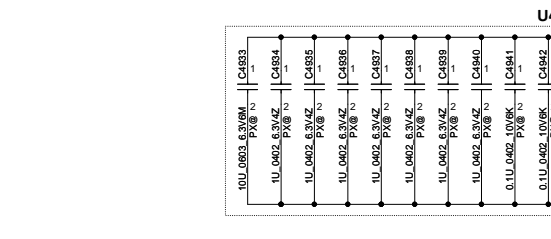
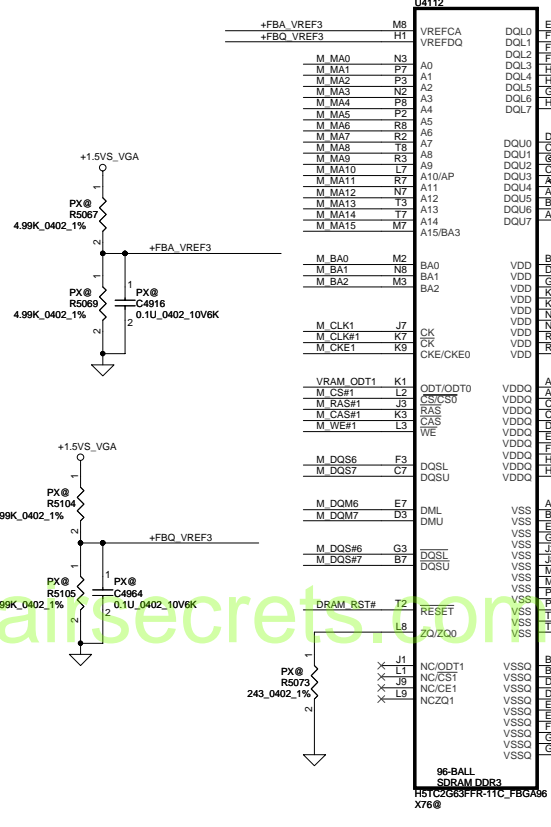
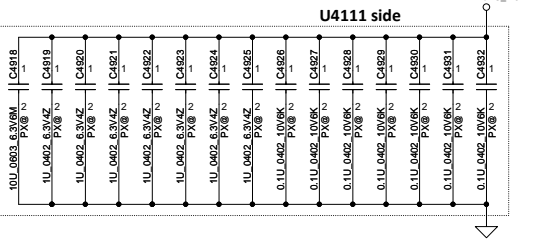
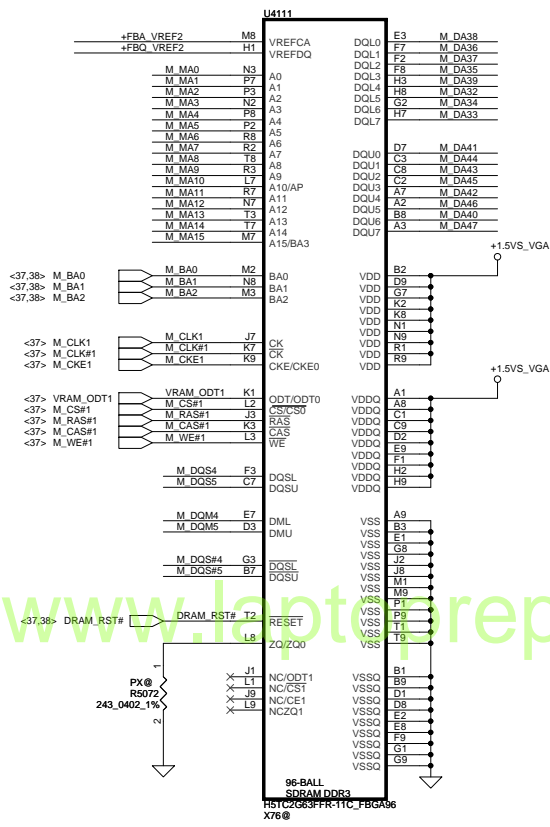
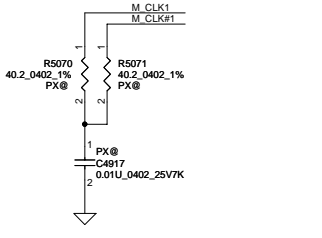
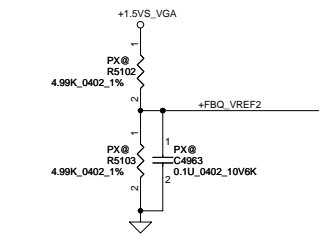
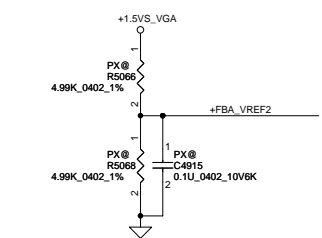
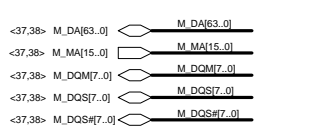
+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)

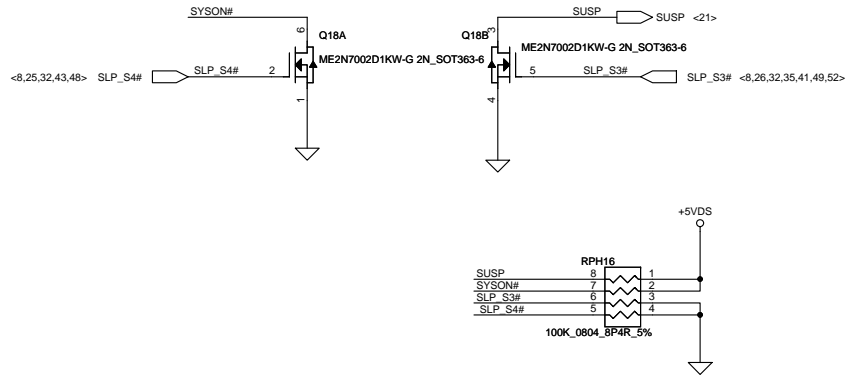
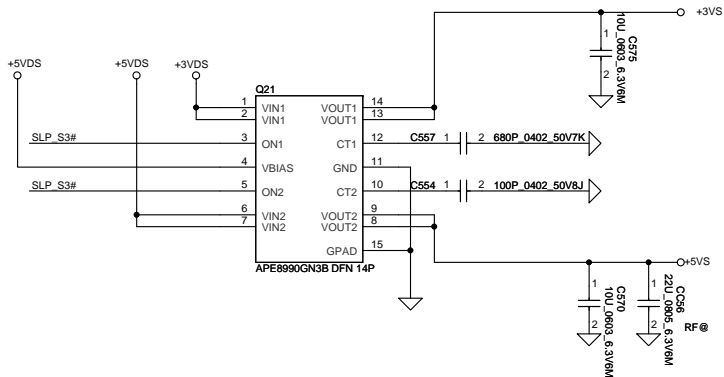


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title
				Topaz Power
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev
				0.5
				LA-B181P
Date: Tuesday, March 25, 2014				Sheet 36 of 62

Memory Partition A - Upper 32 bits

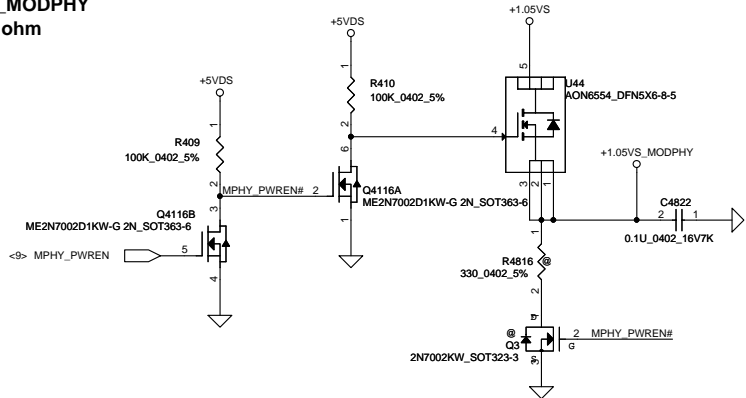


Security Classification		Compal Secret Data		Title	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Customer	Rev
				LA-B181P	05
Date: Tuesday, March 25, 2014				Sheet	39 of 62

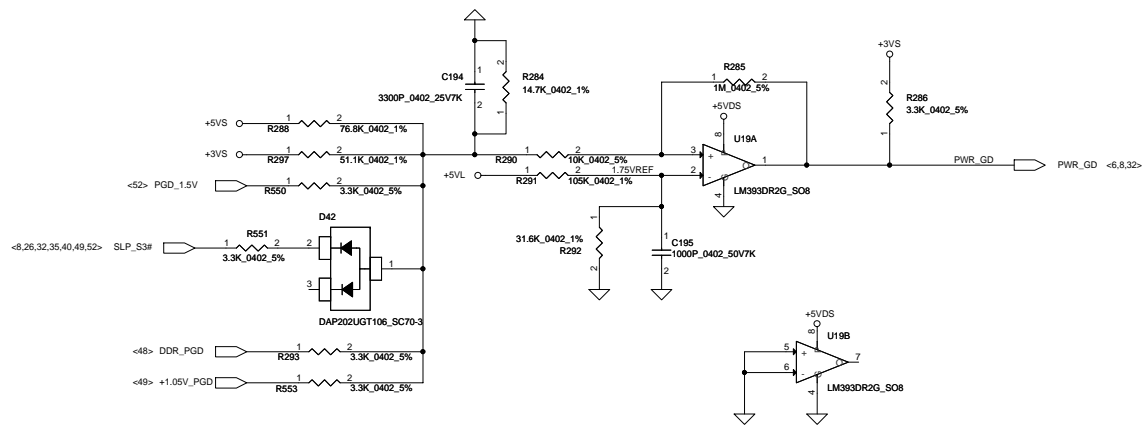


www.laptoprepairsecrets.com

CPU +V1.05DX_MODPHY
 Max Rdson <6m ohm
 1840mA

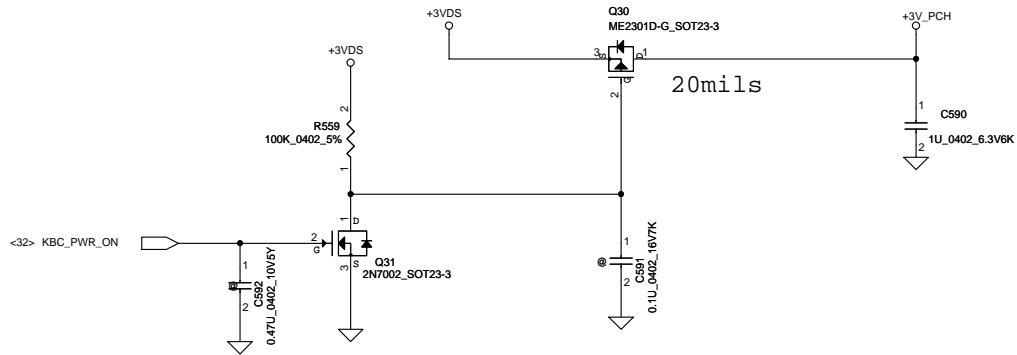


Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-B181P Rev 0.5 Date: Tuesday, March 25, 2014
			Sheet	40 of 62



www.laptoprepairsecrets.com

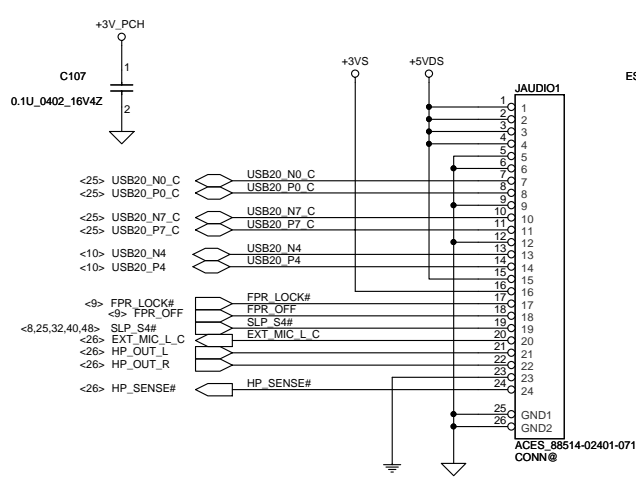
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Document Number	Rev
			LA-B181P	0.5
			Date: Tuesday, March 25, 2014	Sheet 41 of 62



www.laptoprepairsecrets.com

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	DC DC Device-1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-B181P	0.5
				Date:	Tuesday, March 25, 2014	Sheet 42 of 62

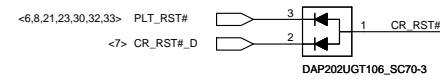
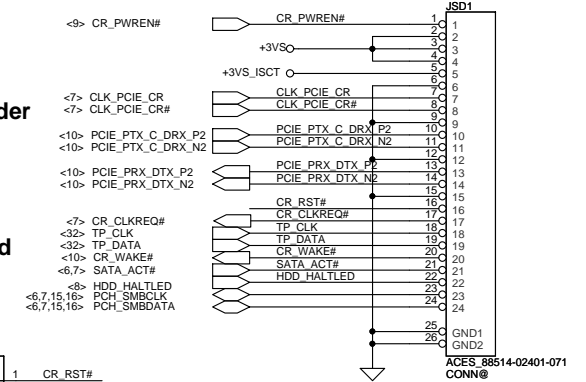
Audio Board



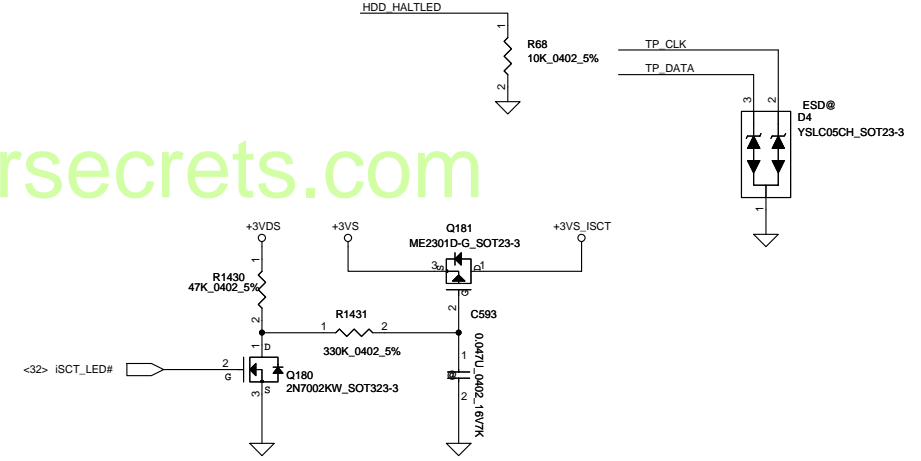
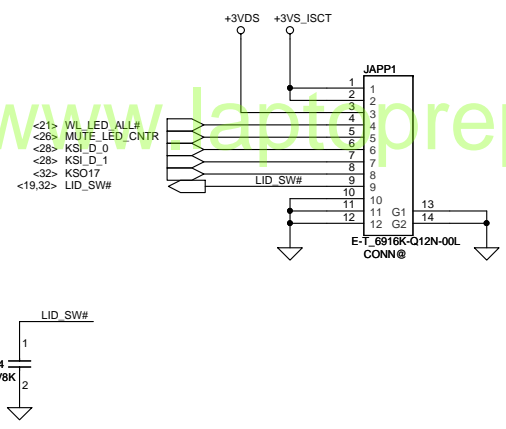
Card Reader Board

Card Reader

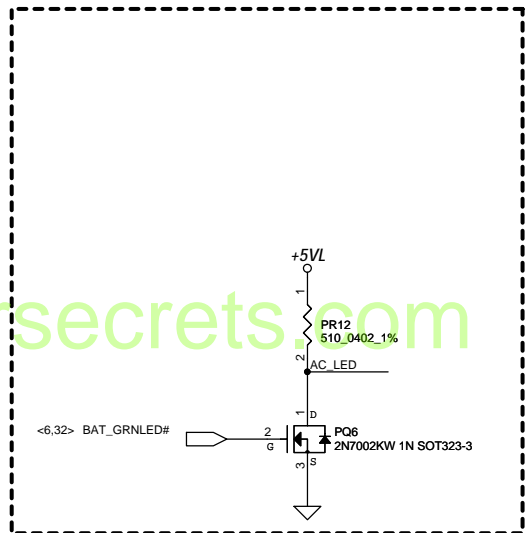
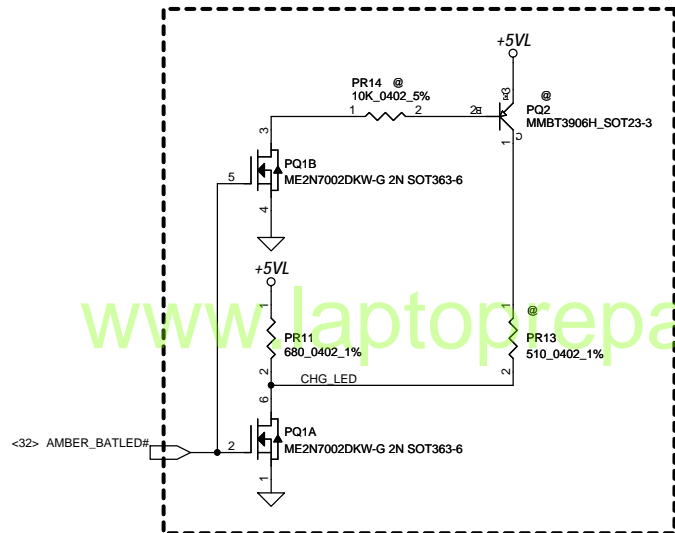
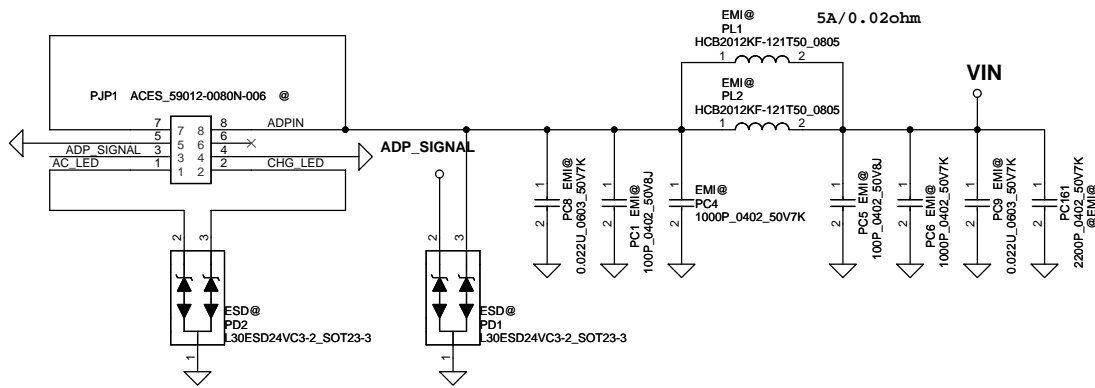
Touch Pad



www.laptoprepairsecrets.com

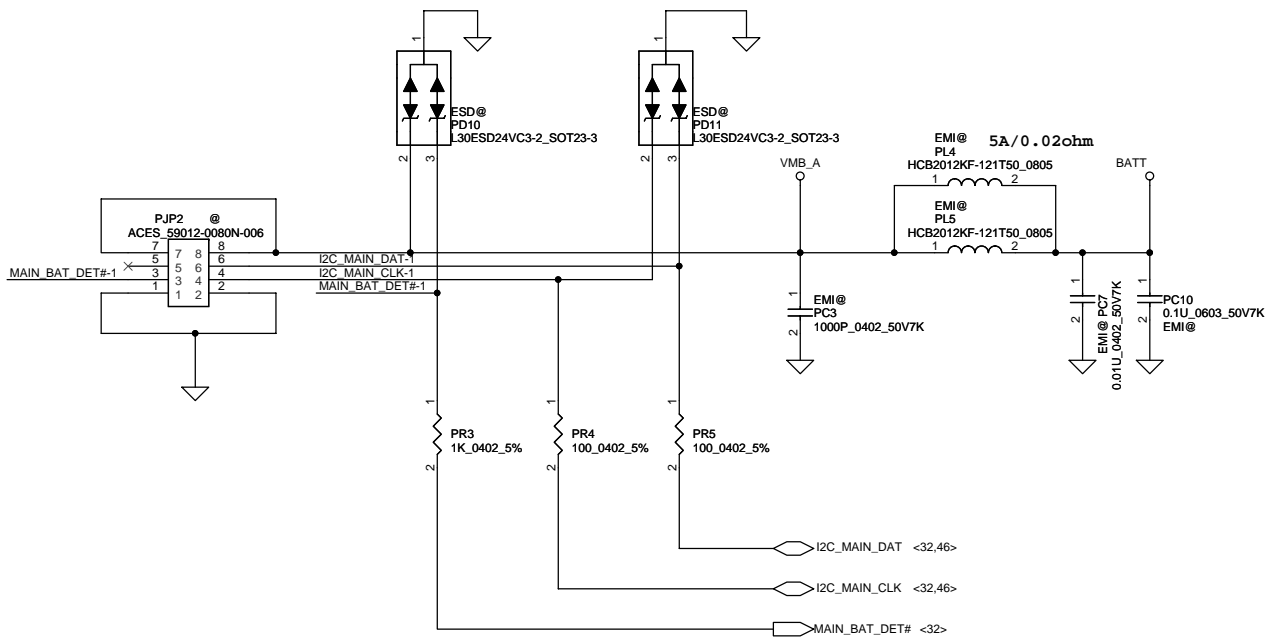


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	DC DC Device-1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number	Rev			
Custom	LA-B181P	0.5			
Date:	Tuesday, March 25, 2014	Sheet	43	of	62



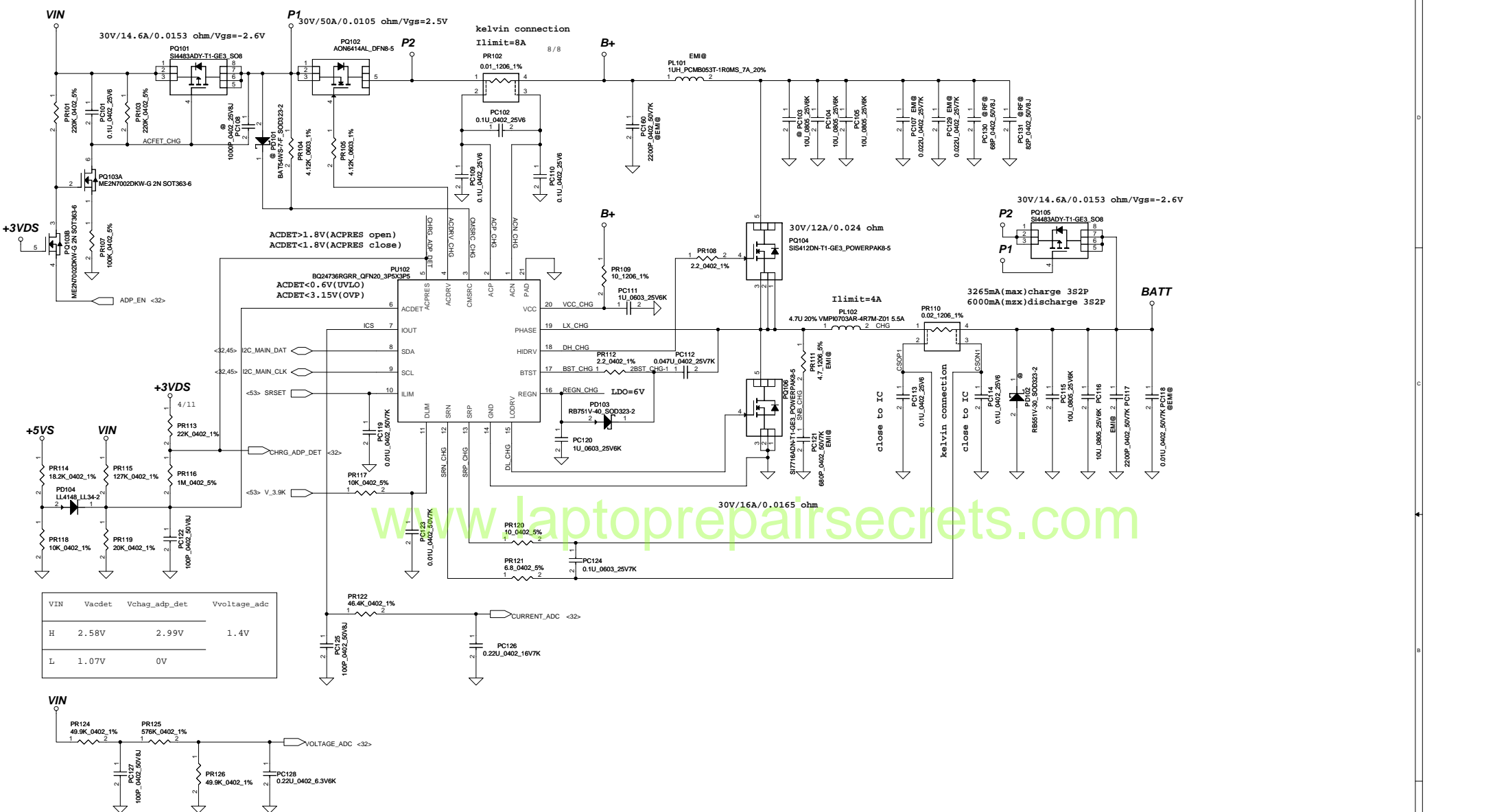
www.laptoprepairsecrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	DC Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B181P
Date:	Tuesday, March 25, 2014	Sheet	44	of	62



www.laptoprepairsecrets.com

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	BATT Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B181P
Date:	Tuesday, March 25, 2014	Sheet	45	of	62
Rev	0.5				



www.laptoprepairsecrets.com

VIN	Vacdet	Vchag_adp_det	Vvoltage_adc
H	2.58V	2.99V	1.4V
L	1.07V	0V	

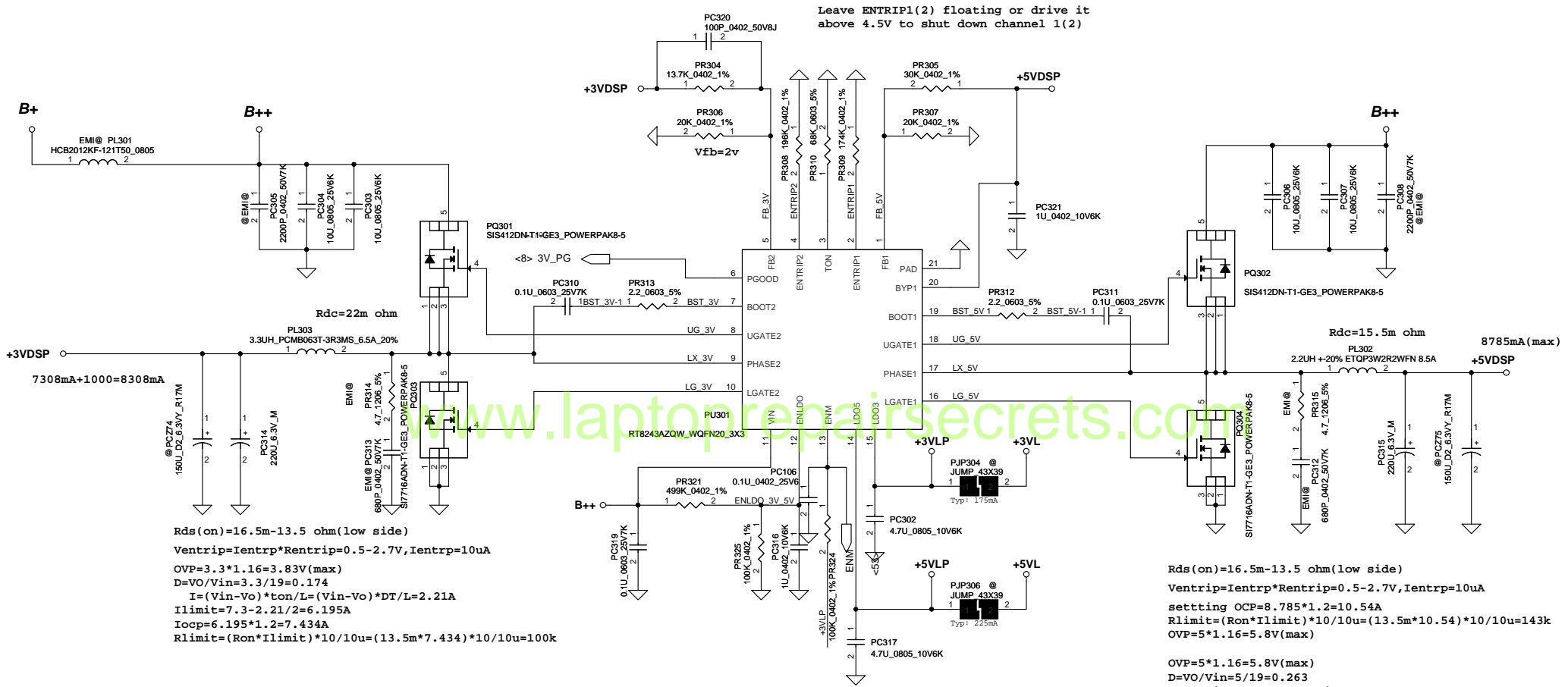
$I_{limit} = 20 * (V_{srp} - V_{srn}) = 20 * I_{ch} * R_{ch}$
 up to $I_{limit} = 1.6V$ (disable)
 $R = 1.0m \text{ ohm}$ $I = 8A$
 $R = 2.0m \text{ ohm}$ $I = 4A$
 $fs = 750k$
 $I_{ripple} = V_{in} * D * (1 - D) / (fs * L)$,
 $D = 0.5$ (worst)
 $I_{ripple} = 1.418A$
 $I_{sat}(L) = I_{ch} + 0.5 * I_{ripple} = 4 + 0.5 * 1.418 = 4.709A$

ILIM > 1.6V disable
 ILIM < 75mV disable
 ILIM > 105mV enable

DLIM > 1.1V disable
 DLIM < 87mV disable
 DLIM > 89mV enable (buck to boost)

default discharger current limit 4.096A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title CHARGER
			Size LA-B181P
			Rev D.5
			Date: Tuesday, March 25, 2014 Sheet 46 of 62

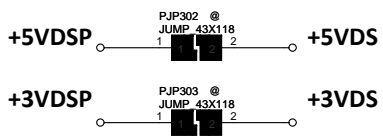


Leave ENTRIP1(2) floating or drive it above 4.5V to shut down channel 1(2)

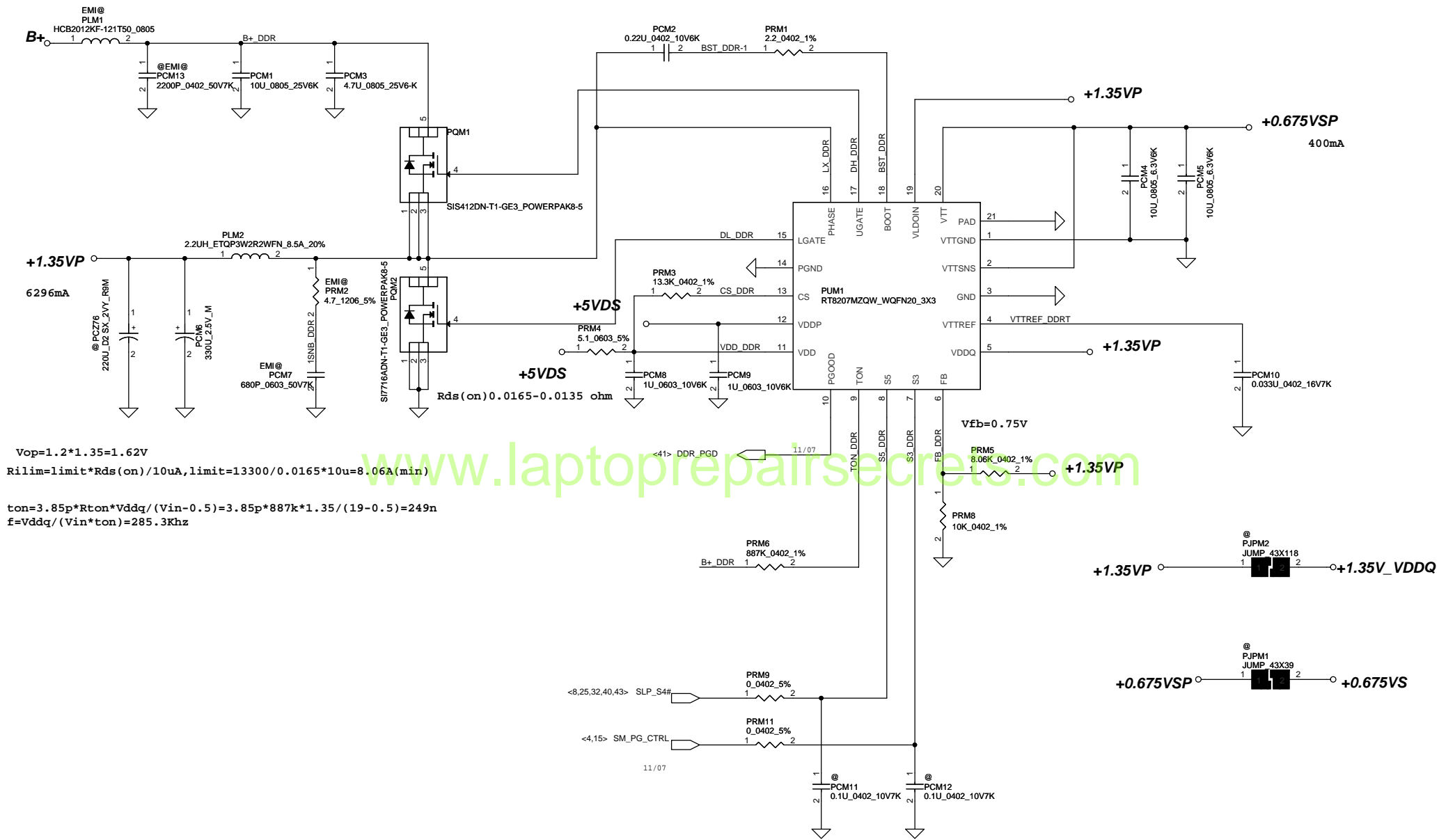
$R_{dc} = 22m\ \Omega$
 $R_{ds(on)} = 16.5m - 13.5\ \Omega$ (low side)
 $V_{entrip} = I_{entrp} * R_{entrp} = 0.5 - 2.7V$, $I_{entrp} = 10\ \mu A$
 $OVP = 3.3 * 1.16 = 3.83V$ (max)
 $D = V_O / V_{in} = 3.3 / 19 = 0.174$
 $I = (V_{in} - V_O) * t_{on} / L = (V_{in} - V_O) * DT / L = 2.21A$
 $I_{limit} = 7.3 - 2.21 / 2 = 6.195A$
 $I_{ocp} = 6.195 * 1.2 = 7.434A$
 $R_{limit} = (R_{on} * I_{limit}) * 10 / 10u = (13.5m * 7.434) * 10 / 10u = 100k$

$R_{dc} = 15.5m\ \Omega$
 $R_{ds(on)} = 16.5m - 13.5\ \Omega$ (low side)
 $V_{entrip} = I_{entrp} * R_{entrp} = 0.5 - 2.7V$, $I_{entrp} = 10\ \mu A$
 setting $OCP = 8.785 * 1.2 = 10.54A$
 $R_{limit} = (R_{on} * I_{limit}) * 10 / 10u = (13.5m * 10.54) * 10 / 10u = 143k$
 $OVP = 5 * 1.16 = 5.8V$ (max)
 $D = V_O / V_{in} = 5 / 19 = 0.263$
 $I = (V_{in} - V_O) * t_{on} / L = (V_{in} - V_O) * DT / L = 5.21A$
 $I_{limit} = 8.785 - 5.21 / 2 = 6.18A$
 $I_{ocp} = 6.195 * 1.2 = 7.416A$
 $R_{limit} = (R_{on} * I_{limit}) * 10 / 10u = (13.5m * 7.416) * 10 / 10u = 100k$

$<1> 5V = 283KHz$ $3V = 330KHz$ ($V_{in} = 6.5 \sim 12V$)
 $<2> 5V = 321KHz$ $3V = 375KHz$ ($V_{in} = 12 \sim 25V$)
 (By $R_{ton} = 68K\ \Omega$)



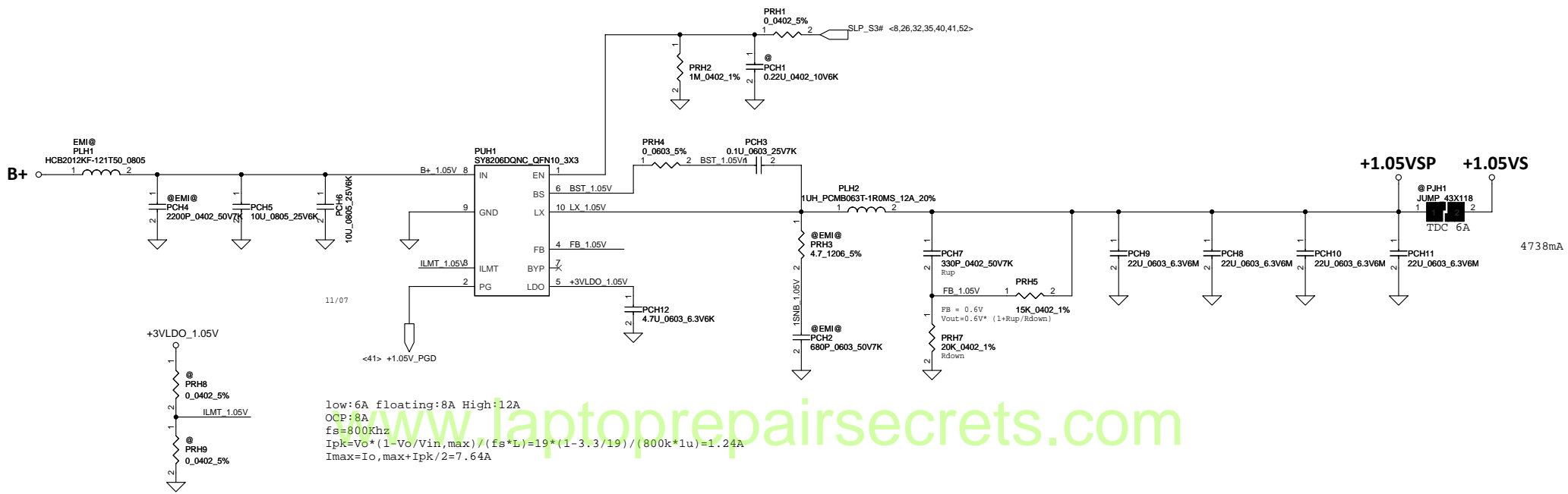
Security Classification		Compal Secret Data		Title	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	3VDSP/5VDSP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B181P	0.5
Date: Tuesday, March 25, 2014				Sheet	47 of 62



$V_{op} = 1.2 * 1.35 = 1.62V$
 $R_{lim} = \text{limit} * R_{ds(on)} / 10uA, \text{limit} = 13300 / 0.0165 * 10u = 8.06A(\text{min})$
 $t_{on} = 3.85p * R_{ton} * V_{ddq} / (V_{in} - 0.5) = 3.85p * 887k * 1.35 / (19 - 0.5) = 249n$
 $f = V_{ddq} / (V_{in} * t_{on}) = 285.3Khz$

www.laptoprepairscrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Custom	0.5
				Date:	Tuesday, March 25, 2014
				Sheet	48 of 62



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	+1.05VS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date:	Tuesday, March 25, 2014
				Sheet	49 of 62
				Rev	0.5

PRZ5:Vo-usr=1.7*(150/(150+9.53))=1.598V
 Vusr=540mV
 PRZ11:disable OSR&PT,Rosr=150K
 PRZ10:setting fs R=150=>1Mhz
 Ramp setting:
 PRZ9=100K type:160mV
 PRZ9=>150K type:40mV
 boot voltage setting:
 Vb-ram=1V=>2V
 Vb-ram=0V=>1.7V
 Vb-ram>1.525V=>0V

Iccmax=32A(15w),Iccmax=40A(28w)
 IccTDC=10A(15w),IccTDC=16A(28w)
 IccDyn=27A(15w),IccDyn=32A(28w)

OCP voatge seeting:
 PRZ8=39K ==>18.9mV
 Vimom=1.7V

Rp_n=10.74k Rcs(eff)=0.6m ohm
 1.7V=10*(1+Rimom/39k)*0.6m*32,Rimom=345k

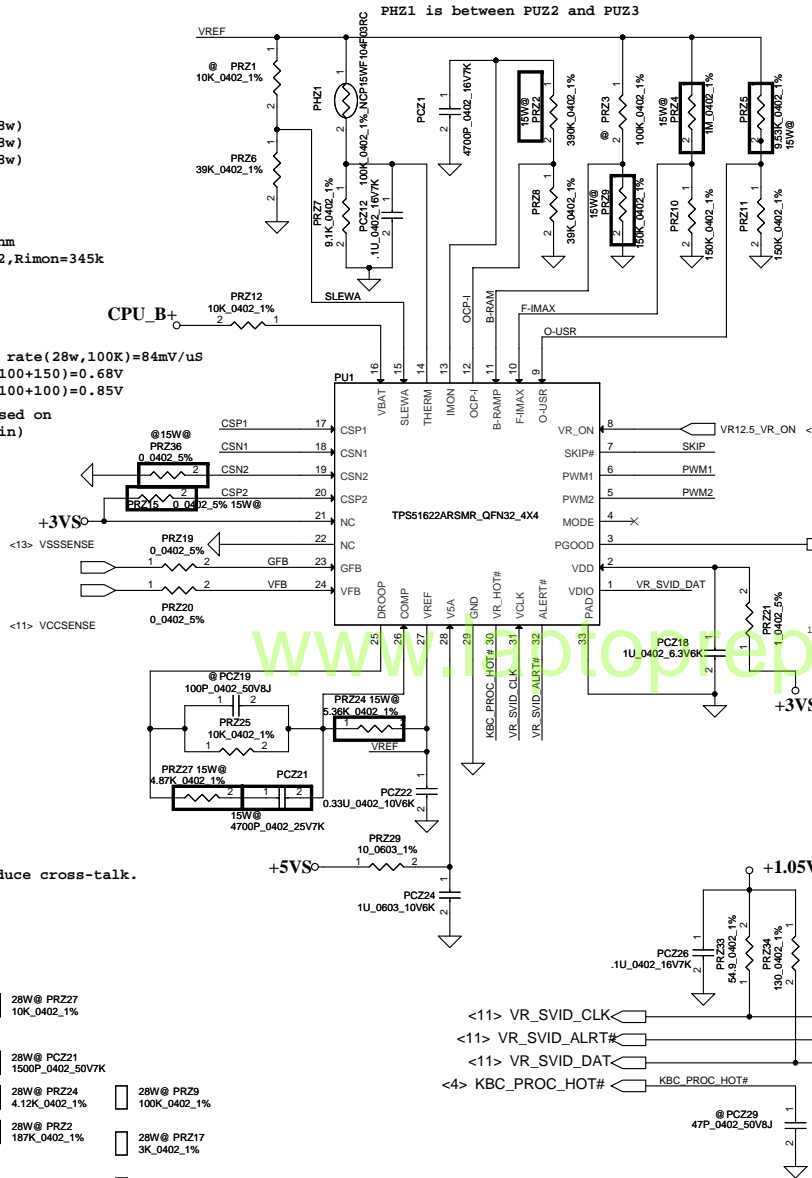
ALERT goes low,THERM=1.08V
 VR_HOT goes low,THERM=1.1V

slew rate(15w,150K)=96mV/uS,slew rate(28w,100K)=84mV/uS
 address selection(15w):1.7*100/(100+150)=0.68V
 address selection(28w):1.7*100/(100+100)=0.85V

On-tome(ton):ON-time is fixed based on
 the input voltage (at the VBAT pin)

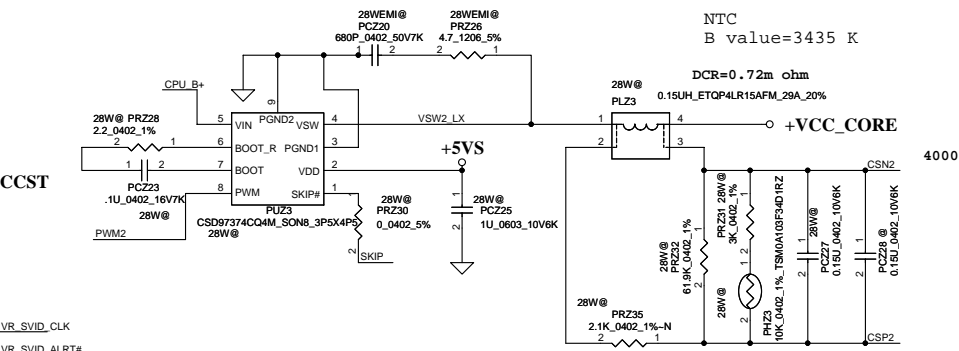
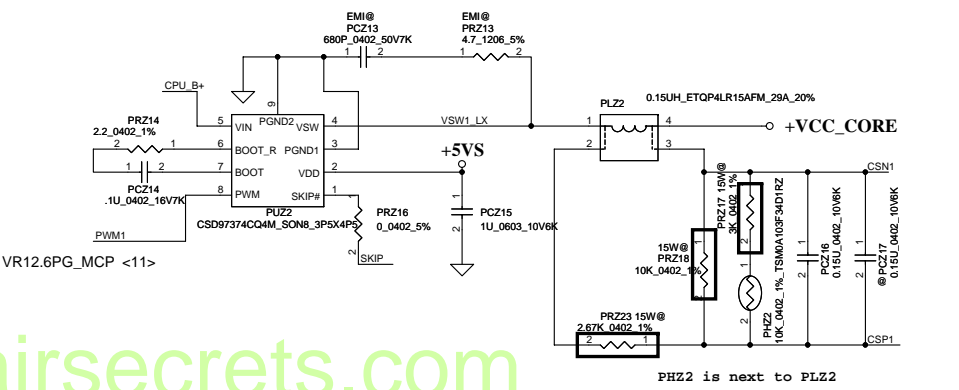
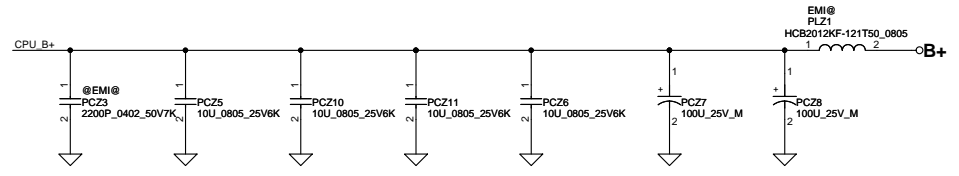
Vssense and Vccsense need to
 be difference pair

Drop:Error amplifier output.

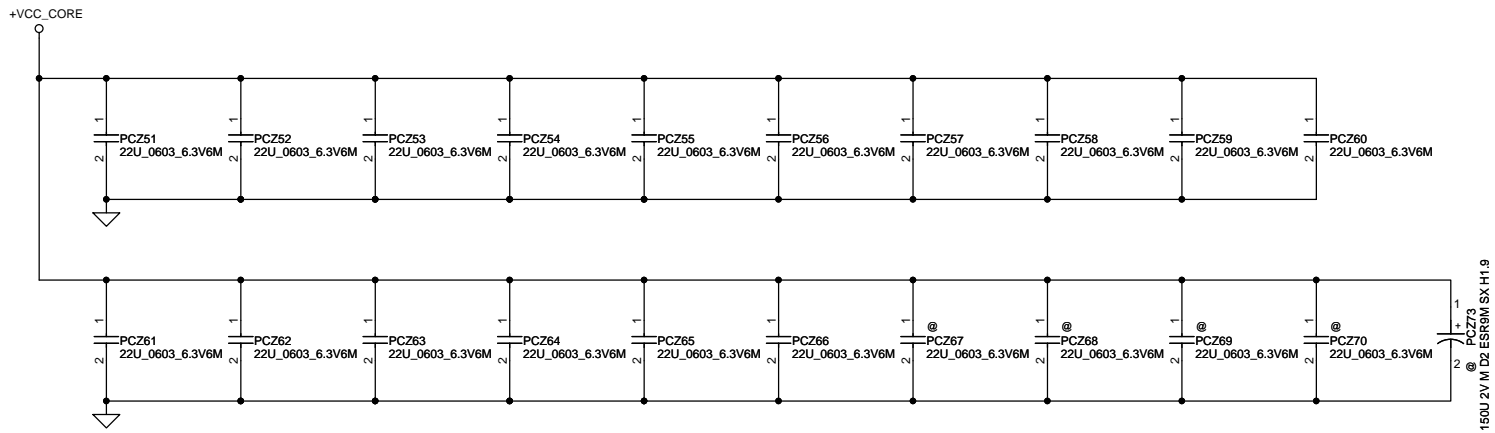


- 28W@ PRZ27 10K_0402_1%
- 28W@ PCZ21 1500P_0402_50V7K
- 28W@ PRZ24 4.12K_0402_1%
- 28W@ PRZ2 187K_0402_1%
- 28W@ PRZ4 806K_0402_1%
- 28W@ PRZ5 280K_0402_1%
- 28W@ PRZ9 100K_0402_1%
- 28W@ PRZ17 3K_0402_1%
- 28W@ PRZ23 2.1K_0402_1%
- 28W@ PRZ18 61.9K_0402_1%

not mount 需特别注意 (15w@,28w@)

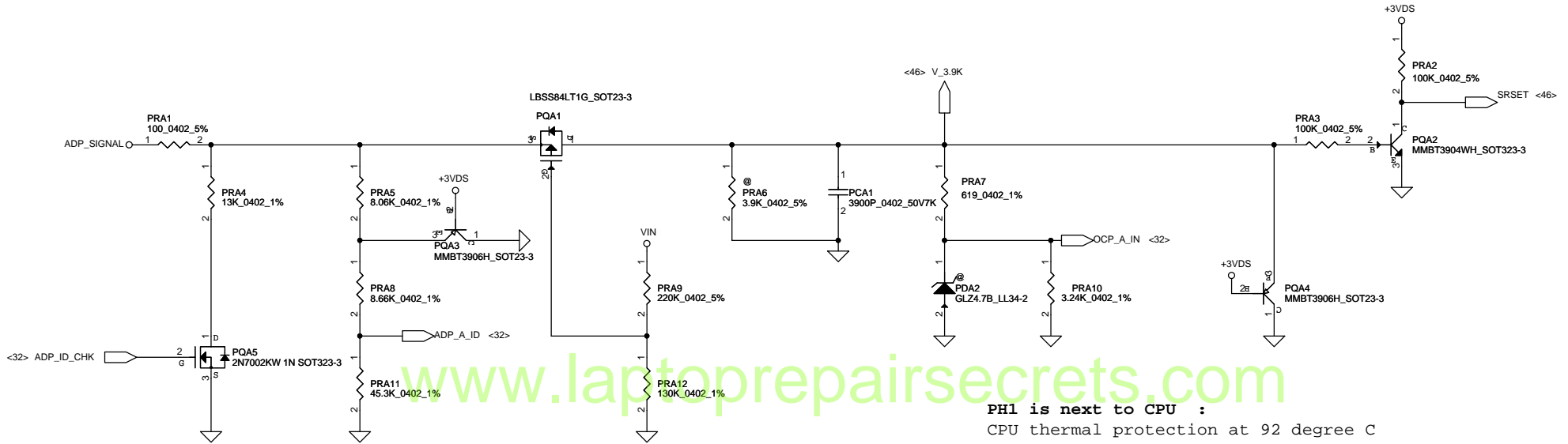


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				LA-B181P
				Rev
				1.5
Date: Tuesday, March 25, 2014		Sheet 50 of 62		

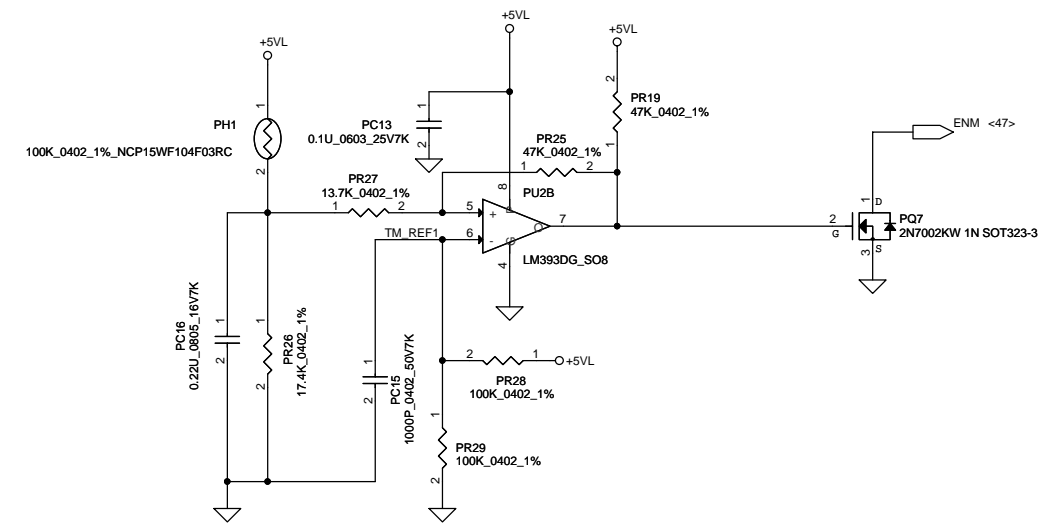
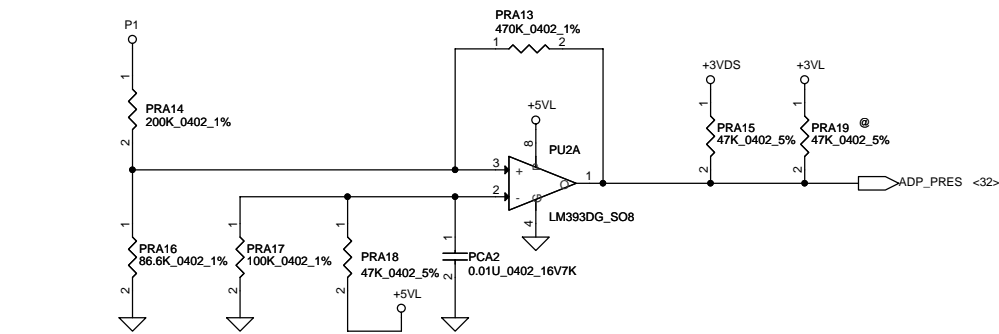


www.laptoprepairsecrets.com

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	PROCESSOR DECOUPLING
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-B181P	0.5
Date: Tuesday, March 25, 2014				Sheet	51 of 62



MEMO:PRA4 and PQA5 are not mount

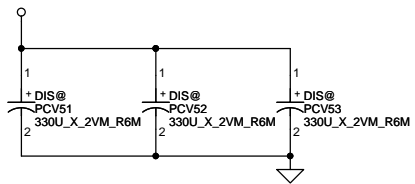


www.laptoprepairsecrets.com

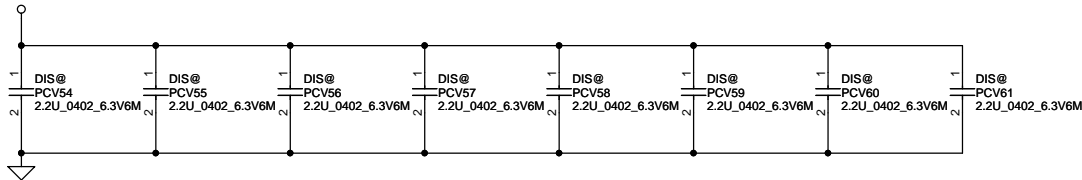
PH1 is next to CPU :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	ADP_OCP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Date:	Tuesday, March 25, 2014	Sheet	53	of	62

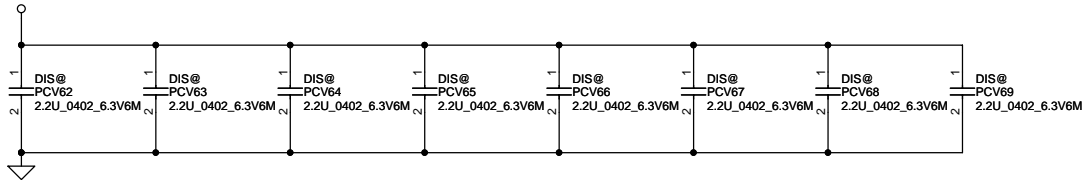
+VGA_CORE



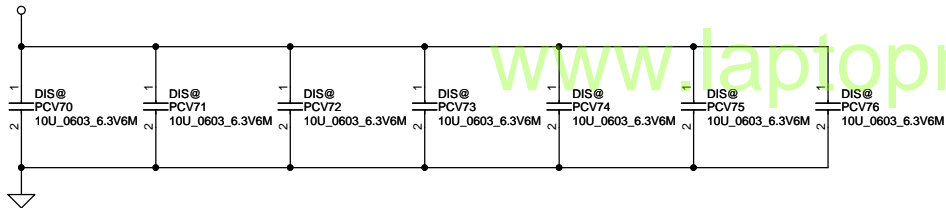
+VGA_CORE



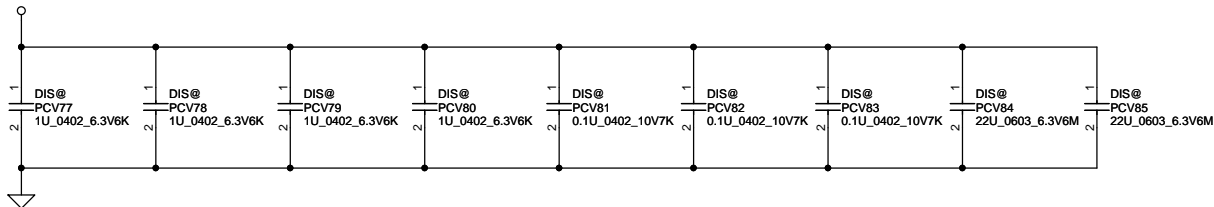
+VGA_CORE



+VGA_CORE



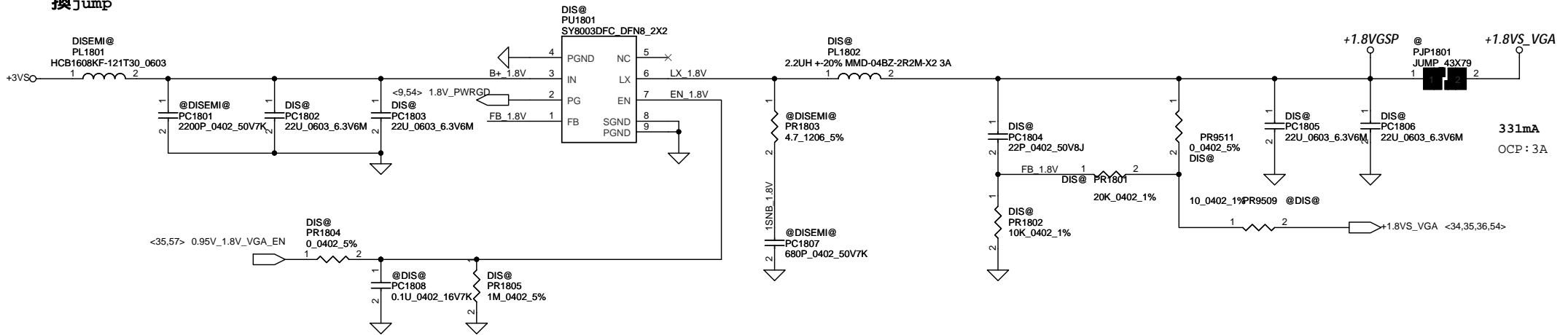
+VGA_CORE



www.laptoprepairsecrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/03	Deciphered Date	2016/09/30	Title	VGA CHIP DECOUPLING
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-B181P
Date:	Tuesday, March 25, 2014	Sheet	55	of	62
Rev	0.5				

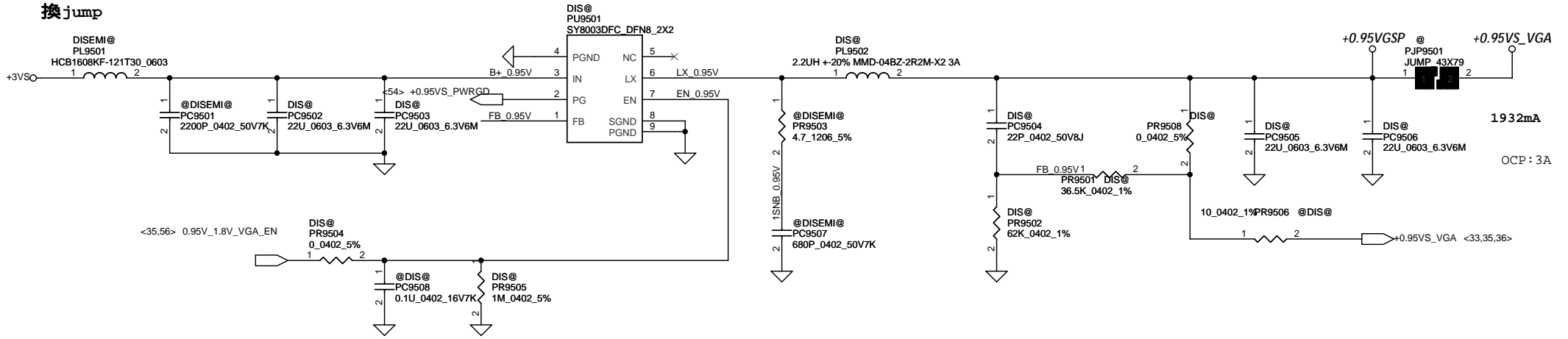
換jump



www.laptoprepairsecrets.com

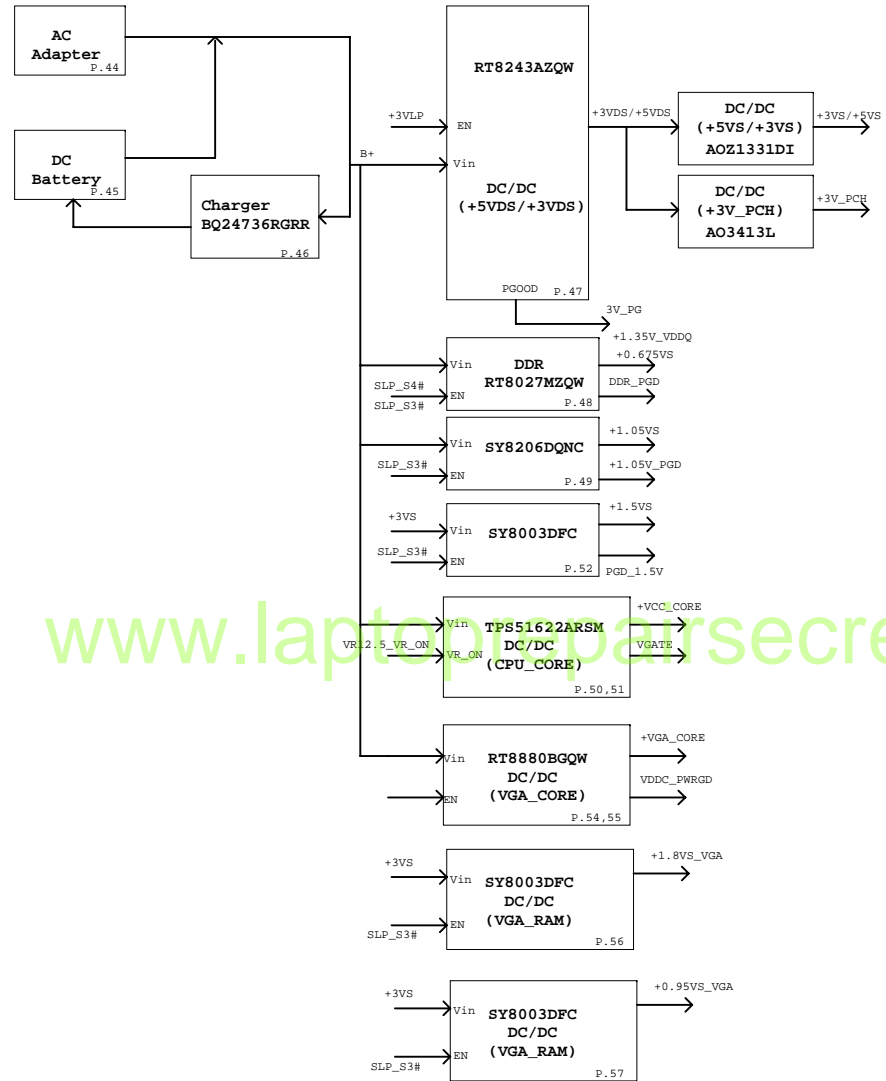
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	+1.8VS VGA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.5
				Date:	LA-B181P
				Sheet	56 of 62

換jump



www.laptoprepairsecrets.com

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title	+0.95VS VGA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.5
				Date	LA-B181P

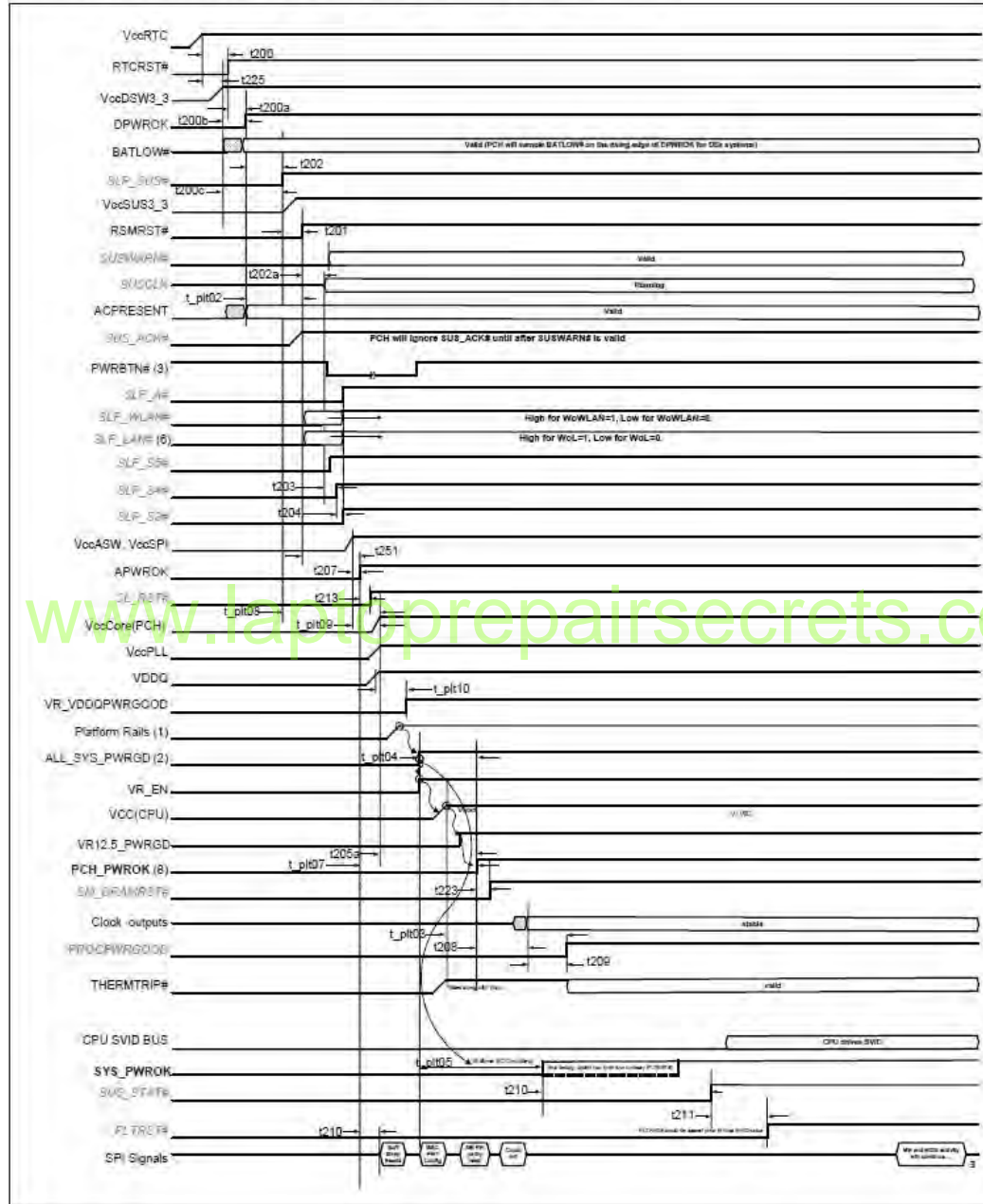


CPU DC/DC	
TPS51622ARSMR 50-51	
INPUTS	OUTPUTS
B+	VCC_CORE
SYSTEM DC/DC	
RT8243AZQW 47	
INPUTS	OUTPUTS
B+	3VDS/5VDS
SYSTEM DC/DC	
RT8207MZQW 48	
INPUTS	OUTPUTS
B+	1.35V_VDDQ
	0.675VS
SYSTEM DC/DC	
SY8206DQNC 49	
INPUTS	OUTPUTS
B+	1.05VS
SYSTEM DC/DC	
SY8003DFC 52	
INPUTS	OUTPUTS
B+	1.5VS
SYSTEM DC/DC	
RT8880BGQW 54-55	
INPUTS	OUTPUTS
B+	+VGA_CORE
SYSTEM DC/DC	
SY8003DFC 56	
INPUTS	OUTPUTS
B+	+1.8VS_VGA
SYSTEM DC/DC	
SY8003DFC 57	
INPUTS	OUTPUTS
B+	+0.95VS_VGA

www.laptoprepairsecrets.com

Power ON Sequence

Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Power ON Sequence
Size	C	Document Number	LA-B181P	Rev
Date:	Tuesday, March 25, 2014	Sheet	59	of 62

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	20131030		Delete 1.PQ307 2.charger air line power circuit 3.change AON7506 to SI7716(PQ106) 4.change NDS0610 to LBSS84L 5.change AON7506 to SI7716 6.change 47U 6.3V to 22U 6.3V (PCH8,PCH9) 7.PR9512 mount	1.customer request 2.customer request 3.customer common part 4.compal change 5.customer common part 6.vender reveiw	DB0 DB0 DB0 DB0
2	20131031		1.10U_0805_25V==>2200p_0402_50V not mount(PC160) 2.PC107,PR111,PC121,PC305,PR314 PC313,PC308,PR315,PC312,PCH4,PCZ3,PRZ13,PCZ13 PCZ20,PCZ26,PCW1,PCV4,PRV70,PCV107 3.change 147K_0402_1% to 237K_0402_1% (PRV34) change 560P_0402_50V7K to 470P_0402_50V7 (PCV88) change 10.7K_0402_1% to 22.6K_0402_1%(PRV47) change 9.76K_0402_1% to 5.6K_0402_1%(PRV51) change 15K_0402_1% to 19.1K_0402_1%(PRV55) change 910K_0402_5% to 20.5K_0402_1%(PRV75) change 910k_0402_1% to 910_0402_1%(PRV53) change 3.48K_0402_1% to 3.4K_0402_1%(PRV69) change 910k_0402_1% to 910_0402_1%(PRV77) 4.remove PR9510,PR9512,PR9514,PR9513 5.remove PC318,PRH10,PRW10,PCW13 6. PRH8,PRW8 not mount 7.22u/0805 6.3V to 22u/0603 6.3V PC1504,PC1501 PC1505,PC1802,PC1803,PC1805,PC1806,PC9502,PC9503, PC9505,PC9506,PCH9,PCH10,PCH11,PCH8 8.0.22U_0402_6.3V6K to 0.22U_0603_50V7K (PC128)	1.EMI feedback 2.EMI feedback 3.power vender feedback 4.power change fb sense 5.for compal module design 6.current limit design	DB0 DB0 DB0 DB1 DB1 DB1 DB1 DB1 SI1 SI1 SI1
3	20131101		1.remove PRW11	1.HW request	
4	20131112		1.not mount PRW7 2.change 0_0402_1% to 0_0402_5%(PR1502,PR1804, PR9504,PR9508,PR9511,PR9515)	2.AMD request	
5	20131202		1.not mount PRZ36,PRV32 and PCV86 2.PC128 change 0.22U_0603_25V to 0.22U_0402_6.3V6K 3.add PD16,PRV43 4.add PRV45,PRV48,PCV99 and PRV50	1.PWR request 2.PWR request 3. customer request 4.richtek request	SI1 SI1 SI2 SI2

www.laptoprepairsecrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
				PIR List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Rev 0.5
				Document Number	LA-B181P
				Date:	Tuesday, March 25, 2014
				Sheet	60 of 62

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
6	20131210		add PRV78 1K_0402_1% PRV62 5.76K_0402_1% PRV64 10K_0402_1% PRV80 1K_0402_1% PRV79 10K_0402_1% PRV52 137K_0402_1%	RITCHTEK issue request	DB0 DB0 DB0 DB0
	20131221		PRM2 Change 4.7_1206_5% to 0.1206_5% PCM7 Change 680P_0603_50V7K to 1000P_0603_50V7K PR314 not mount==>mount PC313 not mount==>mount PR315 not mount==>mount PC312 not mount==>mount PCZ13 not mount==>mount PRZ13 not mount==>mount PCZ20 not mount==>mount (28W) PRZ26 not mount==>mount (28W)	EMI request	DB0 DB0 DB0 DB1 DB1
	20131226		PRV31 Change 10_0402_1% to 1_0402_1% PRV34 Change 127K_0402_1% to 84.5K_0402_1% PRV47 Change 22.6K_0402_1% to 7.32K_0402_1% PRV51 Change 5.6K_0402_1% to 12.4K_0402_1% PRV55 Change 19.1K_0402_1% to 14K_0402_1% PRV75 Change 20.5K_0402_1% to 2.8K_0402_1% PRV77 Change 910_0402_1% to 1.3K_0402_1% PRV53 Change 910_0402_1% to 1.3K_0402_1% PC128 Change 0.22U_0603_6.3V to 0.22U_0402_6.3V	RITCHTEK issue request	DB1 DB1 DB1 DB1 SI1
	20140102		PRM2 Change 0.1206_5% to 4.7_1206_5% PCM7 Change 1000P_0603_50V7K to 680P_0603_50V7K PUV1 change RT8880BGQW to RT8880CGQW	EMI request RITCHTEK request	SI1 SI1
	20140103		PR14,PQ2 and PR13 are not mount. PR11 Change 330_0402_1% to 680_0402_1%	Customer request	SI1
	20140106		PRV80 mount==>not mount PRV79 not mount==>mount	RITCHTEK issue request	
	20140213		add PC8,PC9 and PC10 mount PR111,PC121,PC107 and PC129 PC107 2200P_0402_50V7K==>0.022_0402_25V PC129 0.1U_0402_50V7K==>0.022_0402_25V	EMC request EMC request	
	20140214		add PC161 2200P_0402_50V7K not mount	EMC request	SI1 SI1 SI2 SI2

www.laptoprepairsecrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		Deciphered Date		Title		
				PIR List		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number	Rev
					LA-B181P	0.5
				Date:	Tuesday, March 25, 2014	Sheet 61 of 62

ZPL40/50/70 from DB to DB-R LA-B181P REV:0.1 -> 0.3 Modify <2013.11.28 - 2013.12.05>

Rev	Item	Date	Insert	Page	Change Cause	Modify Description
0.2	1	11/28	CKT, LAYOUT	6	-Design issue	-Change RC225 pin 1 connection from +3VS to +3VS
0.2	2	11/28	CKT, LAYOUT	7	-Follow CHICLET	-Move FPM LPC CLK from part 0 to part 1
0.2	3	11/28	CKT	8	-DGPU_PWR_EN voltage level incorrect issue	-Uninstall RC125
0.2	4	11/28	CKT, LAYOUT	9	-DGPU power on sequence	-Change RC118 to 100K and add GC127 to timing delay.
0.2	5	11/28	CKT, LAYOUT	18	-Footprint incorrect issue	-Modify U16 footprint to SC70-5
0.2	6	11/28	CKT, LAYOUT	21	-No used.	-Remove CLK_PCI_DEBURG from JMIN1 pin 19
0.2	7	11/28	CKT	23	-OS3 can't turn on issue	-Uninstall RL26
0.2	8	11/28	CKT	30	-Follow HP BIOS code request	-Uninstall R154
0.2	9	11/28	CKT, LAYOUT	32	-Avoid leakage issue.	-Swap Q88 pin 1 and pin 3
0.2	10	11/28	CKT, LAYOUT	32	-Footprint incorrect issue	-Modify C187 footprint to 0402 package
0.2	11	11/28	CKT, LAYOUT	33	-Design issue	-Swap GPU FREQ RX bus PIN signal and CV1-CV8 change to 0.22u
0.2	12	11/28	CKT, LAYOUT	28	-Current limit	-Add R860
0.2	13	11/29	CKT, LAYOUT	30	-Vendor request	-U13 pin 6 add external 4.7K PU to +3VS, FPM
0.2	14	11/29	CKT	32	-Follow CHICLET	-Change R255, R257, and R493 to 10Kohm -Delete GC12 and add buffer U20 and U21.
0.2	15	12/02	CKT, LAYOUT	6	-Follow CHICLET	OC33 net name from HDA_SDOUT_AUDIO change to HDA_SDOUT
0.2	16	12/02	CKT, LAYOUT	32	-Follow CHICLET	add R101, R102, R108, R105, R106 1. swap Q12 pin 1 and pin 3
0.2	17	12/02	CKT, LAYOUT	23	-leakage issue and FAR suggest	2. Install RL40 3. Reserve 2 resistor (RL48, RL49) connection Q12.2 to +3VS and +LAN_VDD_3V3.
0.2	18	12/02	CKT, LAYOUT	34	-Follow 2013 RRR	-Add D14
0.2	19	12/02	CKT	35	-DGPU power on sequence	-Uninstall RS076, RS074
0.2	20	12/03	CKT, LAYOUT	40	-Follow CHICLET	-change +1.05VS_MODPHY switch circuit

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.2 -> 0.3 Modify <2013.12.04 - 2013.12.17>

0.3	1	12/04	CKT, LAYOUT	29	-Follow 2013 RRR	-update FAN control circuit delete Q4108, RS080 and add U2, C31
0.3	2	12/05	CKT	35	-DGPU power on sequence	-C4816 from 0.01u change to 0.022u
0.3	3	12/05	CKT	9	-DGPU power on sequence	-Change RC121 to 0ohm and uninstall CC127 (BIOS code control timing)
0.3	4	12/05	CKT	10, 33	-For PCB Gen2	-change C268, C269, C281, C282, C283, C284, C286, C286, CV1, CV2, CV3, CV4, CV5, CV6, CV7, CV8 from 0.22u to 0.1u
0.3	5	12/06	CKT	12	-Follow CHICLET	-Change RC174 from 5.11ohm to 0ohm
0.3	6	12/06	CKT	11	-Follow INTEL schematic	-Change RC156 from 110ohm to 33ohm install
0.3	7	12/06	CKT, LAYOUT	29	-Platform ID identify	-add R82, R86
0.3	8	12/06	CKT, LAYOUT	32	-	-reserve R136, R137 co-lay with U20, U21
0.3	9	12/06	CKT, LAYOUT	40	-	-reserve R135 co-lay with Q185
0.3	10	12/09	CKT, LAYOUT	43	-No leakage issue	-remove Q57
0.3	11	12/09	CKT	26	-Follow CHICLET	-R436 from 220hm change to 33ohm
0.3	12	12/09	CKT, LAYOUT	17	-Follow INTEL schematic	-install Q267, C267, C264, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.3	13	12/09	CKT, LAYOUT	11	-Follow INTEL schematic	-Re-placement RC154
0.3	14	12/09	CKT, LAYOUT	12	-Follow INTEL schematic	-Add RC183, CC47, RC189, CC75
0.3	15	12/10	CKT, LAYOUT	10	-For WWAN, Touch share USB port	-Add R138, R139
0.3	16	12/10	CKT, LAYOUT	4	-Follow CHICLET	-Add C32
0.3	17	12/11	CKT, LAYOUT	6	-Follow INTEL schematic	-reserve RC130
0.3	18	12/11	CKT, LAYOUT	21	-solve SIM card can't detect issue	-delete RS079, Q4107 and add C2
0.3	19	12/13	CKT, LAYOUT	9	-Follow Rant	-R103 change to test point T184
0.3	20	12/13	CKT	8	-solve DGPU power issue	-install RC125
0.3	21	12/13	CKT, LAYOUT	21	-Follow Rant	-Q81, Q4113 from two angle MOS change to dual MOS (Q90)
0.3	22	12/13	CKT, LAYOUT	22	-QDD power issue	-Add Q63
0.3	23	12/13	CKT, LAYOUT	23	-LAN power issue	-delete JHW1, RL26
0.3	24	12/13	CKT, LAYOUT	21	-no need	-delete R205, C292
0.3	25	12/13	CKT	25	-For V drop test	-C1512 from 100u change to 150u
0.3	26	12/13	CKT, LAYOUT	9	-hp request	-QDD, Q488 from GPIO14 change to GPIO3
0.3	27	12/13	CKT, LAYOUT	21	-For GPIO initial status	-add R91
0.3	28	12/14	CKT, LAYOUT	12	-solve power ripple	-add CC77, CC79, CC79
0.3	29	12/16	CKT, LAYOUT	9	-reserve for MBHY sequence	-add RC377

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.3 -> 0.4 Modify <2013.12.18 - 2013.12.25>

0.4	1	12/20	CKT	9	-Follow HP request	-install RC272, RC273
0.4	2	12/20	CKT, LAYOUT	15	-Follow Intel PDG	-Remove RD26, install RD21
0.4	3	12/20	CKT, LAYOUT	16	-Follow Intel PDG	-Uninstall CD32, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.4	4	12/20	CKT, LAYOUT	19	-Follow Vendor request	-Reserve R65
0.4	5	12/20	CKT	19	-Follow HP request	-Change R82, R86 to 0 ohm
0.4	6	12/20	CKT	20	-Follow Intel PDG	-Change RFP3 and RFP4 to 470 ohm
0.4	7	12/20	CKT	21	-Compal Request	-install R91
0.4	8	12/20	CKT, LAYOUT	22	-Customer modify GPIO table	-Remove Q84, R842, Change JQ501 pin 11 netname to QDD_D4H
0.4	9	12/20	CKT	23	-Prepare leakage issue when S3, S5	-Uninstall RL40, RL42, RL48, RL48 install RL34
0.4	10	12/20	CKT	24	-Vendor Request	-Reserve RA40, UA101 pin 37 add RT57 10K PU to +5VS
0.4	11	12/20	CKT	31	-Vendor Request	-Remove R1363, R1365, R1367, C421, C423, C414, L31, L32, L34, R1364, R1366, and R1368. Modify CRT pi filter
0.4	12	12/20	CKT, LAYOUT	40	-Follow Compal common design	-Modify MBHY Power circuit
0.4	13	12/23	CKT, LAYOUT	30	-Follow RF team request	-install C80, C566, C91, C568 -Reserve C90, C564, C91, C565, C92, C566, C93, C567, C95, C569, C110, C579, C111, C579, C108, C576, C82, C559, C83, C560, C84, C561, C86, C565, C89, C563, C94, C568, C96, C571, C112, C580, C109, C977, C106, C374, C97, C572, C105, C573, C130, C581, C131, C582, C132, C583, C133, C584, C134, C585, C135, C586, C136, C587, C137, C588, C138, C589
0.4	14	12/24	CKT, LAYOUT		-Follow ESD team request	-install C113, C129 -Reserve C114, C115, C116, C121, C123, C124, C126, C129

ZPL40/50/70 from SI to PV-1 LA-B181P REV:0.3 -> 0.4 Modify <2014.02.05-2014.>

0.5	1	02/05	CKT	21	-OSable pull high	-RNX change to 8
0.5	2	02/05	CKT	18, 19	-For LVDS SKU	-R163, R63 change to LVDS@
0.5	3	02/05	CKT	19	-For eDP SKU	-R172 change to eDP@
0.5	4	02/05	CKT	19	-For Lid Switch issue	-R166, R175 change to 3.3K
0.5	5	02/05	CKT, LAYOUT	22	-For QDD issue	-add R468, reserve C151 -1. QAZ, QAZ3 combine to dual mos QAZA, QAZB 2. Q91, Q182 combine to dual mos Q91A, Q91B 3. Q86, Q87 combine to dual mos Q86A, Q86B 4. Q63 change to Q63A, Q63B 5. Q412, Q4114 combine to dual mos Q4112A, Q4112B -add D15 and move RS075, C4819 -add C594, C595, C596 -Move U4101 circuit close to JCRT -modify U44 circuit -RS094 from 3.25k change to 0ohm
0.5	6	02/05	CKT, LAYOUT			-add C139, C140, C421 -1. FPR, OFF from GPIO11 change to GPIO65 2. change JAUDD1.16 from +3V_PCH to +3VS 3. disconnect EC pin125 and CPU pin45 rename EC pin125 "PCH_PCIE_WAKEB" to "EC_GPIO25" and add R249 pull up to +3VDS 4. RW13 un-install 5. connector EC pin103 to JMIN1 pin1 (WLAN_WAKEB), JMIN2 pin15 change to NC 6. connector EC pin105 to CPU pin45 (PCH_PCIE_WAKEB) 7. change R93 pull up power rail from +3VS_WLAN to +3VDS and install RN3 8. add JP4102 between +3VDS and +3V_WWAN
0.5	7	02/10	CKT, LAYOUT	25	-For GPU Power Sequence	
0.5	8	02/10	CKT, LAYOUT	38	-Follow ESD team request	
0.5	9	02/10	LA YOUT	31		
0.5	10	02/11	CKT, LAYOUT	40	-SL559M1420VTR is single source issue	
0.5	11	02/12	CKT	30		
0.5	12	02/13	CKT, LAYOUT	11, 19	-Follow RF team request	