LCFC Confidential

Y530 M/B Schematics Document

Coffee Lake H-Processor with DDR4 + NV N17P-G0/G1 GPU

XXXXX

2017-09-11

REV:0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Cover Page			
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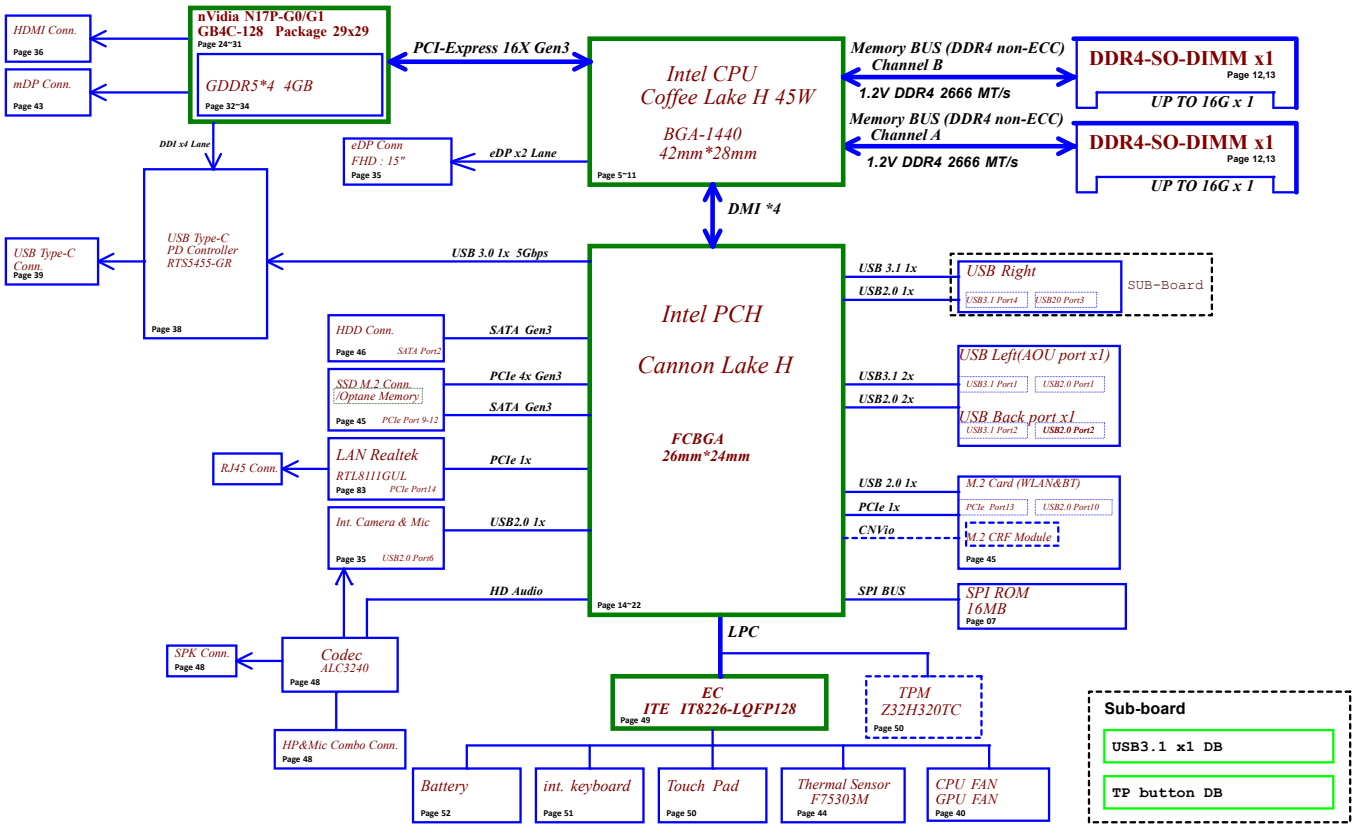

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Title	Block Diagram		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD NVVDDS +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
AOAC@	AOAC support part
CNVI@	CNVi support part
ME@	ME part(connector, hole)
OPT@	For NV GPU part
OPTANE@	Optane memory support part
TPM@	For support TPM sku part
CD@	Cost down part

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	NA
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	M.2 SSD Gen3
1B	NA
2	HDD Gen3
3	NA
4	NA
5	NA

PCIE Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15:24	NA

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Title: **Notes List**

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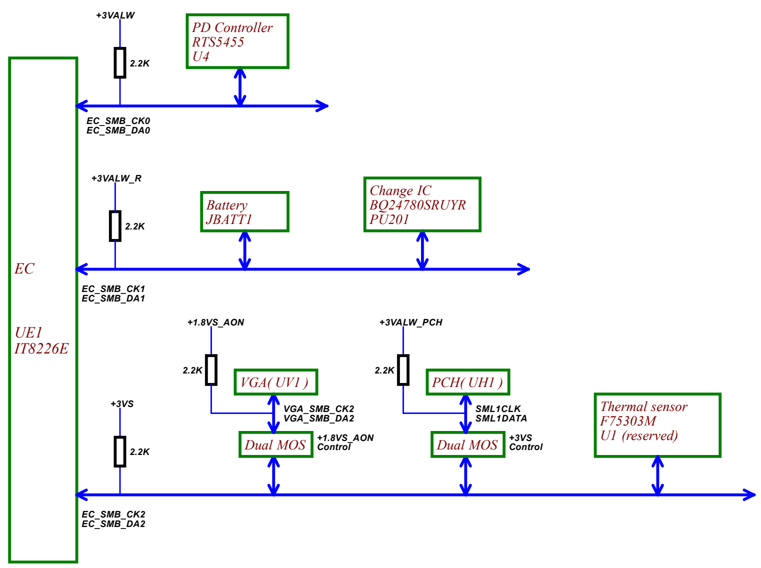

SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS Reserve	X	V +3VALW_PCH	V +3VS	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update

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Title: Blank4

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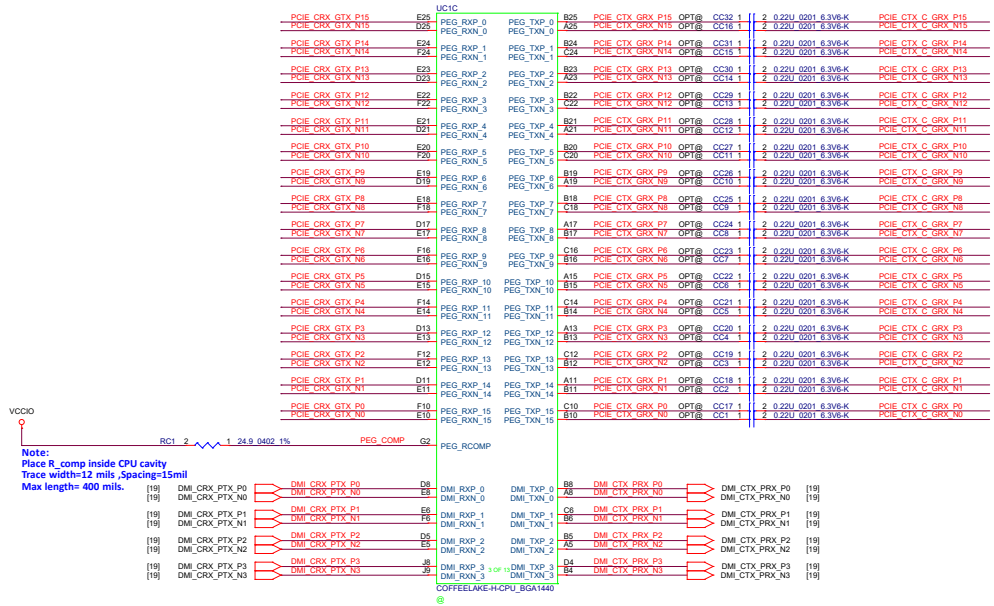
[24] PCIE_CRX_GTX_N[0..15]

[24] PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] [24]

PCIE_CTX_C_GRX_P[0..15] [24]



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Title: **CPU (1/7) DMI,PEG**

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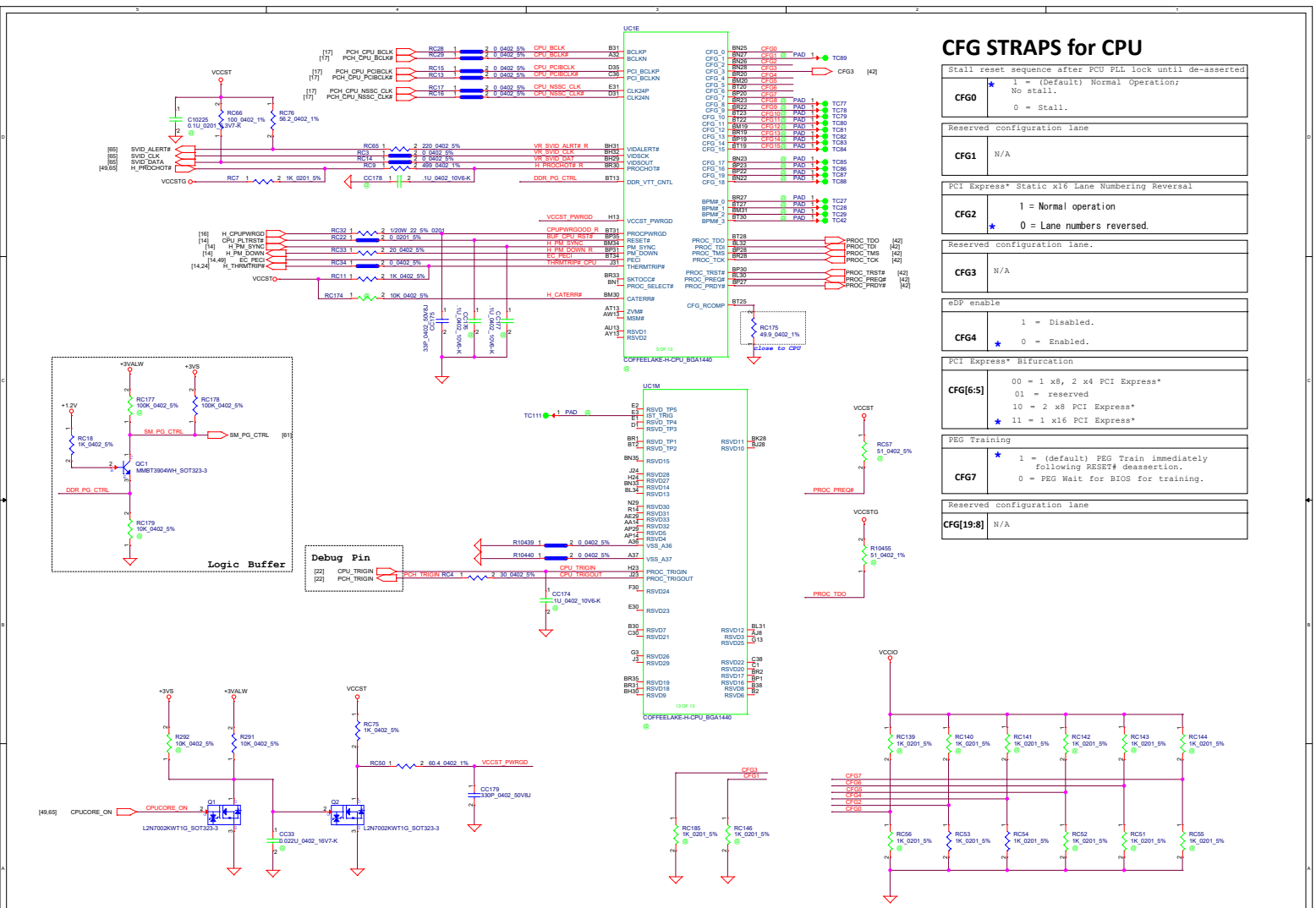

CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	★ 1 = (Default) Normal Operation; No stall. 0 = Stall.

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. ★ 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* ★ 11 = 1 x16 PCI Express*

PEG Training	
CFG7	★ 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS training.

Reserved configuration lane	
CFG[19:8]	N/A

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Title: CPU (2/7) PM, XDP, CLK, CFG

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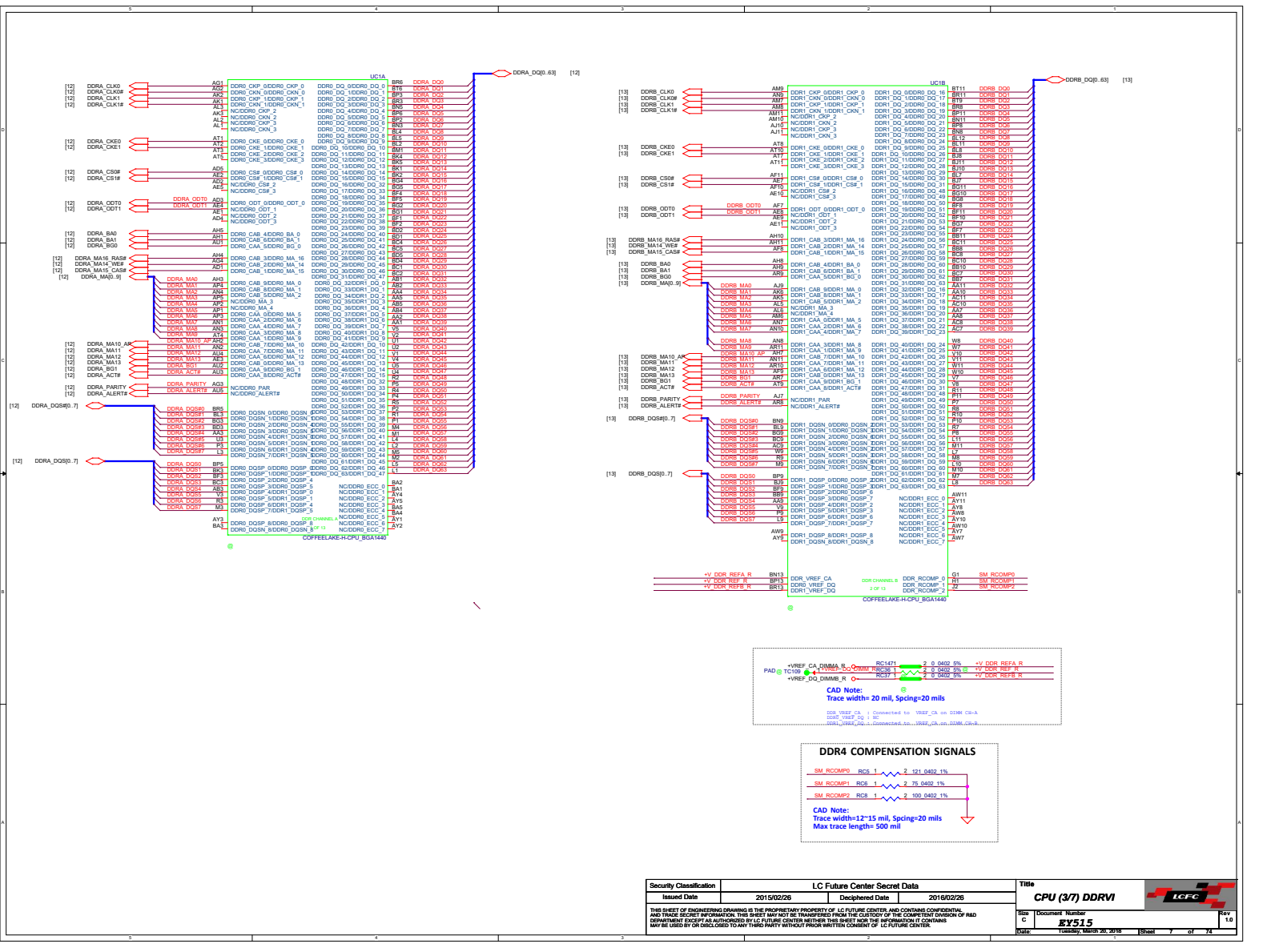

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Title: CPU (3/7) DDRVI

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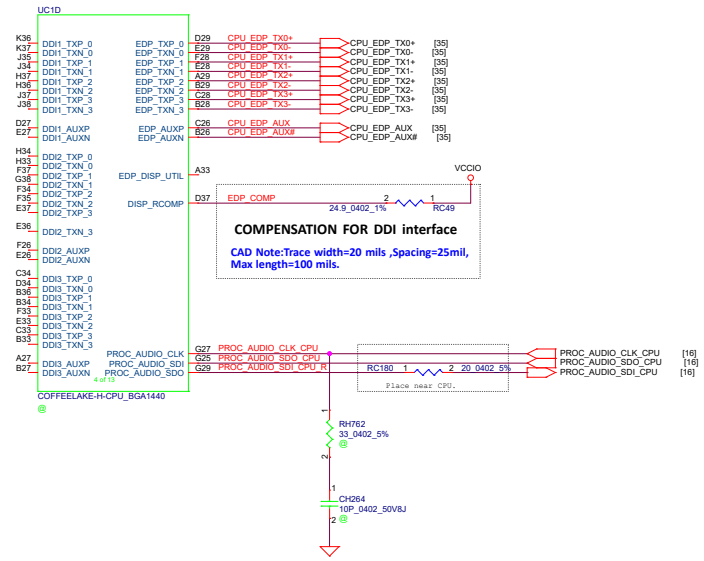

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Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
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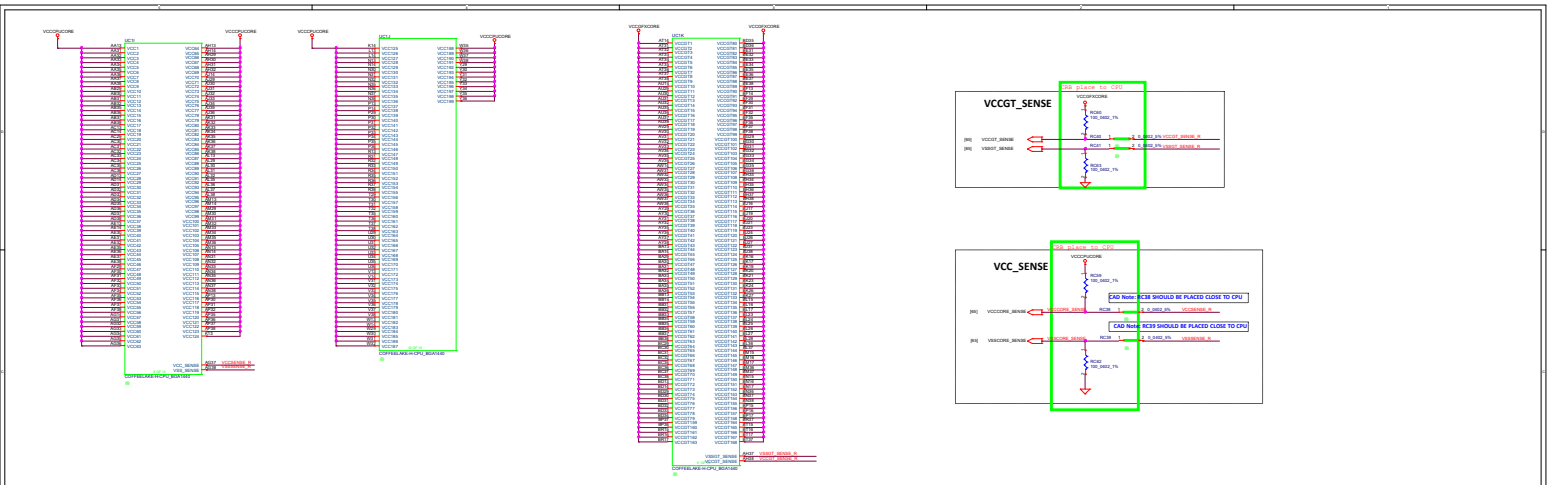

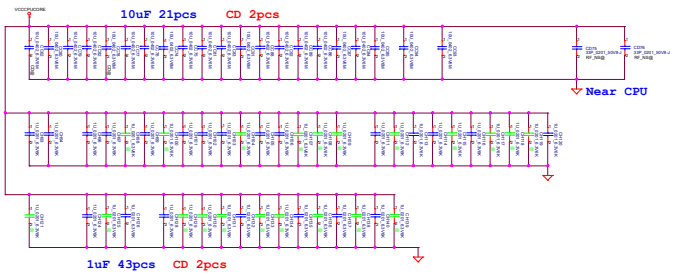

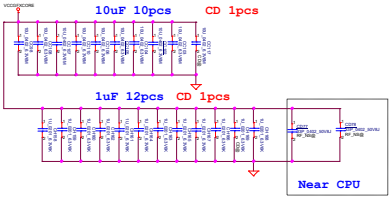

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Title: CPU (5/7) PWR, BYPASS

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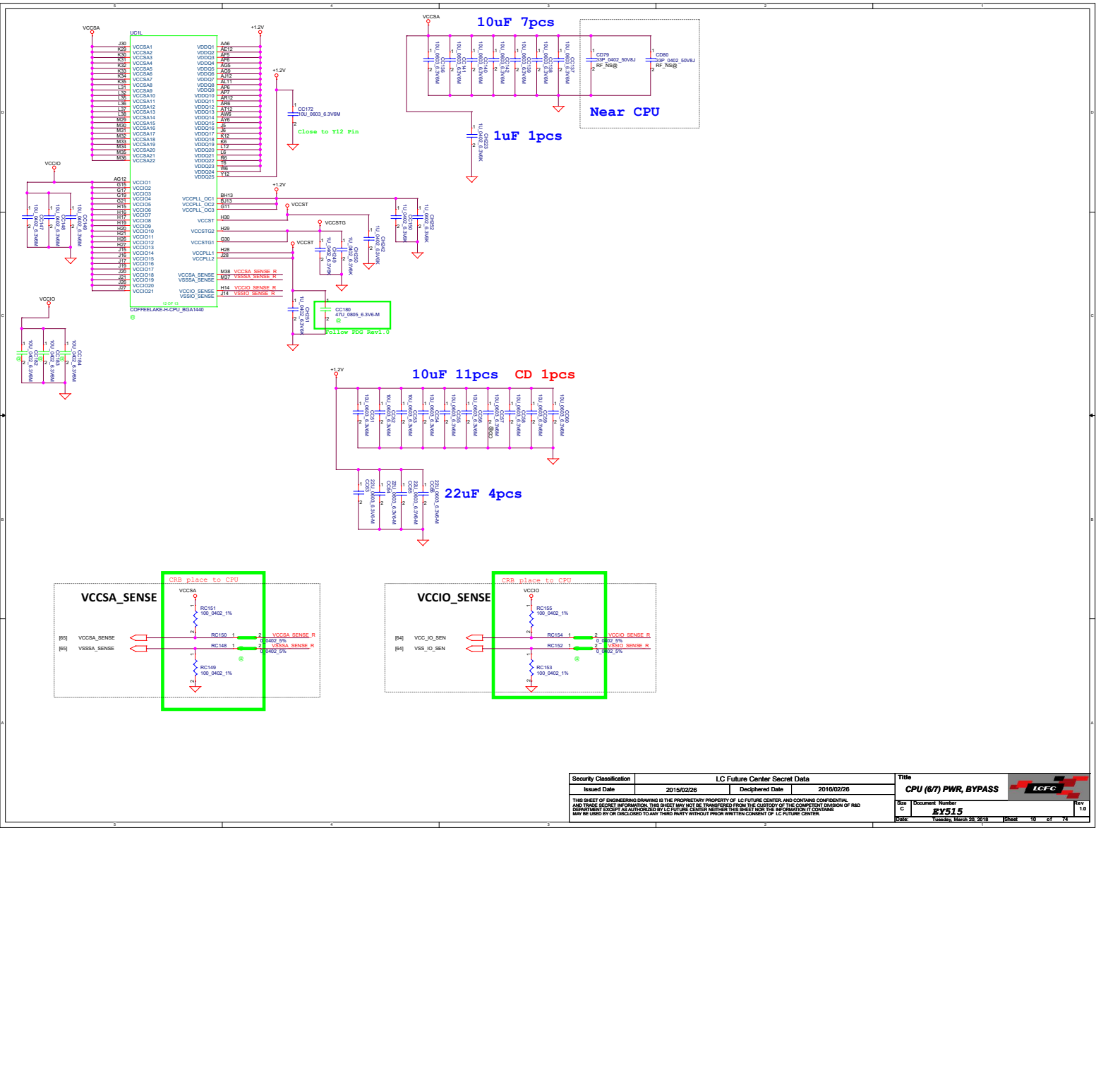

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Title: CPU (6/7) PWR, BYPASS

Size: C | Document Number: EY515 | Rev: 1.0

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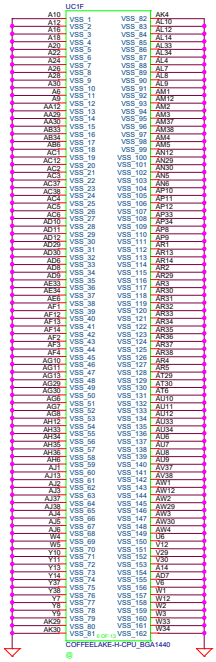

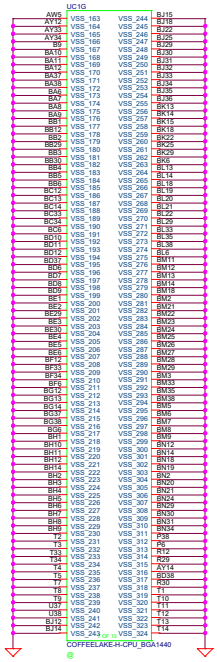

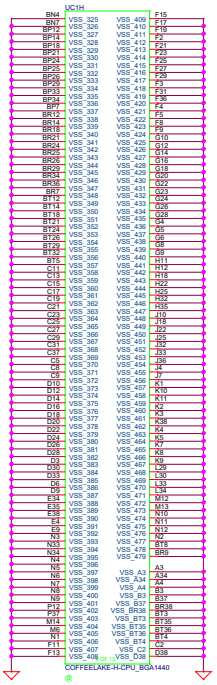

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Title: CPU (6/7) PWR, VSS

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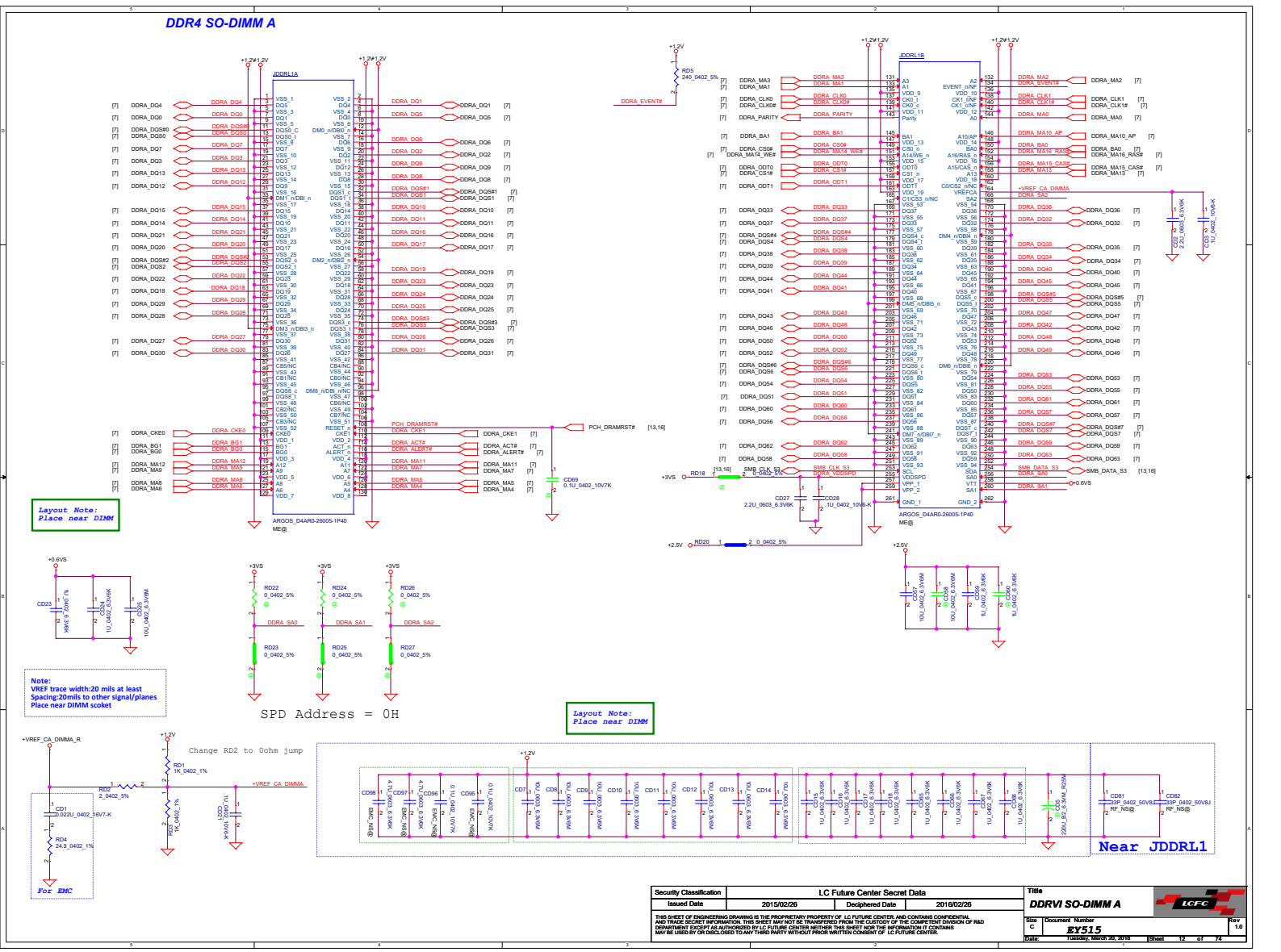

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Title: DDRVI SO-DIMM A

Size: C | Document Number: EY515 | Rev: 1.0

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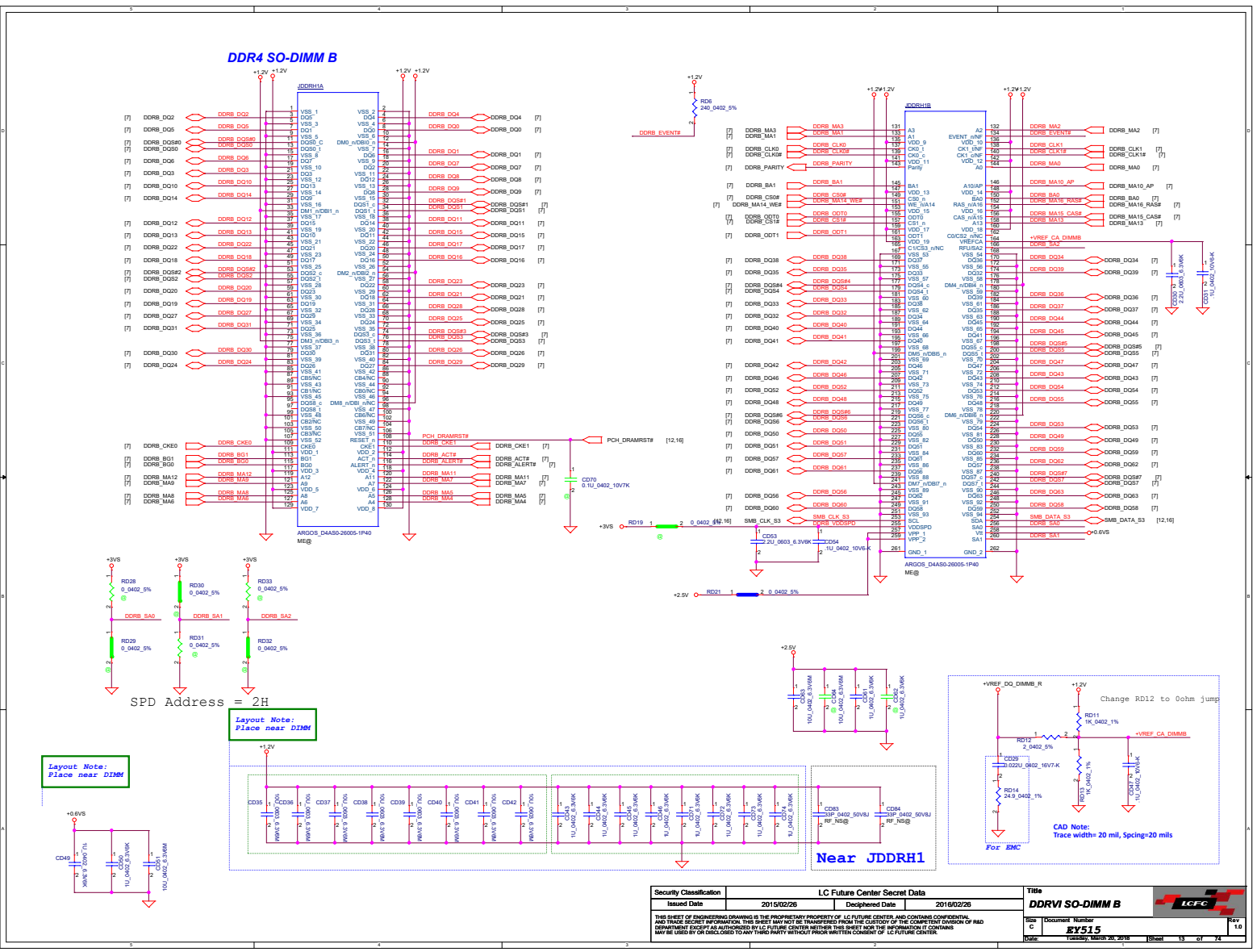

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Size	Document Number		Rev
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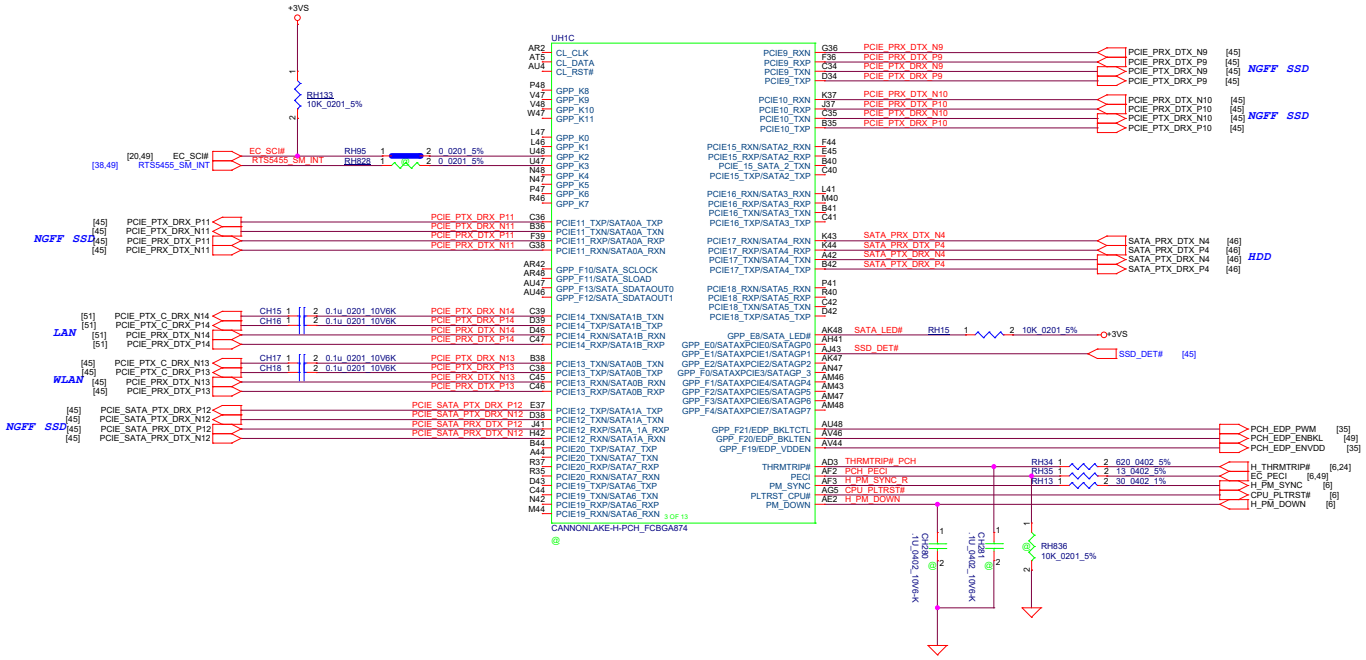

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Title: PCH (1/9) PCIe/SATA/GPPFG

Size	Document Number	Rev
A3	EY515	1.0

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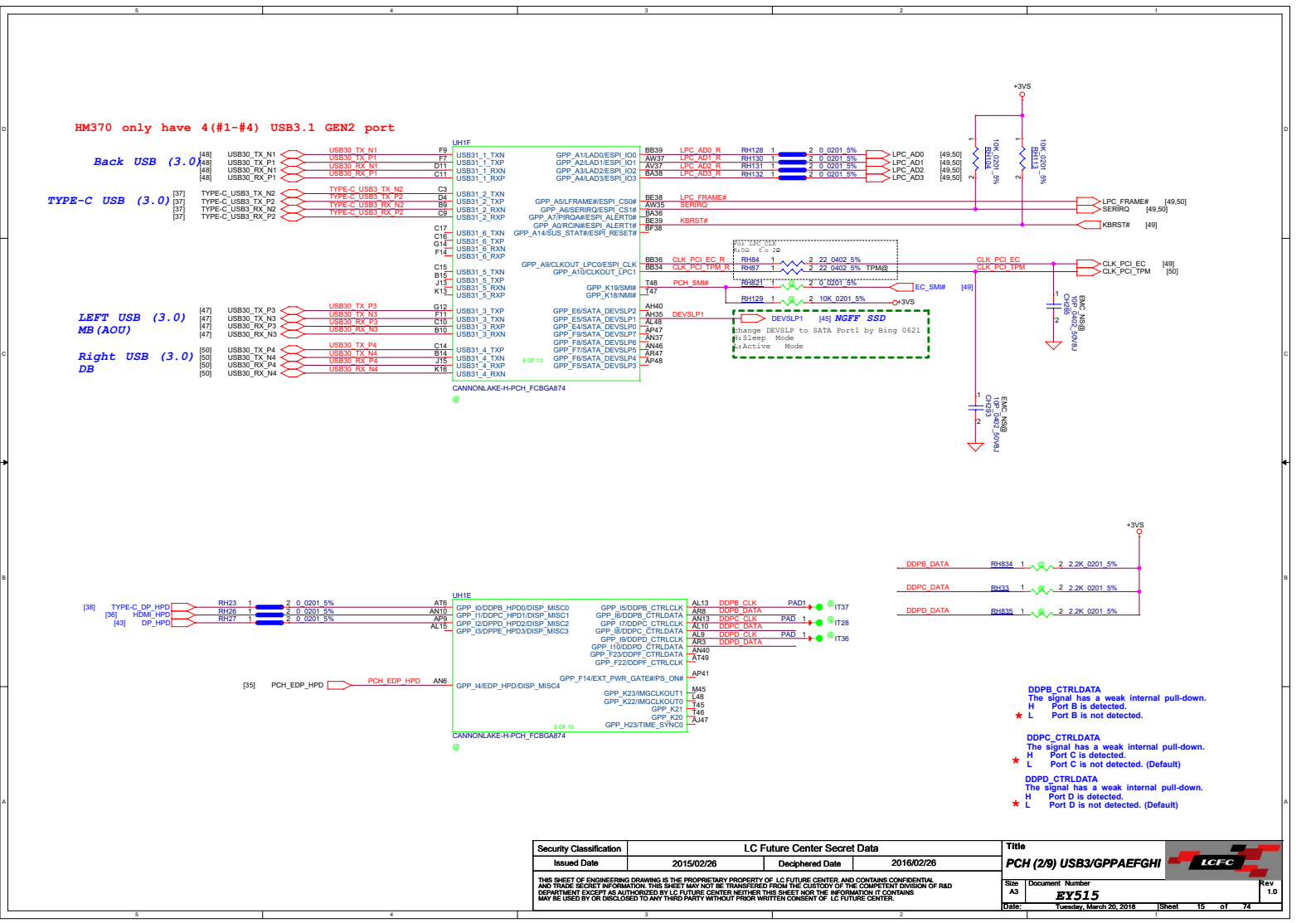

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Title: PCH (2/9) USB3/GPPAEFGHI

Size	Document Number	Rev
A3	EY515	1.0

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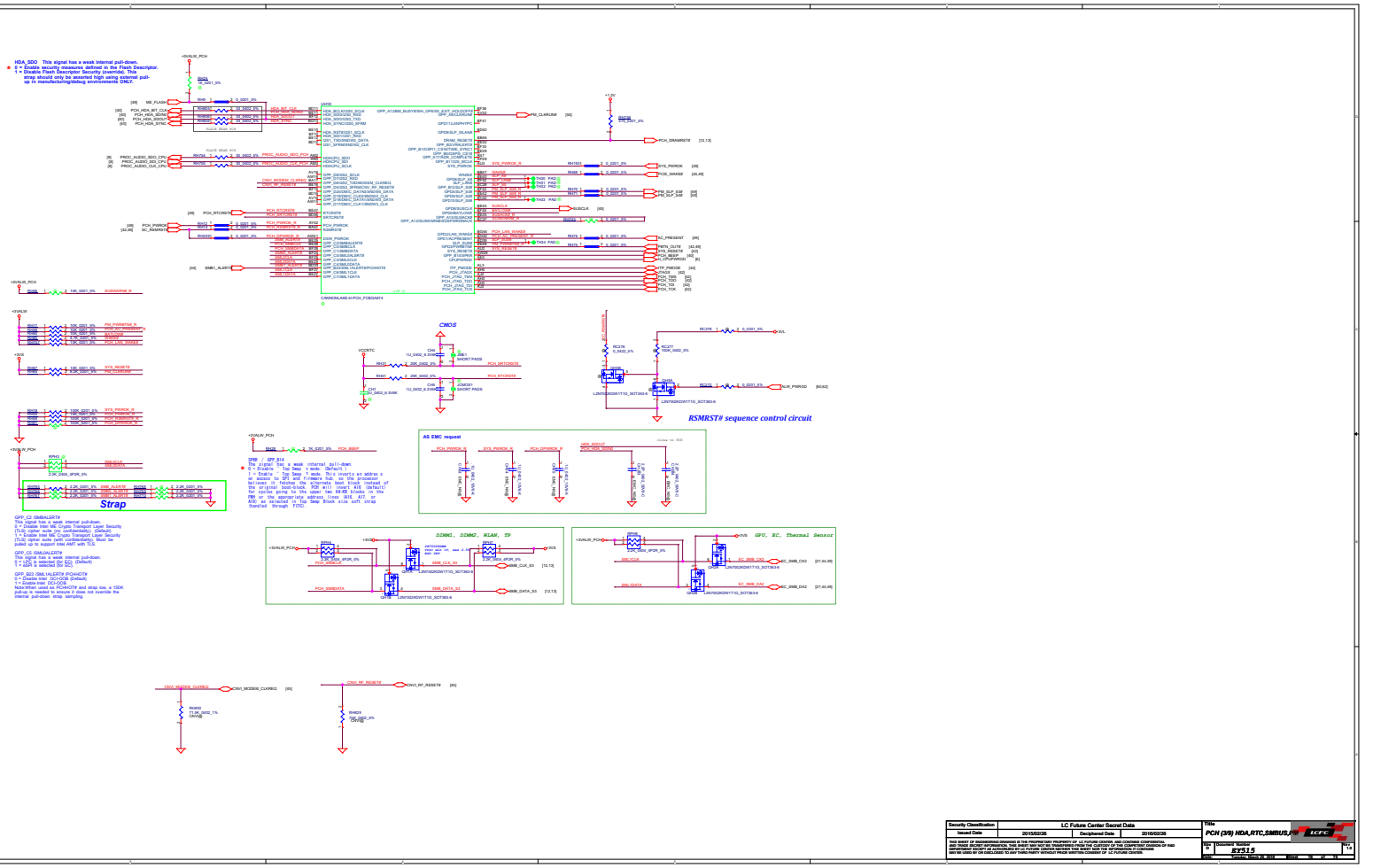

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Title	
	PCH (3/9) HDA,RTC,SMBUS,FWH
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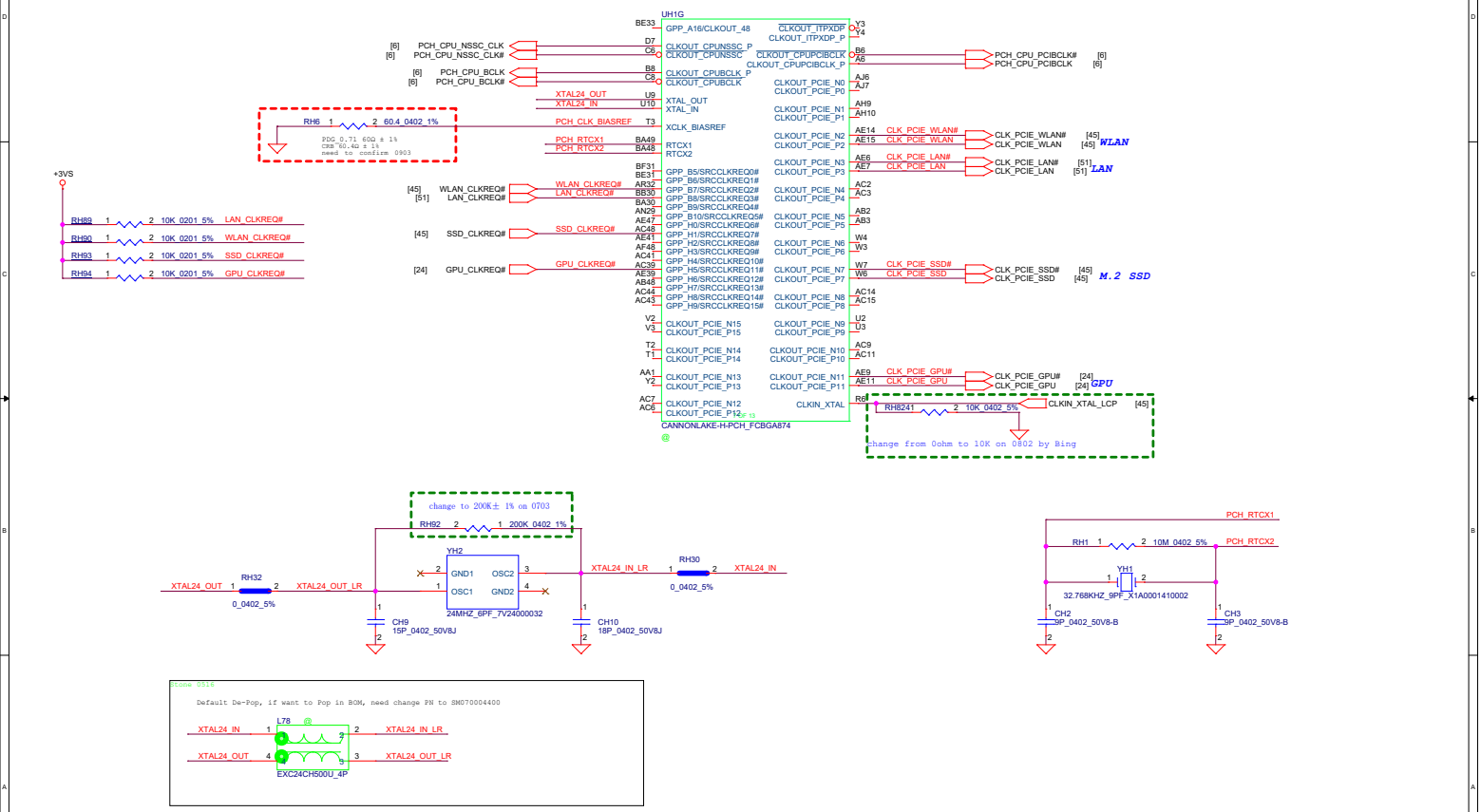

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Title	PCH (3/9) CLOCK,GPPBH		
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A3	EY515		1.0
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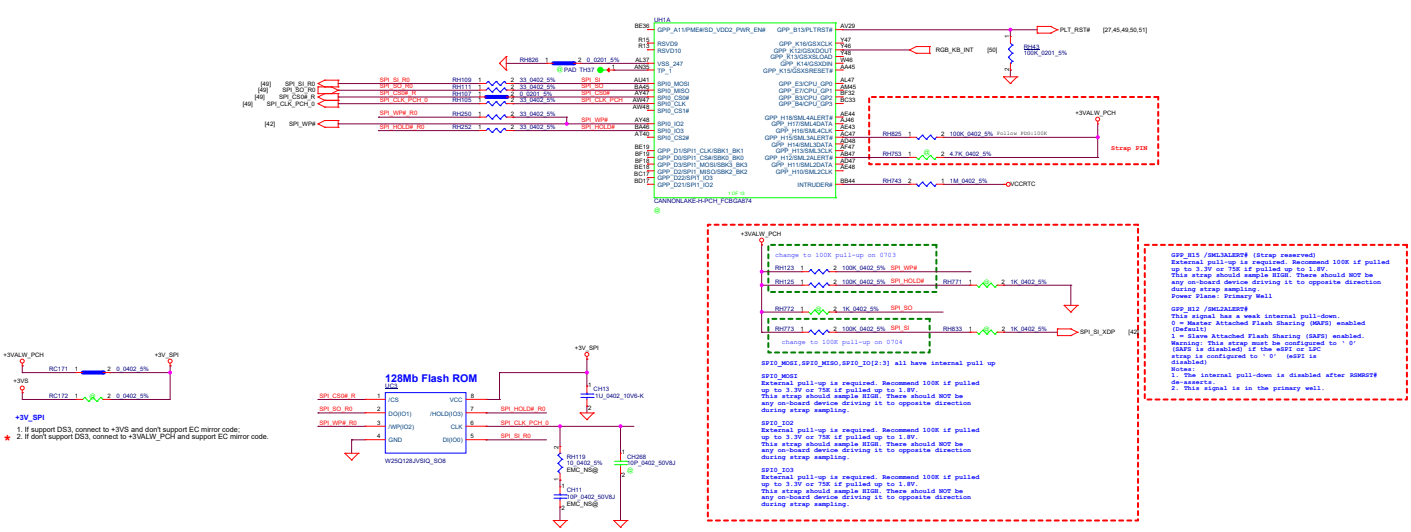

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Title: PCH (5/9) SPI,SMBUS,GPPBEGH

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A2	BY515	1.0

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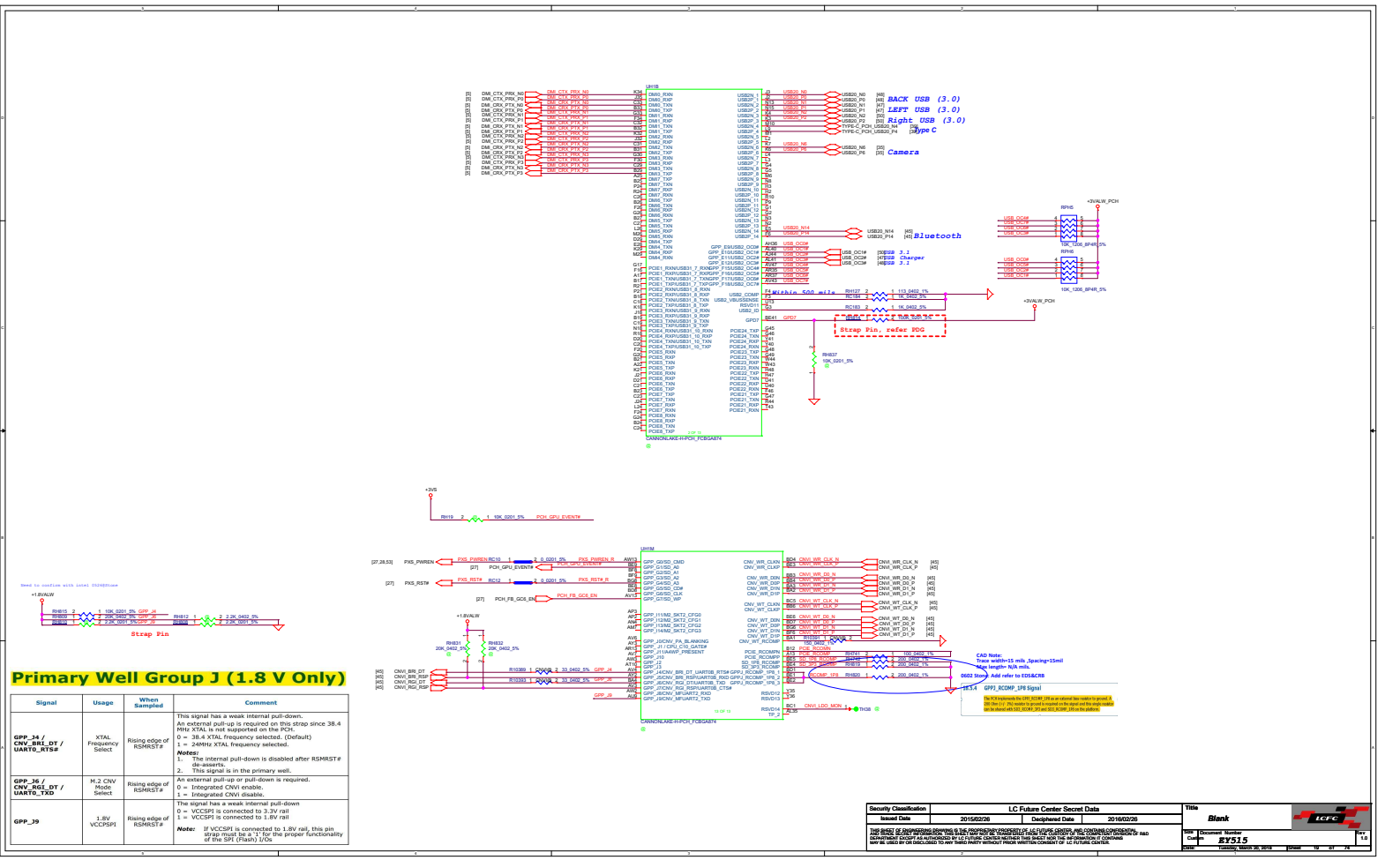

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

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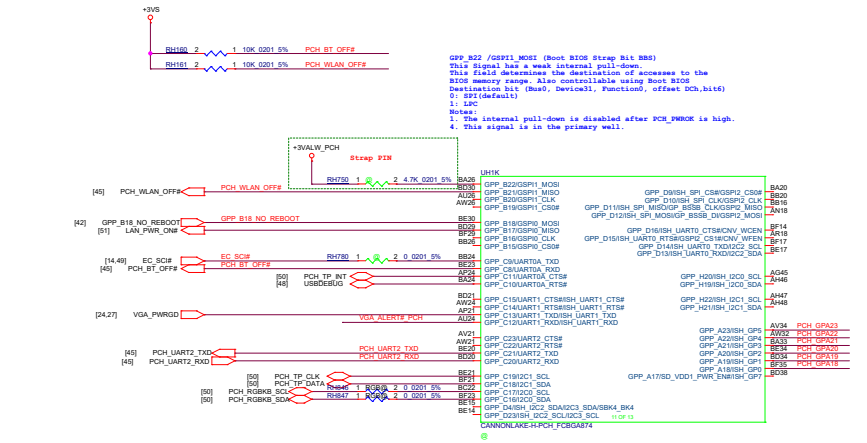
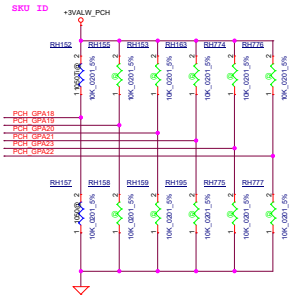
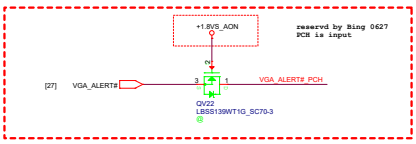


Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC





Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22	PCH_GPA23
1050	0	X	X	X	X	X
1050Ti	1	X	X	X	X	X
1160	X	0	X	X	X	X
KB BL	X	X	1	X	X	X
NO KB BL	X	X	0	X	X	X
PCIE SSD	X	X	X	1	X	X
Optane memory	X	X	X	0	X	X

Title: PCH (6/9) GPPPABCD, I2C

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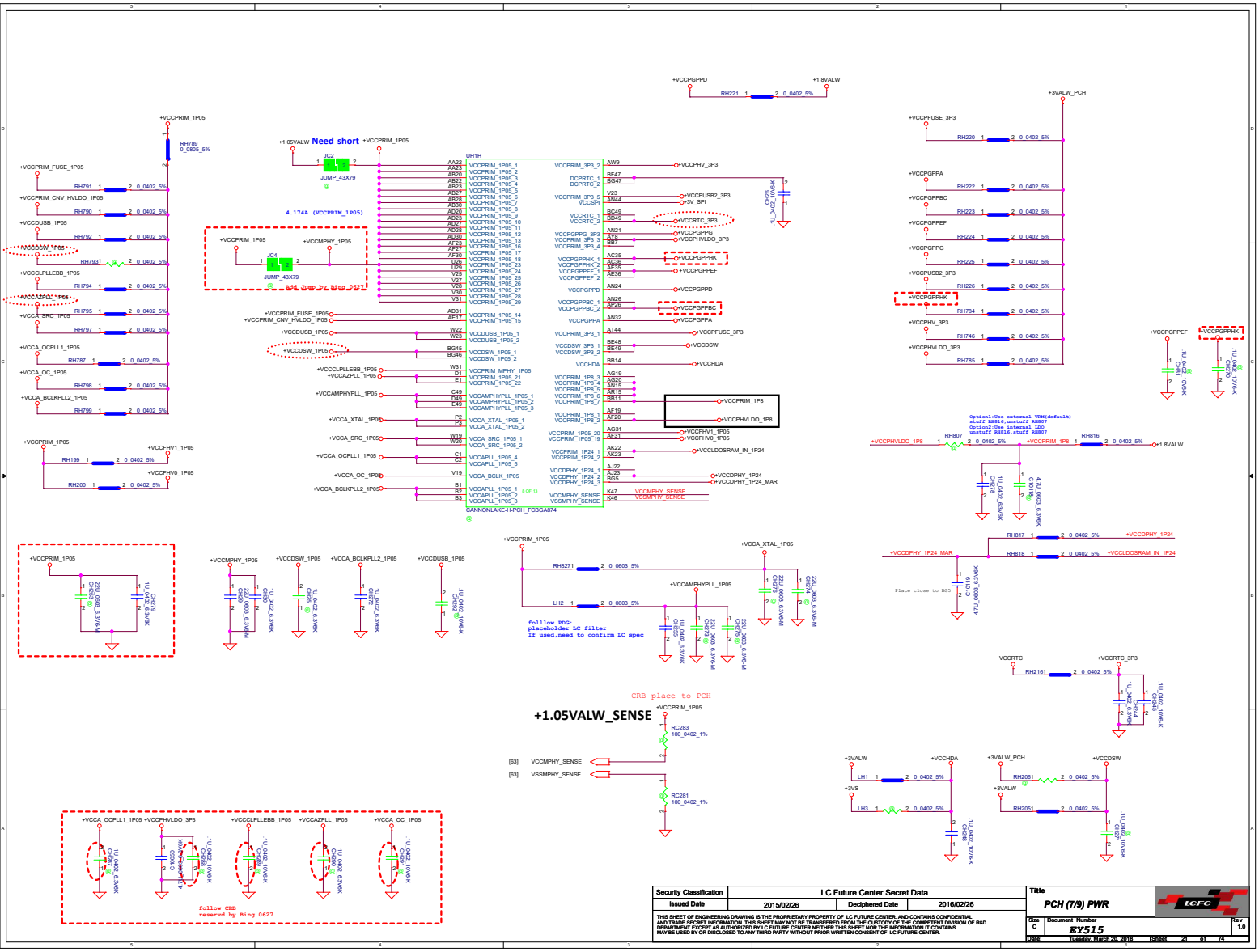

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Title: PCH (7/9) PWR

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C	EY515	1.0

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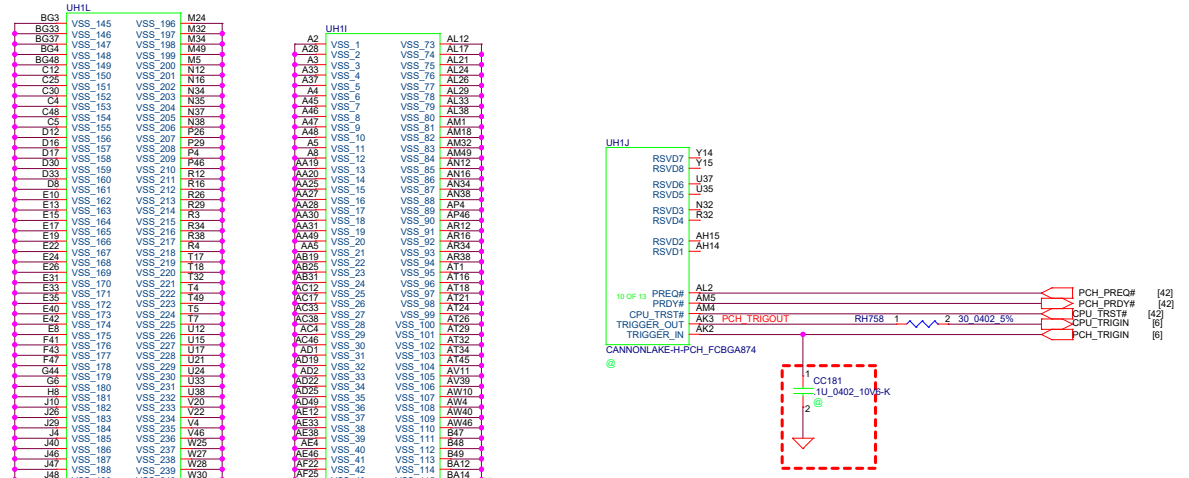

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Title: **PCH (9/9) VSS**

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N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE
SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

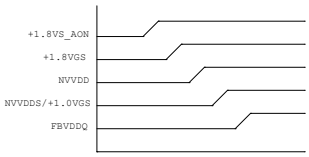
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence

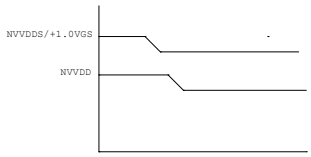


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

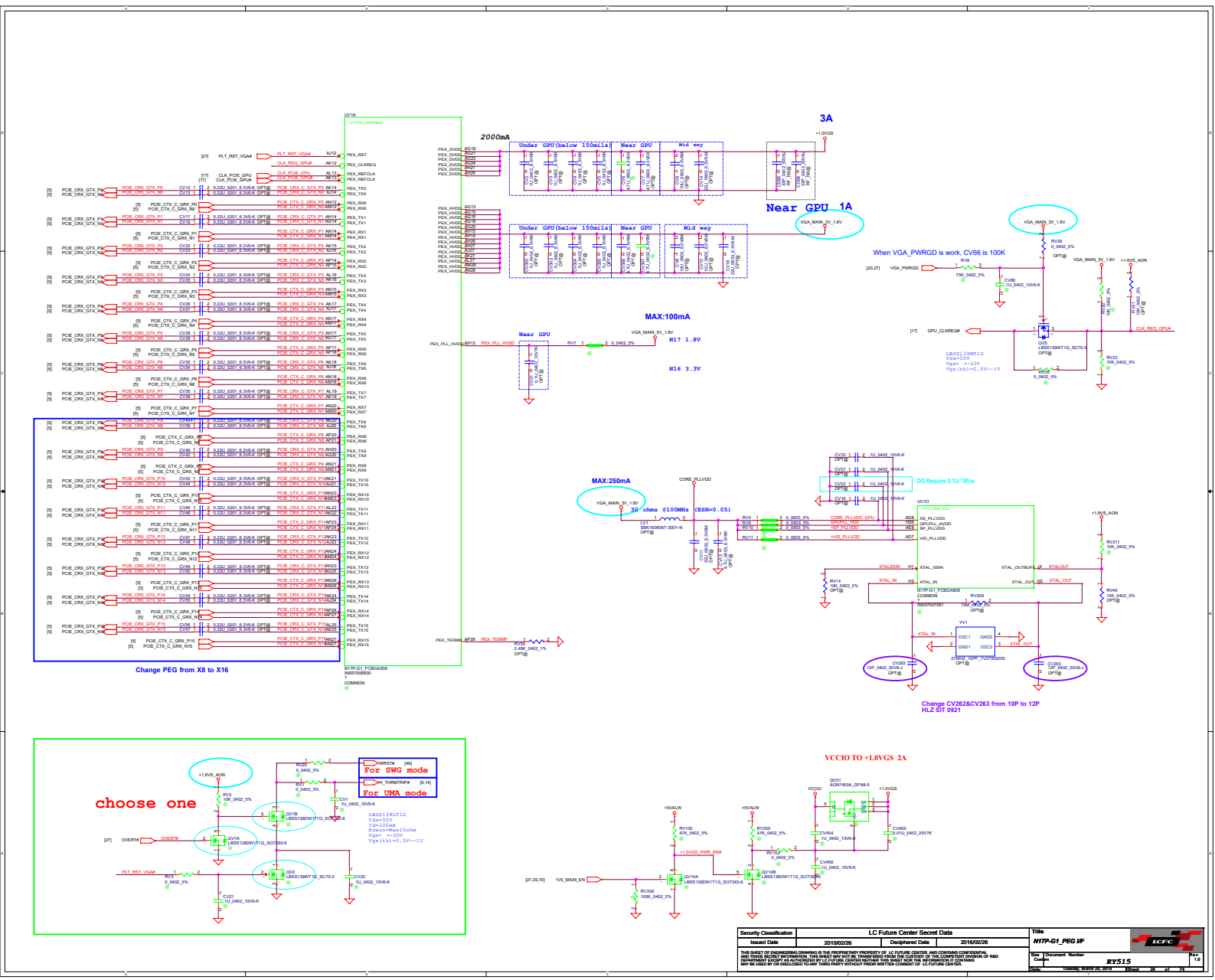
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: VGA Notes List

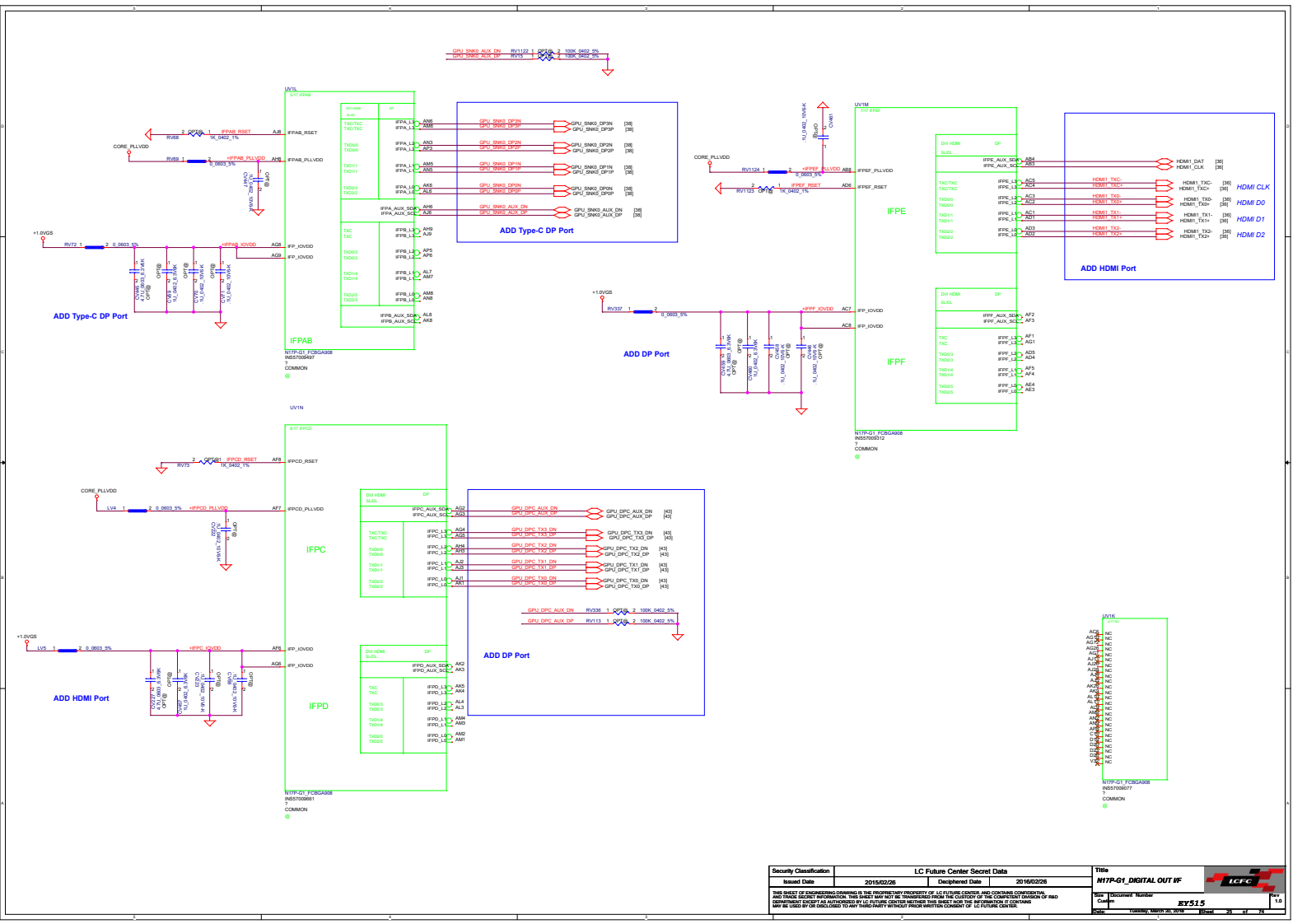
Size	Document Number	Rev
C	EX515	1.0

Date: Tuesday, March 20, 2018 Sheet 23 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N17P-G1_PEG I/F		
Size	Document Number		Rev
Custom		EY515	1.0
Date:	Tuesday, March 08, 2016	Sheet	24 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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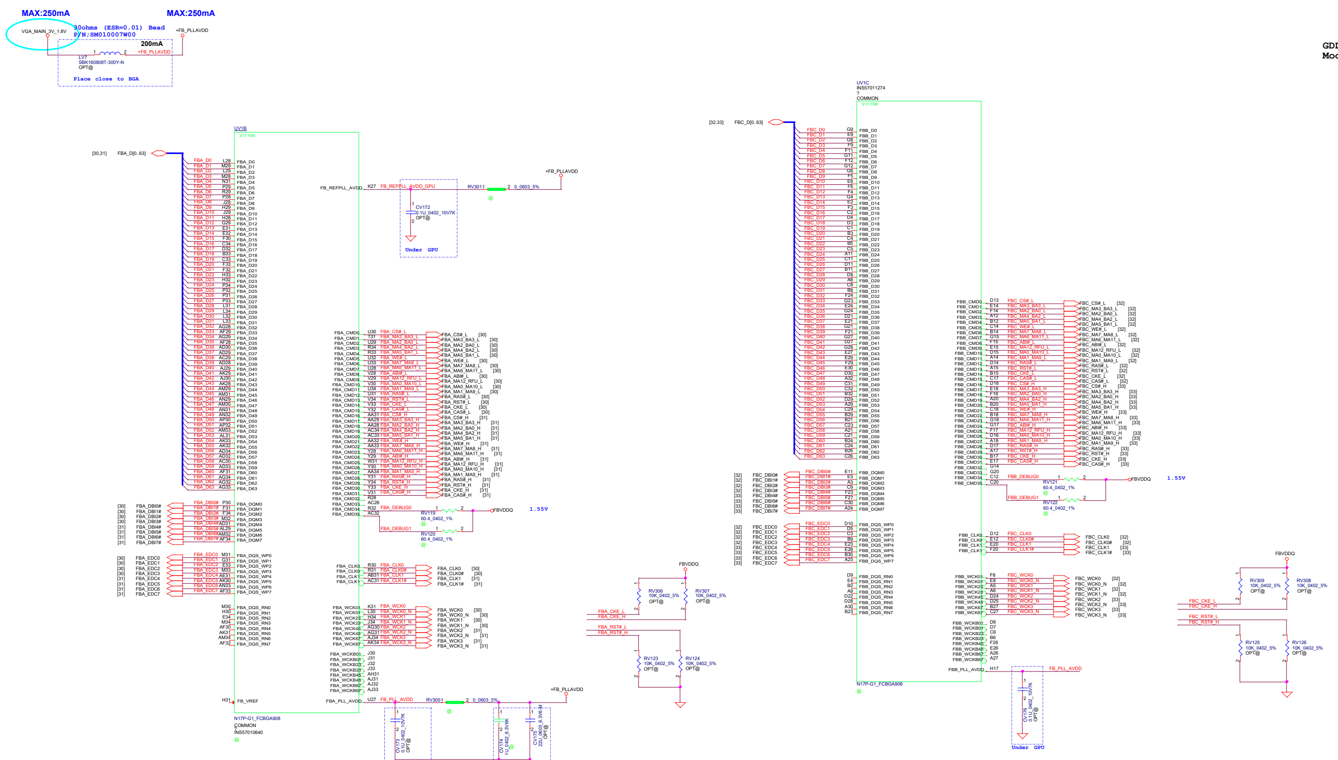
Title: N17P-G1_DIGITAL OUT I/F

Size	Document Number	Rev
Custom	EY515	1.0

Date: Tuesday, March 29, 2016 Sheet 25 of 74

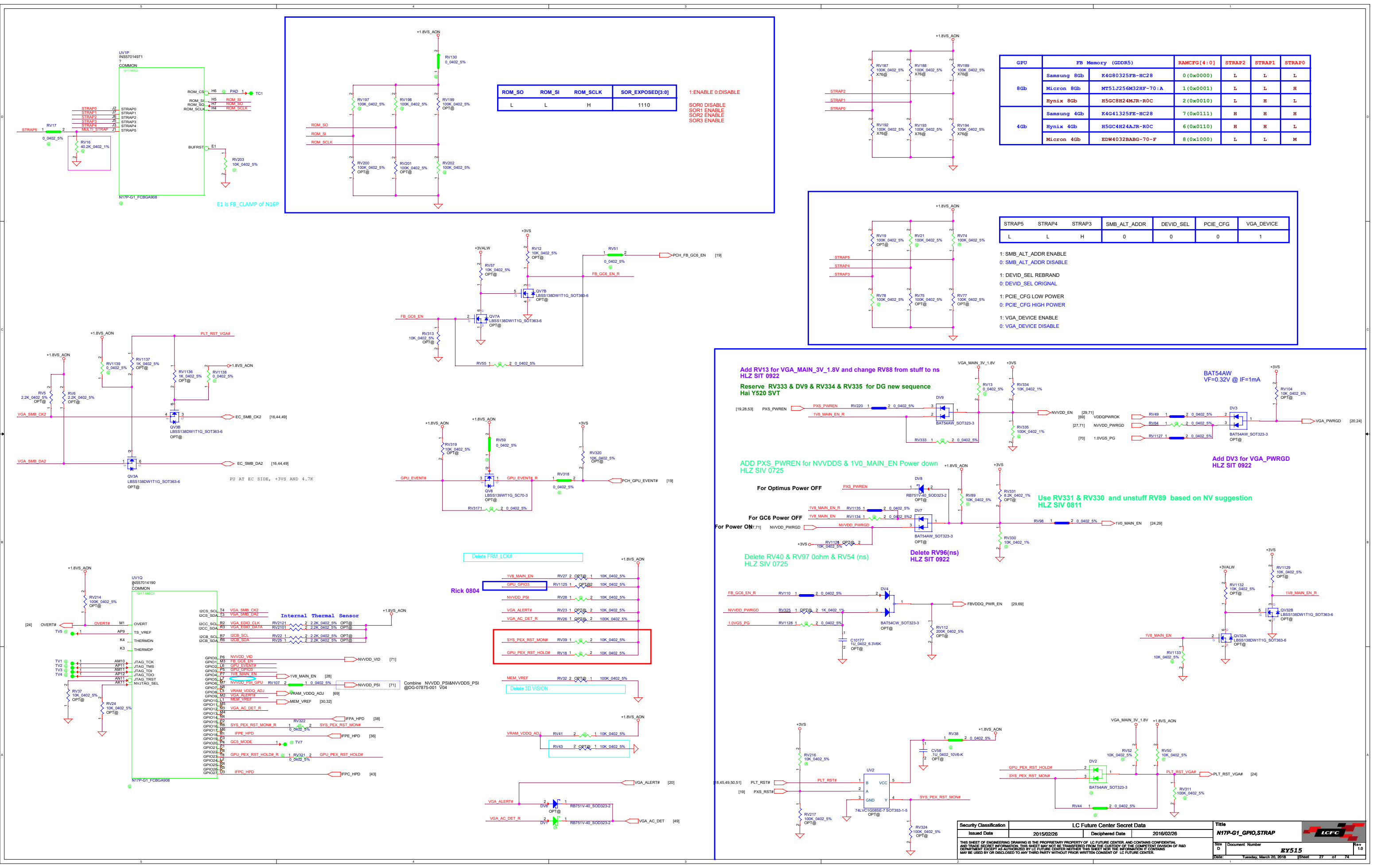


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N17P-G1_VRAM I/F
Size: Custom — Document Number: EY515 — Rev: 1.0
Date: Tuesday, March 20, 2018


E1 is FB_CLAMP of N16P
Internal Thermal Sensor
Rick 0804
Delete FRM_LCK#
Delete 3D-VISION
Combine NVVDD_PSI&NVVDDS_PSI @DG-07875-001 V04
PU AT EC SIDE, +3VS AND 4.7K
Add RV13 for VGA_MAIN_3V_1.8V and change RV88 from stuff to ns
HLZ SIT 0922
Reserve RV333 & DV9 & RV334 & RV335 for DG new sequence
Hai Y520 SVT
BAT54AW
VF=0.32V @ IF=1mA
Add DV3 for VGA_PWRGD
HLZ SIT 0922
ADD PXS_PWREN for NVVDDS & 1V0_MAIN_EN Power down
HLZ SIV 0725
For Optimus Power OFF
For GC6 Power OFF
For Power ON
Use RV331 & RV330 and unstuff RV89 based on NV suggestion
HLZ SIV 0811
Delete RV40 & RV97 0ohm & RV54 (ns)
HLZ SIV 0725
Delete RV96(ns)
HLZ SIT 0922

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	H	1110

1:ENABLE 0:DISABLE

SOR0 DISABLE
SOR1 ENABLE
SOR2 ENABLE
SOR3 ENABLE

GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L
4Gb	Samsung 4Gb	K4G41325FE-HC28	7(0x0111)	H	H	H
	Hynix 4Gb	H5GC4H24AJR-R0C	6(0x0110)	H	H	L
	Micron 4Gb	EDW4032BABG-70-F	8(0x1000)	L	L	M

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

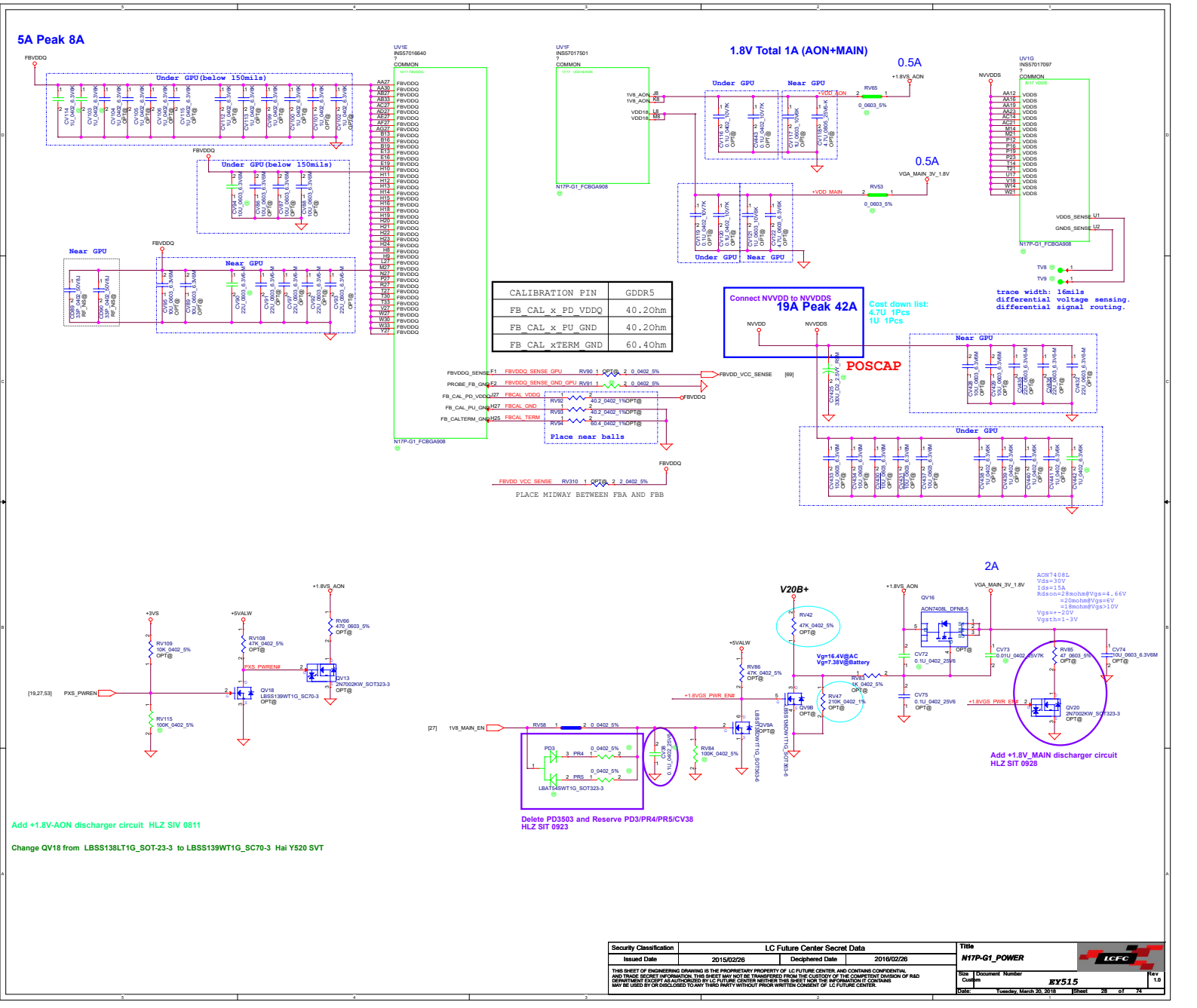
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N17P-G1_GPIO,STRAP

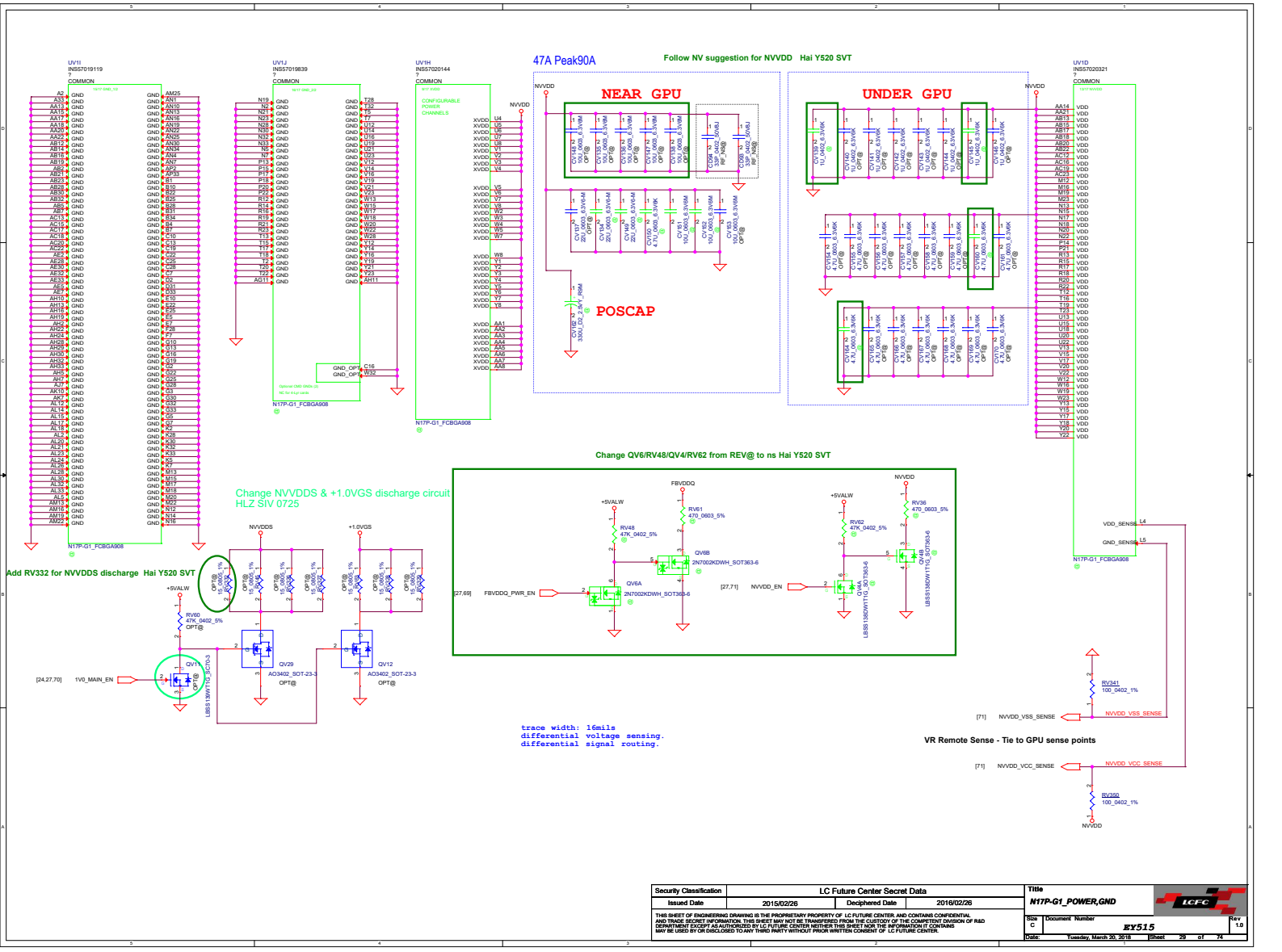
Size: D | Document Number: EY515 | Rev: 1.0

Date: Tuesday, March 20, 2018 |



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

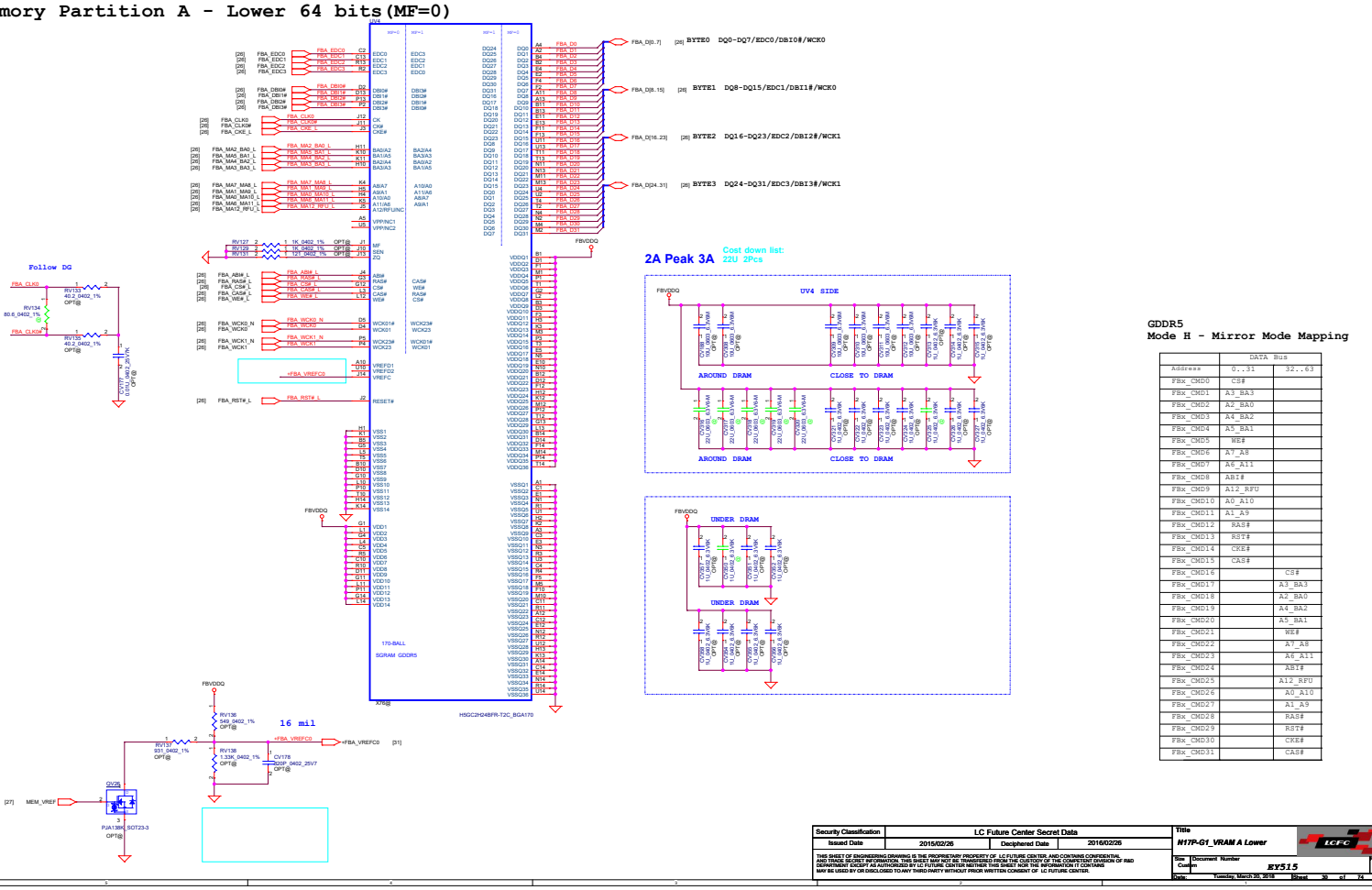
Title	N17P-G1_POWER		
Size	Document Number		Rev
Custom	EY515		1.0
Date:	Tuesday, March 20, 2018	Sheet	29 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N17P-G1_POWER,GND		
Size	Document Number		Rev
C	EY515		1.0
Date:	Tuesday, March 20, 2018	Sheet	29 of 74

Memory Partition A - Lower 64 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

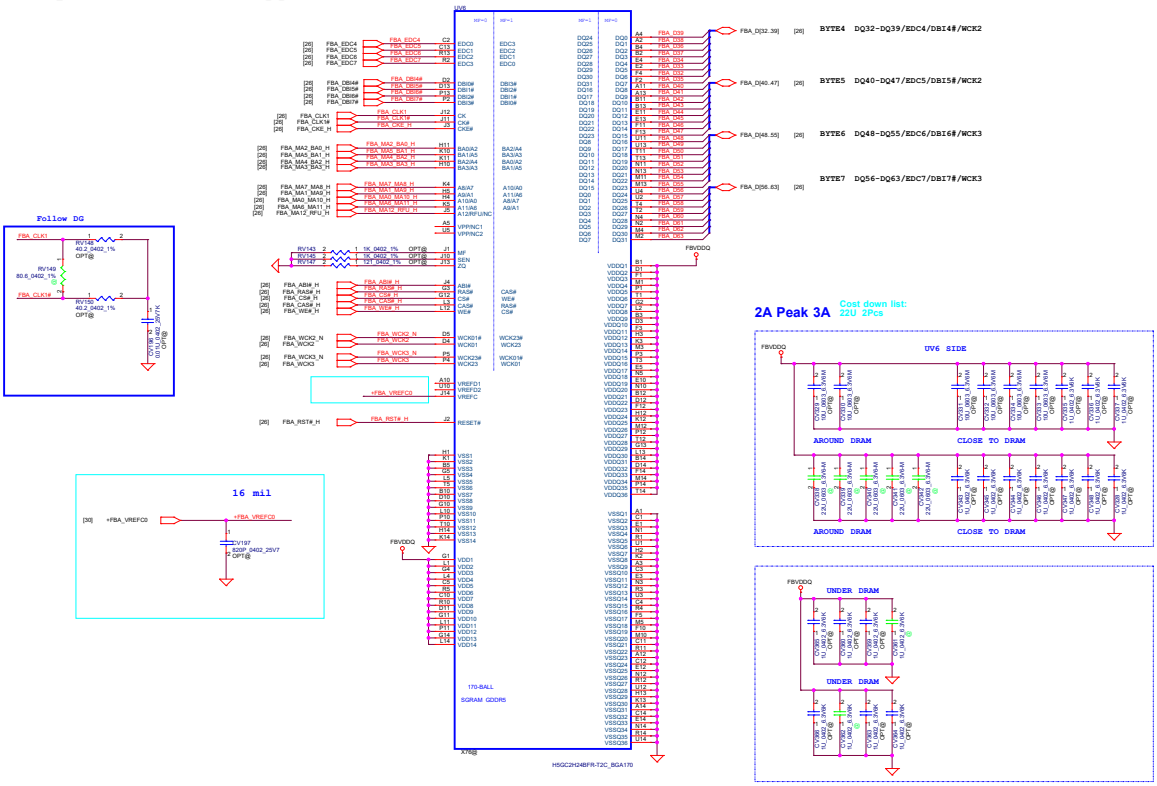
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N17P-G1_VRAM A Lower

Size: Custom | Document Number: EY515 | Rev: 1.0

Date: Tuesday, March 20, 2018 | Sheet 30 of 74

Memory Partition A- Upper 64 bits(MF=0)



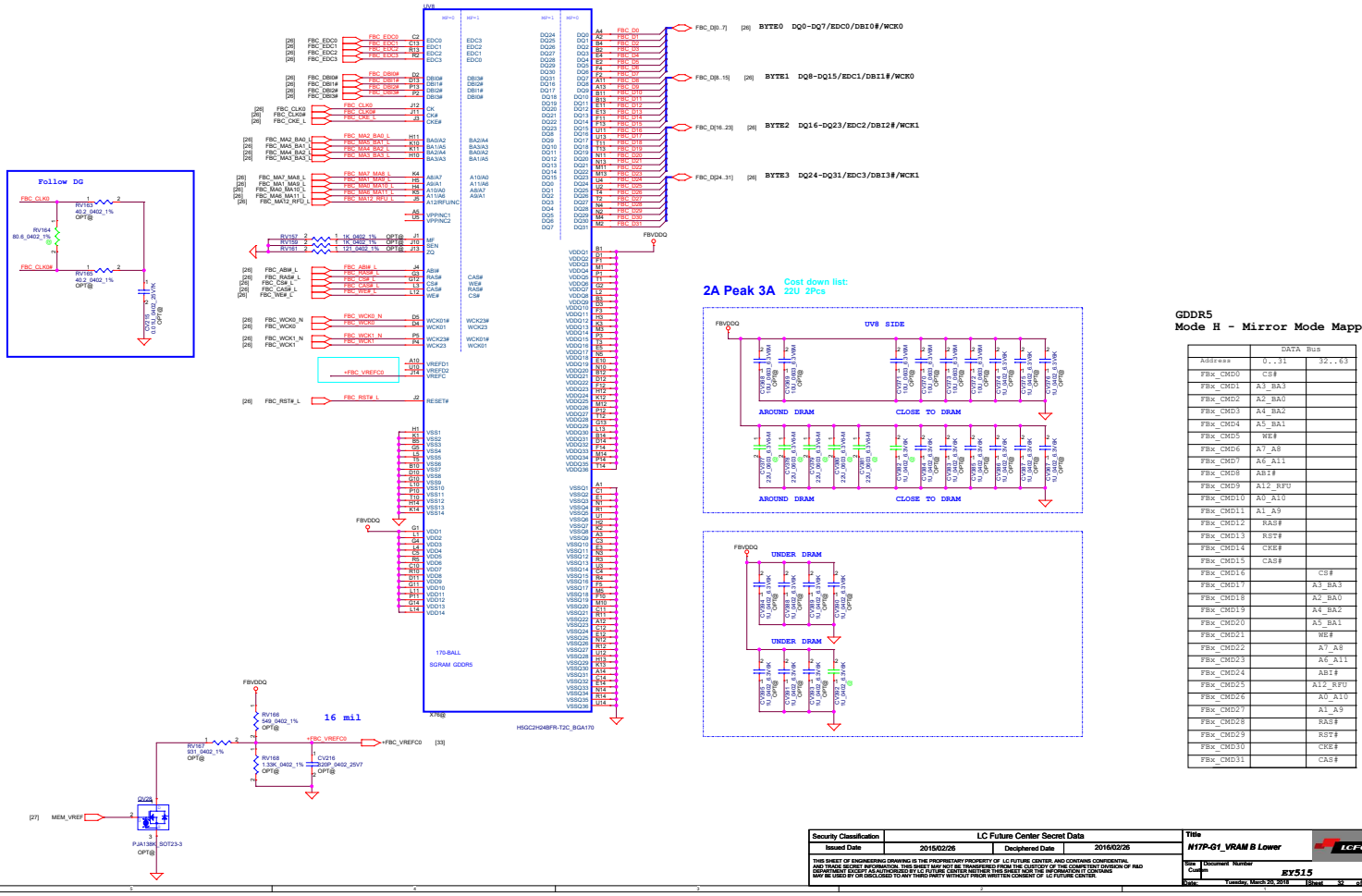
GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N17P-G1_VRAM A Upper		
Size	Document Number		Rev
Custom	EY515		1.0
Date:	Tuesday, March 29, 2016	Sheet 31 of 74	

Memory Partition B - Lower 32 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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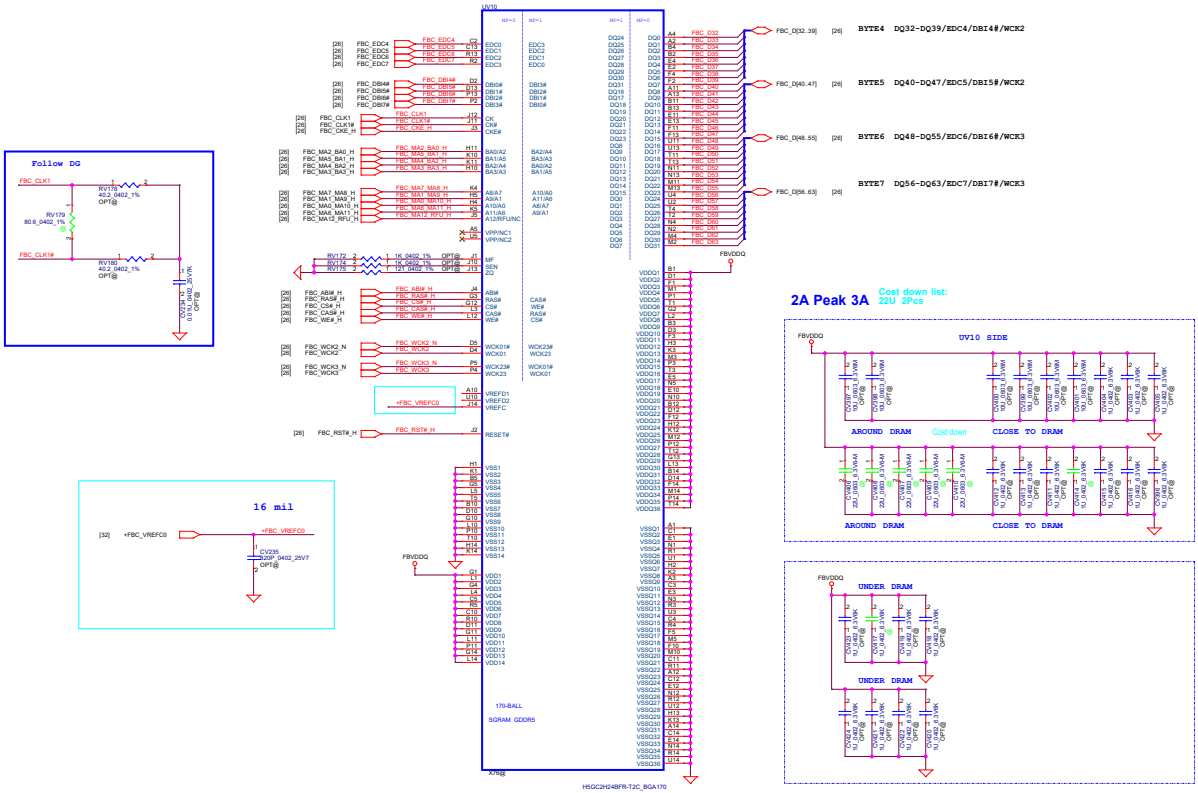
Title	N17P-G1_VRAM B Lower		
Size	Document Number		Rev
Custom	EY515		1.0
Date:	Tuesday, March 29, 2016	Sheet	32 of 74

Memory Partition B - Upper 32 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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Title	N17P-G1_VRAM B Upper		
Size	Document Number		Rev 1.0
Custom	EY515		
Date:	Tuesday, March 29, 2016	Sheet 33 of 74	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

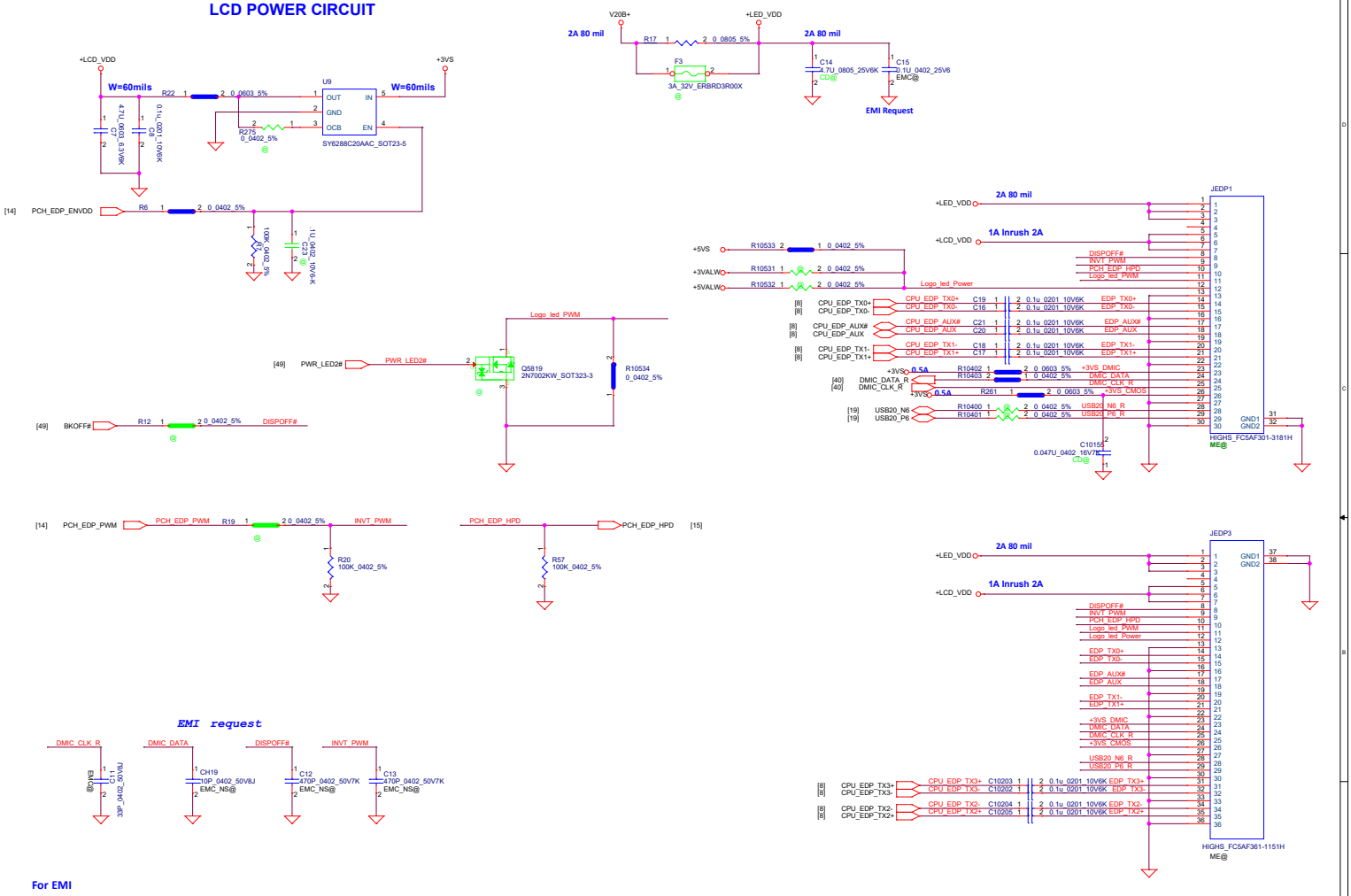
Title

N17P-G1_VRAM B Upper

Size	Document Number	Rev
D	EY515	1.0

Date: Tuesday, March 20, 2018

LCD POWER CIRCUIT

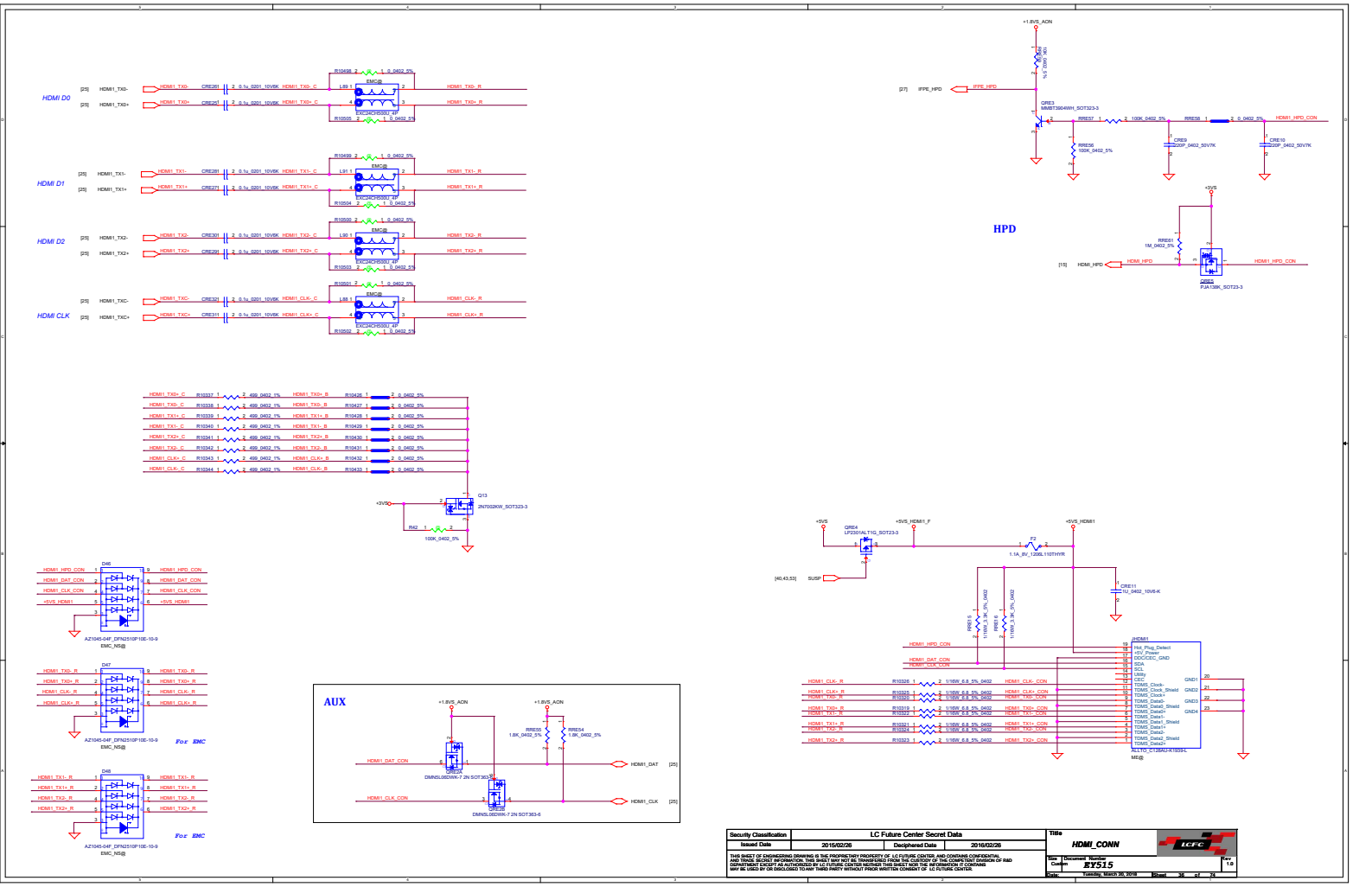


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: eDP/ CMOS/Touch screen

Size	Document Number	Rev
Custom	EY515	1.0

Date: Tuesday, March 20, 2018 Sheet 35 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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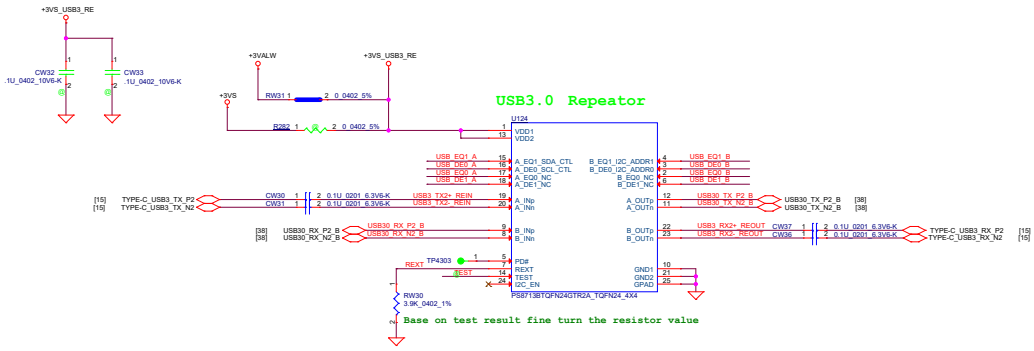
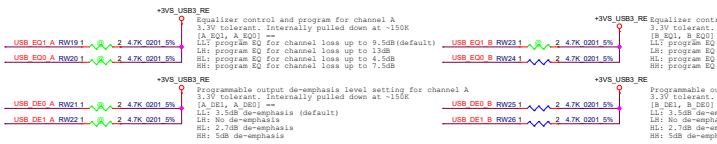
Title	HDMI_CONN		
Size	Document Number		Rev
Custom	EY515		1.0
Date:	Tuesday, March 29, 2016	Sheet	36 of 74





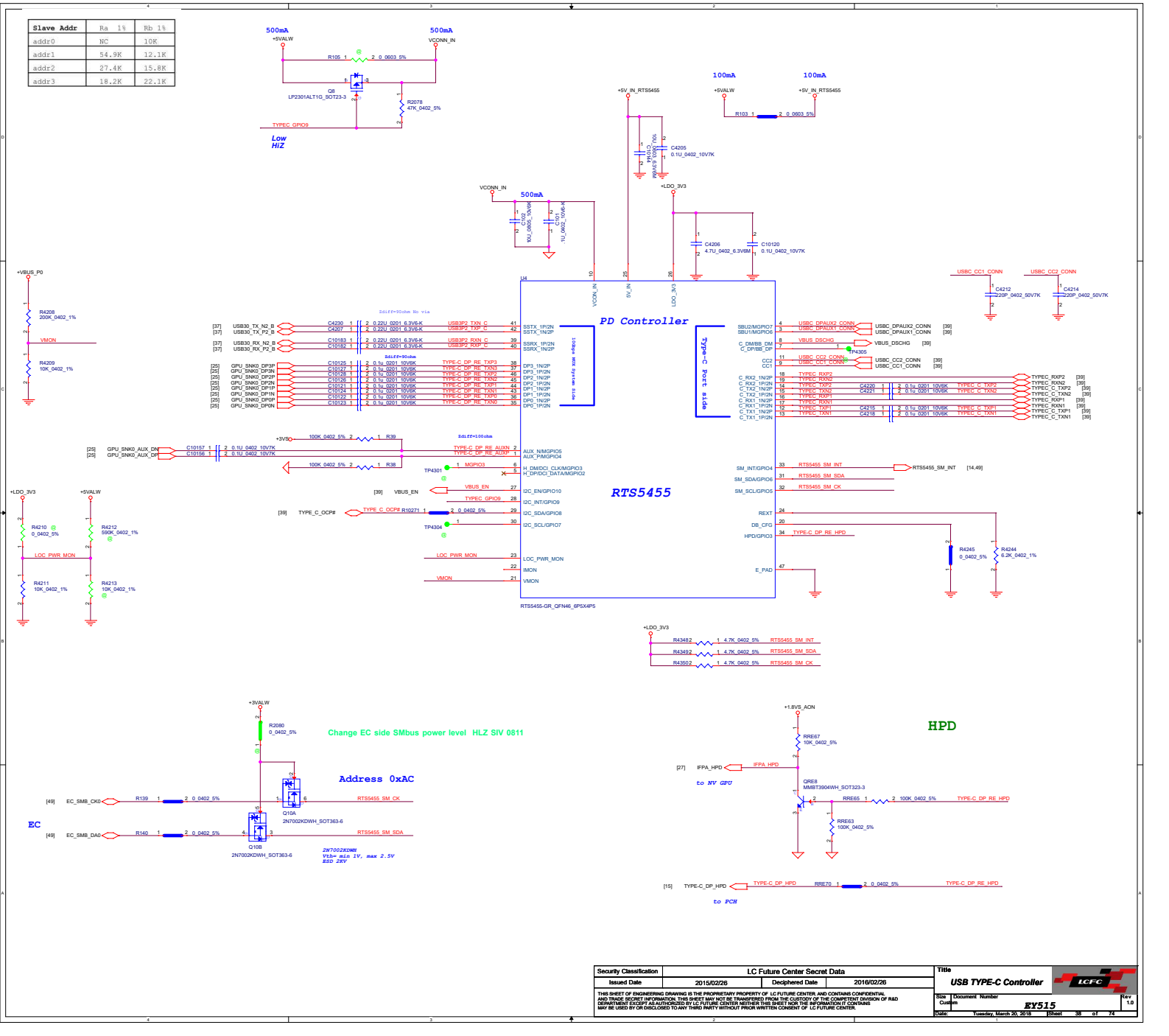
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: DDI Redriver PS8330

Size	Document Number	Rev
C	EY515	1.0

Date: Tuesday, March 20, 2018 Sheet 37 of 74

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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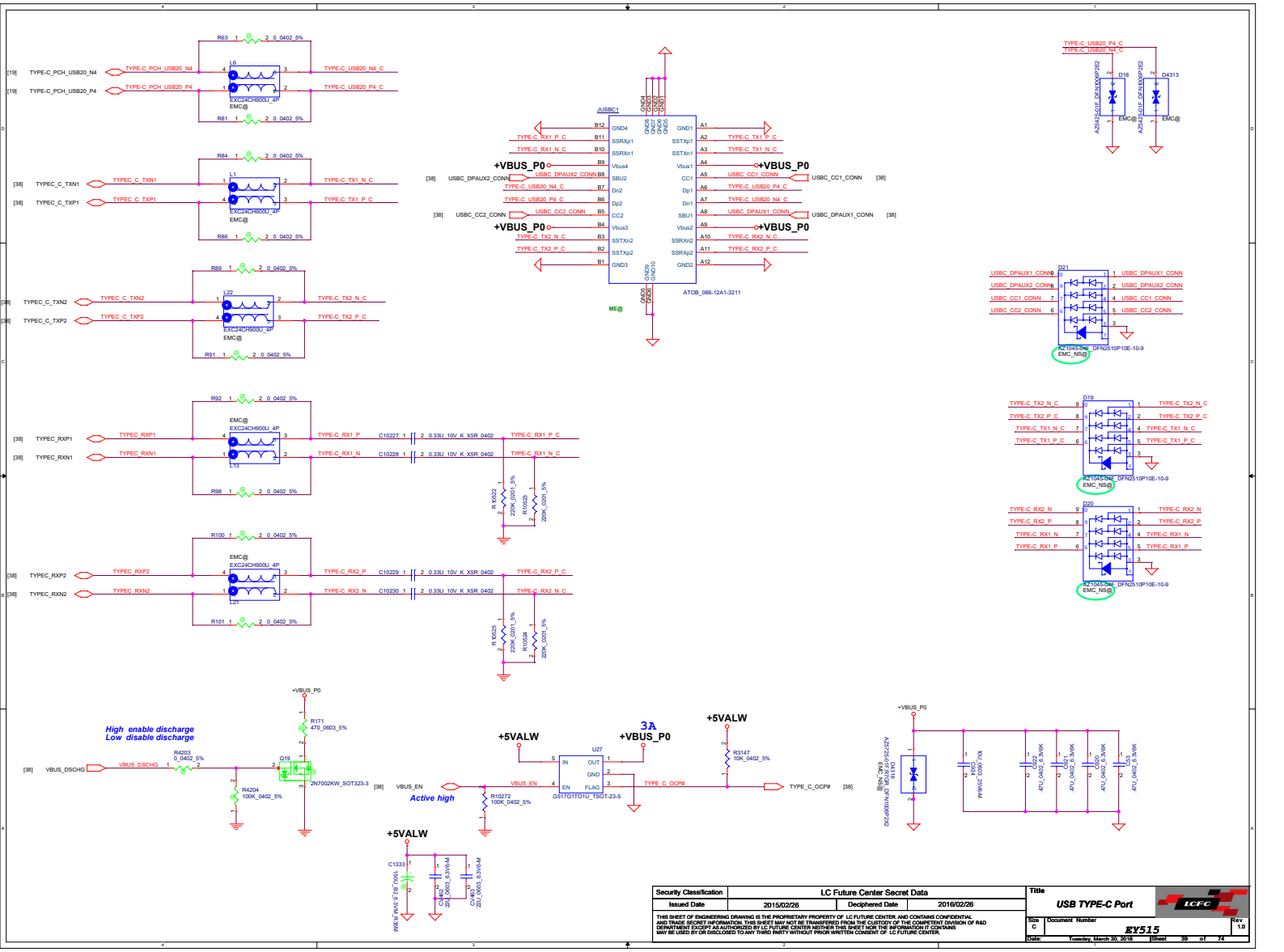
Title: USB TYPE-C Controller

LCFC

Size: Custom | Document Number: EY515 | Rev: 1.0

Date: Tuesday, March 29, 2016 | Sheet 38 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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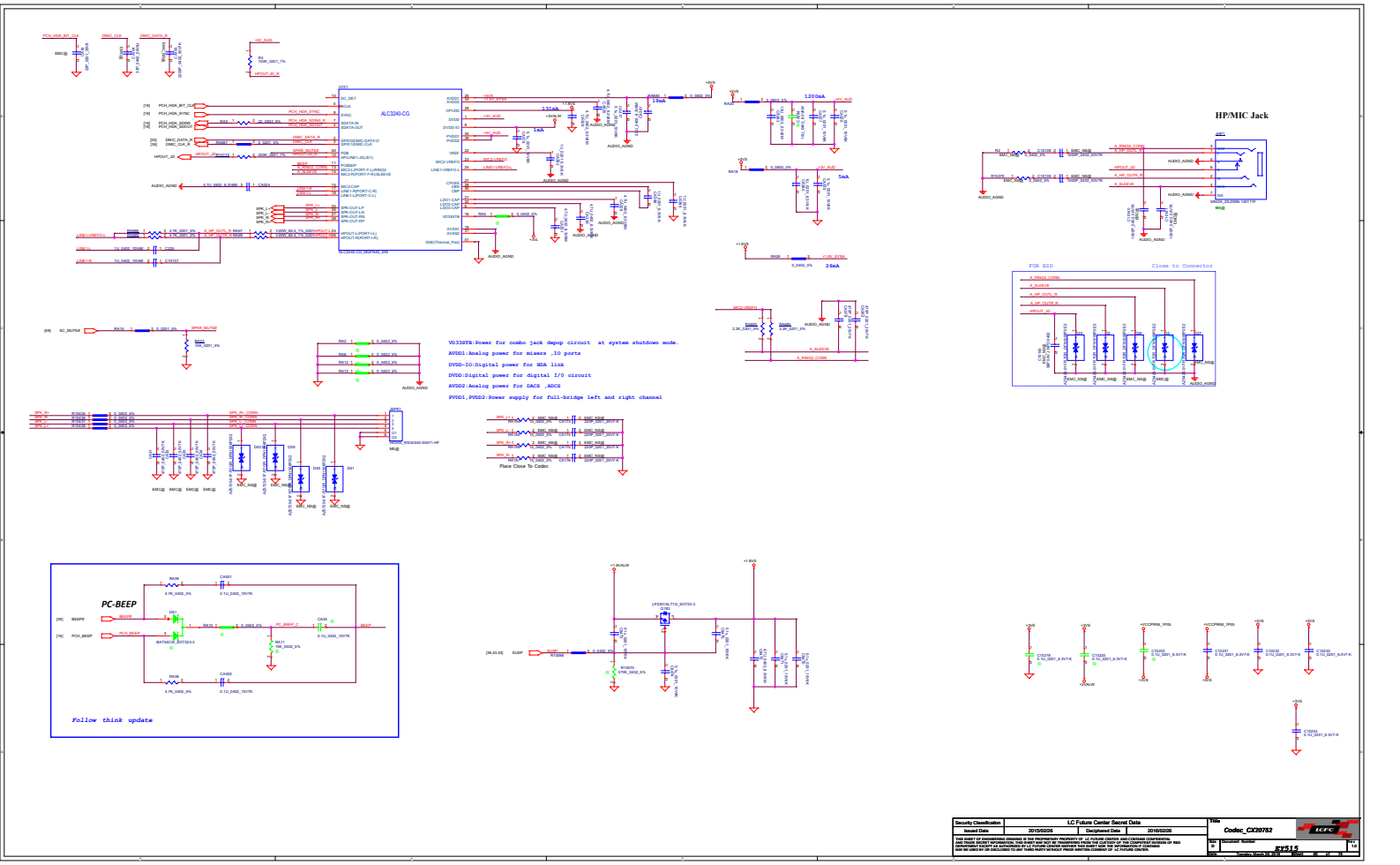
Title: **USB TYPE-C Port**

Size	Document Number	Rev
C	EY515	1.0

Date: Tuesday, March 20, 2018 Sheet 39 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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Title	Codec_CX20752		
Size	Document Number		Rev
B		BY515	1.0
Date:	Tuesday, March 24, 2015	Sheet	46 of 46

Security Classification	LC Future Center Secret Data		
Issued Date	2015/6/23	Deciphered Date	2015/6/23

Title

Audio Jack

Size	Document Number	Rev
C	EY515	1.0

Date: Tuesday, March 20, 2018 Sheet 41 of 74

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

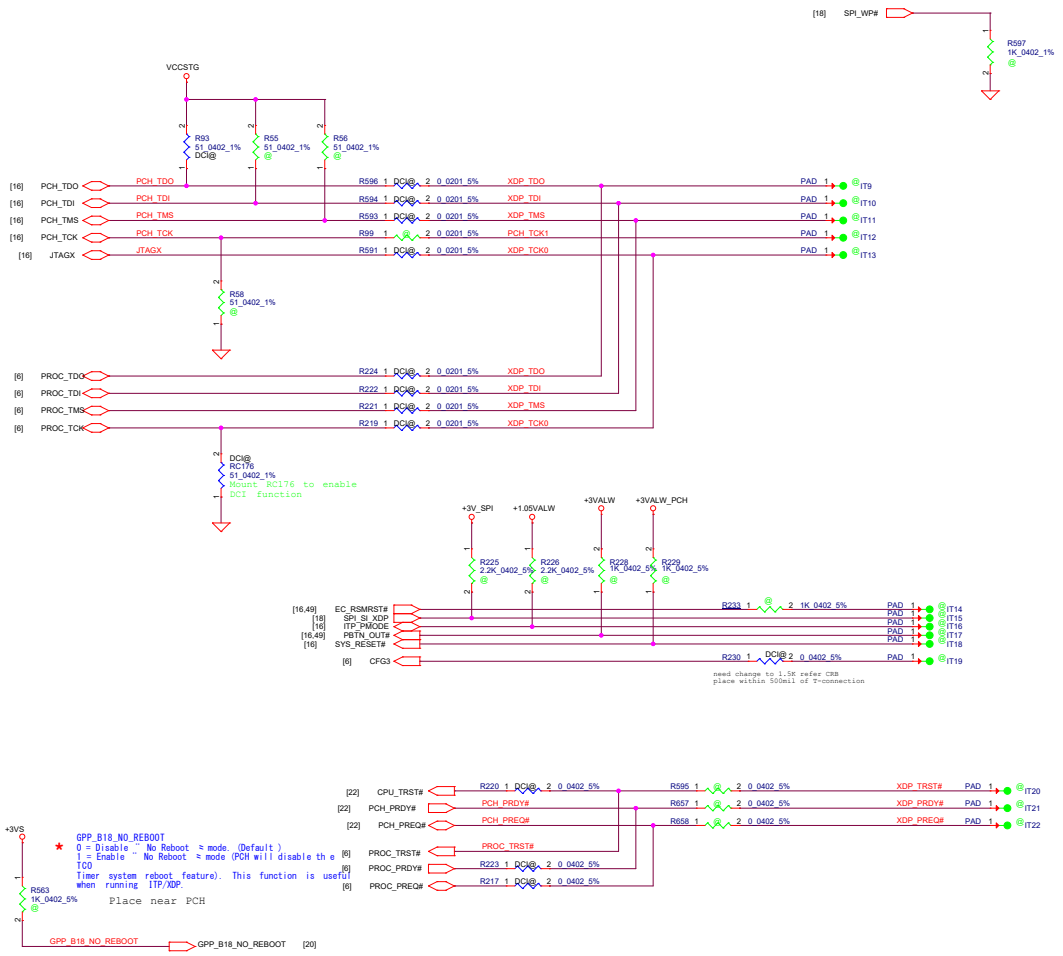
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

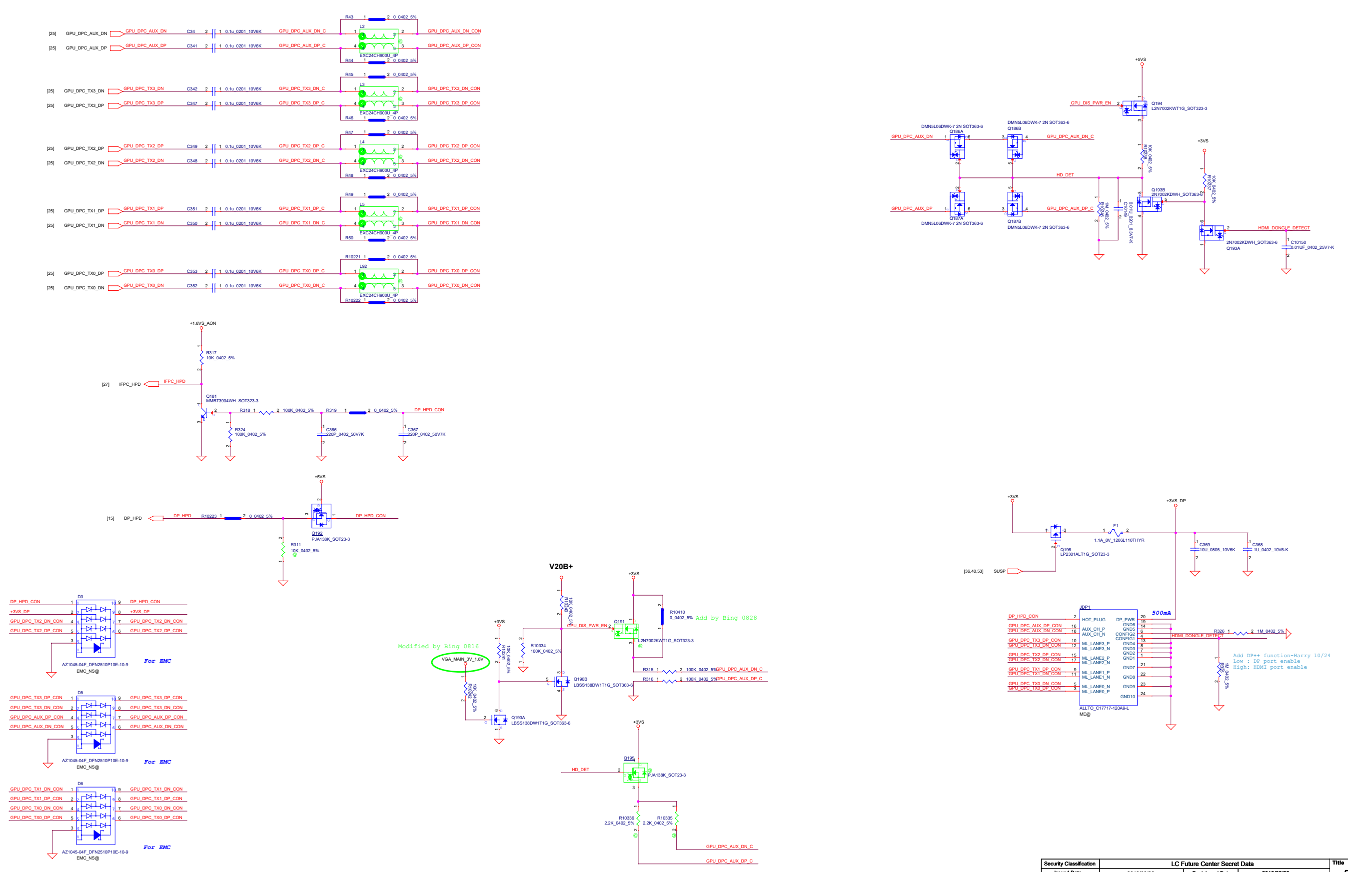
GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

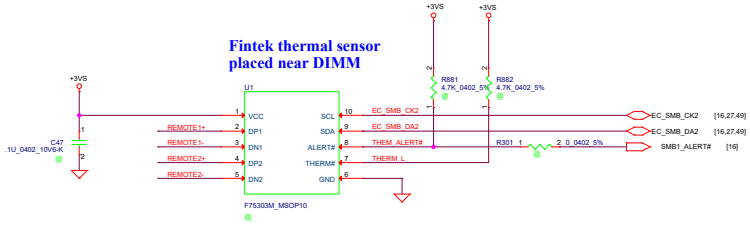


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

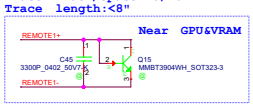
Title	XDP	
Size: Custom	Document Number: EY515	Rev: 1.0
Date: Tuesday, March 20, 2018	Sheet 42 of 74	

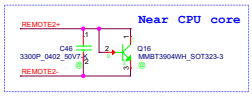


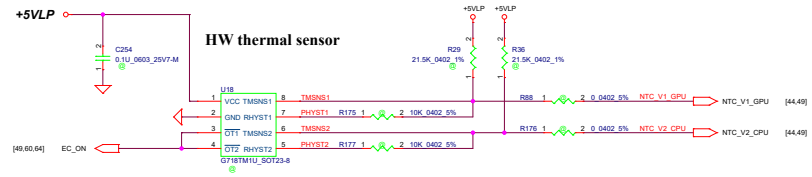
Security Classification	LC Future Center Secret Data			Title: DP
Issued Date	2013/08/08	Deciphered Date	2016/02/26	Size D · Document Number EY515 · Rev 1.0
				Date: Tuesday, March 20, 2018 · Sheet 43 of 74



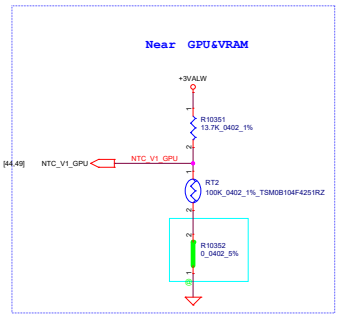
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

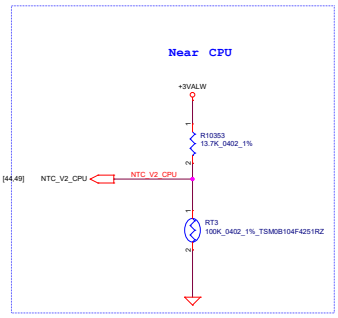




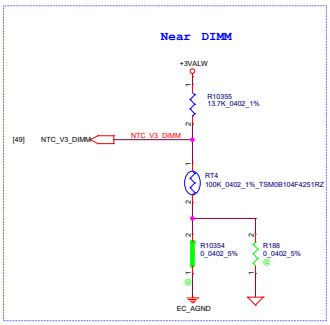


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



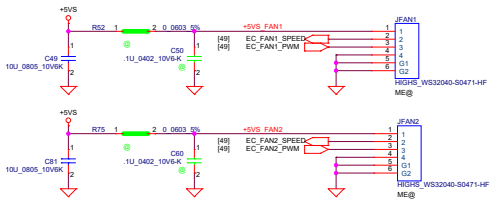


for layout optimized, change the EC_AGND to GND



FAN Conn

Address 1001_101xb



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	
	Thermal sensor/FAN CONN
Size: Custom	Document Number: EY515
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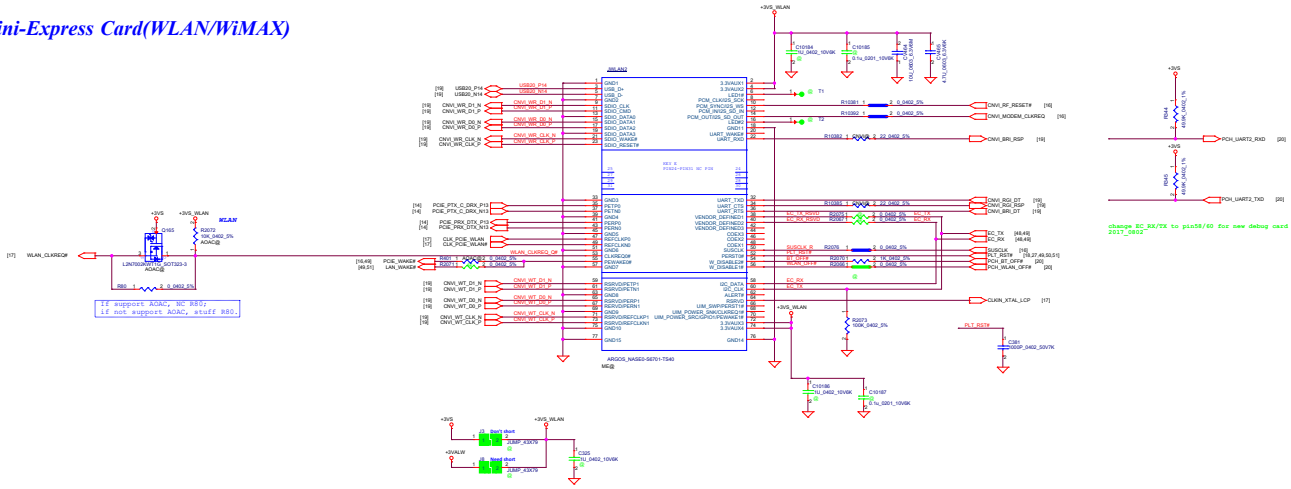
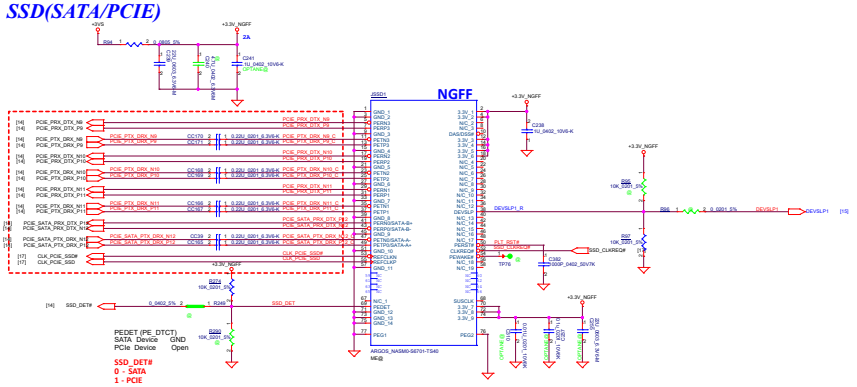
Date: Tuesday, March 20, 2018	Sheet 44 of 74

AMP/Volume Control

Mini-Express Card(WLAN/WiMAX)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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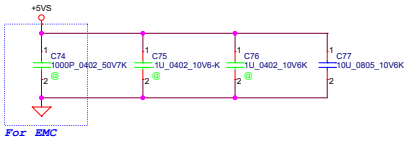
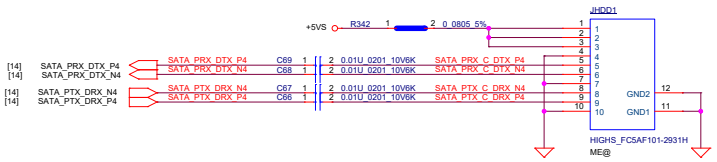
Title	NGFF WLAN	
Size	Document Number	Rev
Custom	RX515	1.0
Date:	Tuesday, March 28, 2017	Sheet 46 of 74

SATA HDD Conn.



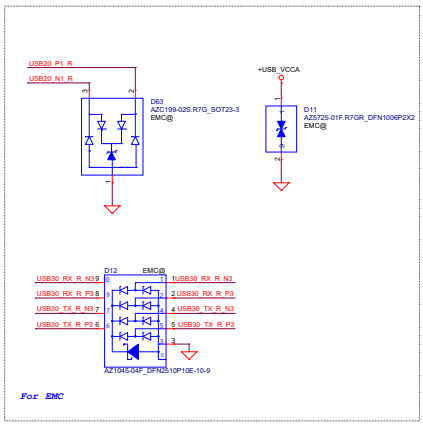


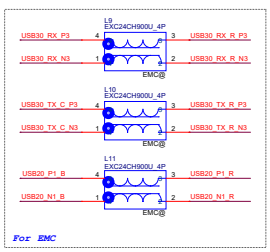
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: HDD/XBOX CONN

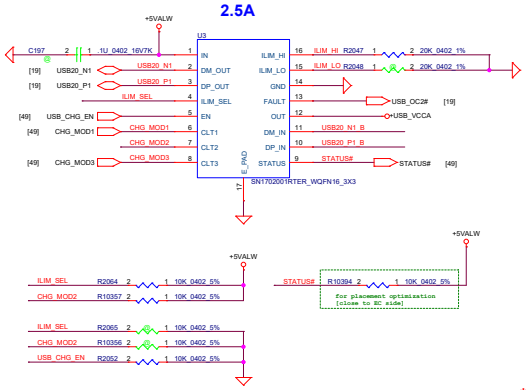
Size	Document Number	Rev
Custom	EY515	1.0

Date: Tuesday, March 20, 2018 Sheet 46 of 74





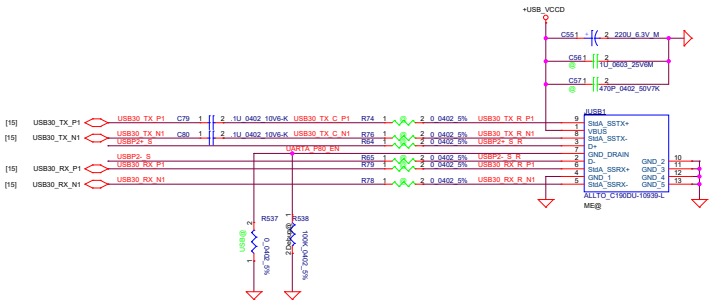
USB charger
2.5A



CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT hold low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

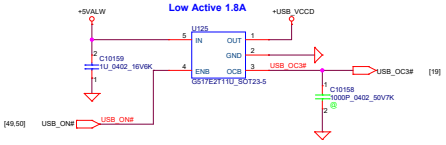
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	USB2.0/USB3.0 PORT (LEFT)		
Size C	Document Number EY515		Rev 1.0
Date: Tuesday, March 20, 2018	Sheet 47 of 74		

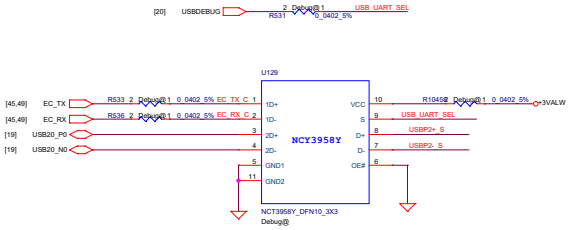


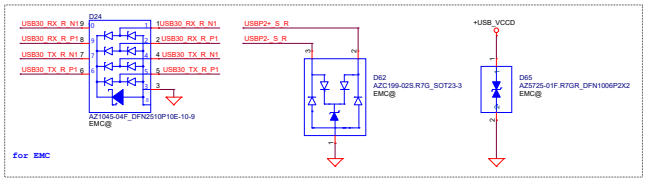
USB3.1 PORT x1

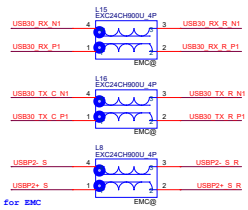
Low Active 1.8A



For USB Debug Function



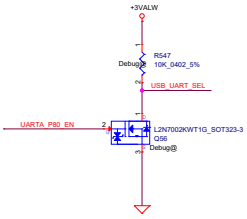




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

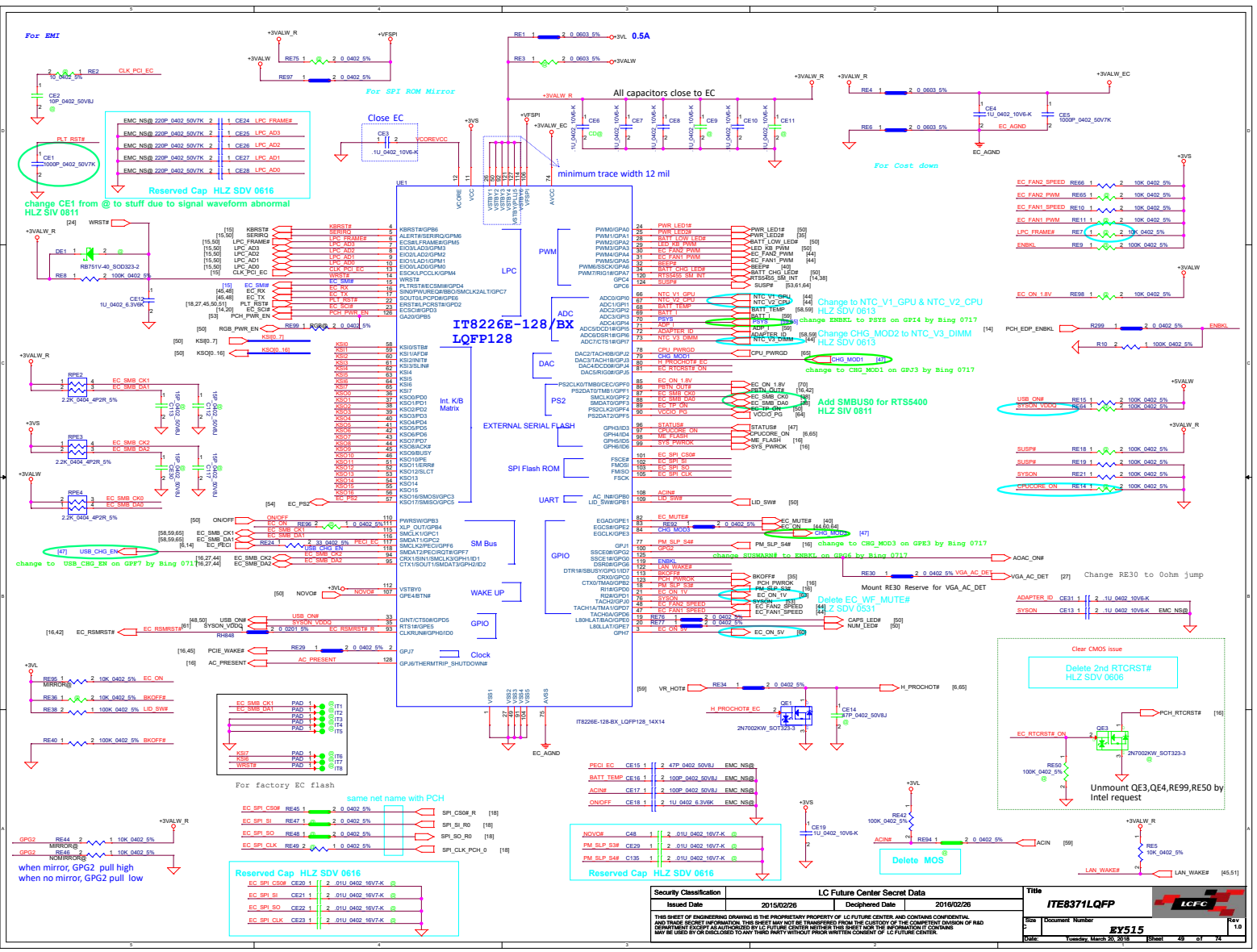
UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/6/23	Deciphered Date	2015/6/23

Title			
USB2.0			
Size C	Document Number EY515		Rev 1.0
Date: Tuesday, March 20, 2018	Sheet 48 of 74		


For EMI
IT8226E-128/BX
LQFP128
LPC
PWM
ADC
DAC
PS2
Int. K/B Matrix
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
Close EC
All capacitors close to EC
minimum trace width 12 mil
For SPI ROM Mirror
For Cost down
Reserved Cap HLZ SDV 0616
change CE1 from @ to stuff due to signal waveform abnormal
HLZ SIV 0811
Change to NTC_V1_GPU & NTC_V2_CPU
HLZ SDV 0613
change ENBKL to PSYS on GPI4 by Bing 0717
Change CHG_MOD2 to NTC_V3_DIMM
HLZ SDV 0613
change to CHG_MOD1 on GPJ3 by Bing 0717
Add SMBUS0 for RTS5400
HLZ SIV 0811
change to USB_CHG_EN on GPF7 by Bing 0717
change SUSWARN# to ENBKL on GPC6 by Bing 0717
change to CHG_MOD3 on GPE3 by Bing 0717
Mount RE30 Reserve for VGA_AC_DET
Change RE30 to 0ohm jump
Delete EC_WF_MUTE#
HLZ SDV 0531
Clear CMOS issue
Delete 2nd RTCRST#
HLZ SDV 0606
Unmount QE3,QE4,RE99,RE50 by Intel request
Delete MOS
For factory EC flash
same net name with PCH
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Reserved Cap HLZ SDV 0616
Reserved Cap HLZ SDV 0616
0.5A
IT8226E-128-BX_LQFP128_14X14
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
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Title
ITE8371LQFP
Size
C
Document Number
EY515
Rev
1.0
Date:
Tuesday, March 20, 2018
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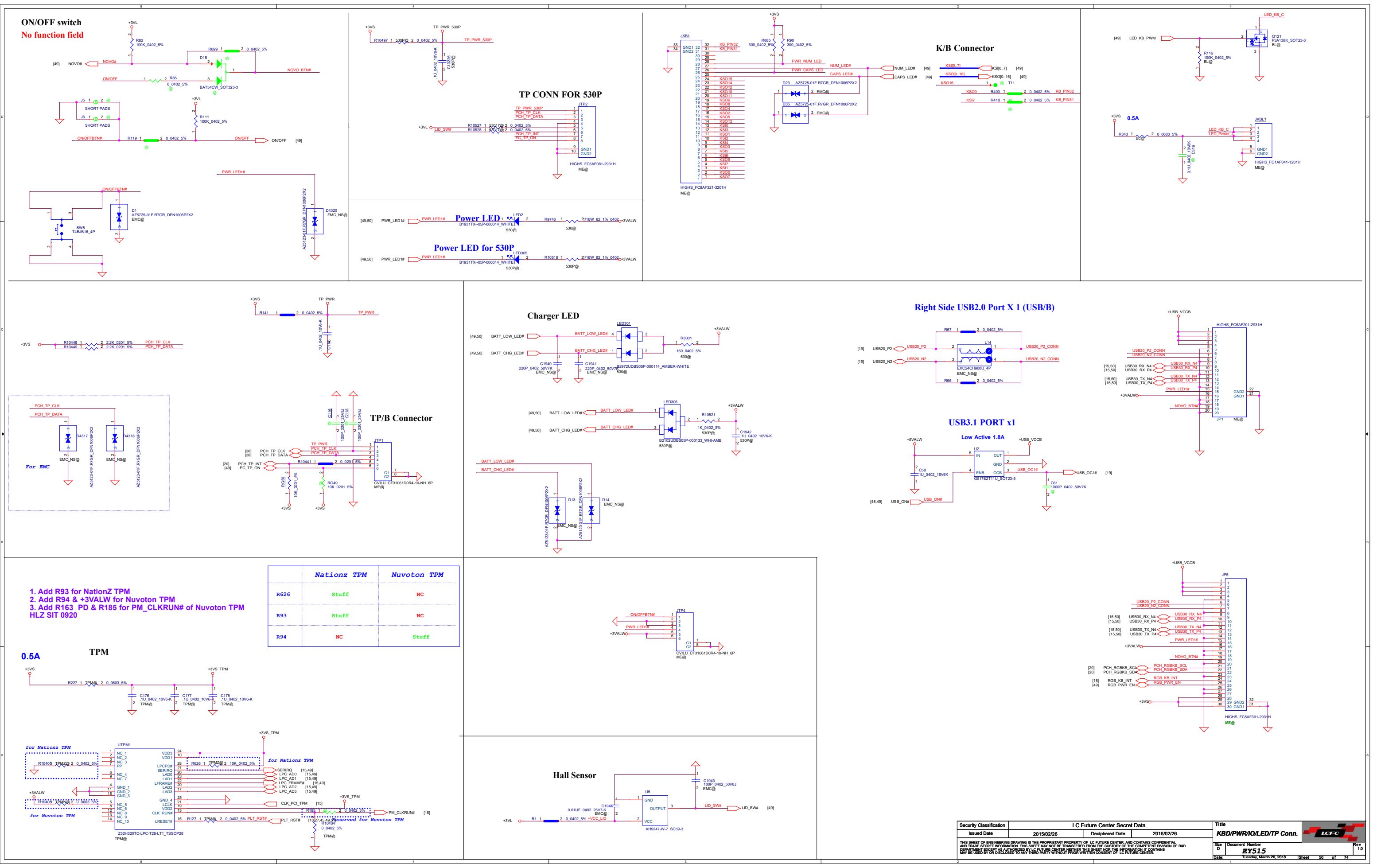
of
74



1. Add R93 for NationZ TPM
2. Add R94 & +3VALW for Nuvoton TPM
3. Add R163 PD & R185 for PM_CLKRUN# of Nuvoton TPM
HLZ SIT 0920

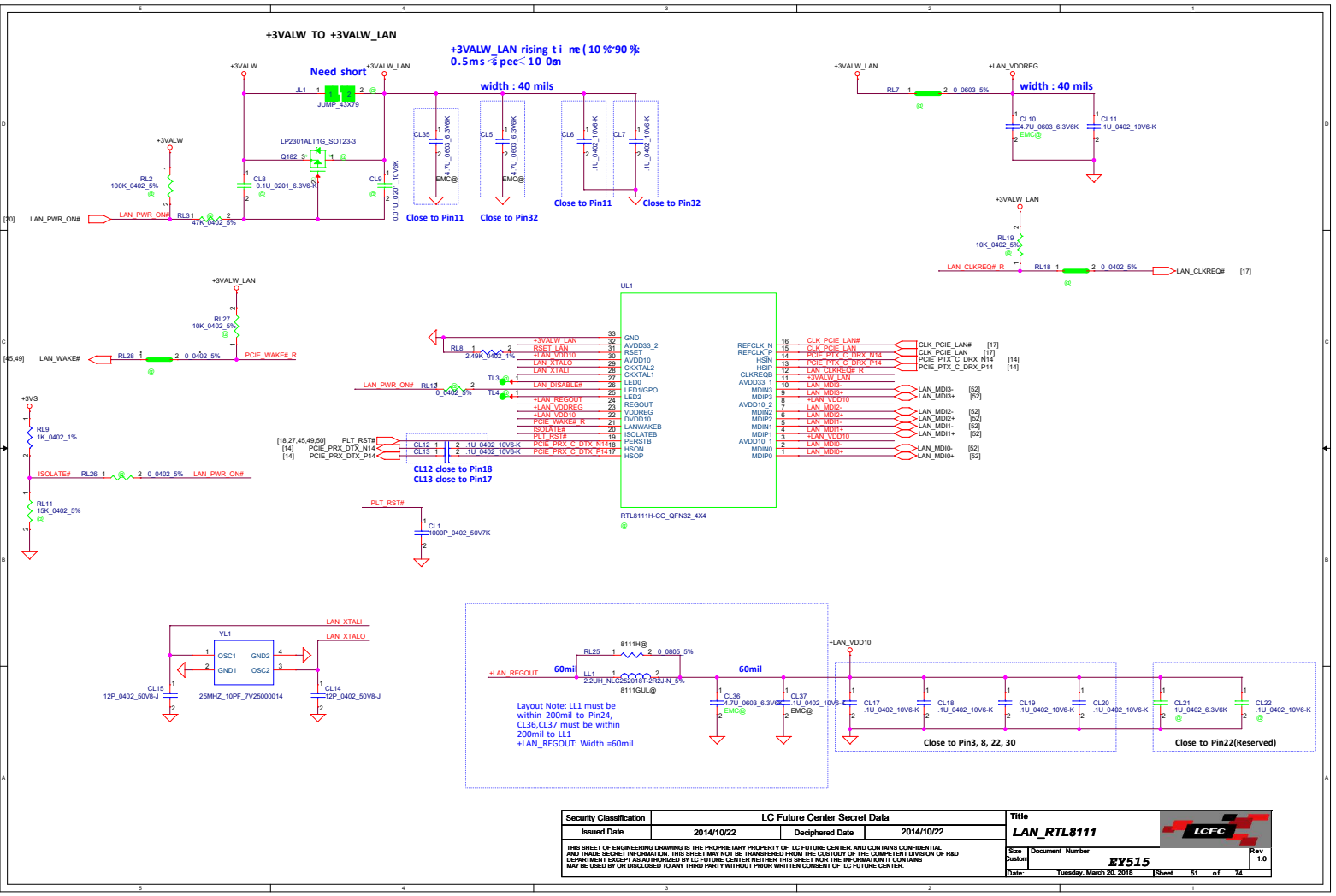
	Nationz TPM	Nuvoton TPM
R626	Stuff	NC
R93	Stuff	NC
R94	NC	Stuff

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: KBD/PWR/IO/LED/TP Conn.

Size: D | Document Number: EY515 | Rev: 1.0

Date: Tuesday, March 20, 2018 |



Security Classification	LC Future Center Secret Data		
Issued Date	2014/10/22	Deciphered Date	2014/10/22

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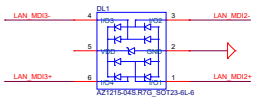
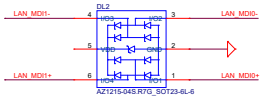
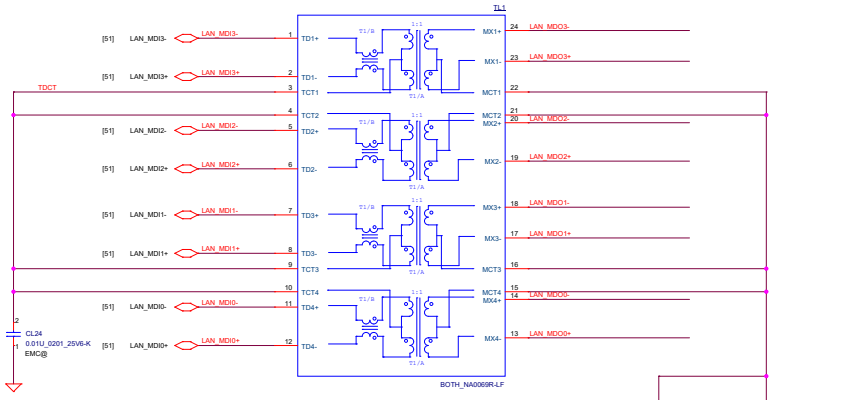
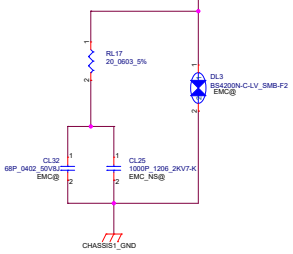
Title	LAN_RTL8111	
Size: Custom	Document Number: EY515	Rev: 1.0
Date: Tuesday, March 20, 2018	Sheet 51 of 74	

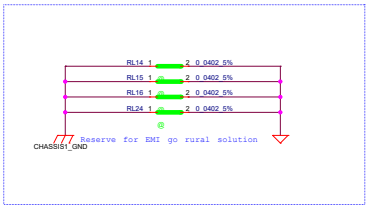
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

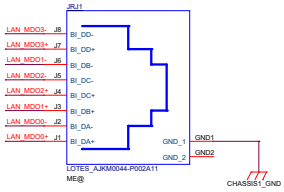












Security Classification	LC Future Center Secret Data		
Issued Date	2014/10/22	Deciphered Date	2014/10/22

Title: LAN_Transformer

Size	Document Number	Rev
C	EY515	1.0

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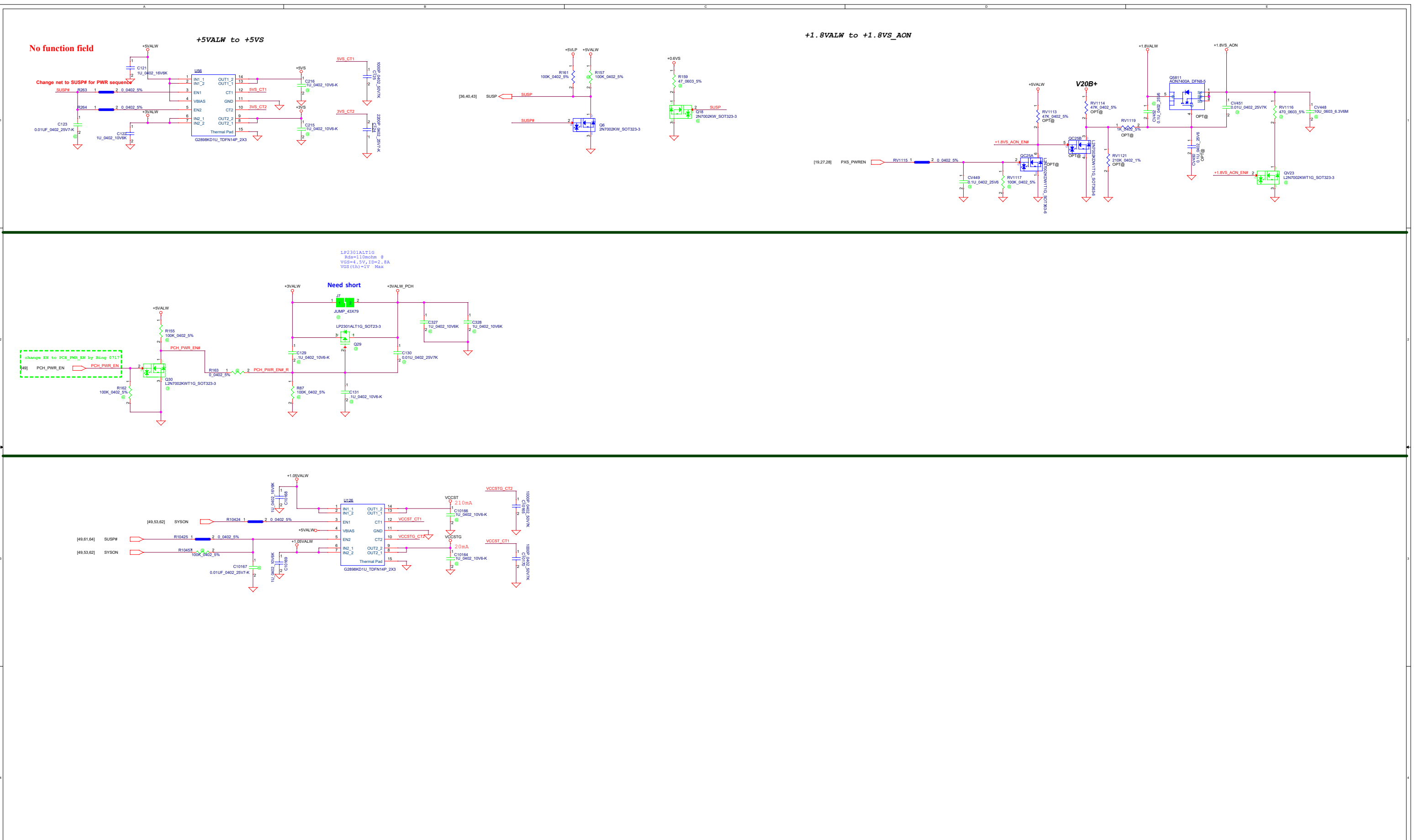
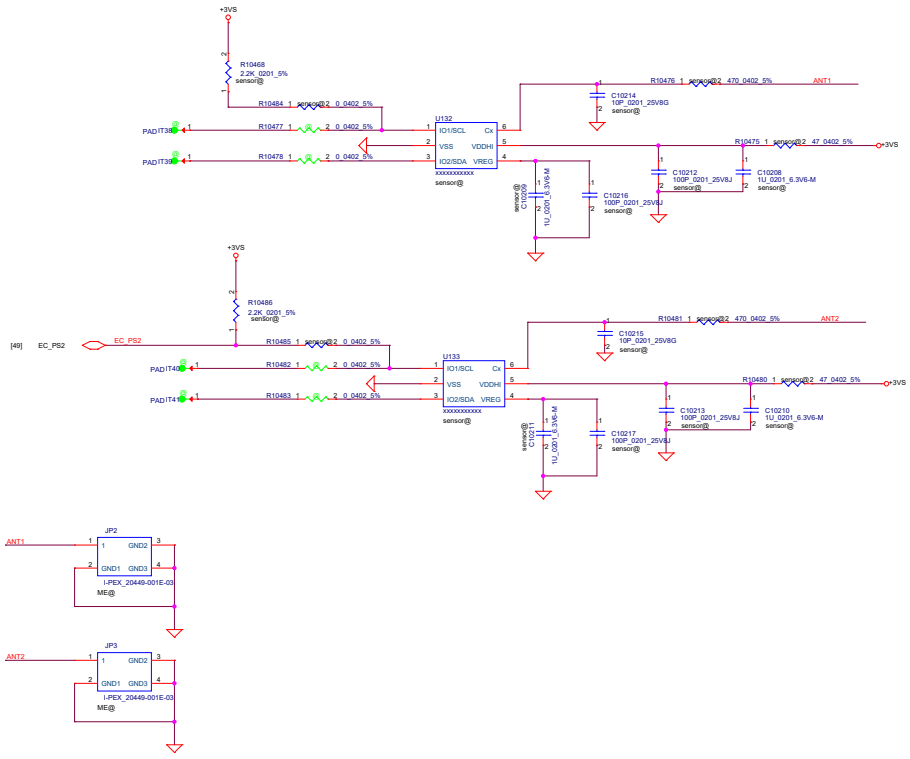


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **DC V TO VS INTERFACE**

Size: D
Document Number: EY515
Rev: 1.0

Date: Tuesday, March 20, 2018



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	*Virtual symbol*		
Size	Document Number		Rev
C	EY515		1.0
Date:	Tuesday, March 20, 2018	Sheet	54 of 74

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Virtual symbol*

Size	Document Number	Rev
C	EY515	1.0

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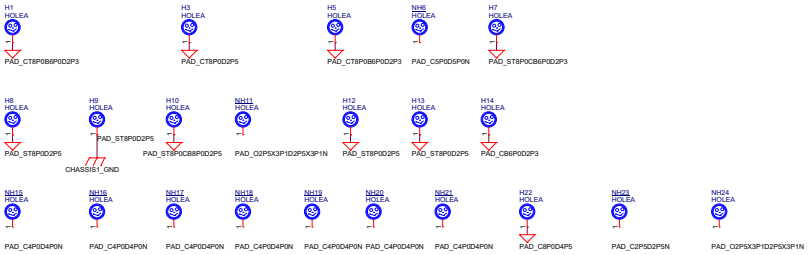
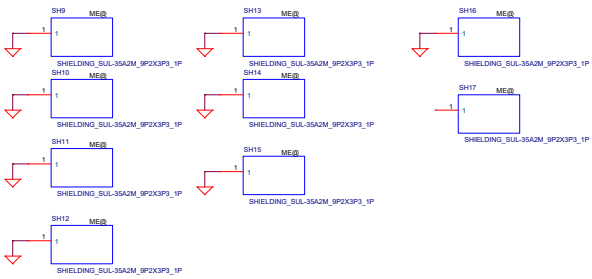
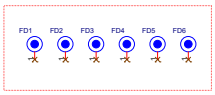




SO-DIMM Shielding

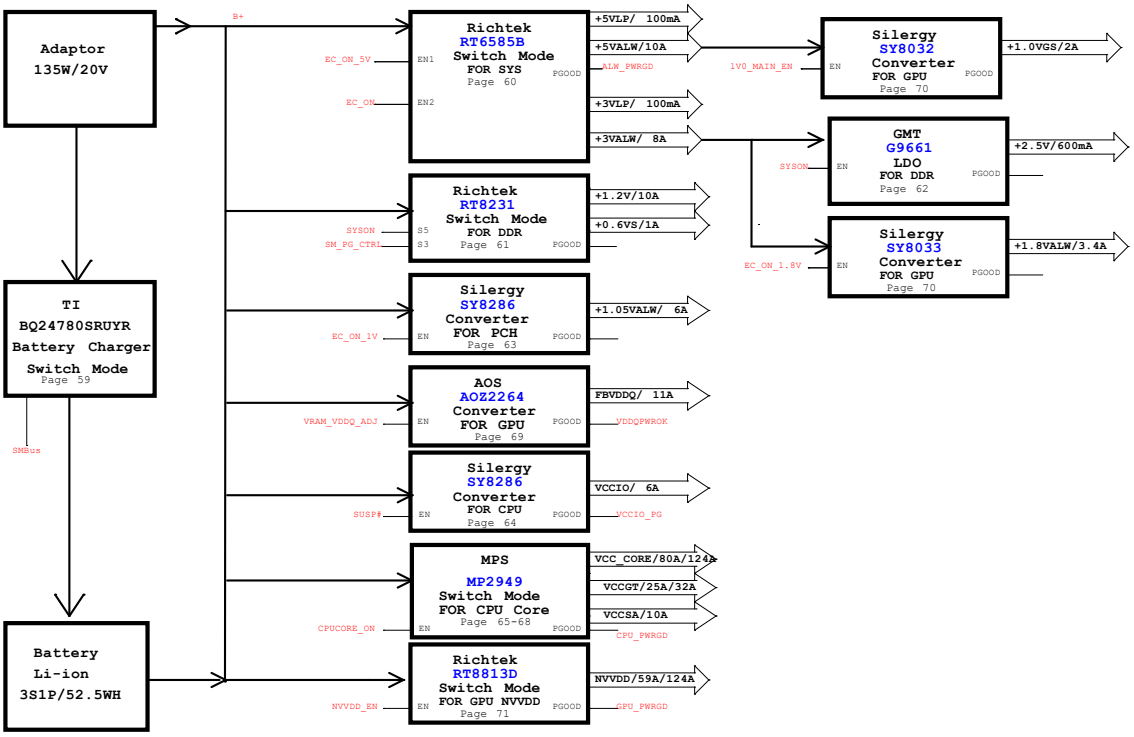


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Blank*

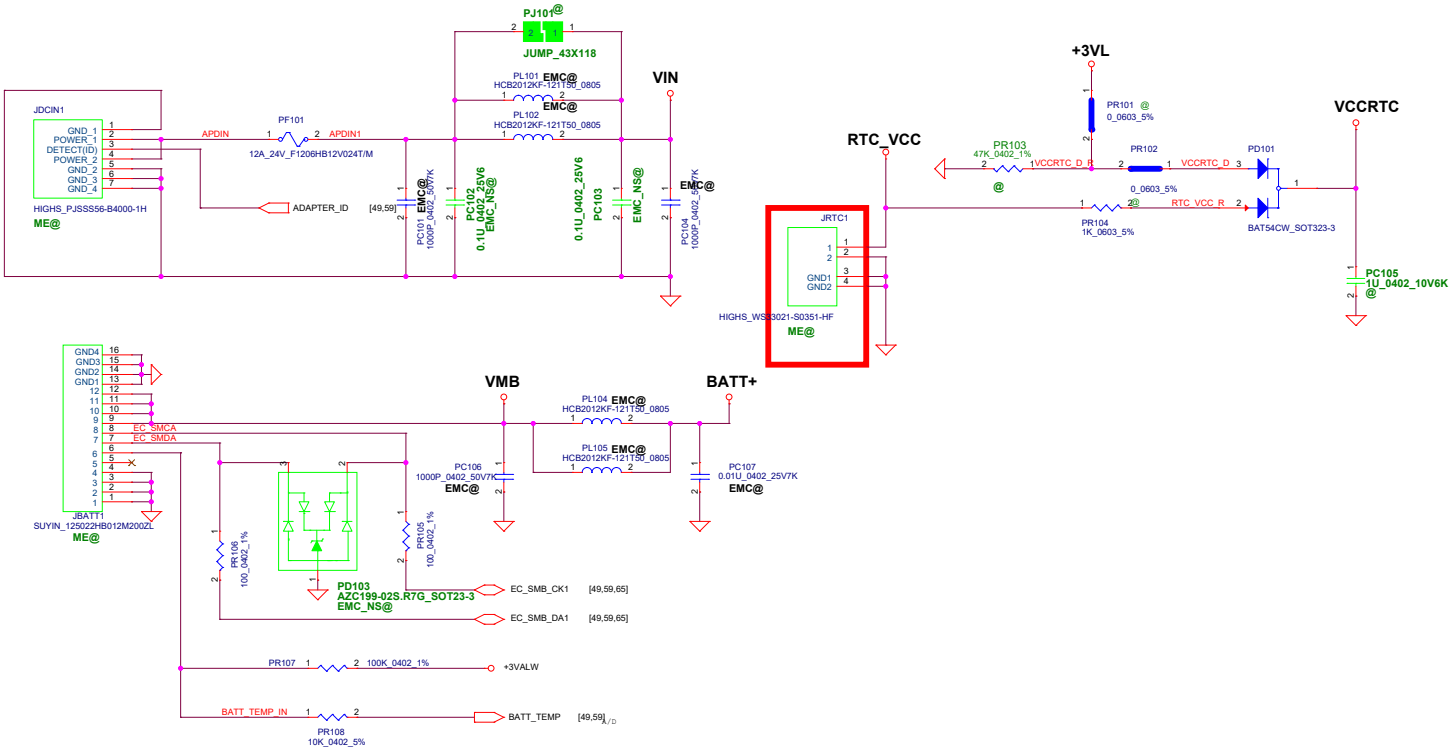
Size	Document Number	Rev
C	EY515	1.0

Date: Tuesday, March 20, 2018 Sheet 56 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	Power Diagram		
Size	Document Number		Rev
Custom	DZ510/DY512		1.0
Date:	Tuesday, March 29, 2016	Sheet	57 of 74

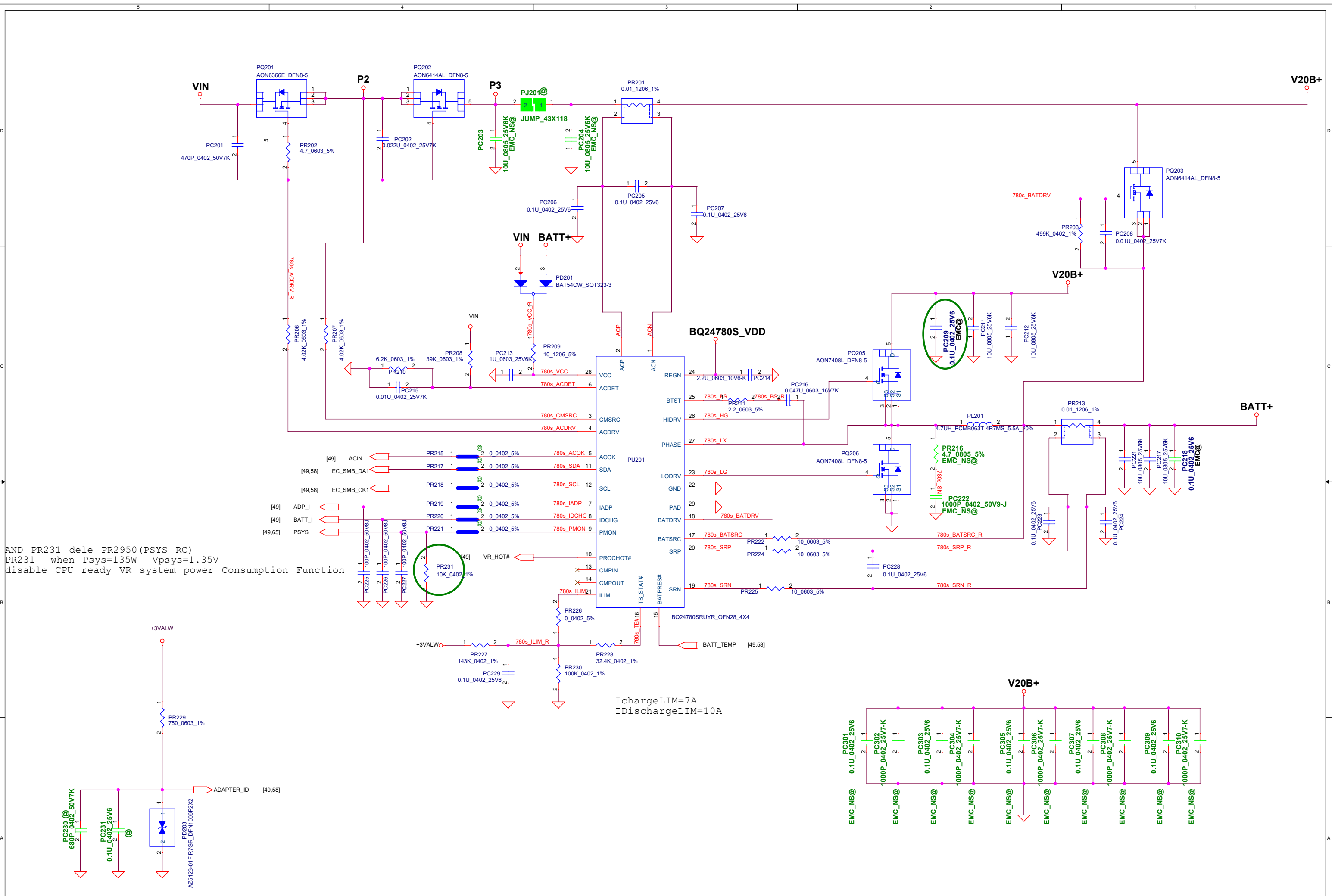


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-DCIN/BATT/RTC

Size	Document Number	Rev
Custom	DZ510/DY512	1.0

Date: Tuesday, March 20, 2018 Sheet 58 of 74

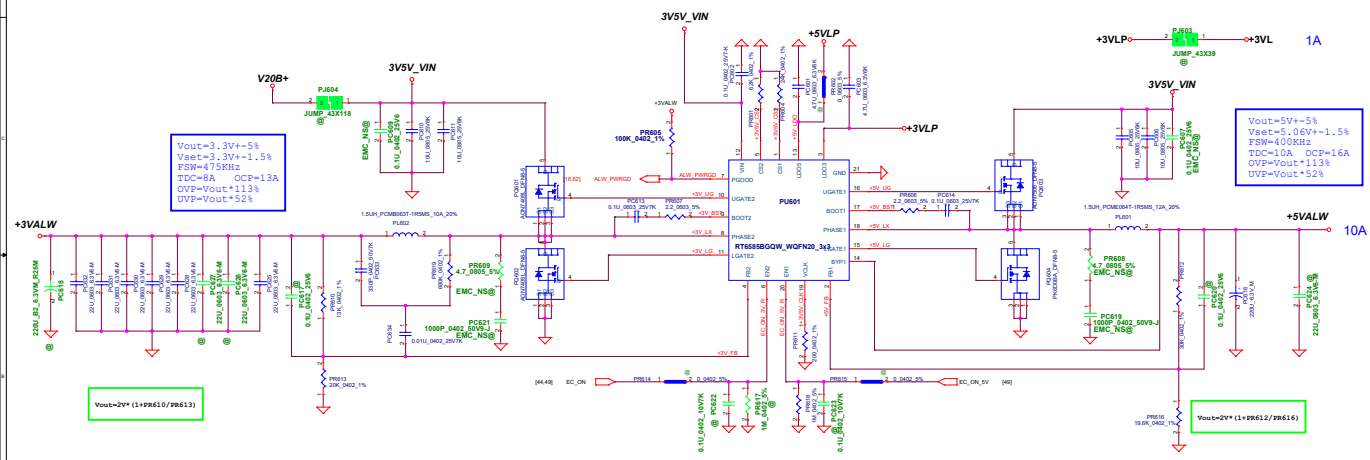


AND PR231 dele PR2950(PSYS RC)
PR231 when Psys=135W Vpsys=1.35V
disable CPU ready VR system power Consumption Function

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-charger**

Size: Custom | Document Number: DY520 | Rev: 0.1



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

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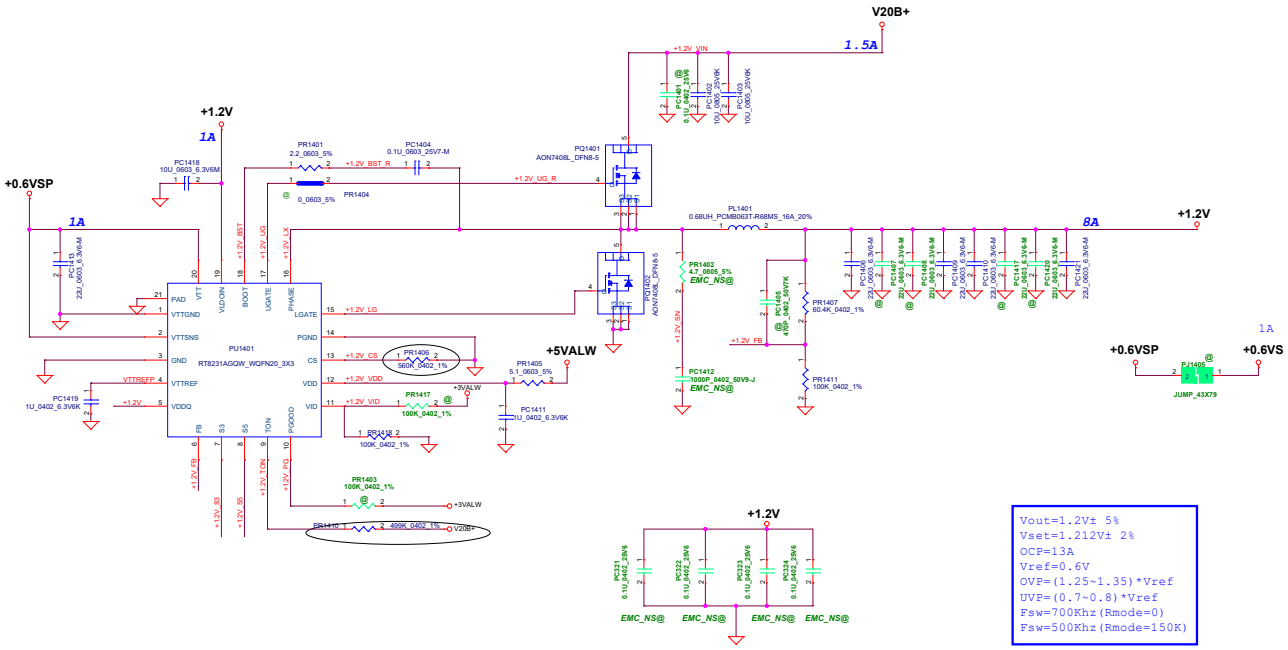
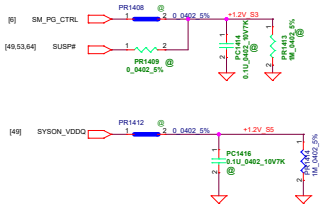
Title: PWR-3/5VALW

Size	Document Number	Rev
Custom	DZ510/DY512	1.0

Date: Tuesday, March 29, 2016 Sheet 60 of 75





Vout=1.2V± 5%
Vset=1.212V± 2%
OCP=13A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz(Rmode=0)
Fsw=500Khz(Rmode=150K)

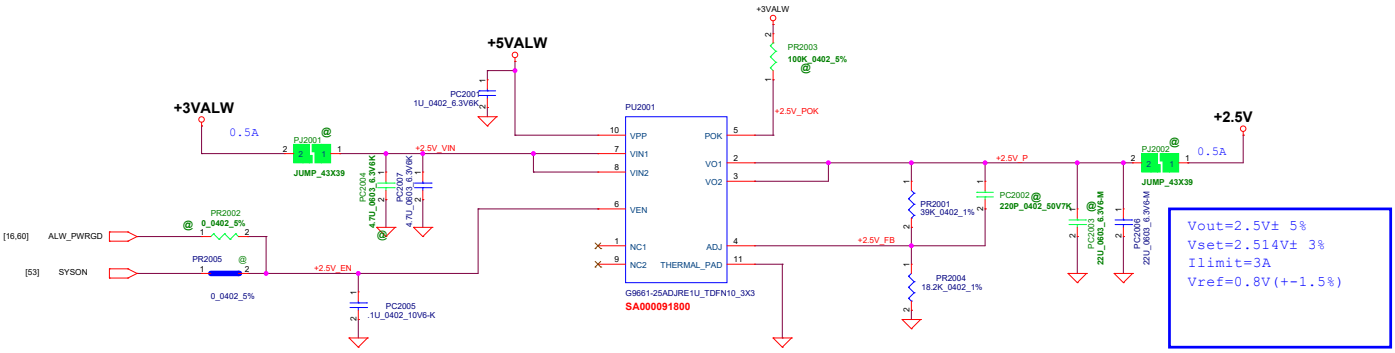
Vout=0.6V± 5%
OCP=1.5A
VTT=1/2VDDQ

STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-VDDQ/VTT		
Size C	Document Number	DY520	Rev 0.1
Date:	Tuesday, March 20, 2018	Sheet	61 of 74

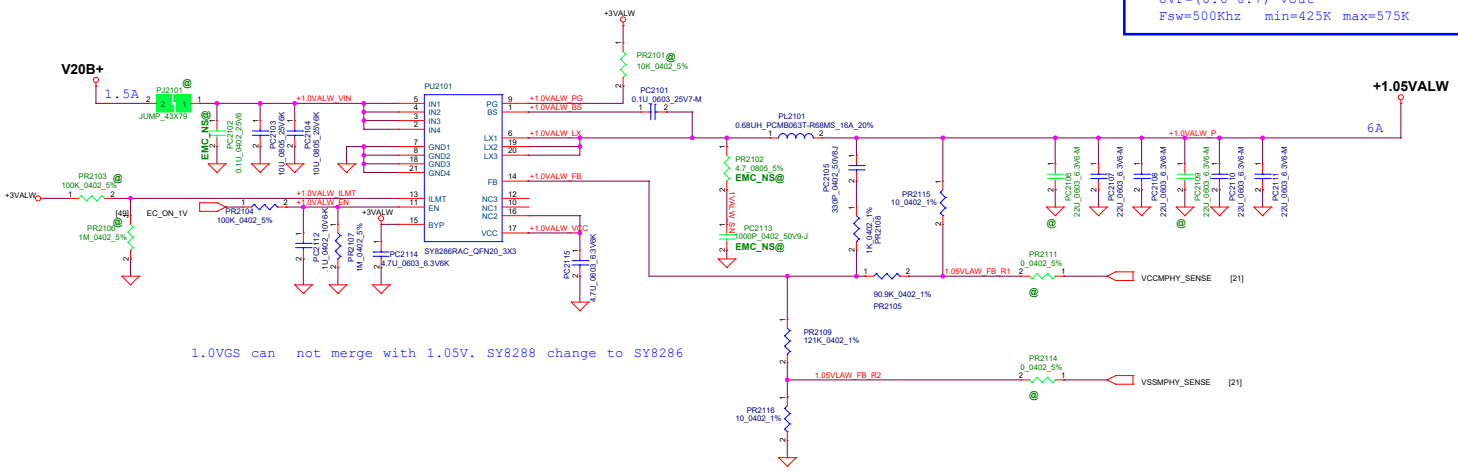


Need again link cis ,only change PN

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-2.5V		
Size: Custom	Document Number: DY520		Rev: 0.1
Date: Tuesday, March 20, 2018	Sheet 62 of 74		

Vout=1.05V± 5%
Vset=1.051V± 1.81%
Vref=0.6V(+-1%)
TDC=8A
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K



1.0VGS can not merge with 1.05V. SY8288 change to SY8286

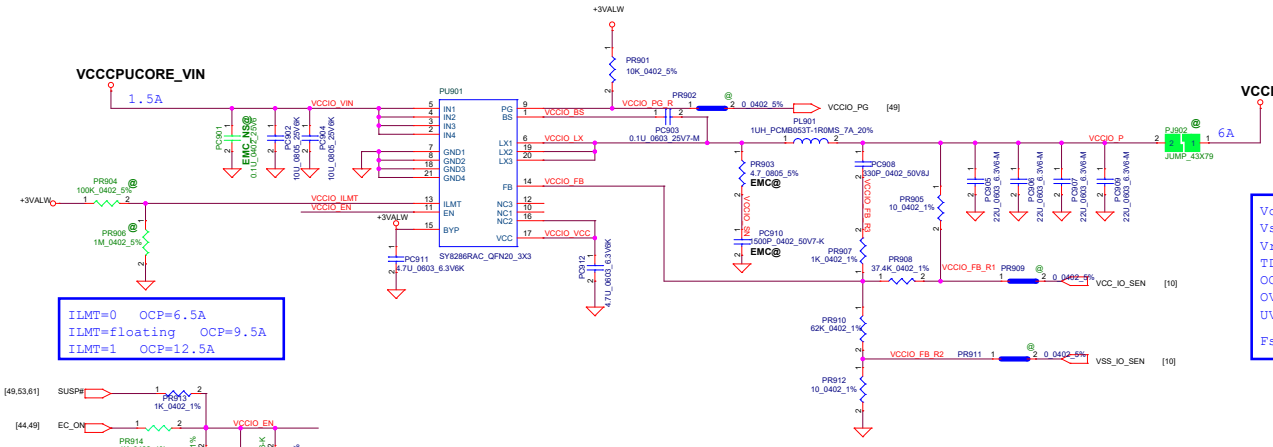
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-1.0VALW

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Tuesday, March 20, 2018 Sheet 63 of 74

VCCIO 20VB+ change to Core VIN for layout



Vout=0.95V± 50mV
Vset=0.962V± 1.78%
Vref=0.6V
TDC=6A
OCP=9.5A TYP=10.5A MAX 11.5A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout

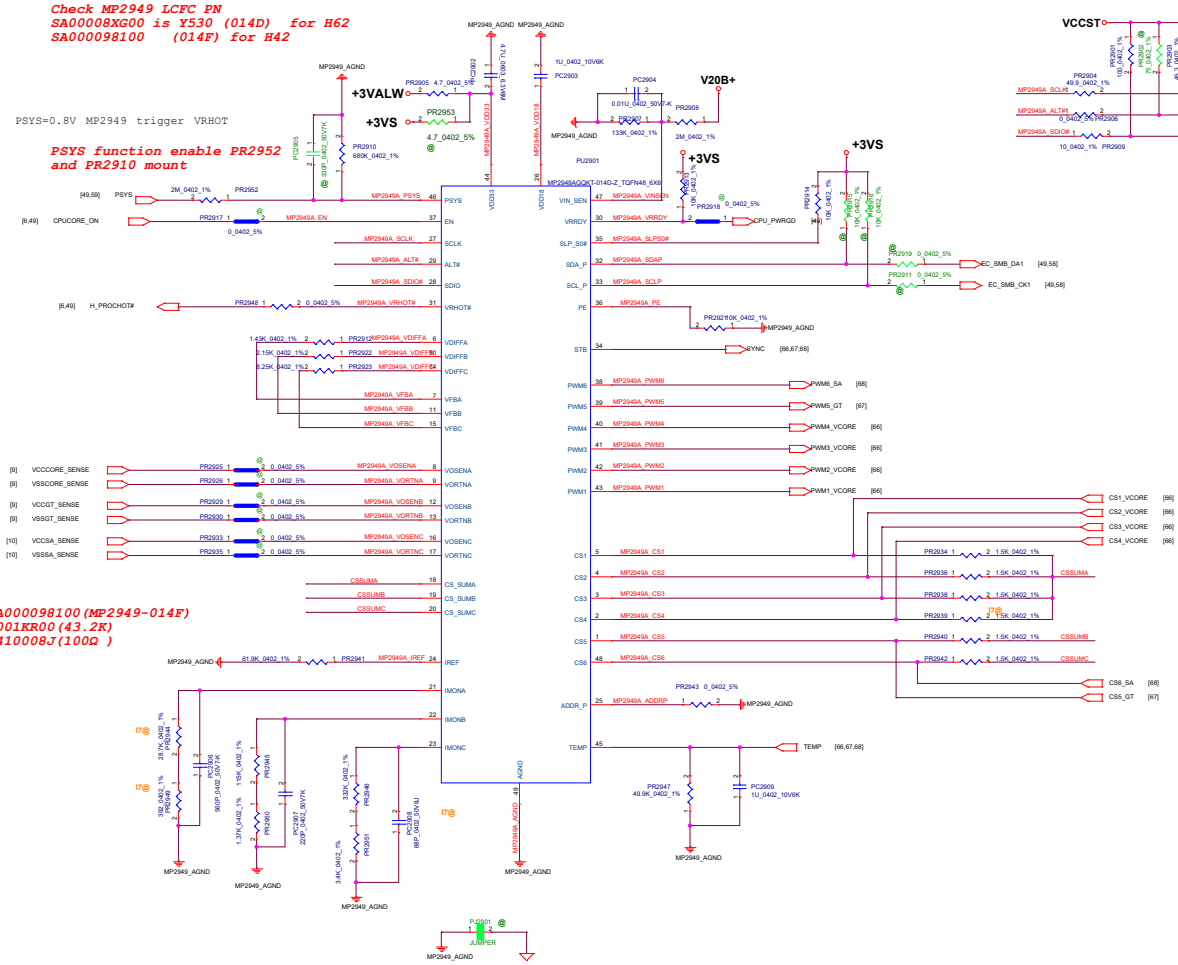
Fsw=500Khz min=425K max=575K

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-VCCIO

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Tuesday, March 20, 2018 Sheet 64 of 74



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Issued Date	2016/01/20	Deciphered Date	2016/01/20

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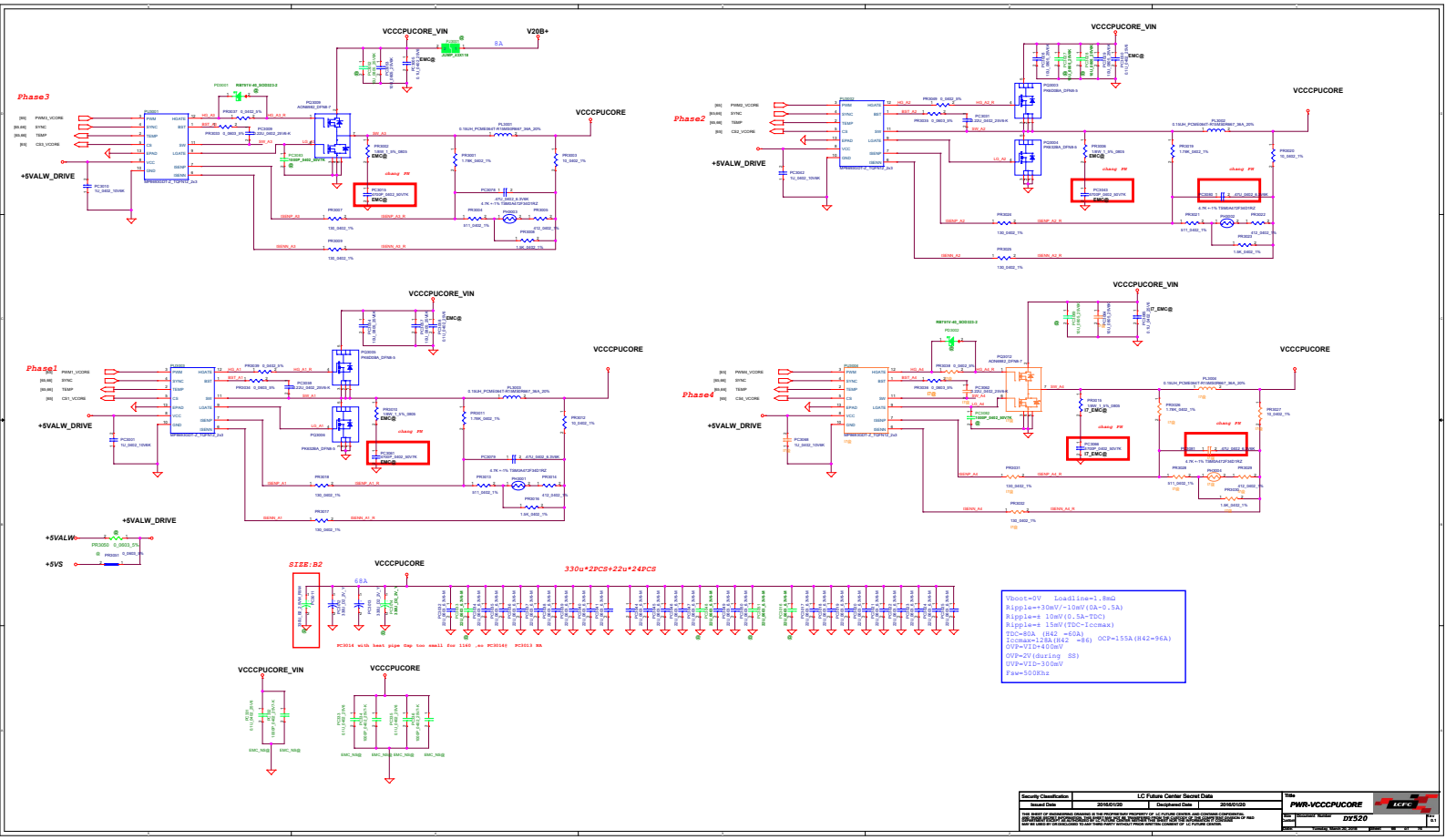
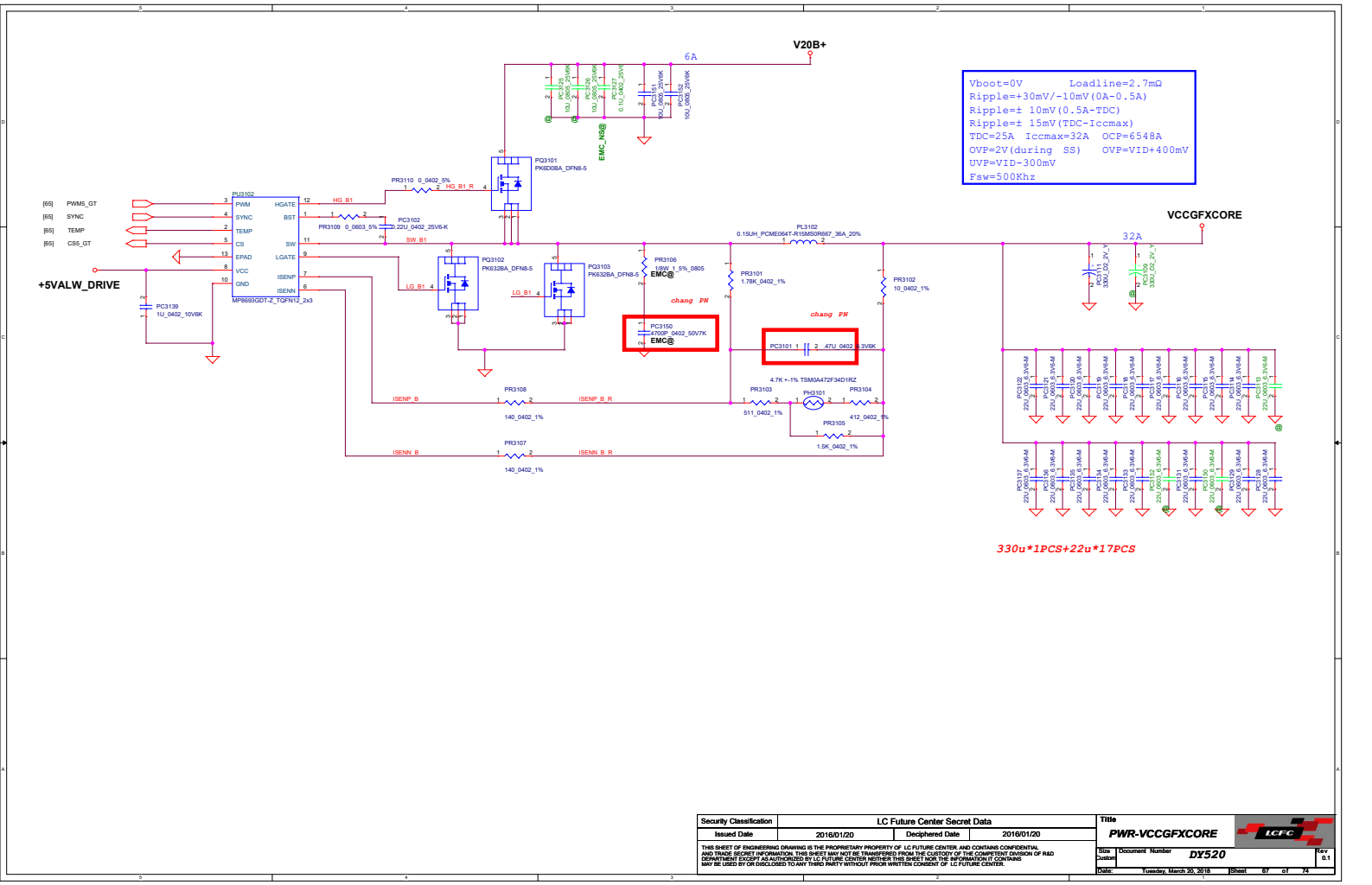
Title	PWR-IMVP8_MP2949		
Size: Custom	Document Number: DY530		Rev: 0.1
Date: Tuesday, March 20, 2018	Sheet 65 of 74		


VCCCPUCORE_VIN
V20B+
VCCCPUCORE
Phase3
Phase2
Phase1
Phase4
+5VALW_DRIVE
+5VALW
+5VS
SIZE:B2
330u*2PCS+22u*24PCS
68A
8A
Vboot=0V Loadline=1.8mΩ
Ripple=+30mV/-10mV(Ia-0.5A)
Ripple=± 10mV(0.5A-TDC)
Ripple=± 15mV(TDC-Iccmax)
TDC=80A (H42 =60A)
Iccmax=128A(H42 =86) OCP=155A(H42=96A)
OVP=VID+400mV
OVP=2V(during SS)
UVP=VID-300mV
Fsw=500Khz
Security Classification
LC Future Center Secret Data
Issued Date
2016/01/20
Deciphered Date
2016/01/20
Title
PWR-VCCCPUCORE
Size
Document Number
DY520
Rev
0.1
Date:
Sheet of



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

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Title: PWR-VCCGFXCORE

Size	Document Number	Rev
Custom	DY520	0.1

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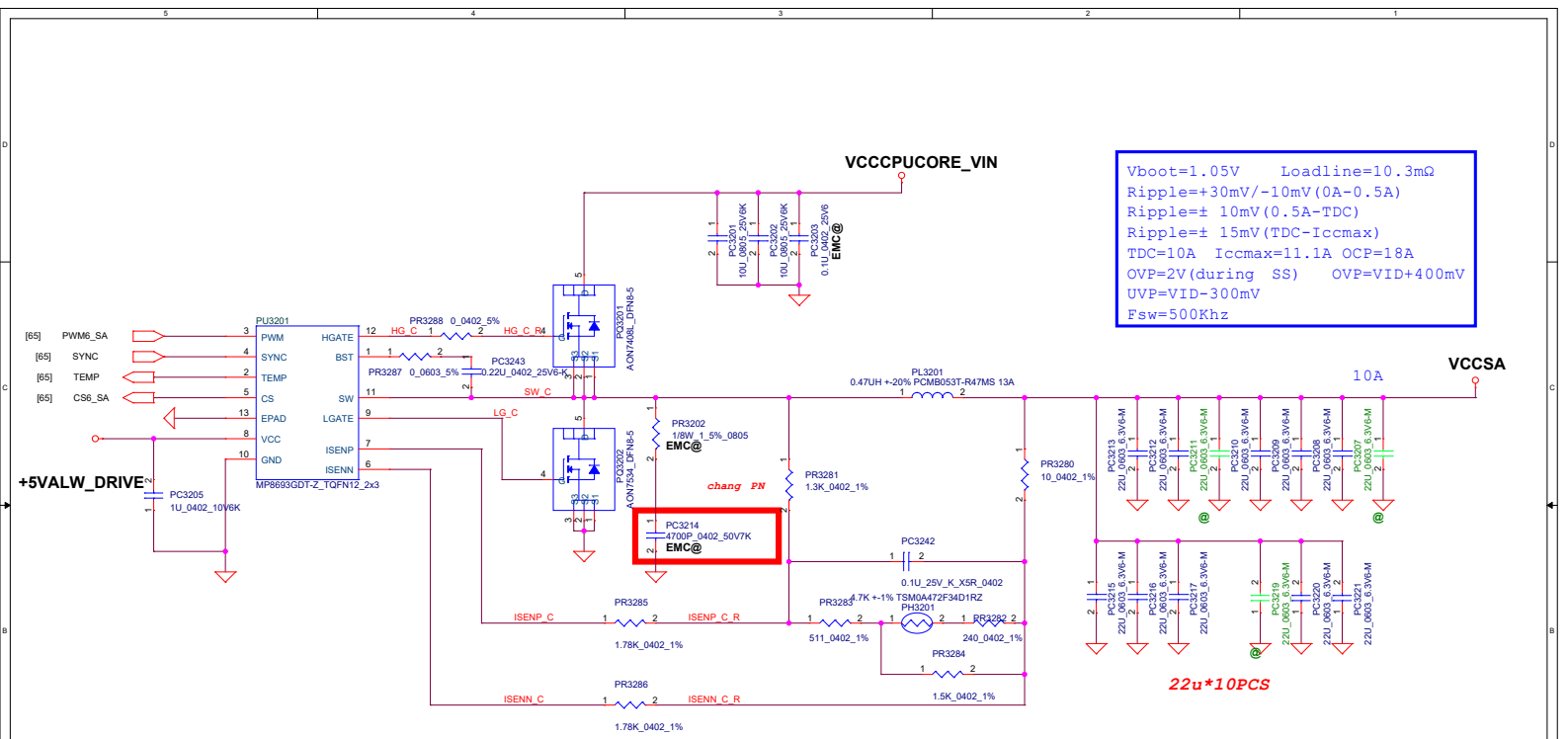
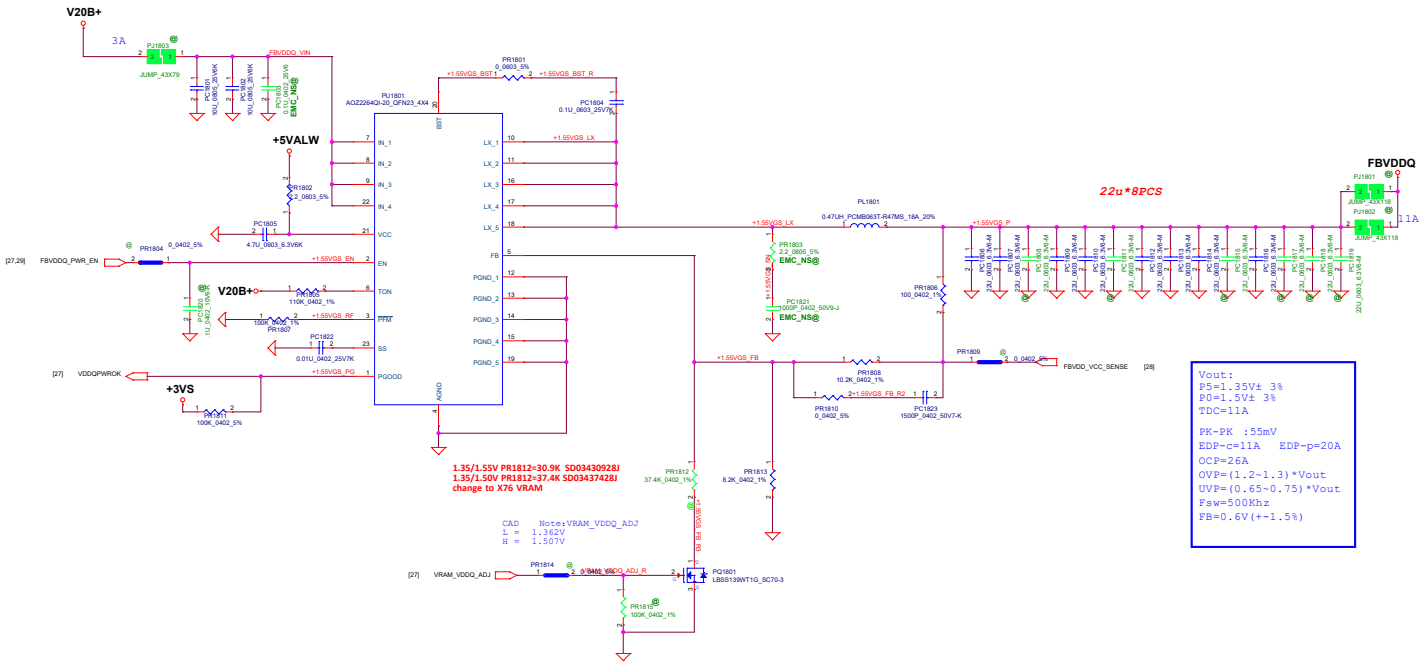


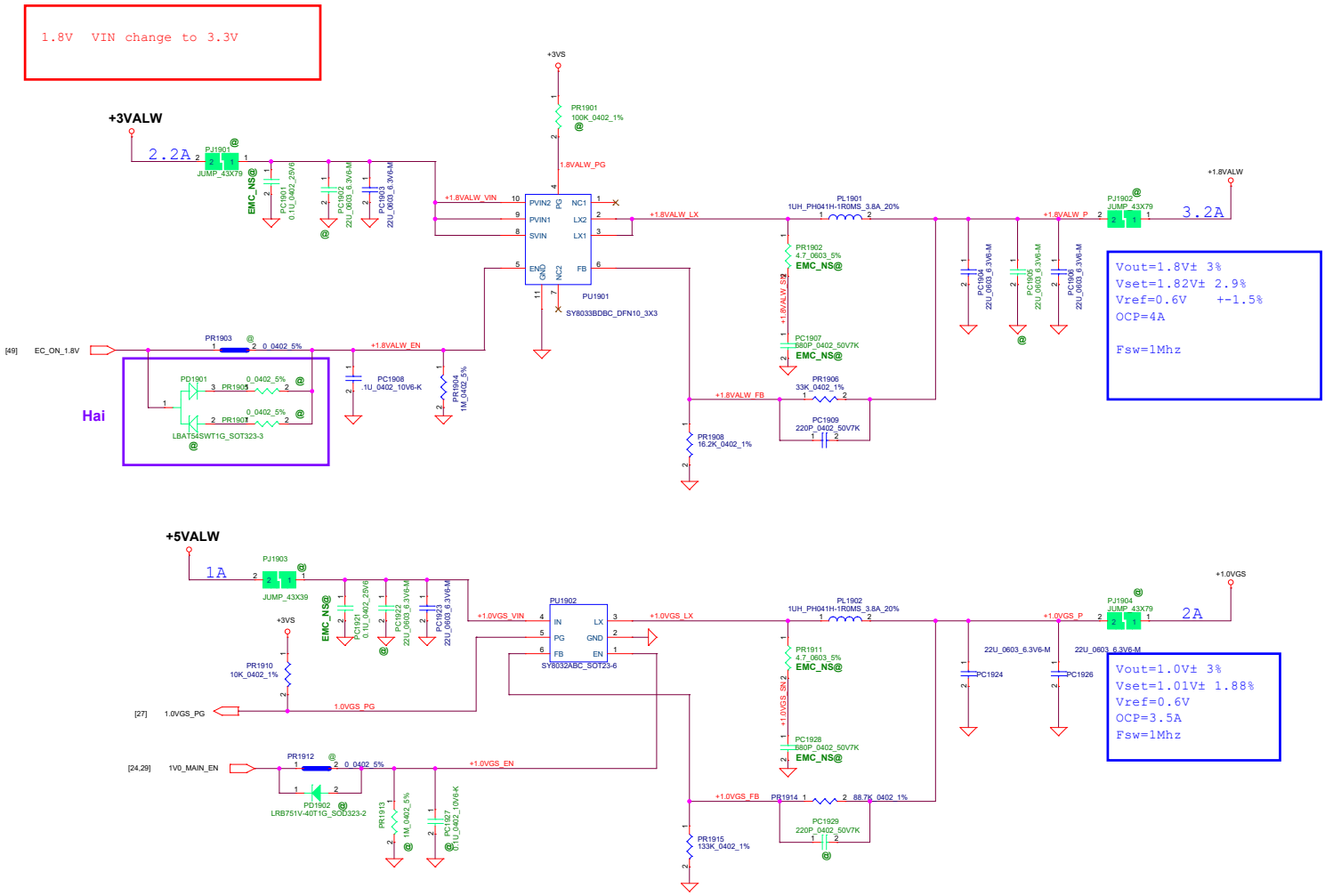
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title			
PWR-VCCSA			
Size: B	Document Number: DY520		Rev: 0.1
Date: Tuesday, March 20, 2018	Sheet 68 of 74		



Security Classification	LC Futures Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-FBVDDQ		
Size	Document Number	DY510/DY511	Rev 1.0
Custom			
Date:	Tuesday, March 29, 2016	Sheet 69 of 74	



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-1.8/1.0VGS**

Size	Document Number	Rev
Custom	DY520	0.1

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PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(Level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR5816	6.19
R2(KΩ)	PR5811	20.5
R3(KΩ)	PR5815	4.32
R4(KΩ)	PR5813	16.5
R5(KΩ)	PR5818	0.309
C(nF)	PC5838	4.7

PSI Level	Power Mode	Phase Configuration
PSI<0.4V	PSH	1Phase DEM
0.8V<PSI<1V	PS0	1Phase FCCM
1.4V<PSI<5.5V	PS1	3Phase FCCM

Vboot=0.8V
Ripple=± 20mV
TDC 50W=59A Iccmax=124A
TDC 40W=50A Iccmax=100A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=345KHz
OCP=190A

50W,330uF*4PCS+22U*11
40W,330uF*3PCS+22U*11
PC5818 for rick require

NVVDD rail ouput cap for debug
EE and Roote sense tie to CPU

PR5822=20K SD03420028J for1050
PR5822=12.1K for1050TI

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Title	PWR-NVVDD	
Size	Document Number	Rev
A	DZ510/DY512	1.0
Date: Tuesday, March 29, 2016	Sheet 21 of 46	

Security Classification	LC Future Center Secret Data
Issued Date	2015/02/26
Deciphered Date	2016/02/26

Title

PWR-Power schematic history

Size: Custom	Document Number: DZ510/DY512	Rev: 1.0
Date: Tuesday, March 29, 2016	Sheet 72 of 74	

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Title		
Blank		
Size D	Document Number DZ510/DY512	Rev 1.0
Date: Tuesday, March 20, 2018	Sheet 73 of 74	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Blank

Size: D

Document Number: DE510/DY512

REV: 1.0

Date: Tuesday, March 29, 2016 Sheet 1 of 1