

# Compal confidential

## *Hamburg 10AD*

### NALAE LA-6053P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

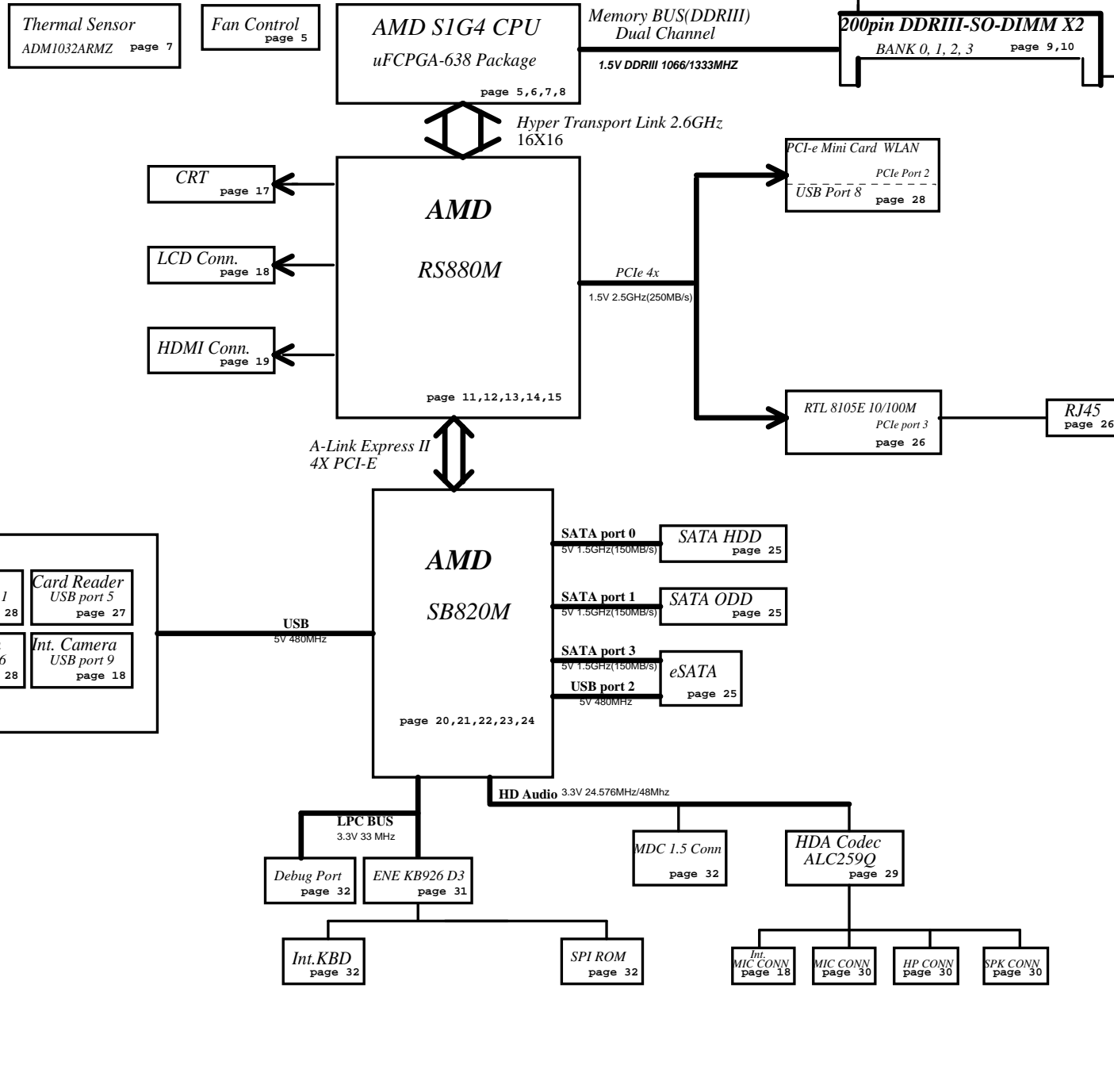
2009-02-04 Rev. 0.2

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Issued Date	2009-02-12	Deciphered Date	2009-02-12	SCHEMATIC, MB A6053	
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Model Name : NALAE

File Name : LA-6053P



**Clock Generator**  
SLG8SP626 page 16

**RTC CKT.**  
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**Power On/Off CKT.**  
page 33

**DC/DC Interface CKT.**  
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**Power Circuit DC/DC**  
page 35,36,37,38,39,40,41

**ODD/B**  
Page 25

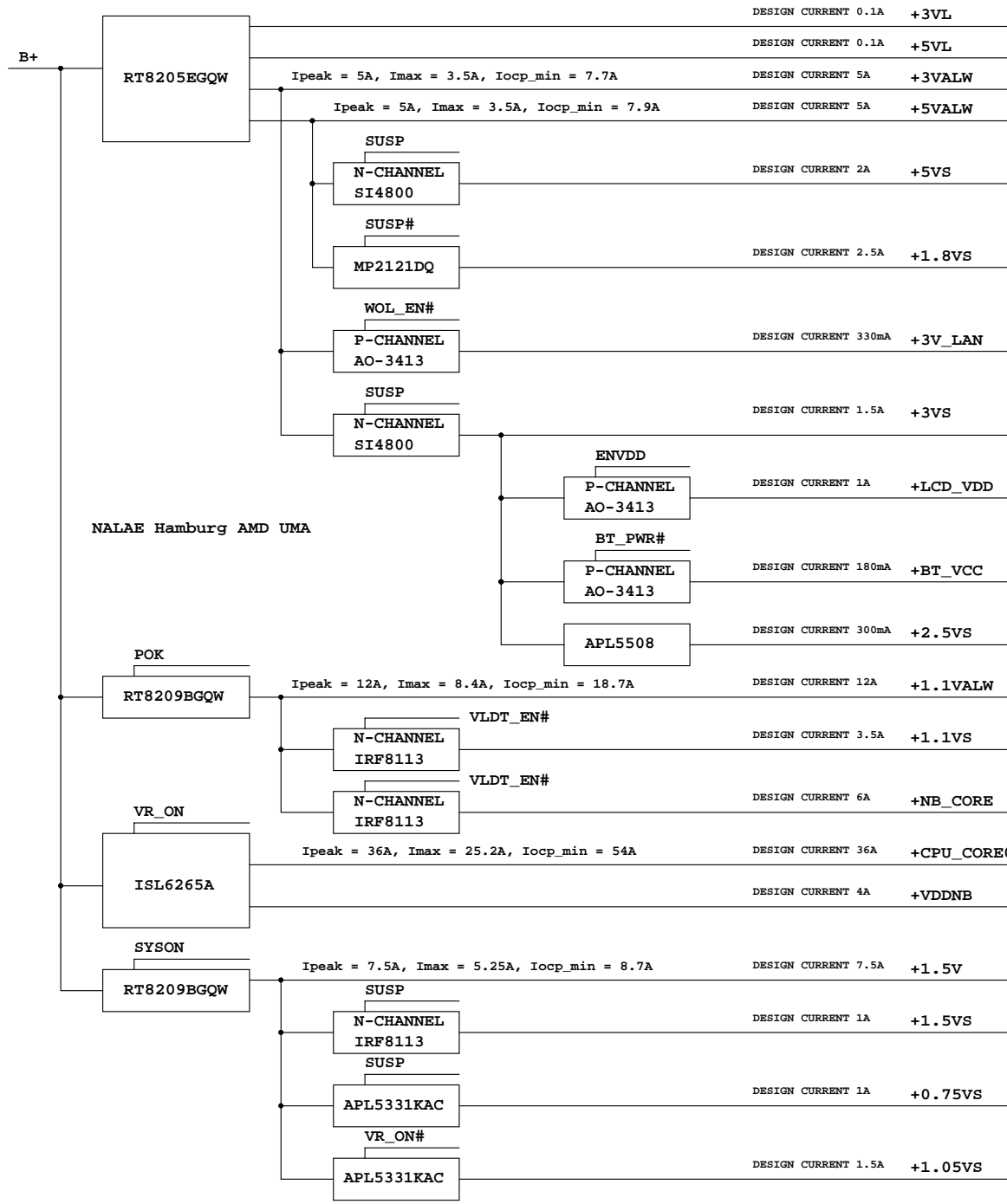
**Power/B**  
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**Audio & USB/B**  
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**LED/B**  
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**Touch Pad/B**  
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## Voltage Rails

O : ON  
X : OFF

power plane State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VDDNB +CPU_CORE +NB_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

@ : just reserve , no build

## BTO (Build-To-Order) Option Table

Function	BLUE TOOTH	HDMI				
Description	( B )	( Y )				
Explain						
BTO	BT@	H@				

## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A2	10100010
CLOCK GENERATOR (EXT.)	D2	11010010

## EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D3		

## EC SM Bus2 address

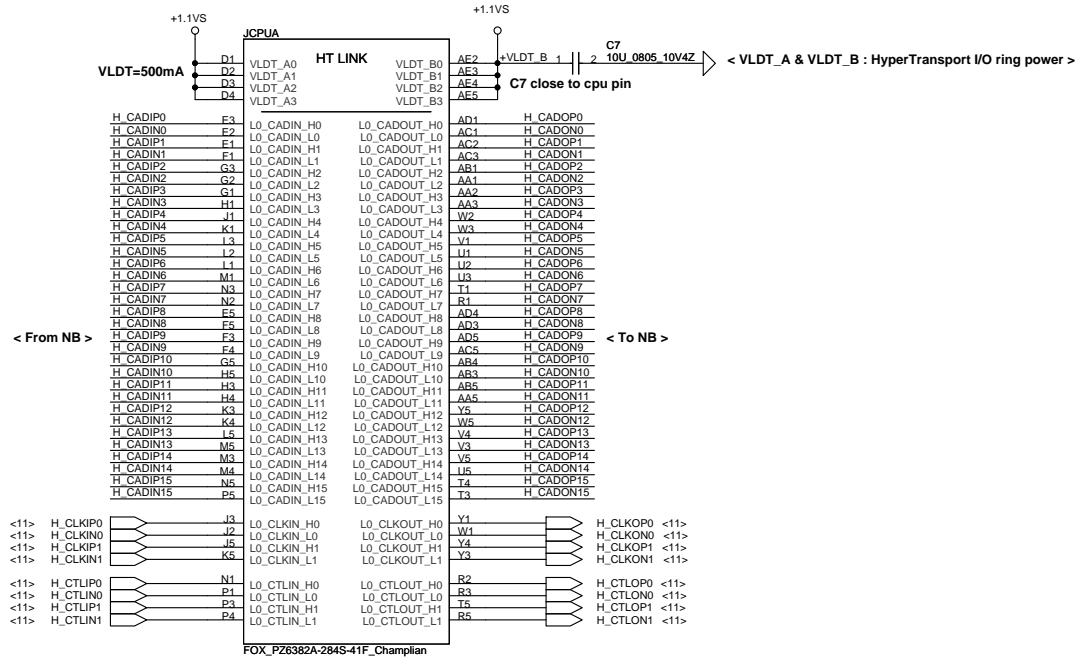
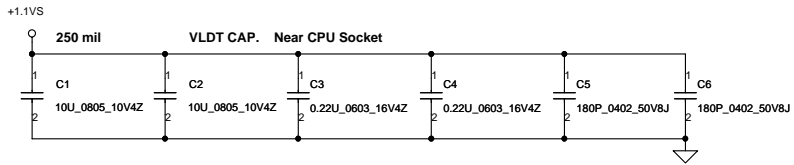
Device	HEX	Address
ADH1032-1 CPU	98H	1001 100X b
ADH1032-2 VGA	9AH	1001 101X b
EC KB926D3		

## SMBUS Control Table

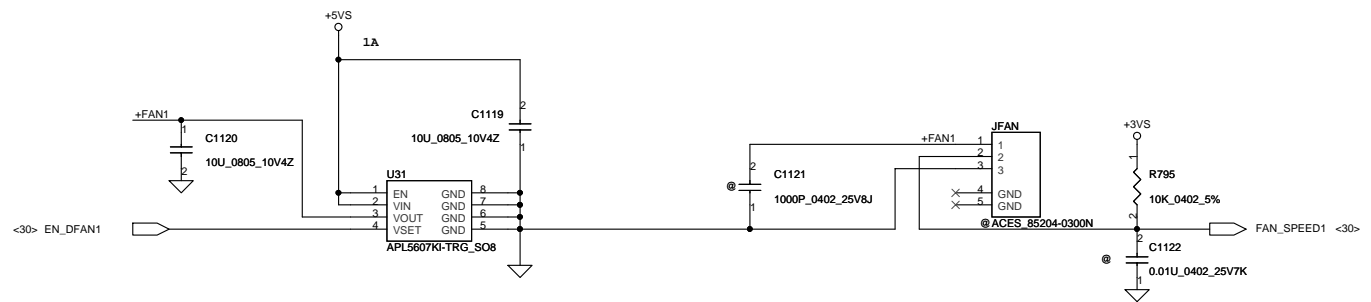
	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V						
EC_SMB_CK2 EC_SMB_DA2	KB926		V					
I2C_CLK I2C_DATA	RS880M						V	
DDC_CLK0 DDC_DATA0	RS880M							V
SCL0 SDA0	SB820			V	V			
SCL1 SDA1	SB820					V		

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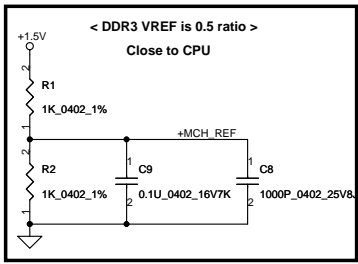
SCHEMATIC.MB A6053



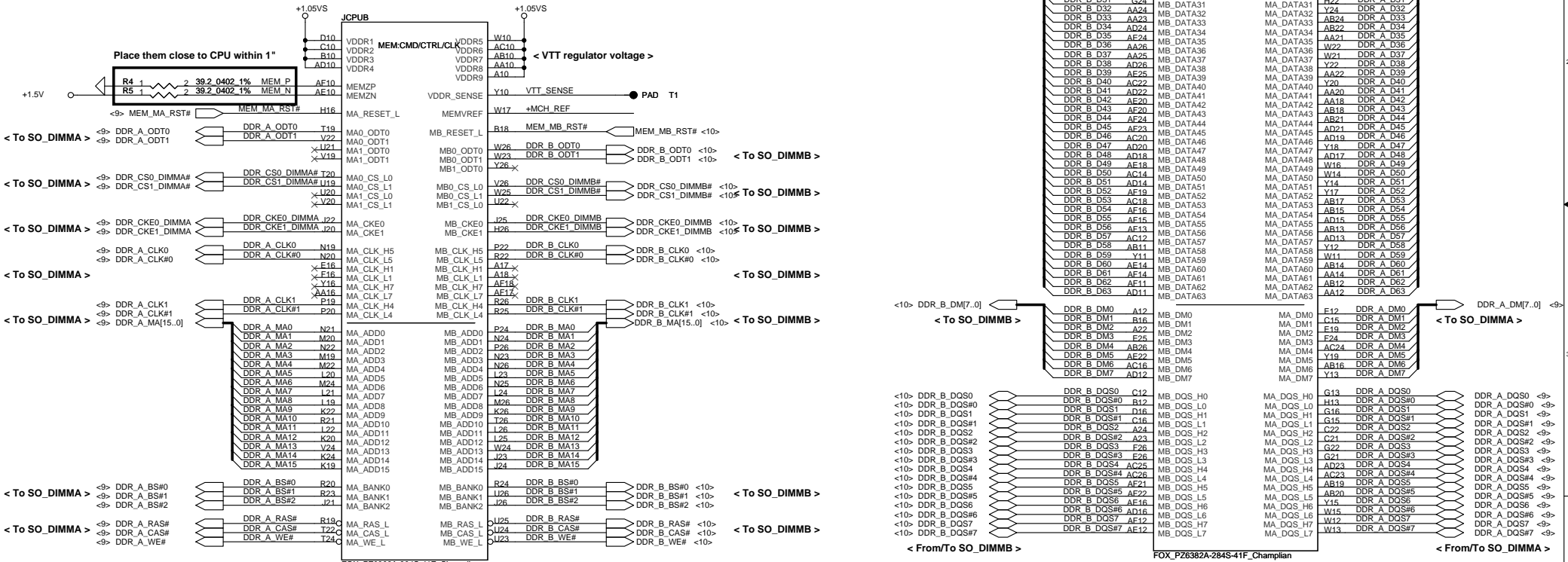
< FAN Control Circuit : Vout = 1.6 x Vset >



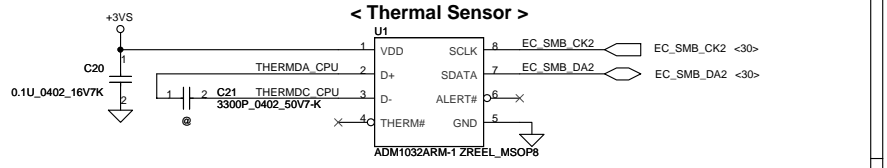
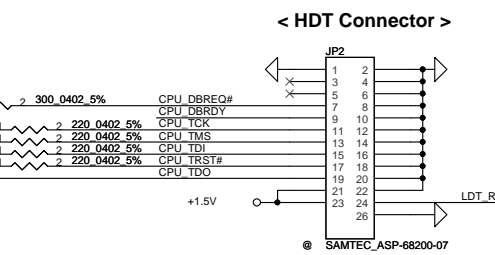
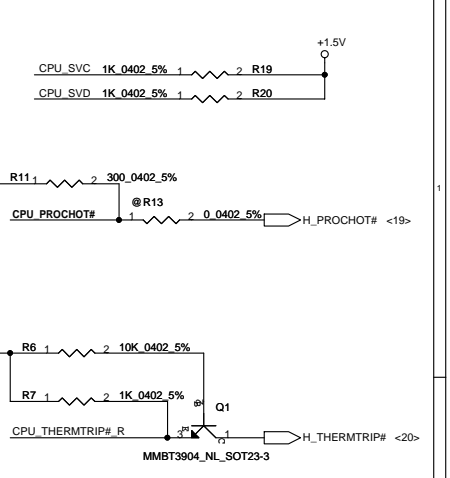
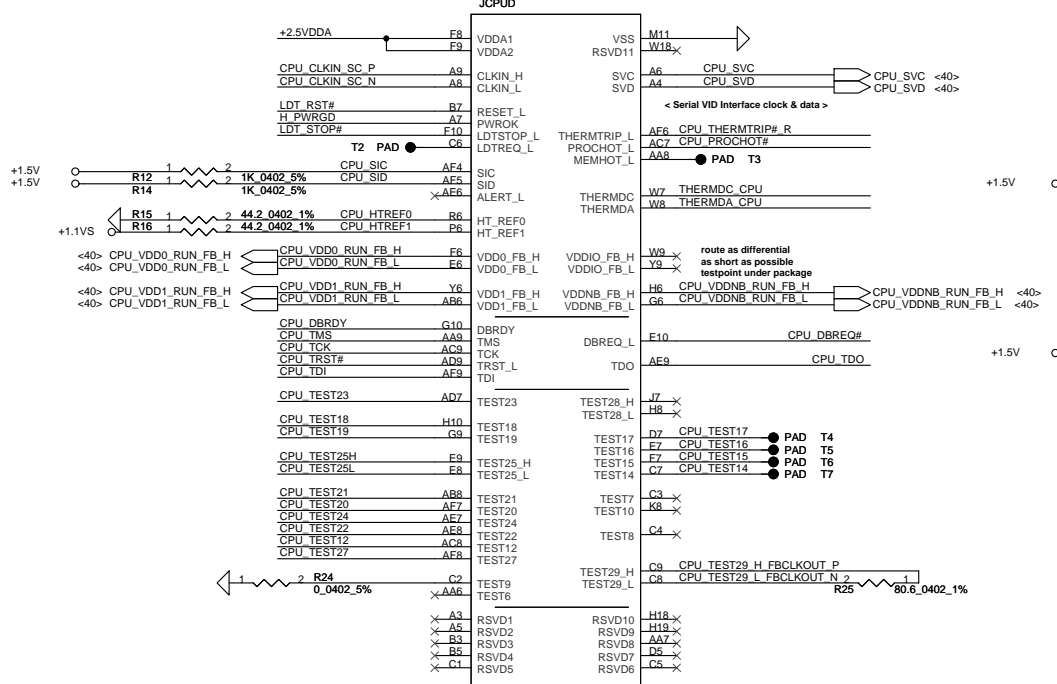
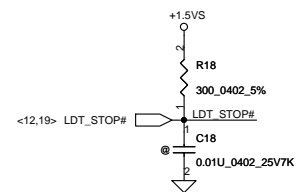
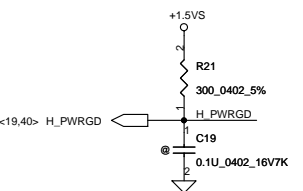
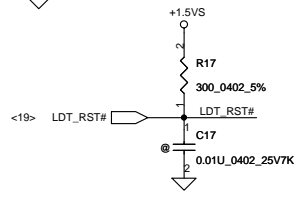
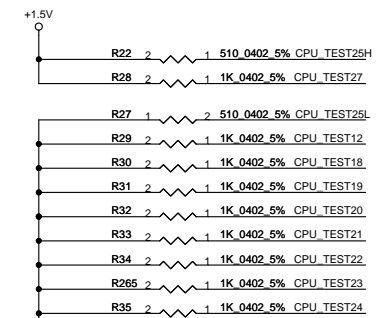
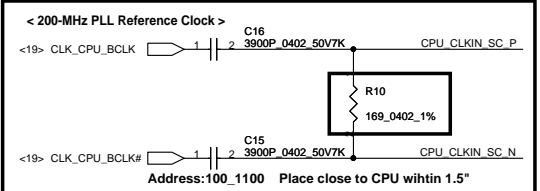
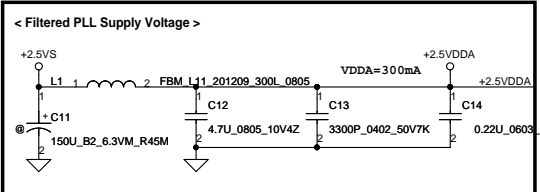
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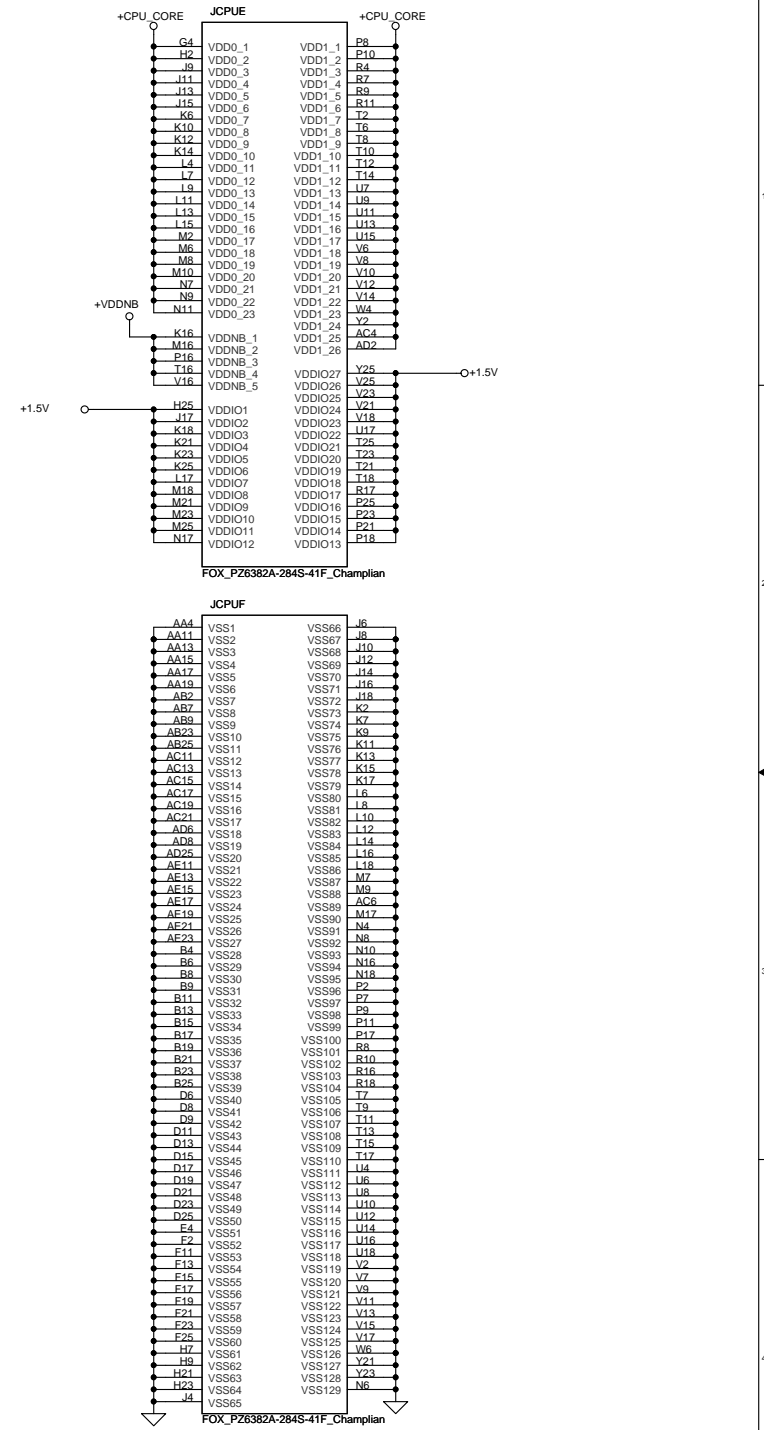
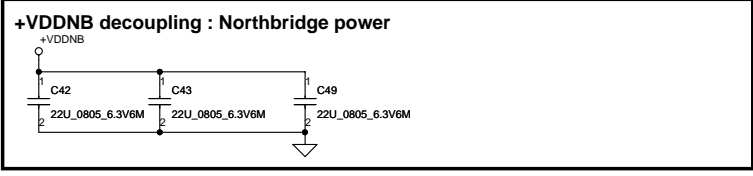
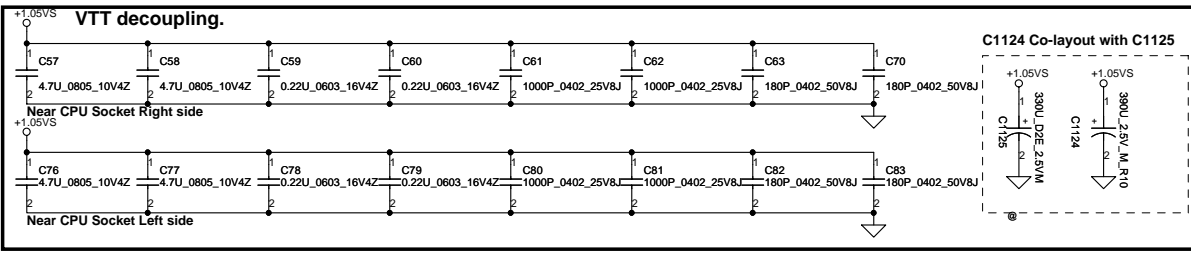
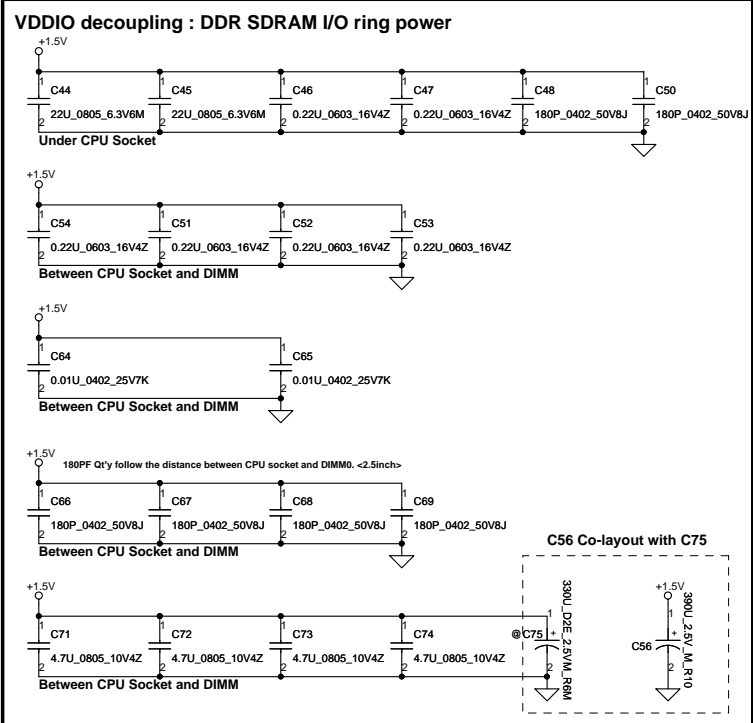
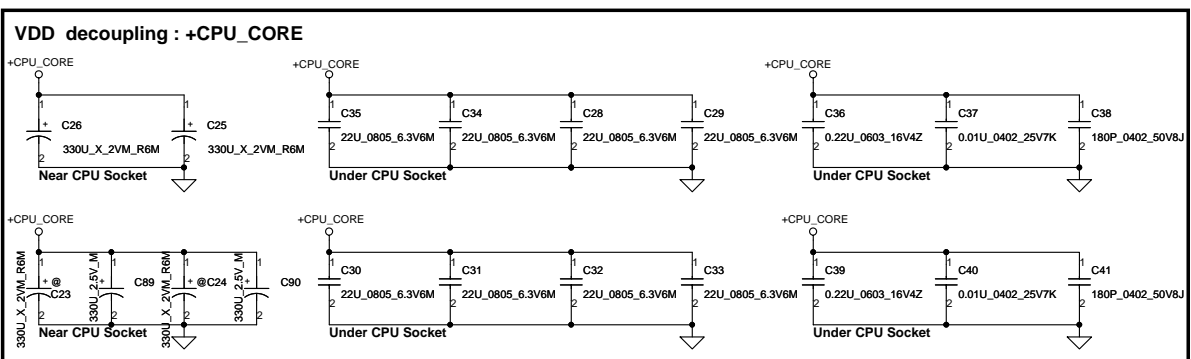
< Processor DDR3 Memory Interface >



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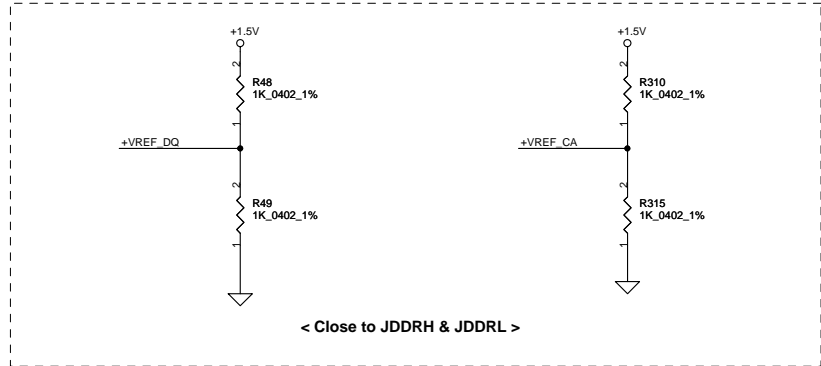
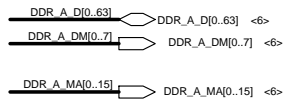
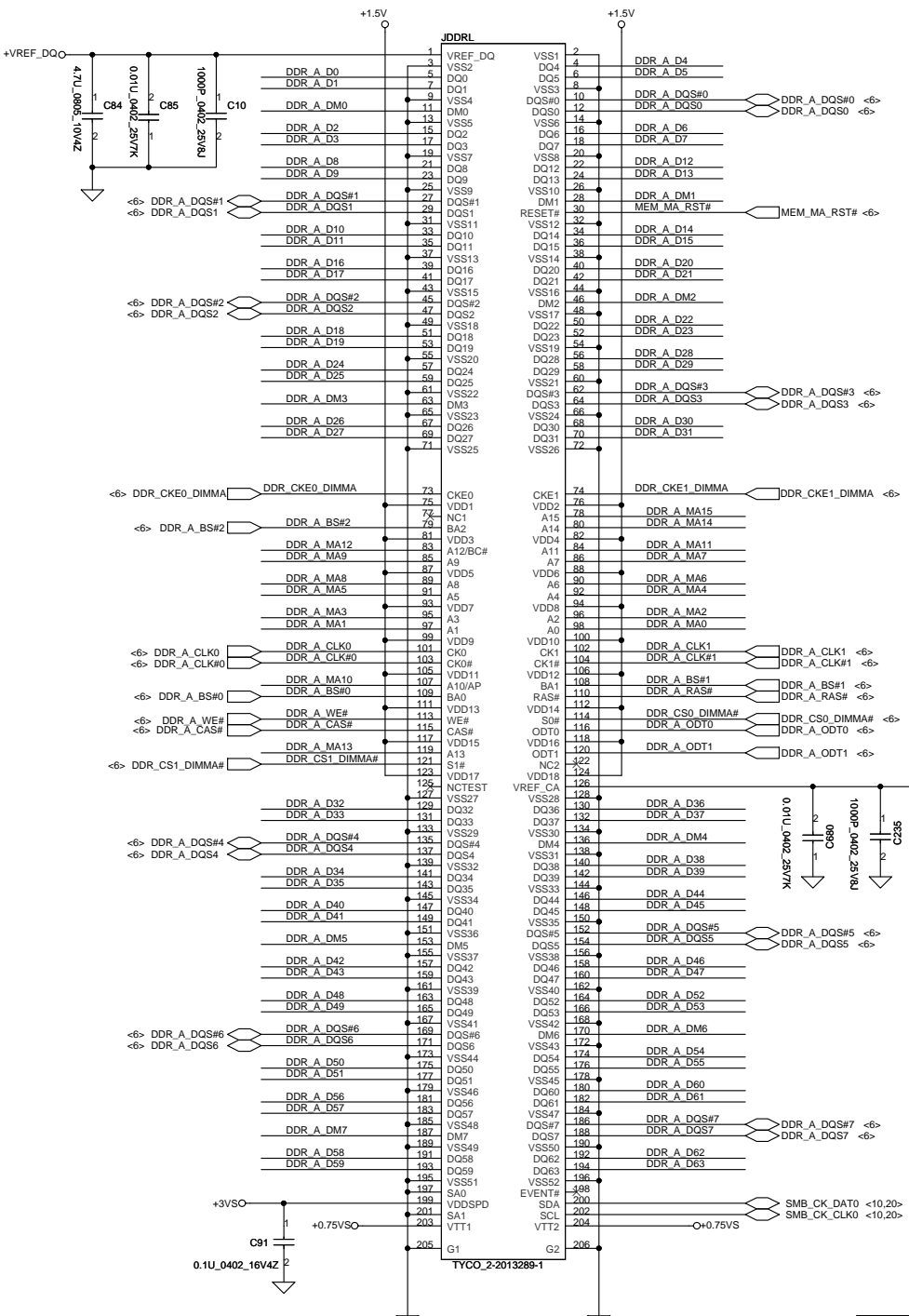


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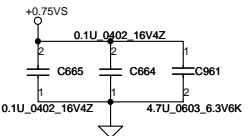
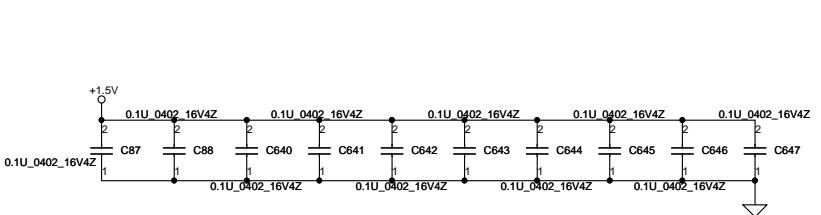


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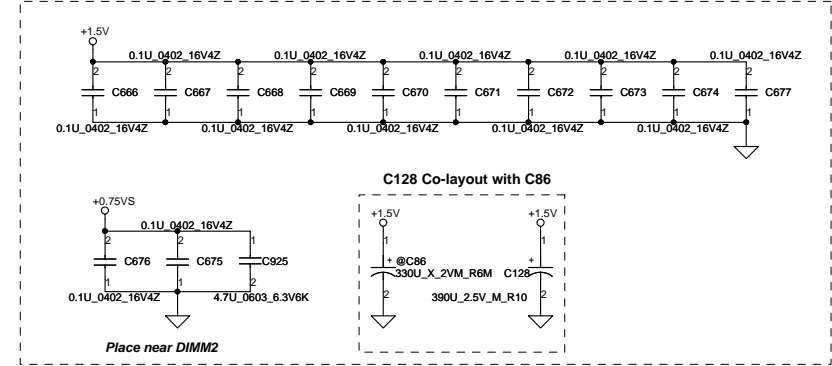
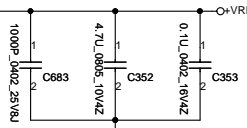
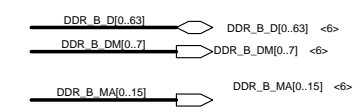
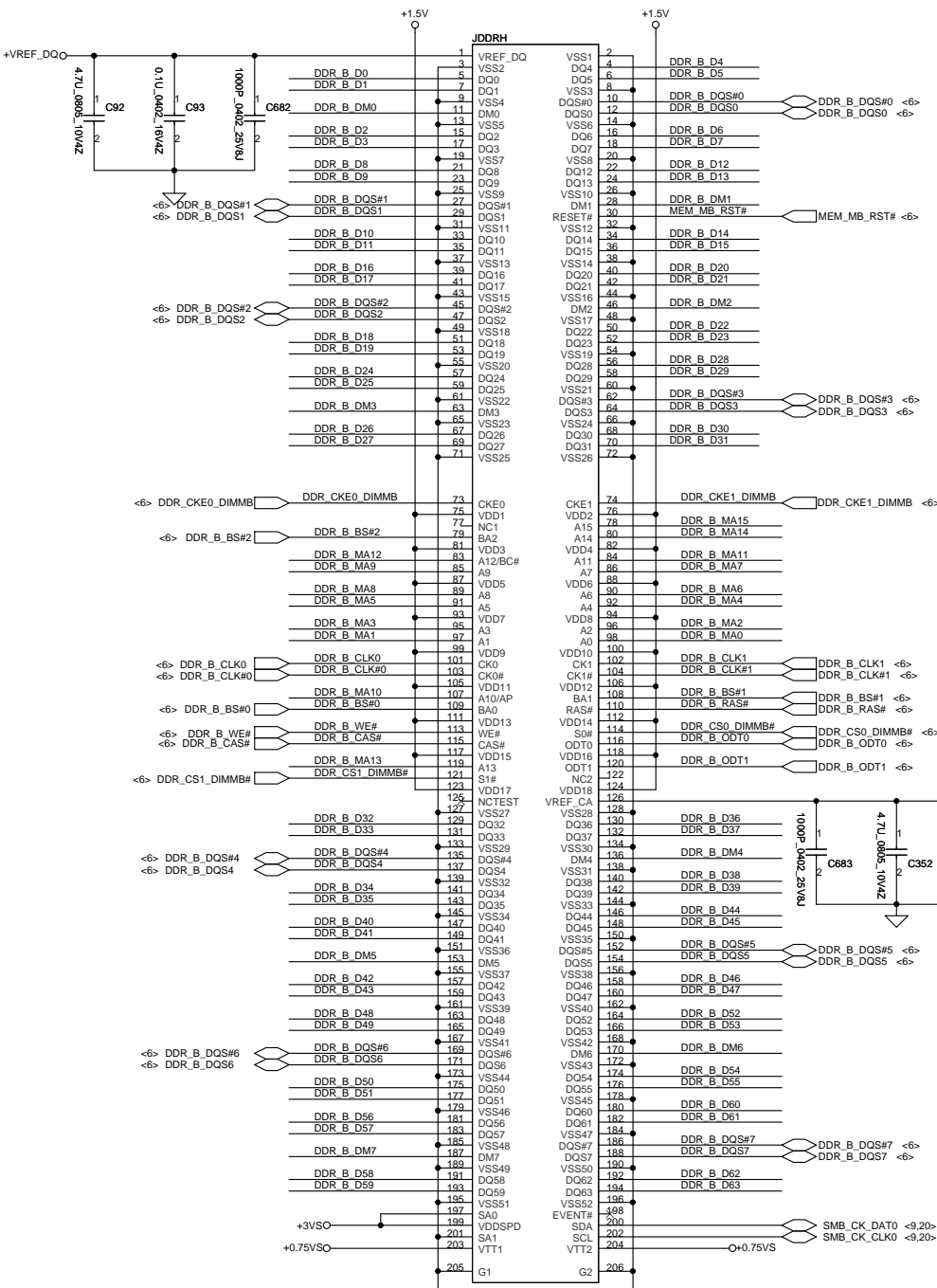
< Close to JDDRH & JDDRL >



Place near DIMM1

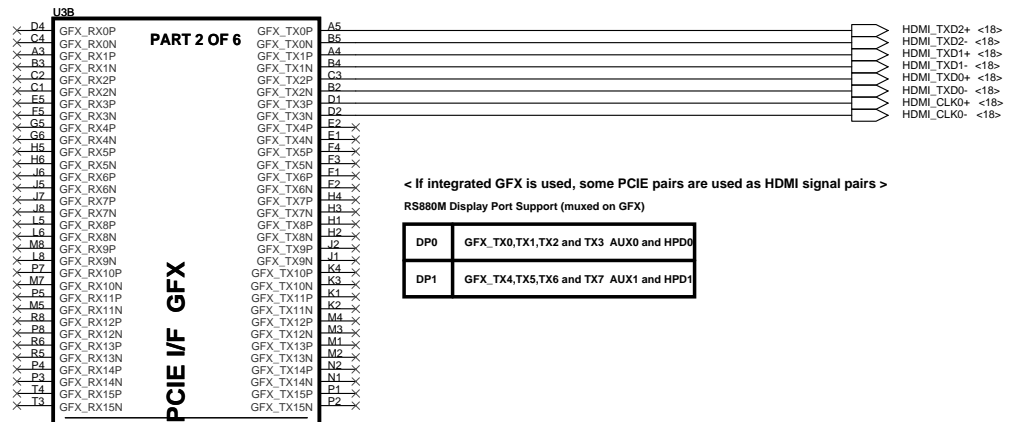
**DIMM\_A STD H:5.2 mm**  
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**DIMM\_B STD H:9.2mm**  
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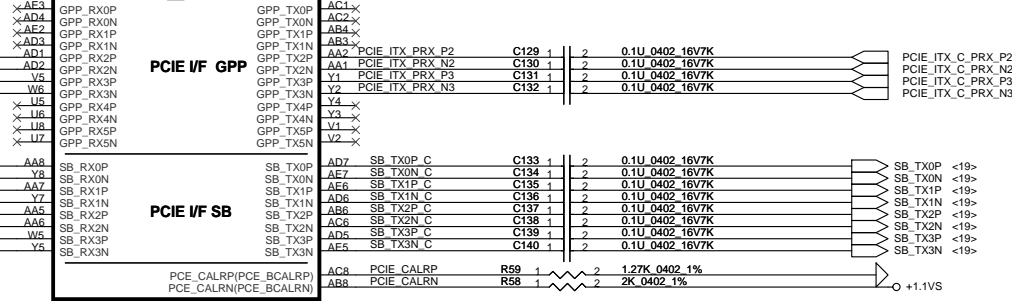
< To WLAN >  
 < To LAN >

< From SB820 : x4 PCIE A-link >

H\_CADOP0[0..15] H\_CADOP[0..15] <5>  
 H\_CADON[0..15] H\_CADON[0..15] <5>

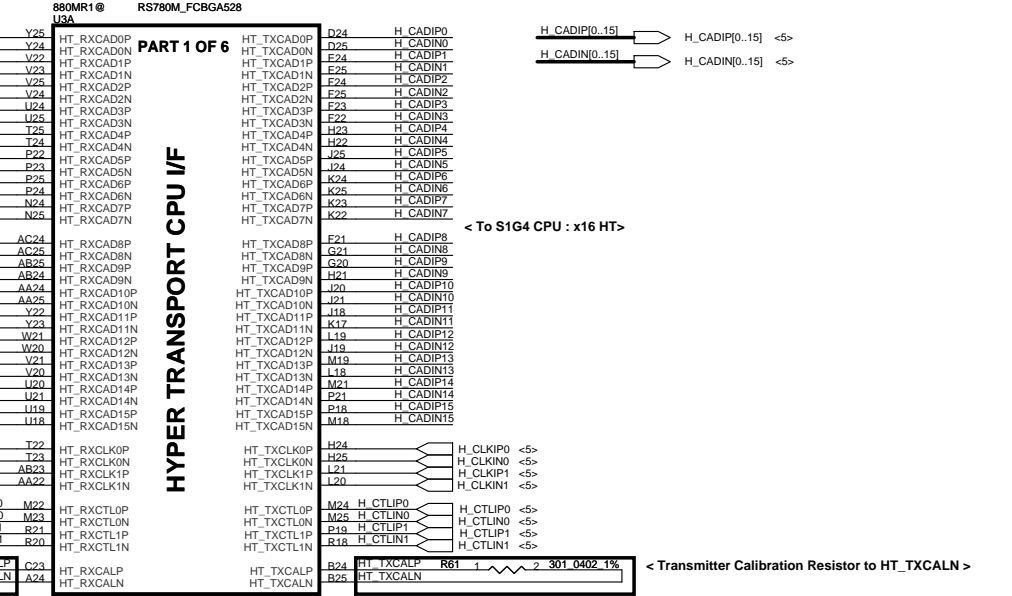
< From S1G4 CPU : x16 HT >

0718 Place within 1" layout 1:2



< To SB820 : x4 PCIE A-link >

< TX Impedance Calibration. Connect to GND >  
 < RX Impedance Calibration. Connect to VDDPCE >

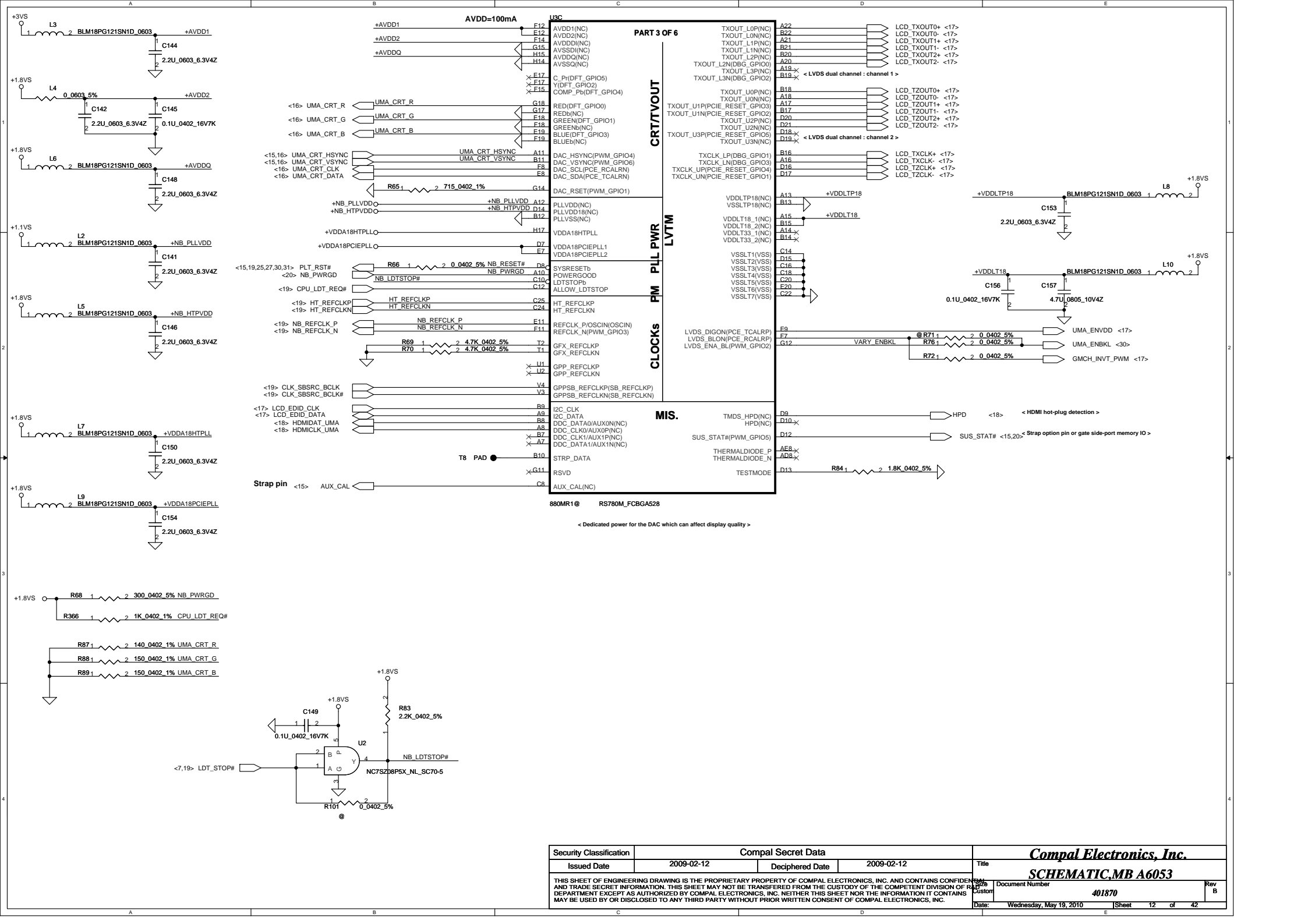


0718 Place within 1" layout 1:2

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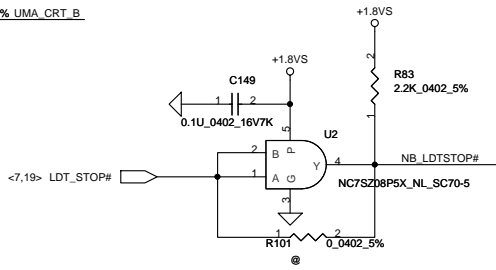
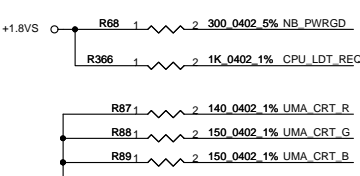
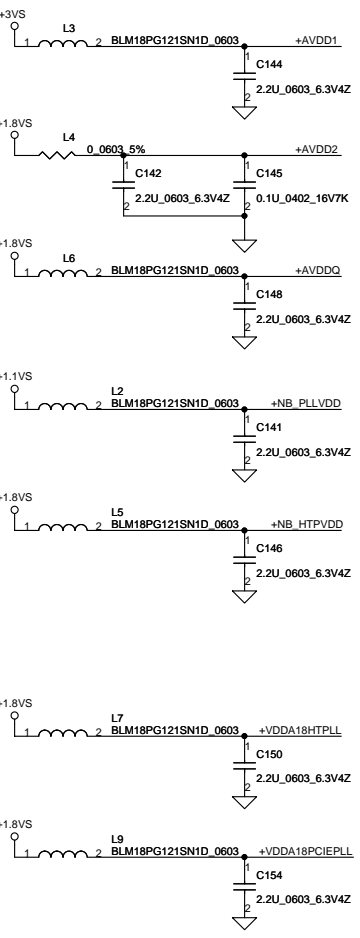


Pin	Signal Name	Notes
F12	AVDD1(100mA)	
F12	AVDD2(100mA)	
F14	AVDD3(100mA)	
G15	AVSSD1(100mA)	
H15	AVSSD2(100mA)	
H14	AVSSQ(100mA)	
E17	C_Pi(DFT_GPIO5)	
F17	Y(DFT_GPIO2)	
F15	COMP_Pi(DFT_GPIO4)	
G19	RED(DFT_GPIO0)	
G17	REDb(100mA)	
F18	GREEN(DFT_GPIO1)	
F18	GREENb(100mA)	
E19	BLUE(DFT_GPIO3)	
F19	BLUEb(100mA)	
A11	UMA CRT HSYNC	
B11	UMA CRT VSYNC	
F8	UMA CRT_CLK	
E8	UMA CRT_DATA	
G14	DAC_RSET(PWM_GPIO1)	
A12	PLLVDD(100mA)	
D14	PLLVSS(100mA)	
B12	HTPVDD	
H17	VDDA18HTPLL	
D7	VDDA18PCIEPLL1	
E7	VDDA18PCIEPLL2	
D8	NB_RESET#	
A10	NB_PWRGD	
C10	NB_LDTSTOP#	
C12	CPU_LDT_REQ#	
C25	HT_REFCLKP	
C24	HT_REFCLKN	
E11	NB_REFCLK_P	
F11	NB_REFCLK_N	
T9	GFX_REFCLKP	
T8	GFX_REFCLKN	
U1	GPP_REFCLKP	
U2	GPP_REFCLKN	
V4	GPPSB_REFCLKP(SB_REFCLKP)	
V3	GPPSB_REFCLKN(SB_REFCLKN)	
B9	I2C_CLK	
A9	I2C_DATA	
B8	DDC_DATA0(AUX0)(NC)	
A8	DDC_CLK0(AUX0)(NC)	
B7	DDC_CLK1(AUX1)(NC)	
A7	DDC_DATA1(AUX1)(NC)	
B10	STRP_DATA	
C8	AUX_CAL	

Pin	Signal Name	Notes
A22	LCD_TXOUT0+ <17>	
B22	LCD_TXOUT0- <17>	
A21	LCD_TXOUT1+ <17>	
B21	LCD_TXOUT1- <17>	
B20	LCD_TXOUT2+ <17>	
A20	LCD_TXOUT2- <17>	
A19	< LVDS dual channel : channel 1 >	
B19	< LVDS dual channel : channel 1 >	
B18	LCD_TZOUT0+ <17>	
A18	LCD_TZOUT0- <17>	
B17	LCD_TZOUT1+ <17>	
A17	LCD_TZOUT1- <17>	
D20	LCD_TZOUT2+ <17>	
D21	LCD_TZOUT2- <17>	
D18	< LVDS dual channel : channel 2 >	
D19	< LVDS dual channel : channel 2 >	
B16	LCD_TXCLK+ <17>	
A16	LCD_TXCLK- <17>	
D17	LCD_TZCLK+ <17>	
D17	LCD_TZCLK- <17>	
A13	+VDDLTP18	
B13	VDDLTP18	
A15	+VDDLTP18	
B15	VDDLTP18	
A14	< LVDS dual channel : channel 1 >	
B14	< LVDS dual channel : channel 1 >	
C14	VSSLT1(VSS)	
D15	VSSLT2(VSS)	
C16	VSSLT3(VSS)	
C18	VSSLT4(VSS)	
C20	VSSLT5(VSS)	
E20	VSSLT6(VSS)	
C22	VSSLT7(VSS)	
E9	UMA_ENVDD <17>	
F7	UMA_ENBKL <30>	
G12	GMCH_INV_T_PWM <17>	
D9	HPD <18>	< HDMI hot-plug detection >
D10	HPD(NC)	
D12	SUS_STAT# <15,20>	< Strap option pin or gate side-port memory IO >
A8	THERMALDIODE_P	
A8	THERMALDIODE_N	
D13	TESTMODE	

880MR1@ RS780M\_FCBGA528

< Dedicated power for the DAC which can affect display quality >



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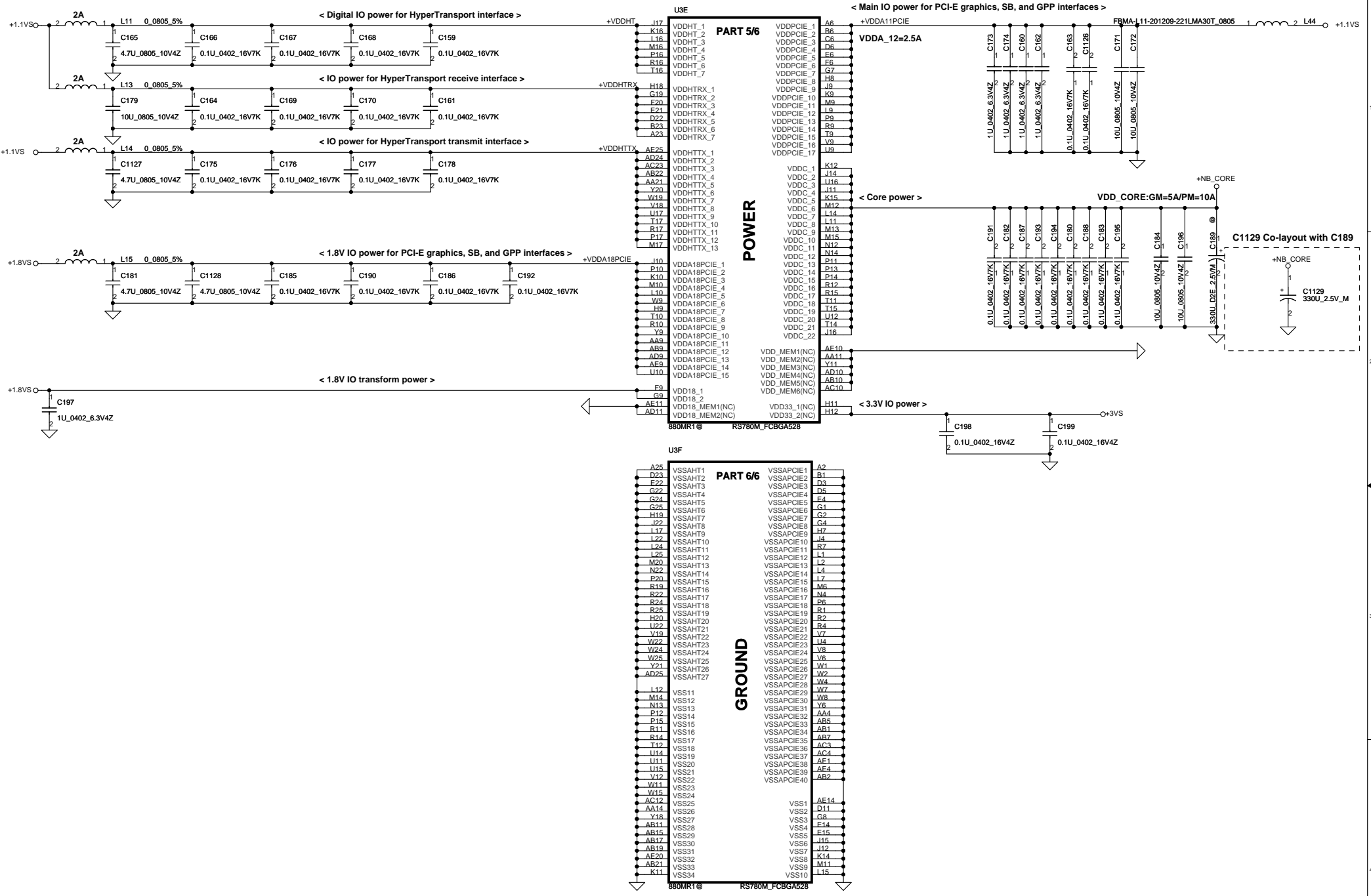
U3D

PAR 4 OF 6

AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
Y11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA15
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)	AC22
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)	AD21
AD17	MEM_BA2(NC)		
W12	MEM_RASb(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17
Y12	MEM_CASb(NC)	MEM_DQS0N/DVO_IDCKN(NC)	W18
AD18	MEM_WEB(NC)	MEM_DQS1P(NC)	AD20
AB13	MEM_CSB(NC)	MEM_DQS1N(NC)	AE21
AB13	MEM_CKE(NC)	MEM_DM0(NC)	W17
Y14	MEM_ODT(NC)	MEM_DM1/DVO_D8(NC)	AE19
W15	MEM_CKP(NC)	IOPLLVD18(NC)	AE23
W14	MEM_CKN(NC)	IOPLLVD1(NC)	AE24
AE12	MEM_COMPp(NC)	IOPLLVS(NC)	AD23
AD12	MEM_COMPn(NC)	MEM_VREF(NC)	AE18

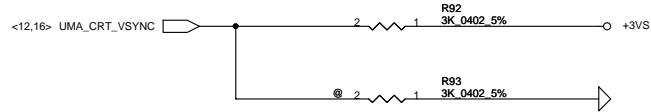
880MR1@ RS780M\_FCBGA528

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< RS880 VSYNC mux at CRT\_VSYNC pull High to 3K >



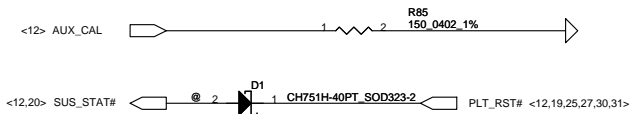
< VSYNC : STRAP\_DEBUG\_BUS\_GPIO\_ENABLE# >

Enables the Test Debug Bus using GPIO.

0 : Enable  
1 : Disable

PIN: RS880--> VSYNC

< RS880 SUS\_STAT# >



< SUS\_SATA# : LOAD\_EEPROM\_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS\_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

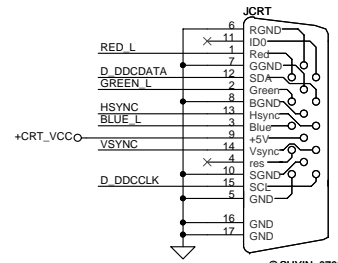
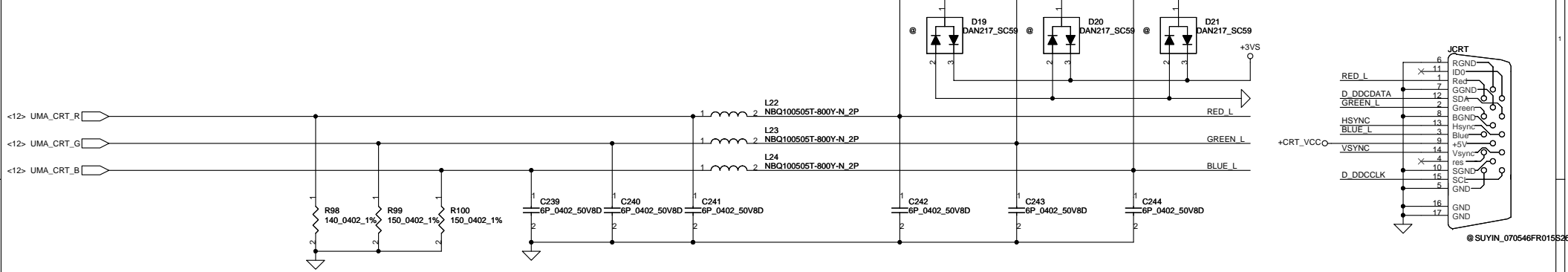
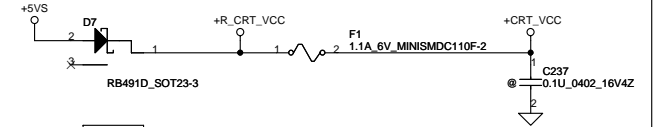
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

RS880: Enables Side port memory ( RS780 use HSYNC#)

1. Disable (RS880)  
0 : Enable (RS880)

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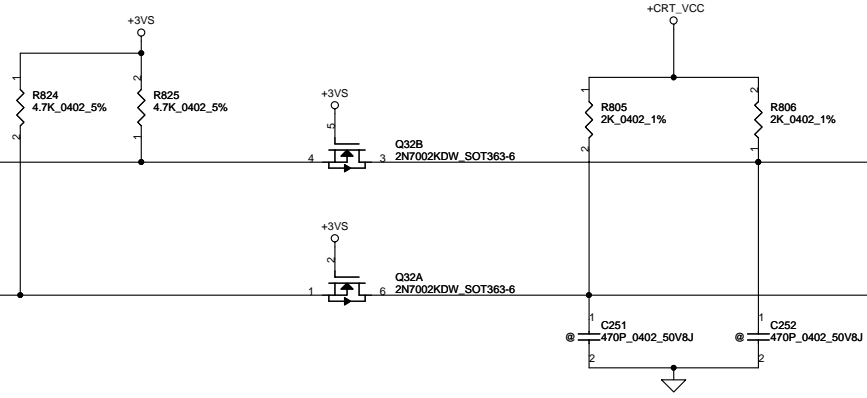
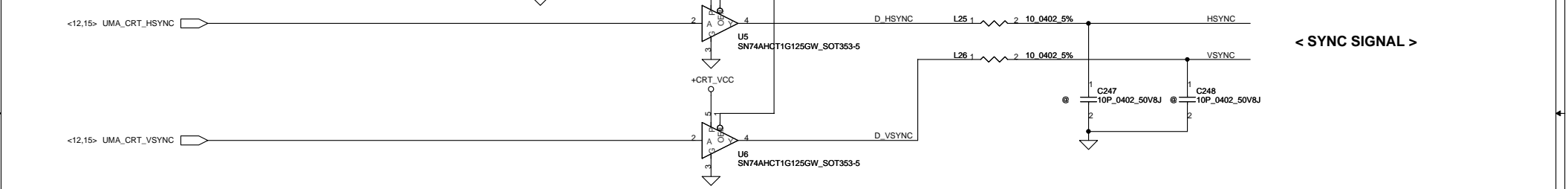
< CRT CONNECTOR >



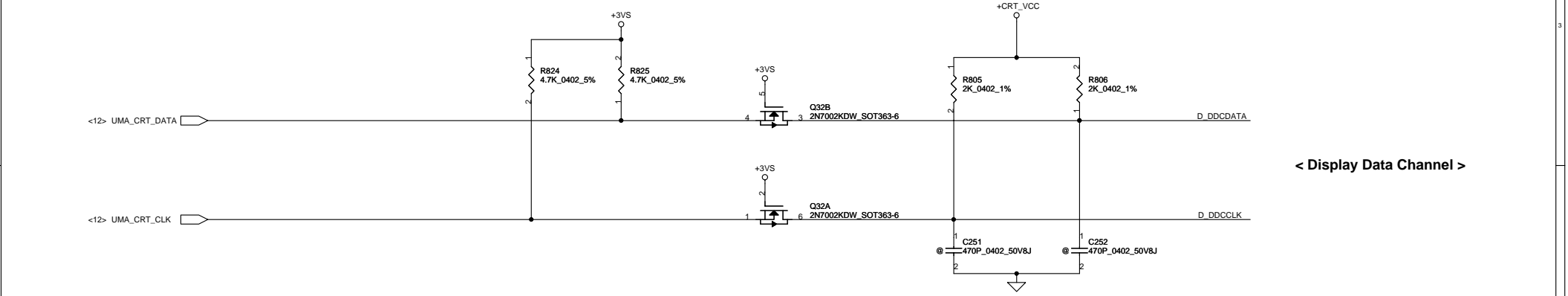
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< SYNC SIGNAL >



< Display Data Channel >

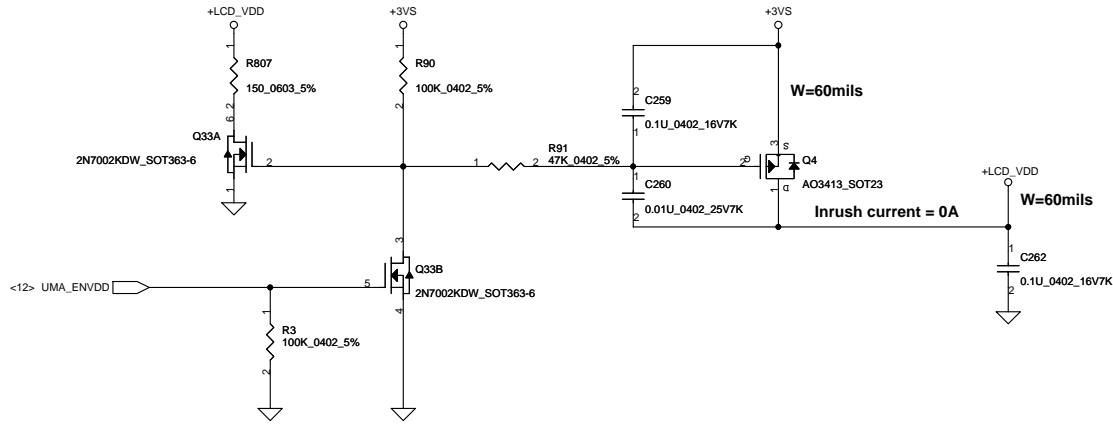


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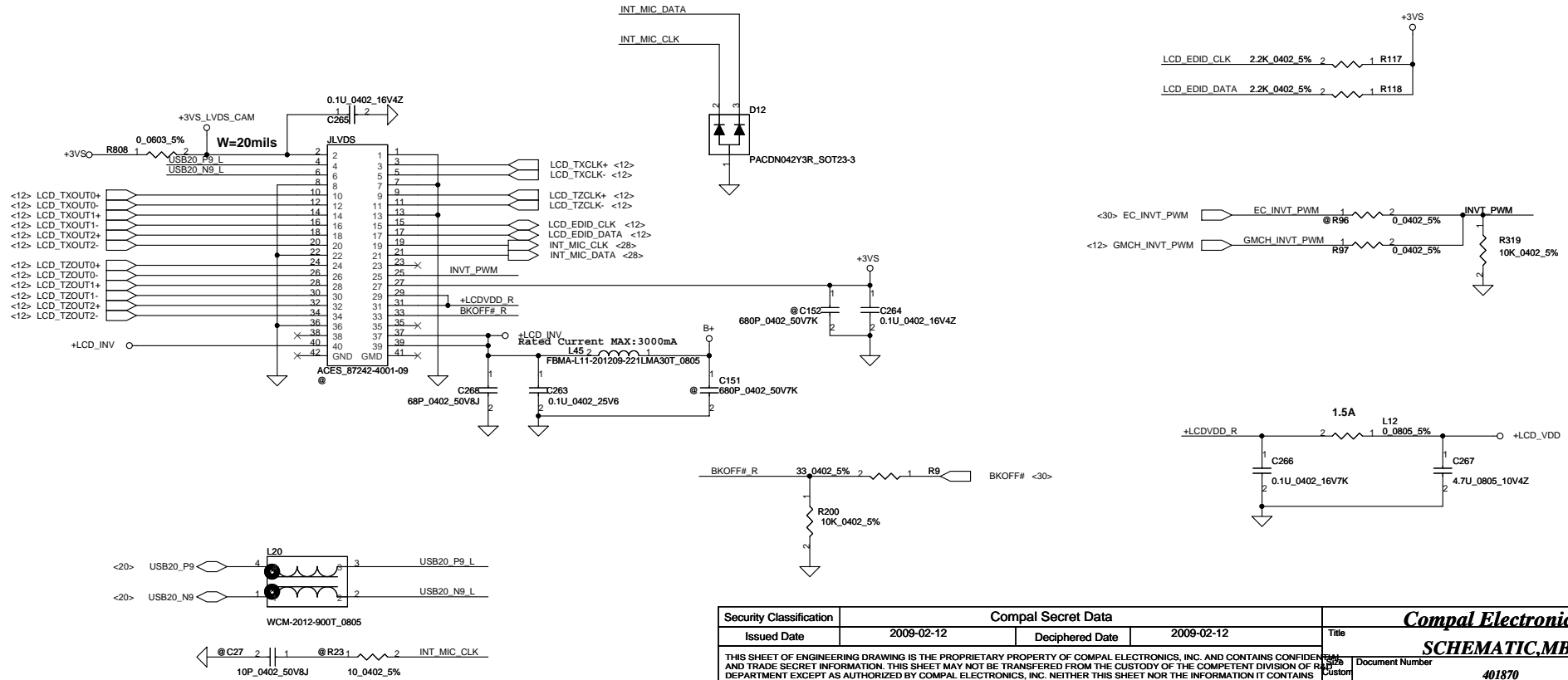
SCHEMATIC\_MB A6053



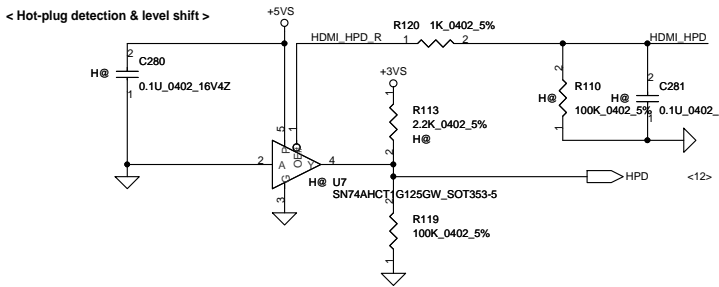
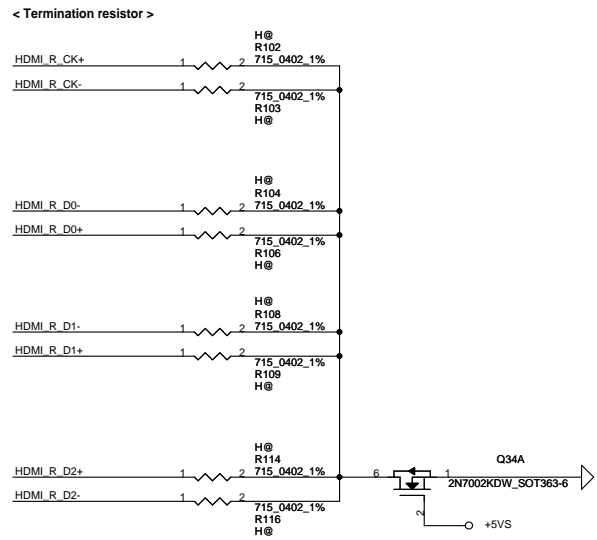
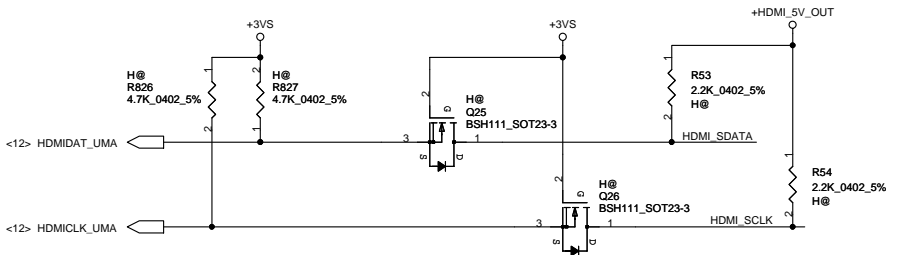
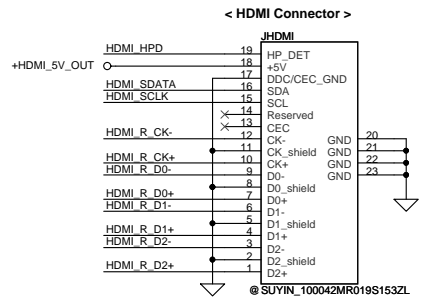
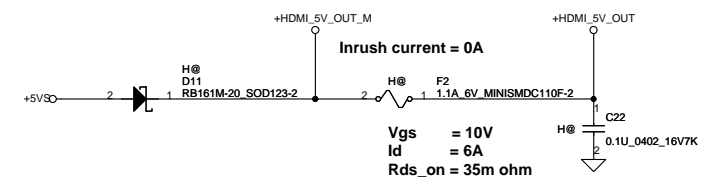
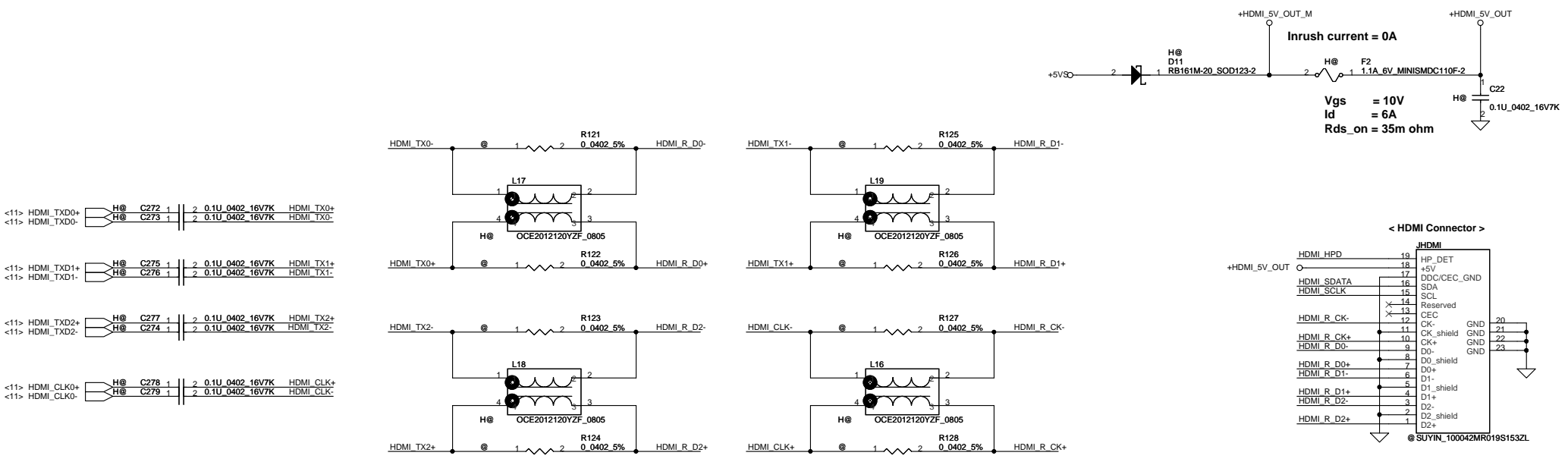
LCD/PANEL BD. Conn.



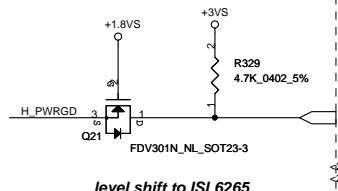
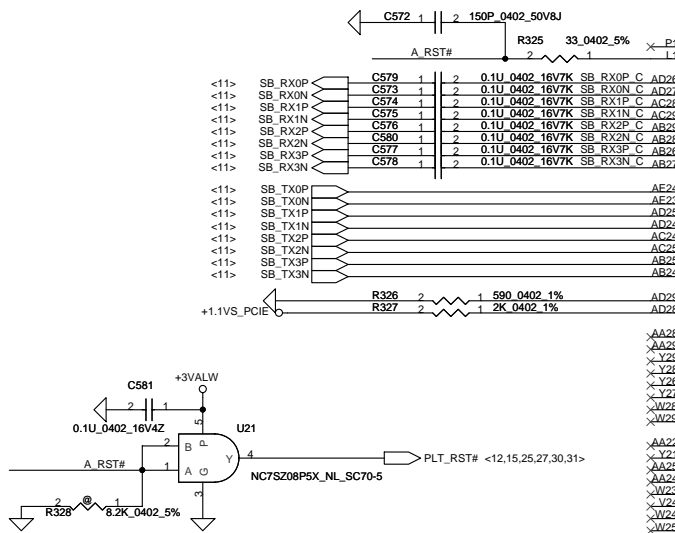
< LVDS Connector >



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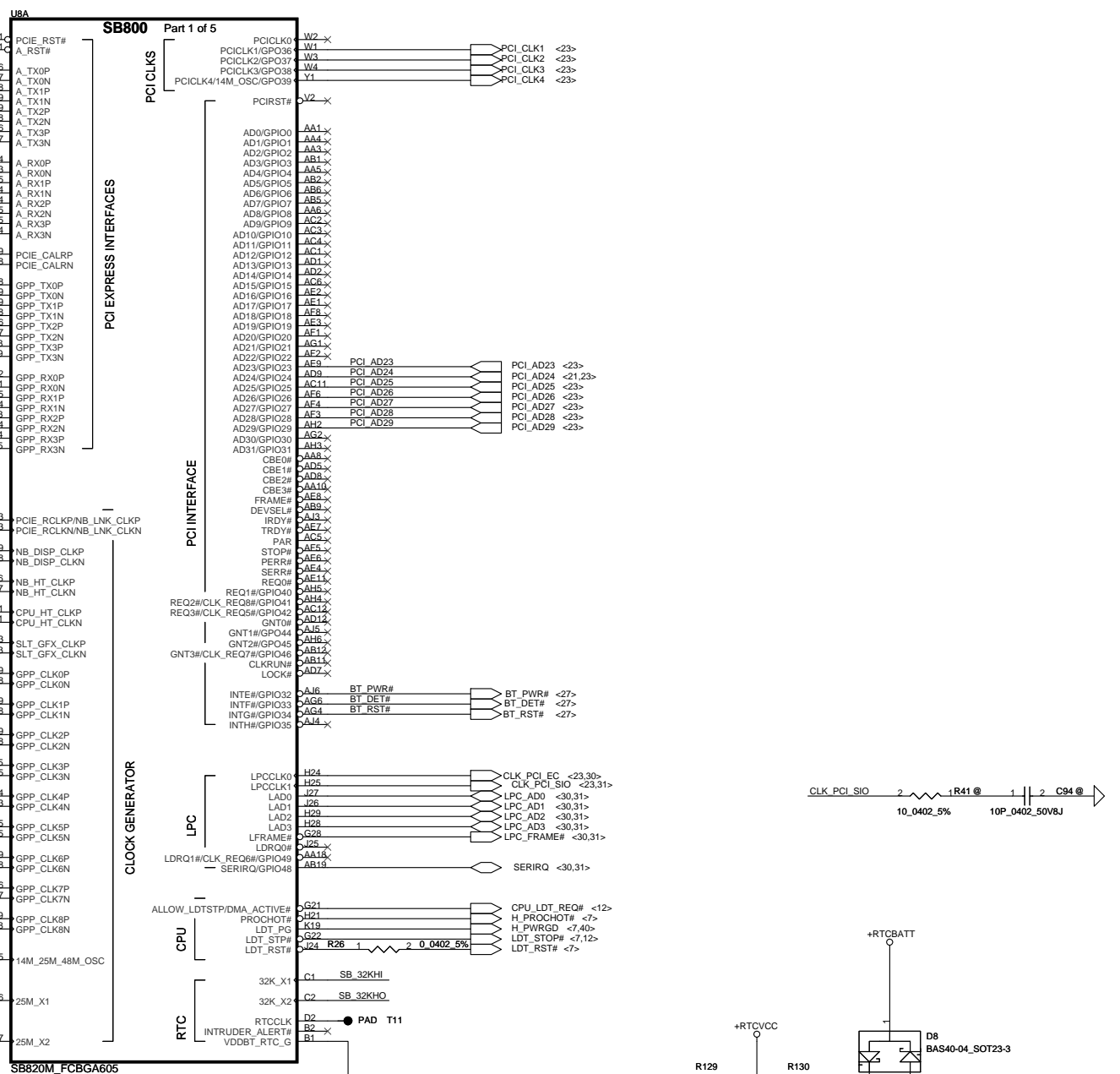
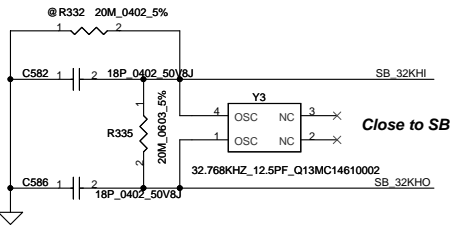
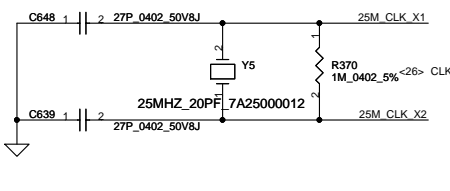


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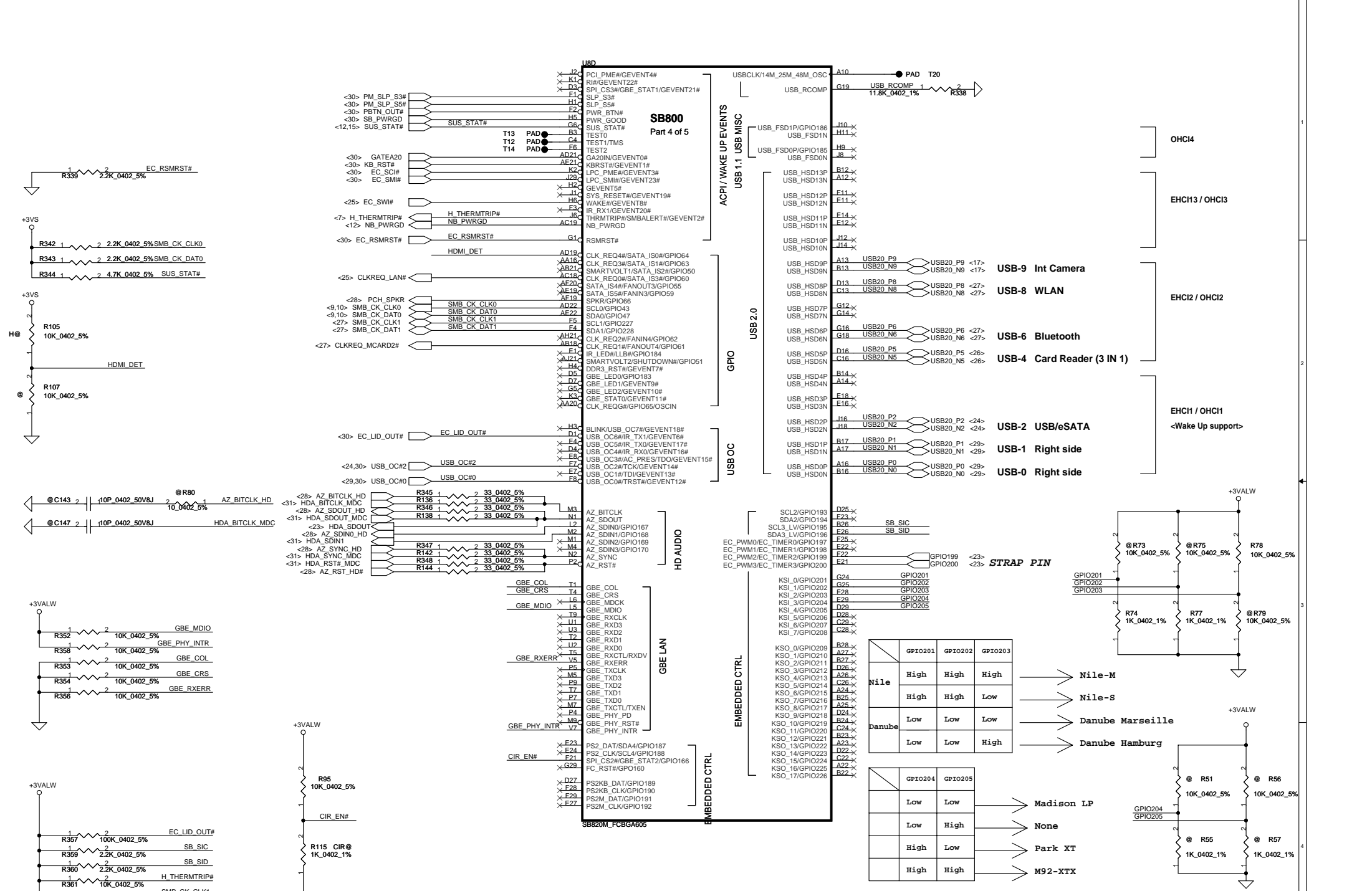
**ISL6265 PWROK input, TTL level: 0.8V-2.0V**

*When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high*



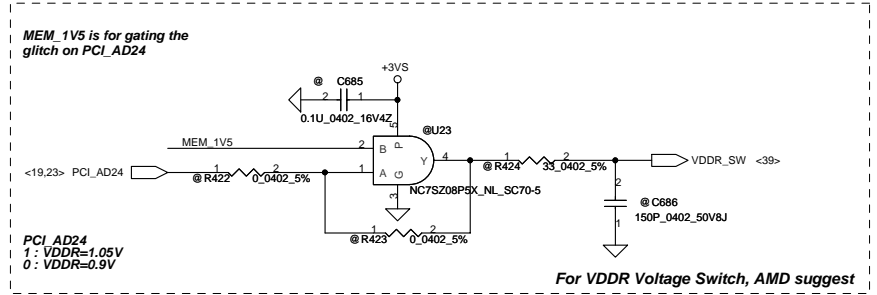
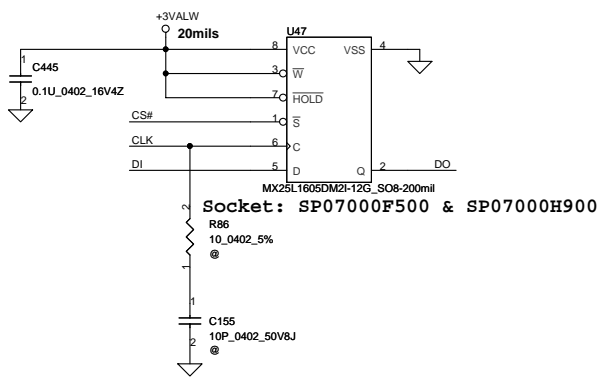
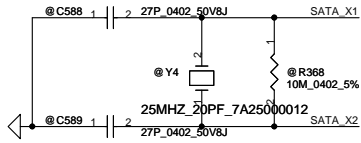
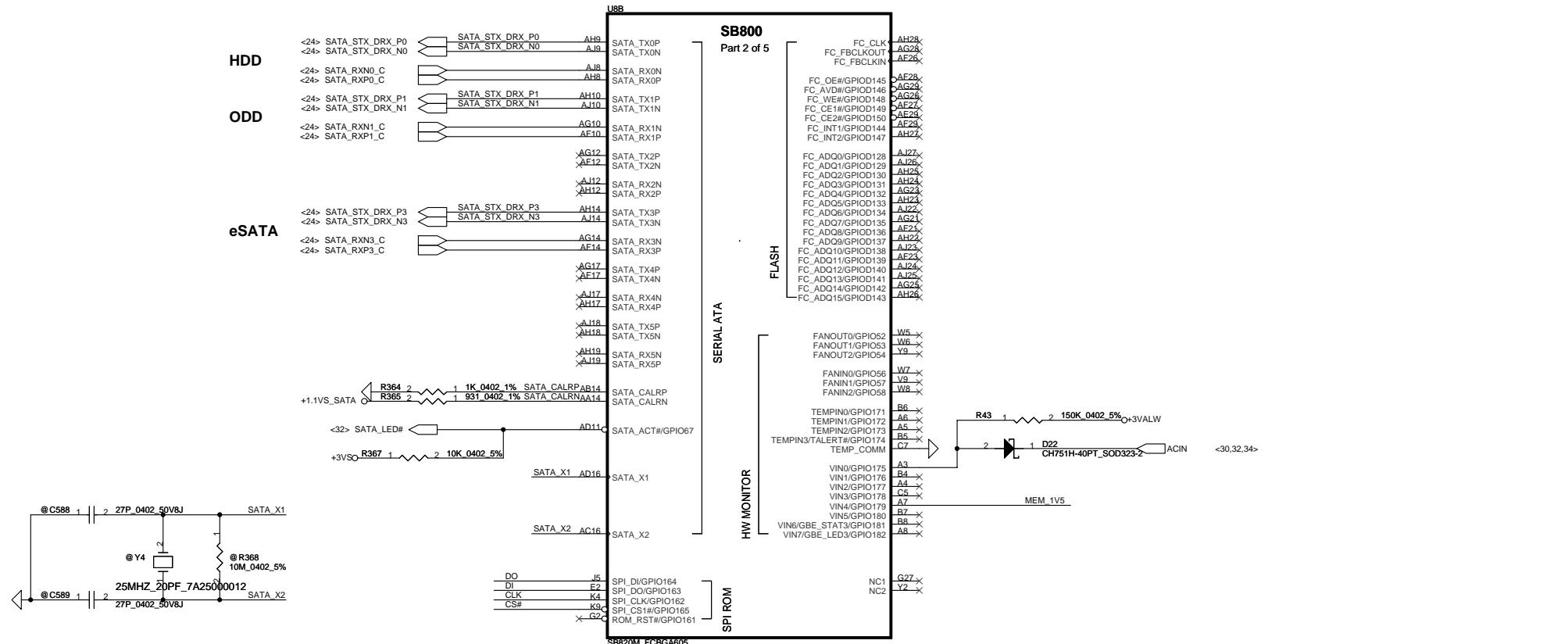
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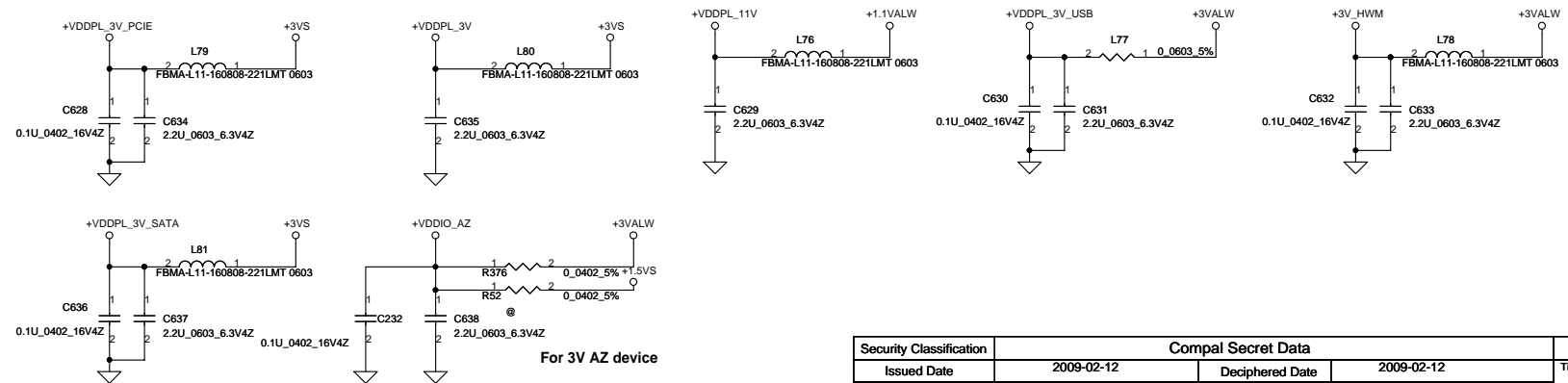
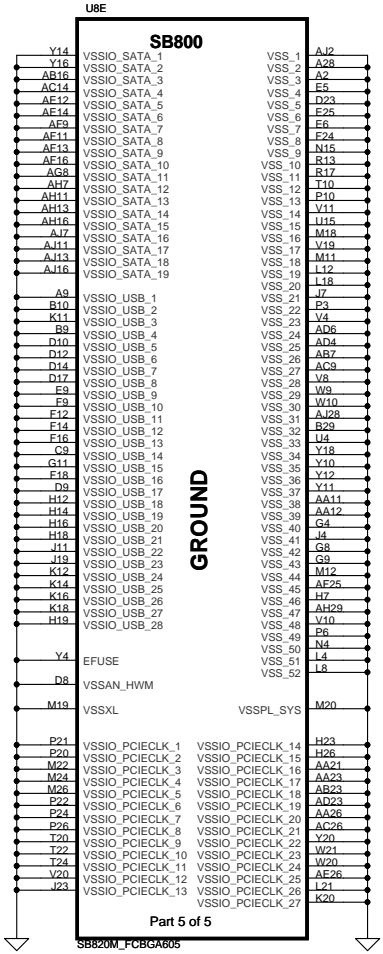
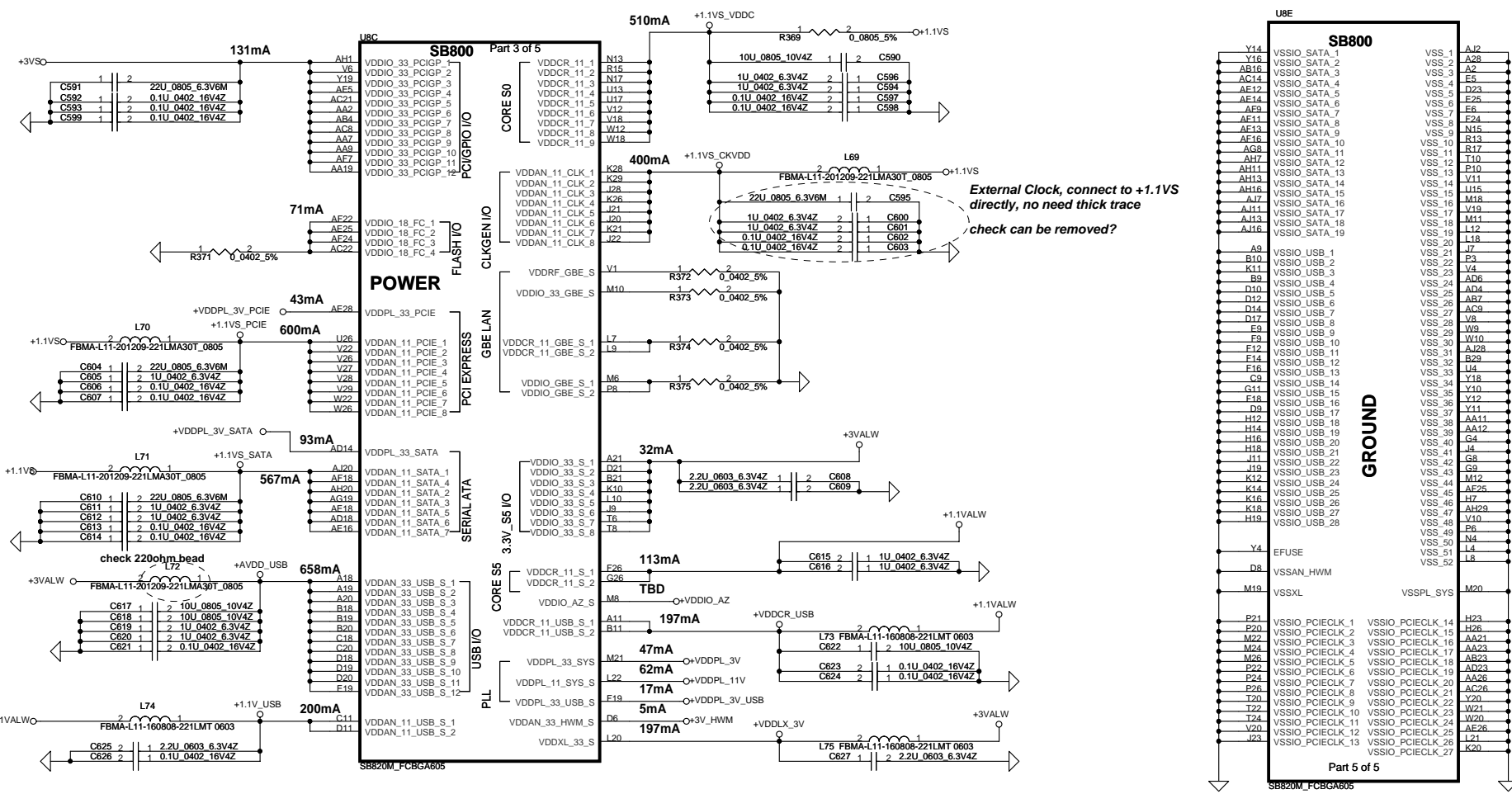


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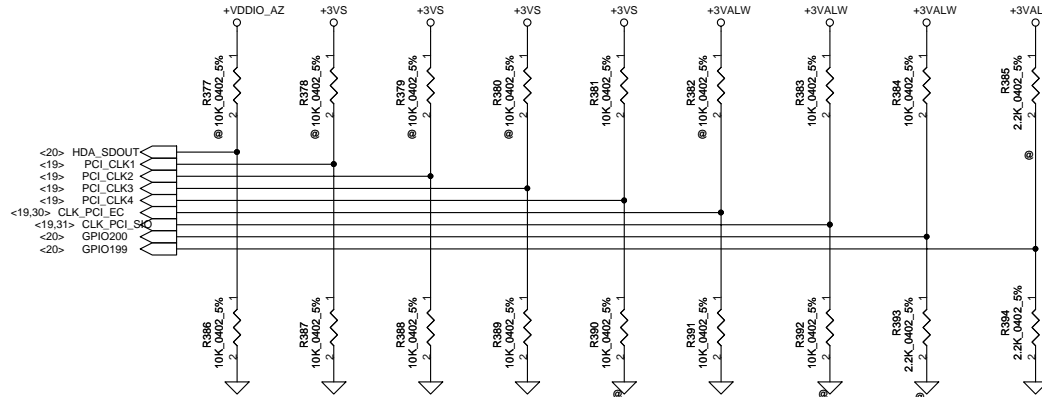


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# REQUIRED STRAPS

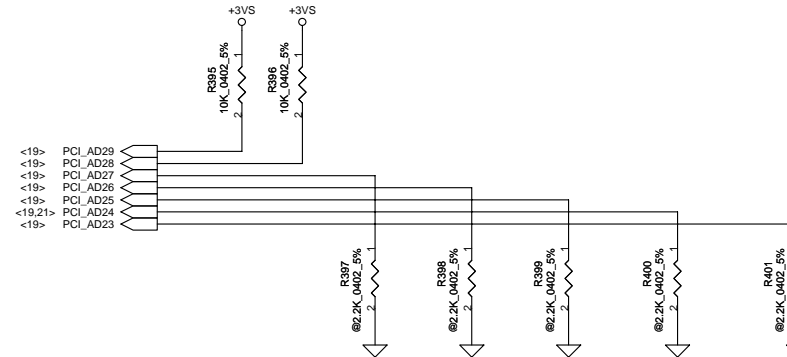
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1		GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT		H,H = Reserved H,L = SPI ROM (Default)	
<b>PULL LOW</b>	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE		L,H = LPC ROM L,L = FWH ROM	



# DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

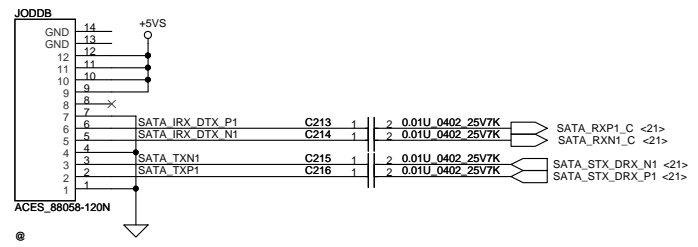
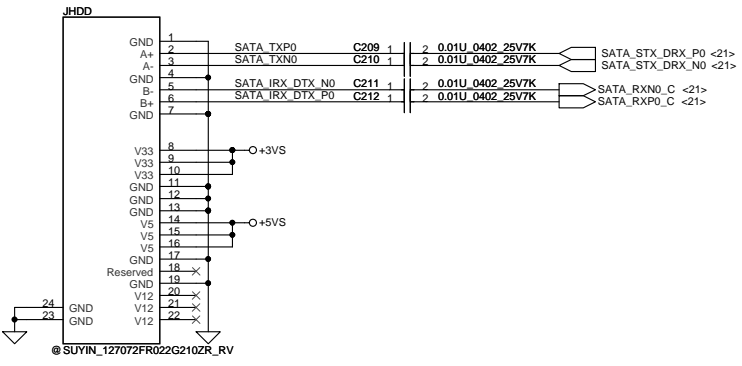
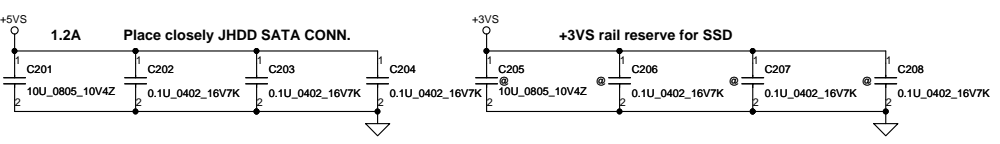
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



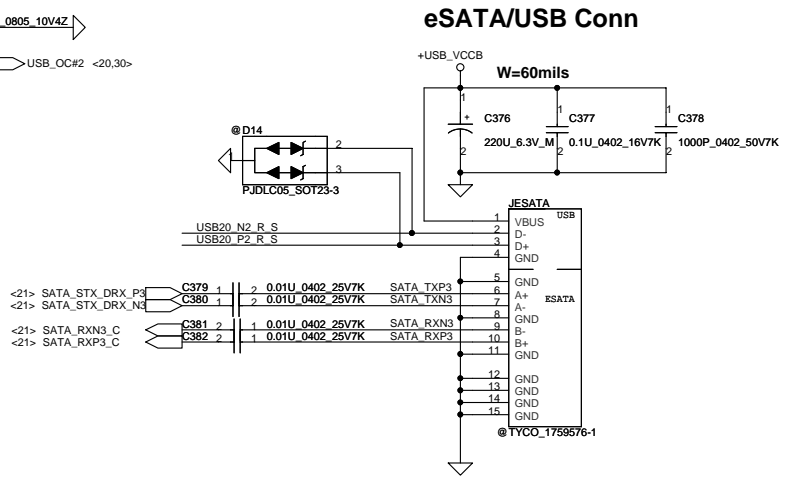
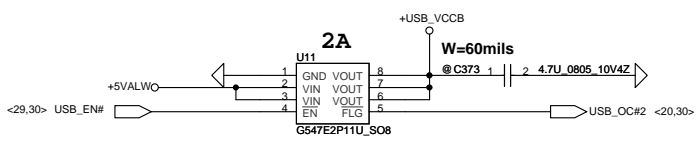
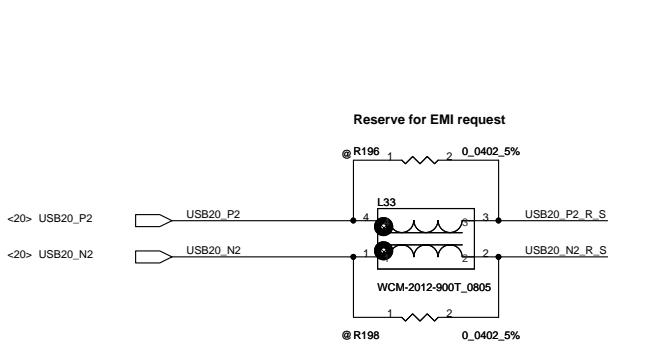
Check AD29,AD28 strap function

check default

< SATA HDD Conn >

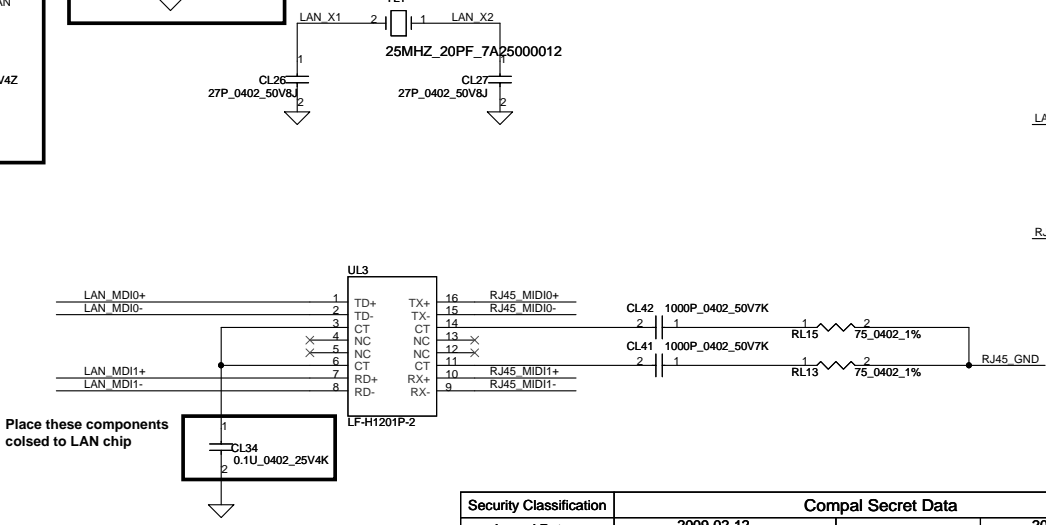
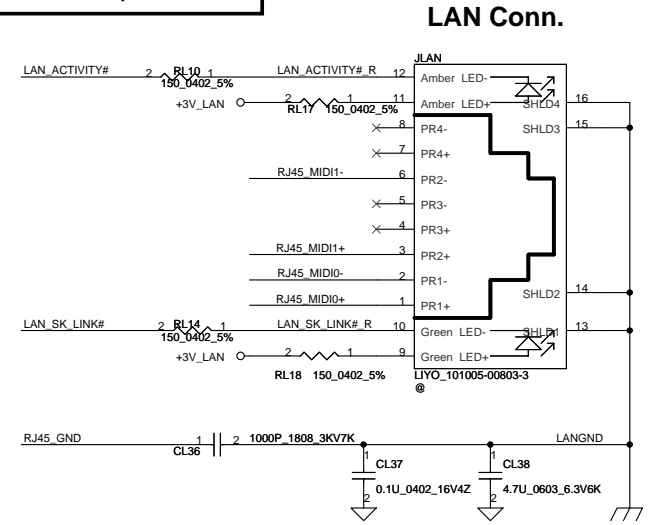
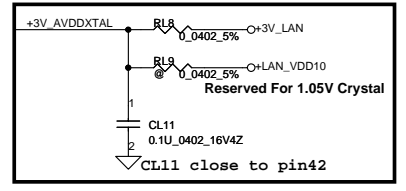
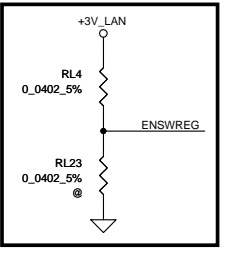
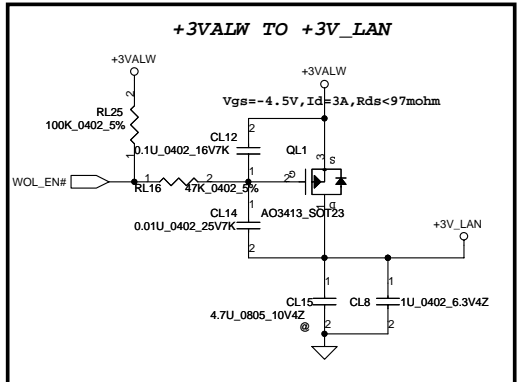
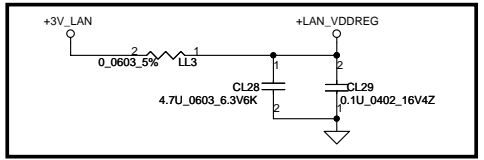
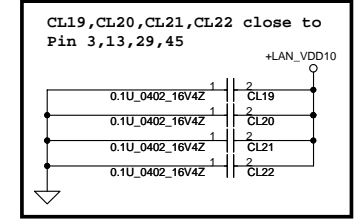
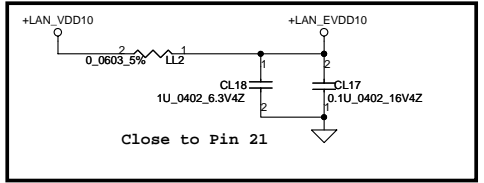
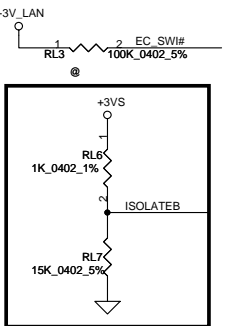
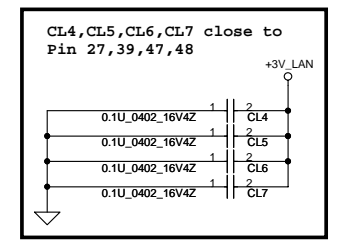
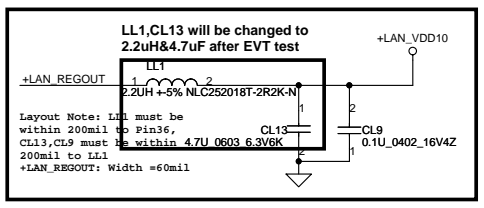
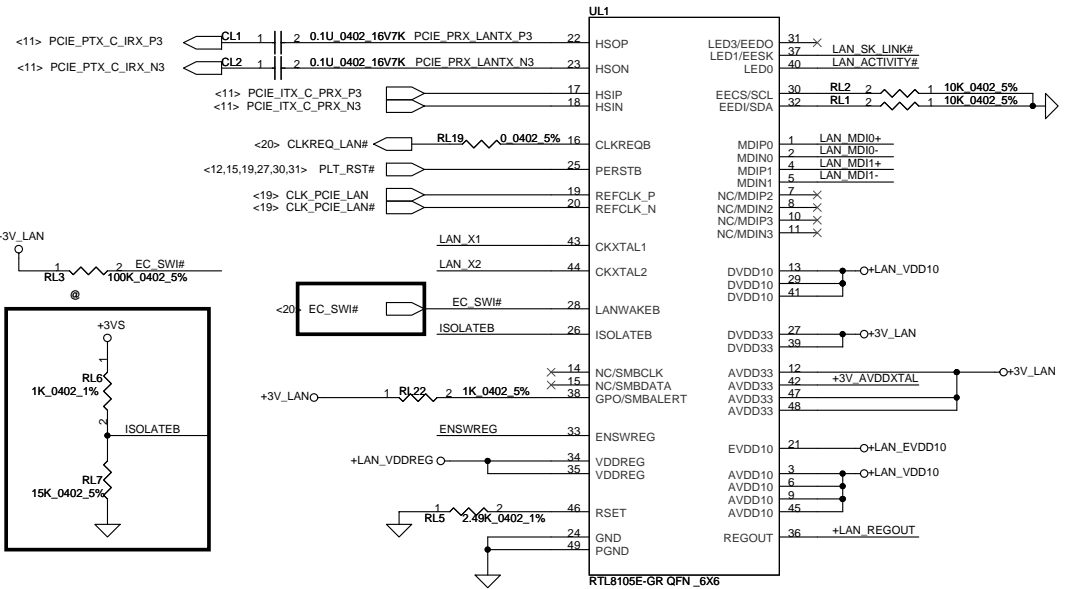


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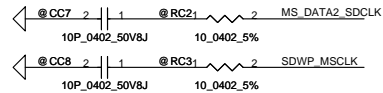
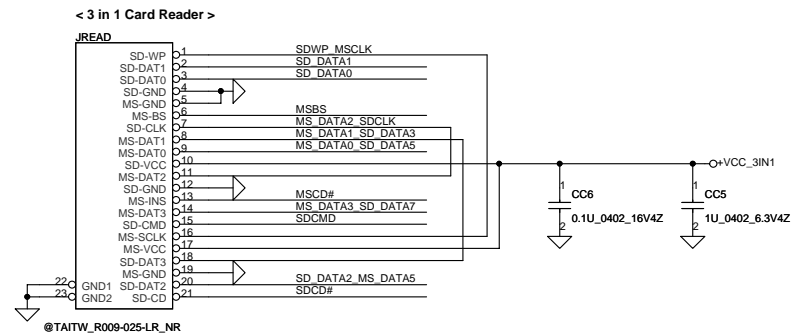
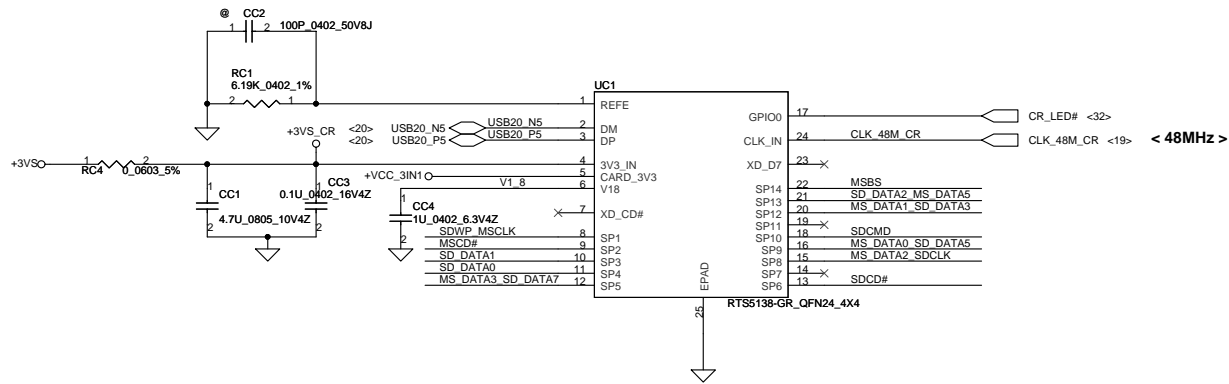
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Schematic, MB A6053	
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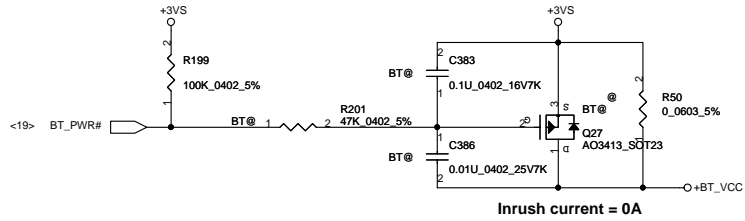
Place these components  
closer to LAN chip

Security Classification		Compal Secret Data		Title	
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2009-02-12		2009-02-12		Compal Electronics, Inc.	
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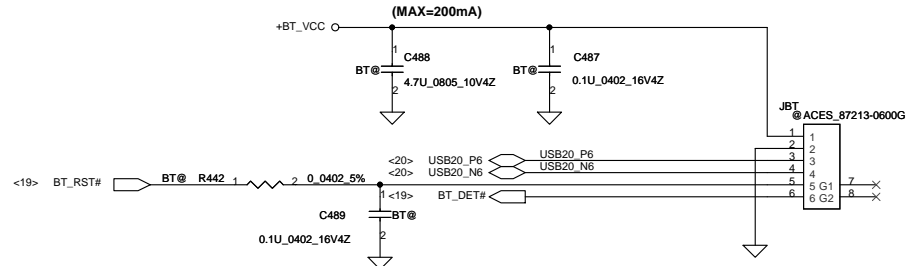


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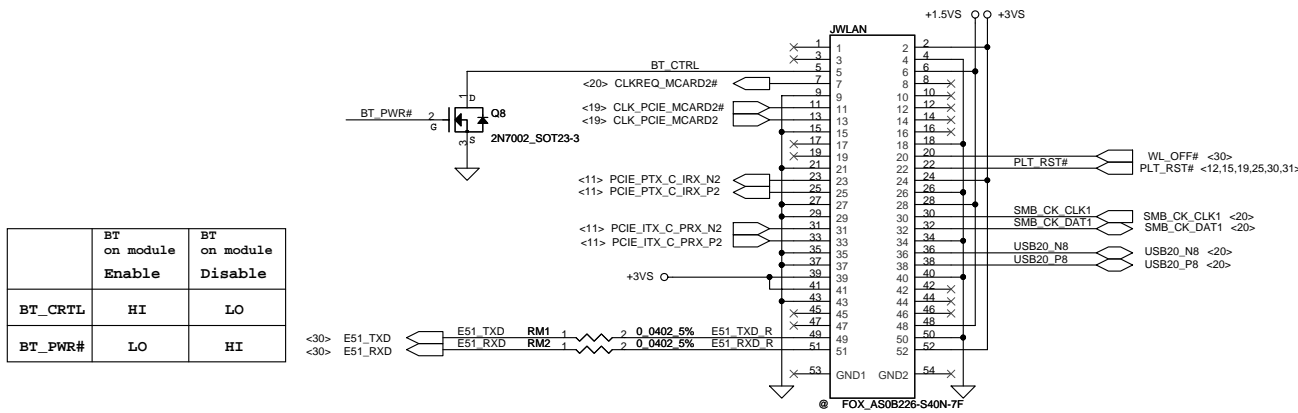
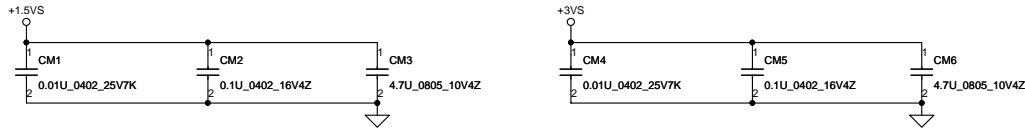
### < Bluetooth Interface, USB port6 >



### < Bluetooth Connector >



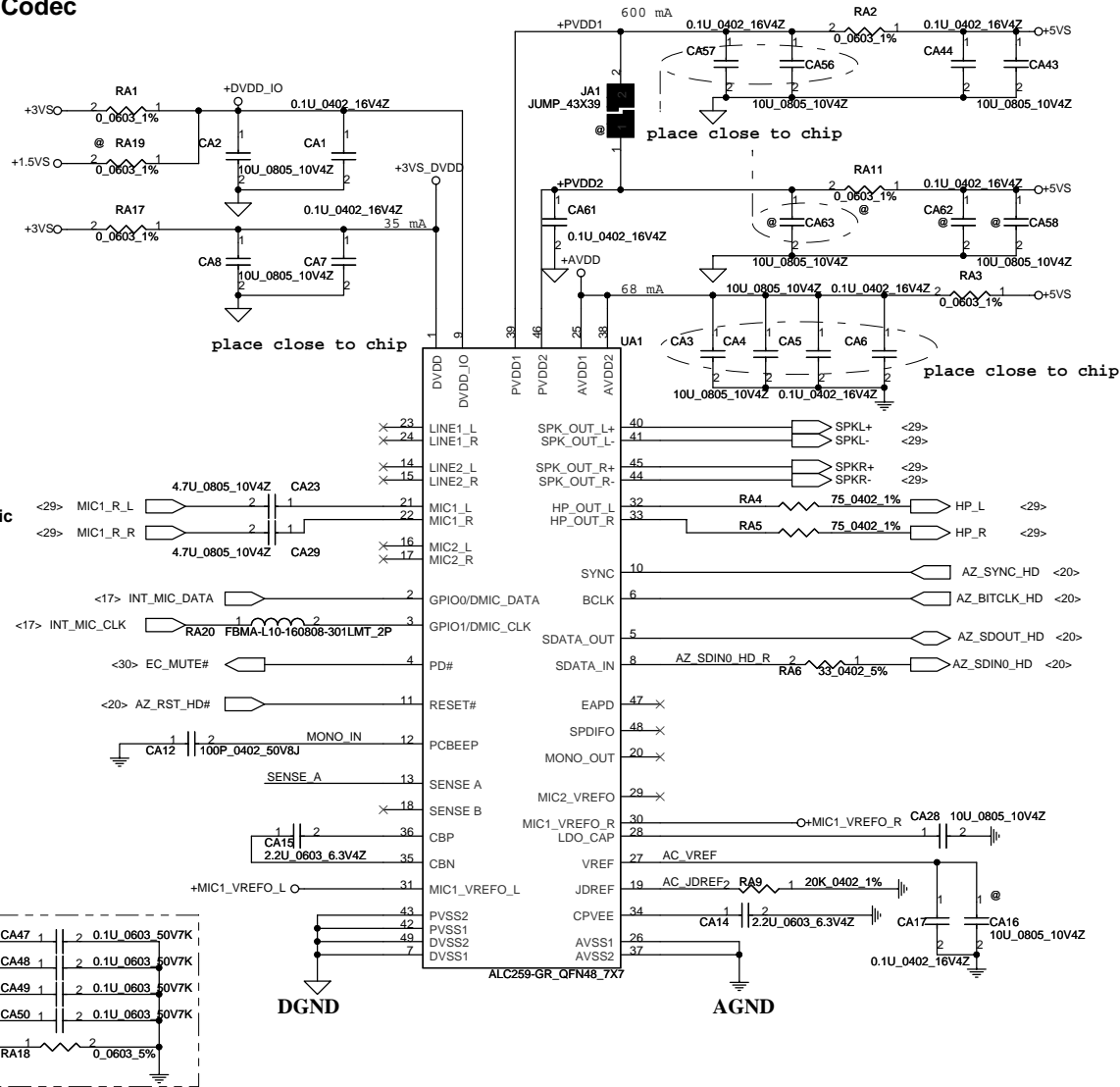
### < PCIe Mini Card for WLAN >



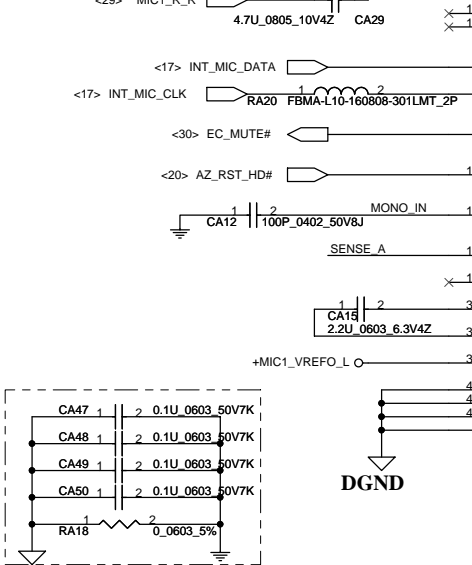
	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

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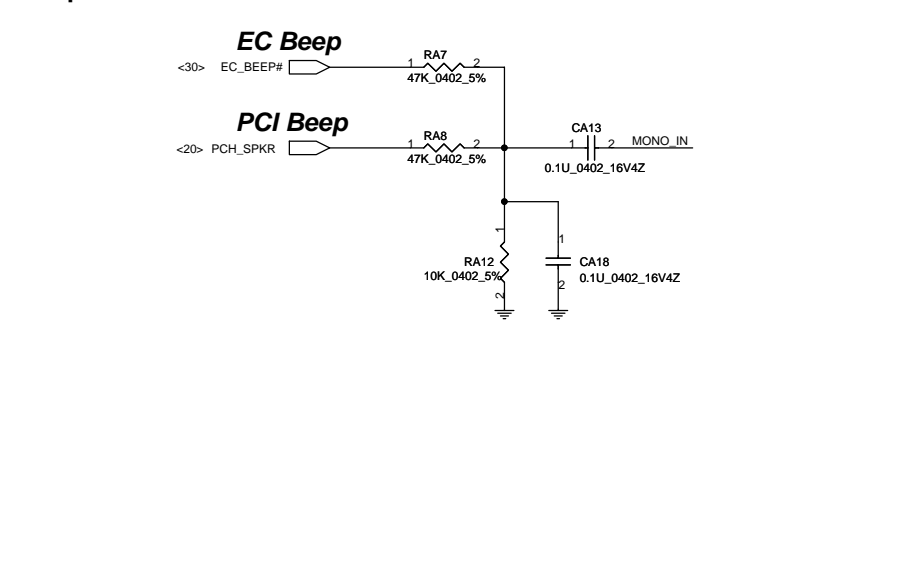
# Codec



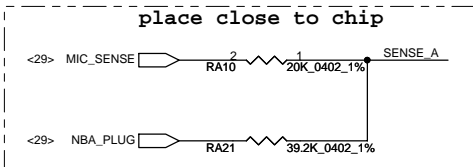
## Ext. Mic



## Beep sound

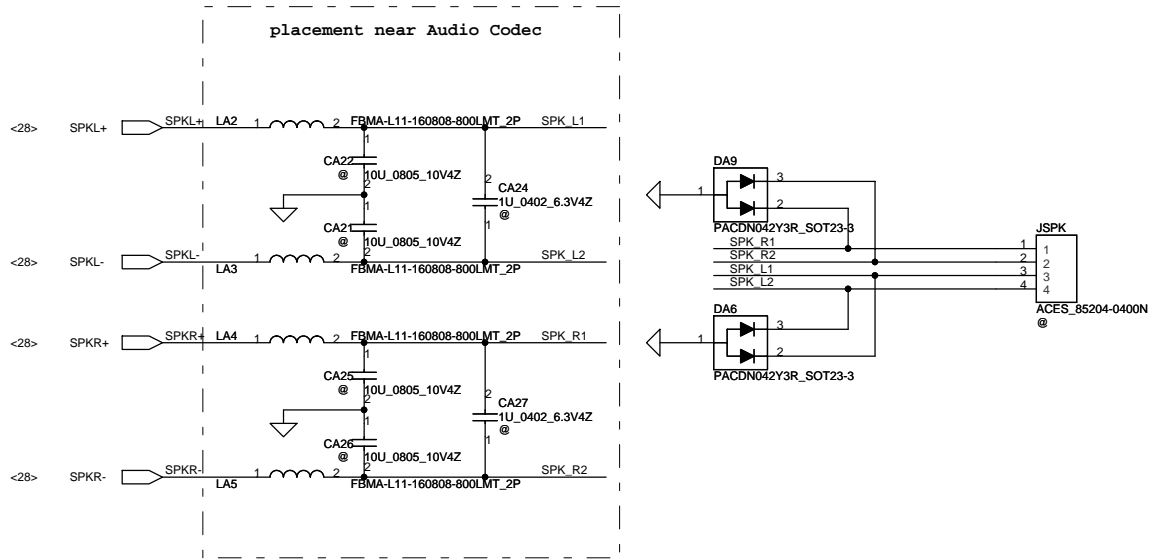


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



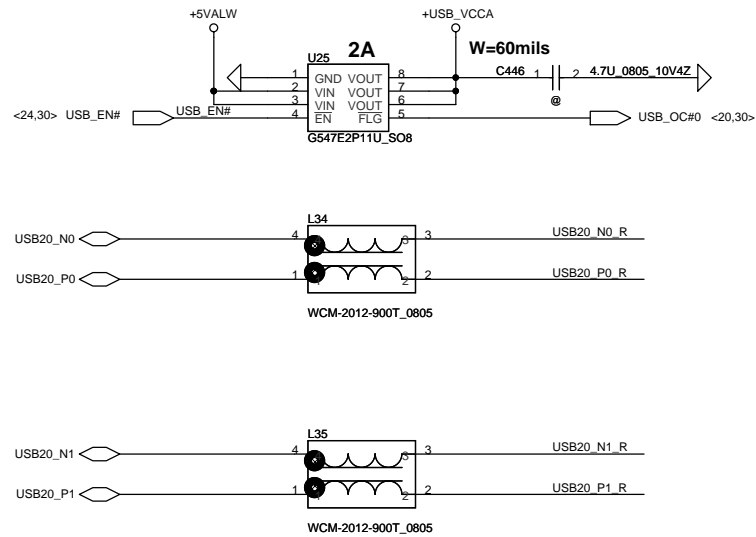
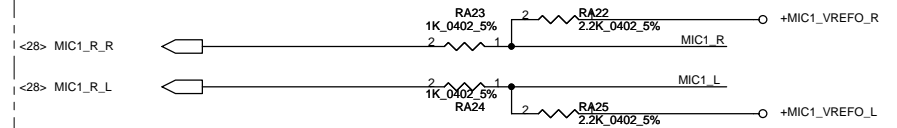
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# Speaker Connector

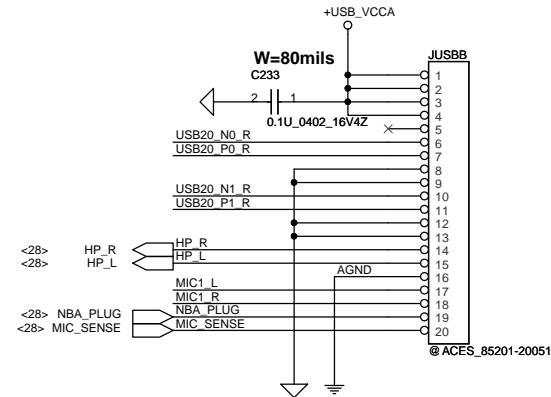


# HeadPhone/LINE Out JACK

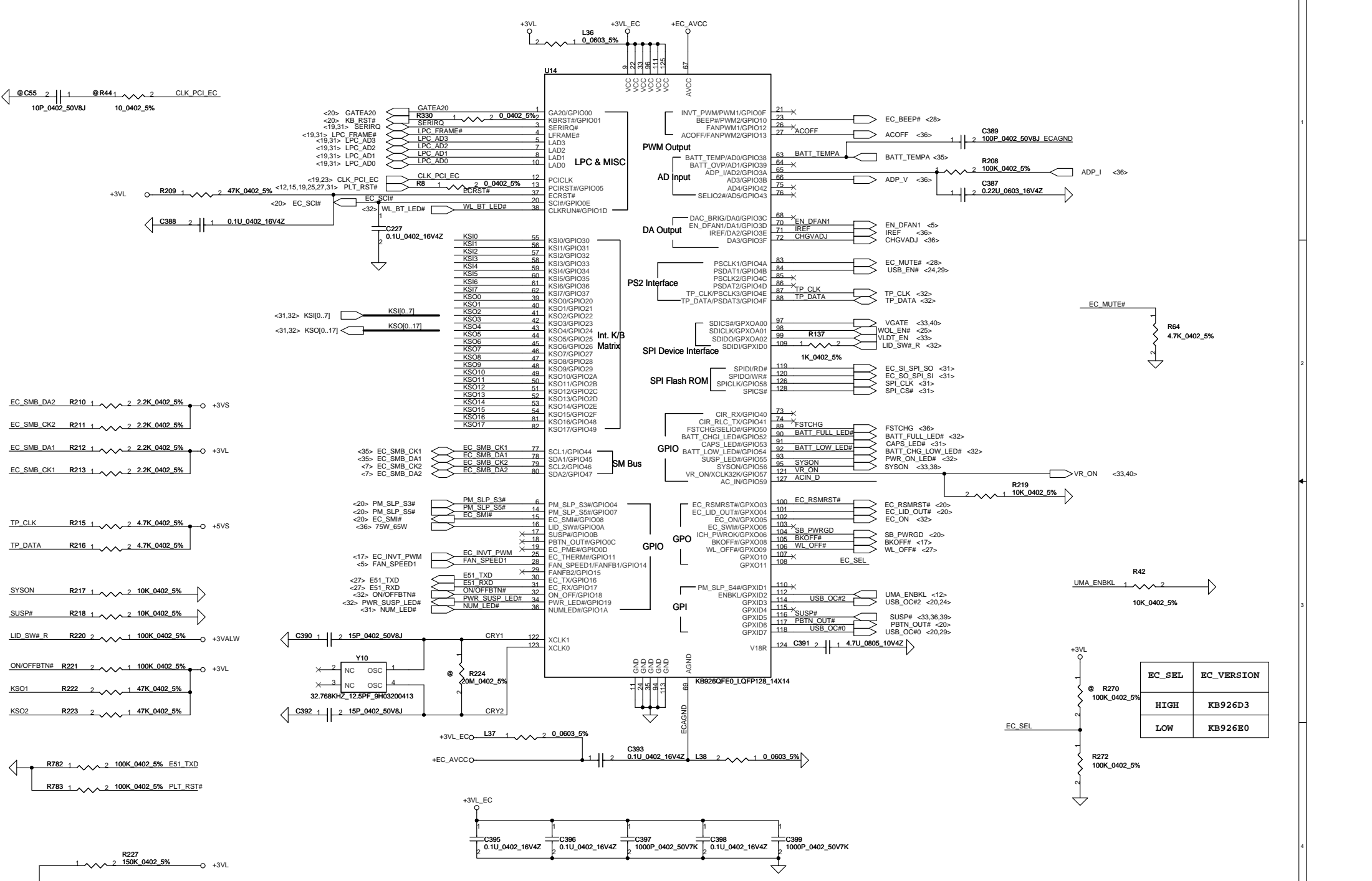
## Ext.MIC/LINE IN JACK



## Audio & USB Sub-Board Conn.

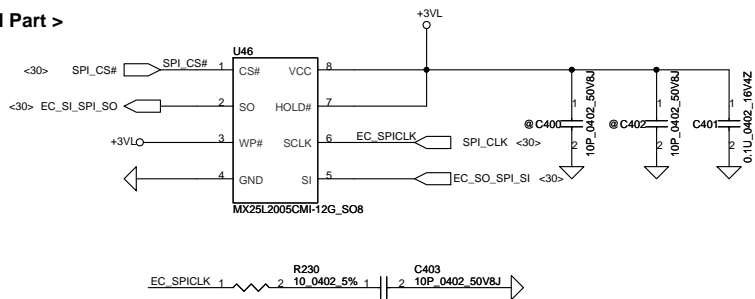


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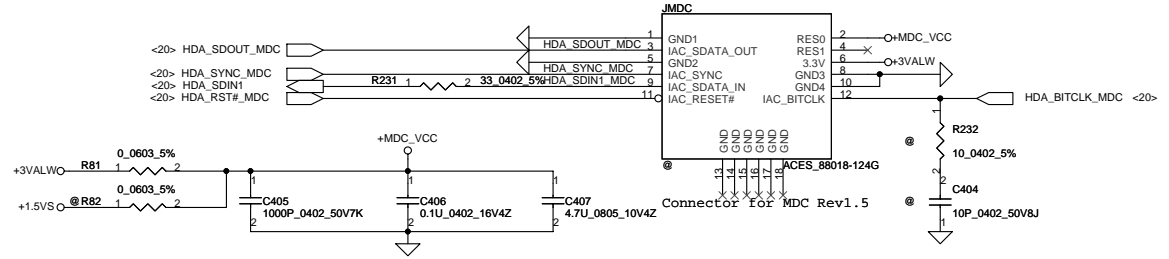


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< ROM Part >

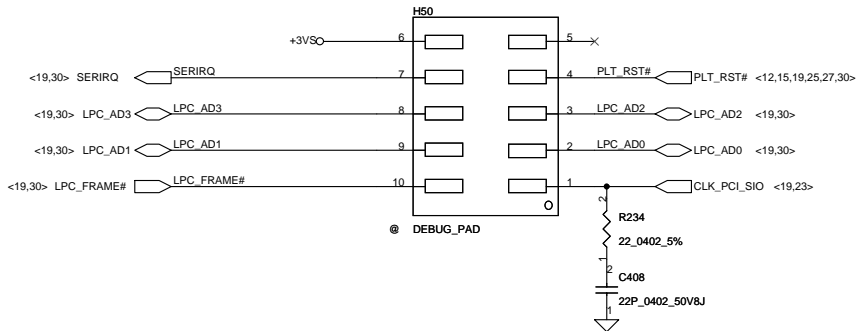


< MDC 1.5 Conn >



< LPC Debug Port >

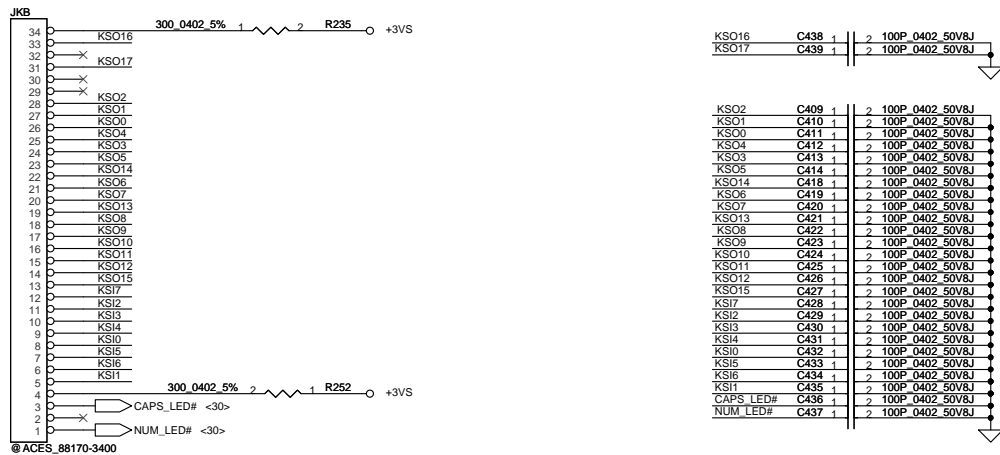
Please place the PAD under DDR DIMM.



< KEYBOARD Conn >



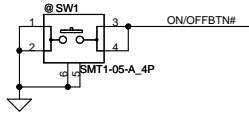
< For EMI >



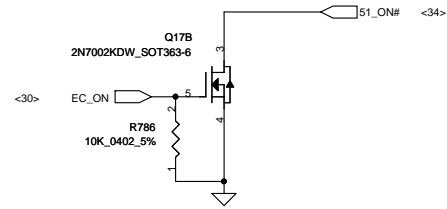
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Compal Electronics, Inc.  
SCHEMATIC, MB A6053

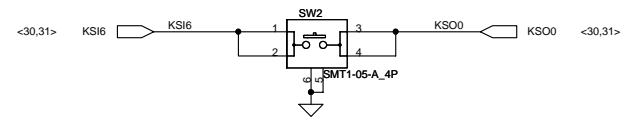
< Power Button for Debug >



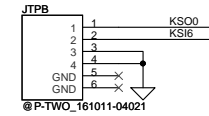
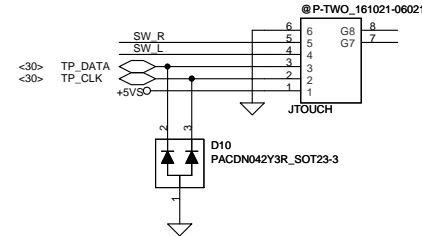
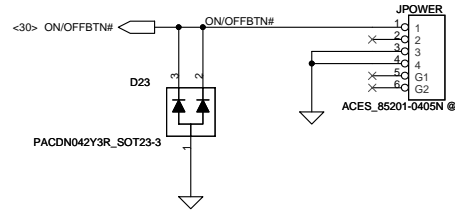
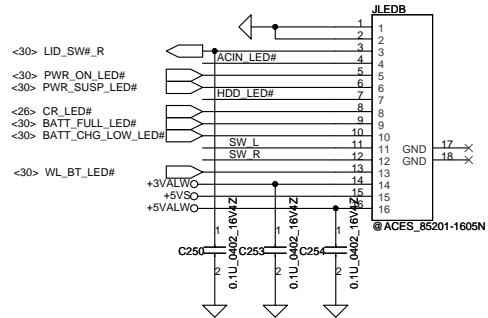
< Power Button Circuit >



< TP on & off BTN on M/B >

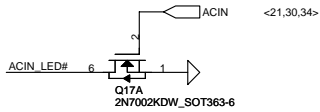


Sub-B Connector

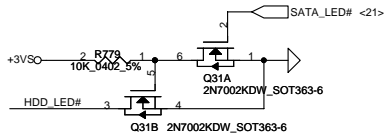


LED Circuit

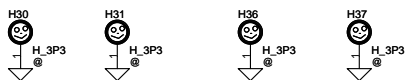
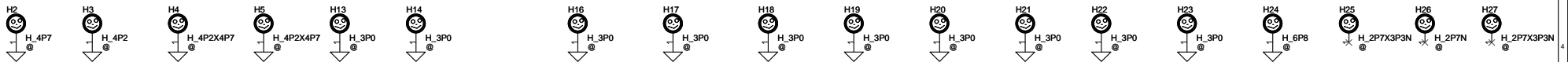
DC-IN LED



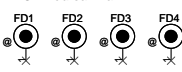
HDD LED



SCREW



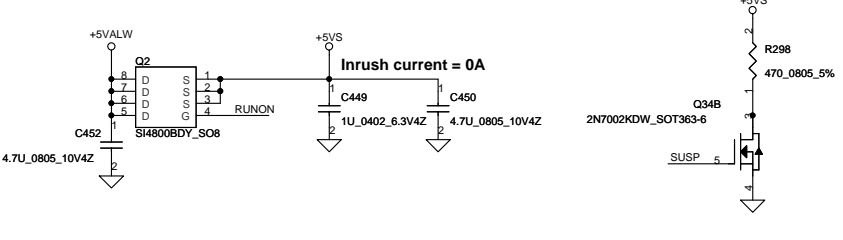
PCB Federal Mark PAD



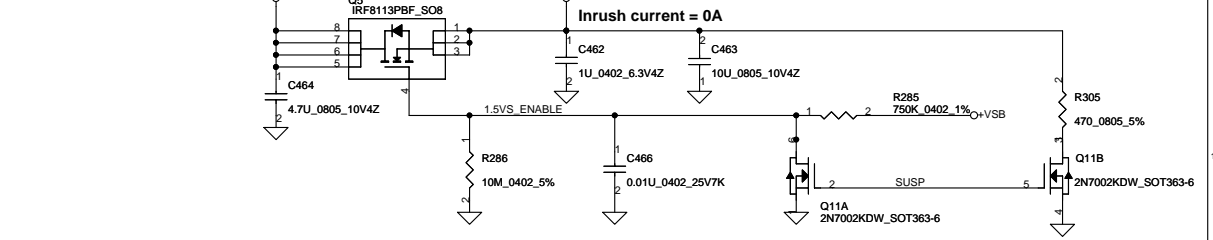
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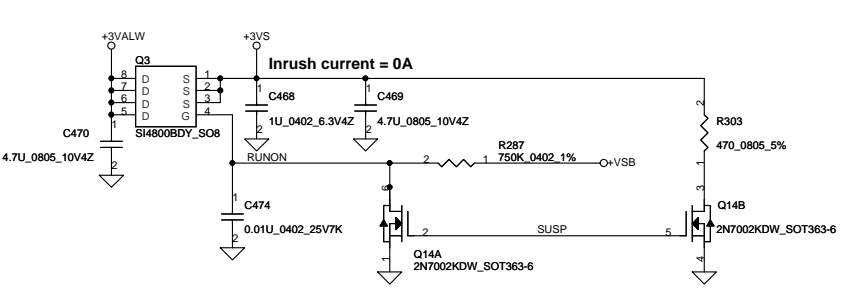
< +5VALW TO +5VS >



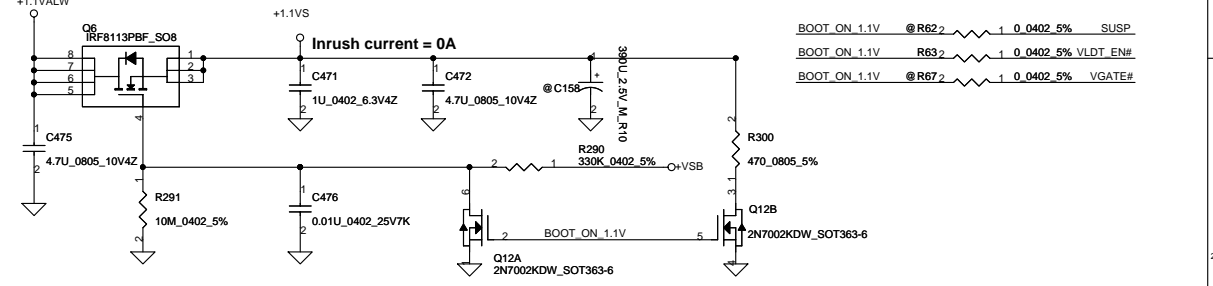
< +1.5V TO +1.5VS >



< +3VALW TO +3VS >

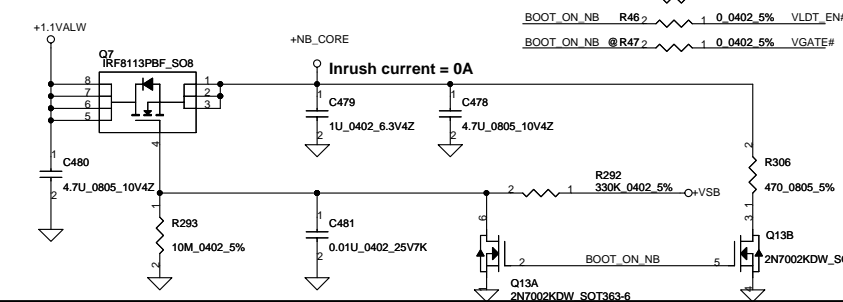


< +1.1VALW TO +1.1VS >



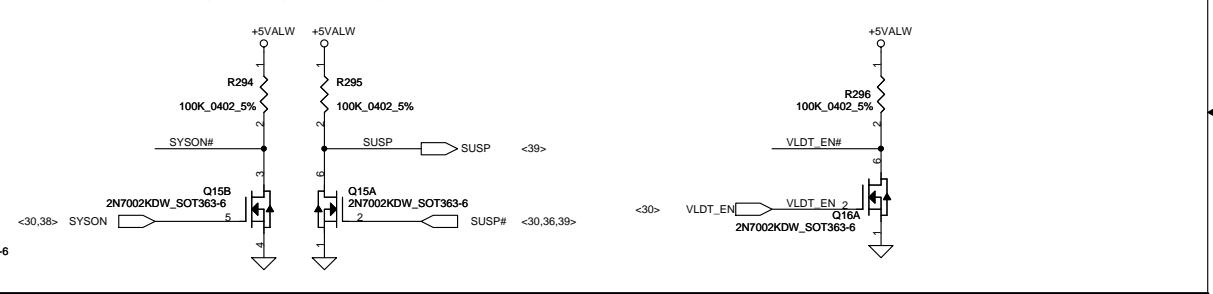
BOOT\_ON\_1.1V @R62 1 0.0402\_5% SUSP  
 BOOT\_ON\_1.1V R63 1 0.0402\_5% VLDT\_EN#  
 BOOT\_ON\_1.1V @R67 1 0.0402\_5% VGATE#

< +1.1VALW TO +NB\_CORE >

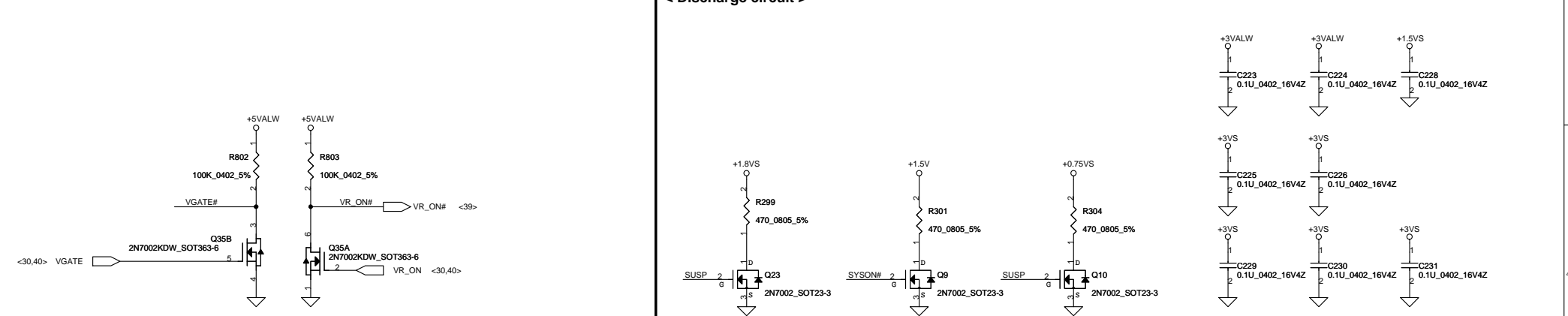


BOOT\_ON\_NB @R45 1 0.0402\_5% SUSP  
 BOOT\_ON\_NB R46 1 0.0402\_5% VLDT\_EN#  
 BOOT\_ON\_NB @R47 1 0.0402\_5% VGATE#

< Inversion of SYSON, SUSP#, VLDT\_EN, EC\_ON >

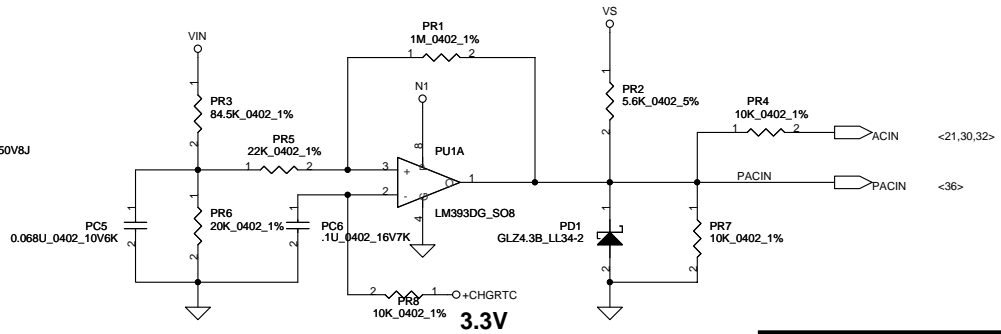
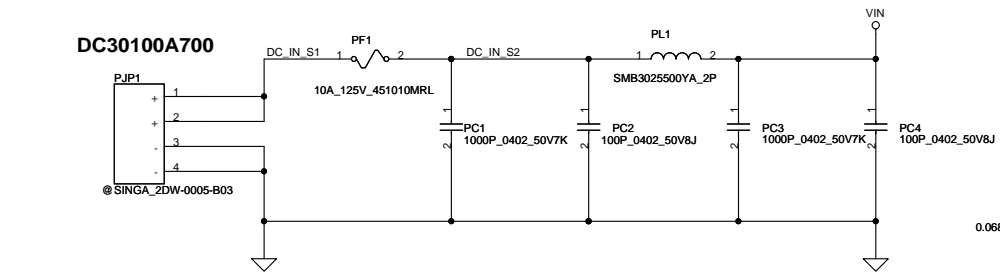


< Discharge circuit >

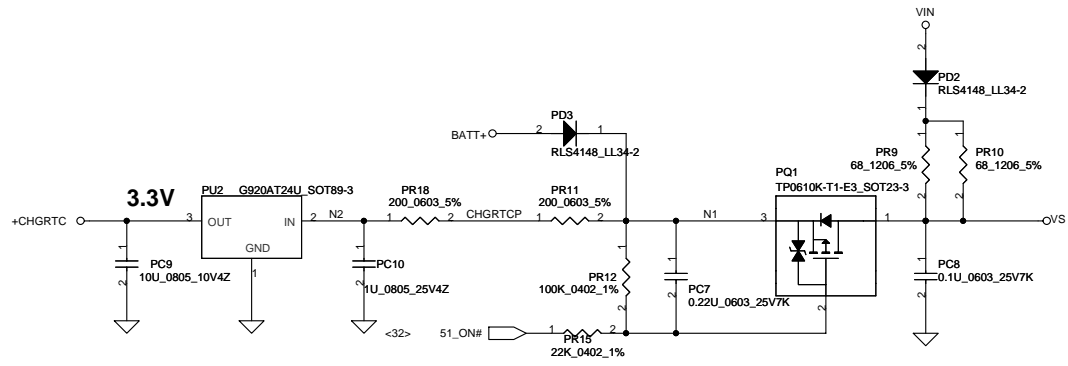


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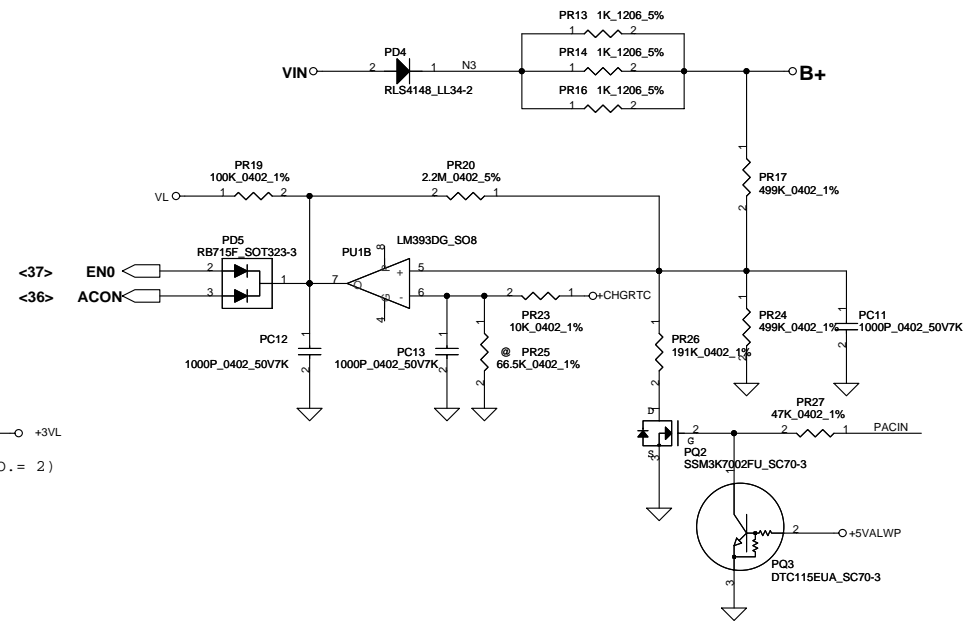
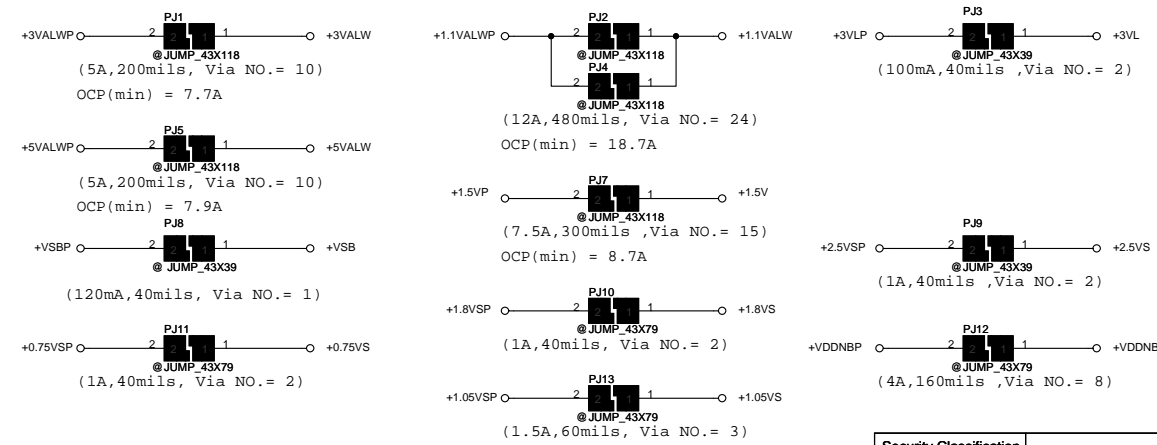
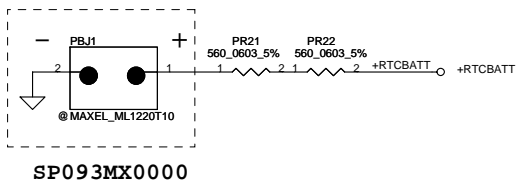
**DC30100A700**



Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

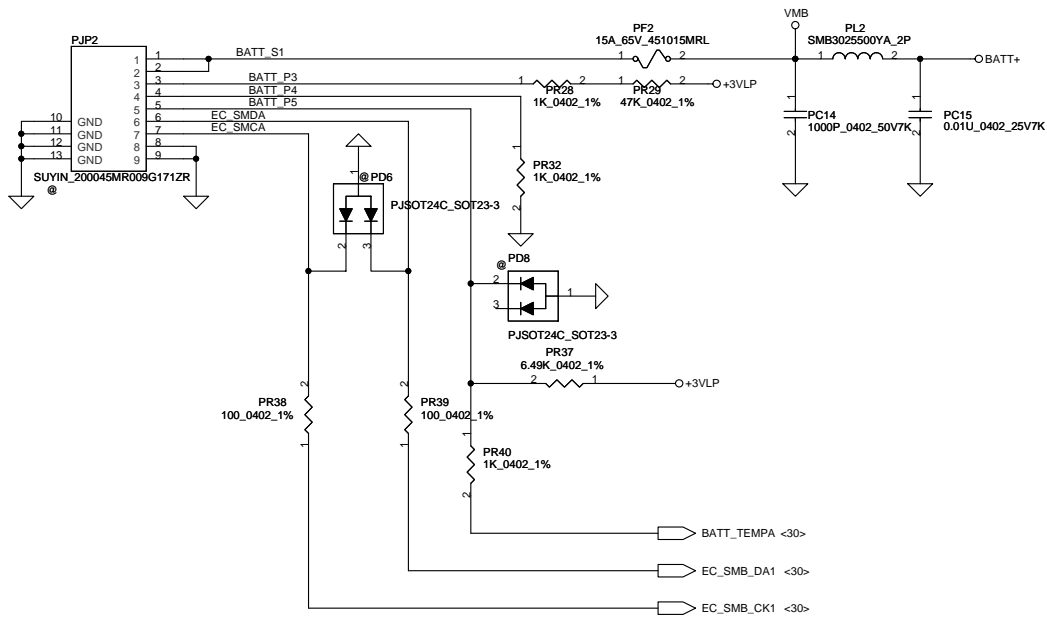


**RTC Battery**



**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**

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**PH1 under CPU botten side :**  
 CPU thermal protection at 90 degree C  
 Recovery at 56 degree C

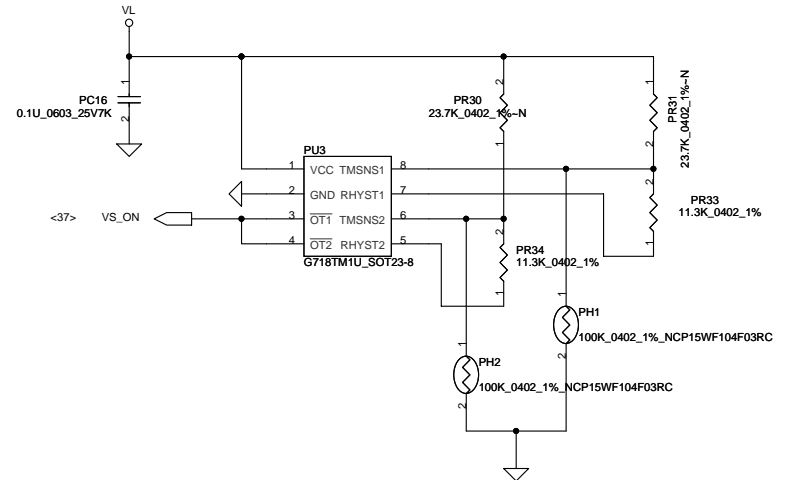
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

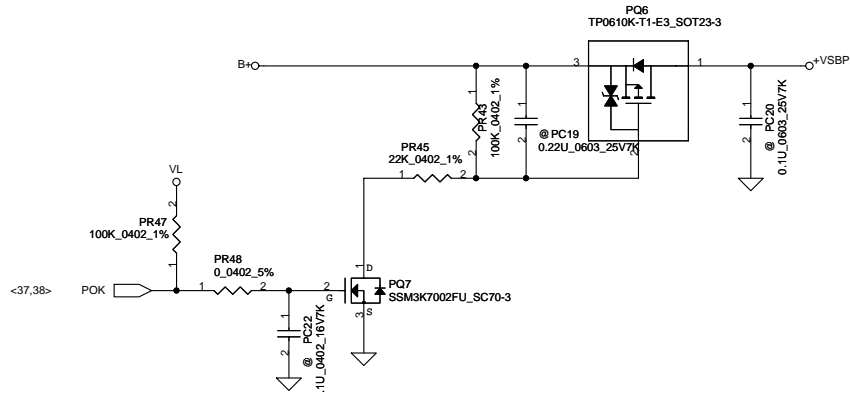
$$R_{tmh} \text{ at } 90C = 7.87K, R_{tml} \text{ at } 56C = 26.1K$$

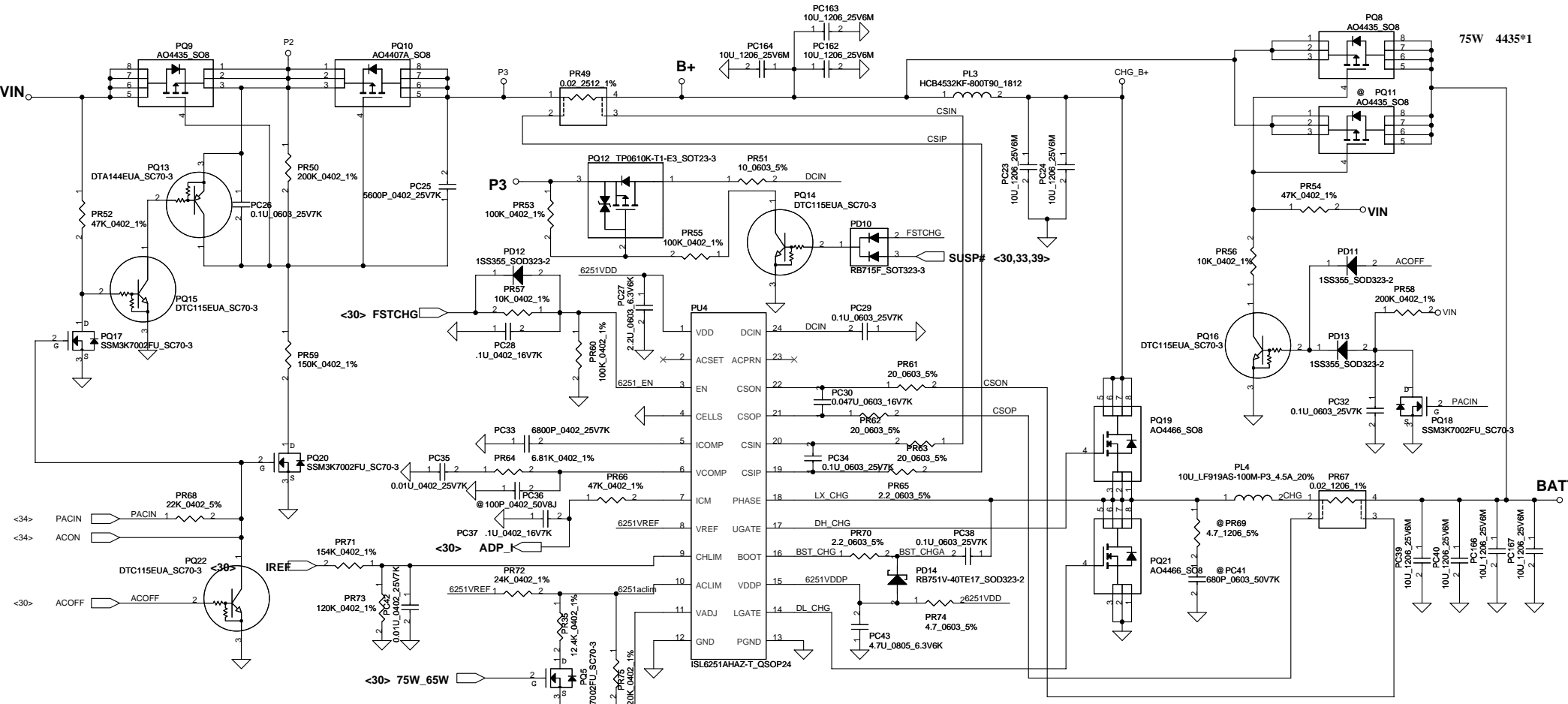
$$R_{set} = 3 * 7.87K = 23.61K \implies 23.7K$$

$$R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \implies 11.3K$$



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 90 degree C  
 Recovery at 56 degree C





CP mode  
 $V_{aclim} = 2.39 * (R_b // 152K / (R_t // 152K + R_b // 152K))$   
 $I_{input} = (1 / PR49) * ((0.05 * V_{aclim}) / (2.39 + 0.05))$   
 where  $V_{aclim} = 0.6221V$ ,  $I_{input} = 3.15A$   
 $V_{aclim} = 1.09986V$ ,  $I_{input} = 3.65A$   
 $V_{aclim} = 0.7717V$ ,  $I_{input} = 4.41A$   
 $V_{aclim} = 0.4204V$ ,  $I_{input} = 5.88A$

CC=0.25A-3.6A  
 IREF=0.9133\*Icharge  
 IREF=0.228V-3.29V  
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.315V

(75W)  $I_{in} = 2.512 ADP\_I$   
 (120W)  $I_{in} = 3.35 ADP\_I$   
 $V_{in} = 7.57 ADP\_V$

$I_{ada} = 0-3.421A(65W)$  CP=3.15A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W\_65W=high  
 $I_{ada} = 0-3.947A(75W)$  CP=3.63A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W\_65W=low  
 $I_{ada} = 0-4.737A(90W)$  CP=4.36A PR49=0.015, PR72=53.6k, PR75=20k, PR35=unpop, PQ5=unpop  
 $I_{ada} = 0-6.316A(120W)$  CP=5.81A PR49=0.015, PR72=8.25k, PR75=26.7k, PR35=unpop, PQ5=unpop  
 CP= 92%\*Iada

CELLS	VDD	GND	Float
CELL number	4	3	2

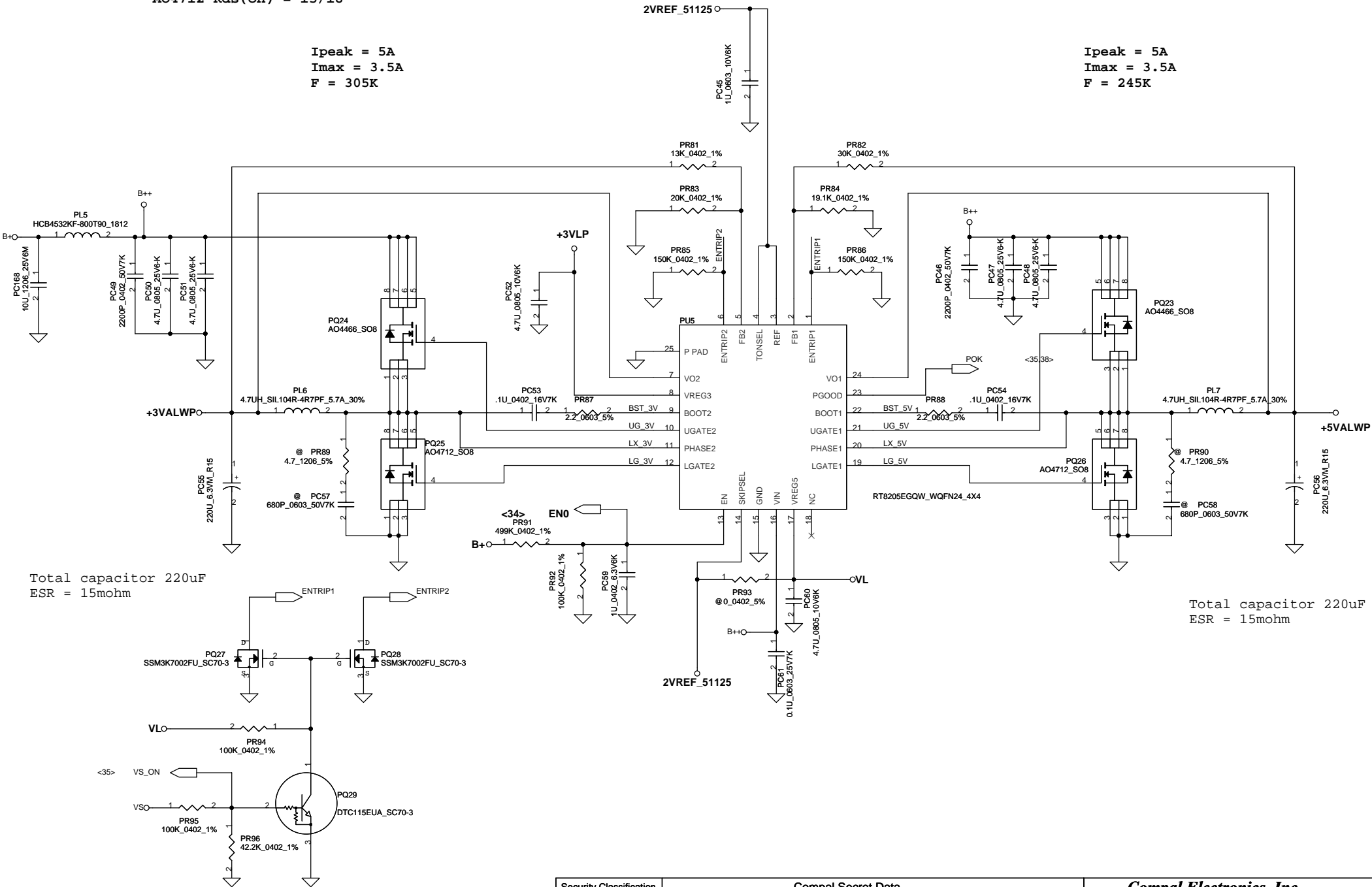
Security Classification	Compal Secret Data	
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		2009/9/25
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AO4712 Rds(on) = 15/18

I<sub>peak</sub> = 5A  
 I<sub>max</sub> = 3.5A  
 F = 305K

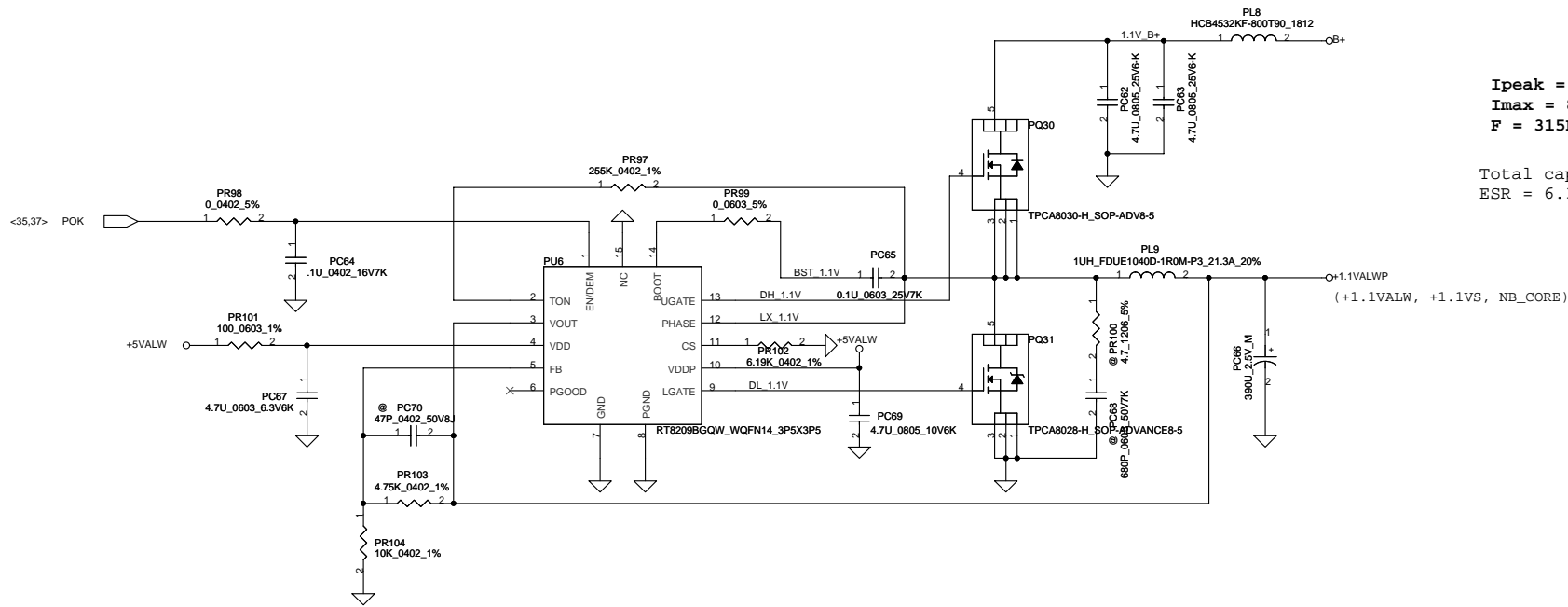
I<sub>peak</sub> = 5A  
 I<sub>max</sub> = 3.5A  
 F = 245K



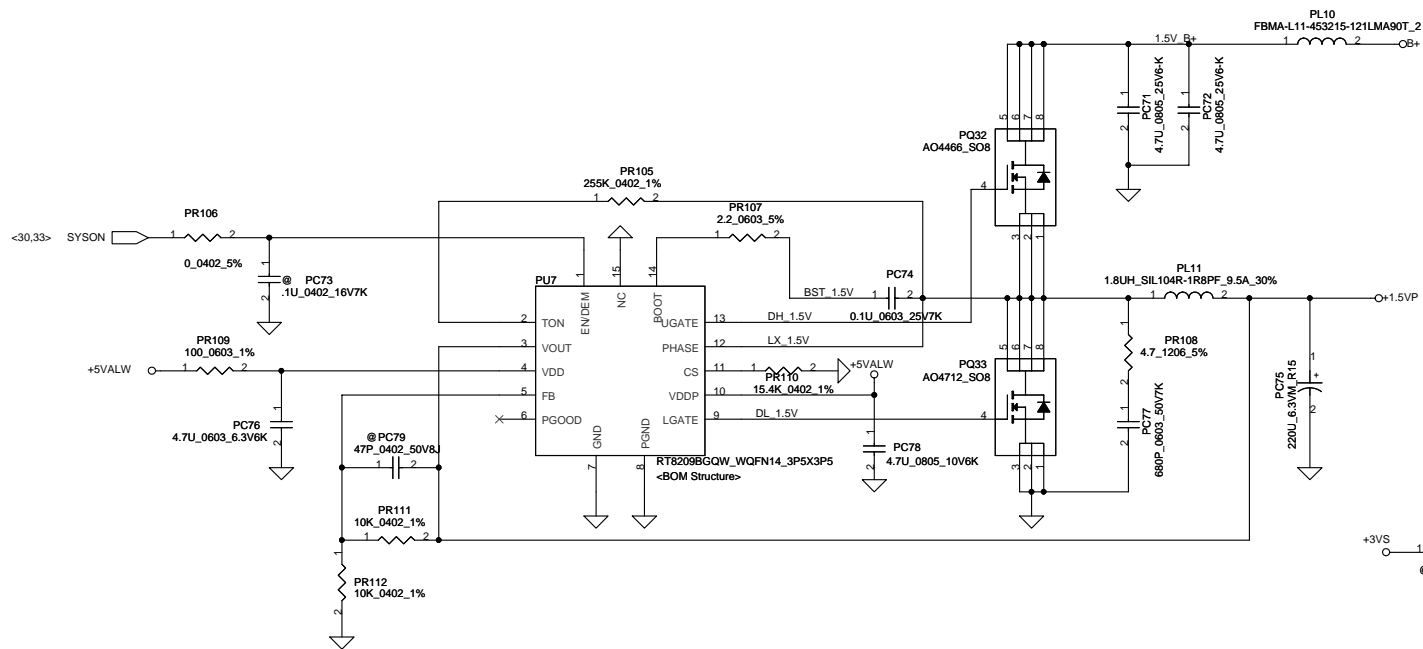
Total capacitor 220uF  
 ESR = 15mohm

Total capacitor 220uF  
 ESR = 15mohm

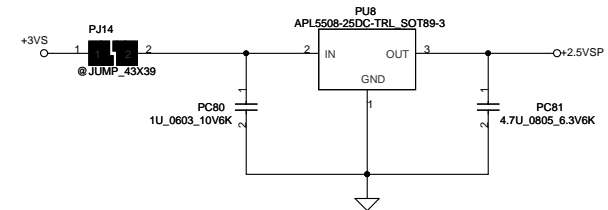
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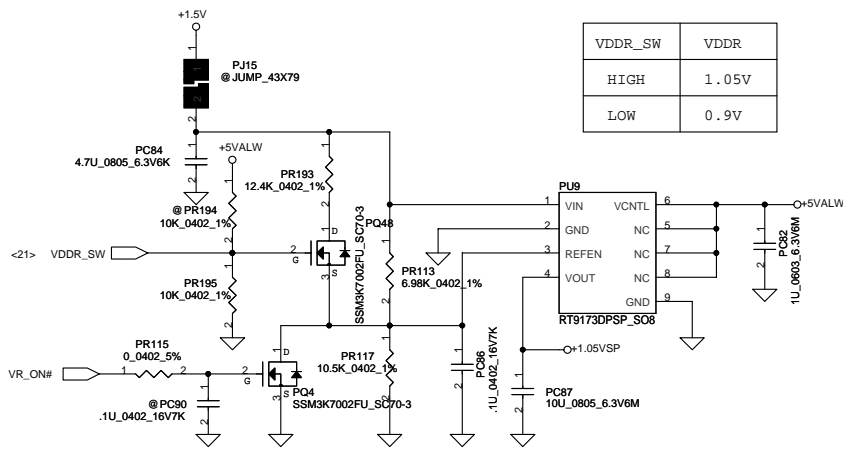
$I_{peak} = 12A$   
 $I_{max} = 8.4A$   
 $F = 315K$   
 Total capacitor 720µF  
 ESR = 6.3mohm



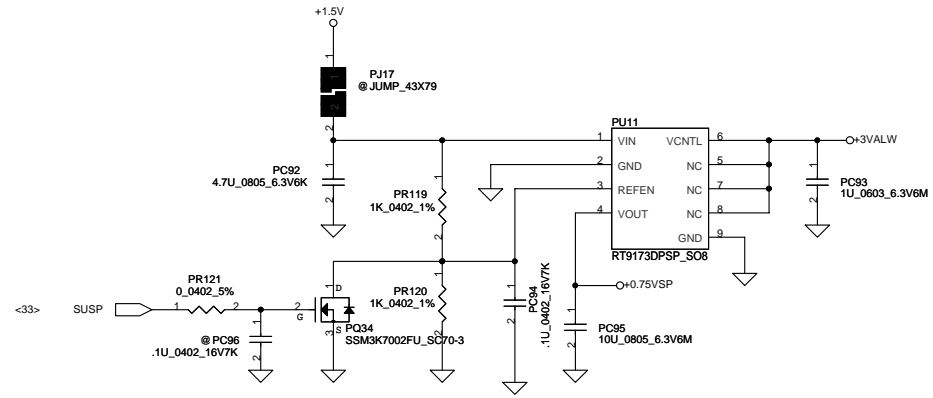
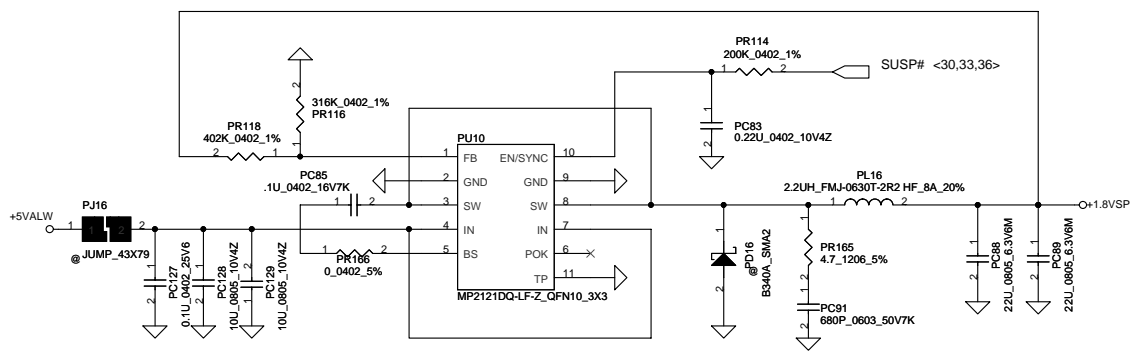
$I_{peak} = 7.5A$   
 $I_{max} = 5.25A$   
 $F = 315K$   
 Total capacitor 610µF  
 ESR = 6mohm



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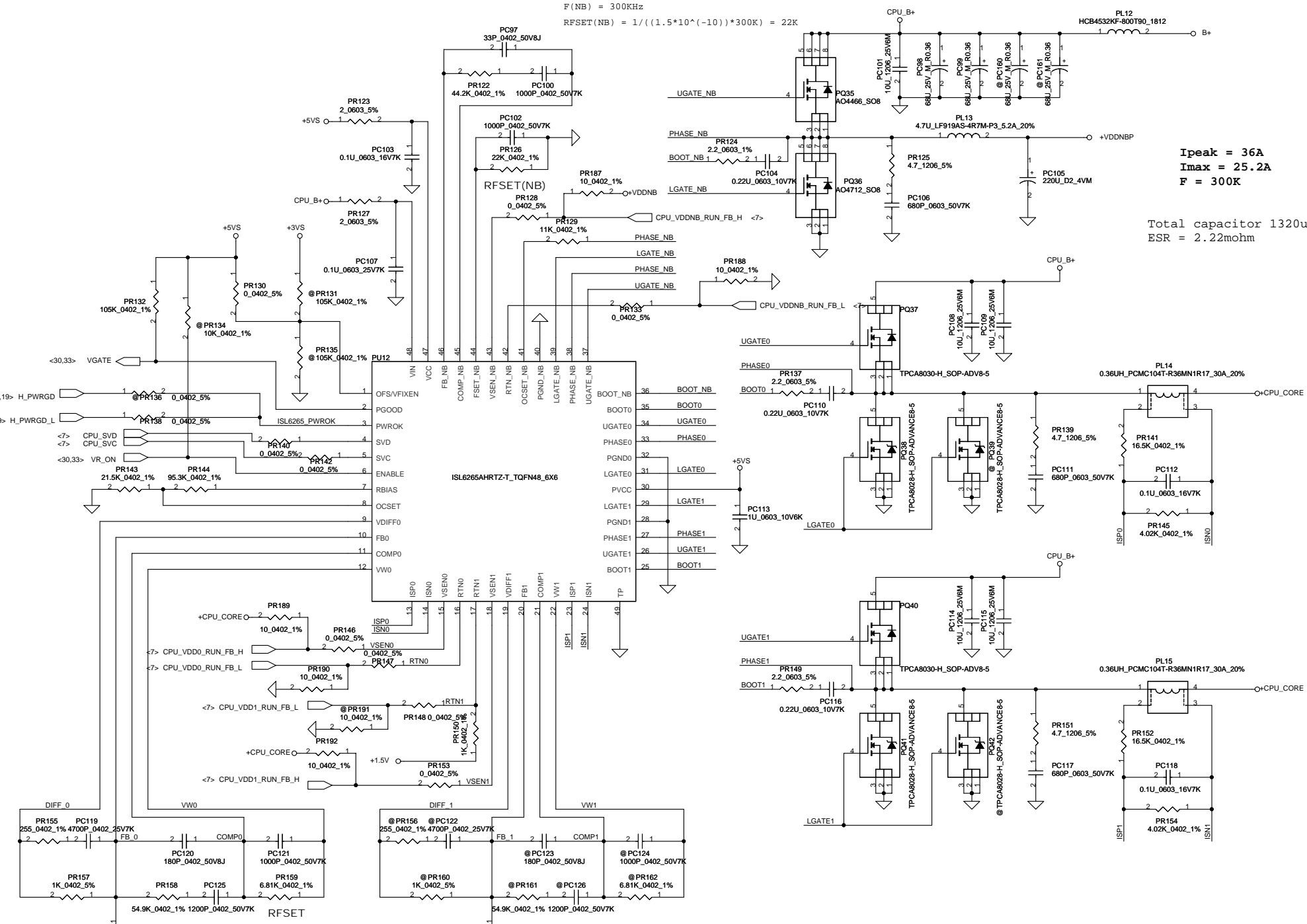


VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V



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F(NB) = 300KHz  
 RFSET(NB) = 1/((1.5\*10<sup>-10</sup>)\*300K) = 22K



I<sub>peak</sub> = 36A  
 I<sub>max</sub> = 25.2A  
 F = 300K

Total capacitor 1320uF  
 ESR = 2.22mohm

period = 1/300KHz = 3.33us  
 RFSET(K) = (3.33(us)-0.4)\*2.33 = 6.83(K)

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**PIR (Product Improve Record)**  
**NALAE LA-6053P SCHEMATIC CHANGE LIST**  
**REVISION CHANGE: 0.1 TO 0.2**

NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	33	Change JLEDB pin define as customer request
2	2009/12/14	25,28,30	Delete JODDB, JBT and JUSBB support pin
3	2009/12/14	33	Change JPOWER Pin2 from GND to NC
4	2009/12/15	28	Add R95 at WLAN Pin5 for BT/WLAN combo Mini Card
5	2009/12/15	25,30	Change U11, U25 P/N from SA00002XX00 to SA000033H00
6	2009/12/15	28	Reverse JBT pin definition
7	2009/12/16	27	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @
8	2009/12/17	33	Cgange JPOWER footprint to ACES_87151-1207_12P (ZIF_上接點)
9	2009/12/17	33	Cgange JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition
10	2009/12/17	33	Cgange JLEDB footprint to ACES_85201-1205N_12P (ZIF_上接點)
11	2009/12/17	25	Cgange JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)
12	2009/12/17	33	Change H36, H37 footprint from H_3P3 to H_3P8

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# Version Change List (P. I. R. List) for Power Circuit

Page#

Item Title

Solution Description

DVT : modification from EVT		
P38	change voltage divider to less than 10K	change PR104, PR111, PR112 to 10K; PR103 to 4.75K
P38	change OCP value	change PR102 to 6.19K
P39	enlarge output cap	change PC88, PC89 to 22uF(SH000000I10)
P40	don't use NIPPON cap	change PC98, PC99 to SF000000S80
P40	pull high RTN1 1.5V	change PR150 to mount
P38	EMI request	change PL10 to SM01000D000; change PR107 to 2.2ohm; add PR108 4.7ohm; add PC77 680pF
P40	EMI request	change PR137, PR149 to 2.2ohm; add PR139, PR1514.7ohm; add PC111, PC117 680pF
P37	choke need to meet thermal module height	change PL6, PL7 to SH000006380
P37	EMI request	change PR87, PR88 to 2.2ohm
P40	production line request	change PC98, PC99 to 68uF; add PC160, PC161 68uF
P36	EMI request for ISN issue	add PC162, PC163, PC164 10uF 1206
P39	mount snubber circuit	mount PR165, PC91
P35	OTP setting common	change PR30 and PR31 to 19.6K; PR34 to 7.87K; PR33 to 8.66K
P39	change IC to low cost	change P09 and P11 to RT9173
P39	change VDER(1.05V) circuit to switchable	add PR193, PR194, PR195 & PQ48
PVT : modification from DVT		
P40	cost down	change PC98, PC99, PC160, PC161 to SF000000W00
P37	common circuit	change PC45 to 1uF
P37	common circuit	mount PC59
P37	change PQ29 solution	change PQ29 to DTC1158UA
P36	add 65W/75W selection circuit	Add PR35 and PQ5
P38	prevent OVP for HW's cost down	change PC66 to 390uF
P36	EMI request for ISN issue	Add PC166, PC167, 10uF 1206
P37	EMI request for ISN issue	Add PC168, 10uF 1206
P40	EMI request	mount snubber circuit PR125, PC106
P38	EMI request for ESD issue	mount PC64 0.1uF
PreMP : modification from PVT		
P35	Thermal request change OTP	change PR30, PR31 to 23.7K; PR33, PR34 to 11.3K
P36	modify 65W/75W resistor	change PR35 to 12.4K
P34	modify RTC circuit	

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