

# Compal confidential

## *Hamburg 10AD*

### NALAE LA-6053P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

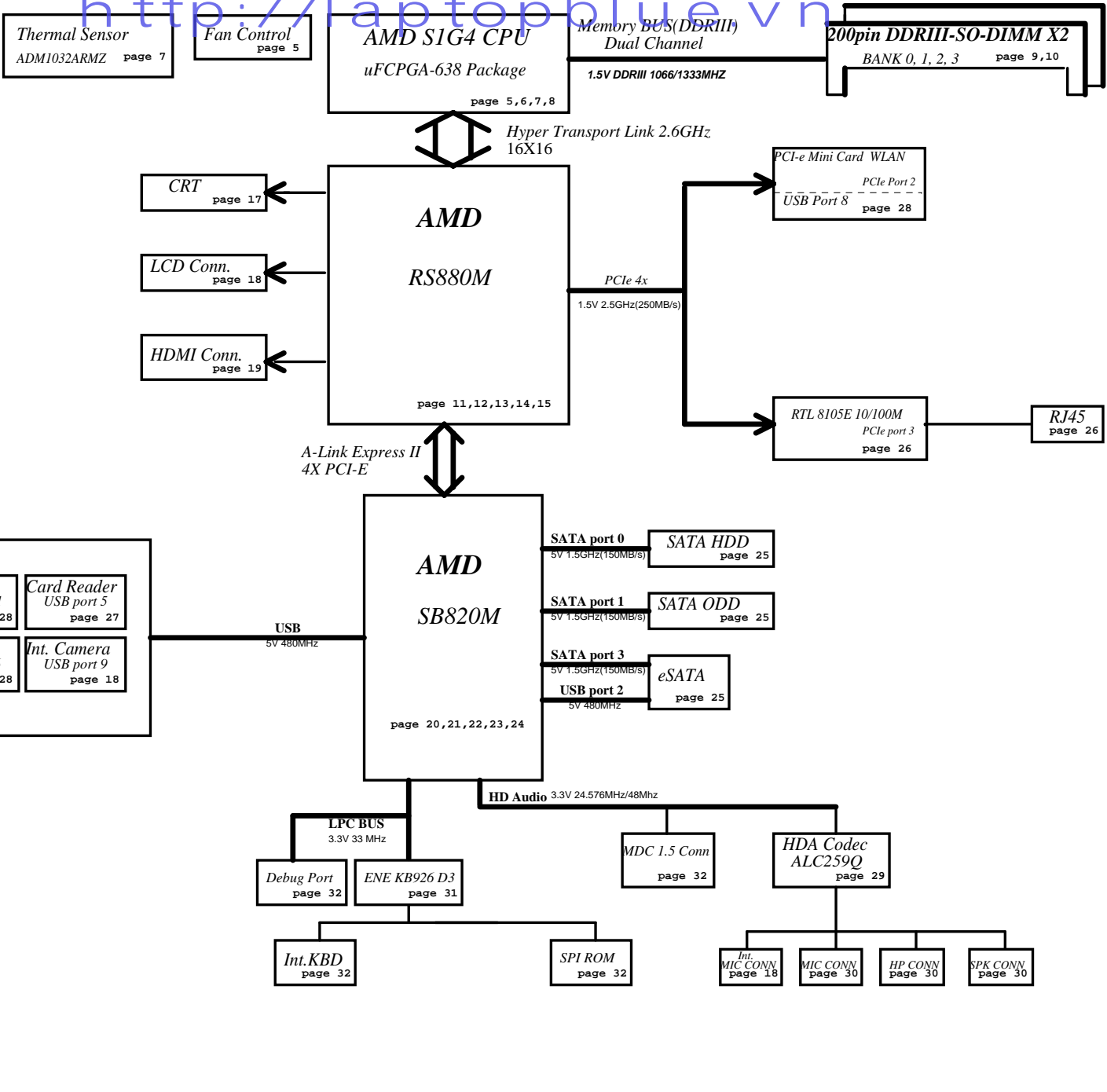
2009-02-04 Rev. 0.2

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Model Name : NALAE

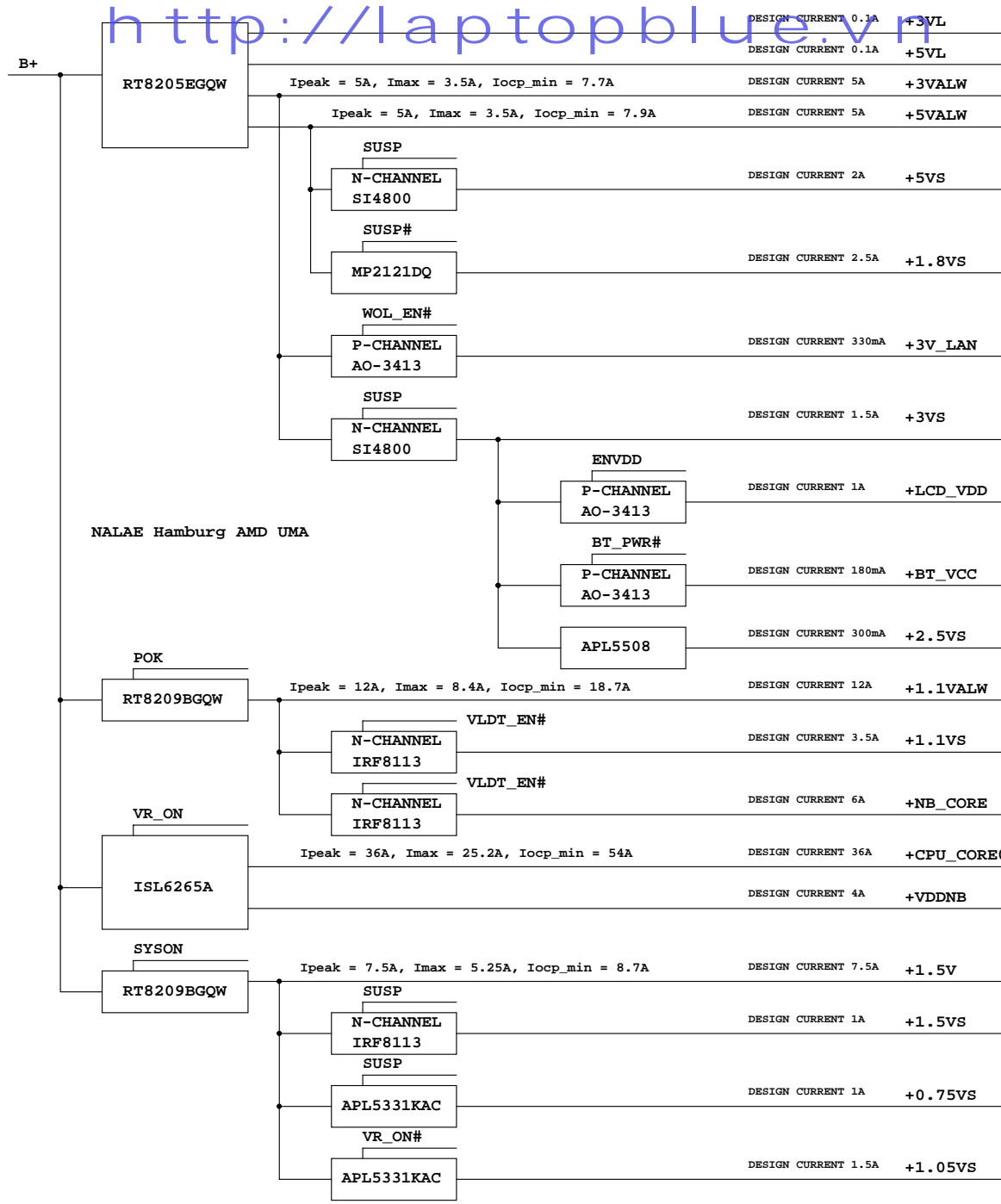
File Name : LA-6053P



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- Power On/Off CKT.  
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- DC/DC Interface CKT.  
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NALAE Hamburg AMD UMA

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### Voltage Rails

O : ON  
X : OFF

State	power plane	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VDDNB +CPU_CORE +NB_CORE
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

@ : just reserve , no build

### BTO (Build-To-Order) Option Table

Function	BLUE TOOTH	HDMI				
Description	( B )	( Y )				
Explain						
BTO	BT@	H@				

### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A2	10100010
CLOCK GENERATOR (EXT.)	D2	11010010

### EC SM Bus1 address

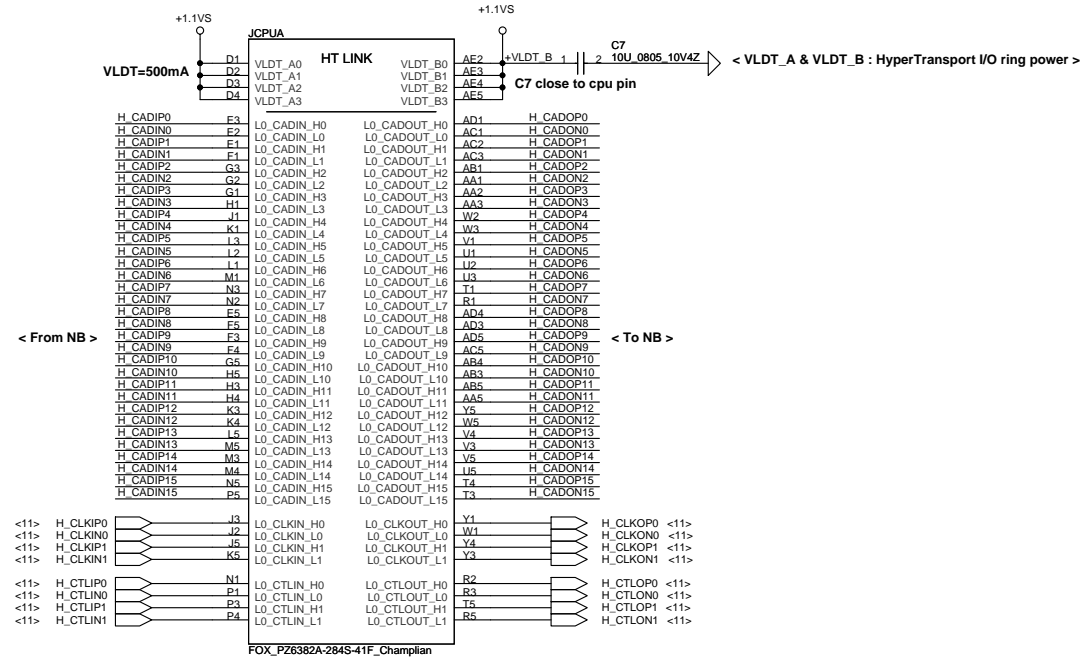
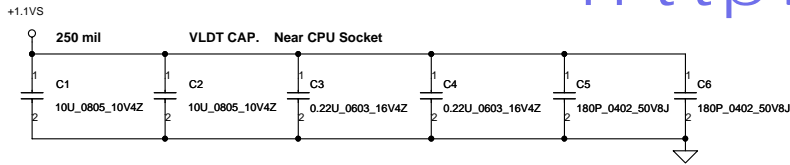
Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D3		

### EC SM Bus2 address

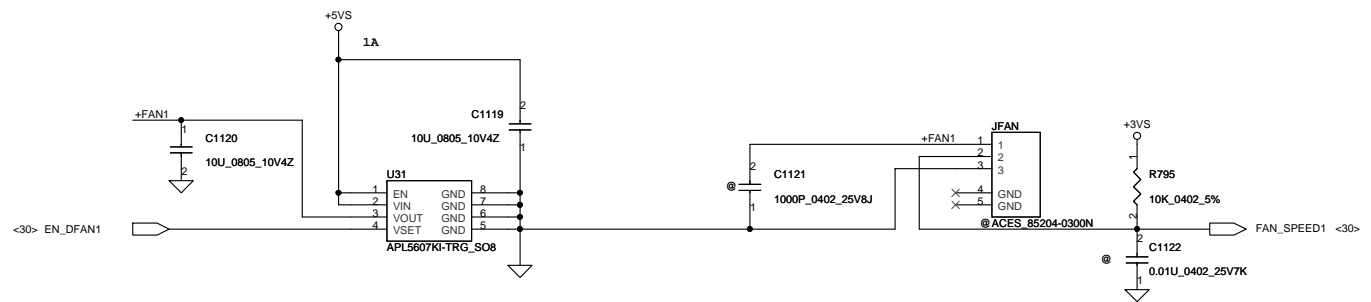
Device	HEX	Address
ADH1032-1 CPU	98H	1001 100X b
ADH1032-2 VGA	9AH	1001 101X b
EC KB926D3		

### SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V						
EC_SMB_CK2 EC_SMB_DA2	KB926		V					
I2C_CLK I2C_DATA	RS880M						V	
DDC_CLK0 DDC_DATA0	RS880M							V
SCL0 SDA0	SB820			V	V			
SCL1 SDA1	SB820					V		

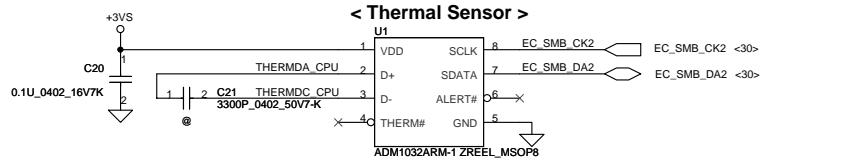
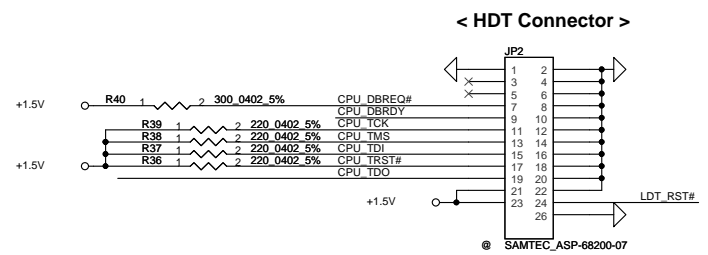
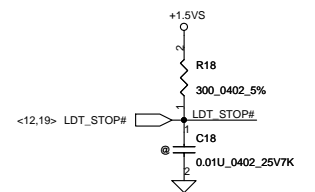
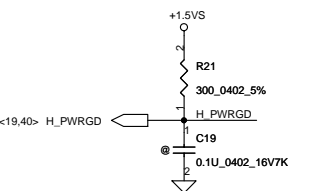
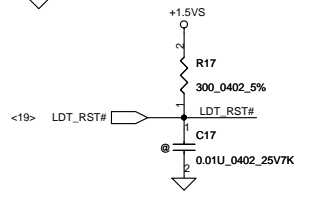
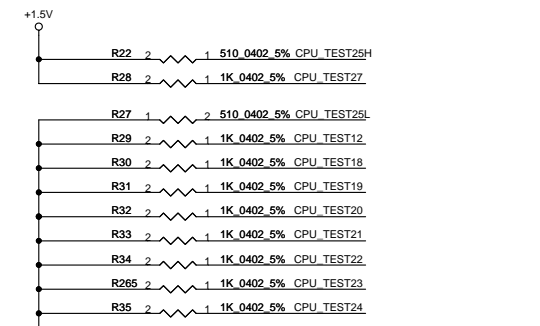
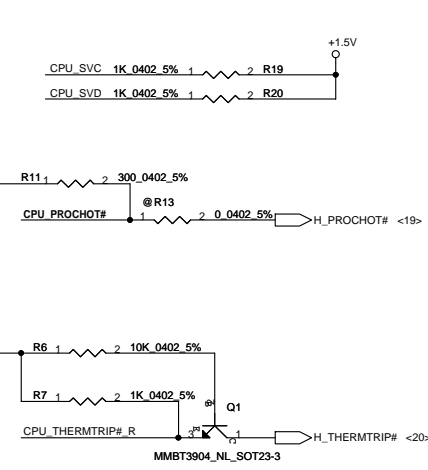
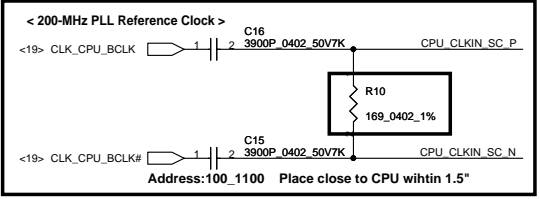
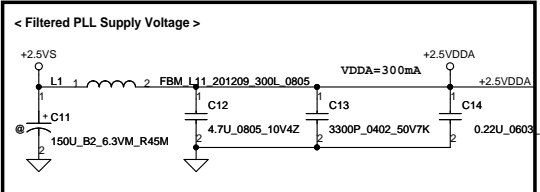


< FAN Control Circuit : Vout = 1.6 x Vset >



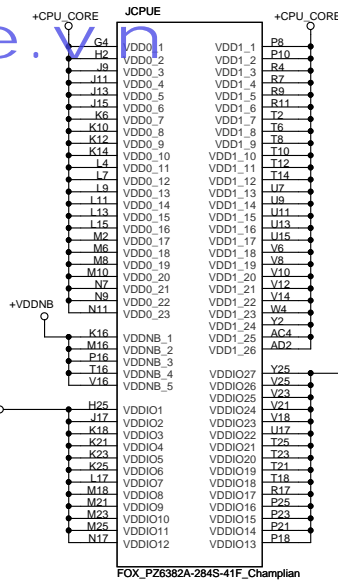
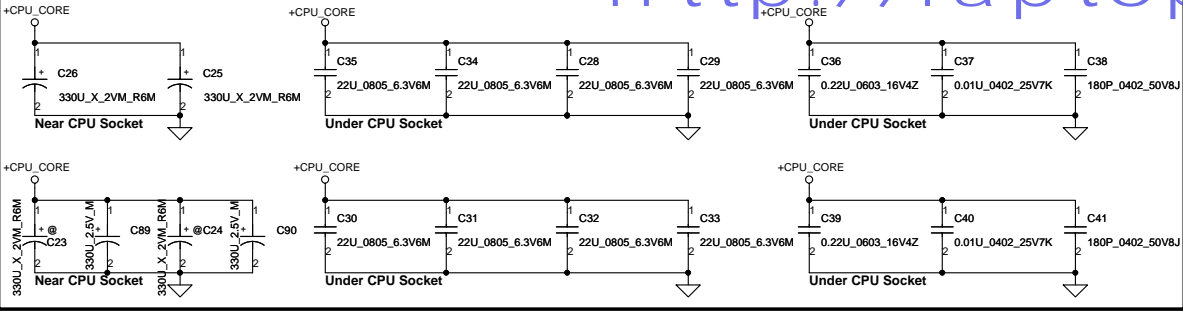
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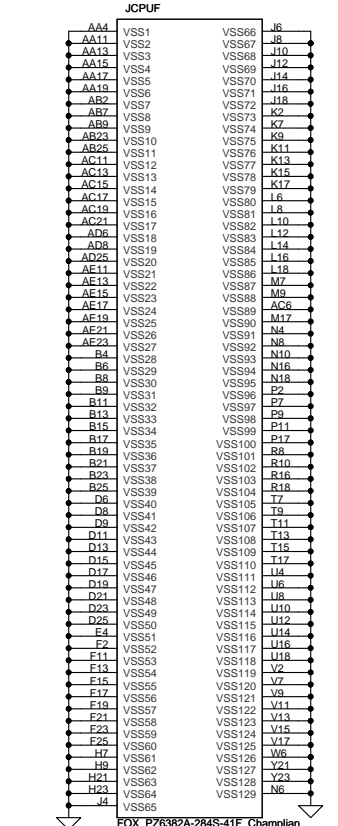
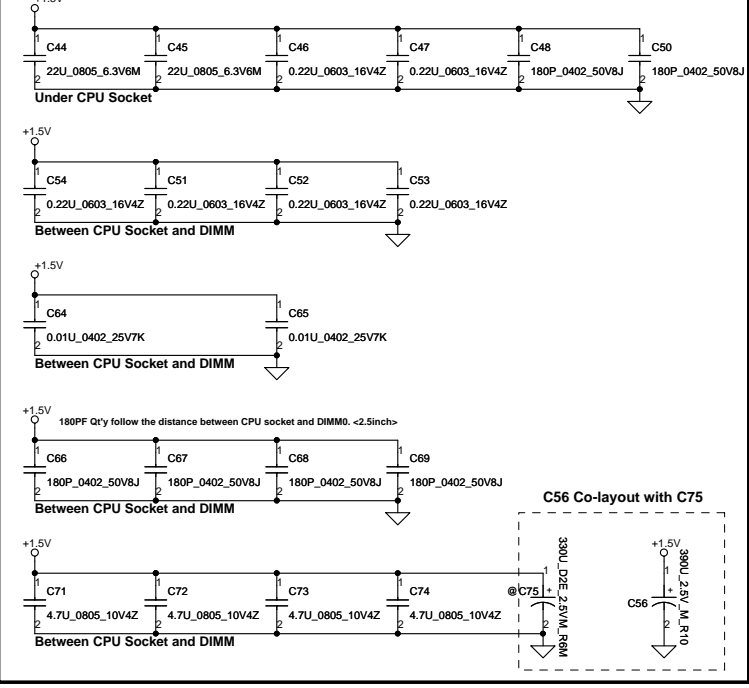


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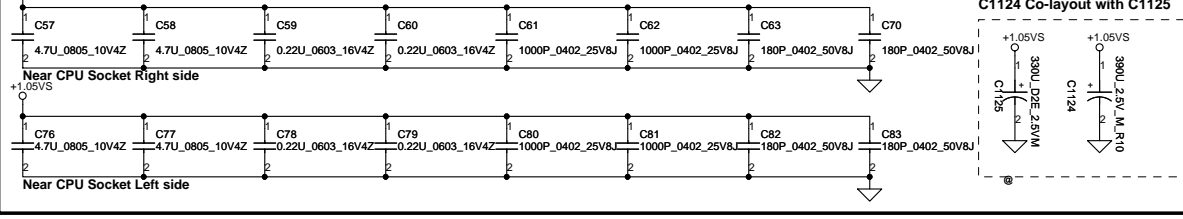
**VDD decoupling : +CPU\_CORE**



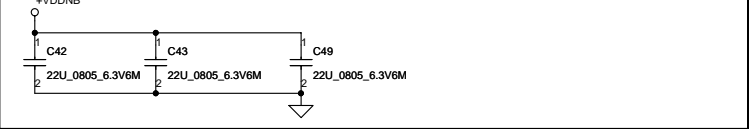
**VDDIO decoupling : DDR SDRAM I/O ring power**



**VTT decoupling.**

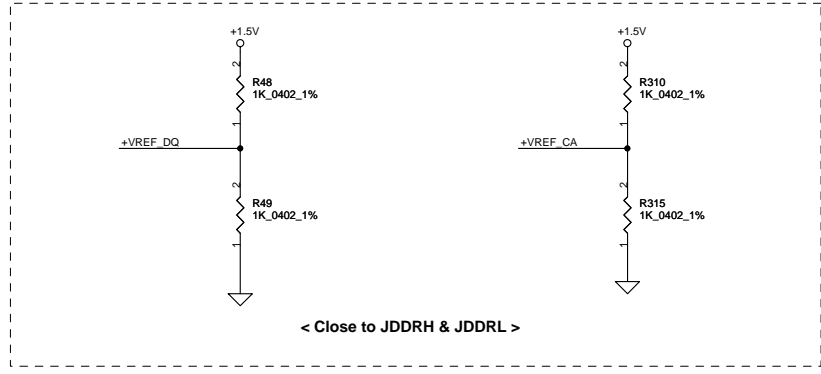
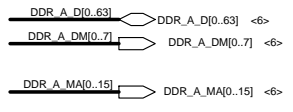
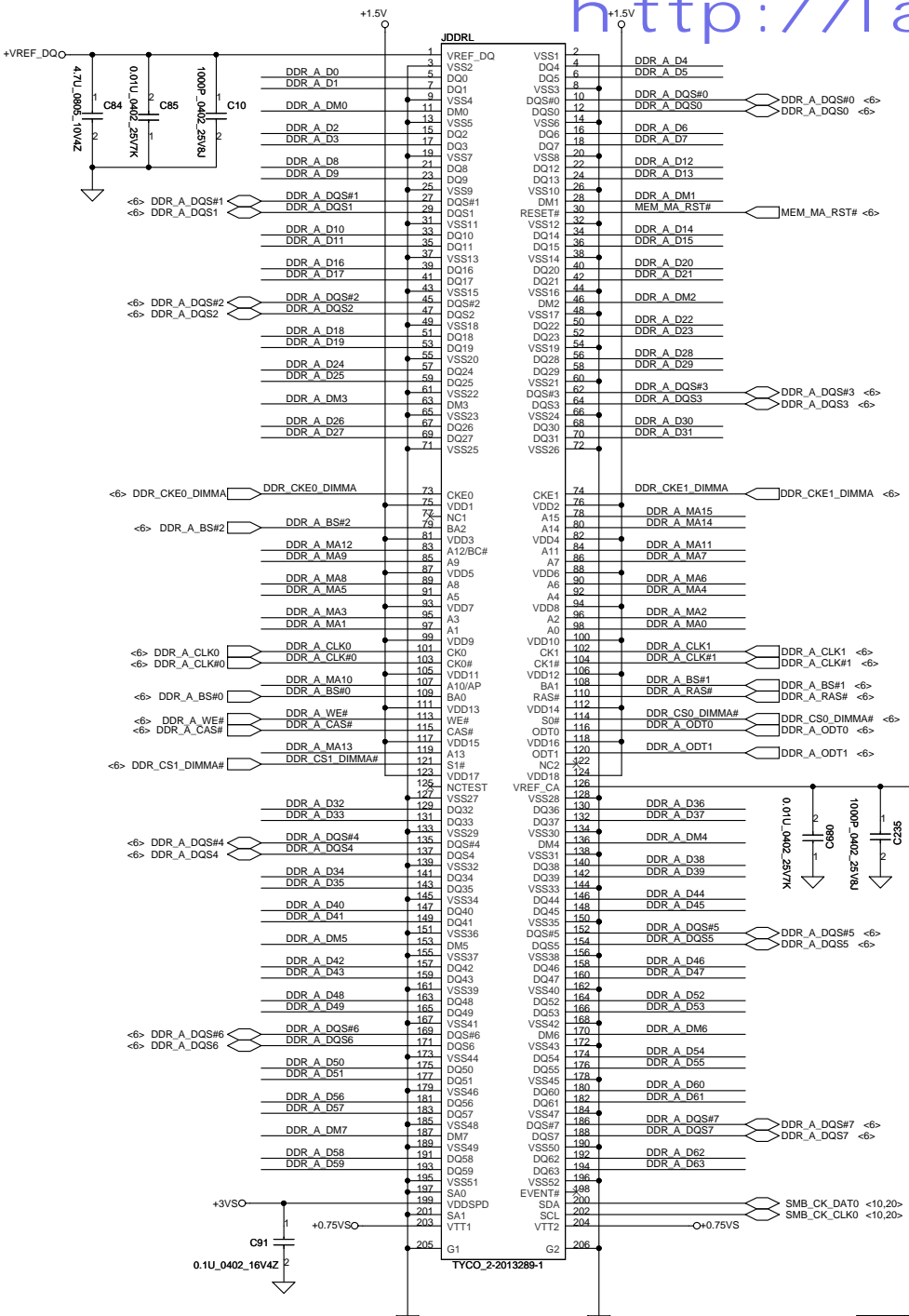


**+VDDNB decoupling : Northbridge power**

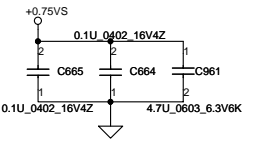
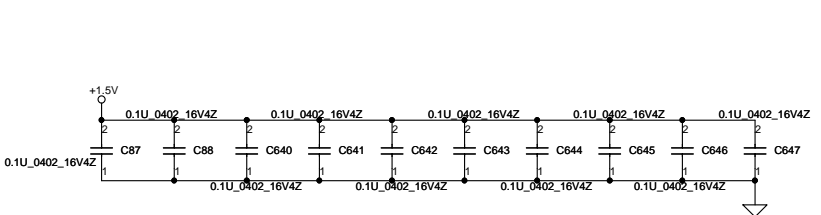


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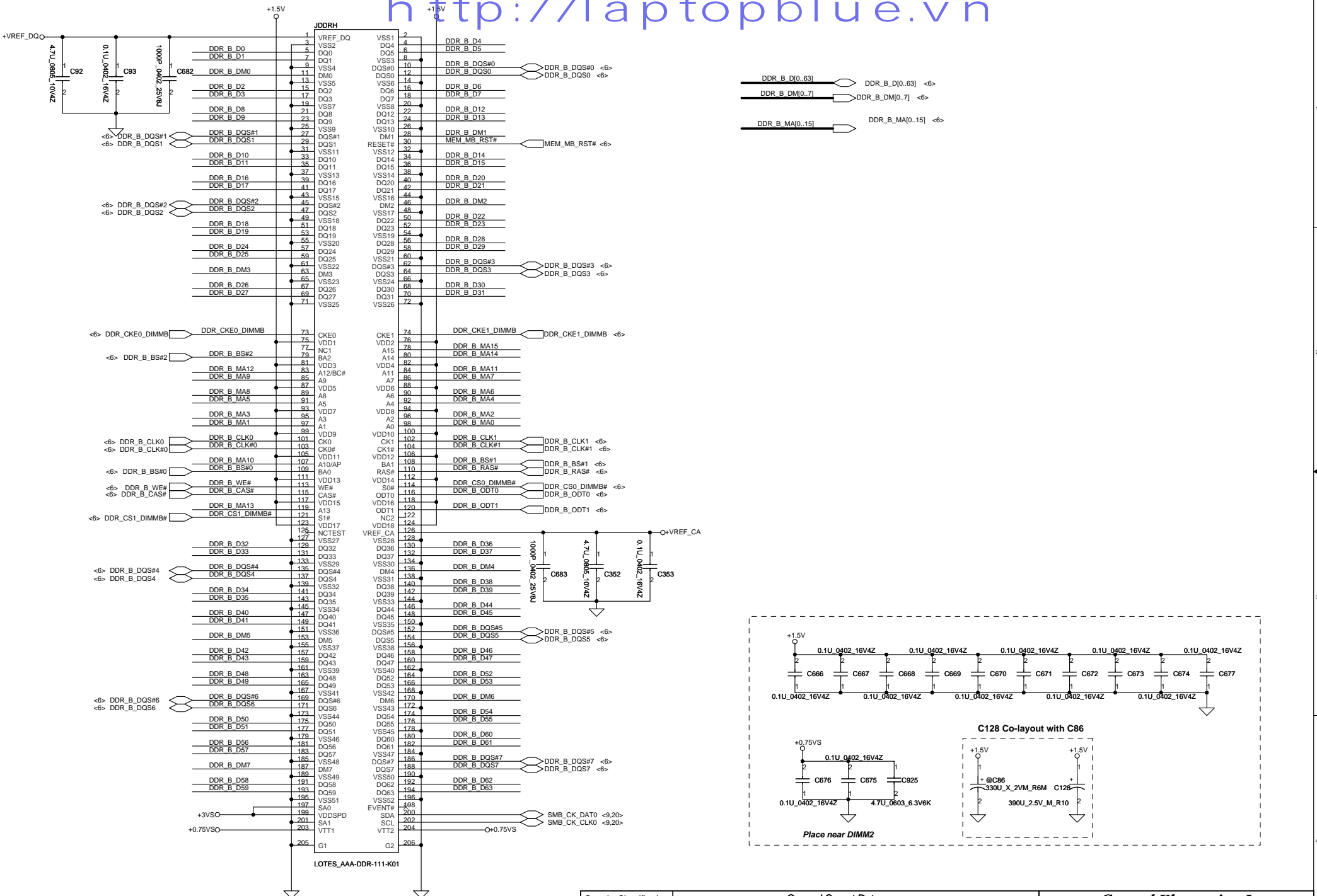
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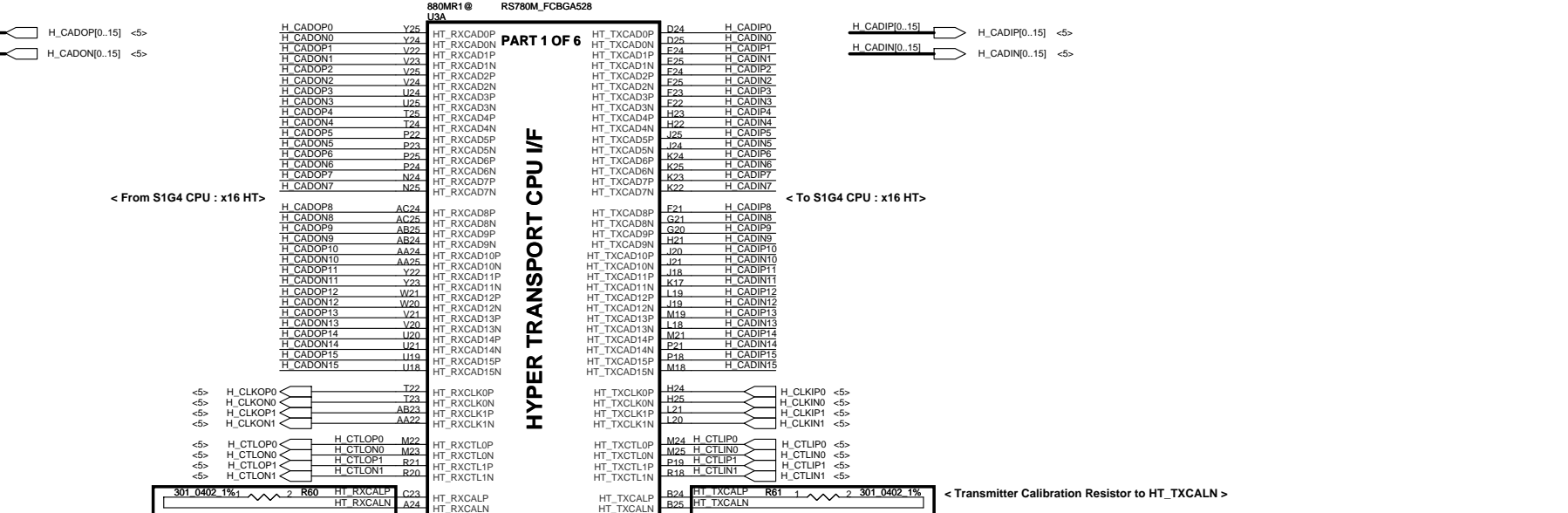
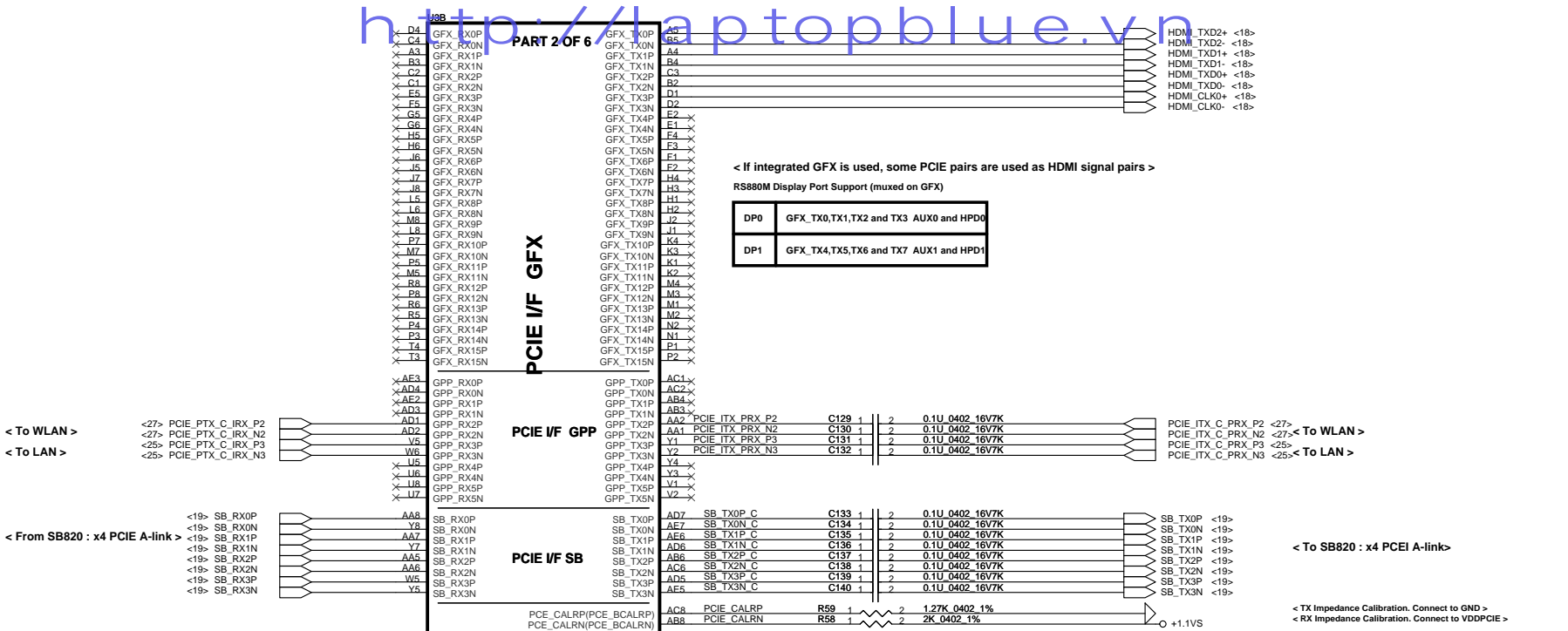


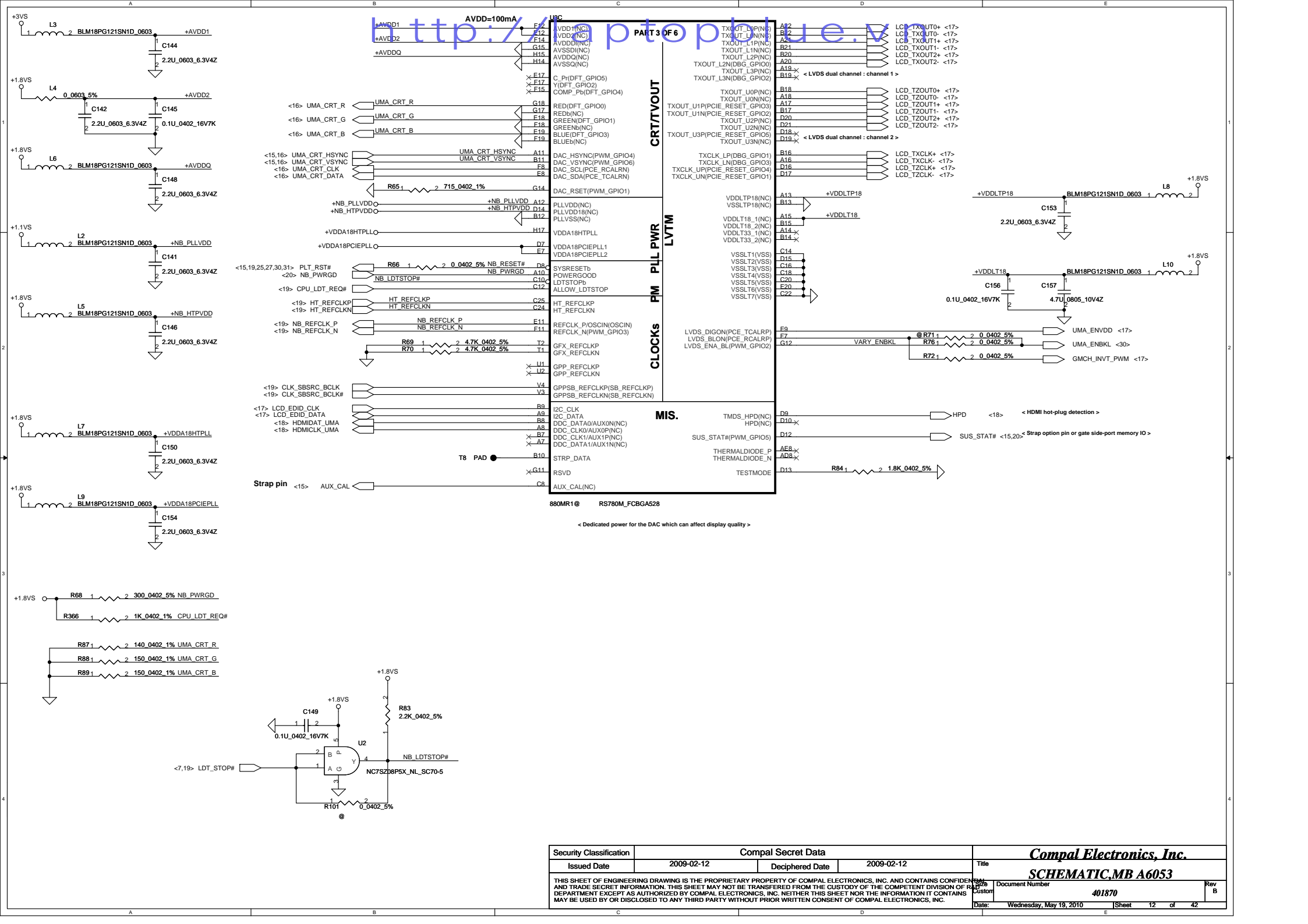
Place near DIMM1

**DIMM\_A STD H:5.2 mm**  
 <Address: 00>

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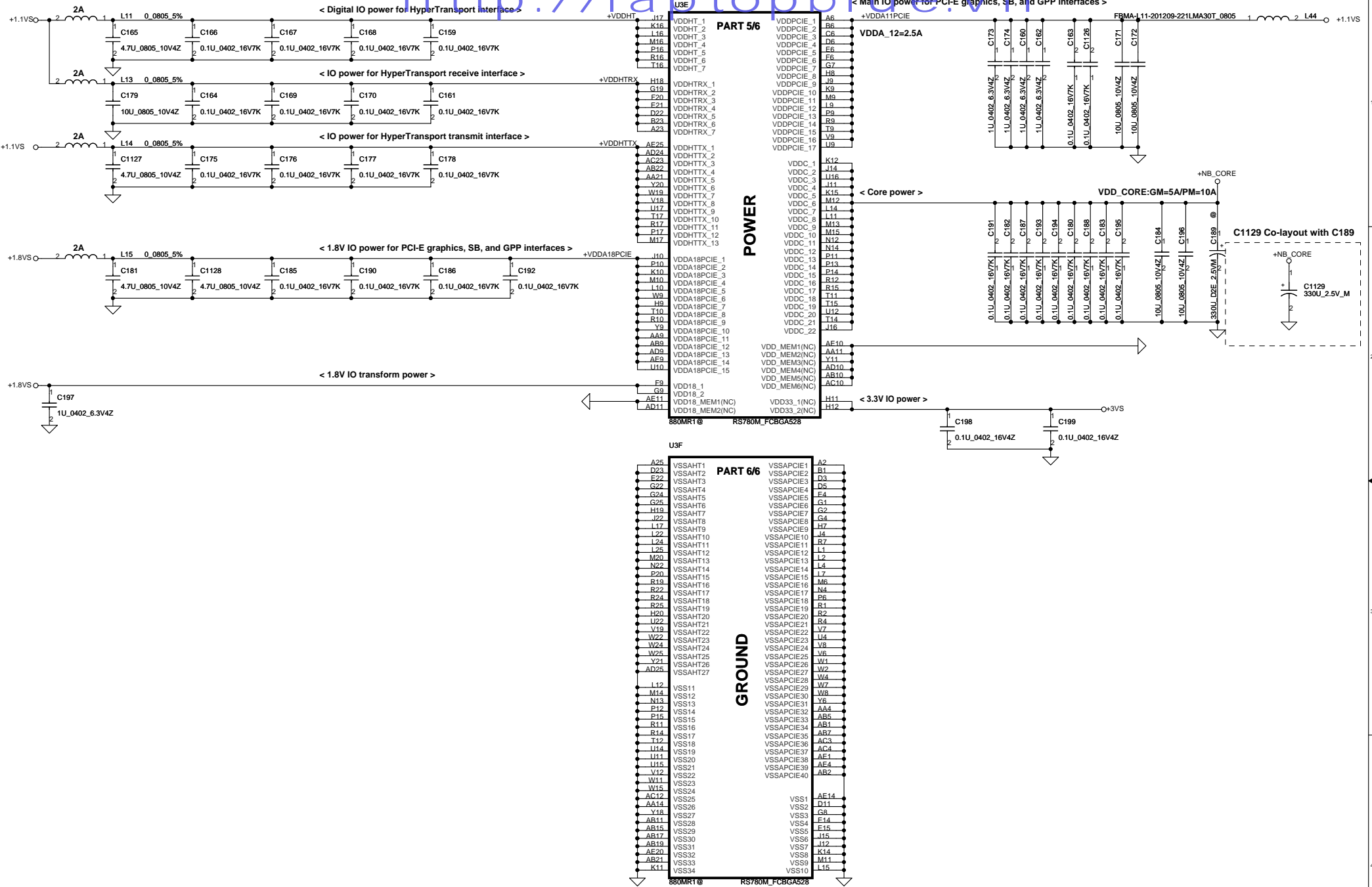
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USD			
>AB12	MEM_A0(NC)	MEM_DQ0/DVO_VS(NC(NC))	AA18
>AE16	MEM_A1(NC)	MEM_DQ1/DVO_HS(NC(NC))	AA20
>Y11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA15
>AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
>AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17
>AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
>AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
>AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
>AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
>AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
>AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
>AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
>AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
>Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
>AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)	AC22
>AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)	AD21
>AD17	MEM_BA2(NC)		
>W12	MEM_RASb(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17
>Y12	MEM_CASb(NC)	MEM_DQS0N/DVO_IDCKN(NC)	W18
>AD18	MEM_WEB(NC)	MEM_DQS1P(NC)	AD20
>AB13	MEM_CSB(NC)	MEM_DQS1N(NC)	AE21
>AB12	MEM_CKE(NC)	MEM_DM0(NC)	W17
>Y14	MEM_ODT(NC)	MEM_DM1/DVO_D8(NC)	AE19
>V15	MEM_CKP(NC)	IOPLLVD18(NC)	AE23
>W14	MEM_CKN(NC)	IOPLLVD1(NC)	AE24
>AE12	MEM_COMP(NC)	IOPLLVS(NC)	AD23
>AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18

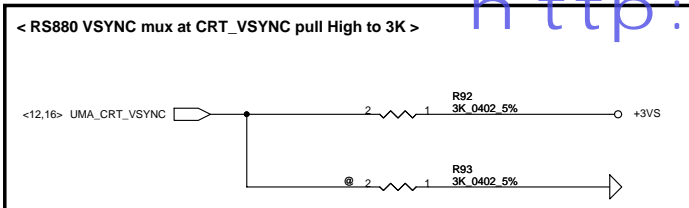
SBD\_MEM/DVO\_I/F

880MR1@ RS780M\_FCBGA528

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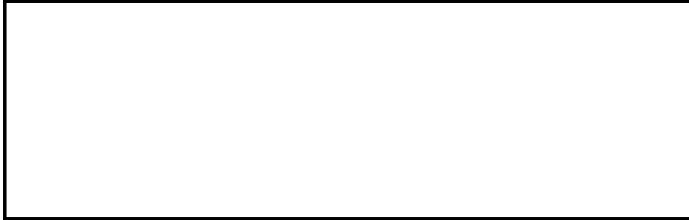


< VSYNC : STRAP\_DEBUG\_BUS\_GPIO\_ENABLE# >

Enables the Test Debug Bus using GPIO.

0 : Enable  
1 : Disable

PIN: RS880--> VSYNC

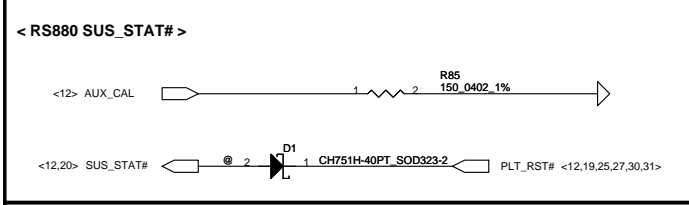


< SUS\_SATA# : LOAD\_EEPROM\_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS\_STAT#



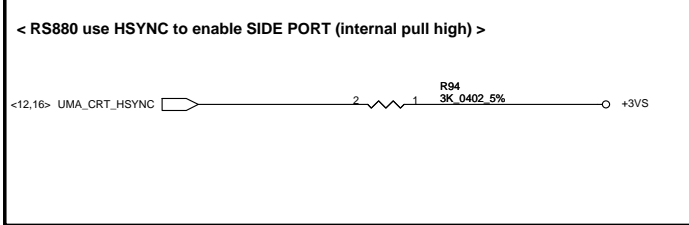
< HSYNC : STRAP\_DEBUG\_BUS\_PCIE\_ENABLE# >

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

RS880: Enables Side port memory ( RS780 use HSYNC#)

1. Disable (RS880)  
0 : Enable (RS880)



< HSYNC : STRAP\_DEBUG\_BUS\_PCIE\_ENABLE# >

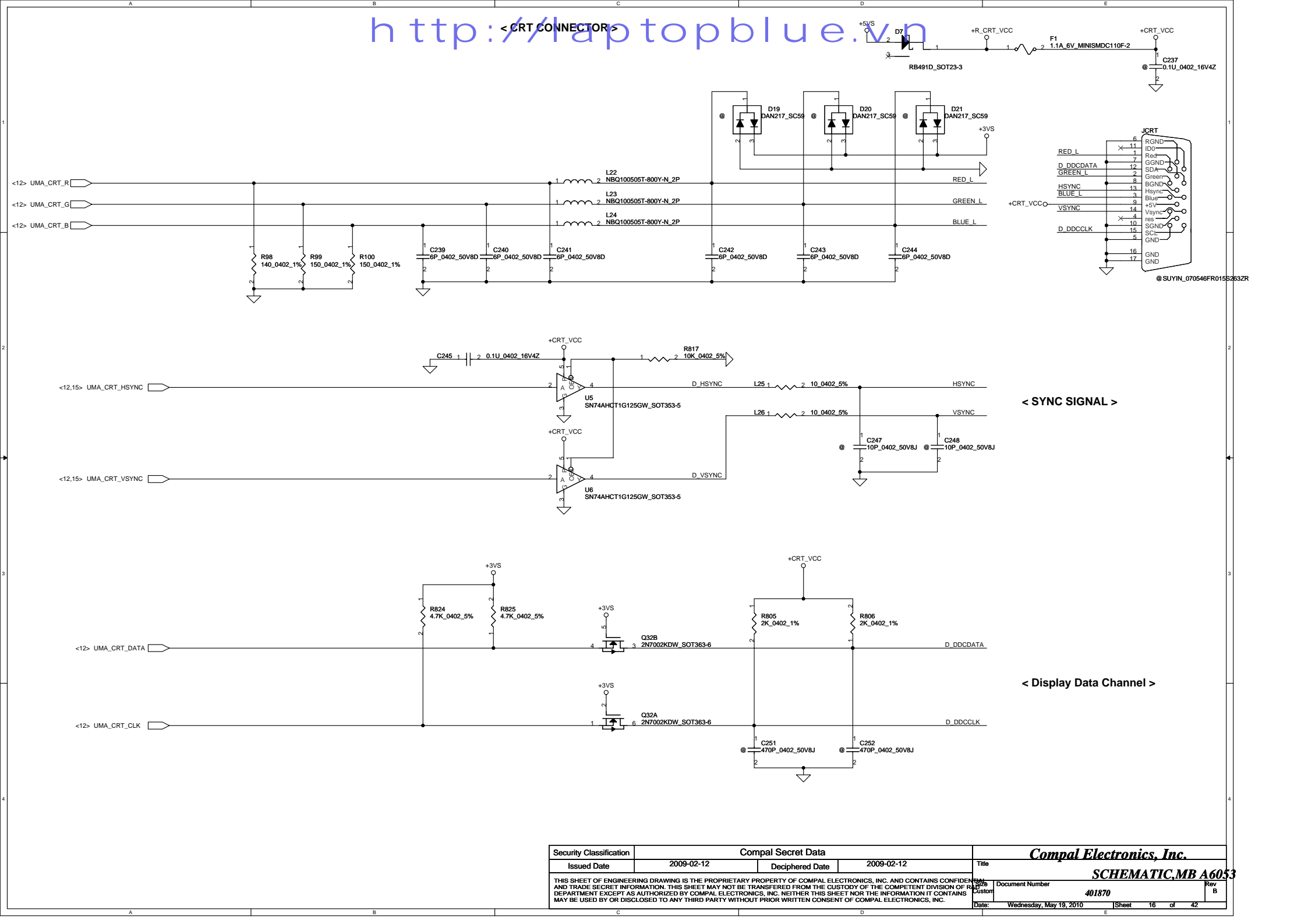
RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

RS880: Enables Side port memory ( RS780 use HSYNC#)

1. Disable (RS880)  
0 : Enable (RS880)

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JCRT

6	RGND
11	IDJ
1	Red
7	GND
12	SDA
2	GREEN L
8	BGND
3	Blue
13	Hsync
9	+5V
4	Vsync
10	res
14	SGND
15	SCL
5	GND
16	GND
17	GND

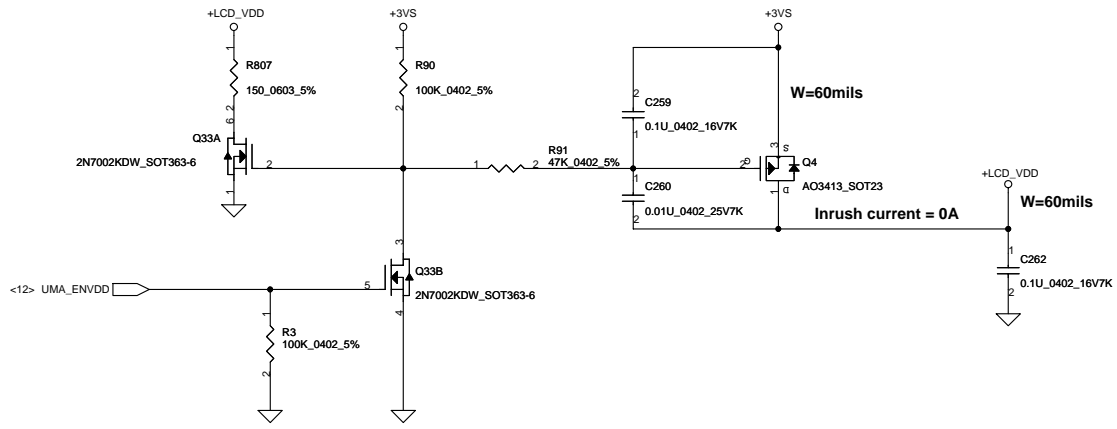
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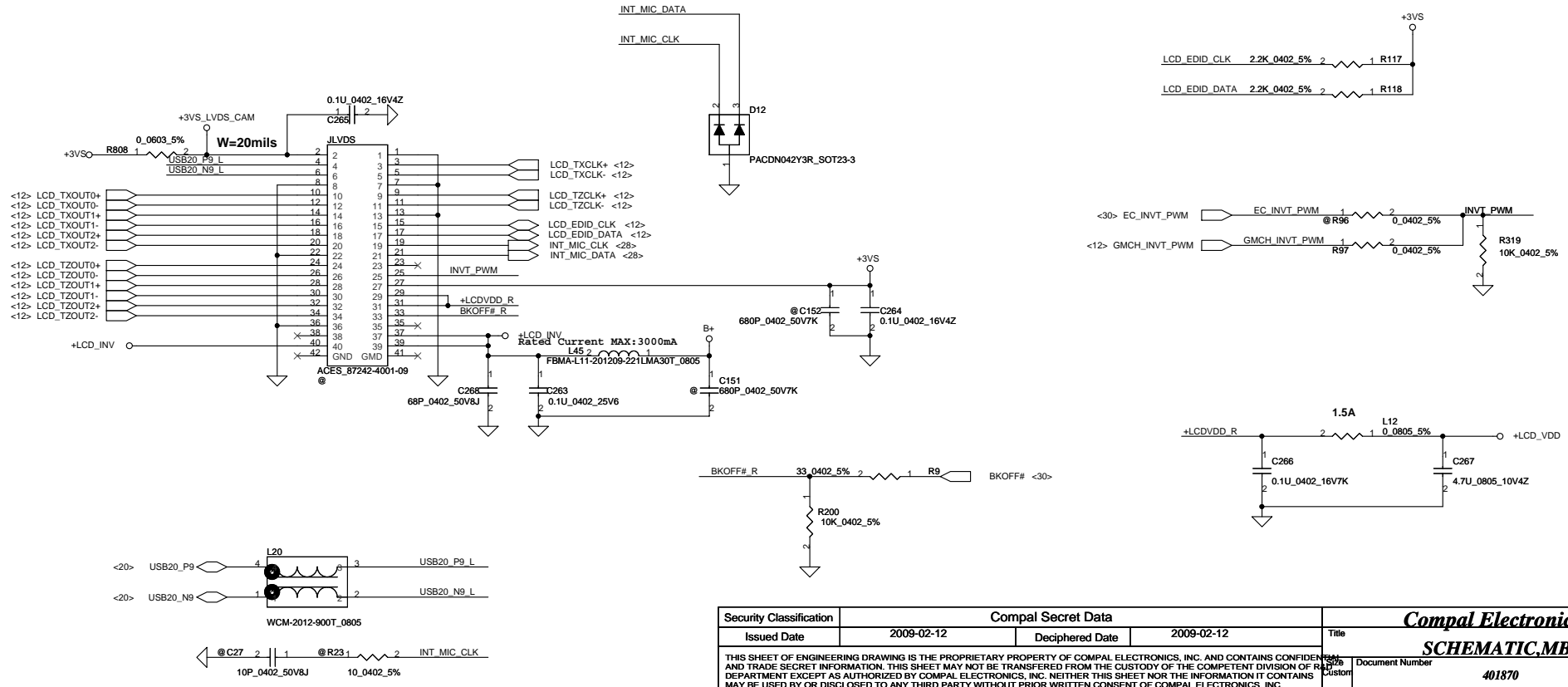
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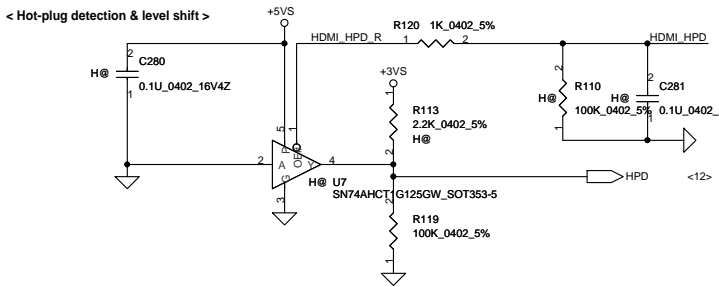
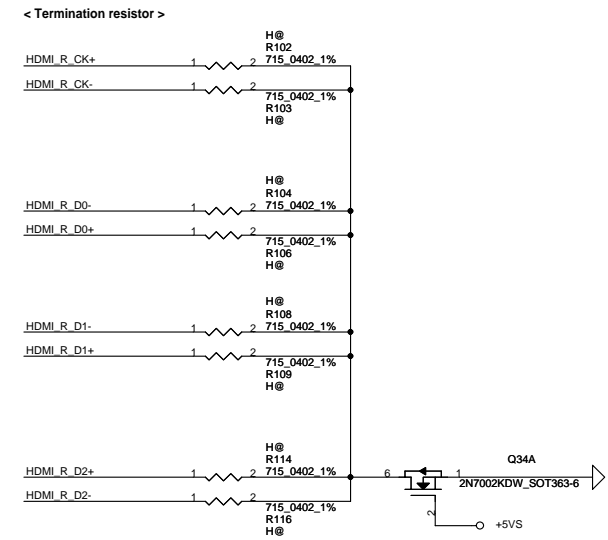
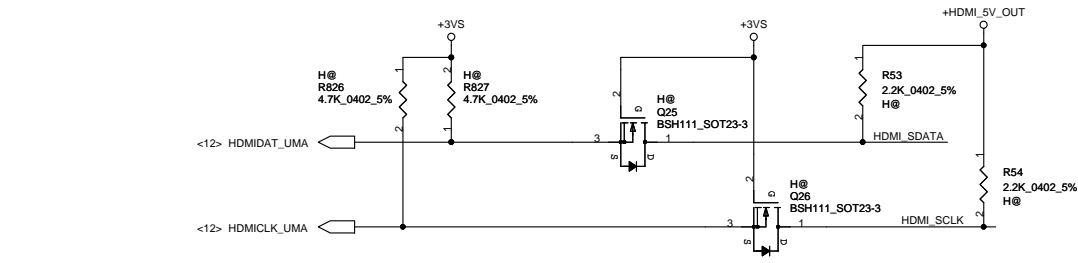
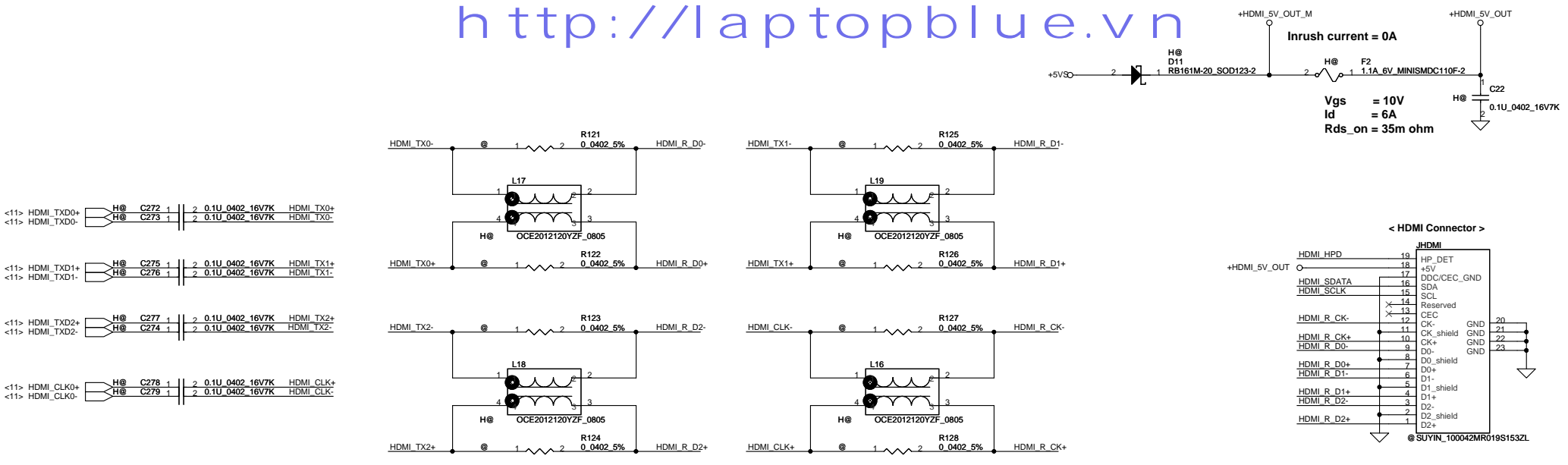
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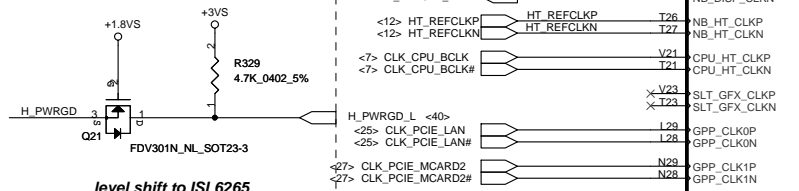
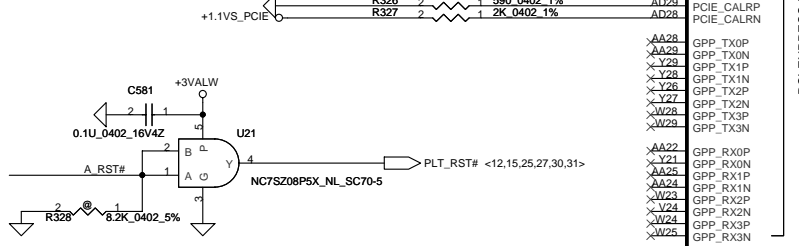
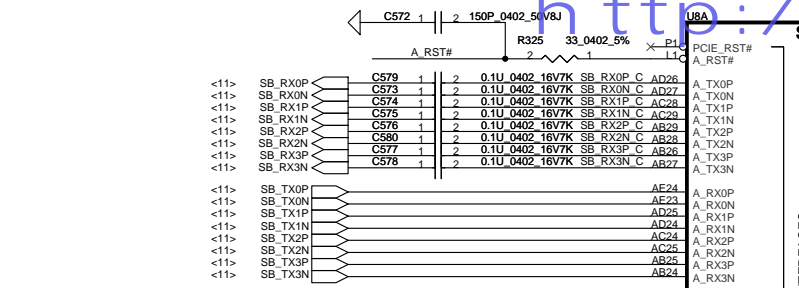


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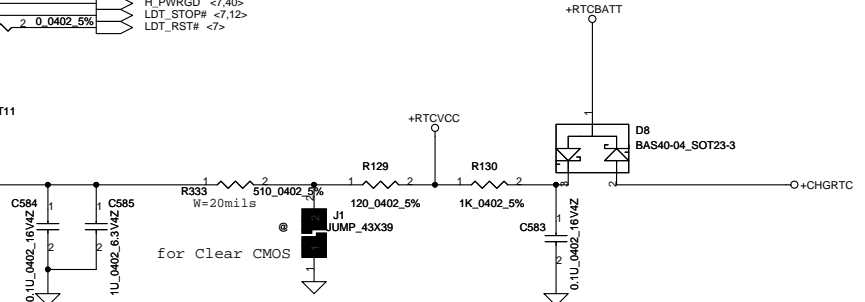
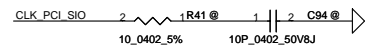
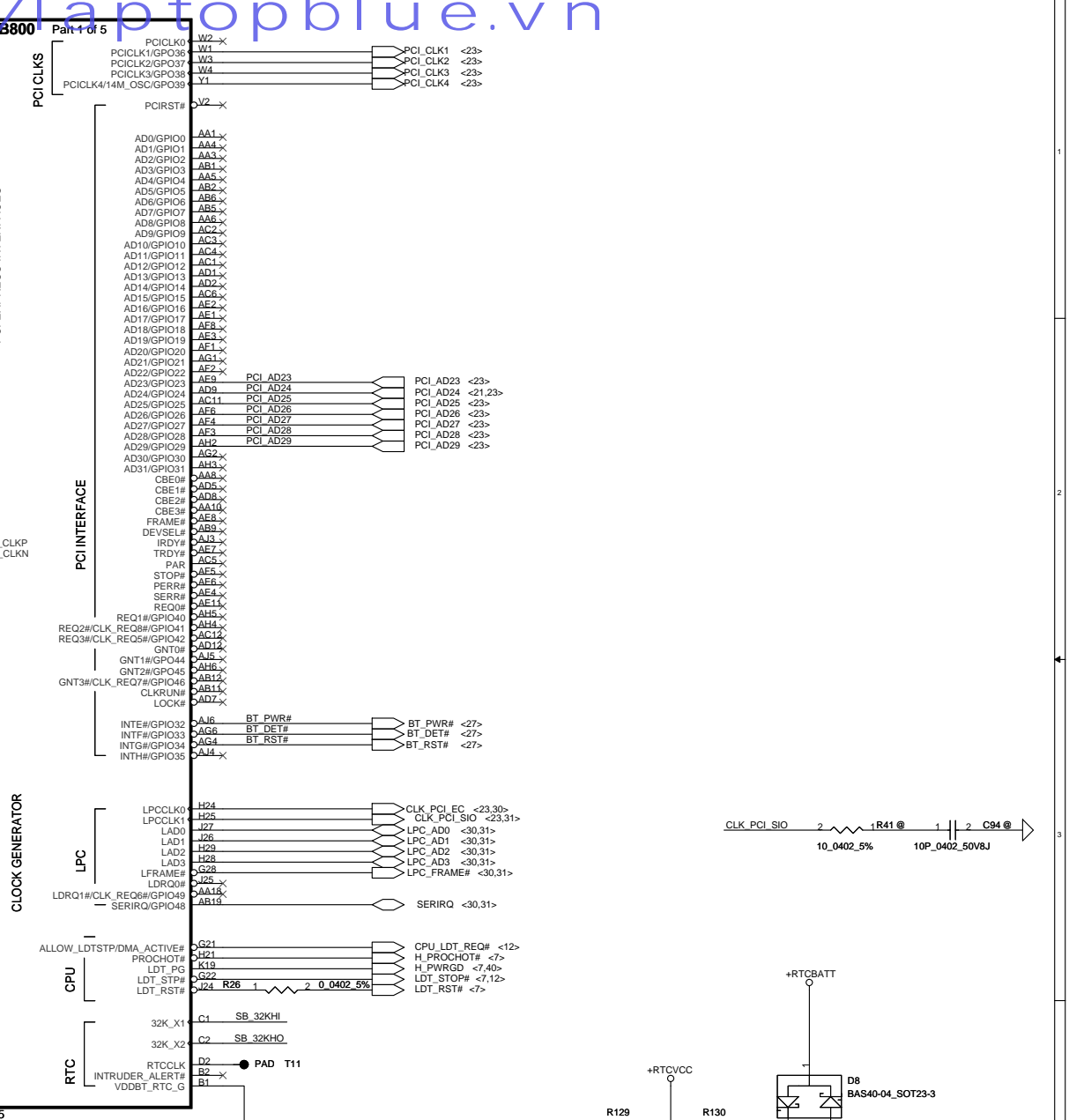
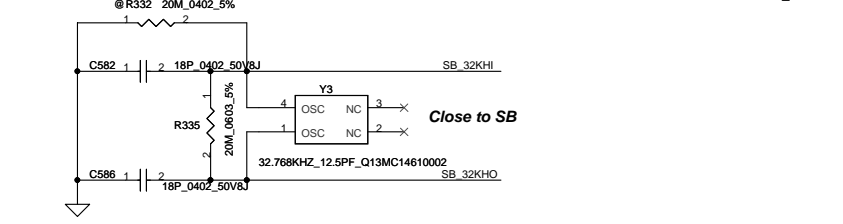
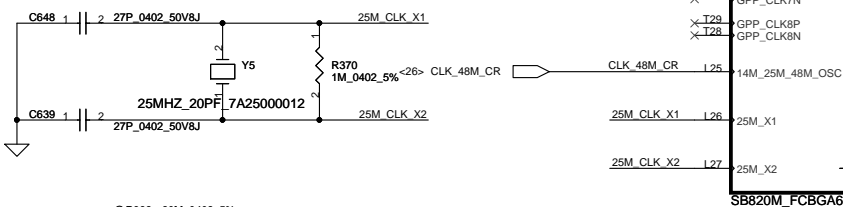




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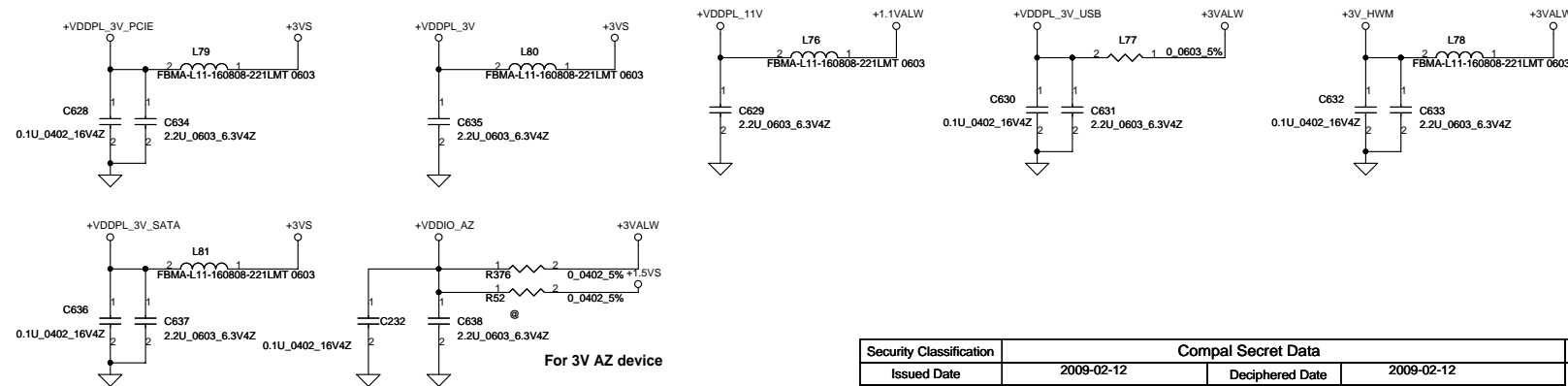
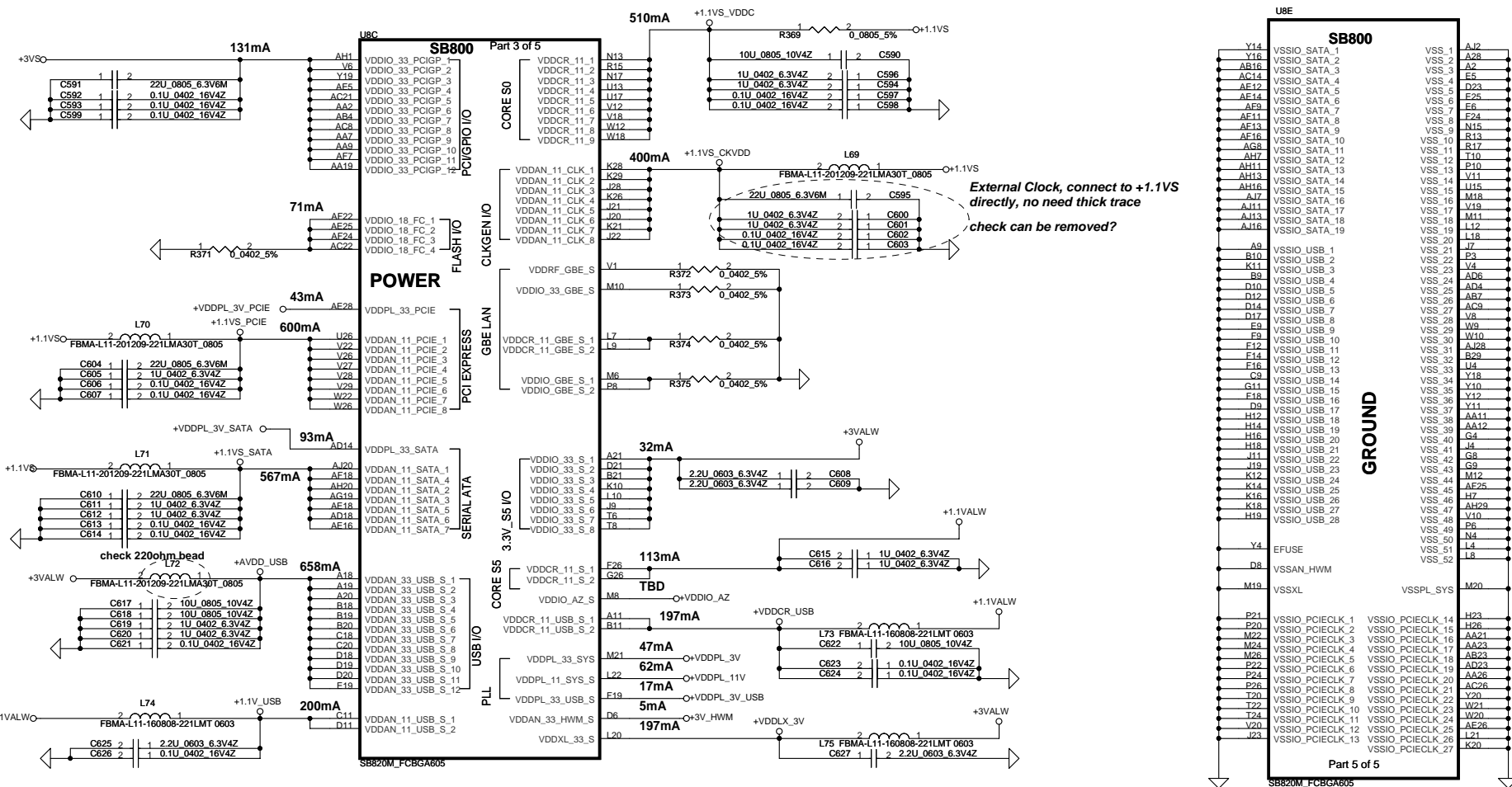
**ISL6265 PWROK input, TTL level: 0.8V-2.0V**  
 When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high



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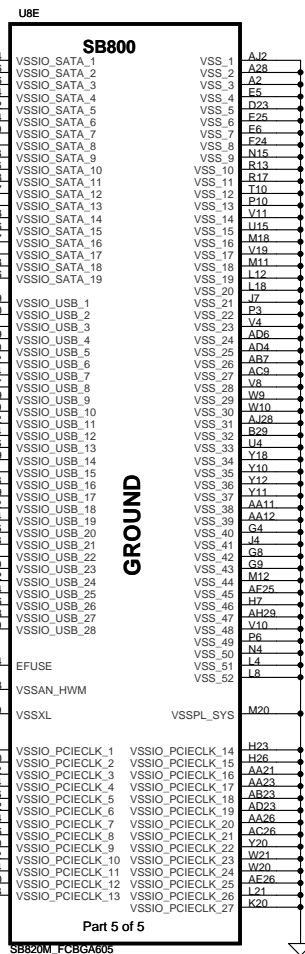






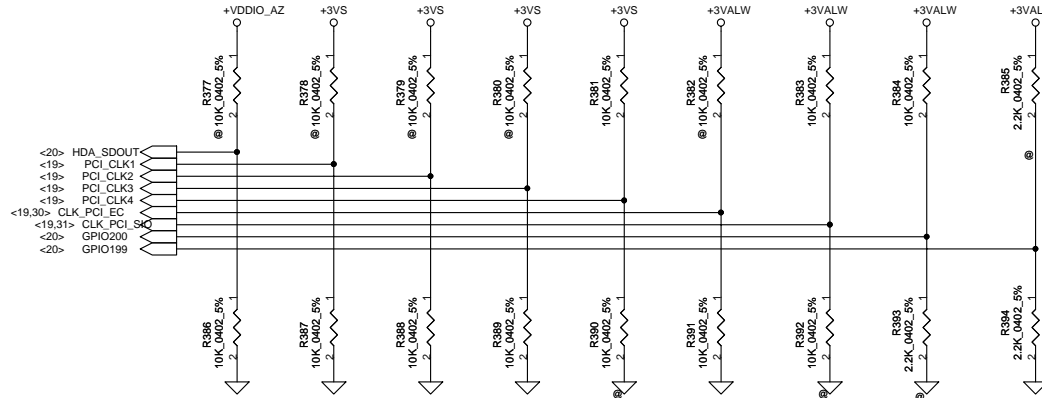
For 3V AZ device

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	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT		H,H = Reserved H,L = SPI ROM (Default)	
<b>PULL LOW</b>	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE		L,H = LPC ROM L,L = FWH ROM	



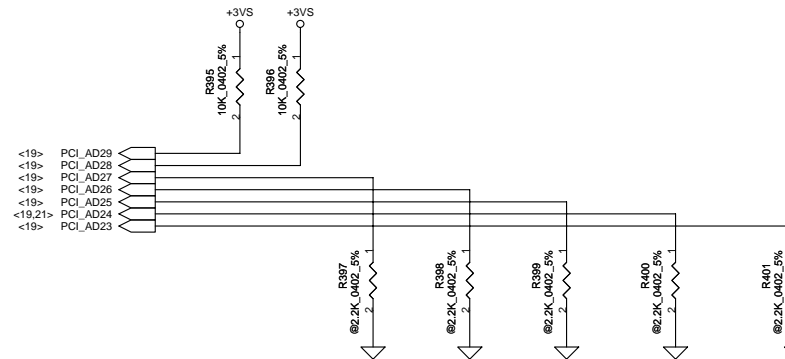
### DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

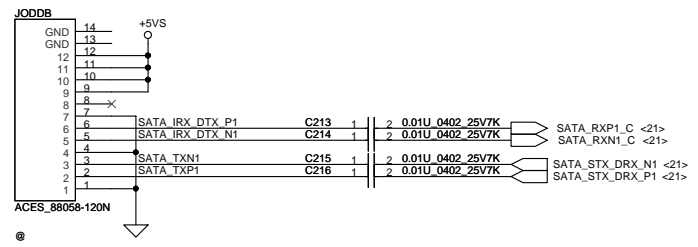
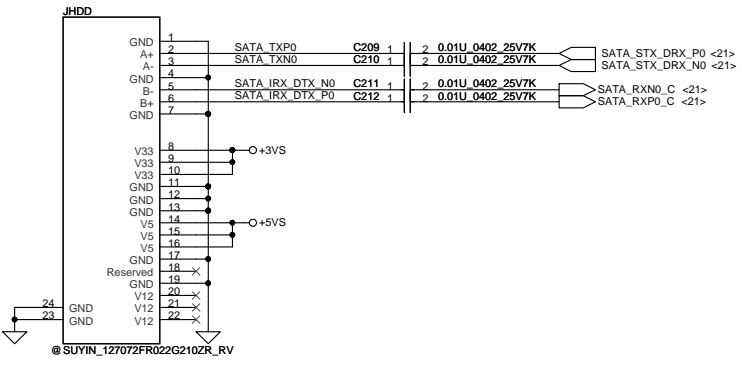
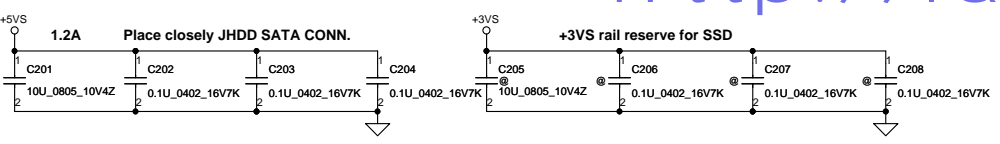
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

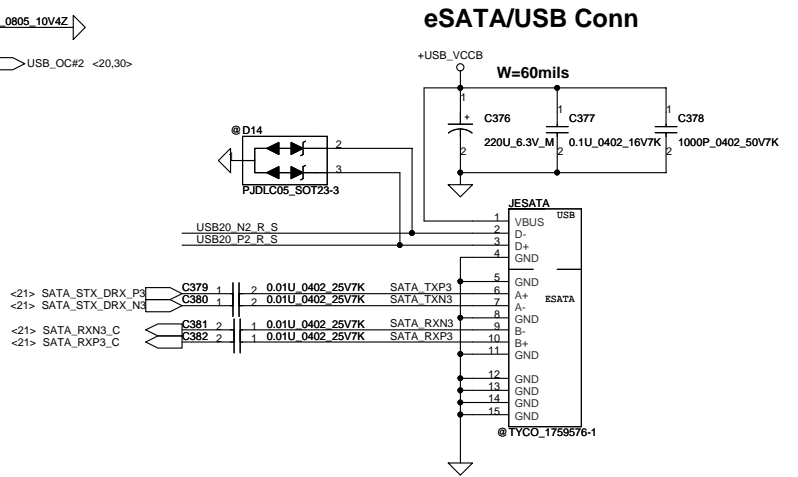
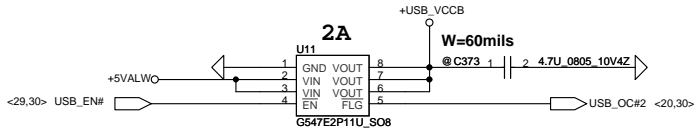
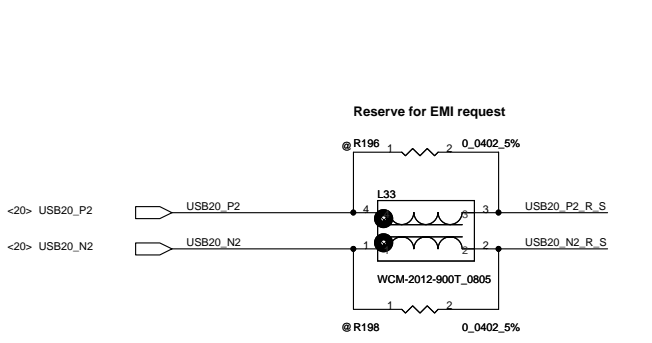
check default



< SATA HDD Conn >

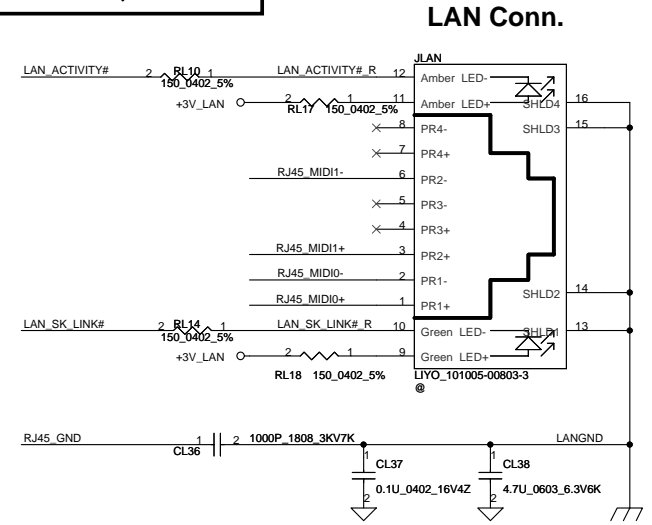
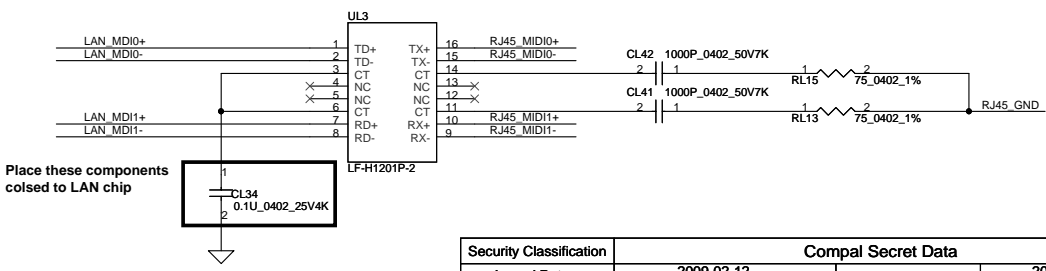
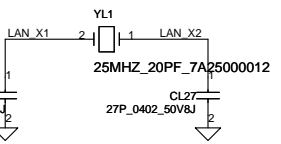
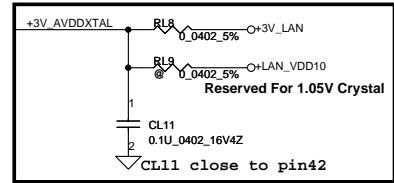
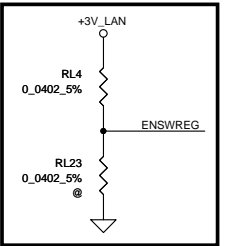
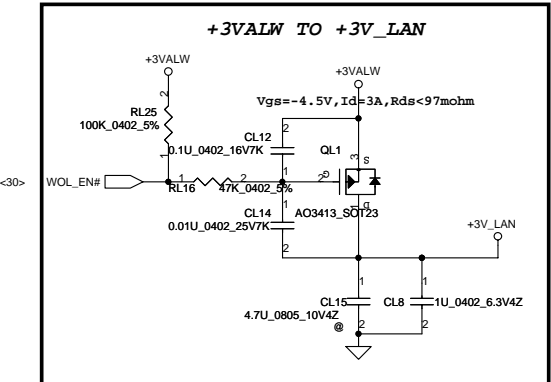
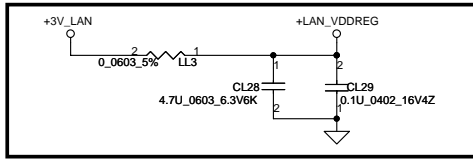
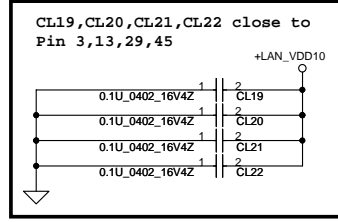
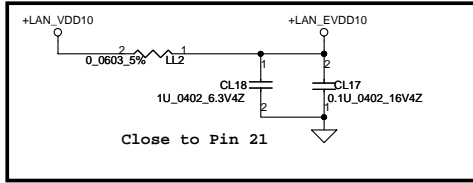
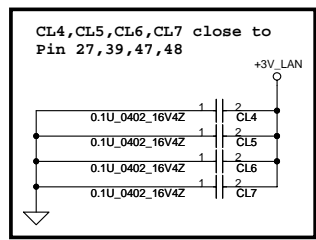
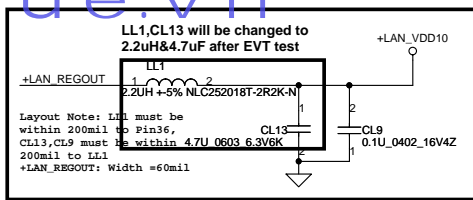
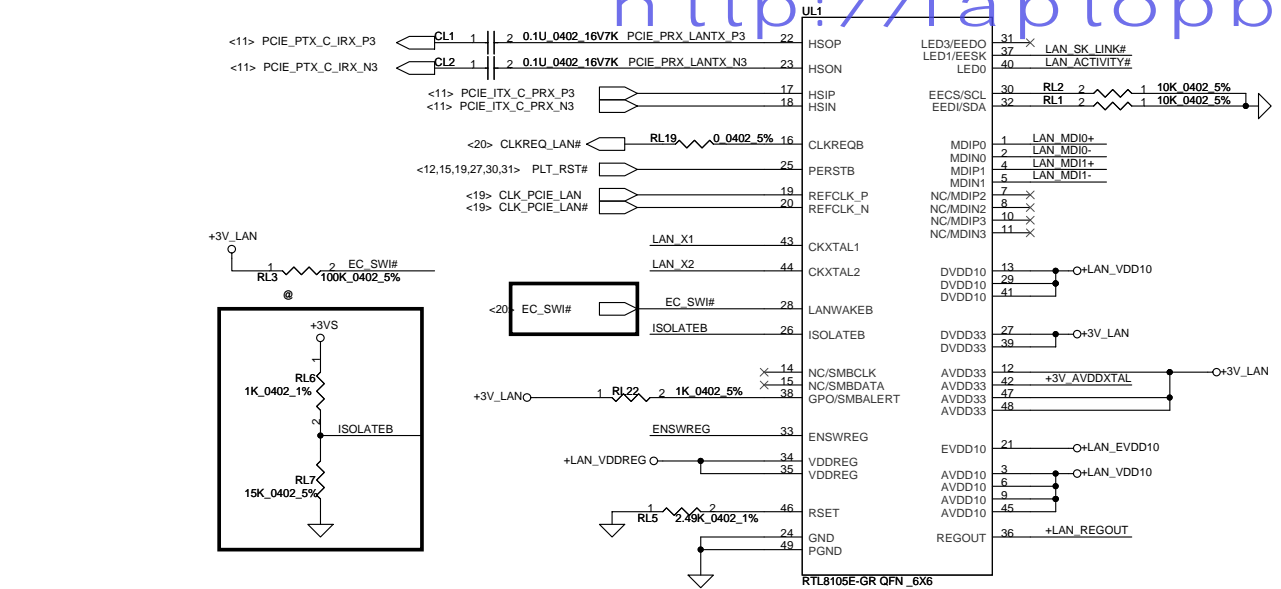


< eSATA/USB >

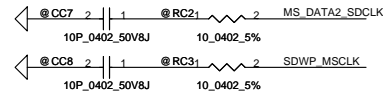
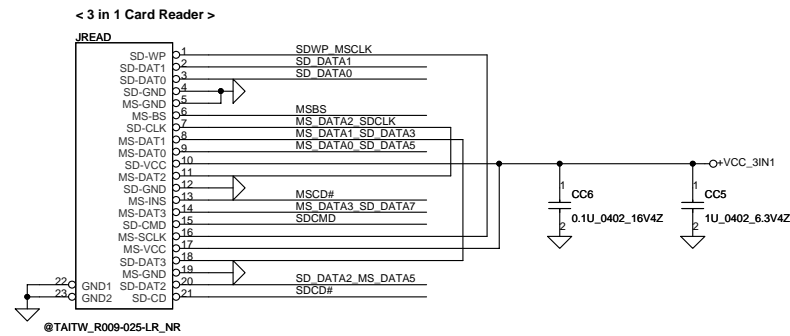
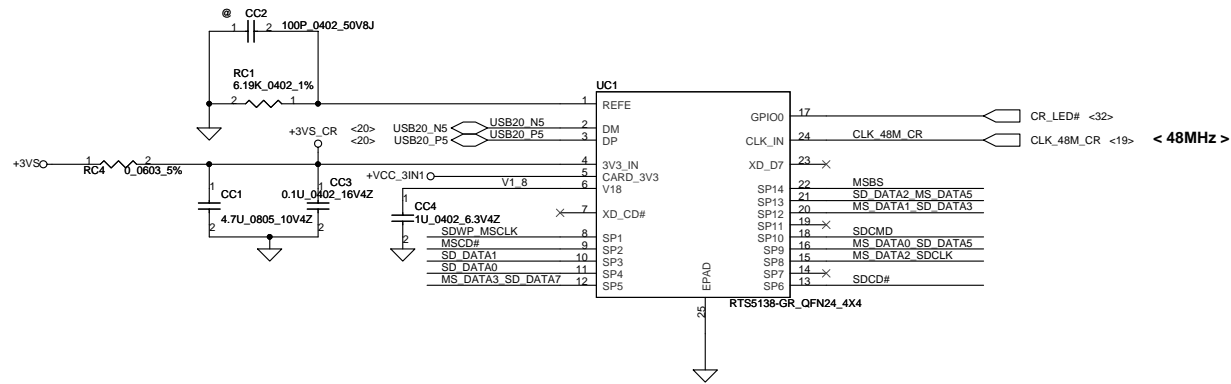


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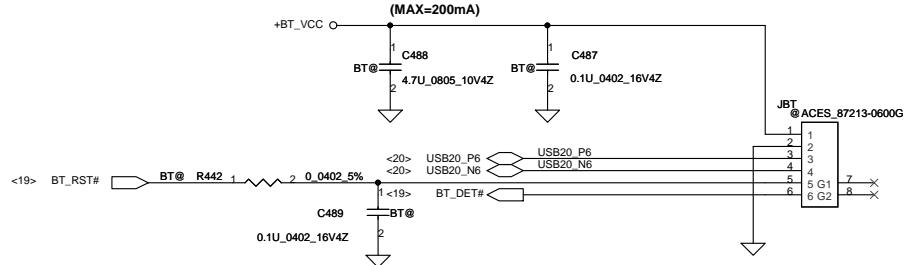
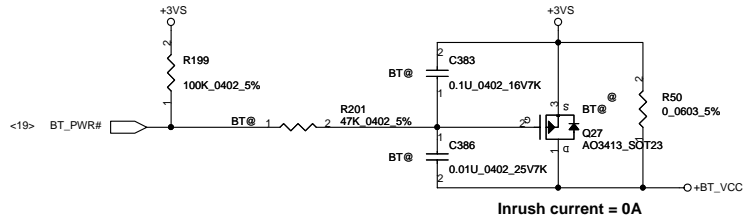
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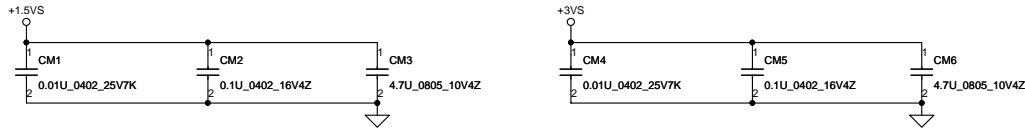
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< Bluetooth Interface, USB port6 >

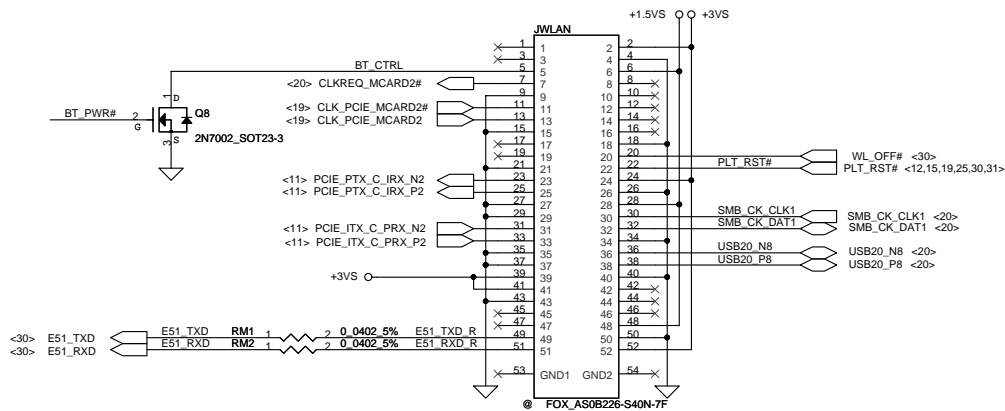
http://laptopblue.vn < Bluetooth Connector >



< PCIe Mini Card for WLAN >



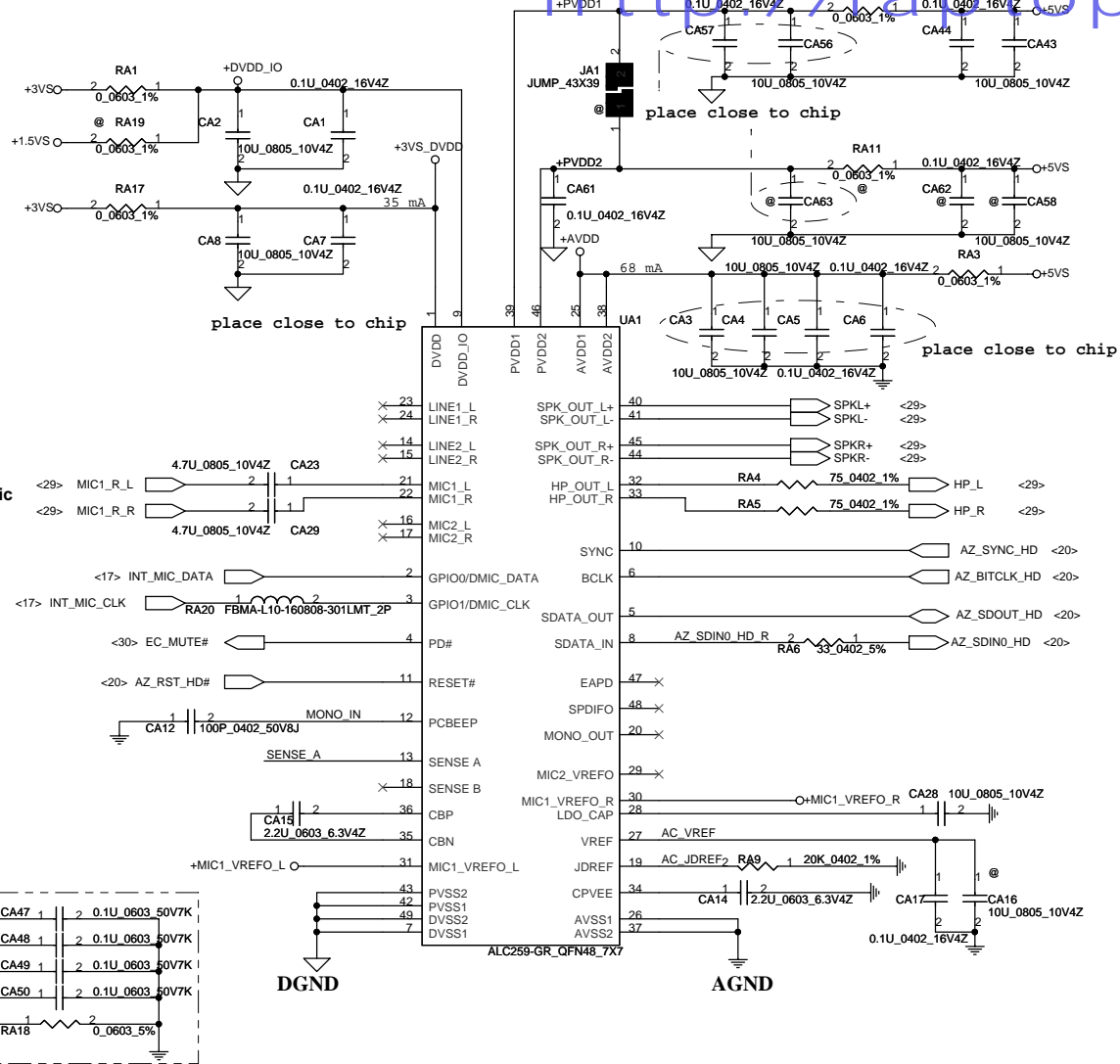
	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI



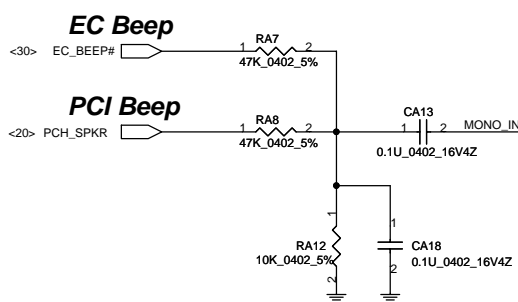
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Codec

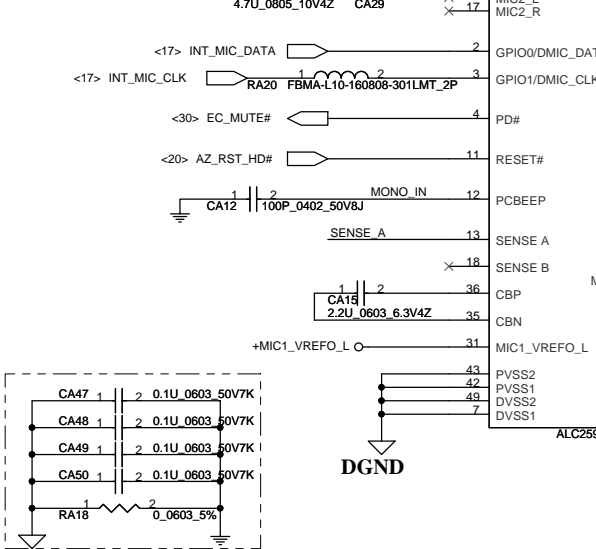
http://laptopblue.vn



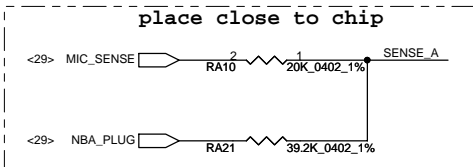
Beep sound



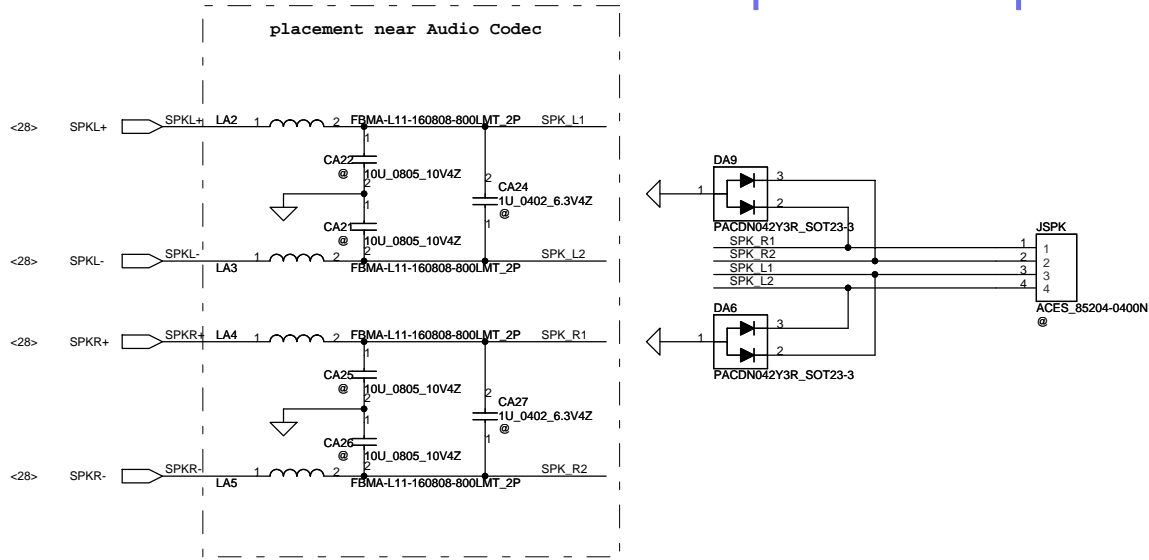
Ext. Mic



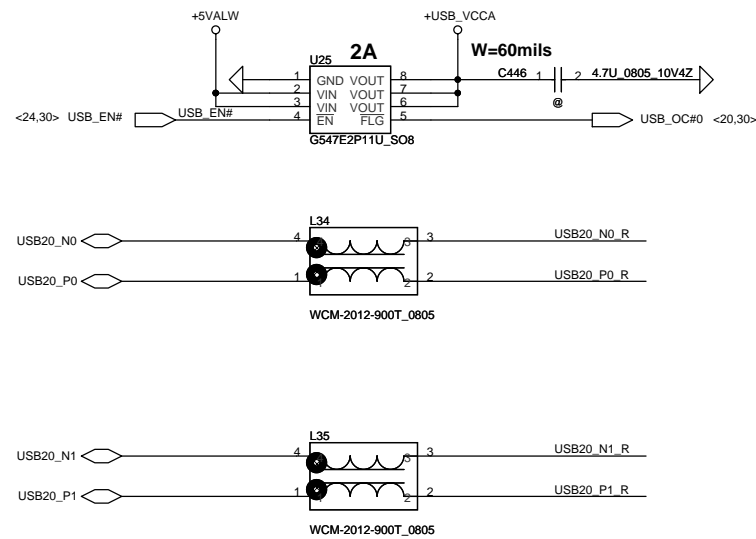
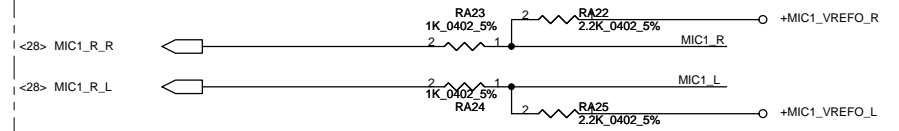
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



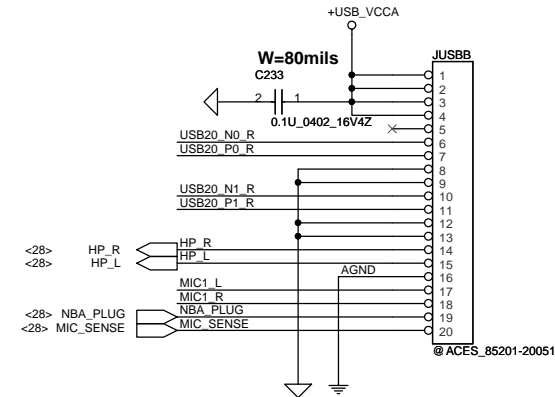
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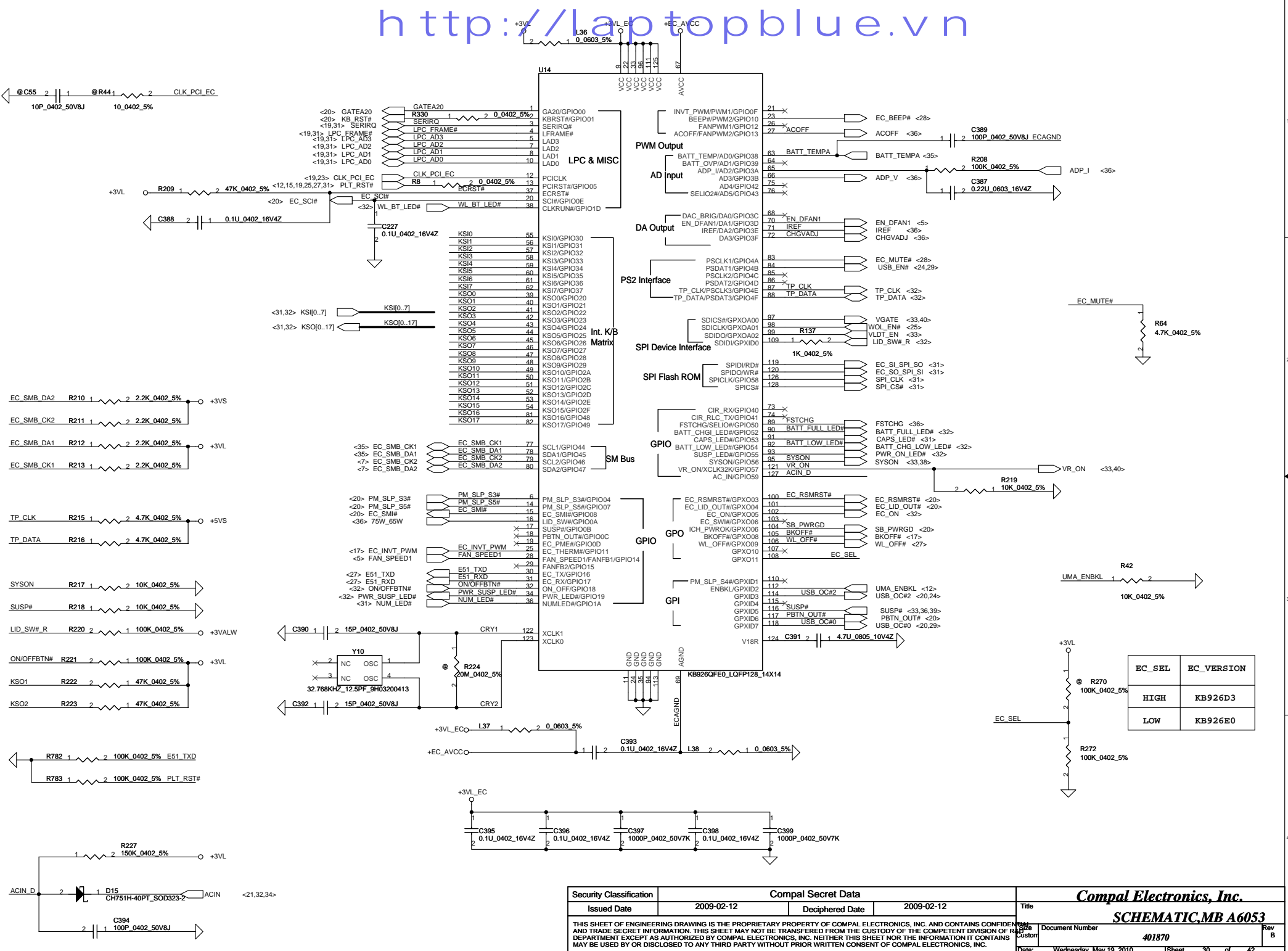
Ext.MIC/LINE IN JACK



Audio & USB Sub-Board Conn.

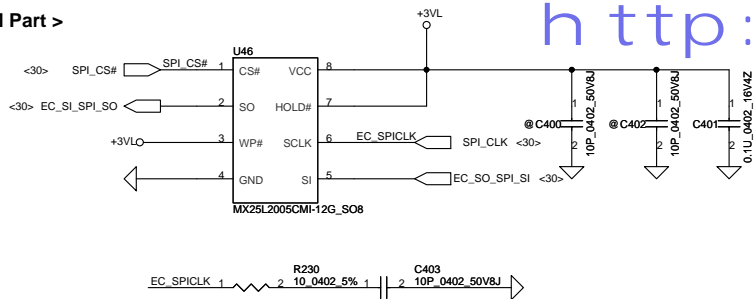


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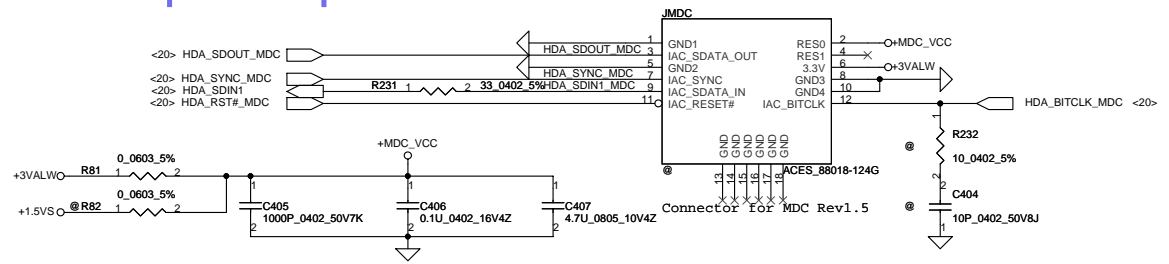


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< ROM Part >

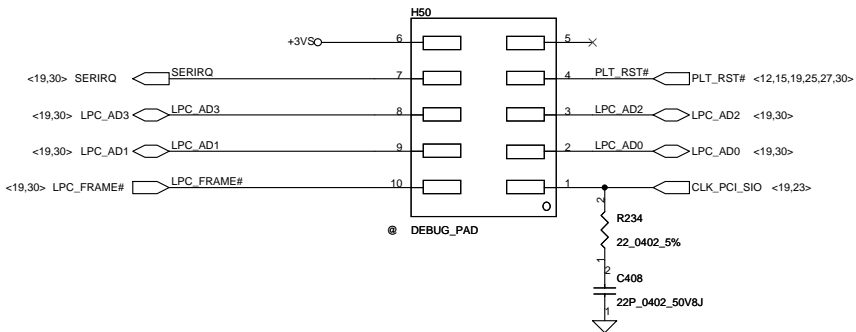


< MDC 1.5 Conn >



< LPC Debug Port >

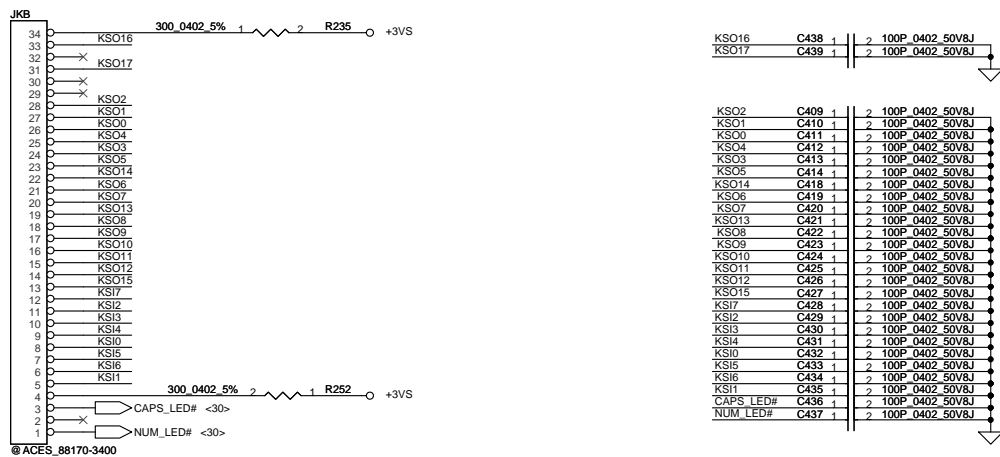
Please place the PAD under DDR DIMM.



< KEYBOARD Conn >

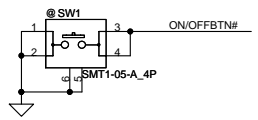


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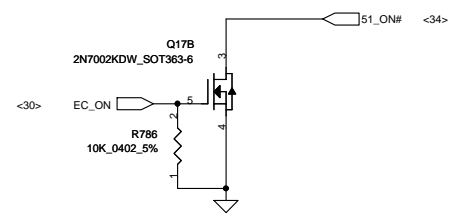


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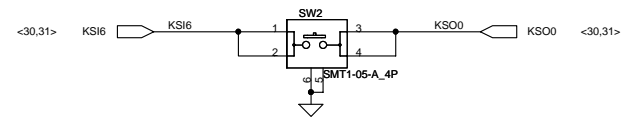
< Power Button for Debug >



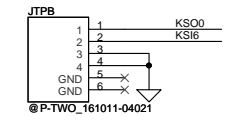
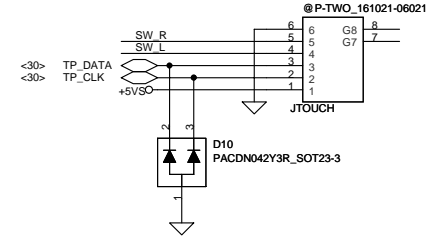
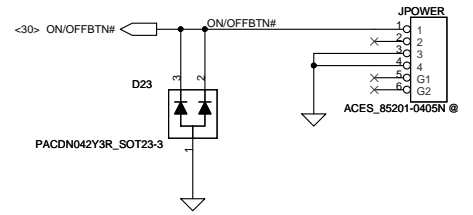
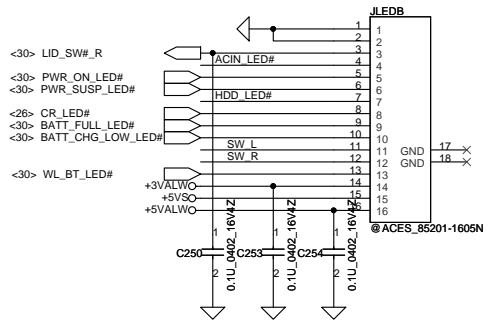
< Power Button Circuit >



< TP on & off BTN on M/B >

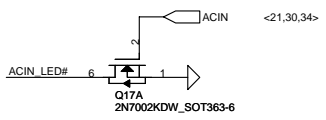


Sub-B Connector

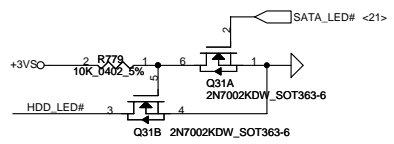


LED Circuit

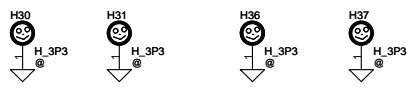
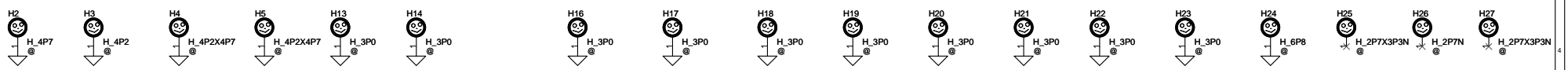
DC-IN LED



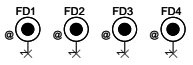
HDD LED



SCREW



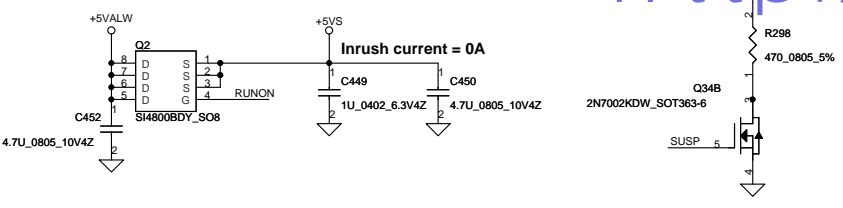
PCB Federal Mark PAD



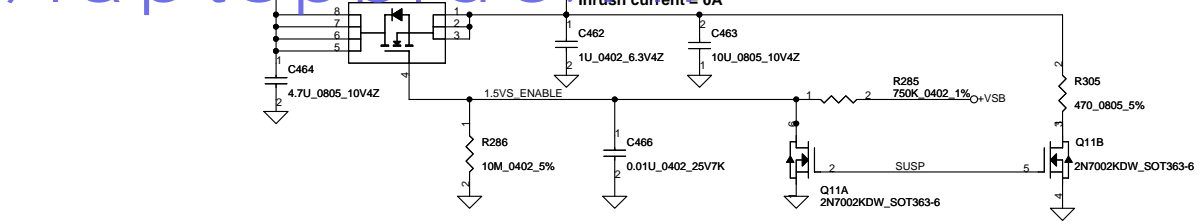
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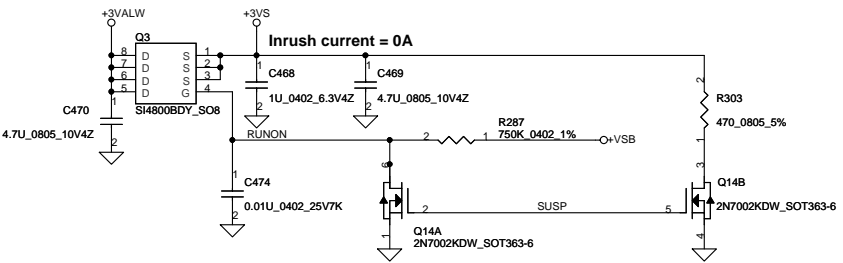
< +5VALW TO +5VS >



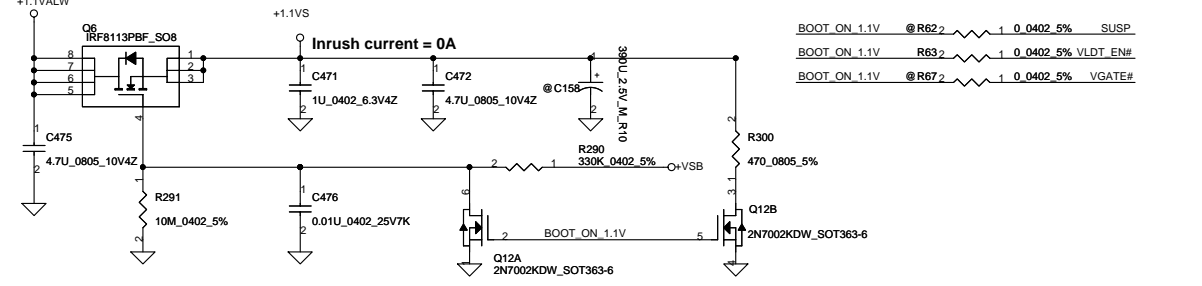
< +1.5V TO +1.5VS >



< +3VALW TO +3VS >

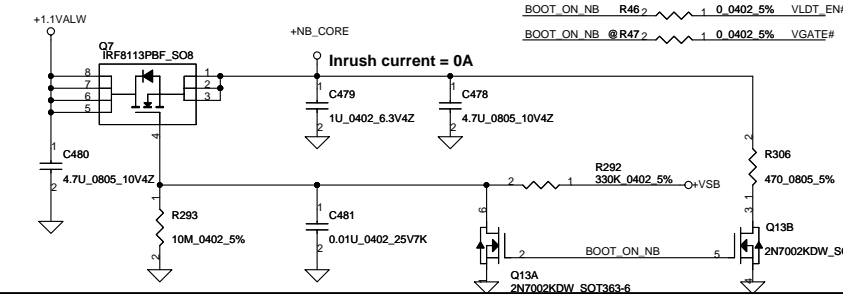


< +1.1VALW TO +1.1VS >



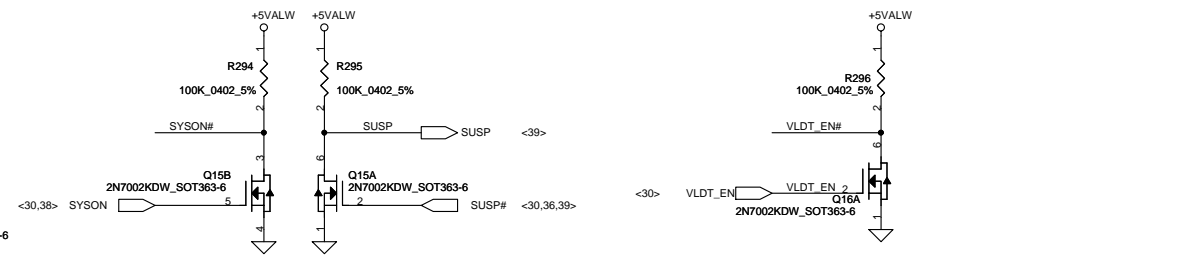
BOOT\_ON 1.1V @R62 1 0.0402 5% SUSP  
 BOOT\_ON 1.1V @R63 1 0.0402 5% VLDT\_EN#  
 BOOT\_ON 1.1V @R67 1 0.0402 5% VGATE#

< +1.1VALW TO +NB\_CORE >

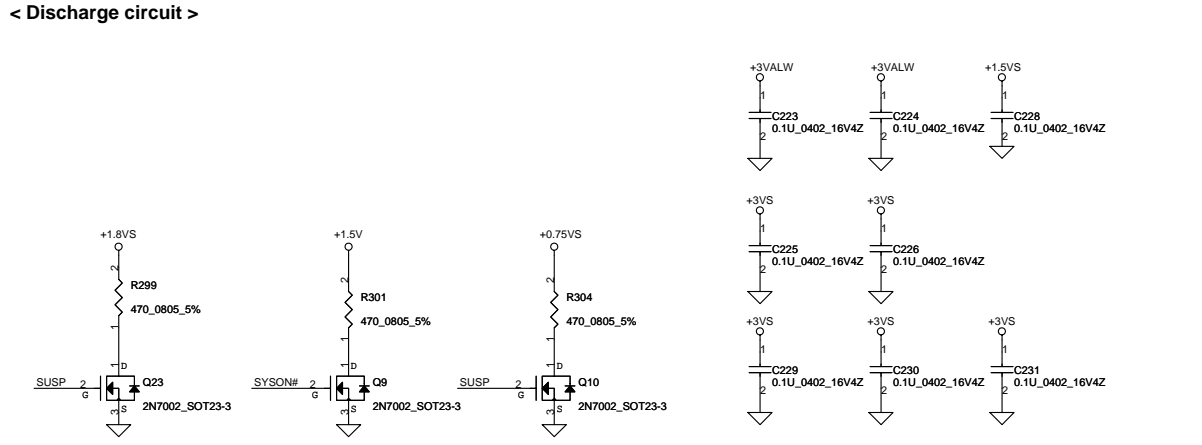
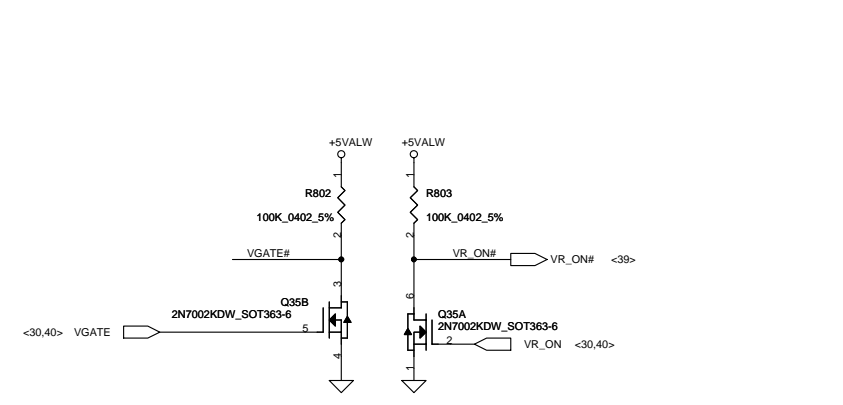


BOOT\_ON NB @R45 1 0.0402 5% SUSP  
 BOOT\_ON NB @R46 1 0.0402 5% VLDT\_EN#  
 BOOT\_ON NB @R47 1 0.0402 5% VGATE#

< Inversion of SYSON, SUSP#, VLDT\_EN, EC\_ON >

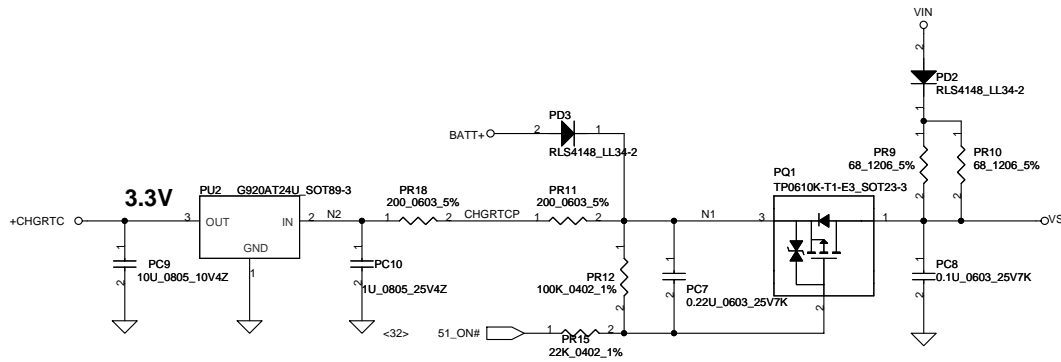
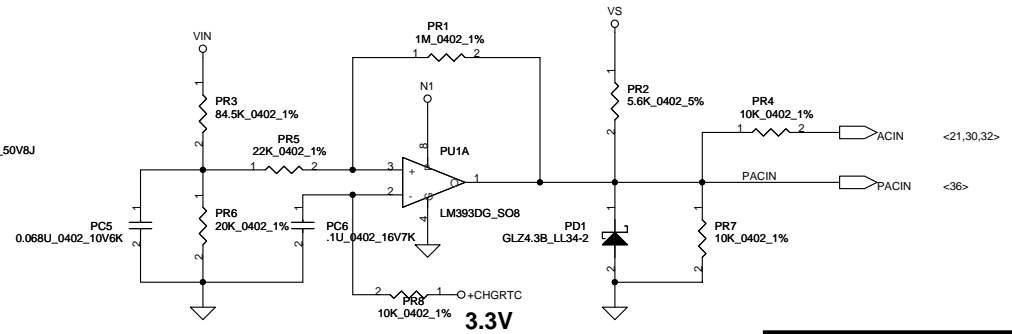
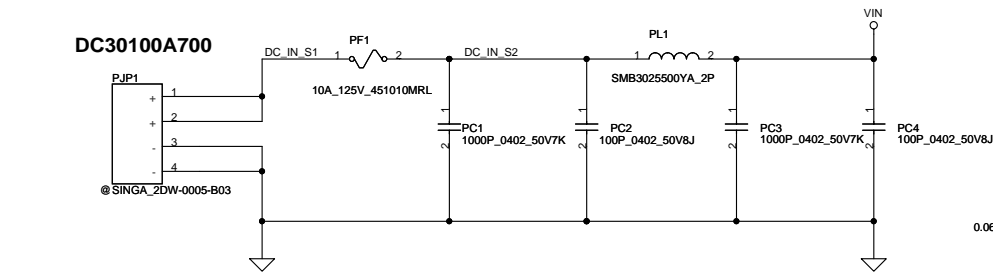


< Discharge circuit >



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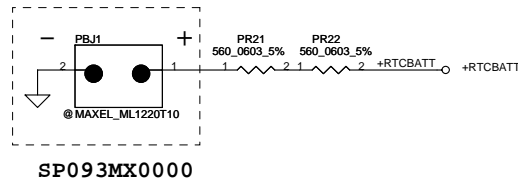
**DC30100A700**



**Vin Detector**

High	18.384	17.901	17.430
Low	17.728	17.257	16.976

**RTC Battery**



**PJ1**  
+3VALWP → 2 → 1 → +3VALW  
(5A, 200mils, Via NO. = 10)  
OCP(min) = 7.7A

**PJ2**  
+1.1VALWP → 2 → 1 → +1.1VALW  
(12A, 480mils, Via NO. = 24)  
OCP(min) = 18.7A

**PJ3**  
+3VLP → 2 → 1 → +3VL  
(100mA, 40mils, Via NO. = 2)

**PJ5**  
+5VALWP → 2 → 1 → +5VALW  
(5A, 200mils, Via NO. = 10)  
OCP(min) = 7.9A

**PJ7**  
+1.5VP → 2 → 1 → +1.5V  
(7.5A, 300mils, Via NO. = 15)  
OCP(min) = 8.7A

**PJ9**  
+2.5VSP → 2 → 1 → +2.5VS  
(1A, 40mils, Via NO. = 2)

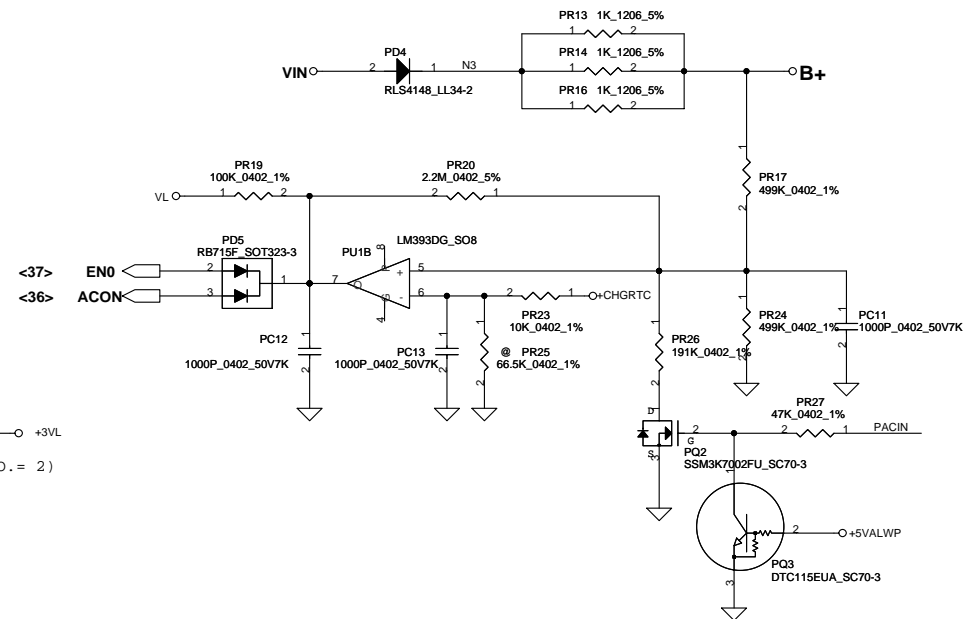
**PJ8**  
+VSBP → 2 → 1 → +VSB  
(120mA, 40mils, Via NO. = 1)

**PJ10**  
+1.8VSP → 2 → 1 → +1.8VS  
(1A, 40mils, Via NO. = 2)

**PJ12**  
+VDDNBP → 2 → 1 → +VDDNB  
(4A, 160mils, Via NO. = 8)

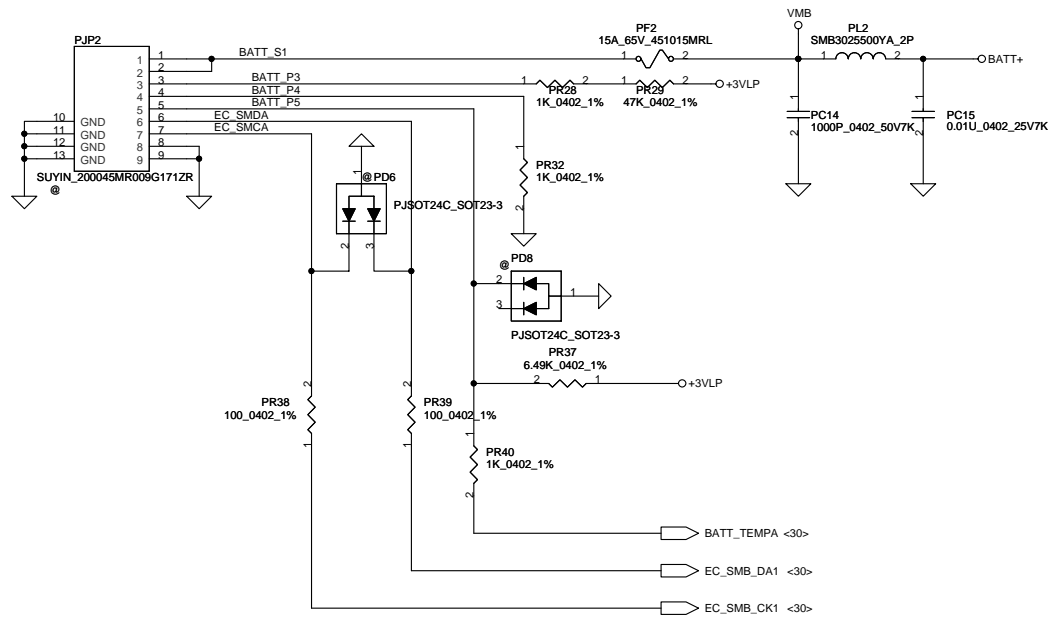
**PJ11**  
+0.75VSP → 2 → 1 → +0.75VS  
(1A, 40mils, Via NO. = 2)

**PJ13**  
+1.05VSP → 2 → 1 → +1.05VS  
(1.5A, 60mils, Via NO. = 3)



**Precharge detector**  
**15.97V/14.84V FOR ADAPTOR**

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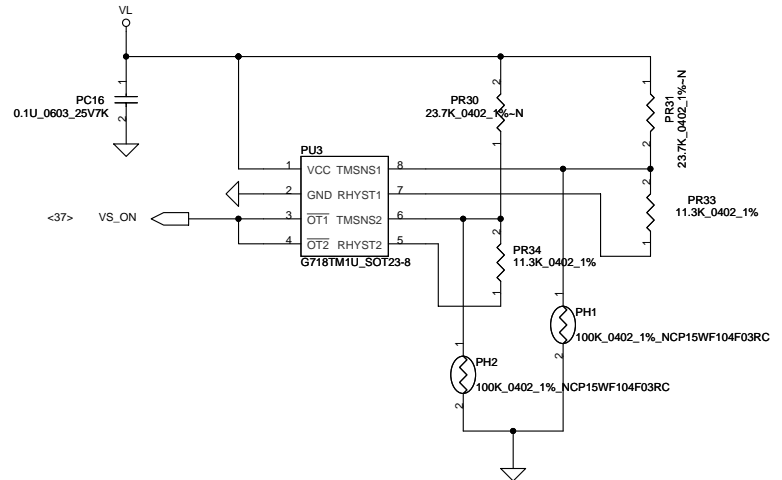


**PH1 under CPU bottom side :**  
 CPU thermal protection at 90 degree C  
 Recovery at 56 degree C

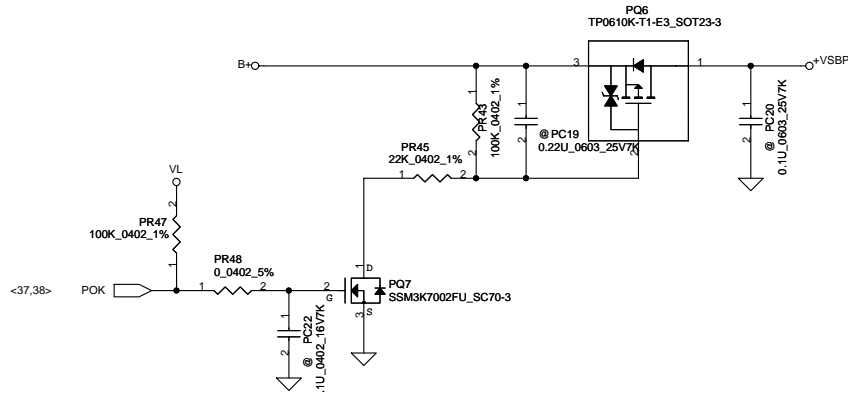
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

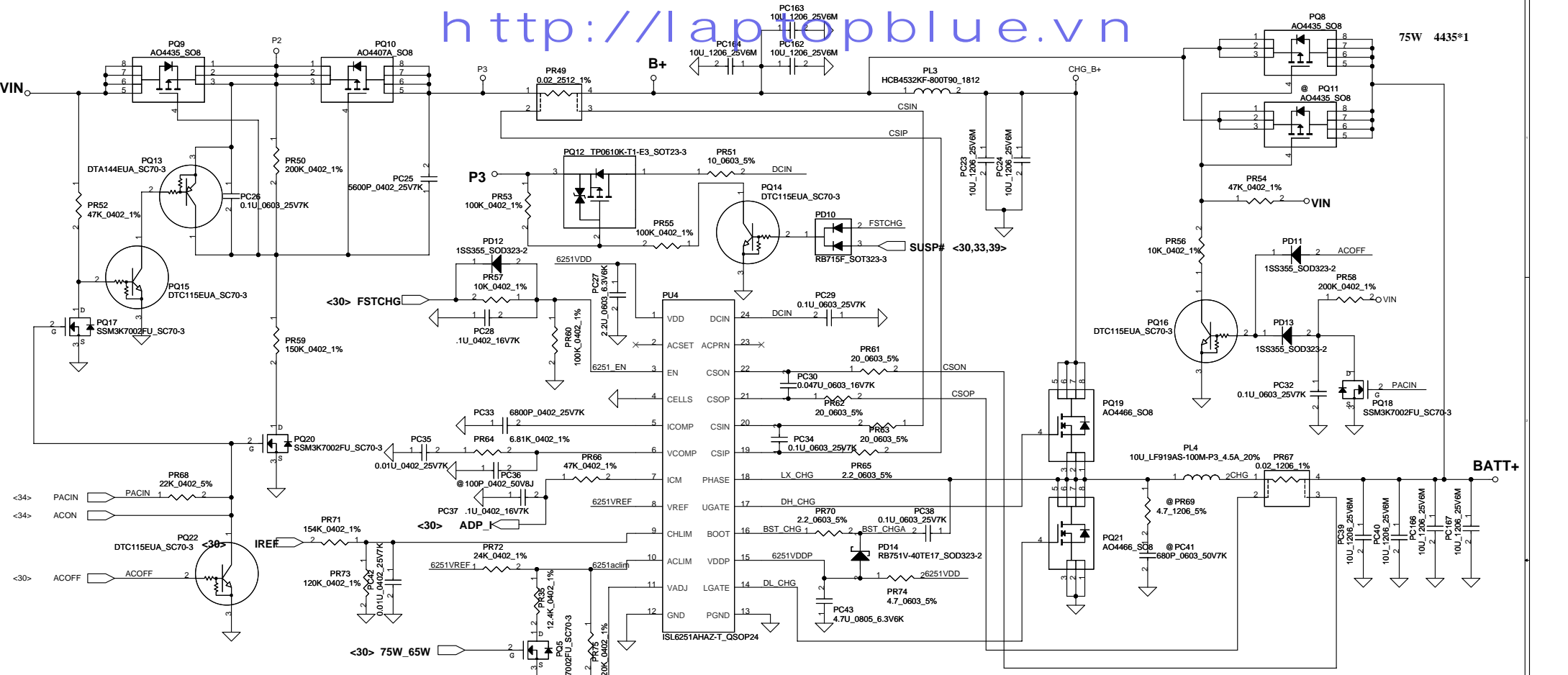
$R_{tmh}$  at 90C = 7.87K,  $R_{tml}$  at 56C = 26.1K  
 $R_{set} = 3 * 7.87K = 23.61K \implies 23.7K$   
 $R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \implies 11.3K$



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 90 degree C  
 Recovery at 56 degree C



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CP mode  
 $V_{aclim} = 2.39 * (R_b // 152K) / (R_t // 152K + R_b // 152K)$   
 $I_{input} = (1/PR49) * ((0.05 * V_{aclim}) / (2.39 + 0.05))$   
 where  $V_{aclim} = 0.6221V$ ,  $I_{input} = 3.15A$   
 $V_{aclim} = 1.09986V$ ,  $I_{input} = 3.65A$   
 $V_{aclim} = 0.7717V$ ,  $I_{input} = 4.41A$   
 $V_{aclim} = 0.4204V$ ,  $I_{input} = 5.88A$

CC=0.25A-3.6A  
 IREF=0.9133\*Icharge  
 IREF=0.228V-3.29V  
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.315V

(75W)  $I_{in} = 2.512 ADP\_I$   
 (120W)  $I_{in} = 3.35 ADP\_I$   
 $V_{in} = 7.57 ADP\_V$

$I_{ada} = 0-3.421A(65W)$  CP=3.15A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W\_65W=high  
 $I_{ada} = 0-3.947A(75W)$  CP=3.63A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W\_65W=low  
 $I_{ada} = 0-4.737A(90W)$  CP=4.36A PR49=0.015, PR72=53.6k, PR75=20k, PR35=unpop, PQ5=unpop  
 $I_{ada} = 0-6.316A(120W)$  CP=5.81A PR49=0.015, PR72=8.25k, PR75=26.7k, PR35=unpop, PQ5=unpop  
 CP= 92%\*Iada

CELLS	VDD	GND	Float
CELL number	4	3	2

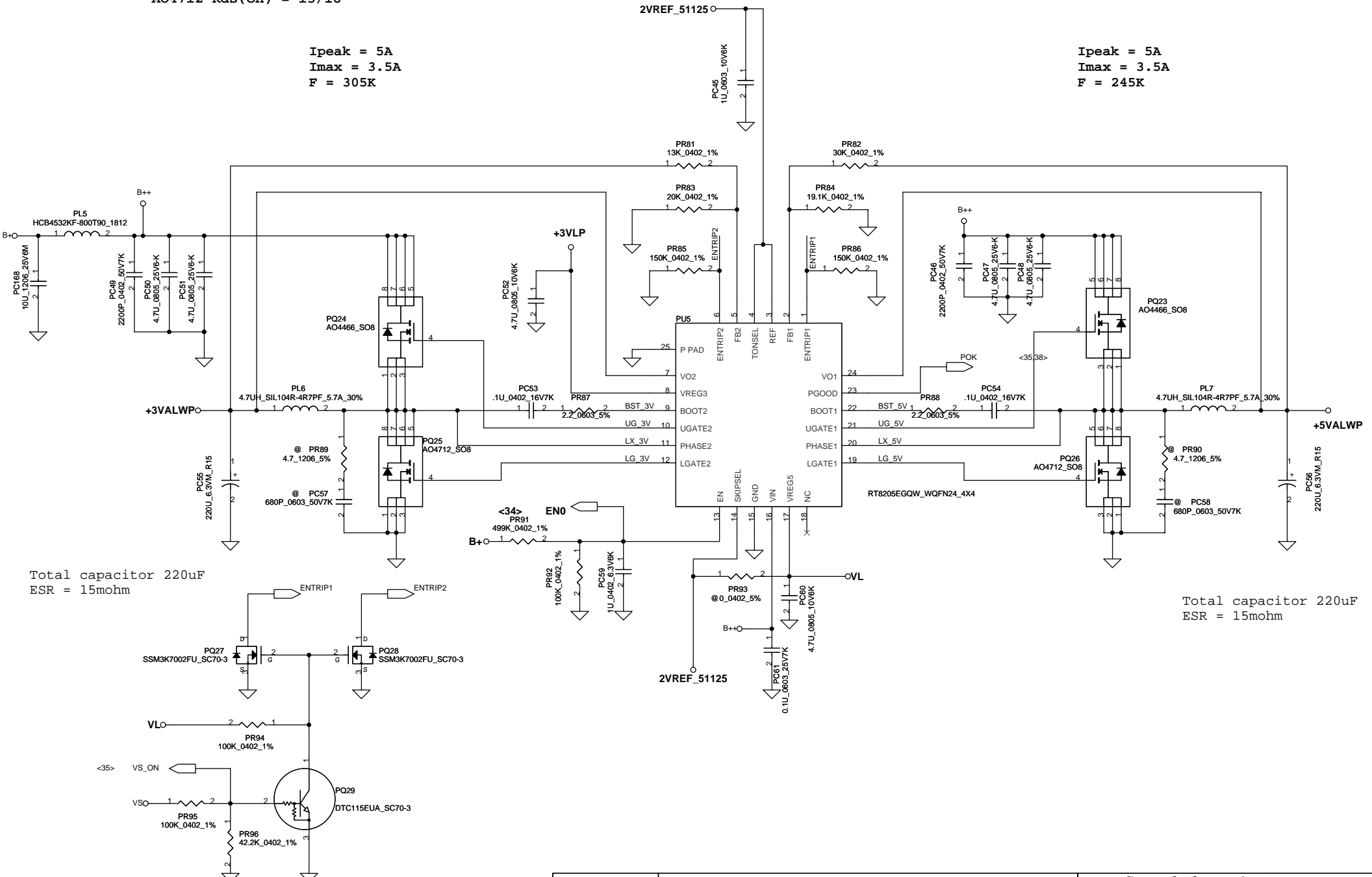
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AO4712 Rds(on) = 15/18

Ipeak = 5A  
 Imax = 3.5A  
 F = 305K

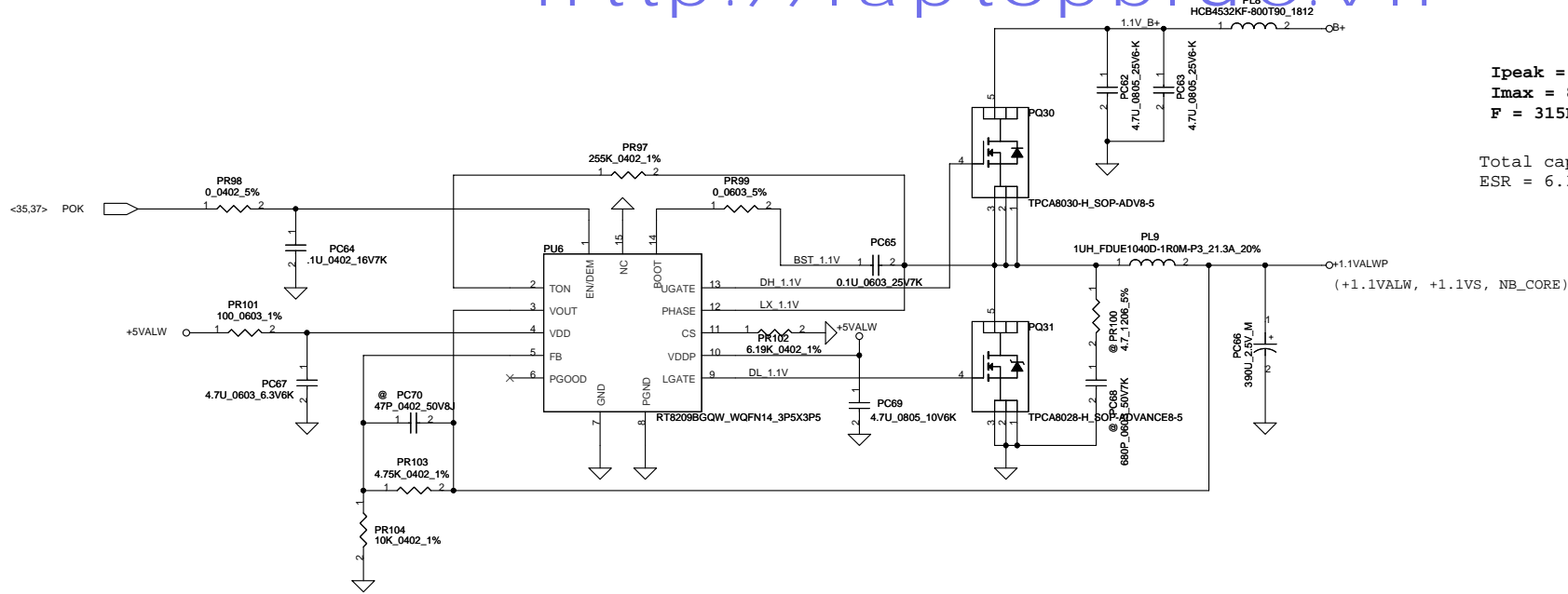
Ipeak = 5A  
 Imax = 3.5A  
 F = 245K



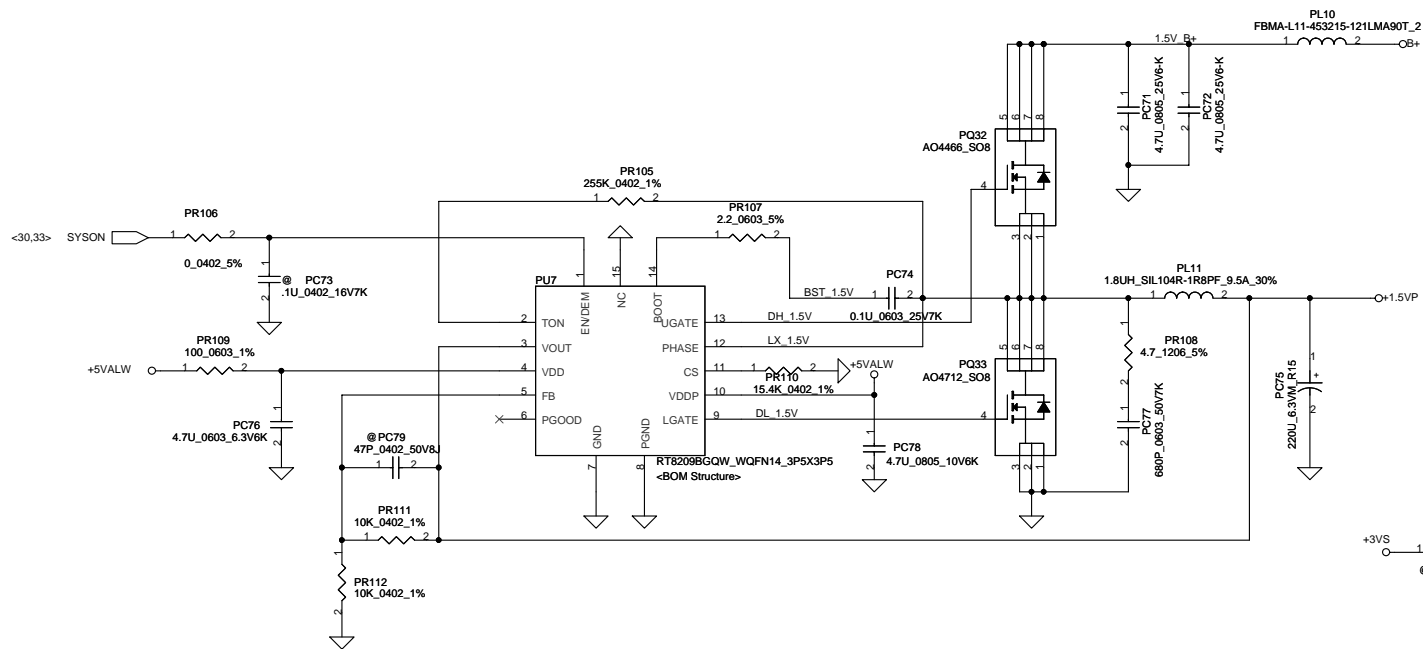
Total capacitor 220uF  
 ESR = 15mohm

Total capacitor 220uF  
 ESR = 15mohm

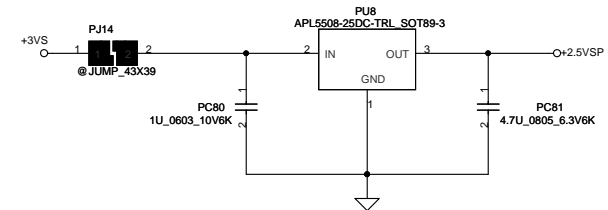
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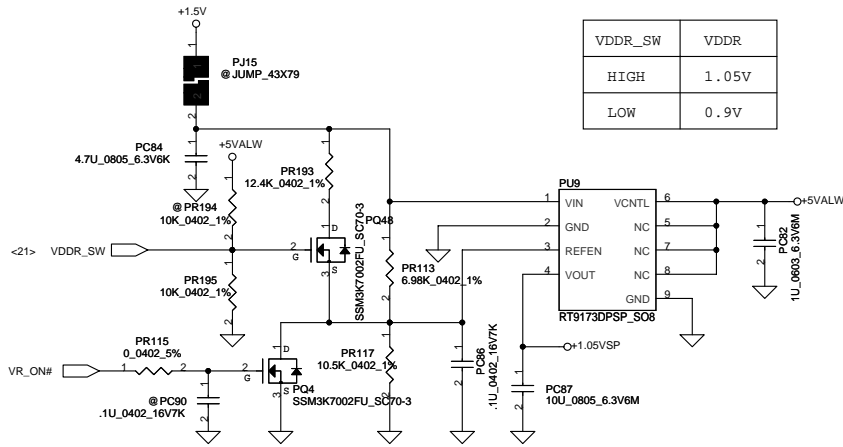
Ipeak = 12A  
 Imax = 8.4A  
 F = 315K  
 Total capacitor 720uF  
 ESR = 6.3mohm



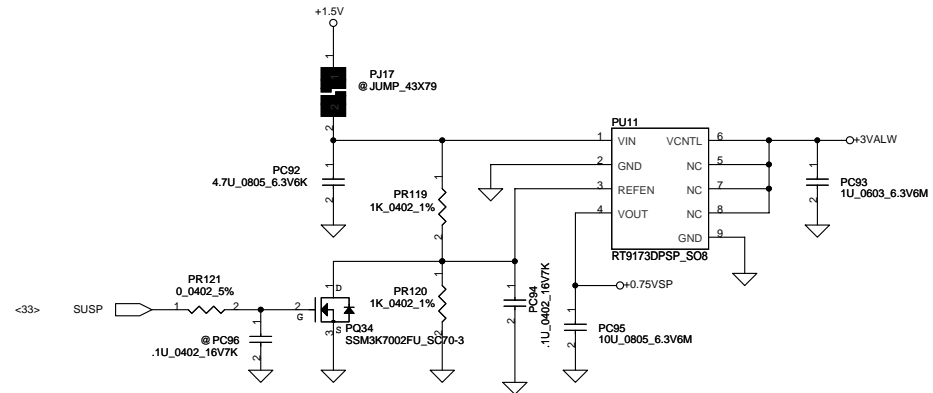
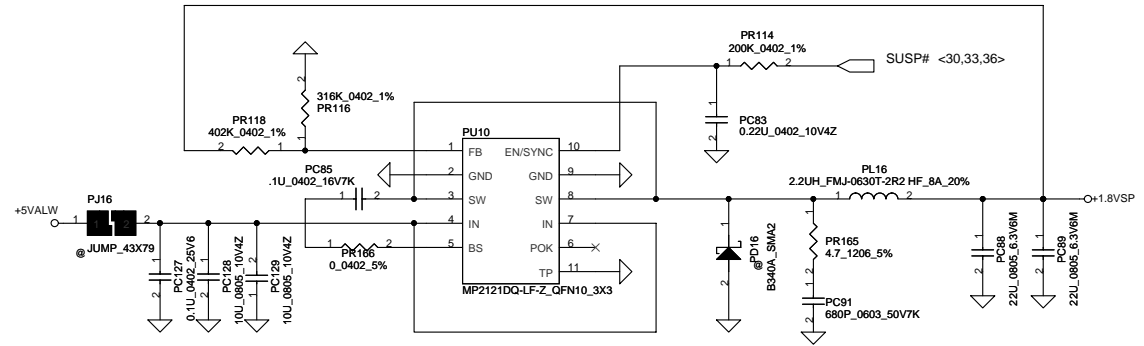
Ipeak = 7.5A  
 Imax = 5.25A  
 F = 315K  
 Total capacitor 610uF  
 ESR = 6mohm



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VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V



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**PIR (Product Improve Record)**  
**NALAE LA-6053P SCHEMATIC CHANGE LIST**  
**REVISION CHANGE: 0.1 TO 0.2**

NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	33	Change JLEDB pin define as customer request
2	2009/12/14	25,28,30	Delete JODDB, JBT and JUSBB support pin
3	2009/12/14	33	Change JPOWER Pin2 from GND to NC
4	2009/12/15	28	Add R95 at WLAN Pin5 for BT/WLAN combo Mini Card
5	2009/12/15	25,30	Change U11, U25 P/N from SA00002XX00 to SA000033H00
6	2009/12/15	28	Reverse JBT pin definition
7	2009/12/16	27	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @
8	2009/12/17	33	Cgange JPOWER footprint to ACES_87151-1207_12P (ZIF_上接點)
9	2009/12/17	33	Cgange JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition
10	2009/12/17	33	Cgange JLEDB footprint to ACES_85201-1205N_12P (ZIF_上接點)
11	2009/12/17	25	Cgange JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)
12	2009/12/17	33	Change H36, H37 footprint from H_3P3 to H_3P8

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# Version Change List (P. I. R. List) for Power Circuit

http://laptopblue.vn

Page#	Item Title	Solution Description
DVT : modification from EVT		
P38	change voltage divider to less than 10K	change PR104, PR111, PR112 to 10K; PR103 to 4.75K
P38	change OCP value	change PR102 to 6.19K
P39	enlarge output cap	change PC88, PC89 to 22uF(SH000000110)
P40	don't use NIPPON cap	change PC98, PC99 to SF000000080
P40	pull high RTN1 1.5V	change PR150 to mount
P38	EMI request	change PL10 to SM010000D700; change PR107 to 2.2ohm; add PR108 4.7ohm; add PC77 680pF
P40	EMI request	change PR137, PR149 to 2.2ohm; add PR139, PR1514.7ohm; add PC111, PC117 680pF
P37	choke need to meet thermal module height	change PL6, PL7 to SH000006380
P37	EMI request	change PR87, PR88 to 2.2ohm
P40	production line request	change PC98, PC99 to 68uF; add PC160, PC161 68uF
P36	EMI request for ISN issue	add PC162, PC163, PC164 10uF 1206
P39	mount snubber circuit	mount PR165, PC91
P35	OTP setting common	change PR30 and PR31 to 19.6K; PR34 to 7.87K; PR33 to 8.66K
P39	change IC to low cost	change P09 and P11 to RT9173
P39	change VDER(1.05V) circuit to switchable	add PR193, PR194, PR195 & PQ48
PVT : modification from DVT		
P40	cost down	change PC98, PC99, PC160, PC161 to SF000000W00
P37	common circuit	change PC45 to 1uF
P37	common circuit	mount PC59
P37	change PQ29 solution	change PQ29 to DTC1158UA
P36	add 65W/75W selection circuit	Add PR35 and PQ5
P38	prevent OVP for HW's cost down	change PC66 to 390uF
P36	EMI request for ISN issue	Add PC166, PC167, 10uF 1206
P37	EMI request for ISN issue	Add PC168, 10uF 1206
P40	EMI request	mount snubber circuit PR125, PC106
P38	EMI request for ESD issue	mount PC64 0.1uF
PreMP : modification from PVT		
P35	Thermal request change OTP	change PR30, PR31 to 23.7K; PR33, PR34 to 11.3K
P36	modify 65W/75W resistor	change PR35 to 12.4K
P34	modify RTC circuit	

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/5/18	Deciphered Date	2008/5/18	Title
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