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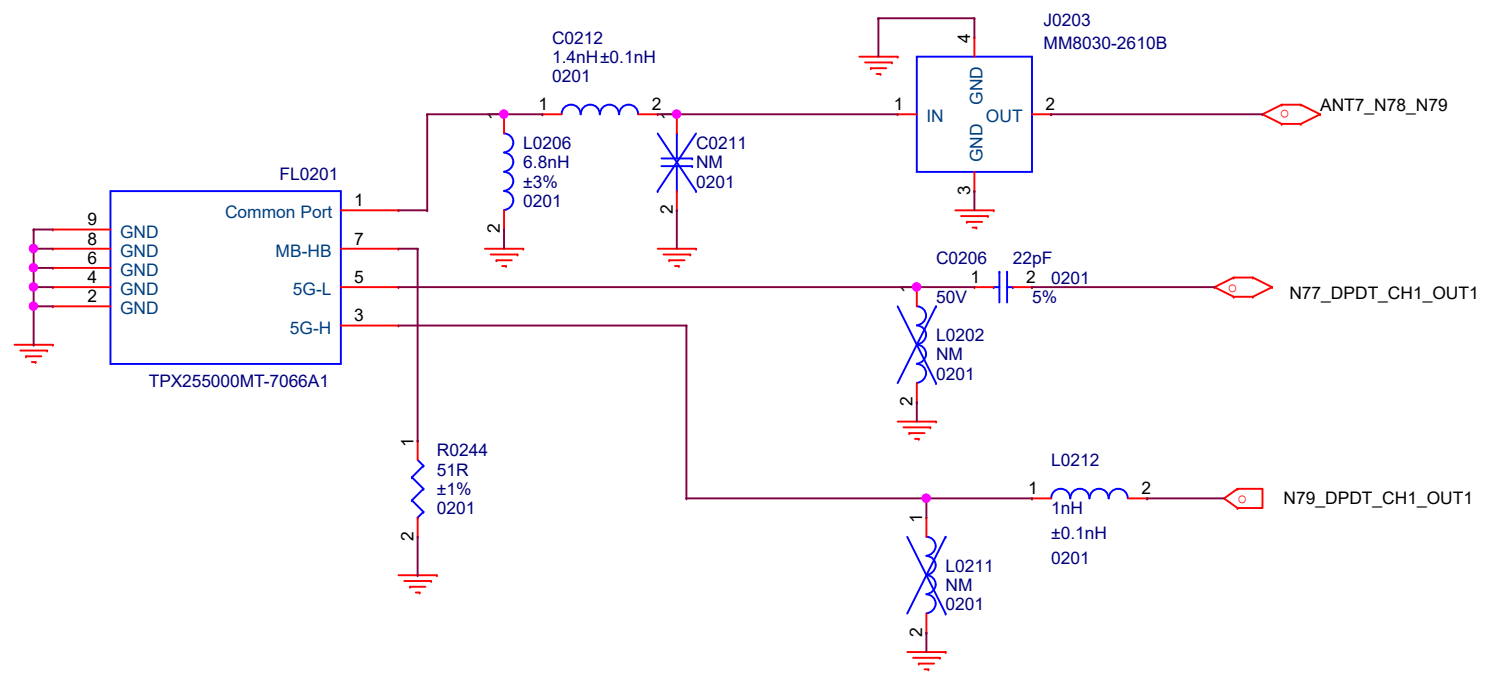
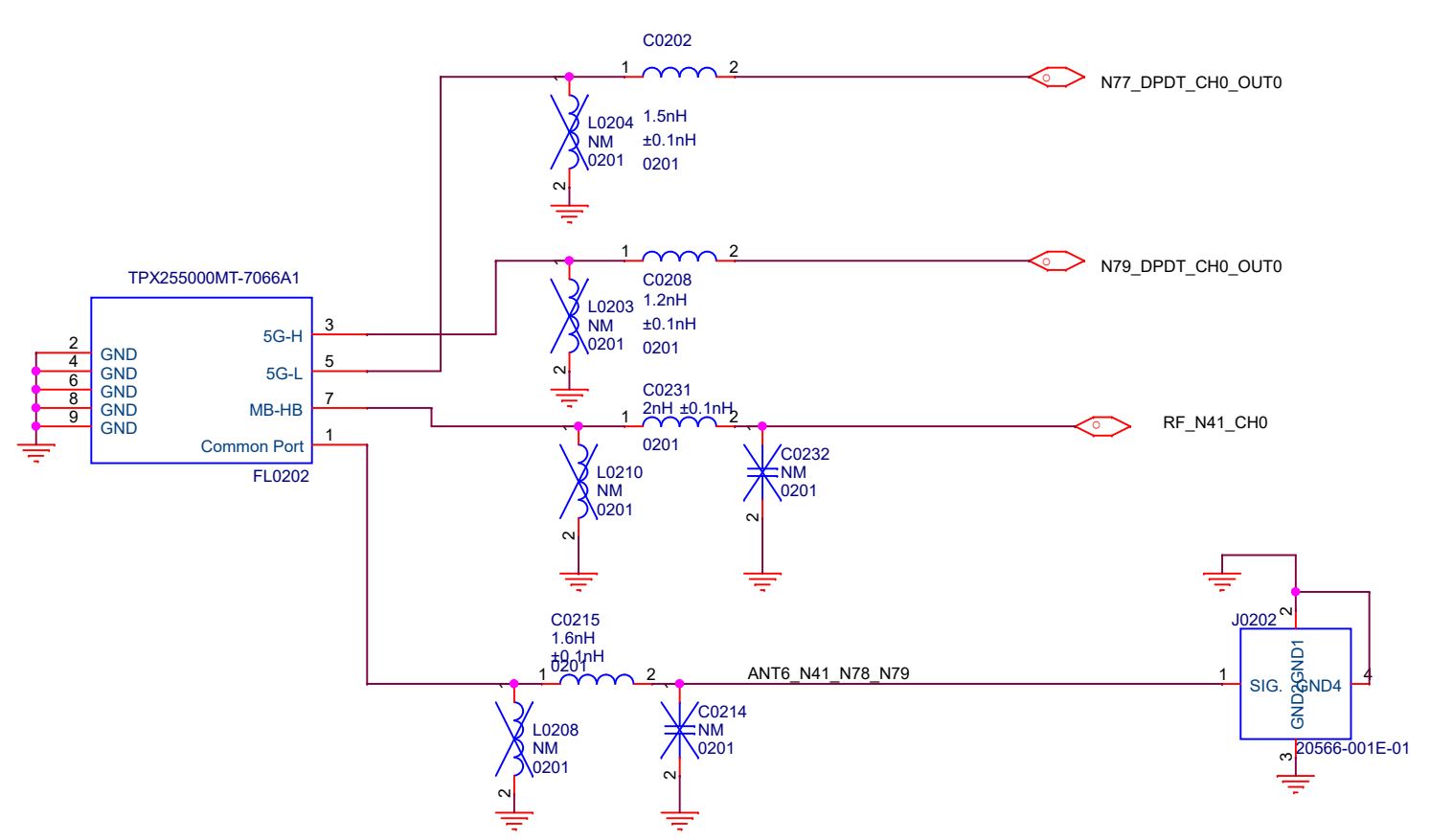
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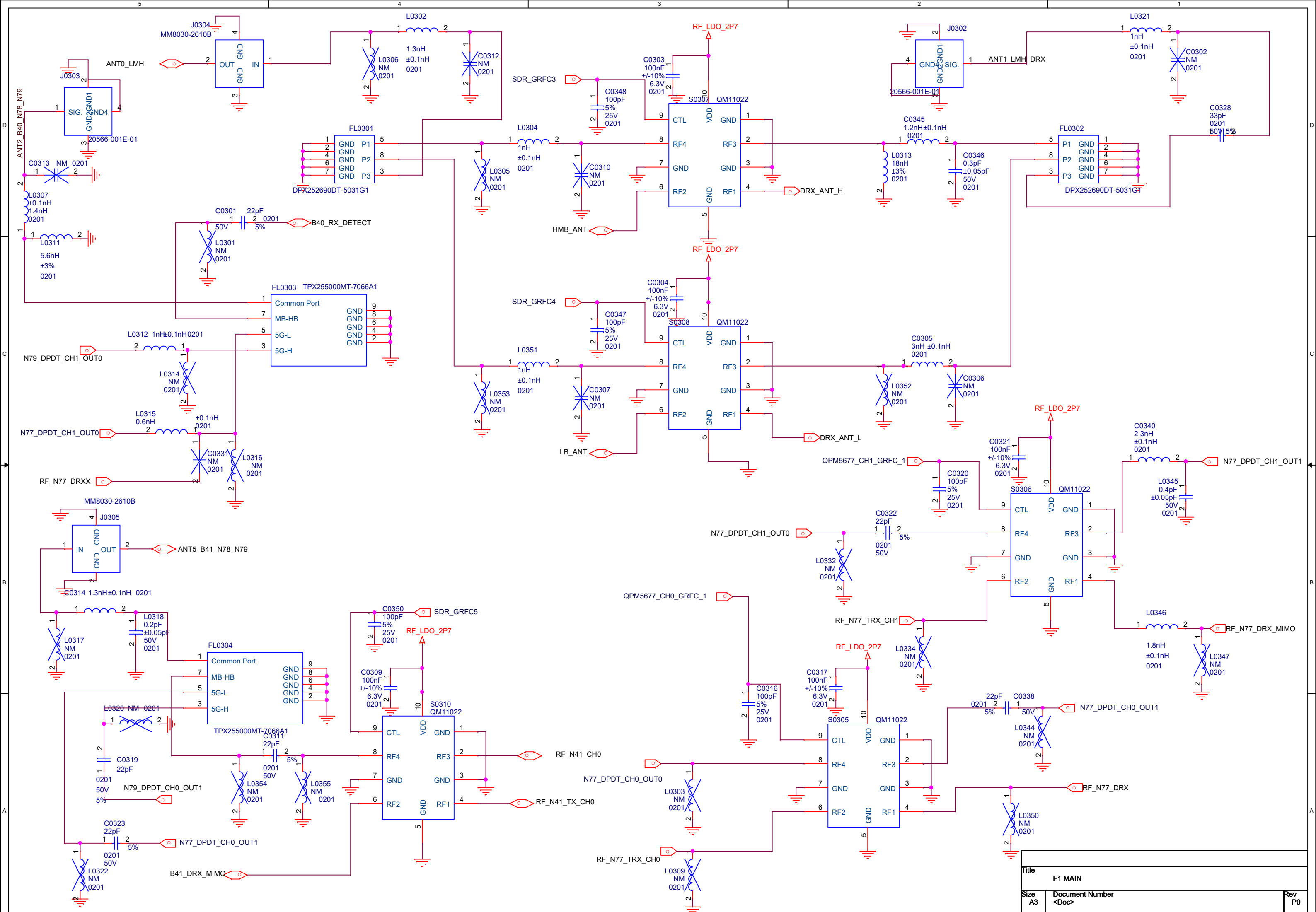
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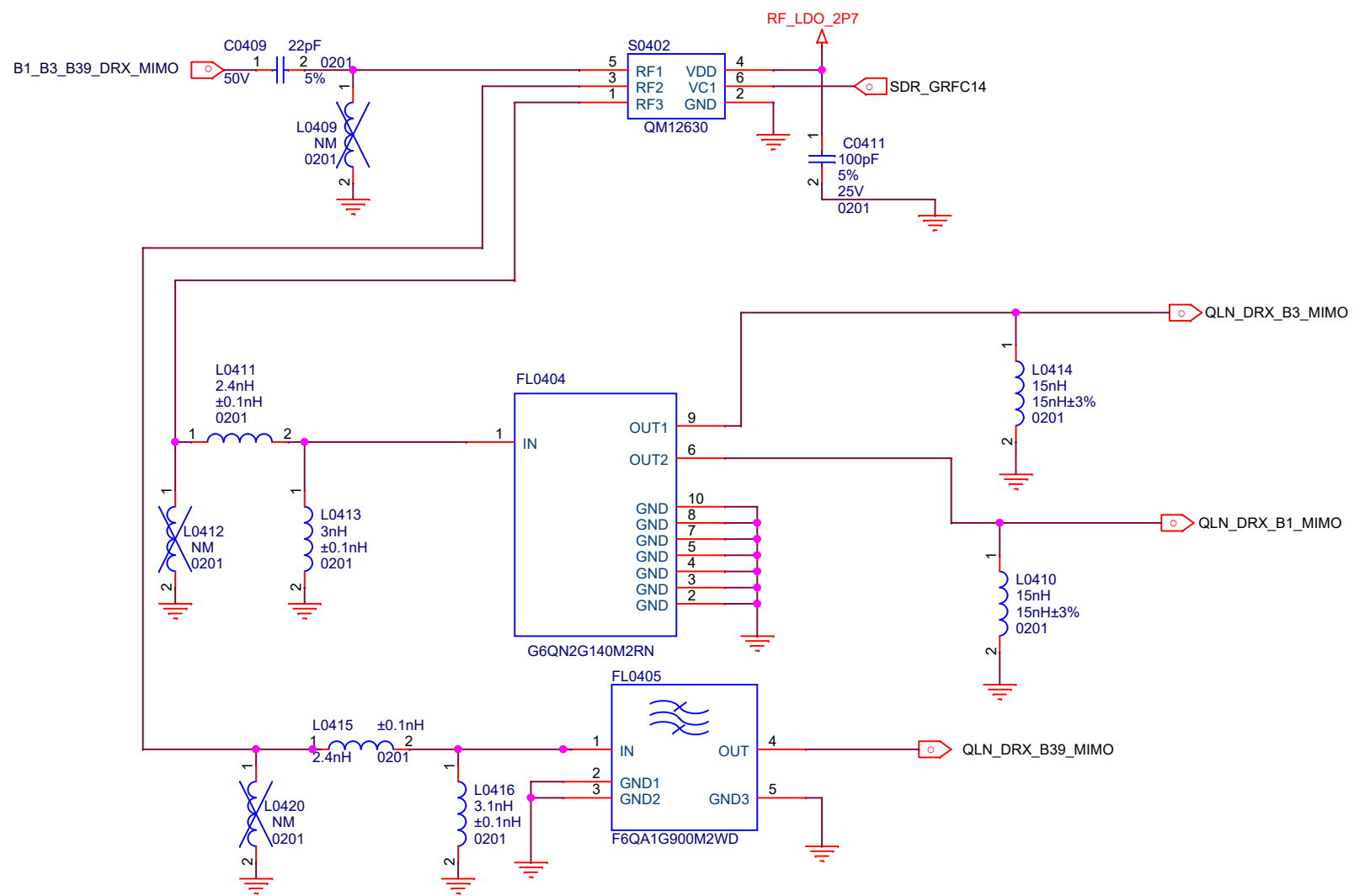
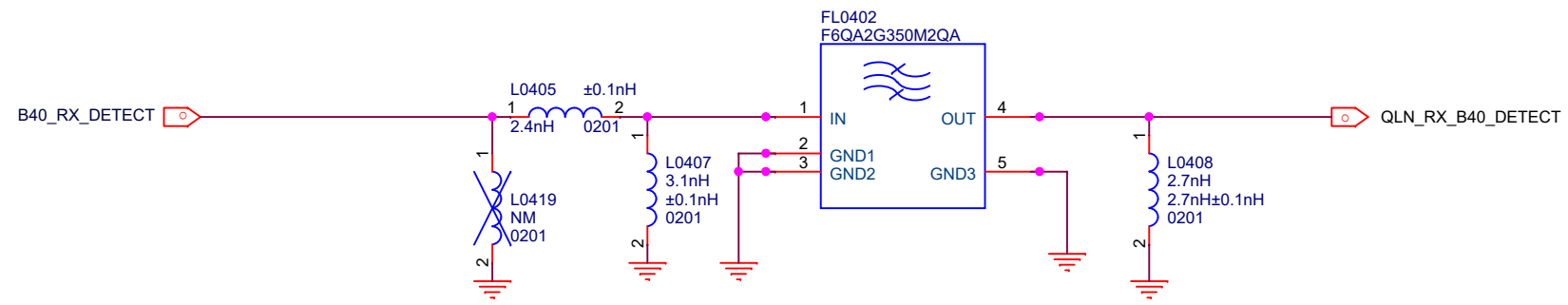
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Size	Document Number	Rev
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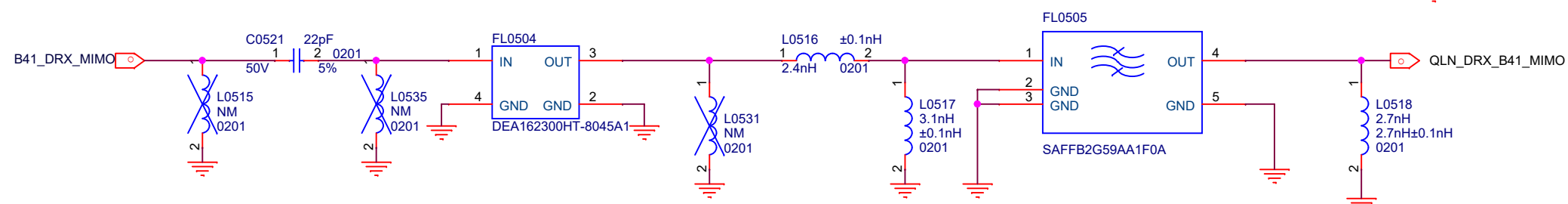
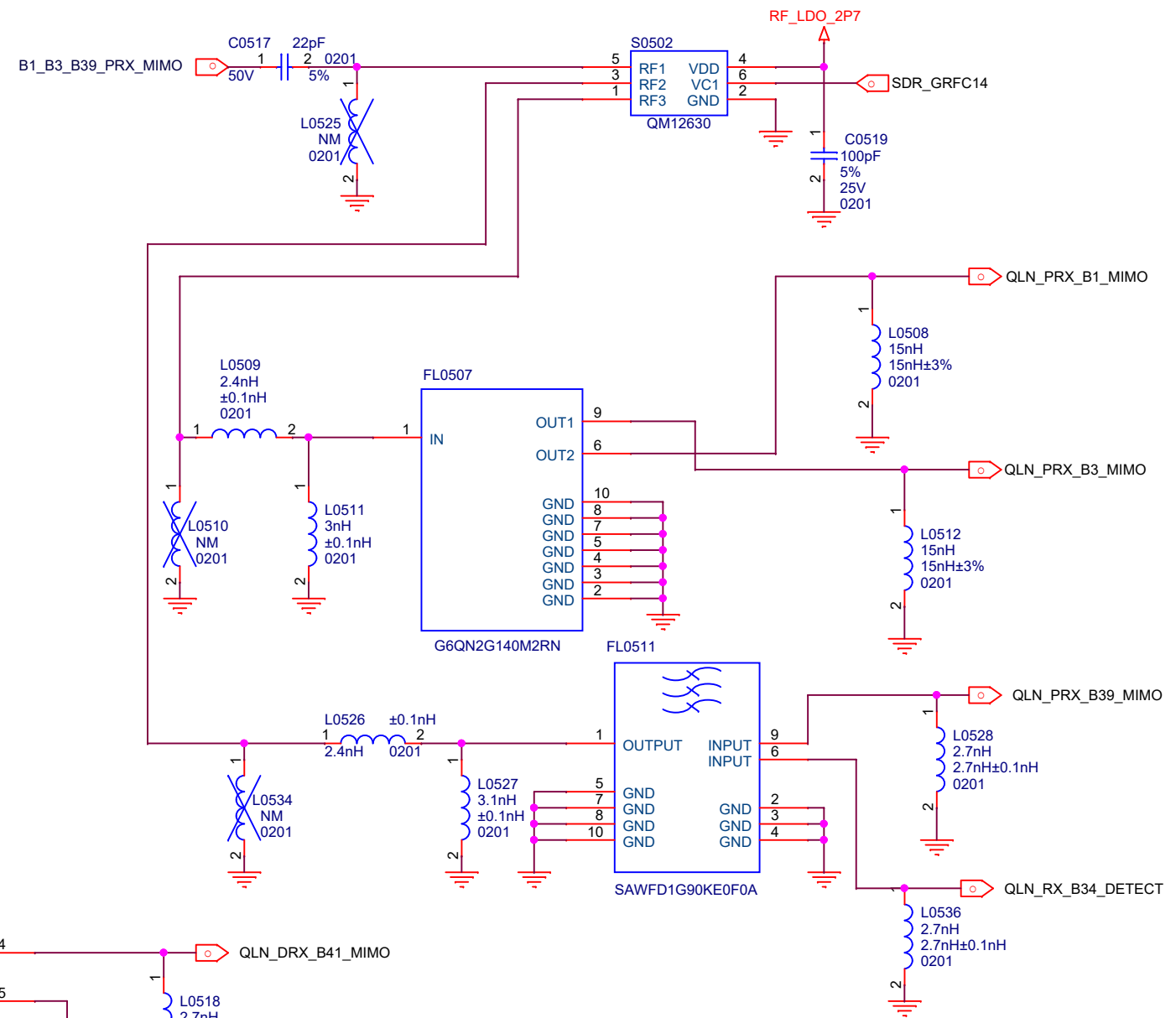
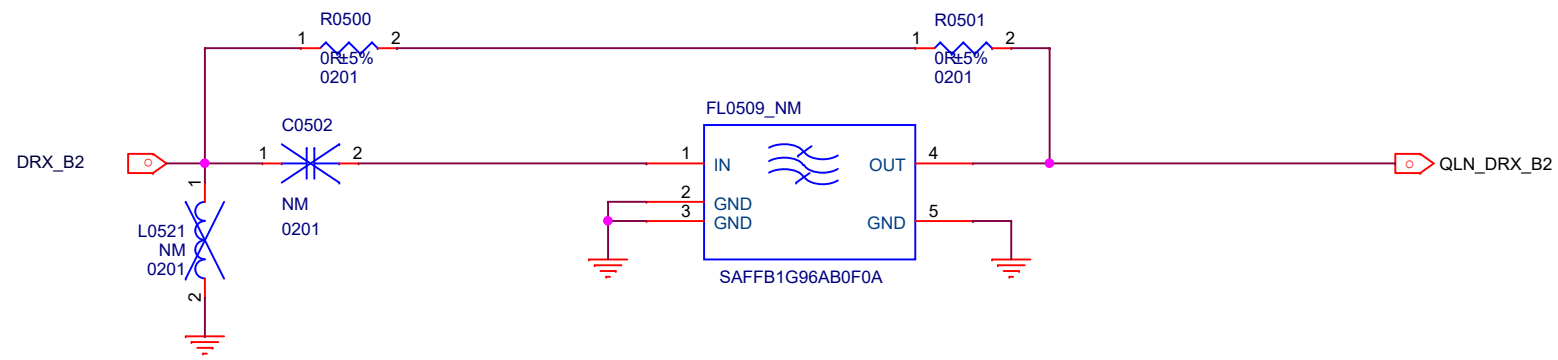
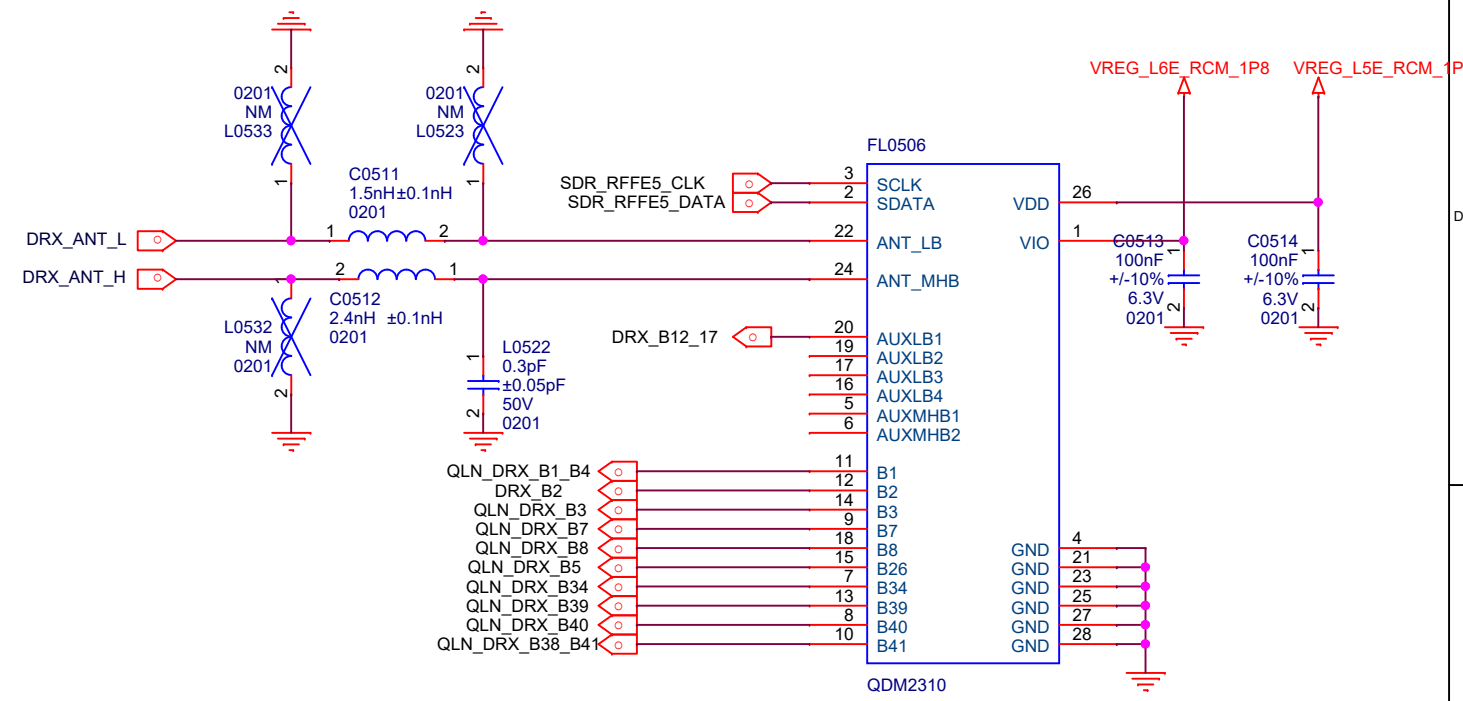
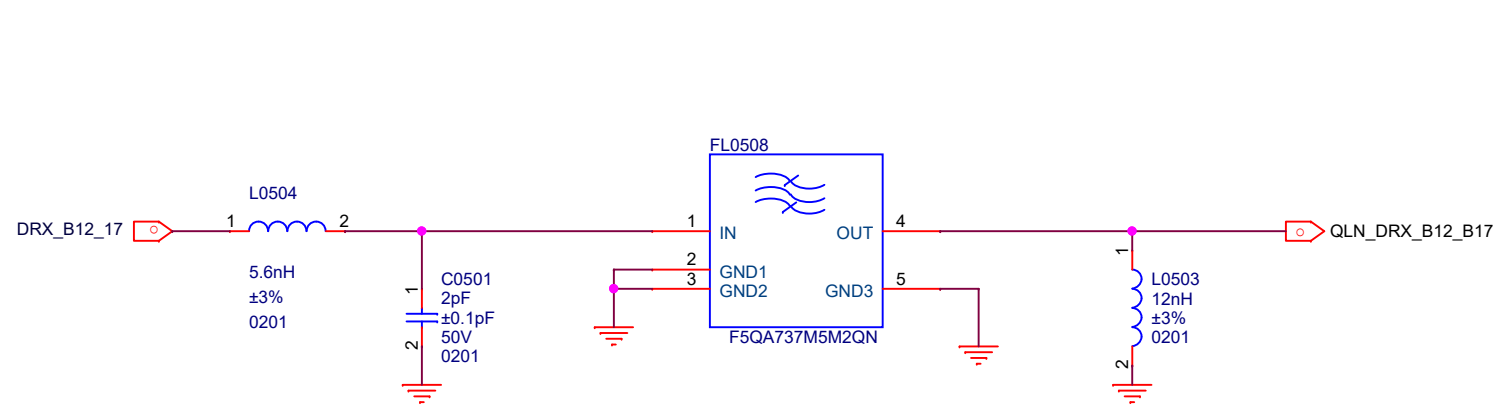
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Size	Document Number	Rev
A3	<Doc>	P0
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Title			F1 MAIN
Size	Document Number	Rev	
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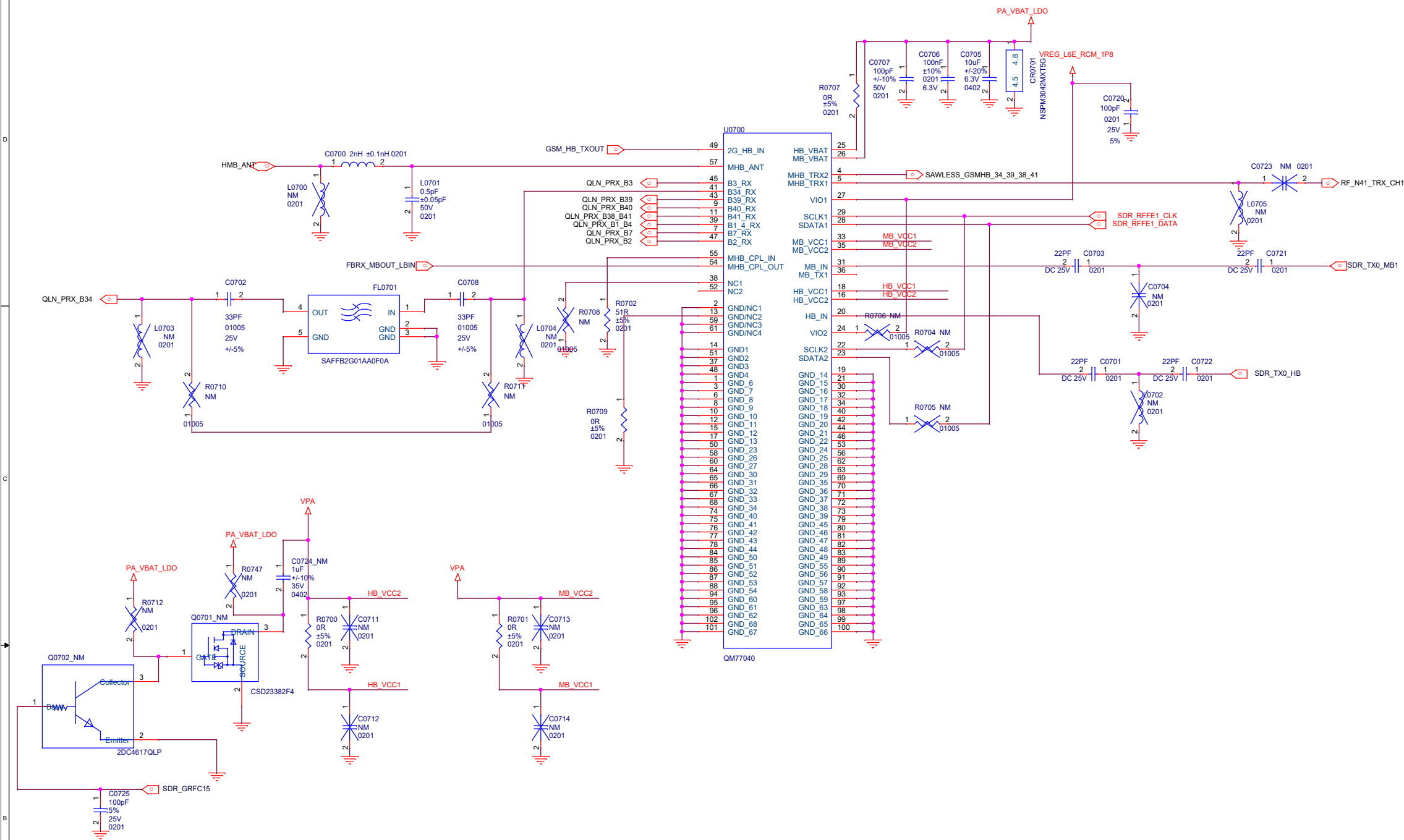


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Size	Document Number	Rev
A3	<Doc>	P0
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Title			F1 MAIN		
Size	Document Number		P0		
A3	<Doc>				
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Title	
F1 MAIN	
Size	Document Number
A3	Reserved(for PA)
Date:	Friday, November 29, 2019
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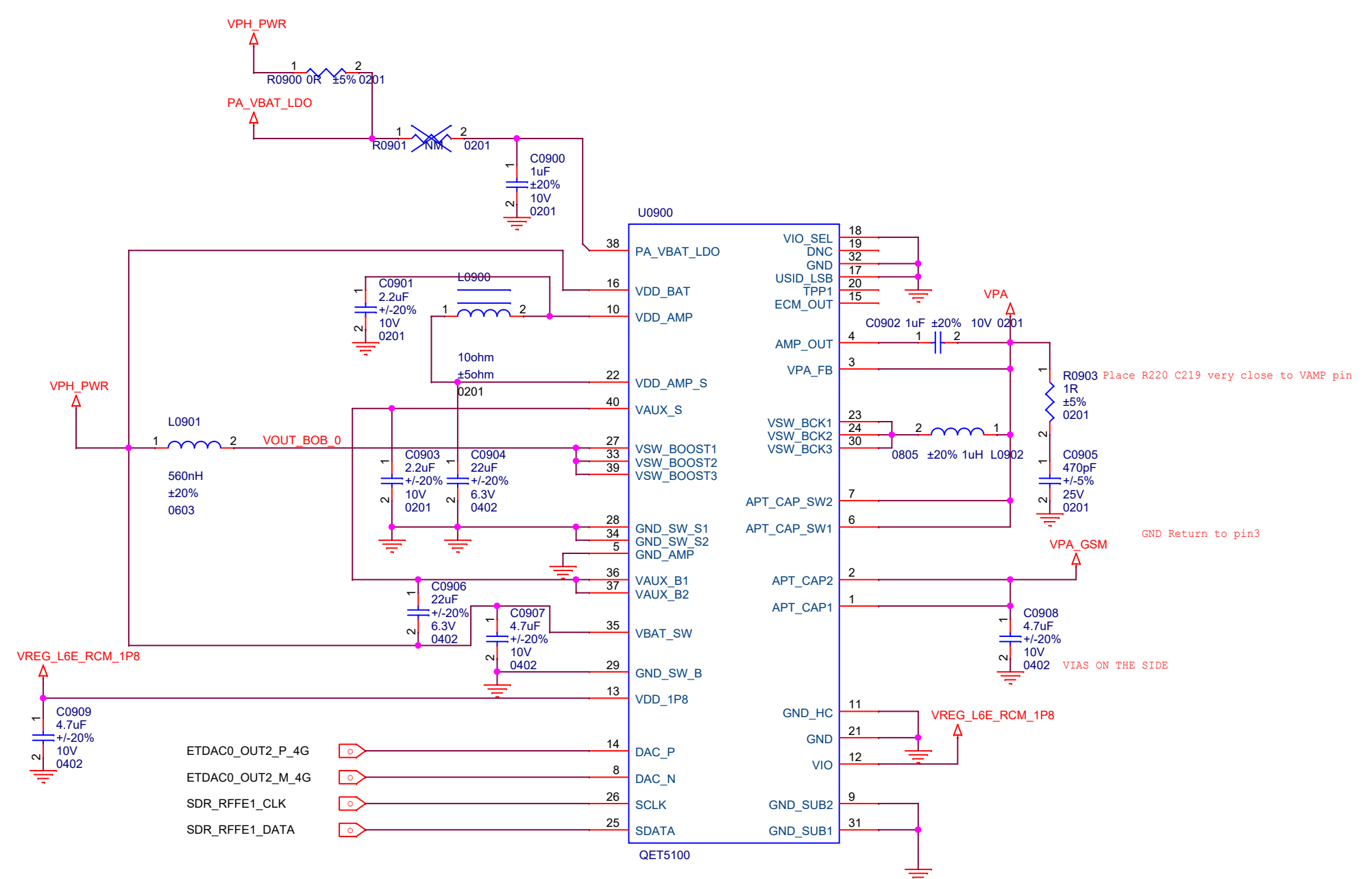
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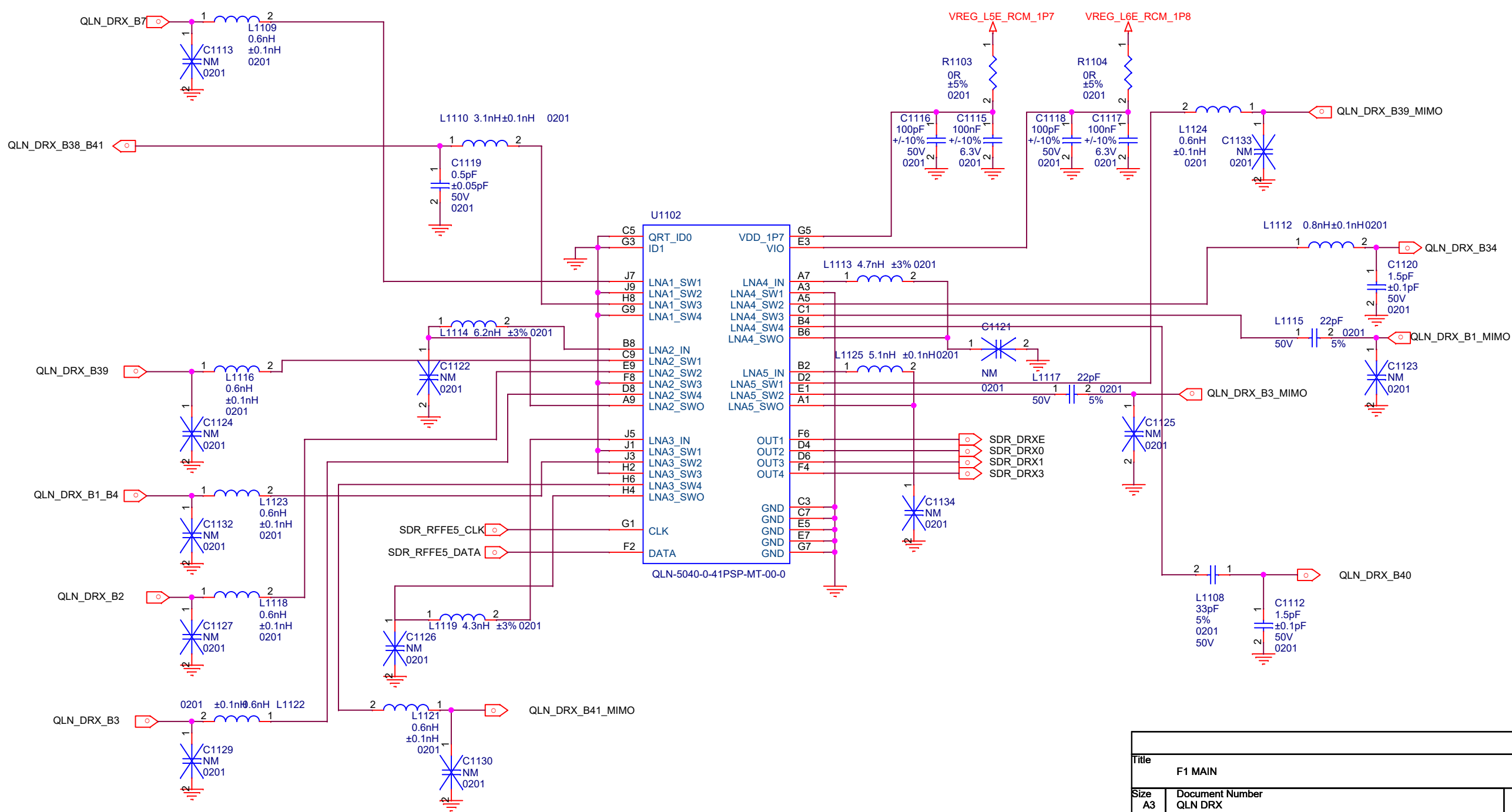
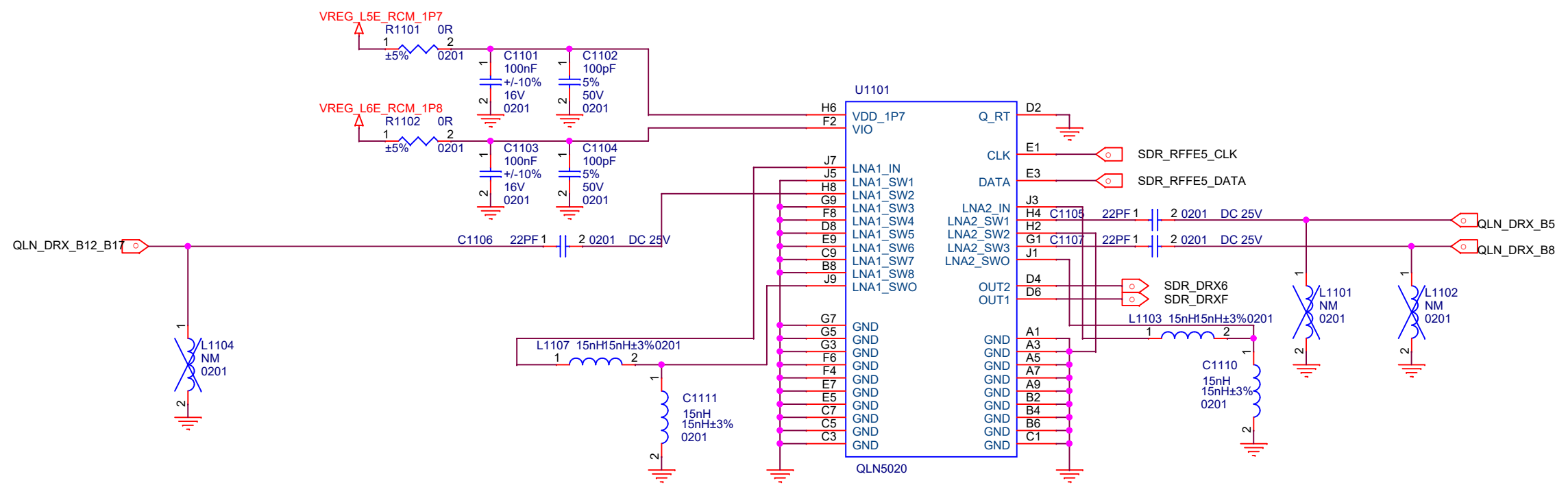
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Size	Document Number	QLN DRX
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Date:	Friday, November 29, 2019	Sheet

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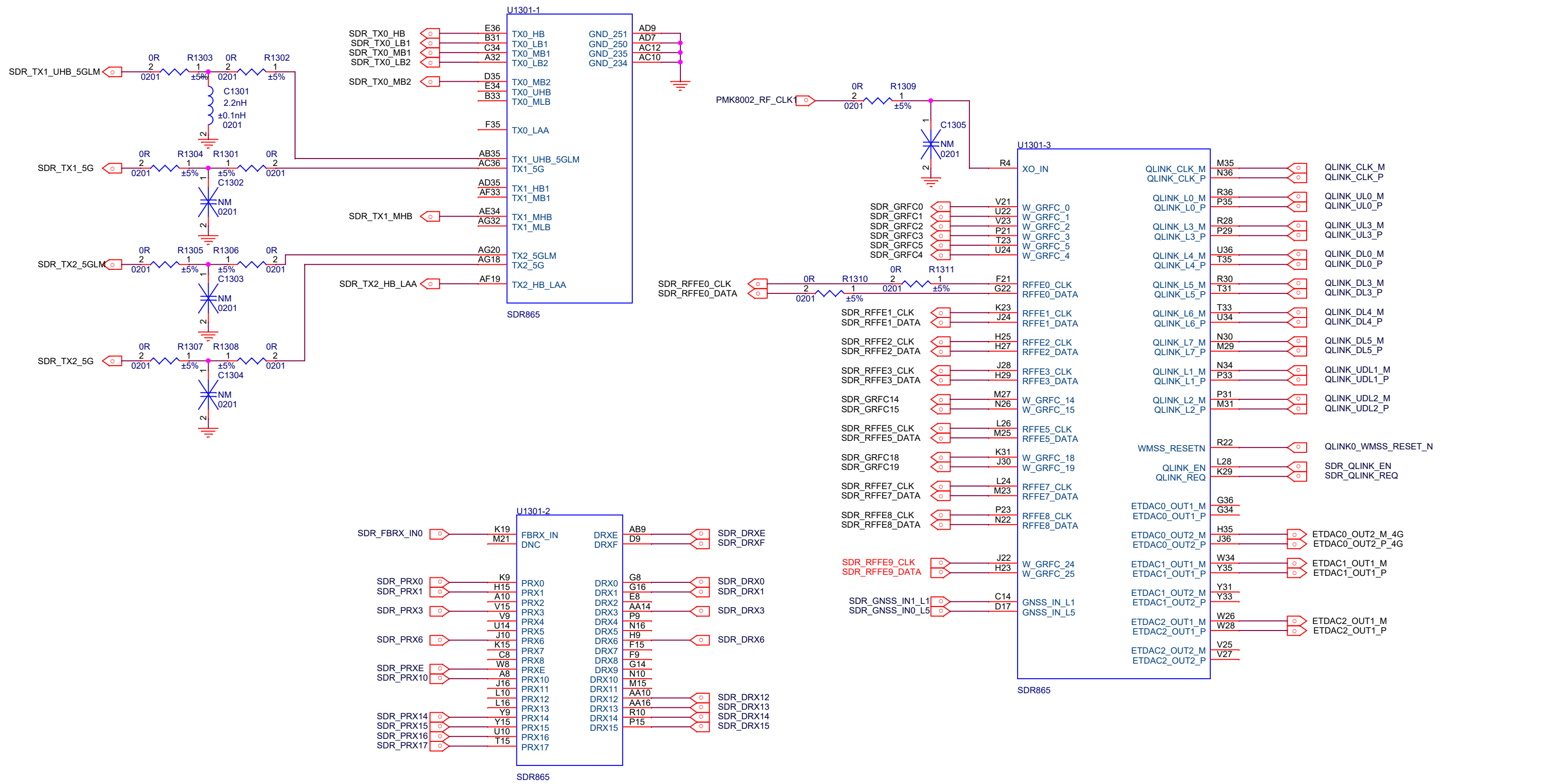
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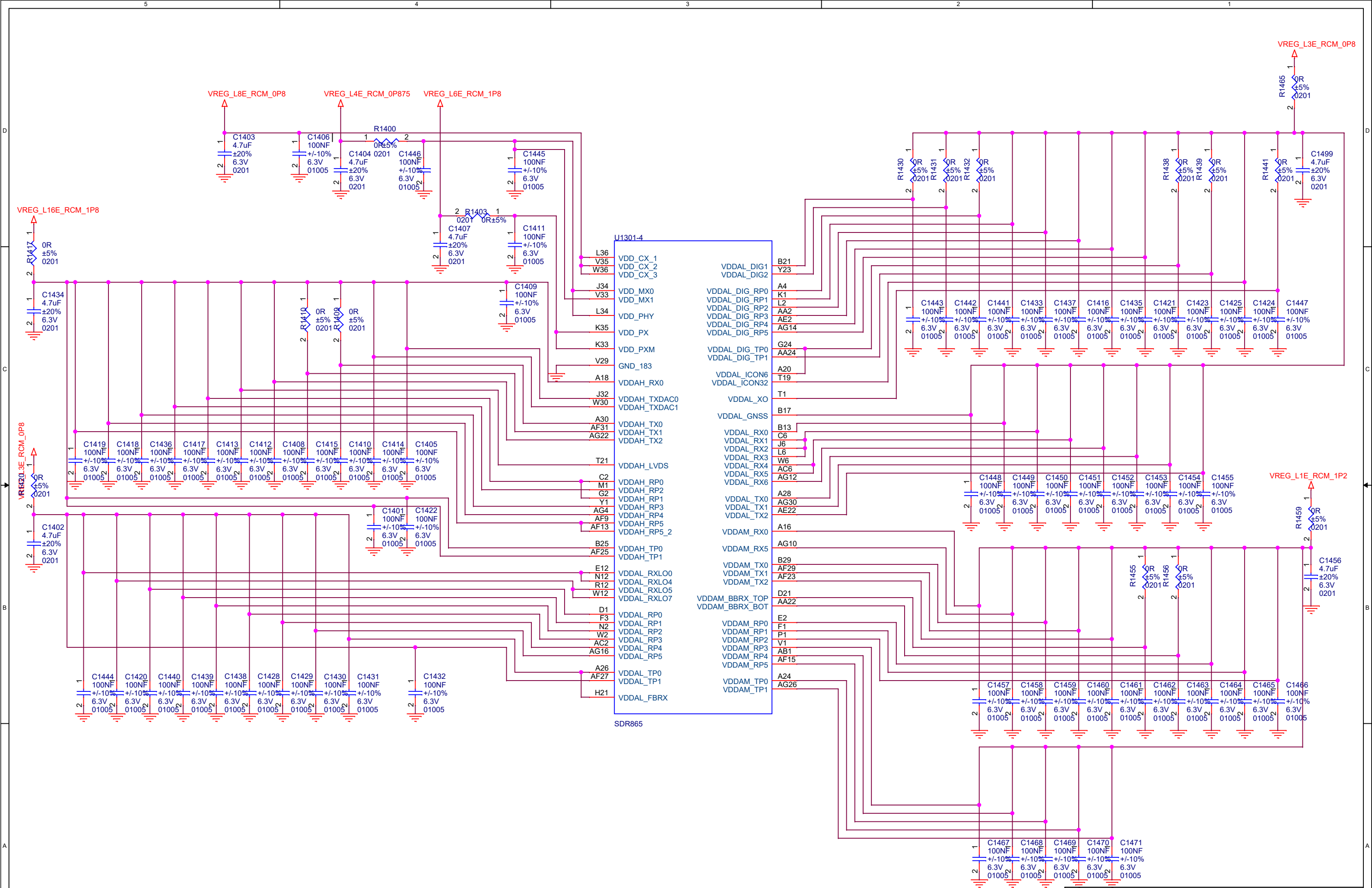
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Date:	Friday, November 29, 2019
Sheet	1



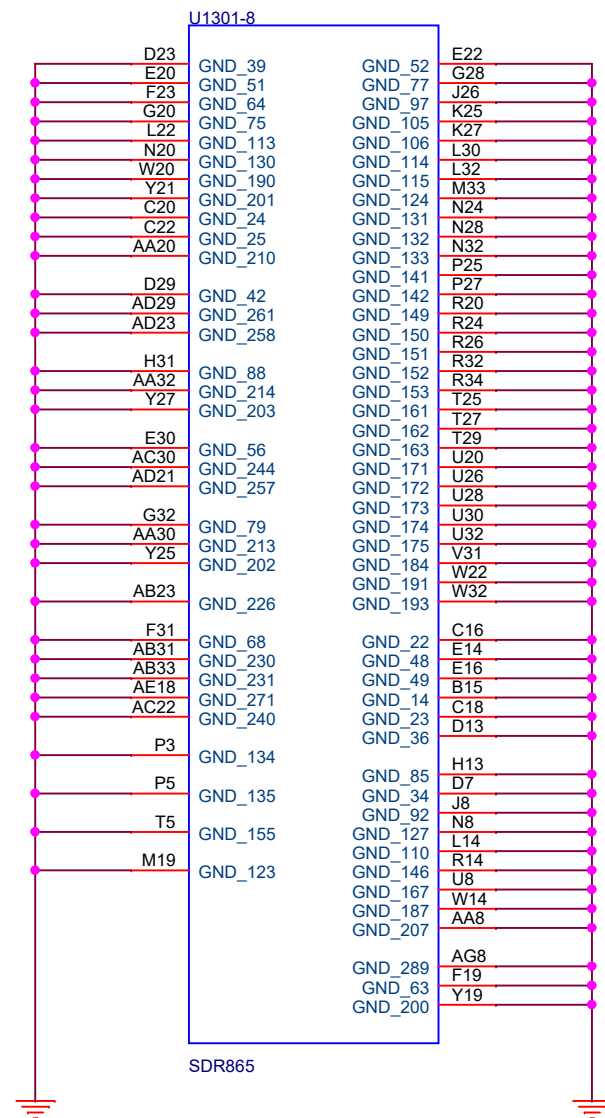
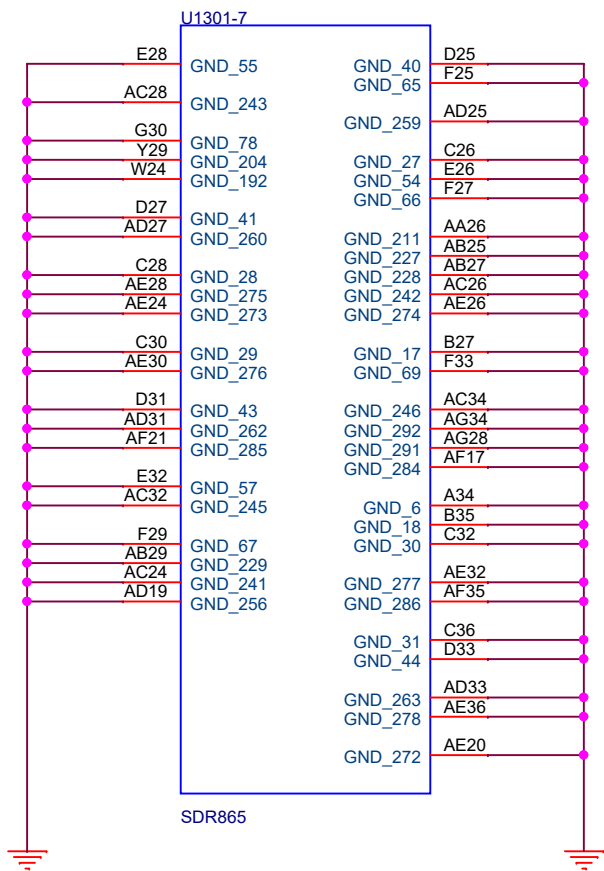
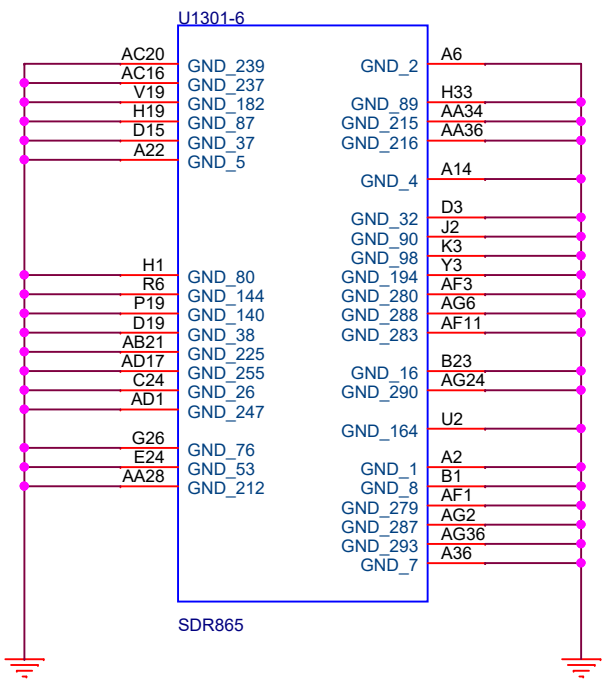
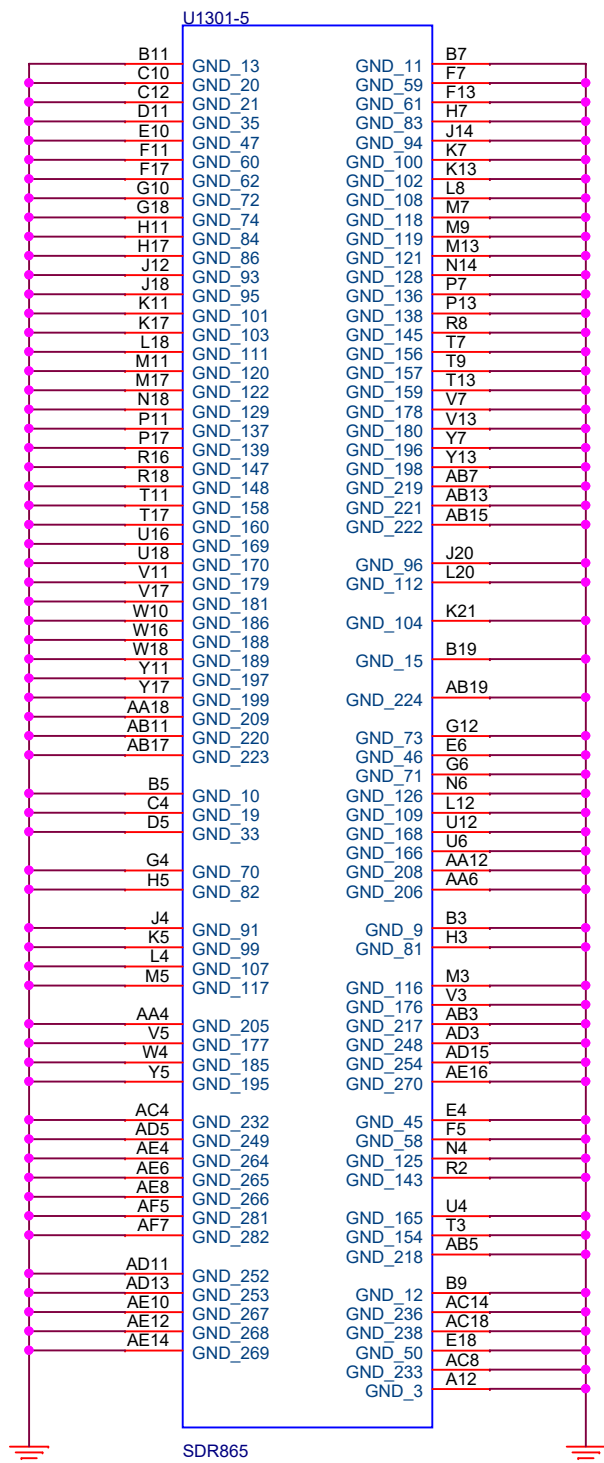


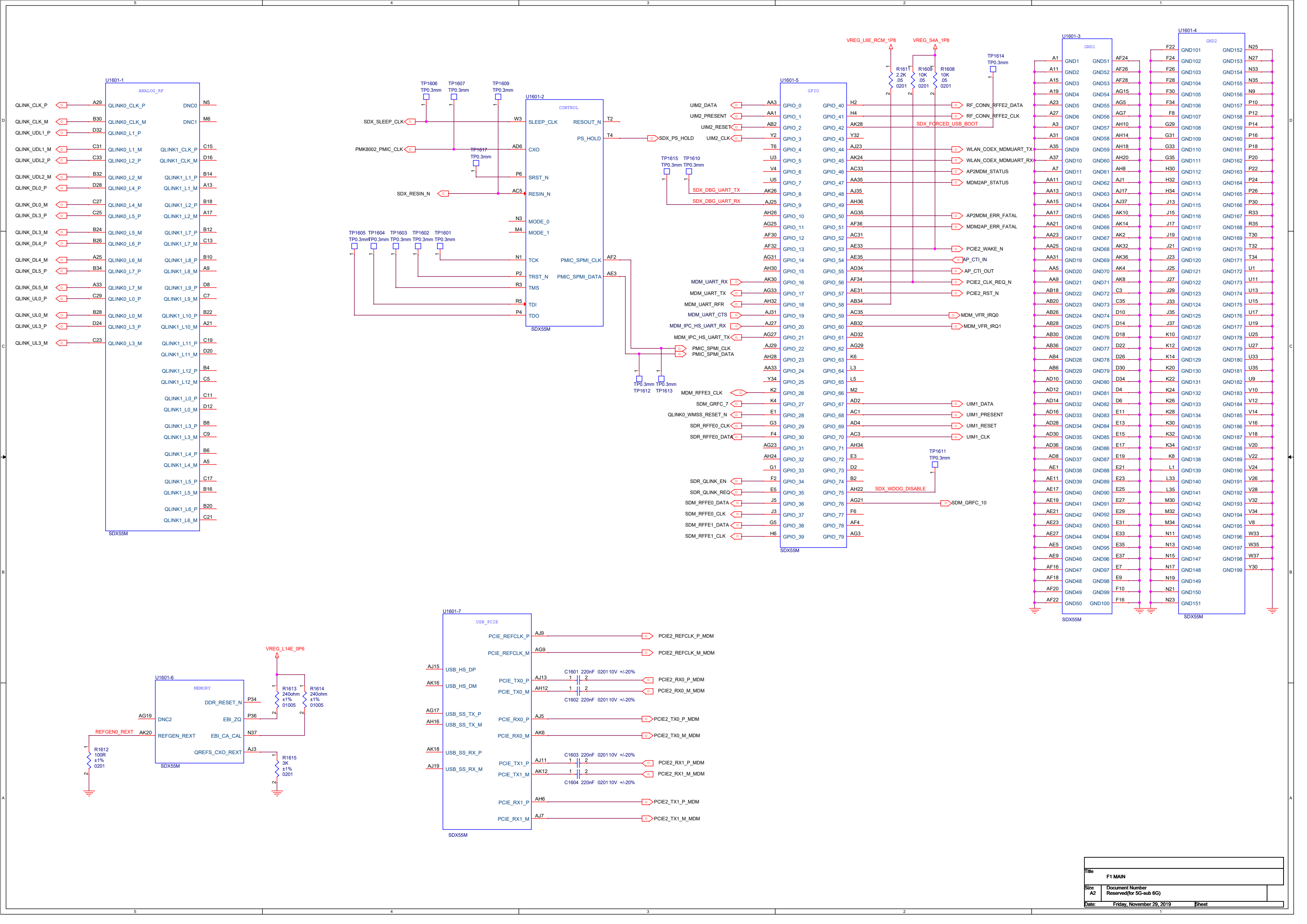
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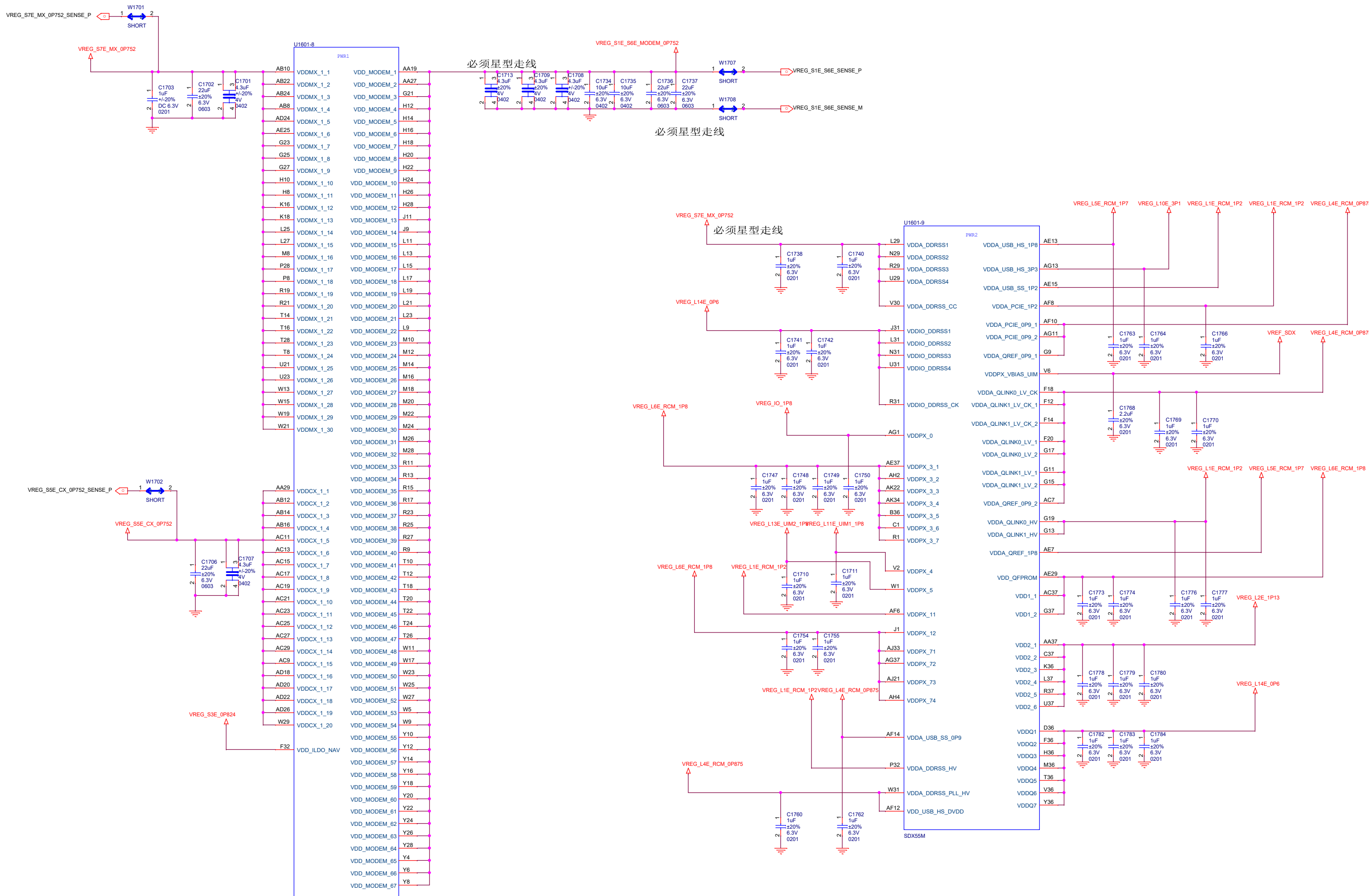
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V35	VDD_CX_2
W36	VDD_CX_3
J34	VDD_MX0
V33	VDD_MX1
L34	VDD_PHY
K35	VDD_PX
K33	VDD_PXM
V29	GND_183
A18	VDDAH_RX0
J32	VDDAH_TXDAC0
W30	VDDAH_TXDAC1
A30	VDDAH_TX0
AF31	VDDAH_TX1
AG22	VDDAH_TX2
T21	VDDAH_LVDS
C2	VDDAH_RP0
M1	VDDAH_RP2
G2	VDDAH_RP1
Y1	VDDAH_RP3
AG4	VDDAH_RP4
AF9	VDDAH_RP5
AF13	VDDAH_RP5_2
B25	VDDAH_TP0
AF25	VDDAH_TP1
E12	VDDAL_RXLO0
N12	VDDAL_RXLO4
R12	VDDAL_RXLO5
W12	VDDAL_RXLO7
D1	VDDAL_RP0
F3	VDDAL_RP1
N2	VDDAL_RP2
W2	VDDAL_RP3
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SDR865

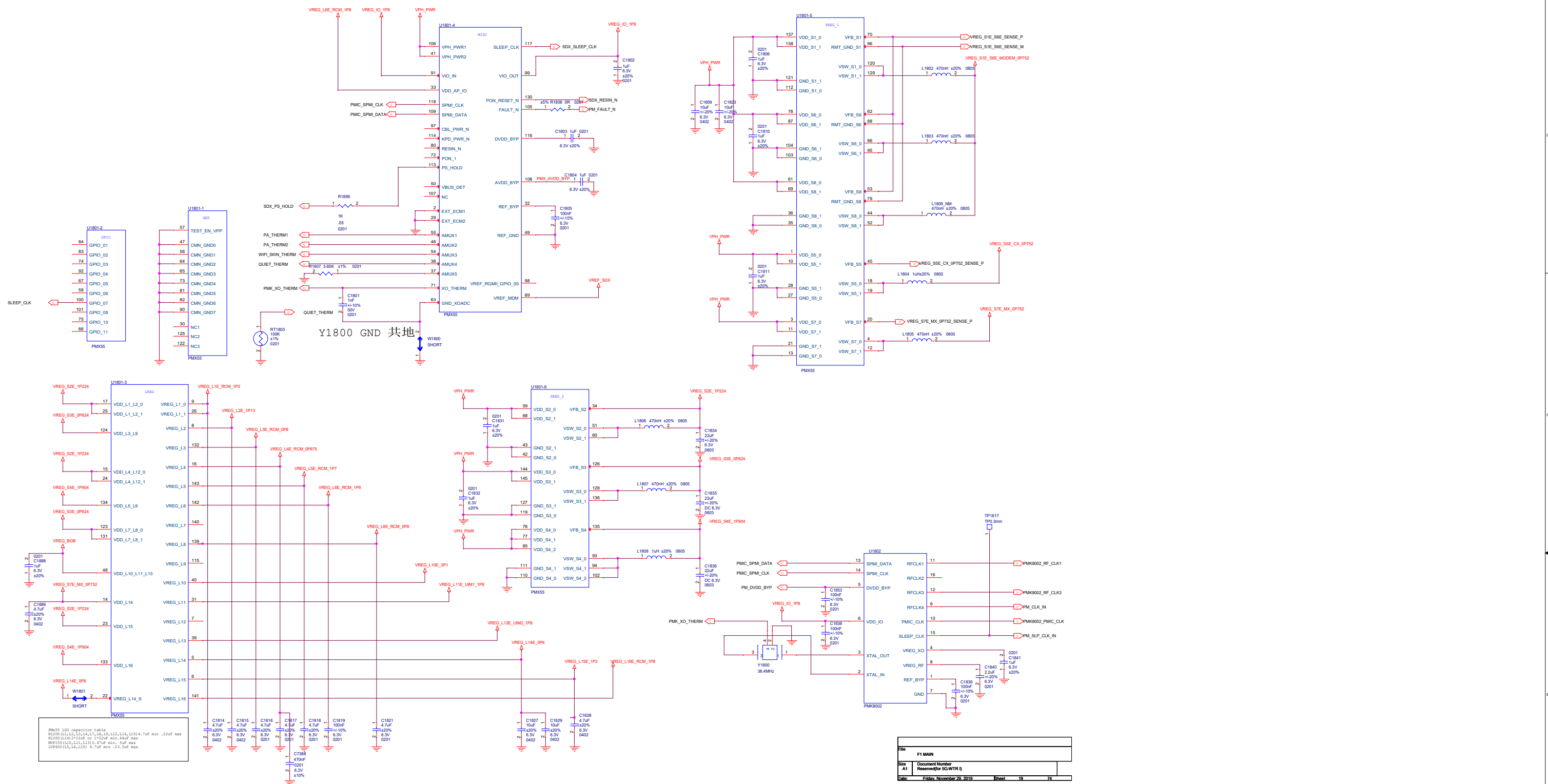
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Size	A3	Document Number	WTR PWR
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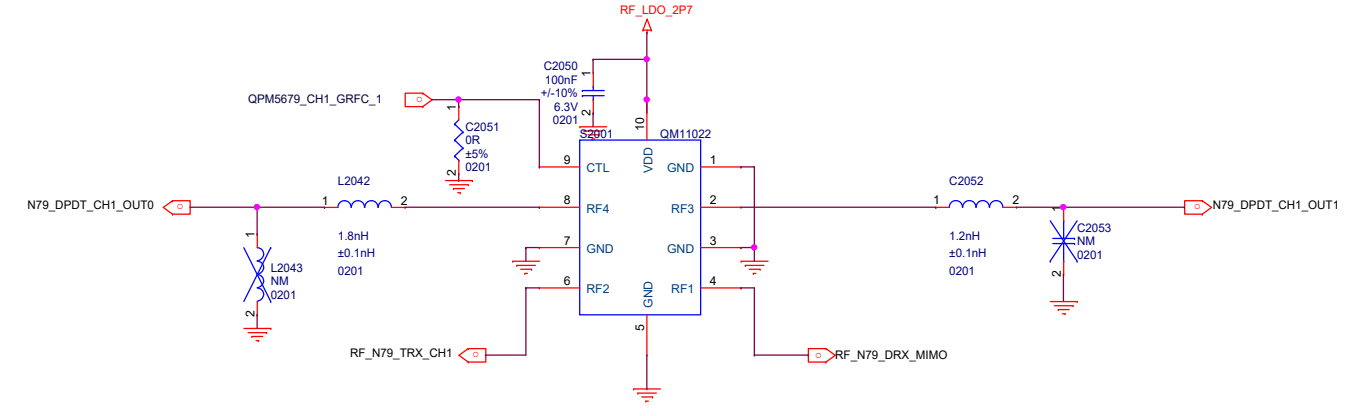
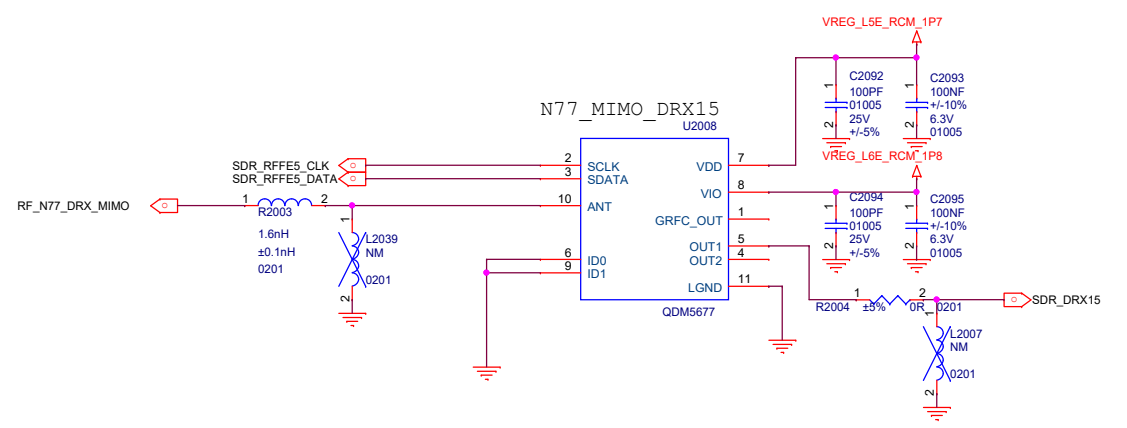
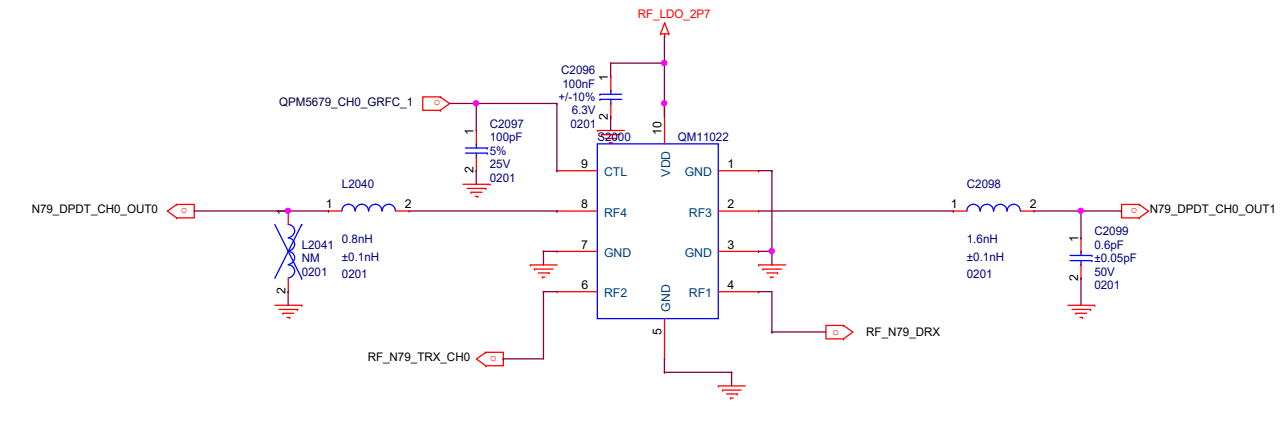
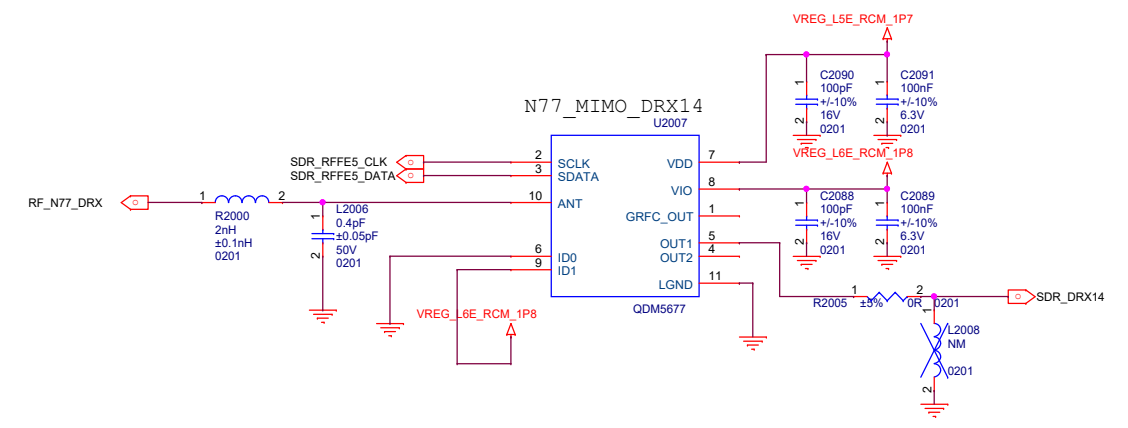
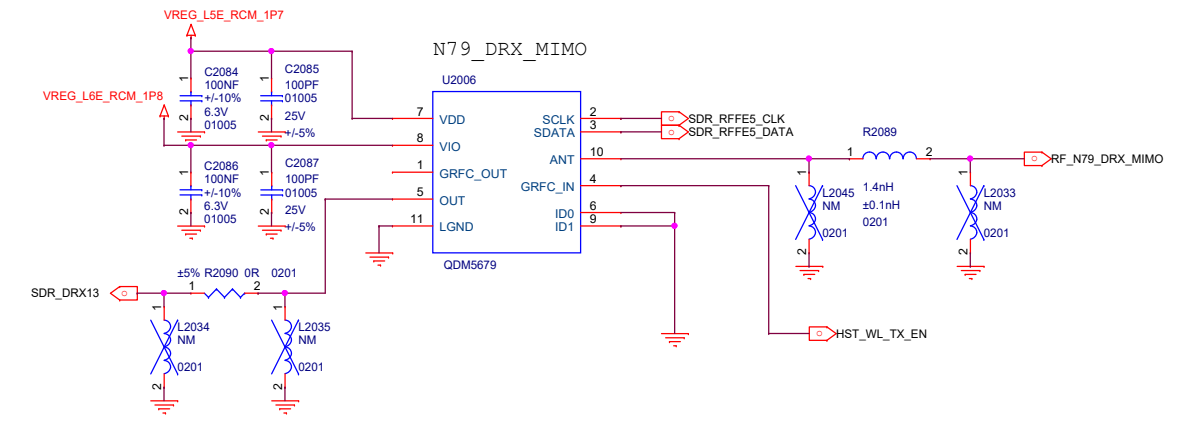
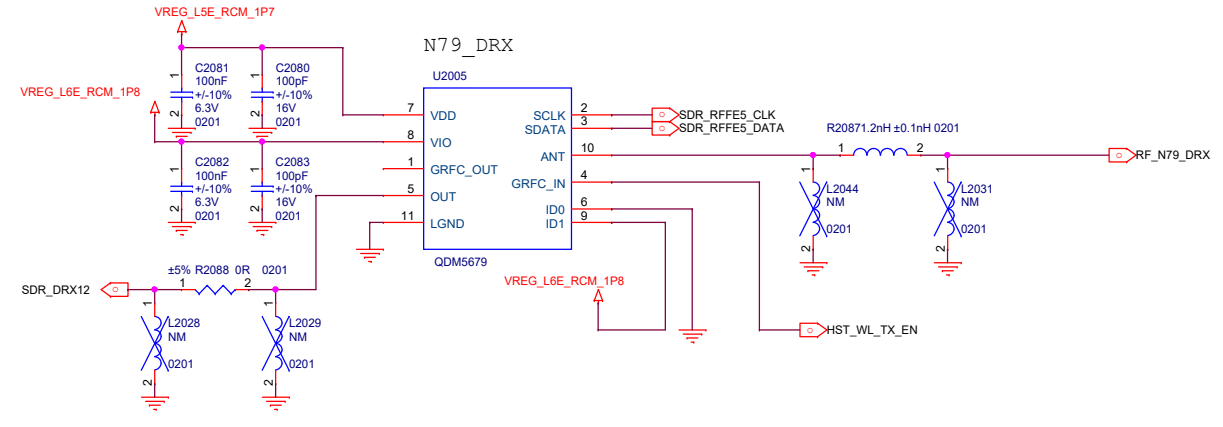
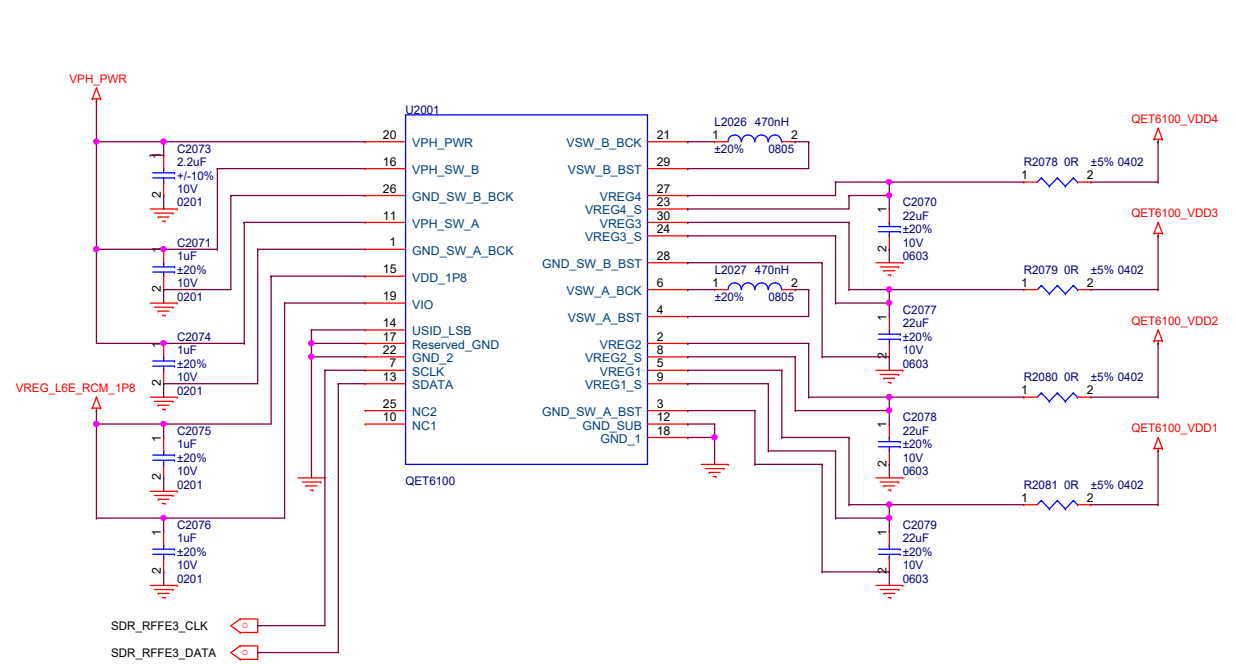


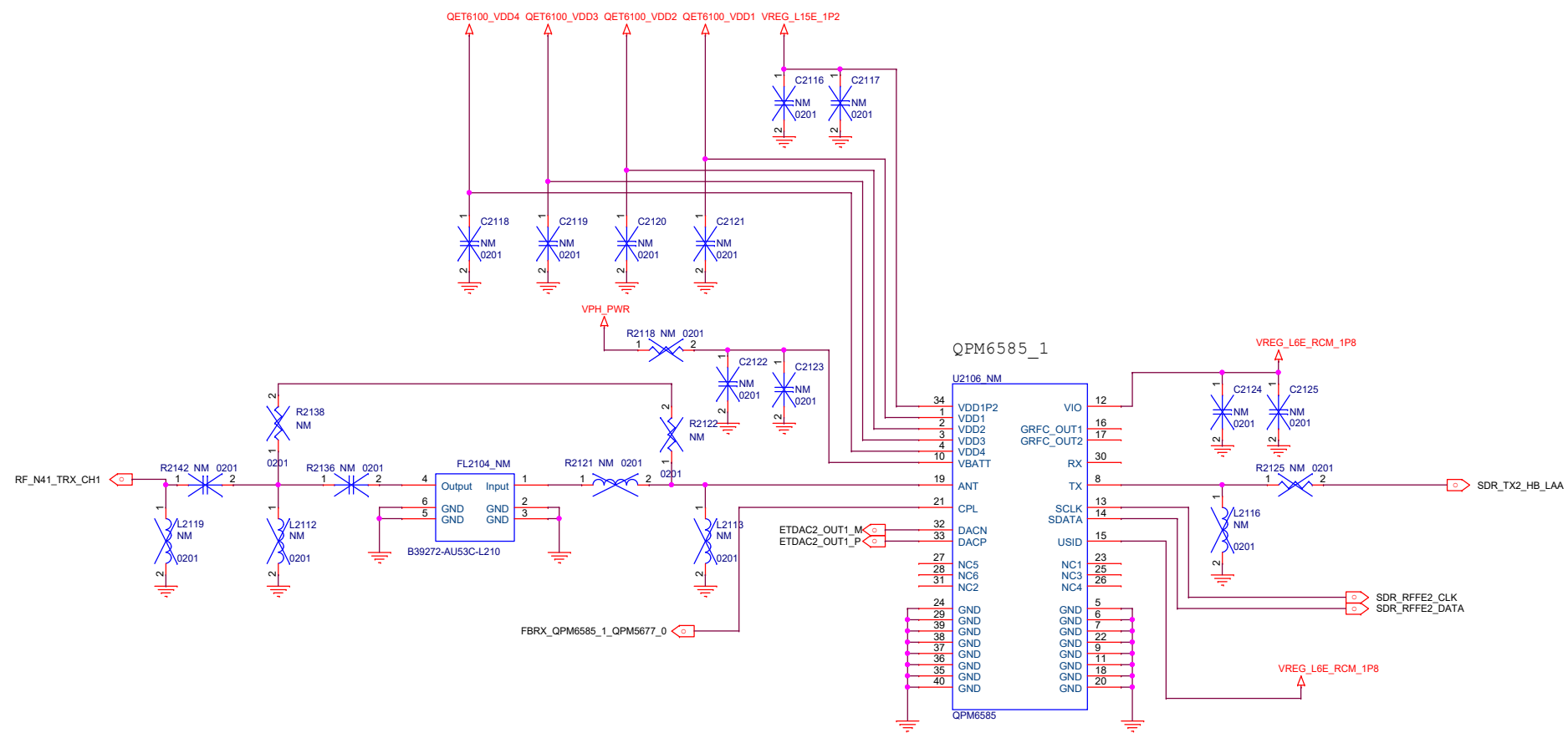
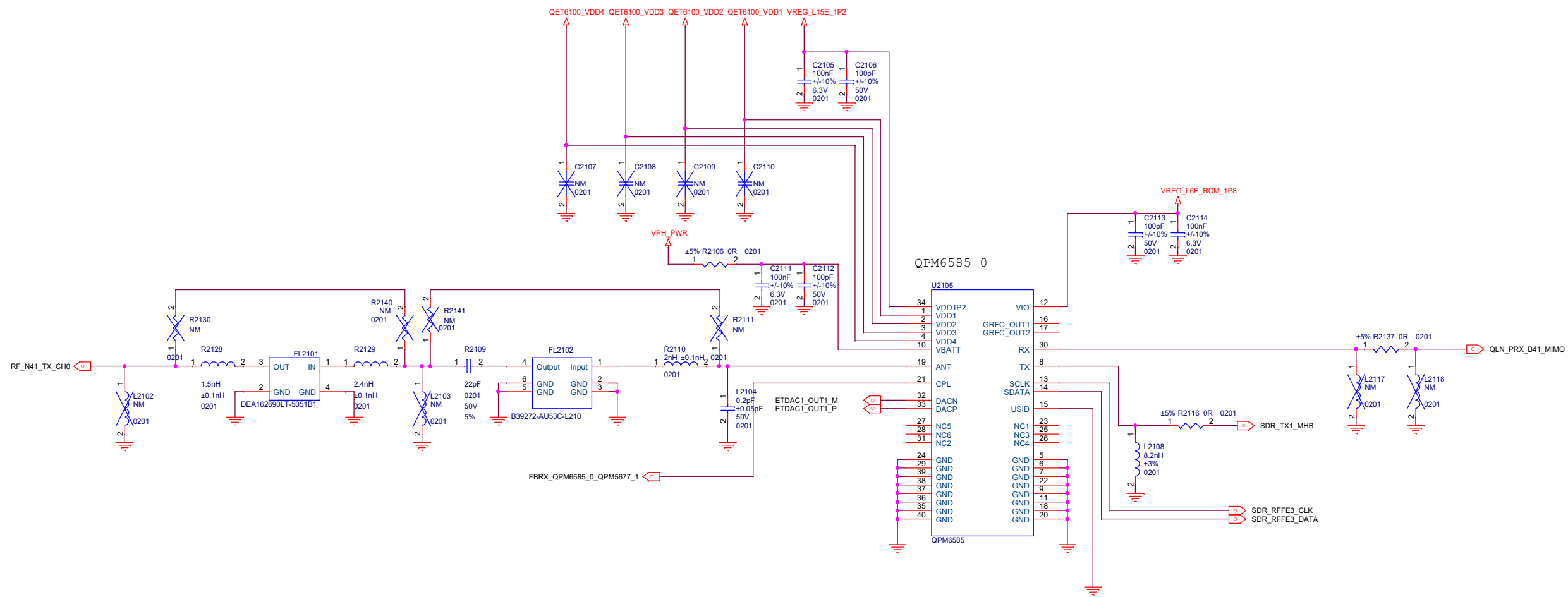
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A2	Reserved(for MM Wave)
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80V 120 capacitor table
 81200 (11,12,13,14,17,18,19,112,114,115) 4.7uF min .22uF max
 81205 (114) 2.2uF or 1.5uF min .4uF max
 809150 (110,111,113) 0.47uF min .5uF max
 809150 (110,111,113) 0.47uF min .5uF max

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Size	A1
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Res	Reserved (for SG-WTR)
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Title	
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A3	Reserved(for PA)
Date:	Friday, November 29, 2019
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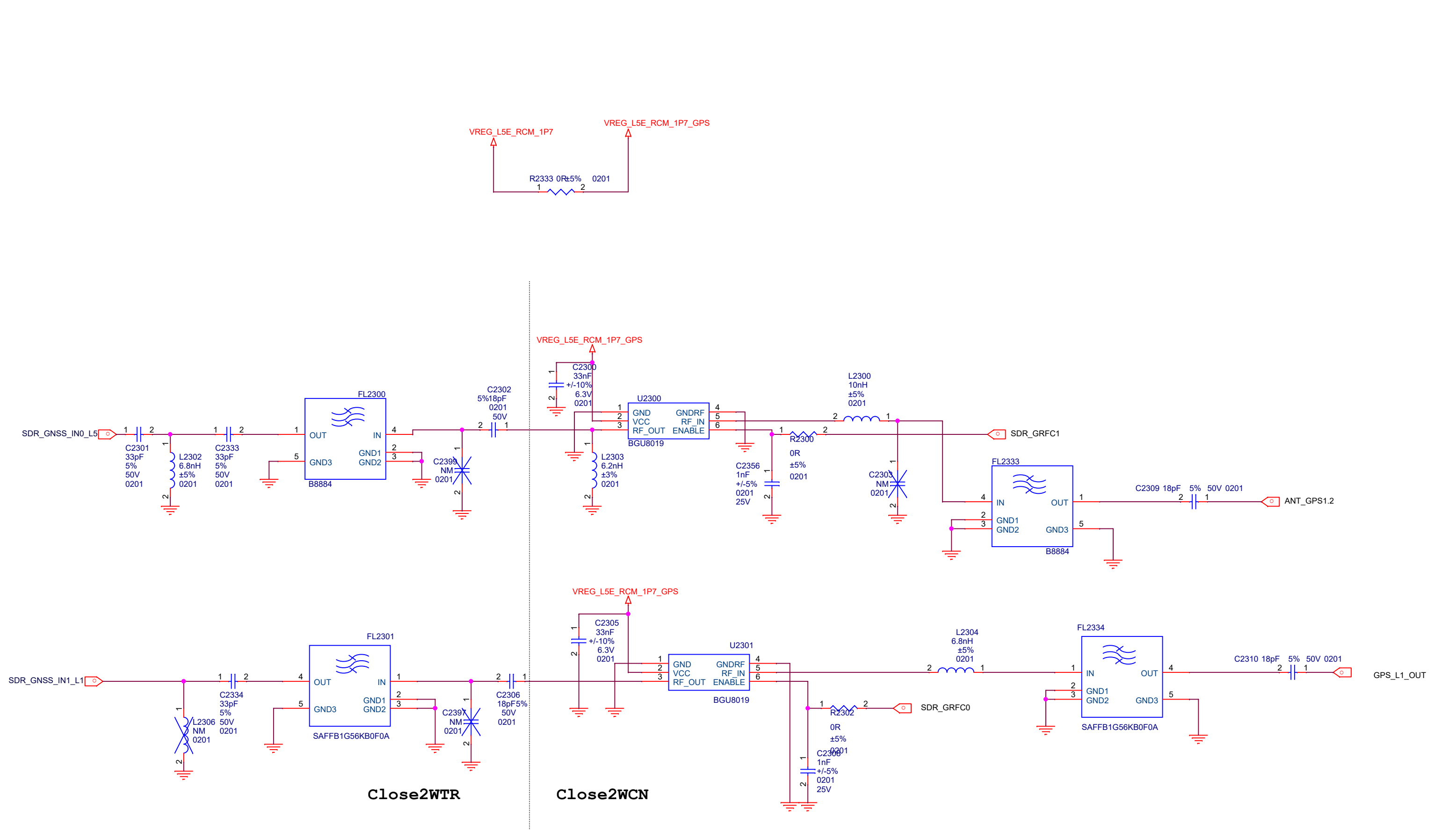
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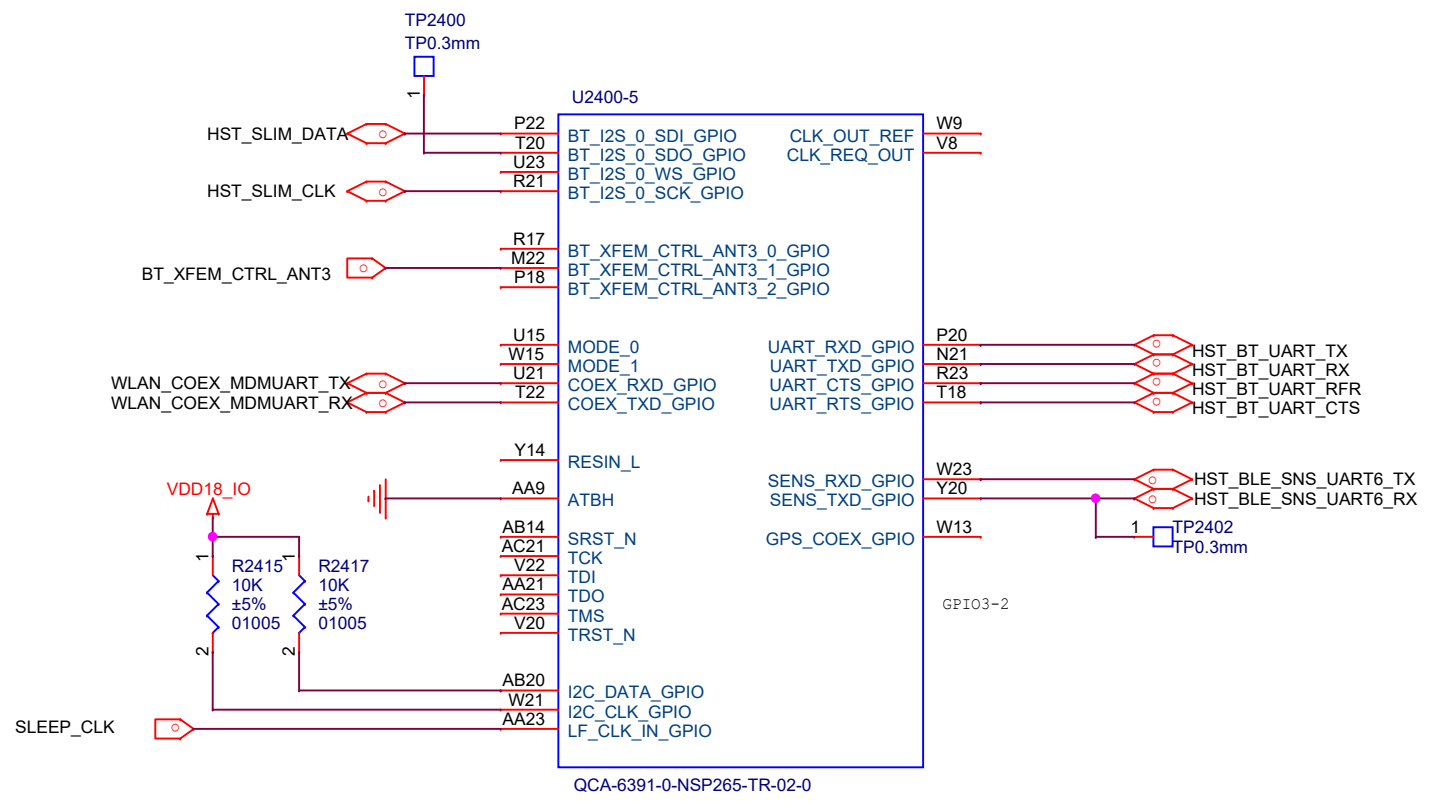
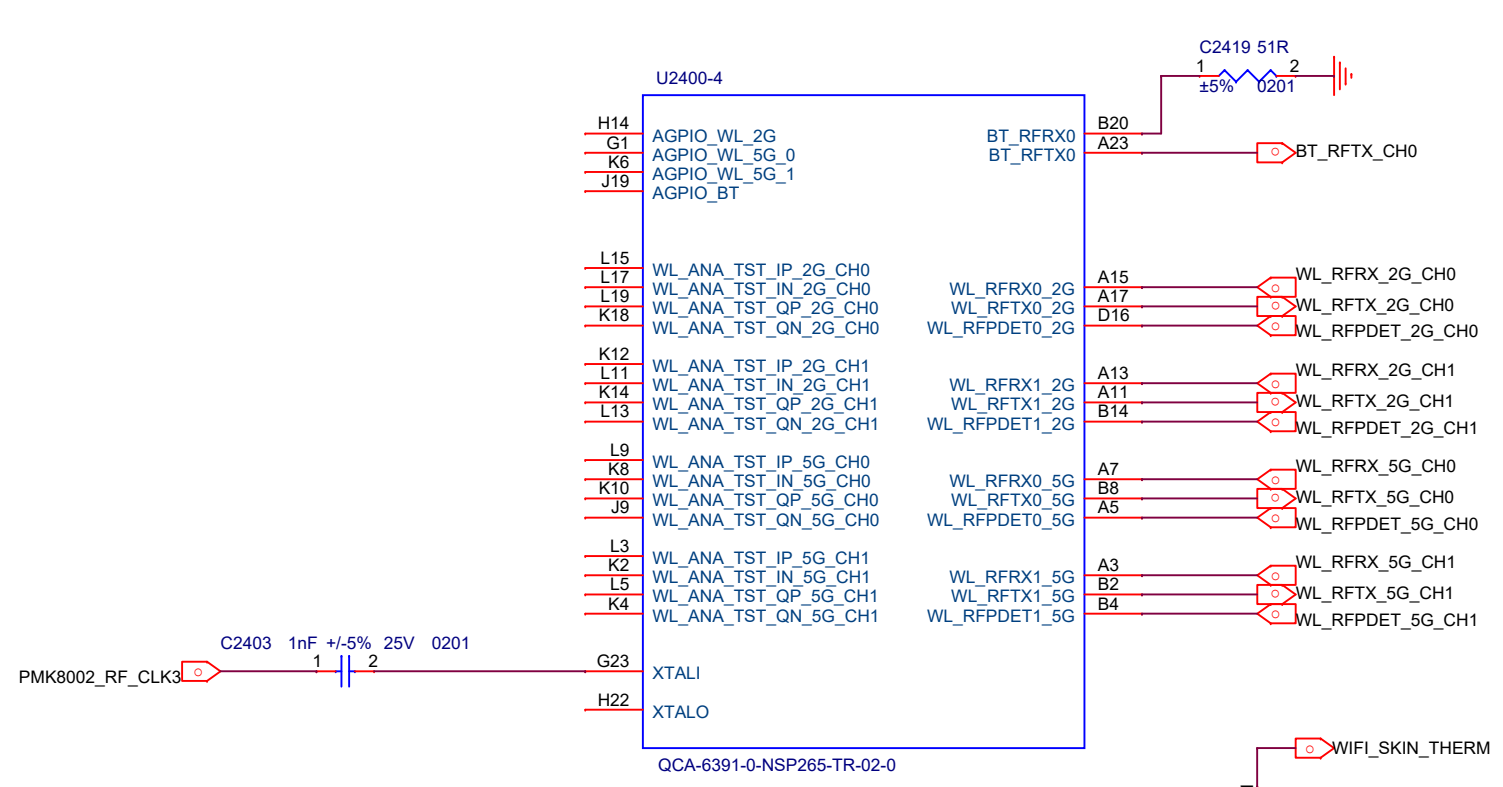
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Close2WTR

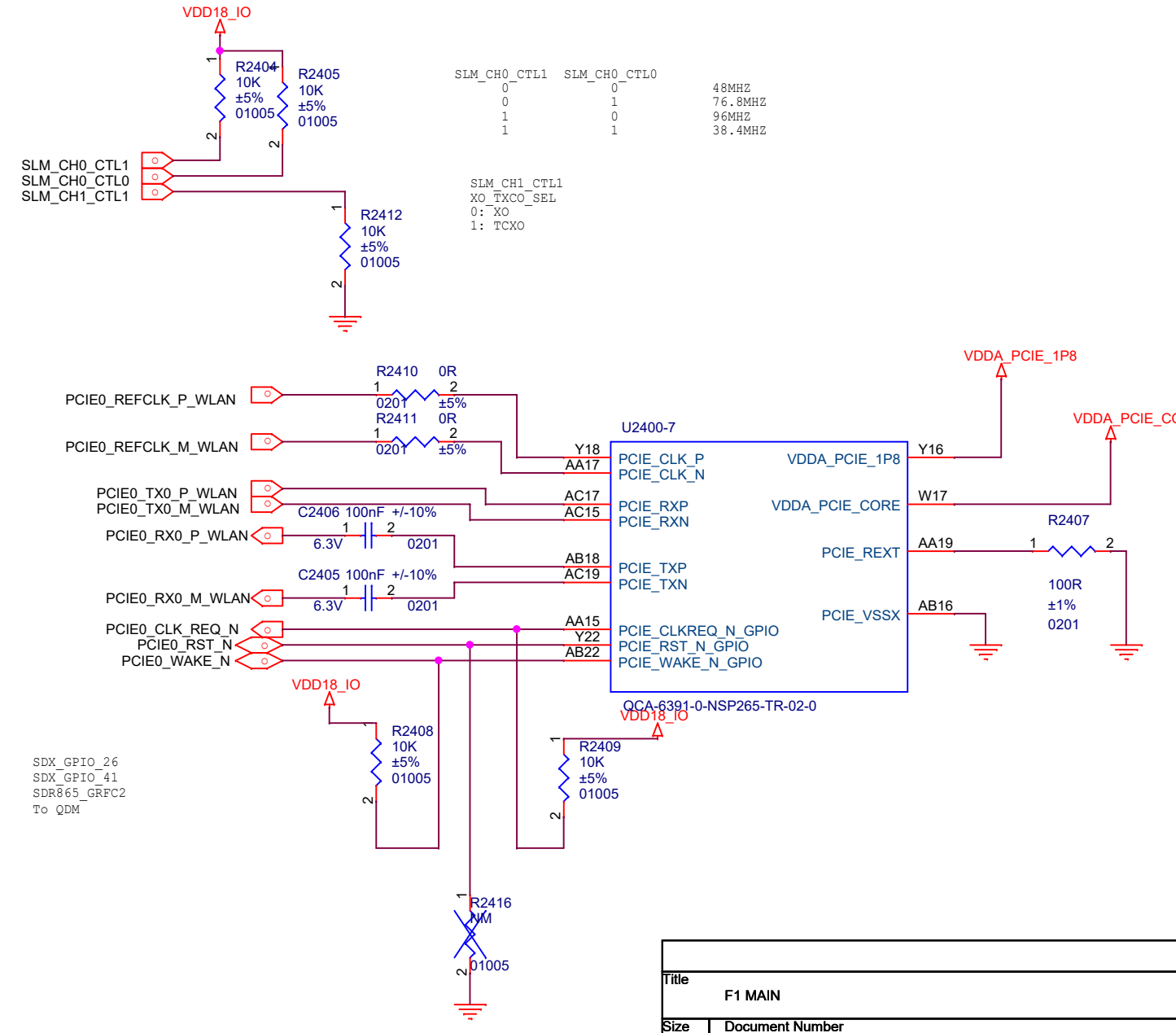
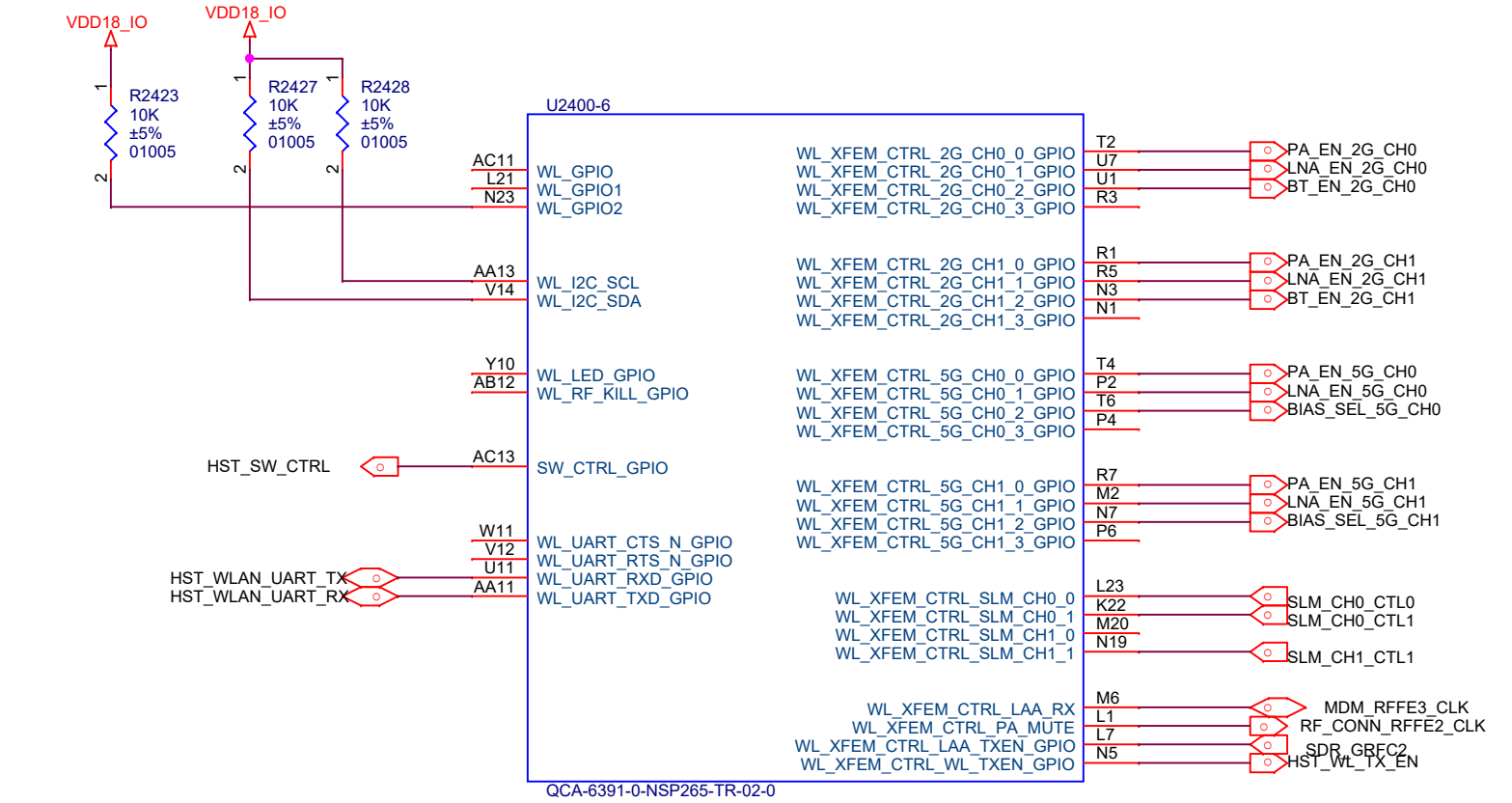
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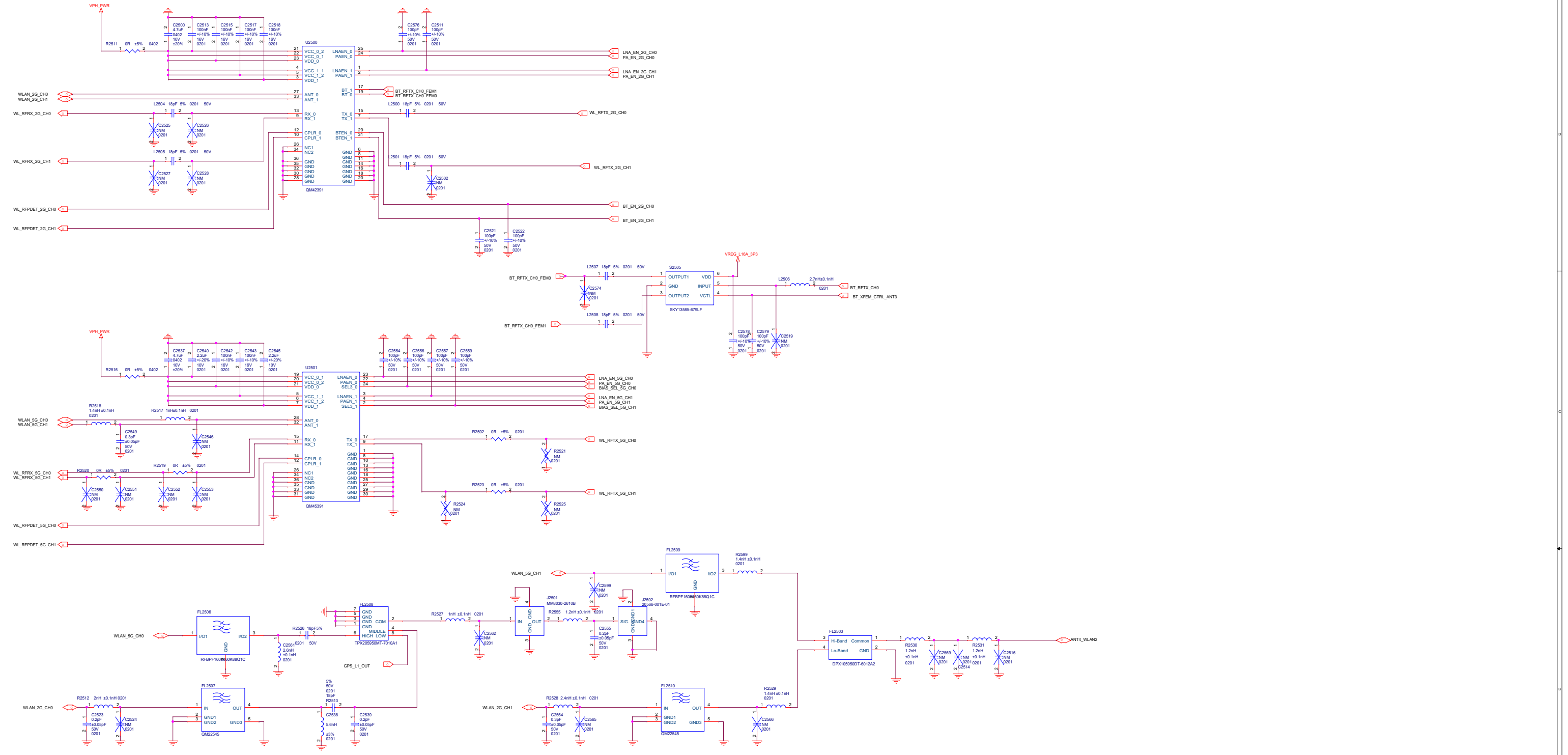
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Size	A3	Document Number	GPS
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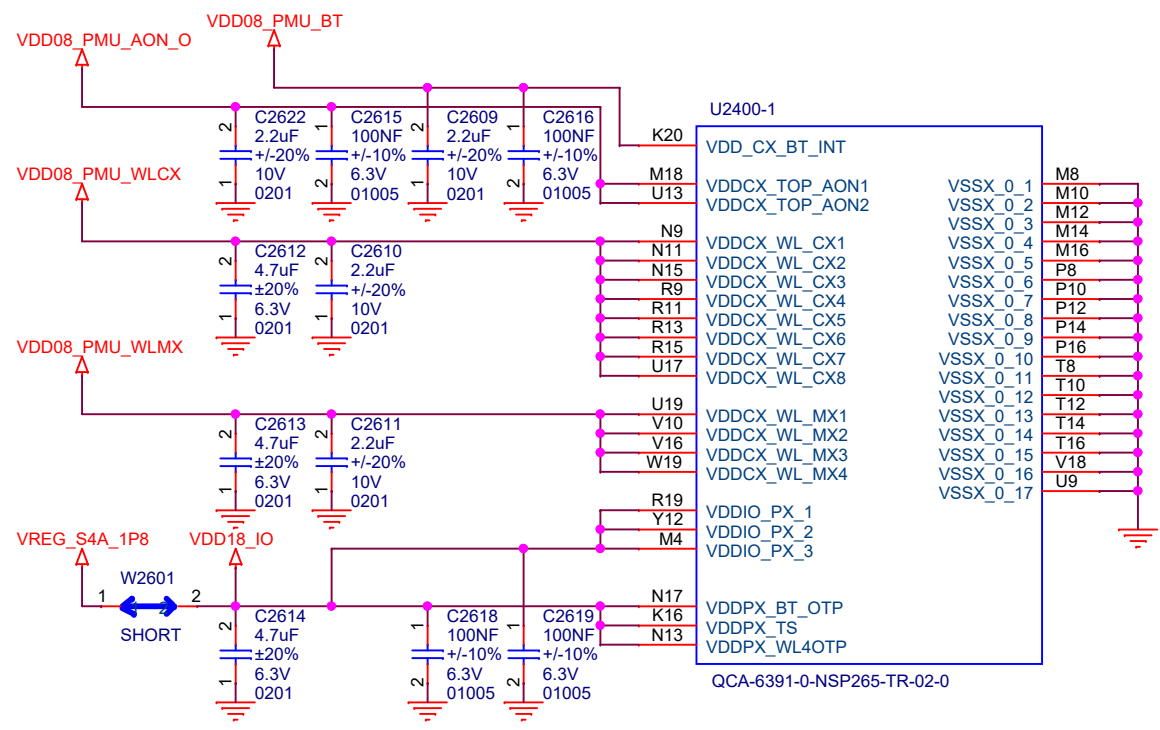
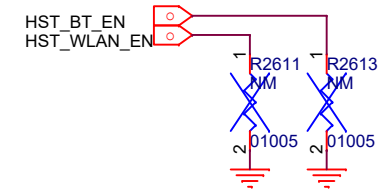
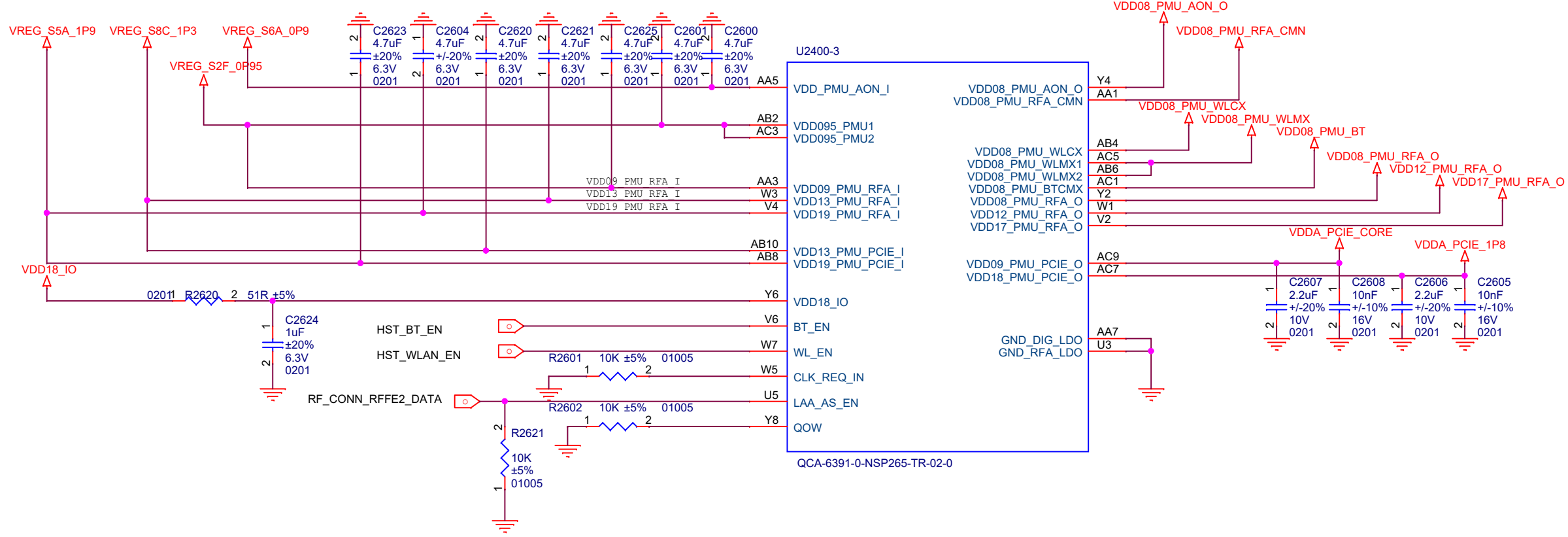
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0	0	48MHZ
0	1	76.8MHZ
1	0	96MHZ
1	1	38.4MHZ

SLM_CH1_CTL1
XO_TXCO_SEL
0: XO
1: TCXO

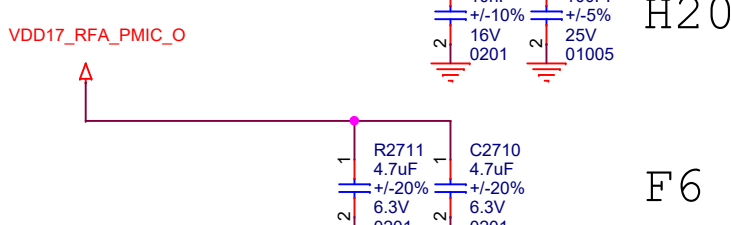
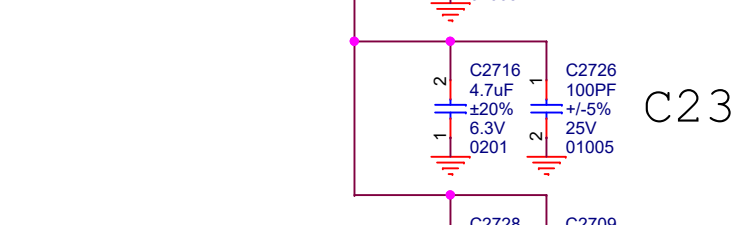
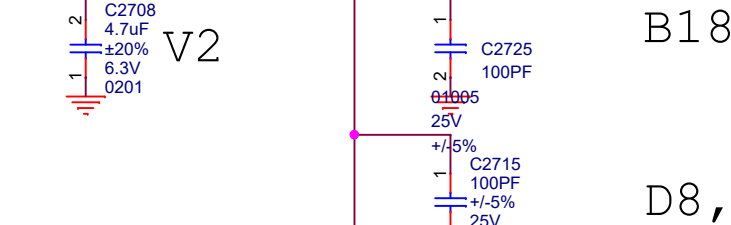
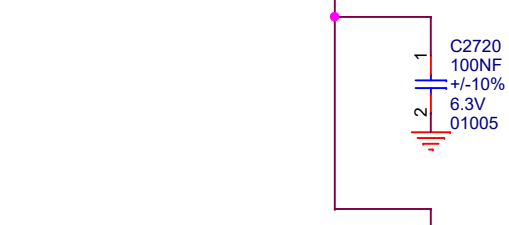
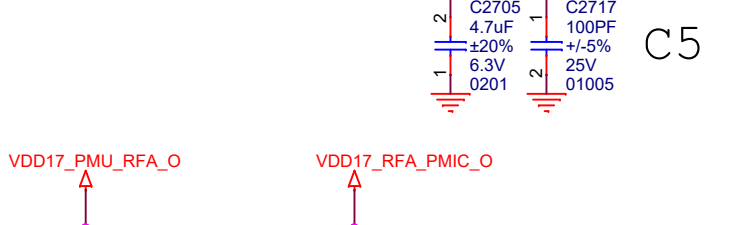
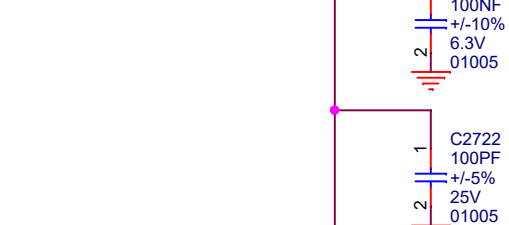
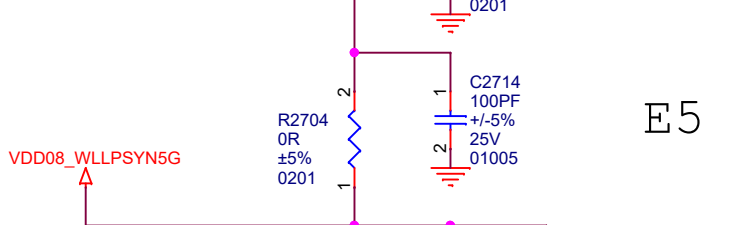
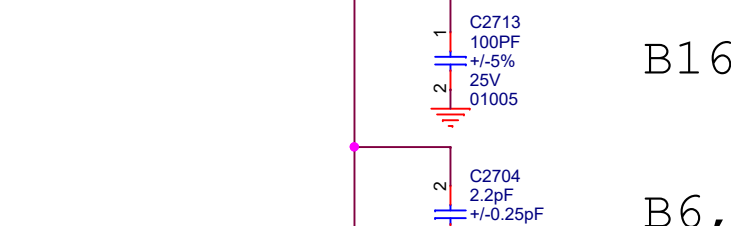
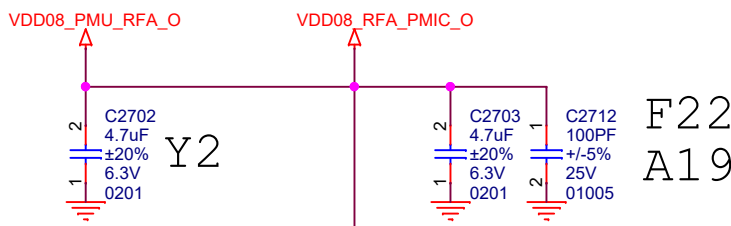
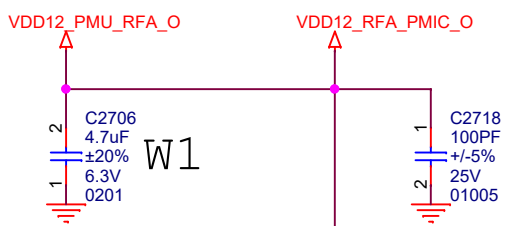
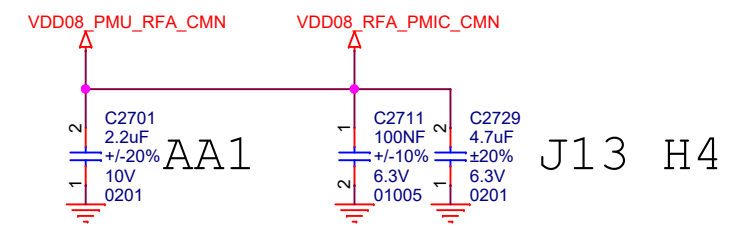




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J11, H16, H12

H8, H2

F16, F12, E15

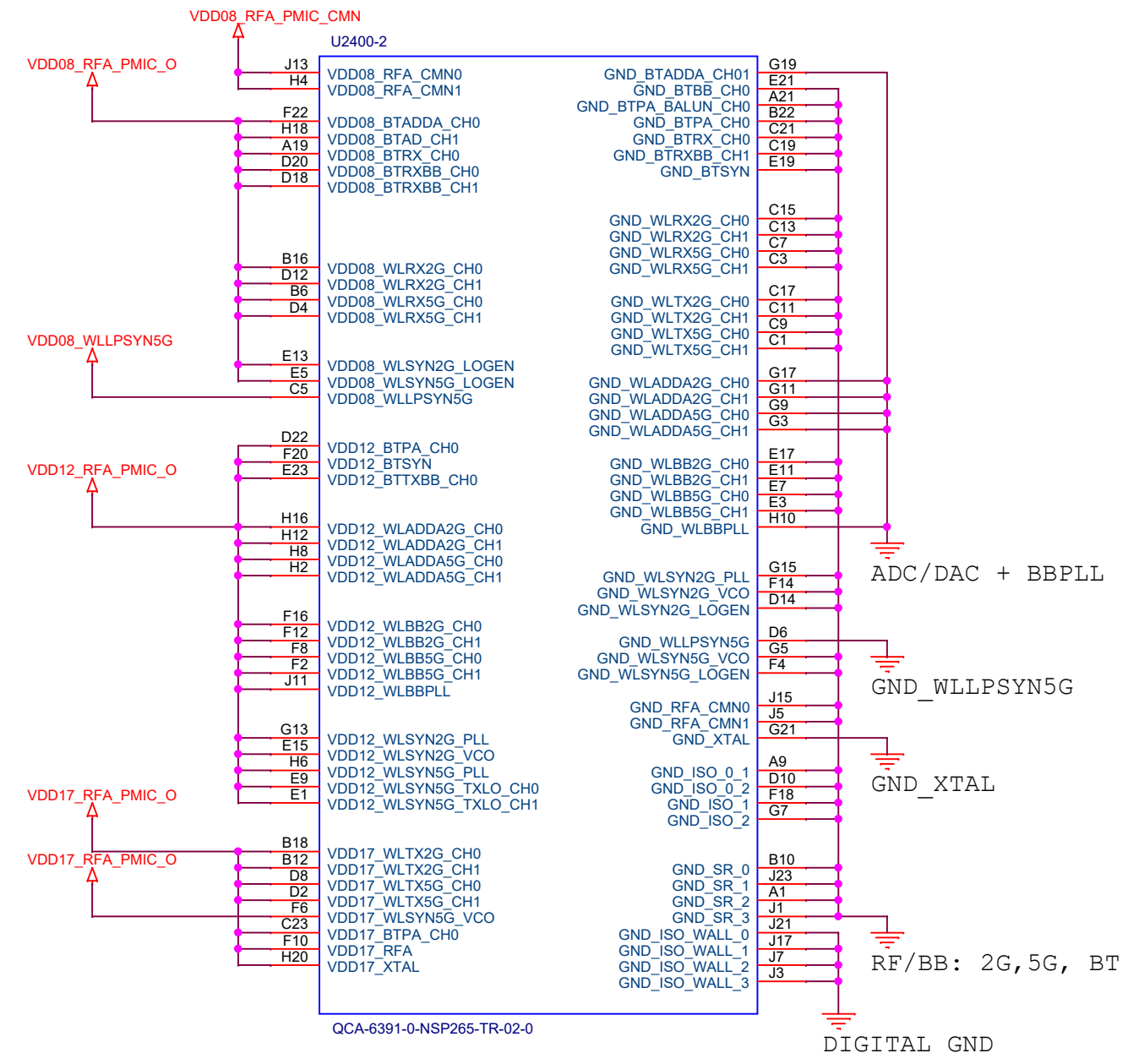
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D22

F20

E23

G13



Title		F1 MAIN	
Size	A3	Document Number	Reserved(for 11ad/11ax)
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Title	
F1 MAIN	
Size	Document Number
A3	WIFI FEM
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F1 MAIN	
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A3	Reserved(for Digital FM)
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F1 MAIN	
Size	Document Number
A3	Reserved(for Analog FM)
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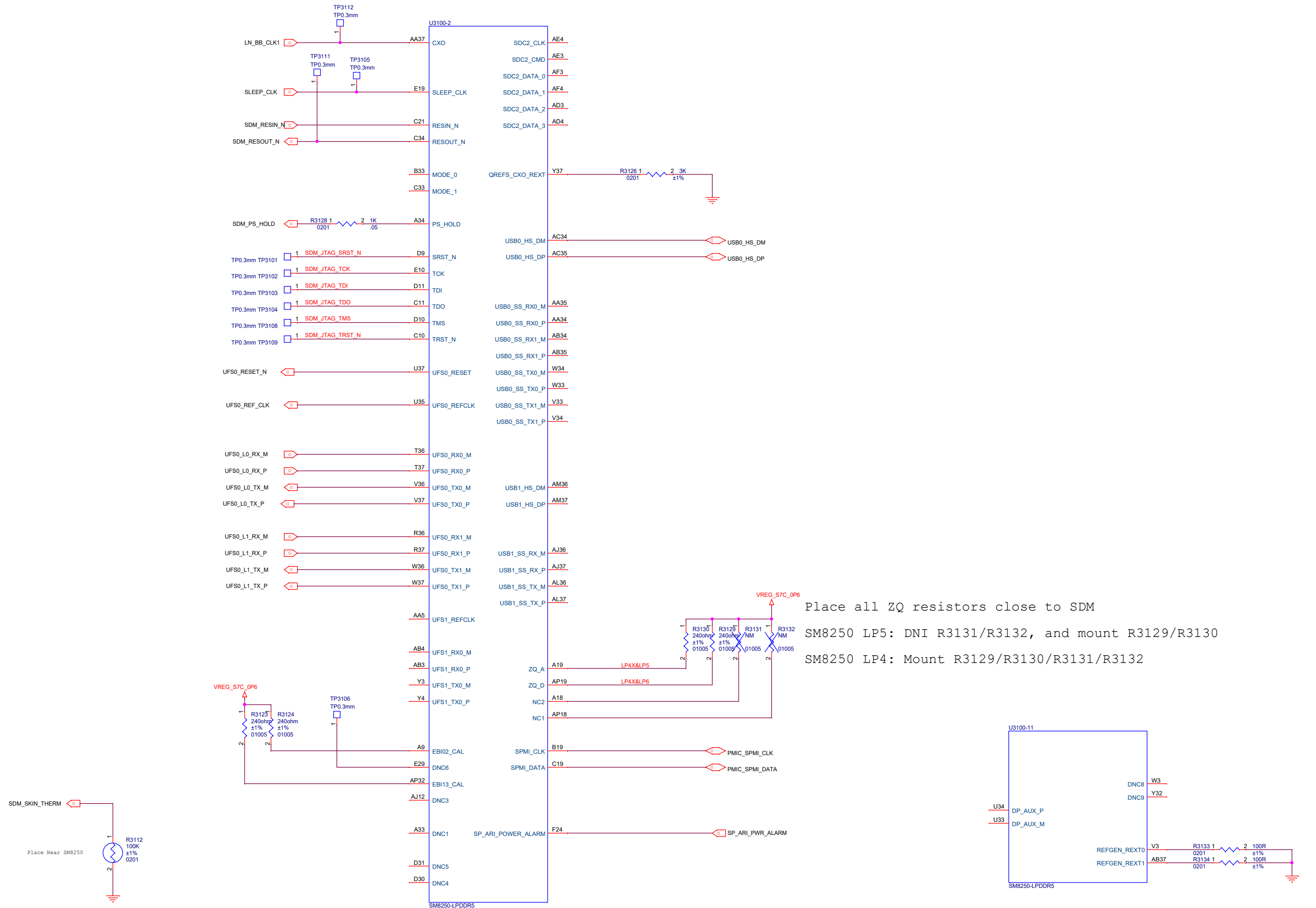
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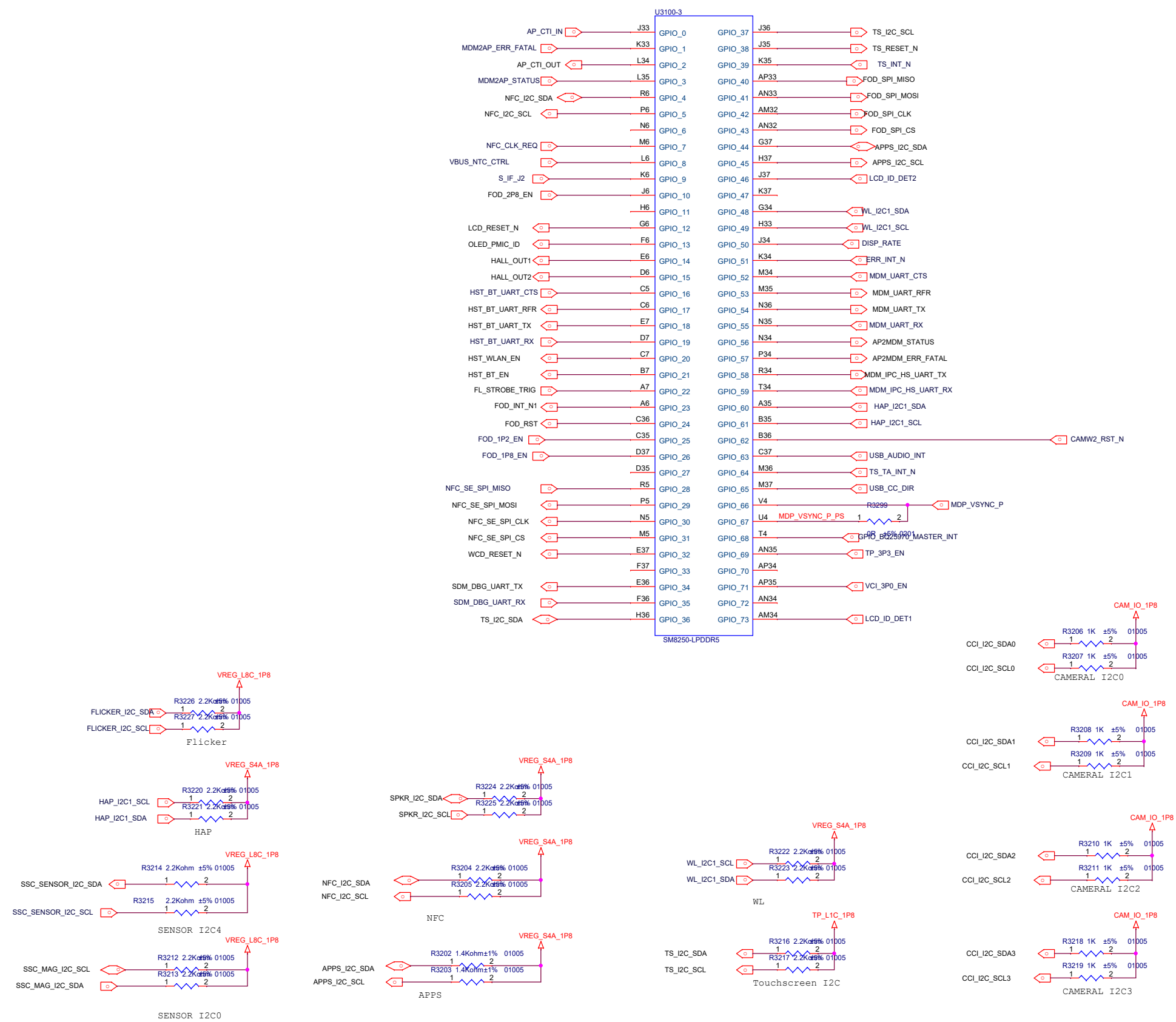
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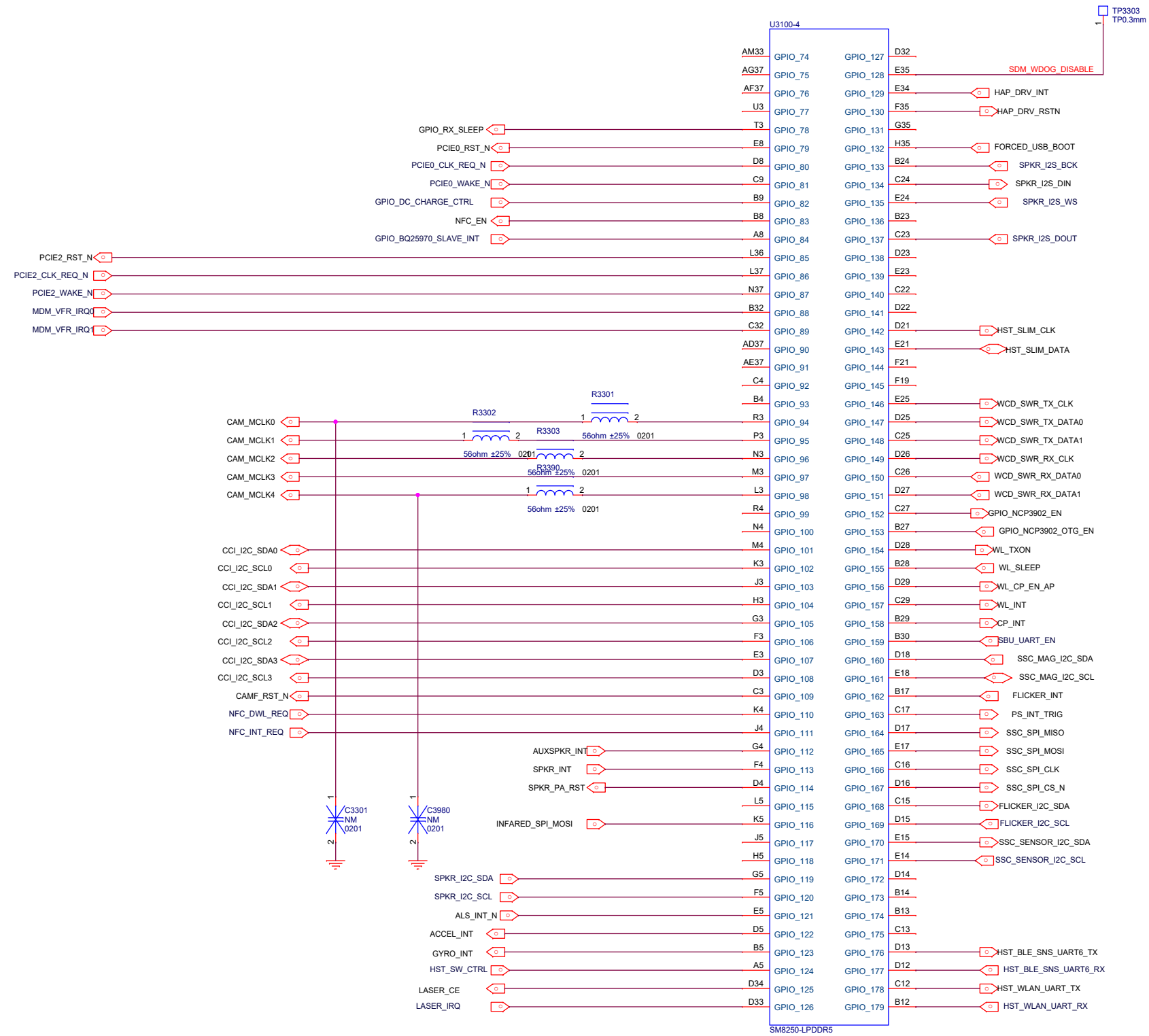
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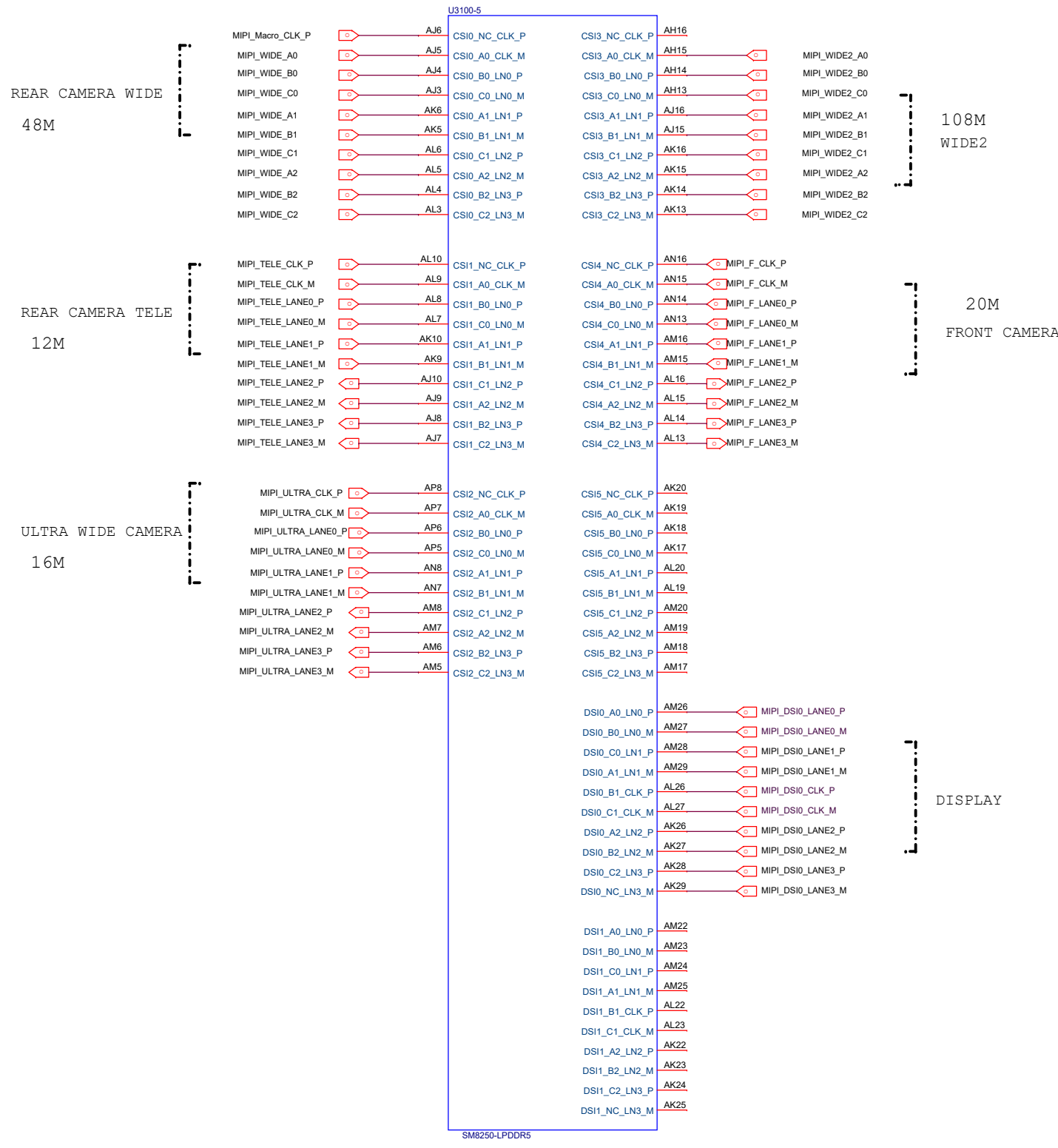
We use current SM8250 symbol as LP5 PKG, and it can be compatible with LP4x PKG



Place all ZQ resistors close to SDM
 SM8250 LP5: DNI R3131/R3132, and mount R3129/R3130
 SM8250 LP4: Mount R3129/R3130/R3131/R3132







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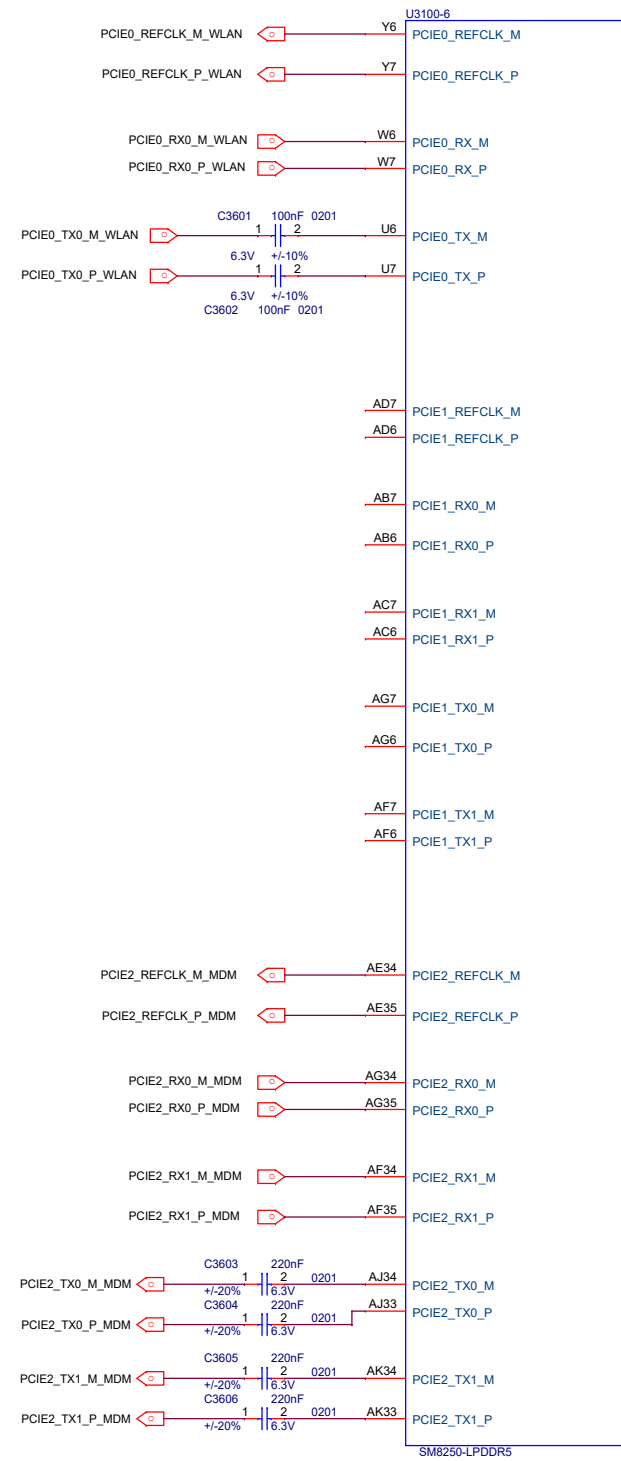
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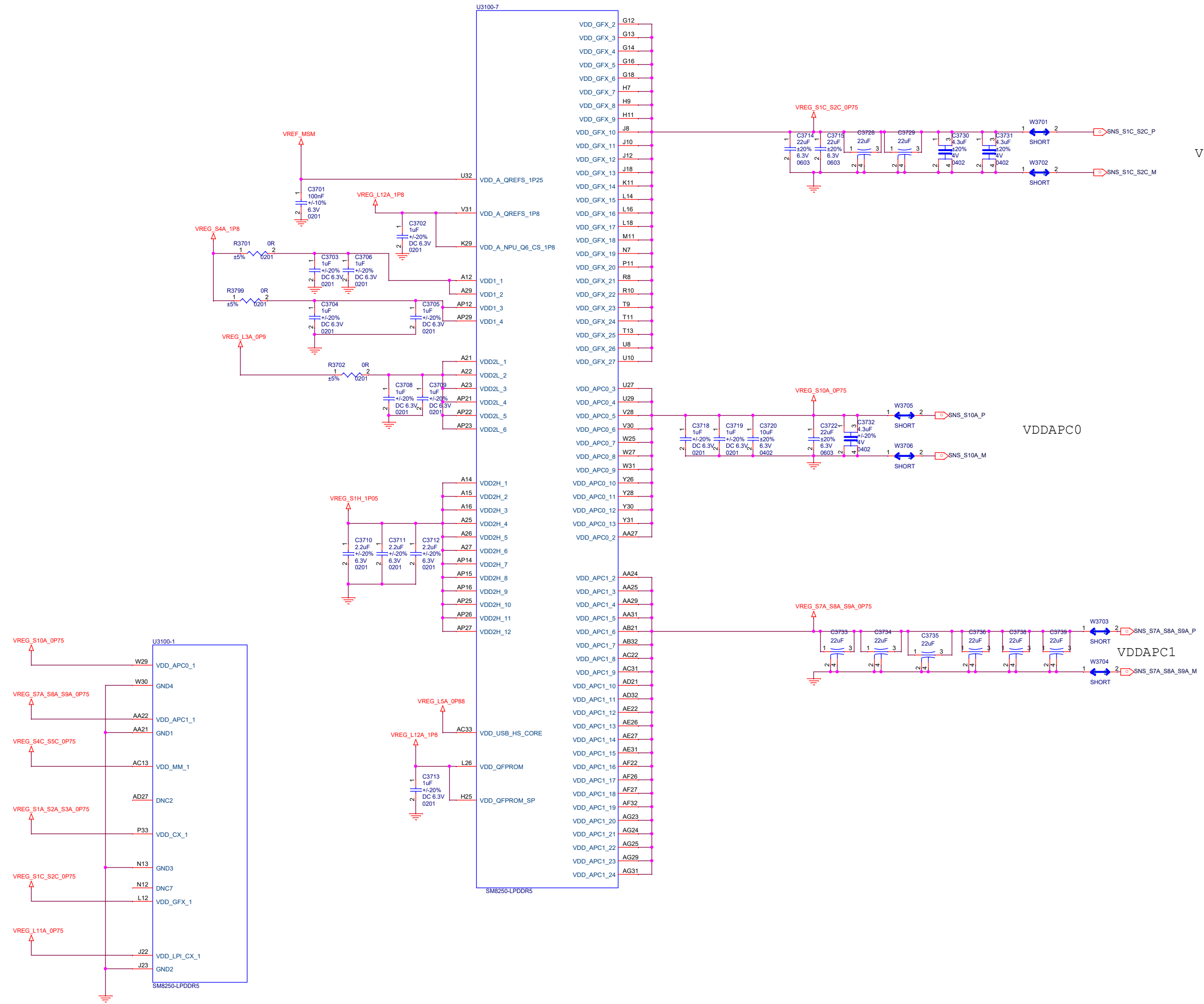
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Size	Document Number
A3	Reserved(for MIPI)
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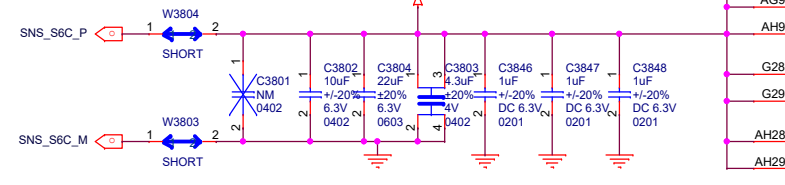
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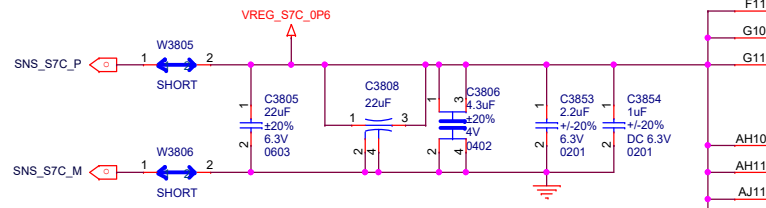
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Date:	Friday, November 29, 2019
Sheet	1

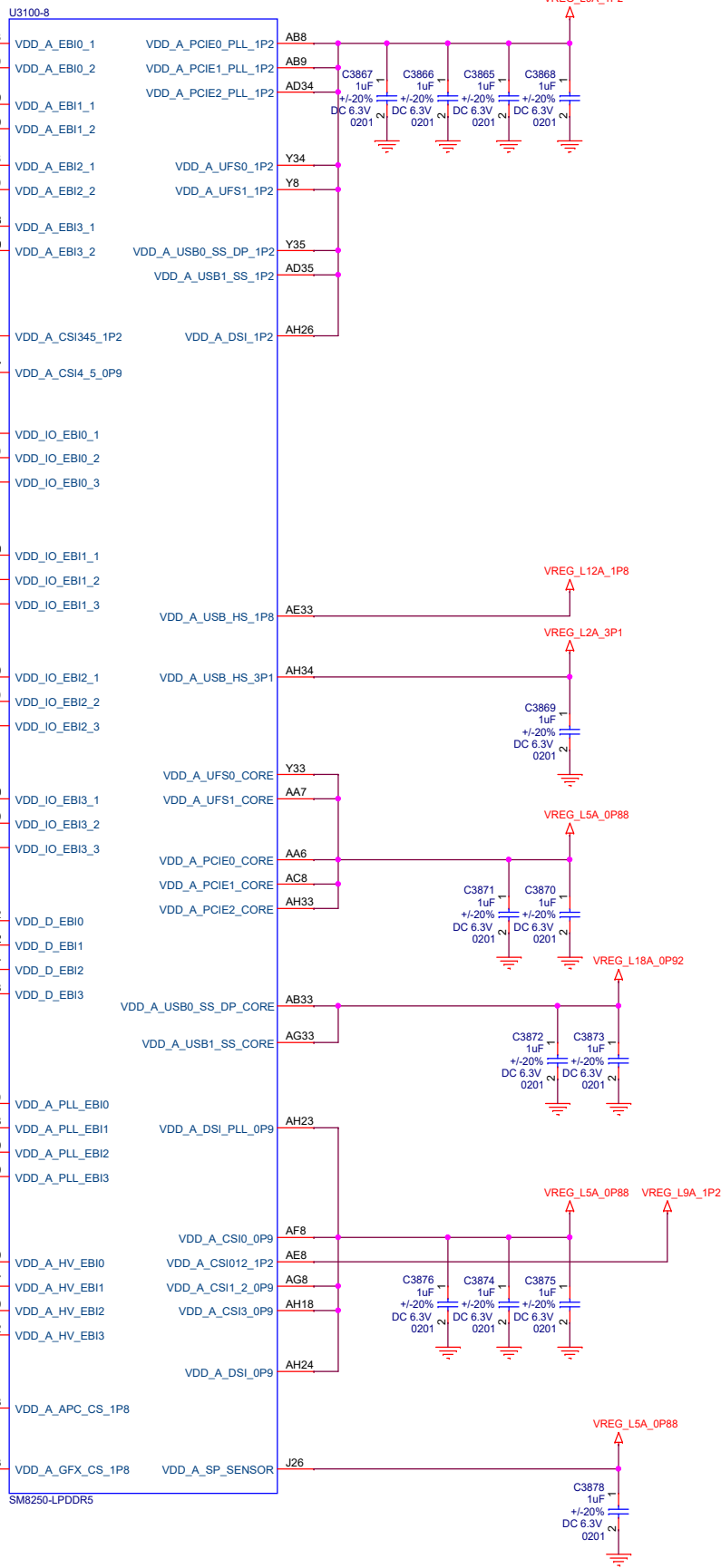
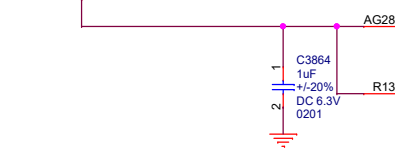
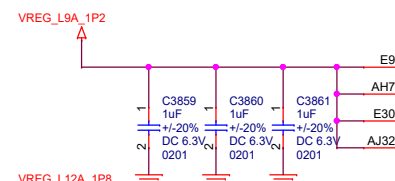
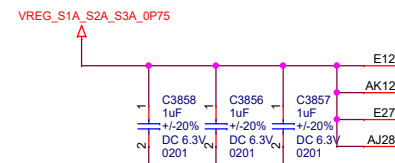
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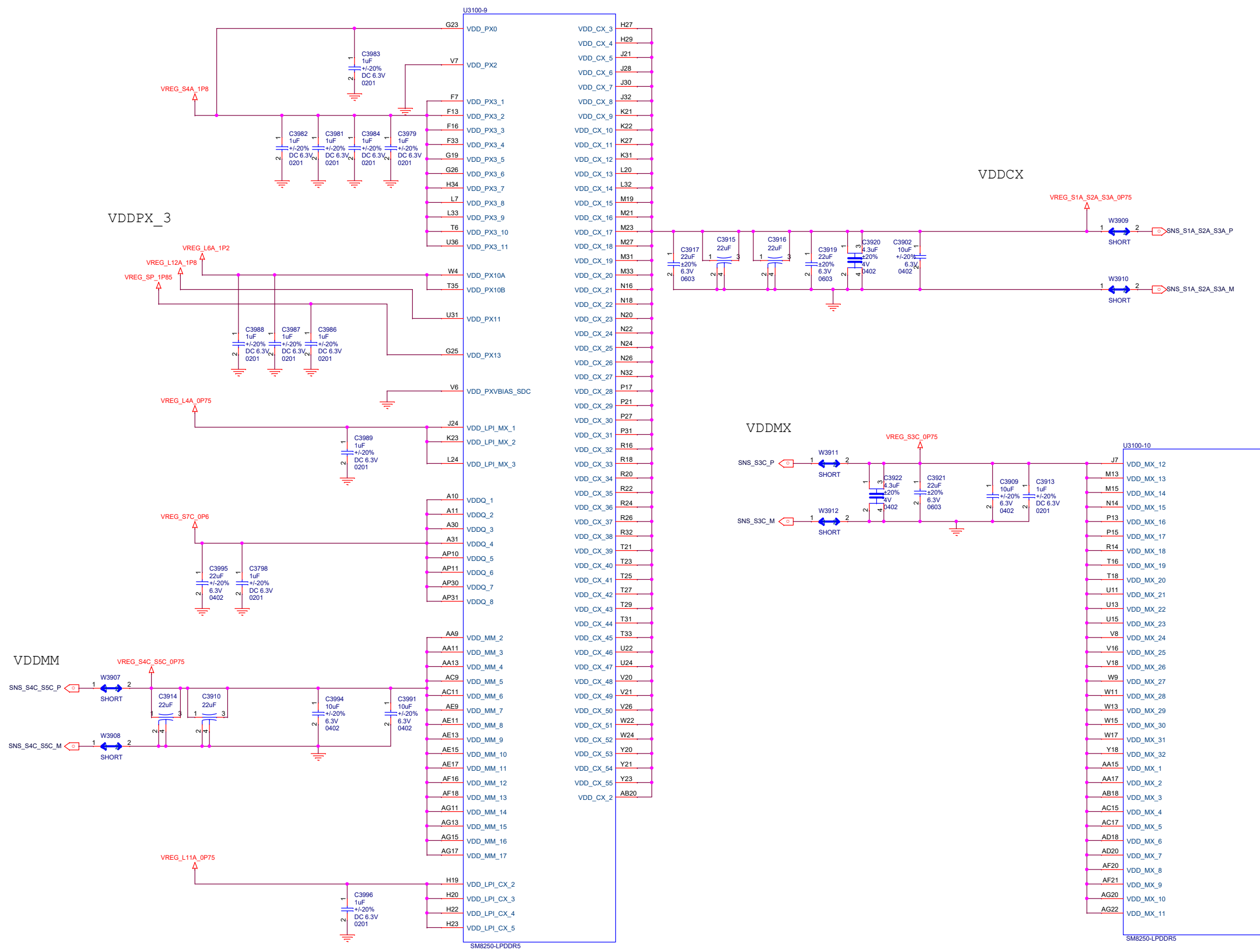


VDDQ/VDDIO_EBI



Share caps with VDDCX





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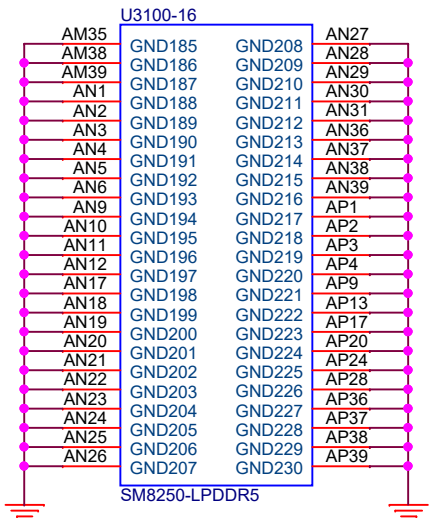
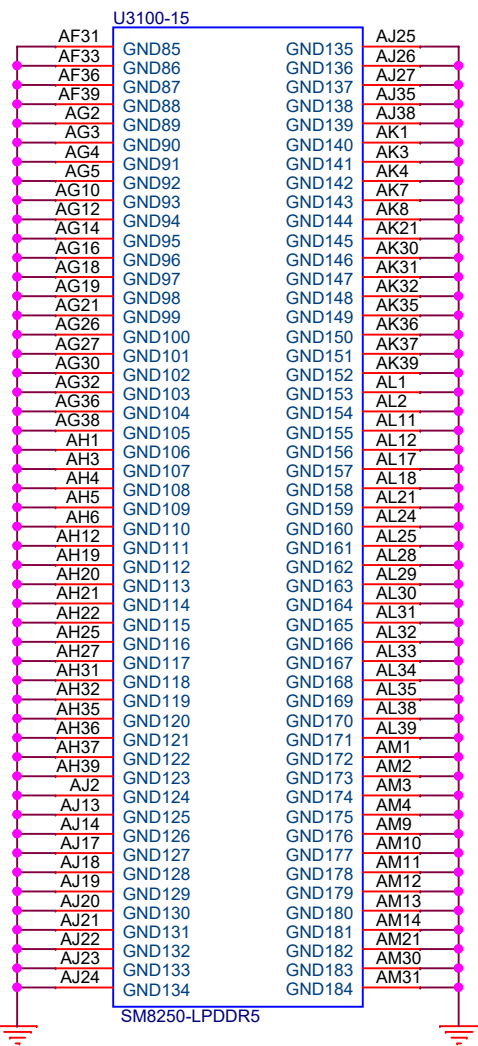
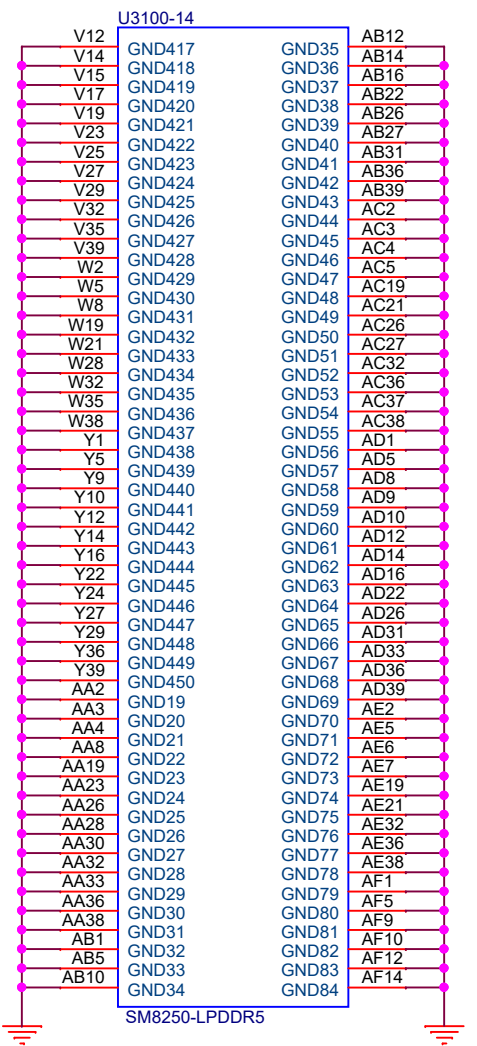
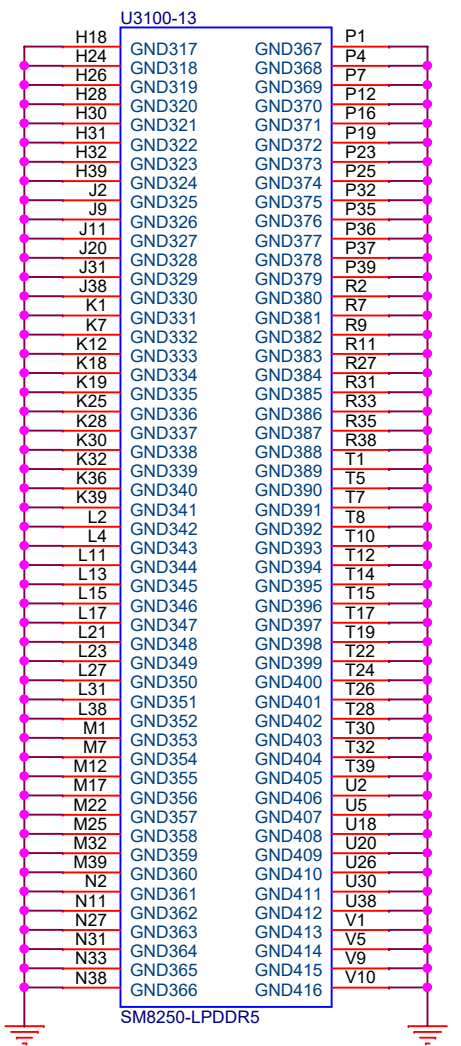
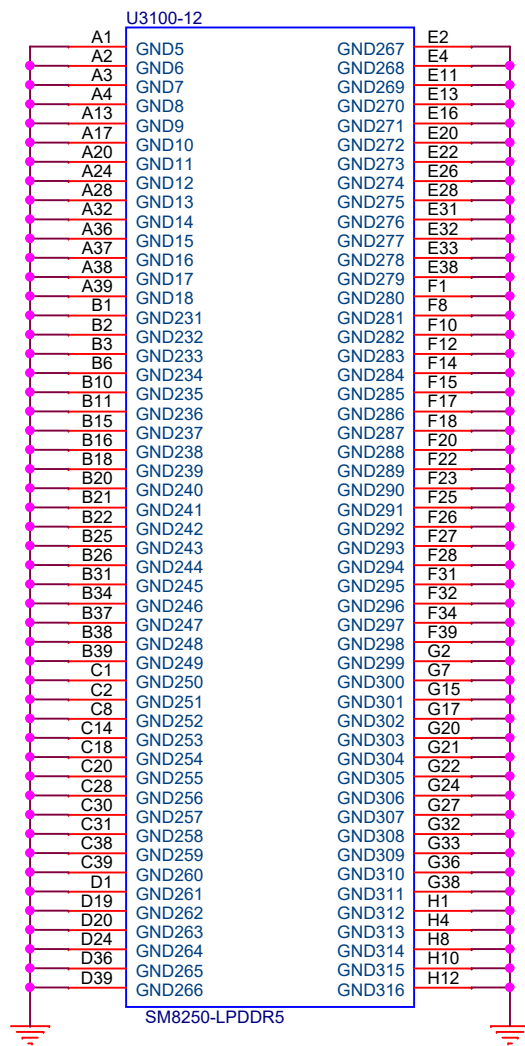
B

B

A

A

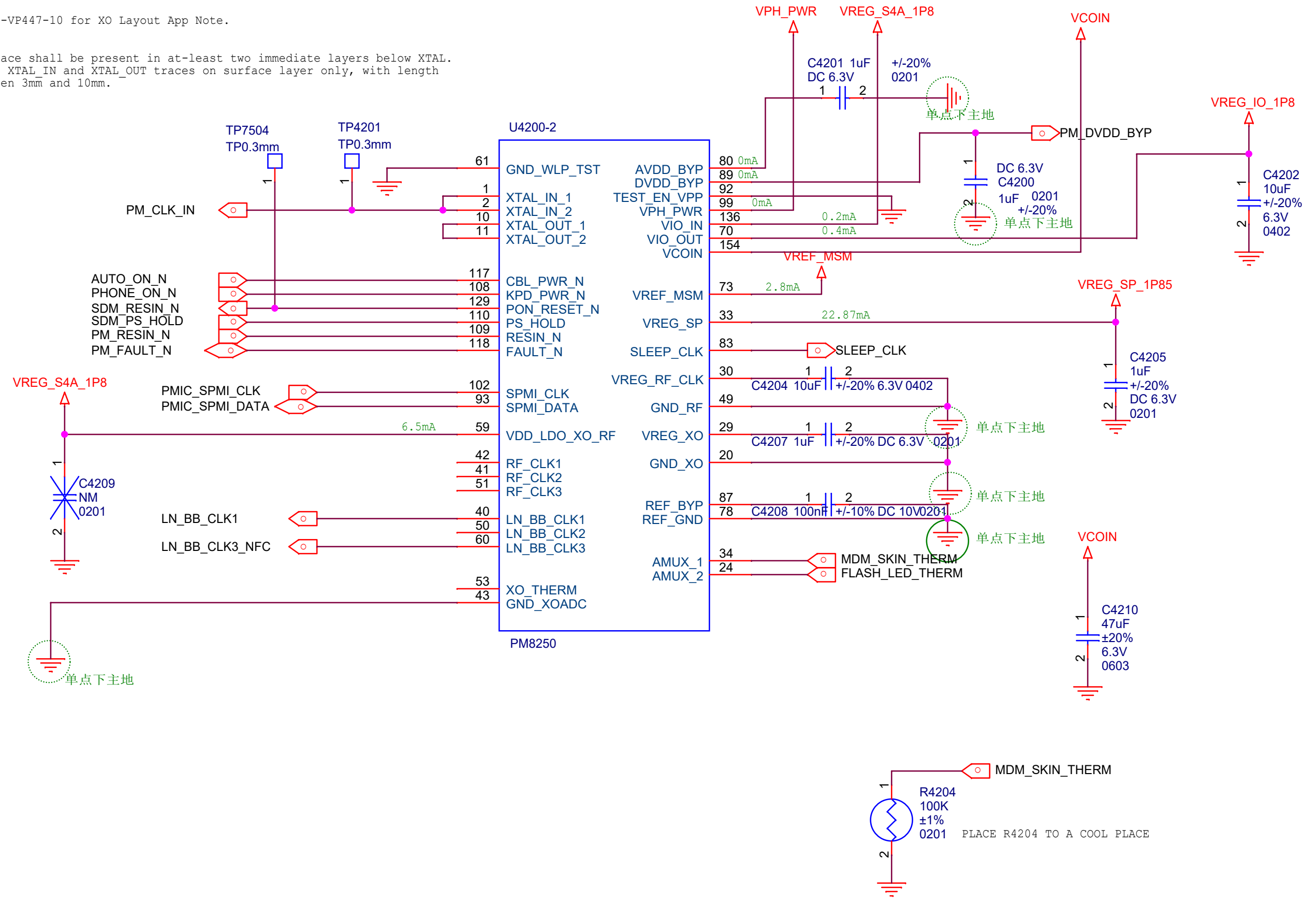
Title		F1 MAIN	
Size	A3	Document Number	SDM855 PWR4
Date:	Friday, November 29, 2019	Sheet	41
			74



Note: Refer to 80-VP447-10 for XO Layout App Note.

Layout Note:

No trace shall be present in at-least two immediate layers below XTAL.
Route XTAL_IN and XTAL_OUT traces on surface layer only, with length between 3mm and 10mm.



Title		F1 MAIN	
Size	A4	Document Number	PM855 XO&CTRL
Date:	Friday, November 29, 2019	Sheet	43 / 74

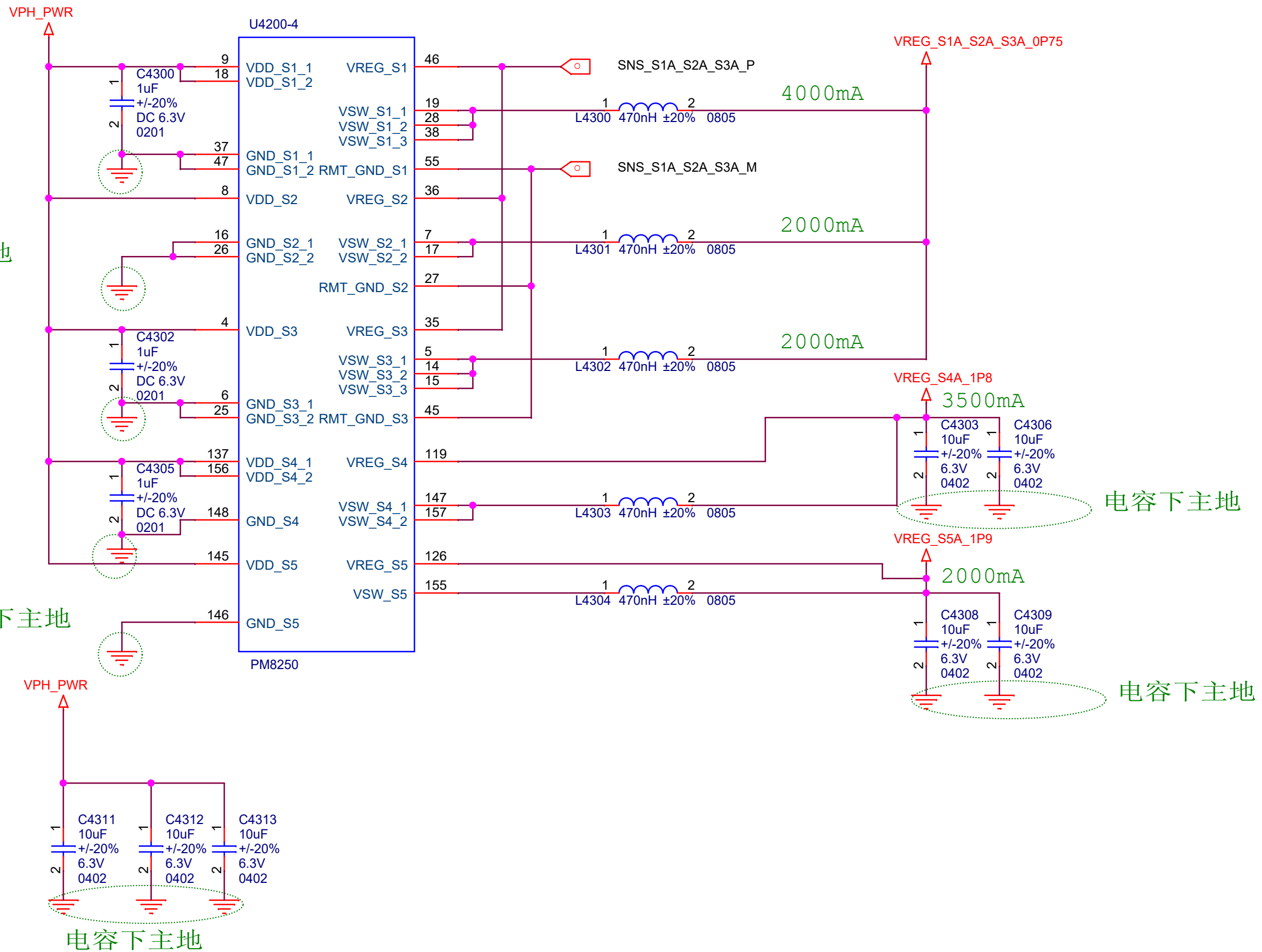
电容下主地

电容下主地

电容下主地

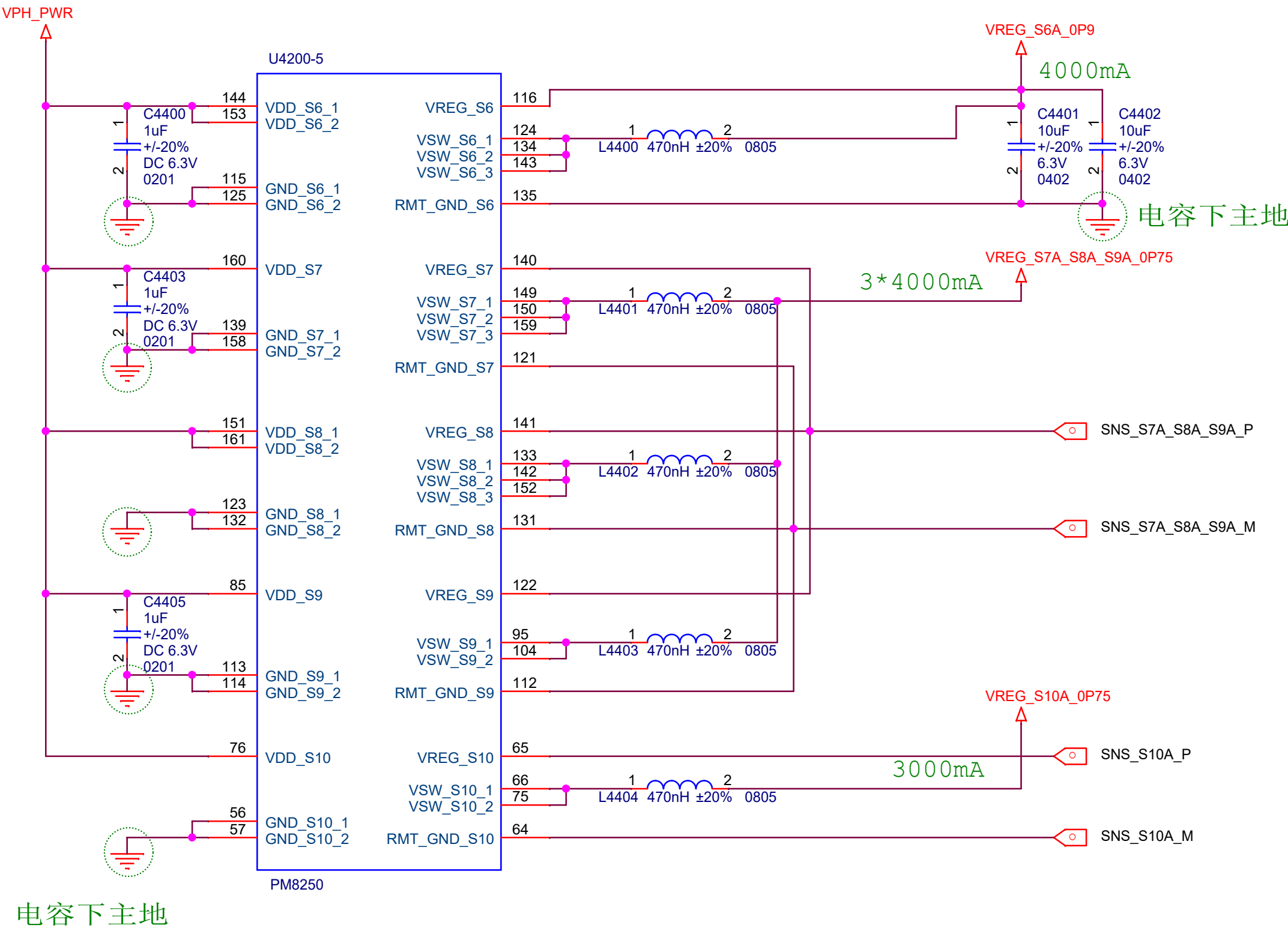
电容下主地

电容下主地



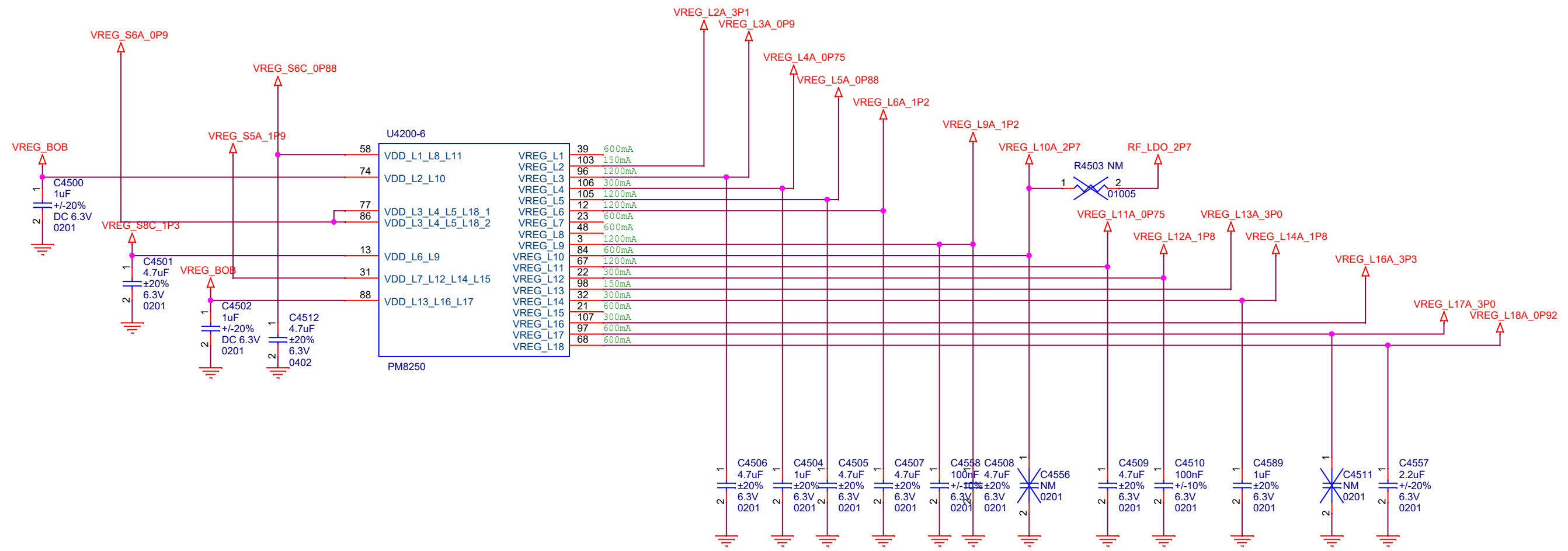
Title		F1 MAIN	
Size	Document Number	PM855 BUCK CONVERTER1	
A4			
Date:	Friday, November 29, 2019	Sheet	44

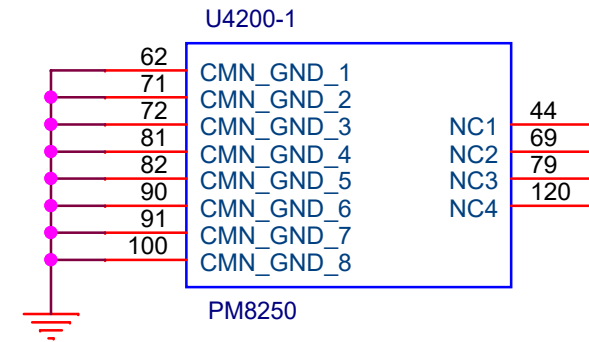
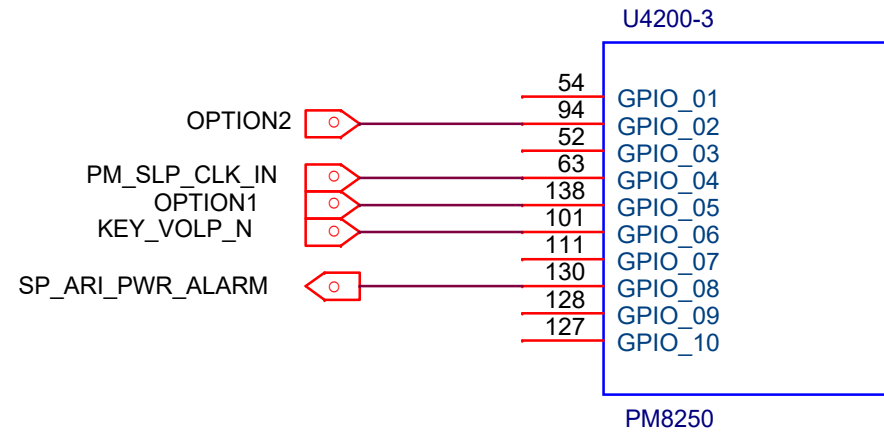
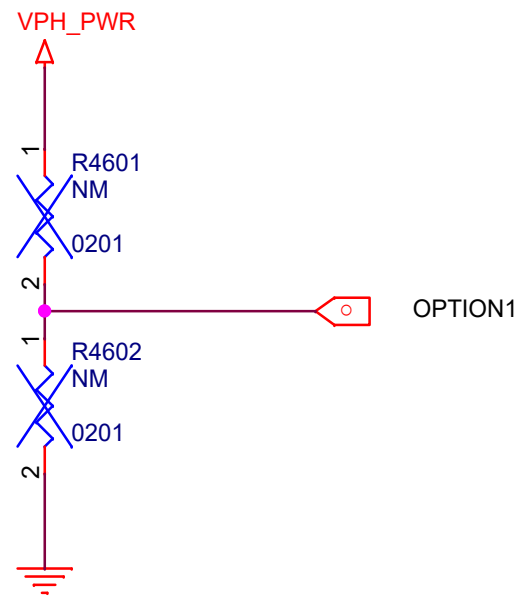
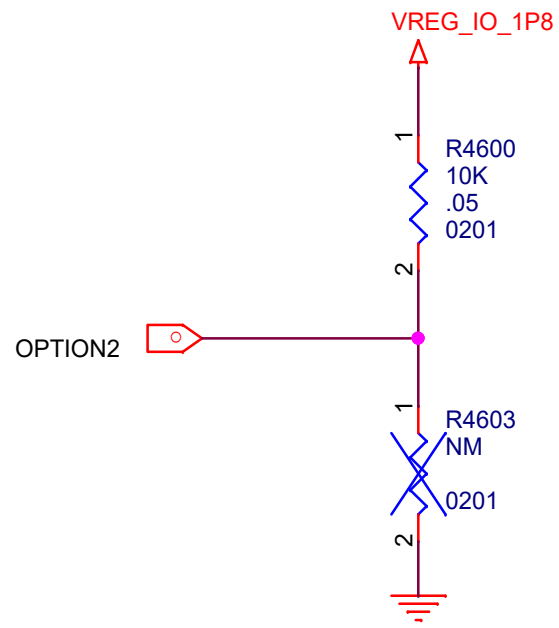
电容下主地



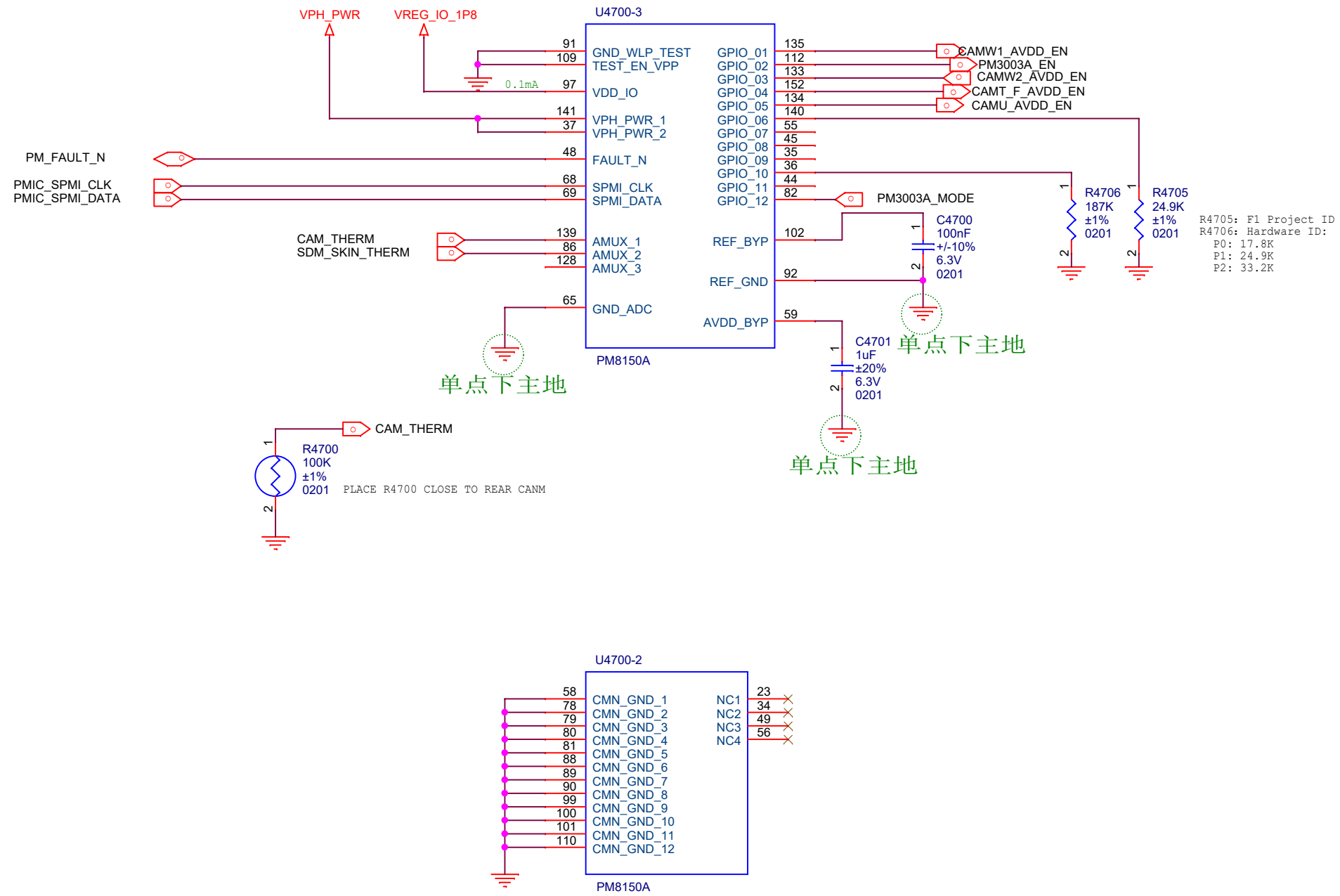
电容下主地

Title		F1 MAIN	
Size	A4	Document Number	PM855 BUCK CONVERTER2
Date:	Friday, November 29, 2019	Sheet	

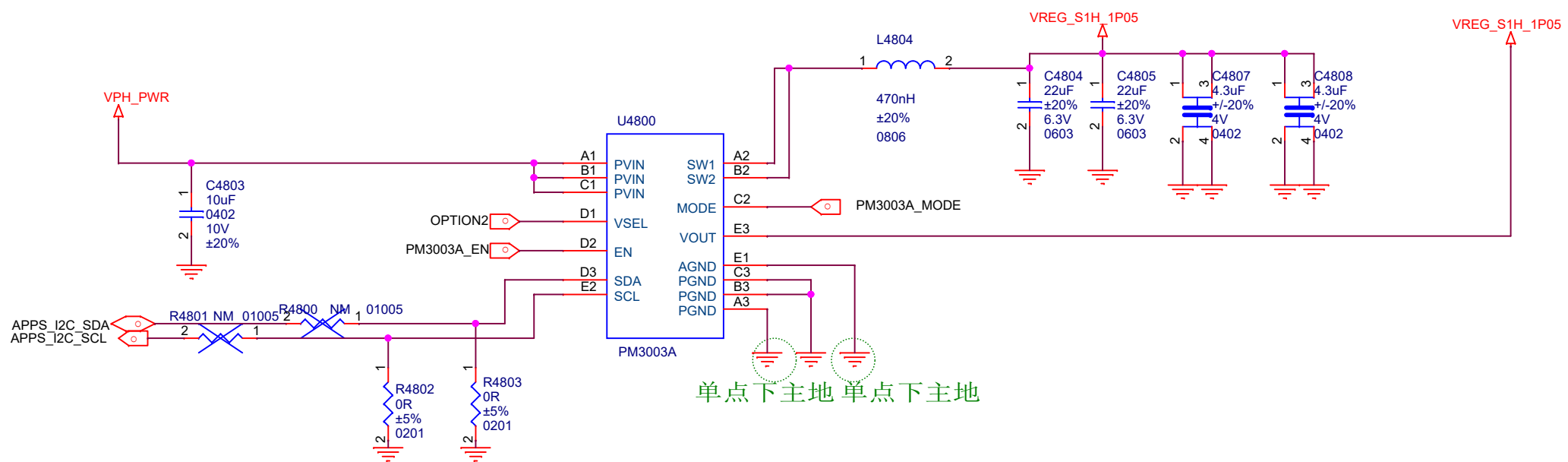
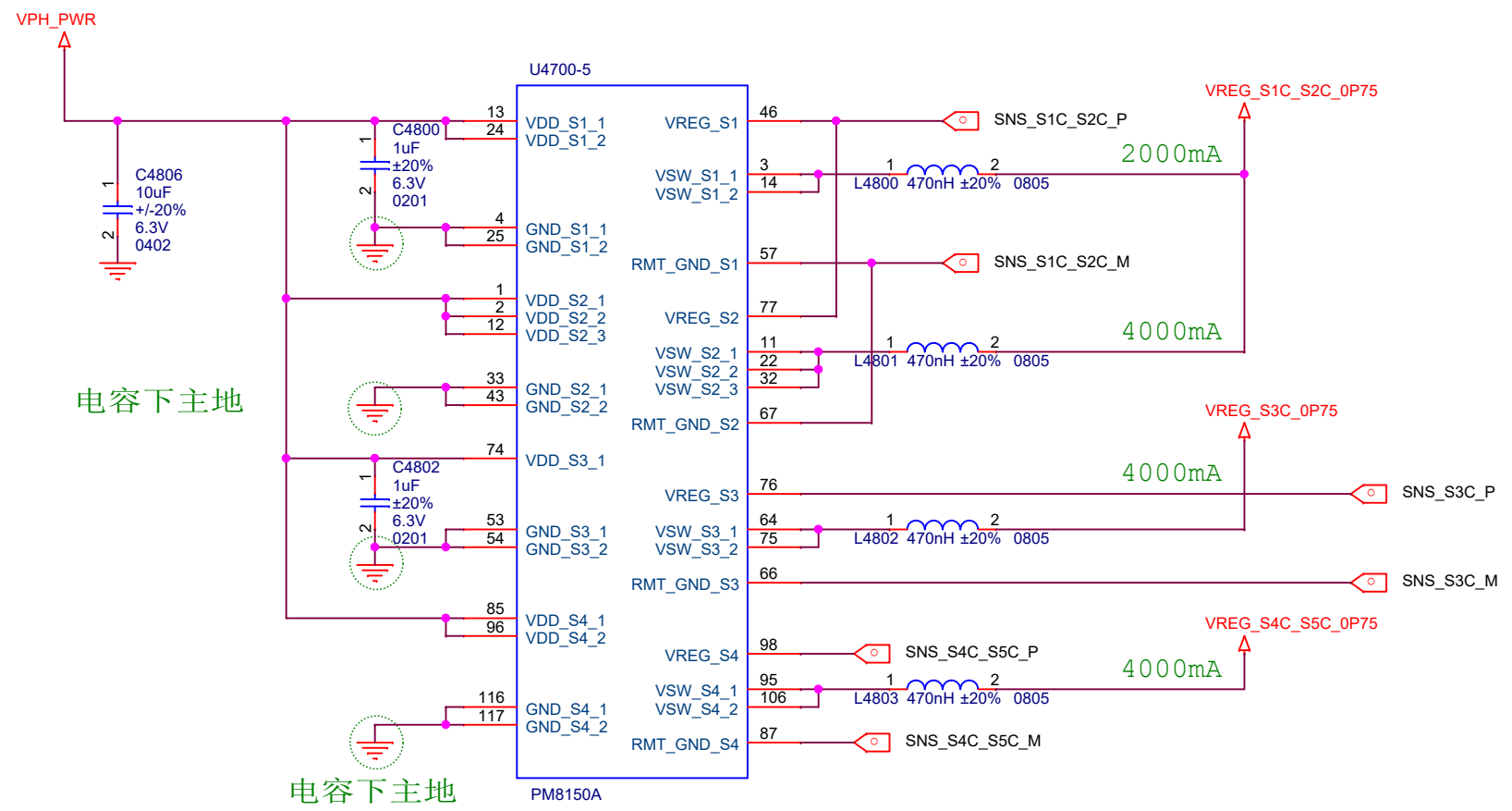




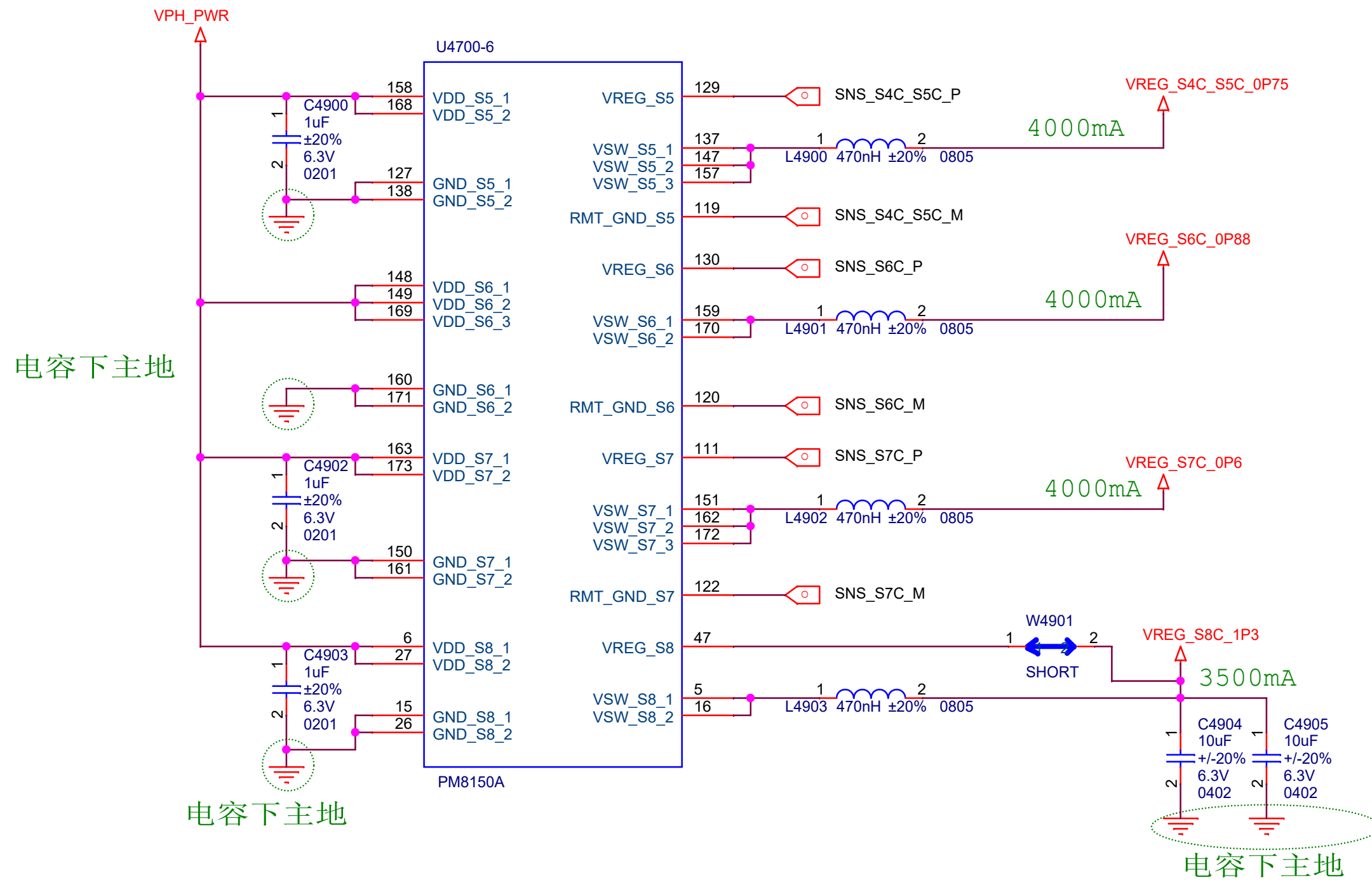
Title		F1 MAIN	
Size	A4	Document Number	PM855 GPIO&GND
Date:	Friday, November 29, 2019	Sheet	47 / 74



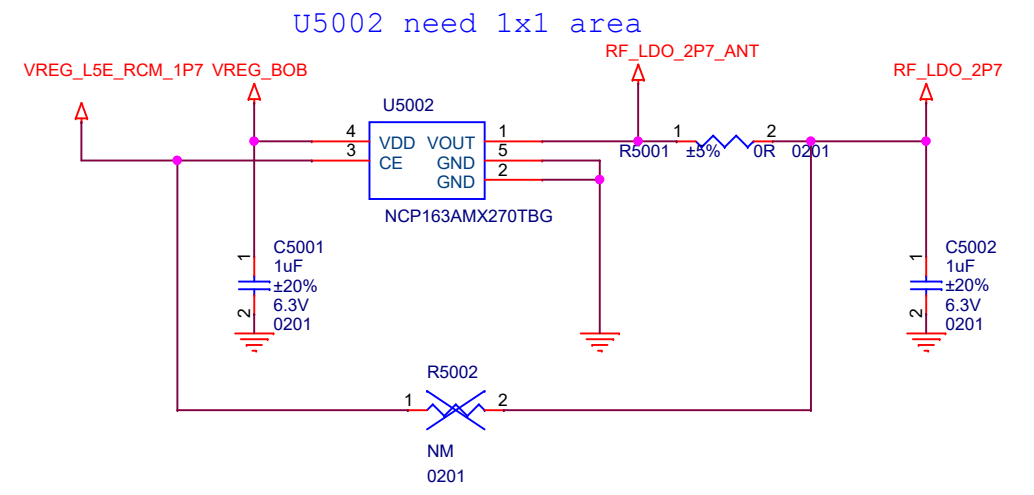
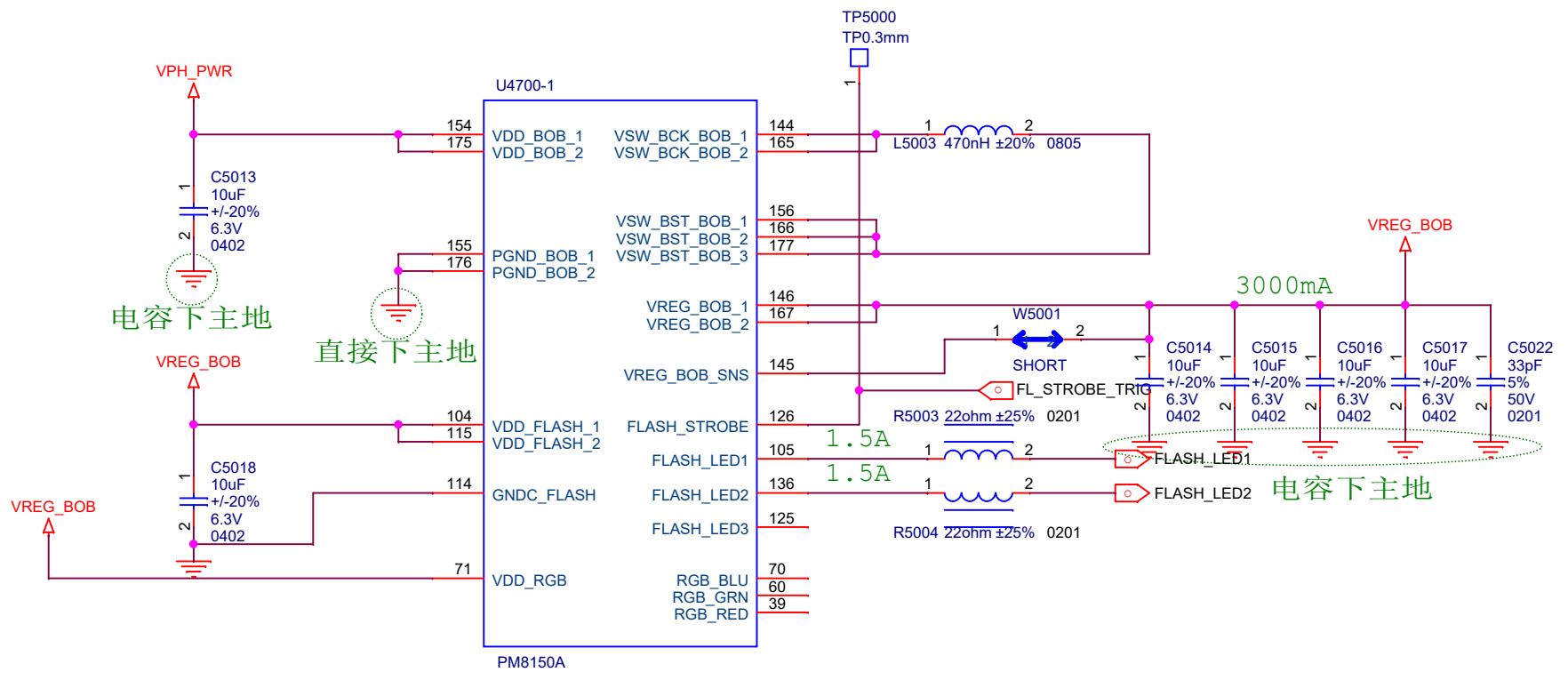
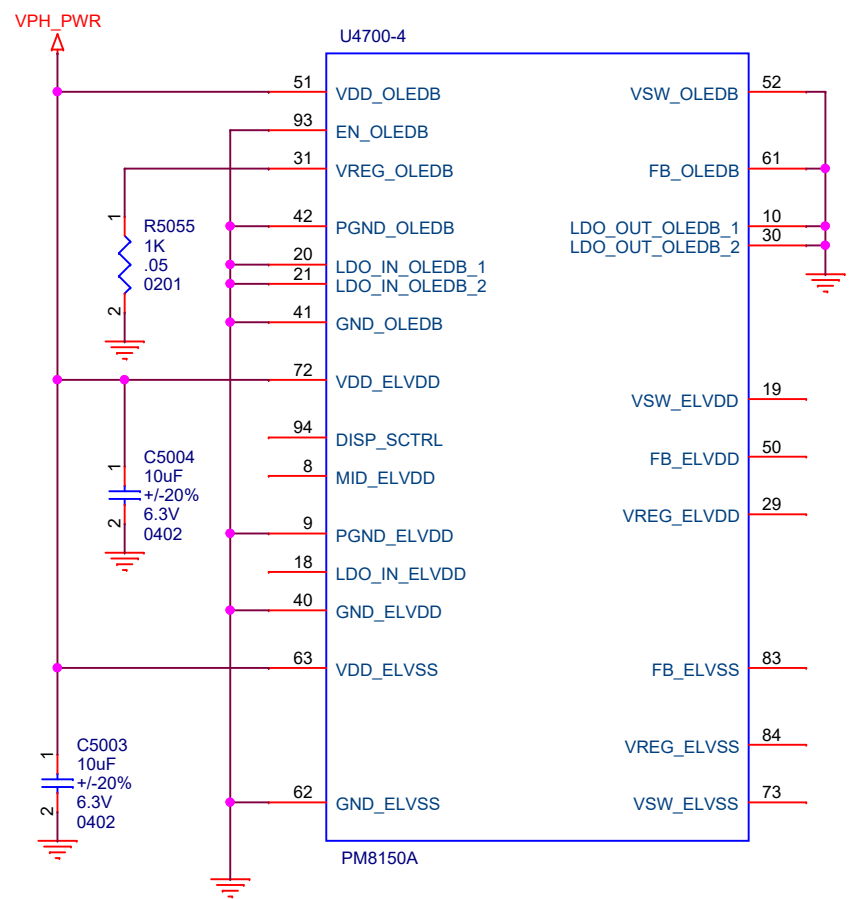
Title		F1 MAIN	
Size	A3	Document Number	PM855A CTRL&GND
Date:	Friday, November 29, 2019	Sheet	48
			74



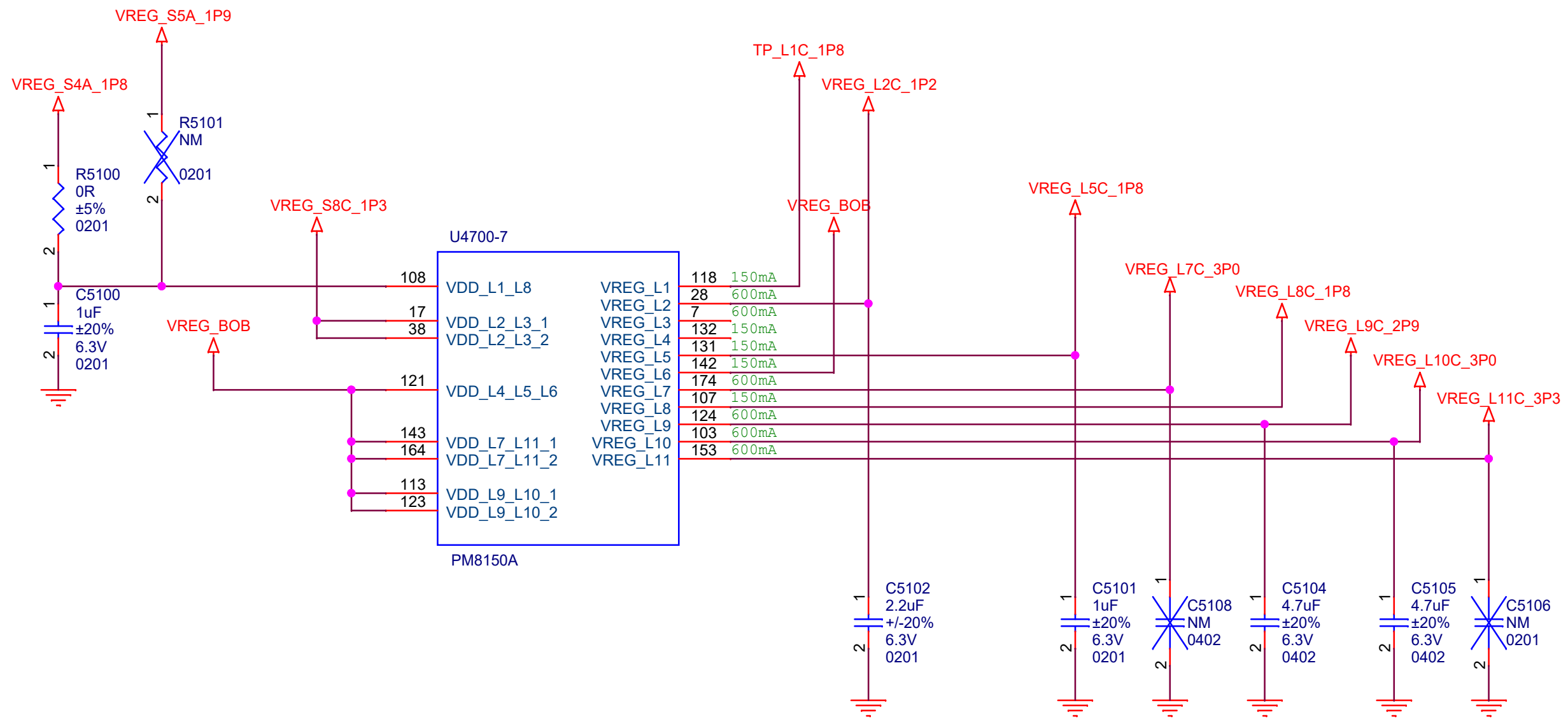
Title		F1 MAIN	
Size	A3	Document Number	PM855A BUCK CONVERTER1
Date:	Friday, November 29, 2019	Sheet	49
			74



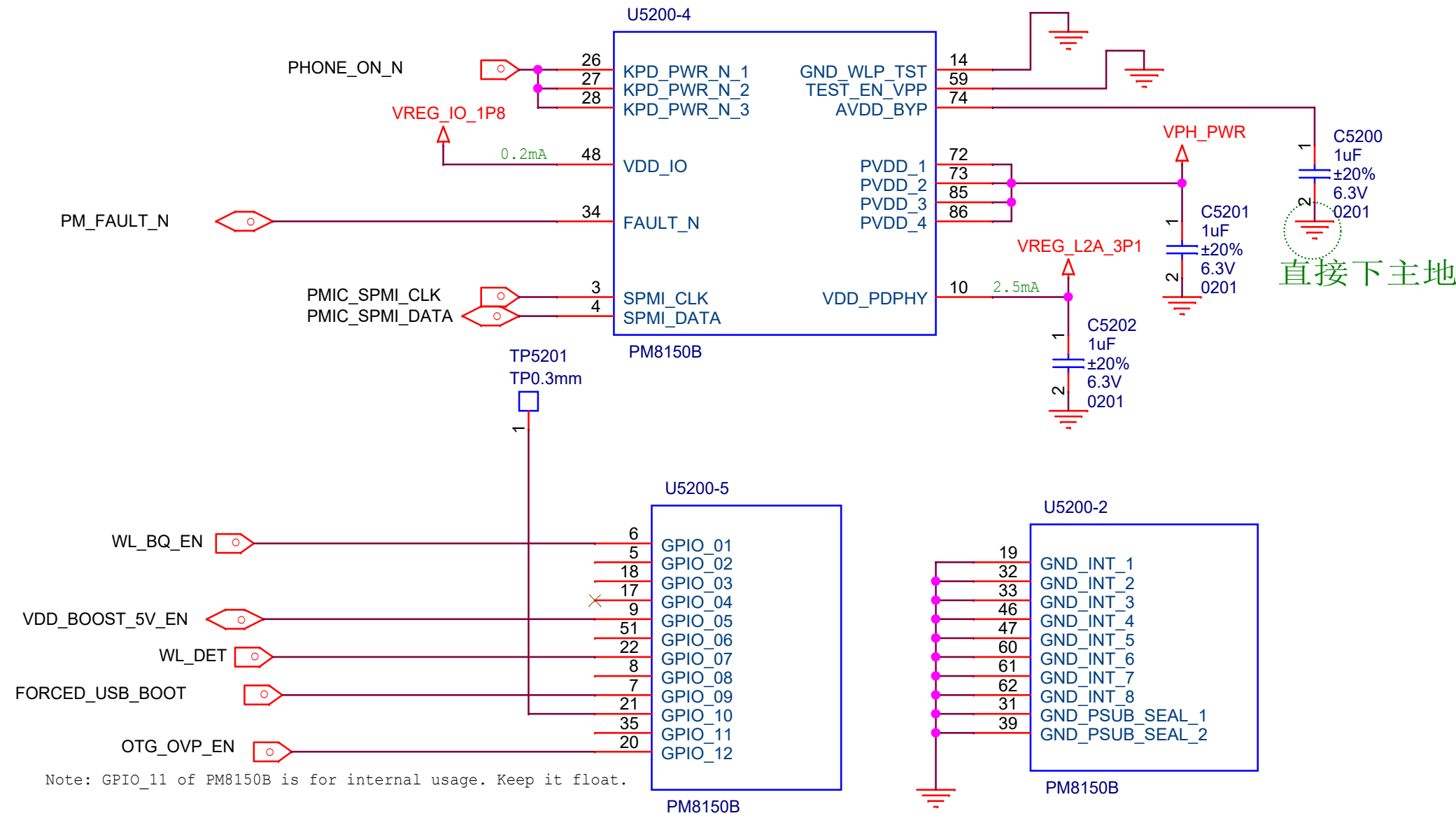
Title		F1 MAIN	
Size	A4	Document Number	PM855A BUCK CONVERTER2
Date:	Friday, November 29, 2019	Sheet	1



Title		F1 MAIN
Size	Document Number	PM855A AMOLED&BOB&FLASH
A3	Date:	Friday, November 29, 2019
Sheet		1

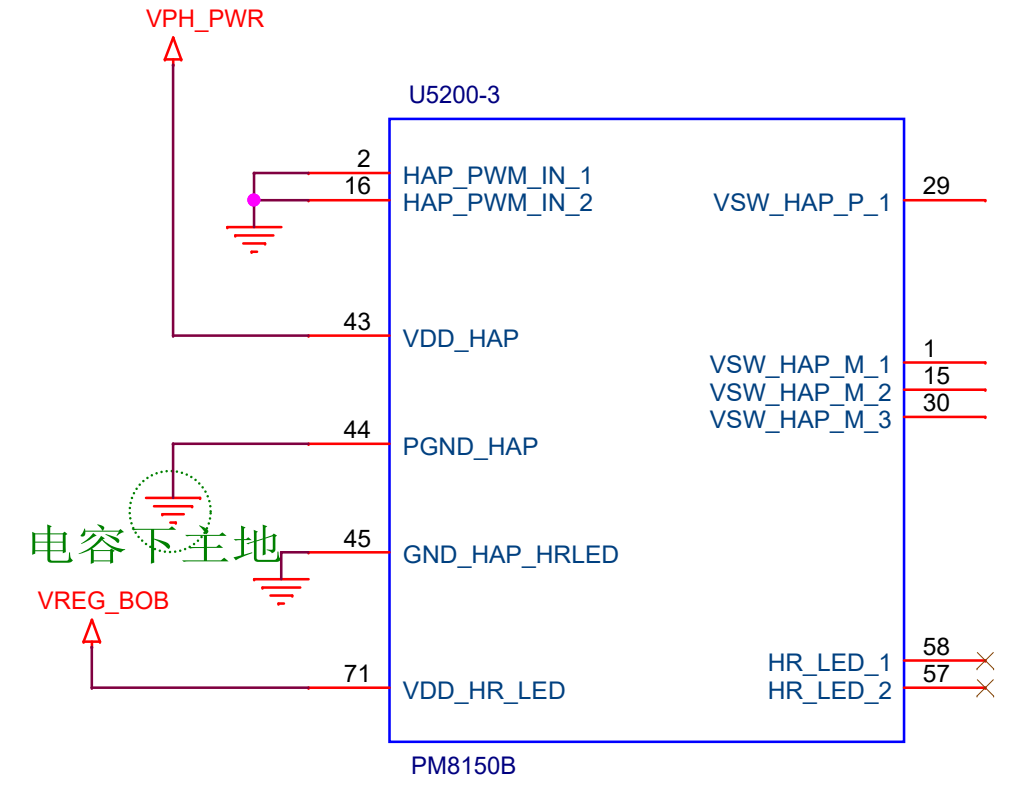
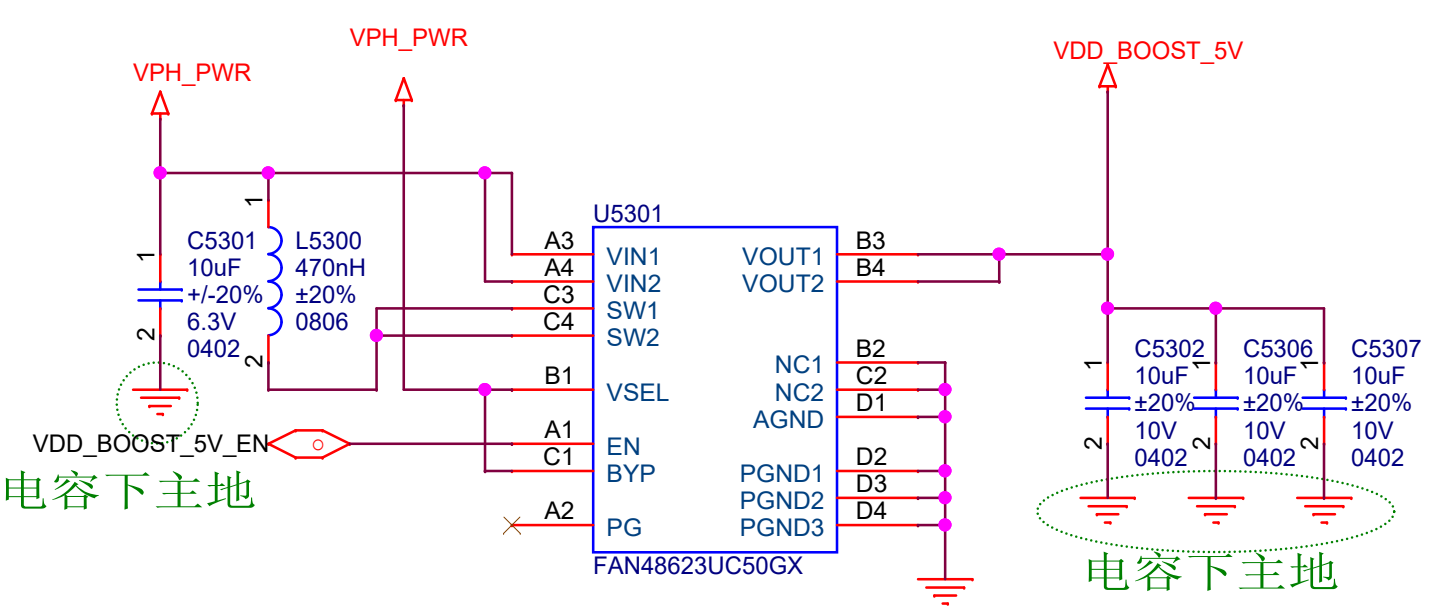


Title		F1 MAIN	
Size	A4	Document Number	PM855A LDOs
Date:	Friday, November 29, 2019	Sheet	52 of 74

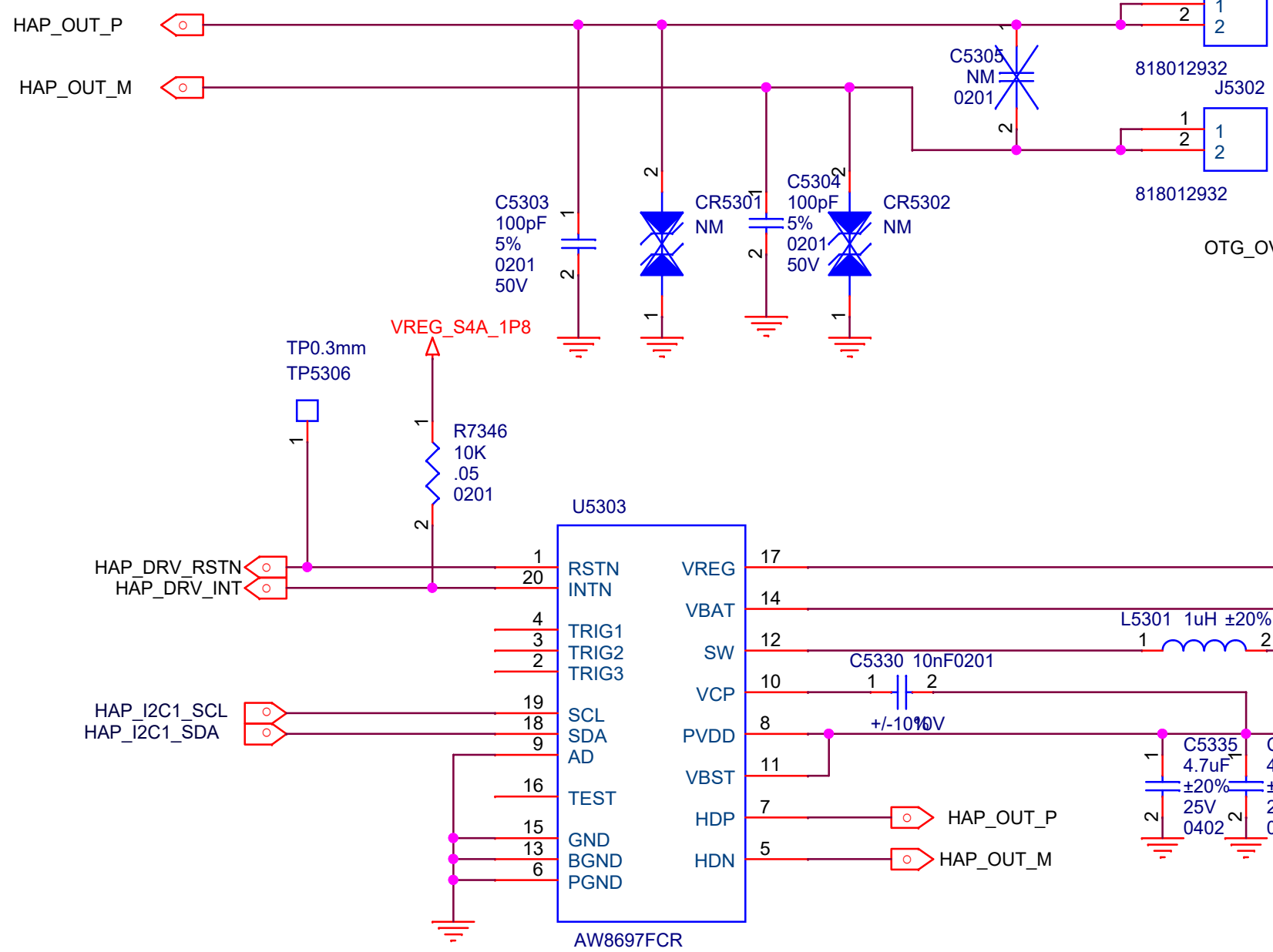


直接下主地

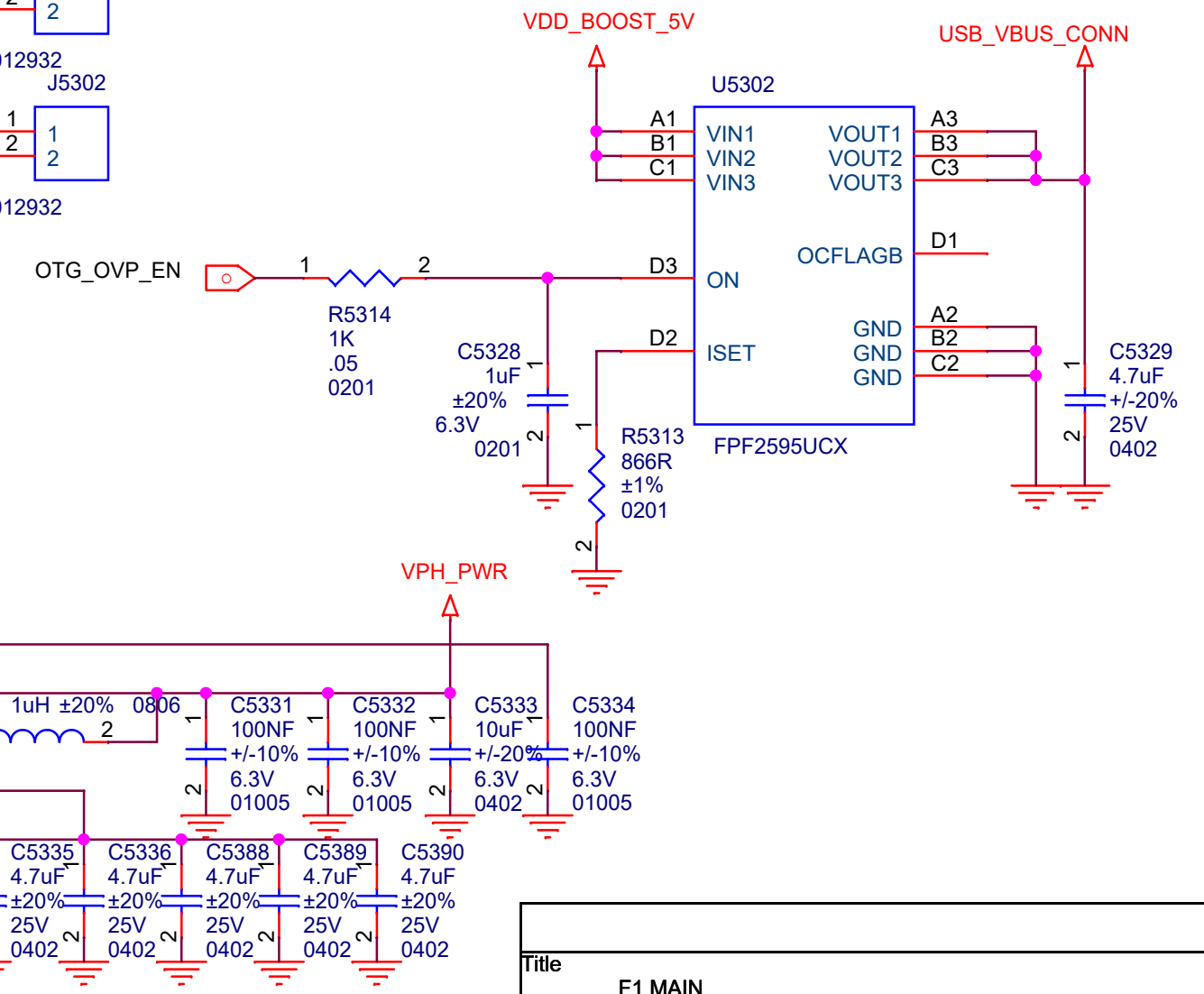
Title		F1 MAIN	
Size	A4	Document Number	PM855B CTRL&GND
Date:	Friday, November 29, 2019	Sheet	53 of 74



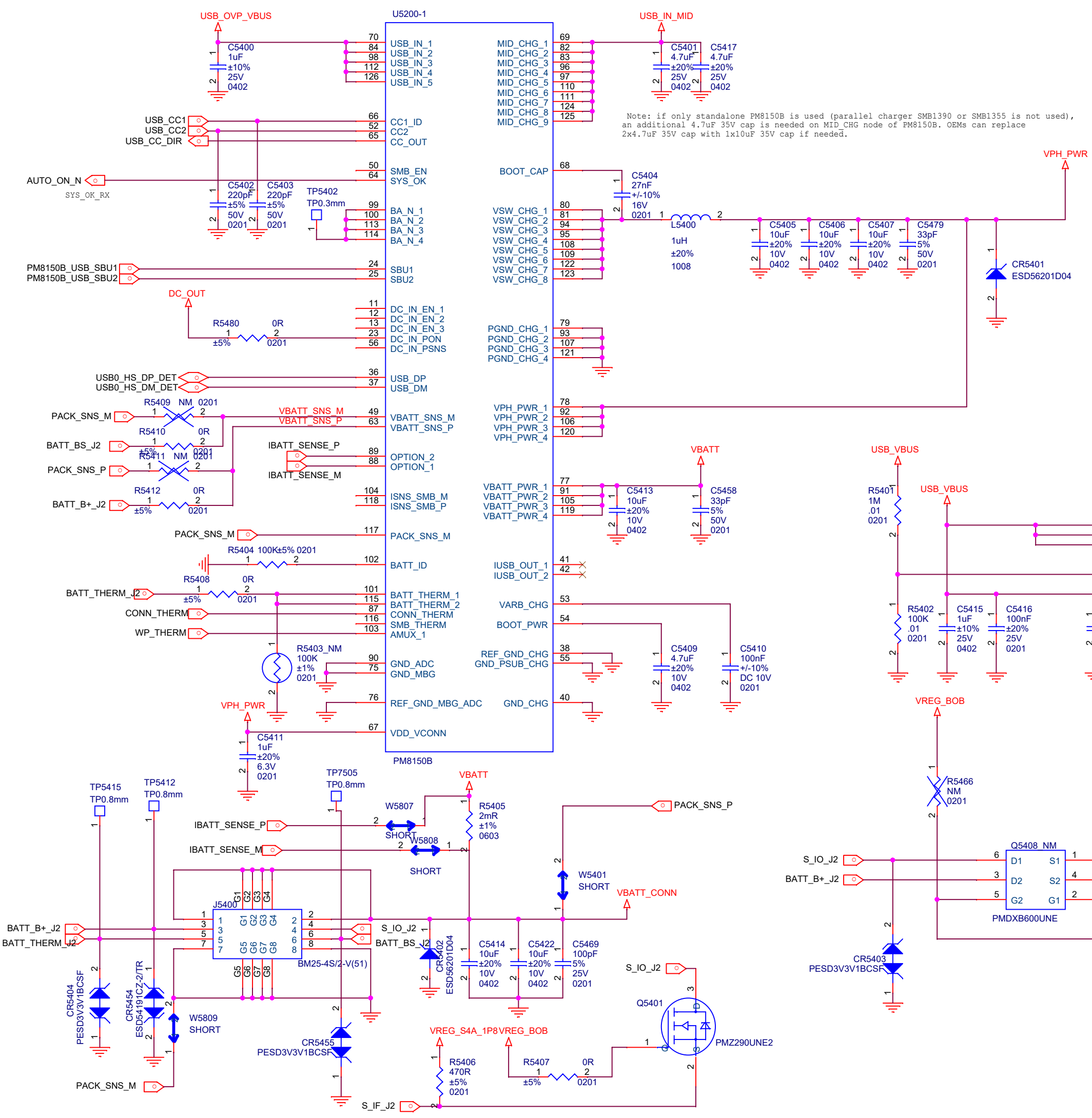
HAPTICS



OTG



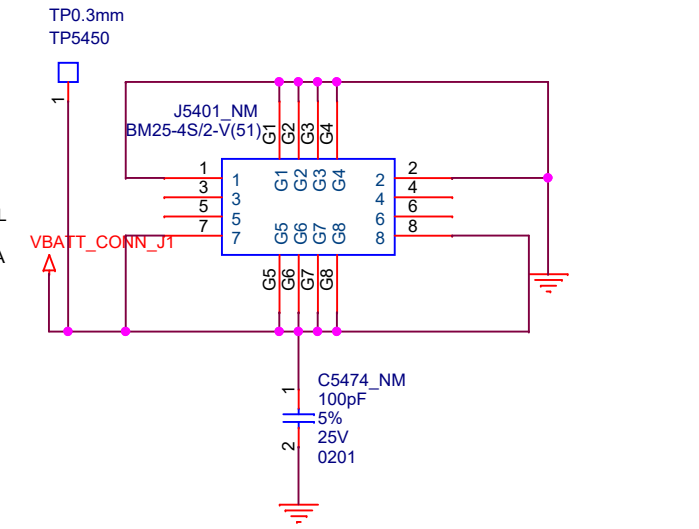
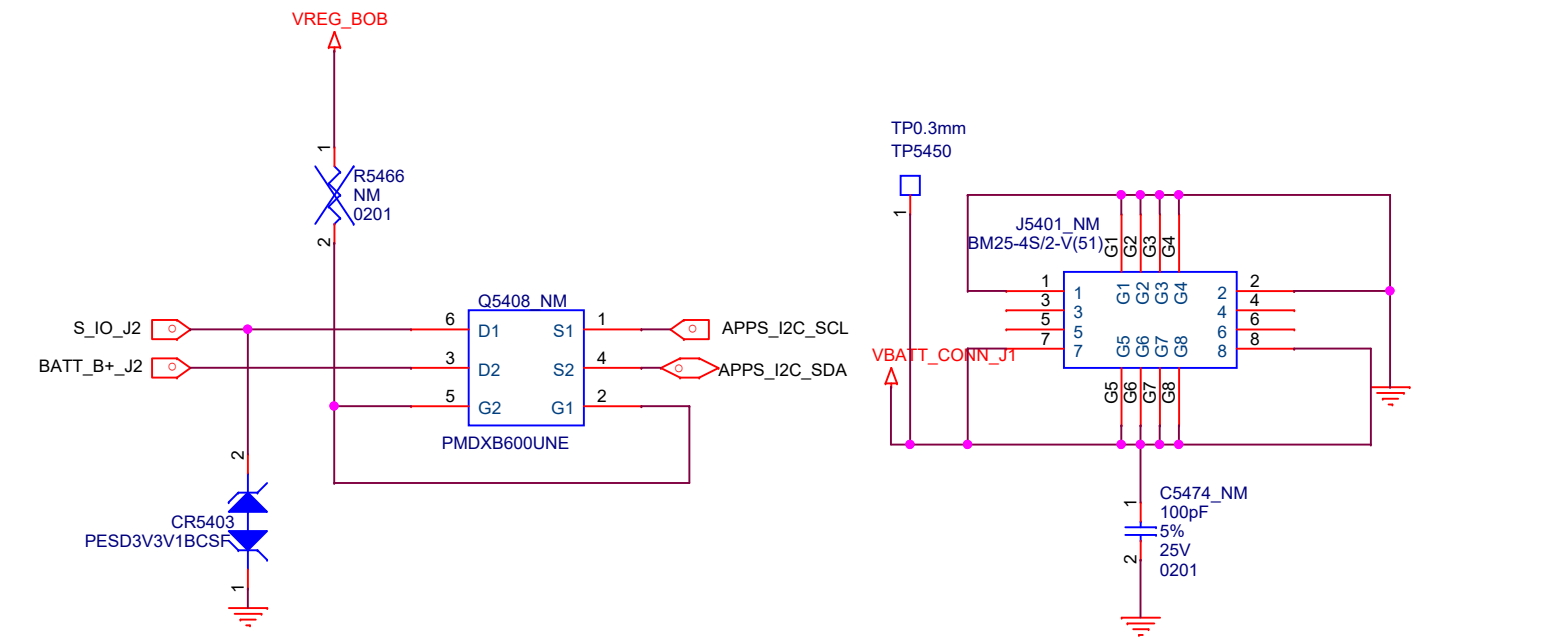
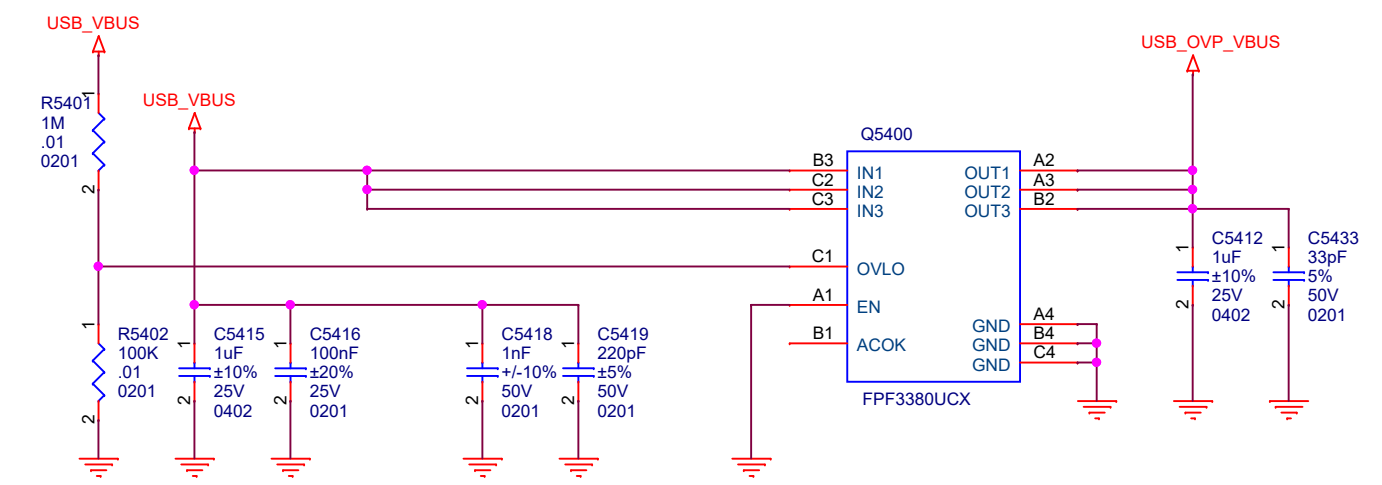
Title		F1 MAIN	
Size	A4	Document Number	PM855B HAPTIC
Date:	Friday, November 29, 2019	Sheet	54 / 74



Note: if only standalone PM8150B is used (parallel charger SMB1390 or SMB1355 is not used), an additional 4.7uF 35V cap is needed on MID_CHG node of PM8150B. OEMs can replace 2x4.7uF 35V cap with 1x10uF 35V cap if needed.

J1方案BOM: J2方案BOM:
 R5409不贴 R5411不贴
 R5403不贴 R5406不贴
 Q5408不贴 J5401不贴

J1:此页BOM不做更改;



Title		F1 MAIN	
Size	A3	Document Number	PM855B Charger
Date:	Friday, November 29, 2019	Sheet	55
		74	

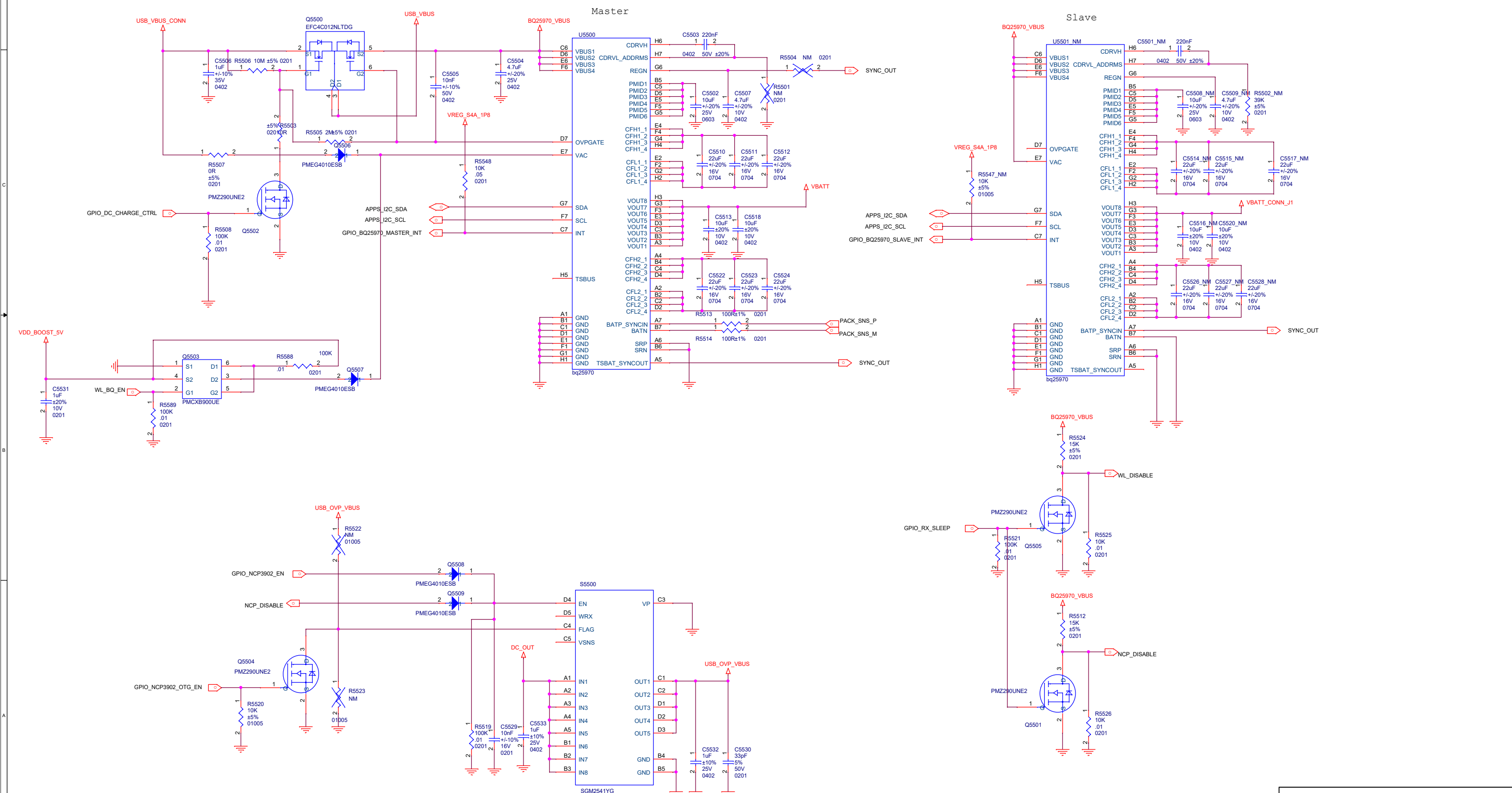
J1:此页BOM不做更改;

J2:R5501不贴

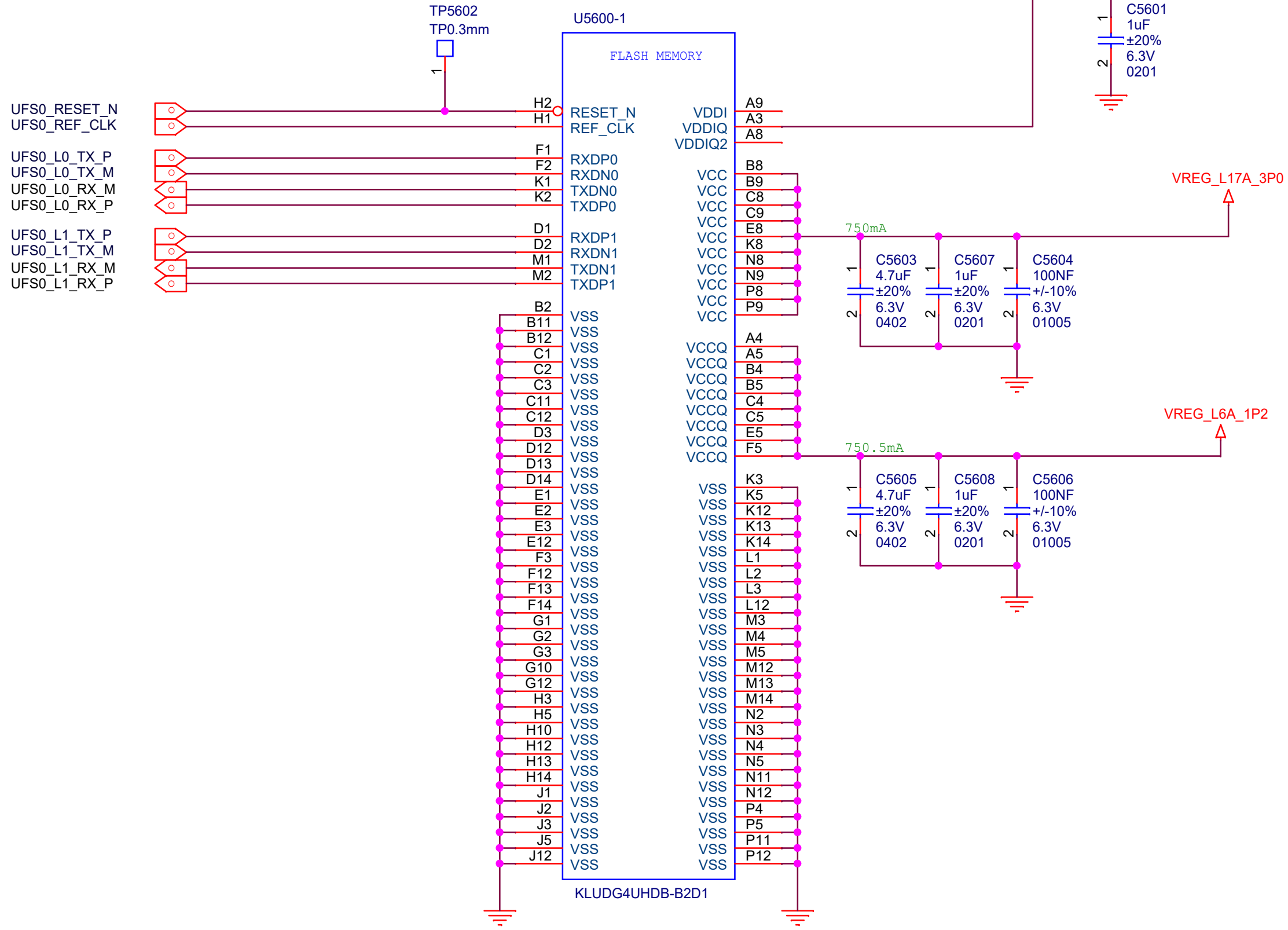
R5504不贴

R5515贴0欧姆电阻

Slave charger的BOM全部不贴



Title	F1 MAIN
Size	A2
Document Number	IR LED
Date:	Friday, November 29, 2019
Sheet	



Title		F1 MAIN	
Size	A4	Document Number	MEMORY
Date:	Friday, November 29, 2019	Sheet	57 74

D

D

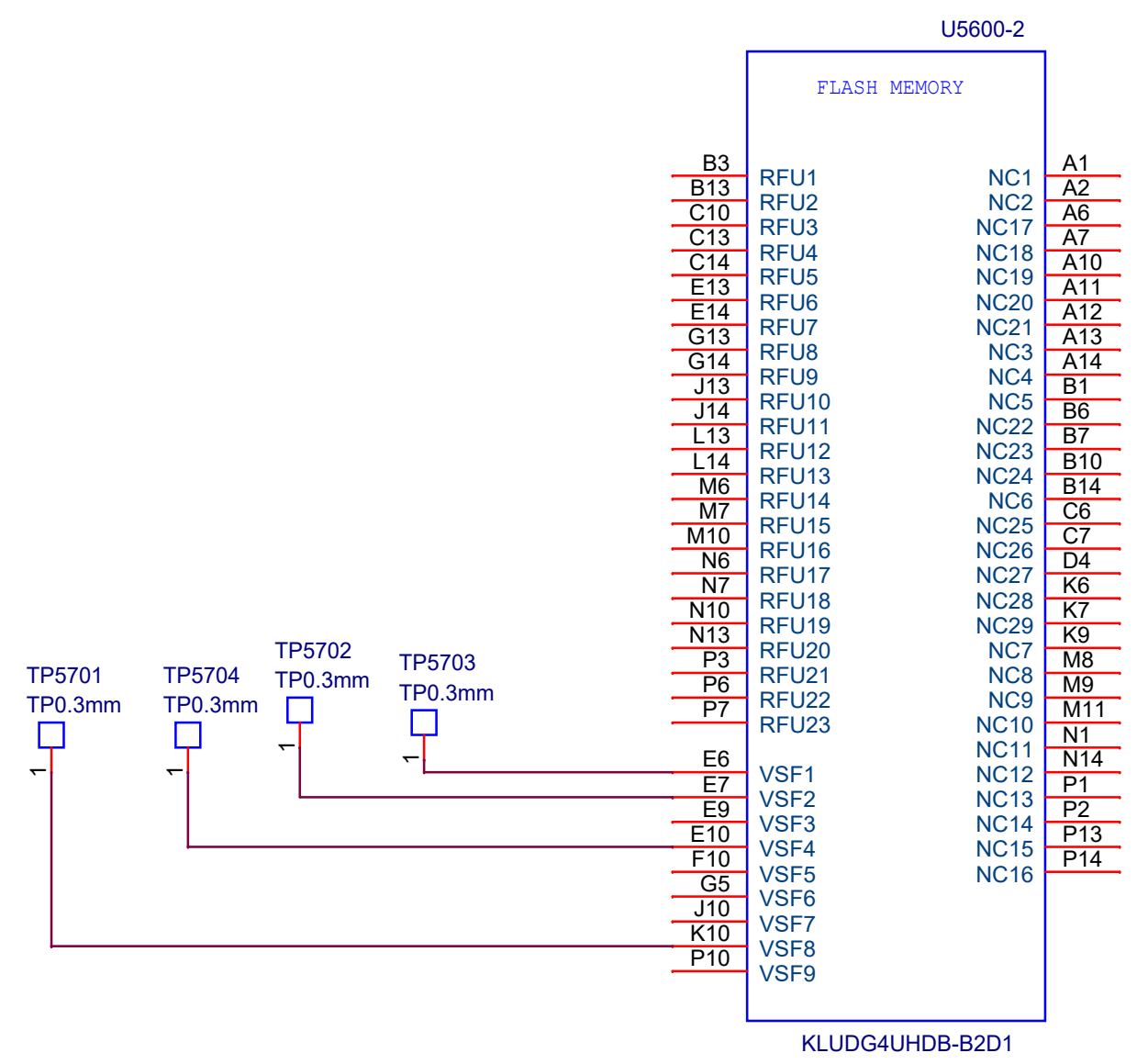
C

C

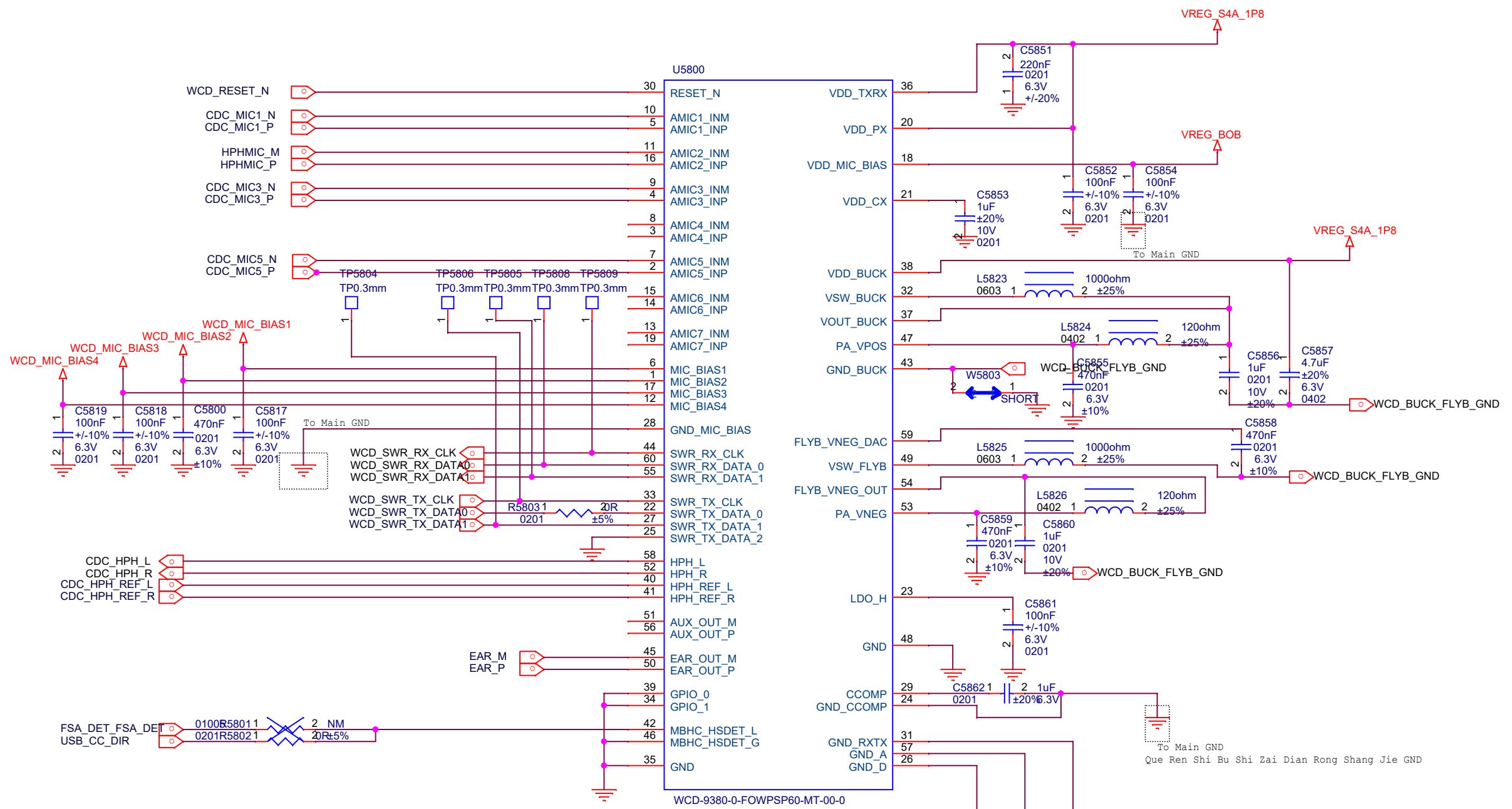
B

B

A



Title		F1 MAIN	
Size	A4	Document Number	MEMORY-2
Date:	Friday, November 29, 2019	Sheet	58 74



NOTE 1: ROUTE AN ISOLATED GROUND TRACE FROM CCOMP_REF TO THE CAP GROUND, THEN VIA TO THE MAIN GROUND PLANE
 NOTE 2: PLACE VDD_BUCK CAP AS CLOSE TO CHIP EDGE AS POSSIBLE AND MINIMIZE LOOP INDUCTANCE
 NOTE 3: USE SHORT AND WIDE TRACES FOR BUCK AND FLYBACK RELATED NETS
 NOTE 4: ANALOG MIC INPUTS SHOULD BE ISOLATED WITH GROUND FROM NOISY OR SWITCHING SIGNALS AND SUPPLIES

Title		F1 MAIN
Size	Document Number	WCD9340-1
A3		
Date:	Friday, November 29, 2019	Sheet

5

4

3

2

1

D

D

C

C

B

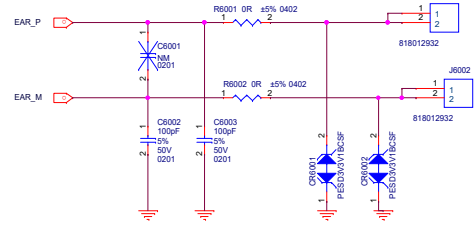
B

A

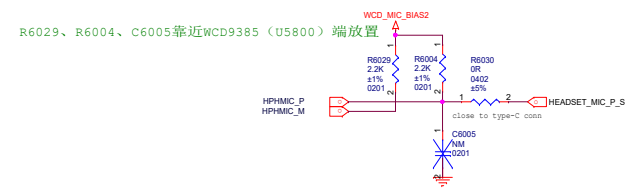
A

Title	
F1 MAIN	
Size	Document Number
A3	WCD9340-2
Date:	Friday, November 29, 2019
Sheet	1

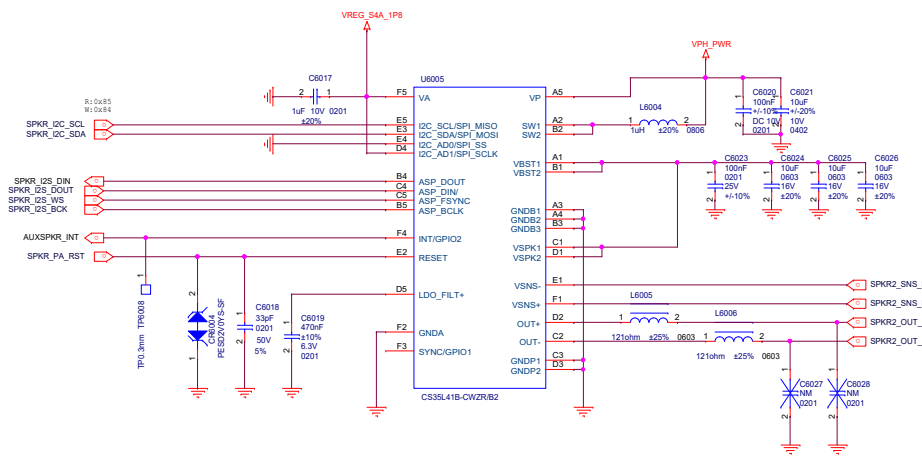
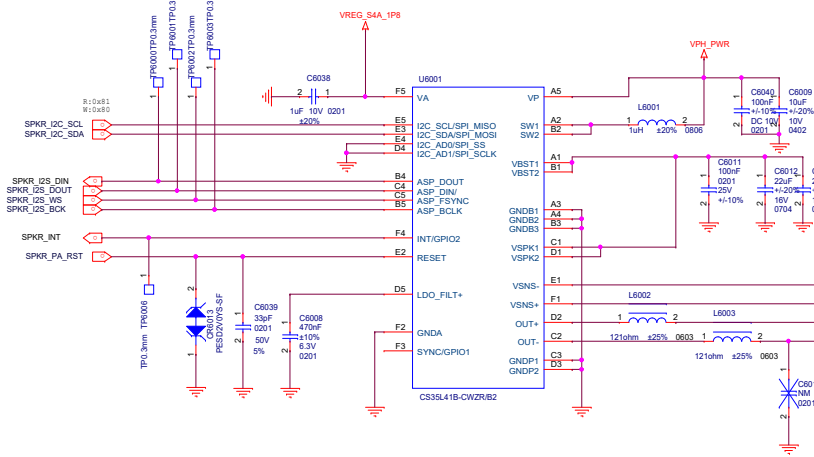
RECEIVER



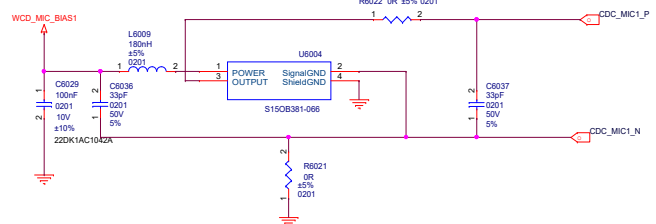
HEADSET



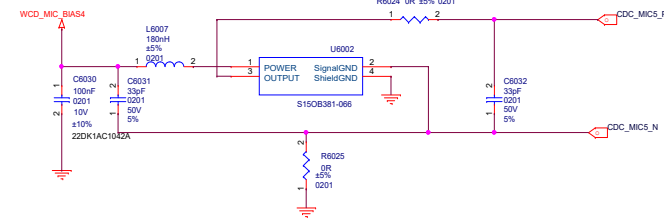
SPKR PA



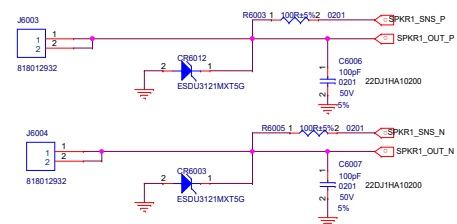
MAIN MIC



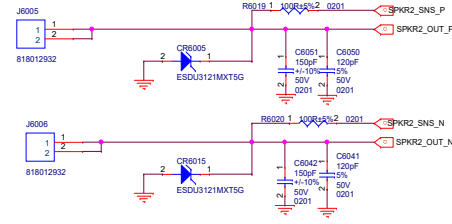
AUX MIC



SPK1

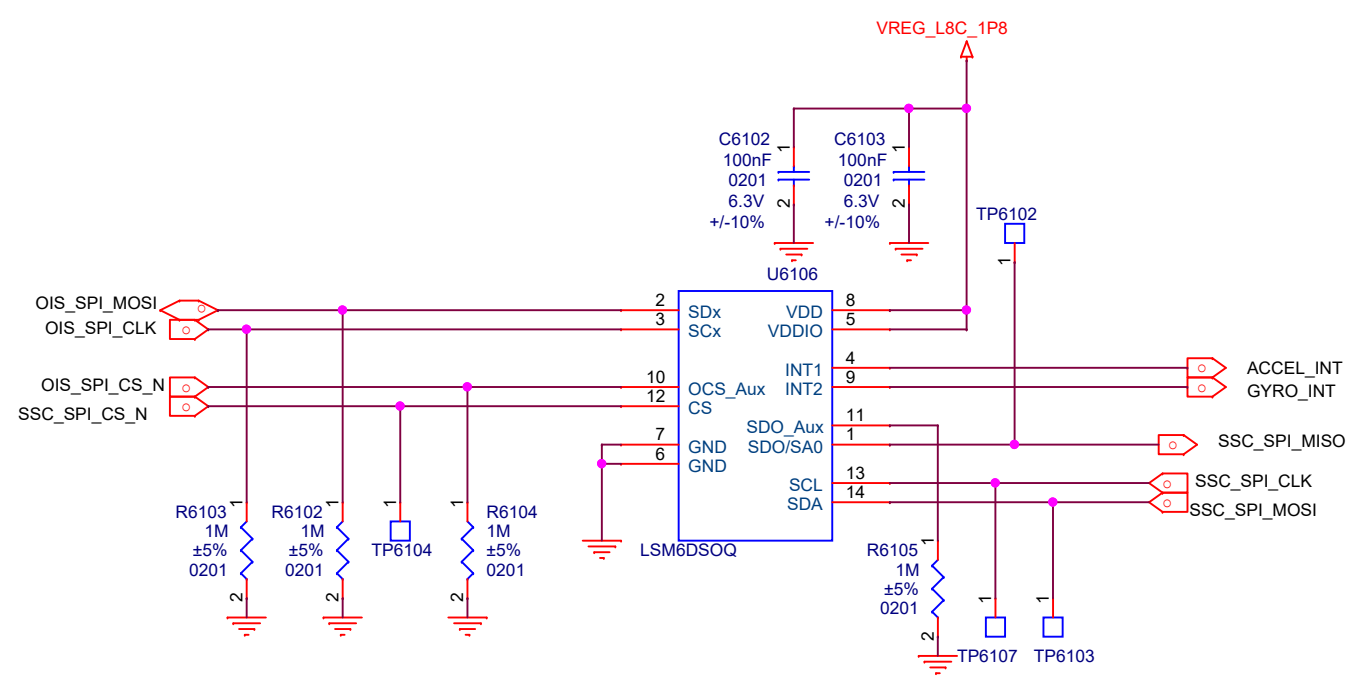


SPK2

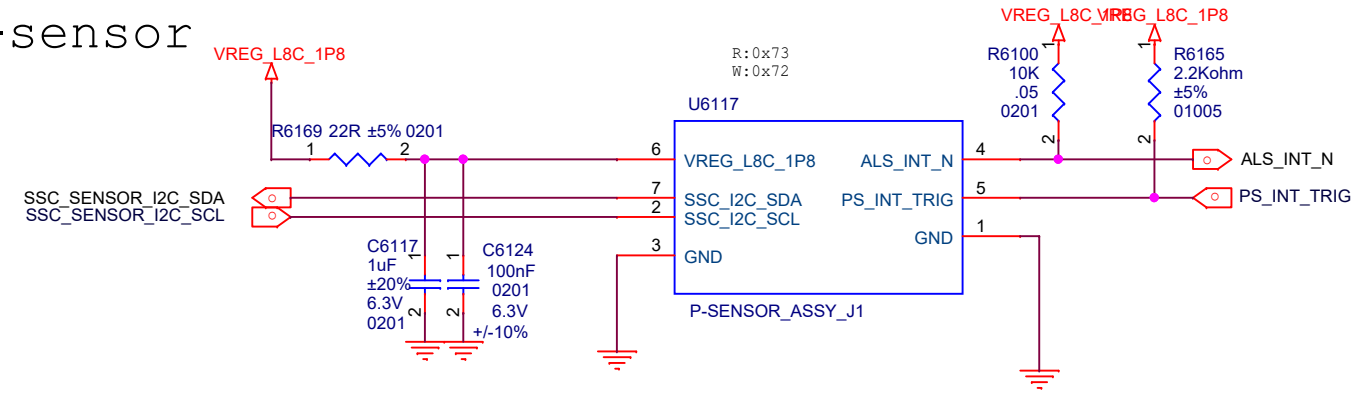


RGB DRIVER

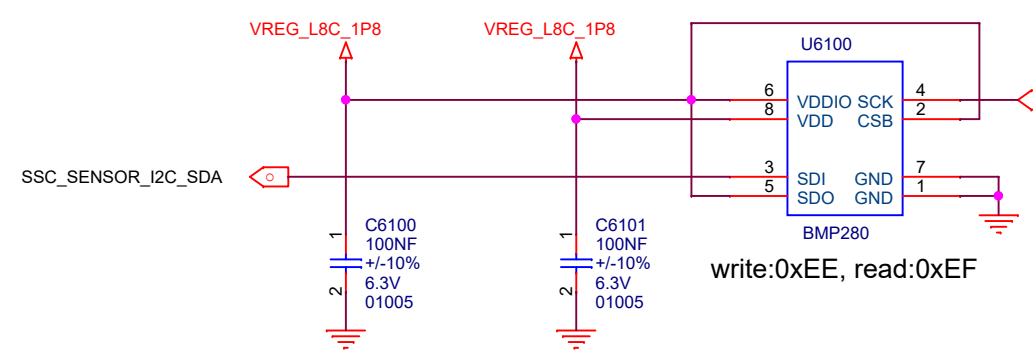
A+G



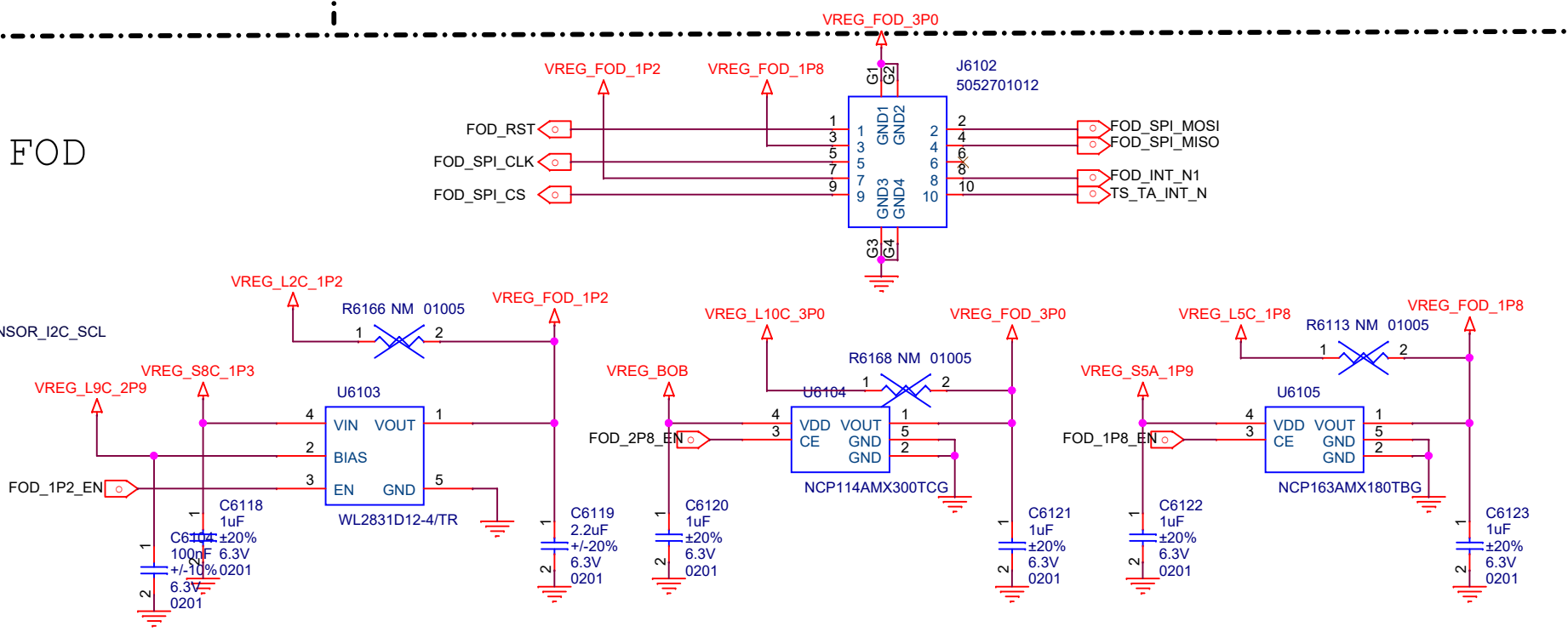
L-sensor



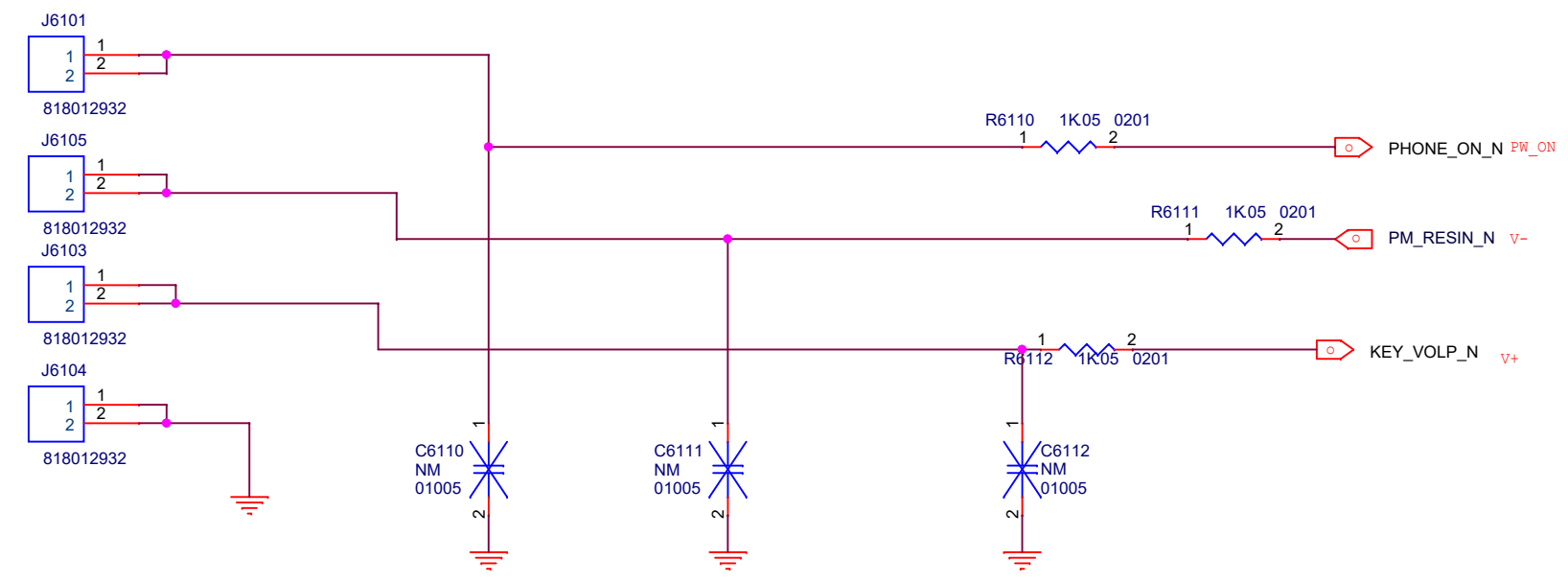
PRESSURE



FOD

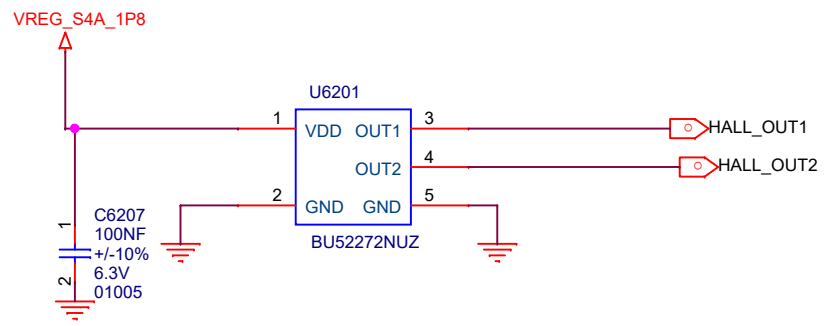


Sidekey

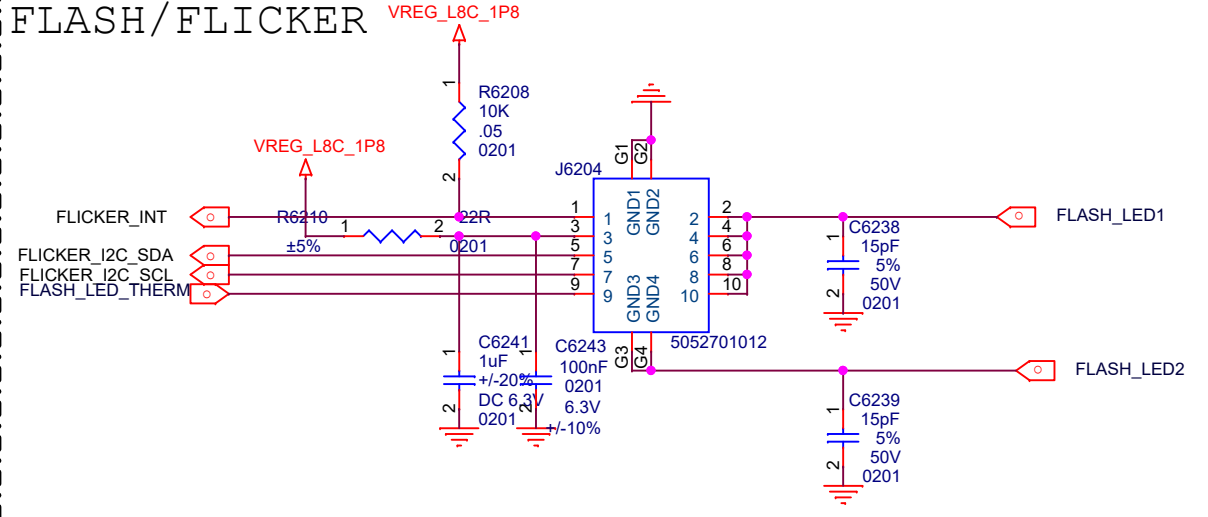


Title		F1 MAIN	
Size	A3	Document Number	SENSOR
Date:	Friday, November 29, 2019	Sheet	62 74

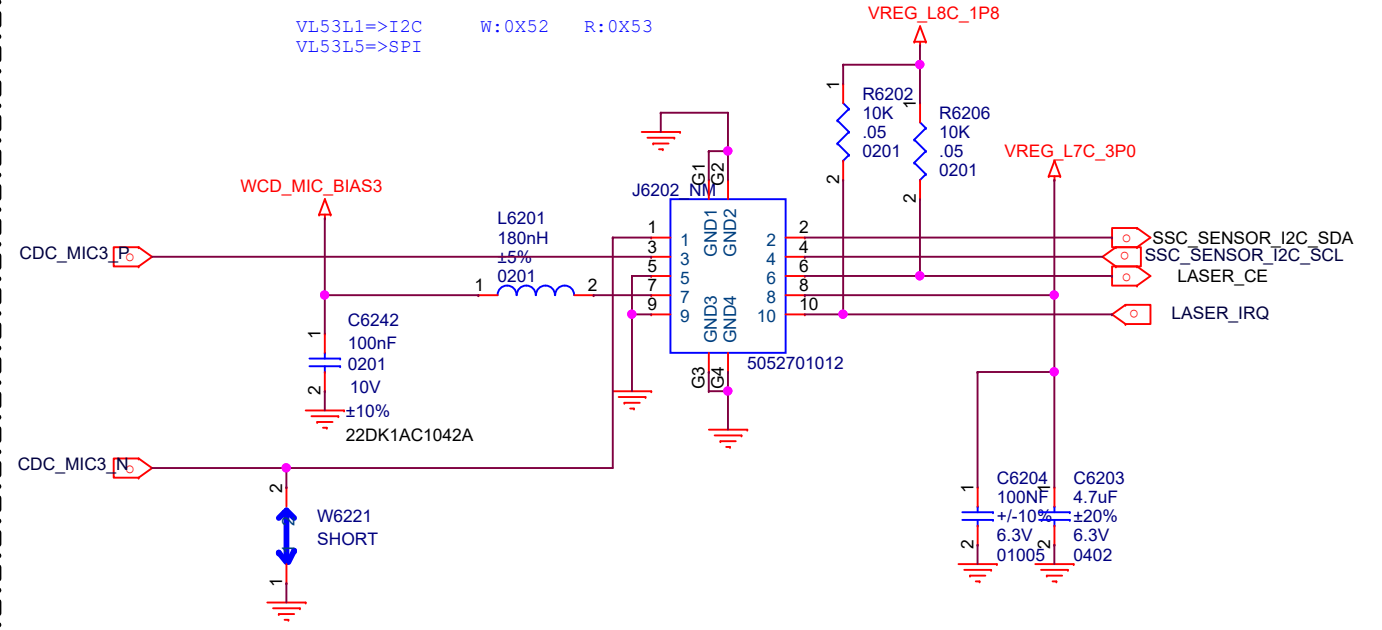
HALL



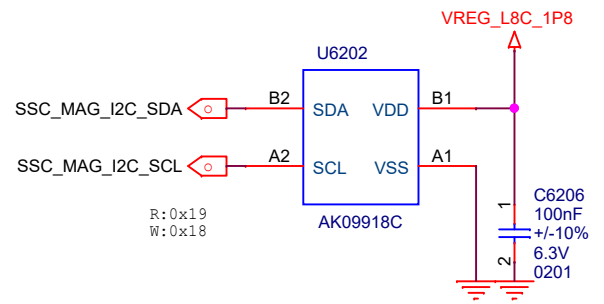
FLASH/FLICKER



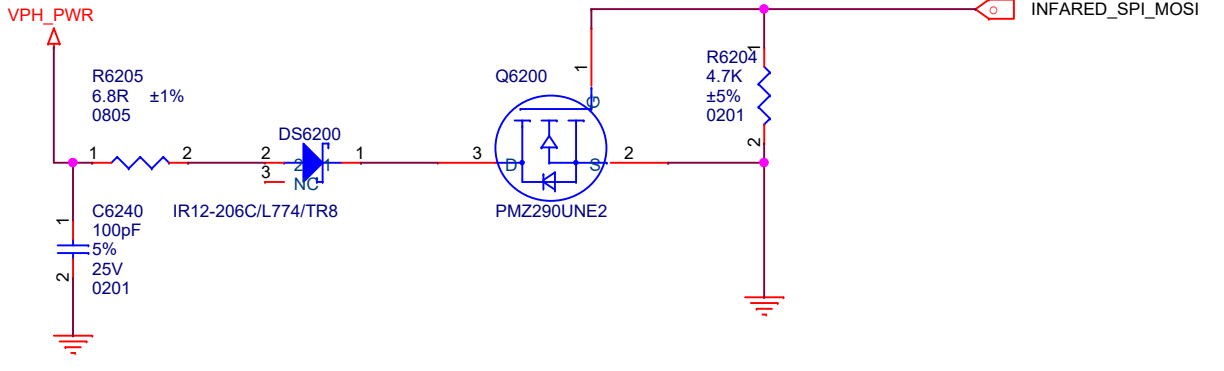
TOF



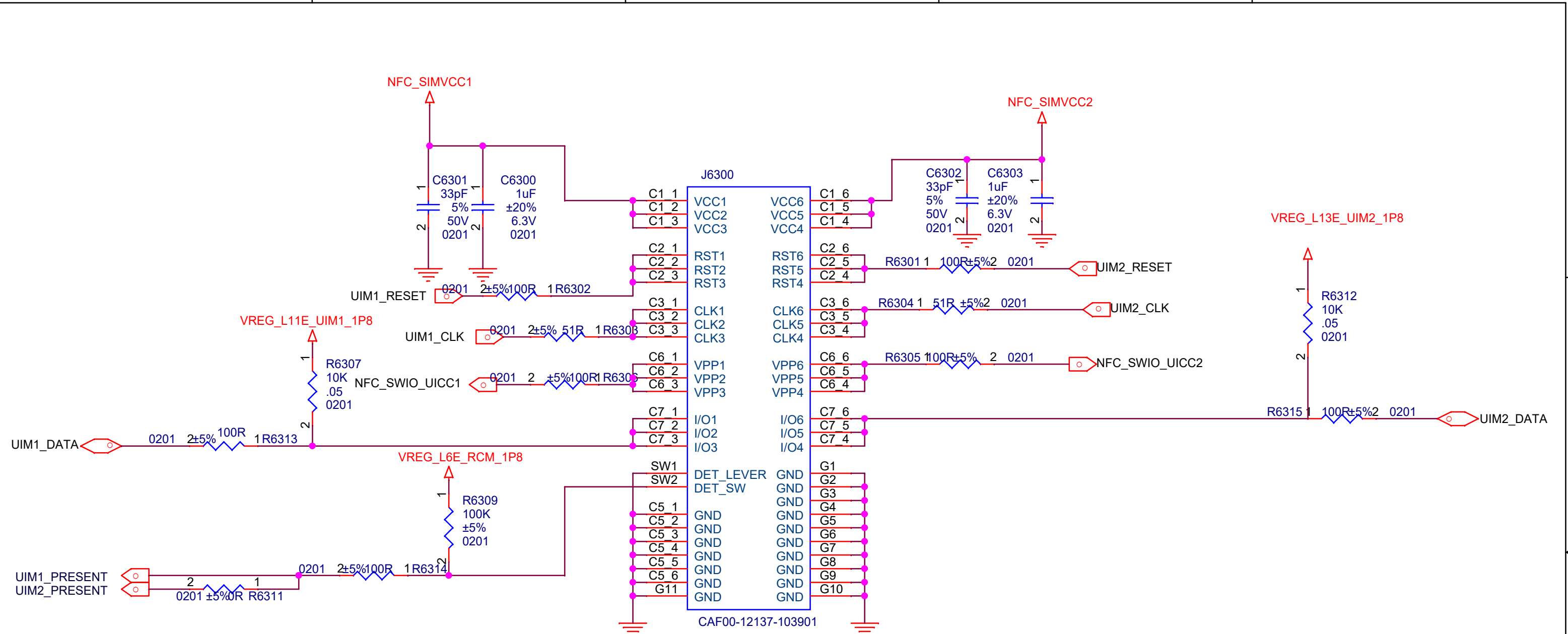
COMPASS



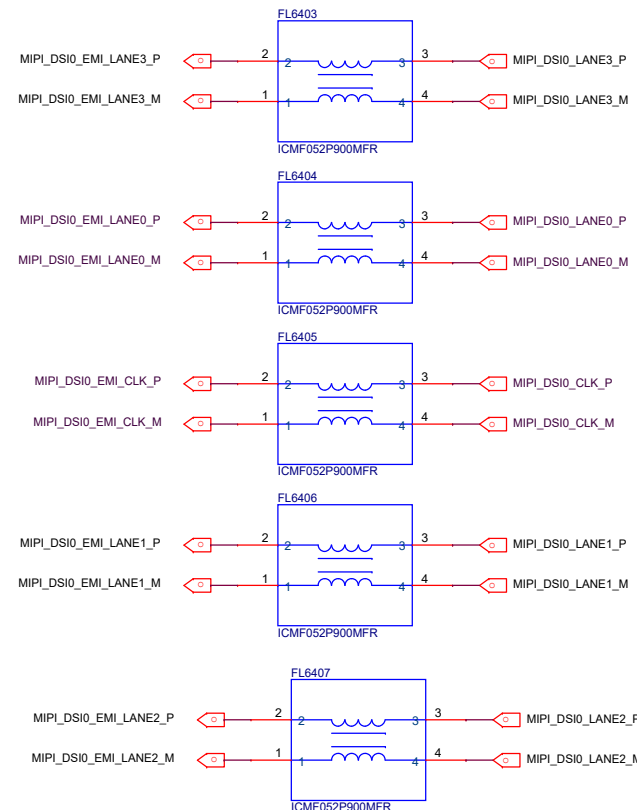
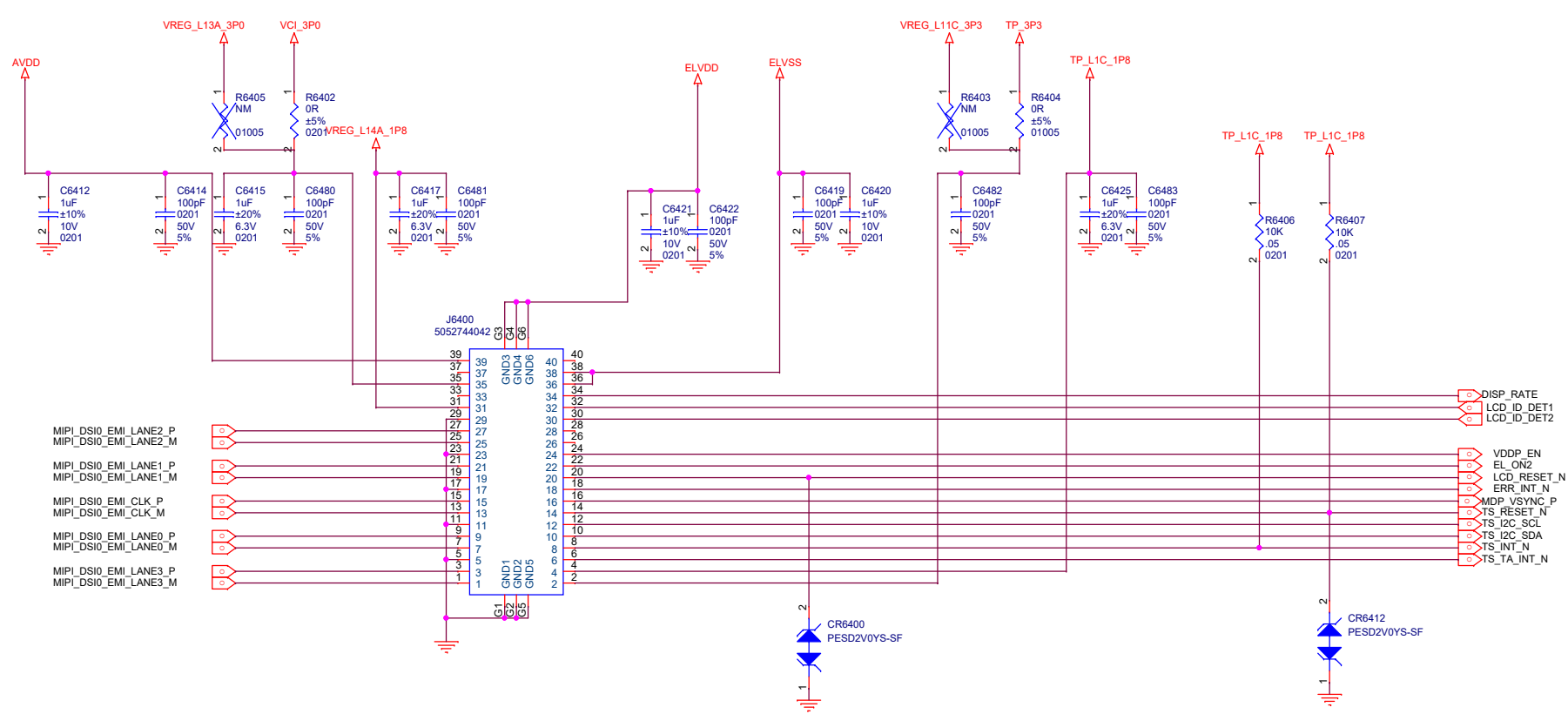
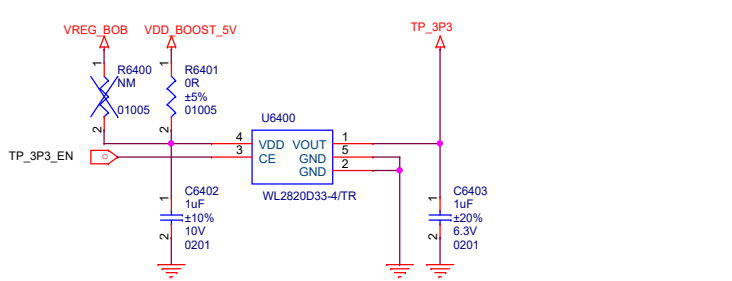
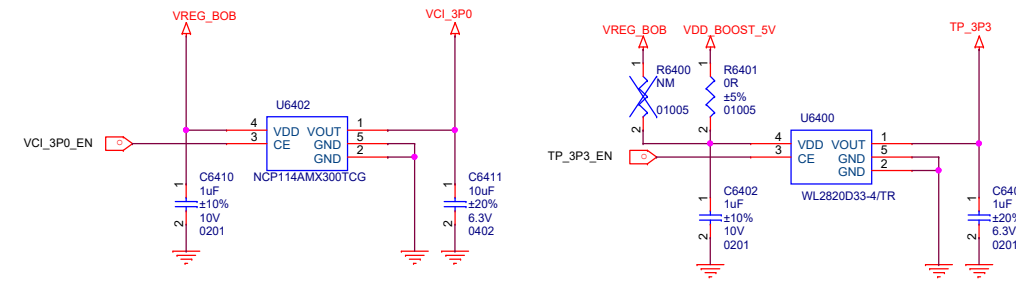
INFRARED



Title		F1 MAIN
Size	Document Number	SENSOR-2
A3	Date:	Friday, November 29, 2019
Sheet	63	74

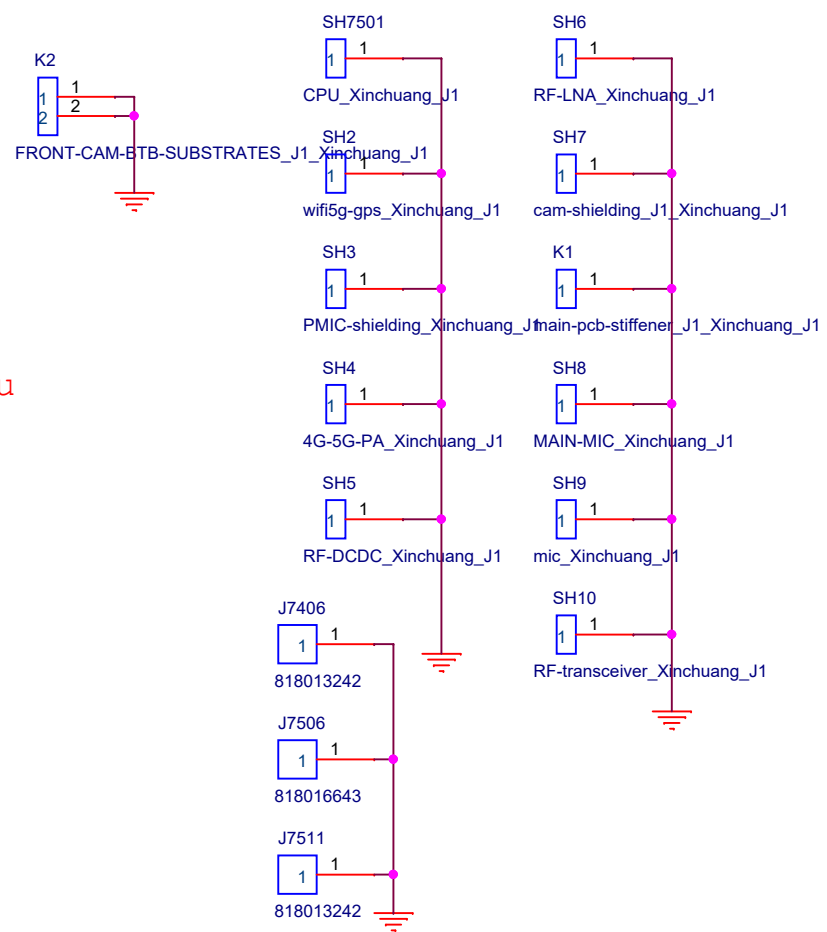
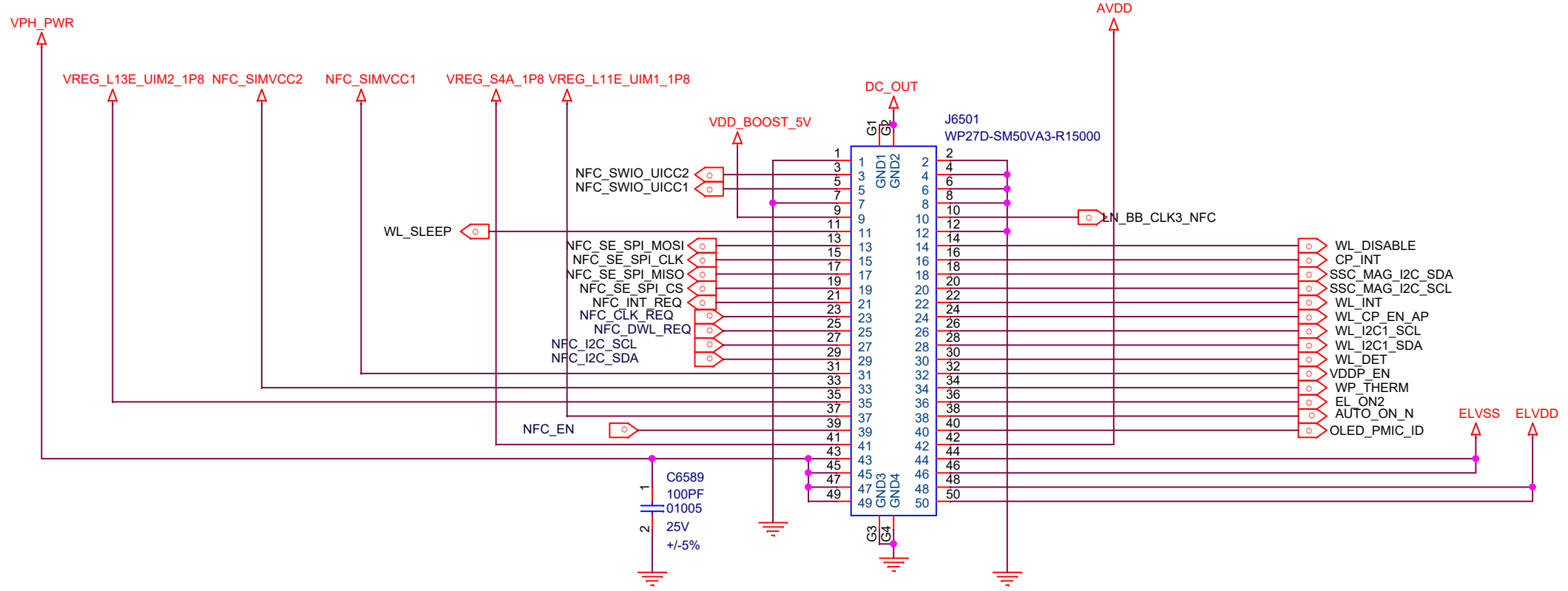


Title		F1 MAIN	
Size	A4	Document Number	SIM
Date:	Friday, November 29, 2019	Sheet	64 / 74

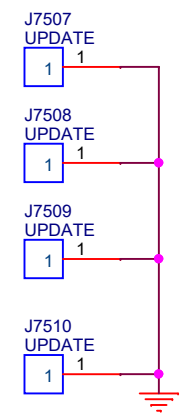


- MIPI_DSI0_EMI_LANE2_P
- MIPI_DSI0_EMI_LANE2_M
- MIPI_DSI0_EMI_LANE1_P
- MIPI_DSI0_EMI_LANE1_M
- MIPI_DSI0_EMI_CLK_P
- MIPI_DSI0_EMI_CLK_M
- MIPI_DSI0_EMI_LANE0_P
- MIPI_DSI0_EMI_LANE0_M
- MIPI_DSI0_EMI_LANE3_P
- MIPI_DSI0_EMI_LANE3_M

- DISP_RATE
- LCD_ID_DET1
- LCD_ID_DET2
- VDDP_EN
- EL_ON2
- LCD_RESET_N
- ERR_INT_N
- MDP_VSYNC_P
- TS_RESET_N
- TS_I2C_SCL
- TS_I2C_SDA
- TS_INT_N
- TS_TA_INT_N

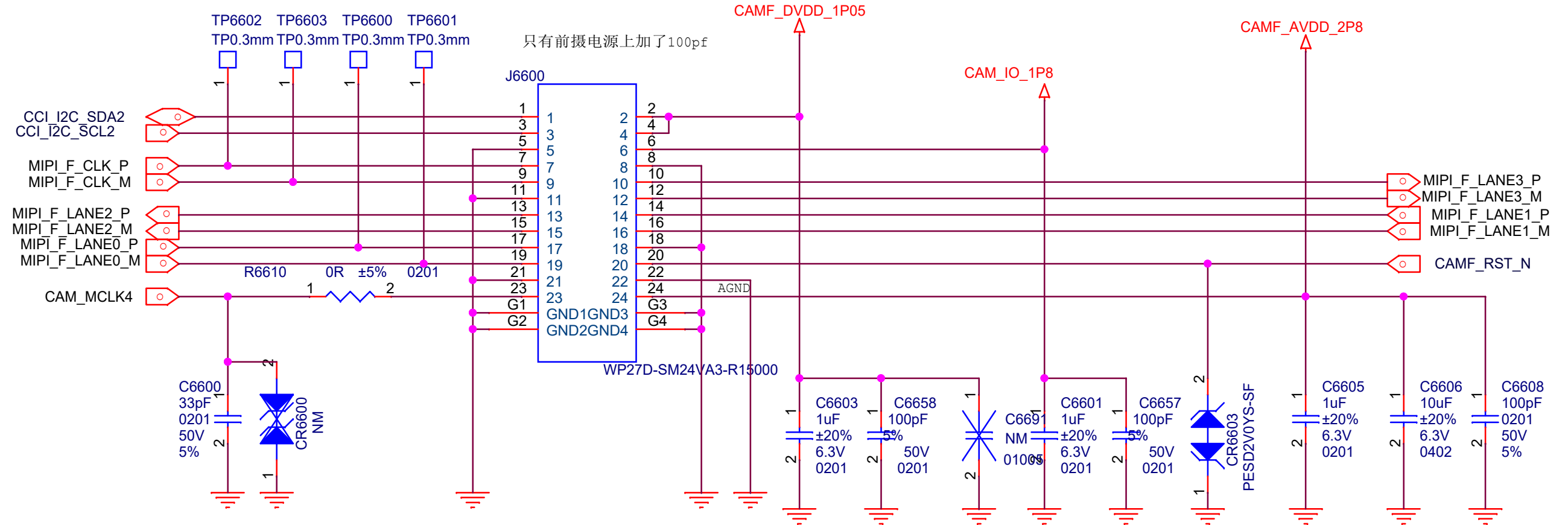


JiDeGengXinKu

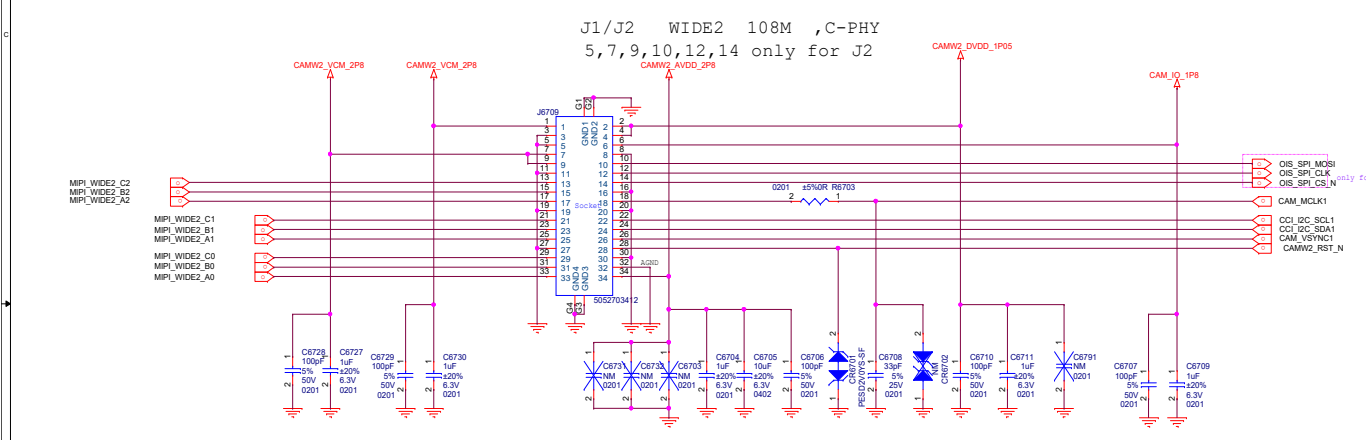
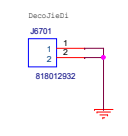
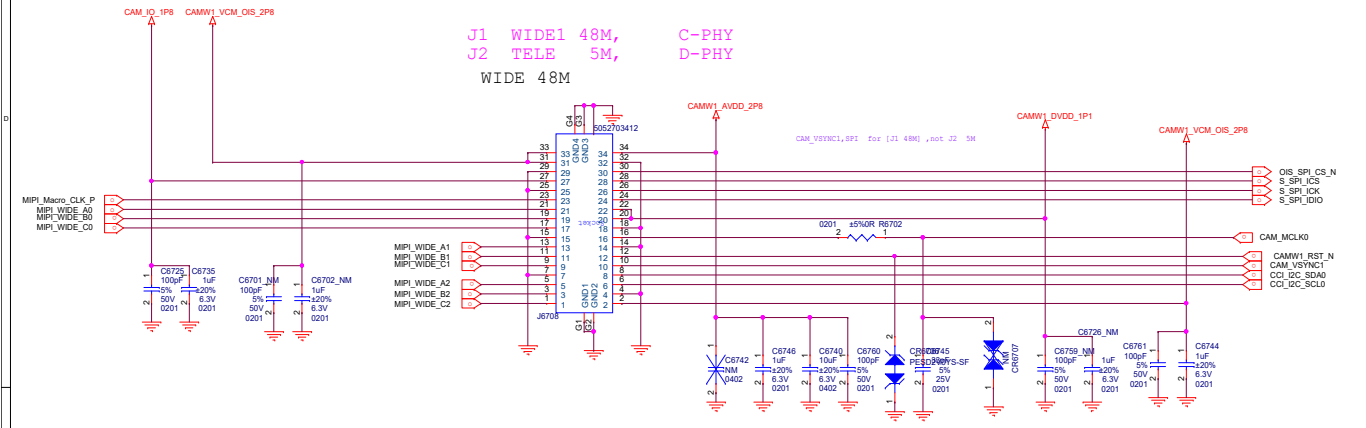


Title		
E1 USB SUB		
Size	Document Number	Rev
A3	BTB	P0
Date:	Friday, November 29, 2019	Sheet 66 of 74

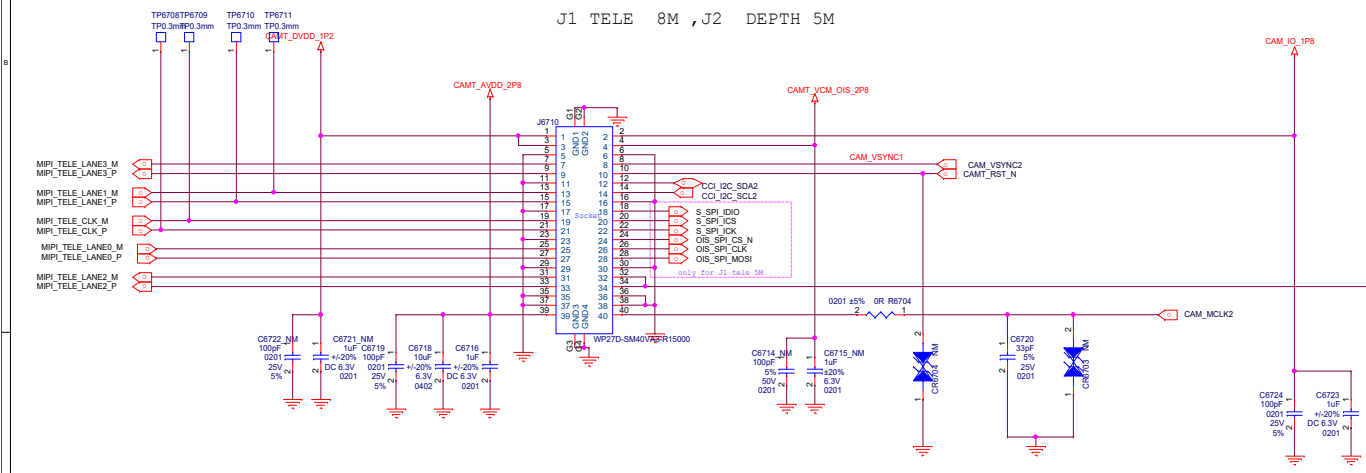
J1/J2 front 20M CAMERA

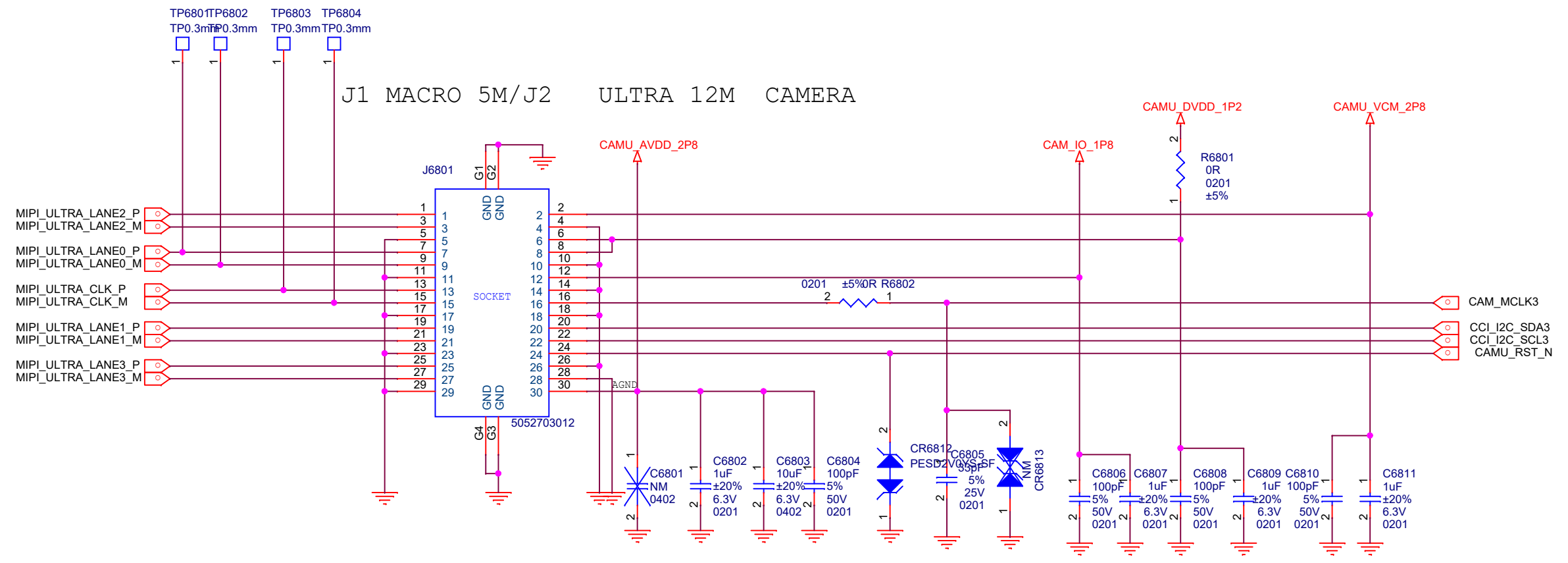


Title		F1 MAIN	
Size	A4	Document Number	Reserved(for Analog FM)
Date:	Friday, November 29, 2019	Sheet	67 / 74



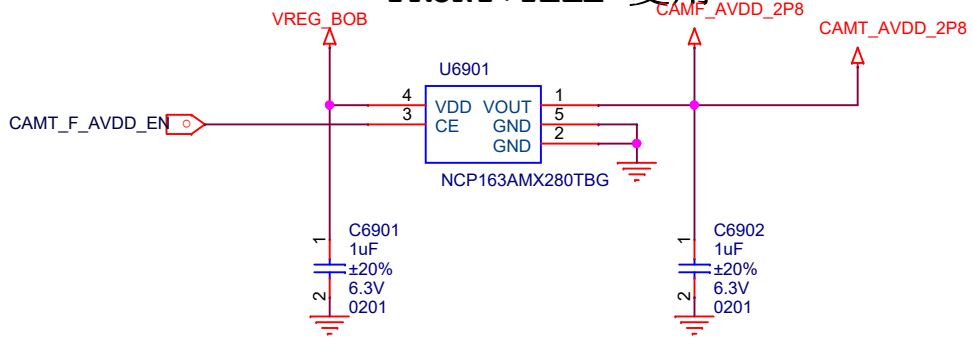
CAM	J1	J2	备注
Front_20M_24pin	相同		
J1(4x 8M)_J2(Depth 5M)_40pin	有 AF+OIS	2 Lan	J2 无 AF +OIS, C6712, C6713, C6714, C6715, J1 only, J2 NM
J1(Ultra108M)_J2(Wide108M)_34pin	有 AF_Cphy	有 AF+OIS, Cphy	J1 无 OIS, C6727, C6728 J2 only, J1 NM
J1(Wide 48M)_J2(Tele 5M)_34pin	有 AF+OIS, Cphy	有 AF_Dphy 2Lan	J2 无 OIS, C6701, C6702 J1 only, J2 NM
J1(Macro5M)_J2(Ultra 16M)_30pin	有 AF_Dphy 2Lan	有 AF	



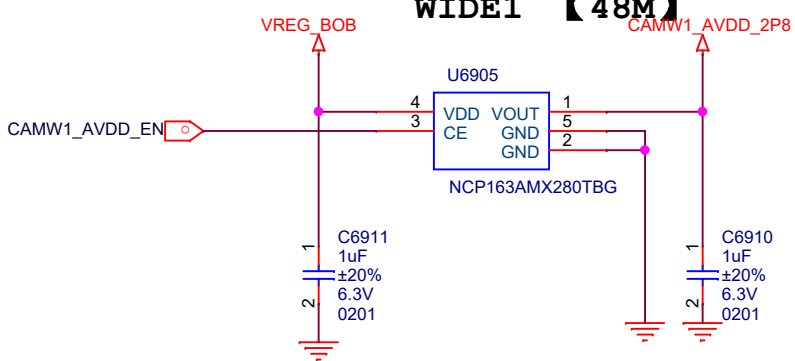


Title		F1 MAIN	
Size	A3	Document Number	ULTRA CAMERA
Date:	Friday, November 29, 2019	Sheet	69 74

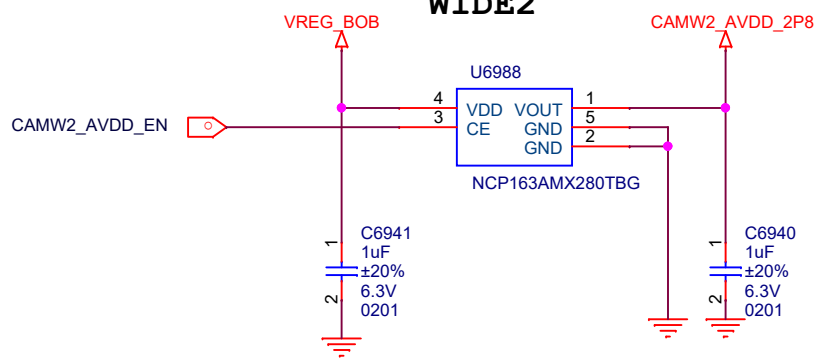
FRONT+TELE 复用 tele 和 front 复用



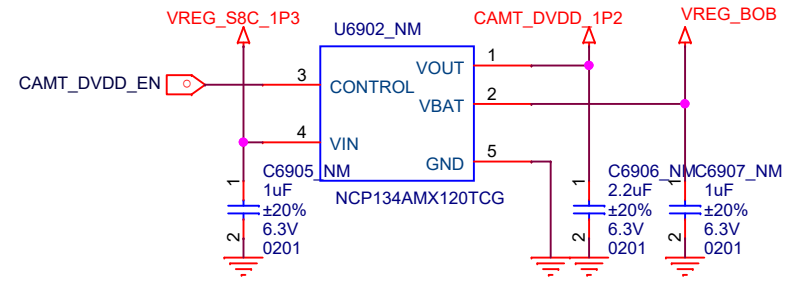
WIDE1 【48M】



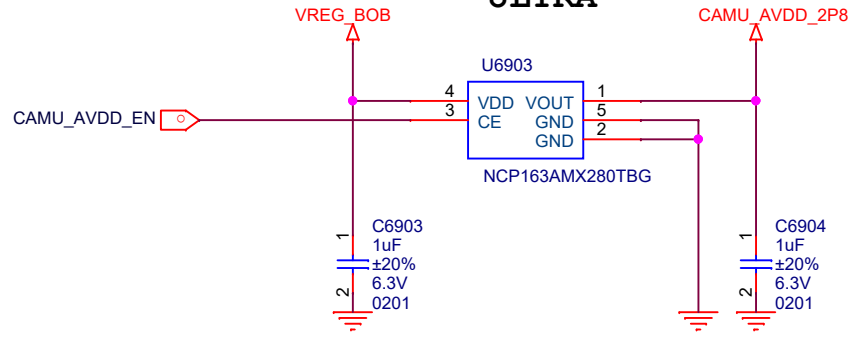
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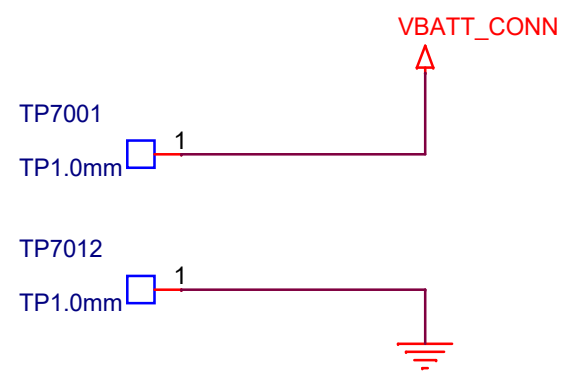
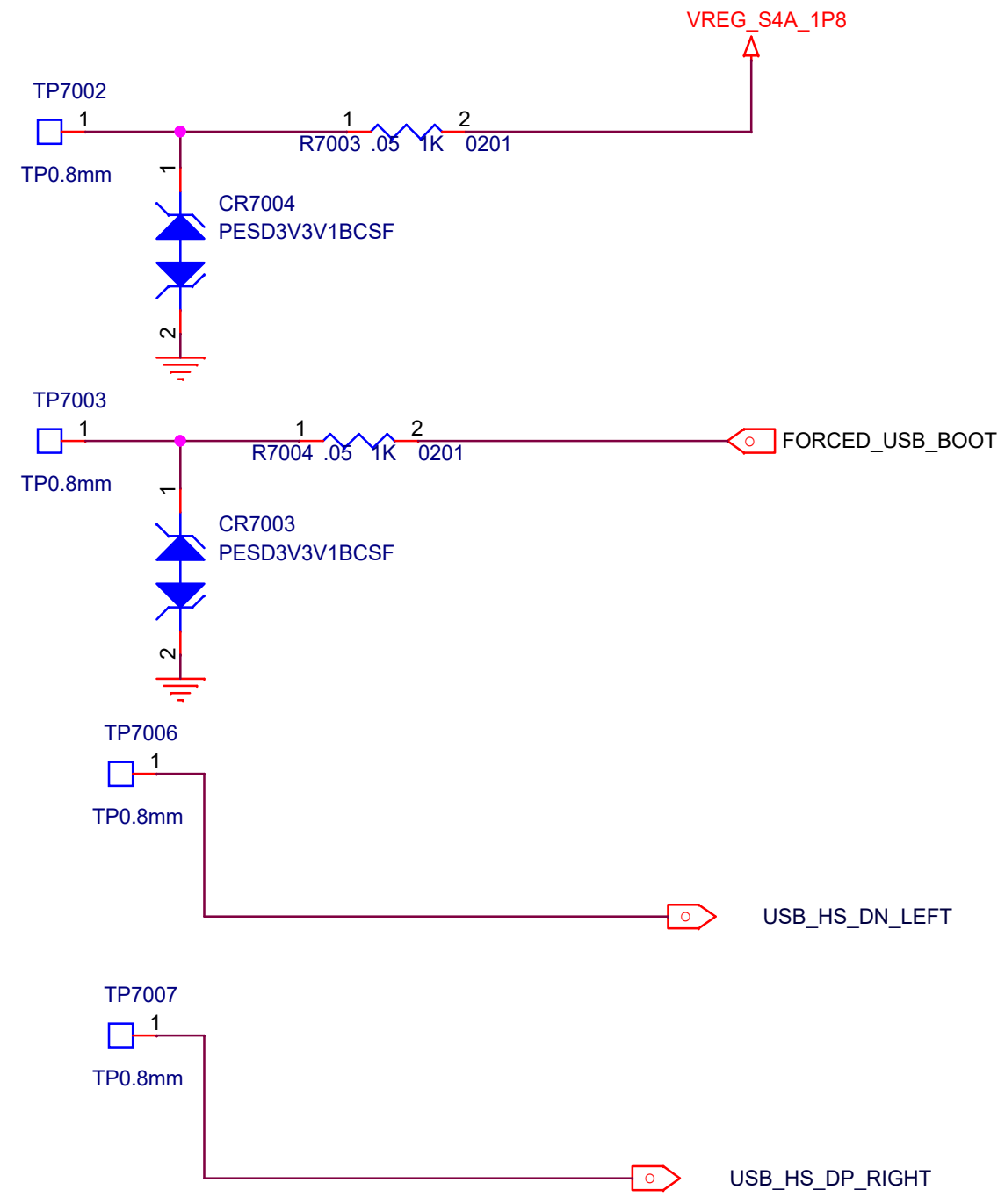
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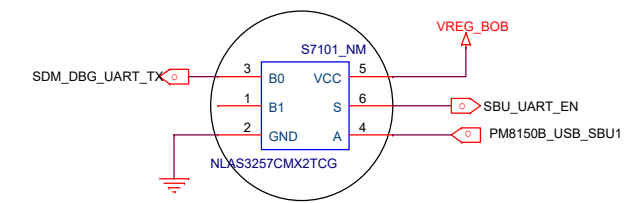
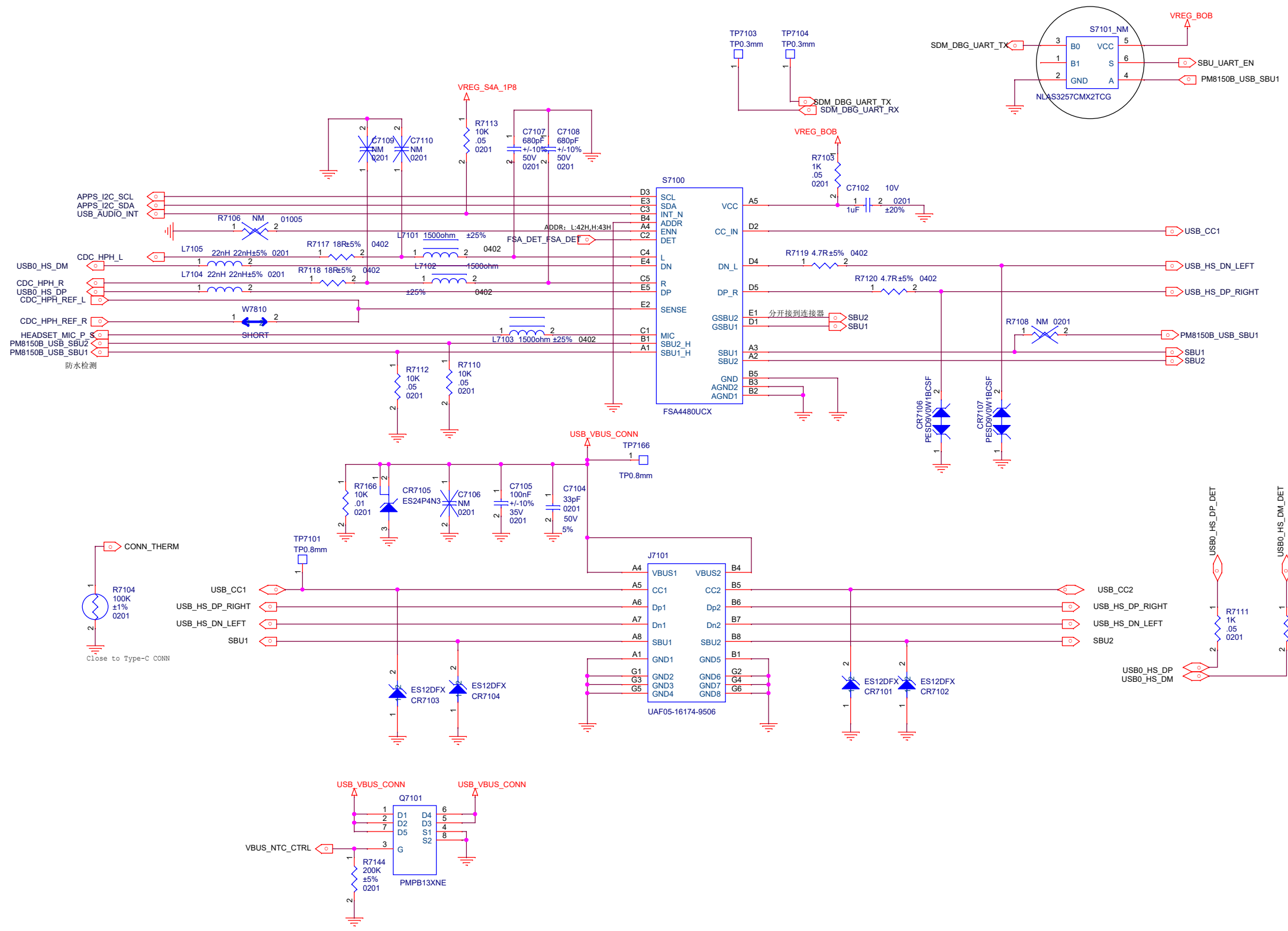
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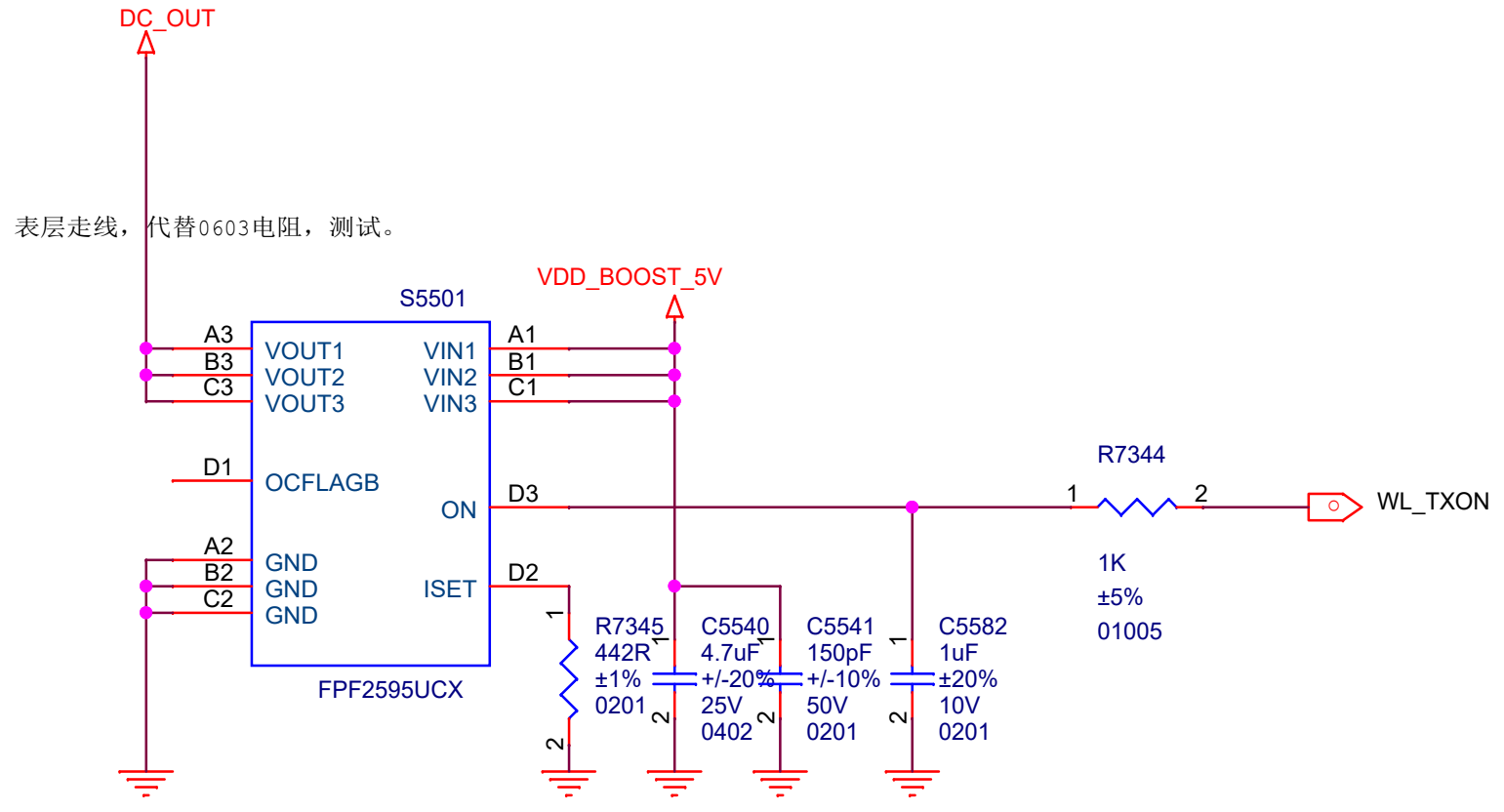


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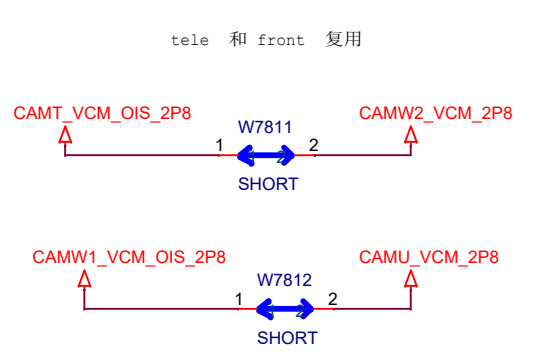
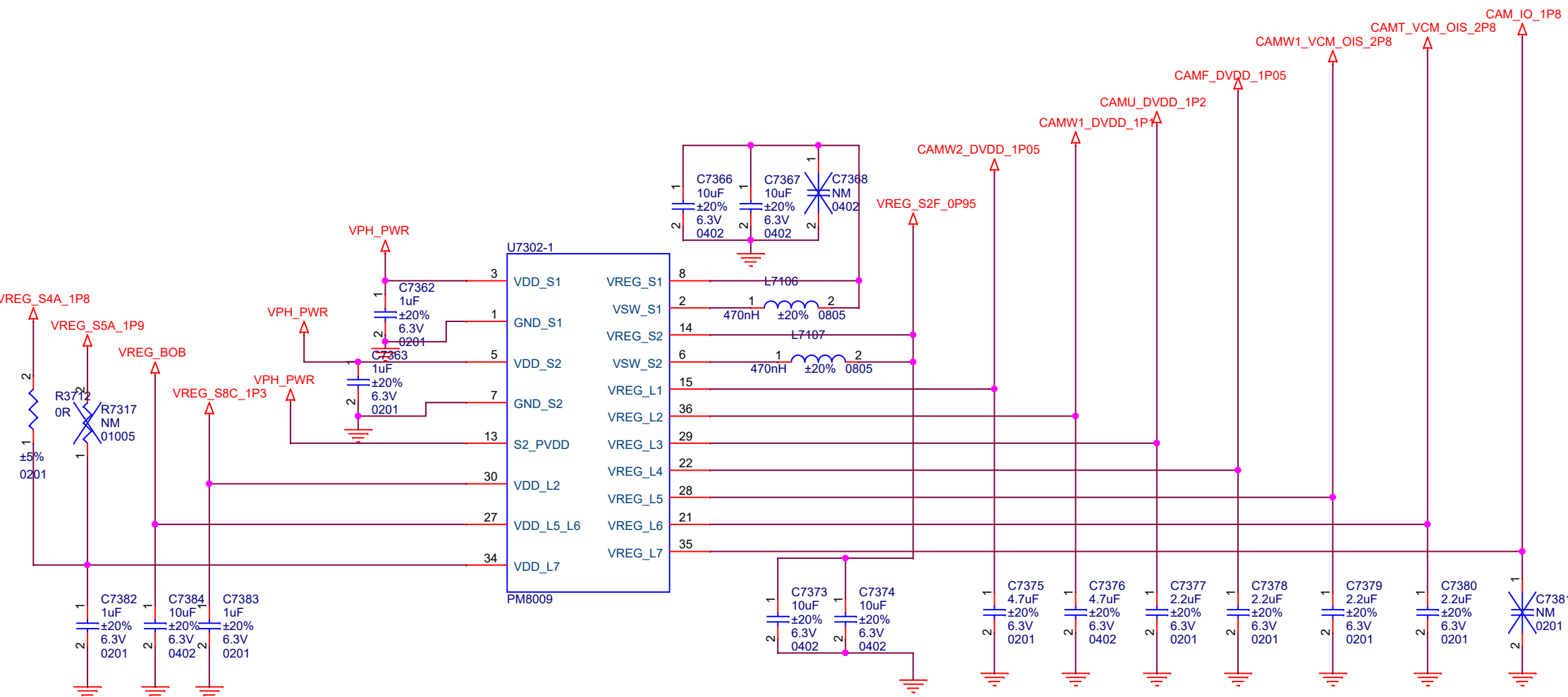
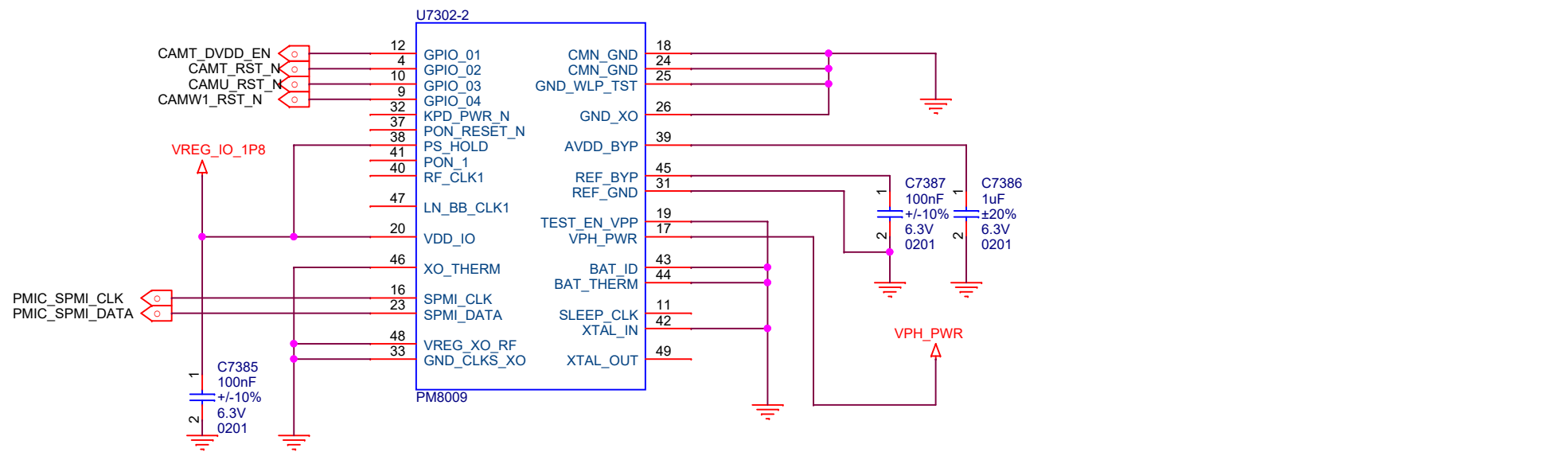
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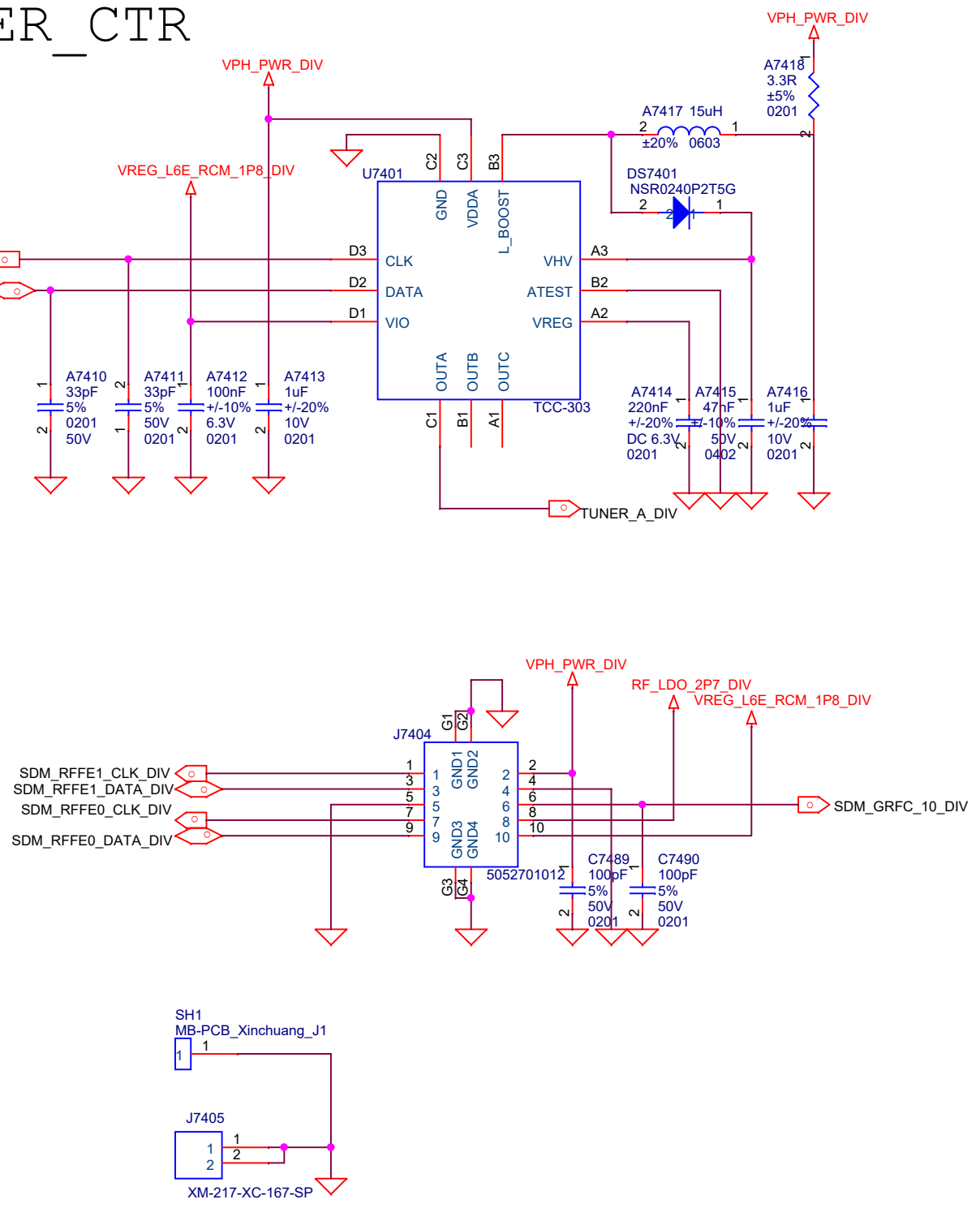
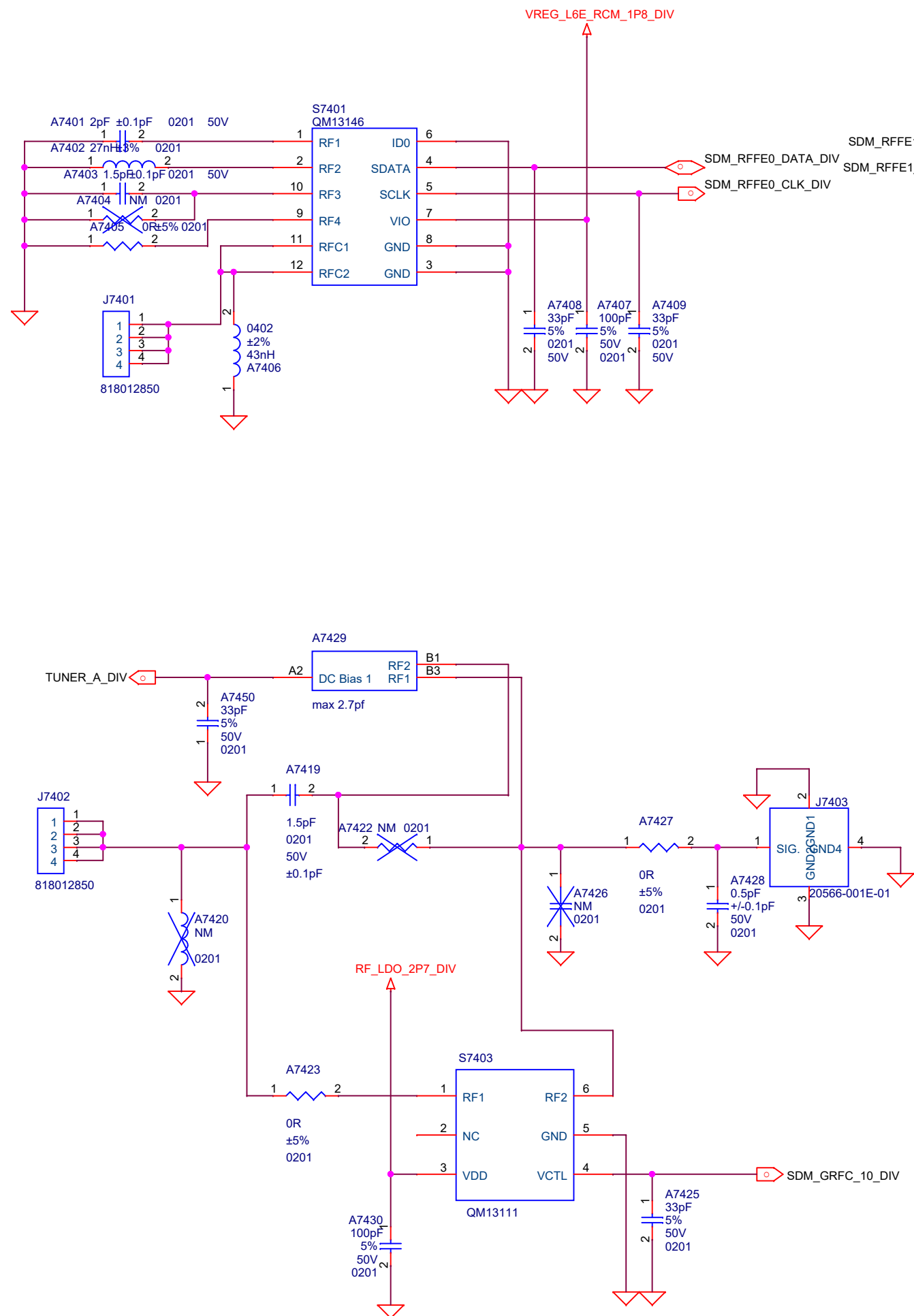
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