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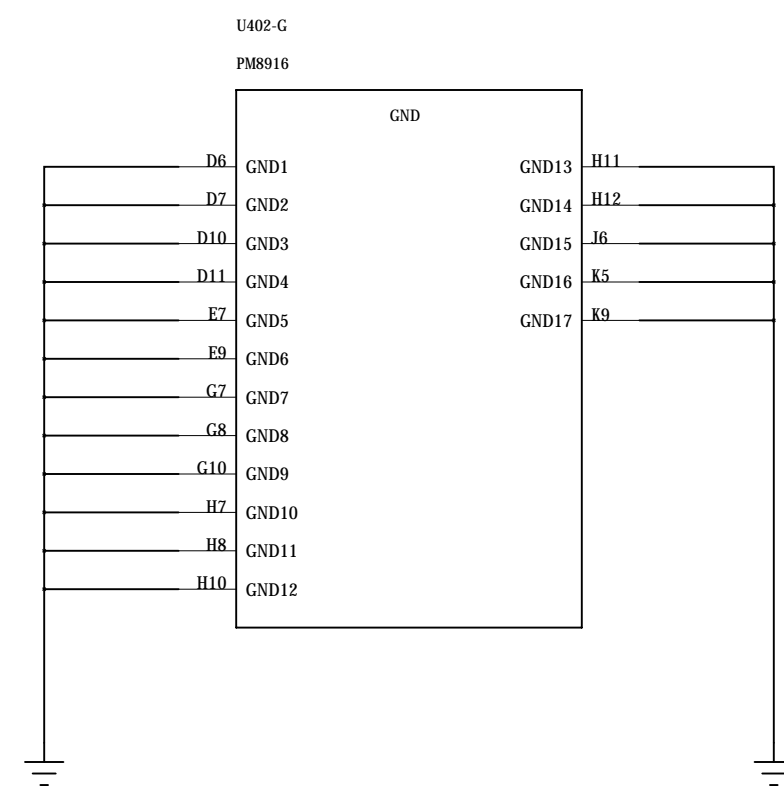
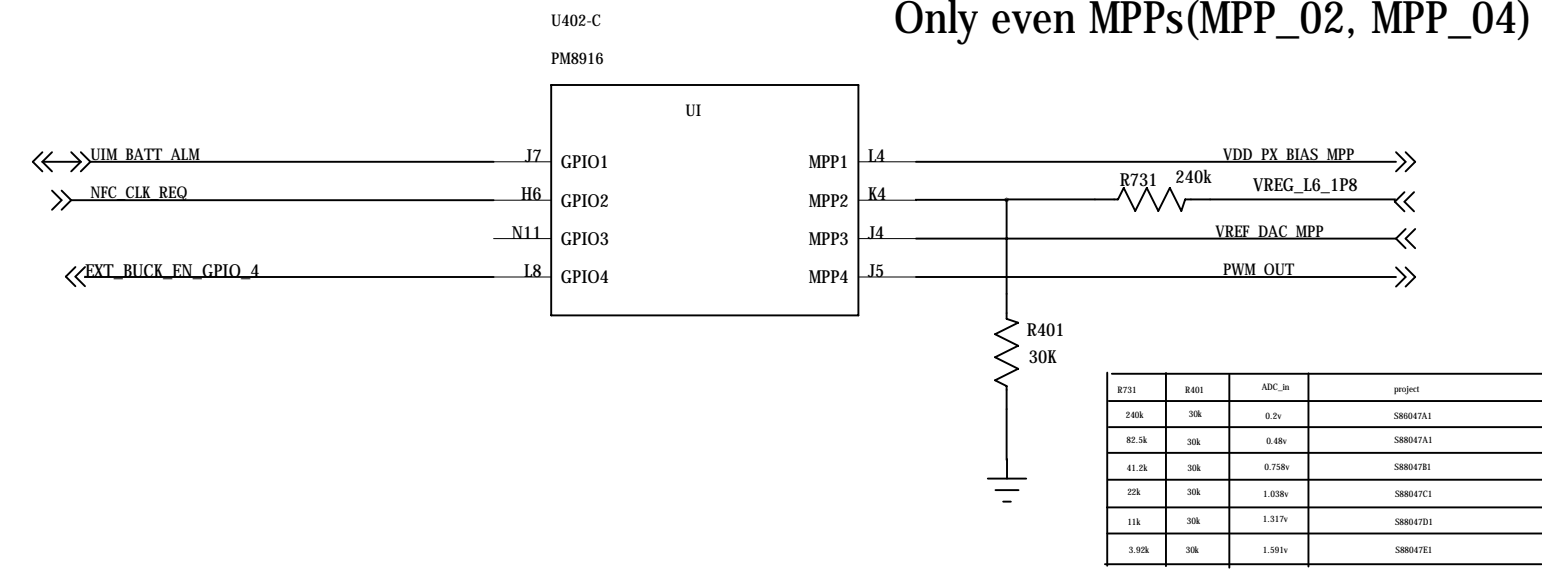
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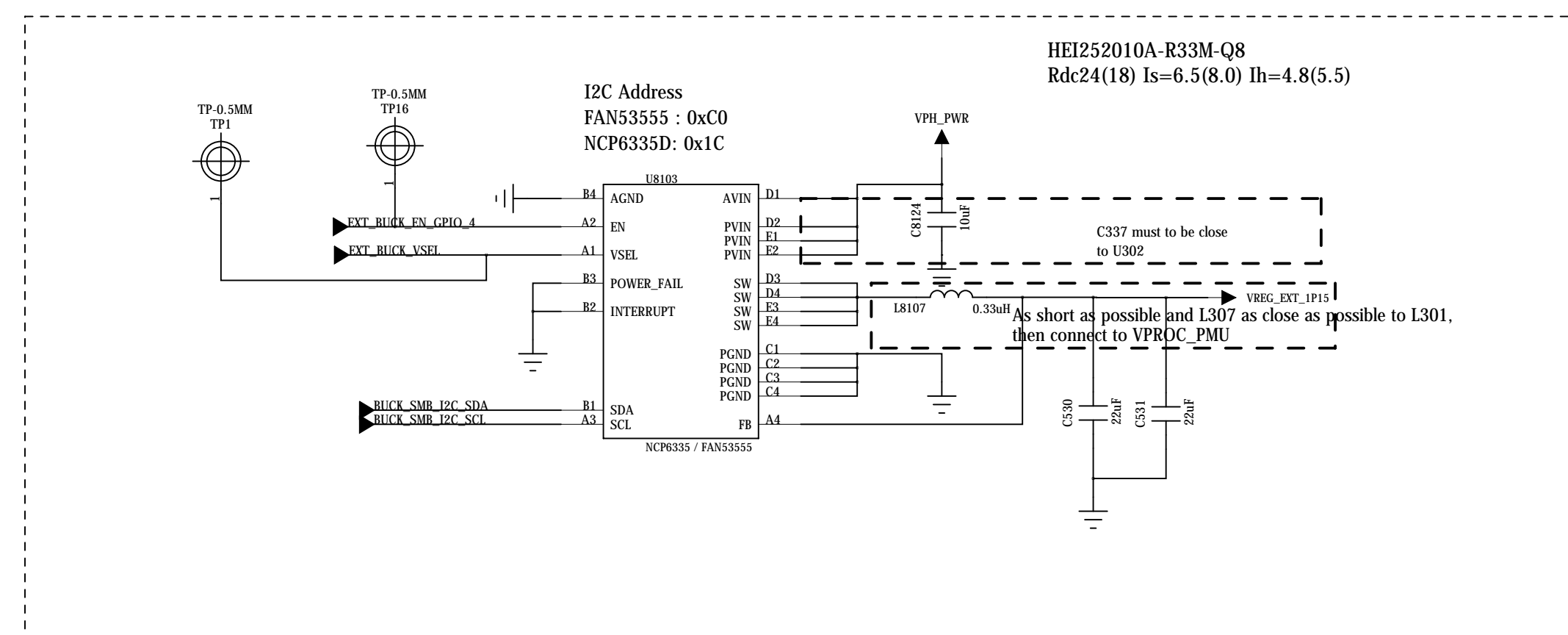
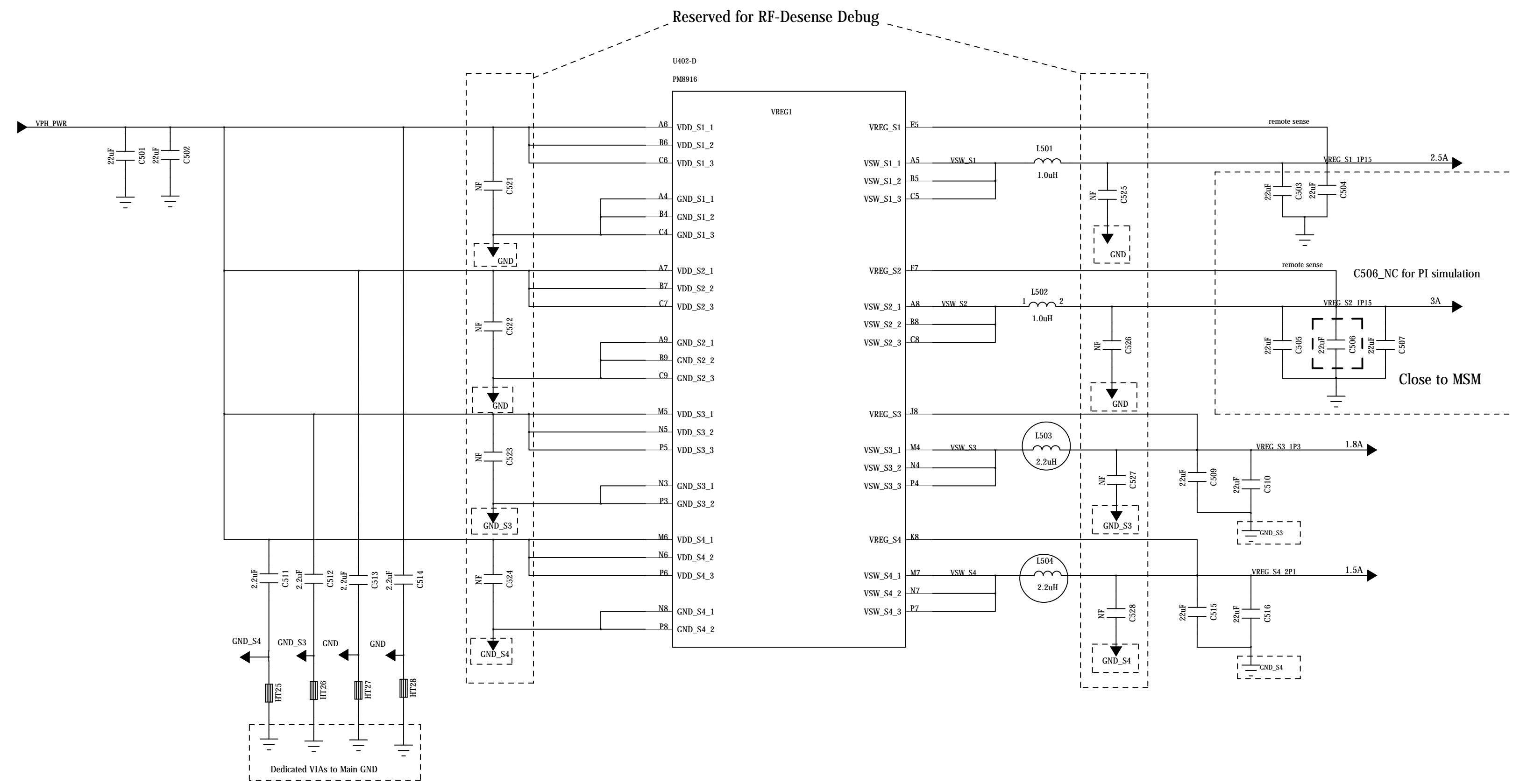
Title

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Only odd MPPs (MPP\_01, MPP\_03) can be configured as analog outputs.  
 Only even MPPs (MPP\_02, MPP\_04) have current sink capability.

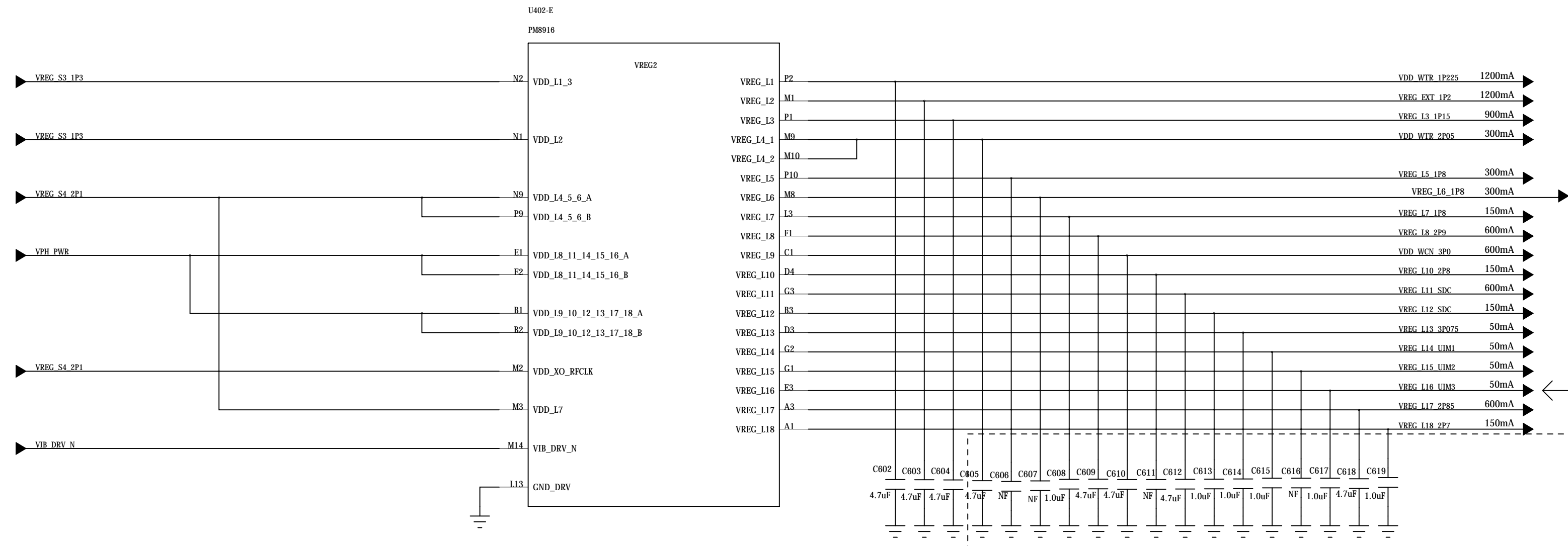




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Software Caution:  
L16 Need to Config to 1.8V and turn on later than L17

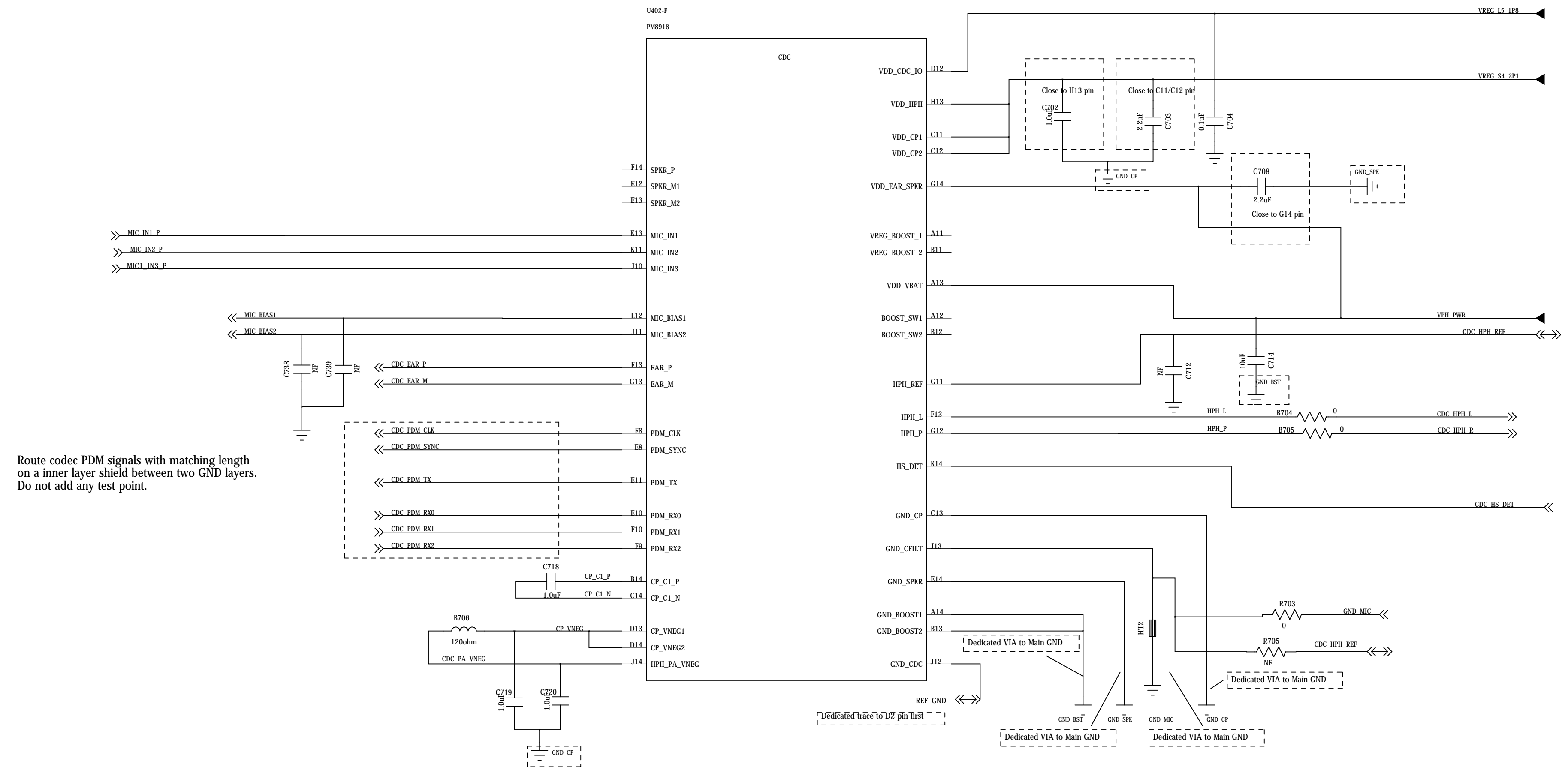
**PSEUDO CAPLESS LDOs**  
L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18

Local output capacitor can NC/Remove depends on remote load capacitors and PCB layout  
LDOs L8, L9, L11, L17 each shall have total effective output capacitance of 4.7uF.  
Please refer to PM8916 training slides(80-NK808-21) for limits on LDO output trace resistance and inductance  
Rest of the LDOs shall each have total effective output capacitance of 1.0uF.

The Pseudo capless LDOs must comply to following tolerable routing requirement:  
P50: R<400mOhms, L<45nH  
P150: R<200mOhms, L<20nH  
P300: R<150mOhms, L<18nH  
P600: R<150mOhms, L<18nH

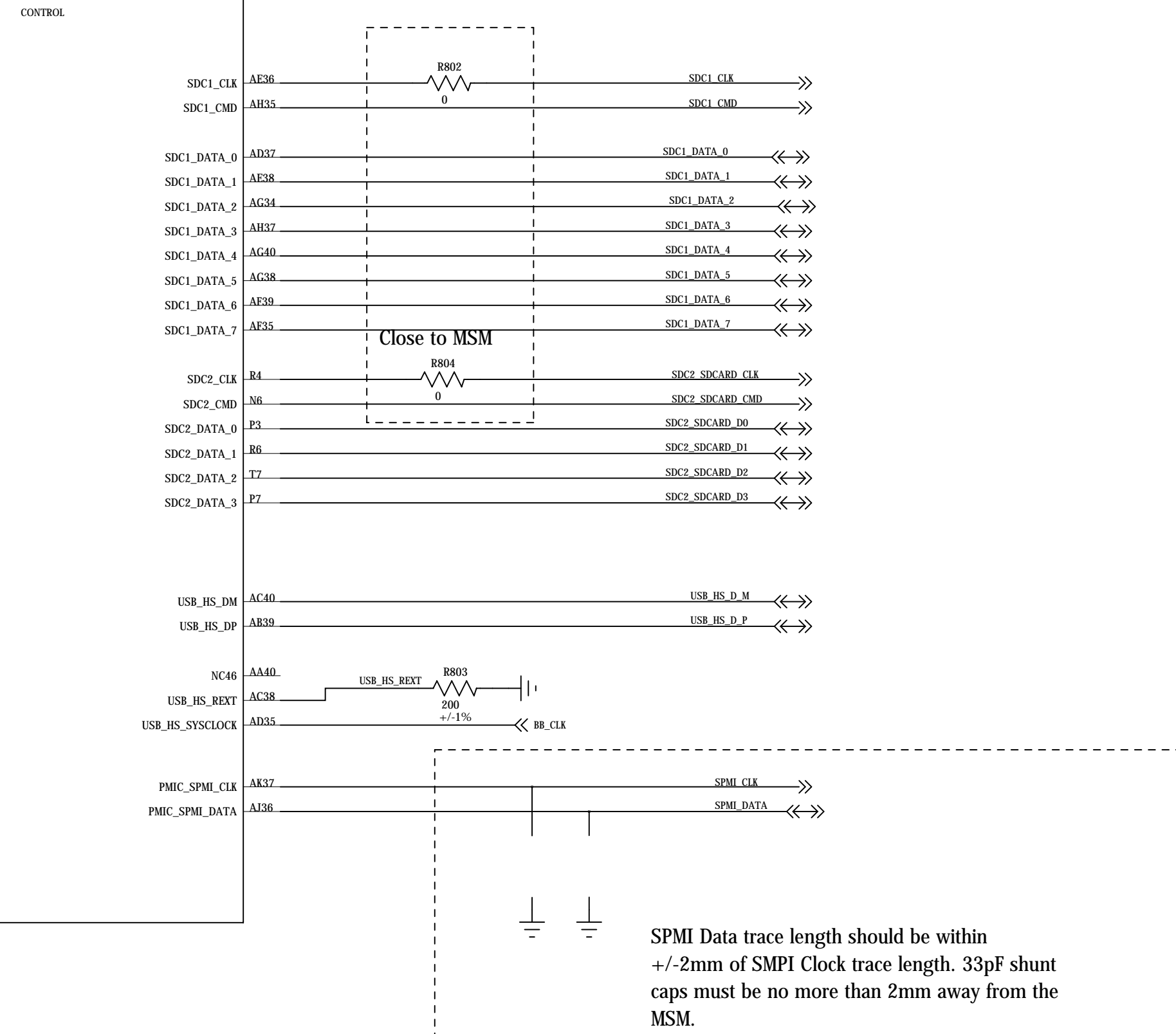
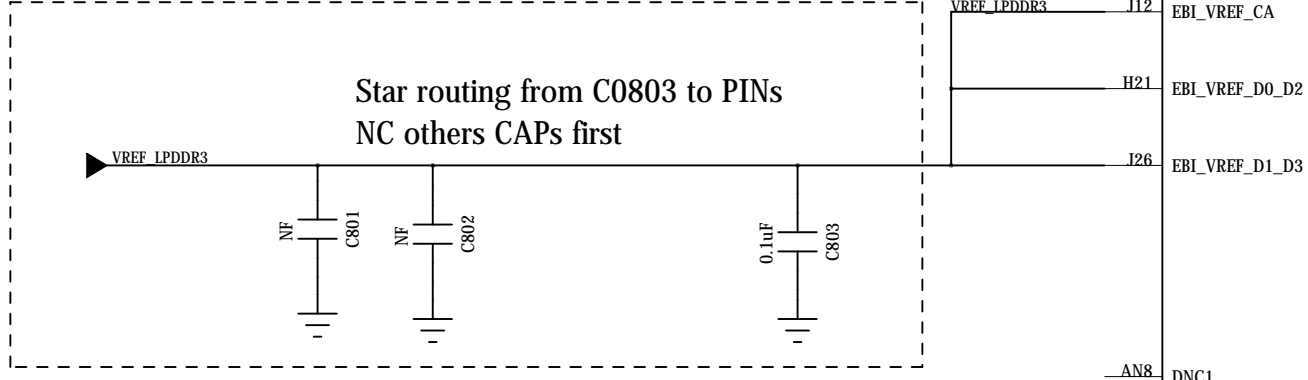
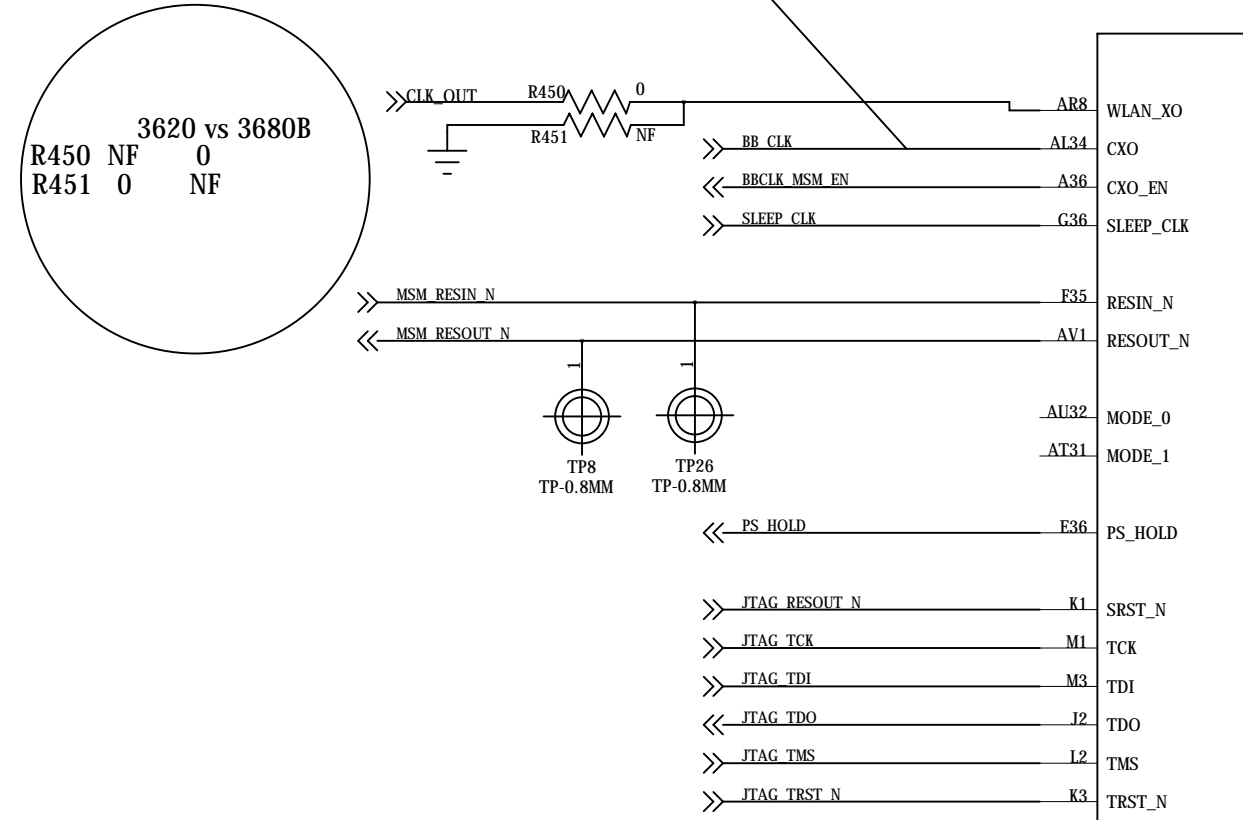
Please ensure when you DNI the output capacitor of Pseudo capless LDOs  
the effective total capacitance at load side shall match above requirement

NC first



Route codec PDM signals with matching length on an inner layer shield between two GND layers. Do not add any test point.

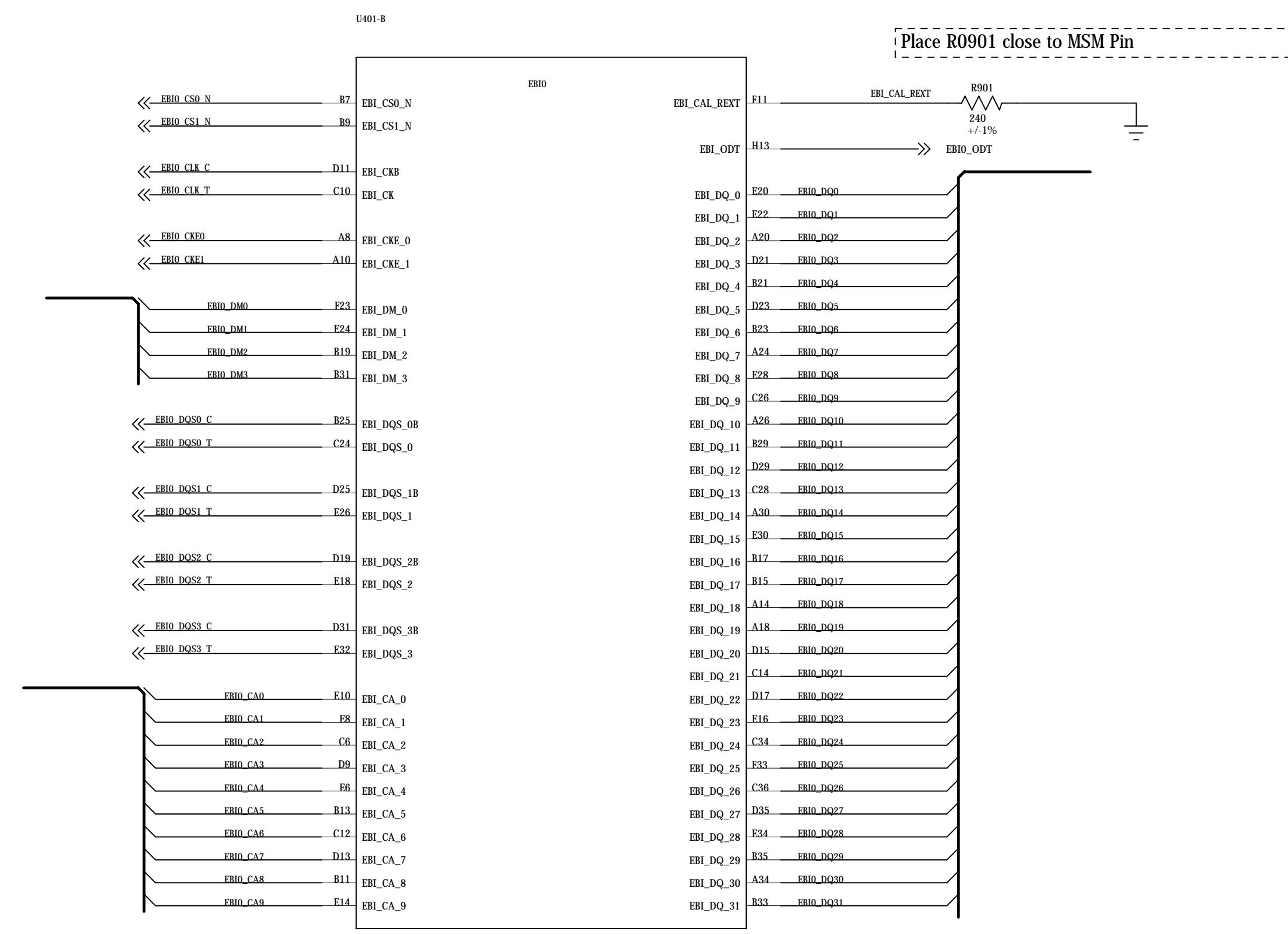
For BBCLK1,AD35 will be the first load and AL34 will be the final load  
Should be a daisy chain route



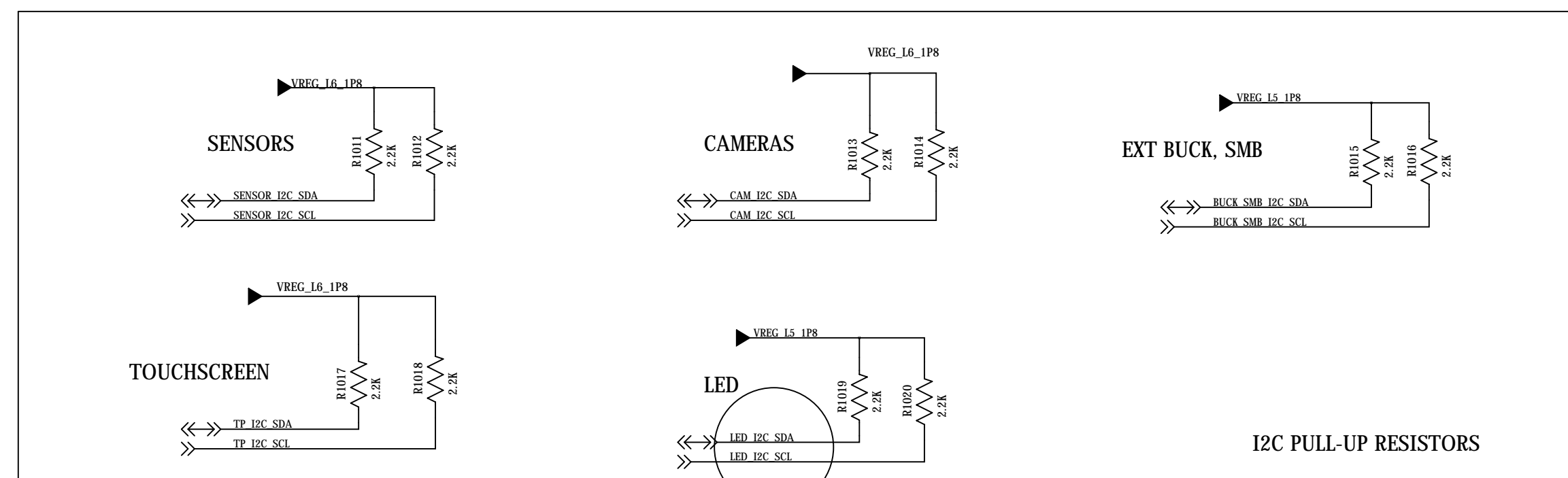
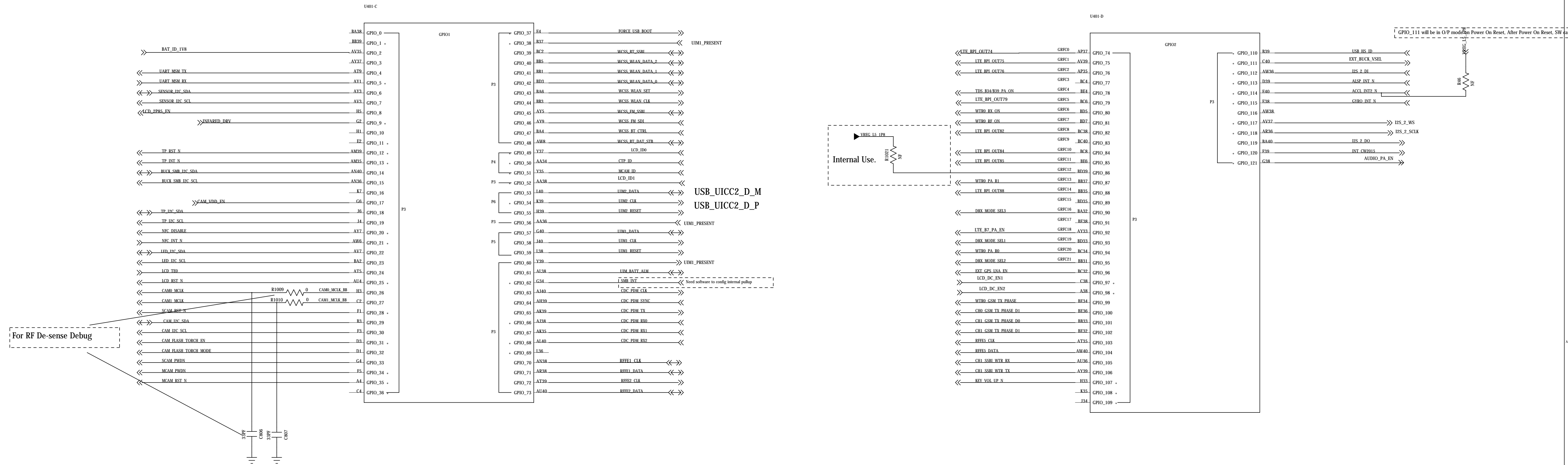
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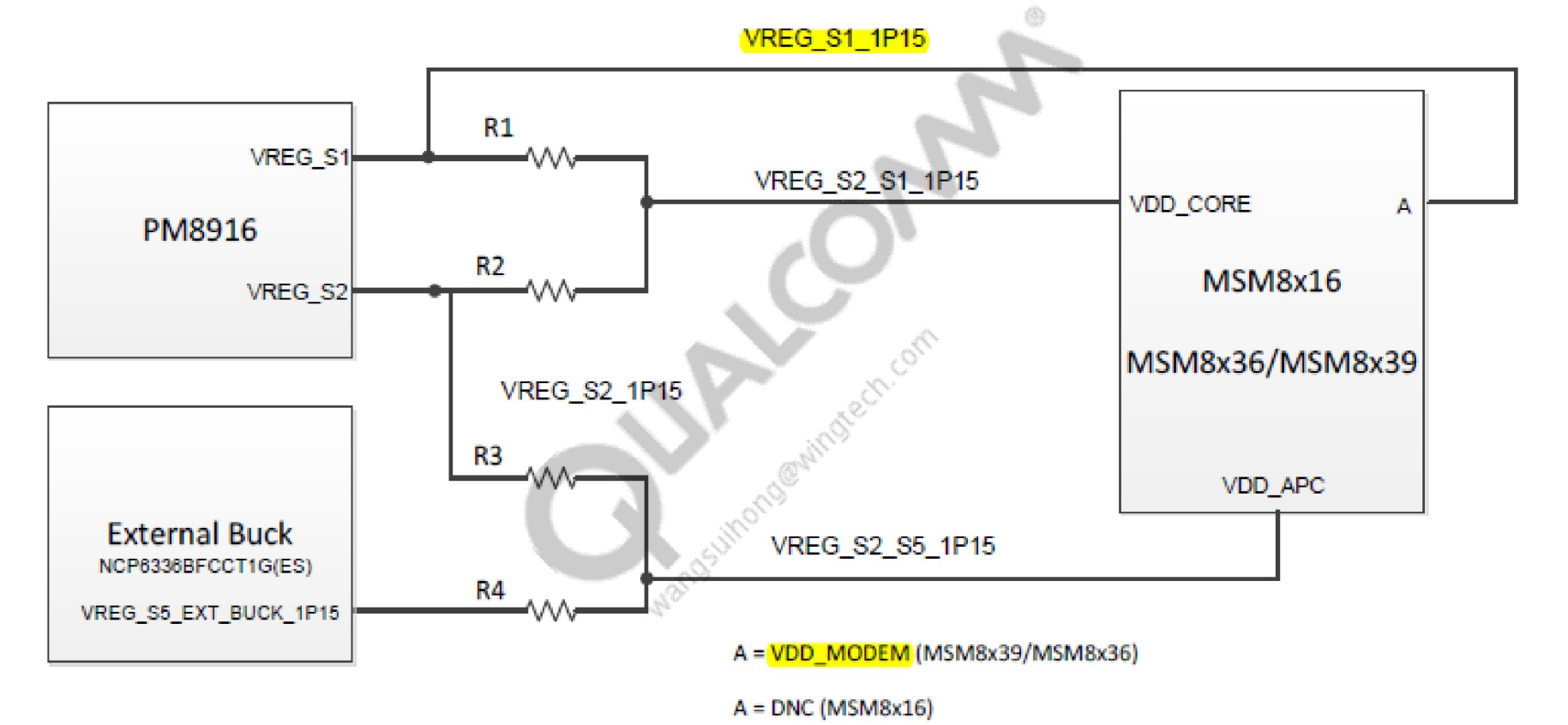
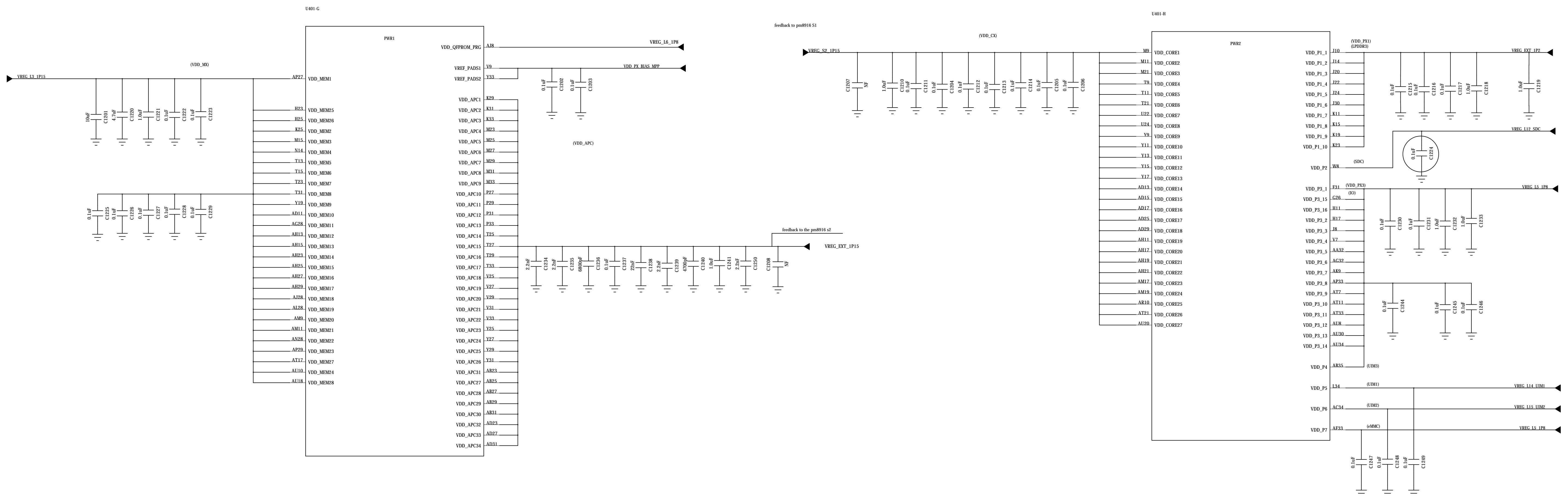


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A = VDD\_MODEM (MSM8x39/MSM8x36)  
 A = DNC (MSM8x16)

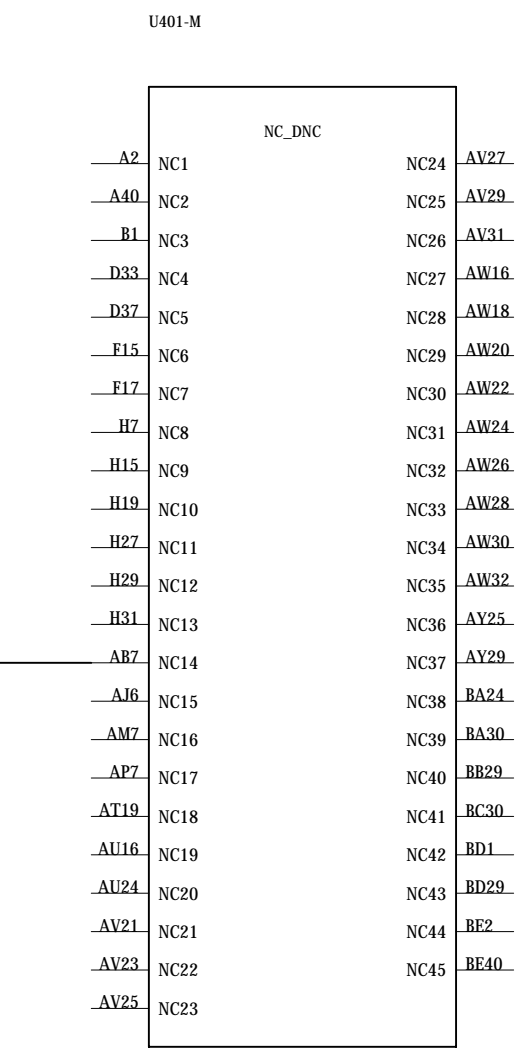
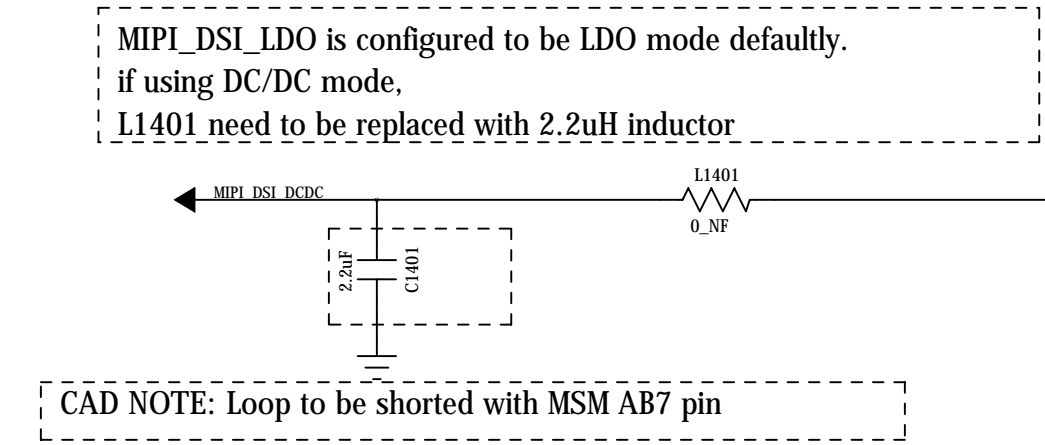
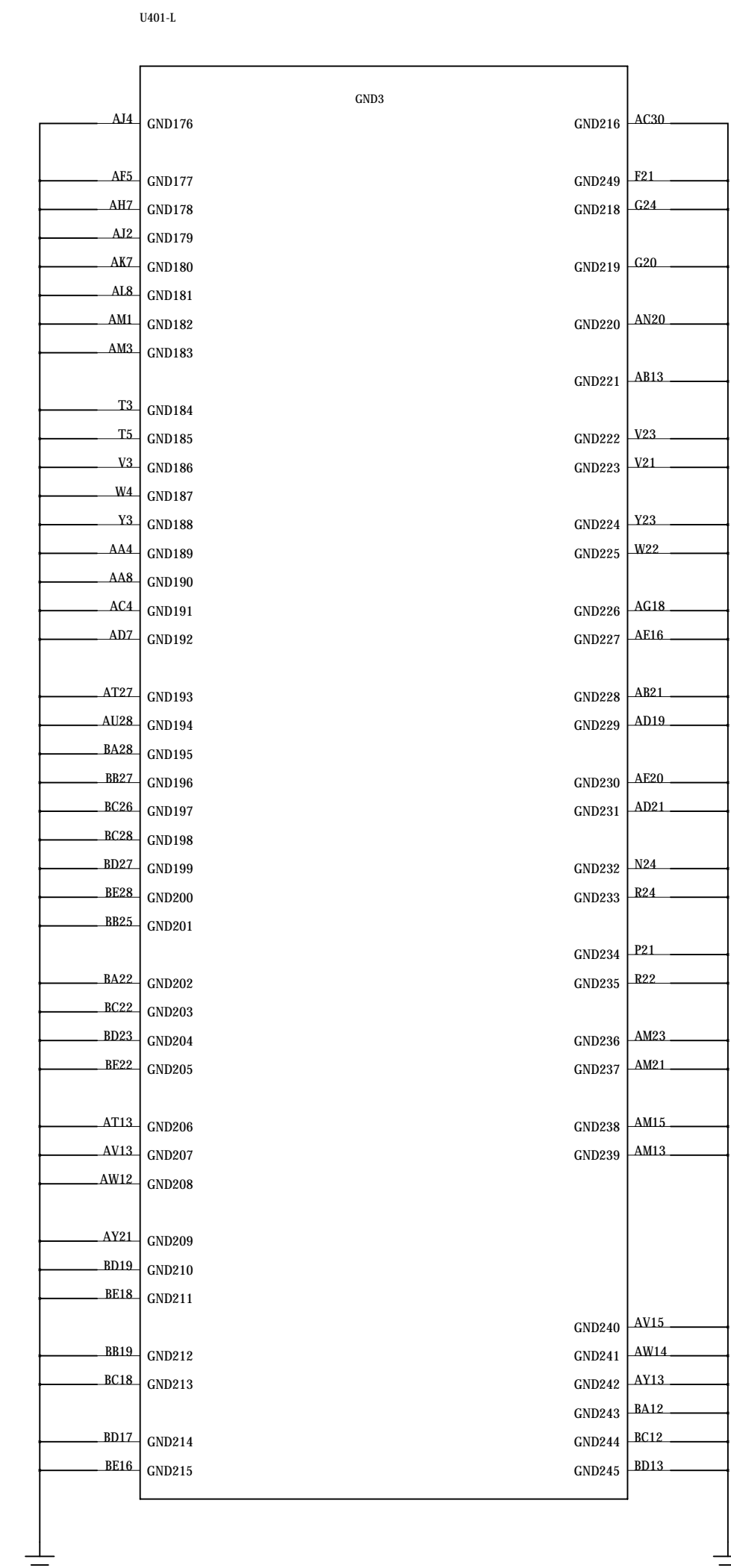
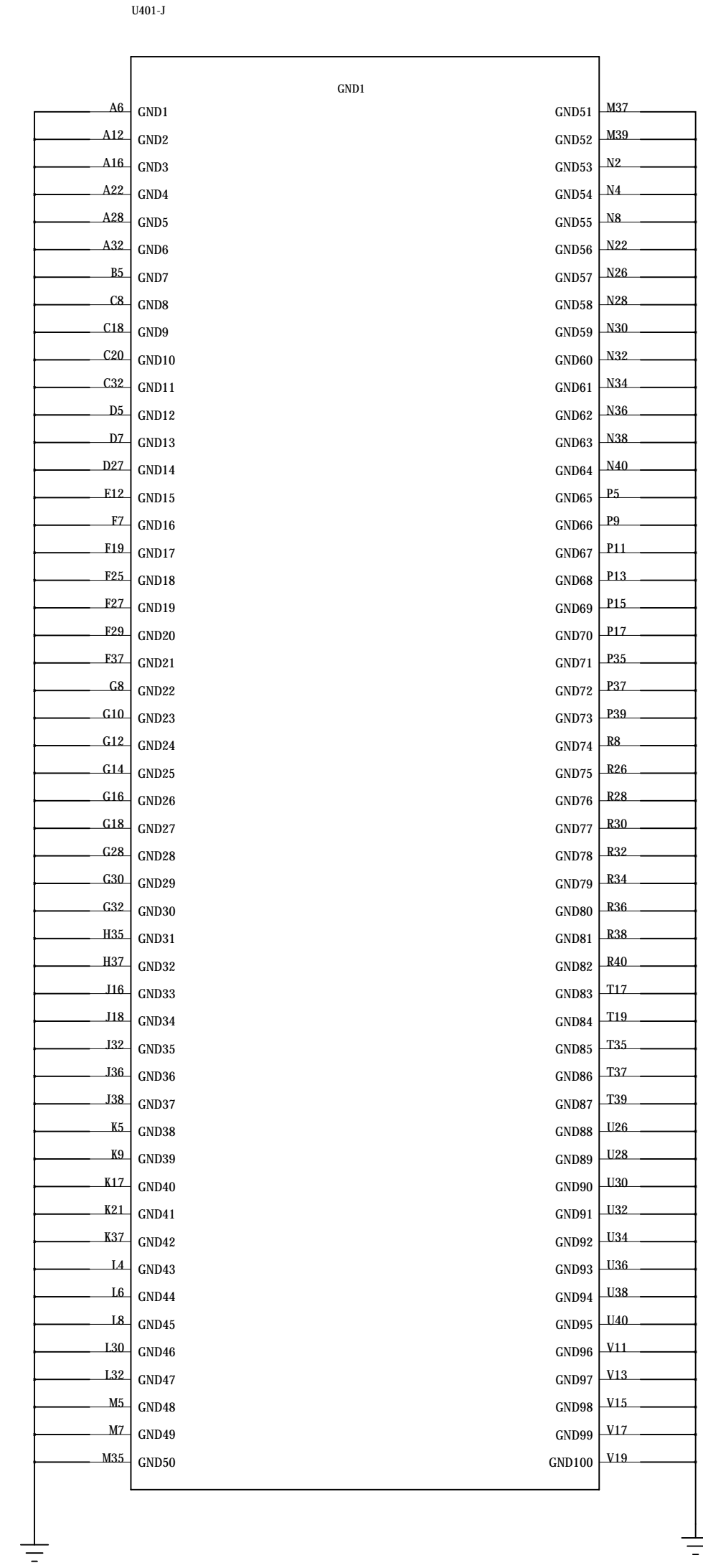
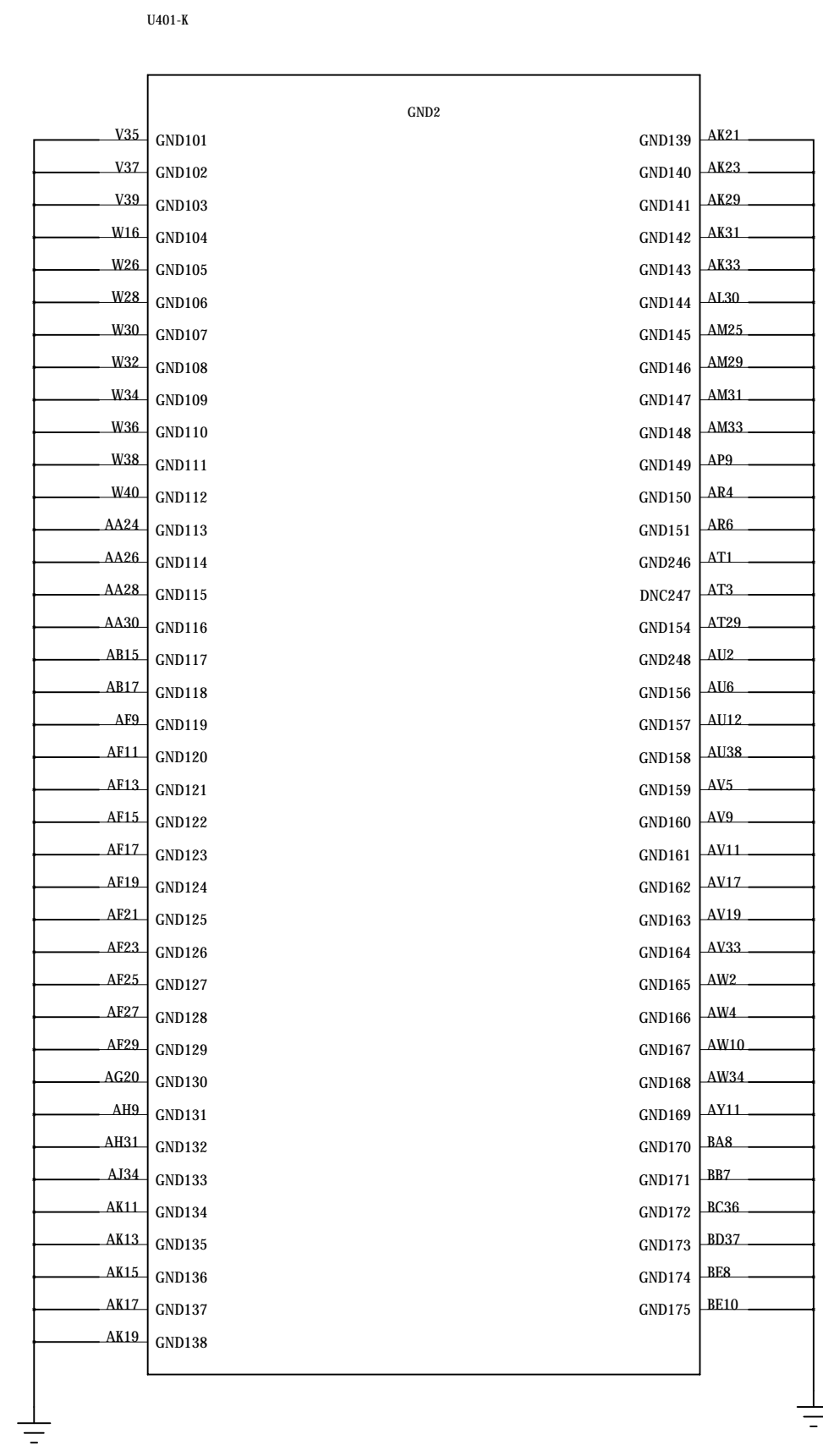
| SoC             | Jumper on | Jumper off |
|-----------------|-----------|------------|
| MSM8x16         | R1, R3    | R2, R4     |
| MSM8x36/MSM8x39 | R2, R4    | R1, R3     |

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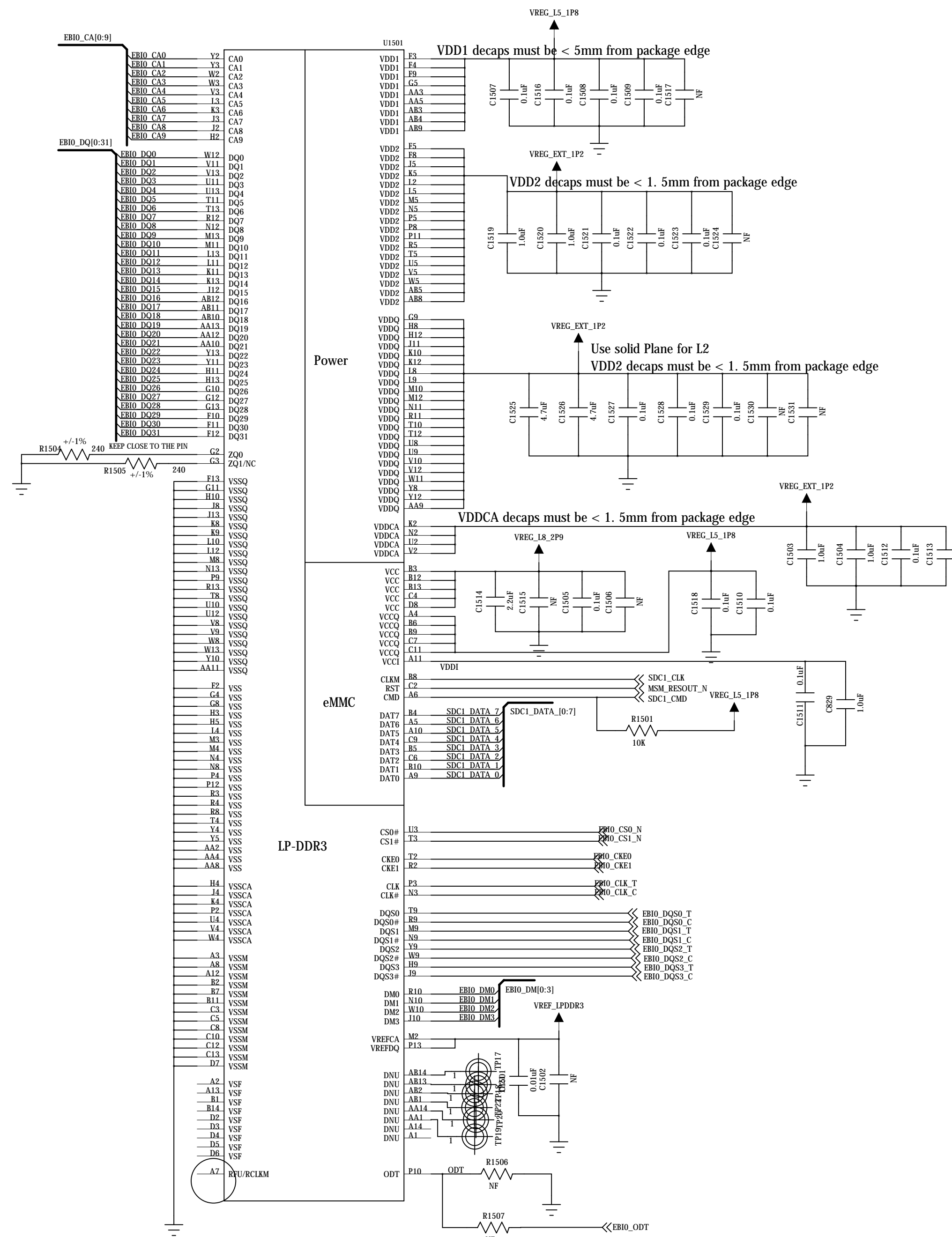
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|          | MICRO/HYNIX | SAMSUNG |
|----------|-------------|---------|
| U1501.G3 | ZQ1         | NC      |
| U1501.A7 | RFU         | RCLK    |

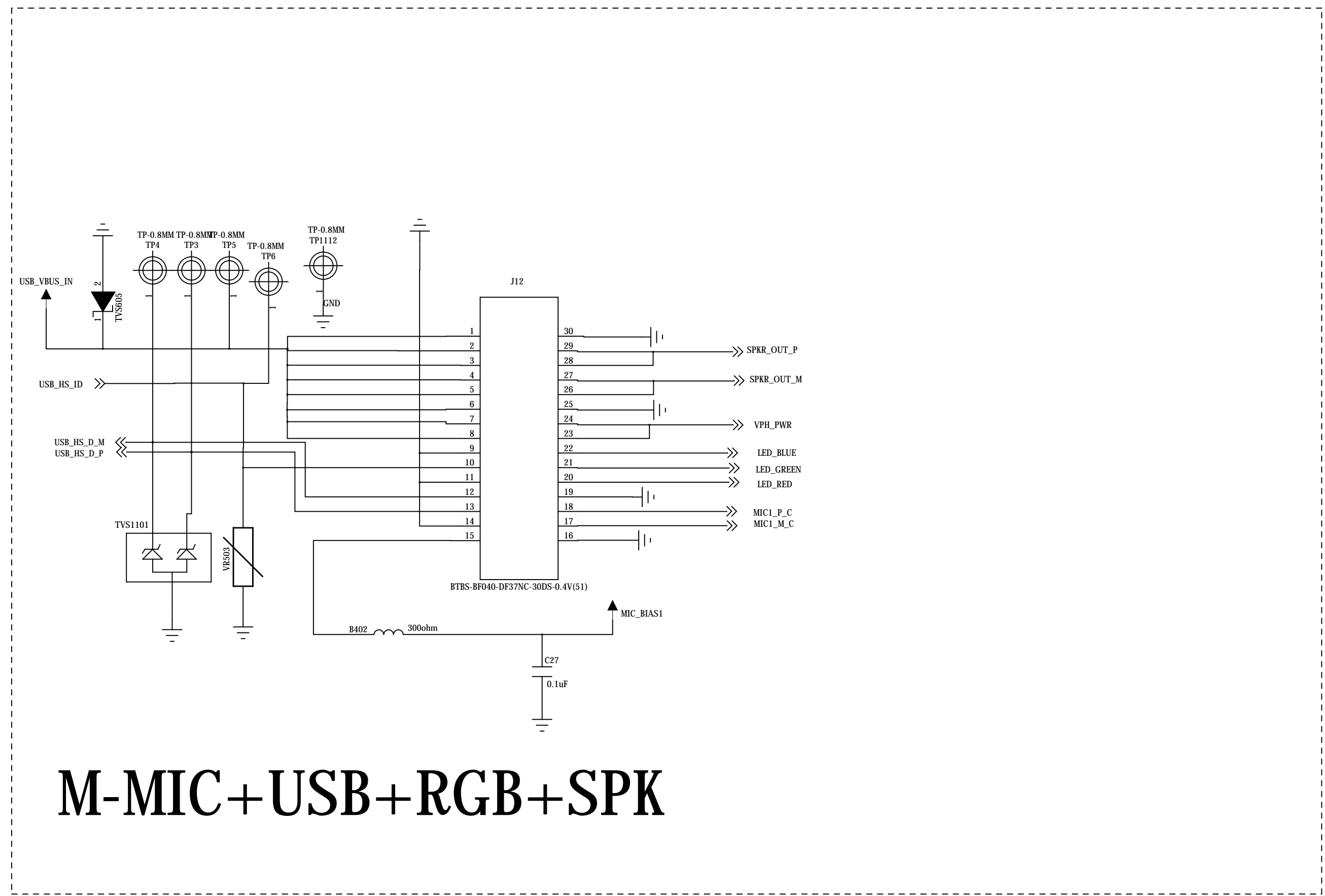


Note: Pull-up resistors on SDC1\_DATA are PCB and eMMC vender dependent

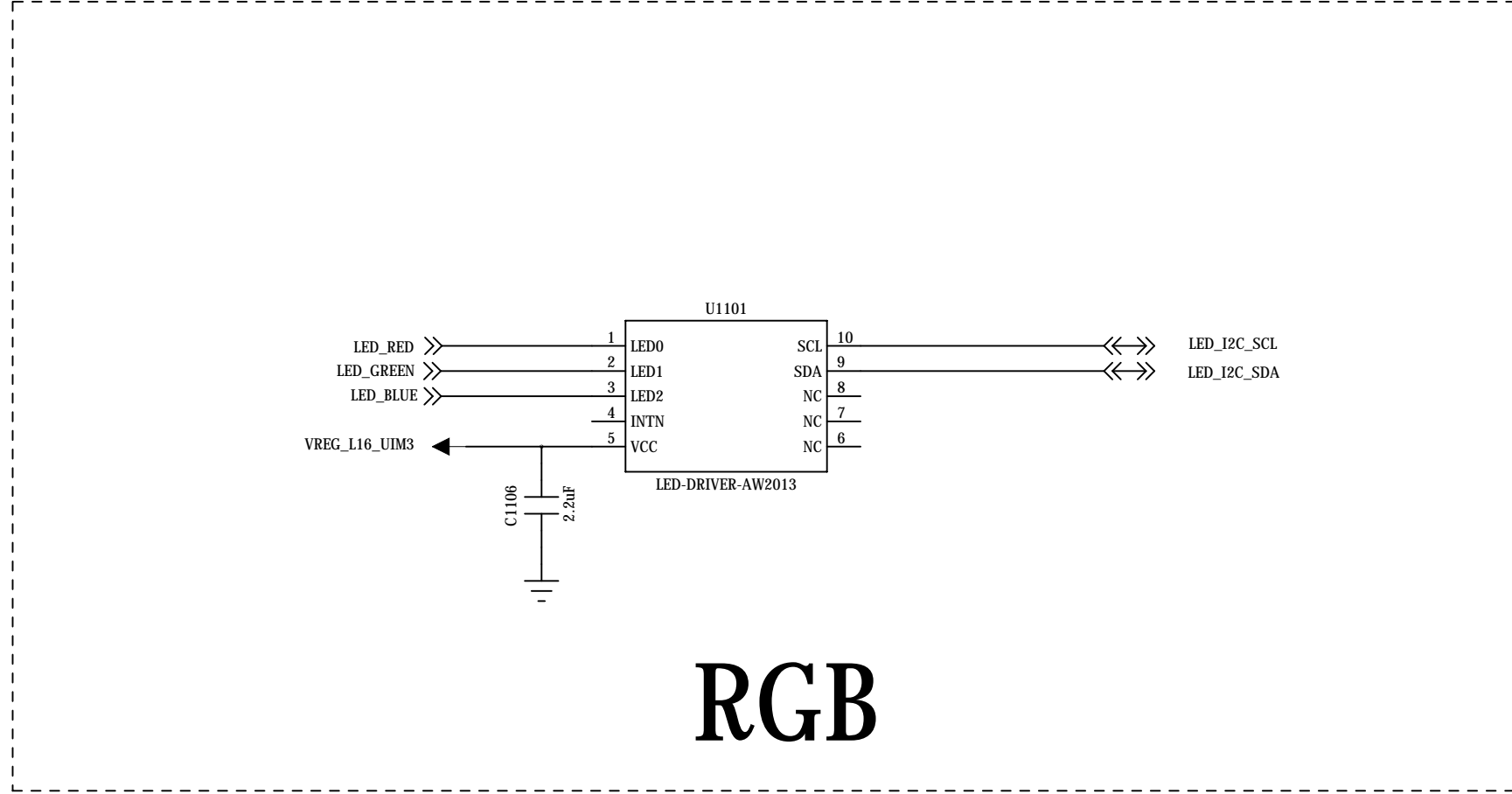
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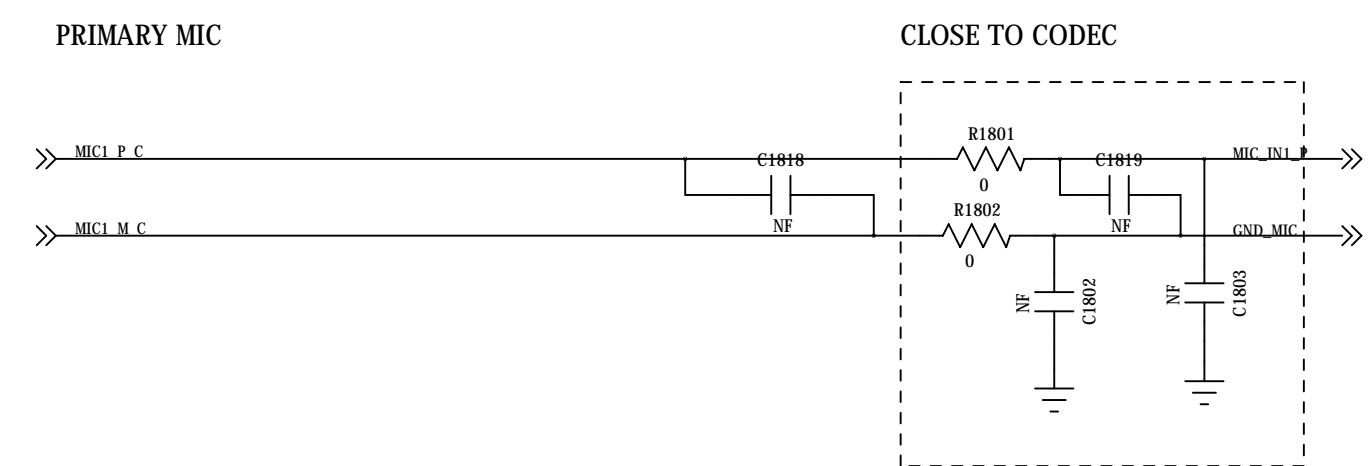
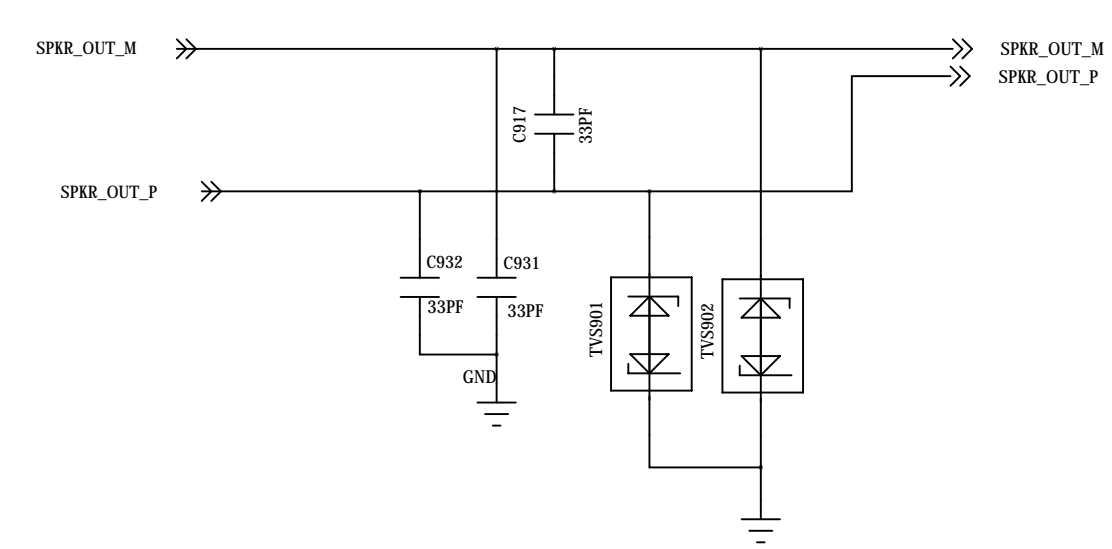
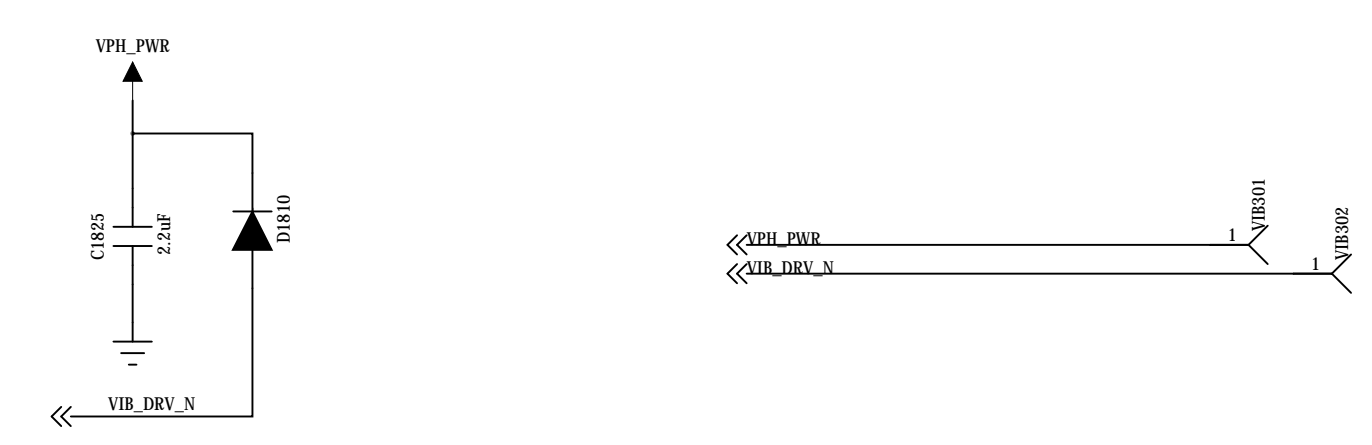
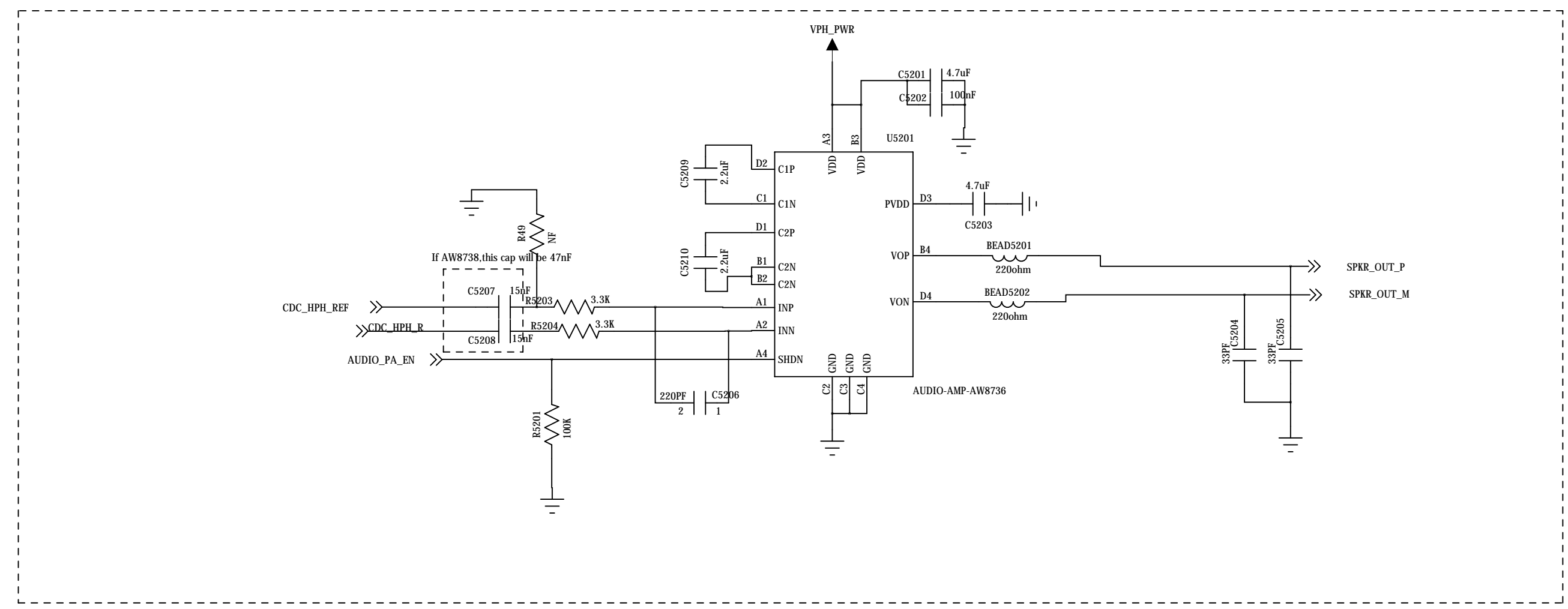
**M-MIC+USB+RGB+SPK**



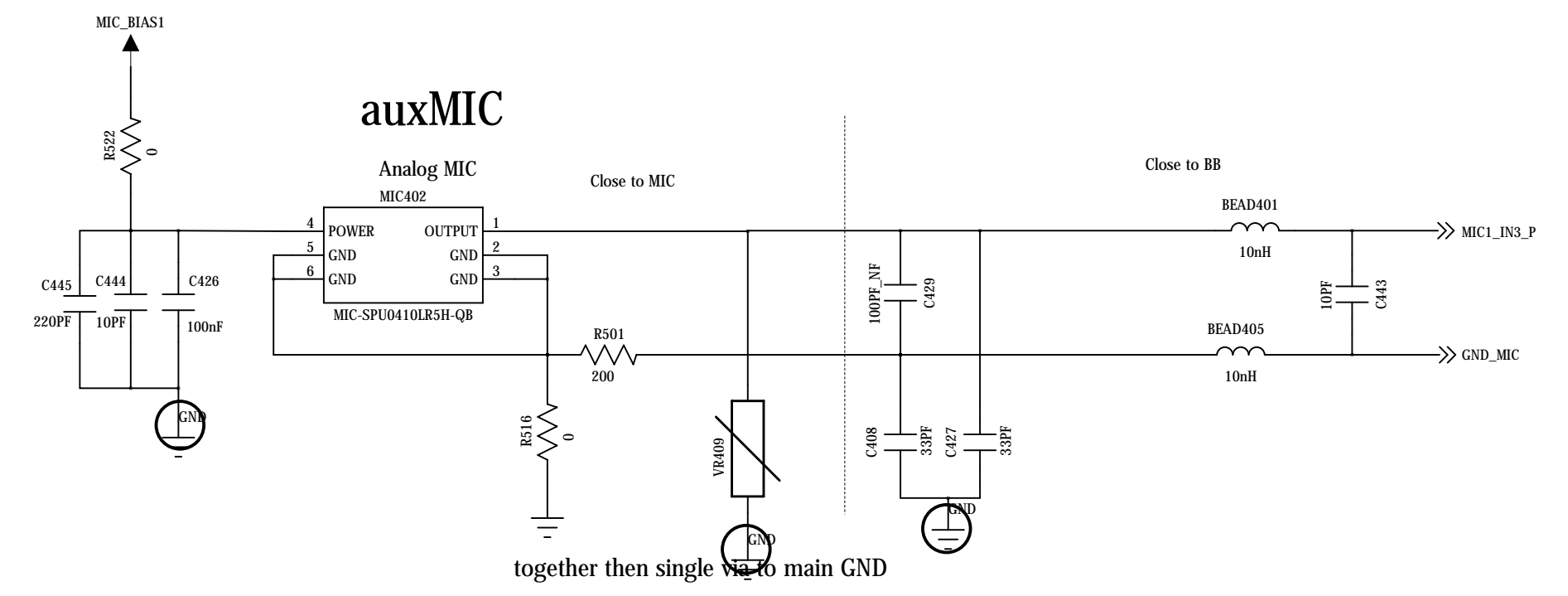
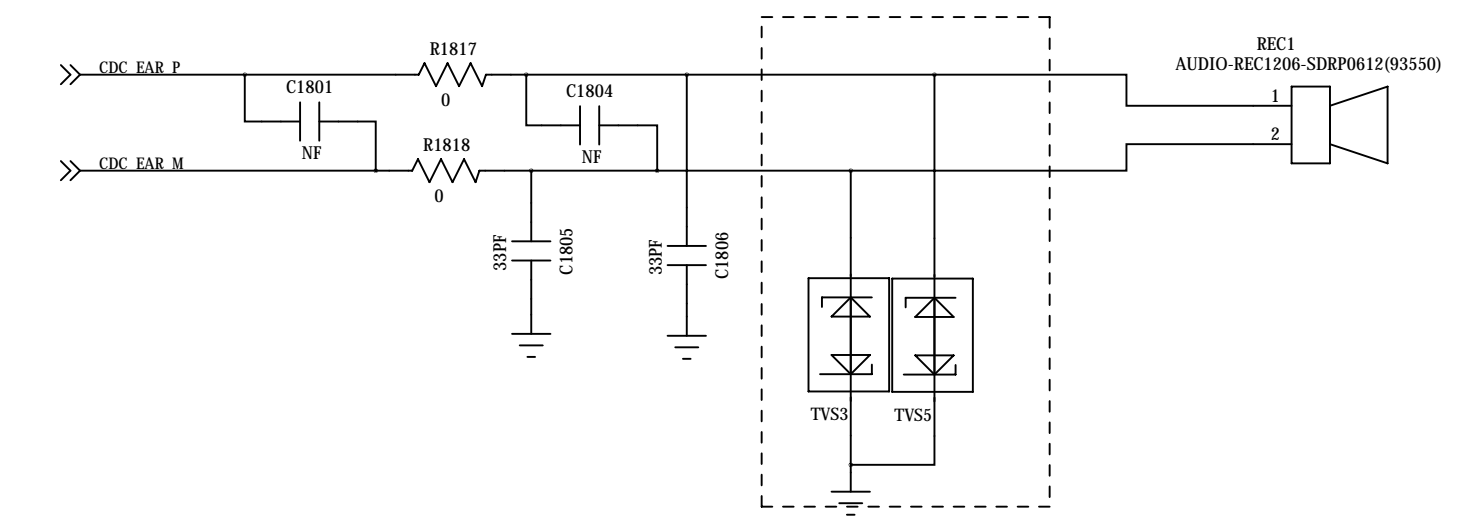
**RGB**

| I2C Address |        |
|-------------|--------|
| Write       | 8B0x8A |
| Read        | 8B0x8B |

Power on sequence: can be applied in any order

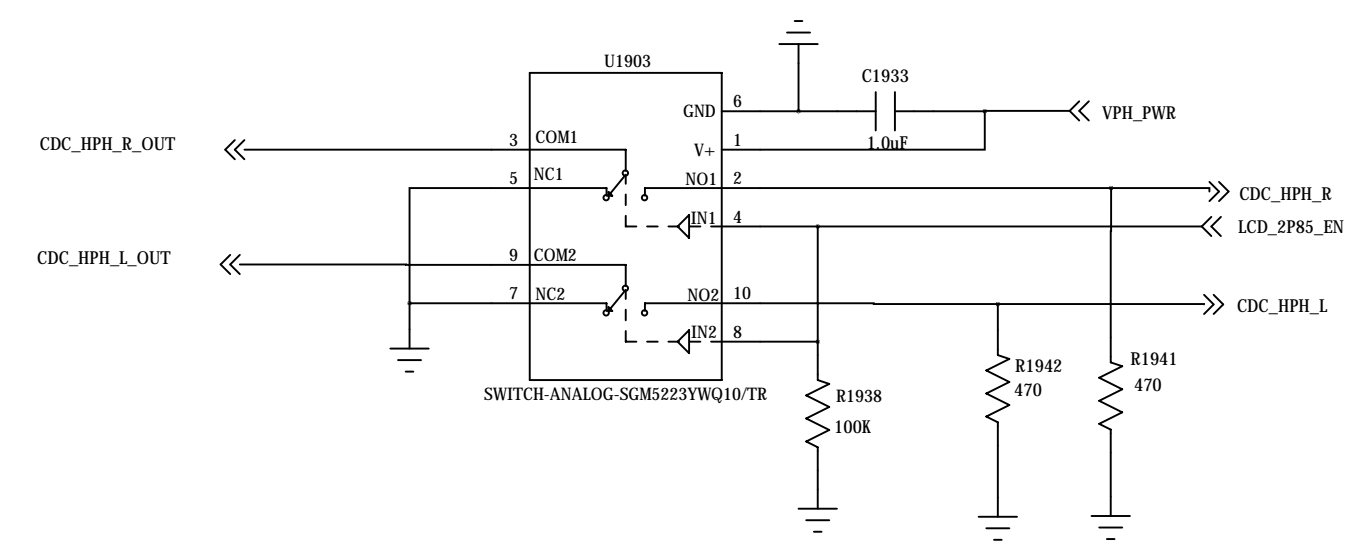
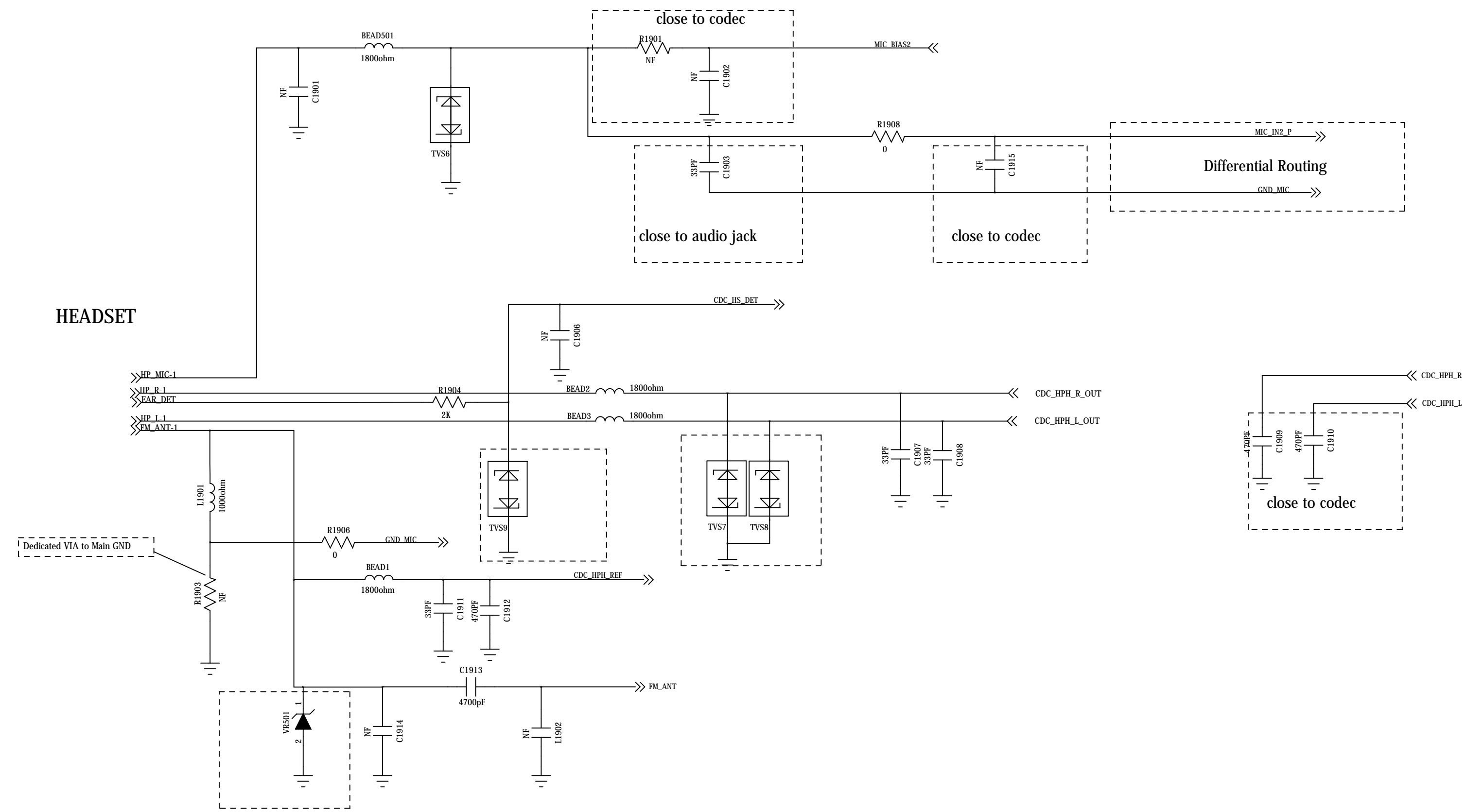
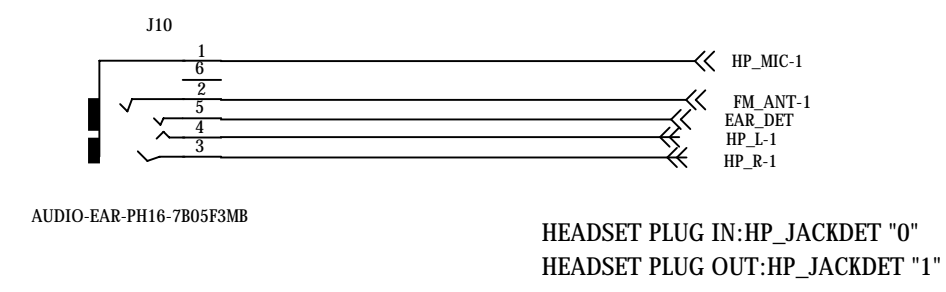


RECEIVER



together then single wire to main GND



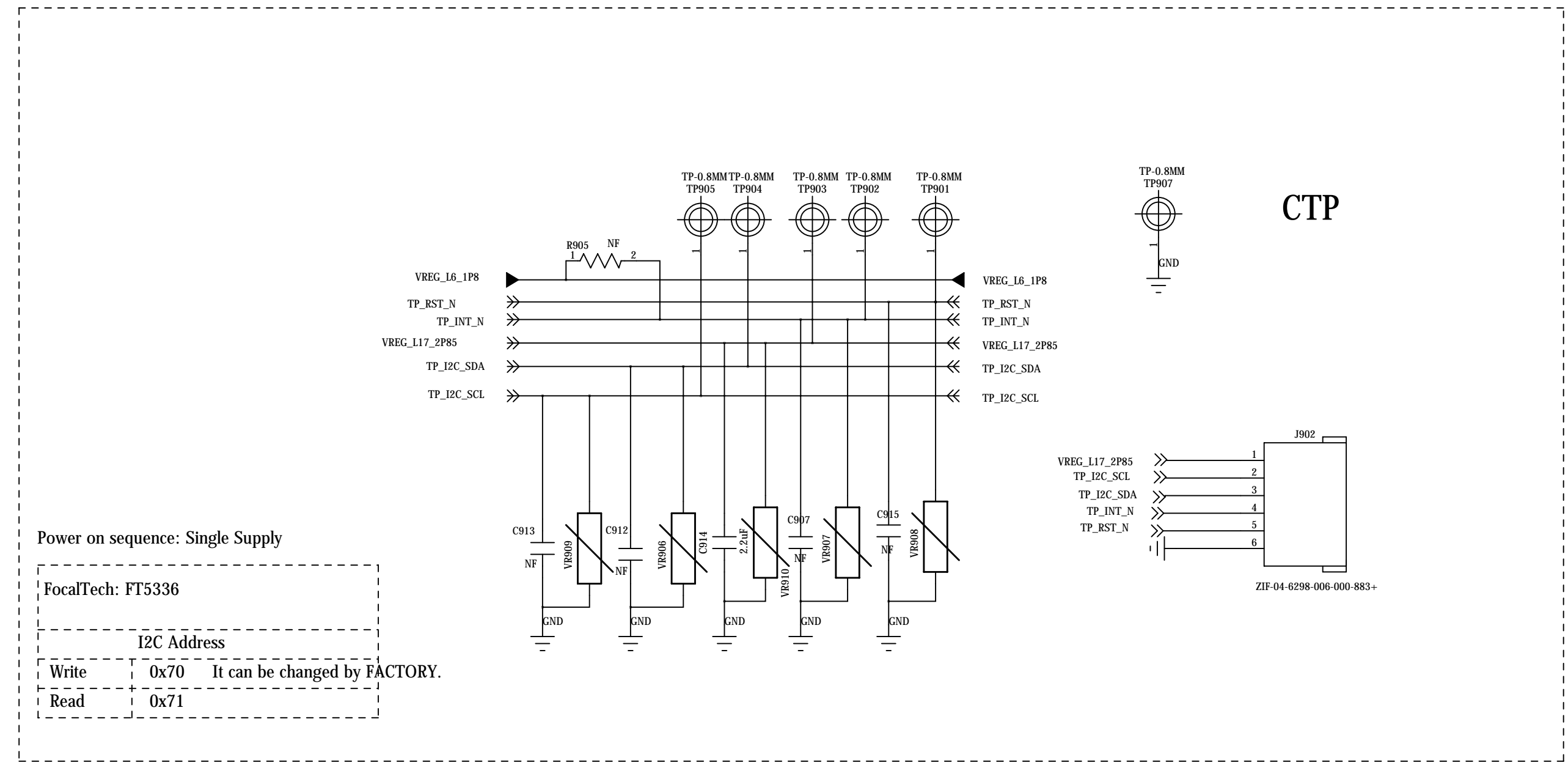


IN=0, COM Connected to NC;  
IN=1, COM Connected to NO;

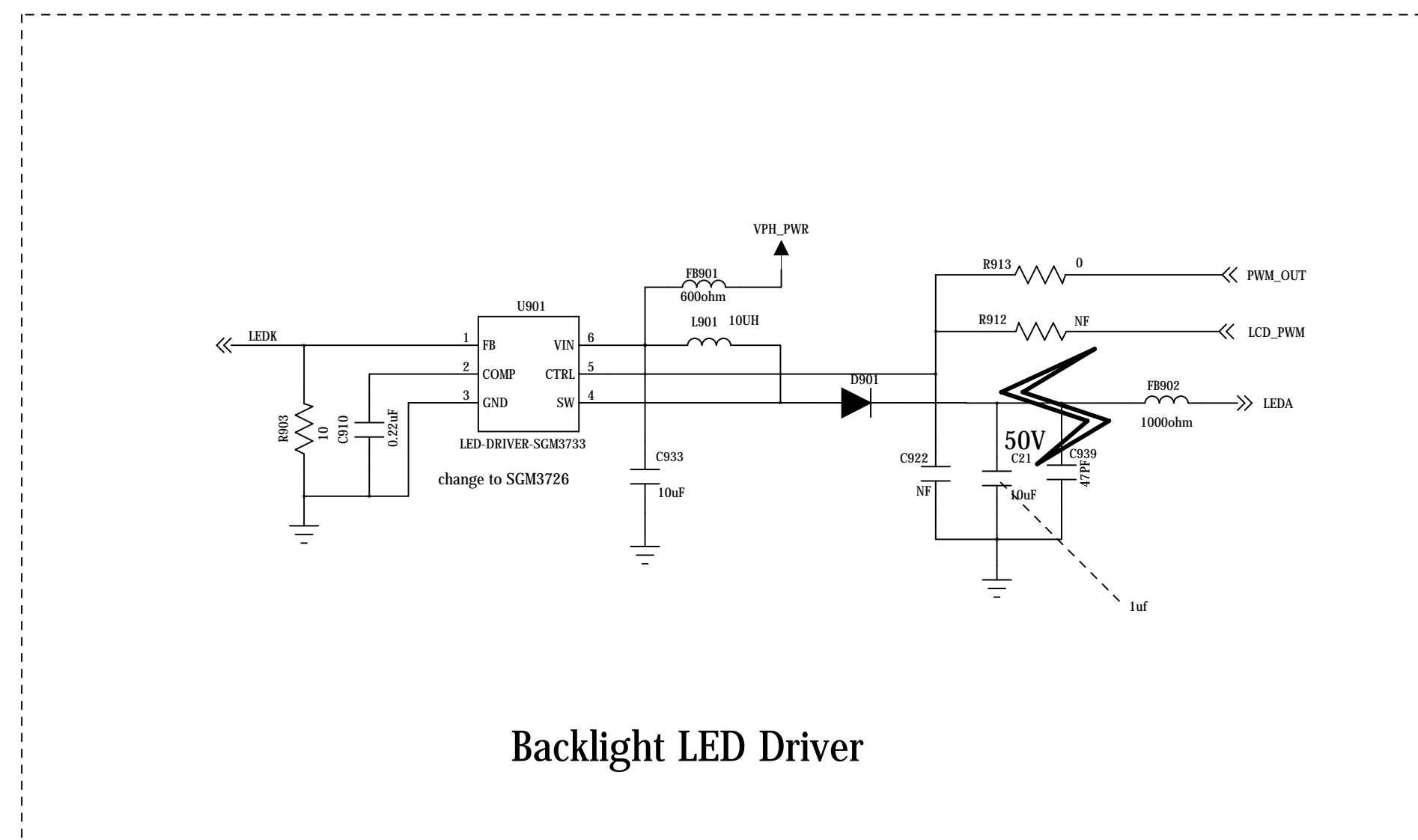
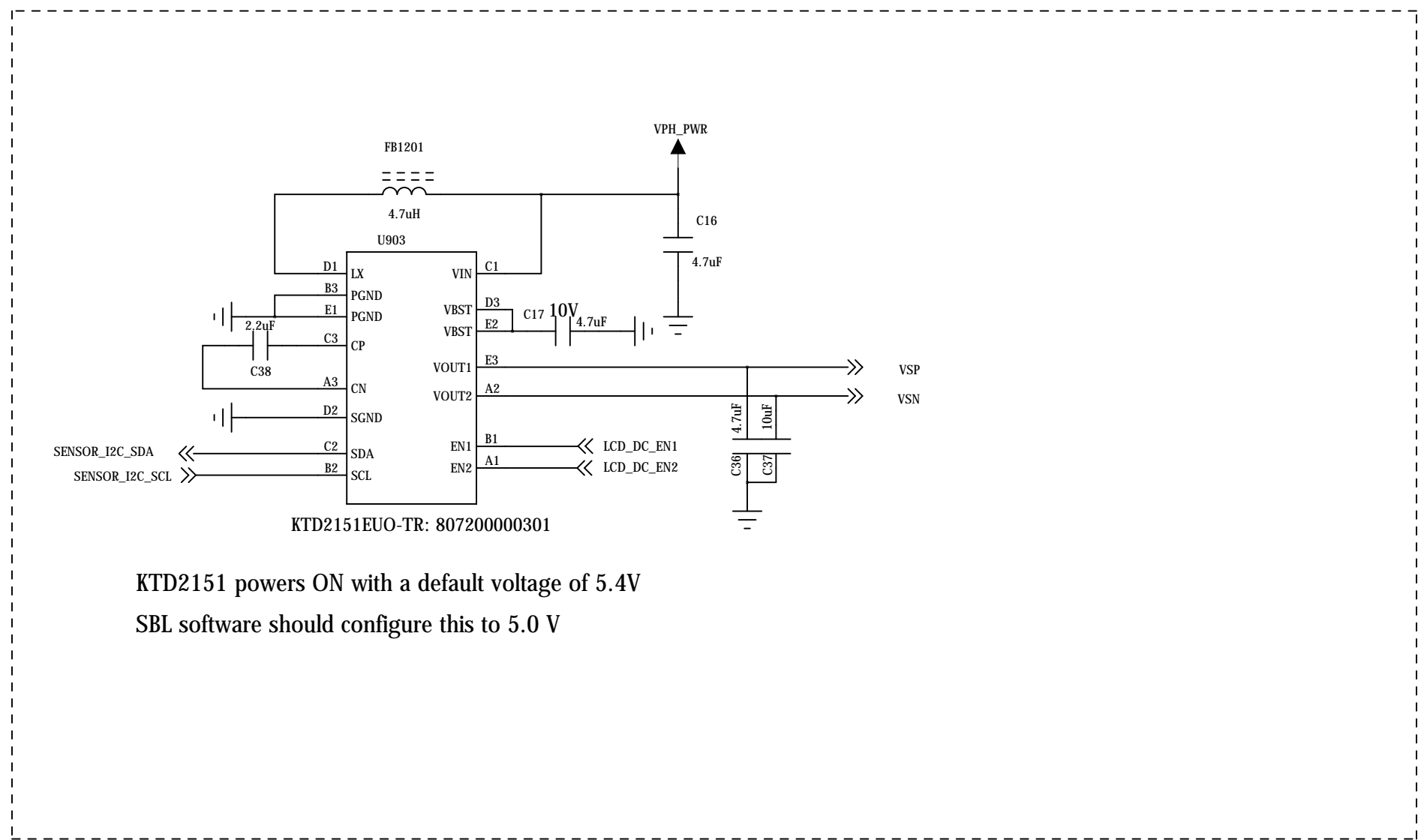
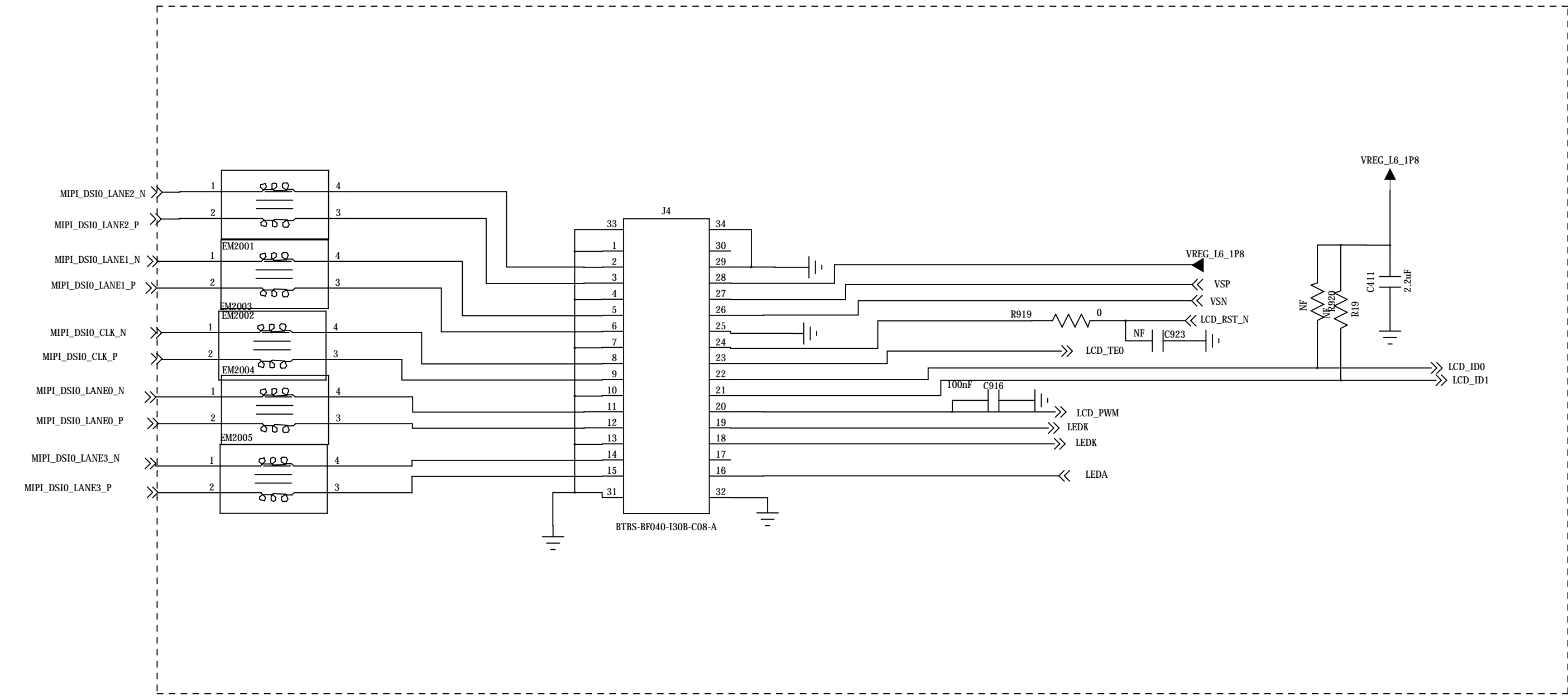
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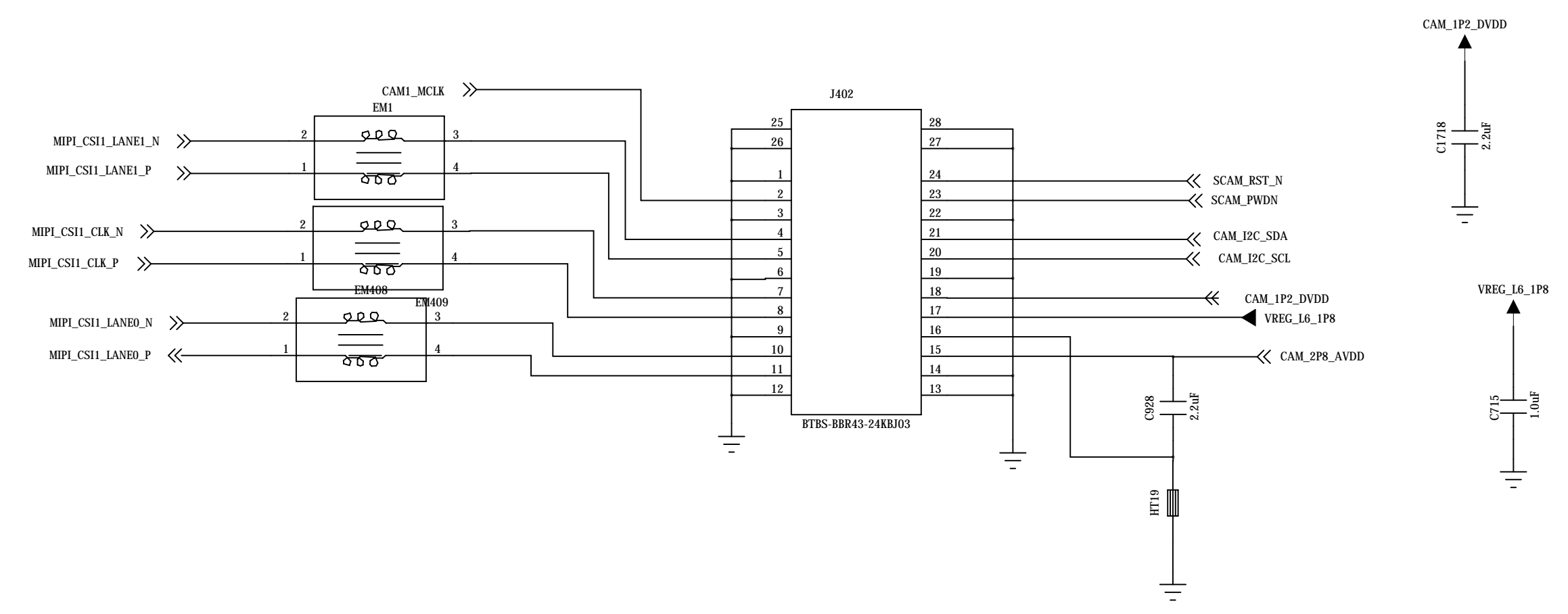


LCD  
5.0" FHD



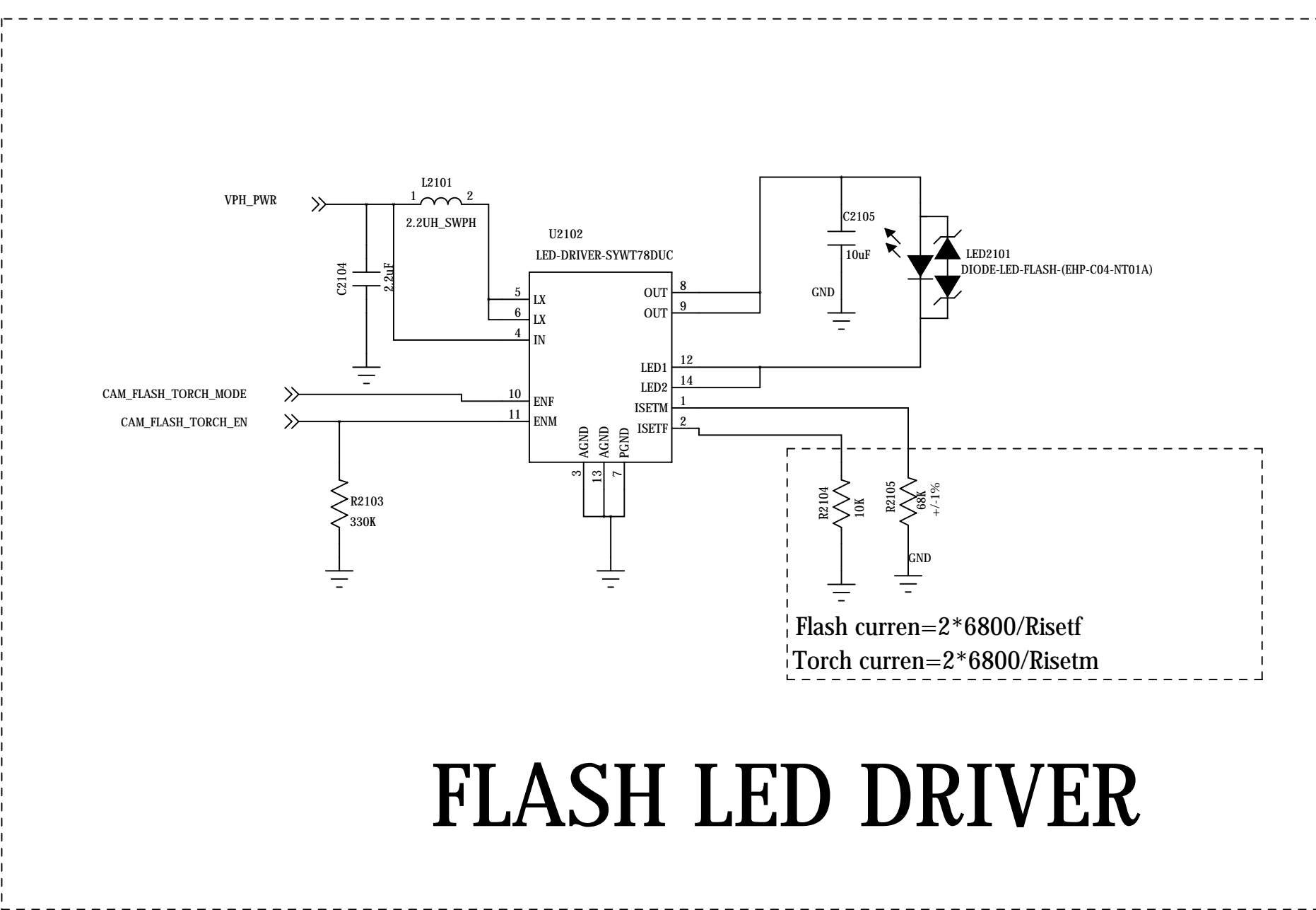
| PIN |            |
|-----|------------|
| 1   | GND        |
| 2   | MCLK       |
| 3   | GND        |
| 4   | MDN1       |
| 5   | MDP1       |
| 6   | GND        |
| 7   | MCN        |
| 8   | MCP        |
| 9   | GND        |
| 10  | MDNO       |
| 11  | MDPO       |
| 12  | GND        |
| 13  | GND        |
| 14  | GND        |
| 15  | AVDD 2.8V  |
| 16  | GND        |
| 17  | DOVDD 1.8V |
| 18  | DVDD 1.2V  |
| 19  | GND        |
| 20  | SCL        |
| 21  | SDA        |
| 22  | GND        |
| 23  | PWDN       |
| 24  | RESET      |

Sub Camera



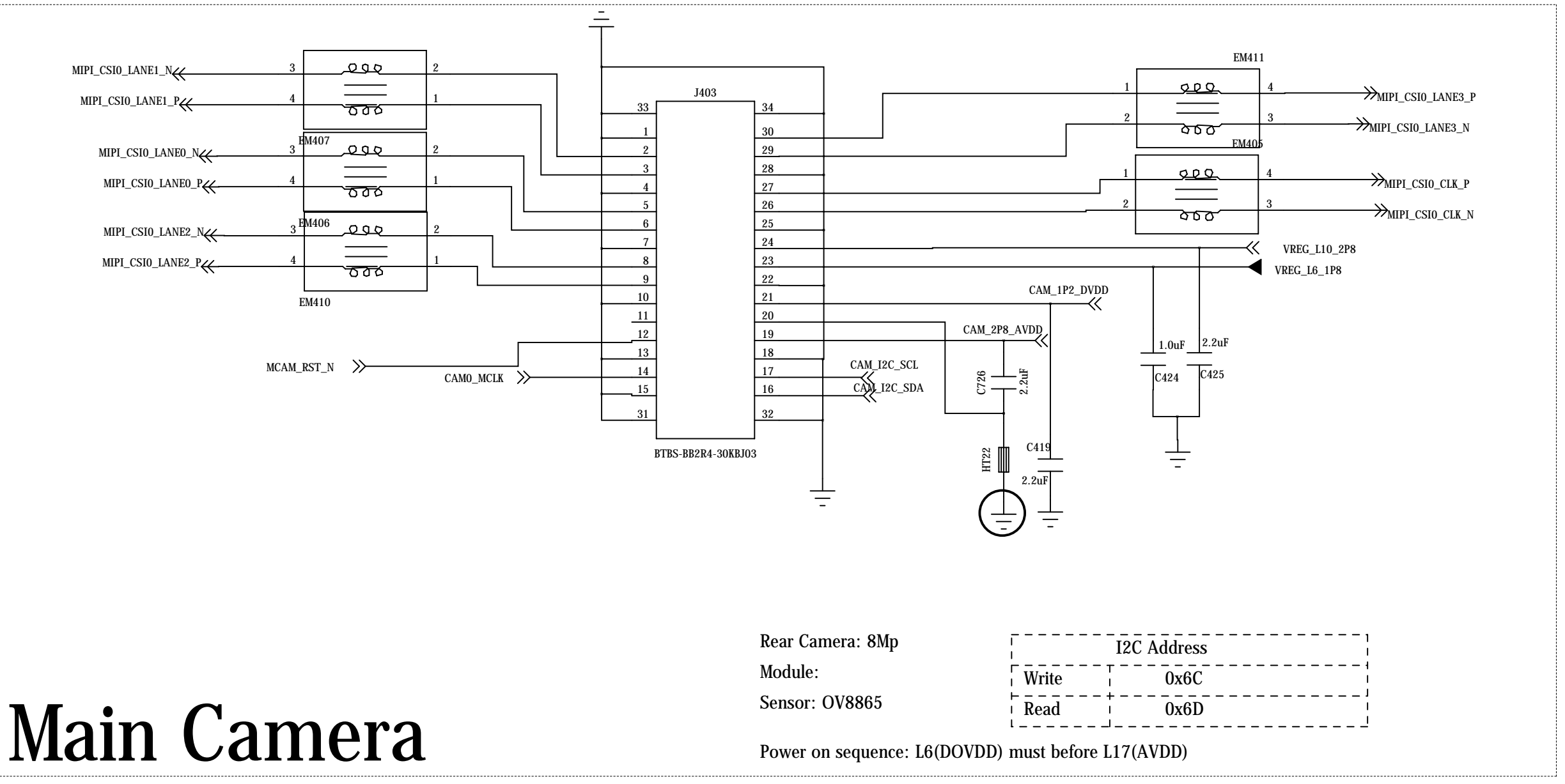
FRONT\_camera

Main Camera / Sub Camera share power domain design should double check the voltage level is compatible

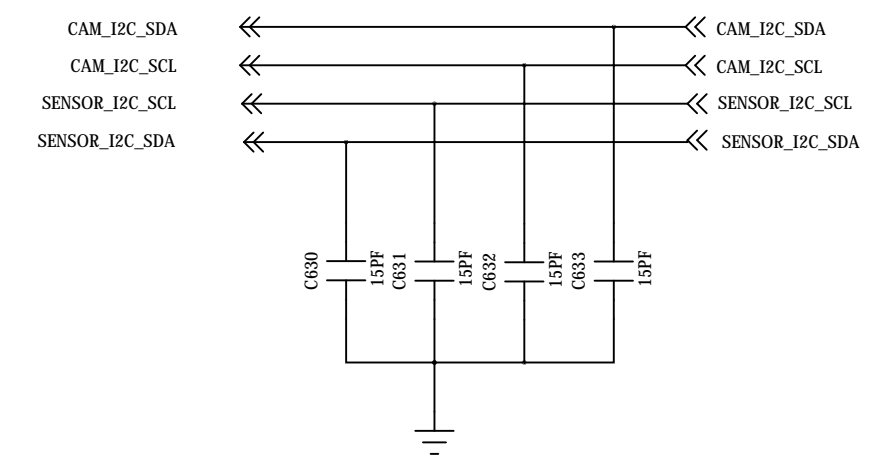


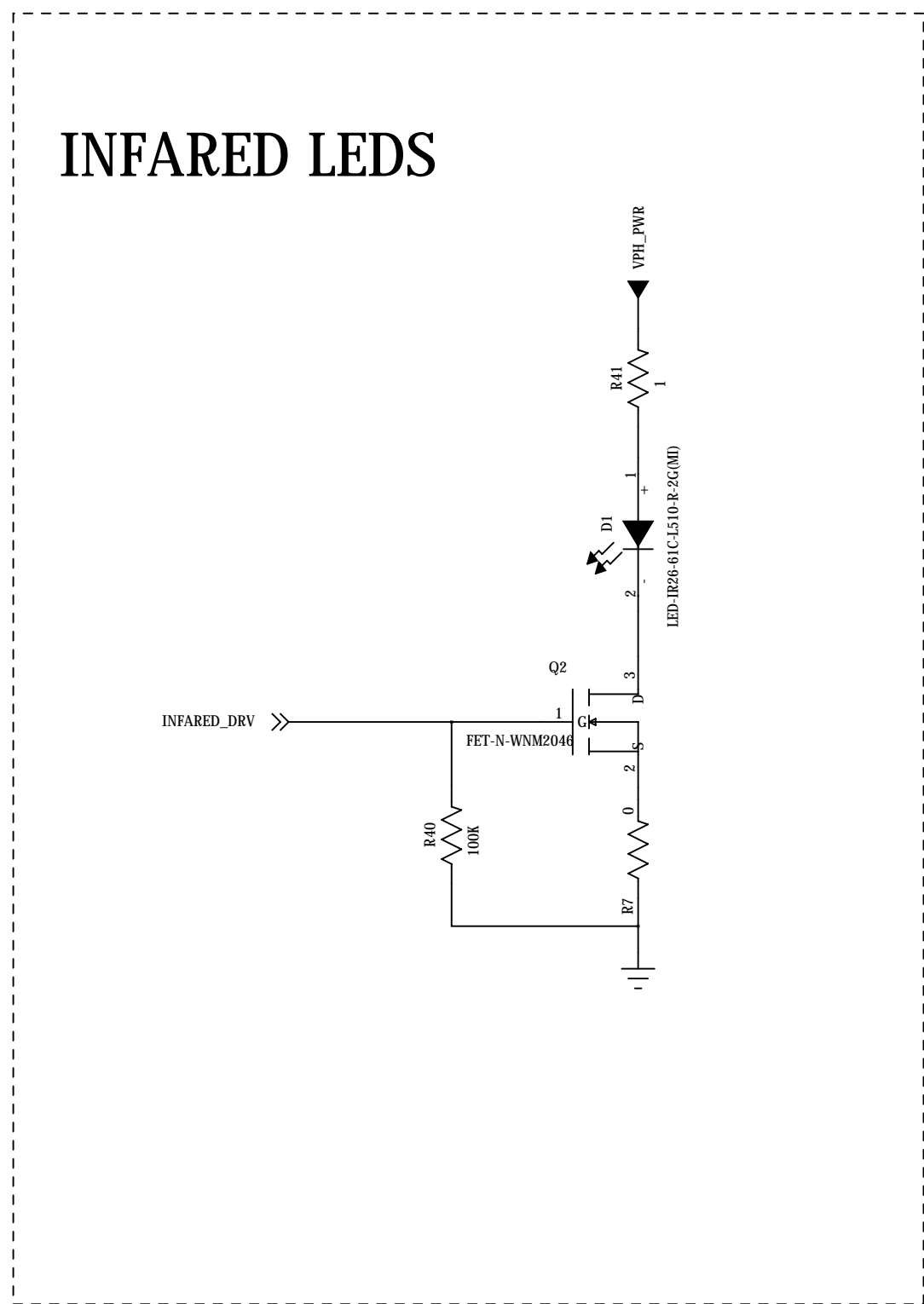
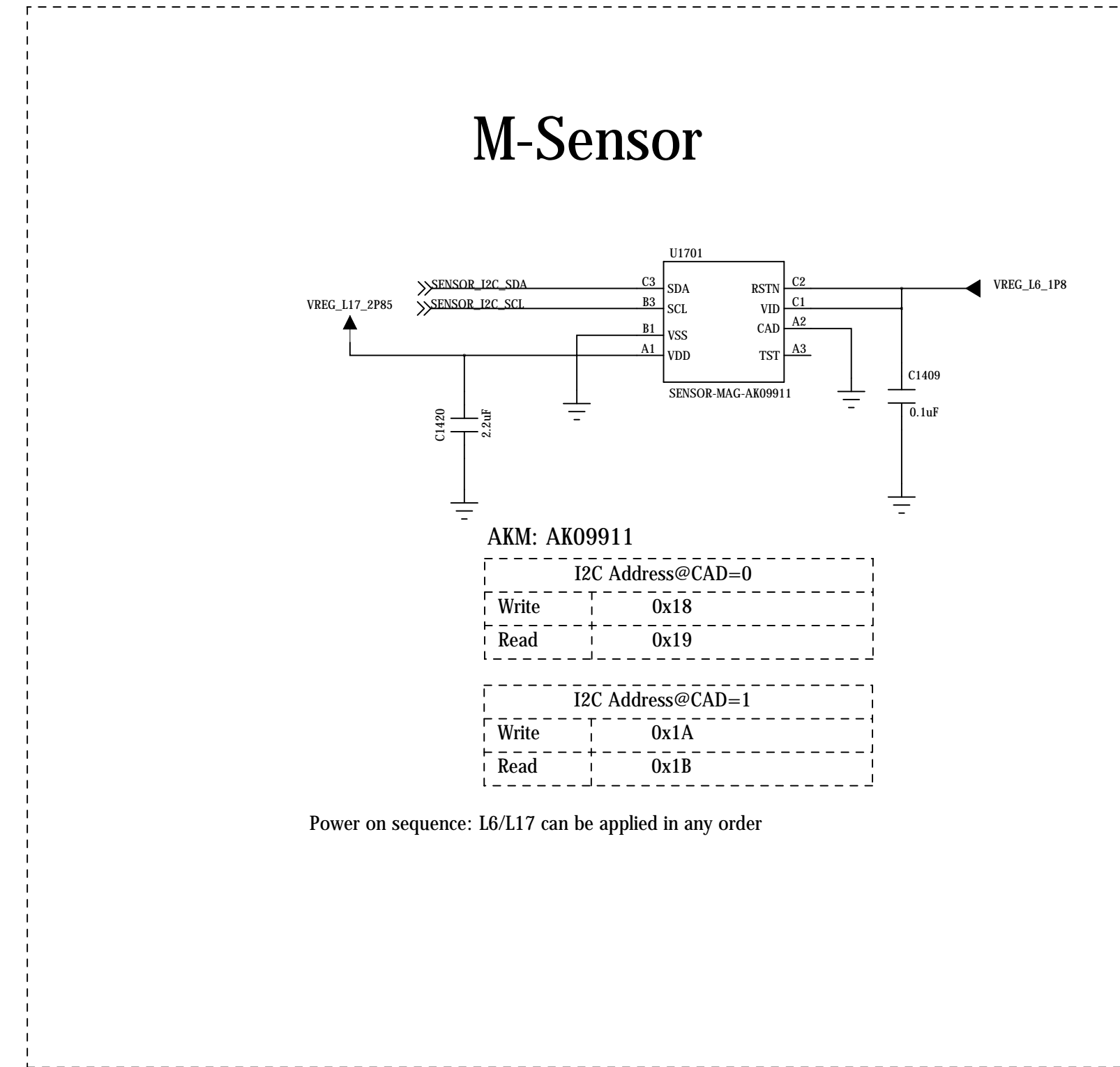
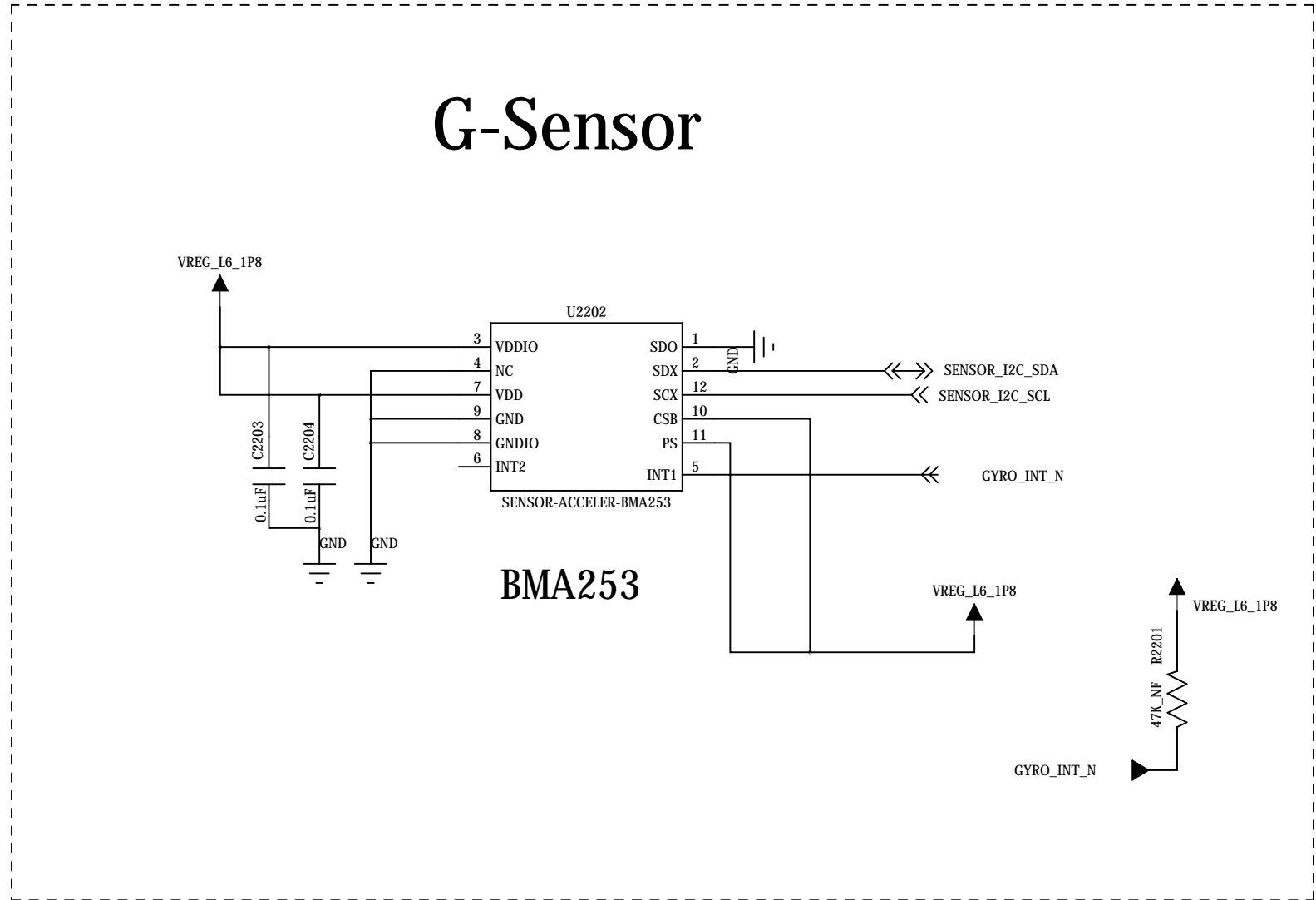
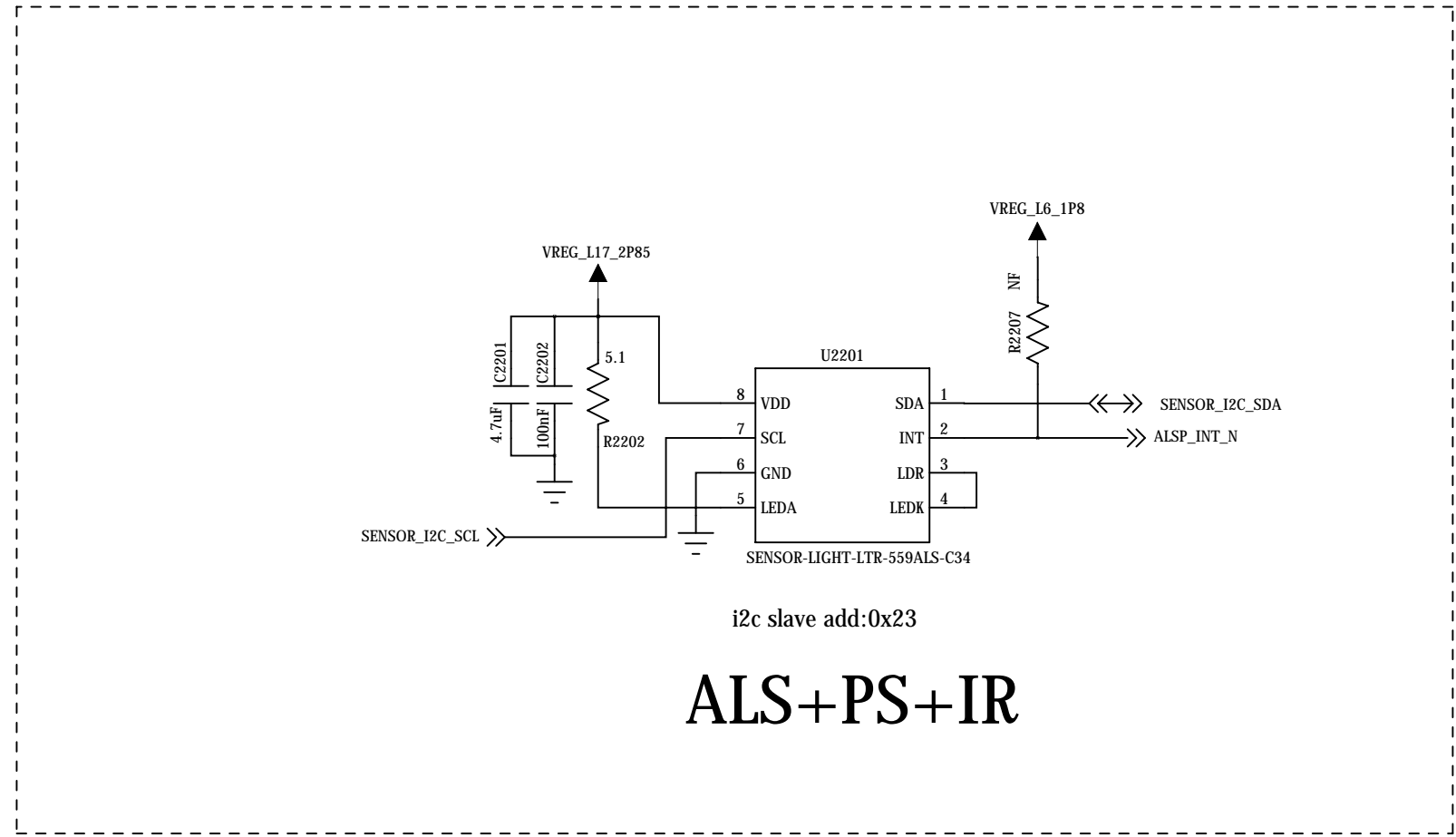
FLASH LED DRIVER

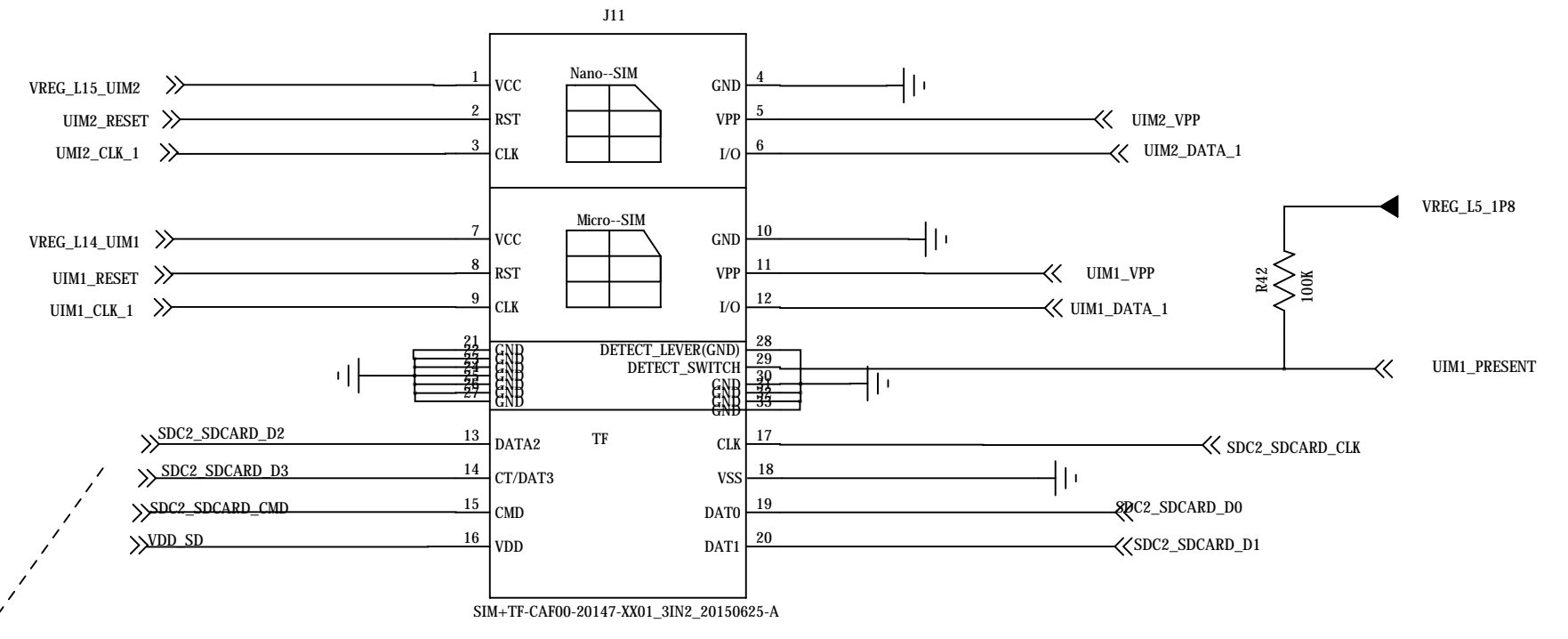
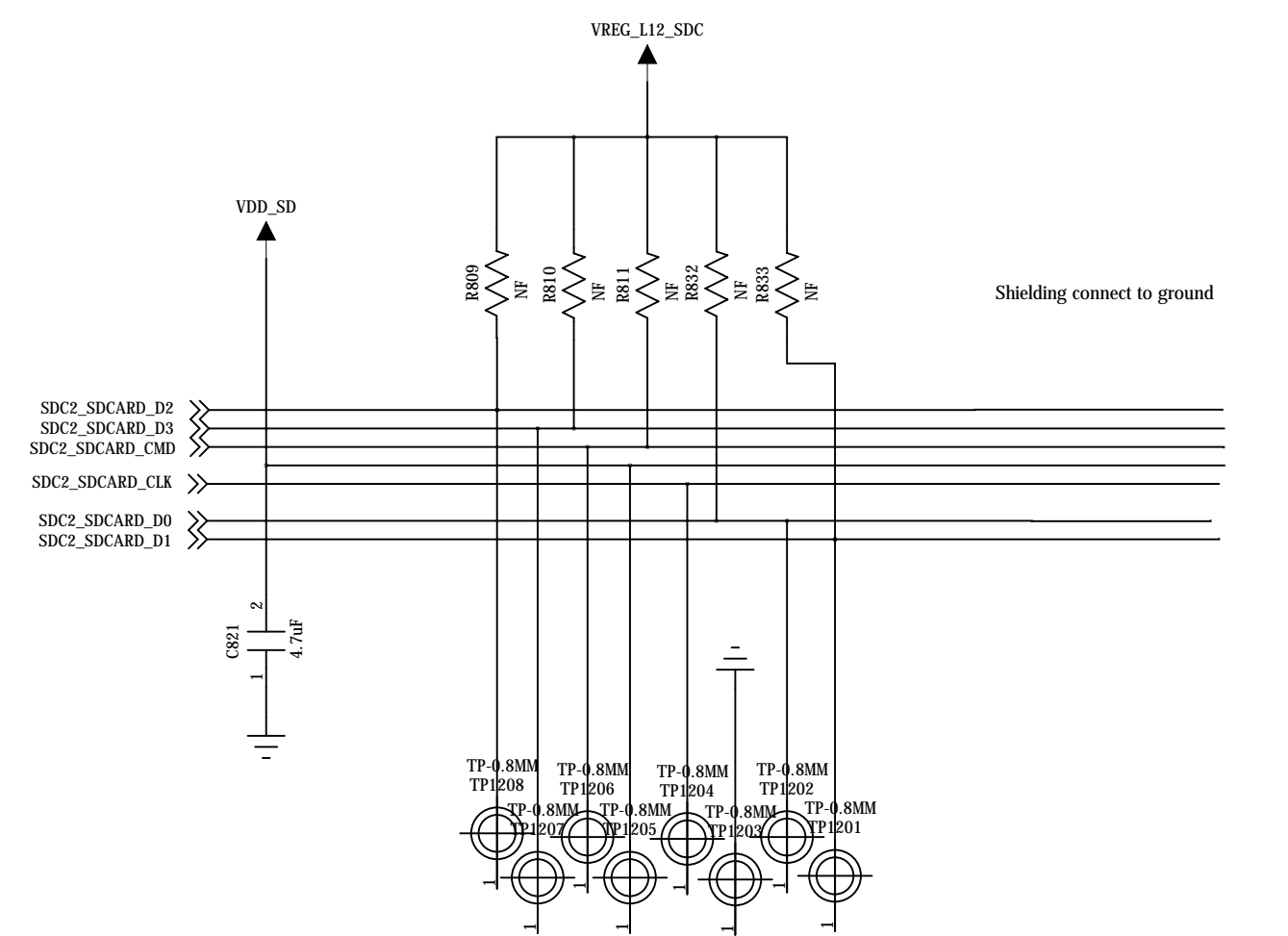
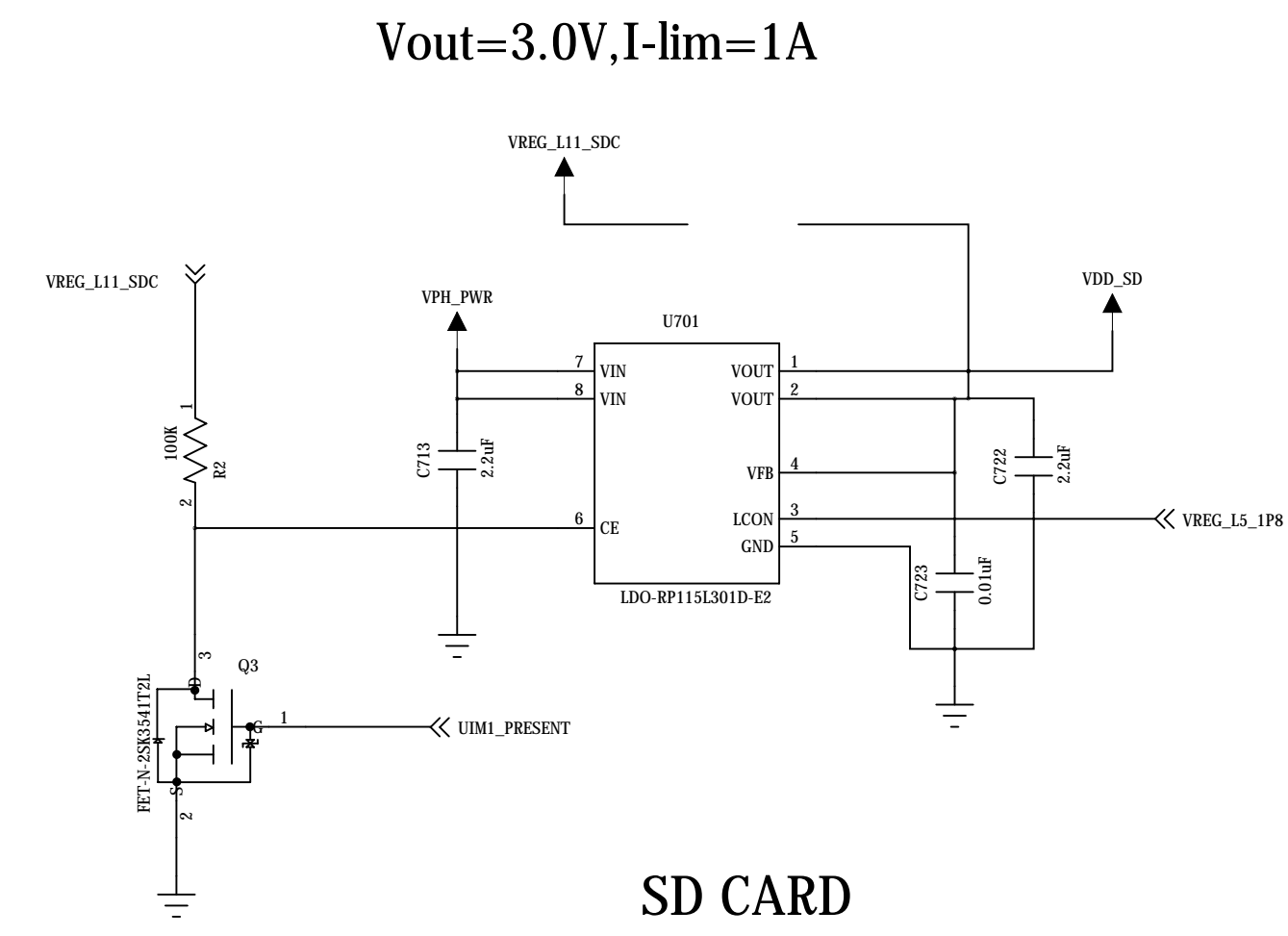
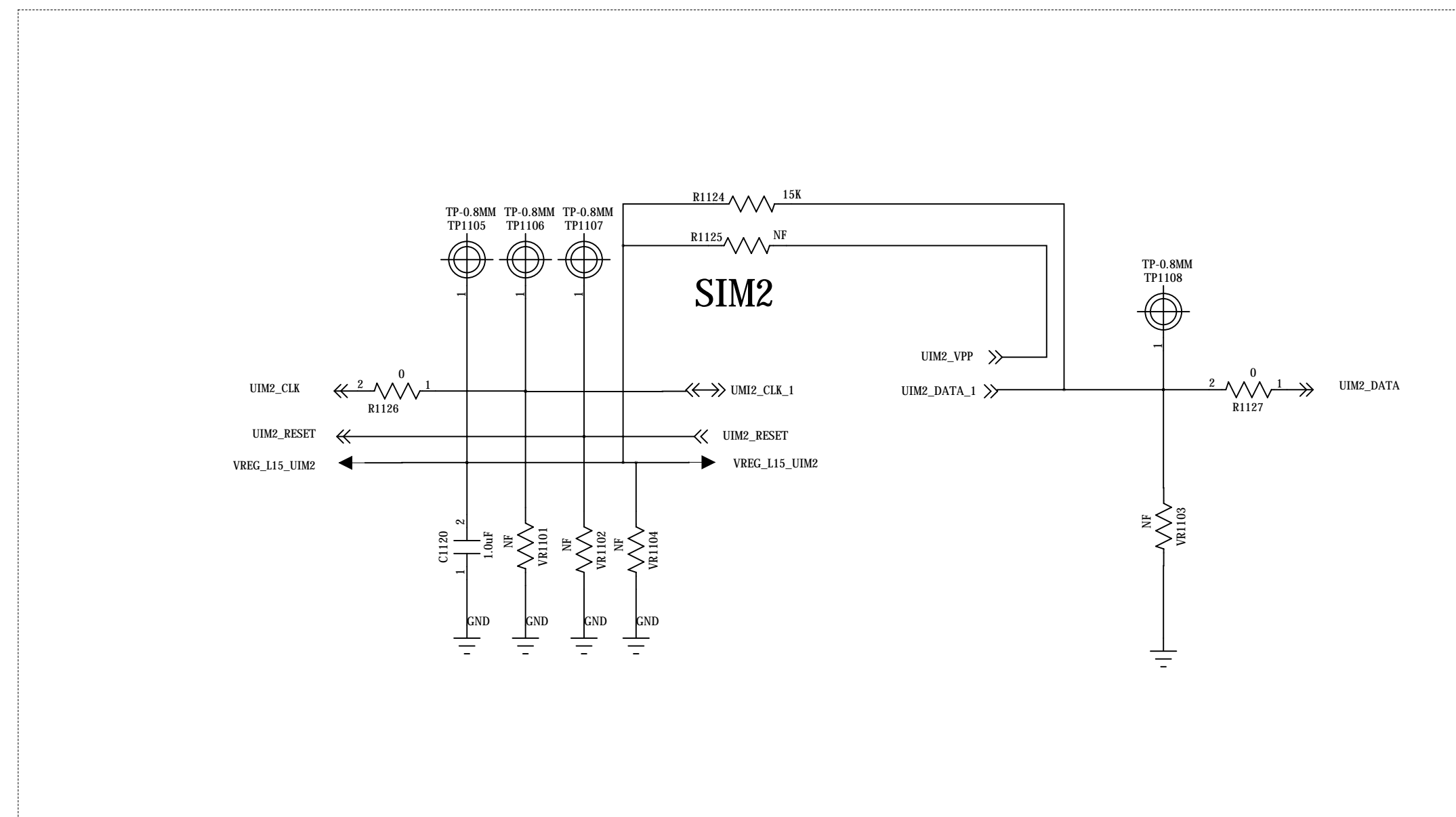
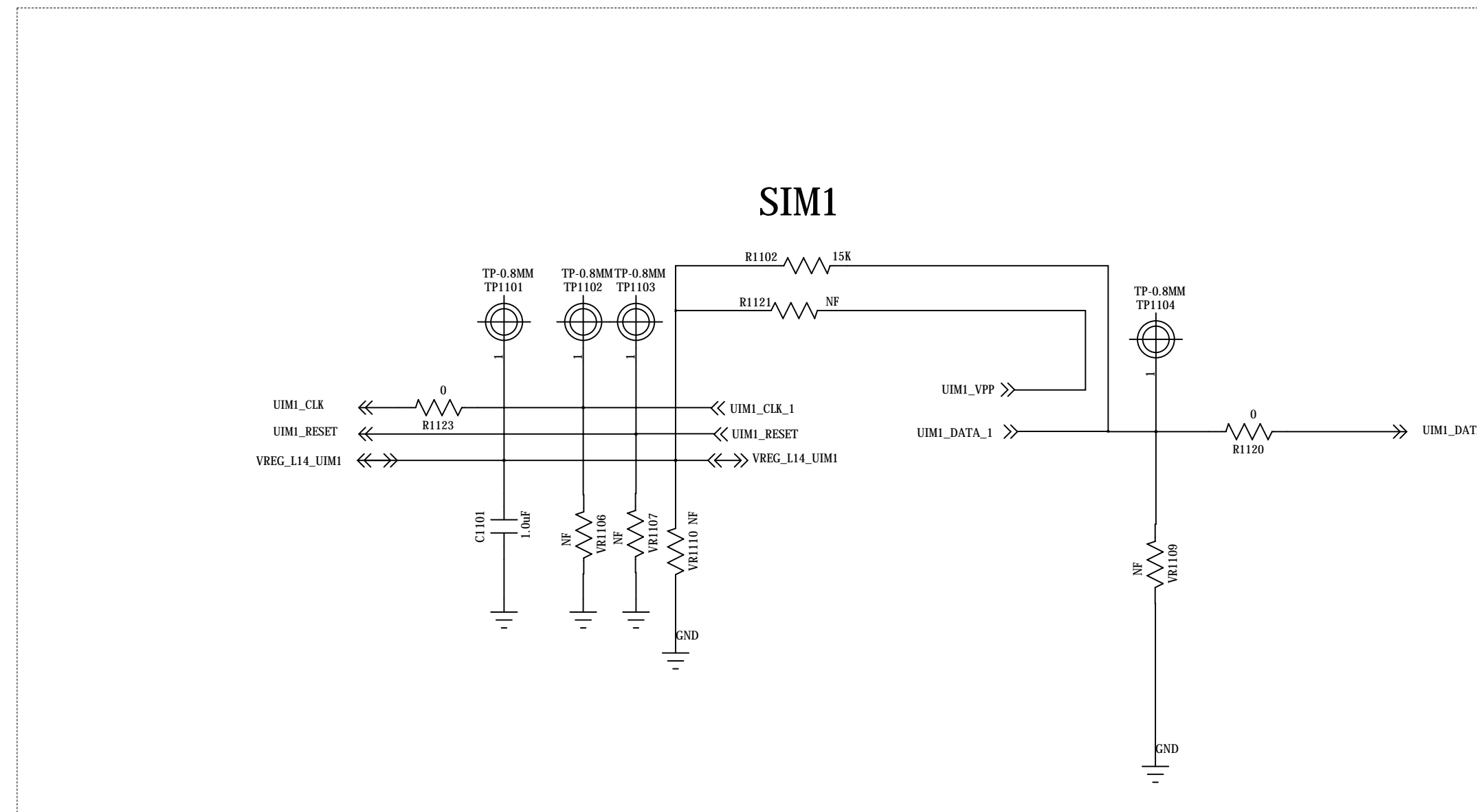
Main Camera / Sub Camera share power domain design should double check the voltage level is compatible



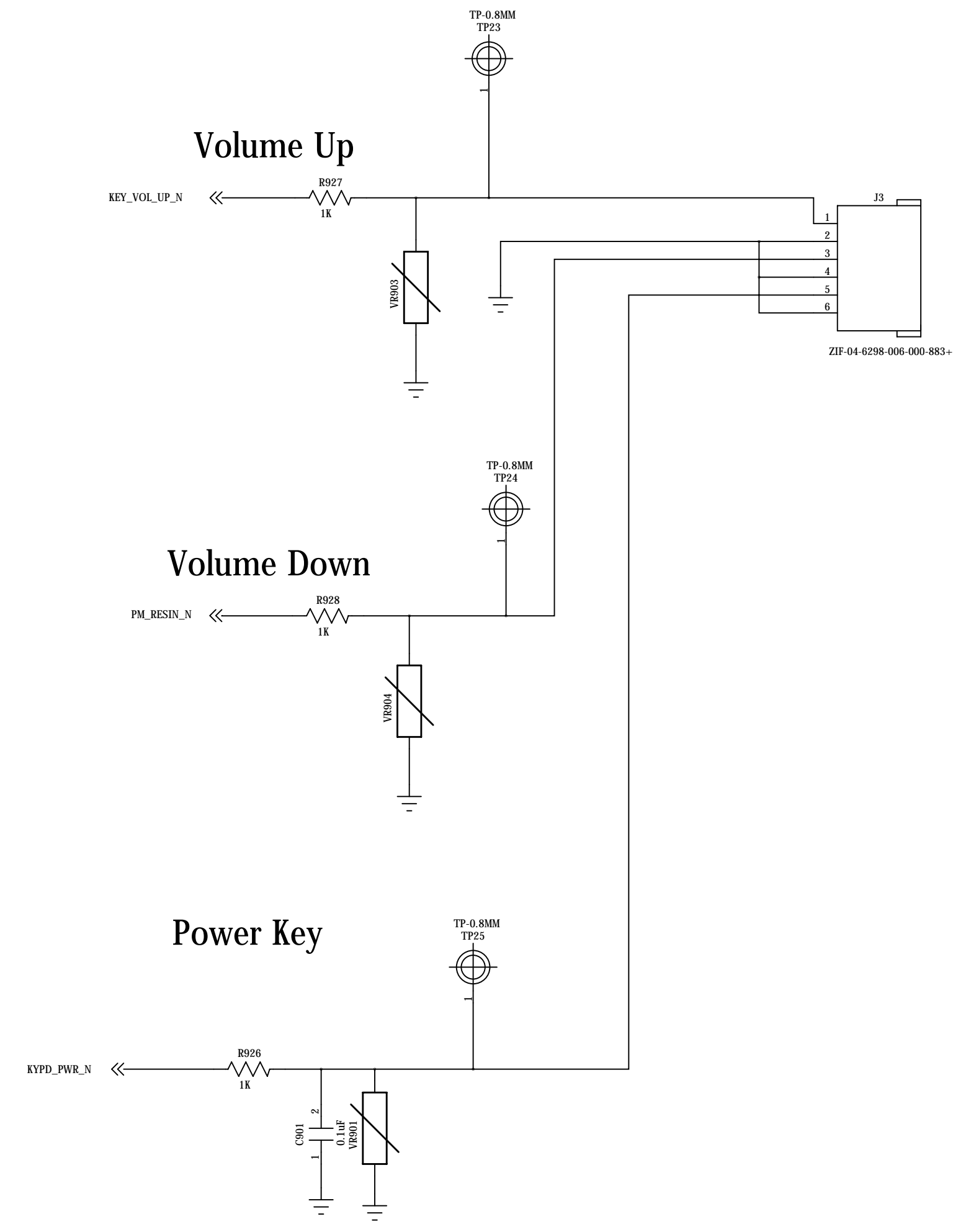
Main Camera

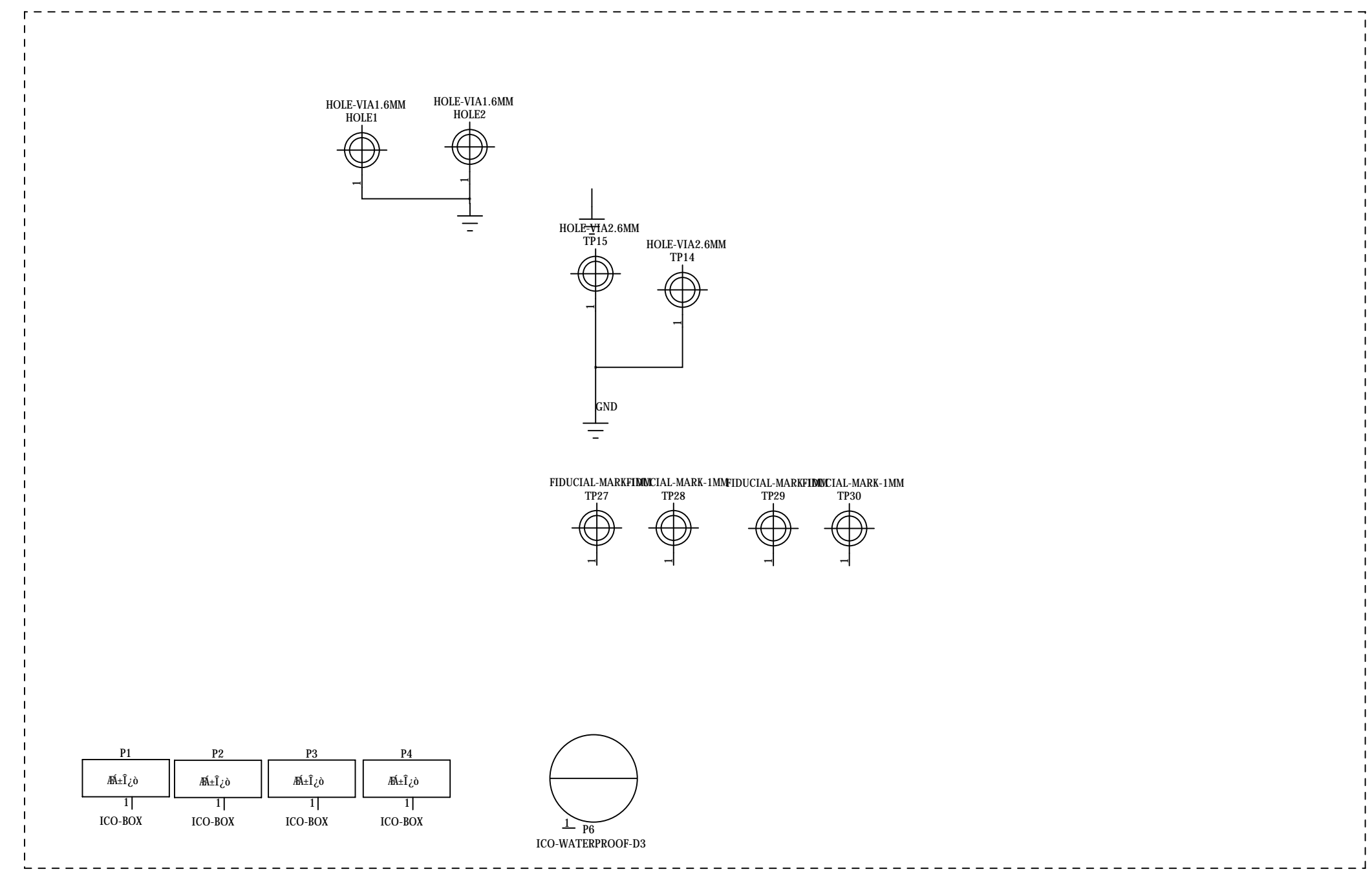
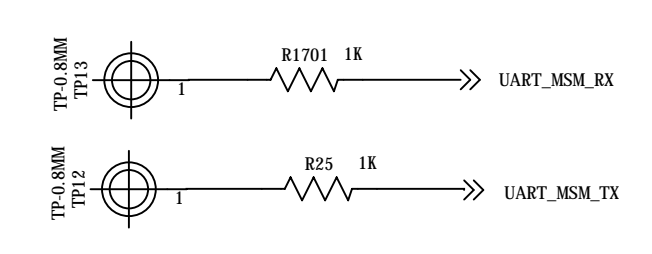
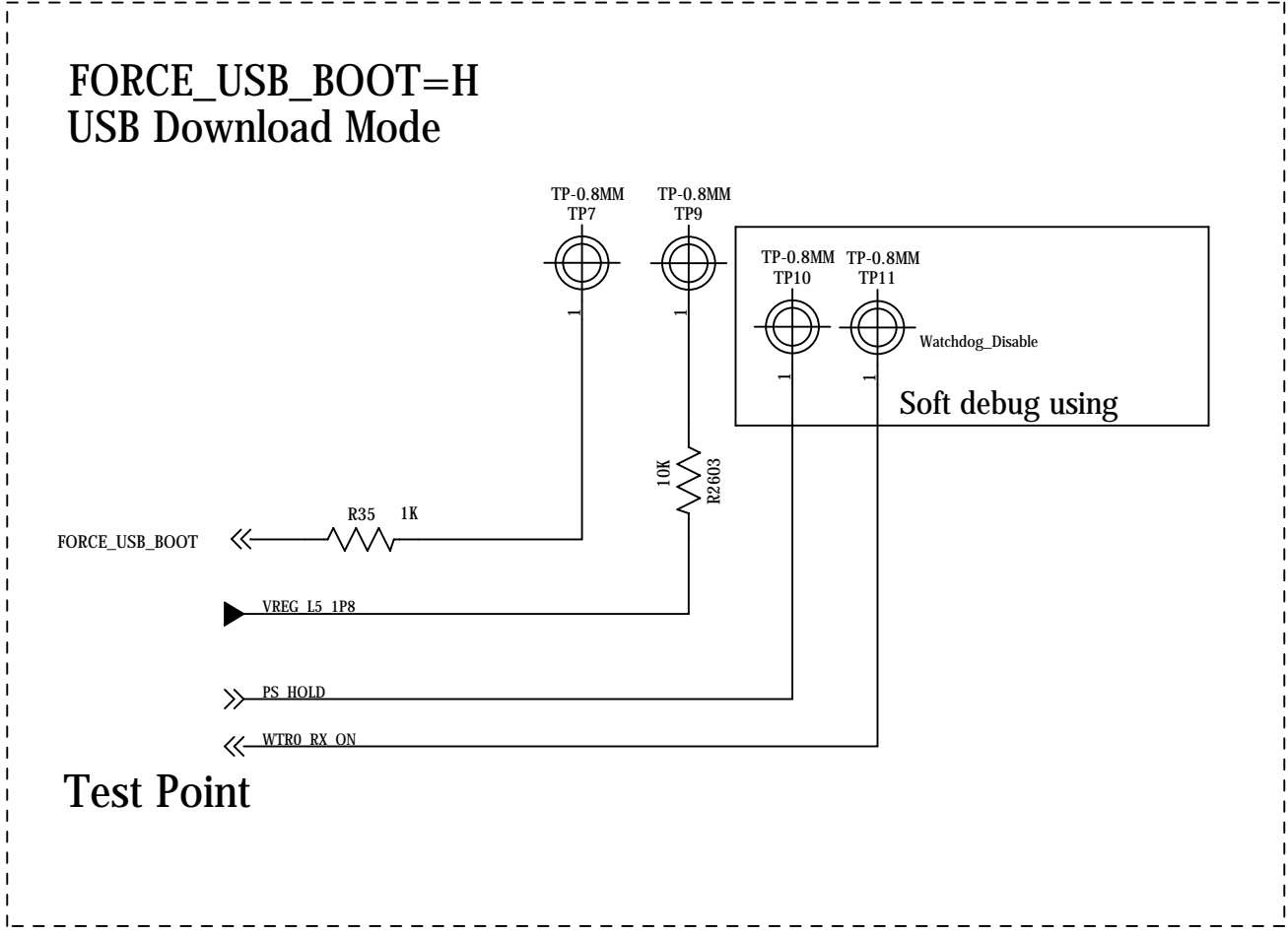






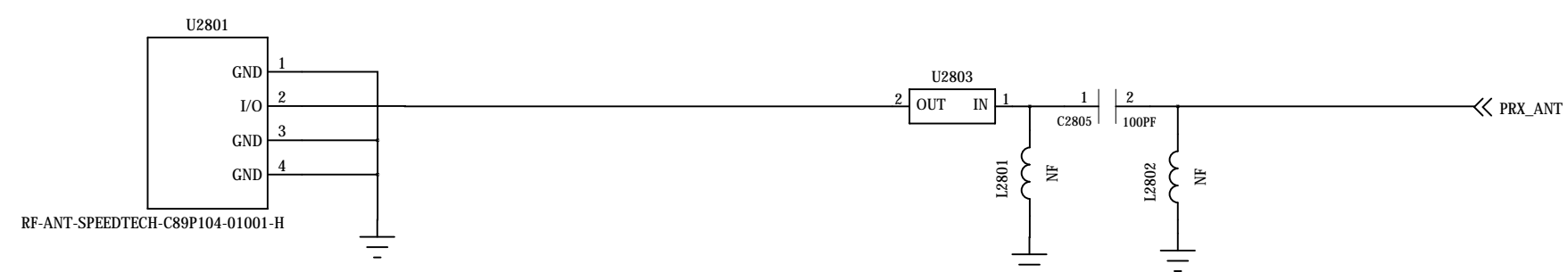
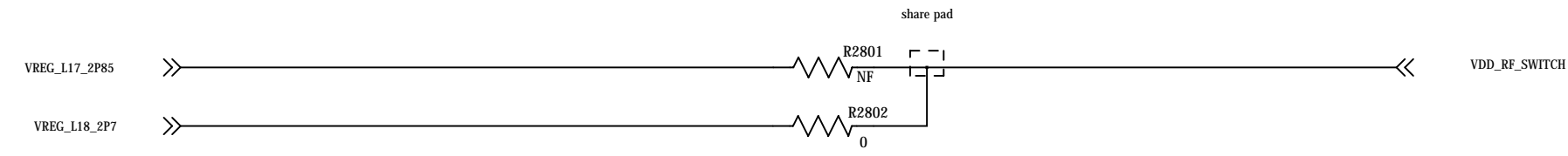
This int should give to GPIO38/GPIO56/GPIO60











|             | ANT_SWITCH_CTL0 | ANT_SWITCH_CTL1 |
|-------------|-----------------|-----------------|
| TRX_B7      |                 |                 |
| TRX_B40     |                 |                 |
| QFE2320_ANT |                 |                 |
| TRX_B38_41  |                 |                 |

|             | ANT_SWITCH_CTL0 | ANT_SWITCH_CTL1 |
|-------------|-----------------|-----------------|
| TRX_B7      |                 |                 |
| TRX_B40     |                 |                 |
| QFE2320_ANT |                 |                 |
| TRX_B38_41  |                 |                 |

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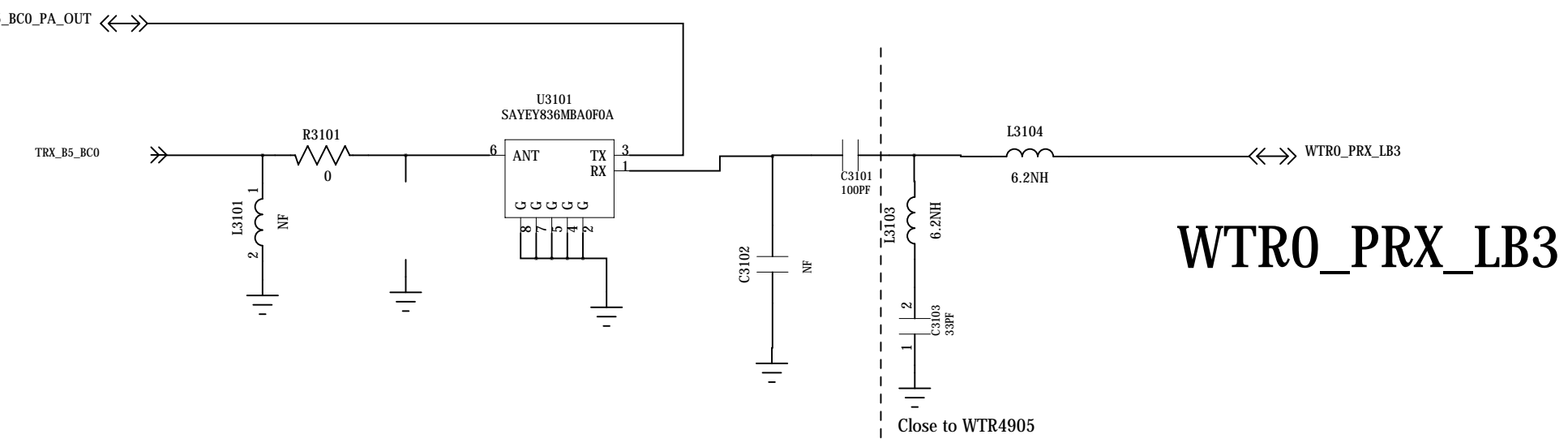
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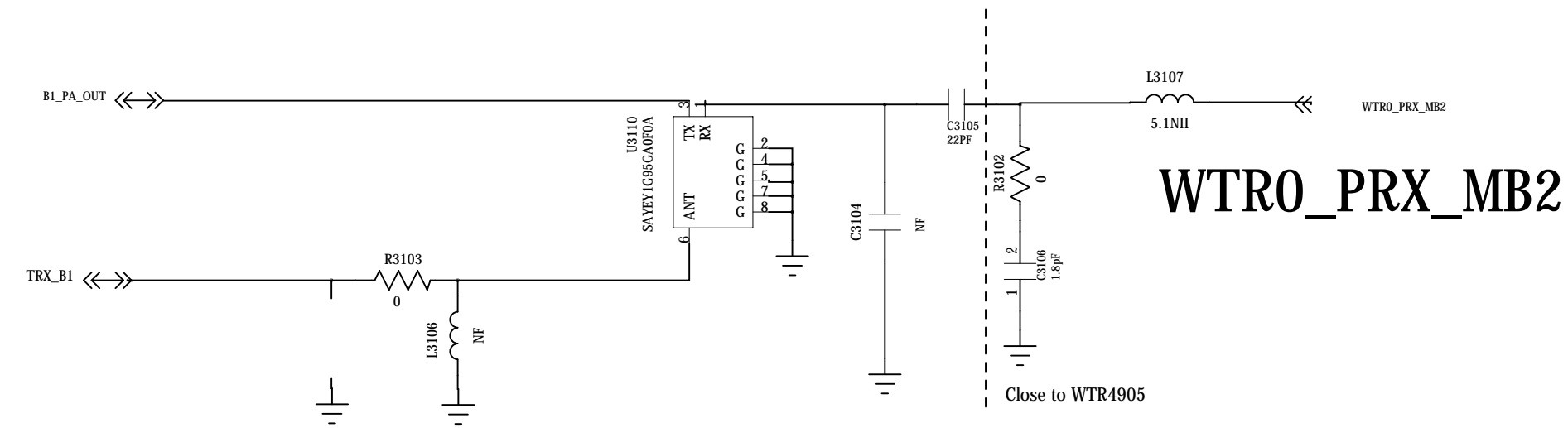




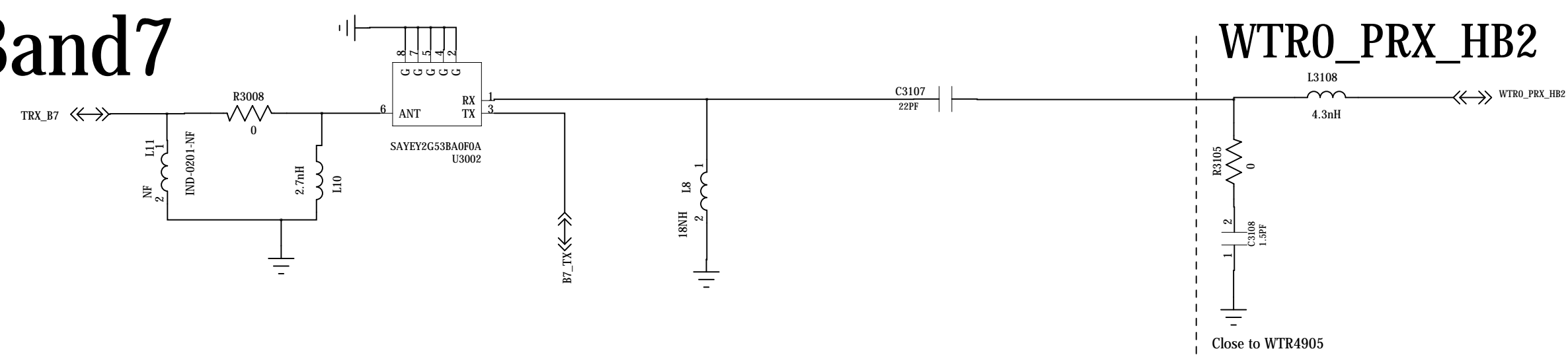
# Band5



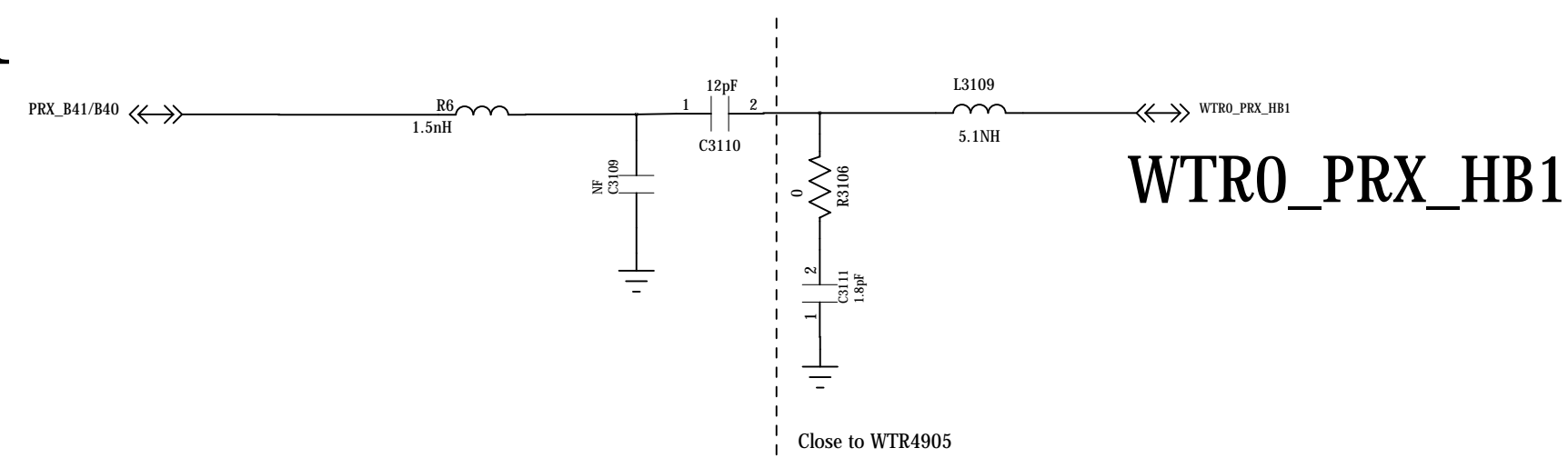
# Band1



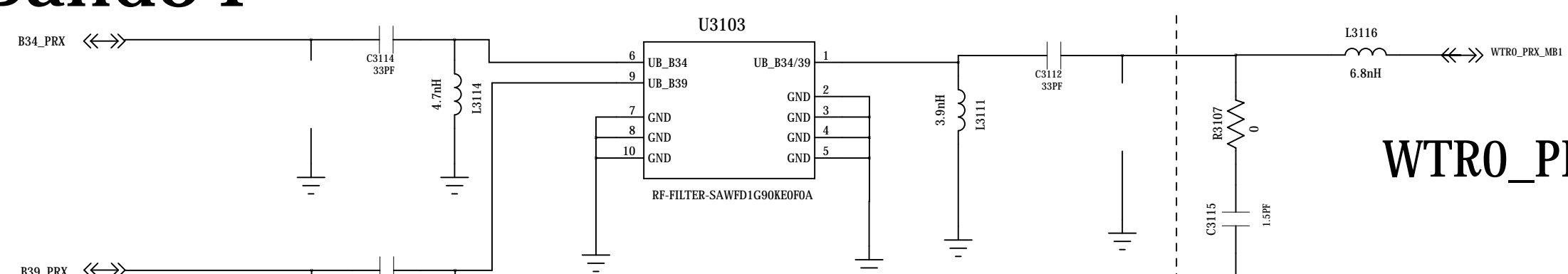
# Band7



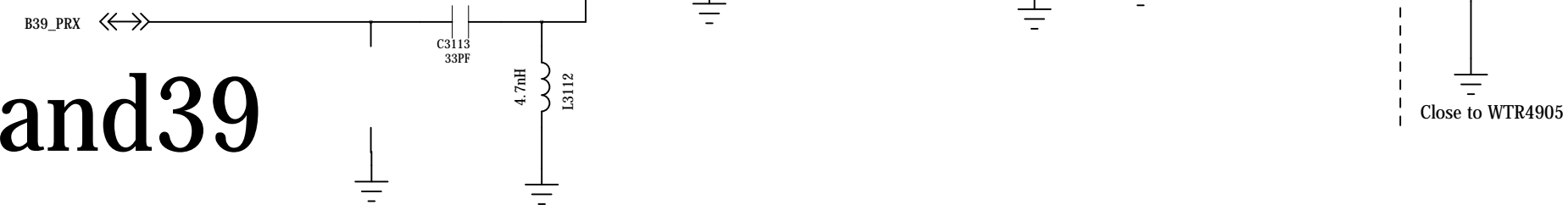
# Band40/41



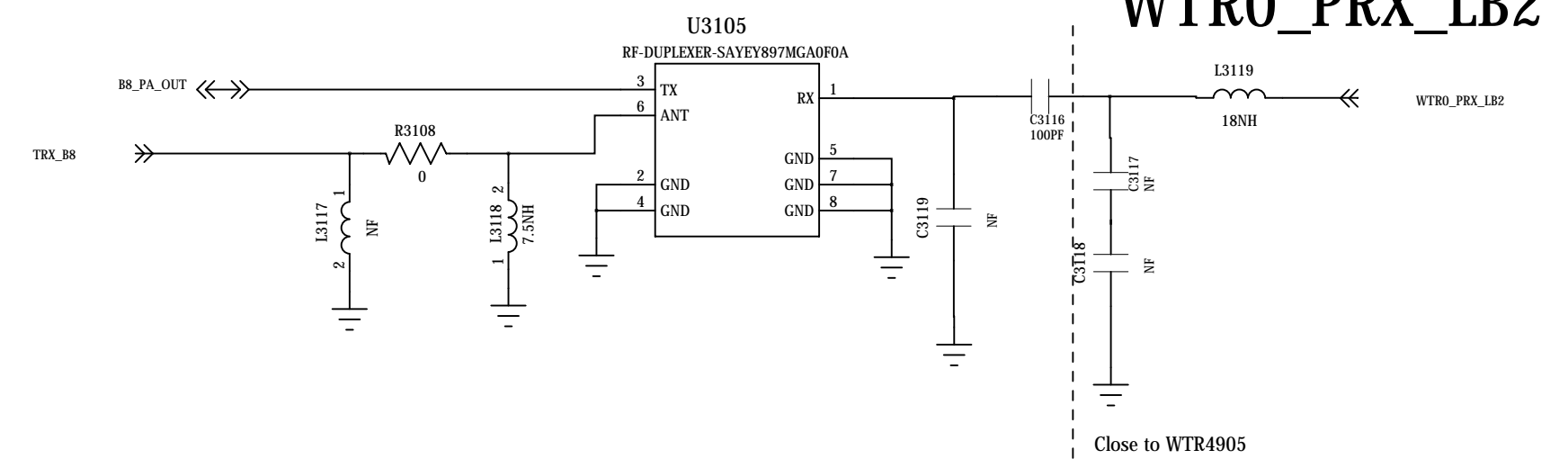
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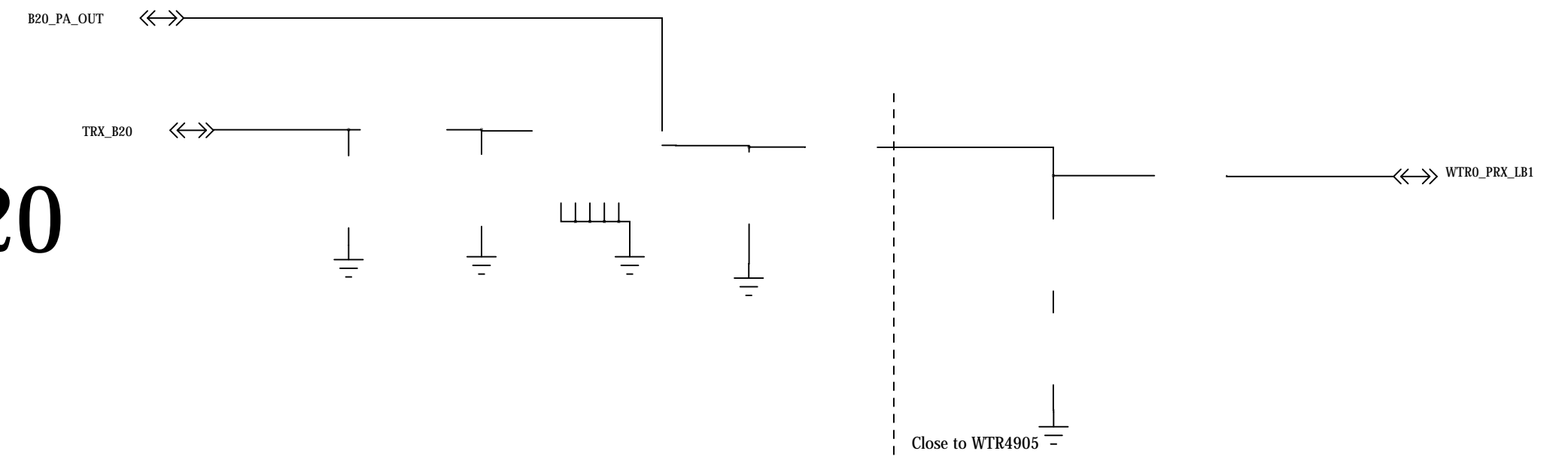
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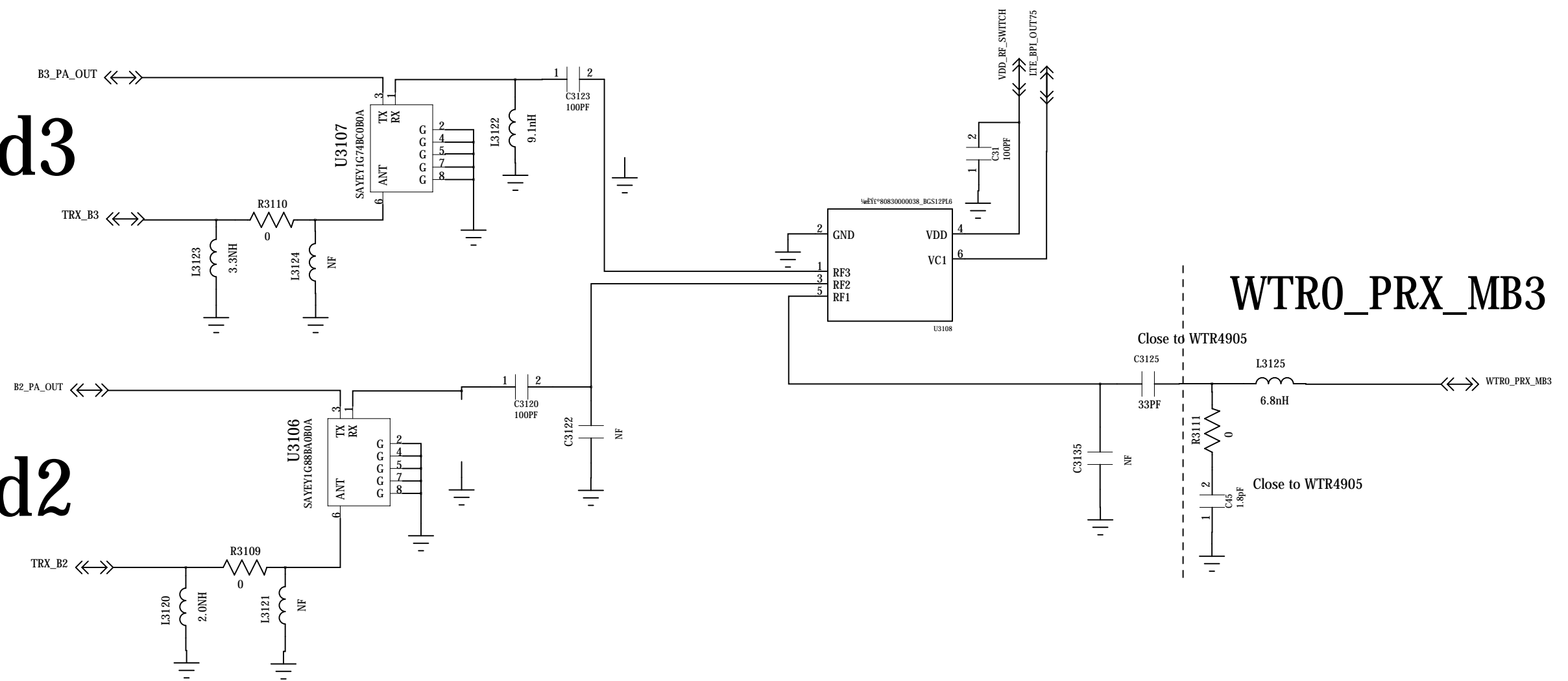
# Band8



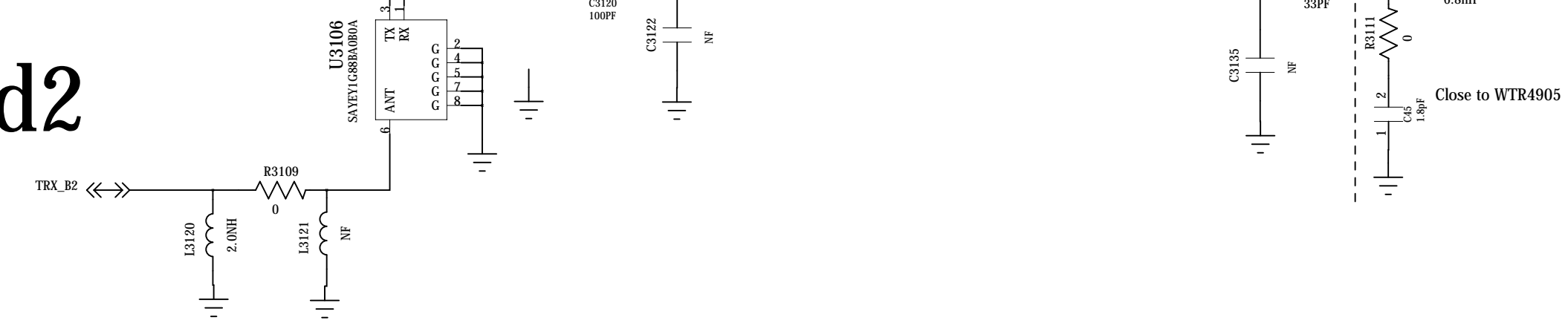
# BandB20



# Band3



# Band2



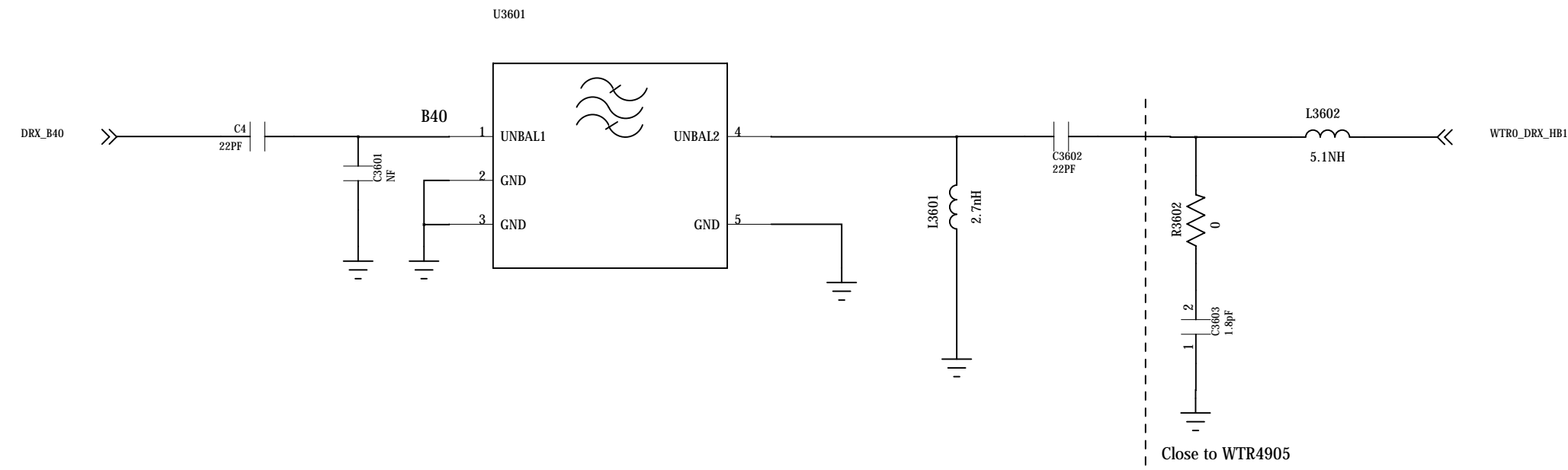
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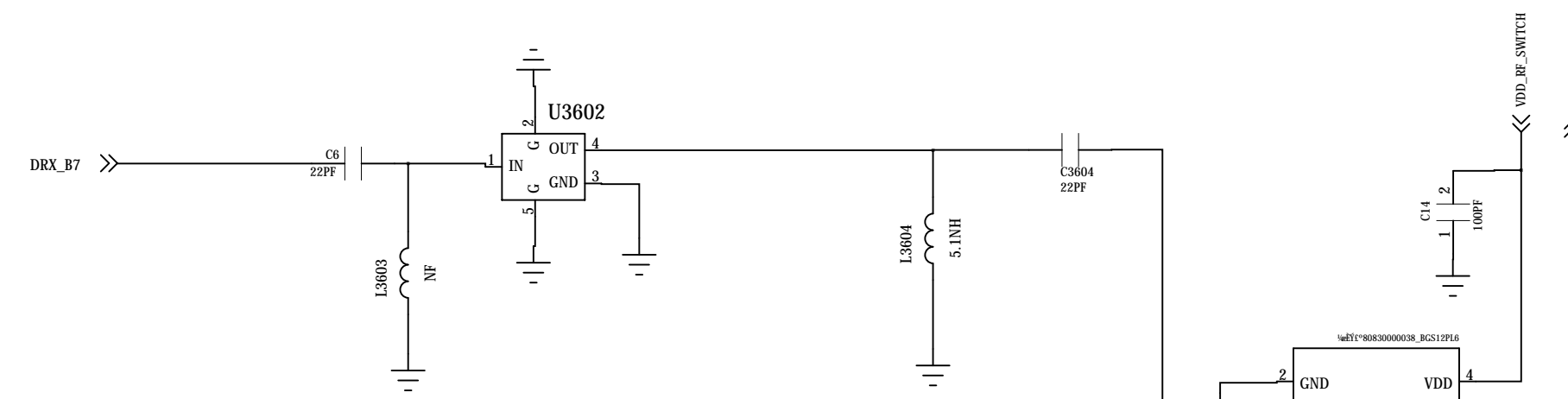


Band40



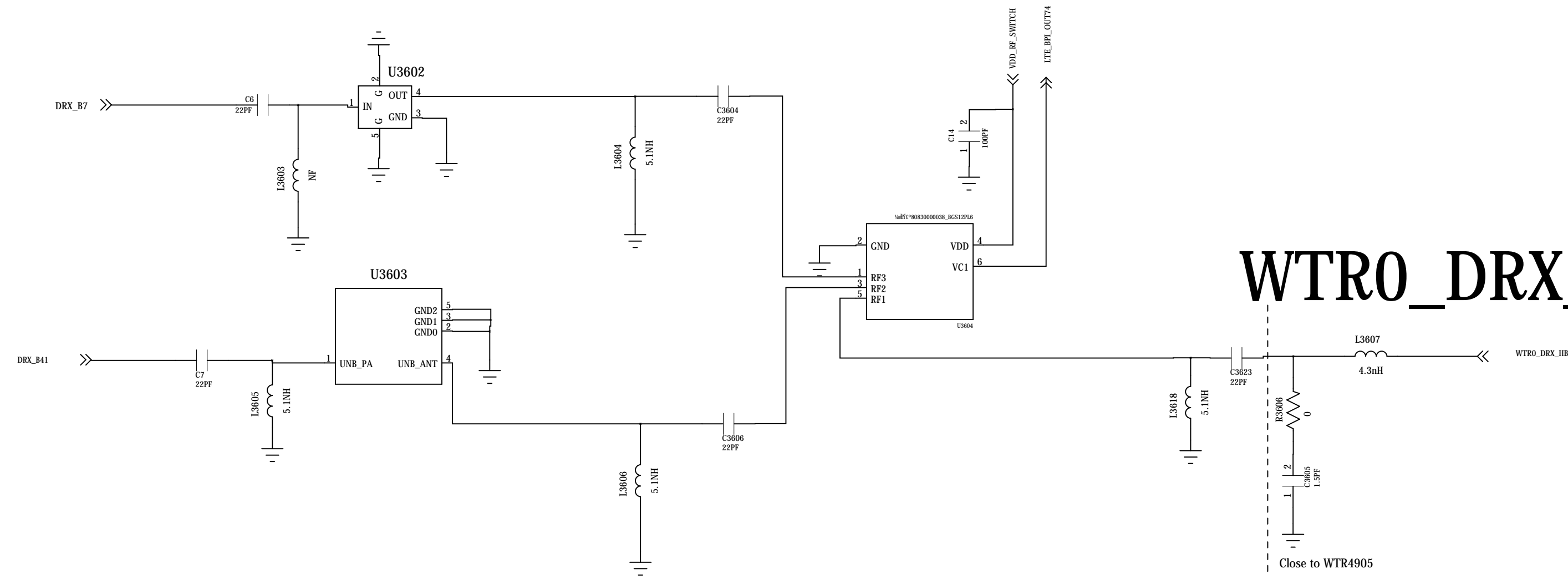
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Band7

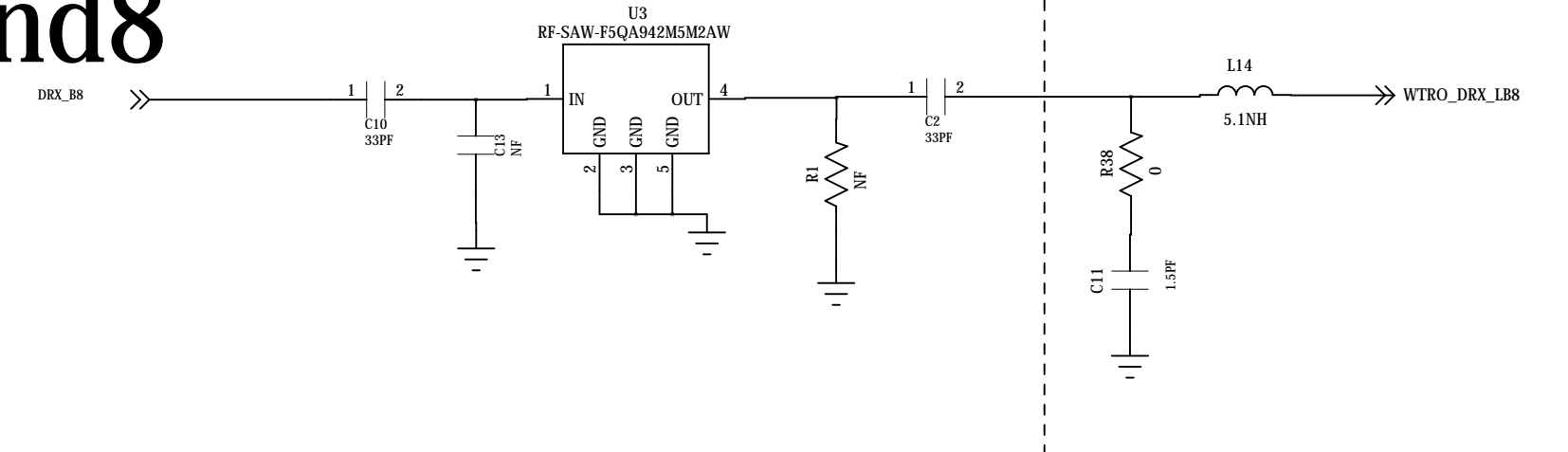


WTR0\_DRX\_HB2

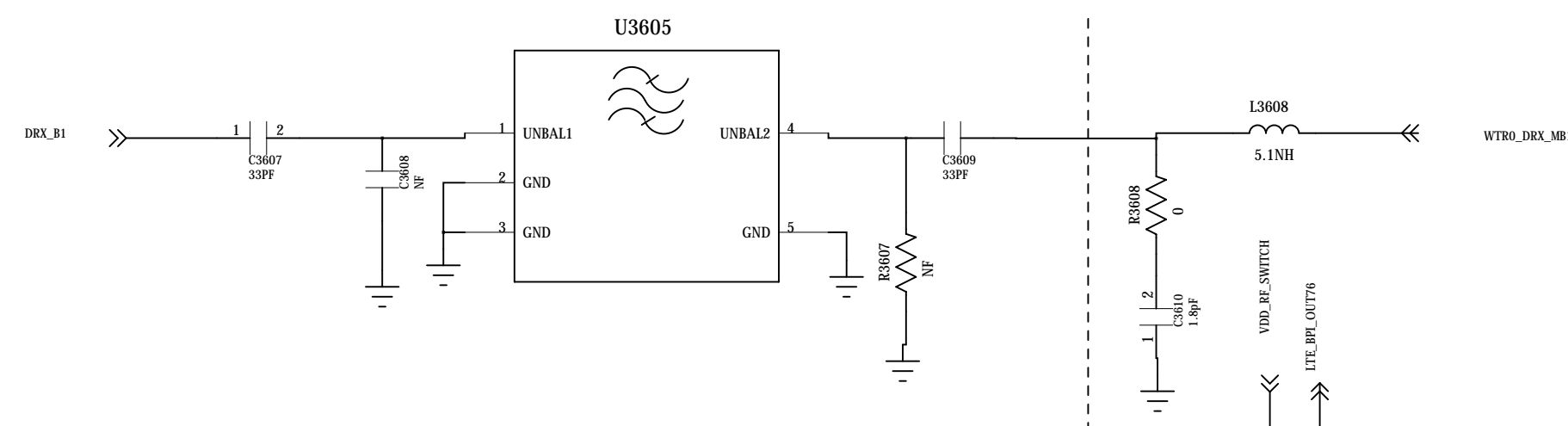
Band41



Band8

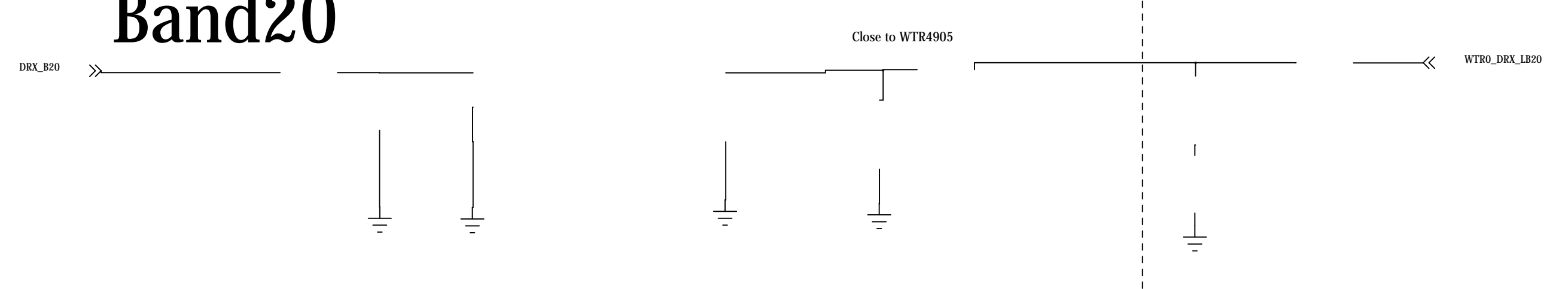


Band1\_4

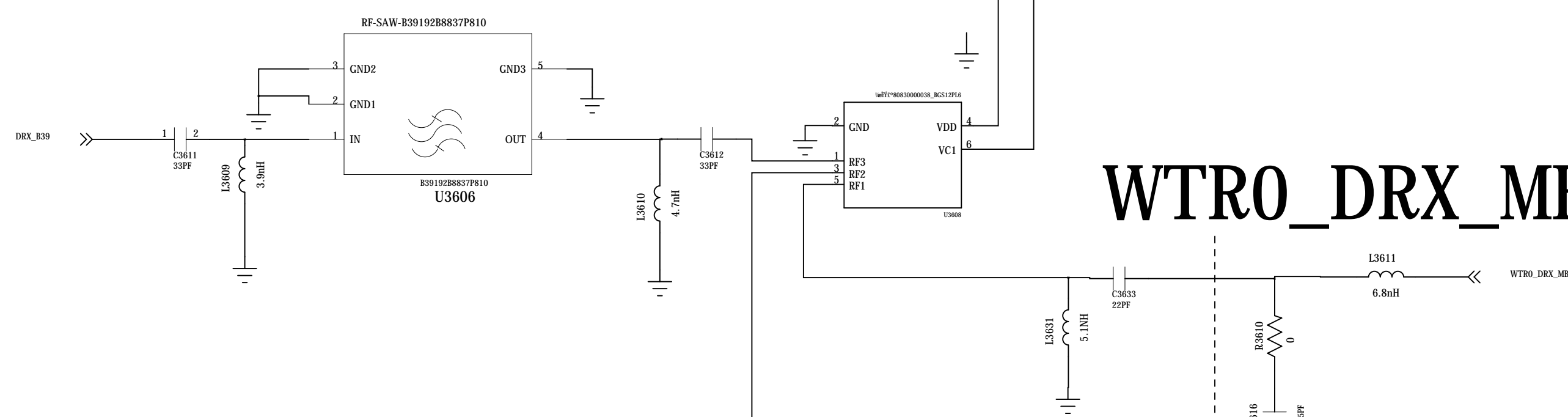


WTR0\_DRX\_MB1

Band20

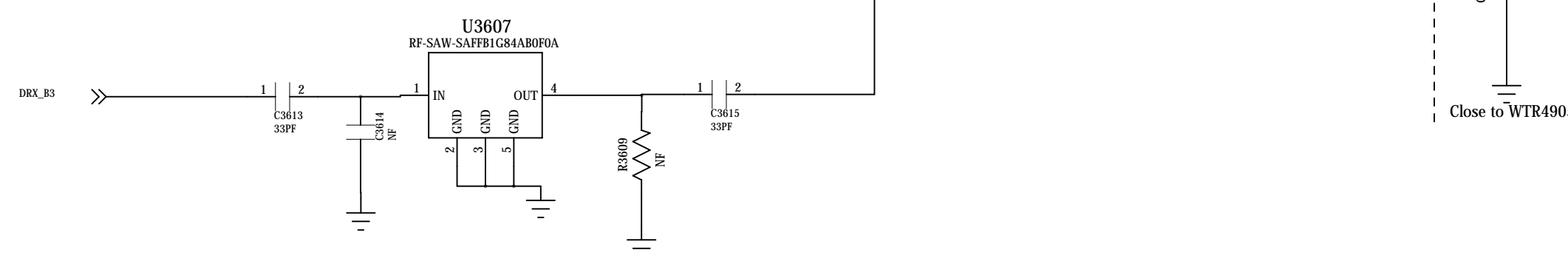


Band39



WTR0\_DRX\_MB2

Band3

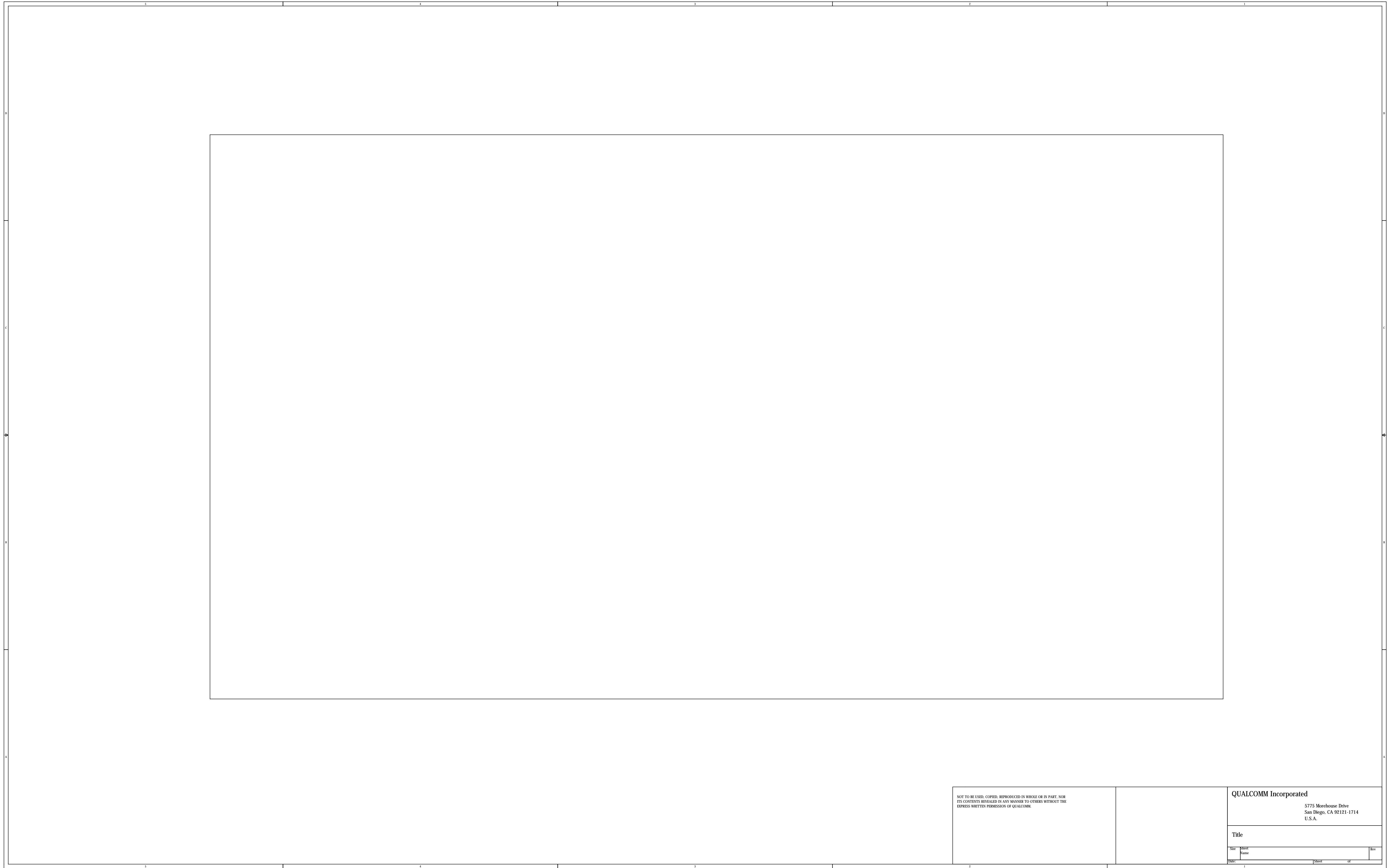


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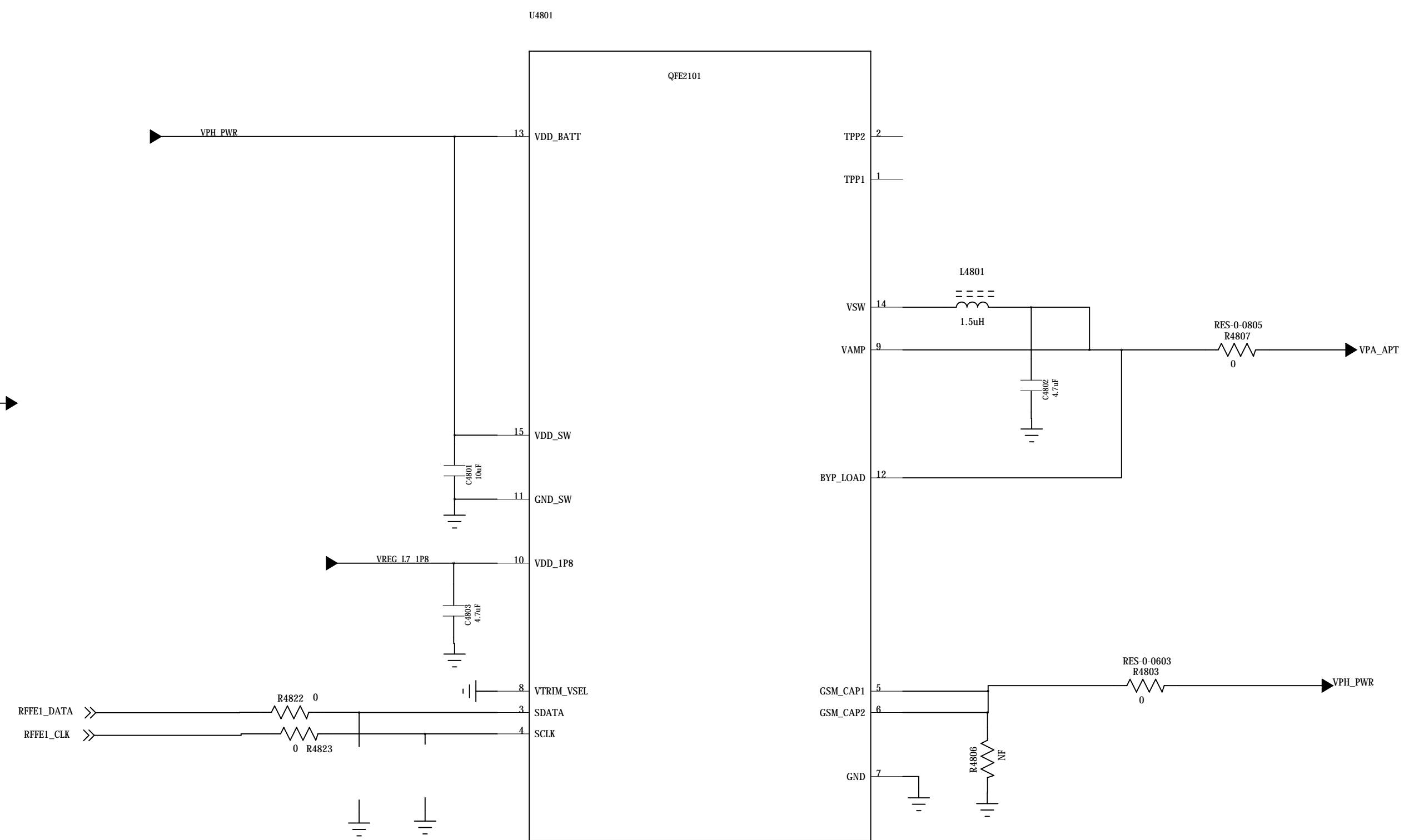
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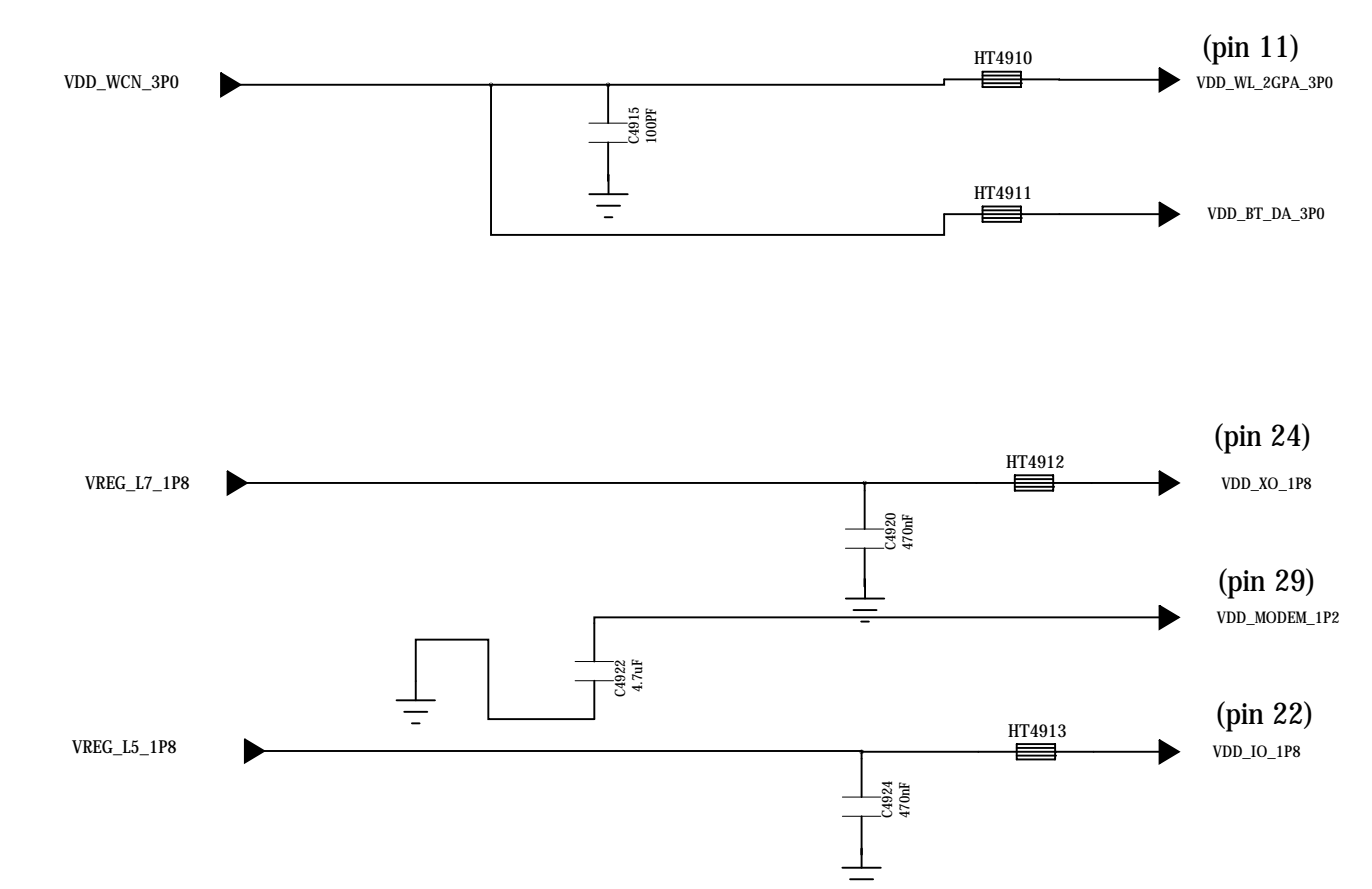
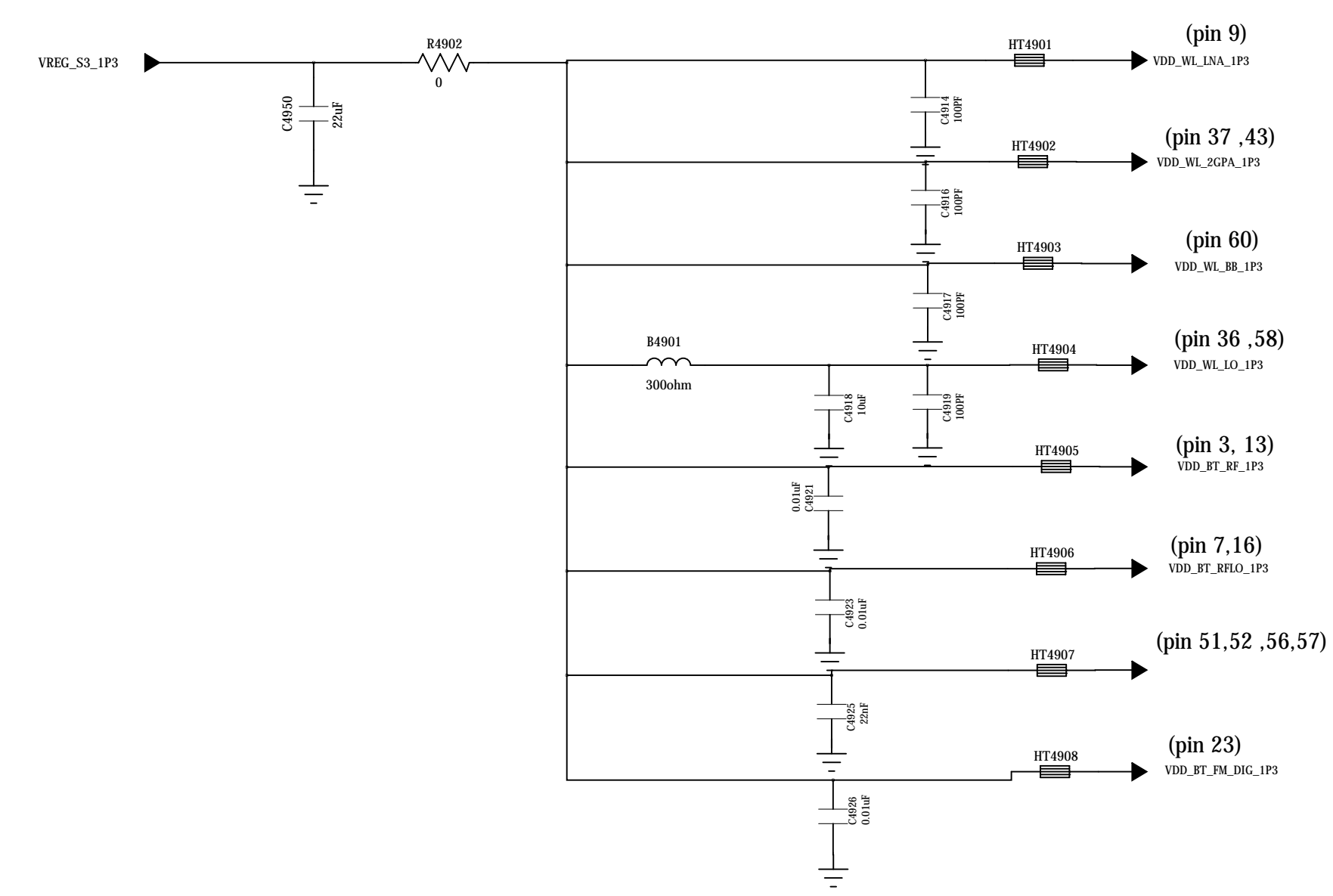
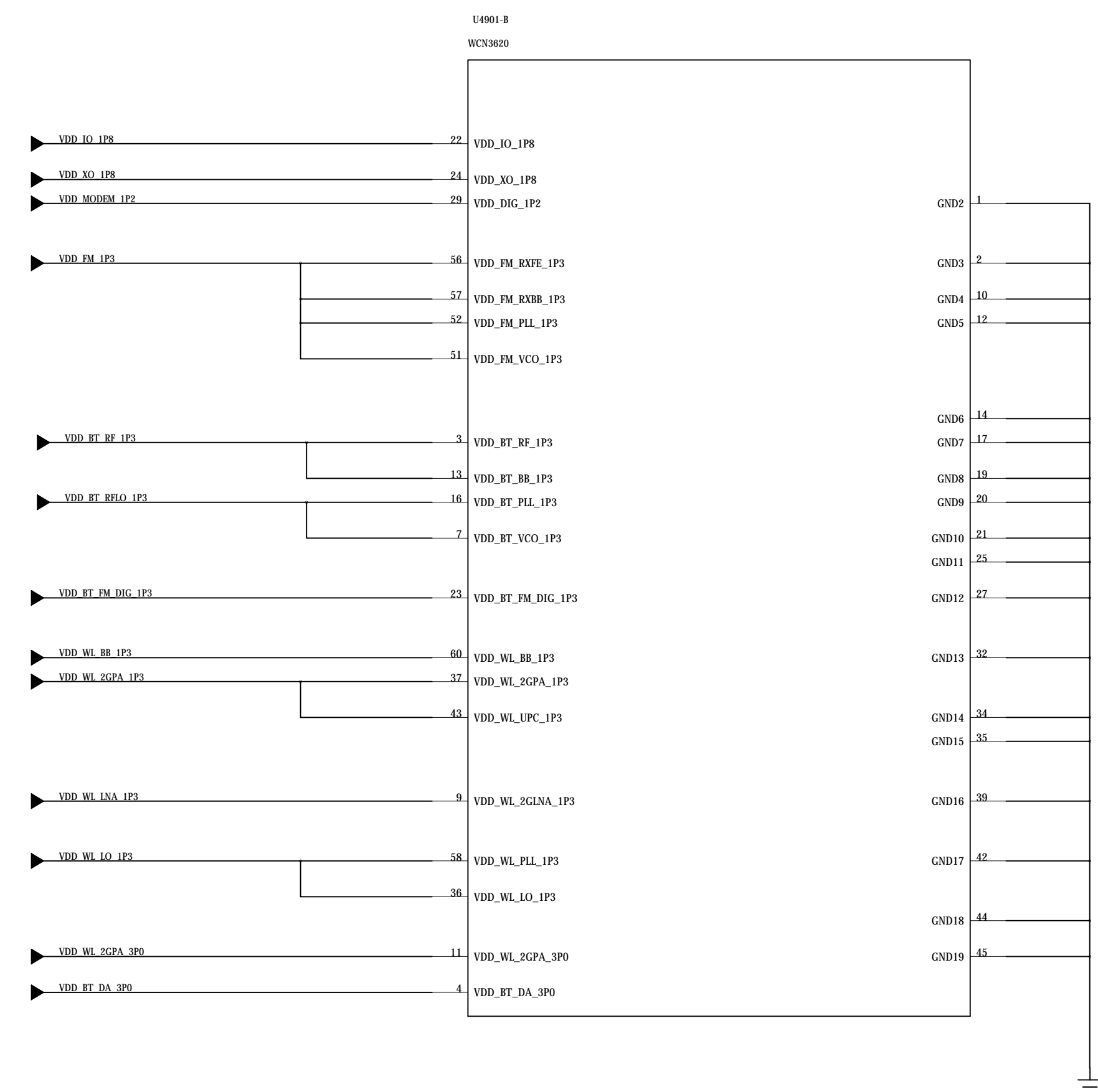
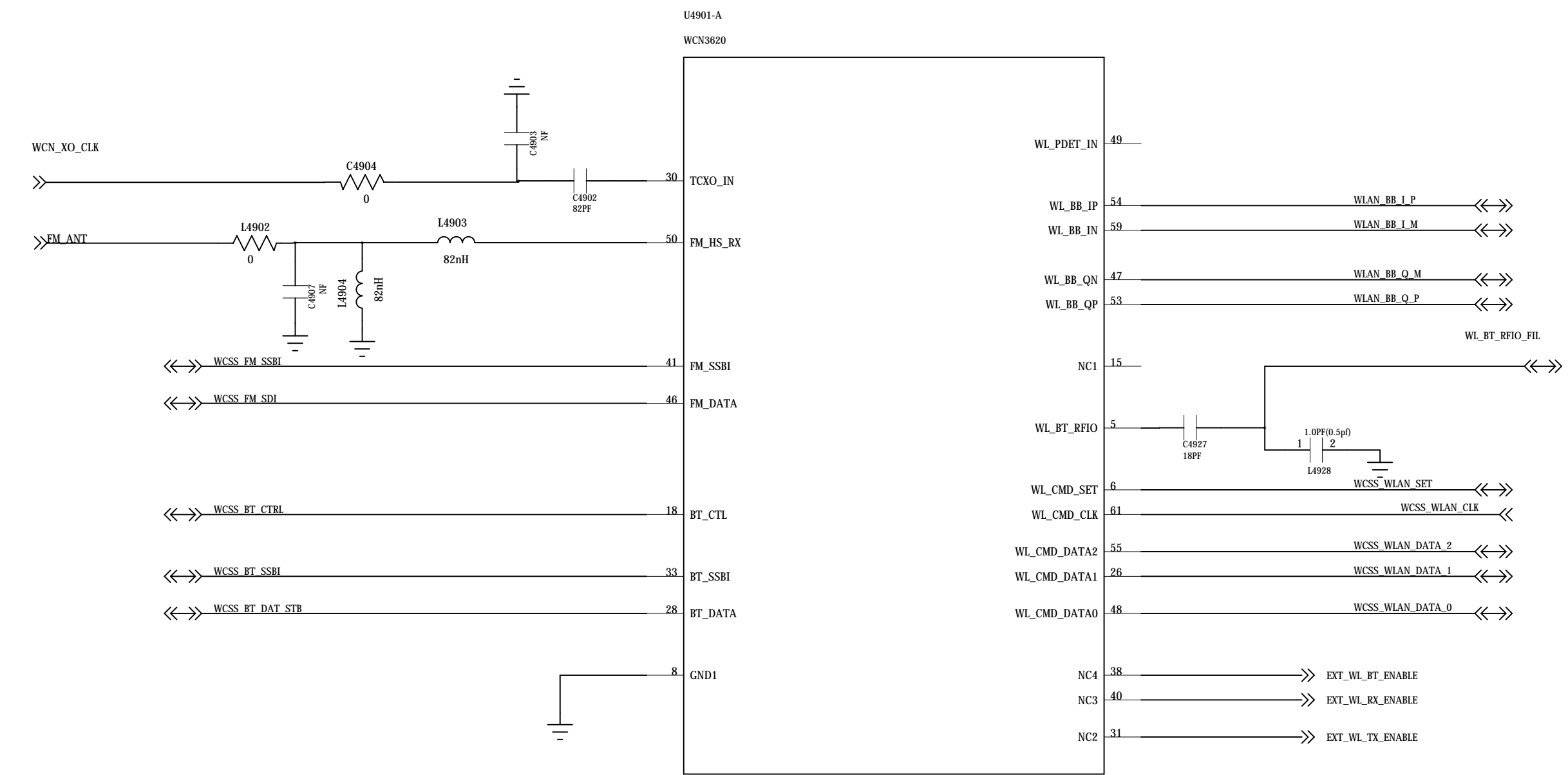
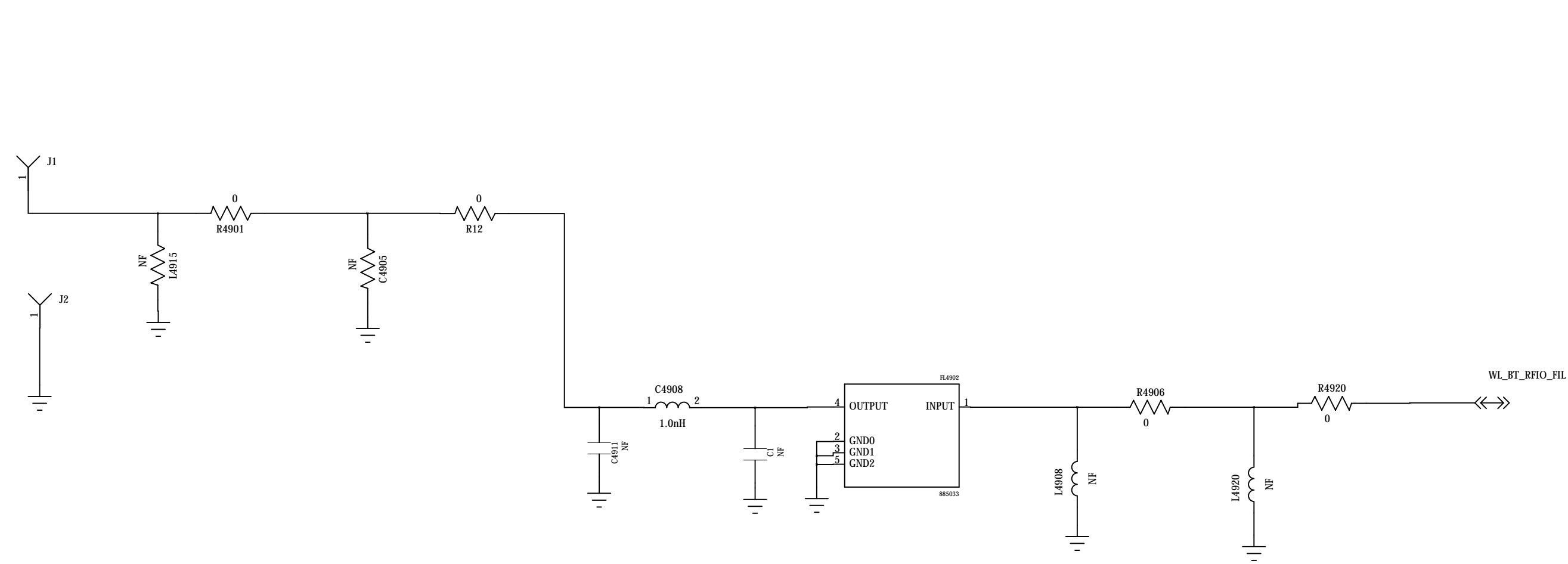
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Date: \_\_\_\_\_ Sheet: \_\_\_\_\_ of \_\_\_\_\_

Note: Use a single low impedance power plane/fill VPA for all ET PA VCC1/VCC2.  
 Refer to 80-NA681-91 rev.B or later revisions for more layout details.



# WIFI/BT



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**Title**  
SCHEMATIC, CCA, MAIN BOARD, QRD8916\_2.4-2, CMCC CSFR, EYT

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|-------|-------|-----|
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