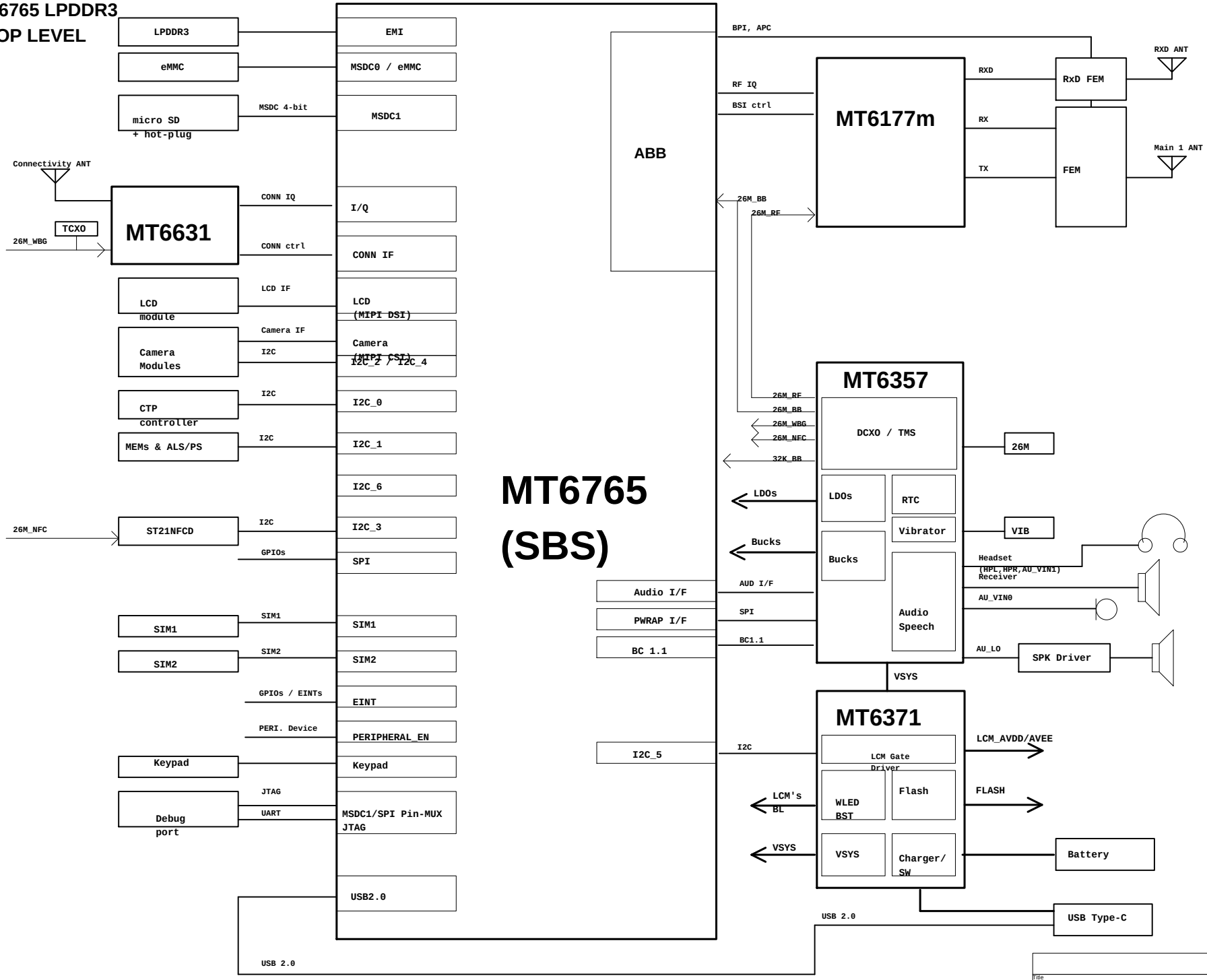
**Project : MT6765 LPDDR3**
**REF_SCH TOP LEVEL**

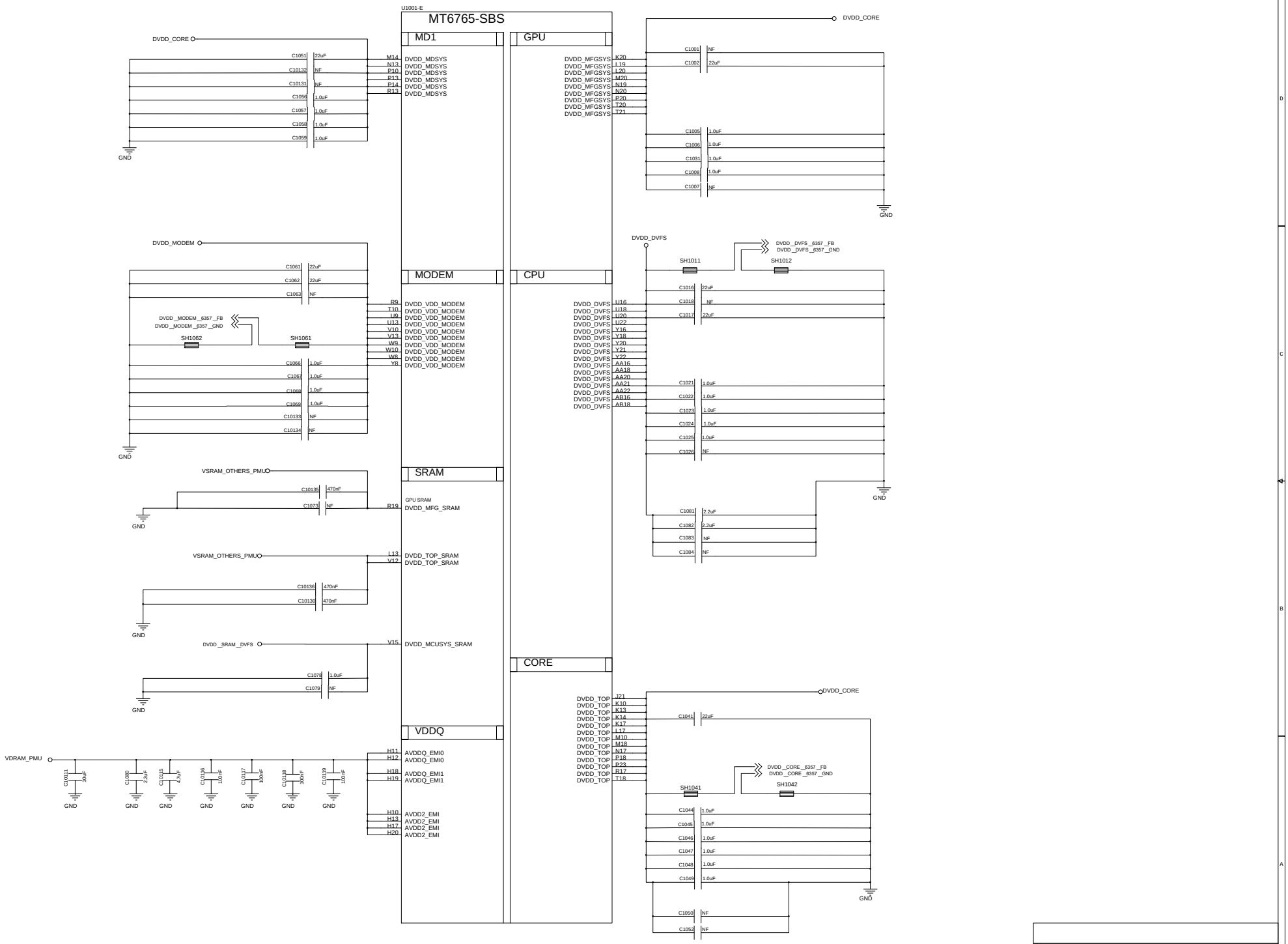



| | |
|---|---|
| Title | 01_Block_Diagram |
| Size A1 | MTK Confidential |
| Date: Friday, December 08, 2017 | Sheet 1 of 34 |

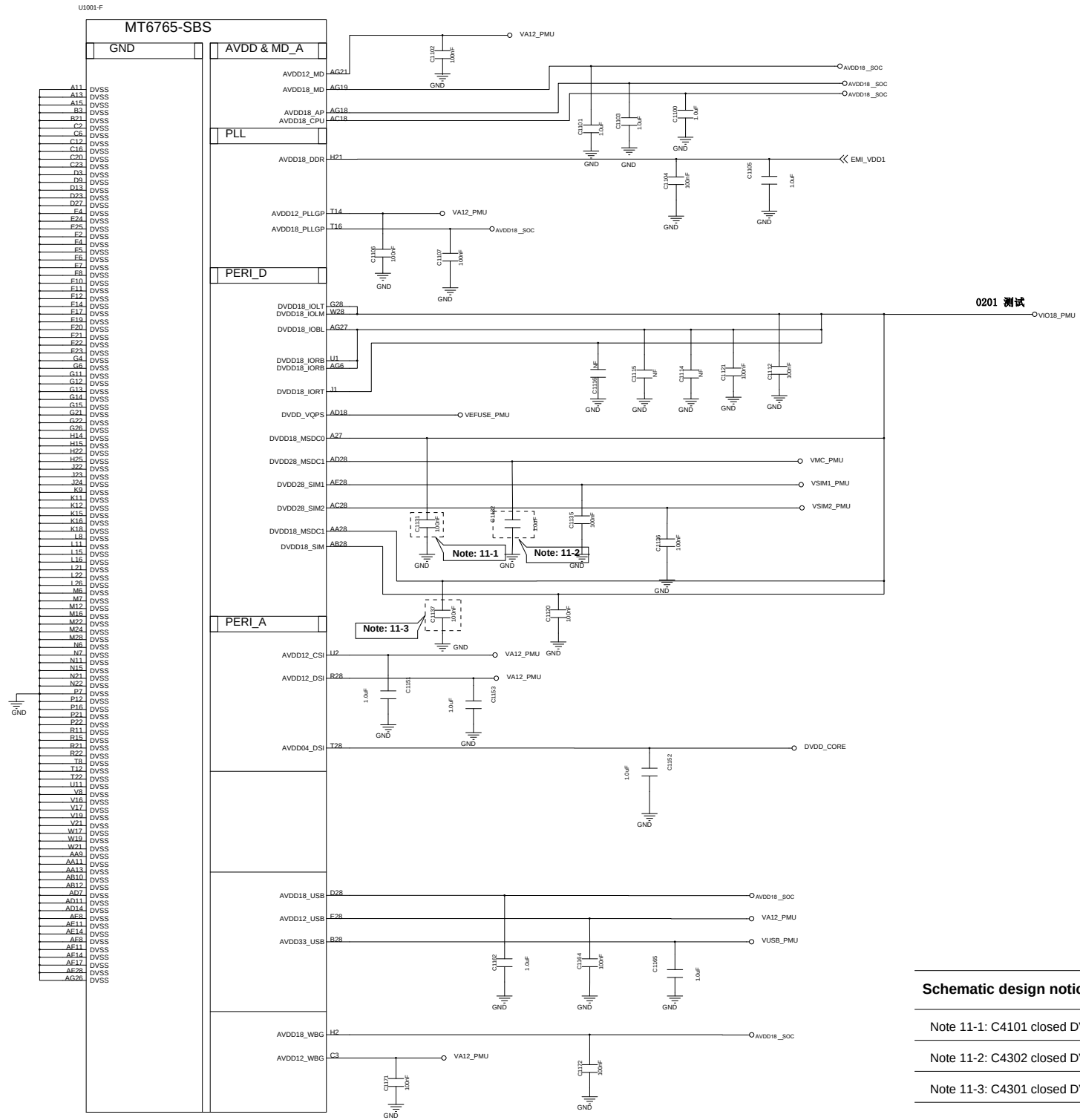
| I2C | Sub SYS | Function | Part Number | I2C Spec. | | i2C Slave Address / Write / Read (7-bit mode) | |
|---|---|---|---|---|---|---|---|
| I2C-0 | AP | Cap Touch controller | GT1151 | 400 Kbps | | 0x5D | Write:0xBA / Read:0xBB |
| | | | | | | | |
| I2C-1 (I3C) | AP Sensor Hub | Magnetic Sensor | AK09918C | 400 Kbps | | 0x0C | Write:0x18 / Read:0x19 |
| | | Ambient Light Sensor / Proximity Sensor | CM36558 | 400 Kbps | | 0x51 | Write:0xA2 / Read:0xA3 |
| | | Pressure Sensor | BMP280 | 400 Kbps | | 0x77 | Write:0xEE / Read:0xEF |
| I2C-2 (I3C) | AP | Rear Camera | IMX230 | 400 Kbps | | 0x1A | Write:0x34 / Read:0x35 |
| | | | EEPROM | 400 Kbps | | 0x50 | Write:0xA0 / Read:0xA1 |
| | | | AF driver | 400 Kbps | | 0x0C | Write:0x18 / Read:0x19 |
| | | | | | | | |
| I2C-3 | AP | Audio Smart PA | RT5510 | 400 Kbps | | 0x34 | Write:0x68 / Read:0x69 |
| | | | | | | | |
| | | NFC | ST21NFCD | 400 Kbps | | 0x08 | Write:0x10 / Read:0x11 |
| I2C-4 (I3C) | AP | Front Camera | S5K2T7 | 400 Kbps | | 0x2D | Write:0x5A / Read:0x5B |
| | | | EEPROM | 400 Kbps | | 0x52 | Write:0xA4 / Read:0xA5 |
| | | | AF driver=NA | | | | |
| I2C-5 | AP | Sub-PMIC | MT6371 PMU | 3.4 Mbps | | 0x34 | Write:0x68 / Read:0x69 |
| | | | MT6371 PD | 3.4 Mbps | | 0x4E | Write:0x9C / Read:0x9D |
| I2C-6 | AP | | | | | | |

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

| Date | Category | Item |
|---|---|---|
| 2017.11.24 (V0.1) | Page 05 | V0.1 Release |
| 2017.12.7 (V0.2) | Page 11 | Change power of AVDD18_DDR(H21) from VIO18_PMU to EMI_VDD1, connecting EMI_VDD1 to SH2102 in star connection |
| | Page 12 | Add Note 12-5 |
| | Page 21 | Add SH2102 for star connection among EMI_VDD1, AVDD18_SOC, and VIO18_PMU |
| | Page 22 | 1. Change C2304 from C / 1 / uF / 10V to C / 1 / uF / 6.3V<br>2. Change R2301 from R / 1.5 / K to R / 7.5 / K<br>3. Update Note 22-5 |
| | Page 44 | 1. To enhance LPDDR3 power off sequence,change C4422 from 0.1uF to 2.2uF, and change C4423 from 0.1uF to 1uF<br>2. Change VDD1 power of eMCP from VIO18_PMU to EMI_VDD1, fulfilling power rail in star connection |
| | Page 51 | 1. Add 2nd source plan for U5004<br>2. Add Note 51-3 and Note 51-4 |




| | |
|---|---|
| Title | 10_BB_ POWER_PDN |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 4 of 34 |

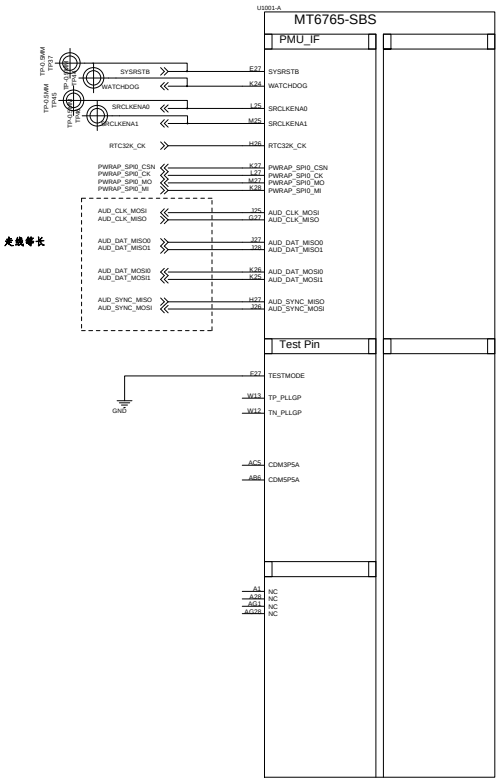


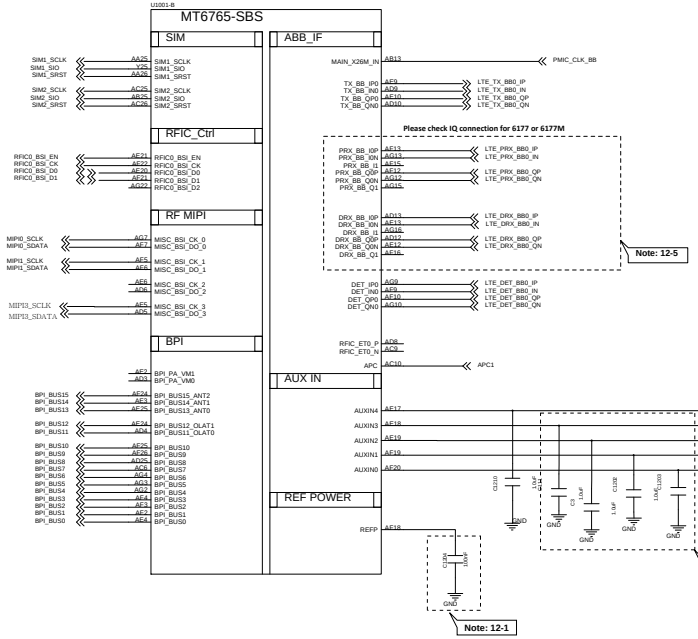

**Schematic design notice of "11_BB_POWER_IO" page.**

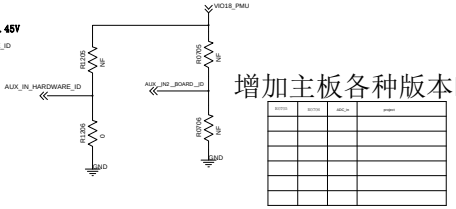
Note 11-1: C4101 closed DVDD18_MSDC0 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: C4301 closed DVDD18_MSDC1 150mil




增加主板各种版本ID

| | | | |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

**Schematic design notice of "12_BB_1" page.**

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

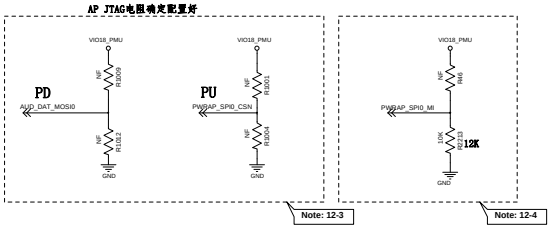
| PWRAP_SPI0_CSN | AUD_DAT_MOSI0 | JTAG Function | |
|---|---|---|---|
| default=PU | default=PD | AP_JTAG | MD_JTAG |
| HI | LO | N/A | N/A |
| HI | HI (by ext. PU) | SPI0+EINT8 | SPI1+SPI3 |
| LO (by ext. PD) | LO | SPI0+EINT8 | N/A |
| LO (by ext. PD) | HI (by ext. PU) | MSDC1 | N/A |

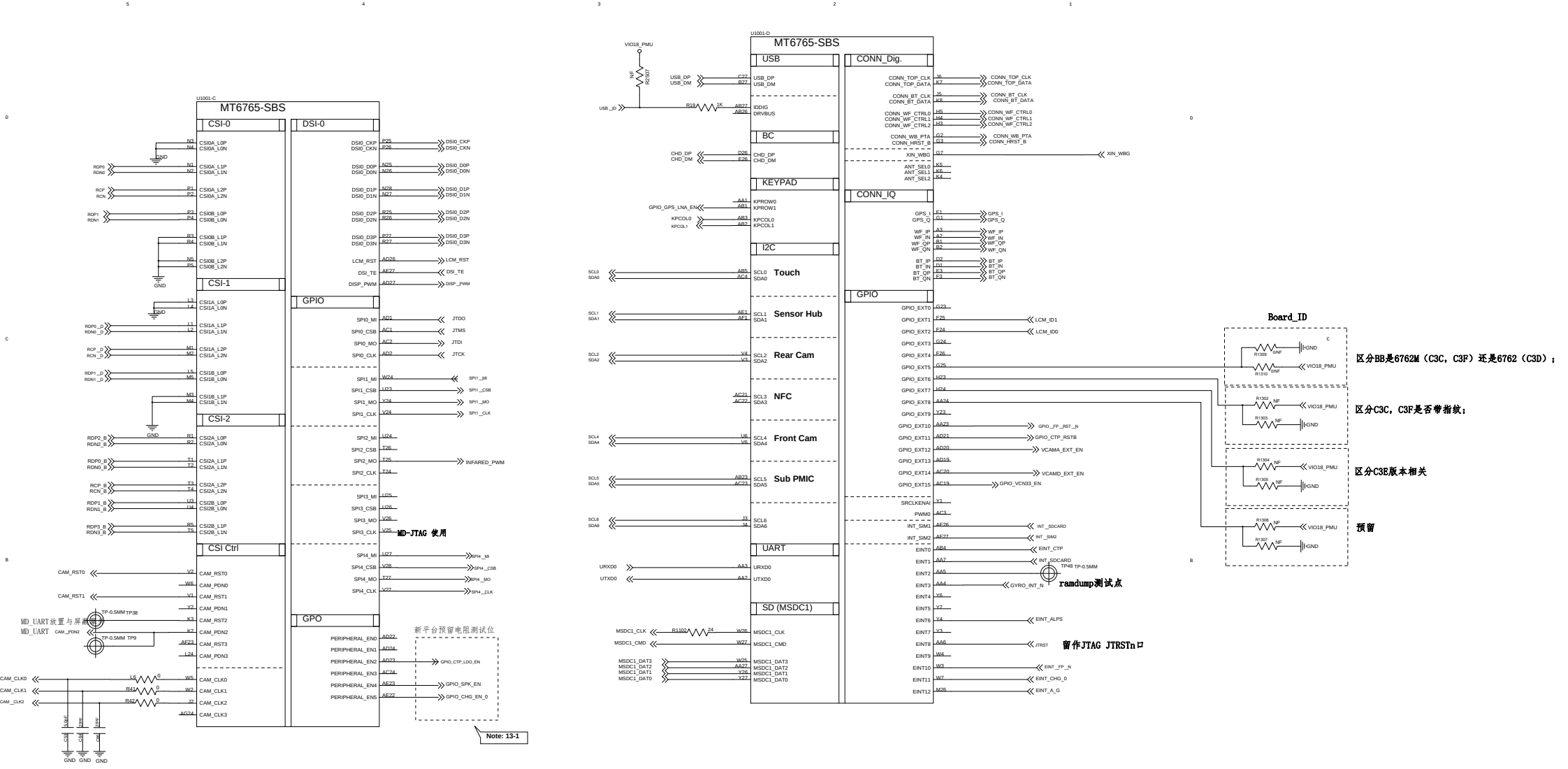
Note 12-4: PWRAP_SPI0_MO and PWRAP_SPI0_MI are DDR type feature in bootstrap

| PWRAP_SPI0_MI | Booting interface | |
|---|---|---|
| default=PU | DDR | MSDC0 pin mux |
| LO (by ext. PD) | LPDDR3 | follow LP3 Ref SCH. |
| HI | LPDDR4X | follow LP4X Ref SCH. |

Note 12-5: Please set unused IQ pins in NC

注释错误







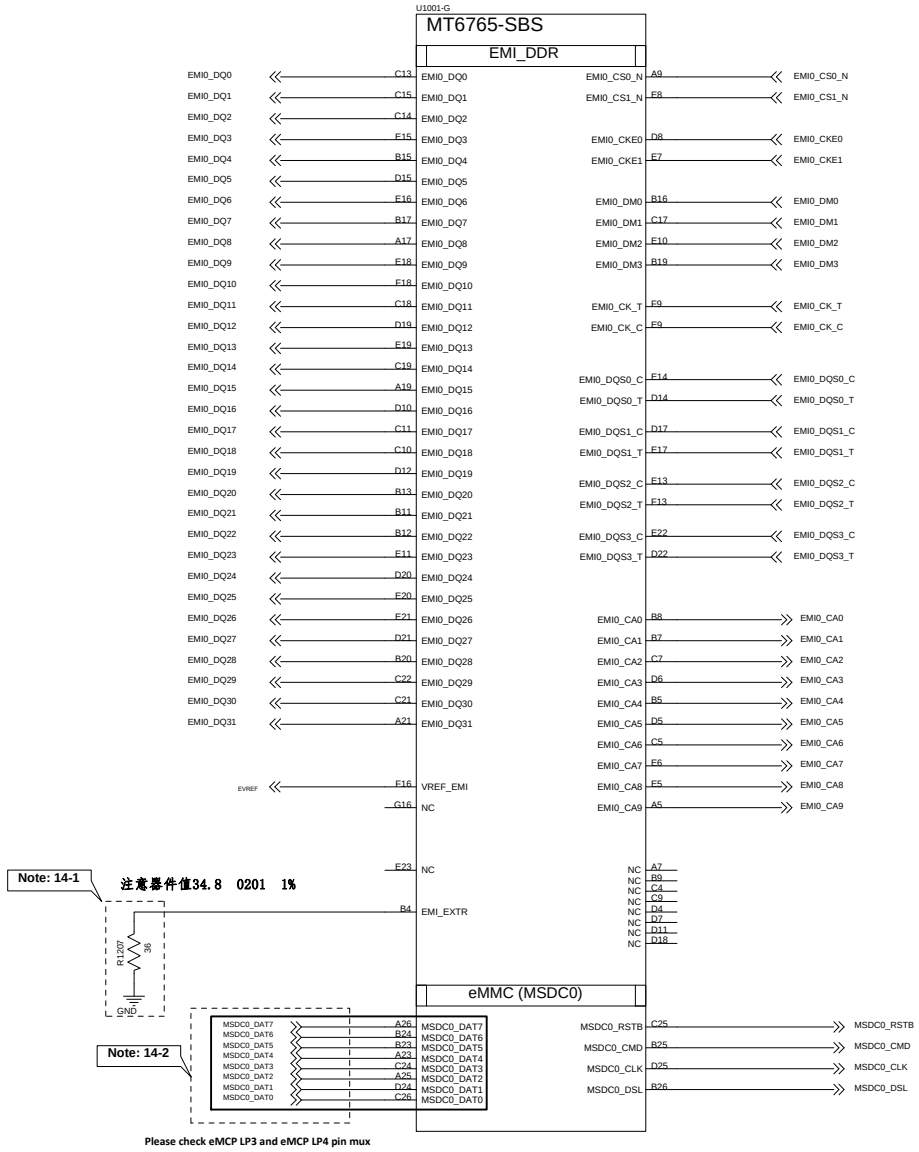


**Schematic design notice of "13_BB_2" page.**

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]

If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

| | | |
|---|---|---|
| Title | 13_BB_2 | |
| Size A1 | MTK Confidential | |
| Date: Thursday, November 02, 2017 | Sheet 7 of 34 | |

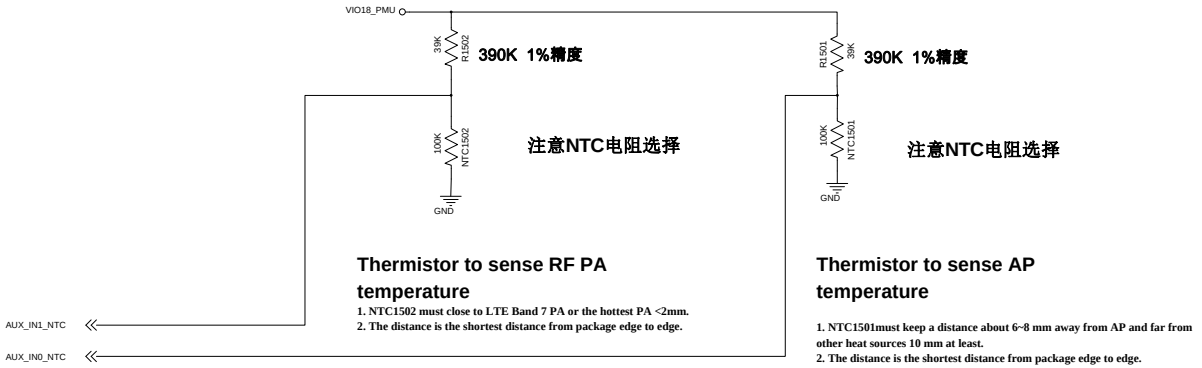



**Schematic design notice of "14_BB_3" page.**

Note 14-1: R4001 please select 34.8 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux

| | | |
|---|---|---|
| Title | 14_BB_3 | |
| Size A1 | MTK Confidential | |
| Date: Thursday, November 02, 2017 | Sheet 8 of 34 | |



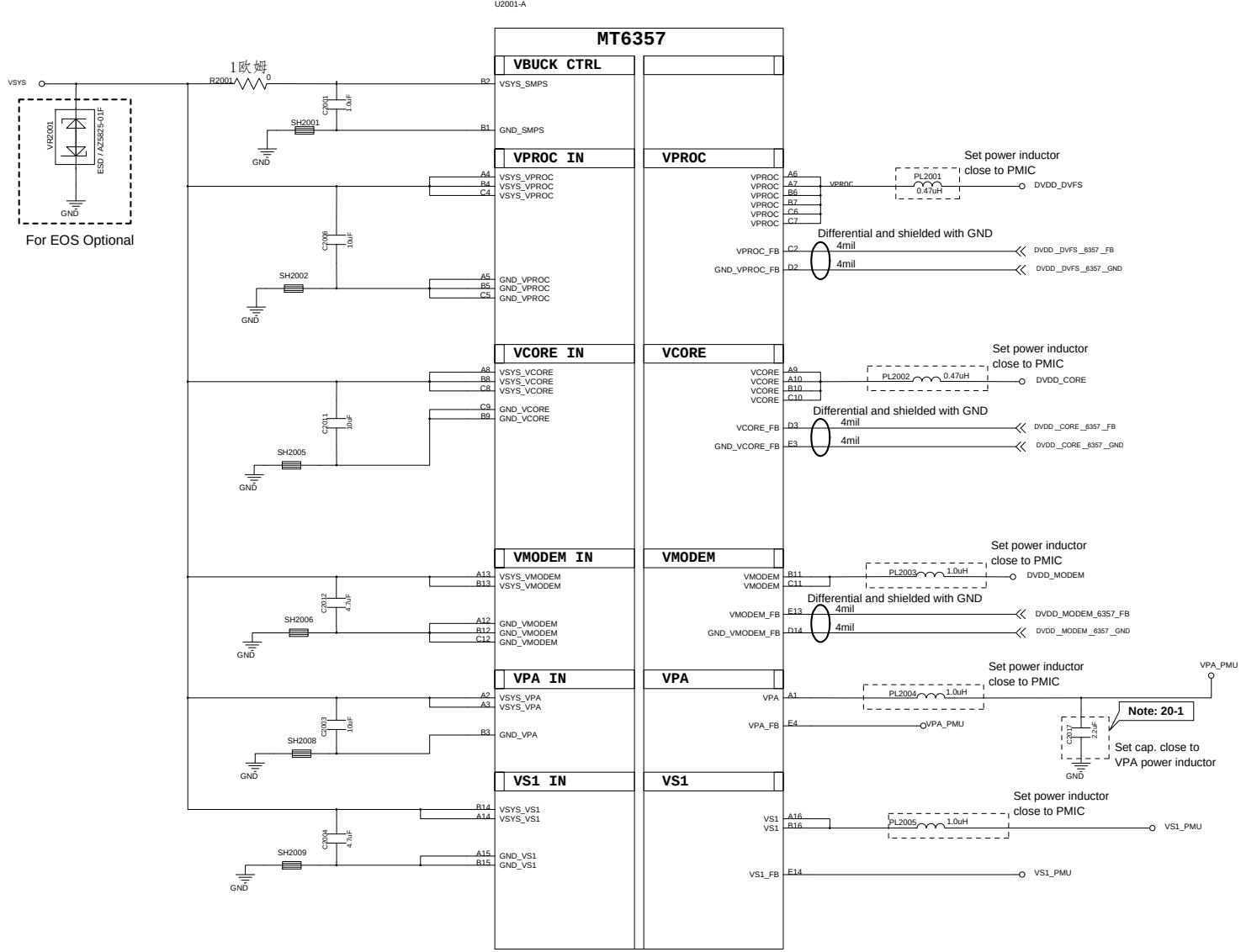

**Thermistor to sense RF PA temperature**

**1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm.**
**2. The distance is the shortest distance from package edge to edge.**

**Thermistor to sense AP temperature**

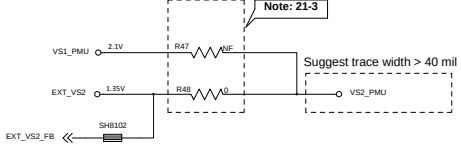
**1. NTC1501must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.**
**2. The distance is the shortest distance from package edge to edge.**

| | |
|---|---|
| Title | 15_BB_AUXADC_Thermal |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 9 of 34 |

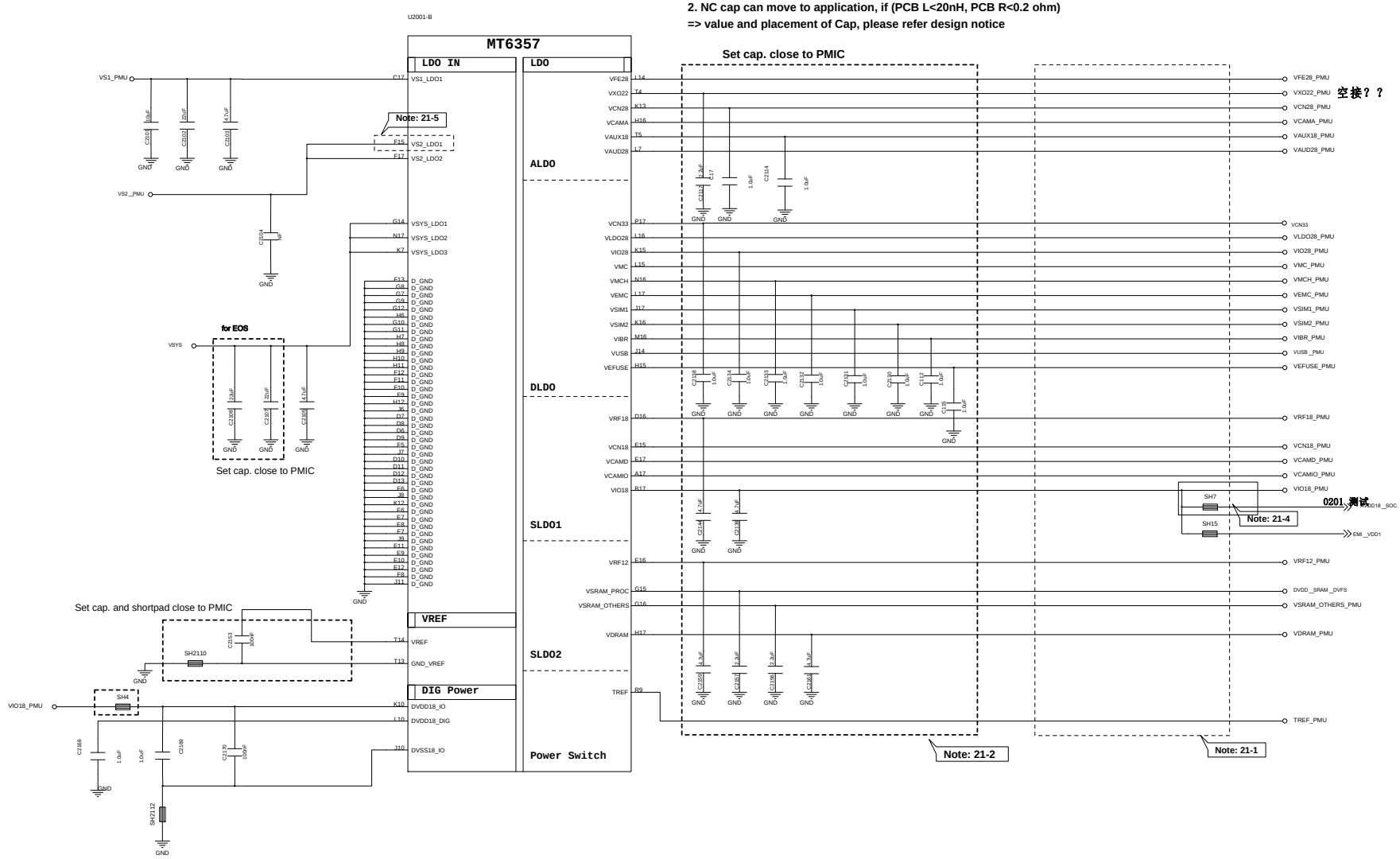



## Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: To reserve a cap., C2041, please choose 0603 size




**1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.**
**2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)**
**=> value and placement of Cap, please refer design notice**




## Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

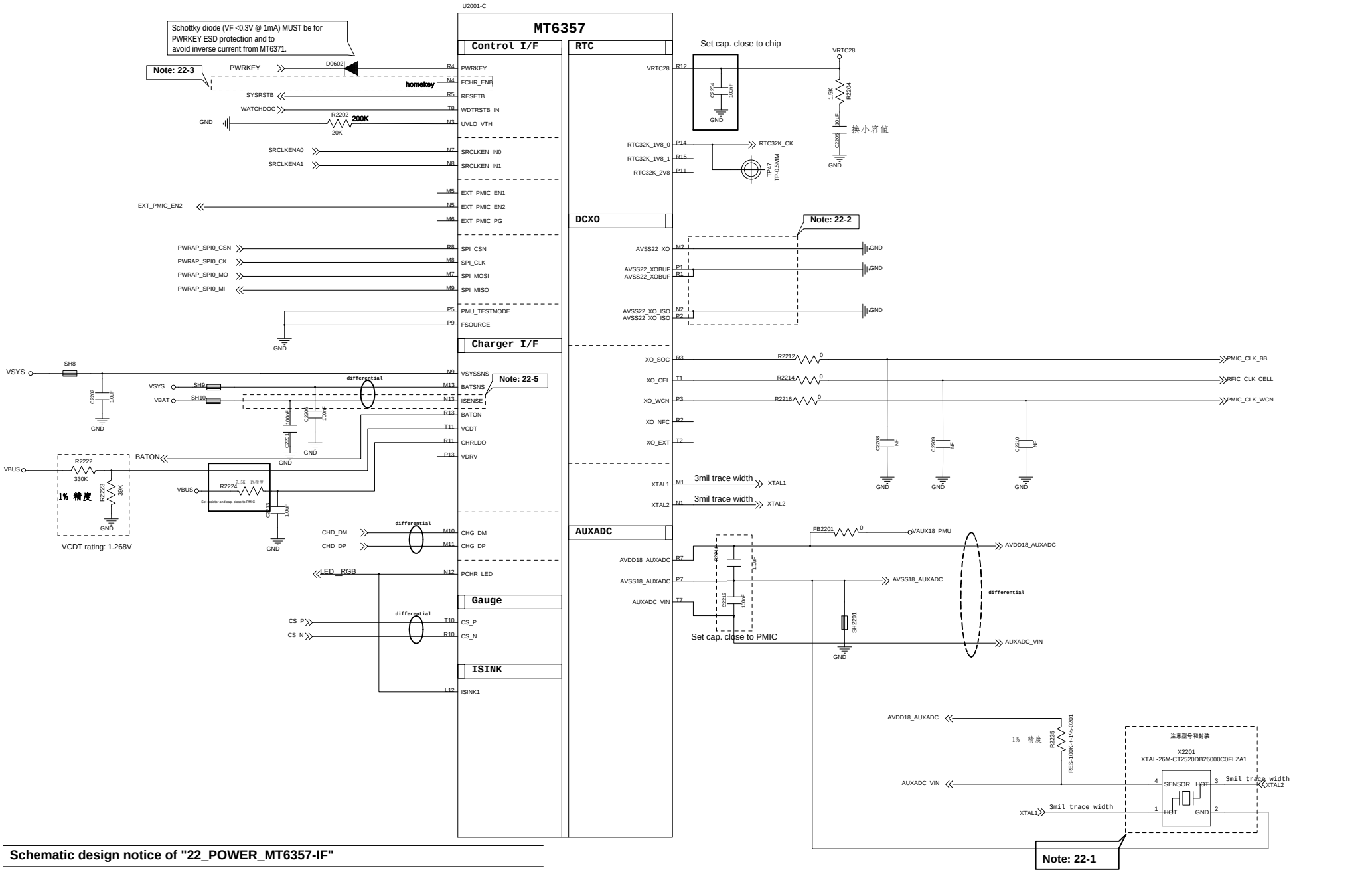
Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

| | Ext. buck option | |
|---|---|---|
| | w/ EXT VS2 Buck | w/o EXT VS2 Buck |
| C2104 | 10uF | 22uF |
| R2851 | 0-ohm , 0603 | NC |
| R2852 | NC | 0-ohm , 0603 |

Note 21-4: Please set SH2101 close to C2141, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2141
Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

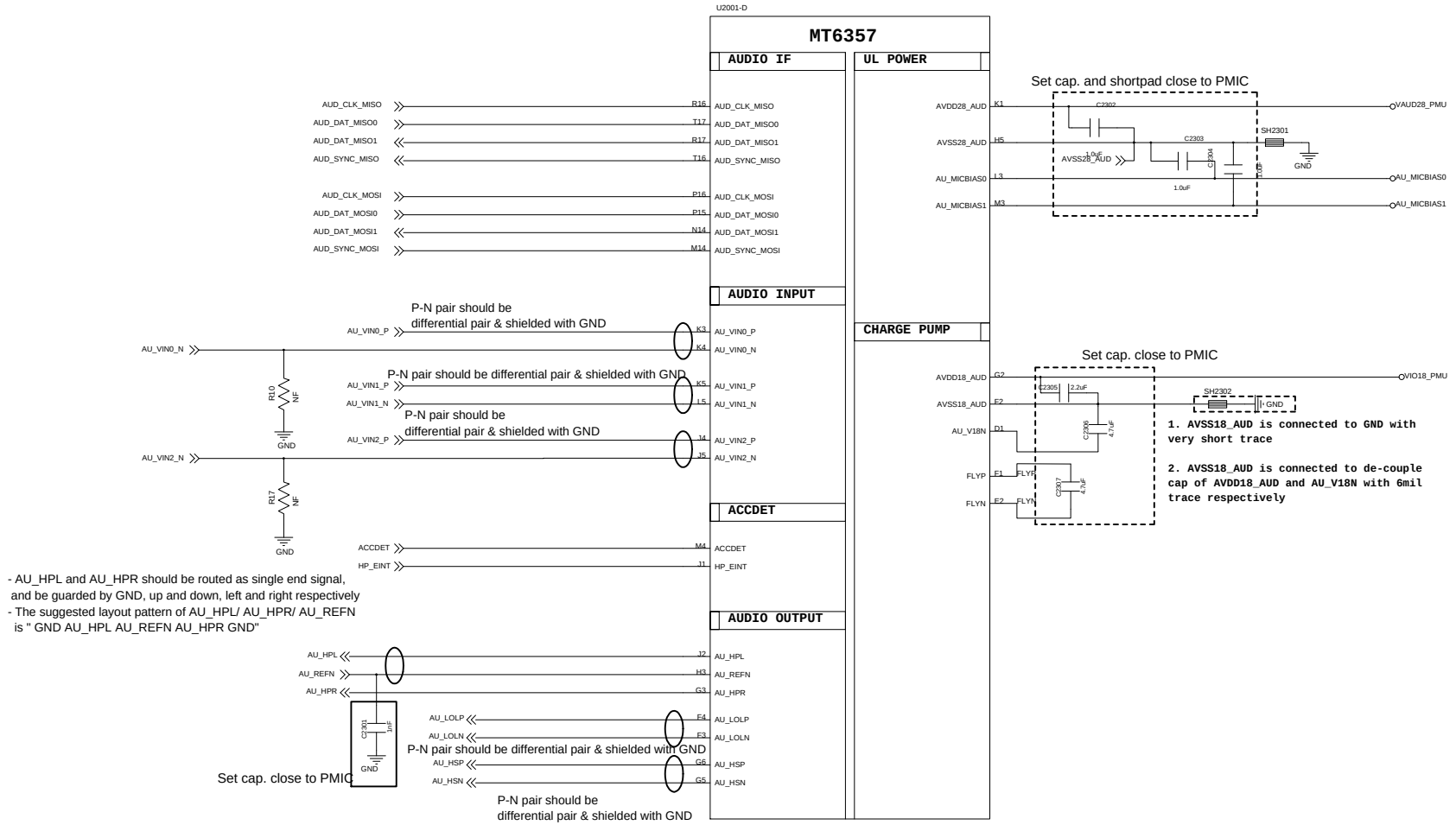



Route AVDD18_AUXADC, AUXADC_VIN, and AVSS18_AUXADC with 3mils width traces and well GND shielding

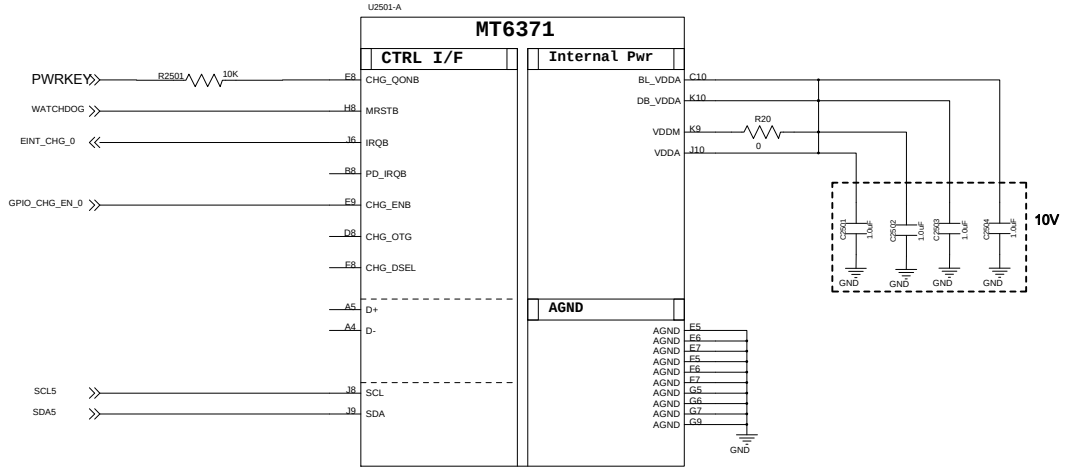
## Schematic design notice of "22_POWER_MT6357-IF"

| | |
|---|---|
| Note 22-1: | Please implement 2520 & 2016 Size TMS PCB co-layout.<br>Please refer to MT6765_MT6357 Co-Clock Design Notice for co-layout guide |
| Note 22-2: | 1. Please Connect P1 and R1 ball first and then to GND<br>2. Please Connect P2 and N2 ball first and then to GND<br>3. Please connect DCXO GND to main GND by independent L1-2 GND via.;<br>DO NOT connect it through L1 GND |
| Note 22-3: | Let floating if disable HOMEKEY function |
| Note 22-4: | Please follow MT6765_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD. |
| Note 22-5: | Please connect to battery connector |

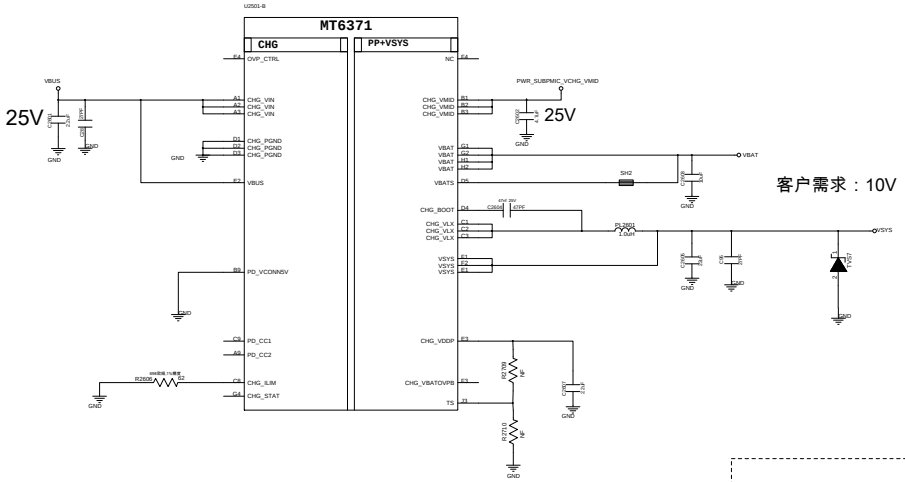
| | |
|---|---|
| Title | 22_POWER_MT6357-IF |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 12 of 34 |

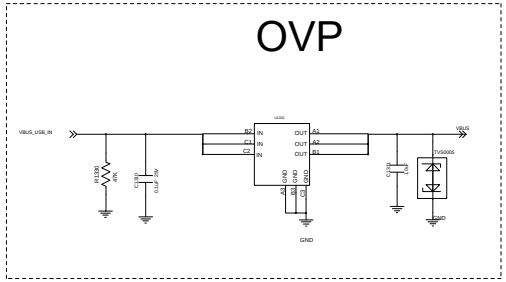


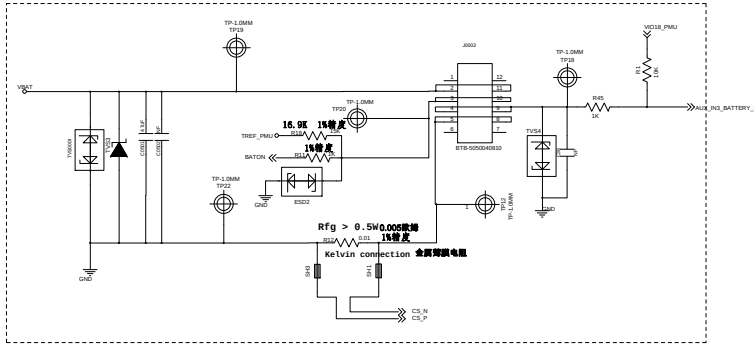

| | |
|---|---|
| Title | 23_POWER_MT6357-Audio |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 13 of 34 |




| | |
|---|---|
| Title | 25_POWER_SubPMIC-General |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 14 of 34 |



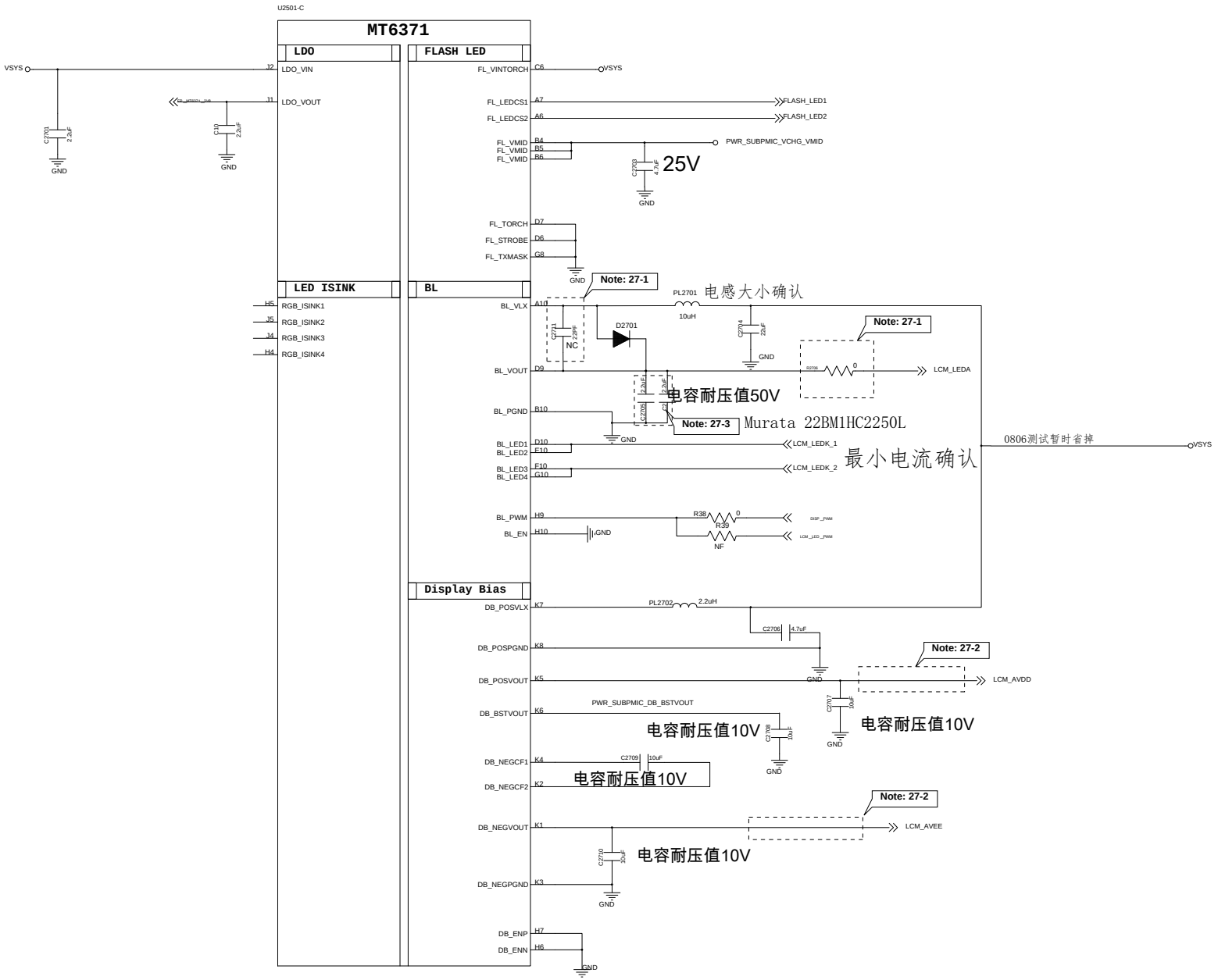

Note: 26-1

**Schematic design notice of "26_POWER_MT6370-Charger + PP" page.**

Note 26-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

| | |
|---|---|
| File | 26_POWER_SubPMIC-Charger + PP |
| Size: A1 | MTK Confidential |
| Date: Thursday, November 02, 2017 | Sheet 15 of 34 |

1




## Schematic design notice of "27_POWER_SubPMIC-HV powers" page:

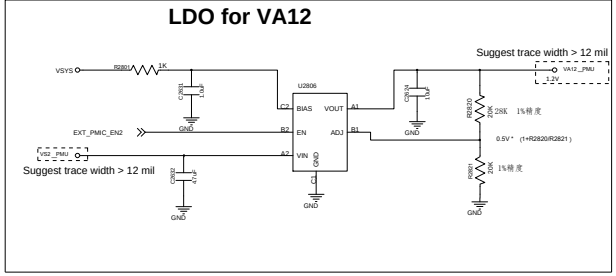
Note 27-1: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0402 cap for BOM fine tuning.

Note 27-2: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0201 cap. for BOM fine tuning.

Note 27-3: C2705 could be replaced with C / 1 / uF / 50V + C / 1 / uF / 50V

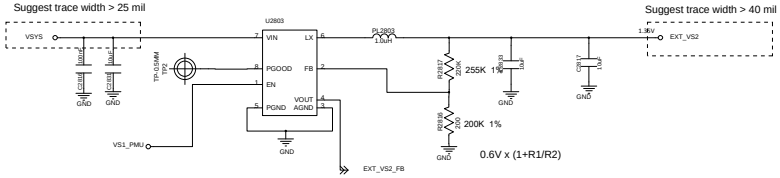
| | |
|---|---|
| Title | 27_POWER_SubPMIC-HV powers |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 16 of 34 |

## LDO for VA12




## Ext. Bulk for VS2

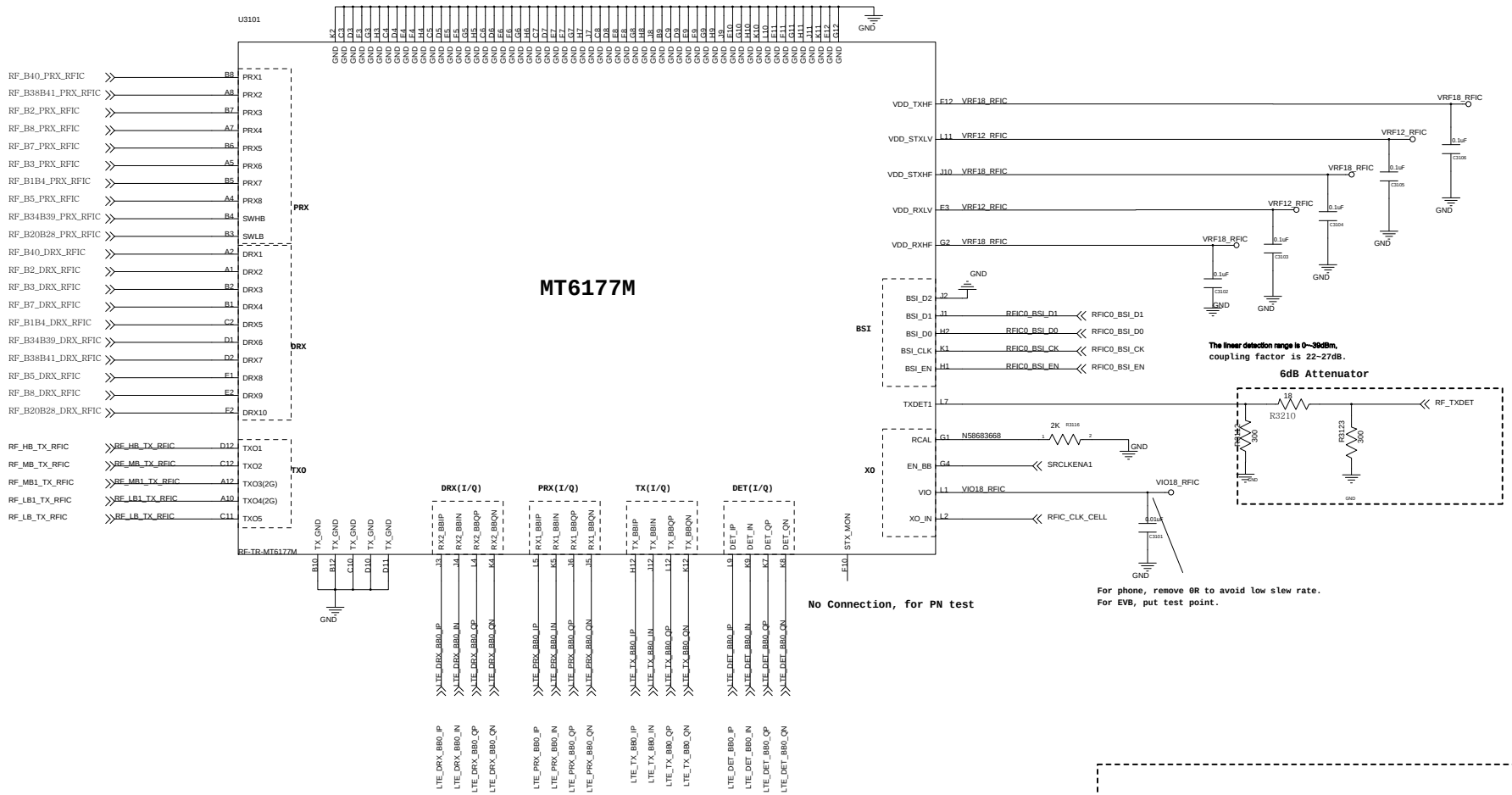
**Note: 28-2**



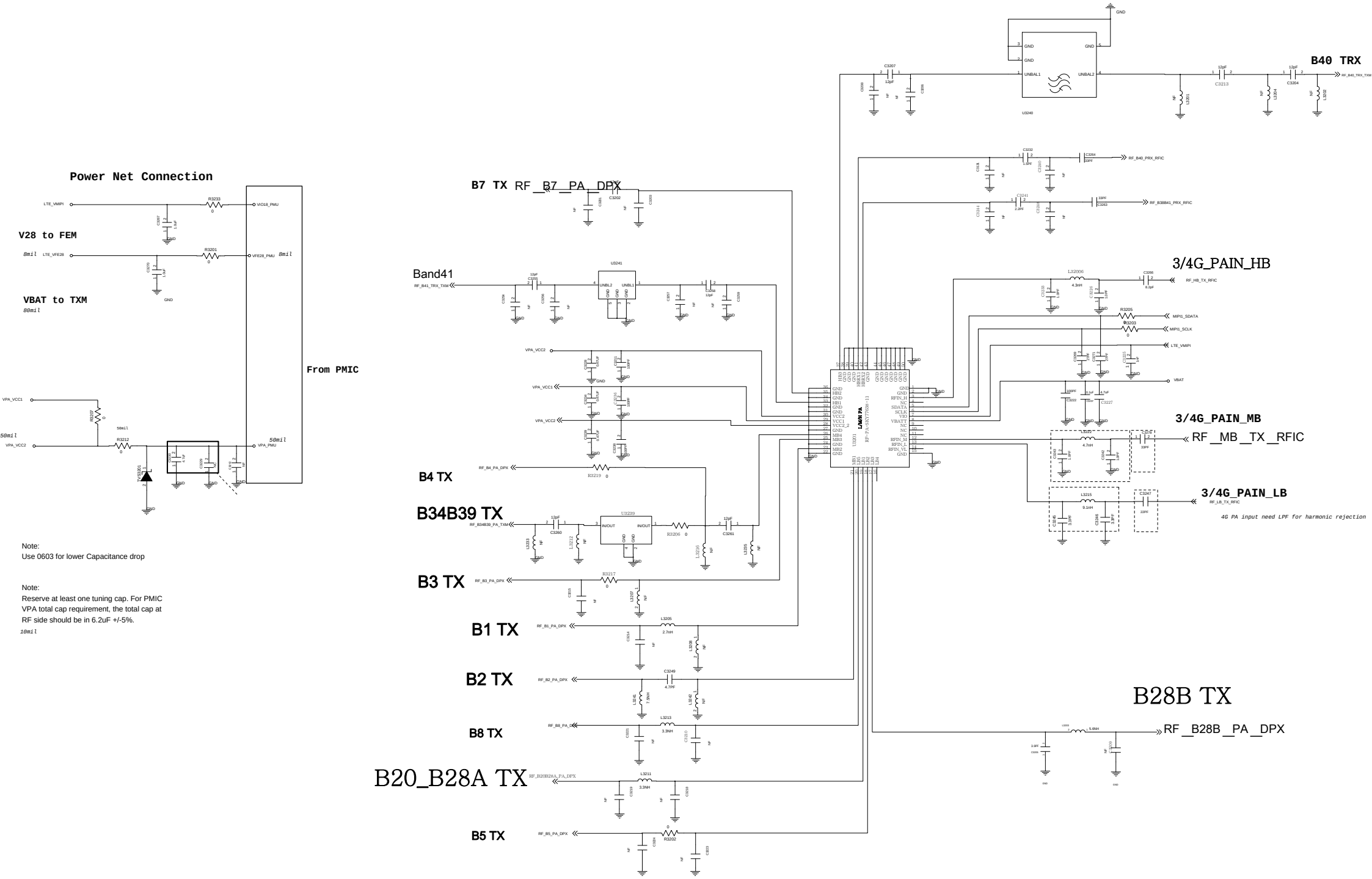

## LDO for VCN33

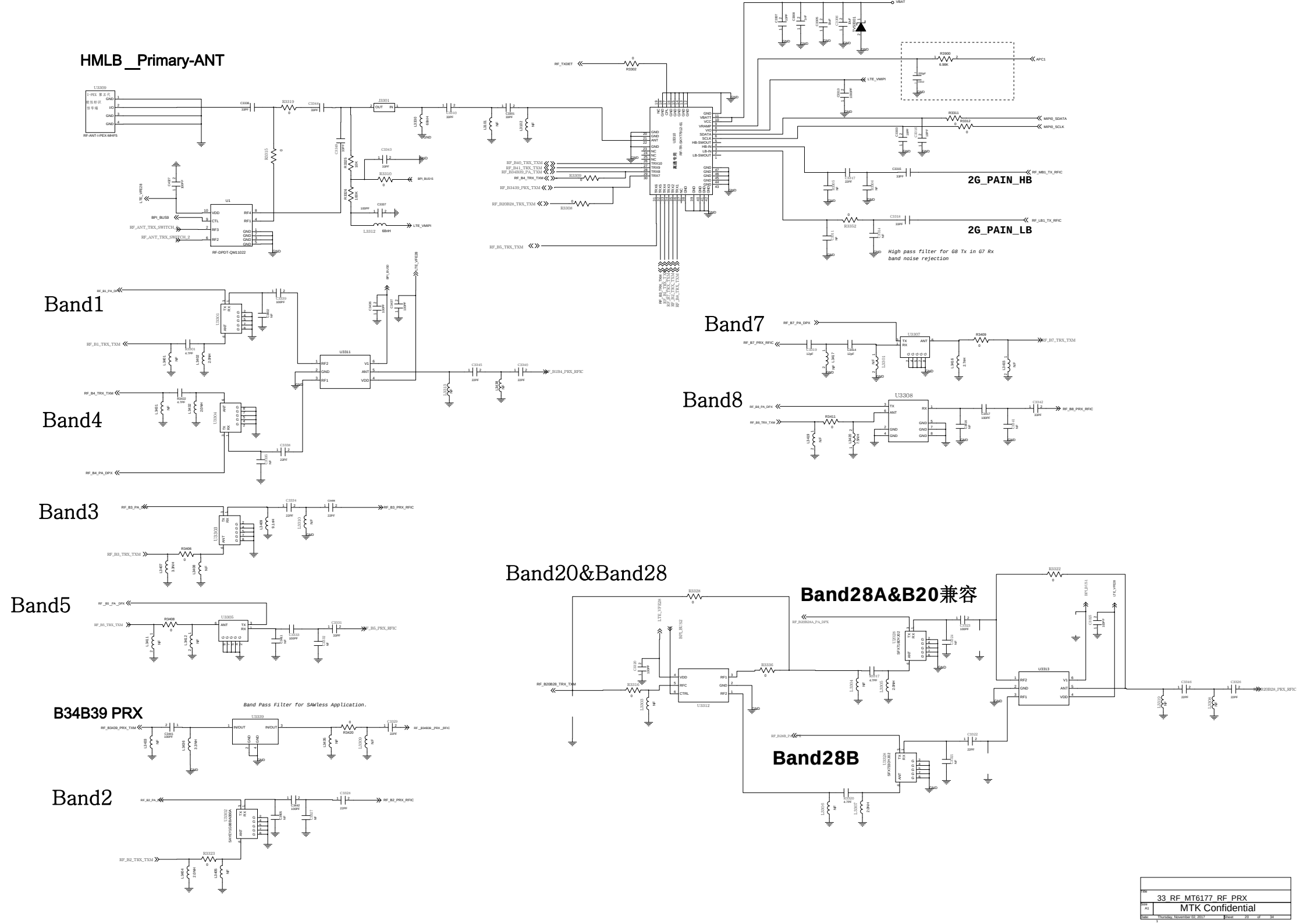
**Please check MT67xx QVL**

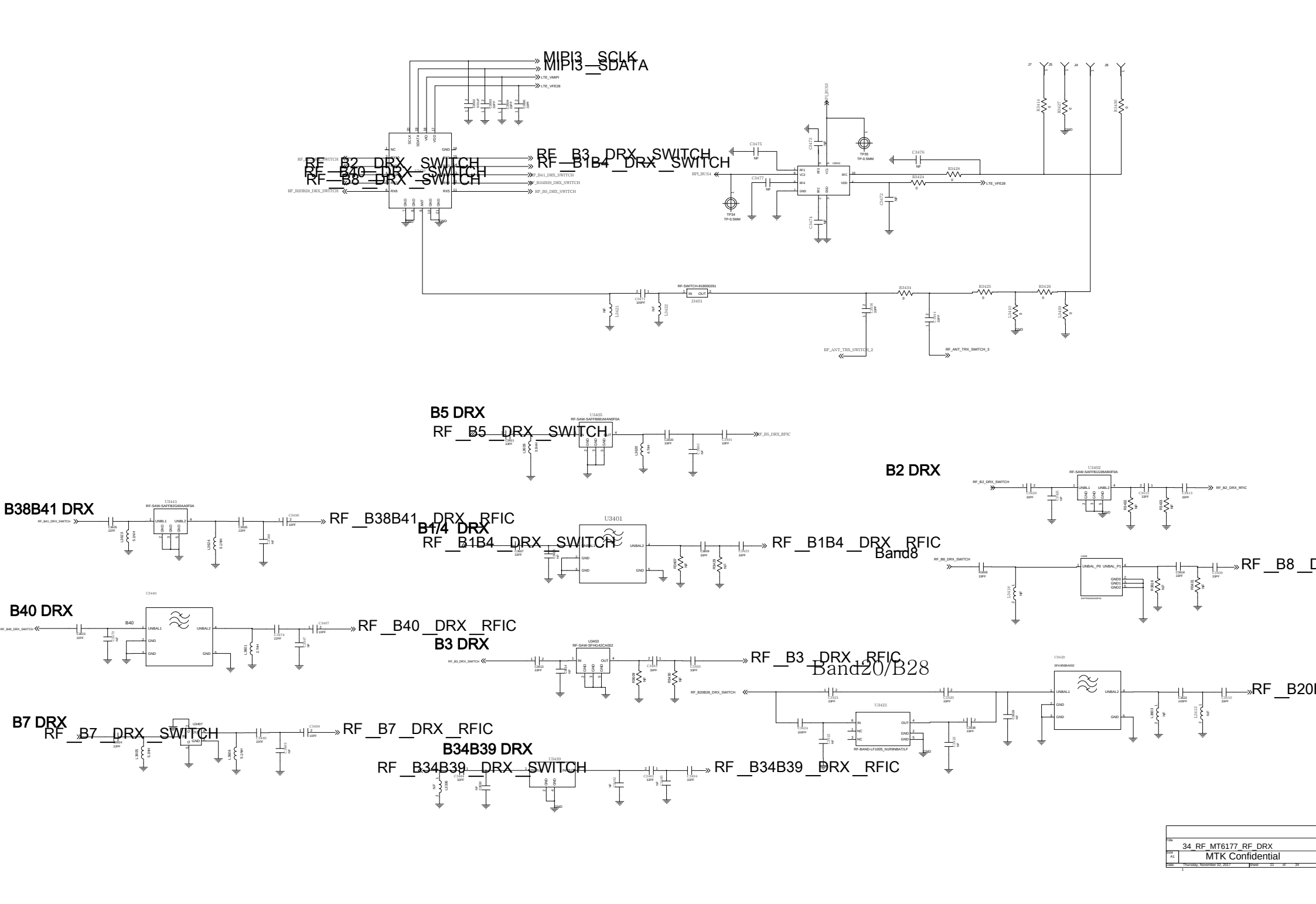
| **Schematic design notice of "28_POWER_ThirdParty-Power"** | |
|---|---|
| Note 28-1: | VA12 Layout placement please close to AP |
| Note 28-2: | VS2 Buck Layout placement please close to PMIC MT6357 |
| Note 28-3: | VCN33 LDO Layout placement please close to MT6631 |



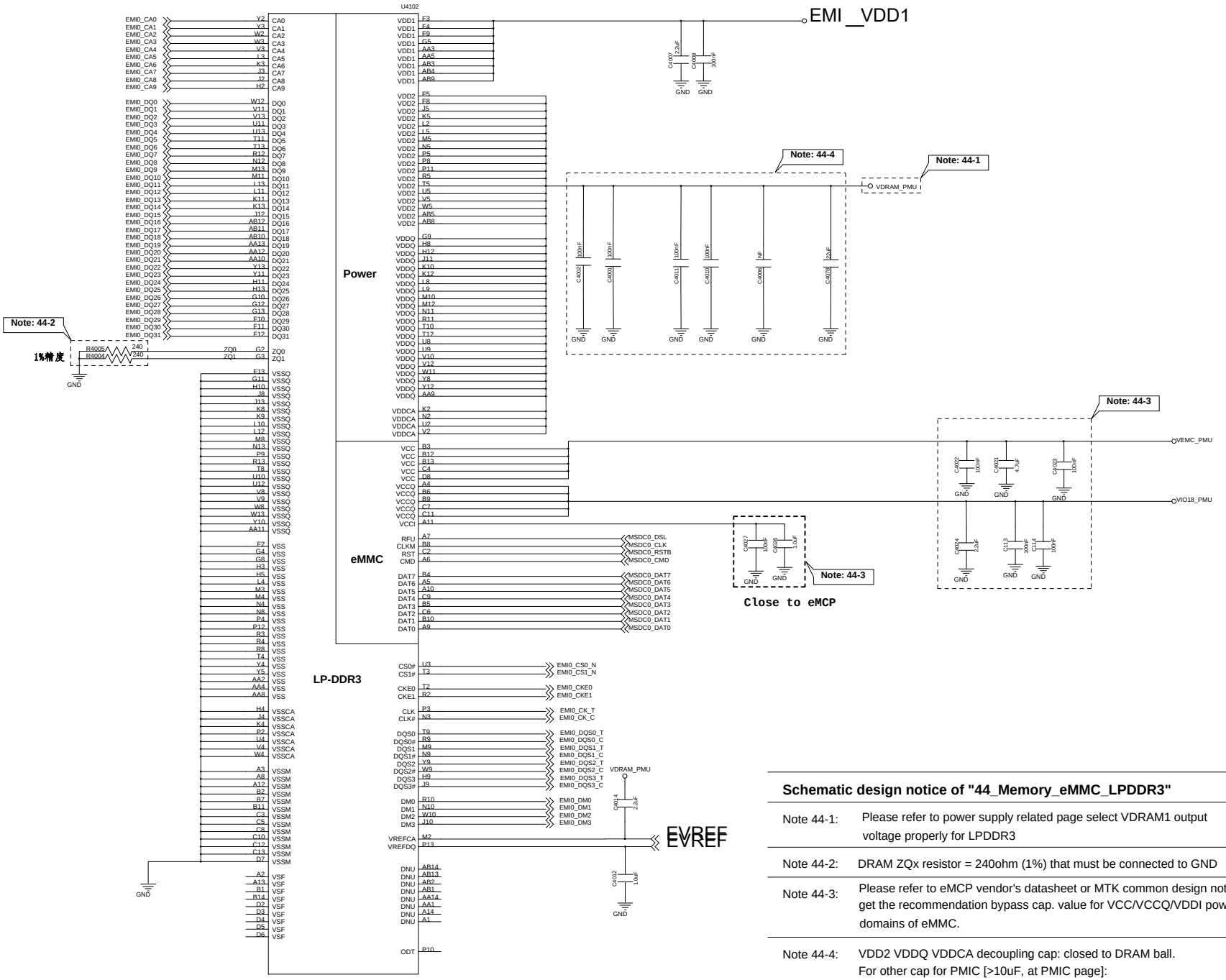

| | |
|---|---|
| Title | 31_RF_MT6177_Pin_Out |
| Size A1 | MTK Confidential |
| Date: Thursday, November 02, 2017 | Sheet 18 of 34 |


Power Net Connection
V28 to FEM
VBAT to TXM
From PMIC
Note:
Use 0603 for lower Capacitance drop
Note:
Reserve at least one tuning cap. For PMIC VPA total cap requirement, the total cap at RF side should be in 6.2uF +/-5%.
B7 TX
RF__B7__PA__DPX
Band41
B4 TX
B34B39 TX
B3 TX
B1 TX
B2 TX
B8 TX
B20_B28A TX
B5 TX
B40 TRX
RF__B40_TRX_TXM
RF__B40_PRX_RFIC
RF__B38B41_PRX_RFIC
3/4G_PAIN_HB
RF__HB_TX_RFIC
MIPI1_SDATA
MIPI1_SCLK
LTE_VMIPI
VBAT
3/4G_PAIN_MB
RF__MB__TX__RFIC
3/4G_PAIN_LB
RF_LB_TX_RFIC
4G PA input need LPF for harmonic rejection
B28B TX
RF__B28B__PA__DPX

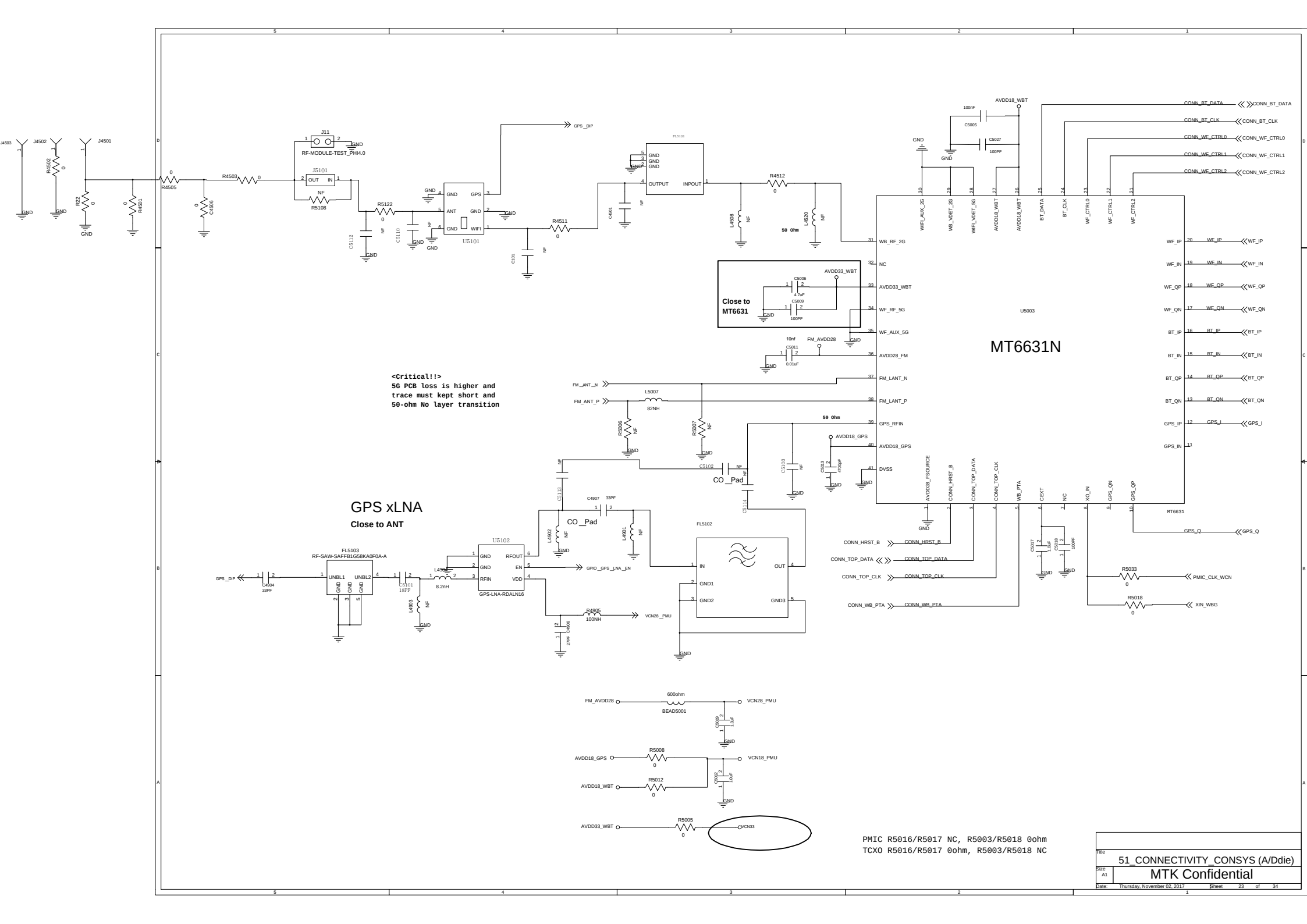

HMLB__Primary-ANT
2G_PAIN_HB
2G_PAIN_LB
High pass filter for G8 Tx in G7 Rx
band noise rejection
Band1
Band4
Band7
Band8
Band3
Band5
Band20&Band28
Band28A&B20兼容
Band28B
B34B39 PRX
Band Pass Filter for SAWless Application.
Band2
33_RF_MT6177_RF_PRX
MTK Confidential


MIPI3_SCLK
MIPI3_SDATA
LTE_VMIPI
LTE_VFE28
RF_B3_DRX_SWITCH
RF_B1B4_DRX_SWITCH
RF_B2_DRX_SWITCH
RF_B40_DRX_SWITCH
RF_B8_DRX_SWITCH
RF_B20B28_DRX_SWITCH
RF_B41_DRX_SWITCH
RF_B34B39_DRX_SWITCH
RF_B5_DRX_SWITCH
BPI_BUS3
BPI_BUS4
RF-SWITCH-81800291
RF_ANT_TRX_SWITCH_2
RF_ANT_TRX_SWITCH_3
B5 DRX
RF_B5_DRX_SWITCH
RF_B5_DRX_RFIC
B38B41 DRX
RF_B41_DRX_SWITCH
RF_B38B41_DRX_RFIC
B1/4 DRX
RF_B1B4_DRX_SWITCH
RF_B1B4_DRX_RFIC
B2 DRX
RF_B2_DRX_SWITCH
RF_B2_DRX_RFIC
Band8
RF_B8_DRX_SWITCH
RF_B8_D
B40 DRX
RF_B40_DRX_SWITCH
RF_B40_DRX_RFIC
B3 DRX
RF_B3_DRX_SWITCH
RF_B3_DRX_RFIC
Band20/B28
RF_B20B28_DRX_SWITCH
RF_B20
B7 DRX
RF_B7_DRX_SWITCH
RF_B7_DRX_RFIC
B34B39 DRX
RF_B34B39_DRX_SWITCH
RF_B34B39_DRX_RFIC
34_RF_MT6177_RF_DRX
MTK Confidential

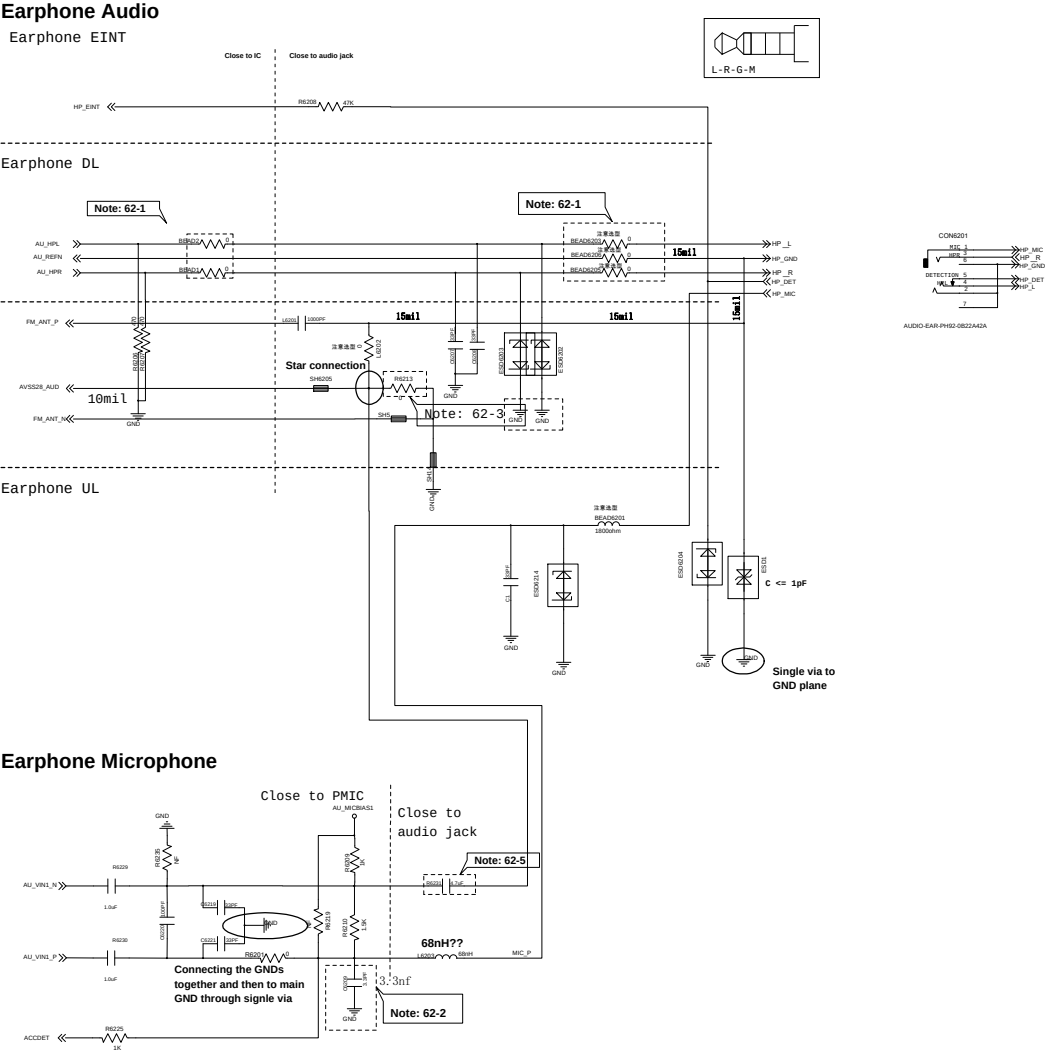
# eMMC+LPDDR3




| Schematic design notice of "44_Memory_eMMC_LPDDR3" | |
|---|---|
| Note 44-1: | Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3 |
| Note 44-2: | DRAM ZQx resistor = 240ohm (1%) that must be connected to GND |
| Note 44-3: | Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC. |
| Note 44-4: | VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.<br>For other cap for PMIC [>10uF, at PMIC page]:<br>please also refer to MMD and layout guide for placement. |


MT6631N
GPS xLNA
Close to ANT
Close to MT6631
<Critical!>
5G PCB loss is higher and
trace must kept short and
50-ohm No layer transition
PMIC R5016/R5017 NC, R5003/R5018 0ohm
TCXO R5016/R5017 0ohm, R5003/R5018 NC
MT6631
U5003
U5101
U5102
FL5101
FL5102
FL5103
RF-SAW-SAFFB1G58KA0F0A-A
GPS-LNA-RDALN16
RF-MODULE-TEST_PHI4.0
CONN_BT_DATA
CONN_BT_CLK
CONN_WF_CTRL0
CONN_WF_CTRL1
CONN_WF_CTRL2
CONN_HRST_B
CONN_TOP_DATA
CONN_TOP_CLK
CONN_WB_PTA
GPS_DIP
GPS_Q
GPS_I
PMIC_CLK_WCN
XIN_WBG
FM_ANT_N
FM_ANT_P
FM_AVDD28
VCN28_PMU
VCN18_PMU
VCN33
AVDD18_WBT
AVDD33_WBT
AVDD18_GPS
50 Ohm
CO_Pad
GPIO_GPS_LNA_EN
Title
51_CONNECTIVITY_CONSYS (A/Ddie)
Size
A1
MTK Confidential
Date: Thursday, November 02, 2017
Sheet 23 of 34

## Earphone Audio



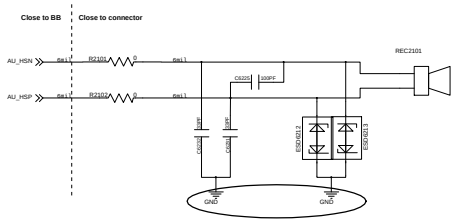




## Earphone Microphone




## Receiver




选择ACC MODE

Note: 62-4

| Platform | MT6357 | |
|---|---|---|
| Mode | ACC mode | DCC mode |
| EINT | HP_EINT | HP_EINT |
| Key-Detection | ACCDET | AU_VIN1_P |
| R6229 | 1uF | 0 ohm |
| R6230 | 1uF | 0 ohm |
| R6209 | 1K | NC |
| R6210 | 1.5K | NC |
| R6219 | NC | 2.49K |
| R6231 | 4.7uF | 0 ohm |
| R6225 | 0 ohm | NC |
| R6208 | 47K ohm | 47K ohm |

**Schematic design notice of "62_PERI_AUDIO_IO" page.**

Note 62-1: Part # of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 62-2: Reserved Cap for CS/RS test, please double check multi-key function when used

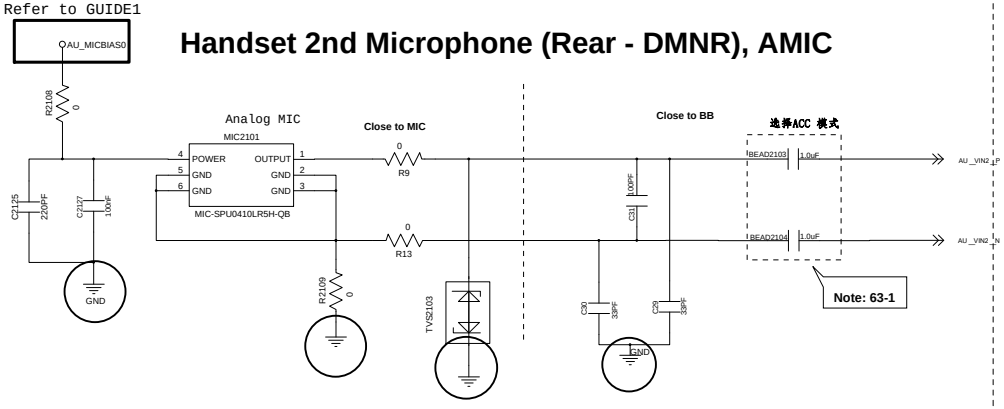
Note 62-3:

| | Earphone Jack @ Main board | Earphone Jack @ Sub board |
|---|---|---|
| R6213 | 0 ohm | 100nF |

Note 62-4: Please Select ACC Mode for Operator Project to Pass Electrical MOS Test; More Information refer to Audio/Speech Design Notice

Note 62-5: Please select R6231 with 0402 size

Refer to GUIDE1

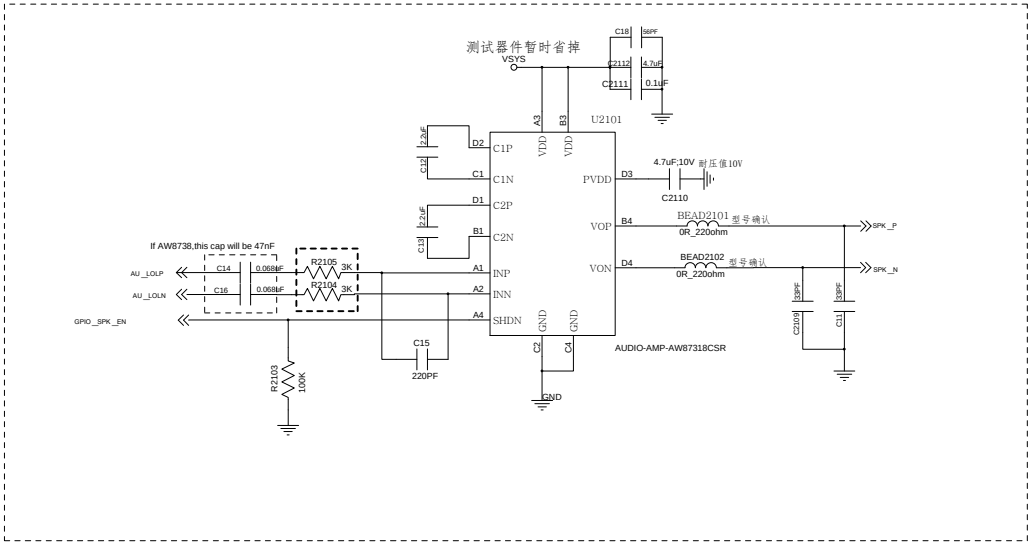



**Connecting the GNDs together and then to main GND through signle via**

**Schematic design notice of "63_PERI_AUDIO_IO" page.**

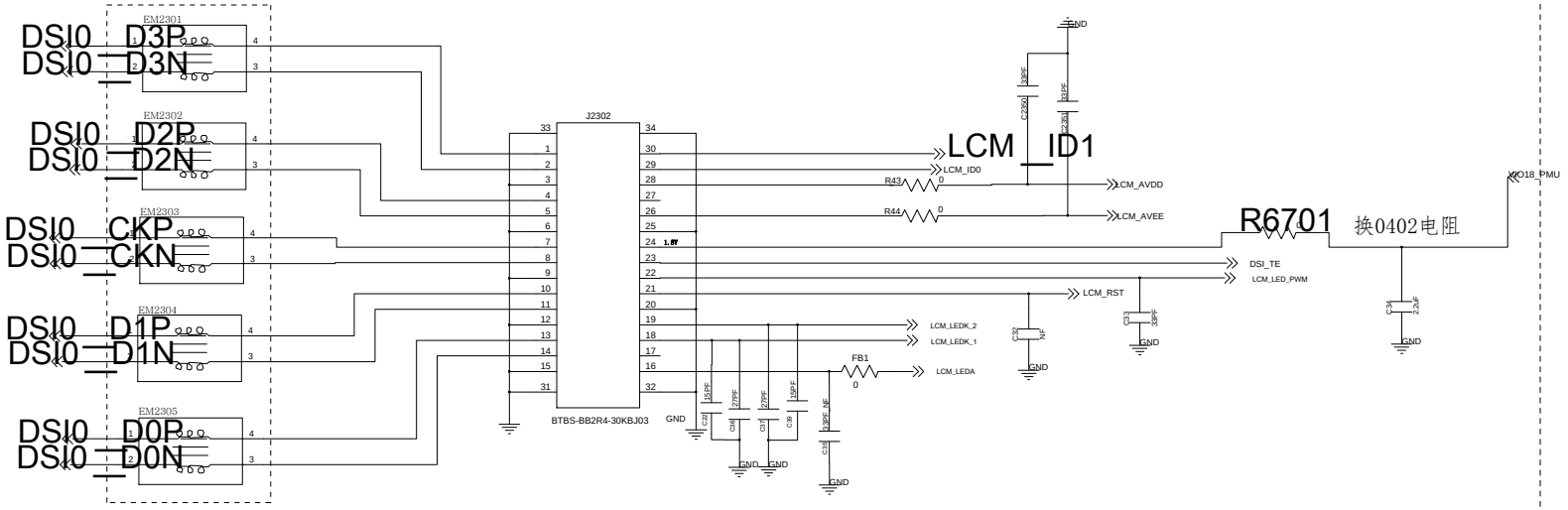
Note 63-1: 1 uF for ACC mode
0 ohm for DCC mode

| | |
|---|---|
| Title | 63_PERI_AUDIO_IO2(2 AMIC) |
| Size A1 | MTK Confidential |
| Date: Thursday, November 02, 2017 | Sheet 25 of 34 |




| | |
|---|---|
| Title | 65_PERI_SPEAKER_AMP |
| Size: A1 | MTK Confidential |
| Date: Thursday, November 02, 2017 | Sheet 26 of 34 |

LCD 接口OK




**Note: 67-1**

Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints.
Extreme care must be taken that no stubs are created by doing so.

LCM_ID

| ID0 | ID1 | vender |
|---|---|---|
| 0 | 1 | EBBG |
| 1 | 0 | 天马 |
| 0 | 0 | BOE |
| | | |

**Schematic design notice of "67_PERI_LCD_CTP" page.**

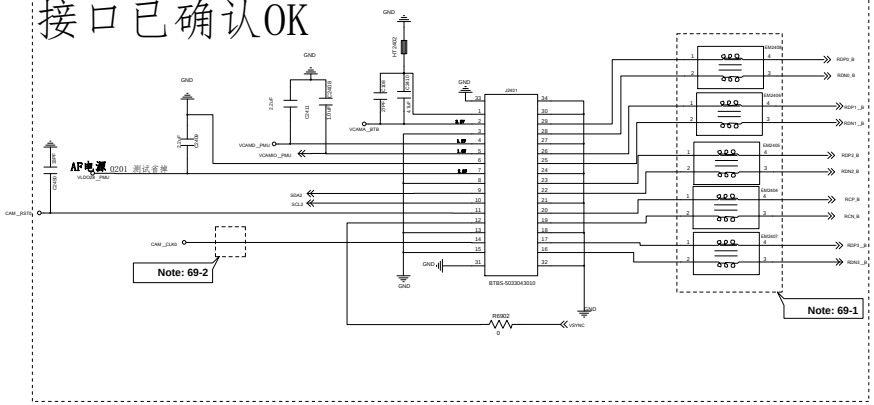
Note 67-1:
It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.

| | |
|---|---|
| Title | 67_PERI_LCD_CTP |
| Size | A1 |
| | MTK Confidential |
| Date: | Thursday, November 02, 2017 |
| Sheet | 27 of 34 |

供应商修改1 pin位置，需要按网络名核对

# Main Camera

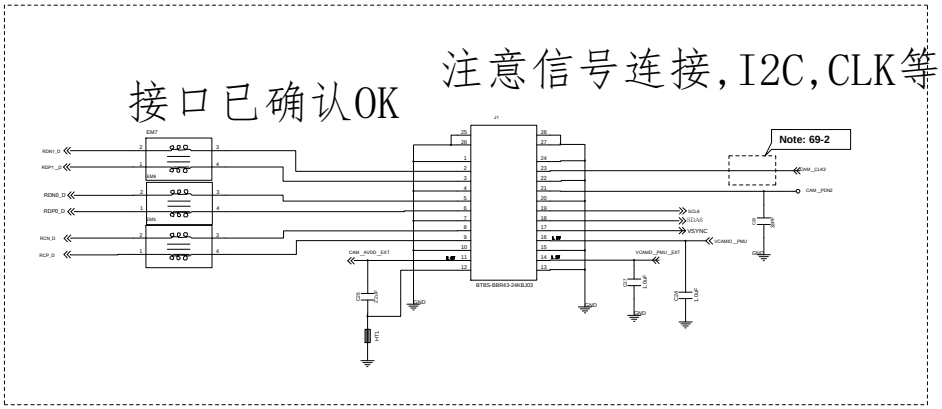
接口已确认OK




增加双摄

接口已确认OK

注意信号连接,I2C,CLK等的选用




**Schematic design notice of "69_PERI_CAMERA" page.**

Note 69-1:

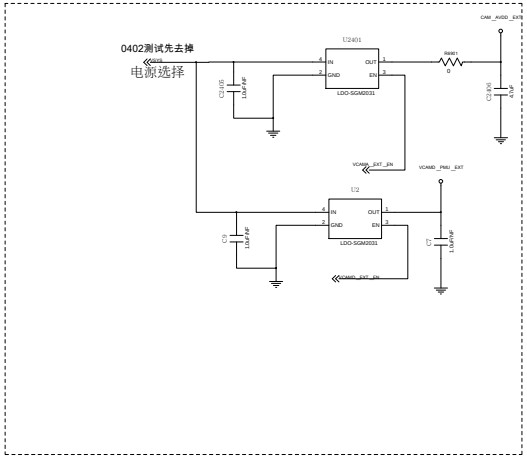
It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.

Note 69-2: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.

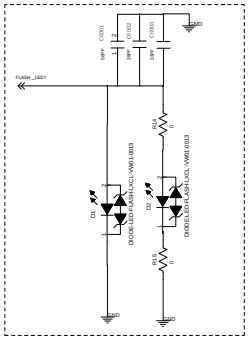
测试器件暂时省掉



AVDD，DVDD需要单独增加LDO

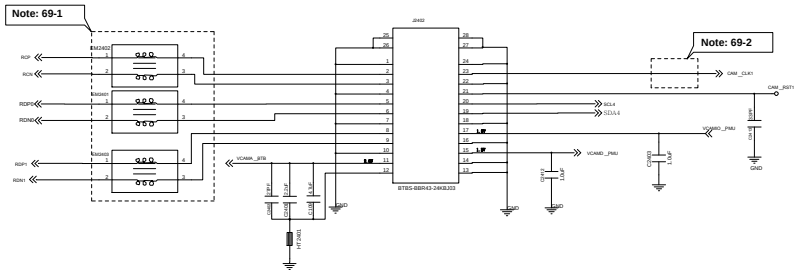



闪光灯

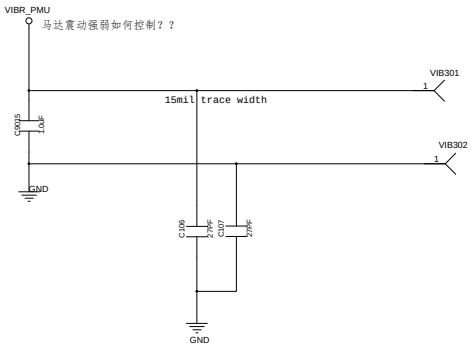


接口已确认OK

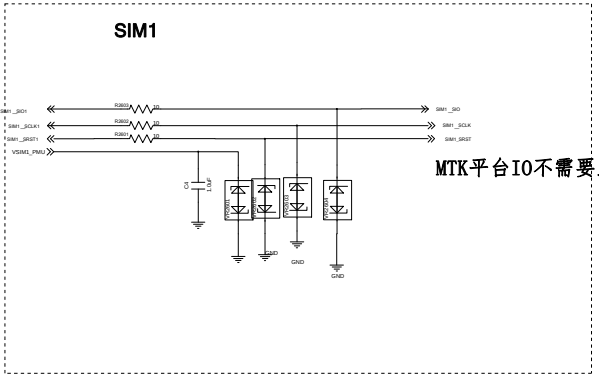
# FRONT_camera



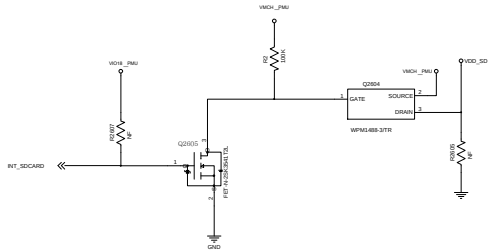
# VIBRATOR

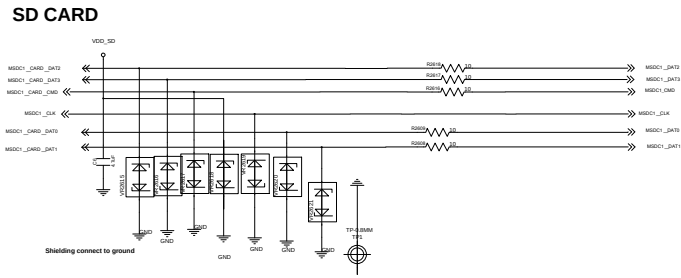


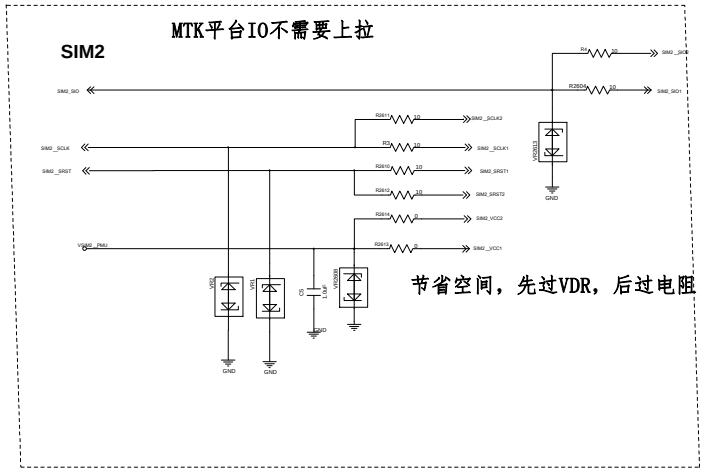

| | | |
|---|---|---|
| Title | 73_PERI_VIBRATOR | |
| Size A1 | MTK Confidential | |
| Date: Thursday, November 02, 2017 | Sheet 29 of 34 | |

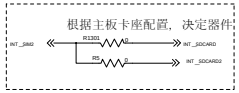



Vout=3.0V,I-lim=1A





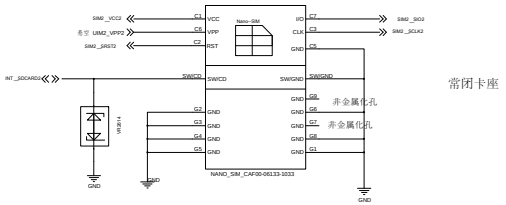



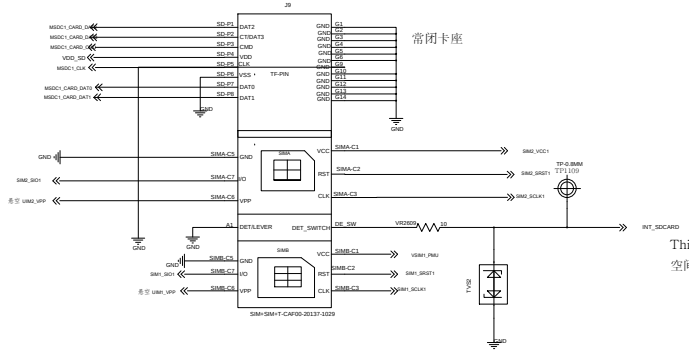




NOTE:

For internal version,ONLY use J2601:
R2603/R2610/R2613/R2604 can be 0Ω, R2611/R2612/R2614/R2615 can be NF,
R1301 can be 0Ω,Q2601 NF;R1302 NF

For India version:
R2611/R2612/R2614/R2615 can be 0Ω,R2603/R2610/R2613/R2604 can be NF.
Q2601 mount;R1301 NF ;R1302 100K



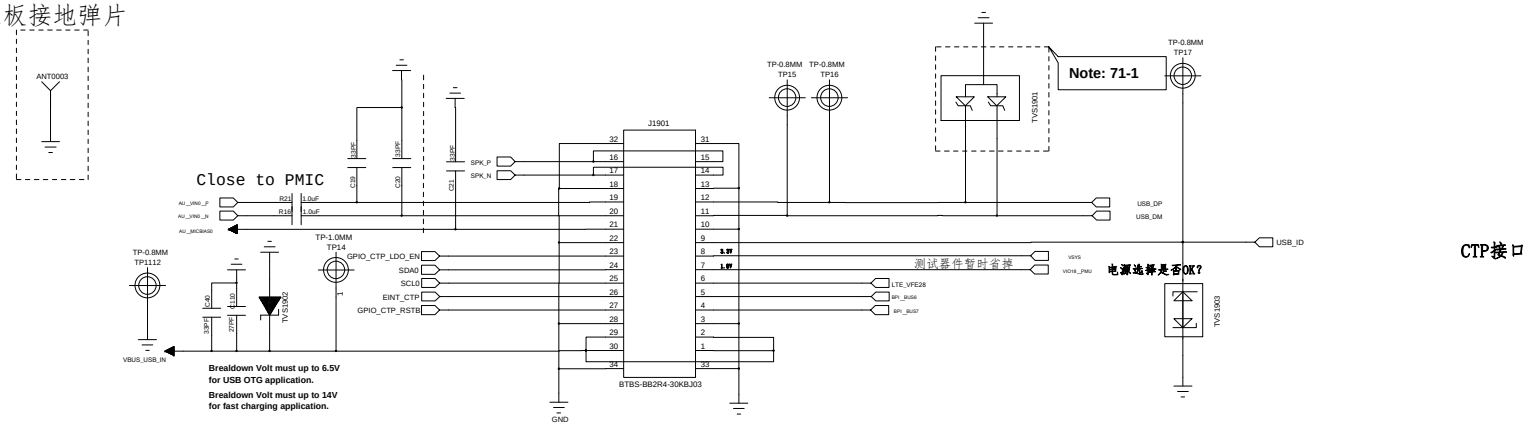




For internal version,R2603/R2610/R2613/R2604 can be 0Ω, R2611/R2612/R2614/R2615 can be NF,
For India version,R2611/R2612/R2614/R2615 can be 0Ω,R2603/R2610/R2613/R2604 can be NF.

SIM/TF card

# M-MIC+USB+RGB+SPK

主板接地弹片




CTP接口

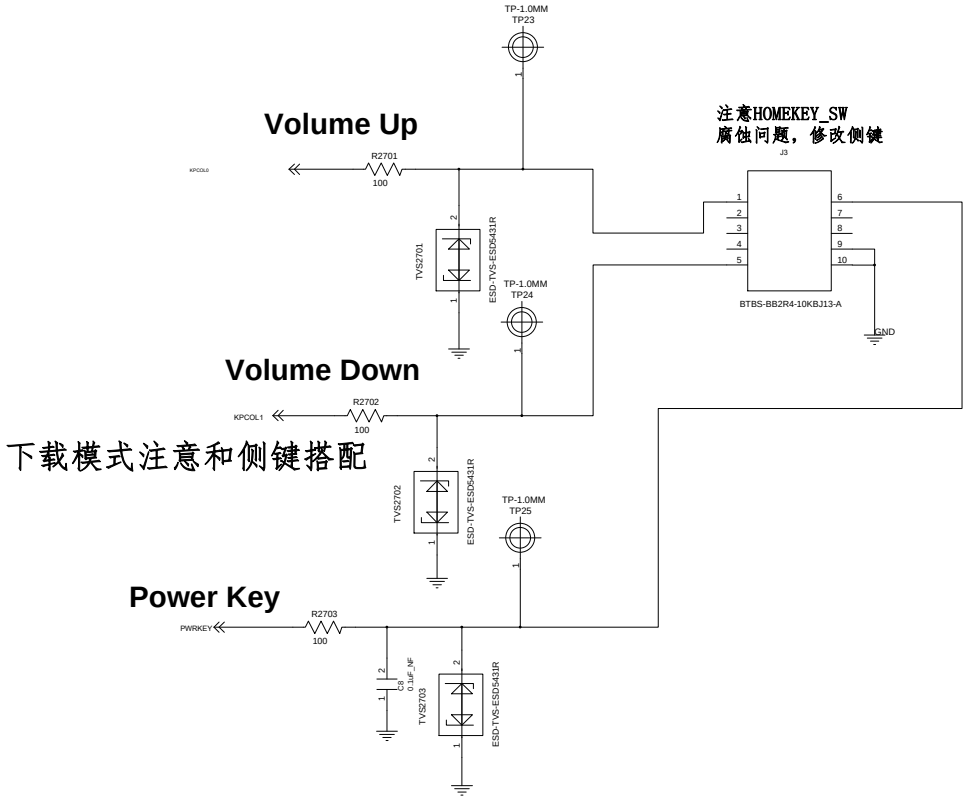
**Schematic design notice of "71_PERI_USB 2.0" page.**

Note 71-1:

For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

# Power Key / Key Pad

**DO NOT put pull-up resistor on PWRKEY**




**Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.**

Note 75-1: DO NOT put pull-up resistor on PWRKEY

Note 75-2:

Volume Up : HOME Key / GND

Volume Down : KPROW0/KPCOL0

| | |
|---|---|
| Title | 75_PERI_KEYPAD |
| Size A1 | MTK Confidential |
| Date: Thursday, November 02, 2017 | Sheet 32 of 34 |

## ALS +UV + Proximity Senso

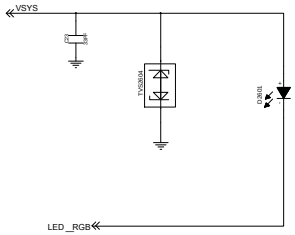
**CM36558 / ALPS + UV I2C address: 0X51 (Write:0xA2, Read:0xA3)**

**CM36558 INT default Output High, Active Low**

For LTR-578 R2330 0OHM
For STK3321 R2330 NC

ALS+PS+IR

## RGB

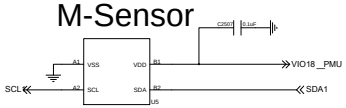



## INFARED LEDS


选择PWM接口




## M-Sensor

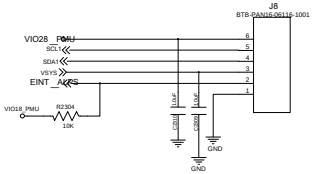



AKM: AK09918 I2C address is 0x0C

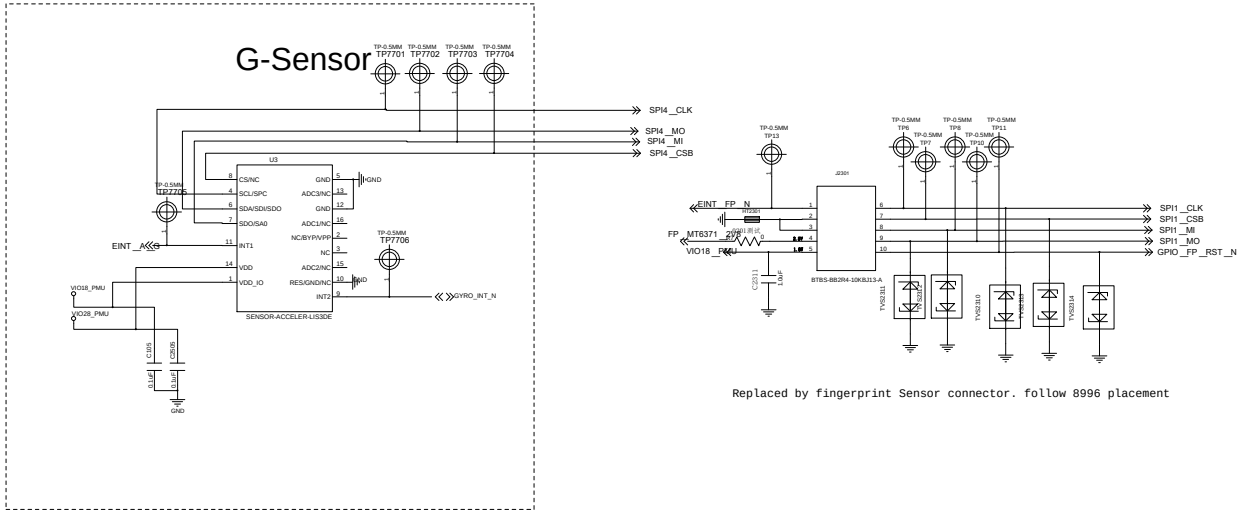
## Accerometer + Gyro Sensor

**default SPI (if sensor hub support)**

**6DSx INT1/2 default Output Low, Active high**




## G-Sensor

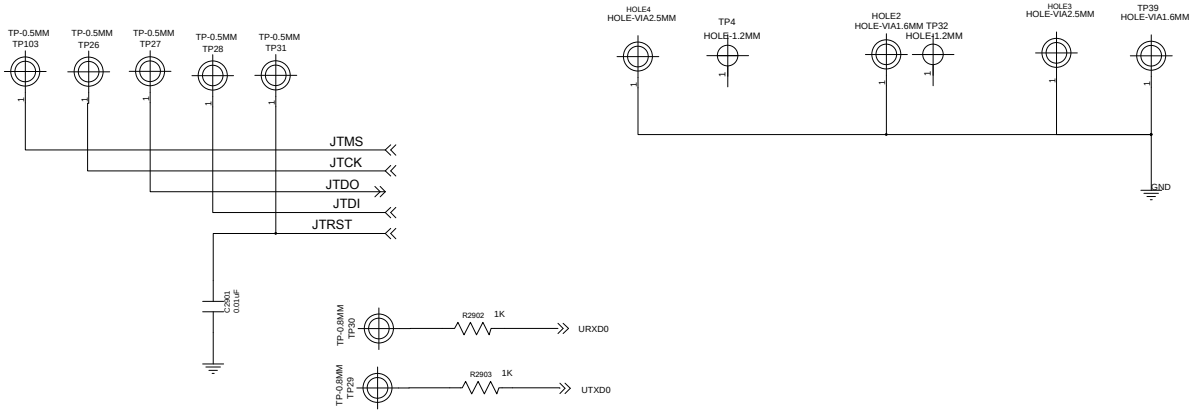



Replaced by fingerprint Sensor connector. follow 8996 placement

测试器件暂时省掉

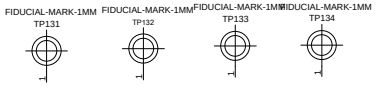
**Schematic design notice of "77_PERI_SENSORS_MEMs_ALS/PS" page.**

| | |
|---|---|
| Note 77-1: | [M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail |
| Note 77-2: | [A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide |
| Note 77-3: | [A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C** |
| Note 77-4: | [A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse. |
| Note 77-5: | [Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU) |
| Note 77-6: | DO NOT share Sensor hub i2C to other non-SCP device |




PCBA AUTOMATIC TEST point

mark 点




## Shielding Frame

| | 屏蔽盖 | 屏蔽框 |
|---|---|---|
| BB | P1 屏蔽框 1 ICO-BOX | P2 屏蔽框 1 ICO-BOX |
| RF | P3 屏蔽框 1 ICO-BOX | P4 屏蔽框 1 ICO-BOX |
| SUB-PMU | | P5 屏蔽框 1 ICO-BOX |
| WCN | | P6 屏蔽框 1 ICO-BOX |

Title: 90_DEBUG_IO
Size: A1
MTK Confidential
Date: Thursday, November 02, 2017
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