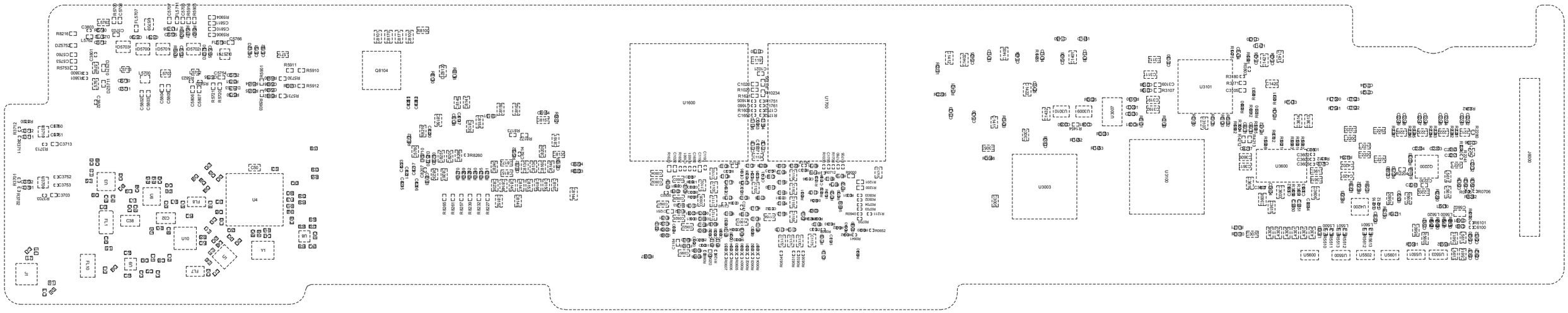
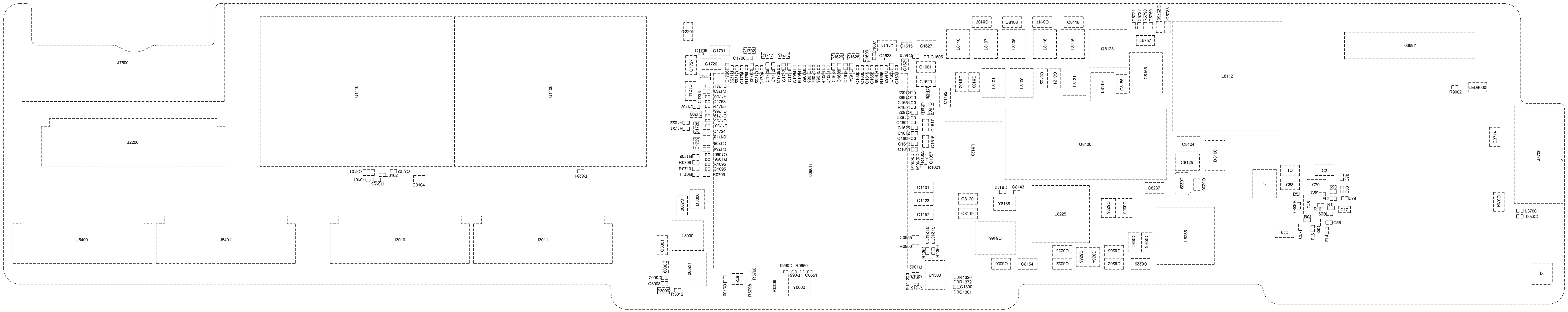
820-2996-11-BOT MLB 位置圖 0908



820-2996-11-TOP MLB 位置圖 0908



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0001231154	ENGINEERING RELEASED	2011-09-06

J2 MLB - DVT OK2FAB

LAST_MODIFIED=Tue Sep 6 17:35:11 2011

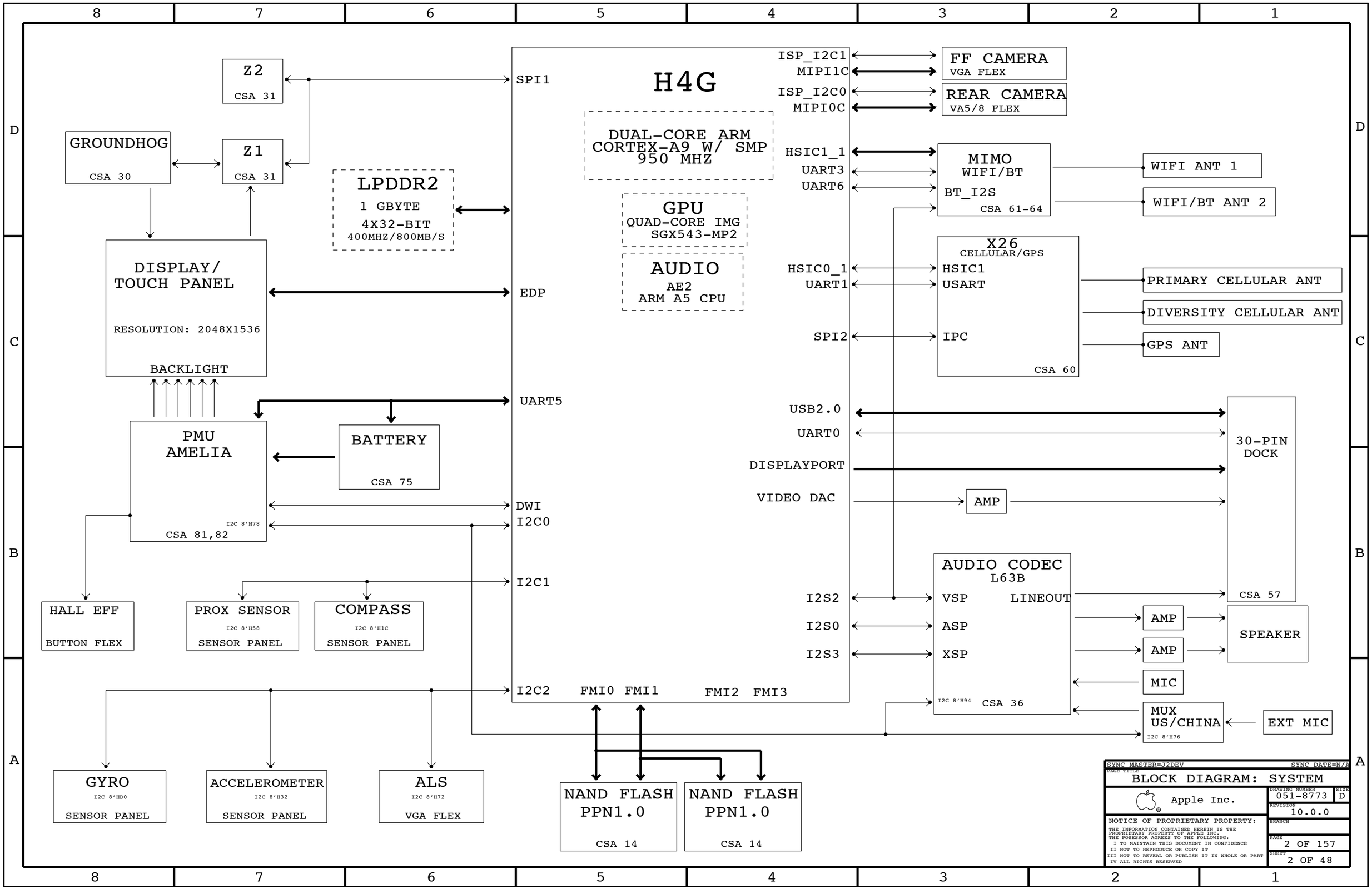
DRAWING
DRAWING
MLB
Schematic / PCB #'s

SYNC_MASTER=MIKE SYNC_DATE=NA

DRAWING TITLE
SCH,J2,MLB

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 1 OF 157
SHEET 1 OF 48



SYNC MASTER=J2DEV SYNC DATE=N/A

PAGE TITLE

BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 2 OF 157

SHEET 2 OF 48

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP

SPEAKER
INTERNAL_MIC

NAND_IO_1V8
NAND_IO=3V3

SNOTE
DEV
MLB
J2

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE
AUDIO	SPEAKER,INTERNAL_MIC

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-2352 (J1 16G)	EEEE_DNKT	CRITICAL	EEEE_J1_16G
825-7691	1	EEEE FOR 639-2058 (J1 32G)	EEEE_DM2N	CRITICAL	EEEE_J1_32G
825-7691	1	EEEE FOR 639-2059 (J1 64G)	EEEE_DM2P	CRITICAL	EEEE_J1_64G
825-7691	1	EEEE FOR 639-2353 (J2 16G)	EEEE_DNKV	CRITICAL	EEEE_J2_16G
825-7691	1	EEEE FOR 639-1572 (J2 32G)	EEEE_DHWV	CRITICAL	EEEE_J2_32G
825-7691	1	EEEE FOR 639-1871 (J2 64G)	EEEE_DKQL	CRITICAL	EEEE_J2_64G
825-7691	1	EEEE FOR 639-1870 (J2 128G)	EEEE_DKQK	CRITICAL	EEEE_J2_128G
825-7691	1	EEEE FOR 639-2844 (J2A 16G)	EEEE_DRJQ	CRITICAL	EEEE_J2A_16G
825-7691	1	EEEE FOR 639-2826 (J2A 32G)	EEEE_DRF6	CRITICAL	EEEE_J2A_32G
825-7691	1	EEEE FOR 639-2827 (J2A 64G)	EEEE_DRF5	CRITICAL	EEEE_J2A_64G

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-2105	1	FENCE,NAND,TOP,MLB,J2	PD_FENCE_NAND	CRITICAL	
806-1857	1	FENCE,LARGE,TOP,MLB,J2	PD_FENCE_LARGE	CRITICAL	
806-2349	1	FENCE,SMALLER,TOP,MLB,J2	PD_FENCE_SMALL	CRITICAL	
806-1860	1	FENCE,1,BTM,MLB,J2	PD_FENCE_BTM1	CRITICAL	
806-1865	1	FENCE,2,BTM,MLB,J2	PD_FENCE_BTM2	CRITICAL	
806-2352	1	FENCE,SMALLER,BTM,MLB,J2	PD_FENCE_BTM3	CRITICAL	

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8773	1	SCH,MLB,J2	SCH1	CRITICAL	?
820-2996	1	PCBF,MLB,J2	PCB1	CRITICAL	?
085-3058	1	DEV BOM,MLB,J2	DEV1		?

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0533	1	IC,SOC,H4G,FCBGA1225	U0600	CRITICAL	?

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0561	1	IC,PMU,AMELIA,D1974AB	U8100	CRITICAL	?

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0579	2	SDRAM,LPDDR2,512MB,SAMSUNG 46NM	U1600,U1700	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0580	333S0579		U1600,U1700	LPDDR2,HYNIX 44NM
333S0581	333S0579		U1600,U1700	LPDDR2,ELPIDA 45NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0781	1	HYNIX 26NM PPN1.0 16GB	U1400	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0804	335S0781	16GB_PROD	U1400	TOSHIBA 24NM PPN1.0

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0781	2	HYNIX 26NM PPN1.0 16GB	U1400,U1410	CRITICAL	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0804	335S0781	32GB_PROD	U1400,U1410	TOSHIBA 24NM PPN1.0

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0782	2	HYNIX 26NM PPN1.0 32GB	U1400,U1410	CRITICAL	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0805	335S0782	64GB_PROD	U1400,U1410	TOSHIBA 24NM PPN1.0

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0814	2	HYNIX 26NM PPN1.0 64GB	U1400,U1410	CRITICAL	128GB_PROD

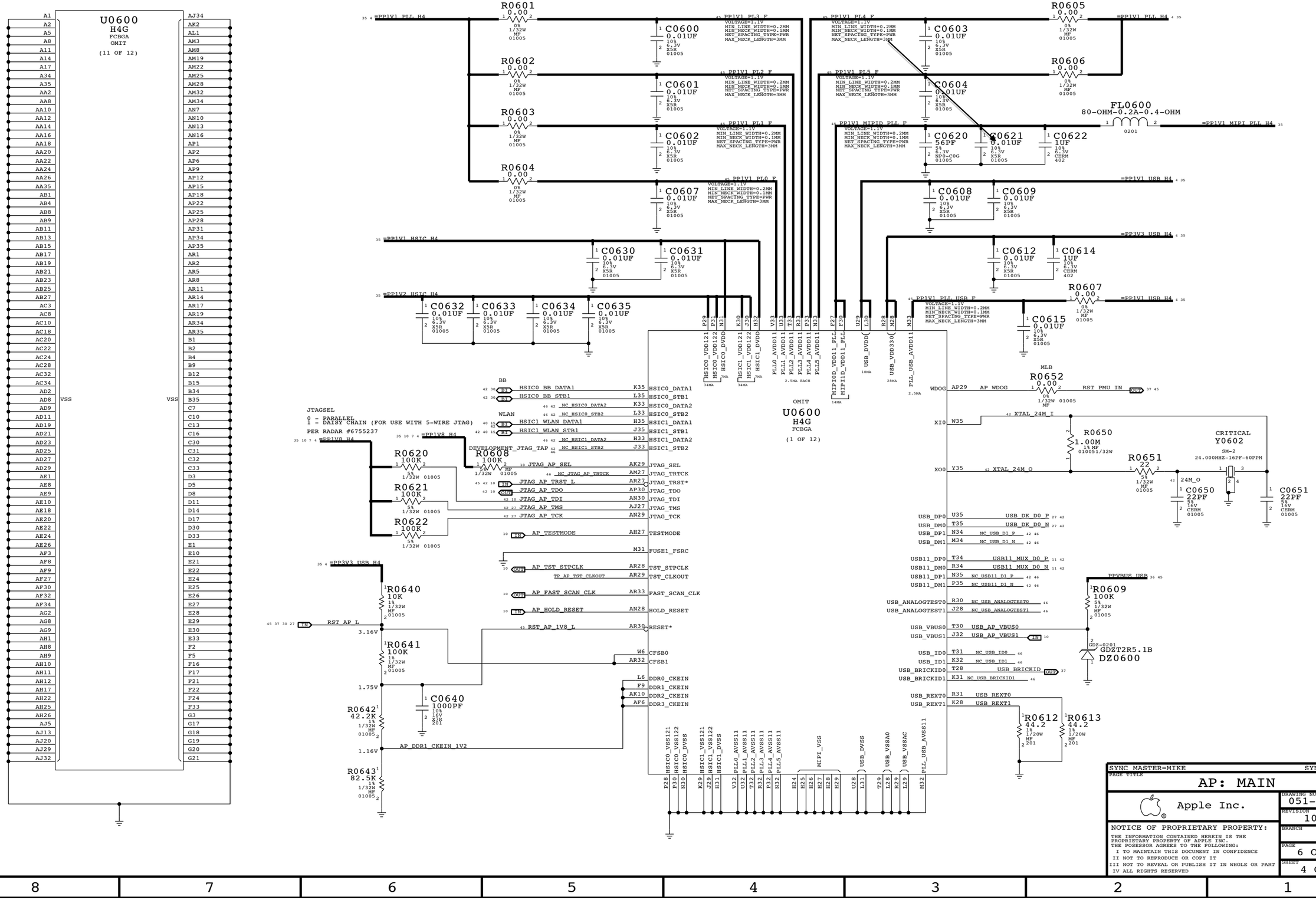
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0806	335S0814	128GB_PROD	U1400,U1410	TOSHIBA 24NM PPN1.0

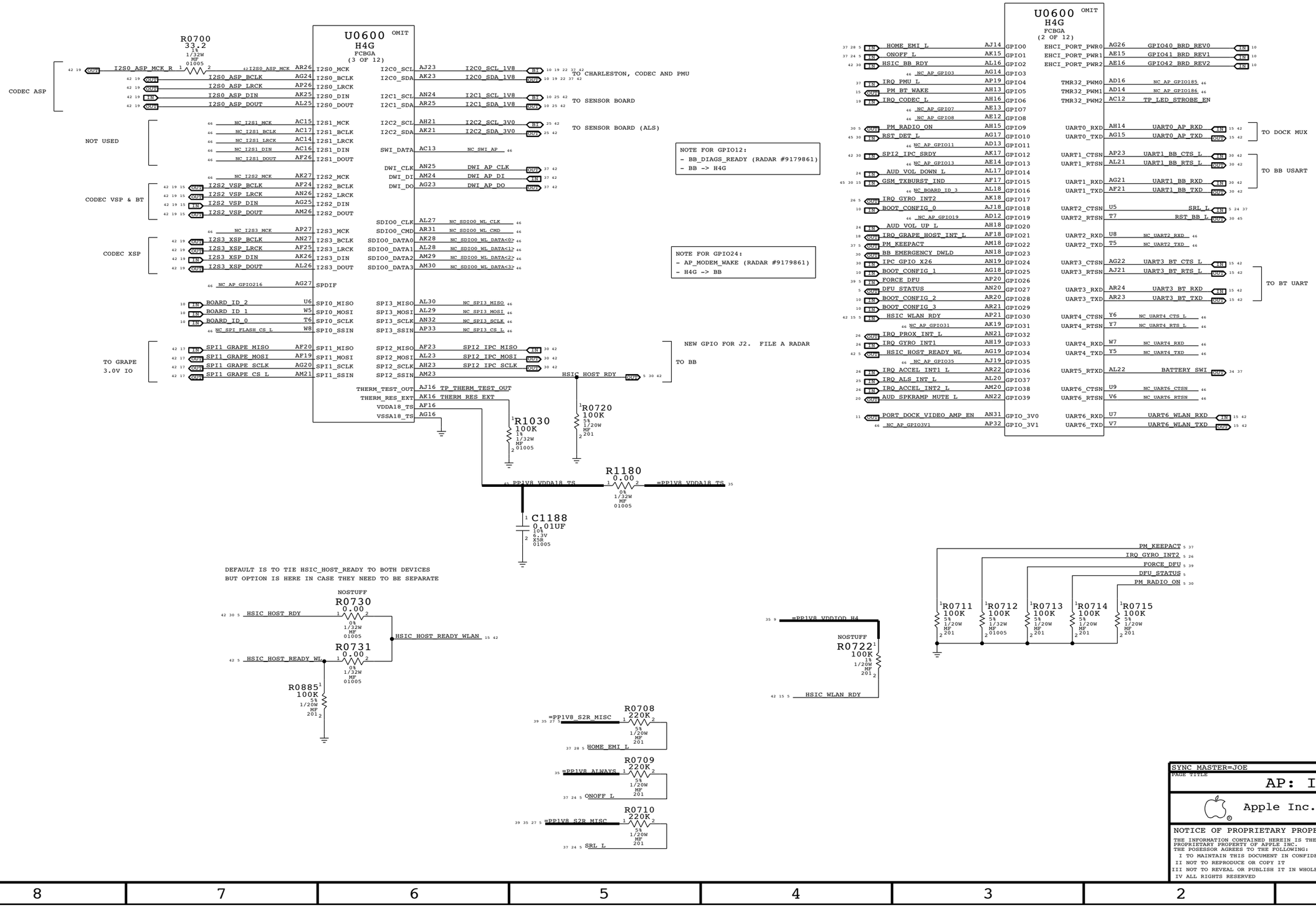
SYNC_MASTER=MIKE SYNC_DATE=N/A

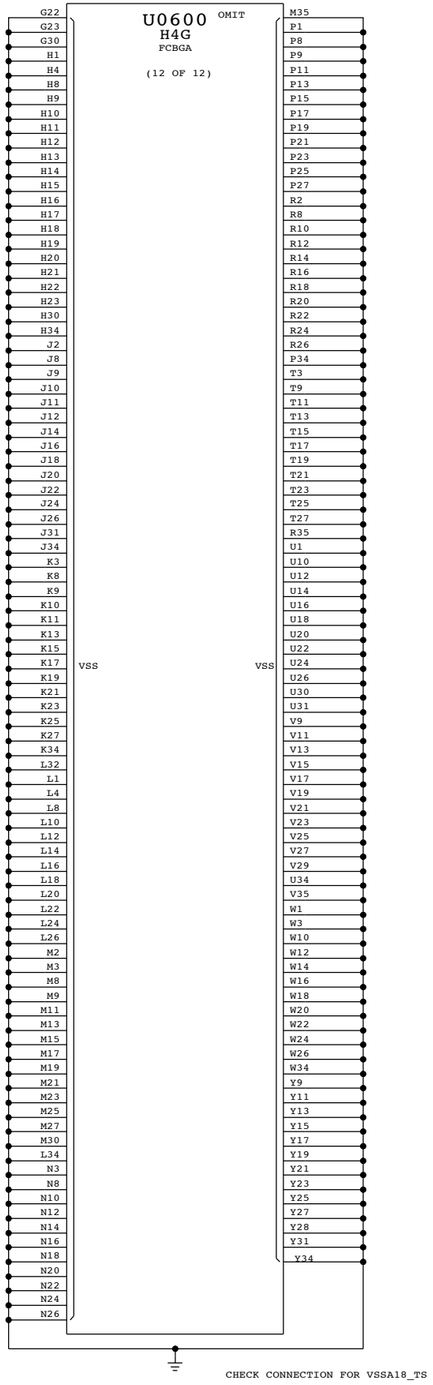
PAGE TITLE
BOM TABLES

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 4 OF 157
SHEET 3 OF 48


U0600
H4G
FCBGA
OMIT
(11 OF 12)
VSS
VSS
JTAGSEL
0 - PARALLEL
1 - DAISY CHAIN (FOR USE WITH 5-WIRE JTAG)
PER RADAR #6755237
DEVELOPMENT_JTAG_TAP
BB
WLAN
R0601 0.00
R0602 0.00
R0603 0.00
R0604 0.00
R0605 0.00
R0606 0.00
R0607 0.00
R0608 100K
R0620 100K
R0621 100K
R0622 100K
R0640 10K
R0641 100K
R0642 42.2K
R0643 82.5K
C0600 0.01UF
C0601 0.01UF
C0602 0.01UF
C0603 0.01UF
C0604 0.01UF
C0607 0.01UF
C0608 0.01UF
C0609 0.01UF
C0612 0.01UF
C0614 1UF
C0615 0.01UF
C0620 56PF
C0621 0.01UF
C0622 1UF
C0630 0.01UF
C0631 0.01UF
C0632 0.01UF
C0633 0.01UF
C0634 0.01UF
C0635 0.01UF
C0640 1000PF
FL0600 80-OHM-0.2A-0.4-OHM
R0650 1.00M
R0651 22
C0650 22PF
C0651 22PF
CRITICAL
Y0602
SM-2
24.000MHZ-16PF-60PPM
R0652 0.00
MLB
R0609 100K
DZ0600 GDZT2R5.1B
R0612 44.2
R0613 44.2
HSIC0_BB_DATA1
HSIC0_BB_STB1
NC_HSIC0_DATA2
NC_HSIC0_STB2
HSIC1_WLAN_DATA1
HSIC1_WLAN_STB1
NC_HSIC1_DATA2
NC_HSIC1_STB2
JTAG_AP_SEL
NC_JTAG_AP_TRTCK
JTAG_AP_TRST_L
JTAG_AP_TDO
JTAG_AP_TDI
JTAG_AP_TMS
JTAG_AP_TCK
AP_TESTMODE
AP_TST_STPCLK
TP_AP_TST_CLKOUT
AP_FAST_SCAN_CLK
AP_HOLD_RESET
RST_AP_L
RST_AP_1V8_L
AP_DDR1_CKEIN_1V2
WDOG
AP_WDOG
RST_PMU_IN
XTAL_24M_I
XTAL_24M_O
USB_DK_D0_P
USB_DK_D0_N
NC_USB_D1_P
NC_USB_D1_N
USB11_MUX_D0_P
USB11_MUX_D0_N
NC_USB11_D1_P
NC_USB11_D1_N
NC_USB_ANALOGTEST0
NC_USB_ANALOGTEST1
USB_AP_VBUS0
USB_AP_VBUS1
NC_USB_ID0
NC_USB_ID1
USB_BRICKID
NC_USB_BRICKID1
USB_REXT0
USB_REXT1
PPVBUS_USB
HSIC0_DATA1
HSIC0_STB1
HSIC0_DATA2
HSIC0_STB2
HSIC1_DATA1
HSIC1_STB1
HSIC1_DATA2
HSIC1_STB2
JTAG_SEL
JTAG_TRTCK
JTAG_TRST*
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
TESTMODE
FUSE1_FSRC
TST_STPCLK
TST_CLKOUT
FAST_SCAN_CLK
HOLD_RESET
RESET*
CFSB0
CFSB1
DDR0_CKEIN
DDR1_CKEIN
DDR2_CKEIN
DDR3_CKEIN
SYNC_MASTER=MIKE
SYNC DATE=N/A
PAGE TITLE
AP: MAIN
Apple Inc.
DRAWING NUMBER 051-8773
SIZE D
REVISION 10.0.0
BRANCH
PAGE 6 OF 157
SHEET 4 OF 48
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U0600 OMIT
H4G
FCBGA
(3 OF 12)
R0700 33.2 1% 1/32W MF 01005
I2S0_ASP_MCK_R
CODEC ASP
I2S0_ASP_BCLK
I2S0_ASP_LRCK
I2S0_ASP_DIN
I2S0_ASP_DOUT
NOT USED
NC_I2S1_MCK
NC_I2S1_BCLK
NC_I2S1_LRCK
NC_I2S1_DIN
NC_I2S1_DOUT
CODEC VSP & BT
I2S2_VSP_BCLK
I2S2_VSP_LRCK
I2S2_VSP_DIN
I2S2_VSP_DOUT
CODEC XSP
NC_I2S3_MCK
I2S3_XSP_BCLK
I2S3_XSP_LRCK
I2S3_XSP_DIN
I2S3_XSP_DOUT
NC_AP_GPIO216
BOARD_ID_2
BOARD_ID_1
BOARD_ID_0
NC_SPI_FLASH_CS_L
TO GRAPE 3.0V IO
SPI1_GRAPE_MISO
SPI1_GRAPE_MOSI
SPI1_GRAPE_SCLK
SPI1_GRAPE_CS_L
I2S0_MCK
I2S0_BCLK
I2S0_LRCK
I2S0_DIN
I2S0_DOUT
I2S1_MCK
I2S1_BCLK
I2S1_LRCK
I2S1_DIN
I2S1_DOUT
I2S2_MCK
I2S2_BCLK
I2S2_LRCK
I2S2_DIN
I2S2_DOUT
I2S3_MCK
I2S3_BCLK
I2S3_LRCK
I2S3_DIN
I2S3_DOUT
SPDIF
SPI0_MISO
SPI0_MOSI
SPI0_SCLK
SPI0_SSIN
SPI1_MISO
SPI1_MOSI
SPI1_SCLK
SPI1_SSIN
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
SWI_DATA
DWI_CLK
DWI_DI
DWI_DO
SDIO0_CLK
SDIO0_CMD
SDIO0_DATA0
SDIO0_DATA1
SDIO0_DATA2
SDIO0_DATA3
SPI3_MISO
SPI3_MOSI
SPI3_SCLK
SPI3_SSIN
SPI2_MISO
SPI2_MOSI
SPI2_SCLK
SPI2_SSIN
THERM_TEST_OUT
THERM_RES_EXT
VDDA18_TS
VSSA18_TS
I2C0_SCL_1V8
I2C0_SDA_1V8
I2C1_SCL_1V8
I2C1_SDA_1V8
I2C2_SCL_3V0
I2C2_SDA_3V0
NC_SWI_AP
DWI_AP_CLK
DWI_AP_DI
DWI_AP_DO
NC_SDIO0_WL_CLK
NC_SDIO0_WL_CMD
NC_SDIO0_WL_DATA<0>
NC_SDIO0_WL_DATA<1>
NC_SDIO0_WL_DATA<2>
NC_SDIO0_WL_DATA<3>
NC_SPI3_MISO
NC_SPI3_MOSI
NC_SPI3_SCLK
NC_SPI3_CS_L
SPI2_IPC_MISO
SPI2_IPC_MOSI
SPI2_IPC_SCLK
HSIC_HOST_RDY
TP_THERM_TEST_OUT
THERM_RES_EXT
TO CHARLESTON, CODEC AND PMU
TO SENSOR BOARD
TO SENSOR BOARD (ALS)
NOTE FOR GPIO12:
- BB_DIAGS_READY (RADAR #9179861)
- BB -> H4G
NOTE FOR GPIO24:
- AP_MODEM_WAKE (RADAR #9179861)
- H4G -> BB
NEW GPIO FOR J2. FILE A RADAR
TO BB
R0720 100K 5% 1/20W MF 201
R1030 100K 1% 1/32W MF 01005
R1180 0.00 0% 1/32W MF 01005
C1188 0.01UF 10% 6.3V X5R 01005
=PP1V8_VDDA18_TS
DEFAULT IS TO TIE HSIC_HOST_READY TO BOTH DEVICES
BUT OPTION IS HERE IN CASE THEY NEED TO BE SEPARATE
NOSTUFF
R0730 0.00 0% 1/32W MF 01005
R0731 0.00 0% 1/32W MF 01005
R0885 100K 5% 1/20W MF 201
HSIC_HOST_RDY
HSIC_HOST_READY_WL
HSIC_HOST_READY_WLAN
R0708 220K 5% 1/20W MF 201
R0709 220K 5% 1/20W MF 201
R0710 220K 5% 1/20W MF 201
=PP1V8_S2R_MISC
=PP1V8_ALWAYS
HOME_EMI_L
ONOFF_L
SRL_L
U0600 OMIT
H4G
FCBGA
(2 OF 12)
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO29
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
GPIO_3V0
GPIO_3V1
HOME_EMI_L
ONOFF_L
HSIC_BB_RDY
NC_AP_GPIO3
IRQ_PMU_L
PM_BT_WAKE
IRQ_CODEC_L
NC_AP_GPIO7
NC_AP_GPIO8
PM_RADIO_ON
RST_DET_L
NC_AP_GPIO11
SPI2_IPC_SRDY
NC_AP_GPIO13
AUD_VOL_DOWN_L
GSM_TXBURST_IND
NC_BOARD_ID_3
IRQ_GYRO_INT2
BOOT_CONFIG_0
NC_AP_GPIO19
AUD_VOL_UP_L
IRQ_GRAPE_HOST_INT_L
PM_KEEPACT
BB_EMERGENCY_DWLD
IPC_GPIO_X26
BOOT_CONFIG_1
FORCE_DFU
DFU_STATUS
BOOT_CONFIG_2
BOOT_CONFIG_3
HSIC_WLAN_RDY
NC_AP_GPIO31
IRQ_PROX_INT_L
IRQ_GYRO_INT1
HSIC_HOST_READY_WL
NC_AP_GPIO35
IRQ_ACCEL_INT1_L
IRQ_ALS_INT_L
IRQ_ACCEL_INT2_L
AUD_SPKRAMP_MUTE_L
PORT_DOCK_VIDEO_AMP_EN
NC_AP_GPIO3V1
EHCI_PORT_PWR0
EHCI_PORT_PWR1
EHCI_PORT_PWR2
TMR32_PWM0
TMR32_PWM1
TMR32_PWM2
UART0_RXD
UART0_TXD
UART1_CTSN
UART1_RTSN
UART1_RXD
UART1_TXD
UART2_CTSN
UART2_RTSN
UART2_RXD
UART2_TXD
UART3_CTSN
UART3_RTSN
UART3_RXD
UART3_TXD
UART4_CTSN
UART4_RTSN
UART4_RXD
UART4_TXD
UART5_RTXD
UART6_CTSN
UART6_RTSN
UART6_RXD
UART6_TXD
GPIO40_BRD_REV0
GPIO41_BRD_REV1
GPIO42_BRD_REV2
NC_AP_GPIO185
NC_AP_GPIO186
TP_LED_STROBE_EN
UART0_AP_RXD
UART0_AP_TXD
UART1_BB_CTS_L
UART1_BB_RTS_L
UART1_BB_RXD
UART1_BB_TXD
RST_BB_L
NC_UART2_RXD
NC_UART2_TXD
UART3_BT_CTS_L
UART3_BT_RTS_L
UART3_BT_RXD
UART3_BT_TXD
NC_UART4_CTS_L
NC_UART4_RTS_L
NC_UART4_RXD
NC_UART4_TXD
BATTERY_SWI
NC_UART6_CTSN
NC_UART6_RTSN
UART6_WLAN_RXD
UART6_WLAN_TXD
TO DOCK MUX
TO BB USART
TO BT UART
PM_KEEPACT
IRQ_GYRO_INT2
FORCE_DFU
DFU_STATUS
PM_RADIO_ON
R0711 100K 5% 1/20W MF 201
R0712 100K 5% 1/32W MF 01005
R0713 100K 5% 1/20W MF 201
R0714 100K 5% 1/20W MF 201
R0715 100K 5% 1/20W MF 201
=PP1V8_VDDIOD_H4
NOSTUFF
R0722 100K 1% 1/20W MF 201
HSIC_WLAN_RDY
SYNC_MASTER=JOE
SYNC_DATE=N/A
PAGE TITLE
AP: I/Os
Apple Inc.
DRAWING NUMBER 051-8773
SIZE D
REVISION 10.0.0
BRANCH
PAGE 7 OF 157
SHEET 5 OF 48
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



CHECK CONNECTION FOR VSSA18_TS

45 9 6 PPIO_NAND_H4

R0832 100K 5% 1/32W MF 01005
R0836 100K 5% 1/32W MF 01005
R0831 100K 5% 1/32W MF 01005
R0834 100K 5% 1/32W MF 01005

44 12 6 FMI1_CE0_L
44 12 6 FMI1_CE1_L
44 12 6 FMI0_CE0_L
44 12 6 FMI0_CE1_L

45 9 6 PPIO_NAND_H4

NOSTUFF R0800 100K 5% 1/32W MF 01005
NOSTUFF R0801 100K 5% 1/32W MF 01005
NOSTUFF R0802 100K 5% 1/32W MF 01005
NOSTUFF R0803 100K 5% 1/32W MF 01005

44 12 6 FMI0_WE_L
44 12 6 FMI0_RE_N
44 12 6 FMI1_WE_L
44 12 6 FMI1_RE_N

44 12 6 FMI0_ALE
44 12 6 FMI0_CLE
44 12 6 FMI1_ALE
44 12 6 FMI1_CLE

NOSTUFF R0810 100K 5% 1/32W MF 01005
NOSTUFF R0811 100K 5% 1/32W MF 01005
NOSTUFF R0812 100K 5% 1/32W MF 01005
NOSTUFF R0813 100K 5% 1/32W MF 01005

35 28 =PP3V0_IO_MISC

R0804 100K 5% 1/32W MF 01005

FMI2-3_CEN IS 3.0V

U0600 OMIT
H4G
FCBGA
(4 OF 12)

44 12 6	OUTPUT	FMI0_CE0_L	AH31	FMI0_CEN0	FMI2_CEN0	AE35	SPK_ID
44 12 6	OUTPUT	FMI0_CE1_L	AF31	FMI0_CEN1	FMI2_CEN1	AB28	NC_FMI2_CE1_L 46
46		NC_FMI0_CE2_L	AD28	FMI0_CEN2	FMI2_CEN2	AA28	NC_FMI2_CE2_L 46
46		NC_FMI0_CE3_L	AG29	FMI0_CEN3	FMI2_CEN3	AB30	NC_FMI2_CE3_L 46
46		NC_FMI0_CE4_L	Y29	FMI0_CEN4	FMI2_CEN4	AE28	PM_LCDVDD_PWREN OUTPUT 16
46		NC_FMI0_CE5_L	AH28	FMI0_CEN5	FMI2_CEN5	AF28	NC_FMI2_CE5_L 46
46		NC_FMI0_CE6_L	AG28	FMI0_CEN6	FMI2_CEN6	AA29	RST_GRAPE_L OUTPUT 17 45
46		NC_FMI0_CE7_L	AM31	FMI0_CEN7	FMI2_CEN7	AB31	GRAPE_FW_DNLD_EN_L OUTPUT 17
44 12	BIDIR	FMI0_AD<0>	AG35	FMI0_IO0	FMI2_IO0	AC31	NC_FMI2_AD<0> 46
44 12	BIDIR	FMI0_AD<1>	AF35	FMI0_IO1	FMI2_IO1	AB33	NC_FMI2_AD<1> 46
44 12	BIDIR	FMI0_AD<2>	AH35	FMI0_IO2	FMI2_IO2	AC35	NC_FMI2_AD<2> 46
44 12	BIDIR	FMI0_AD<3>	AH33	FMI0_IO3	FMI2_IO3	AE34	NC_FMI2_AD<3> 46
44 12	BIDIR	FMI0_AD<4>	AG31	FMI0_IO4	FMI2_IO4	AD34	NC_FMI2_AD<4> 46
44 12	BIDIR	FMI0_AD<5>	AG32	FMI0_IO5	FMI2_IO5	AD32	NC_FMI2_AD<5> 46
44 12	BIDIR	FMI0_AD<6>	AG34	FMI0_IO6	FMI2_IO6	AD35	NC_FMI2_AD<6> 46
44 12	BIDIR	FMI0_AD<7>	AH32	FMI0_IO7	FMI2_IO7	AD31	NC_FMI2_AD<7> 46
44 12 6	OUTPUT	FMI0_ALE	AE32	FMI0_ALE	FMI2_ALE	AB34	NC_FMI2_ALE 46
44 12 6	OUTPUT	FMI0_CLE	AF33	FMI0_CLE	FMI2_CLE	AB32	NC_FMI2_CLE 46
44 12 6	OUTPUT	FMI0_WE_L	AH34	FMI0_WEN	FMI2_WEN	AB35	NC_FMI2_WE_L 46
44 12 6	OUTPUT	FMI0_RE_N	AE33	FMI0_REN	FMI2_REN	AD33	NC_FMI2_RE_L 46
44 12	OUTPUT	FMI0_DQS_P	AG33	FMI0_DQS	FMI2_DQS	AC33	NC_FMI2_DQS 46
44 12 6	OUTPUT	FMI1_CE0_L	AJ33	FMI1_CEN0	FMI3_CEN0	W31	NC_FMI3_CE0_L 46
44 12 6	OUTPUT	FMI1_CE1_L	AN33	FMI1_CEN1	FMI3_CEN1	W28	NC_FMI3_CE1_L 46
46		NC_FMI1_CE2_L	AD30	FMI1_CEN2	FMI3_CEN2	W29	NC_FMI3_CE2_L 46
46		NC_FMI1_CE3_L	AE30	FMI1_CEN3	FMI3_CEN3	V30	NC_FMI3_CE3_L 46
46		NC_FMI1_CE4_L	AJ31	FMI1_CEN4	FMI3_CEN4	AG30	NC_FMI3_CE4_L 46
46		NC_FMI1_CE5_L	AJ30	FMI1_CEN5	FMI3_CEN5	AC30	NC_FMI3_CE5_L 46
46		NC_FMI1_CE6_L	AL31	FMI1_CEN6	FMI3_CEN6	AH30	NC_FMI3_CE6_L 46
46		NC_FMI1_CE7_L	AK31	FMI1_CEN7	FMI3_CEN7	AE31	NC_FMI3_CE7_L 46
44 12	BIDIR	FMI1_AD<0>	AL32	FMI1_IO0	FMI3_IO0	AA34	NC_FMI3_AD<0> 46
44 12	BIDIR	FMI1_AD<1>	AN35	FMI1_IO1	FMI3_IO1	W33	NC_FMI3_AD<1> 46
44 12	BIDIR	FMI1_AD<2>	AK32	FMI1_IO2	FMI3_IO2	AA33	NC_FMI3_AD<2> 46
44 12	BIDIR	FMI1_AD<3>	AK33	FMI1_IO3	FMI3_IO3	V34	NC_FMI3_AD<3> 46
44 12	BIDIR	FMI1_AD<4>	AL33	FMI1_IO4	FMI3_IO4	AA30	NC_FMI3_AD<4> 46
44 12	BIDIR	FMI1_AD<5>	AK34	FMI1_IO5	FMI3_IO5	V31	NC_FMI3_AD<5> 46
44 12	BIDIR	FMI1_AD<6>	AM33	FMI1_IO6	FMI3_IO6	W32	NC_FMI3_AD<6> 46
44 12	BIDIR	FMI1_AD<7>	AJ35	FMI1_IO7	FMI3_IO7	Y30	NC_FMI3_AD<7> 46
44 12 6	OUTPUT	FMI1_ALE	AN34	FMI1_ALE	FMI3_ALE	Y33	NC_FMI3_ALE 46
44 12 6	OUTPUT	FMI1_CLE	AK35	FMI1_CLE	FMI3_CLE	W30	NC_FMI3_CLE 46
44 12 6	OUTPUT	FMI1_WE_L	AM35	FMI1_WEN	FMI3_WEN	AA32	NC_FMI3_WE_L 46
44 12 6	OUTPUT	FMI1_RE_N	AL35	FMI1_REN	FMI3_REN	AA31	NC_FMI3_RE_L 46
44 12	OUTPUT	FMI1_DQS_P	AL34	FMI1_DQS	FMI3_DQS	Y32	NC_FMI3_DQS 46

NEW GPIO FOR J2. FILE A RADAR

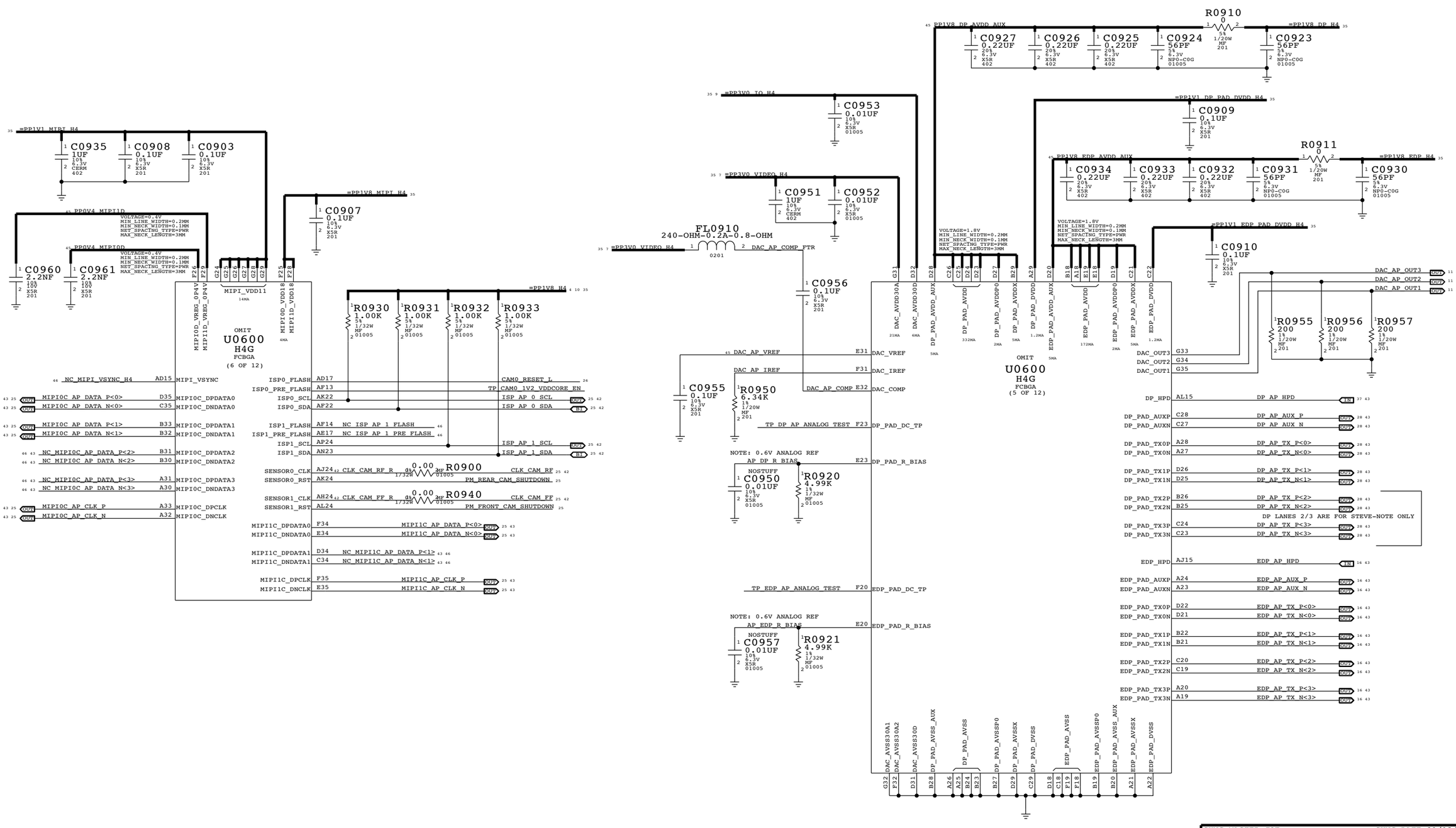
CHECK WITH GRAPE ON VOLTAGE FOR THESE TWO SIGNALS

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
AP: NAND

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 8 OF 157
SHEET 6 OF 48



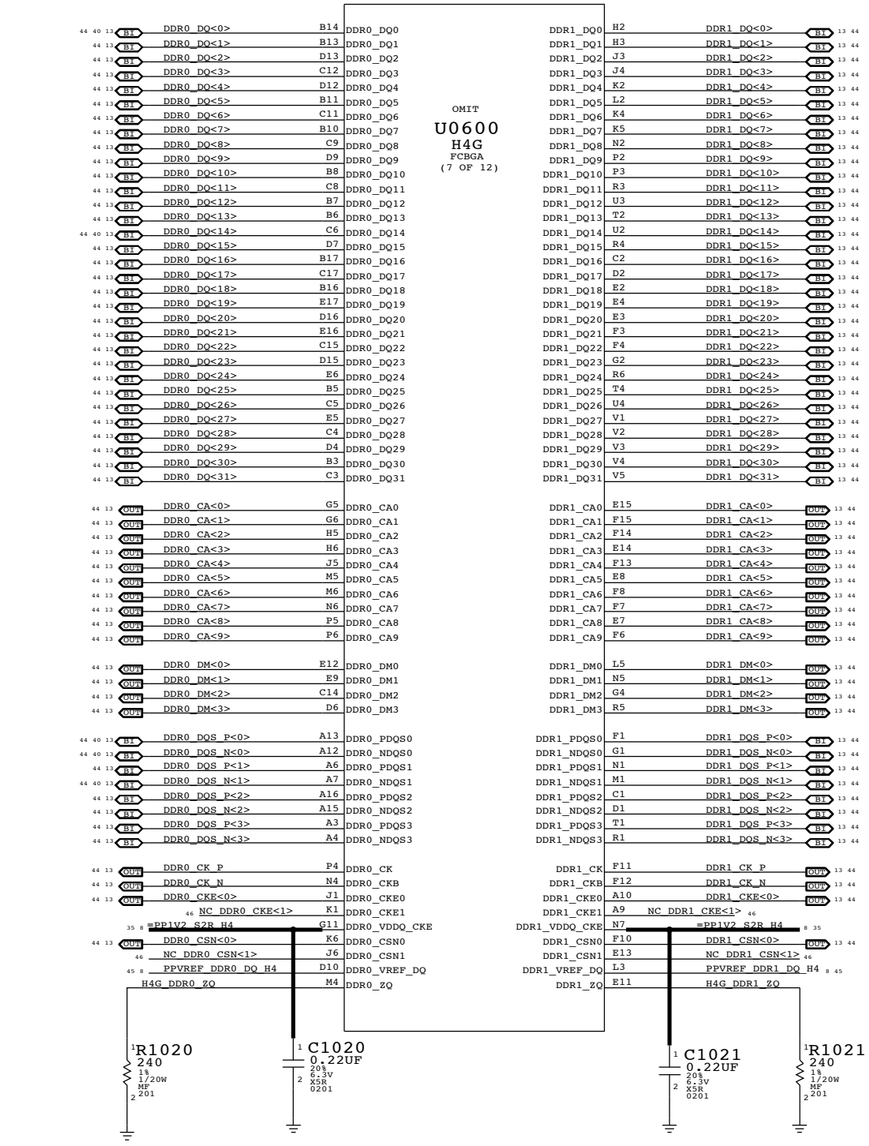
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S0279	132S0154		C0960,C0961	RADAR:9624625

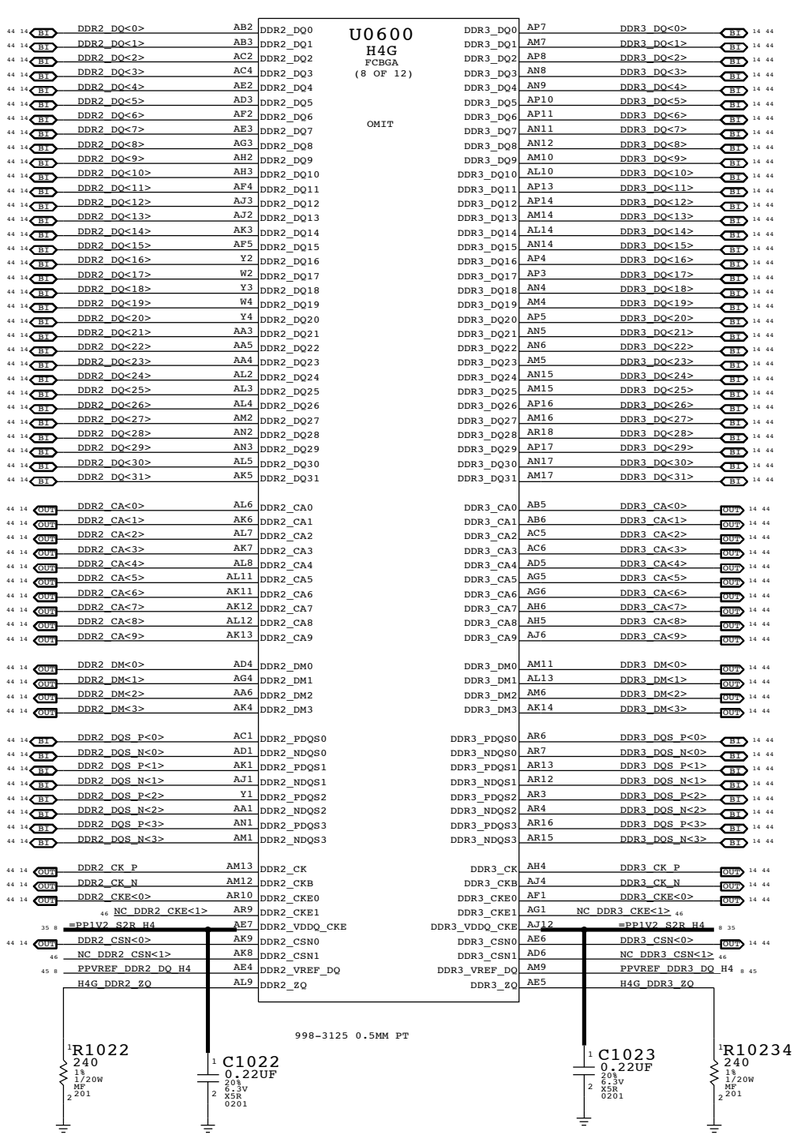
SYNC_MASTER=JOE SYNC_DATE=01/13/2011

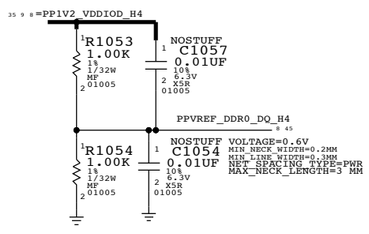
PAGE TITLE
AP: TV,DP,MIPI

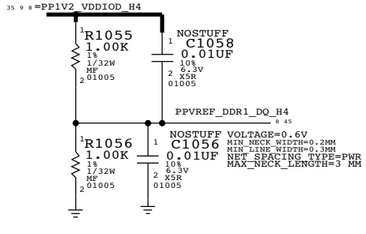
Apple Inc.

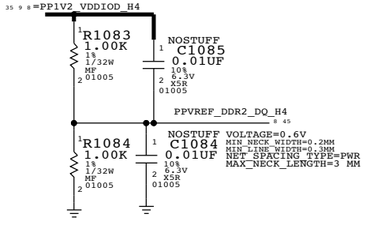
DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 9 OF 157
SHEET 7 OF 48

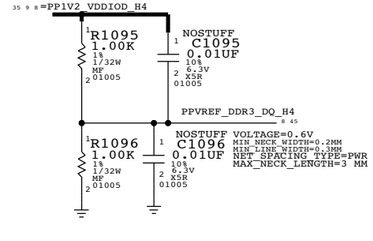












SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

AP: DDR

Apple Inc.

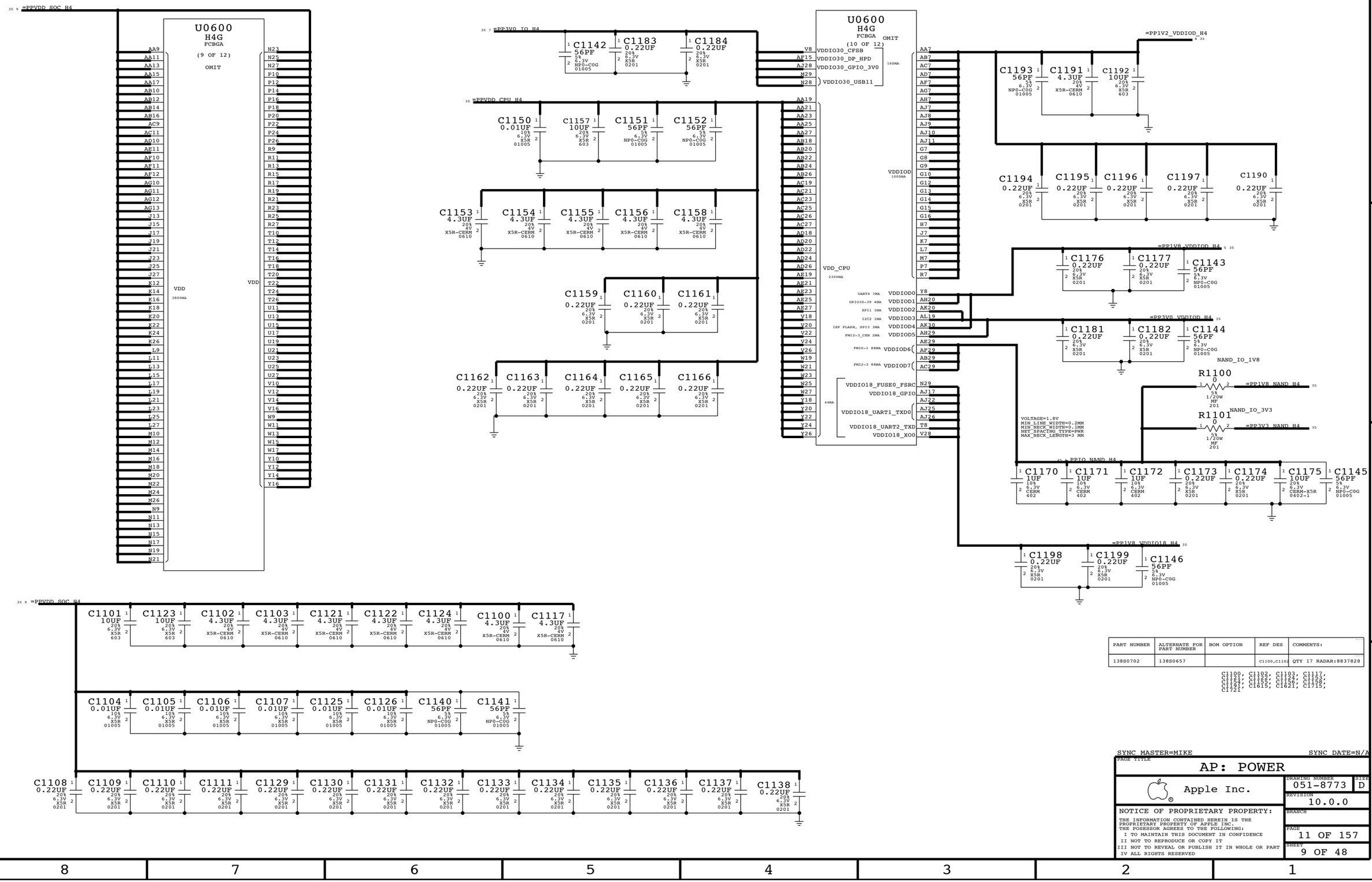
DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

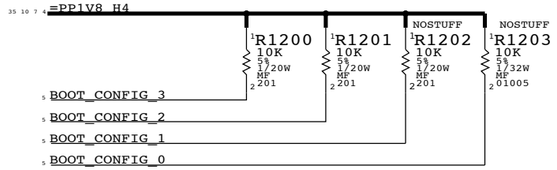
PAGE 10 OF 157

SHEET 8 OF 48



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		C1100,C1102	QTY 17 RADAR:8837828

BOOT CONFIG ID

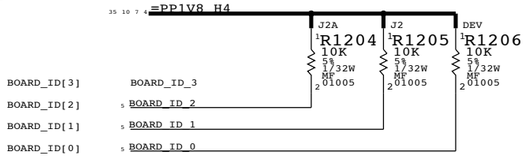


BOOT_CONFIG[3-0]	
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

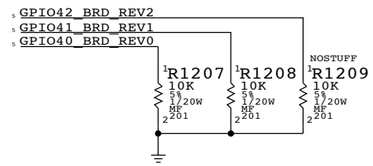


BOARD_ID[3-0]	
0000	J1 AP
0001	J1 DEV
0010	J2 AP
0011	J2 DEV
0100	J2A AP
0101	J2A DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 0
001	PROTO 1 LOCAL
010	PROTO 1 CHINA
011	PROTO 2
100	EVT

S/W READ FLOW

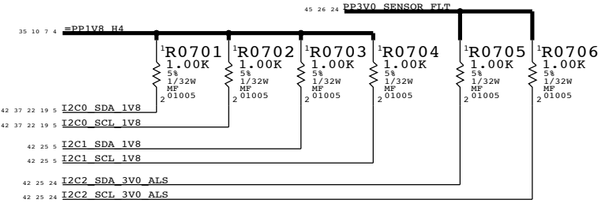
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

FOR REFERENCE

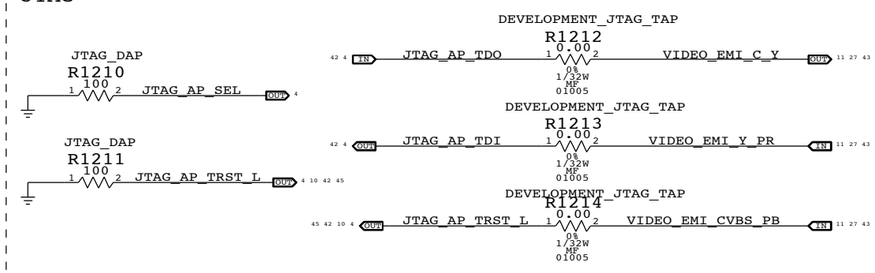
BOOT_CONFIG[3:0]

	0000	SPI0
	0001	SPI1
	0010	SPI0 W/TEST
	0011	SPI1 W/TEST
	0100	FMI0 2CS
	0101	FMI0 4CS
	0110	FMI0 4CS W/TEST
	0111	RESERVED
	1000	FMI1 2 CS
	1001	FMI1 4 CS
	1010	FMI1 4CS W/TEST
CURRENT SETTING ->	1100	FMI0/1 2/2 CS
	1101	FMI0/1 4/4 CS
	1110	FMI0/1 4/4 CS W/TEST
	1111	RESERVED

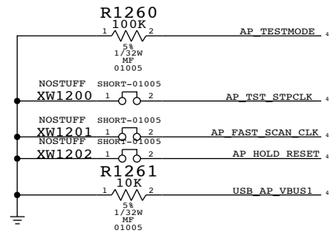
I2C PULL-UPS



JTAG



2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	



SYNC_MASTER=ALEX SYNC_DATE=N/A

PAGE TITLE

AP: MISC & ALIASES

Apple Inc.

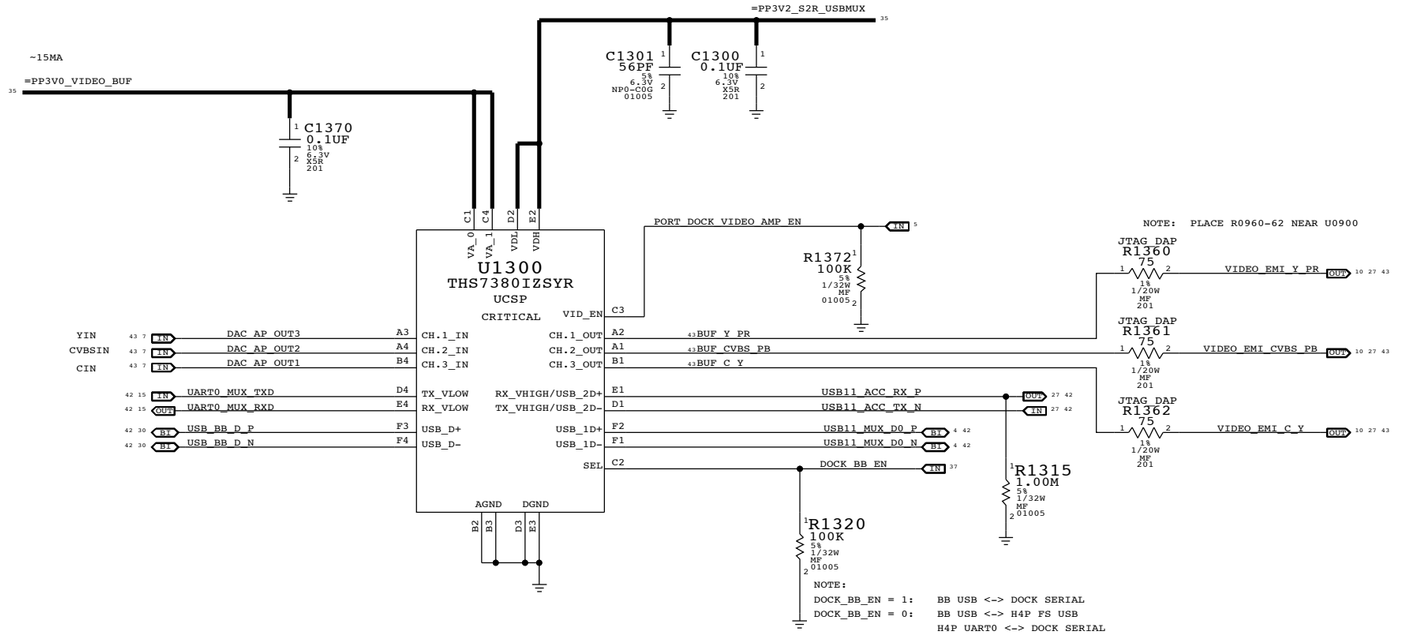
DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 12 OF 157

SHEET 10 OF 48



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0539	343S0520		U1300	RADAR:9009078

SYNC MASTER=CHOPIN SYNC DATE=12/10/2010

PAGE TITLE

AP: VIDEO BUFFER,BB USB MUXES

Apple Inc.

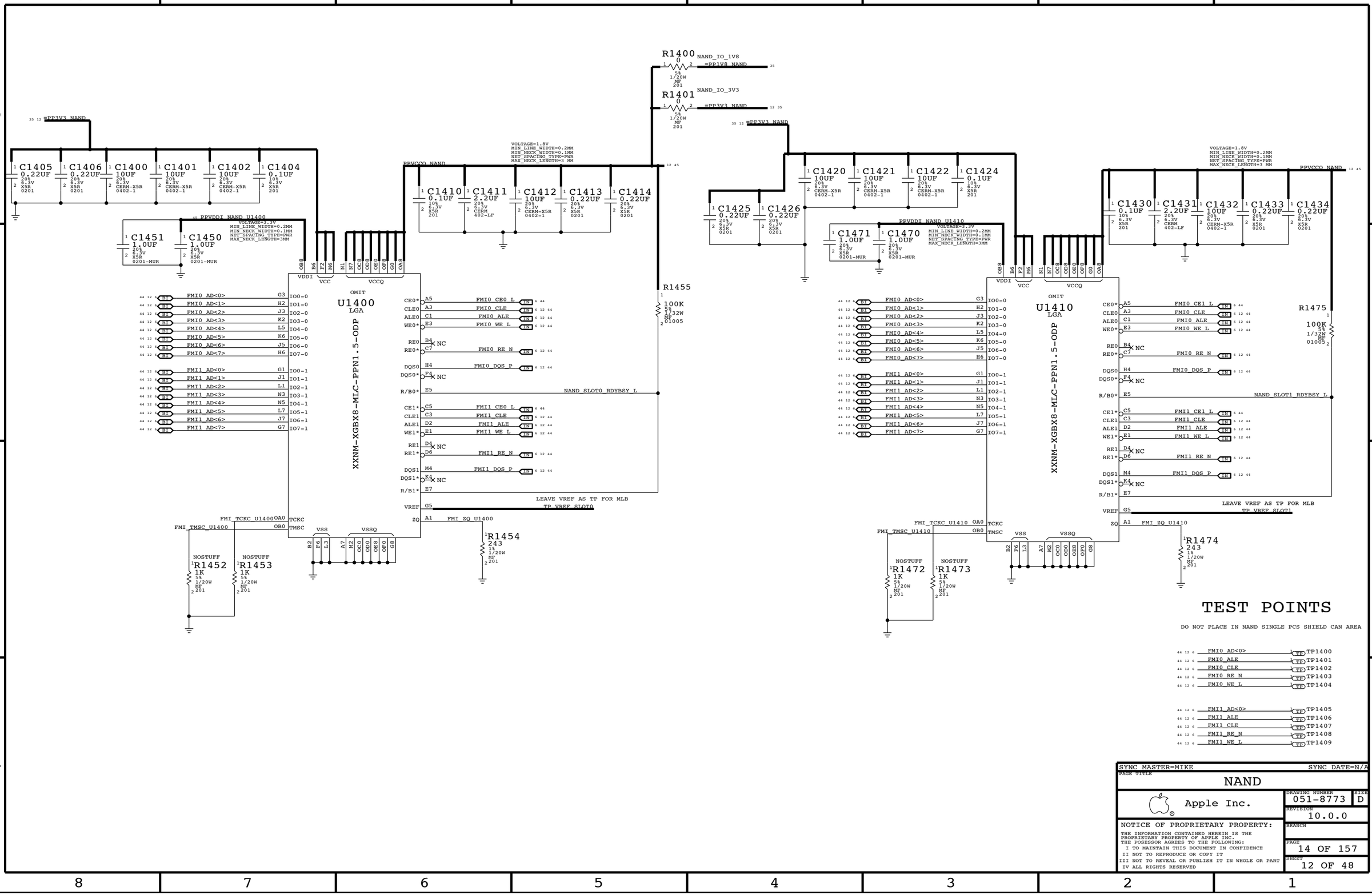
DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 13 OF 157

SHEET 11 OF 48



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

NAND

Apple Inc.

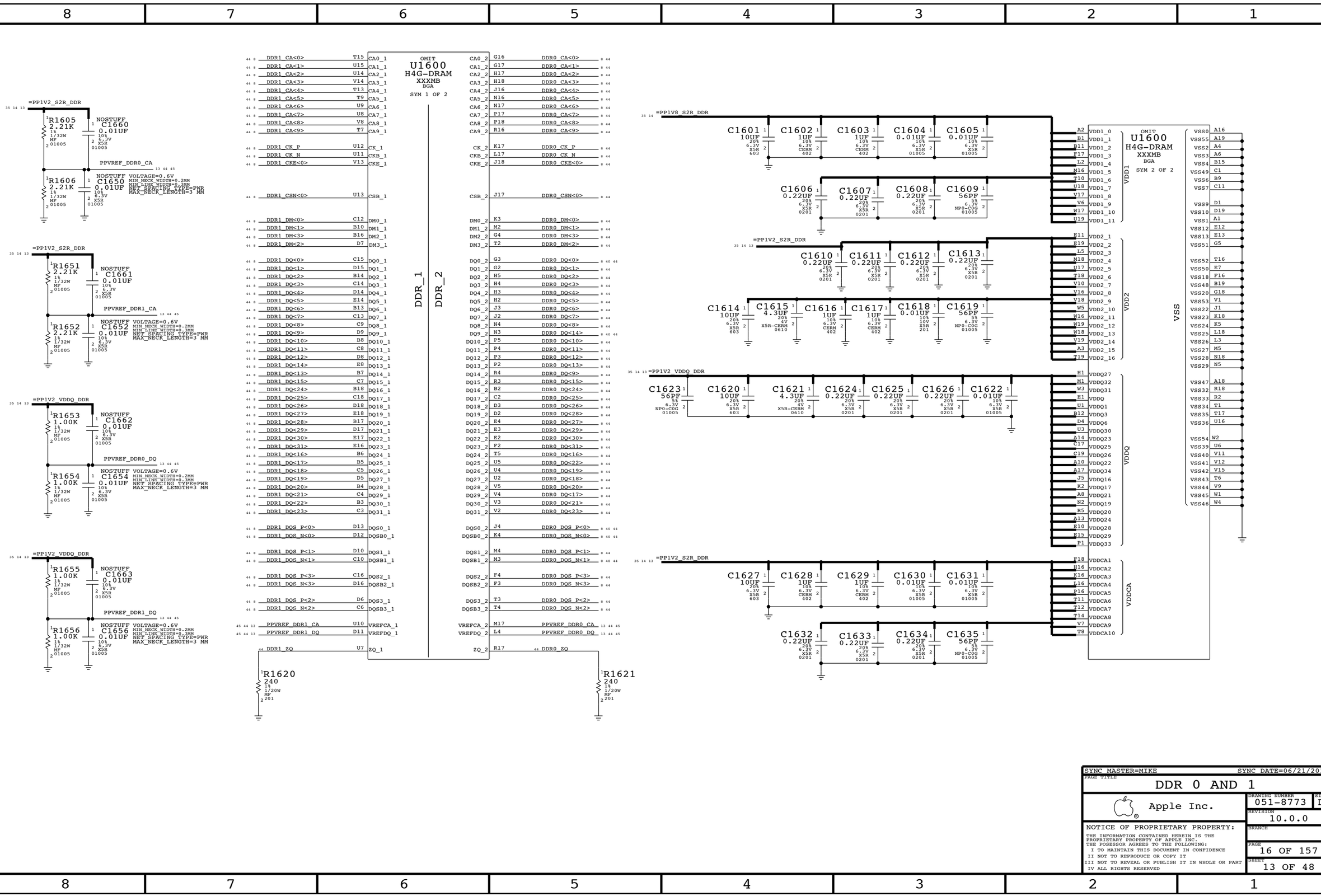
DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 14 OF 157

SHEET 12 OF 48


=PP1V2_S2R_DDR
R1605 2.21K 1% 1/32W MF 01005
C1660 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR0_CA
R1606 2.21K 1% 1/32W MF 01005
C1650 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
=PP1V2_S2R_DDR
R1651 2.21K 1% 1/32W MF 01005
C1661 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR1_CA
R1652 2.21K 1% 1/32W MF 01005
C1652 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_DDR
R1653 1.00K 1% 1/32W MF 01005
C1662 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR0_DQ
R1654 1.00K 1% 1/32W MF 01005
C1654 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_DDR
R1655 1.00K 1% 1/32W MF 01005
C1663 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR1_DQ
R1656 1.00K 1% 1/32W MF 01005
C1656 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
OMIT
U1600
H4G-DRAM
XXXMB
BGA
SYM 1 OF 2
DDR_1
DDR_2
DDR1_CA<0> T15 CA0_1
DDR1_CA<1> U15 CA1_1
DDR1_CA<2> U14 CA2_1
DDR1_CA<3> V14 CA3_1
DDR1_CA<4> T13 CA4_1
DDR1_CA<5> T9 CA5_1
DDR1_CA<6> U9 CA6_1
DDR1_CA<7> U8 CA7_1
DDR1_CA<8> V8 CA8_1
DDR1_CA<9> T7 CA9_1
DDR1_CK_P U12 CK_1
DDR1_CK_N U11 CKB_1
DDR1_CKE<0> V13 CKE_1
DDR1_CSN<0> U13 CSB_1
DDR1_DM<0> C12 DM0_1
DDR1_DM<1> B10 DM1_1
DDR1_DM<2> B16 DM2_1
DDR1_DM<2> D7 DM3_1
DDR1_DQ<0> C15 DQ0_1
DDR1_DQ<1> D15 DQ1_1
DDR1_DQ<2> B14 DQ2_1
DDR1_DQ<3> C14 DQ3_1
DDR1_DQ<4> D14 DQ4_1
DDR1_DQ<5> E14 DQ5_1
DDR1_DQ<6> B13 DQ6_1
DDR1_DQ<7> C13 DQ7_1
DDR1_DQ<8> C9 DQ8_1
DDR1_DQ<9> D9 DQ9_1
DDR1_DQ<10> B8 DQ10_1
DDR1_DQ<11> C8 DQ11_1
DDR1_DQ<12> D8 DQ12_1
DDR1_DQ<14> E8 DQ13_1
DDR1_DQ<13> B7 DQ14_1
DDR1_DQ<15> C7 DQ15_1
DDR1_DQ<24> B18 DQ16_1
DDR1_DQ<25> C18 DQ17_1
DDR1_DQ<26> D18 DQ18_1
DDR1_DQ<27> E18 DQ19_1
DDR1_DQ<28> B17 DQ20_1
DDR1_DQ<29> D17 DQ21_1
DDR1_DQ<30> E17 DQ22_1
DDR1_DQ<31> E16 DQ23_1
DDR1_DQ<16> B6 DQ24_1
DDR1_DQ<17> B5 DQ25_1
DDR1_DQ<18> C5 DQ26_1
DDR1_DQ<19> D5 DQ27_1
DDR1_DQ<20> B4 DQ28_1
DDR1_DQ<21> C4 DQ29_1
DDR1_DQ<22> B3 DQ30_1
DDR1_DQ<23> C3 DQ31_1
DDR1_DQS_P<0> D13 DQS0_1
DDR1_DQS_N<0> D12 DQSB0_1
DDR1_DQS_P<1> D10 DQS1_1
DDR1_DQS_N<1> C10 DQSB1_1
DDR1_DQS_P<3> C16 DQS2_1
DDR1_DQS_N<3> D16 DQSB2_1
DDR1_DQS_P<2> D6 DQS3_1
DDR1_DQS_N<2> C6 DQSB3_1
PPVREF_DDR1_CA U10 VREFCA_1
PPVREF_DDR1_DQ D11 VREFDQ_1
DDR1_ZQ U7 ZQ_1
R1620 240 1% 1/20W MF 201
CA0_2 G16 DDR0_CA<0>
CA1_2 G17 DDR0_CA<1>
CA2_2 H17 DDR0_CA<2>
CA3_2 H18 DDR0_CA<3>
CA4_2 J16 DDR0_CA<4>
CA5_2 N16 DDR0_CA<5>
CA6_2 N17 DDR0_CA<6>
CA7_2 P17 DDR0_CA<7>
CA8_2 P18 DDR0_CA<8>
CA9_2 R16 DDR0_CA<9>
CK_2 K17 DDR0_CK_P
CKB_2 L17 DDR0_CK_N
CKE_2 J18 DDR0_CKE<0>
CSB_2 J17 DDR0_CSN<0>
DM0_2 K3 DDR0_DM<0>
DM1_2 M2 DDR0_DM<1>
DM2_2 G4 DDR0_DM<2>
DM3_2 T2 DDR0_DM<3>
DQ0_2 G3 DDR0_DQ<0>
DQ1_2 G2 DDR0_DQ<1>
DQ2_2 H5 DDR0_DQ<2>
DQ3_2 H4 DDR0_DQ<3>
DQ4_2 H3 DDR0_DQ<4>
DQ5_2 H2 DDR0_DQ<5>
DQ6_2 J3 DDR0_DQ<6>
DQ7_2 J2 DDR0_DQ<7>
DQ8_2 N4 DDR0_DQ<8>
DQ9_2 N3 DDR0_DQ<14>
DQ10_2 P5 DDR0_DQ<10>
DQ11_2 P4 DDR0_DQ<11>
DQ12_2 P3 DDR0_DQ<12>
DQ13_2 P2 DDR0_DQ<13>
DQ14_2 R4 DDR0_DQ<9>
DQ15_2 R3 DDR0_DQ<15>
DQ16_2 B2 DDR0_DQ<24>
DQ17_2 C2 DDR0_DQ<25>
DQ18_2 D3 DDR0_DQ<26>
DQ19_2 D2 DDR0_DQ<28>
DQ20_2 E4 DDR0_DQ<27>
DQ21_2 E3 DDR0_DQ<29>
DQ22_2 E2 DDR0_DQ<30>
DQ23_2 F2 DDR0_DQ<31>
DQ24_2 T5 DDR0_DQ<16>
DQ25_2 U5 DDR0_DQ<22>
DQ26_2 U4 DDR0_DQ<19>
DQ27_2 U2 DDR0_DQ<18>
DQ28_2 V5 DDR0_DQ<20>
DQ29_2 V4 DDR0_DQ<17>
DQ30_2 V3 DDR0_DQ<21>
DQ31_2 V2 DDR0_DQ<23>
DQS0_2 J4 DDR0_DQS_P<0>
DQSB0_2 K4 DDR0_DQS_N<0>
DQS1_2 M4 DDR0_DQS_P<1>
DQSB1_2 M3 DDR0_DQS_N<1>
DQS2_2 F4 DDR0_DQS_P<3>
DQSB2_2 F3 DDR0_DQS_N<3>
DQS3_2 T3 DDR0_DQS_P<2>
DQSB3_2 T4 DDR0_DQS_N<2>
VREFCA_2 M17 PPVREF_DDR0_CA
VREFDQ_2 L4 PPVREF_DDR0_DQ
ZQ_2 R17 DDR0_ZQ
R1621 240 1% 1/20W MF 201
=PP1V8_S2R_DDR
C1601 10UF 20% 6.3V X5R 603
C1602 1UF 10% 6.3V CERM 402
C1603 1UF 10% 6.3V CERM 402
C1604 0.01UF 10% 6.3V X5R 01005
C1605 0.01UF 10% 6.3V X5R 01005
C1606 0.22UF 20% 6.3V X5R 0201
C1607 0.22UF 20% 6.3V X5R 0201
C1608 0.22UF 20% 6.3V X5R 0201
C1609 56PF 5% 6.3V NPO-C0G 01005
=PP1V2_S2R_DDR
C1610 0.22UF 20% 6.3V X5R 0201
C1611 0.22UF 20% 6.3V X5R 0201
C1612 0.22UF 20% 6.3V X5R 0201
C1613 0.22UF 20% 6.3V X5R 0201
C1614 10UF 20% 6.3V X5R 603
C1615 4.3UF 20% 4V X5R-CERM 0610
C1616 1UF 10% 6.3V CERM 402
C1617 1UF 10% 6.3V CERM 402
C1618 0.01UF 10% 10V X5R 201
C1619 56PF 5% 6.3V NPO-C0G 01005
=PP1V2_VDDQ_DDR
C1623 56PF 5% 6.3V NPO-C0G 01005
C1620 10UF 20% 6.3V X5R 603
C1621 4.3UF 20% 4V X5R-CERM 0610
C1624 0.22UF 20% 6.3V X5R 0201
C1625 0.22UF 20% 6.3V X5R 0201
C1626 0.22UF 20% 6.3V X5R 0201
C1622 0.01UF 10% 6.3V X5R 01005
=PP1V2_S2R_DDR
C1627 10UF 20% 6.3V X5R 603
C1628 1UF 10% 6.3V CERM 402
C1629 1UF 10% 6.3V CERM 402
C1630 0.01UF 10% 6.3V X5R 01005
C1631 0.01UF 10% 6.3V X5R 01005
C1632 0.22UF 20% 6.3V X5R 0201
C1633 0.22UF 20% 6.3V X5R 0201
C1634 0.22UF 20% 6.3V X5R 0201
C1635 56PF 5% 6.3V NPO-C0G 01005
OMIT
U1600
H4G-DRAM
XXXMB
BGA
SYM 2 OF 2
VDD1
VDD2
VDDQ
VDDCA
VSS
A2 VDD1_0
B1 VDD1_1
B11 VDD1_2
F17 VDD1_3
L2 VDD1_4
M16 VDD1_5
T10 VDD1_6
U18 VDD1_7
V17 VDD1_8
V6 VDD1_9
W17 VDD1_10
U19 VDD1_11
E11 VDD2_1
E19 VDD2_2
L5 VDD2_3
M18 VDD2_4
U17 VDD2_5
T18 VDD2_6
V10 VDD2_7
V16 VDD2_8
V18 VDD2_9
W5 VDD2_10
W16 VDD2_11
W19 VDD2_12
W18 VDD2_13
V19 VDD2_14
A3 VDD2_15
T19 VDD2_16
H1 VDDQ27
M1 VDDQ32
W3 VDDQ31
E1 VDDQ
U1 VDDQ1
B12 VDDQ3
D4 VDDQ6
U3 VDDQ30
A14 VDDQ23
C17 VDDQ25
C19 VDDQ26
A10 VDDQ22
A17 VDDQ34
J5 VDDQ16
K2 VDDQ17
A8 VDDQ21
N2 VDDQ19
R5 VDDQ20
A13 VDDQ24
E10 VDDQ28
E15 VDDQ29
P1 VDDQ33
F18 VDDCA1
H16 VDDCA2
K16 VDDCA3
L16 VDDCA4
P16 VDDCA5
T11 VDDCA6
T12 VDDCA7
T14 VDDCA8
V7 VDDCA9
T8 VDDCA10
VSS0 A16
VSS55 A19
VSS2 A4
VSS3 A6
VSS4 B15
VSS49 C1
VSS6 B9
VSS7 C11
VSS9 D1
VSS10 D19
VSS1 A1
VSS12 E12
VSS13 E13
VSS51 G5
VSS52 T16
VSS50 E7
VSS18 F16
VSS48 B19
VSS20 G18
VSS53 V1
VSS22 J1
VSS23 K18
VSS24 K5
VSS25 L18
VSS26 L3
VSS27 M5
VSS28 N18
VSS29 N5
VSS47 A18
VSS32 R18
VSS33 R2
VSS34 T1
VSS35 T17
VSS36 U16
VSS54 W2
VSS39 U6
VSS40 V11
VSS41 V12
VSS42 V15
VSS43 T6
VSS44 V9
VSS45 W1
VSS46 W4
SYNC MASTER=MIKE
SYNC DATE=06/21/2010
PAGE TITLE
DDR 0 AND 1
Apple Inc.
DRAWING NUMBER 051-8773
SIZE D
REVISION 10.0.0
BRANCH
PAGE 16 OF 157
SHEET 13 OF 48
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


=PP1V2_S2R_DDR
R1705 2.21K 1% 1/32W MF 01005
C1760 0.01UF 10% 6.3V X5R 01005
NOSTUFF
PPVREF_DDR2_CA
R1706 2.21K 1% 1/32W MF 01005
C1750 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V2_S2R_DDR
R1751 2.21K 1% 1/32W MF 01005
C1761 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR3_CA
R1752 2.21K 1% 1/32W MF 01005
C1752 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_DDR
R1753 1.00K 1% 1/32W MF 01005
C1762 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR2_DQ
R1754 1.00K 1% 1/32W MF 01005
C1754 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_DDR
R1755 1.00K 1% 1/32W MF 01005
C1763 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR3_DQ
R1756 1.00K 1% 1/32W MF 01005
C1756 0.01UF 10% 6.3V X5R 01005
NOSTUFF VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
OMIT
U1700
H4G-DRAM
XXXMB
BGA
SYM 1 OF 2
DDR_1
DDR_2
DDR3_CA<0> T15 CA0_1
DDR3_CA<1> U15 CA1_1
DDR3_CA<2> U14 CA2_1
DDR3_CA<3> V14 CA3_1
DDR3_CA<4> T13 CA4_1
DDR3_CA<5> T9 CA5_1
DDR3_CA<6> U9 CA6_1
DDR3_CA<7> U8 CA7_1
DDR3_CA<8> V8 CA8_1
DDR3_CA<9> T7 CA9_1
DDR3_CK_P U12 CK_1
DDR3_CK_N U11 CKB_1
DDR3_CKE<0> V13 CKE_1
DDR3_CSN<0> U13 CSB_1
DDR3_DM<0> C12 DM0_1
DDR3_DM<1> B10 DM1_1
DDR3_DM<3> B16 DM2_1
DDR3_DM<2> D7 DM3_1
DDR3_DQ<0> C15 DQ0_1
DDR3_DQ<1> D15 DQ1_1
DDR3_DQ<2> B14 DQ2_1
DDR3_DQ<3> C14 DQ3_1
DDR3_DQ<4> D14 DQ4_1
DDR3_DQ<5> E14 DQ5_1
DDR3_DQ<6> B13 DQ6_1
DDR3_DQ<7> C13 DQ7_1
DDR3_DQ<8> C9 DQ8_1
DDR3_DQ<9> D9 DQ9_1
DDR3_DQ<10> B8 DQ10_1
DDR3_DQ<11> C8 DQ11_1
DDR3_DQ<12> D8 DQ12_1
DDR3_DQ<13> E8 DQ13_1
DDR3_DQ<14> B7 DQ14_1
DDR3_DQ<15> C7 DQ15_1
DDR3_DQ<24> B18 DQ16_1
DDR3_DQ<25> C18 DQ17_1
DDR3_DQ<26> D18 DQ18_1
DDR3_DQ<27> E18 DQ19_1
DDR3_DQ<28> B17 DQ20_1
DDR3_DQ<29> D17 DQ21_1
DDR3_DQ<30> E17 DQ22_1
DDR3_DQ<31> E16 DQ23_1
DDR3_DQ<16> B6 DQ24_1
DDR3_DQ<17> B5 DQ25_1
DDR3_DQ<18> C5 DQ26_1
DDR3_DQ<19> D5 DQ27_1
DDR3_DQ<20> B4 DQ28_1
DDR3_DQ<21> C4 DQ29_1
DDR3_DQ<22> B3 DQ30_1
DDR3_DQ<23> C3 DQ31_1
DDR3_DQS_P<0> D13 DQS0_1
DDR3_DQS_N<0> D12 DQSB0_1
DDR3_DQS_P<1> D10 DQS1_1
DDR3_DQS_N<1> C10 DQSB1_1
DDR3_DQS_P<3> C16 DQS2_1
DDR3_DQS_N<3> D16 DQSB2_1
DDR3_DQS_P<2> D6 DQS3_1
DDR3_DQS_N<2> C6 DQSB3_1
PPVREF_DDR3_CA U10 VREFCA_1
PPVREF_DDR3_DQ D11 VREFDQ_1
DDR3_ZQ U7 ZQ_1
R1720 240 1% 1/20W MF 201
CA0_2 G16 DDR2_CA<0>
CA1_2 G17 DDR2_CA<1>
CA2_2 H17 DDR2_CA<2>
CA3_2 H18 DDR2_CA<3>
CA4_2 J16 DDR2_CA<4>
CA5_2 N16 DDR2_CA<5>
CA6_2 N17 DDR2_CA<6>
CA7_2 P17 DDR2_CA<7>
CA8_2 P18 DDR2_CA<8>
CA9_2 R16 DDR2_CA<9>
CK_2 K17 DDR2_CK_P
CKB_2 L17 DDR2_CK_N
CKE_2 J18 DDR2_CKE<0>
CSB_2 J17 DDR2_CSN<0>
DM0_2 K3 DDR2_DM<0>
DM1_2 M2 DDR2_DM<1>
DM2_2 G4 DDR2_DM<3>
DM3_2 T2 DDR2_DM<2>
DQ0_2 G3 DDR2_DQ<0>
DQ1_2 G2 DDR2_DQ<1>
DQ2_2 H5 DDR2_DQ<2>
DQ3_2 H4 DDR2_DQ<3>
DQ4_2 H3 DDR2_DQ<4>
DQ5_2 H2 DDR2_DQ<5>
DQ6_2 J3 DDR2_DQ<6>
DQ7_2 J2 DDR2_DQ<7>
DQ8_2 N4 DDR2_DQ<8>
DQ9_2 N3 DDR2_DQ<15>
DQ10_2 P5 DDR2_DQ<10>
DQ11_2 P4 DDR2_DQ<11>
DQ12_2 P3 DDR2_DQ<12>
DQ13_2 P2 DDR2_DQ<13>
DQ14_2 R4 DDR2_DQ<14>
DQ15_2 R3 DDR2_DQ<9>
DQ16_2 B2 DDR2_DQ<24>
DQ17_2 C2 DDR2_DQ<25>
DQ18_2 D3 DDR2_DQ<26>
DQ19_2 D2 DDR2_DQ<27>
DQ20_2 E4 DDR2_DQ<30>
DQ21_2 E3 DDR2_DQ<29>
DQ22_2 E2 DDR2_DQ<28>
DQ23_2 F2 DDR2_DQ<31>
DQ24_2 T5 DDR2_DQ<16>
DQ25_2 U5 DDR2_DQ<20>
DQ26_2 U4 DDR2_DQ<18>
DQ27_2 U2 DDR2_DQ<19>
DQ28_2 V5 DDR2_DQ<23>
DQ29_2 V4 DDR2_DQ<21>
DQ30_2 V3 DDR2_DQ<22>
DQ31_2 V2 DDR2_DQ<17>
DQS0_2 J4 DDR2_DQS_P<0>
DQSB0_2 K4 DDR2_DQS_N<0>
DQS1_2 M4 DDR2_DQS_P<1>
DQSB1_2 M3 DDR2_DQS_N<1>
DQS2_2 F4 DDR2_DQS_P<3>
DQSB2_2 F3 DDR2_DQS_N<3>
DQS3_2 T3 DDR2_DQS_P<2>
DQSB3_2 T4 DDR2_DQS_N<2>
VREFCA_2 M17 PPVREF_DDR2_CA
VREFDQ_2 L4 PPVREF_DDR2_DQ
ZQ_2 R17 DDR2_ZQ
R1721 240 1% 1/20W MF 201
=PP1V8_S2R_DDR
C1701 10UF 20% 6.3V X5R 603
C1702 1UF 10% 6.3V CERM 402
C1703 1UF 10% 6.3V CERM 402
C1704 0.01UF 10% 6.3V X5R 01005
C1705 0.01UF 10% 6.3V X5R 01005
C1706 0.22UF 20% 6.3V X5R 0201
C1707 0.22UF 20% 6.3V X5R 0201
C1708 0.22UF 20% 6.3V X5R 0201
C1709 56PF 5% 6.3V NPO-COG 01005
=PP1V2_S2R_DDR
C1710 0.22UF 20% 6.3V X5R 0201
C1711 0.22UF 20% 6.3V X5R 0201
C1712 0.22UF 20% 6.3V X5R 0201
C1713 0.22UF 20% 6.3V X5R 0201
C1714 10UF 20% 6.3V X5R 603
C1715 4.3UF 20% 4V X5R-CERM 0610
C1716 1UF 10% 6.3V CERM 402
C1717 1UF 10% 6.3V CERM 402
C1718 0.01UF 10% 6.3V X5R 201
C1719 56PF 5% 6.3V NPO-COG 01005
=PP1V2_VDDQ_DDR
C1723 56PF 5% 6.3V NPO-COG 01005
C1720 10UF 20% 6.3V X5R 603
C1721 4.3UF 20% 4V X5R-CERM 0610
C1724 0.22UF 20% 6.3V X5R 0201
C1725 0.22UF 20% 6.3V X5R 0201
C1726 0.22UF 20% 6.3V X5R 0201
C1722 0.01UF 10% 6.3V X5R 01005
=PP1V2_S2R_DDR
C1727 10UF 20% 6.3V X5R 603
C1728 1UF 10% 6.3V CERM 402
C1729 1UF 10% 6.3V CERM 402
C1730 0.01UF 10% 6.3V X5R 01005
C1731 0.01UF 10% 6.3V X5R 01005
C1732 0.22UF 20% 6.3V X5R 0201
C1733 0.22UF 20% 6.3V X5R 0201
C1734 0.22UF 20% 6.3V X5R 0201
C1735 56PF 5% 6.3V NPO-COG 01005
OMIT
U1700
H4G-DRAM
XXXMB
BGA
SYM 2 OF 2
VDD1
VDD2
VDDQ
VDDCA
VSS
A2 VDD1_0
B1 VDD1_1
B11 VDD1_2
F17 VDD1_3
L2 VDD1_4
M16 VDD1_5
T10 VDD1_6
U18 VDD1_7
V17 VDD1_8
V6 VDD1_9
W17 VDD1_10
U19 VDD1_11
E11 VDD2_1
E19 VDD2_2
L5 VDD2_3
M18 VDD2_4
U17 VDD2_5
T18 VDD2_6
V10 VDD2_7
V16 VDD2_8
V18 VDD2_9
W5 VDD2_10
W16 VDD2_11
W19 VDD2_12
W18 VDD2_13
V19 VDD2_14
A3 VDD2_15
T19 VDD2_16
H1 VDDQ27
M1 VDDQ32
W3 VDDQ31
E1 VDDQ
U1 VDDQ1
B12 VDDQ3
D4 VDDQ6
U3 VDDQ30
A14 VDDQ23
C17 VDDQ25
C19 VDDQ26
A10 VDDQ22
A17 VDDQ34
J5 VDDQ16
K2 VDDQ17
A8 VDDQ21
N2 VDDQ19
R5 VDDQ20
A13 VDDQ24
E10 VDDQ28
E15 VDDQ29
P1 VDDQ33
F18 VDDCA1
H16 VDDCA2
K16 VDDCA3
L16 VDDCA4
P16 VDDCA5
T11 VDDCA6
T12 VDDCA7
T14 VDDCA8
V7 VDDCA9
T8 VDDCA10
VSS0 A16
VSS55 A19
VSS2 A4
VSS3 A6
VSS4 B15
VSS49 C1
VSS6 B9
VSS7 C11
VSS9 D1
VSS10 D19
VSS1 A1
VSS12 E12
VSS13 E13
VSS51 G5
VSS52 T16
VSS50 E7
VSS18 F16
VSS48 B19
VSS20 G18
VSS53 V1
VSS22 J1
VSS23 K18
VSS24 K5
VSS25 L18
VSS26 L3
VSS27 M5
VSS28 N18
VSS29 N5
VSS47 A18
VSS32 R18
VSS33 R2
VSS34 T1
VSS35 T17
VSS36 U16
VSS54 W2
VSS39 U6
VSS40 V11
VSS41 V12
VSS42 V15
VSS43 T6
VSS44 V9
VSS45 W1
VSS46 W4
SYNC_MASTER=MIKE
SYNC_DATE=06/21/2010
PAGE TITLE
DDR 2 AND 3
Apple Inc.
DRAWING NUMBER 051-8773
SIZE D
REVISION 10.0.0
BRANCH
PAGE 17 OF 157
SHEET 14 OF 48
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

WIFI ALIASES

42 40 4	HSIC1_WLAN_DATA1	MAKE_BASE=TRUE	HSIC_DATA_4330	31 33
42 40 4	HSIC1_WLAN_STB1	MAKE_BASE=TRUE	HSIC_STROBE_4330	31 33
42 5	HSIC_HOST_READY_WLAN	MAKE_BASE=TRUE	WLAN_GPIO1	31 33
42 5	HSIC_WLAN_RDY	MAKE_BASE=TRUE	HSIC_DEVICE_READY	31
45 37	RST_WLAN_L	MAKE_BASE=TRUE	WLAN_ENABLE	31 33
37	PM_WLAN_HOST_WAKE	MAKE_BASE=TRUE	WLAN_GPIO0	31 33
45 37	RST_BT_L	MAKE_BASE=TRUE	BT_RESET_N	31 33
37	PM_BT_HOST_WAKE	MAKE_BASE=TRUE	BT_HOST_WAKE	31 33
5	PM_BT_WAKE	MAKE_BASE=TRUE	BT_WAKE	31 33
42 5	UART3_BT_RXD	MAKE_BASE=TRUE	BT_UART_TXD	31 33
42 5	UART3_BT_TXD	MAKE_BASE=TRUE	BT_UART_RXD	31 33
42 5	UART3_BT_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_N	31 33
42 5	UART3_BT_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_N	31 33
42 37	CLK_32K_WLAN	MAKE_BASE=TRUE	CLK32K	32 33
42 19 5	I2S2_VSP_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK	31
42 19 5	I2S2_VSP_DOUT	MAKE_BASE=TRUE	BT_PCM_DIN	31
42 19 5	I2S2_VSP_DIN	MAKE_BASE=TRUE	BT_PCM_DOUT	31
42 19 5	I2S2_VSP_LRCK	MAKE_BASE=TRUE	BT_PCM_SYNC	31
42 5	UART6_WLAN_RXD	MAKE_BASE=TRUE	WLAN_GPIO4	31 33
42 5	UART6_WLAN_TXD	MAKE_BASE=TRUE	WLAN_GPIO3	31 33

UART ALIASES

42 5	UART0_AP_RXD	MAKE_BASE=TRUE	UART0_MUX_RXD	11 42
42 5	UART0_AP_TXD	MAKE_BASE=TRUE	UART0_MUX_TXD	11 42

OBSOLETE ALIASES

	NC_EXT_SMPS_REQ	MAKE_BASE=TRUE	EXT_SMPS_REQ	
	NC_EXT_PWM_REQ	MAKE_BASE=TRUE	EXT_PWM_REQ	
	NC_BT_GPIO5	MAKE_BASE=TRUE	BT_GPIO5	31
	TP_WLAN_GPIO5	MAKE_BASE=TRUE	WLAN_GPIO5	31
45 30 5	GSM_TXBURST_IND	MAKE_BASE=TRUE	LED_DRIVE_GSMB	

NEED TO DOUBLE CHECK IF WE NEED THIS IN IPAD, OR IF THIS MIGHT BE A PHONE SPECIFIC ISSUE

SYNC_MASTER=ALEX SYNC_DATE=09/30/2010

PAGE TITLE
MLB ALIASES/CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 21 OF 157

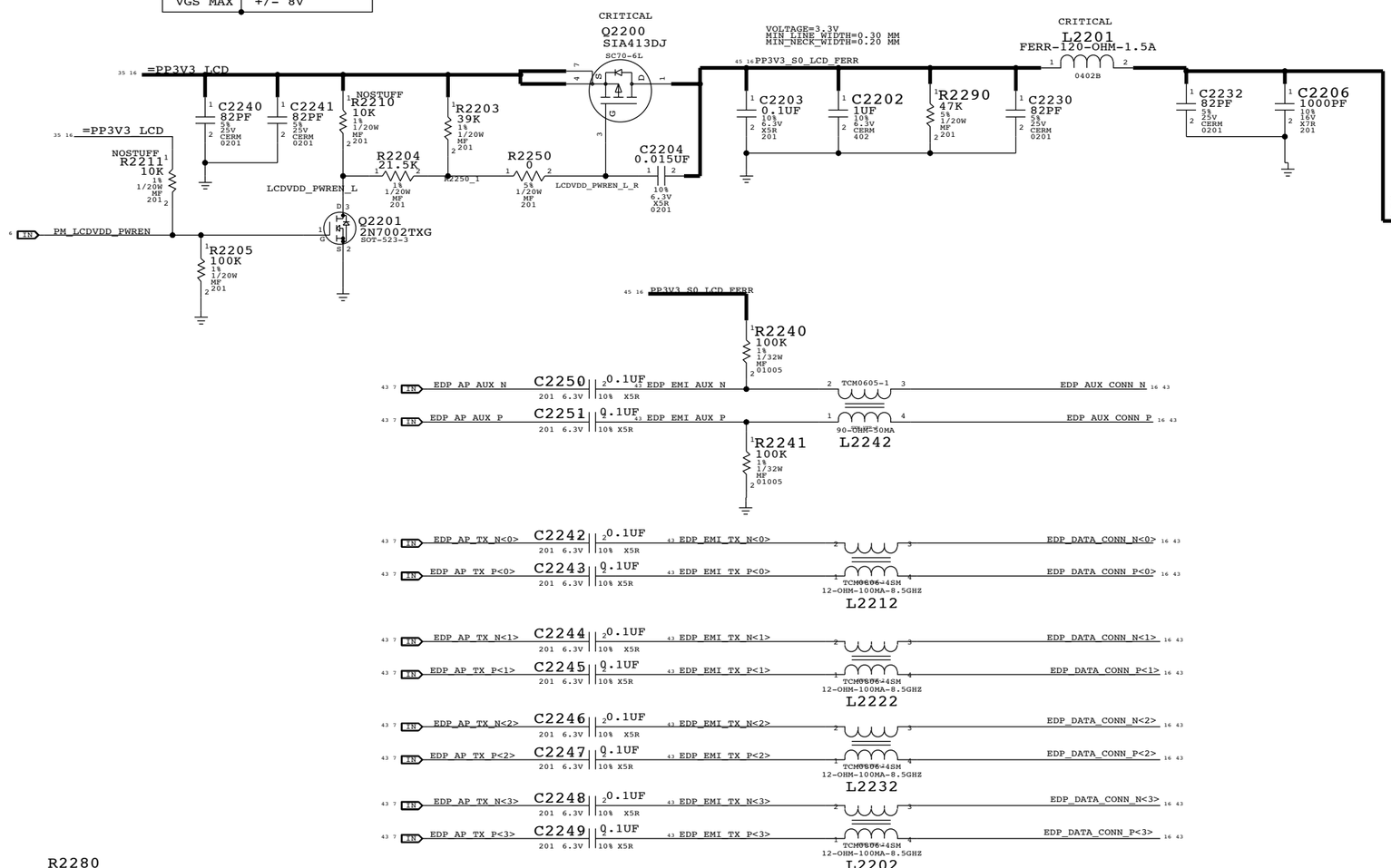
SHEET 15 OF 48

EDP CONNECTOR

SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0903	376S0796		Q2200	RADAR:8379470
155S0667	155S0583			RADAR:8616060, RADAR: 9015335



SYNC MASTER=JOE SYNC DATE=01/19/2011

PAGE TITLE

VIDEO: EDP CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 22 OF 157

SHEET 16 OF 48

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

CONNECTORS TO GRAPE FLEX

R3070 0 5% 1/20W MF 201
AG_SHLD_TST_FLEX → AG_SHLD_TST
R3071 0 5% 1/20W MF 201 NOSTUFF
C3070 0.1UF 10% 25V X5R 402

CRITICAL
P/N 518S0828

MT_PANEL_OUT<36> MT_PANEL_OUT<38> MT_PANEL_IN<29> MT_PANEL_IN<27> MT_PANEL_IN<25> MT_PANEL_IN<23> MT_PANEL_IN<21> MT_PANEL_IN<19> MT_PANEL_IN<17> MT_PANEL_IN<15> MT_PANEL_IN<13> MT_PANEL_IN<11> MT_PANEL_IN<9> MT_PANEL_IN<7> MT_PANEL_IN<5> MT_PANEL_IN<3> MT_PANEL_IN<1> AG_SHLD_TST_FLEX
MT_PANEL_OUT<37> MT_PANEL_OUT<39> MT_PANEL_IN<28> MT_PANEL_IN<26> MT_PANEL_IN<24> MT_PANEL_IN<22> MT_PANEL_IN<20> MT_PANEL_IN<18> MT_PANEL_IN<16> MT_PANEL_IN<14> MT_PANEL_IN<12> MT_PANEL_IN<10> MT_PANEL_IN<8> MT_PANEL_IN<6> MT_PANEL_IN<4> MT_PANEL_IN<2> MT_PANEL_IN<0>
F-RT-SM
502250-8037
J3010
MATES WITH LEFTMOST GRAPE FLEX TAIL

CRITICAL
MT_PANEL_OUT<1> MT_PANEL_OUT<3> MT_PANEL_OUT<5> MT_PANEL_OUT<7> MT_PANEL_OUT<9> MT_PANEL_OUT<11> MT_PANEL_OUT<13> MT_PANEL_OUT<15> MT_PANEL_OUT<17> MT_PANEL_OUT<19> MT_PANEL_OUT<21> MT_PANEL_OUT<23> MT_PANEL_OUT<25> MT_PANEL_OUT<27> MT_PANEL_OUT<29> MT_PANEL_OUT<31> MT_PANEL_OUT<33> MT_PANEL_OUT<35>
MT_PANEL_OUT<0> MT_PANEL_OUT<2> MT_PANEL_OUT<4> MT_PANEL_OUT<6> MT_PANEL_OUT<8> MT_PANEL_OUT<10> MT_PANEL_OUT<12> MT_PANEL_OUT<14> MT_PANEL_OUT<16> MT_PANEL_OUT<18> MT_PANEL_OUT<20> MT_PANEL_OUT<22> MT_PANEL_OUT<24> MT_PANEL_OUT<26> MT_PANEL_OUT<28> MT_PANEL_OUT<30> MT_PANEL_OUT<32> MT_PANEL_OUT<34>
F-RT-SM
502250-8037
J3011
MATES WITH RIGHTMOST GRAPE FLEX TAIL

PP18V_GRAPE
C3005 0.1UF 10% 25V X5R 402
C3007 0.1UF 10% 25V X5R 402
C3053 0.1UF 10% 25V X5R 402
=PP3V0_GRAPE_MARIOJ
C3006 0.1UF 10% 6.3V X5R 201
VDDH VCC_DIG

U3003 GROUNDHOG BGA
CRITICAL
OMIT

MUX_IN<0> MUX_IN<1> MUX_IN<2> MUX_IN<3> MUX_IN<4> MUX_IN<5> MUX_IN<6> MUX_IN<7> MUX_IN<8> MUX_IN<9> MUX_IN<10> MUX_IN<11> MUX_IN<12> MUX_IN<13> MUX_IN<14> MUX_IN<15> MUX_IN<16> MUX_IN<17> MUX_IN<18> MUX_IN<19>
MUX0 MUX1 MUX2 MUX3 MUX4 MUX5 MUX6 MUX7 MUX8 MUX9 MUX10 MUX11 MUX12 MUX13 MUX14 MUX15 MUX16 MUX17 MUX18 MUX19 MUX20 MUX21 MUX22 MUX23
Z1_BON_L<0> Z1_BON_L<1> Z1_BON_L<2> Z1_BON_L<3> Z1_BON_L<4> Z1_BON_L<5>
BON_L0 BON_L1 BON_L2 BON_L3 BON_L4 BON_L5
VSTM0 … VSTM47 ← MT_PANEL_OUT<0> … MT_PANEL_OUT<39>
A_AD_R0 A_AD_R1 A_AD_R2 ← Z1_B_ADR<0> Z1_B_ADR<1> Z1_B_ADR<2>
GND

BOOST CONVERTOR

MIN_NECK_MIDTH SHOULD BE 0.4MM
CRITICAL L3000 4.7UH-700MA-280MOHM
VR_BOOST_L → VLF → VR_BOOST_SW
CRITICAL D3000 B0520WSXG SOD-323
PP18V_R_GRAPE
R3066 0.1 1% 1/20W MF 201
LOAD CURRENT ~ 153UA
PP18V_GRAPE
C3009 0.1UF 10% 16V X5R 402
C3008 33PF 5% 25V NPO-C0G 201
R3009 1M 1% 1/16W MF-LF 402
C3000 1UF 10% 25V X5R 603-1
=PP3V0_GRAPE
CRITICAL
U3000 TPS61045 QFN-1
VIN L DO FB CTRL SW THRML PAD PGND GND
VR_BOOST_FBK PM_BOOST_EN
NCX
C3001 2.2UF 10% 6.3V X5R 603
C3002 470PF 10% 16V X5R-X7R 201
R3012 71.5K 1% 1/20W MF 201
AGND_U3000
XW3000 SM

U3007 POFP1

=PP3V0_GRAPE
R3030 10K 5% 1/20W MF 201
R3031 10K 5% 1/20W MF 201
C3030 0.1UF 10% 6.3V X5R 201
CRITICAL
VCCA VCCB
DIR_U3007
SPI1_GRAPE_SCLK
SPI1_GRAPE_CS_L
SPI1_GRAPE_MOSI
GRAPE_FW_DNLD_EN_L
1A1 2A1 1DIR 1OE* 1A2 2A2 2DIR 2OE*
SN74AVCH4T245RSV
(A -> B)
GND
1B1 2B1 1B2 2B2
Z1_SCLK Z2_H_CS_L Z1_MISO Z1_CS_OE
TO Z1/Z2
APN:311S0485
C3031 0.1UF 10% 6.3V X5R 201
R3032 3.3K 5% 1/20W MF 201
R3033 10K 5% 1/20W MF 201

U3010 SN74LVC1G126DRYR-M LLP

Z1_CS_OE Z2_H_CS_L → OE A Y → Z1_CS_L
GND NC

U3009 SN74LVC1G125DRYR-M LLP

=PP3V0_GRAPE
C3041 0.1UF 10% 6.3V X5R 201
CRITICAL
SPI1_GRAPE_MISO → Z1_MOSI
Z1_CS_OE
NC

=PP3V0_GRAPE
C3050 0.1UF 10% 6.3V X5R 201
CRITICAL

SPI1_GRAPE_SCLK MAKE_BASE=TRUE → GRAPE_SCLK
SPI1_GRAPE_CS_L MAKE_BASE=TRUE → GRAPE_CS_L
SPI1_GRAPE_MOSI MAKE_BASE=TRUE → GRAPE_MOSI
RST_GRAPE_L MAKE_BASE=TRUE → RST_GRAPE_Z1_L
RST_GRAPE_Z2_L
SPI1_GRAPE_MISO MAKE_BASE=TRUE → GRAPE_MISO
TO Z2

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=RAMSIN SYNC_DATE=12/17/2010
PAGE TITLE
GRAPE: GROUNDHOG,CONN,BOOST

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 30 OF 157
SHEET 17 OF 48

ZEPHYR 1+ ASIC

=PP3V0_GRAPE_Z1 35

R3101 4.7 5% 1/20W MF 201

C3102 0.1UF 10% 6.3V X5R 201

C3104 2.2UF 20% 4V X5R 402

C3103 0.1UF 10% 6.3V X5R 201

MT_3V3_INT 43

45 18 Z1_1V8_OUT

C3101 2.2UF 20% 4V X5R 402

=PP3V0_GRAPE 17 18 35

R3155 100K 5% 1/20W MF 201

G6 G7 G8 K4 K10 — VDDANA

C10 — VDDDIG CRITICAL

C5 C9 — VDDIO

B6 — V18

U3100
BCM5973
BGA

17 MT_PANEL_IN<0>	H2	IN0	
17 MT_PANEL_IN<1>	G2	IN1	
17 MT_PANEL_IN<2>	D7	IN2	
17 MT_PANEL_IN<3>	C1	IN3	
17 MT_PANEL_IN<4>	F1	IN4	
17 MT_PANEL_IN<5>	J1	IN5	
17 MT_PANEL_IN<6>	D2	IN6	
17 MT_PANEL_IN<7>	D1	IN7	
17 MT_PANEL_IN<8>	K7	IN8	
17 MT_PANEL_IN<9>	H1	IN9	
17 MT_PANEL_IN<10>	E1	IN10	
17 MT_PANEL_IN<11>	E2	IN11	
17 MT_PANEL_IN<12>	J2	IN12	
17 MT_PANEL_IN<13>	G1	IN13	
17 MT_PANEL_IN<14>	F2	IN14	
17 MT_PANEL_IN<15>	J7	IN15	
17 MT_PANEL_IN<16>	K2	IN16	
17 MT_PANEL_IN<17>	N4	IN17	
17 MT_PANEL_IN<18>	M5	IN18	
17 MT_PANEL_IN<19>	N5	IN19	
17 MT_PANEL_IN<20>	M6	IN20	
17 MT_PANEL_IN<21>	N3	IN21	
17 MT_PANEL_IN<22>	M3	IN22	
17 MT_PANEL_IN<23>	L1	IN23	
17 MT_PANEL_IN<24>	K1	IN24	
17 MT_PANEL_IN<25>	L2	IN25	
17 MT_PANEL_IN<26>	N6	IN26	
17 MT_PANEL_IN<27>	M2	IN27	
17 MT_PANEL_IN<28>	M4	IN28	
17 MT_PANEL_IN<29>	M1	IN29	
17 MUX_IN<0>	N2	IN30	
17 MUX_IN<1>	N1	IN31	
17 MUX_IN<2>	N13	IN32	
17 MUX_IN<3>	N12	IN33	
17 MUX_IN<4>	M10	IN34	
17 MUX_IN<5>	M13	IN35	
17 MUX_IN<6>	N8	IN36	
17 MUX_IN<7>	M12	IN37	
17 MUX_IN<8>	K13	IN38	
17 MUX_IN<9>	L13	IN39	
17 MUX_IN<10>	L12	IN40	
17 MUX_IN<11>	M11	IN41	
17 MUX_IN<12>	N11	IN42	
17 MUX_IN<13>	M8	IN43	
17 MUX_IN<14>	N9	IN44	
17 MUX_IN<15>	M9	IN45	
17 MUX_IN<16>	N10	IN46	
17 MUX_IN<17>	K12	IN47	
17 MUX_IN<18>	J13	IN48	
17 MUX_IN<19>	F12	IN49	
NC	C13	IN50	
NC	C12	IN51	
NC	B12	IN52	
NC	E13	IN53	
NC	B13	IN54	
NC	N7	IN55	
NC	B13	IN56	
NC	C12	IN57	
NC	B12	IN58	
NC	F13	IN59	
NC	C13	IN60	
NC	E7	IN61	
NC	M7	IN62	
NC	G12	IN63	

SCLK	A11	Z1_SCLK	IN 17 18
CS*	B10	Z1_CS_L	IN 17
MISO	B9	Z1_MISO	IN 17 18 40
MOSI	B8	Z1_MOSI	OUT 17 18
GO	A8	Z1_GO	18
DONE	B7	Z1_DONE	18
PCLK	A12	Z1_PCLK	18
STMOUT	A10		
STMIN	A13	Z1_STMIN	
B_ADR0	A5	Z1_B_ADR<0>	17 40
B_ADR1	B5	Z1_B_ADR<1>	17 40
B_ADR2	A6	Z1_B_ADR<2>	17 40
BON_L0	A2	Z1_BON_L<0>	17
BON_L1	A1	Z1_BON_L<1>	17
BON_L2	A3	Z1_BON_L<2>	17
BON_L3	A4	Z1_BON_L<3>	17
BON_L4	B4	Z1_BON_L<4>	17 40
BON_L5	B3	Z1_BON_L<5>	17 40
TM	A9	U3100_TM	
RESET*	A7	RST_GRAPE_Z1_L	17

R3181 100 1% 1/32W MF 01005

GNDANA — GNDDIG GNDIO

B1 B2 B12 B13 C2 C1 C6 C7 C8 C11 C12 D3 D11 F7 H7 L3 L4 L5 L6 L7 L8 L9 L10 L11 C4 B11

ARM9 MCU (Z2 BASED)

45 Z2_VDDCORE

VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR

C3111 10UF 20% 6.3V CERM-X5R 0402-1

C3109 0.1UF 10% 6.3V X5R 201

VDDANA AND VDDCORE ARE EACH GENERATED WITHIN Z2 AND BYPASSED OUTSIDE

45 Z2_VDDANA

VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR

C3112 2.2UF 20% 4V X5R 402

C3110 0.1UF 10% 6.3V X5R 201

=PP3V0_GRAPE_Z2 35

C3105 0.1UF 10% 6.3V X5R 201

C3107 4.7UF 20% 6.3V X5R-CERM1 402

VOLTAGE=1.8V NET_SPACING_TYPE=PWR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

45 Z2_3V3_1V8_IN

R3190 1.00 1% 1/20W MF 201

Z1_1V8_OUT 18 45

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM VOLTAGE=1.8V NET_SPACING_TYPE=PWR

MIN_NECK_MIDTH SHOULD BE 0.4MM

C3108 0.1UF 10% 6.3V X5R 201

C3106 0.1UF 10% 6.3V X5R 201

C3191 10UF 20% 6.3V CERM-X5R 0402-1

C3192 10UF 20% 6.3V CERM-X5R 0402-1

D2 E1 G8 H2 J5 E2 E3 — VDDANA VDDCORE VDDIO VDDLDO

CRITICAL
U3101
BCM5974CKFBGH
FBGA

R3120 0 5% 1/20W MF 201

Z1_CS_OE 17

Z2 - PRODUCT STRAP OPTIONS

BON_L5	BON_L4	BON_L3	MODE
LOW	X	X	K48
FLOAT	FLOAT	FLOAT	K94
FLOAT	LOW	FLOAT	J2
ALL OTHER STRAPS			CRITICAL ERROR
DEFAULT			J2

B_ADR0	F9		
B_ADR1	F8	Z1_PCLK	18
B_ADR2	G9		
BON_L0	J8	Z1_CS_OE_R	
BON_L1	H9	NC_BON_L1	46
BON_L2	J9	AG_SHLD_TST	17
BON_L3	H7	NC_BON_L3	46
BON_L4	J7		
BON_L5	H5	NC_BON_L5	46
GPIO0	J2	IRQ_GRAPE_HOST_INT_L	OUT 5
GPIO1	J3	PM_BOOST_EN	OUT 17
GPIO2	H4	Z1_GO	18
GPIO3	J6	Z1_DONE	18
GPIO4	G3	GRAPE_CS_L	IN 17
GPIO5	F3	GRAPE_MOSI	IN 17
GPIO6	F4	GRAPE_MISO	OUT 17
GPIO7	H6	GRAPE_SCLK	IN 17
JTAG_TCK	G6	TP_U3101_TCK	
JTAG_TDI	E8	TP_U3101_TDI	
JTAG_TDO	E9	TP_U3101_TDO	
JTAG_TMS	F7	TP_U3101_TMS	
H_CS*	H1	Z2_H_CS_L	IN 17
H_SCLK	J1	Z1_SCLK	IN 17 18
H_SDI	H3	Z1_MISO	IN 17 18 40
H_SDO	J4	Z1_MOSI	OUT 17 18
A_CS*	F1	Z2_A_CS_L	
A_SCLK	G1	TP_Z2_A_SCLK	
A_SDI	F2	TP_Z2_A_SDI	
A_SDO	G4	TP_Z2_A_SDO	
TM0	E7	TP_U3101_TM0	
TM1	D4	U3101_TM1	
CLKIN	E5	HOST_REFCLK	CLK_32K_PMU IN 17 42
CLKOUT	E4	NC	MAKE_BASE=TRUE
INTERNAL PU RESET*	D5	RST_GRAPE_Z2_L	IN 17

R3160 100K 5% 1/20W MF 201

=PP3V0_GRAPE 17 18 35

R3107 100K 5% 1/20W MF 201

R3180 100 1% 1/32W MF 01005

CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

NC	A9	IN0_0	
NC	B9	IN0_1	
NC	A7	IN1_0	
NC	A8	IN1_1	
NC	B8	IN2_0	
NC	C8	IN2_1	
NC	B7	IN3_0	
NC	A7	IN3_1	
NC	A6	IN4_0	
NC	B6	IN4_1	
NC	C6	IN5_0	
NC	C5	IN5_1	
NC	B5	IN6_0	
NC	A5	IN6_1	
NC	A4	IN7_0	
NC	B4	IN7_1	
NC	A3	IN8_0	
NC	B3	IN8_1	
NC	C2	IN9_0	
NC	A2	IN9_1	
NC	B2	IN10_0	
NC	C1	IN10_1	
NC	B1	IN11_0	
NC	A1	IN11_1	
NC	E6	ARMTAPMD*	
	F6	BOOT_CFG0	
	D3	BOOT_CFG1	
NC	G5	FLOO	
NC	F5	LFOO	
NC	G7	EXTFLLIN	

BOOT_CFG0_R

BOOT_CFG1_R

R3173 0 5% 1/20W MF 201

35 18 17 =PP3V0_GRAPE

R3171 0

GND — C3 C4 D6 D7 D8 C9 D9 G2 D1 H8

SYNC_MASTER=RAMSIN SYNC_DATE=12/17/2010

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 31 OF 157

SHEET 18 OF 48

L63B AUDIO CODEC

APN:338S0940

=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
=PP1V7_VA_VCP

C3600 1000PF 10% 6.3V X5R-CERM 01005
C3601 0.1UF 20% 4V X5R 01005
C3602 0.1UF 20% 4V X5R 01005
C3603 10UF 20% 6.3V CERM-X5R 0402-1
C3604 0.1UF 10% 6.3V X5R 201
C3605 27PF 5% 16V NPO-COG 01005
C3606 10UF 20% 4V X5R 402
C3607 0.1UF 20% 4V X5R 01005
C3608 4.7UF 20% 4V TANT 402-3

XW3600 SM
XW3601 SM
XW3602 SM
GND_AUDIO_CODEC

CRITICAL
U3600
CS42L63B
WLCSP-1

I2C ADDRESS: 1001010X??

I2C0_SCL_1V8
I2C0_SDA_1V8
IRQ_CODEC_L
RST_L63_L
AUD_MIK_HS1_INT_L
I2S0_ASP_MCK_R
I2S0_ASP_LRCK
I2S0_ASP_BCLK
I2S0_ASP_DOUT
I2S0_ASP_DIN
I2S2_VSP_LRCK
I2S2_VSP_BCLK
I2S2_VSP_DOUT
I2S2_VSP_DIN
I2S3_XSP_LRCK
I2S3_XSP_BCLK
I2S3_XSP_DOUT
I2S3_XSP_DIN
DMIC_SCLK_SENSOR
DMIC_SD_SENSOR

R3601 22 5% 1/32W MF 01005 — I2S_L63_ASP_SDOUT
R3602 22 5% 1/32W MF 01005 — I2S_L63_VSP_SDOUT
R3603 22 5% 1/32W MF 01005 — I2S_L63_XSP_SDOUT
R3608 22 5% 1/32W MF 01005
R3621 22 5% 1/32W MF 01005

SCL
SDA
INT*
RESET*
WAKE*
MCLK
ASP_LRCLK
ASP_SCLK
ASP_SDIN
ASP_SDOUT
VSP_LRCLK
VSP_SLCLK
VSP_SDIN
VSP_SDOUT
XSP_LRCLK
XSP_SCLK
XSP_SDIN/DAC2B_MUTE
XSP_SDOUT
DMIC_SCLK
DMIC_SD
LINEINA
LINEINA_REF
LINEINB
LINEINB_REF
MIC1_BIAS
MIC1
MIC1_REF
MIC1_BIAS_FILT
MIC2_BIAS
MIC2_DETECT
MIC2
MIC2_REF
MIC2_DETECT_REF
MIC2_BIAS_FILT
MIC3A_BIAS
MIC3A
MIC3A_REF
MIC3A_BIAS_FILT
MIC3B_BIAS
MIC3B
MIC3B_REF
MIC3B_BIAS_FILT

DMIC_SCLK_CODEC
DMIC_SD_CODEC
NC_LINE_IN1_CODEC
NC_LINE_IN1_REF_CODEC
NC_LINE_IN2_CODEC
NC_LINE_IN2_REF_CODEC
NC_MIC1_BIAS_CODEC
NC_MIC1P_CODEC
NC_MIC1N_CODEC
NC_MIC1_FILT_CODEC

HP_DETECT
HPOUTB
HPOUTA
HPOUT_REF
LINEOUT1B
LINEOUT1A
LINEOUT1_REF
LINEOUT2A
LINEOUT2A_REF
LINEOUT2B
LINEOUT2B_REF
EAROUT+
EAROUT-
SPEAKEROUTA+
SPEAKEROUTA-
SPEAKEROUTB+
SPEAKEROUTB-
FLYP
FLYC
FLYN
SPEAKER_VQ
FILT+

HP_DET
HP_R
HP_L
HP_REF
CODEC_LINE_OUT_R
CODEC_LINE_OUT_L
CODEC_LINE_OUT_REF
LEFT_CH_OUT_P
LEFT_CH_OUT_REF
RIGHT_CH_OUT_P
RIGHT_CH_OUT_REF
NC_EAROUT_AP
NC_EAROUT_AN

C3617 2.2UF 20% 10V X5R-CERM 402
C3618 2.2UF 20% 10V X5R-CERM 402
VHP_FLYC
VHP_FLYN
SPKR_VQ
FILT_POS

NOT USING SPEAKER AMPLIFIER WITH SPEAKER LOAD.

+VCP_FILT
-VCP_FILT
VHPPFILT
VHPNFILT

C3609 4.7UF 20% 6.3V X5R-CERM1 402
C3611 4.7UF 20% 6.3V X5R-CERM1 402
C3613 10UF 20% 6.3V CERM-X5R 0402-1
C3614 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C3615 4.7UF 20% 6.3V X5R-CERM1 402
2.2UF RECOMMENDED CRITICAL C3616 4.7UF 20% 6.3V X5R-CERM1 402

GNDD GNDA GNDCP GNDP GND

EXT_MIC_BIAS
HSMIC_C_P
EXT_MIC_P
EXT_MIC_REF
HSMIC_C_N

R3604 1.00K 1% 1/32W MF 01005
R3605 1.00K 1% 1/32W MF 01005

GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=75 MM

MIN_LINE_WIDTH=1.0MM
MIN_NECK_WIDTH=0.2MM

GND_AUDIO_HP_AMP

SYNC_MASTER=KAVITHA SYNC_DATE=02/03/2011

PAGE TITLE: AUDIO: L63B CODEC

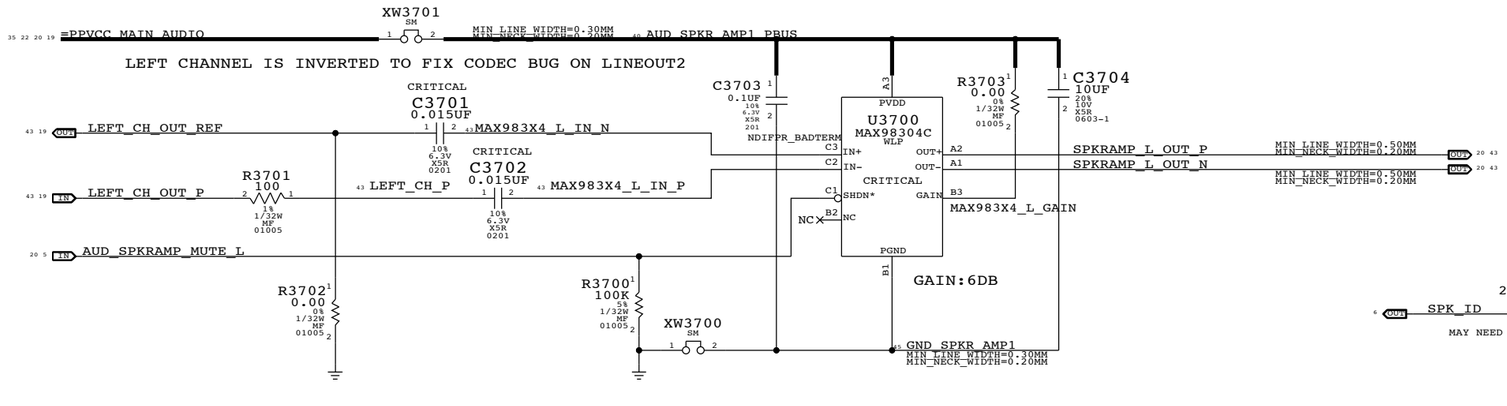
Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D
REVISION: 10.0.0
BRANCH:
PAGE: 36 OF 157
SHEET: 19 OF 48

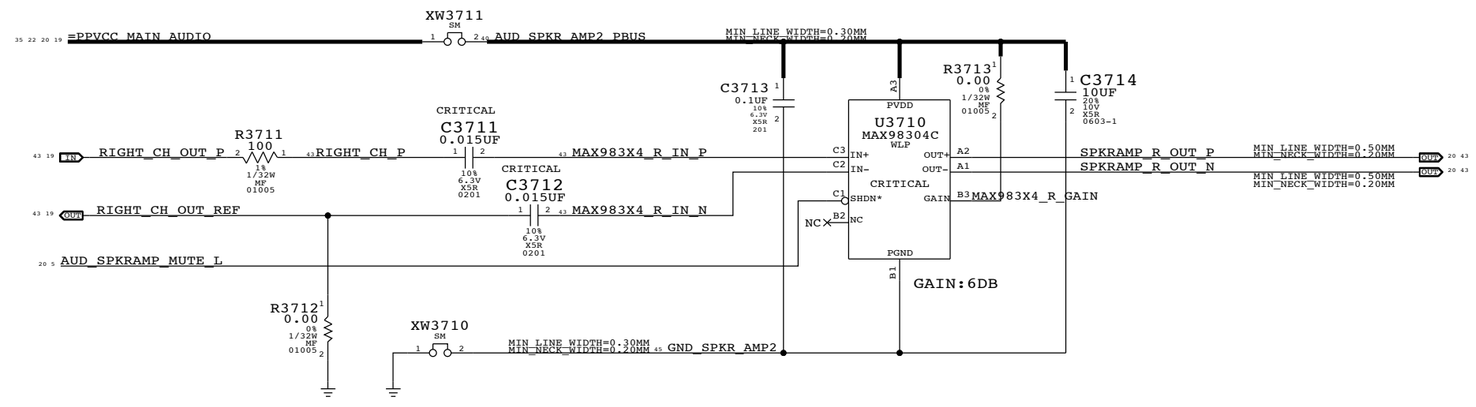
SPEAKER AMPLIFIER

APN:353S3317)
TURN ON TIME: 3.5MS
75HZ +/- XXX% TURN ON DELAY: ?MS

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

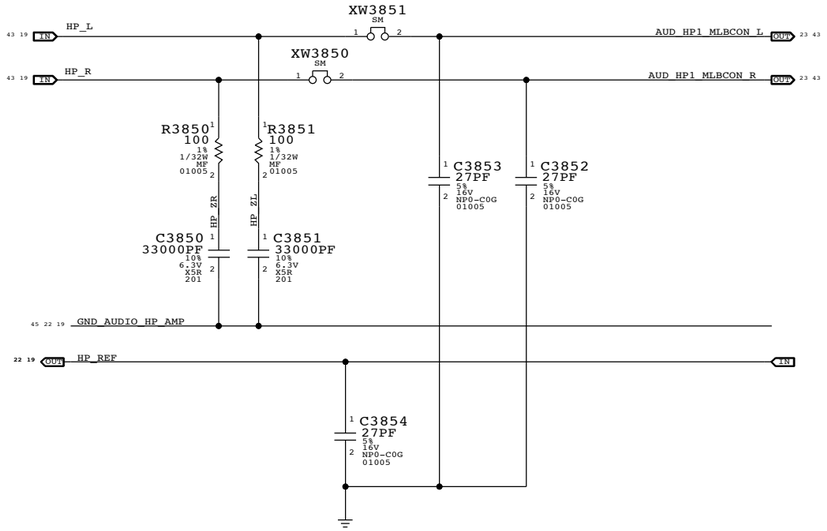


L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710

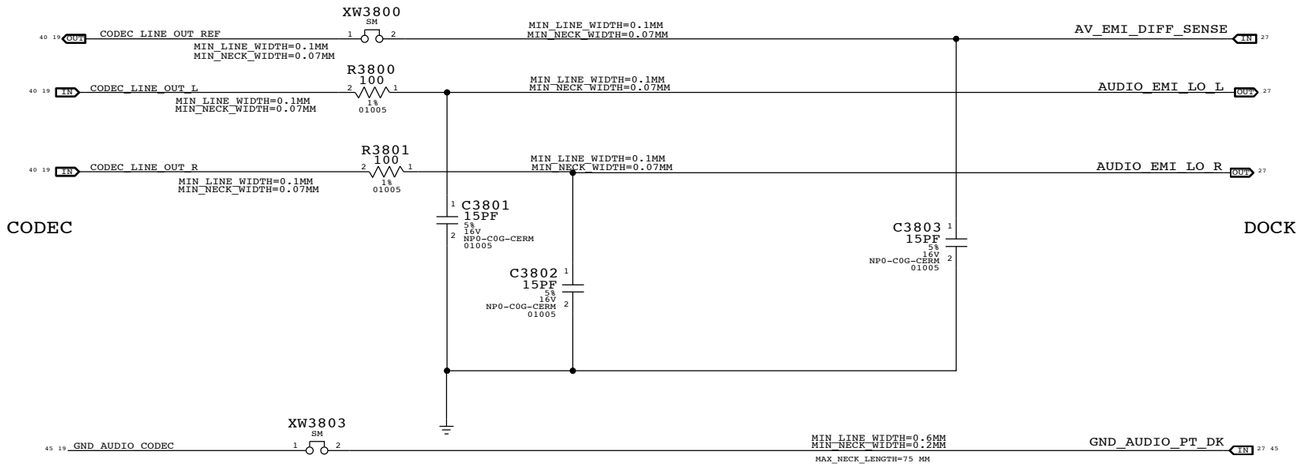


SYNC MASTER=KAVITHA	SYNC DATE=02/03/2011
PAGE TITLE	AUDIO: SPEAKER AMP
Apple Inc.	DRAWING NUMBER 051-8773 SIZE D
	REVISION 10.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE 37 OF 157
	SHEET 20 OF 48

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC_MASTER=KAVITHA SYNC_DATE=02/03/2011

PAGE TITLE

AUDIO: HEADPHONE OUT

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

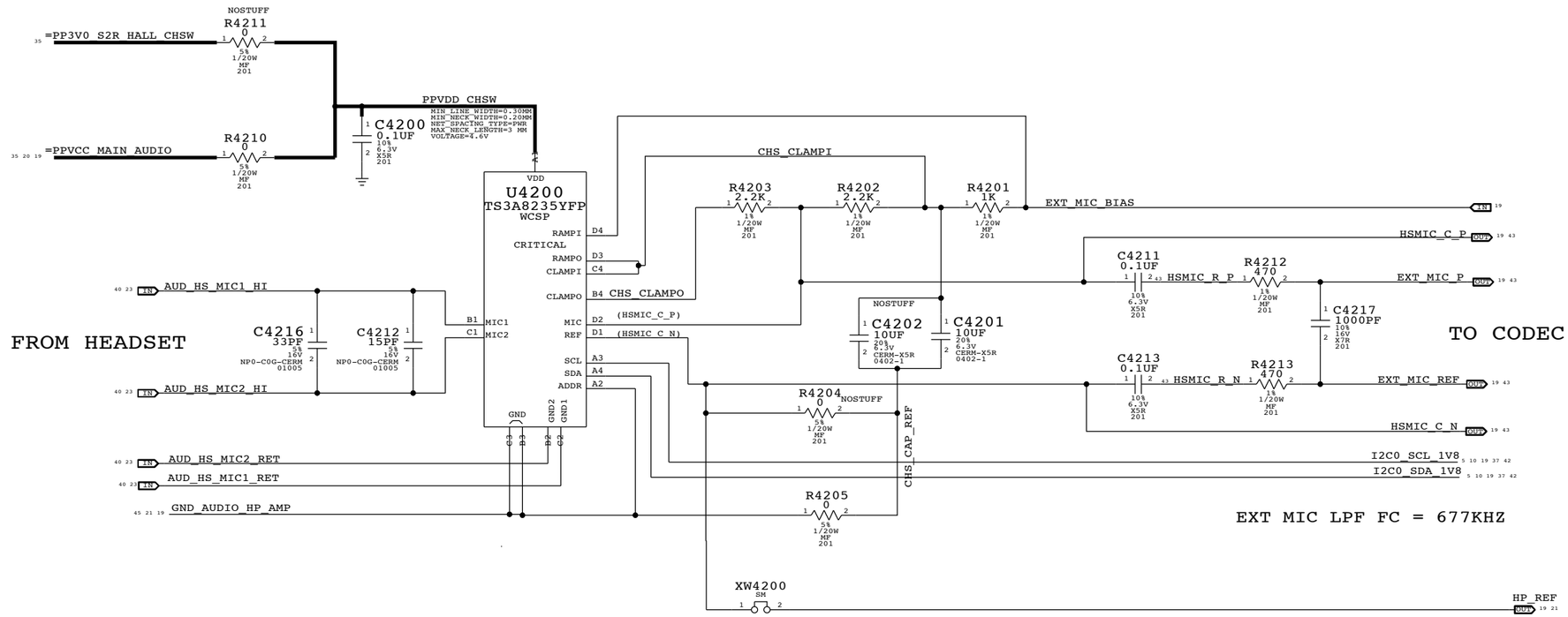
REVISION 10.0.0

BRANCH

PAGE 38 OF 157

SHEET 21 OF 48

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



SYNC_MASTER=KAVITHA SYNC_DATE=02/03/2011

PAGE TITLE

AUDIO: DETECT/MIC BIAS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

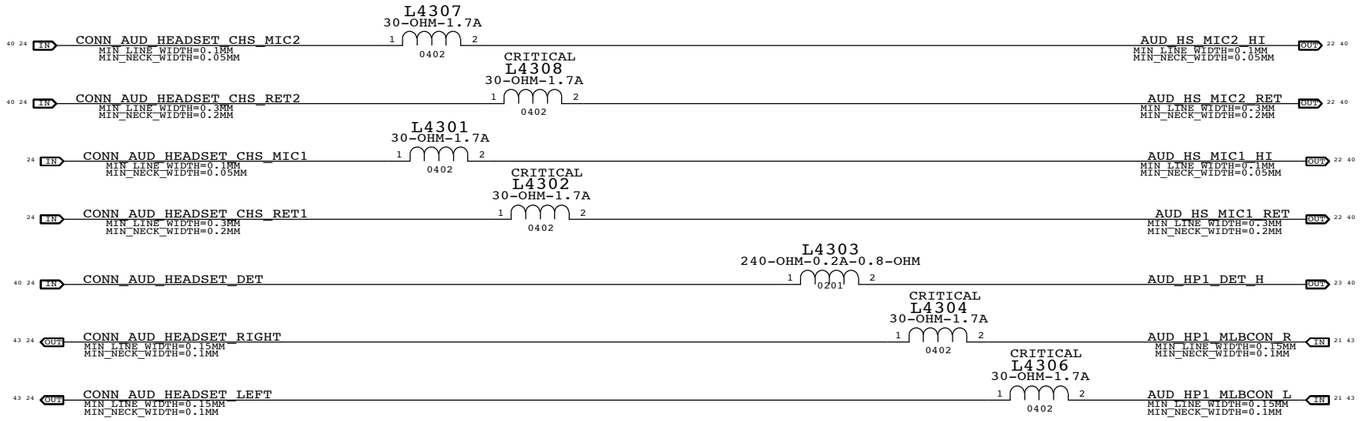
BRANCH

PAGE 42 OF 157

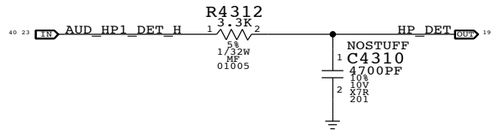
SHEET 22 OF 48

HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29

PLACE ALL COMPONENTS NEAR J5401



HEADSET JACK INSERTION DETECT



SYNC_MASTER=KAVITHA SYNC_DATE=02/03/2011

PAGE TITLE

AUDIO: HP/MIC FILTERS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 43 OF 157

SHEET 23 OF 48

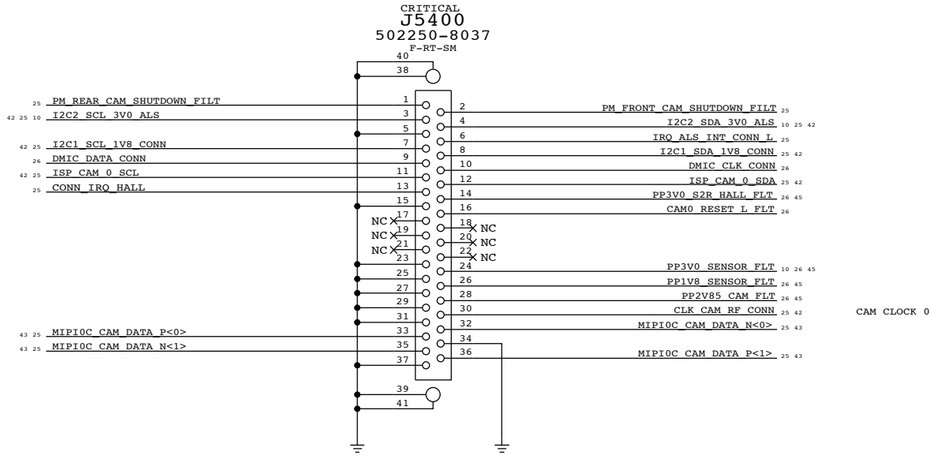
APN: 518S0828

CRITICAL

J5400

502250-8037

F-RT-SM



CAM CLOCK 0

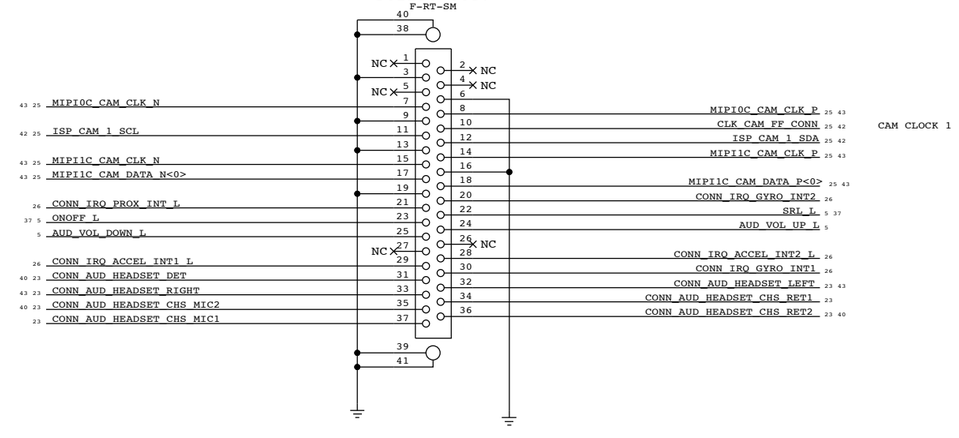
APN: 518S0828

CRITICAL

J5401

502250-8037

F-RT-SM



CAM CLOCK 1

SYNC_MASTER=MARK SYNC_DATE=01/11/2011

PAGE TITLE

CONNECTOR: SENSOR

Apple Inc.

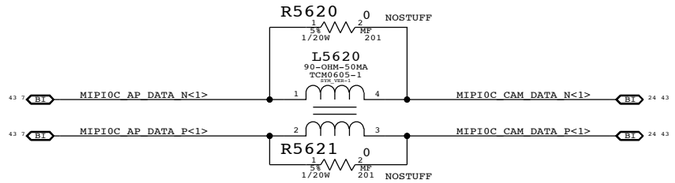
DRAWING NUMBER 051-8773 SIZE D

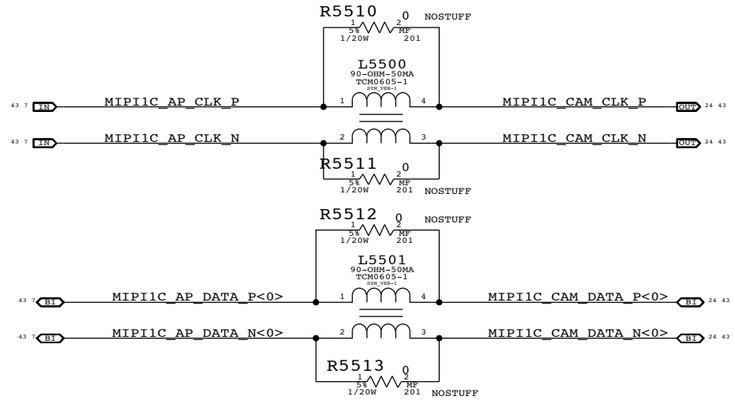
REVISION 10.0.0

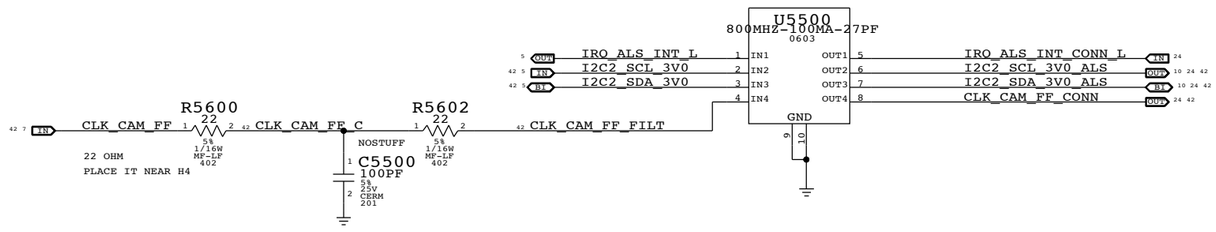
BRANCH

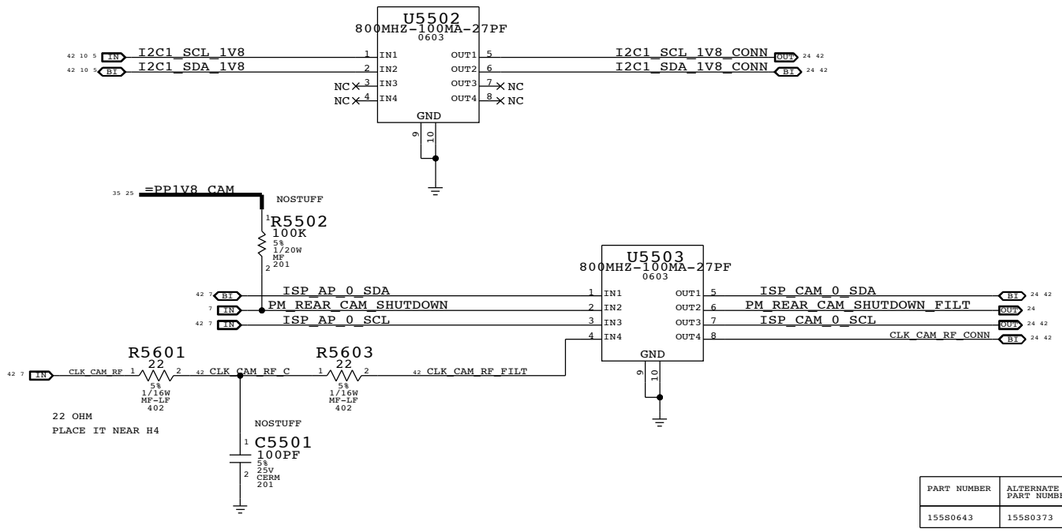
PAGE 54 OF 157

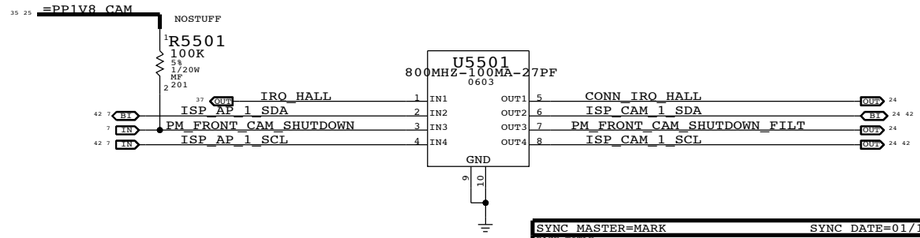
SHEET 24 OF 48











PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0643	155S0373	?	U5502,U5503,U5501,U5500,U5601	RADAR:8376668

SYNC_MASTER=MARK SYNC_DATE=01/11/2011

PAGE TITLE

SENSOR PANEL FILTERS 1

Apple Inc.

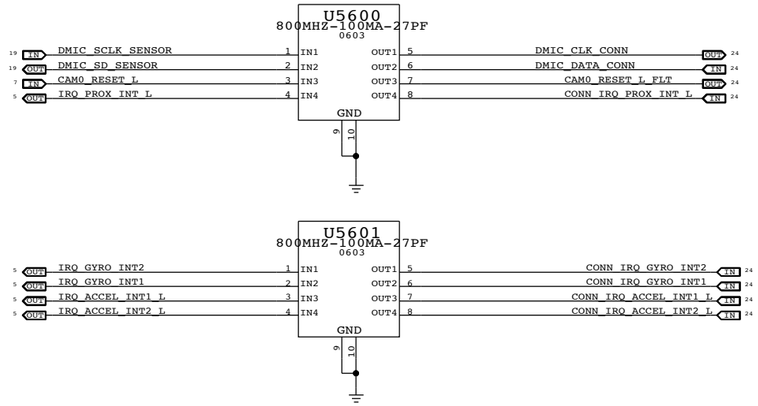
DRAWING NUMBER 051-8773 SIZE D

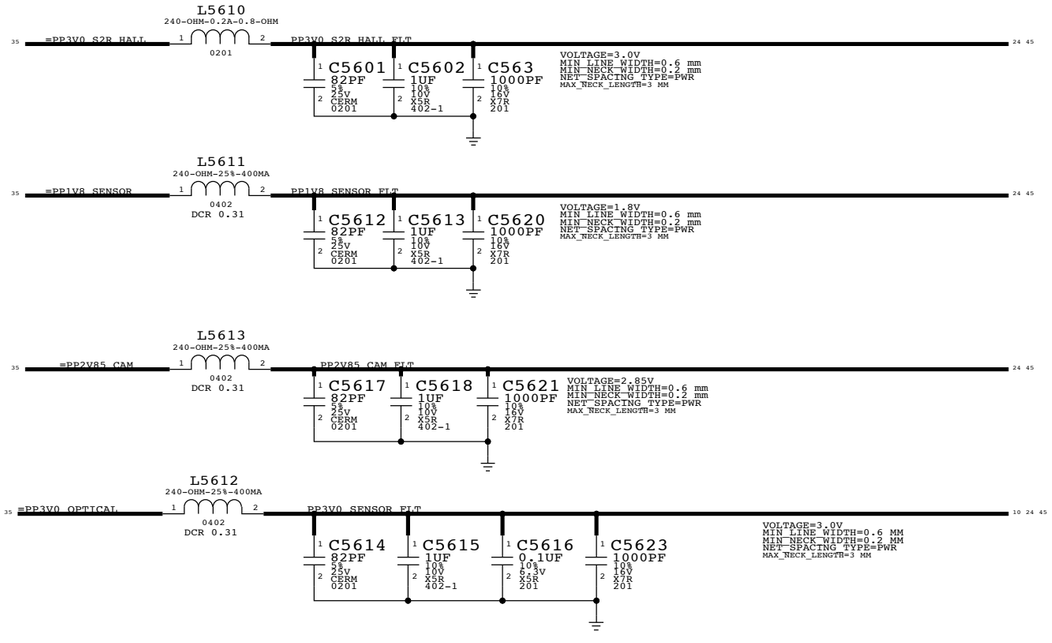
REVISION 10.0.0

BRANCH

PAGE 55 OF 157

SHEET 25 OF 48





SYNC MASTER=MARK SYNC DATE=01/11/2011

PAGE TITLE

SENSOR PANEL FILTERS 2

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

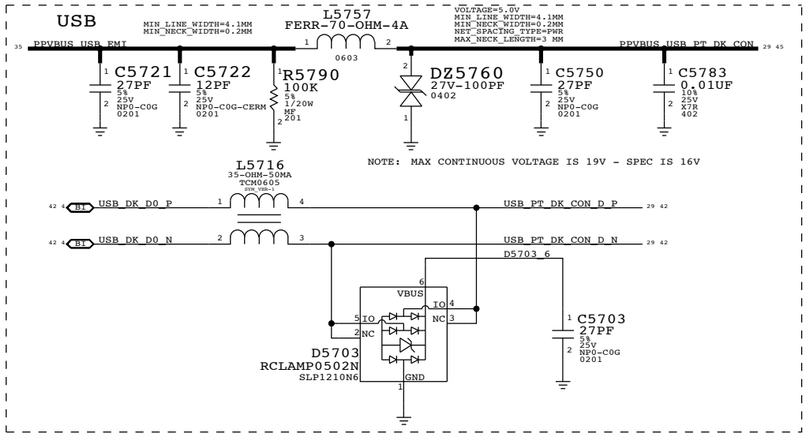
REVISION 10.0.0

BRANCH

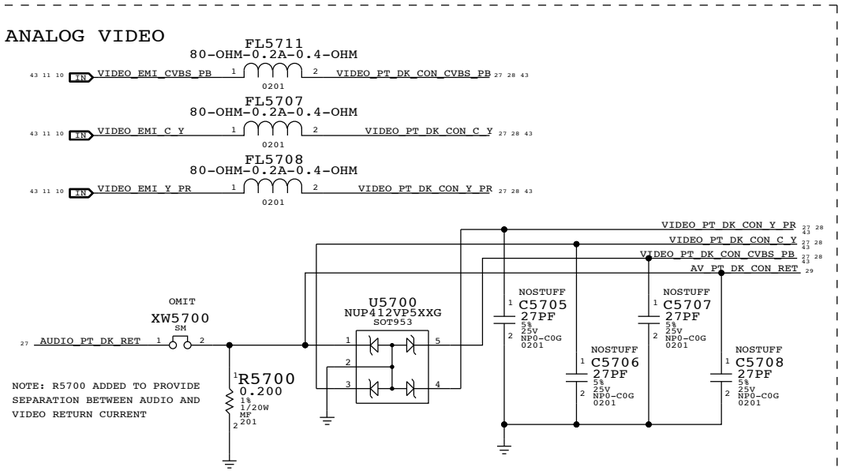
PAGE 56 OF 157

SHEET 26 OF 48

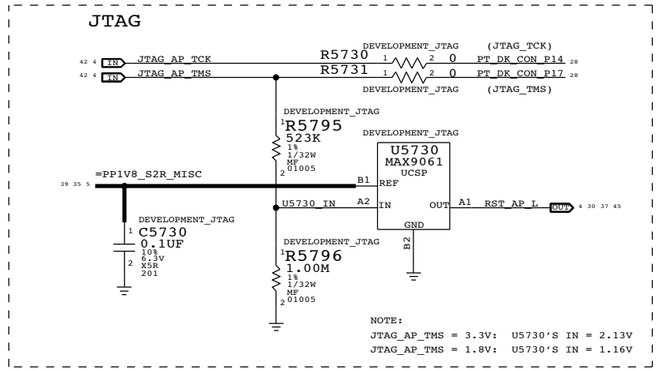
USB



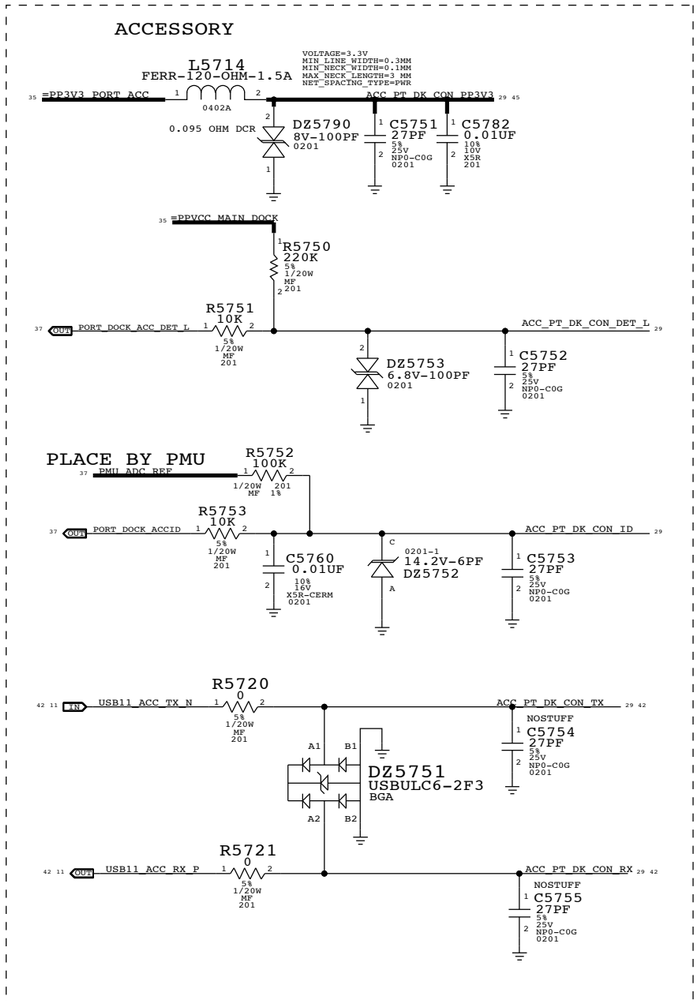
ANALOG VIDEO



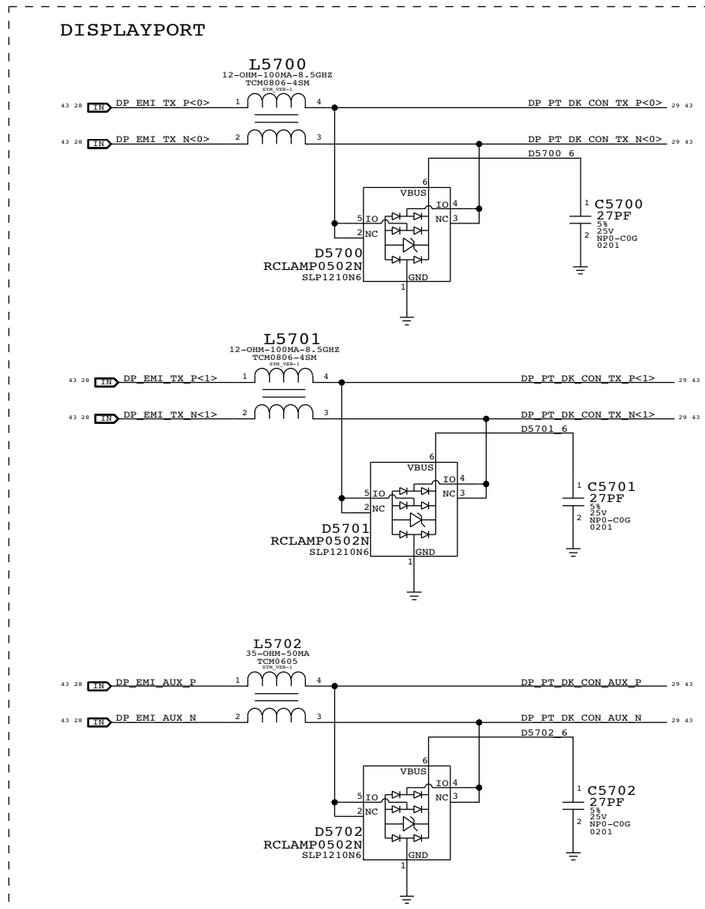
JTAG



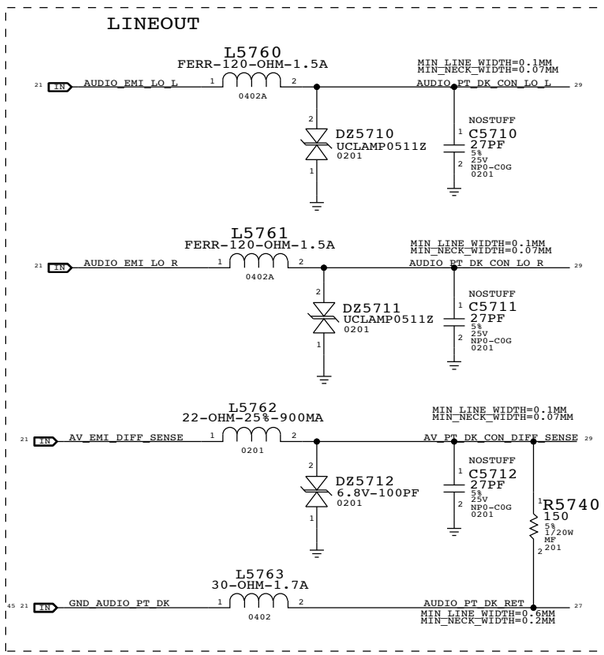
ACCESSORY



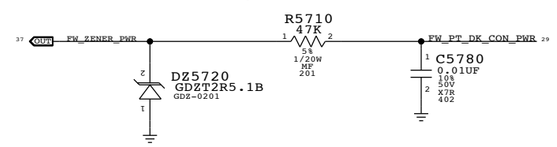
DISPLAYPORT



LINEOUT



FIREWIRE DETECT/ DISPLAYPORT HPD



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	RADAR:8972666
377S0111	377S0099		DZ5710,DZ5711	RADAR:8849707
377S0107	377S0066		D5700,D5701,D5702,D5703	RADAR:8947642
155S0625	155S0559		L5700,L5701	RADAR:8423156
377S0116	377S0108		DZ5760	RADAR:8370432
155S0725	155S0276		FL0609, FL5707, FL5708, FL5711	QTY 4 RADAR:9625553
155S0513	155S0320		L5762	RADAR:9625601

SYNC_MASTER=JOE SYNC_DATE=01/19/2011

PAGE TITLE

IO FLEX: DOCK COMPONENTS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

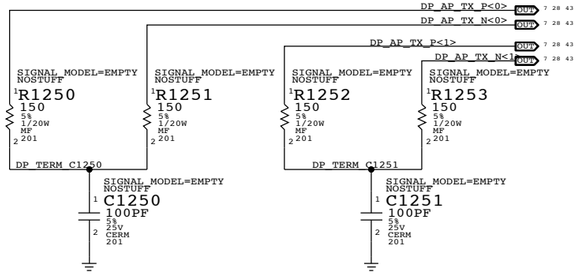
REVISION 10.0.0

BRANCH

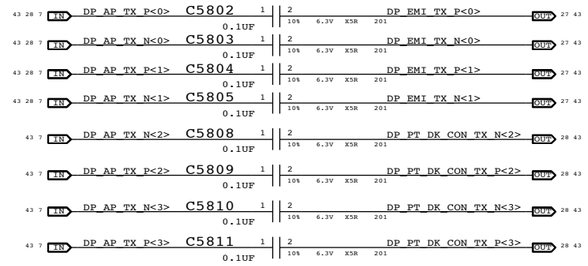
PAGE 57 OF 157

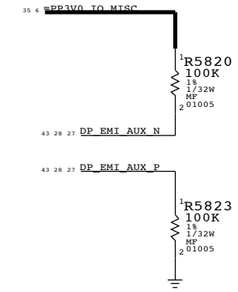
SHEET 27 OF 48

PLACEMENT NOTE: NEAR U0600

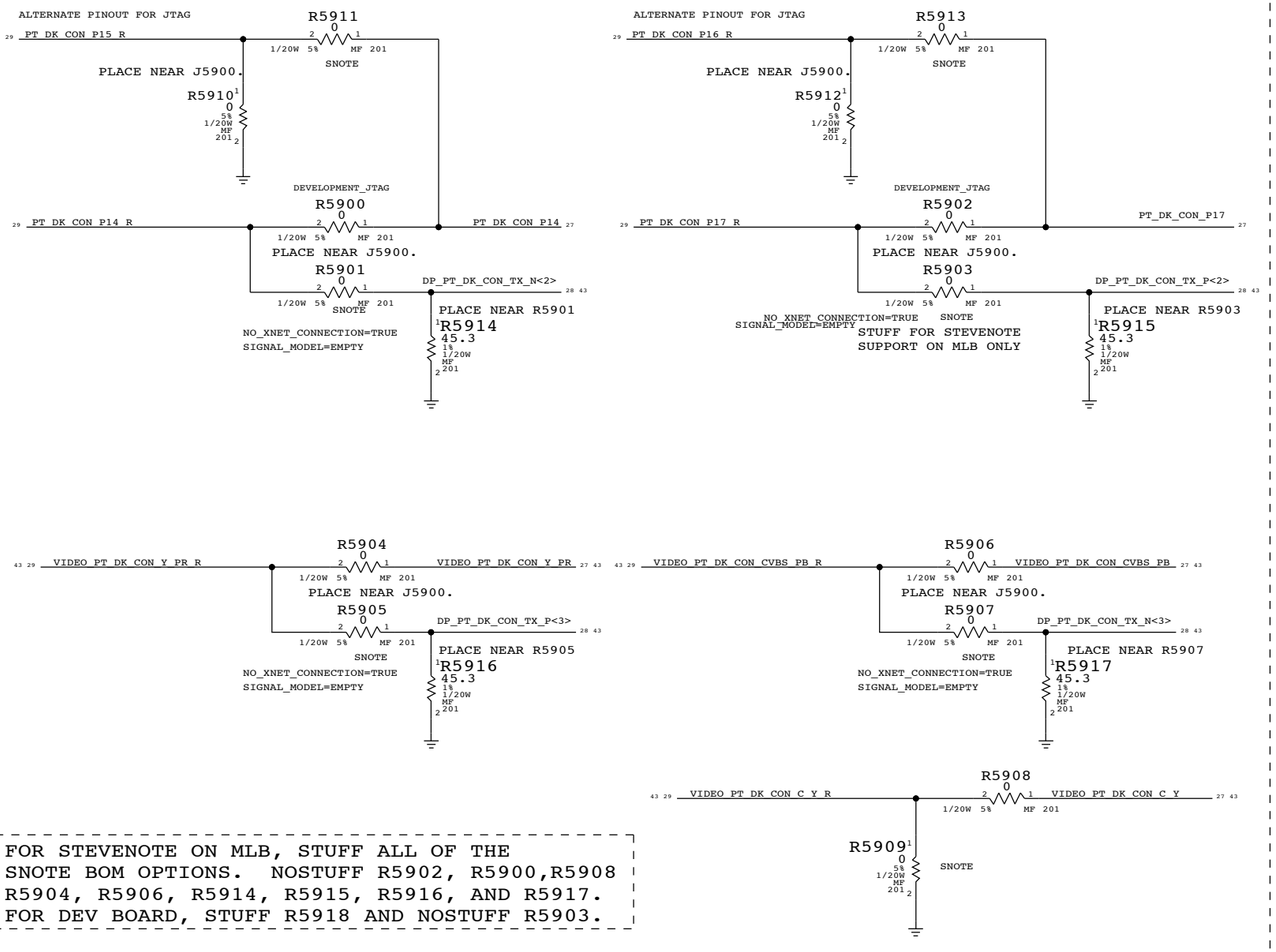


DISPLAYPORT AC COUPLING

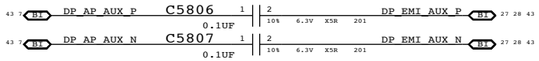


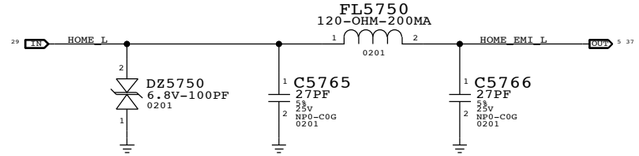


STUFFING OPTIONS FOR DP LANES 2, 3 FOR STEVENOTE.



FOR STEVENOTE ON MLB, STUFF ALL OF THE SNOTE BOM OPTIONS. NOSTUFF R5902, R5900,R5908 R5904, R5906, R5914, R5915, R5916, AND R5917. FOR DEV BOARD, STUFF R5918 AND NOSTUFF R5903.





SYNC_MASTER=JOE SYNC_DATE=01/19/2011

PAGE TITLE: DISPLAY PORT MISC

Apple Inc.

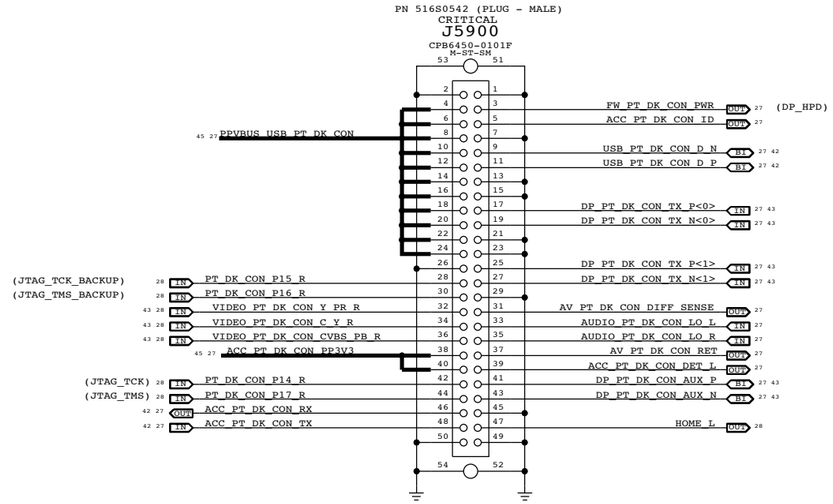
DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

BRANCH:

PAGE: 58 OF 157

SHEET: 28 OF 48



SYNC_MASTER=JOE SYNC_DATE=01/19/2011

PAGE TITLE

IO FLEX: B2B CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

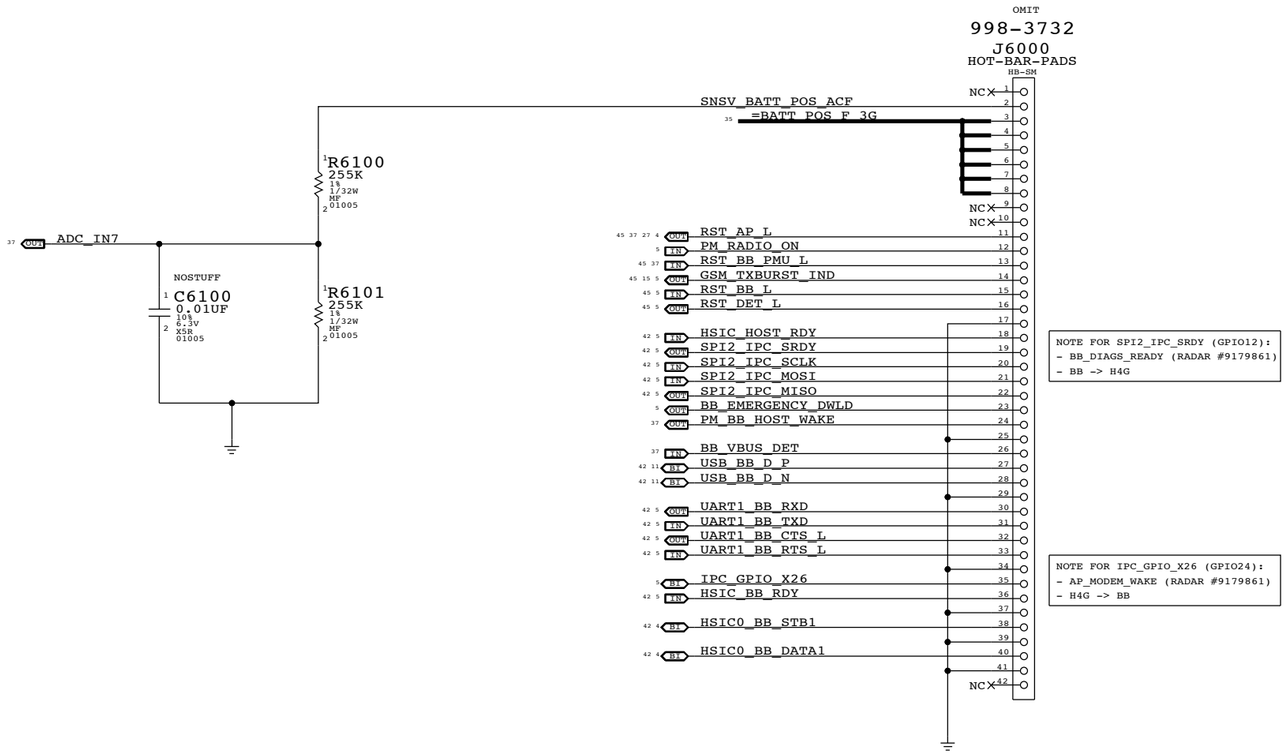
REVISION 10.0.0

BRANCH

PAGE 59 OF 157

SHEET 29 OF 48

X26 CELLULAR/GPS CONNECTOR



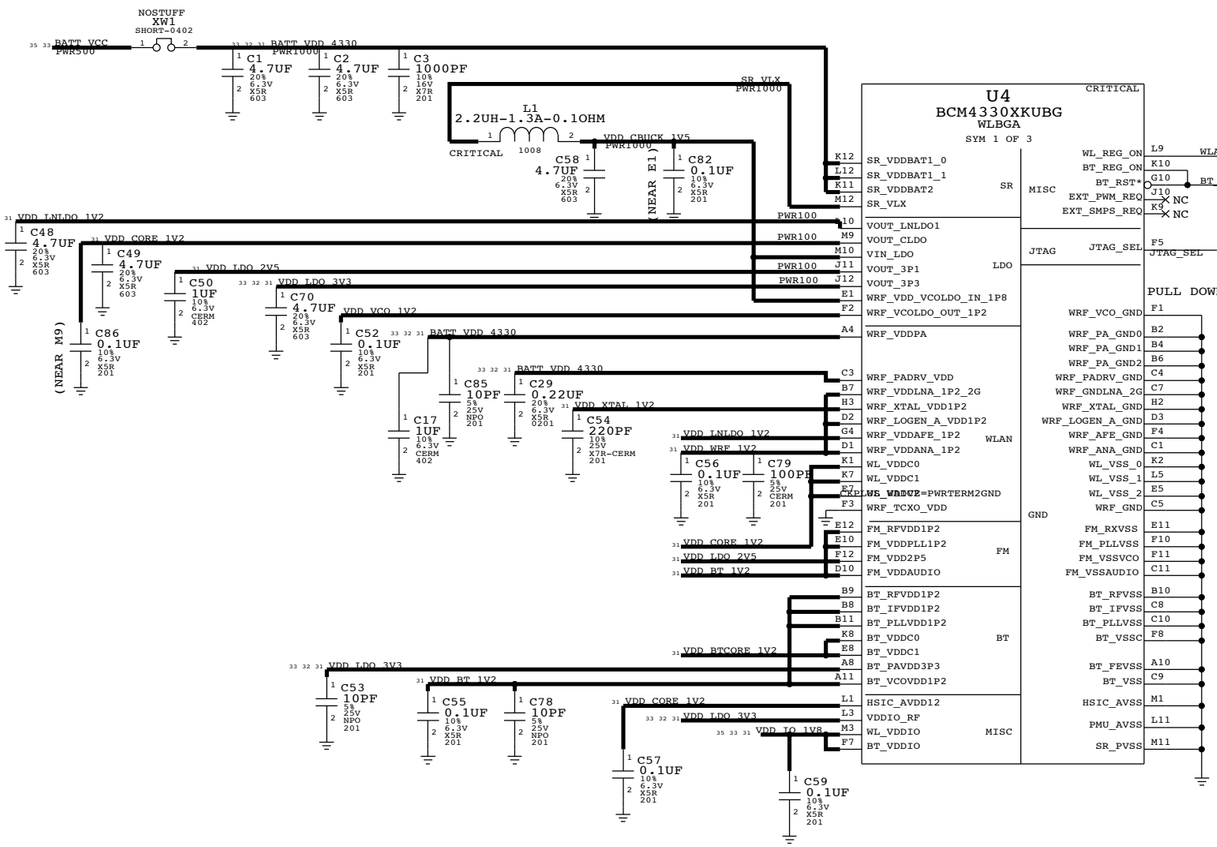
SYNC_MASTER=JOE SYNC_DATE=01/19/2011

PAGE TITLE
CONNECTOR: X26

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 60 OF 157
SHEET 30 OF 48

WLAN/BT POWER



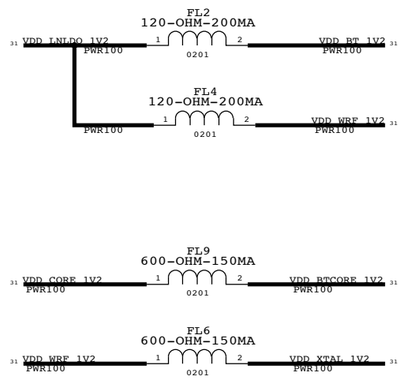
BOOTSTRAPPING OPTIONS

GPIO6	SDIO_DATA2	SDIO_DATA1	MODE	DEF.ARM STATE
0	X	X	SDIO	RESET
1	0	X	GSPI	RESET
1	1	0	HSIC	RUNNING
1	1	1	BOOTLOADERLESS HSIC	RUNNING

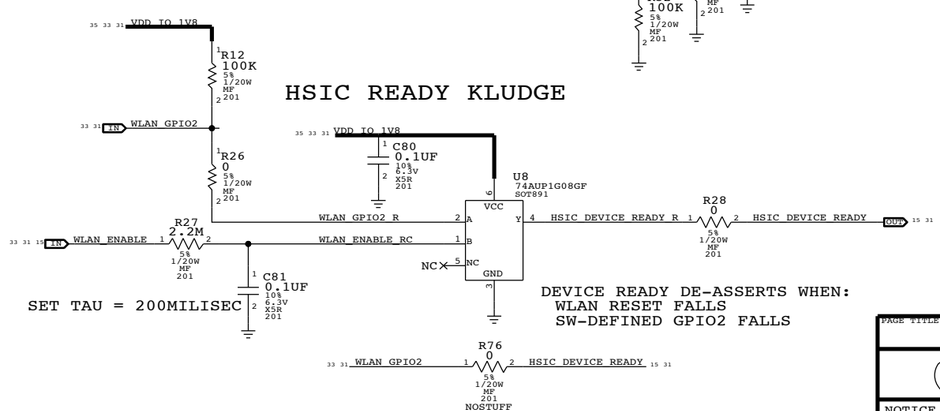
ALTERNATE PARTS AVAILABLE:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0548	311S0398	ANDGATE_TI	U8	TI
155S0657	155S0537	FERRITE_TY	FL2,FL4	TAIYO YUDEN
155S0337	155S0444	FERRITE_TDK	FL6,FL9	TDK

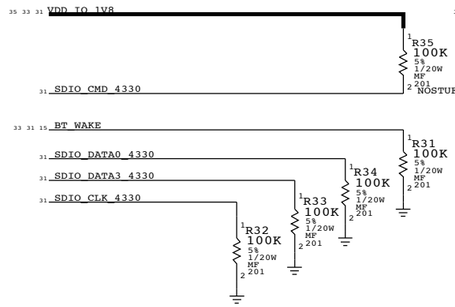
SUPPLY FILTERING



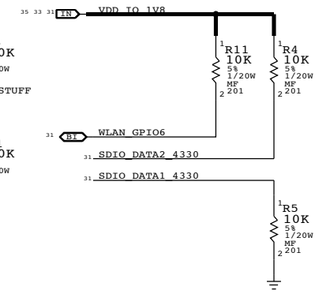
HSIC READY KLUDGE



PULL-UP/DOWN RESISTORS



BOOTSTRAP RESISTORS

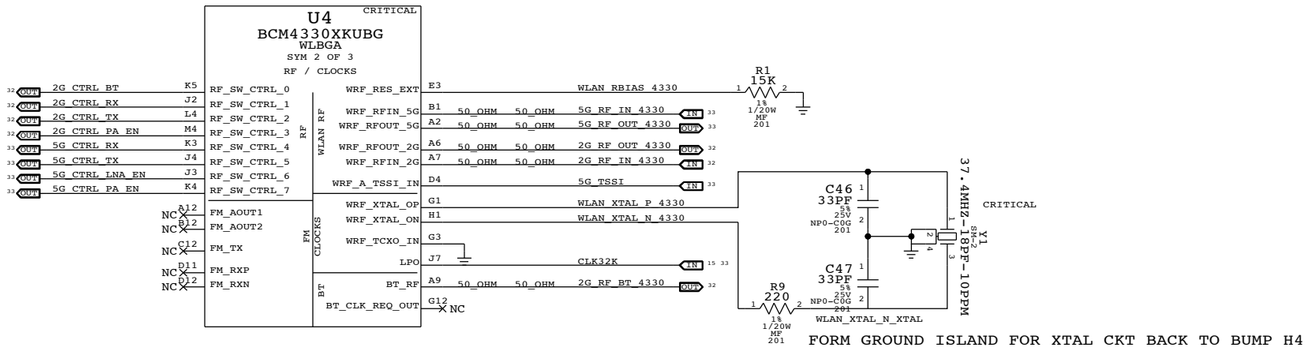


PAGE TITLE	WLAN BB & POWER
Apple Inc.	DRAWING NUMBER 051-8773 · SIZE D
	REVISION 10.0.0
	BRANCH
	PAGE 61 OF 157
	SHEET 31 OF 48

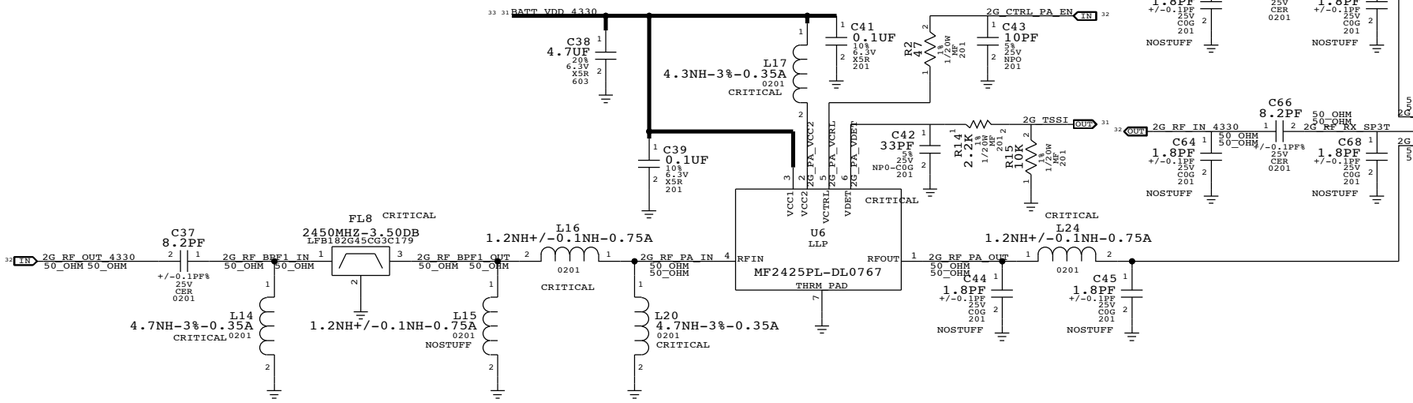
WLAN TRANSCEIVER

RF I/O PLAN

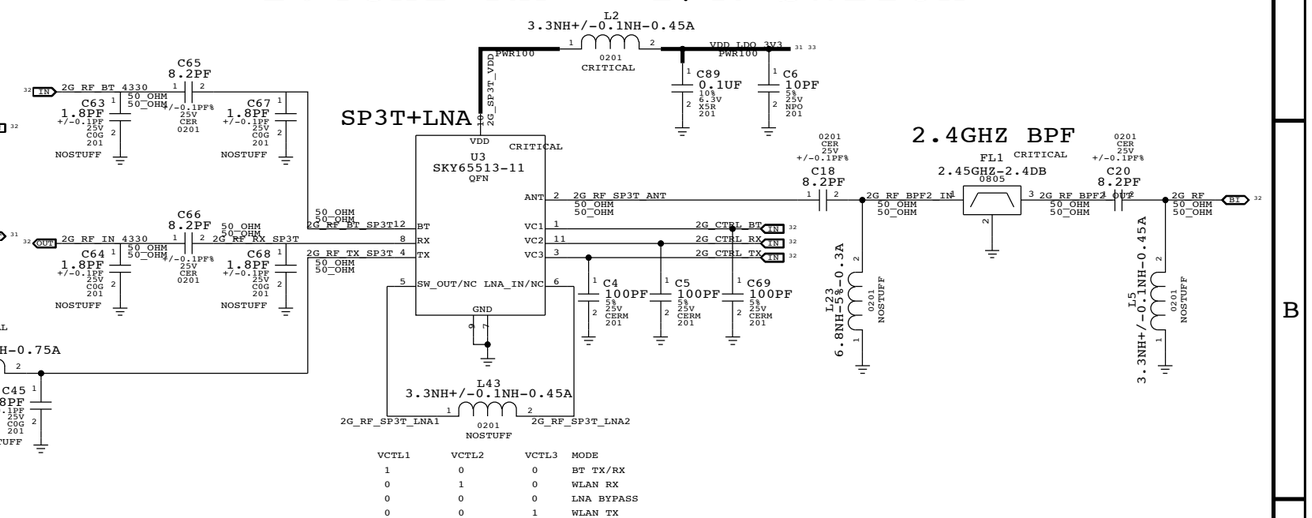
RF_SW_CTRL_0: 2G_CTRL_BT
RF_SW_CTRL_1: 2G_CTRL_RX
RF_SW_CTRL_2: 2G_CTRL_TX
RF_SW_CTRL_3: 2G_CTRL_PA_EN
RF_SW_CTRL_4: 5G_CTRL_RX
RF_SW_CTRL_5: 5G_CTRL_TX
RF_SW_CTRL_6: 5G_CTRL_LNA_EN
RF_SW_CTRL_7: 5G_CTRL_PA_EN



2.4GHZ TX



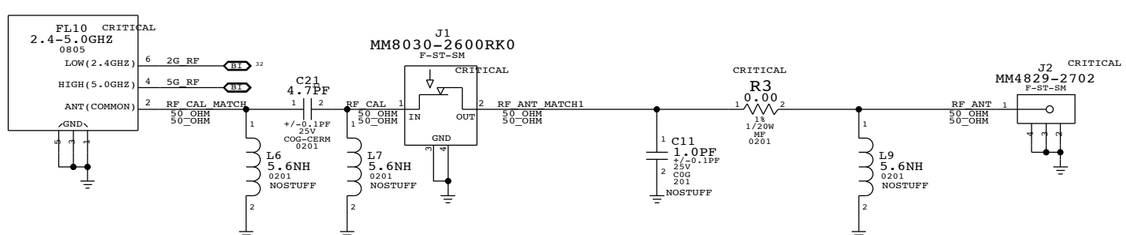
2.4GHZ RX + T/R SWITCH



2.4GHZ/5GHZ DIPLEXER

CONDUCTED TEST PORT

ANTENNA CONNECTOR

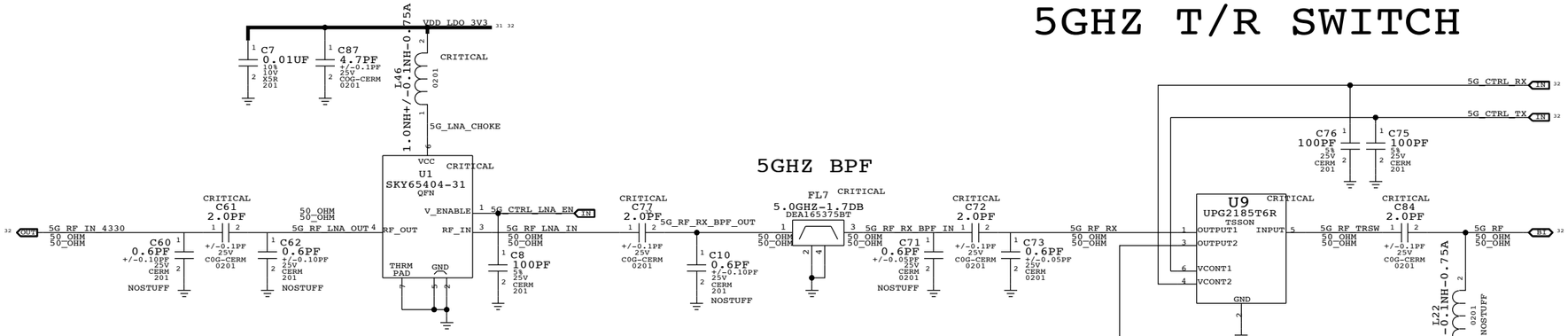


PAGE TITLE	
WLAN 2.4GHZ AND ANT	
Apple Inc.	DRAWING NUMBER 051-8773 SIZE D
	REVISION 10.0.0
	BRANCH
	PAGE 62 OF 157
	SHEET 32 OF 48

5GHZ FRONT-END CONTROL

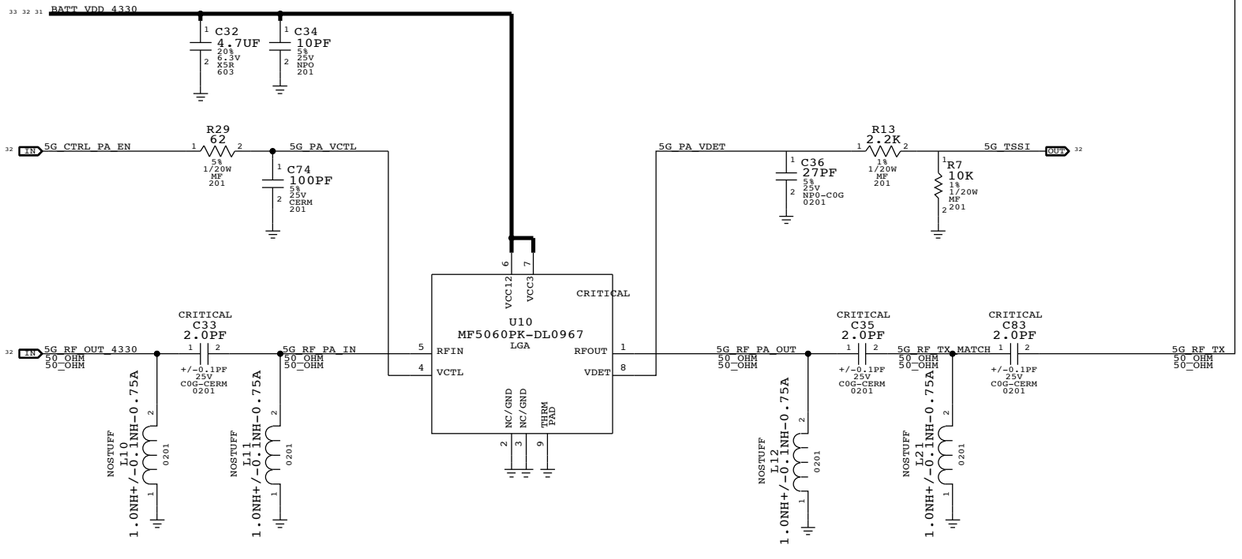
VCRL1	VCTL2	PA_EN	LNA_EN	MODE
1	0	0	1	RX SUPERBYPASS MODE -- 26DB GAIN STEP
0	1	0	1	RX
1	0	1	0	TX

5GHZ LNA



5GHZ T/R SWITCH

5GHZ PA



TEST POINTS

TEST AND PROBE POINTS

TP1 WLAN_ENABLE
TP7 WLAN_GPIO0
TP3 WLAN_GPIO1
TP4 WLAN_GPIO2
TP5 WLAN_GPIO3
TP10 WLAN_GPIO4
TP6 CLK32K
PP29 HSIC_DATA 4330
PP30 HSIC_STROBE 4330

TP2 BT_RESET_N
TP26 BT_UART_TXD
TP27 BT_UART_RXD
TP28 BT_UART_RTS_N
TP29 BT_UART_CTS_N
TP8 BT_HOST_WAKE
TP9 BT_WAKE

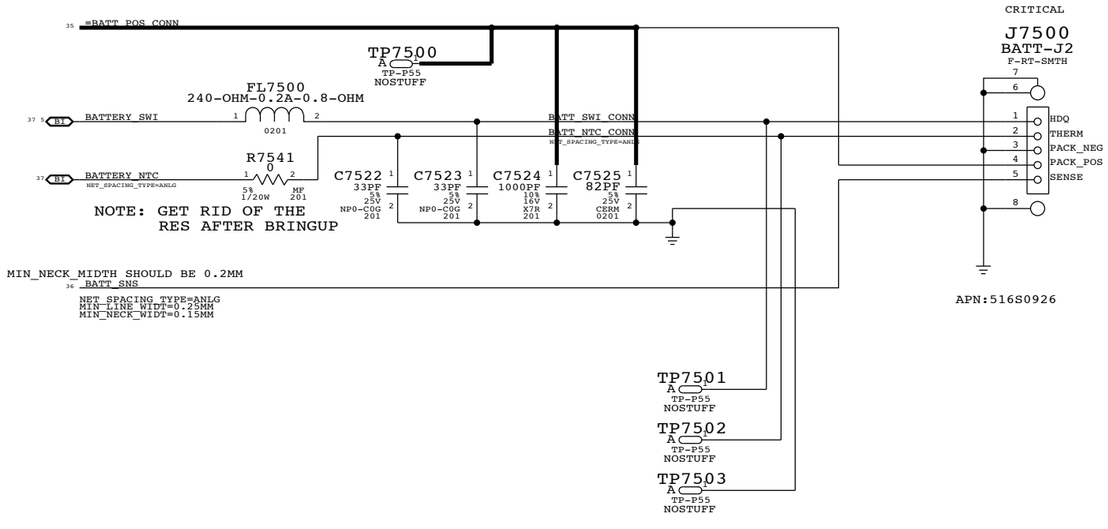
TP15 BATT_VCC
TP16 BATT_VDD_4330
TP17 VDD_IO_1V8
TP18
TP19

All: TP-P6 NOSTUFF; TP-1P0-TOP NOSTUFF

PAGE TITLE
WLAN 5GHZ AND TEST POINTS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 63 OF 157
SHEET 33 OF 48



SYNC_MASTER=MADHAVI SYNC_DATE=01/13/2011

PAGE TITLE

POWER: BATTERY CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 75 OF 157

SHEET 34 OF 48

POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

LDO1
45 36 PP3V0_GRAPE
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_GRAPE 17 18
→ =PP3V0_GRAPE_MARIO1 17
→ =PP3V0_GRAPE_Z1 18
→ =PP3V0_GRAPE_Z2 18

LDO2
45 40 36 PP1V7_VA_VCP
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V7_VA_VCP 19

LDO3
45 36 PP3V0_VIDEO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_H4 7

LDO4
45 36 PP3V0_OPTICAL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_OPTICAL 26

LDO5
45 36 PP3V2_LDO5
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V2_LDO5

LDO6
45 36 PP3V3_ACC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_PORT_ACC 27

LDO7
45 36 PP3V0_VIDEO_BUF
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_BUF 11

LDO8
45 36 PP3V2_S2R_USBMUX
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V2_S2R_USBMUX 11

LDO9
45 36 PP3V0_IO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_IO_MISC 6 28
→ =PP3V0_IO_H4 7 9
→ =PP3V0_VDDIOD_H4 9

LDO10
45 36 PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_S2R_HALL 26
→ =PP3V0_S2R_HALL_CHSW 22

LDO11
45 36 PP2V85_CAM
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP2V85_CAM 26

LDO12
45 36 PP1V1
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V1_PLL_H4 4
→ =PP1V1_MIPI_H4 7
→ =PP1V1_DP_PAD_DVDD_H4 7
→ =PP1V1_USB_H4 4
→ =PP1V1_HSIC_H4 4
→ =PP1V1_MIPI_PLL_H4 4
→ =PP1V1_EDP_PAD_DVDD_H4 7

45 36 PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_ALWAYS 5

BUCK RAILS

BUCK0
45 36 PP1V25_CPU
MAKE_BASE=TRUE
VOLTAGE=1.25V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVDD_CPU_H4 9

BUCK2
45 36 PP1V2_SOC
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVDD_SOC_H4 9

BUCK3
45 36 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S2R_MISC 5 27 39
→ VDD_IO_1V8 31 33
→ =PP1V8_S2R_DDR 13 14

CPU1V8_SW (BUCK3)
36 45 PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_CAM 25
→ =PP1V8_SENSOR 26
→ =PP1V8_DP_H4 7
→ =PP1V8_AUDIO 19
→ =PP1V8_H4 4 7 10
→ =PP1V8_NAND_H4 9
→ =PP1V8_MIPI_H4 7
→ =PP1V8_NAND 12
→ =PP1V8_VDDIO18_H4 9
→ =PP1V8_EDP_H4 7
→ =PP1V8_VDDIOD_H4 5 9
→ =PP1V8_VDDA18_TS 5

WDIG_SW (BUCK3)
45 36 PP1V8_GRAPE
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_GRAPE

BUCK4
45 36 PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V2_S2R_H4 8
→ =PP1V2_S2R_DDR 13 14

BUCK4_SW
45 36 PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V2_VDDIOD_H4 8 9
→ =PP1V2_HSIC_H4 4
→ =PP1V2_VDDQ_DDR 13 14

BUCK5
45 36 PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
→ =PP3V3_NAND 12
→ =PP3V3_USB_H4 4
→ =PP3V3_NAND_H4 9
→ =PP3V3_LCD 16

VOUT_LED_A
45 37 PPLED_OUT_A
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPLED_REG_A 16

VOUT_LED_B
45 37 PPLED_OUT_B
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPLED_REG_B 16

CHARGER MAIN

45 37 36 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVCC_MAIN_LED 37
→ =PPVCC_MAIN_AUDIO 19 20 22
→ =PPVCC_MAIN_DOCK 27

BATTERY

45 39 36 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =BATT_POS_F_3G 30
→ =BATT_POS_CONN 34
→ BATT_VCC 31 33 USED BY WIFI_BT

USB POWER INPUT

27 PPVBUS_USB_EMI
→ PPVBUS_USB_DCIN 36 45
MAKE_BASE=TRUE

LCM_BOOST

45 37 PP5V25_VLCM2
MAKE_BASE=TRUE
VOLTAGE=5.25V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP5V25_GRAPE_VDDH

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.15MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

SYNC_MASTER=MADHAVI SYNC_DATE=01/13/2011
PAGE TITLE
POWER ALIASES

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 80 OF 157
SHEET 35 OF 48

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299	?	Y8138	RADAR:8788152
152S1452	152S1292	?	L8128	RADAR:8376462

ALTERNATE FOUNDRY

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

NOTE: FOR NO BATTERY SITUATION

VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 10UF CAP AT EACH VDD INPUT)

NOTE: CONCERNED ABOUT ESR > 20MOHM
NOTE: CHANGE SOME 1UF TO 4.7UF

LDO BYPASS

SYNC_MASTER=MADHAVI	SYNC_DATE=01/13/2011
PAGE TITLE: POWER: AMELIA PMU	
Apple Inc.	DRAWING NUMBER: 051-8773 SIZE: D
	REVISION: 10.0.0
	BRANCH:
	PAGE: 81 OF 157
	SHEET: 36 OF 48

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

(TEMP5 - TOP SIDE NEAR NAND)
(TEMP6 BOTTOM SIDE NEAR BRIDGE FLEX)
BOARD_TEMP5_P
BOARD_TEMP6_P

R8281 10KOHM-1% 0201
R8282 10KOHM-1% 0201
C8281 100PF 5% 6.3V CERM 01005
C8282 100PF 5% 6.3V CERM 01005
XW8281 NOSTUFF
XW8282 NOSTUFF
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU

C8206 0.01UF 10% 6.3V X5R 01005
C8207 0.01UF 10% 6.3V X5R 01005
R8260 220K 5% 1/32W MF 01005 NOSTUFF

FW_ZENER_PWR
DP_AP_HPD
HOME_EMI_L
ONOFF_L
SRL_L
PORT_DOCK_ACC_DET_L
PORT_DOCK_ACCID
USB_BRICKID
ADC_IN7

(TEMP1 - BOTTOM SIDE NEAR I/O FLEX CONN)
(TEMP2 - BOTTOM SIDE NEAR PMU)
(TEMP3 - BOTTOM SIDE NEAR H4G)
(TEMP4 - BOTTOM SIDE NEAR WIFI)
BOARD_TEMP1_P
BOARD_TEMP2_P
BOARD_TEMP3_P
BOARD_TEMP4_P
BOARD_TEMP5_P
BOARD_TEMP6_P
NC_BOARD_TEMP7
NC_BOARD_TEMP8
BATTERY_NTC
PMU_TCAL

R8216 CRITICAL 10KOHM-1% 0201
R8222 CRITICAL 10KOHM-1% 0201
R8218 CRITICAL 10KOHM-1% 0201
R8280 CRITICAL 10KOHM-1% 0201
C8215 100PF 5% 6.3V CERM 01005
C8221 100PF 5% 6.3V CERM 01005
C8217 100PF 5% 6.3V CERM 01005
C8223 100PF 5% 6.3V CERM 01005
XW8200 NOSTUFF
XW8201 NOSTUFF
XW8202 NOSTUFF
XW8203 NOSTUFF
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU
PLACE XW AND CAP CLOSE TO PMU

C8220 100PF 5% 6.3V CERM 01005
R8219 3.92K 0.1% 402 1/16W MF CRITICAL
RESISTOR FOR TEMP CALIBRATION

PM_KEEPACT
PMU_SHDWN (INTERNAL PULL-DOWN)
RST_PMU_IN (INTERNAL PULL-DOWN)
RST_AP_L
IRQ_PMU_L (PULLUP INSIDE H4P)
I2C0_SCL_1V8
I2C0_SDA_1V8
DWI_AP_CLK (INTERNAL PULL-DOWN)
DWI_AP_DO (INTERNAL PULL-DOWN)
DWI_AP_DI
DWI NAMING RELATIVE TO AP

U8100 D1974AB TFBGA OMIT
SYM 1 OF 4

FW_DPHP_DET	L29		
DPHP	K18		
BUTTON1	K16		
BUTTON2	K17		
BUTTON3	J17		
ACC_DET	A1		
ACC_ID	M2		
BRICK_ID	N28		
ADC_IN7	N27		
ADC_IN31	M26		
TDEV1	N30		
TDEV2	M30		
TDEV3	M29		
TDEV4	L30		
TDEV5	A29		
TDEV6	A28		
TDEV7	B26		
TDEV8	D25		
TBAT	C30		
TCAL	D26		
KEEPACT	B28		
SHDN	A2		
RESET_IN	B30		
RESET*	B29		
IRQ*	B27		
SCL	C29		
SDA	D30		
DWI_CK	N29		
DWI_DI	M27		
DWI_DO	M28		

DIGITAL INPUT REFERENCES
ANALOG INPUT
TEMPERATURE
GPIO
WDOG
RESET
I2C & DWI
ANALOG MUX

C8204 0.1UF 10% 6.3V X5R 201
R8203 200K 1% 1/20W MF 201
PLACEMENT NOTE: PLACE NEAR PIN K4
C8212 0.1UF 10% 6.3V X5R 201
C8209 1UF 10% 6.3V CERM 402
C8210 0.22UF 20% 6.3V X5R 0201 PLACEMENT NOTE: PLACE NEAR PIN K24

IREF	M1	PMU_IREF	
VREF	L1	PMU_VREF	
VDD_REF	K24	PMU_VDD_REF	
VDD_REF_A	K4		
VDD_RTC	M9	PMU_VDD_RTC	
ADC_REF	K9		

PMU_ADC_REF
C8214 1000PF 10% 6.3V X5R-CERM 01005

GPIO1	B22	CLK_32K_PMU	(CPU1V8; PUSH-PULL) USED BY ZEPHYR2. WHICH IS NOW POR
GPIO2	B23	CLK_32K_WLAN	(1.8_S2R; PUSH-PULL)
GPIO3	B24	RST_BT_L	(1.8_S2R; PUSH-PULL; NO PD REQ'D PER BB TEAM)
GPIO4	D21	RST_WLAN_L	(1.8_S2R; PUSH-PULL; NO PD REQ'D PER BB TEAM)
GPIO5	D20	RST_BB_PMU_L	(1.8_S2R; PUSH-PULL)
GPIO6	D14	BATTERY_SWI	(FALLING EDGE SENSITIVE) 2.5V ALWAYS ON PU IN BMU
GPIO7	D19	PM_BT_HOST_WAKE	(INTERNAL PD; RISING EDGE SENSITIVE)
GPIO8	E16	PM_WLAN_HOST_WAKE	(INTERNAL PD; RISING EDGE SENSITIVE)
GPIO9	D17	PM_BB_HOST_WAKE	(INTERNAL PD; RISING EDGE SENSITIVE) CAN'T BE USED FOR 32K CLK OUTPUT
GPIO10	D18	AUD_MIK_HS1_INT_L	(INTERNAL PU TO PP1V8_S2R; RISING EDGE SENSITIVE)
GPIO11	D15	DOCK_BB_EN	(1.8_S2R; PUSH-PULL) EXT PD BY BB MUXES
GPIO12	K21	NC_PMU_GPIO12	NEED RADAR TO STOP GENERATING 32K CLOCK
GPIO13	J20	NC_PMU_GPIO13	
GPIO14	K20	RST_L63_L	(INTERNAL PU TO 1.8_S2R)
GPIO15	J19	IRQ_HALL	(BOTH EDGES SENSITIVE) EXT PU
GPIO16	K19	NC_PMU_GPIO16	
GPIO17	J18	NC_PMU_GPIO17	

AMUX_A0	J28	NC_PMU_AMUX_A0
AMUX_A1	H28	NC_PMU_AMUX_A1
AMUX_A2	K26	NC_PMU_AMUX_A2
AMUX_A3	K27	NC_PMU_AMUX_A3
AMUX_AY	K29	NC_PMU_AMUX_AY
AMUX_B0	G28	NC_PMU_AMUX_B0
AMUX_B1	F28	NC_PMU_AMUX_B1
AMUX_B2	E28	NC_PMU_AMUX_B2
AMUX_B3	D27	NC_PMU_AMUX_B3
AMUX_BY	D29	NC_PMU_AMUX_BY

(WHAT SIGNALS DO YOU WANT MEASURED?)

VDD_LCM_SW	M25	PPVCC_MAIN
VDD_BOOST_LCM	N26	PP6V0_LCM_BT
LX_BOOST_LCM	M24	LCM_LX
LCM_FB	N25	PP6V0_LCM_VBOOST
VDD_LCM	M14	
LCM2_EN	K30	NC_LCM2_EN
VLCM1	N14	NC_VLCM1
VLCM2	M13	
VLCM3	N13	

(INTERNAL PULLDOWN; TE ENABLE)
PP5V25_WLCM2
BB_VBUS_DET
C8240 2.2UF 20% 10V X5R 402
C8238 1UF 10% 6.3V CERM 402
C8236 2.2UF 20% 10V X5R-CERM 402
C8237 10UF 20% 10V X5R 0603-1

LED BACKLIGHT LCM/GRAPE

WLED1_A	N15	LED_IO1_A_R
WLED2_A	M15	LED_IO2_A_R
WLED3_A	M16	LED_IO3_A_R
WLED4_A	M16	LED_IO4_A_R
WLED5_A	N17	LED_IO5_A_R
WLED6_A	M17	LED_IO6_A_R
WLED_LXA	M21 / N21	
VOUT_WLED_A	K22	
WLED_LXB	M23 / N23	
VOUT_WLED_B	K23	
WLED1_B	N18	LED_IO1_B_R
WLED2_B	N19	LED_IO2_B_R
WLED3_B	M18	LED_IO3_B_R
WLED4_B	N20	LED_IO4_B_R
WLED5_B	M19	LED_IO5_B_R
WLED6_B	M20	LED_IO6_B_R

I2C ADDRESS: 0111100X (0X78)

(NOTE: 2MHZ)
CRICITAL L8229 2.2UH-1.05A-0.195OHM VLS201612E-SM
CRICITAL D8230 PMEG2005AEL SOD882

WLED_LX_A
(PPLED_OUT_A)
=PPVCC_MAIN_LED
CRITICAL L8225 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8228 PMEG4010BEA SOD-323
CRITICAL C8226 10UF 20% 10V X5R 603
PPLED_OUT_A
CRITICAL C8232 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8233 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8234 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8235 4.7UF 10% 35V X5R-CERM 0603

R8227 1.00 1% 1/20W MF 201
R8231 1.00 1% 1/20W MF 201
R8232 1.00 1% 1/20W MF 201
R8235 1.00 1% 1/20W MF 201
R8239 1.00 1% 1/20W MF 201
R8240 1.00 1% 1/20W MF 201

LED_IO_1_A
LED_IO_2_A
LED_IO_3_A
LED_IO_4_A
LED_IO_5_A
LED_IO_6_A

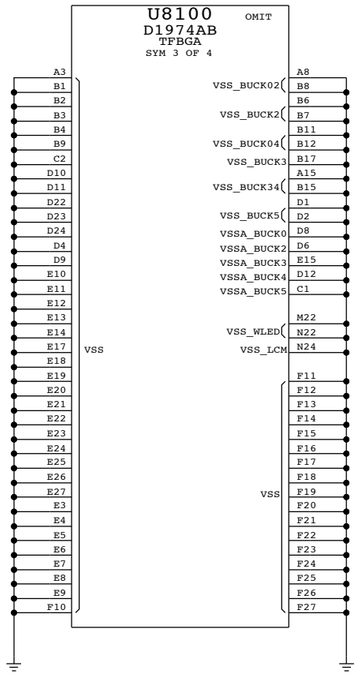
WLED_LX_B
(PPLED_OUT_B)
=PPVCC_MAIN_LED
CRITICAL L8255 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8258 PMEG4010BEA SOD-323
CRITICAL C8256 10UF 20% 10V X5R 603
PPLED_OUT_B
CRITICAL C8262 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8263 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8264 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8265 4.7UF 10% 35V X5R-CERM 0603

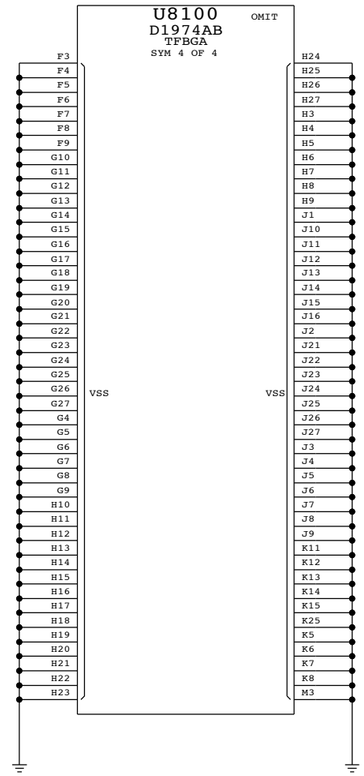
R8257 1.00 1% 1/20W MF 201
R8261 1.00 1% 1/20W MF 201
R8262 1.00 1% 1/20W MF 201
R8265 1.00 1% 1/20W MF 201
R8269 1.00 1% 1/20W MF 201
R8270 1.00 1% 1/20W MF 201

LED_IO_1_B
LED_IO_2_B
LED_IO_3_B
LED_IO_4_B
LED_IO_5_B
LED_IO_6_B

C8201 0.01UF 10% 50V X7R 402 PLACEMENT_NOTE=PLACE NEAR U8100.K22
C8266 0.01UF 10% 50V X7R 402 PLACEMENT_NOTE=PLACE NEAR U8100.K22
C8251 0.01UF 10% 50V X7R 402 PLACEMENT_NOTE=PLACE NEAR U8100.K23
C8267 0.01UF 10% 50V X7R 402 PLACEMENT_NOTE=PLACE NEAR U8100.K23

SYNC_MASTER=MLB SYNC_DATE=01/14/2011
PAGE TITLE
POWER: AMELIA PMU
Apple Inc.
DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 82 OF 157
SHEET 37 OF 48





SYNC MASTER=MADHAVI SYNC DATE=01/13/2011

PAGE TITLE

POWER: AMELIA VSS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

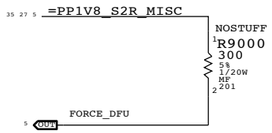
BRANCH

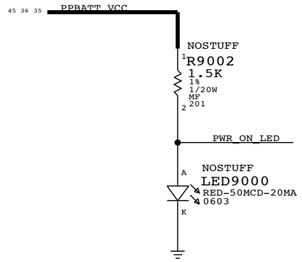
PAGE 83 OF 157

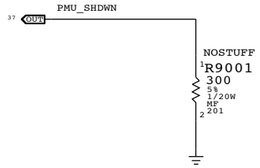
SHEET 38 OF 48

DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN







SYNC MASTER=ALEX SYNC DATE=10/04/2010

PAGE TITLE
DEBUG AND MISC

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 90 OF 157

SHEET 39 OF 48

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

FID9300 FID 0P5SM1P0SQ-NSP
FID9301 FID 0P5SM1P0SQ-NSP
FID9302 FID 0P5SM1P0SQ-NSP
FID9303 FID 0P5SM1P0SQ-NSP
FID9304 FID 0P5SM1P0SQ-NSP
FID9305 FID 0P5SM1P0SQ-NSP

SL9300 TH-NSP SL-1.1X0.4-1.4X0.7
SL9301 TH-NSP SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP SL-1.1X0.4-1.4X0.7
SL9304 TH-NSP SL-1.1X0.4-1.4X0.7
SL9305 TH-NSP SL-1.1X0.4-1.4X0.7
SL9306 TH-NSP SL-1.1X0.4-1.4X0.7
SL9310 TH-NSP SL-1.1X0.4-1.4X0.7
SL9312 TH-NSP SL-1.1X0.4-1.4X0.7
SL9313 TH-NSP SL-1.1X0.4-1.4X0.7
SL9314 TH-NSP SL-1.1X0.4-1.4X0.7
SL9315 TH-NSP SL-1.1X0.4-1.4X0.7
SL9316 TH-NSP SL-1.1X0.4-1.4X0.7

PROBE POINTS

PP0 P4MM SM	CODEC_LINE_OUT_REF	19 21
PP1 P4MM SM	CODEC_LINE_OUT_R	19 21
PP2 P4MM SM	AUD_SPKR_AMP2_PBUS	20
PP3 P4MM SM	AUD_SPKR_AMP1_PBUS	20
PP4 P4MM SM	CODEC_LINE_OUT_L	19 21
PP5 P4MM SM	DDR0_DQS_P<0>	8 13 44
PP6 P4MM SM	DDR0_DQ<0>	8 13 44
PP7 P4MM SM	DDR0_DQS_N<0>	8 13 44
PP8 P4MM SM	DDR0_DQS_N<1>	8 13 44
PP9 P4MM SM	DDR0_DQ<14>	8 13 44
PP10 P4MM SM	HSIC1_WLAN_DATA1	4 15 42
PP11 P4MM SM	HSIC1_WLAN_STB1	4 15 42
PP12 P4MM SM	Z1_BON_L<5>	17 18
PP13 P4MM SM	Z1_B_ADR<2>	17 18
PP14 P4MM SM	Z1_B_ADR<1>	17 18
PP15 P4MM SM	Z1_B_ADR<0>	17 18
PP16 P4MM SM	Z1_MISO	17 18
PP17 P4MM SM	Z1_BON_L<4>	17 18
PP18 P4MM SM	PP1V7_VA_VCP	35 36 45
PP19 P4MM SM	CONN_AUD_HEADSET_CHS_RET2	23 24
PP20 P4MM SM	CONN_AUD_HEADSET_CHS_MIC2	23 24
PP21 P4MM SM	CONN_AUD_HEADSET_DET	23 24
PP22 P4MM SM	AUD_HP1_DET_H	23
PP23 P4MM SM	AUD_HS_MIC2_RET	22 23
PP24 P4MM SM	AUD_HS_MIC1_HI	22 23
PP25 P4MM SM	AUD_HS_MIC1_RET	22 23
PP26 P4MM SM	AUD_HS_MIC2_HI	22 23

SYNC_MASTER=ALEX SYNC_DATE=10/04/2010

PAGE TITLE
FCT/ICT TEST/BRACKETS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 93 OF 157
SHEET 40 OF 48

MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL1,ISL12	Y	0.110 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL5,ISL8	Y	0.077 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL3	Y	0.055 MM	0.050 MM	3.0 MM		
45_OHM_SE	*	N	0.055 MM	0.050 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL1,ISL12	Y	0.088 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL3	Y	0.050 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL5,ISL8	Y	0.062 MM	0.050 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.110 MM	0.110 MM
90_OHM_DIFF	ISL3	Y	0.051 MM	0.051 MM	=STANDARD	0.120 MM	0.120 MM
90_OHM_DIFF	ISL5,ISL8	Y	0.072 MM	0.075 MM	=STANDARD	0.120 MM	0.120 MM

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM
LED	*	Y	0.2 MM	0.10MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.057 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.086 MM	?
2:1_SPACING	*	0.114 MM	?
2.5:1_SPACING	*	0.143 MM	?
3:1_SPACING	*	0.171 MM	?
4:1_SPACING	*	0.228 MM	?
5:1_SPACING	*	0.285 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.25 MM	10.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	10.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
LED	*	*	3:1_SPACING

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC_MASTER=MIKE SYNC DATE=01/21/2011

PAGE TITLE
CONSTRAINTS: MLB RULES

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 150 OF 157
SHEET 41 OF 48

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I63	CLK_50S	CLK	CLK_32K_PMU	18 37
I162	CLK_50S	CLK	CLK_32K_WLAN	15 37
I81	CLK_50S	CLK	CLK_32K_GPS	
I88	CLK_50S	CLK	CLK_CAM_FF	7 25
I89	CLK_50S	CLK	CLK_CAM_FF_FILT	25
I95	SE_50S	0P2MM_SPACING	CLK_CAM_FF_CONN	24 25
I96	CLK_50S	CLK	CLK_CAM_RF	7 25
I98	CLK_50S	CLK	CLK_CAM_RF_FILT	25
I225	CLK_50S	CLK	CLK_CAM_RF_CONN	24 25
I135	CLK_50S	CLK	I2S0_ASP_MCK	5
I133	CLK_50S	CLK	I2S0_ASP_MCK_R	5 19
I152	CLK_50S	CLK	CLK_CAM_FF_R	7
I150	CLK_50S	CLK	CLK_CAM_RF_R	7
I235	CLK_50S	CLK	CLK_CAM_FF_C	25
I233	CLK_50S	CLK	CLK_CAM_RF_C	25

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I231	UART_50S	UART	UART0_AP_RXD	5 15
I230	UART_50S	UART	UART0_AP_TXD	5 15
I174	UART_50S	UART	UART0_MUX_RXD	11 15
I173	UART_50S	UART	UART0_MUX_TXD	11 15
I178	UART_50S	UART	UART1_BB_CTS_L	5 30
I176	UART_50S	UART	UART1_BB_RTS_L	5 30
I177	UART_50S	UART	UART1_BB_TXD	5 30
I175	UART_50S	UART	UART1_BB_RXD	5 30
I170	UART_50S	UART	UART3_BT_CTS_L	5 15
I167	UART_50S	UART	UART3_BT_RTS_L	5 15
I171	UART_50S	UART	UART3_BT_RXD	5 15
I169	UART_50S	UART	UART3_BT_TXD	5 15
I232	UART_50S	UART	UART6_WLAN_RXD	5 15
I234	UART_50S	UART	UART6_WLAN_TXD	5 15

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I184	SPI_50S	SPI	SPI1_GRAPE_MISO	5 17
I184	SPI_50S	SPI	SPI1_GRAPE_MOSI	5 17
I185	SPI_50S	SPI	SPI1_GRAPE_SCLK	5 17
I186	SPI_50S	SPI	SPI1_GRAPE_CS_L	5 17
I189	SPI_50S	SPI	SPI2_IPC_MISO	5 30
I188	SPI_50S	SPI	SPI2_IPC_MOSI	5 30
I187	SPI_50S	SPI	SPI2_IPC_SCLK	5 30
I190	SPI_50S	SPI	SPI2_IPC_SRDY	5 30

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I157		DWI	DWI_AP_CLK	5 37
I155		DWI	DWI_AP_DI	5 37
I154		DWI	DWI_AP_DO	5 37

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I116		JTAG	JTAG_AP_TCK	4 27
I115		JTAG	JTAG_AP_TMS	4 27
I114		JTAG	JTAG_AP_TDI	4 10
I113		JTAG	JTAG_AP_TDO	4 10
I120		RST	JTAG_AP_TRST_L	4 10 45

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I1	I2C_50S	I2C	I2C1_SDA_1V8	5 10 25
I2	I2C_50S	I2C	I2C1_SCL_1V8	5 10 25
I3	I2C_50S	I2C	I2C0_SDA_1V8	5 10 19 22 37
I4	I2C_50S	I2C	I2C0_SCL_1V8	5 10 19 22 37
I61	I2C_50S	I2C	I2C2_SDA_3V0	5 25
I62	I2C_50S	I2C	I2C2_SCL_3V0	5 25
I98	I2C_50S	I2C	ISP_AP_0_SCL	7 25
I99	I2C_50S	I2C	ISP_AP_0_SDA	7 25
I100	I2C_50S	I2C	ISP_AP_1_SCL	7 25
I101	I2C_50S	I2C	ISP_AP_1_SDA	7 25
I102	I2C_50S	I2C	I2C2_SCL_3V0_ALS	10 24 25
I103	I2C_50S	I2C	I2C2_SDA_3V0_ALS	10 24 25
I224	I2C_50S	I2C	I2C1_SCL_1V8_CONN	24 25
I223	I2C_50S	I2C	I2C1_SDA_1V8_CONN	24 25
I125	I2C_50S	I2C	ISP_CAM_1_SCL	24 25
I126	I2C_50S	I2C	ISP_CAM_1_SDA	24 25
I220	I2C_50S	I2C	ISP_CAM_0_SCL	24 25
I221	I2C_50S	I2C	ISP_CAM_0_SDA	24 25

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I92		CRYSTAL	XTAL_24M_I	4
I90		CRYSTAL	XTAL_24M_O	4
I93		CRYSTAL	24M_O	4
I230		CRYSTAL	PMU_XTAL	36
I231		CRYSTAL	PMU_EXTAL	36

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I140	I2S_50S	I2S	I2S0_ASP_BCLK	5 19
I145	I2S_50S	I2S	I2S0_ASP_LRCK	5 19
I142	I2S_50S	I2S	I2S0_ASP_DIN	5 19
I141	I2S_50S	I2S	I2S0_ASP_DOUT	5 19
I159	I2S_50S	I2S	I2S_L63_ASP_SDOUT	19
I144	I2S_50S	I2S	I2S2_VSP_BCLK	5 15 19
I148	I2S_50S	I2S	I2S2_VSP_LRCK	5 15 19
I147	I2S_50S	I2S	I2S2_VSP_DIN	5 15 19
I146	I2S_50S	I2S	I2S2_VSP_DOUT	5 15 19
I160	I2S_50S	I2S	I2S_L63_VSP_SDOUT	19
I143	I2S_50S	I2S	I2S3_XSP_BCLK	5 19
I149	I2S_50S	I2S	I2S3_XSP_LRCK	5 19
I136	I2S_50S	I2S	I2S3_XSP_DIN	5 19
I138	I2S_50S	I2S	I2S3_XSP_DOUT	5 19
I161	I2S_50S	I2S	I2S_L63_XSP_SDOUT	19

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I5	USB_90D	USB	USB_DK_D0_P	4 27
I6	USB_90D	USB	USB_DK_D0_N	4 27
I7	USB_90D	USB	USB_DK_CON_D0_P	
I8	USB_90D	USB	USB_DK_CON_D0_N	
I82	USB_90D	USB	USB_BB_D_P	11 30
I83	USB_90D	USB	USB_BB_D_N	11 30
I84	USB_90D	USB	USB11_MUX_D0_P	4 11
I85	USB_90D	USB	USB11_MUX_D0_N	4 11
I124	USB_90D	USB	USB11_ACC_TX_N	11 27
I125	USB_90D	USB	USB11_ACC_RX_P	11 27
I171	USB_90D	USB	ACC_PT_DK_CON_TX	27 29
I172	USB_90D	USB	ACC_PT_DK_CON_RX	27 29
I204	USB_90D	USB	EXTRA_USB_D1_N	
I206	USB_90D	USB	EXTRA_USB_D1_P	
I205	USB_90D	USB	NC_USB11_D1_N	4 46
I207	USB_90D	USB	NC_USB11_D1_P	4 46
I208	USB_90D	USB	NC_USB_D1_N	4 46
I209	USB_90D	USB	NC_USB_D1_P	4 46
I210	USB_90D	USB	TP_WLAN_USB_DN	
I211	USB_90D	USB	TP_WLAN_USB_DP	
I212	USB_90D	USB	USB_GPIO_DM	
I214	USB_90D	USB	USB_GPIO_DM_CONN	
I213	USB_90D	USB	USB_GPIO_DP	
I215	USB_90D	USB	USB_GPIO_DP_CONN	
I216	USB_90D	USB	USB_PT_DK_CON_D_N	27 29
I217	USB_90D	USB	USB_PT_DK_CON_D_P	27 29
I218	USB_90D	USB	USB_UART_DM	
I219	USB_90D	USB	USB_UART_DM_CONN	
I222	USB_90D	USB	USB_UART_DP	
I221	USB_90D	USB	USB_UART_DP_CONN	
I223	USB_90D	USB	EXTRA_USB11_D1_N	
I224	USB_90D	USB	EXTRA_USB11_D1_P	

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I191	HSIC	HSIC_BB	HSIC0_BB_DATA1	4 30
I192	HSIC	HSIC_BB	HSIC0_BB_STB1	4 30
I193	HSIC	HSIC_WLAN	HSIC1_WLAN_DATA1	4 15 40
I194	HSIC	HSIC_WLAN	HSIC1_WLAN_STB1	4 15 40
I195	HSIC	HSIC	HSIC_BB_RDY	5 30
I196	HSIC	HSIC	HSIC_HOST_RDY	5 30
I197	HSIC	HSIC	HSIC_HOST_READY_WL	5
I198	HSIC	HSIC	HSIC_HOST_READY_WLAN	5 15
I199	HSIC	HSIC	HSIC_WLAN_RDY	5 15
I200	HSIC	HSIC	NC_HSIC0_DATA2	4 46
I201	HSIC	HSIC	NC_HSIC0_STB2	4 46
I202	HSIC	HSIC	NC_HSIC1_DATA2	4 46
I203	HSIC	HSIC	NC_HSIC1_STB2	4 46

SYNC_MASTER=MIKE SYNC_DATE=01/21/2011

PAGE TITLE
CONSTRAINTS: LOW SPEED BUS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 151 OF 157
SHEET 42 OF 48

ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
R213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
R214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
R215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
R232	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
R233	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
R231	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
R219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 27
R220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 27
R221	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 27
R222	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 27 28
R224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 27 28
R223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 27 28
R526	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB_R 28 29
R527	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y_R 28 29
R528	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR_R 28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
R335	MIPI_90D	MIPI0C	MIPI0C_AP_CLK_P 7 25
R336	MIPI_90D	MIPI0C	MIPI0C_AP_CLK_N 7 25
R338	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_P 24 25
R339	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_N 24 25
R331	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_P<0> 7 25
R332	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_N<0> 7 25
R330	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_N<1> 7 25
R329	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_N<2> 7 46
R327	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_N<3> 7 46
R326	MIPI_90D	MIPI0C	MIPI0C_AP_DATA_P<1> 7 25
R325	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_P<2> 7 46
R324	MIPI_90D	MIPI0C	NC_MIPI0C_AP_DATA_P<3> 7 46
R516	CAM_100DVA3	CAM	MIPI0C_CAM_DATA_N<0> 24 25
R518	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_N<1> 24 25
R521	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_N<2>
R520	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_N<3>
R519	CAM_100DVA3	CAM	MIPI0C_CAM_DATA_P<0> 24 25
R522	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_P<1> 24 25
R523	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_P<2>
R525	MIPI_90D	MIPI0C	MIPI0C_CAM_DATA_P<3>
R333	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_DEBUG_N
R334	MIPI_90D	MIPI0C	MIPI0C_CAM_CLK_DEBUG_P
R337	MIPI_90D	MIPI0C	MIPI0C_CAM_D0_DEBUG_N
R328	MIPI_90D	MIPI0C	MIPI0C_CAM_D0_DEBUG_P
R323	MIPI_90D	MIPI0C	MIPI0C_CAM_D1_DEBUG_N
R322	MIPI_90D	MIPI0C	MIPI0C_CAM_D1_DEBUG_P
R321	MIPI_90D	MIPI0C	MIPI0C_CAM_D2_DEBUG_N
R320	MIPI_90D	MIPI0C	MIPI0C_CAM_D2_DEBUG_P
R318	MIPI_90D	MIPI0C	MIPI0C_CAM_D3_DEBUG_N
R319	MIPI_90D	MIPI0C	MIPI0C_CAM_D3_DEBUG_P
R345	MIPI_90D	MIPI1C	MIPI1C_AP_DATA_P<0> 7 25
R346	MIPI_90D	MIPI1C	MIPI1C_AP_DATA_N<0> 7 25
R536	MIPI_90D	MIPI1C	NC_MIPI1C_AP_DATA_P<1> 7 46
R534	MIPI_90D	MIPI1C	NC_MIPI1C_AP_DATA_N<1> 7 46
R347	MIPI_90D	MIPI1C	MIPI1C_AP_CLK_P 7 25
R348	MIPI_90D	MIPI1C	MIPI1C_AP_CLK_N 7 25
R356	CAM_100DVGA	CAM	MIPI1C_CAM_DATA_P<0> 24 25
R355	CAM_100DVGA	CAM	MIPI1C_CAM_DATA_N<0> 24 25
R358	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_P 24 25
R359	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_N 24 25
R416	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_DEBUG_N
R417	MIPI_90D	MIPI1C	MIPI1C_CAM_CLK_DEBUG_P
R418	MIPI_90D	MIPI1C	MIPI1C_CAM_D0_DEBUG_N
R419	MIPI_90D	MIPI1C	MIPI1C_CAM_D0_DEBUG_P

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
R410	DP_90D	DP	DP_AP_AUX_N 7 28
R411	DP_90D	DP	DP_AP_AUX_P 7 28
R418	DP_50S	DP	DP_AP_HPD 7 37
R419	DP_90D	DP	DP_AP_TX_N<0> 7 28
R420	DP_90D	DP	DP_AP_TX_N<1> 7 28
R422	DP_90D	DP	DP_AP_TX_P<0> 7 28
R421	DP_90D	DP	DP_AP_TX_P<1> 7 28
R423	DP_90D	DP	DP_EMI_AUX_N 27 28 43
R424	DP_90D	DP	DP_EMI_AUX_P 27 28 43
R425	DP_90D	DP	DP_EMI_TX_N<0> 27 28
R427	DP_90D	DP	DP_EMI_TX_N<1> 27 28
R426	DP_90D	DP	DP_EMI_TX_P<0> 27 28
R428	DP_90D	DP	DP_EMI_TX_P<1> 27 28
R429	DP_90D	DP	DP_PT_DK_CON_AUX_N 27 29 43
R430	DP_90D	DP	DP_PT_DK_CON_AUX_P 27 29 43
R431	DP_90D	DP	DP_PT_DK_CON_TX_N<0> 27 29
R432	DP_90D	DP	DP_PT_DK_CON_TX_N<1> 27 29
R433	DP_90D	DP	DP_PT_DK_CON_TX_P<0> 27 29
R434	DP_90D	DP	DP_PT_DK_CON_TX_P<1> 27 29
R466	DP_90D	DP	DP_AP_TX_N<2> 7 28
R467	DP_90D	DP	DP_AP_TX_N<3> 7 28
R469	DP_90D	DP	DP_AP_TX_P<2> 7 28
R468	DP_90D	DP	DP_AP_TX_P<3> 7 28
R470	DP_90D	DP	DP_EMI_AUX_N 27 28 43
R471	DP_90D	DP	DP_EMI_AUX_P 27 28 43
R472	DP_90D	DP	DP_EMI_TX_N<2>
R473	DP_90D	DP	DP_EMI_TX_N<3>
R474	DP_90D	DP	DP_EMI_TX_P<2>
R475	DP_90D	DP	DP_EMI_TX_P<3>
R476	DP_90D	DP	DP_PT_DK_CON_AUX_N 27 29 43
R477	DP_90D	DP	DP_PT_DK_CON_AUX_P 27 29 43
R478	DP_90D	DP	DP_PT_DK_CON_TX_N<2> 28
R479	DP_90D	DP	DP_PT_DK_CON_TX_N<3> 28
R480	DP_90D	DP	DP_PT_DK_CON_TX_P<2> 28
R481	DP_90D	DP	DP_PT_DK_CON_TX_P<3> 28

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LED	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
R482	LED	LEDA	LED_IO1_A_R 37
R484	LED	LEDB	LED_IO1_B_R 37
R483	LED	LEDA	LED_IO2_A_R 37
R485	LED	LEDB	LED_IO2_B_R 37
R487	LED	LEDA	LED_IO3_A_R 37
R486	LED	LEDB	LED_IO3_B_R 37
R489	LED	LEDA	LED_IO4_A_R 37
R488	LED	LEDB	LED_IO4_B_R 37
R490	LED	LEDA	LED_IO5_A_R 37
R491	LED	LEDB	LED_IO5_B_R 37
R492	LED	LEDA	LED_IO6_A_R 37
R493	LED	LEDB	LED_IO6_B_R 37
R494	LED	LEDA	LED_IO_1_A 16 37
R495	LED	LEDB	LED_IO_1_B 16 37
R496	LED	LEDA	LED_IO_2_A 16 37
R497	LED	LEDB	LED_IO_2_B 16 37
R498	LED	LEDA	LED_IO_3_A 16 37
R499	LED	LEDB	LED_IO_3_B 16 37
R500	LED	LEDA	LED_IO_4_A 16 37
R501	LED	LEDB	LED_IO_4_B 16 37
R502	LED	LEDA	LED_IO_5_A 16 37
R503	LED	LEDB	LED_IO_5_B 16 37
R504	LED	LEDA	LED_IO_6_A 16 37
R505	LED	LEDB	LED_IO_6_B 16 37

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
R435	EDP_90D	EDP	EDP_AP_AUX_N 7 16
R436	EDP_90D	EDP	EDP_AP_AUX_P 7 16
R437	EDP_50S	EDP	EDP_AP_HPD 7 16
R439	EDP_90D	EDP	EDP_AP_TX_N<0> 7 16
R438	EDP_90D	EDP	EDP_AP_TX_N<1> 7 16
R440	EDP_90D	EDP	EDP_AP_TX_N<2> 7 16
R442	EDP_90D	EDP	EDP_AP_TX_N<3> 7 16
R443	EDP_90D	EDP	EDP_AP_TX_P<0> 7 16
R444	EDP_90D	EDP	EDP_AP_TX_P<1> 7 16
R441	EDP_90D	EDP	EDP_AP_TX_P<2> 7 16
R445	EDP_90D	EDP	EDP_AP_TX_P<3> 7 16
R447	EDP_90D	EDP	EDP_AUX_CONN_N 16
R446	EDP_90D	EDP	EDP_AUX_CONN_P 16
R449	EDP_90D	EDP	EDP_DATA_CONN_N<0> 16
R448	EDP_90D	EDP	EDP_DATA_CONN_N<1> 16
R450	EDP_90D	EDP	EDP_DATA_CONN_N<2> 16
R451	EDP_90D	EDP	EDP_DATA_CONN_N<3> 16
R452	EDP_90D	EDP	EDP_DATA_CONN_P<0> 16
R454	EDP_90D	EDP	EDP_DATA_CONN_P<1> 16
R453	EDP_90D	EDP	EDP_DATA_CONN_P<2> 16
R455	EDP_90D	EDP	EDP_DATA_CONN_P<3> 16
R457	EDP_90D	EDP	EDP_EMI_AUX_N 16
R456	EDP_90D	EDP	EDP_EMI_AUX_P 16
R458	EDP_90D	EDP	EDP_EMI_TX_N<0> 16
R460	EDP_90D	EDP	EDP_EMI_TX_N<1> 16
R459	EDP_90D	EDP	EDP_EMI_TX_N<2> 16
R462	EDP_90D	EDP	EDP_EMI_TX_N<3> 16
R461	EDP_90D	EDP	EDP_EMI_TX_P<0> 16
R463	EDP_90D	EDP	EDP_EMI_TX_P<1> 16
R464	EDP_90D	EDP	EDP_EMI_TX_P<2> 16
R465	EDP_90D	EDP	EDP_EMI_TX_P<3> 16

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
R509	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
R507	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
R508	AUDIO	AUDIO	LEFT_CH_P 20
R511	AUDIO	AUDIO	MAX983X4_L_IN_N 20
R510	AUDIO	AUDIO	MAX983X4_L_IN_P 20
R531	AUDIO	AUDIO	SPKRAMP_L_OUT_N 20
R530	AUDIO	AUDIO	SPKRAMP_L_OUT_P 20
R513	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
R514	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
R529	AUDIO	AUDIO	RIGHT_CH_P 20
R515	AUDIO	AUDIO	MAX983X4_R_IN_P 20
R512	AUDIO	AUDIO	MAX983X4_R_IN_N 20
R533	AUDIO	AUDIO	SPKRAMP_R_OUT_N 20
R532	AUDIO	AUDIO	SPKRAMP_R_OUT_P 20
R537	AUDIO	AUDIO	EXT_MIC_P 19 22
R538	AUDIO	AUDIO	EXT_MIC_REF 19 22
R535	AUDIO	AUDIO	HSMIC_C_P 19 22
R539	AUDIO	AUDIO	HSMIC_C_N 19 22
R540	AUDIO	AUDIO	HSMIC_R_P 22
R541	AUDIO	AUDIO	HSMIC_R_N 22
R542	AUDIO	AUDIO	AUD_HP1_MLBCON_R 21 23
R543	AUDIO	AUDIO	AUD_HP1_MLBCON_L 21 23
R544	AUDIO	AUDIO	CONN_AUD_HEADSET_RIGHT 23 24
R545	AUDIO	AUDIO	CONN_AUD_HEADSET_LEFT 23 24
R547	AUDIO	AUDIO	HP_R 19 21
R548	AUDIO	AUDIO	HP_L 19 21

SYNC_MASTER=MIKE SYNC_DATE=01/21/2011

PAGE TITLE

CONSTRAINTS: DISPLAY/AUDIO

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 152 OF 157

SHEET 43 OF 48

DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I221	DDR_50S	DDR	DDR0_CA<9..0>	8 13
I222	DDR_50S	DDR	DDR0_DM<3..0>	8 13
I223	DDR_90D	DDR	DDR0_CK_P	8 13
I224	DDR_90D	DDR	DDR0_CK_N	8 13
I225	DDR_50S	DDR	DDR0_CKE<1..0>	8 13
I226	DDR_50S	DDR	DDR0_CSN<2..0>	8 13
I227	DDR_50S	DDR	DDR0_ZO	13
I228	DDR_50S	DDR0	DDR0_DQ<7..0>	8 13 40
I229	DDR_50S	DDR0	DDR0_DQS_P<0>	8 13 40
I230	DDR_50S	DDR0	DDR0_DQS_N<0>	8 13 40
I231	DDR_50S	DDR1	DDR0_DQ<15..8>	8 13 40
I232	DDR_50S	DDR1	DDR0_DQS_P<1>	8 13
I233	DDR_50S	DDR1	DDR0_DQS_N<1>	8 13 40
I234	DDR_50S	DDR2	DDR0_DQ<23..16>	8 13
I235	DDR_50S	DDR2	DDR0_DQS_P<2>	8 13
I236	DDR_50S	DDR2	DDR0_DQS_N<2>	8 13
I237	DDR_50S	DDR3	DDR0_DQ<31..24>	8 13
I238	DDR_50S	DDR3	DDR0_DQS_P<3>	8 13
I239	DDR_50S	DDR3	DDR0_DQS_N<3>	8 13
I201	DDR_50S	DDR	DDR1_CA<9..0>	8 13
I202	DDR_50S	DDR	DDR1_DM<3..0>	8 13
I203	DDR_90D	DDR	DDR1_CK_P	8 13
I204	DDR_90D	DDR	DDR1_CK_N	8 13
I205	DDR_50S	DDR	DDR1_CKE<1..0>	8 13
I206	DDR_50S	DDR	DDR1_CSN<2..0>	8 13
I208	DDR_50S	DDR	DDR1_ZO	13
I210	DDR_50S	DDR0	DDR1_DQ<7..0>	8 13
I209	DDR_50S	DDR0	DDR1_DQS_P<0>	8 13
I211	DDR_50S	DDR0	DDR1_DQS_N<0>	8 13
I212	DDR_50S	DDR1	DDR1_DQ<15..8>	8 13
I213	DDR_50S	DDR1	DDR1_DQS_P<1>	8 13
I214	DDR_50S	DDR1	DDR1_DQS_N<1>	8 13
I215	DDR_50S	DDR2	DDR1_DQ<23..16>	8 13
I216	DDR_50S	DDR2	DDR1_DQS_P<2>	8 13
I217	DDR_50S	DDR2	DDR1_DQS_N<2>	8 13
I218	DDR_50S	DDR3	DDR1_DQ<31..24>	8 13
I219	DDR_50S	DDR3	DDR1_DQS_P<3>	8 13
I220	DDR_50S	DDR3	DDR1_DQS_N<3>	8 13
I181	DDR_50S	DDR	DDR2_CA<9..0>	8 14
I182	DDR_50S	DDR	DDR2_DM<3..0>	8 14
I183	DDR_90D	DDR	DDR2_CK_P	8 14
I184	DDR_90D	DDR	DDR2_CK_N	8 14
I185	DDR_50S	DDR	DDR2_CKE<1..0>	8 14
I186	DDR_50S	DDR	DDR2_CSN<2..0>	8 14
I188	DDR_50S	DDR	DDR2_ZO	14
I189	DDR_50S	DDR0	DDR2_DQ<7..0>	8 14
I187	DDR_50S	DDR0	DDR2_DQS_P<0>	8 14
I191	DDR_50S	DDR0	DDR2_DQS_N<0>	8 14
I192	DDR_50S	DDR1	DDR2_DQ<15..8>	8 14
I193	DDR_50S	DDR1	DDR2_DQS_P<1>	8 14
I194	DDR_50S	DDR1	DDR2_DQS_N<1>	8 14
I195	DDR_50S	DDR2	DDR2_DQ<23..16>	8 14
I196	DDR_50S	DDR2	DDR2_DQS_P<2>	8 14
I197	DDR_50S	DDR2	DDR2_DQS_N<2>	8 14
I198	DDR_50S	DDR3	DDR2_DQ<31..24>	8 14
I199	DDR_50S	DDR3	DDR2_DQS_P<3>	8 14
I200	DDR_50S	DDR3	DDR2_DQS_N<3>	8 14
I138	DDR_50S	DDR	DDR3_CA<9..0>	8 14
I139	DDR_50S	DDR	DDR3_DM<3..0>	8 14
I141	DDR_90D	DDR	DDR3_CK_P	8 14
I144	DDR_90D	DDR	DDR3_CK_N	8 14
I142	DDR_50S	DDR	DDR3_CKE<1..0>	8 14
I147	DDR_50S	DDR	DDR3_CSN<2..0>	8 14
I148	DDR_50S	DDR	DDR3_ZO	14
I137	DDR_50S	DDR0	DDR3_DQ<7..0>	8 14
I170	DDR_50S	DDR0	DDR3_DQS_P<0>	8 14
I171	DDR_50S	DDR0	DDR3_DQS_N<0>	8 14
I172	DDR_50S	DDR1	DDR3_DQ<15..8>	8 14
I173	DDR_50S	DDR1	DDR3_DQS_P<1>	8 14
I174	DDR_50S	DDR1	DDR3_DQS_N<1>	8 14
I175	DDR_50S	DDR2	DDR3_DQ<23..16>	8 14
I176	DDR_50S	DDR2	DDR3_DQS_P<2>	8 14
I177	DDR_50S	DDR2	DDR3_DQS_N<2>	8 14
I178	DDR_50S	DDR3	DDR3_DQ<31..24>	8 14
I179	DDR_50S	DDR3	DDR3_DQS_P<3>	8 14
I180	DDR_50S	DDR3	DDR3_DQS_N<3>	8 14

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I68	NAND_50S	NAND0	FMI0_AD<0>	6 12
I69	NAND_50S	NAND0	FMI0_AD<1>	6 12
I70	NAND_50S	NAND0	FMI0_AD<2>	6 12
I71	NAND_50S	NAND0	FMI0_AD<3>	6 12
I72	NAND_50S	NAND0	FMI0_AD<4>	6 12
I73	NAND_50S	NAND0	FMI0_AD<5>	6 12
I74	NAND_50S	NAND0	FMI0_AD<6>	6 12
I75	NAND_50S	NAND0	FMI0_AD<7>	6 12
I76	NAND_50S	NAND0	FMI0_ALE	6 12
I77	NAND_50S	NAND0	FMI0_CE0_L	6 12
I78	NAND_50S	NAND0	FMI0_CE1_L	6 12
I120	NAND_50S	NAND0	FMI0_CE2_L	
I121	NAND_50S	NAND0	FMI0_CE3_L	
I122	NAND_50S	NAND0	FMI0_CE4_L	
I123	NAND_50S	NAND0	FMI0_CE5_L	
I124	NAND_50S	NAND0	FMI0_CE6_L	
I125	NAND_50S	NAND0	FMI0_CE7_L	
I126	NAND_50S	NAND0	FMI0_CLE	6 12
I127	NAND_50S	NAND0	FMI0_DQS_N	
I128	NAND_50S	NAND0	FMI0_DQS_P	6 12
I129	NAND_50S	NAND0	FMI0_RB0_L	
I130	NAND_50S	NAND0	FMI0_RB1_L	
I131	NAND_50S	NAND0	FMI0_RE_N	6 12
I132	NAND_50S	NAND0	FMI0_RE_P	
I133	NAND_50S	NAND0	FMI0_WE_L	6 12
I134	NAND_50S	NAND0	FMI0_WP_L	
I135	NAND_50S	NAND1	FMI1_AD<0>	6 12
I136	NAND_50S	NAND1	FMI1_AD<1>	6 12
I137	NAND_50S	NAND1	FMI1_AD<2>	6 12
I138	NAND_50S	NAND1	FMI1_AD<3>	6 12
I139	NAND_50S	NAND1	FMI1_AD<4>	6 12
I140	NAND_50S	NAND1	FMI1_AD<5>	6 12
I143	NAND_50S	NAND1	FMI1_AD<6>	6 12
I145	NAND_50S	NAND1	FMI1_AD<7>	6 12
I146	NAND_50S	NAND1	FMI1_ALE	6 12 44
I147	NAND_50S	NAND1	FMI1_CE0_L	6 12
I148	NAND_50S	NAND1	FMI1_CE1_L	6 12
I149	NAND_50S	NAND1	FMI1_CE2_L	
I150	NAND_50S	NAND1	FMI1_CE3_L	
I151	NAND_50S	NAND1	FMI1_CE4_L	
I152	NAND_50S	NAND1	FMI1_CE5_L	
I153	NAND_50S	NAND1	FMI1_CE6_L	
I154	NAND_50S	NAND1	FMI1_CE7_L	
I155	NAND_50S	NAND1	FMI1_CLE	6 12 44
I156	NAND_50S	NAND1	FMI1_DQS_N	
I157	NAND_50S	NAND1	FMI1_DQS_P	6 12
I158	NAND_50S	NAND1	FMI1_RB0_L	
I159	NAND_50S	NAND1	FMI1_RB1_L	
I160	NAND_50S	NAND1	FMI1_RE_N	6 12
I161	NAND_50S	NAND1	FMI1_RE_P	
I162	NAND_50S	NAND1	FMI1_WE_L	6 12 44
I163	NAND_50S	NAND1	FMI1_WP_L	44
I164	NAND_50S	NAND1	FMI1_CLE	6 12 44
I165	NAND_50S	NAND1	FMI1_ALE	6 12 44
I166	NAND_50S	NAND1	FMI1_RE_L	
I167	NAND_50S	NAND1	FMI1_WE_L	6 12 44
I168	NAND_50S	NAND1	FMI1_WP_L	44

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
I49	NAND_50S	NAND0	SLOT0_FMI0_AD<0>
I50	NAND_50S	NAND0	SLOT0_FMI0_AD<1>
I51	NAND_50S	NAND0	SLOT0_FMI0_AD<2>
I52	NAND_50S	NAND0	SLOT0_FMI0_AD<3>
I53	NAND_50S	NAND0	SLOT0_FMI0_AD<4>
I54	NAND_50S	NAND0	SLOT0_FMI0_AD<5>
I55	NAND_50S	NAND0	SLOT0_FMI0_AD<6>
I56	NAND_50S	NAND0	SLOT0_FMI0_AD<7>
I57	NAND_50S	NAND0	SLOT0_FMI0_ALE
I58	NAND_50S	NAND0	SLOT0_FMI0_CE0_L
I59	NAND_50S	NAND0	SLOT0_FMI0_CE1_L
I60	NAND_50S	NAND0	SLOT0_FMI0_CLE
I62	NAND_50S	NAND0	SLOT0_FMI0_DQS_P
I61	NAND_50S	NAND0	SLOT0_FMI0_RE_N
I63	NAND_50S	NAND0	SLOT0_FMI0_WE_L
I64	NAND_50S	NAND1	SLOT0_FMI1_AD<0>
I65	NAND_50S	NAND1	SLOT0_FMI1_AD<1>
I67	NAND_50S	NAND1	SLOT0_FMI1_AD<2>
I66	NAND_50S	NAND1	SLOT0_FMI1_AD<3>
I79	NAND_50S	NAND1	SLOT0_FMI1_AD<4>
I80	NAND_50S	NAND1	SLOT0_FMI1_AD<5>
I81	NAND_50S	NAND1	SLOT0_FMI1_AD<6>
I83	NAND_50S	NAND1	SLOT0_FMI1_AD<7>
I82	NAND_50S	NAND1	SLOT0_FMI1_ALE
I84	NAND_50S	NAND1	SLOT0_FMI1_CE0_L
I85	NAND_50S	NAND1	SLOT0_FMI1_CE1_L
I86	NAND_50S	NAND1	SLOT0_FMI1_CLE
I87	NAND_50S	NAND1	SLOT0_FMI1_DQS_P
I88	NAND_50S	NAND1	SLOT0_FMI1_RE_N
I89	NAND_50S	NAND1	SLOT0_FMI1_WE_L
I90	NAND_50S	NAND0	SLOT1_FMI0_AD<0>
I91	NAND_50S	NAND0	SLOT1_FMI0_AD<1>
I93	NAND_50S	NAND0	SLOT1_FMI0_AD<2>
I92	NAND_50S	NAND0	SLOT1_FMI0_AD<3>
I94	NAND_50S	NAND0	SLOT1_FMI0_AD<4>
I95	NAND_50S	NAND0	SLOT1_FMI0_AD<5>
I96	NAND_50S	NAND0	SLOT1_FMI0_AD<6>
I97	NAND_50S	NAND0	SLOT1_FMI0_AD<7>
I98	NAND_50S	NAND0	SLOT1_FMI0_ALE
I99	NAND_50S	NAND0	SLOT1_FMI0_CE0_L
I100	NAND_50S	NAND0	SLOT1_FMI0_CE1_L
I101	NAND_50S	NAND0	SLOT1_FMI0_CLE
I102	NAND_50S	NAND0	SLOT1_FMI0_DQS_P
I103	NAND_50S	NAND0	SLOT1_FMI0_RE_N
I104	NAND_50S	NAND0	SLOT1_FMI0_WE_L
I105	NAND_50S	NAND1	SLOT1_FMI1_AD<0>
I106	NAND_50S	NAND1	SLOT1_FMI1_AD<1>
I107	NAND_50S	NAND1	SLOT1_FMI1_AD<2>
I108	NAND_50S	NAND1	SLOT1_FMI1_AD<3>
I109	NAND_50S	NAND1	SLOT1_FMI1_AD<4>
I110	NAND_50S	NAND1	SLOT1_FMI1_AD<5>
I111	NAND_50S	NAND1	SLOT1_FMI1_AD<6>
I112	NAND_50S	NAND1	SLOT1_FMI1_AD<7>
I113	NAND_50S	NAND1	SLOT1_FMI1_ALE
I114	NAND_50S	NAND1	SLOT1_FMI1_CE0_L
I115	NAND_50S	NAND1	SLOT1_FMI1_CE1_L
I116	NAND_50S	NAND1	SLOT1_FMI1_CLE
I117	NAND_50S	NAND1	SLOT1_FMI1_DQS_P
I118	NAND_50S	NAND1	SLOT1_FMI1_RE_N
I119	NAND_50S	NAND1	SLOT1_FMI1_WE_L

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I156		PWR	PPVREF_DDR0_CA	13 45
I157		PWR	PPVREF_DDR0_DQ	13 45
I158		PWR	PPVREF_DDR1_CA	13 45
I159		PWR	PPVREF_DDR1_DQ	13 45

SYNC_MASTER=MIKE SYNC_DATE=01/21/2011

PAGE TITLE: CONSTRAINTS: DDR/FMI

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D
REVISION: 10.0.0
BRANCH:
PAGE: 153 OF 157
SHEET: 44 OF 48

PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P255 3.0V	PP_PWR	PWR	MT_3V3_INT 18 45
P256 1.8V	PP_PWR	PWR	Z1_1V8_OUT 18
P257 1.8V	PP_PWR	PWR	Z2_VDDCORE 18
P258 1.8V	PP_PWR	PWR	Z2_VDDANA 18
P259 1.8V	PP_PWR	PWR	Z2_3V3_1V8_IN 18

ELECTRICAL_CONSTRAINT_SET	VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P224	3.3V	PP_PWR	PWR	ACC_PT_DK_CON_PP3V3 27 29
B1		PP_PWR	PWR	BUCK0_FB 36
B2		PP_PWR	PWR	BUCK0_LXL 36
B3		PP_PWR	PWR	BUCK0_LXM 36
B4		PP_PWR	PWR	BUCK2_FB 36
B5		PP_PWR	PWR	BUCK2_LXL 36
B6		PP_PWR	PWR	BUCK2_LXM 36
B7		PP_PWR	PWR	BUCK2_LXR 36
B8		PP_PWR	PWR	BUCK3_FB 36
B9		PP_PWR	PWR	BUCK3_LXL 36
B12		PP_PWR	PWR	BUCK3_LXM 36
B11		PP_PWR	PWR	BUCK4_FB 36
B10		PP_PWR	PWR	BUCK4_LXL 36
B13		PP_PWR	PWR	BUCK4_LXM 36
B15		PP_PWR	PWR	BUCK5_FB 36
B14		PP_PWR	PWR	BUCK5_LX 36
B16	0.4V	PP_PWR	PWR	PP0V4_MIPI0D 7
B17	0.4V	PP_PWR	PWR	PP0V4_MIPI1D 7
E1	1.1V	PP_PWR	PWR	PP1V1 35 36
E15	1.2V	PP_PWR	PWR	PP1V2 35 36
E20	1.1V	PP_PWR	PWR	PP1V8 35 36
F21	1.1V	PP_PWR	PWR	PP1V1_MIPID_PLL_F 4
F2	1.1V	PP_PWR	PWR	PP1V1_PL0_F 4
F22	1.1V	PP_PWR	PWR	PP1V1_PL1_F 4
F24	1.1V	PP_PWR	PWR	PP1V1_PL2_F 4
F25	1.1V	PP_PWR	PWR	PP1V1_PL3_F 4
F26	1.1V	PP_PWR	PWR	PP1V1_PL4_F 4
F28	1.1V	PP_PWR	PWR	PP1V1_PL5_F 4
F27	1.1V	PP_PWR	PWR	PP1V1_PLL_USB_F 4
F29	1.25V	PP_PWR	PWR	PP1V25_CPU 35 36
E30	1.2V	PP_PWR	PWR	PP1V2_S2R 35 36
E31	1.2V	PP_PWR	PWR	PP1V2_SOC 35 36
E32	1.7V	PP_PWR	PWR	PP1V7_VA_VCP 35 36 40
E33	1.8V	PP_PWR	PWR	PP1V8_ALWAYS 35 36
E34	1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX 7
E35	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX 7
E36	1.8V	PP_PWR	PWR	PP1V8_GRAPE 35 36
E37	1.8V	PP_PWR	PWR	PP1V8_S2R 35 36
E38	1.8V	PP_PWR	PWR	PP1V8_SENSOR_FLT 24 26
E39	1.8V	PP_PWR	PWR	PP1V8_VDDA18_TS 5
E40	2.85V	PP_PWR	PWR	PP2V85_CAM 35 36
E41	2.85V	PP_PWR	PWR	PP2V85_CAM_FLT 24 26
E42	3.0V	PP_PWR	PWR	PP3V0_GRAPE 35 36
E43	3.0V	PP_PWR	PWR	PP3V0_IO 35 36
E44	3.0V	PP_PWR	PWR	PP3V0_OPTICAL 35 36
E45	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL 35 36
E46	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL_FLT 24 26
E47	3.0V	PP_PWR	PWR	PP3V0_SENSOR_FLT 10 24 26
E49	3.0V	PP_PWR	PWR	PP3V0_VIDEO 35 36
E51	3.0V	PP_PWR	PWR	PP3V0_VIDEO_BUF 35 36
E50	3.2V	PP_PWR	PWR	PP3V2_LDO5 35 36
E53	3.2V	PP_PWR	PWR	PP3V2_S2R_USBMUX 35 36
E52	3.3V	PP_PWR	PWR	PP3V3_ACC 35 36
E54	3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F 16
E55	3.3V	PP_PWR	PWR	PP3V3_OUT 35 36
E56	3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR 16
E57	5.25V	PP_PWR	PWR	PP5V25_VLCM2 35 37
E58	6.0V	PP_PWR	PWR	PP6V0_LCM_HI 37
E59	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST 37
E60	4.2V	PWR500	PWR	PPBATT_VCC 35 36 39
E61	1.8V	PP_PWR	PWR	PPIO_NAND_H4 6 9
E62	20.4V	PP_PWR	PWR	PPLED_BACK_REG_A 16
E63	20.4V	PP_PWR	PWR	PPLED_BACK_REG_B 16
E64	20.4V	PP_PWR	PWR	PPLED_OUT_A 35 37
E65	20.4V	PP_PWR	PWR	PPLED_OUT_B 35 37
E66	6.0V	PP_PWR	PWR	PPVBUS_PROT 36
E67	6.0V	PP_PWR	PWR	PPVBUS_USB 4 36
E68	6.0V	PP_PWR	PWR	PPVBUS_USB_DCIN 35 36
E69	5.0V	PP_PWR	PWR	PPVBUS_USB_PT_DK_CON 27 29
B20	1.8V	PP_PWR	PWR	PPVCCO_NAND 12
B21	4.7V	PP_PWR	PWR	PPVCC_MAIN 35 36 37
B22	0.6V	PP_PWR	PWR	PPVREF_DDR0_CA 13 44
B23	0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ 13 44
B24	0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ_H4 8
B26	0.6V	PP_PWR	PWR	PPVREF_DDR1_CA 13 44
B25	0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ 13 44
B27	0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ_H4 8
B28	0.6V	PP_PWR	PWR	PPVREF_DDR2_CA 14
B29	0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ 14
B30	0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ_H4 8
B31	0.6V	PP_PWR	PWR	PPVREF_DDR3_CA 14
B32	0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ 14
B33	0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ_H4 8
F210	4.6V	PP_PWR	PWR	BATT_POS_RC 36
B34	18V	PP_PWR	PWR	PP18V_GRAPE 17
B35	18V	PP_PWR	PWR	PP18V_R_GRAPE 17
P260		PP_PWR	PWR	DAC_AP_VREF 7
P261	3.3V	PP_PWR	PWR	PPVDDI_NAND_U1400 12
P262		PP_PWR	PWR	VR_BOOST_SW 17
P263		PP_PWR	PWR	VR_BOOST_L 17
P264	3.0V	PP_PWR	PWR	MT_3V3_INT 18 45

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND_PH	*	GND

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B192	GND	GND		GND
B200	GND	GND	VOLTAGE=0V	GND_AUDIO_CODEC 19 21
B201	GND	GND	VOLTAGE=0V	GND_AUDIO_HP_AMP 19 21 22
B202	GND	GND	VOLTAGE=0V	GND_AUDIO_PT_DK 21 27
B203	GND	GND	VOLTAGE=0V	GND_SPKR_AMP1 20
B204	GND	GND	VOLTAGE=0V	GND_SPKR_AMP2 20
B206	GND	GND	VOLTAGE=0V	GND_PMU
B208	GND	GND		AGND
B217	GND	GND		AGND_U3000 17

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
B165		RST	BB_TRST_L
B160		RST	DBG_RST
B169		RST	DEBUG_RST_L
B173		RST	GSM_TXBURST_IND 5 15 30
B163		RST	JTAG_AP_TRST_L 4 10 42
B170		RST	RST_AP_1V8_L 4
B166		RST	RST_AP_L 4 27 30 37
B172		RST	RST_BB_L 5 30
B174		RST	RST_BB_PMU_L 30 37
B171		RST	RST_BT_L 15 37
B175		RST	RST_DET_L 5 30
B176		GRAPE	RST_GRAPE_L 6 17
B177		RST	RST_L63_L 19 37
B178		RST	RST_PMU_IN 4 37
B179		RST	RST_WLAN_L 15 37
B180		RST	SIMCRD_RST
B182		RST	TP_WLAN_TRST_L
B183		RST	UD881_RST
B184		RST	UD882_RST

SYNC_MASTER=MIKE SYNC_DATE=01/21/2011

PAGE TITLE
CONSTRAINTS: POWER / GND

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D
REVISION 10.0.0
BRANCH
PAGE 154 OF 157
SHEET 45 OF 48

SNS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SNS	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_90D	*	90_OHM_DIFF

E58	NC_HSIC0_DATA2	NO_TEST=TRUE	4 42
E59	NC_HSIC0_STB2	NO_TEST=TRUE	4 42
E60	NC_HSIC1_DATA2	NO_TEST=TRUE	4 42
E61	NC_HSIC1_STB2	NO_TEST=TRUE	4 42
E62	NC_JTAG_AP_TRTCK	NO_TEST=TRUE	4
E64	NC_USB_D1_P	NO_TEST=TRUE	4 42
E65	NC_USB_D1_N	NO_TEST=TRUE	4 42
E66	NC_USB11_D1_P	NO_TEST=TRUE	4 42
E67	NC_USB11_D1_N	NO_TEST=TRUE	4 42
E68	NC_USB_ANALOGTEST0	NO_TEST=TRUE	4
E69	NC_USB_ANALOGTEST1	NO_TEST=TRUE	4
E60	NC_USB_ID0	NO_TEST=TRUE	4
E61	NC_USB_ID1	NO_TEST=TRUE	4
E62	NC_USB_BRICKID1	NO_TEST=TRUE	4
E63	NC_I2S1_MCK	NO_TEST=TRUE	5
E64	NC_I2S1_BCLK	NO_TEST=TRUE	5
E65	NC_I2S1_LRCK	NO_TEST=TRUE	5
E66	NC_I2S1_DIN	NO_TEST=TRUE	5
E67	NC_I2S1_DOUT	NO_TEST=TRUE	5
E68	NC_I2S2_MCK	NO_TEST=TRUE	5
E69	NC_I2S3_MCK	NO_TEST=TRUE	5
E70	NC_AP_GPIO216	NO_TEST=TRUE	5
E71	NC_SPI_FLASH_CS_L	NO_TEST=TRUE	5
E72	NC_SWI_AP	NO_TEST=TRUE	5
E73	NC_SDIO0_WL_CLK	NO_TEST=TRUE	5
E74	NC_SDIO0_WL_CMD	NO_TEST=TRUE	5
E75	NC_SDIO0_WL_DATA<0>	NO_TEST=TRUE	5
E76	NC_SDIO0_WL_DATA<1>	NO_TEST=TRUE	5
E77	NC_SDIO0_WL_DATA<2>	NO_TEST=TRUE	5
E78	NC_SDIO0_WL_DATA<3>	NO_TEST=TRUE	5
E81	NC_SPI3_MISO	NO_TEST=TRUE	5
E82	NC_SPI3_MOSI	NO_TEST=TRUE	5
E83	NC_SPI3_SCLK	NO_TEST=TRUE	5
E84	NC_SPI3_CS_L	NO_TEST=TRUE	5
E90	NC_AP_GPIO3	NO_TEST=TRUE	5
E91	NC_AP_GPIO7	NO_TEST=TRUE	5
E92	NC_AP_GPIO8	NO_TEST=TRUE	5
E93	NC_AP_GPIO11	NO_TEST=TRUE	5
E94	NC_AP_GPIO13	NO_TEST=TRUE	5
E95	NC_BOARD_ID_3	NO_TEST=TRUE	5
E96	NC_AP_GPIO19	NO_TEST=TRUE	5
E97	NC_AP_GPIO31	NO_TEST=TRUE	5
E98	NC_AP_GPIO35	NO_TEST=TRUE	5
E99	NC_AP_GPIO3V1	NO_TEST=TRUE	5
E101	NC_AP_GPIO185	NO_TEST=TRUE	5
E100	NC_AP_GPIO186	NO_TEST=TRUE	5
E102	NC_UART2_RXD	NO_TEST=TRUE	5
E103	NC_UART2_TXD	NO_TEST=TRUE	5
E107	NC_UART4_CTS_L	NO_TEST=TRUE	5
E106	NC_UART4_RTS_L	NO_TEST=TRUE	5
E105	NC_UART4_RXD	NO_TEST=TRUE	5
E108	NC_UART4_TXD	NO_TEST=TRUE	5
E110	NC_UART6_CTSN	NO_TEST=TRUE	5
E109	NC_UART6_RTSN	NO_TEST=TRUE	5

E111	NC_FMI0_CE2_L	NO_TEST=TRUE	6
E113	NC_FMI0_CE3_L	NO_TEST=TRUE	6
E111	NC_FMI0_CE4_L	NO_TEST=TRUE	6
E112	NC_FMI0_CE5_L	NO_TEST=TRUE	6
E112	NC_FMI0_CE6_L	NO_TEST=TRUE	6
E112	NC_FMI0_CE7_L	NO_TEST=TRUE	6
E112	NC_FMI1_CE2_L	NO_TEST=TRUE	6
E112	NC_FMI1_CE3_L	NO_TEST=TRUE	6
E112	NC_FMI1_CE4_L	NO_TEST=TRUE	6
E112	NC_FMI1_CE5_L	NO_TEST=TRUE	6
E112	NC_FMI1_CE6_L	NO_TEST=TRUE	6
E113	NC_FMI1_CE7_L	NO_TEST=TRUE	6
E113	NC_FMI2_CE1_L	NO_TEST=TRUE	6
E113	NC_FMI2_CE2_L	NO_TEST=TRUE	6
E113	NC_FMI2_CE3_L	NO_TEST=TRUE	6
E112	NC_FMI2_CE5_L	NO_TEST=TRUE	6
E113	NC_FMI2_AD<0>	NO_TEST=TRUE	6
E113	NC_FMI2_AD<1>	NO_TEST=TRUE	6
E113	NC_FMI2_AD<2>	NO_TEST=TRUE	6
E113	NC_FMI2_AD<3>	NO_TEST=TRUE	6
E113	NC_FMI2_AD<4>	NO_TEST=TRUE	6
E113	NC_FMI2_AD<5>	NO_TEST=TRUE	6
E114	NC_FMI2_AD<6>	NO_TEST=TRUE	6
E114	NC_FMI2_AD<7>	NO_TEST=TRUE	6
E114	NC_FMI2_ALE	NO_TEST=TRUE	6
E114	NC_FMI2_CLE	NO_TEST=TRUE	6
E114	NC_FMI2_WE_L	NO_TEST=TRUE	6
E114	NC_FMI2_RE_L	NO_TEST=TRUE	6
E114	NC_FMI2_DQS	NO_TEST=TRUE	6
E115	NC_FMI3_CE0_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE1_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE2_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE3_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE4_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE5_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE6_L	NO_TEST=TRUE	6
E115	NC_FMI3_CE7_L	NO_TEST=TRUE	6
E116	NC_FMI3_AD<0>	NO_TEST=TRUE	6
E116	NC_FMI3_AD<1>	NO_TEST=TRUE	6
E115	NC_FMI3_AD<2>	NO_TEST=TRUE	6
E116	NC_FMI3_AD<3>	NO_TEST=TRUE	6
E116	NC_FMI3_AD<4>	NO_TEST=TRUE	6
E116	NC_FMI3_AD<5>	NO_TEST=TRUE	6
E116	NC_FMI3_AD<6>	NO_TEST=TRUE	6
E116	NC_FMI3_AD<7>	NO_TEST=TRUE	6
E117	NC_FMI3_ALE	NO_TEST=TRUE	6
E116	NC_FMI3_CLE	NO_TEST=TRUE	6
E116	NC_FMI3_WE_L	NO_TEST=TRUE	6
E117	NC_FMI3_RE_L	NO_TEST=TRUE	6
E117	NC_FMI3_DQS	NO_TEST=TRUE	6
E117	NC_MIPI_VSYNC_H4	NO_TEST=TRUE	7
E117	NC_MIPI0C_AP_DATA_P<2>	NO_TEST=TRUE	7 43
E117	NC_MIPI0C_AP_DATA_N<2>	NO_TEST=TRUE	7 43
E117	NC_MIPI0C_AP_DATA_P<3>	NO_TEST=TRUE	7 43
E118	NC_MIPI0C_AP_DATA_N<3>	NO_TEST=TRUE	7 43
E118	NC_MIPI1C_AP_DATA_P<1>	NO_TEST=TRUE	7 43
E118	NC_MIPI1C_AP_DATA_N<1>	NO_TEST=TRUE	7 43
E118	NC_ISP_AP_1_FLASH	NO_TEST=TRUE	7
E118	NC_ISP_AP_1_PRE_FLASH	NO_TEST=TRUE	7

E180	NC_DDR0_CKE<1>	NO_TEST=TRUE	8
E181	NC_DDR1_CKE<1>	NO_TEST=TRUE	8
E180	NC_DDR2_CKE<1>	NO_TEST=TRUE	8
E182	NC_DDR3_CKE<1>	NO_TEST=TRUE	8
E180	NC_DDR0_CSN<1>	NO_TEST=TRUE	8
E183	NC_DDR1_CSN<1>	NO_TEST=TRUE	8
E183	NC_DDR2_CSN<1>	NO_TEST=TRUE	8
E200	NC_DDR3_CSN<1>	NO_TEST=TRUE	8
E205	NC_PMU_VBUCK0_SW0_G	NO_TEST=TRUE	36
E204	NC_PMU_VBUCK0_SW0_S	NO_TEST=TRUE	36
E226	NC_VBUS_A_OV_L	NO_TEST=TRUE	36
E207	NC_BOARD_TEMP7	NET_SPACING_TYPE=ANLG NO_TEST=TRUE	37
E208	NC_BOARD_TEMP8	NET_SPACING_TYPE=ANLG NO_TEST=TRUE	37
E210	NC_PMU_GPIO12	NO_TEST=TRUE	37
E212	NC_PMU_GPIO13	NO_TEST=TRUE	37
E213	NC_PMU_GPIO16	NO_TEST=TRUE	37
E213	NC_PMU_GPIO17	NO_TEST=TRUE	37
E216	NC_PMU_AMUX_A0	NO_TEST=TRUE	37
E218	NC_PMU_AMUX_A1	NO_TEST=TRUE	37
E217	NC_PMU_AMUX_A2	NO_TEST=TRUE	37
E220	NC_PMU_AMUX_A3	NO_TEST=TRUE	37
E210	NC_PMU_AMUX_AY	NO_TEST=TRUE	37
E223	NC_PMU_AMUX_B0	NO_TEST=TRUE	37
E222	NC_PMU_AMUX_B1	NO_TEST=TRUE	37
E223	NC_PMU_AMUX_B2	NO_TEST=TRUE	37
E222	NC_PMU_AMUX_B3	NO_TEST=TRUE	37
E225	NC_PMU_AMUX_BY	NO_TEST=TRUE	37

E220	NC_BON_L1	NO_TEST=TRUE	18
E220	NC_BON_L3	NO_TEST=TRUE	18
E220	NC_BON_L5	NO_TEST=TRUE	18
E240	NC_EAROUT_AP	NO_TEST=TRUE	19
E241	NC_EAROUT_AN	NO_TEST=TRUE	19
E231	NC_LINE_IN1_CODEC	NO_TEST=TRUE	19
E231	NC_LINE_IN1_REF_CODEC	NO_TEST=TRUE	19
E231	NC_LINE_IN2_CODEC	NO_TEST=TRUE	19
E231	NC_LINE_IN2_REF_CODEC	NO_TEST=TRUE	19
E231	NC_MIC1_BIAS_CODEC	NO_TEST=TRUE	19
E231	NC_MIC1P_CODEC	NO_TEST=TRUE	19
E231	NC_MIC1N_CODEC	NO_TEST=TRUE	19
E231	NC_MIC1_FILT_CODEC	NO_TEST=TRUE	19
E240	NC_D5703_6	NO_TEST=TRUE	
E241	NC_D5700_6	NO_TEST=TRUE	
E242	NC_D5701_6	NO_TEST=TRUE	
E243	NC_D5702_6	NO_TEST=TRUE	
E245	NC_LCM2_EN	NO_TEST=TRUE	37
E245	NC_VLCM1	NO_TEST=TRUE	37

SYNC_MASTER=MIKE SYNC_DATE=01/21/2011

PAGE TITLE

CONSTRAINTS: DEBUG

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 155 OF 157

SHEET 46 OF 48

SYNC MASTER=MIKE SYNC DATE=01/21/2011

PAGE TITLE

FUNC TEST POINTS

Apple Inc.

DRAWING NUMBER 051-8773 SIZE D

REVISION 10.0.0

BRANCH

PAGE 156 OF 157

SHEET 47 OF 48

SYNC MASTER=MIKE SYNC DATE=01/21/2011

PAGE TITLE

FUNC TEST POINTS

Apple Inc.

DRAWING NUMBER 051-8773

SIZE D

REVISION 10.0.0

BRANCH

PAGE 157 OF 157

SHEET 48 OF 48